JITR1/R2_DDR3

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM/PM+ICH9-M core logic

Friday, April 18, 2008

REV:1.0

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Compal Electronics, Inc.			
Title: Cover Sheet			
Size: Custom	Document Number: JITR1_LA-4141P		Rev: 1.0
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Compal confidential
File Name :

ZZZ2
14W_PCB_LA4142P

POWER Board | **CAP SENSE LEDs Board** | **CONTROL Board**

VRAM 16*16
VRAM 32*16
page20,21

nVIDIA NB9M
page16,19

PCI-E X16

Mobile Penryn
uFCPGA-478 CPU
page5,6,7

H_A#(3..35)
H_D#(0..63)
FSB
667/800/1066MHz

MODEM_CX20548
MDC board

Clock Gen.
SLG8SP556VTR
ICS9LPRS387AKLFT
page22

HDMI CONN
page23

CH7318
page23

PCI-E

Intel Cantiga GMCH
PCBGA 1329
page 8,9,10,11,12,13

DDR2 -667 (1.8V)
DDR2 -800 (1.8V)
Dual Channel

DDR2-SO-DIMM X2
BANK 0, 1, 2, 3
page 14,15

CRT & TV OUT
page25

LVDS I/F

LVDS Connector
page24

DMI

C-Line

Intel ICH9-M
mBGA-676
page26,27,28,29

AZALIA
12*USB2.0
4*SATA serial

AMP&Audio Jack
page24

Audio Codec
AMOM_CX20561
page30

PCI Express Mini card Slot 1
page32

PCI Express Mini card Slot 2
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6*PCI-E BUS

New Card
page40

3.3V / 33 MHz

PCI BUS

BCM5906
10/100/LAN
page33

1394+Card Reader
O2 OZ129T
page36

RJ45 CONN
page34

1394 Conn
page36

Card reader(XD/SD
MMC/MS/MS-Pro
HD SD)
page36

LPC BUS

EC
ENE KB926
page35

Int.KBD
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BIOS
page38

Touch Pad
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CMOS Camera
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BlueTooth Conn
page32

USB conn X3
page43

SATA HDD Connector
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SATA CDROM Connector
page39

SUB Board page32,36

*RJ45 CONN
*RJ11 CONN
*MIC IN JACK
*HP OUT JACK
*LED
*SWITCH
*1394 CONN
*DC JACK
*USB CONN
*SWITCH

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Title: **MB Block Diagram**

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DDR2 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	V	X	X	X	X	X	V	V	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

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Title: MB Notes List

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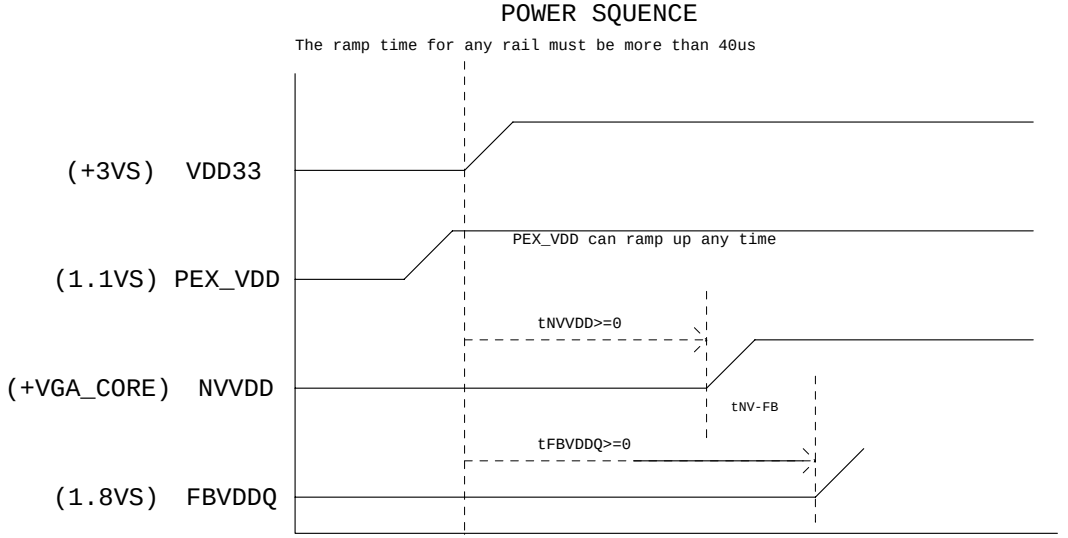
VGA and DDR2 Voltage Rails (NB9M-GS)

power plane / State			+1.8V	+3VS +VGA_CORE
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EDP at Tj = 97C*

Power Supply Rail	(V)	NB9M-GS GDDR3	NB9M-GS DDR2	NB9M-GE GDDR3	NB9M-GE DDR2
NVVDD	Variable	11.22A	10.87A	9.2A	8.88A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1550mA			
PEX_PLLVDD	1.1	165mA			
PLLVDD	1.1	55mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.425A			
FBVDD/Q	1.8	2.24A	1.65A	2.17A	1.63A
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	2.76A	2.17A	2.69A	2.15A
DACA_VDD	3.3	110mA			
DACB_VDD	3.3	125mA			
DACC_VDD	3.3	110mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	80mA			
TOTAL	3.3	0.445A			

POWER SQUENCE



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Title: VGA Notes List			
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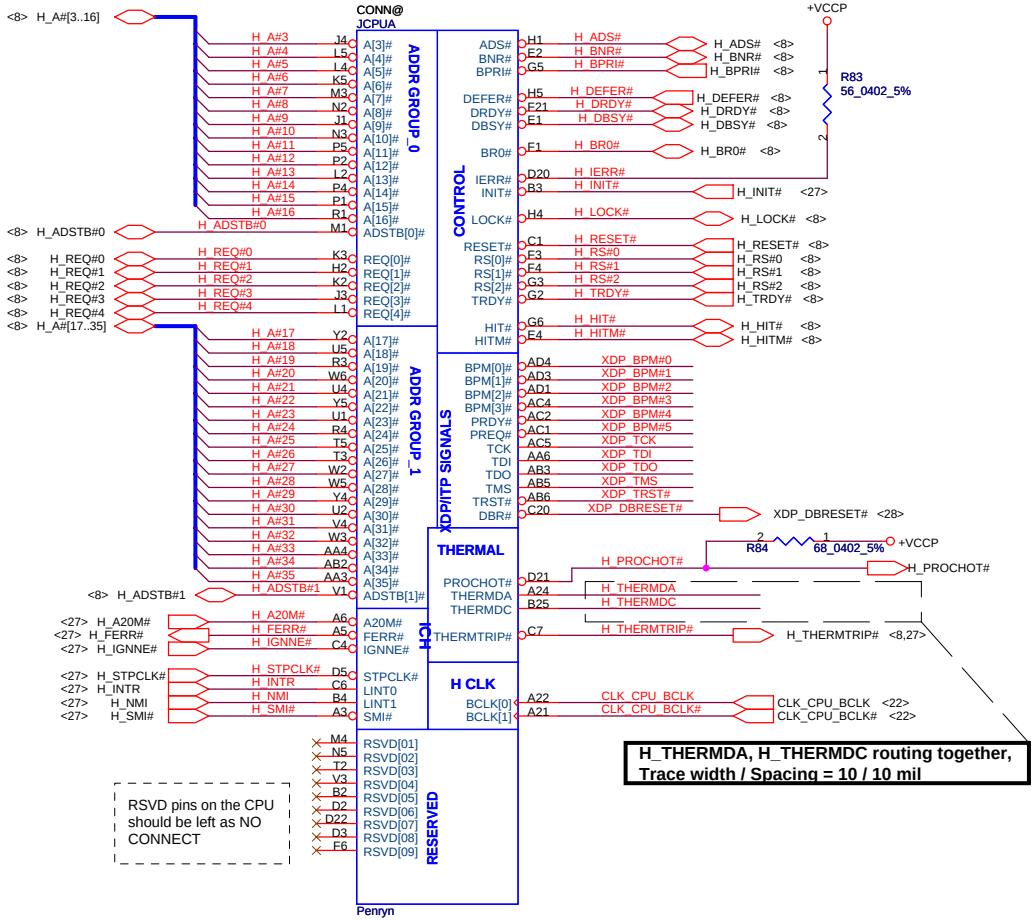

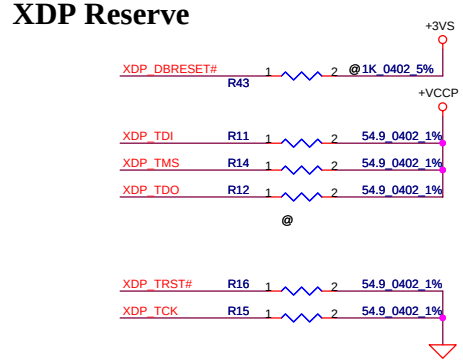

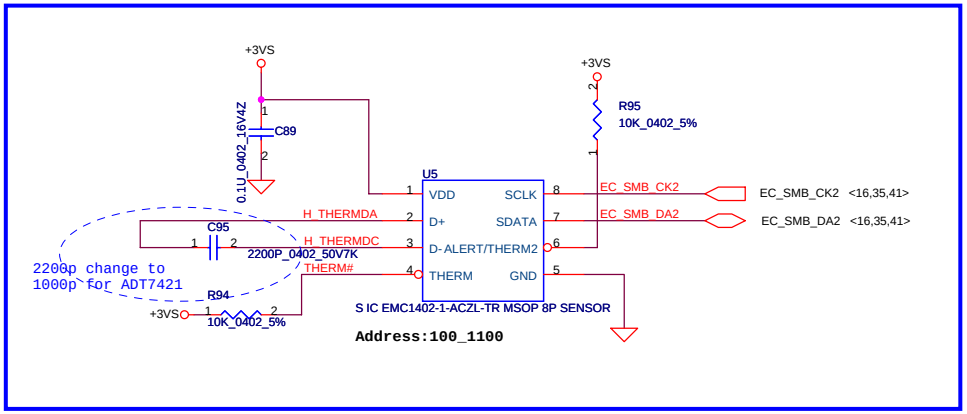

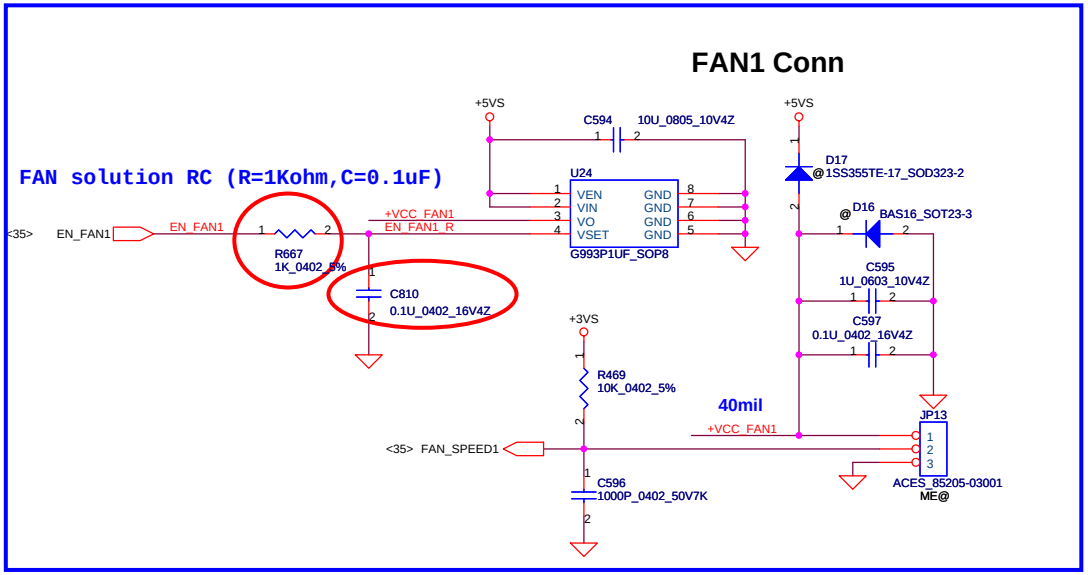

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Title: Penryn (1/3)			
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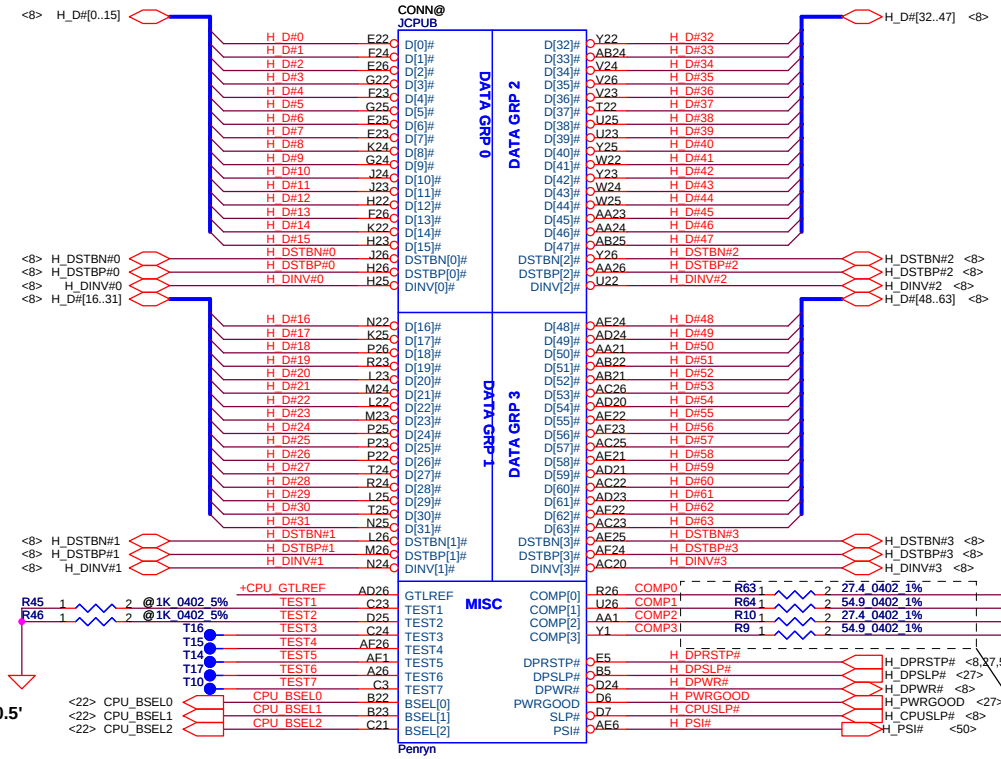
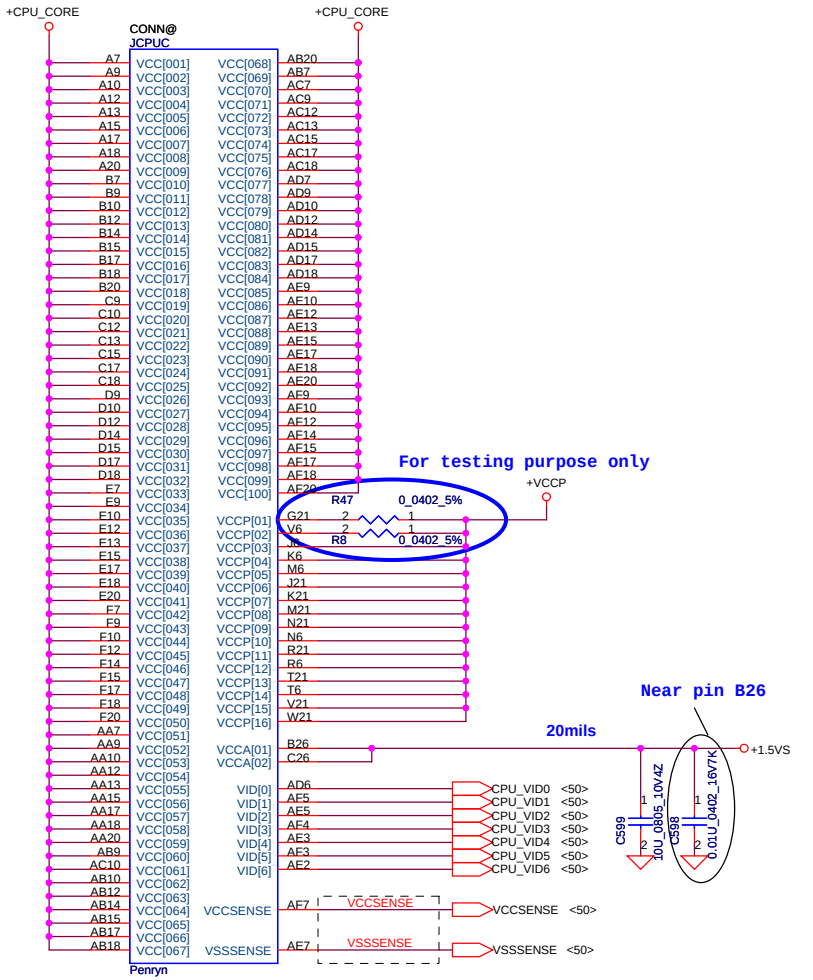
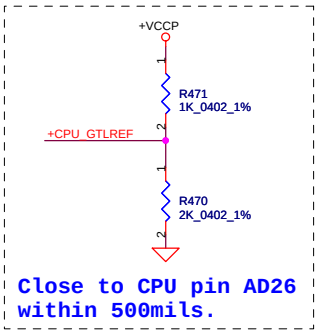




layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

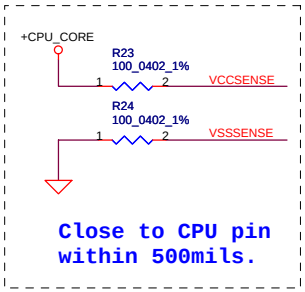


Layout note: Z0=55 ohm
0.5" max for GTLREF.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Length match within 25 mils.
The trace width/space/other is 16/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



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Compal Electronics, Inc.

Title: Penryn (2/3)

Size	Document Number	Rev
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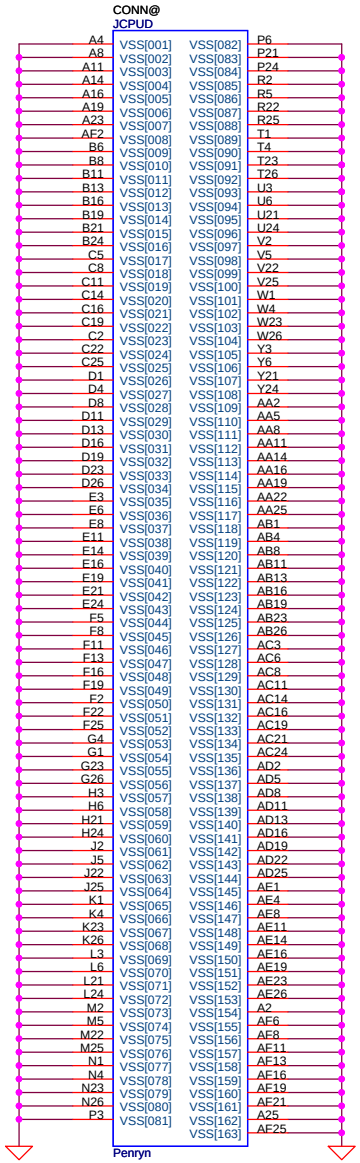
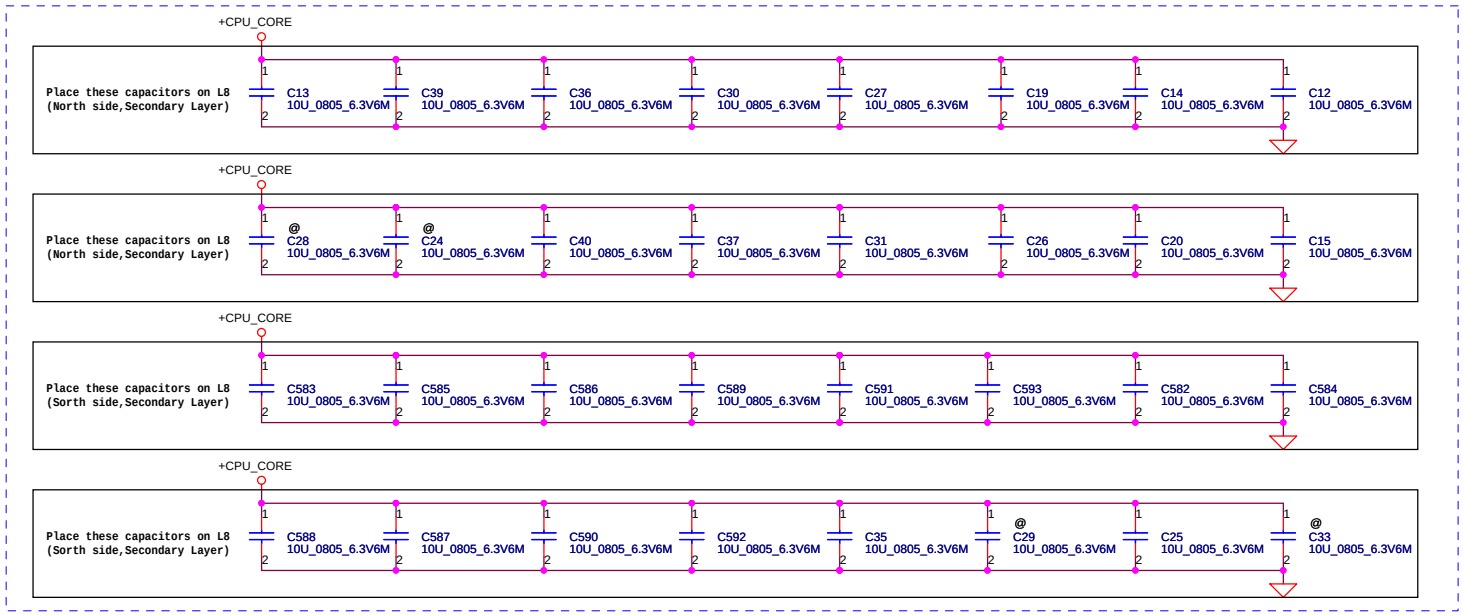
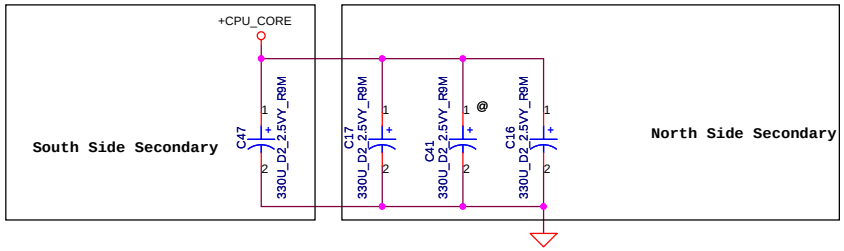


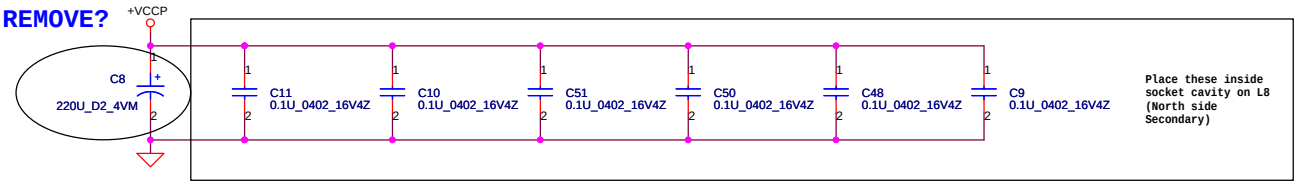


Mid Frequence Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF

REMOVE?



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Title: **Penryn (3/3)**

Size	Document Number	Rev
B	JITR1_LA-4141P	0.1

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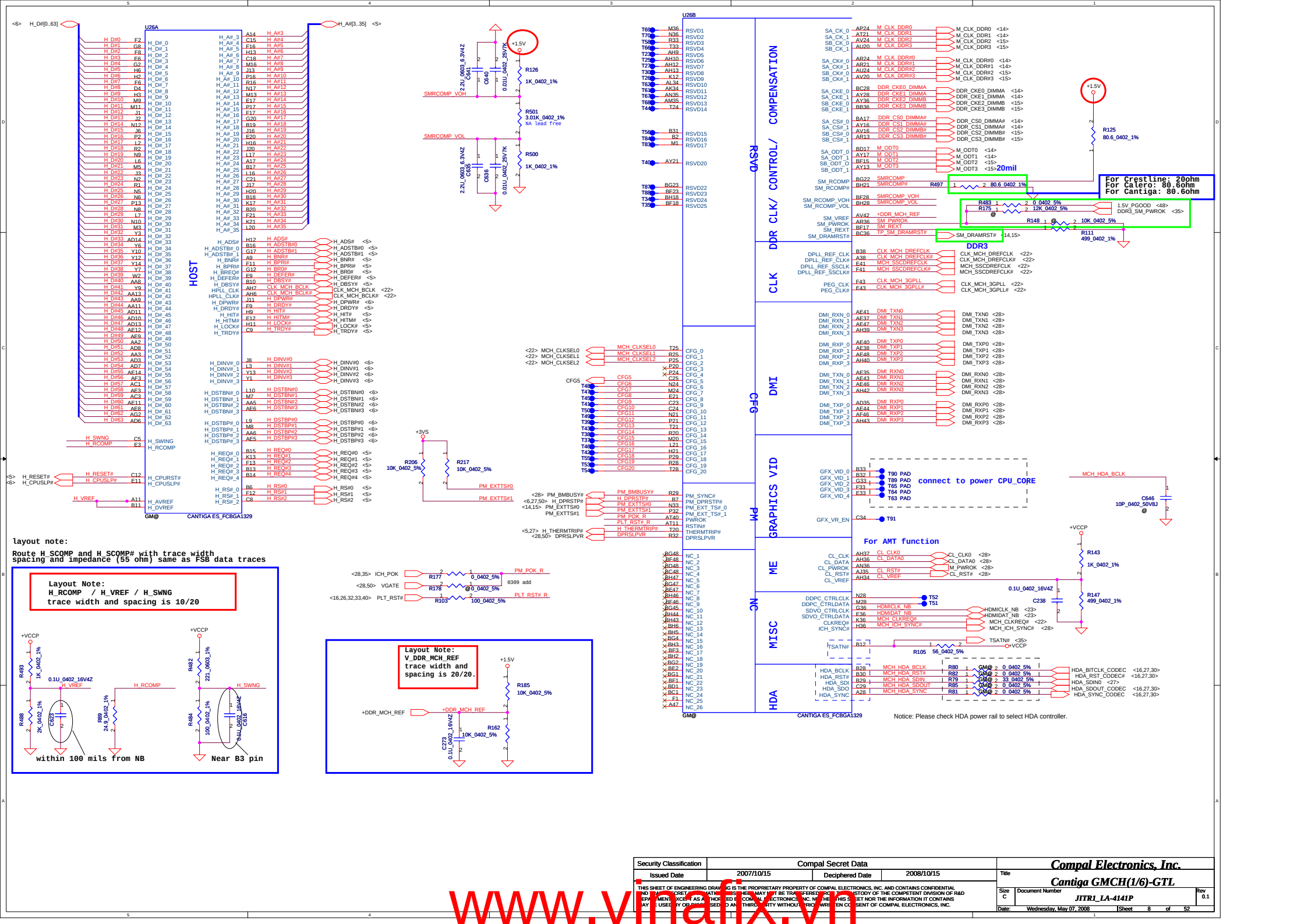

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Title: Cantiga GMCH(1/6)-GTL

Size	Document Number	Rev
C	JITR1_LA-4141P	0.1

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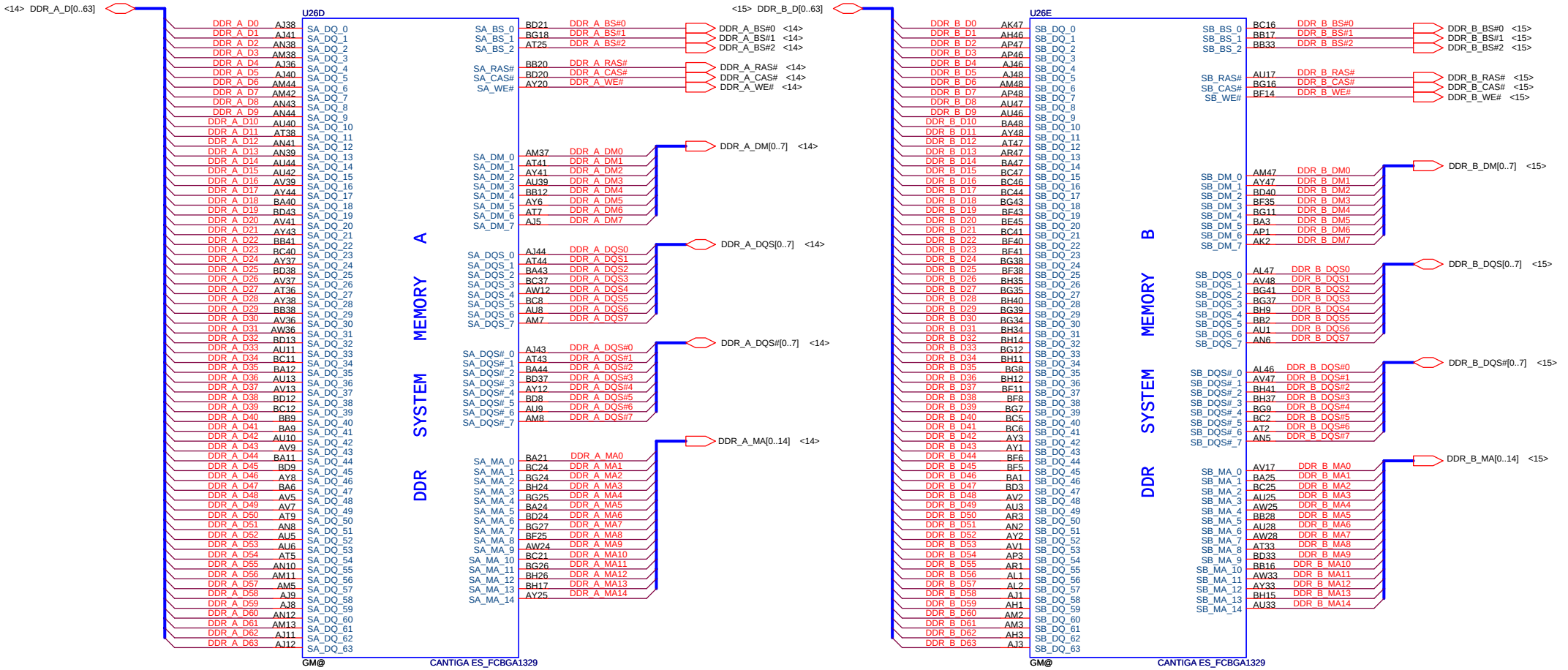

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Title: Cantiga GMCH (2/6)-DDRII

Size	Document Number	Rev
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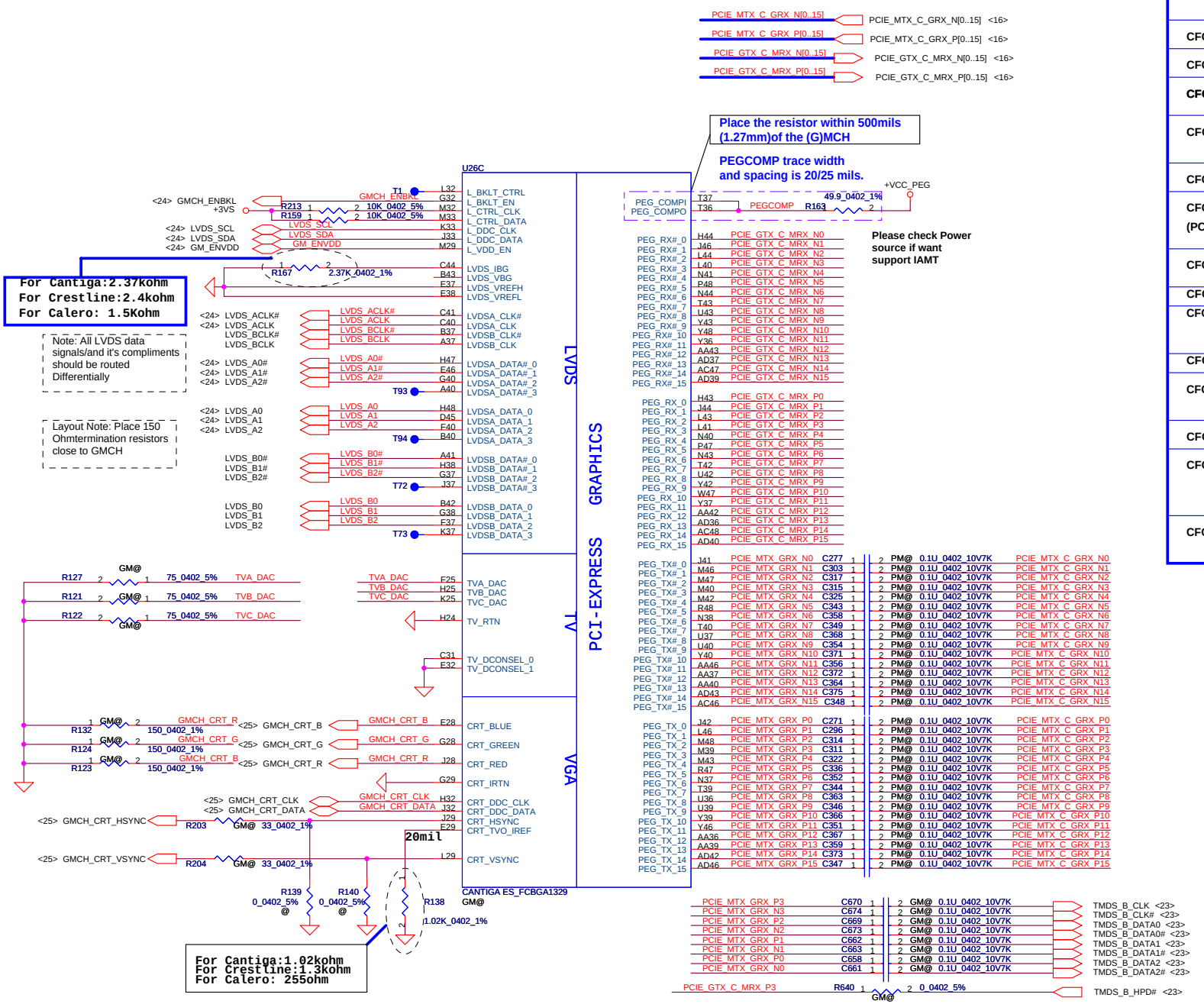
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.



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Compal Electronics, Inc.			
Title: Cantiga GMCH (3/6)-VGA/LVDS/TV			
Size: Custom	Document Number: JITR1_LA-4141P		Rev: 0.1
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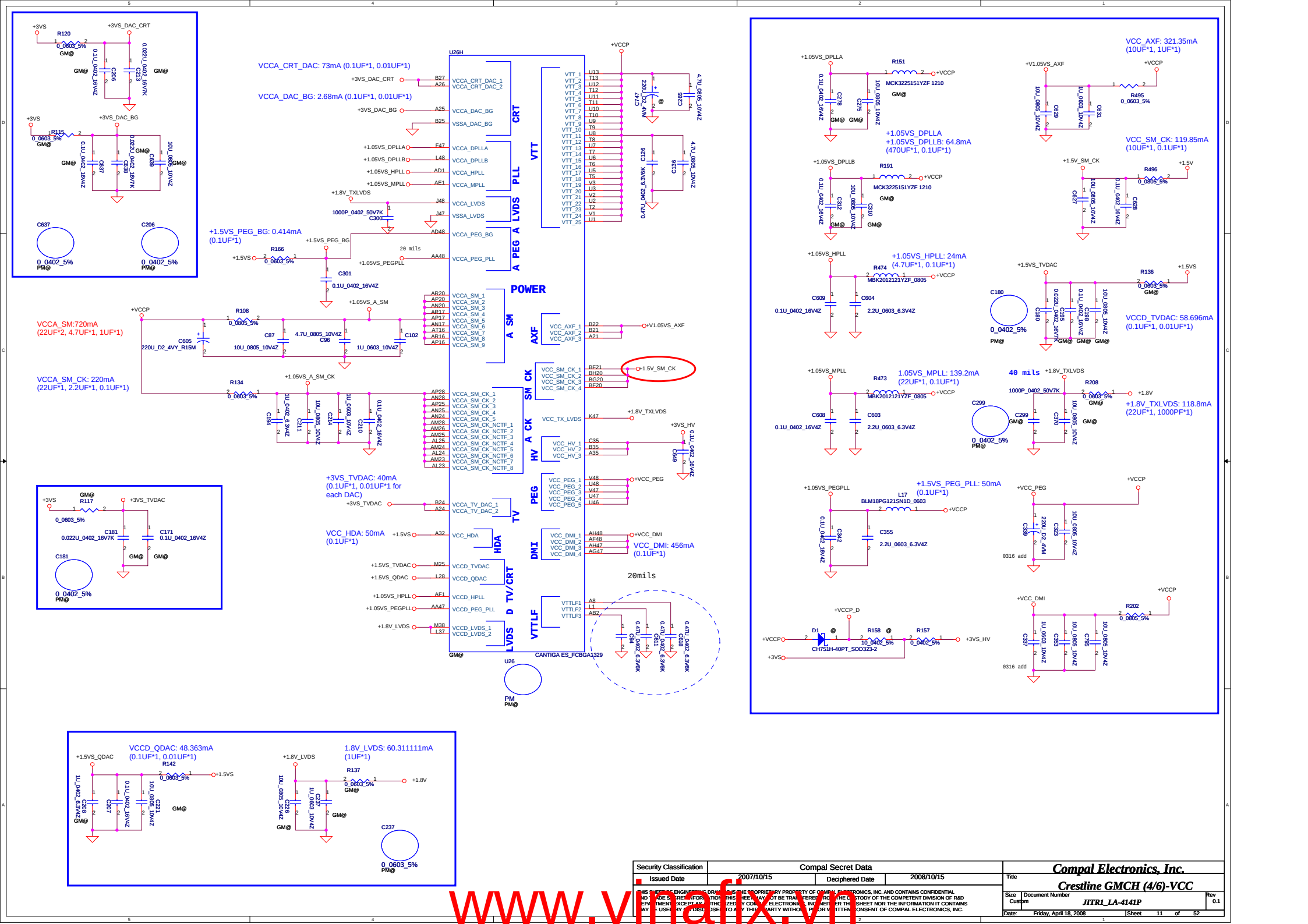

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Compal Electronics, Inc.			
Title: Crestline GMCH (4/6)-VCC			
Size: Custom	Document Number: JITR1_LA-4141P		Rev: 0.1
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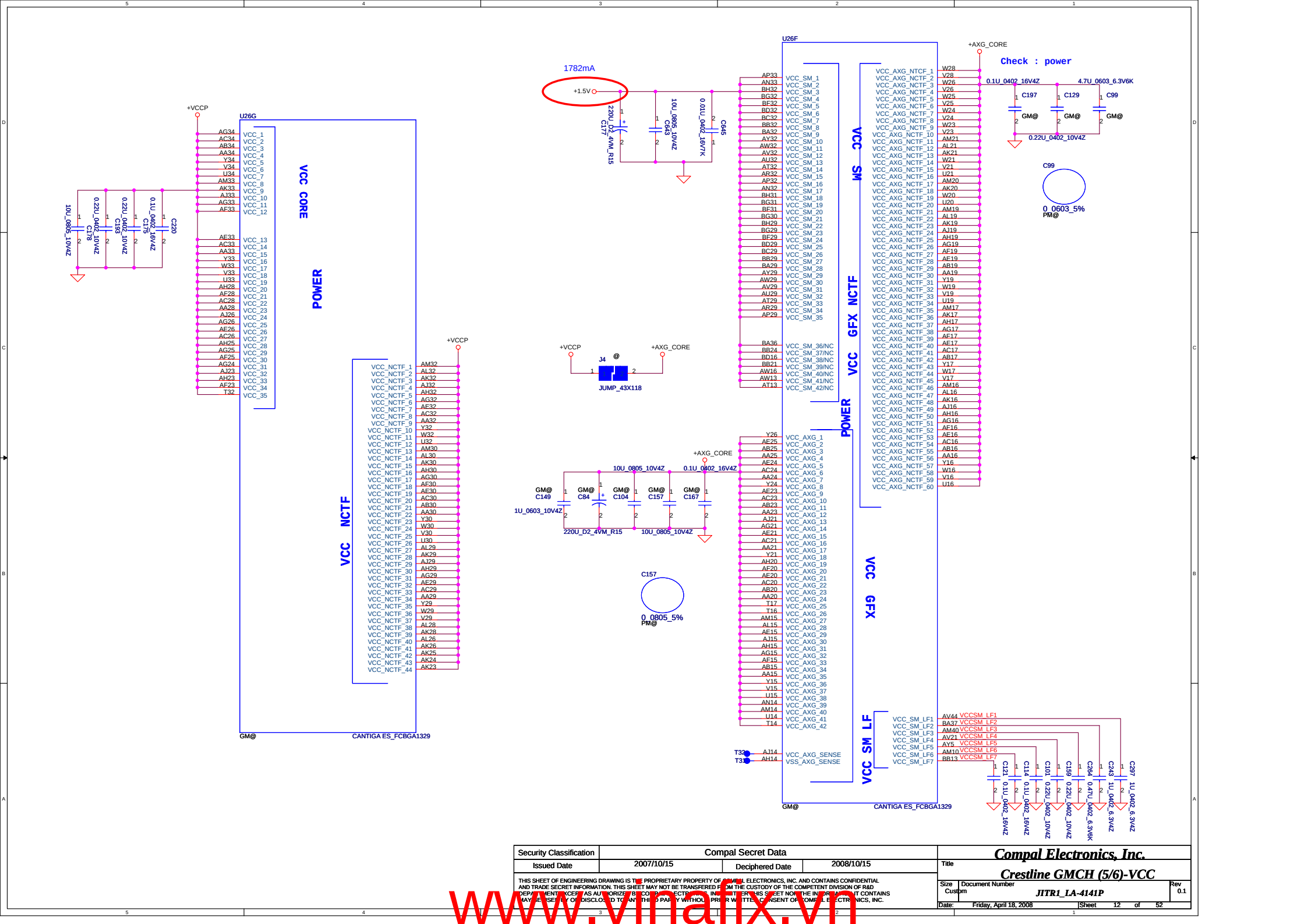

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Title: **Crestline GMCH (5/6)-VCC**

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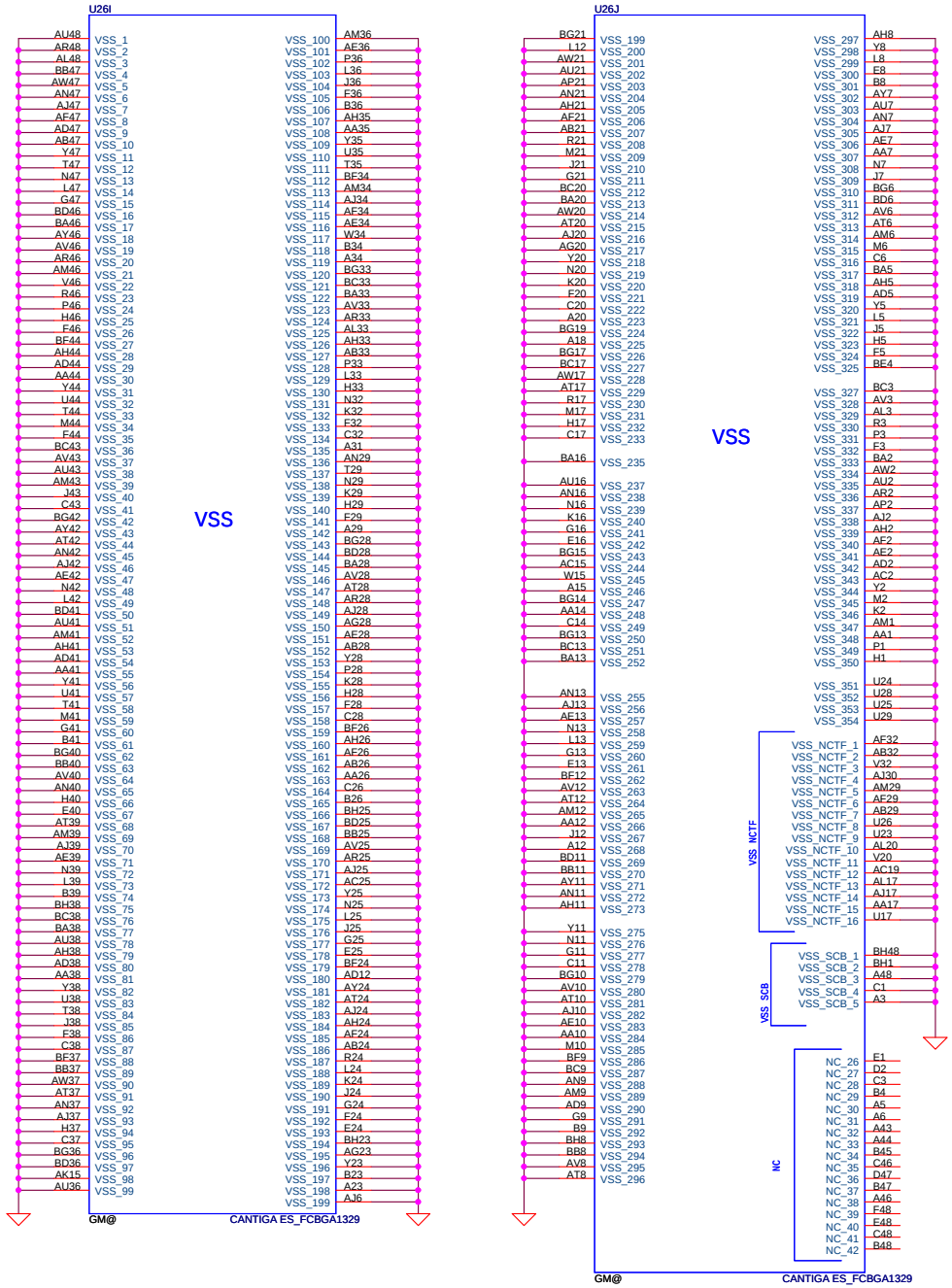

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Compal Electronics, Inc.	
Title	Cantiga GMCH (6/6)-GND
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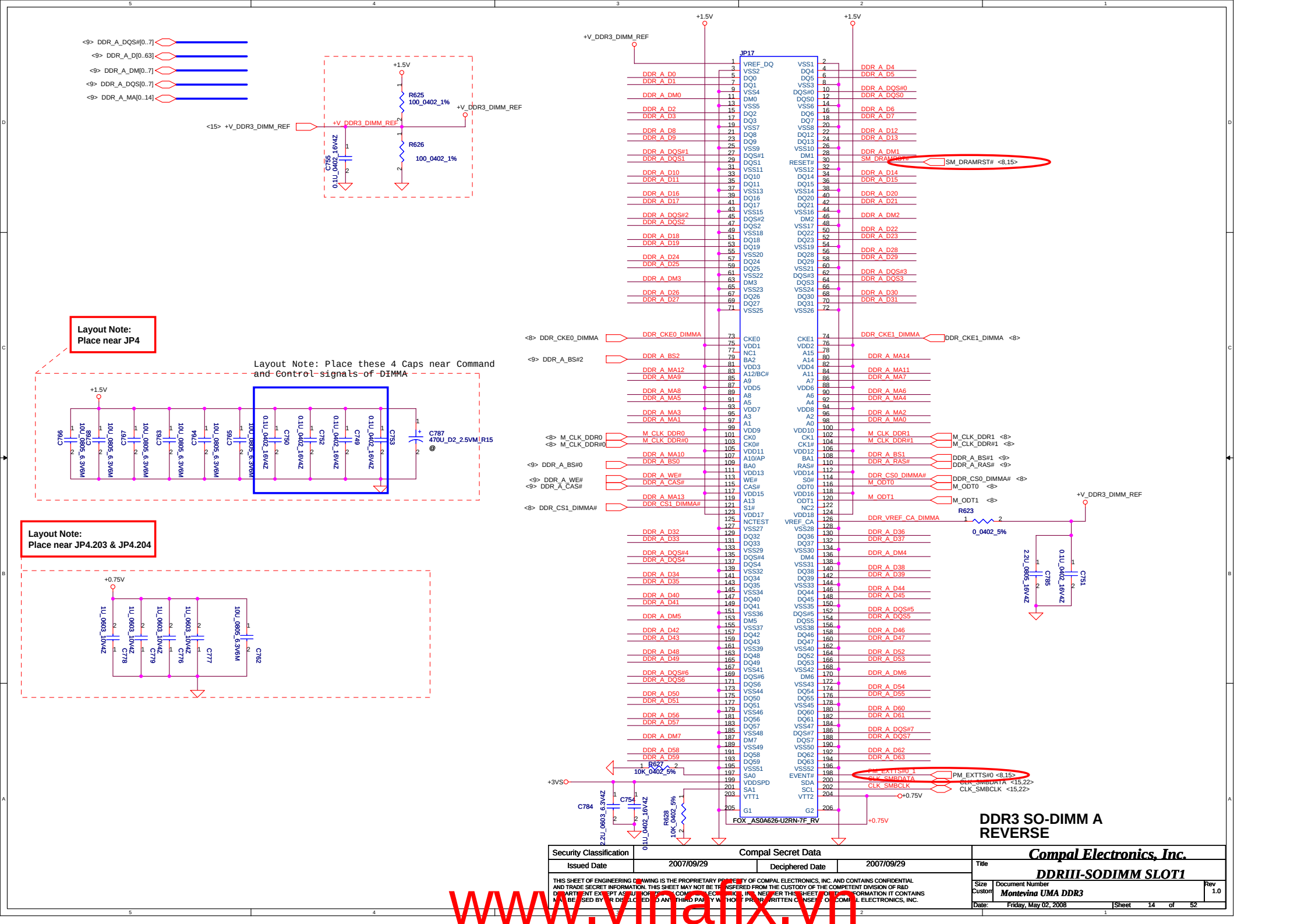

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Title: DDRIII-SODIMM SLOT1

Size	Document Number	Rev
Custom	Montevina UMA DDR3	1.0

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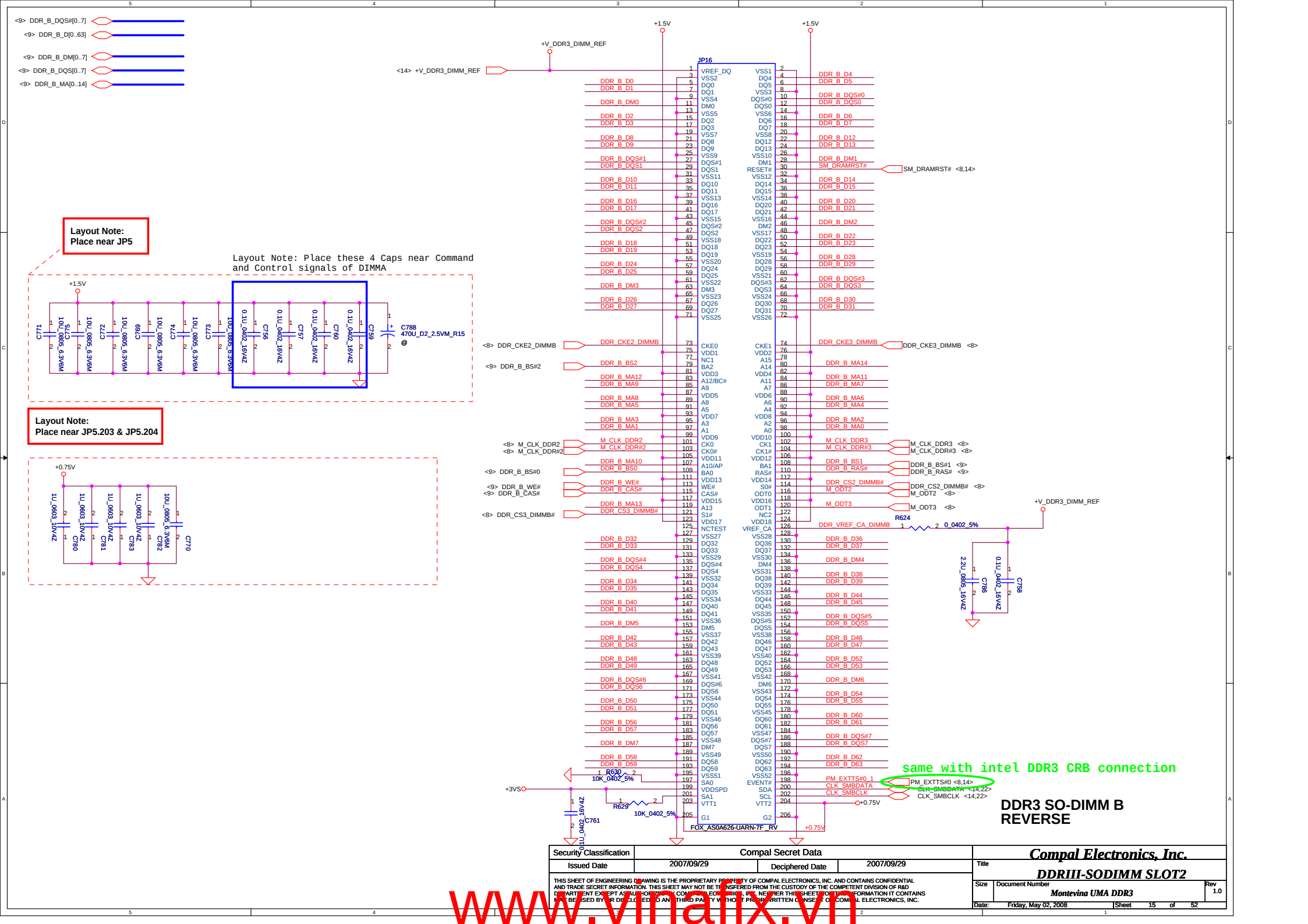
Layout Note:
Place near JP5
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA
Layout Note:
Place near JP5.203 & JP5.204
JP16
FOX_AS0A626-UARN-7F_RV
same with intel DDR3 CRB connection
DDR3 SO-DIMM B
REVERSE
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DDRIII-SODIMM SLOT2
Montevina UMA DDR3
Compal Secret Data
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U27A

Part 1 of 5

PCI EXPRESS

PEX_RX0 PEX_RX0_N PEX_RX1 PEX_RX1_N PEX_RX2 PEX_RX2_N PEX_RX3 PEX_RX3_N PEX_RX4 PEX_RX4_N PEX_RX5 PEX_RX5_N PEX_RX6 PEX_RX6_N PEX_RX7 PEX_RX7_N PEX_RX8 PEX_RX8_N PEX_RX9 PEX_RX9_N PEX_RX10 PEX_RX10_N PEX_RX11 PEX_RX11_N PEX_RX12 PEX_RX12_N PEX_RX13 PEX_RX13_N PEX_RX14 PEX_RX14_N PEX_RX15 PEX_RX15_N

PEX_TX0 PEX_TX0_N PEX_TX1 PEX_TX1_N PEX_TX2 PEX_TX2_N PEX_TX3 PEX_TX3_N PEX_TX4 PEX_TX4_N PEX_TX5 PEX_TX5_N PEX_TX6 PEX_TX6_N PEX_TX7 PEX_TX7_N PEX_TX8 PEX_TX8_N PEX_TX9 PEX_TX9_N PEX_TX10 PEX_TX10_N PEX_TX11 PEX_TX11_N PEX_TX12 PEX_TX12_N PEX_TX13 PEX_TX13_N PEX_TX14 PEX_TX14_N PEX_TX15 PEX_TX15_N

PEX_REFCLK PEX_REFCLK_N

PEX_TSTCLK_OUT PEX_TSTCLK_OUT_N

PEX_TERMP

PEX_RST_N

GPIO

GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13 GPIO14 GPIO15 GPIO16 GPIO17 GPIO18 GPIO19

DACA

DACA_HSYNC DACA_VSYNC DACA_RED DACA_BLUE DACA_GREEN DACA_VREF DACA_RSET

DACB

DACB_CSYNC DACB_RED DACB_BLUE DACB_GREEN DACB_VREF DACB_RSET

DACC

DACC_HSYNC DACC_VSYNC DACC_RED DACC_BLUE DACC_GREEN DACC_VREF DACC_RSET

I2C

I2CA_SCL I2CA_SDA I2CB_SCL I2CB_SDA I2CC_SCL I2CC_SDA I2CD_SCL I2CD_SDA I2CE_SCL I2CE_SDA I2CH_SCL I2CH_SDA I2CS_SCL I2CS_SDA

TEST

JTAG_TCK JTAG_TDI JTAG_TDO JTAG_TMS JTAG_TRST_N TESTMODE

CLK

XTAL_SSIN XTAL_OUTBUFF XTAL_OUT XTAL_IN

HDA

SPDIF VDD_SENSE HDA_RST_N HDA_SDI HDA_SDO HDA_SYNC HDA_BCLK

NB9M-GS_BGA533

PM@

<10> PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]

<10> PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]

<10> PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]

<10> PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

PCIE_MTX_C_GRX_P0 AE12
PCIE_MTX_C_GRX_N0 AE12
PCIE_MTX_C_GRX_P1 AG12
PCIE_MTX_C_GRX_N1 AG13
PCIE_MTX_C_GRX_P2 AF13
PCIE_MTX_C_GRX_N2 AE13
PCIE_MTX_C_GRX_P3 AE15
PCIE_MTX_C_GRX_N3 AF15
PCIE_MTX_C_GRX_P4 AG15
PCIE_MTX_C_GRX_N4 AG16
PCIE_MTX_C_GRX_P5 AE16
PCIE_MTX_C_GRX_N5 AE16
PCIE_MTX_C_GRX_P6 AE18
PCIE_MTX_C_GRX_N6 AF18
PCIE_MTX_C_GRX_P7 AG18
PCIE_MTX_C_GRX_N7 AG19
PCIE_MTX_C_GRX_P8 AF19
PCIE_MTX_C_GRX_N8 AE19
PCIE_MTX_C_GRX_P9 AE21
PCIE_MTX_C_GRX_N9 AF21
PCIE_MTX_C_GRX_P10 AG21
PCIE_MTX_C_GRX_N10 AG22
PCIE_MTX_C_GRX_P11 AF22
PCIE_MTX_C_GRX_N11 AE22
PCIE_MTX_C_GRX_P12 AE24
PCIE_MTX_C_GRX_N12 AF24
PCIE_MTX_C_GRX_P13 AG24
PCIE_MTX_C_GRX_N13 AF25
PCIE_MTX_C_GRX_P14 AG25
PCIE_MTX_C_GRX_N14 AG26
PCIE_MTX_C_GRX_P15 AF27
PCIE_MTX_C_GRX_N15 AE27

PCIE_GTX_C_MRX_P0 C261 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P0 AD10
PCIE_GTX_C_MRX_N0 C260 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N0 AD11
PCIE_GTX_C_MRX_P1 C294 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P1 AD12
PCIE_GTX_C_MRX_N1 C293 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N1 AC12
PCIE_GTX_C_MRX_P2 C259 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P2 AB11
PCIE_GTX_C_MRX_N2 C258 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N2 AB12
PCIE_GTX_C_MRX_P3 C292 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P3 AD13
PCIE_GTX_C_MRX_N3 C291 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N3 AD14
PCIE_GTX_C_MRX_P4 C257 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P4 AD15
PCIE_GTX_C_MRX_N4 C256 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N4 AC15
PCIE_GTX_C_MRX_P5 C290 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P5 AB14
PCIE_GTX_C_MRX_N5 C289 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N5 AB15
PCIE_GTX_C_MRX_P6 C255 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P6 AC16
PCIE_GTX_C_MRX_N6 C254 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N6 AD16
PCIE_GTX_C_MRX_P7 C287 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P7 AD17
PCIE_GTX_C_MRX_N7 C288 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N7 AD18
PCIE_GTX_C_MRX_P8 C253 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P8 AC18
PCIE_GTX_C_MRX_N8 C252 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N8 AB18
PCIE_GTX_C_MRX_P9 C285 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P9 AB19
PCIE_GTX_C_MRX_N9 C286 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N9 AB20
PCIE_GTX_C_MRX_P10 C251 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P10 AD19
PCIE_GTX_C_MRX_N10 C250 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N10 AD20
PCIE_GTX_C_MRX_P11 C284 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P11 AD21
PCIE_GTX_C_MRX_N11 C283 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N11 AC21
PCIE_GTX_C_MRX_P12 C249 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P12 AB21
PCIE_GTX_C_MRX_N12 C248 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N12 AB22
PCIE_GTX_C_MRX_P13 C282 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P13 AC22
PCIE_GTX_C_MRX_N13 C281 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N13 AD22
PCIE_GTX_C_MRX_P14 C267 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P14 AD23
PCIE_GTX_C_MRX_N14 C266 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N14 AD24
PCIE_GTX_C_MRX_P15 C280 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_P15 AE25
PCIE_GTX_C_MRX_N15 C279 PM@ 0.1U_0402_10V7K PCIE_GTX_MRX_N15 AE26

<22> CLK_PCIE_VGA CLK_PCIE_VGA AB10
<22> CLK_PCIE_VGA# CLK_PCIE_VGA# AC10

R183 200_0402_5% PM@
R504 2.4K_0402_1% PM@
<8,26,32,33,40> PLT_RST# PLT_RST#
@R173 10K_0402_5%

OSC_SPREAD D11
OSC_OUT E9
@ R48 22_0402_5%
R99 10K_0402_5% PM@
R100 10K_0402_5% PM@
If External Spread Spectrum not stuff than stuff resistor

XTALOUT E10
XTALIN D10

Y3
OUT GND GND IN
27MHZ_16PF_X7S027000BG1H-U
PM@
C612 18P_0402_50V8J PM@
C614 18P_0402_50V8J PM@

GPIO0 N1
GPIO1 G1 NV_INVTPWM HDMI_DETECT_VGA <23>
GPIO2 C1 PAD T86
GPIO3 M2 VGA_ENVDD VGA_ENVDD <24>
GPIO4 M3 VGA_ENBKL VGA_ENBKL <24>
GPIO5 K3
GPIO6 K2
GPIO7 J2
GPIO8 C2
GPIO9 M1
GPIO10 D2
GPIO11 D1
GPIO12 J3
GPIO13 J1
GPIO14 K1
GPIO15 F3
GPIO16 G3
GPIO17 G2 PAD T29
GPIO18 F1
GPIO19 F2

DACA_HSYNC AD2 VGA_HSYNC VGA_HSYNC <25>
DACA_VSYNC AD1 VGA_VSYNC VGA_VSYNC <25>
DACA_RED AE2 VGA_CRT_R VGA_CRT_R <25>
DACA_BLUE AD3 VGA_CRT_B VGA_CRT_B <25>
DACA_GREEN AE3 VGA_CRT_G VGA_CRT_G <25>
DACA_VREF AF1 DACA_VREF C648 2 1 PM@ 0.1U_0402_16V4Z
DACA_RSET AE1 DACA_RSET R503 PM@ 124_0402_1%

CRT OUT

DACB_CSYNC D6
DACB_RED F7
DACB_BLUE E6
DACB_GREEN E7
DACB_VREF G6
DACB_RSET F8

DACC_HSYNC U6
DACC_VSYNC U4
DACC_RED T5
DACC_BLUE R4
DACC_GREEN T4
DACC_VREF R6
DACC_RSET V6

I2CA_SCL R1 VGA_DDCCLK VGA_DDCCLK <25>
I2CA_SDA T3 VGA_DDCDATA VGA_DDCDATA <25>
I2CB_SCL R2 R116 2.2K_0402_5% PM@
I2CB_SDA R3 R119 2.2K_0402_5% PM@
I2CC_SCL A2 VGA_LVDS_SCL VGA_LVDS_SCL <24>
I2CC_SDA B1 VGA_LVDS_SDA VGA_LVDS_SDA <24>
I2CD_SCL N2 R196 2.2K_0402_5% PM@
I2CD_SDA N3 R193 2.2K_0402_5% PM@
I2CE_SCL Y6 VGA_HDMI_SCL VGA_HDMI_SCL <23>
I2CE_SDA W6 VGA_HDMI_SDA VGA_HDMI_SDA <23>
I2CH_SCL A3 HDCP_SMB_CK1
I2CH_SDA A4 HDCP_SMB_DAI
I2CS_SCL T1 EC_SMB_CK2 EC_SMB_CK2 <5,35,41>
I2CS_SDA T2 EC_SMB_DA2 EC_SMB_DA2 <5,35,41>

+3VS

JTAG_TCK AE3 JTAG_TCK PAD T60
JTAG_TDI AG4
JTAG_TDO AF4 JTAG_TDO PAD T59
JTAG_TMS AE4
JTAG_TRST_N AG3 JTAG_TRST_N PAD T92
TESTMODE AD25 TESTMODE R616 1 2 PM@ 10K_0402_5%

SPDIF F9 SPDIF_IN PAD T28
VDD_SENSE W15 +VGASENSE +VGASENSE

HDA_RST_N C6 HDA_RST_CODEC# PM@ HDA_RST_CODEC# <8,27,30>
HDA_SDI A6 HDA_SDIN1_R R86 1 2 33_0402_5% HDA_SDIN1 <27>
HDA_SDO B6 HDA_SDOUT_CODEC HDA_SDOUT_CODEC <8,27,30>
HDA_SYNC B7 HDA_SYNC_CODEC HDA_SYNC_CODEC <8,27,30>
HDA_BCLK A7 HDA_BITCLK_CODEC HDA_BITCLK_CODEC <8,27,30>

C86 10P_0402_50V8J

VGA_CRT_R R164 1 PM@ 2 150_0402_1%
VGA_CRT_G R168 1 PM@ 2 150_0402_1%
VGA_CRT_B R180 1 PM@ 2 150_0402_1%

+3VS
R75 2.2K_0402_5% PM@
R69 2.2K_0402_5% PM@
R65 10K_0402_5% @
PM@ C79 0.1U_0402_16V4Z
U4
VCC WP SCL SDA A0 A1 A2 GND
AT24C16AN-10SU-2.7_SO8
PM@
HDCP_SMB_CK1
HDCP_SMB_DAI
R71 2.2K_0402_5% @
R70 100K_0402_1% PM@

External Spread Spectrum

U3
REFOUT XOUT XIN/CLKIN VSS MODOUT VDD
ASM3P2872AF-06OR_TSOT-23-6
OSC_OUT
@ R55 OSC_SPREAD 22_0402_5%
+3VS
C66 0.1U_0402_16V4Z @

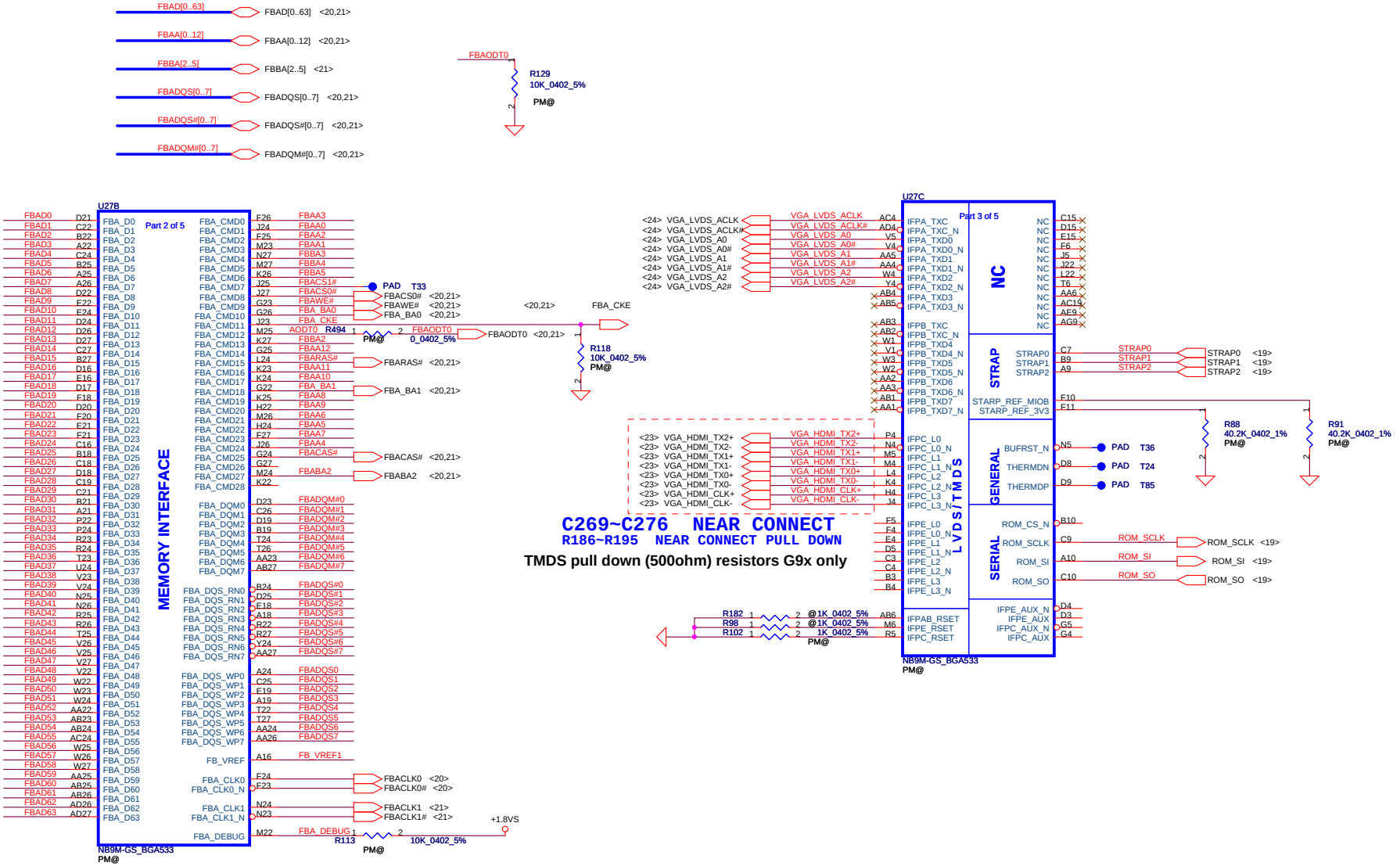
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: NB9M-GS PCIE,LVDS,GPIO,CLK

Size	Document Number	Rev
B	JITR1_LA-4141P	0.1

Date: Wednesday, May 07, 2008 Sheet 16 of 52



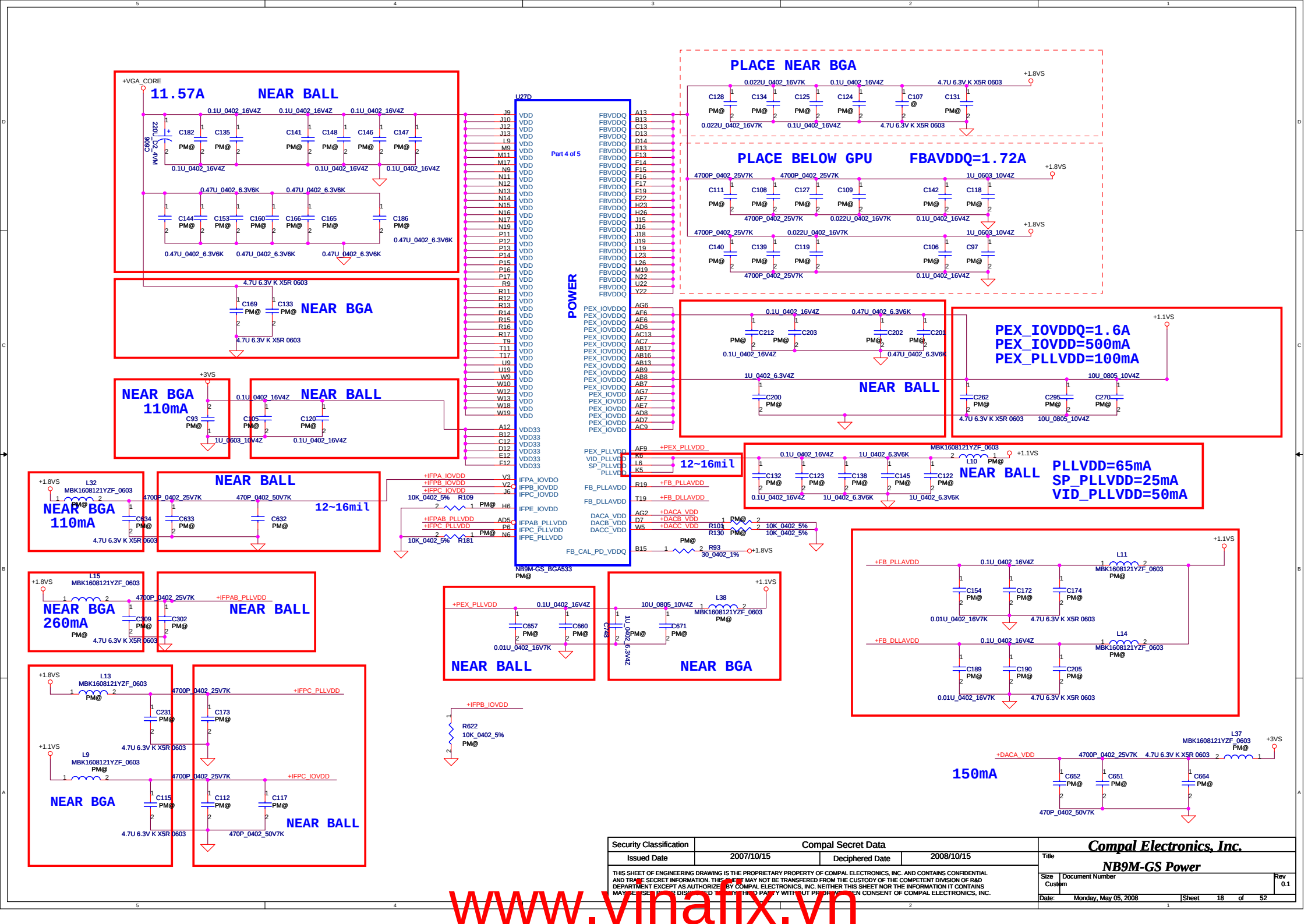
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: NB9M-GS Memory

Size	Document Number	Rev
B	JITR1_LA-4141P	0.1

Date: Friday, May 02, 2008 Sheet 17 of 52



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

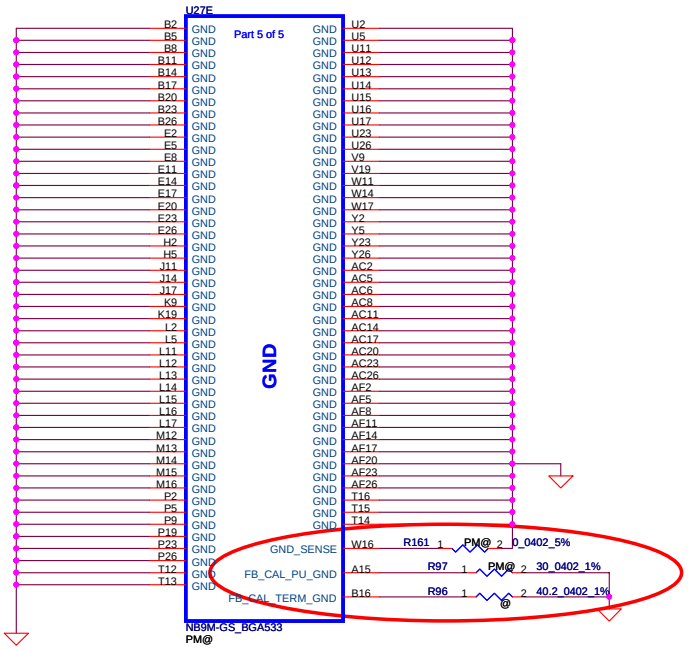
Compal Electronics, Inc.

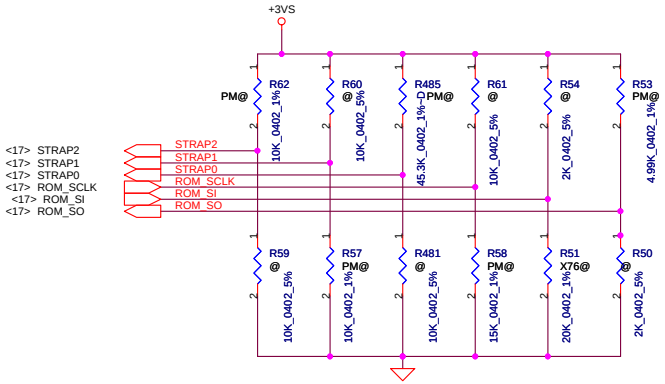
Title: NB9M-GS Power

Size	Document Number	Rev
Custom		0.1

Date: Monday, May 05, 2008 | Sheet 18 of 52

A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available





GB1 Family GPU Strap Qptions

X76

GPU	FB Memory		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
		32Mx16(5)	PU 5K	PD 15K	PD 30K	PU 10K	PD 10K	PU 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
		32Mx16(7)	PU 5K	PD 15K	PD 45K	PU 10K	PD 10K	PU 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K
		32Mx16(6)	PU 5K	PD 15K	PD 35K	PU 10K	PD 10K	PU 45K

Component	Manufacturer	Compal PN	Compal X76 PN
DDR2 VRAM (32M*16)	Hynix	SA000012G30	X7611338L04
	Qimonda	SA00001YF10	X7611338L05
	Samsung	SA00001KH10	X7611338L06

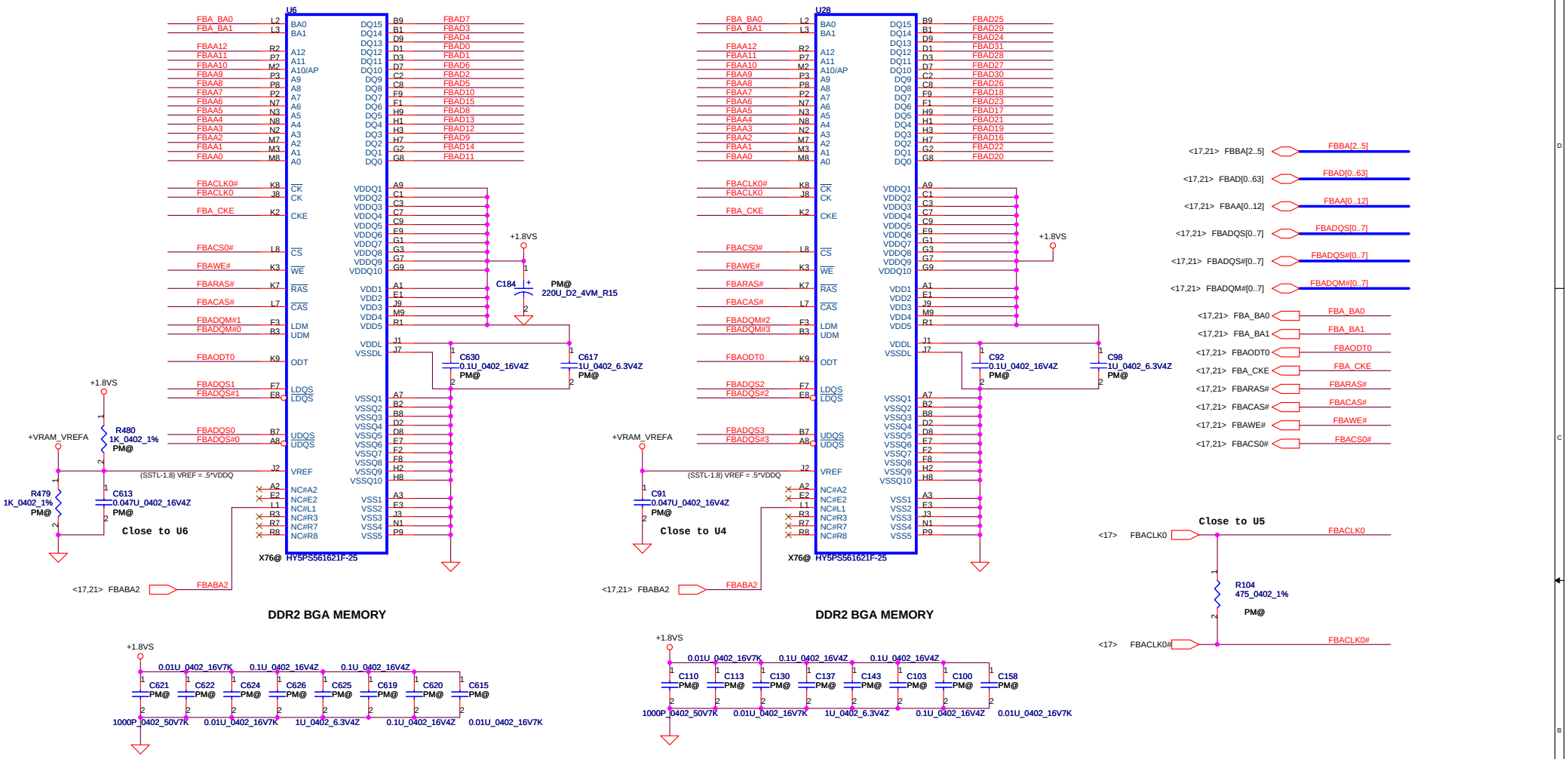
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: NB9M-GE GND & STRAP

Size	Document Number	Rev
B	JITR1_LA-4141P	0.1

Date: Friday, May 02, 2008 Sheet 19 of 52



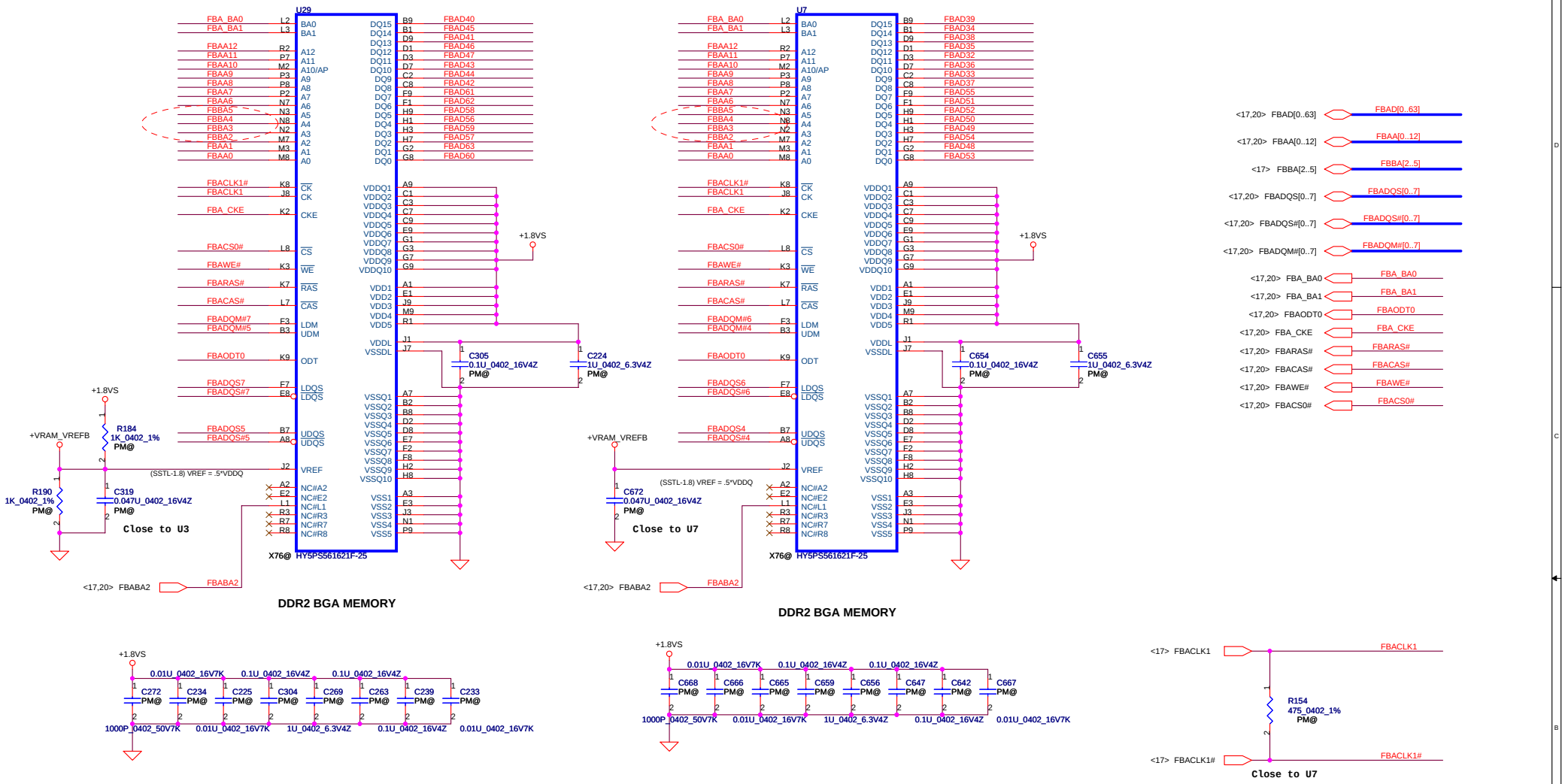
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: VRAM DDRA

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

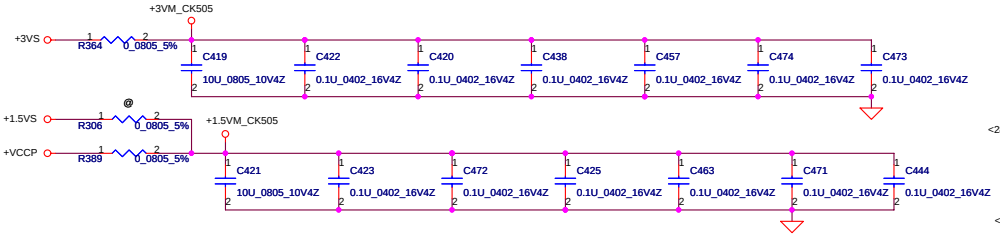
Date: Friday, May 02, 2008 Sheet 20 of 52

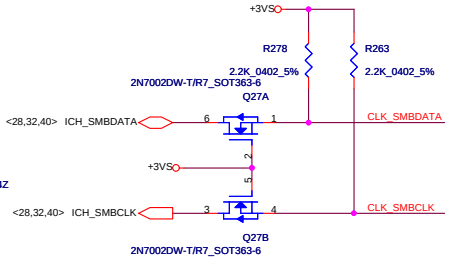


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: VRAM DDRB			
Size: Custom	Document Number: JITR1_LA-4141P		Rev: 0.1
Date: Friday, May 02, 2008	Sheet 21 of 52		

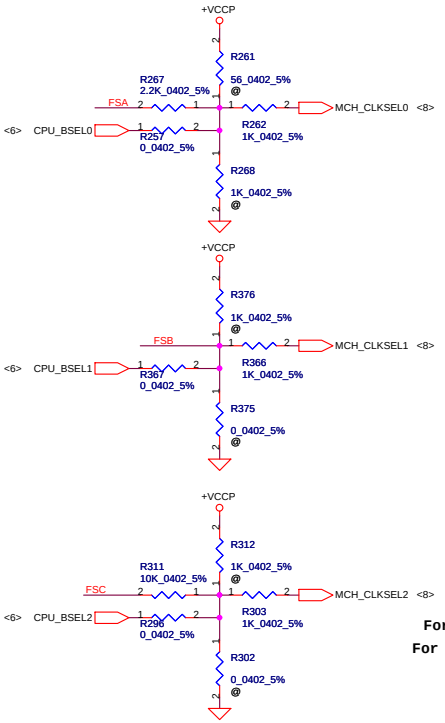
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

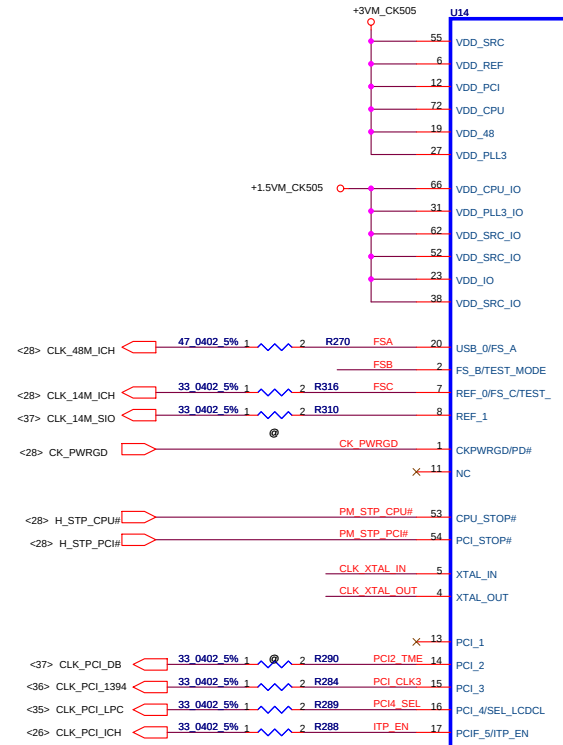


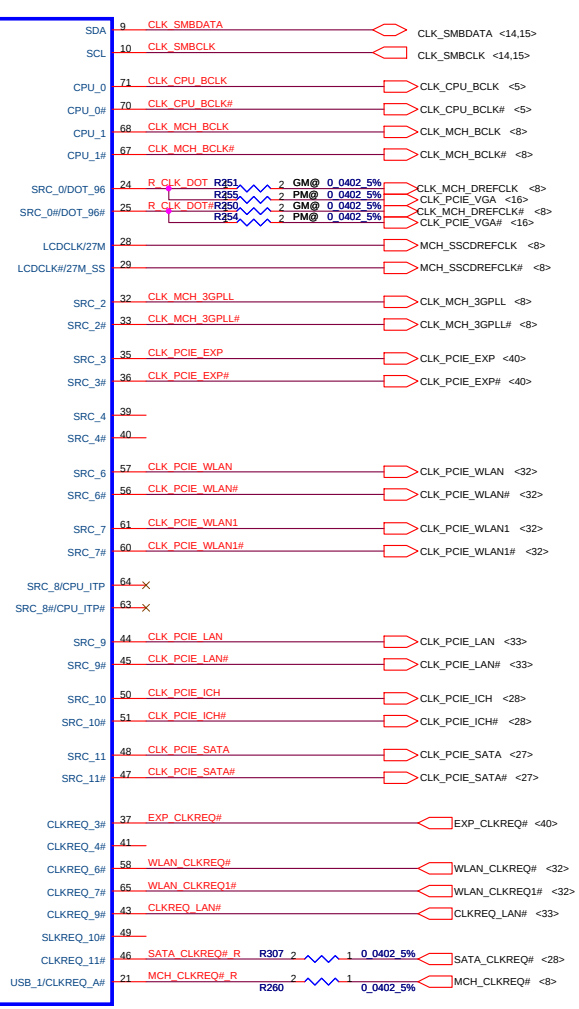


SA000020K00 (Silego : SLG8SP556VTR)

SA000020H00 (ICS : ICS9LPRS387AKLFT)

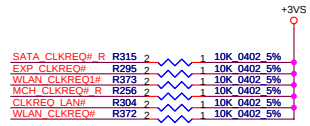






SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

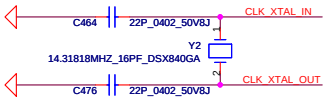


REQ PORT LIST

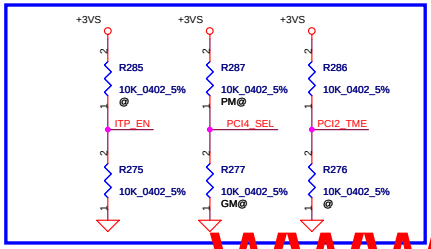
PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS



Routing the trace at least 10mil



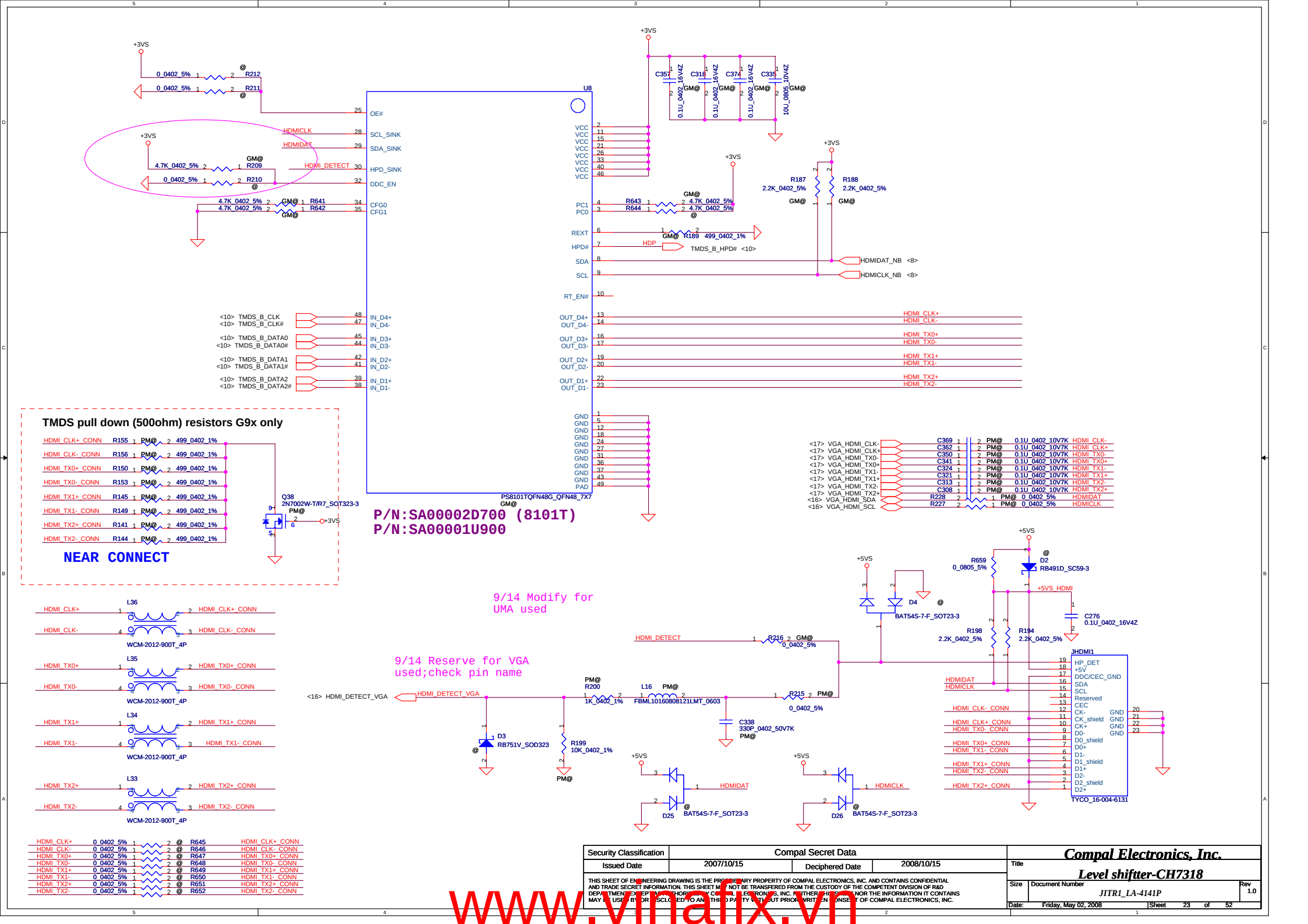
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Clock generator**

Size	Document Number	Rev
	JITR1_LA-4141P	1.0

Date: Monday, May 05, 2008 Sheet 22 of 52


U8
PS8101TQFN48G_QFN48_7X7
GM@
P/N:SA00002D700 (8101T)
P/N:SA00001U900
TMDS pull down (500ohm) resistors G9x only
NEAR CONNECT
Q38
2N7002W-T/R7_SOT323-3
9/14 Modify for
UMA used
9/14 Reserve for VGA
used;check pin name
JHDMI1
TYCO_16-004-6131
D2
RB491D_SC59-3
D4
BAT54S-7-F_SOT23-3
D3
RB751V_SOD323
D25
D26
L36
L35
L34
L33
WCM-2012-900T_4P
FBML10160808121LMT_0603
Compal Electronics, Inc.
Level shiftter-CH7318
JITR1_LA-4141P
Security Classification
Compal Secret Data
Issued Date
2007/10/15
Deciphered Date
2008/10/15
Friday, May 02, 2008
Sheet 23 of 52
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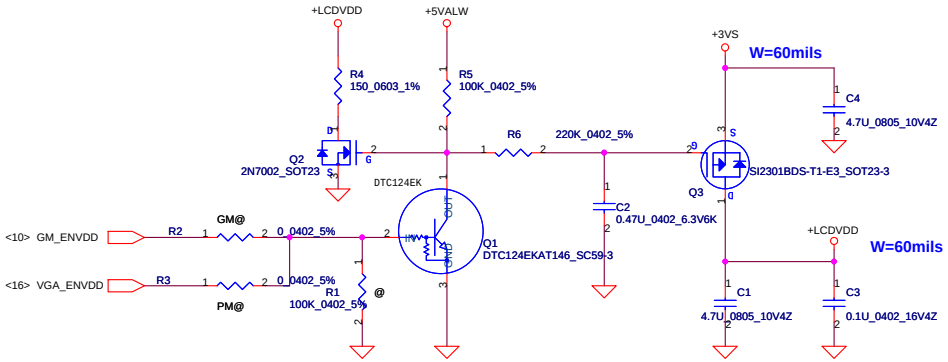
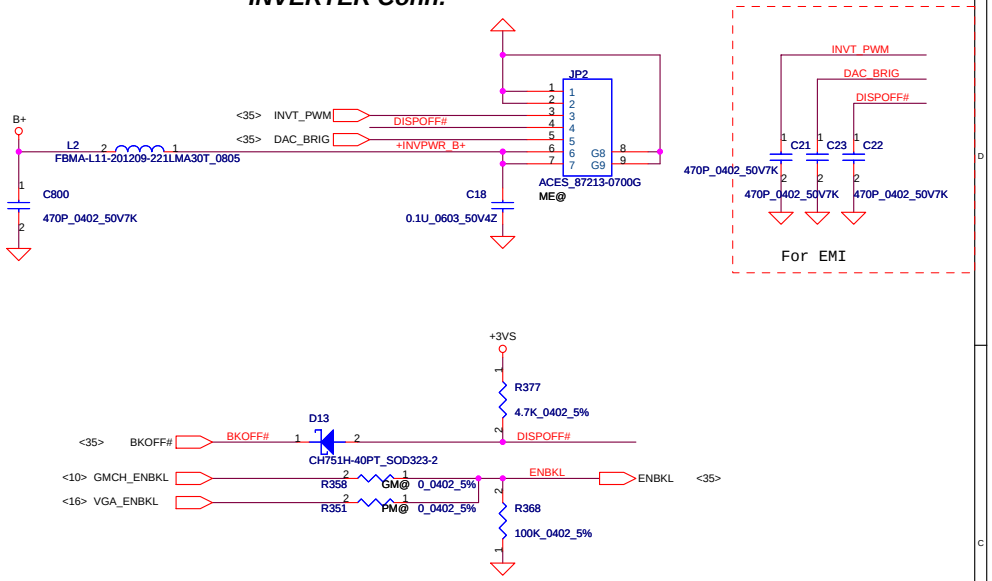
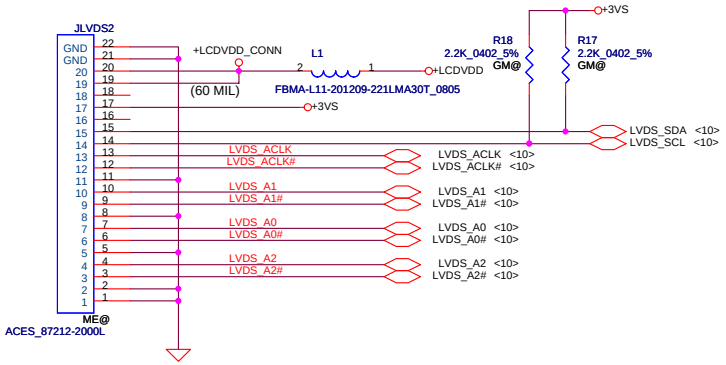
LCD POWER CIRCUIT



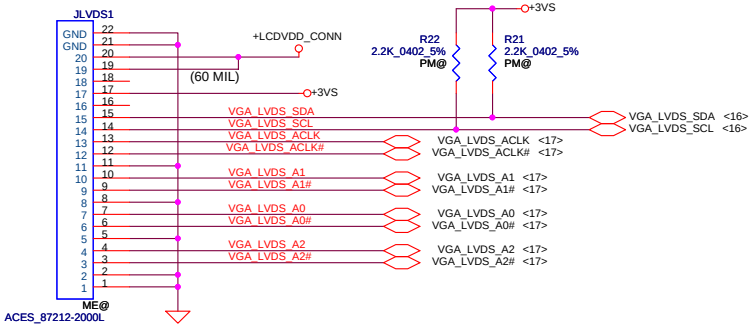
INVERTER Conn.



LCD/PANEL BD. Conn.



LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

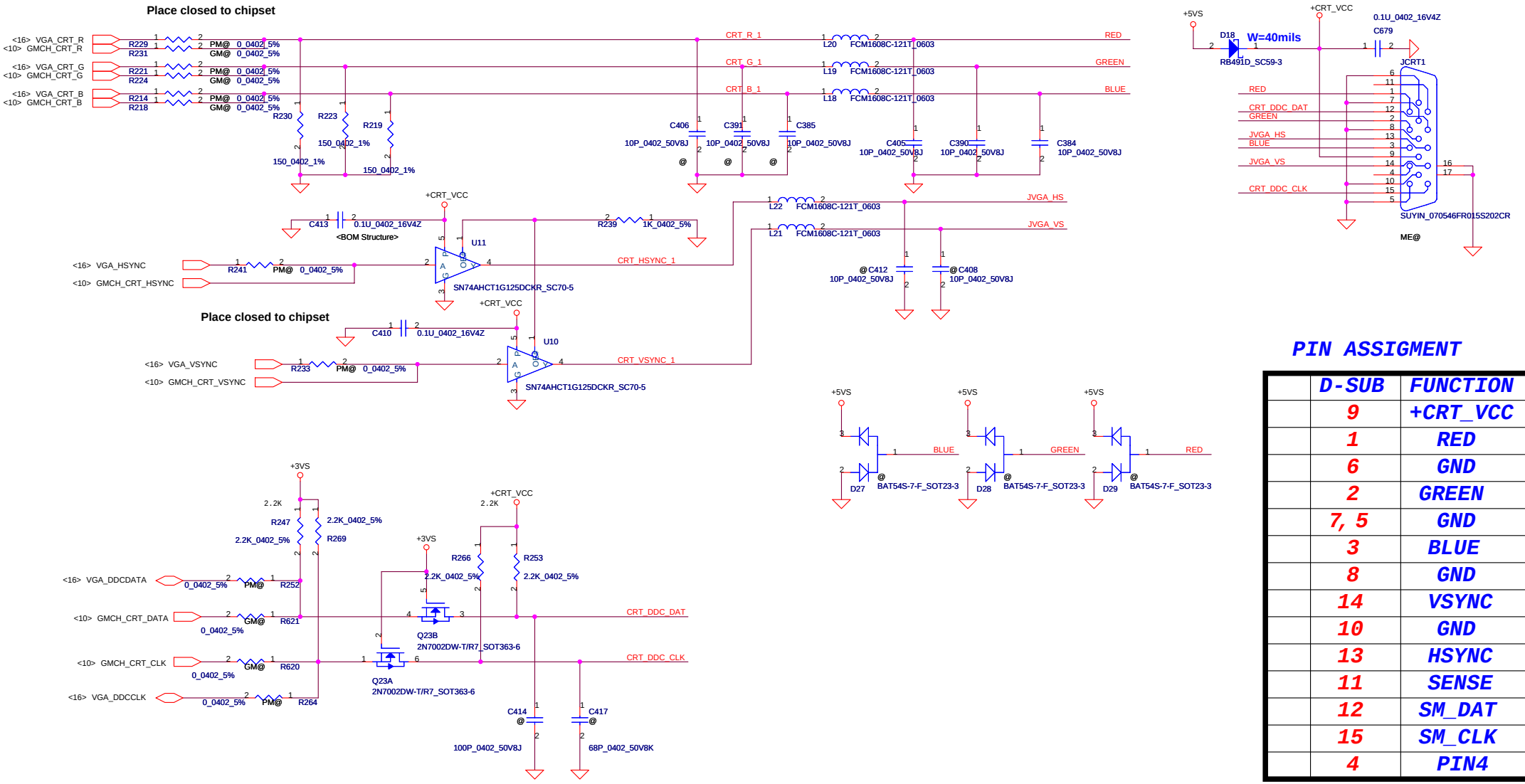
Compal Electronics, Inc.

Title: LVDS & DVI Connector

Size	Document Number	Rev
B	JITR1_LA-4141P	0.1

Date: Friday, May 02, 2008 Sheet 24 of 52

CRT Connector



PIN ASSIGMENT

	D-SUB	FUNCTION
	9	+CRT_VCC
	1	RED
	6	GND
	2	GREEN
	7, 5	GND
	3	BLUE
	8	GND
	14	VSYNC
	10	GND
	13	HSYNC
	11	SENSE
	12	SM_DAT
	15	SM_CLK
	4	PIN4

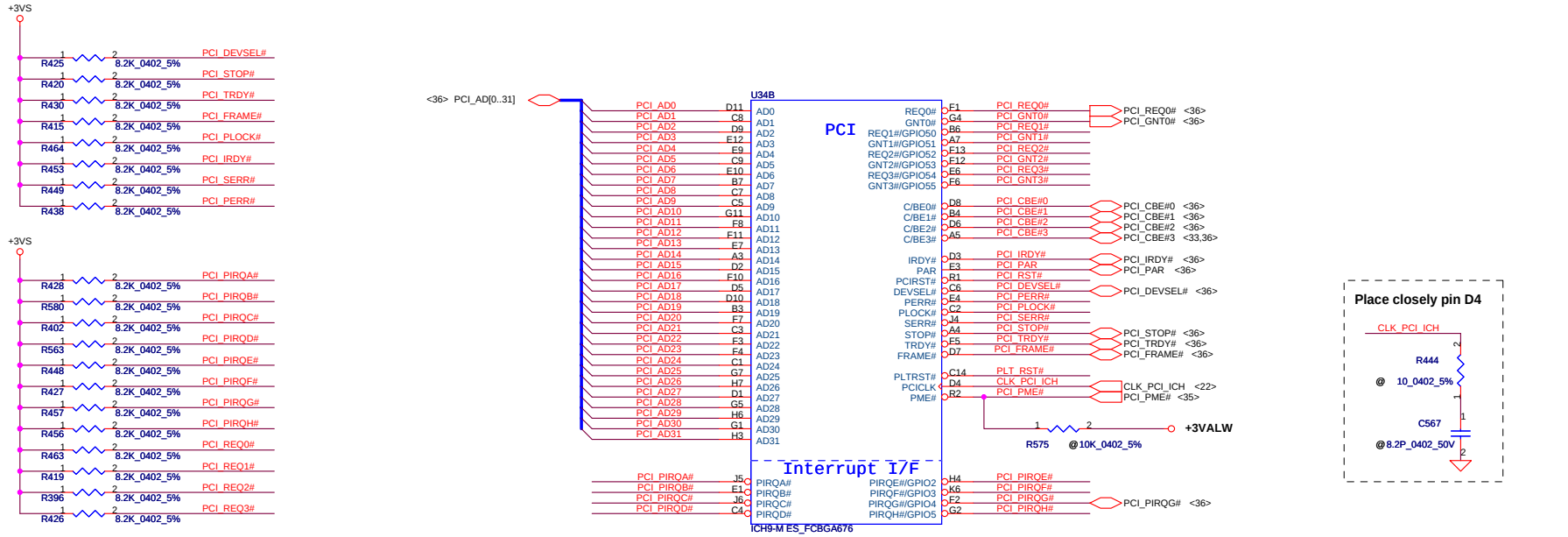
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **CRT & TV-OUT Connector**

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

Date: Friday, May 02, 2008 Sheet 25 of 52

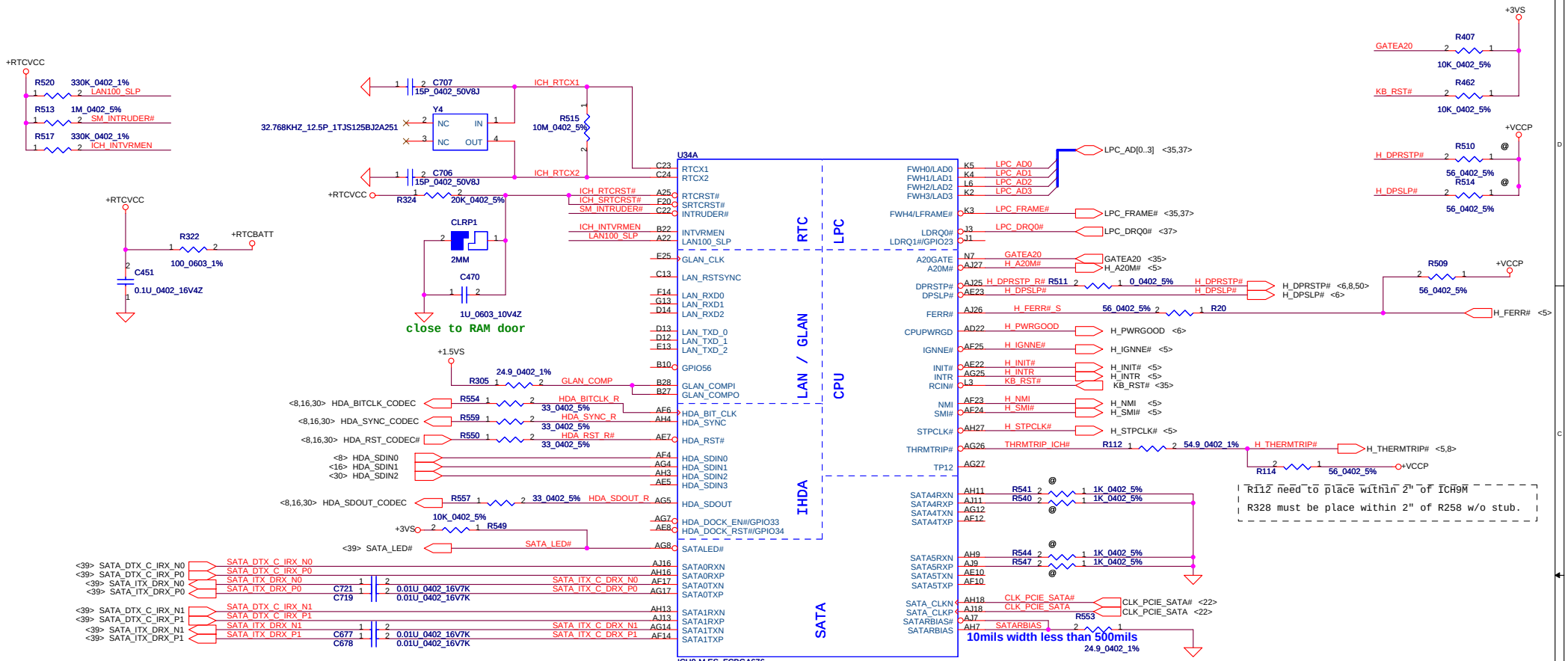


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

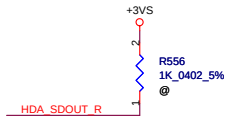
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	ICH9M(1/4)-PCI		
Size	Document Number	JITR1_LA-4141P	Rev 0.1
Date: Friday, May 02, 2008	Sheet 26 of 52		



Need check



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

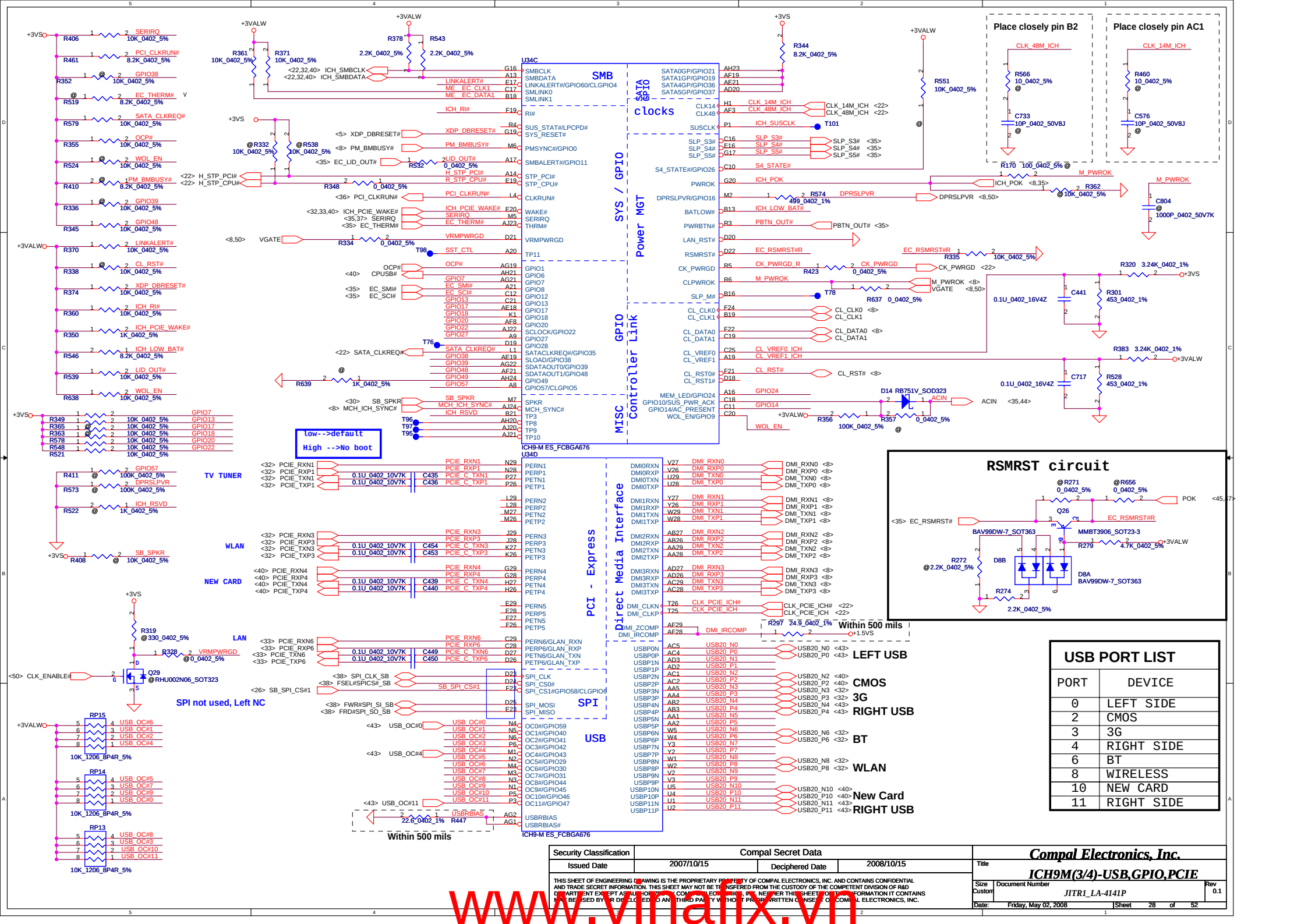
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

Date: Friday, May 02, 2008 Sheet 27 of 52



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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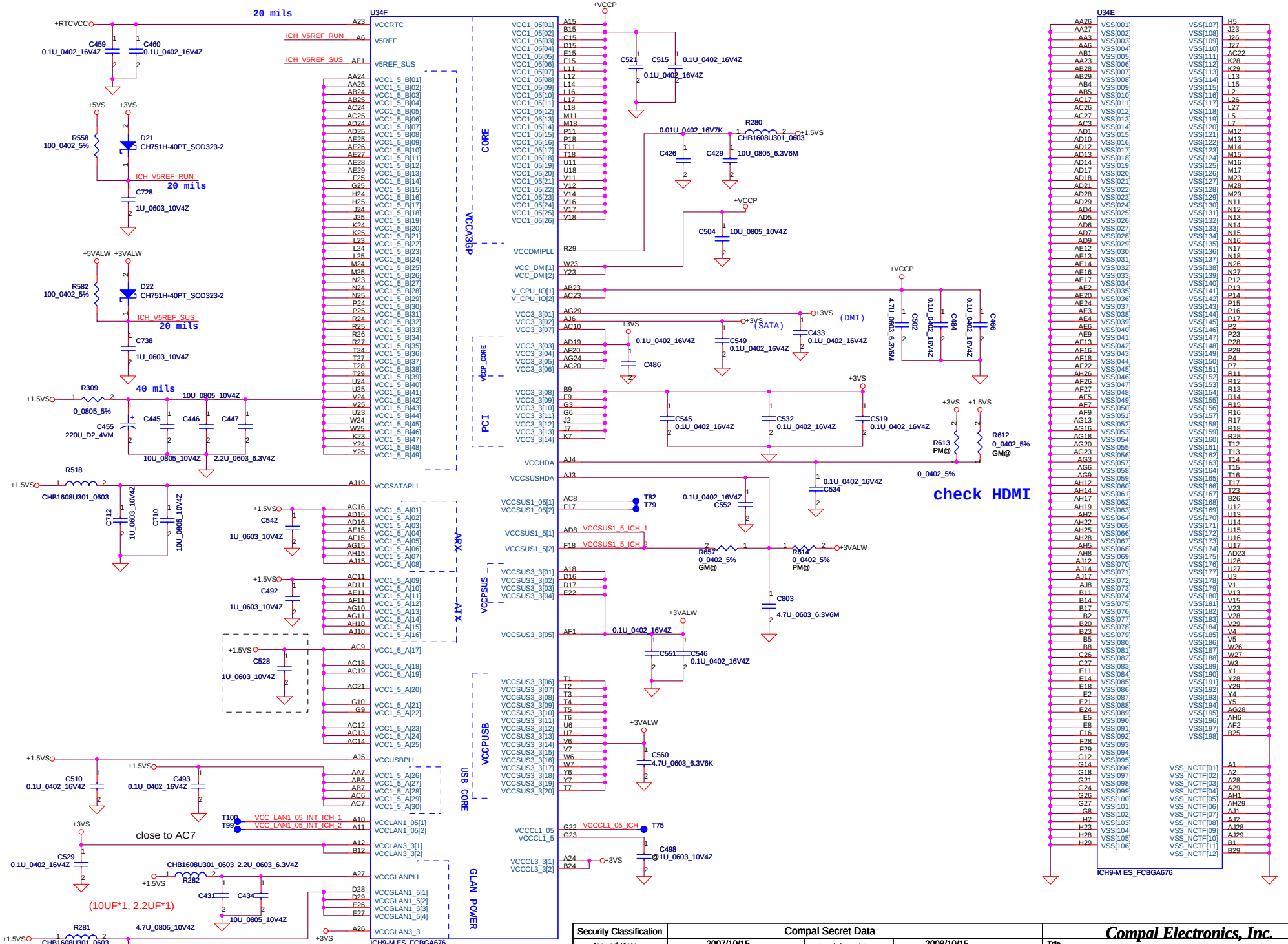
Compal Electronics, Inc.

Title: ICH9M(3/4)-USB,GPIO,PCIE

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

Date: Friday, May 02, 2008 | Sheet 28 of 52



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: ICH9M(4/4)-POWER&GND

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

Date: Monday, May 05, 2008 | Sheet 29 of 52

AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

CHANGE TO 0ohm (2008/05/05)

CODEC POWER

(3.33V)
250mW

W=40Mil

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

4.7kohm for MICL + MICR
2.2kohm for MICL or MICR

PC_BEEP dB control

external MIC

Internal MIC / Array MIC
Internal WOOFER
Internal SPKR.

port A : 5.11K ohm
port B : 10.0K ohm
port C : 20.0K ohm
port D : 39.2K ohm

DIGITAL ANALOG

Place these C and R around AGND and DGND, then choose the one which is close to Codec to populate

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: CX20561-AMOM Codec

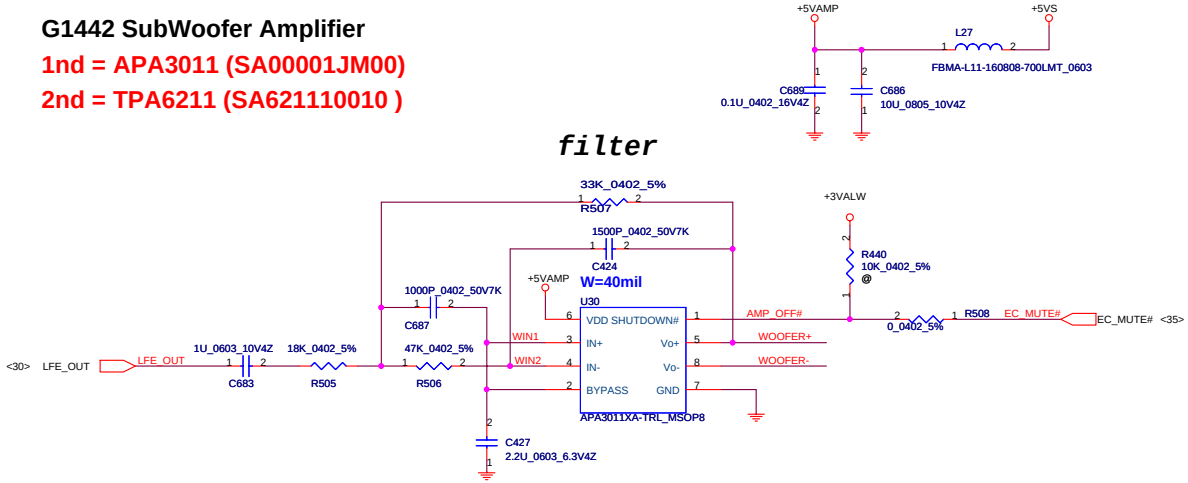
Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

Date: Wednesday, May 07, 2008 | Sheet 30 of 52

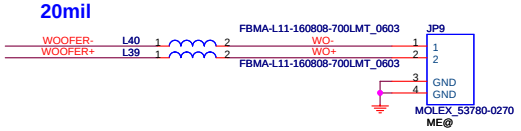
G1442 SubWoofer Amplifier

1nd = APA3011 (SA00001JM00)

2nd = TPA6211 (SA621110010)



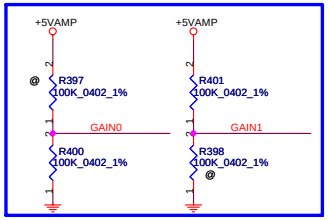
SubWoofer Conn.



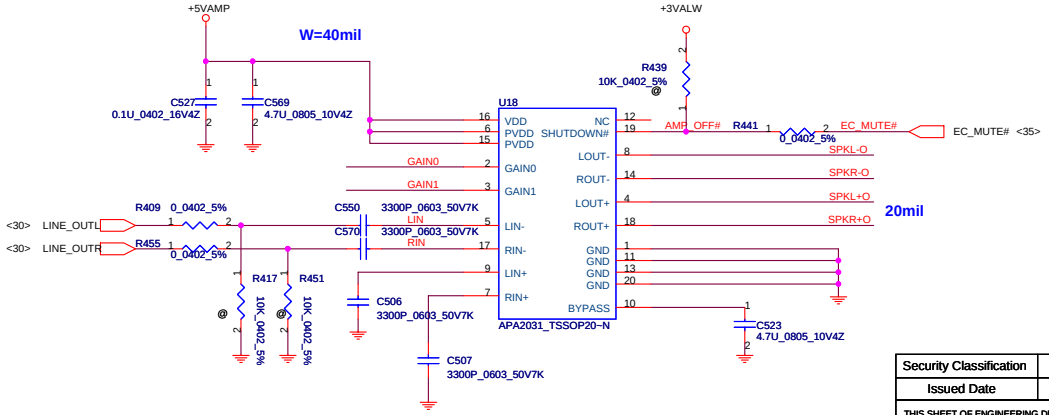
Speaker Amplifier

1nd = APA2031 (SA00001RZ00)

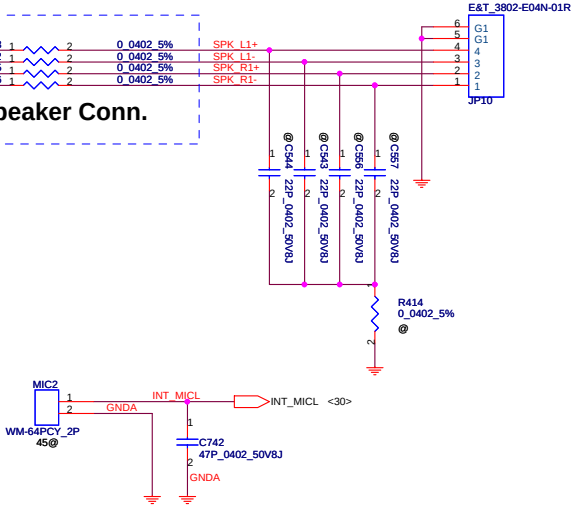
2nd = G1431F2U (SA000012Y00)



GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



INT MIC



Speaker Conn.

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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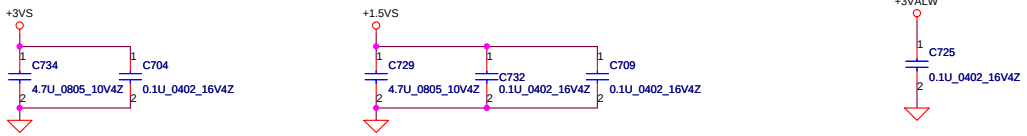
Compal Electronics, Inc.

Title: **AMP/VR/Audio Jack/MIC**

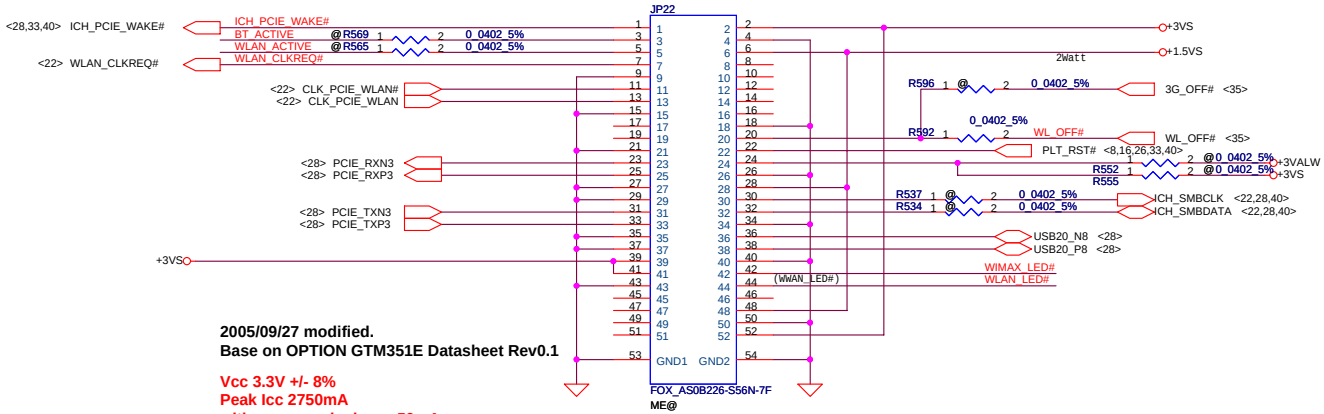
Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

Date: Friday, May 02, 2008 | Sheet 31 of 52

Mini-Express Card for 3G Or TV Tuner
Mini-Express Card for WLAN



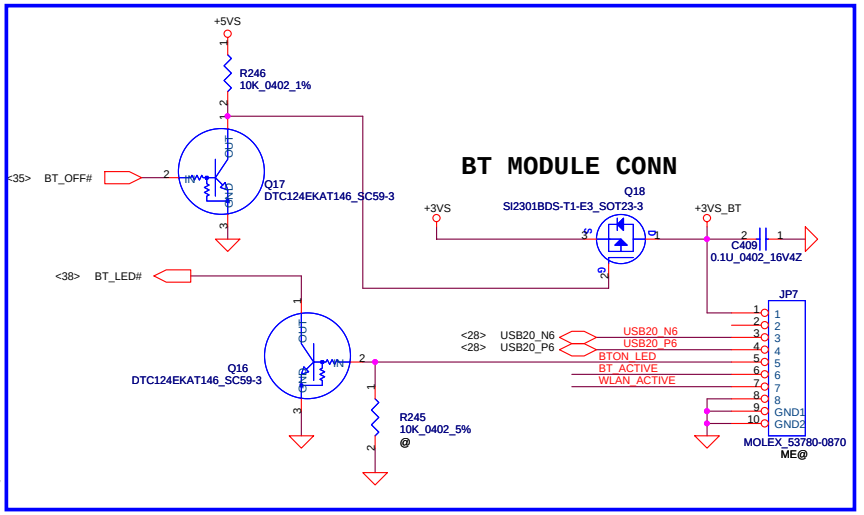
Mini-Express Card(Slot 1-WLAN WIMAX)

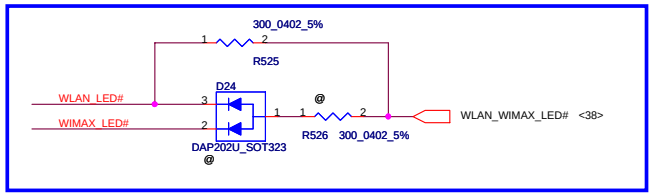


2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

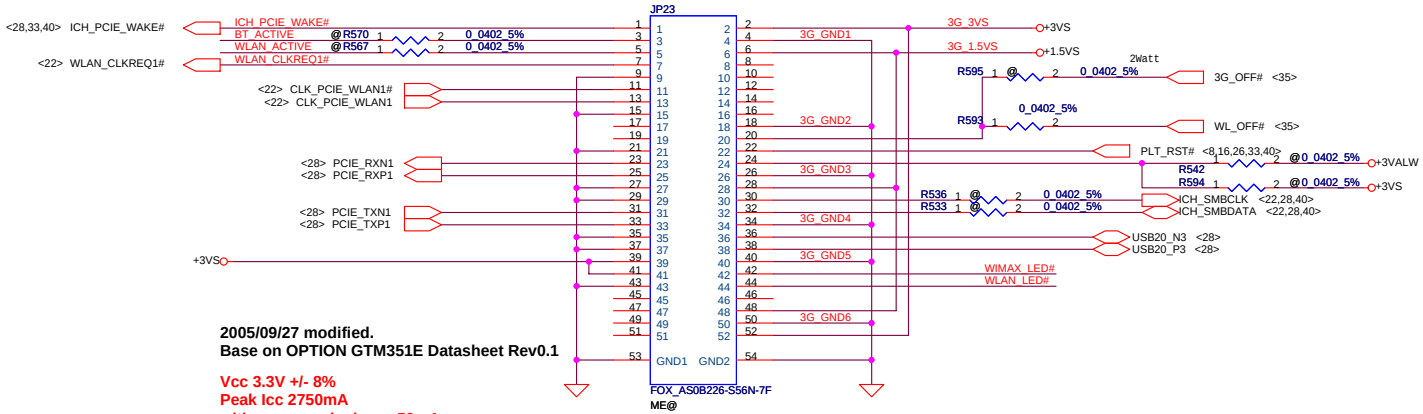
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

BT MODULE CONN





Mini-Express Card(Slot 2-WLAN WIMAX)



2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Mini-Card/3G/FeliCa/BT**

Size	Document Number	Rev
	JITR1_LA-4141P	0.1

Date: Monday, May 05, 2008 Sheet 32 of 52

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

Layout Notice : 1.2V filter. Place as close chip as possible.

(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

Notice : 4.7u 6.3V capactor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

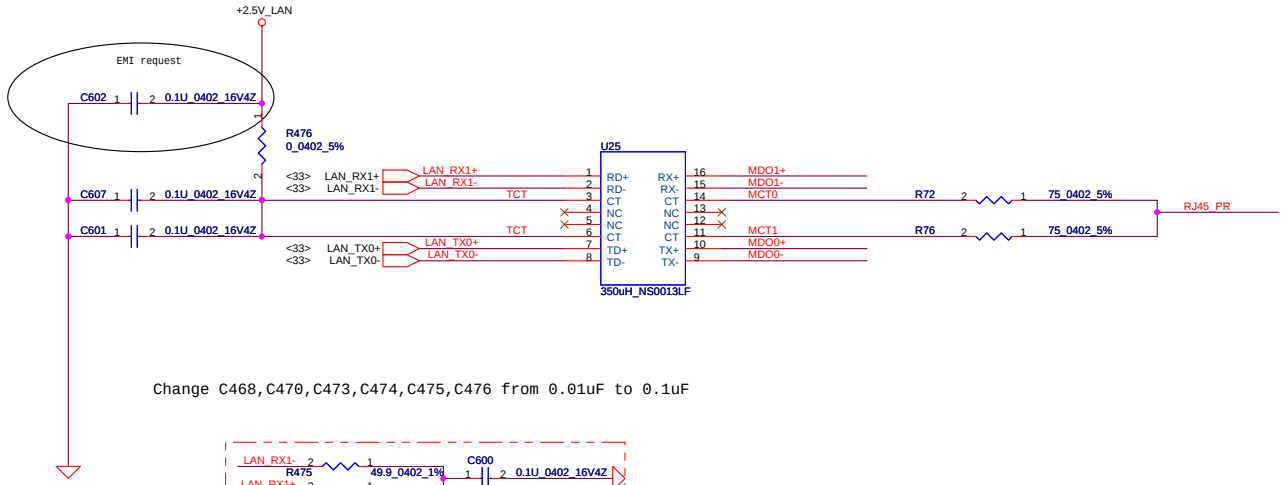
Compal Electronics, Inc.

Title: BCM5787MKML

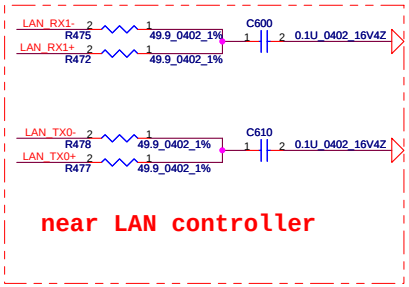
Size: Custom | Document Number: JITR1_LA-4141P | Rev: 0.1

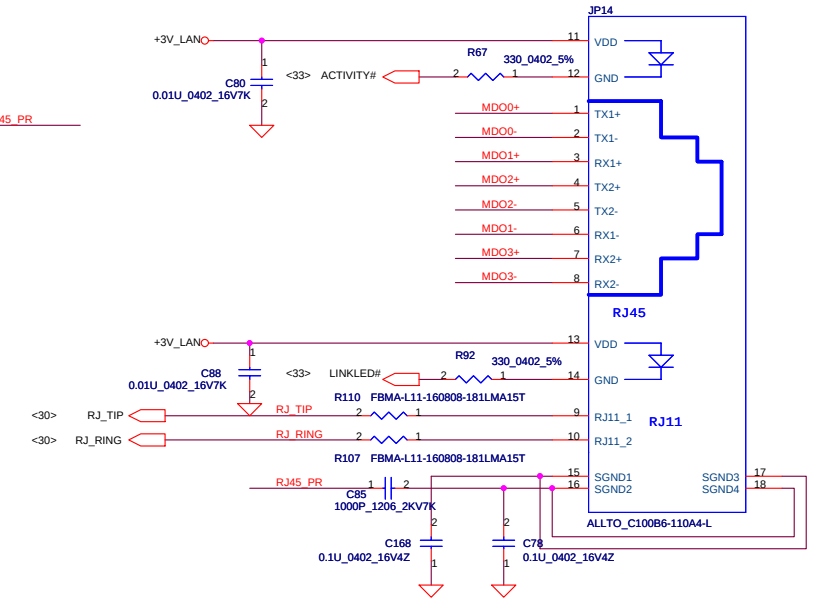
Date: Friday, May 02, 2008 | Sheet 33 of 52

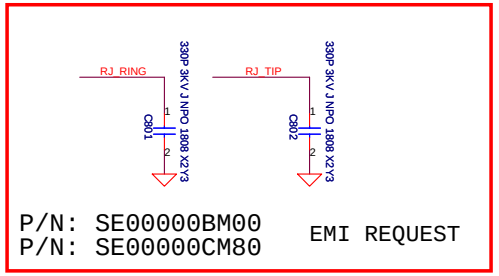
RJ11+RJ45 CONN



Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

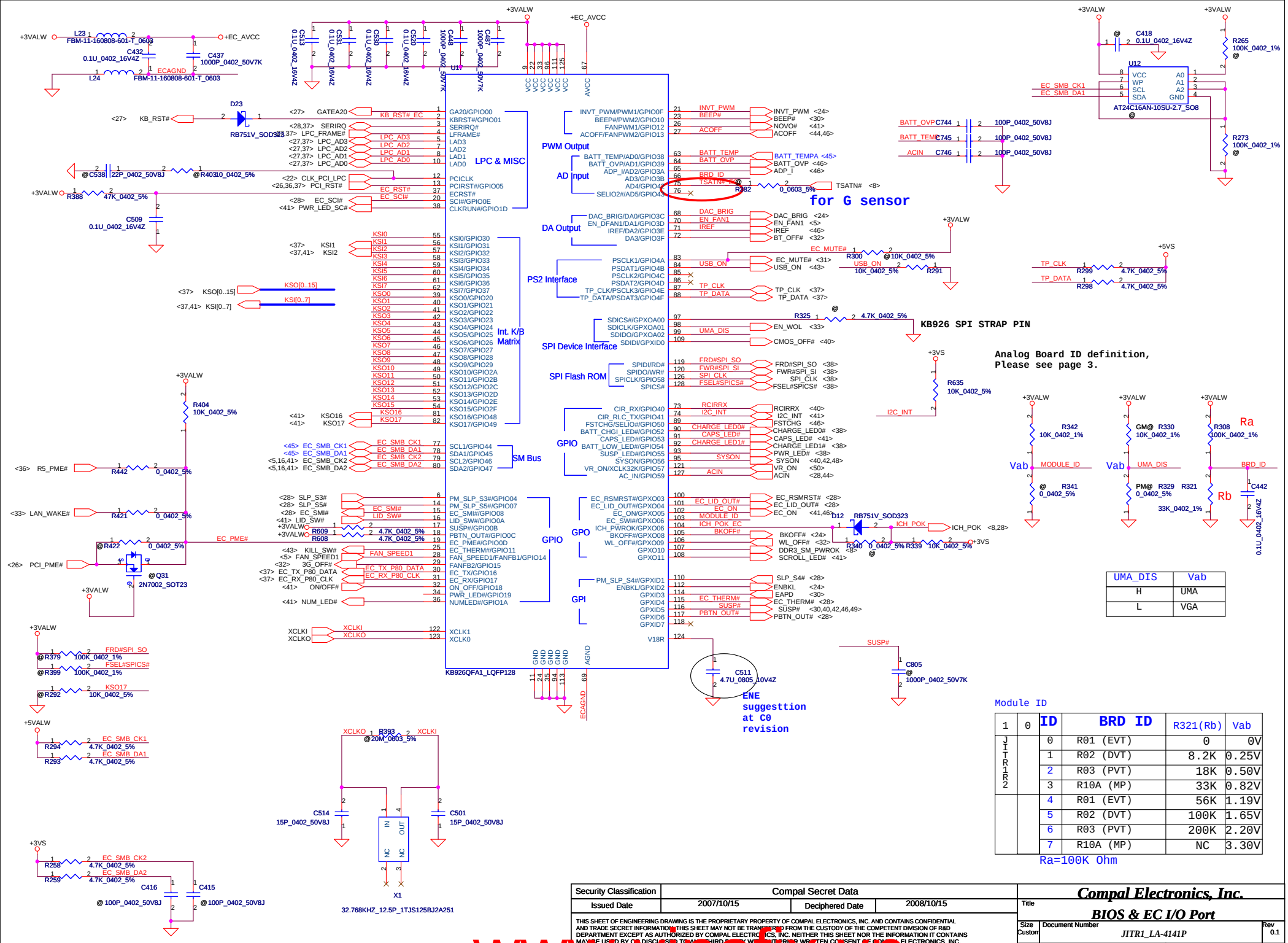






Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: LAN CONTROLLER			
Size: Custom	Document Number: JITR1_LA-4141P		Rev: 0.1
Date: Friday, May 02, 2008	Sheet 34 of 52		



UMA_DIS	Vab
H	UMA
L	VGA

Module ID

		ID	BRD ID	R321(Rb)	Vab
JITR12	1	0	0	R01 (EVT)	0	0V
			1	R02 (DVT)	8.2K	0.25V
			2	R03 (PVT)	18K	0.50V
			3	R10A (MP)	33K	0.82V
			4	R01 (EVT)	56K	1.19V
			5	R02 (DVT)	100K	1.65V
			6	R03 (PVT)	200K	2.20V
			7	R10A (MP)	NC	3.30V

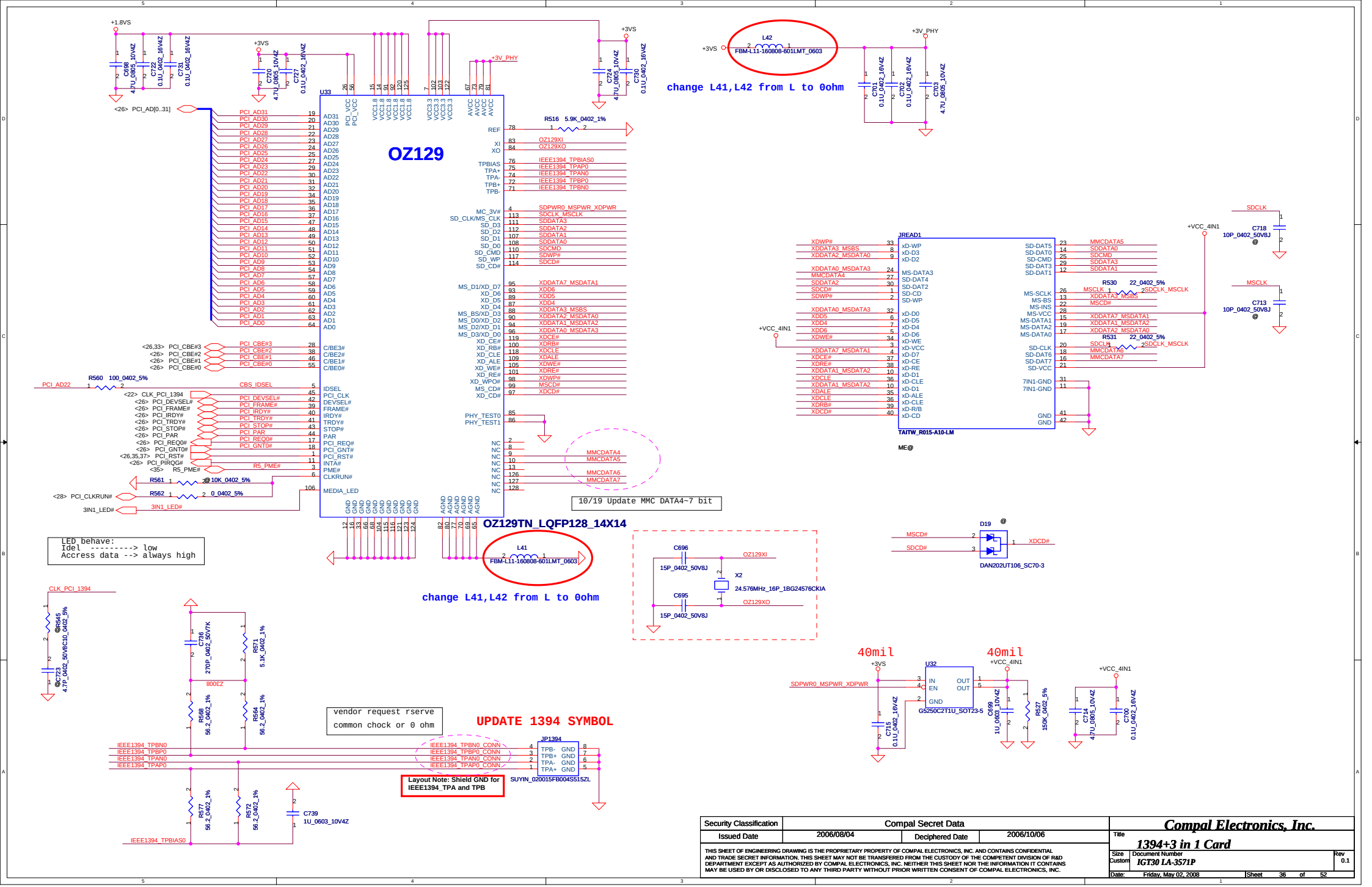
Ra=100K Ohm

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: BIOS & EC I/O Port

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1
Date: Monday, May 05, 2008	Sheet 35 of 52	



Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

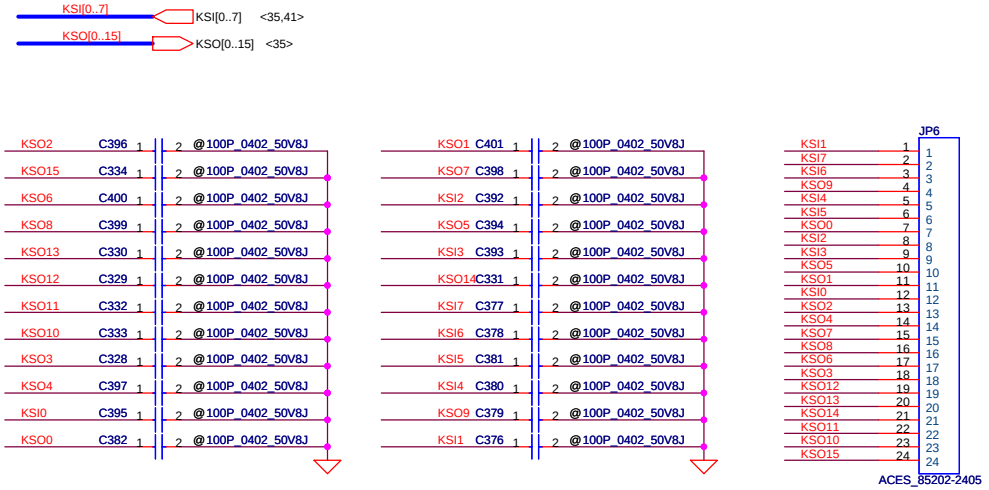
Compal Electronics, Inc.

Title: **1394+3 in 1 Card**

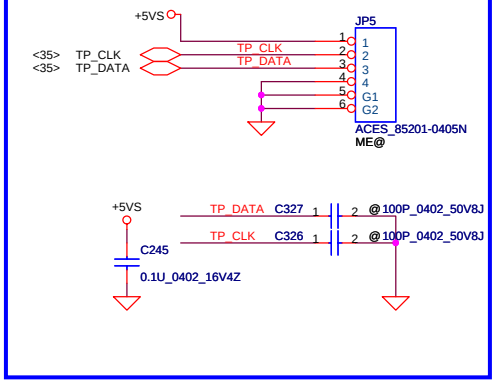
Size	Document Number	Rev
Custom	IGT30 LA-3571P	0.1

Date: Friday, May 02, 2008 | Sheet 36 of 52

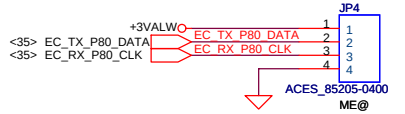
INT_KBD Conn.



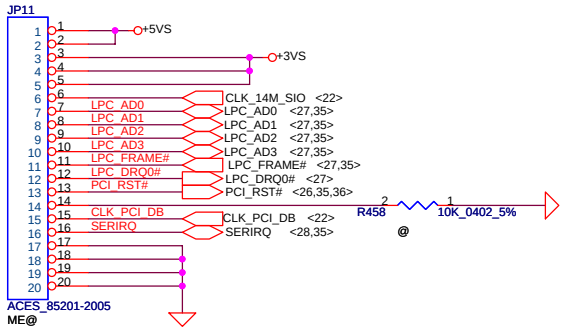
To TP/B Conn.



EC DEBUG PORT



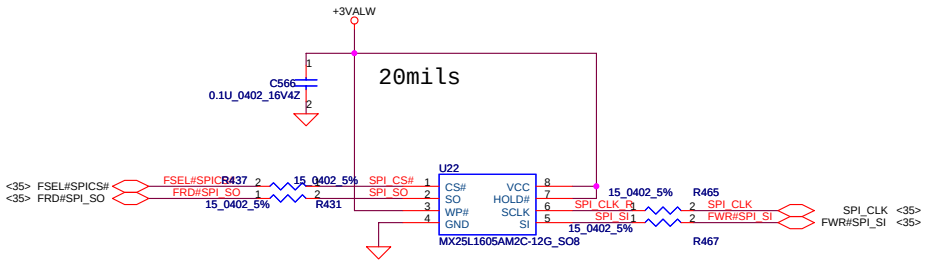
FOR LPC SIO DEBUG PORT

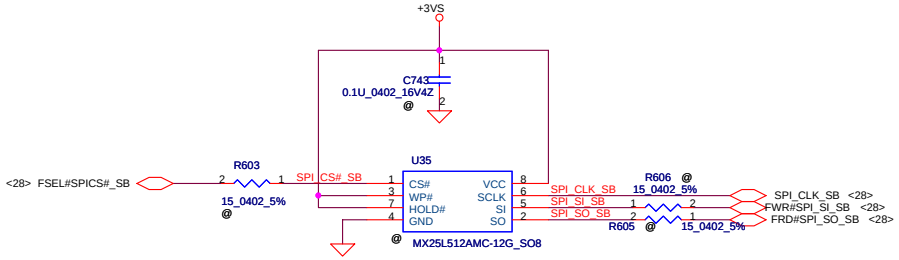


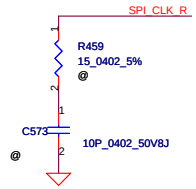
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

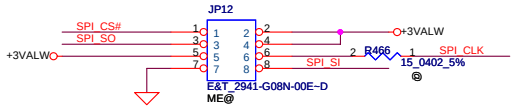
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: JITR1_LA-4141P		Rev: 0.1
Date: Friday, May 02, 2008	Sheet 37 of 52		

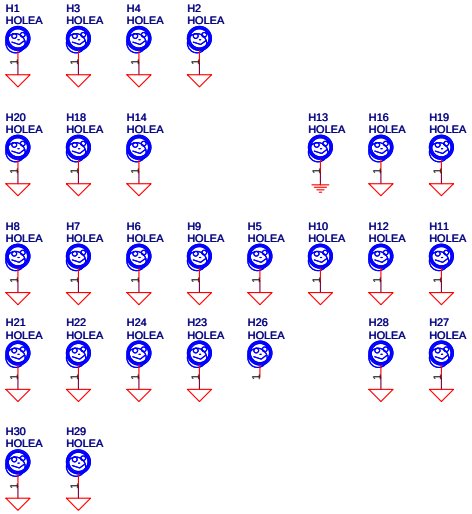
FOR EC 16M SPI ROM



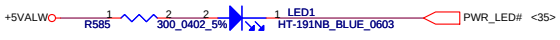


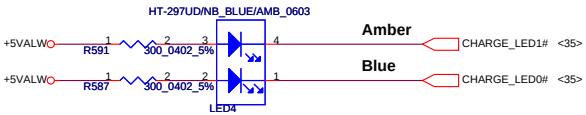




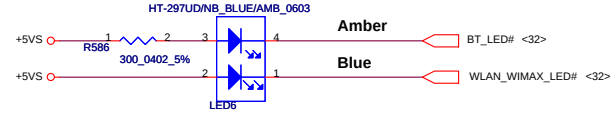


LED





Blue&Amber



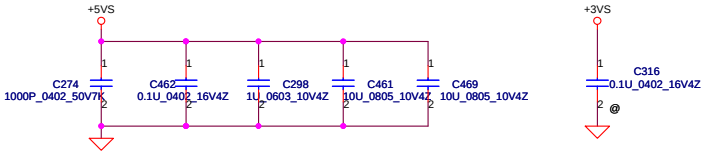
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

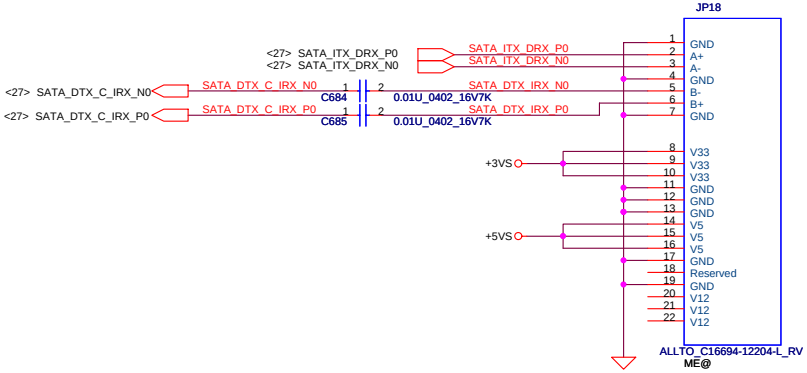
Title: **LED/EC SPI ROM**

Size	Document Number	Rev
B	JITR1_LA-4141P	0.1

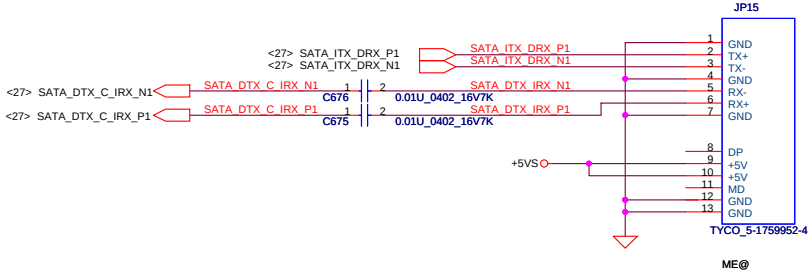
Date: Monday, May 05, 2008 Sheet 38 of 52

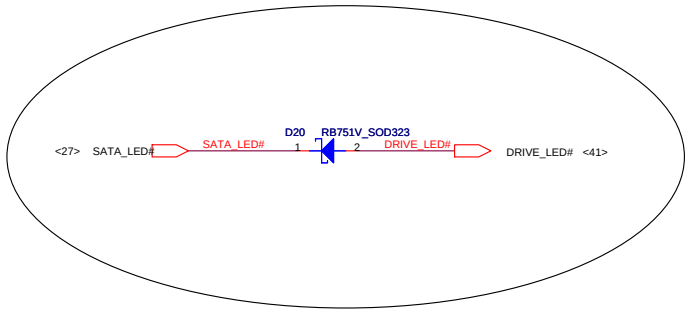


SATA HDD Conn.



SATA ODD Conn.

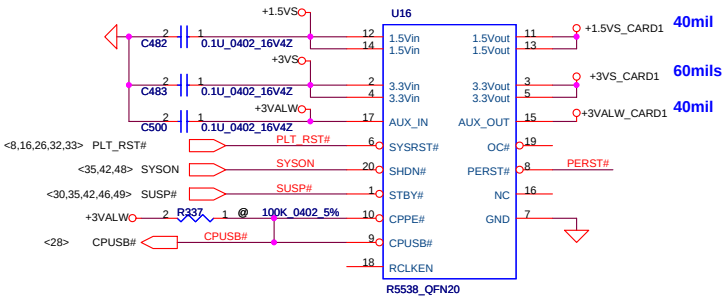


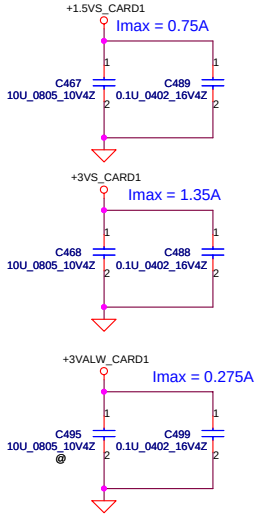


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

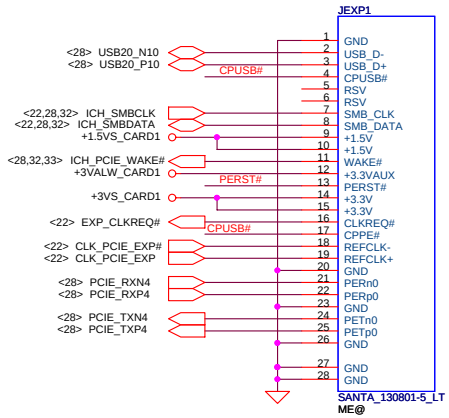
Compal Electronics, Inc.			
Title: HDD & ODD Connector			
Size: B	Document Number: JITR1_LA-4141P		Rev: 0.1
Date: Friday, May 02, 2008		Sheet 39 of 52	

Express Card Power Switch



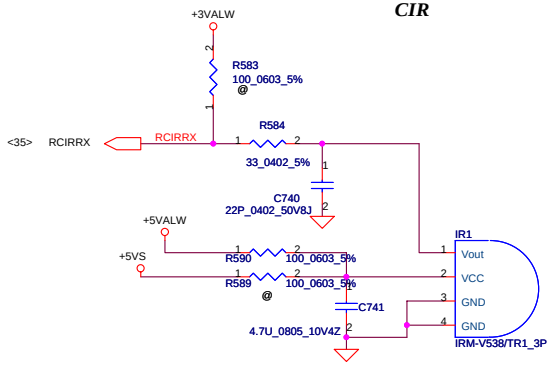


New Card Socket (Left/TOP)

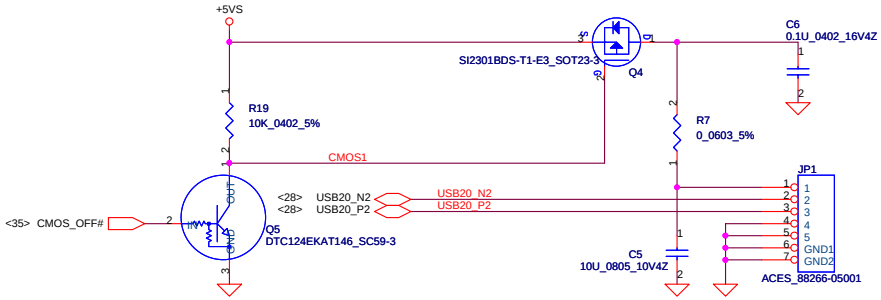


(NEW)

CIR



CMOS Camera Conn



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

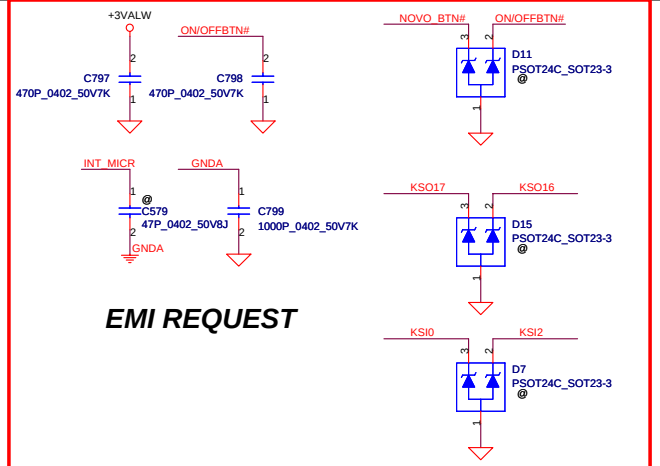
Compal Electronics, Inc.

Title: NEW CARD & CMOS Connector

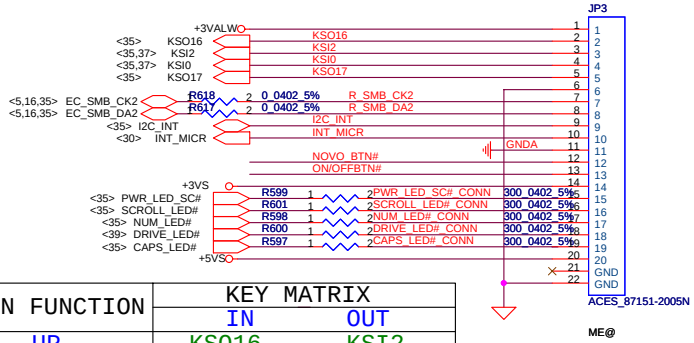
Size	Document Number	Rev
B	JITR1_LA-4141P	0.1

Date: Friday, May 02, 2008 Sheet 40 of 52

EMI REQUEST



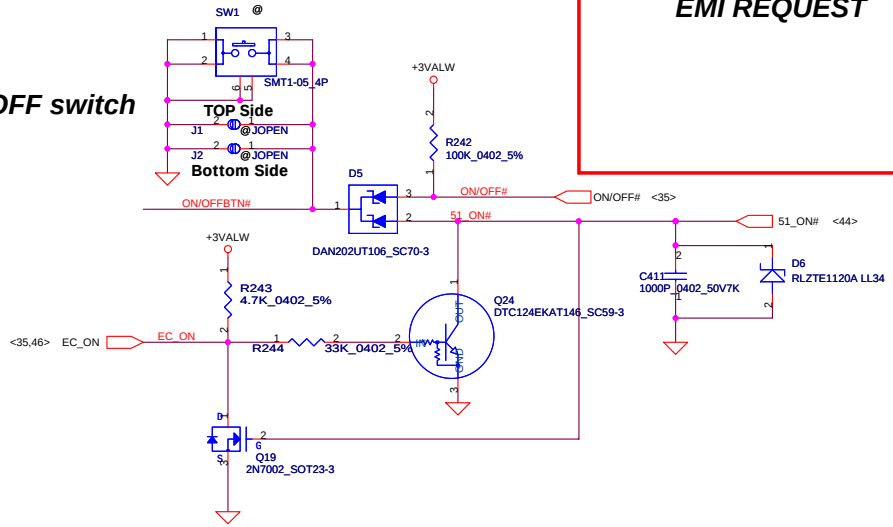
Switch Board Conn.



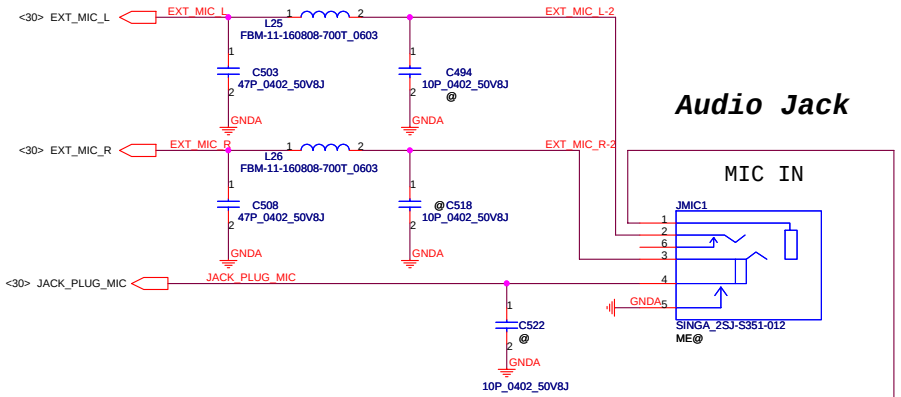
BTN FUNCTION	KEY MATRIX	
	IN	OUT
UP	KSO16	KSI2
DOWN	KSO17	KSI2
OK	KSO17	KSI0

Power Button

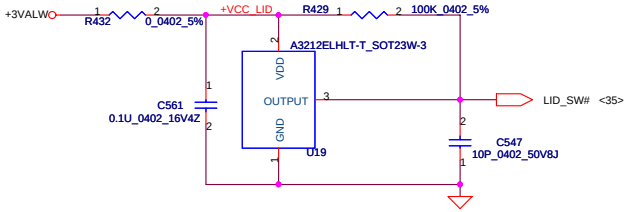
ON/OFF switch

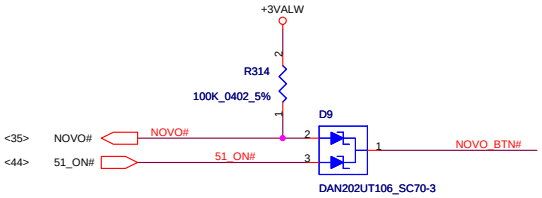


Audio Jack

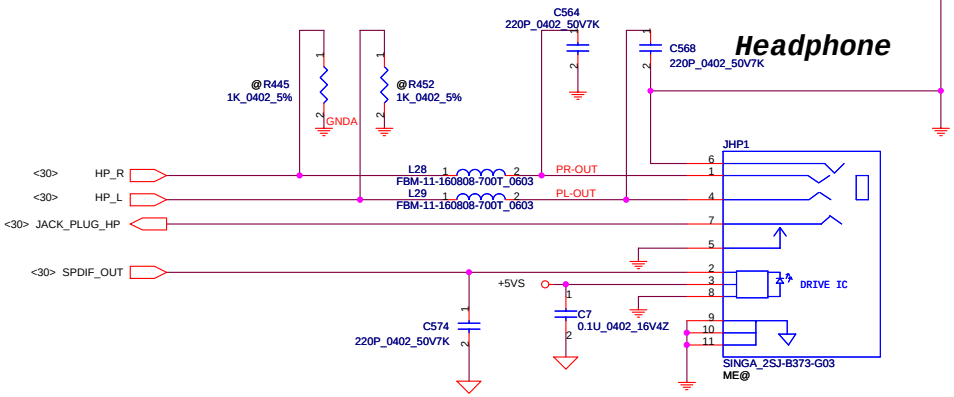


Lid Switch





Headphone



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

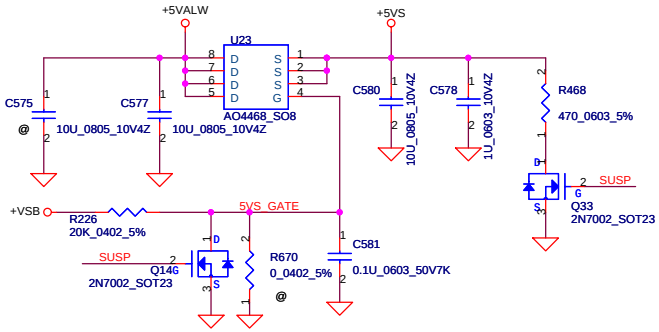
Compal Electronics, Inc.

Title: **Audio Jack & SW connector**

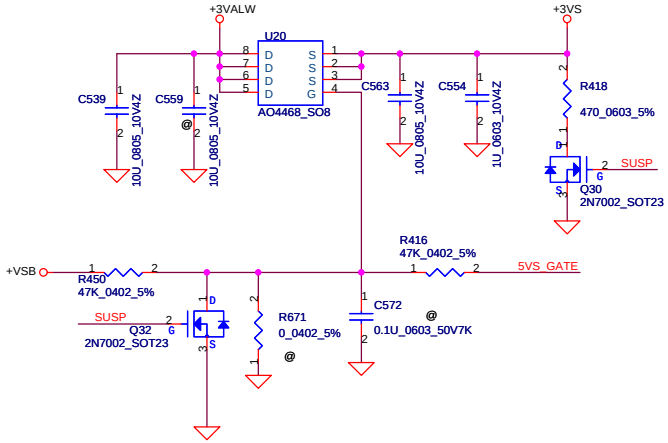
Size	Document Number	Rev
B	JITR1_LA-4141P	0.1

Date: Wednesday, May 07, 2008 Sheet 41 of 52

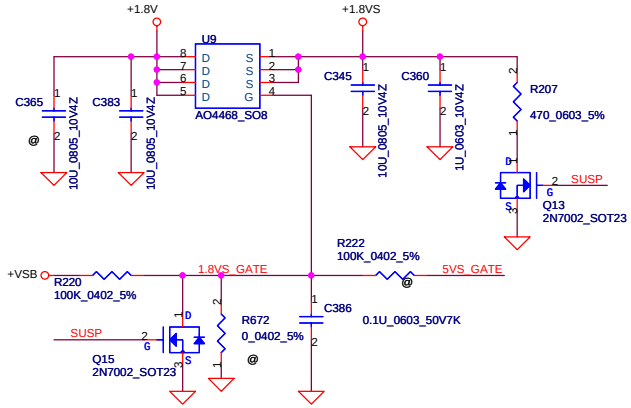
+5VALW TO +5VS



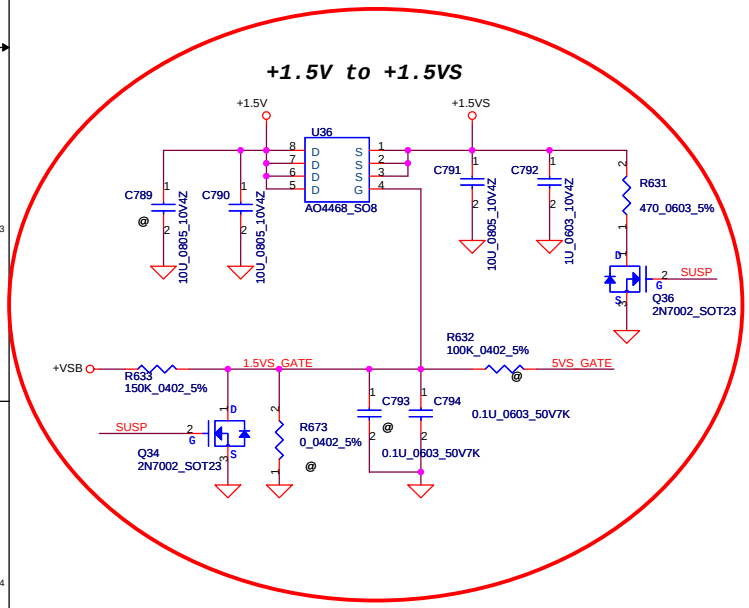
+3VALW TO +3VS

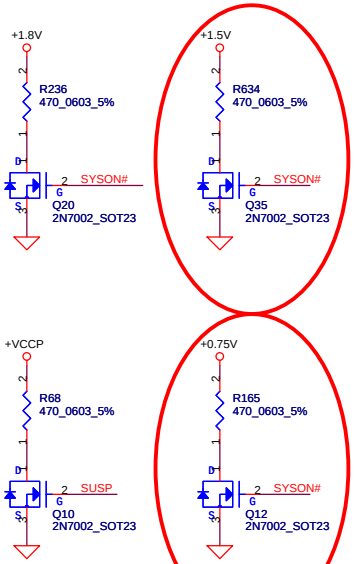


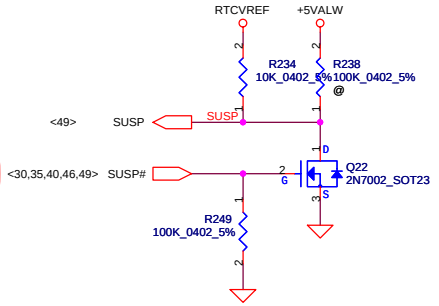
+1.8V to +1.8VS

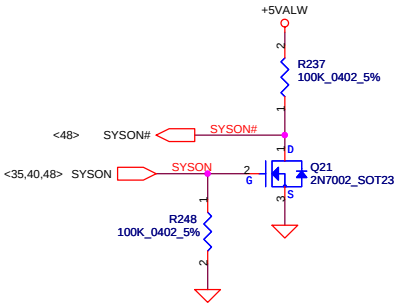


+1.5V to +1.5VS









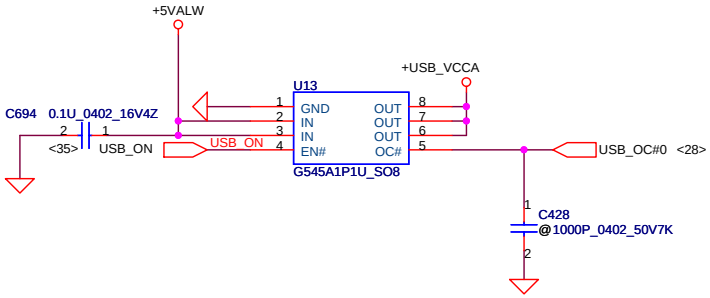
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

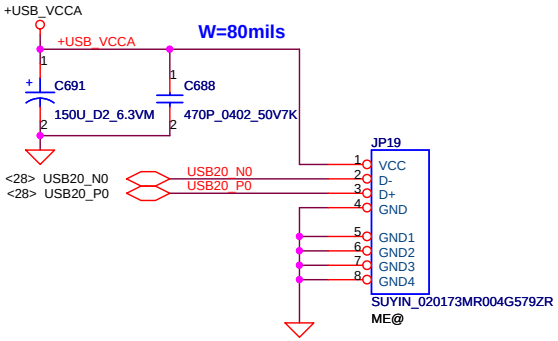
Title: DC Interface

Size	Document Number	Rev
Custom	LA-3691P	1.0

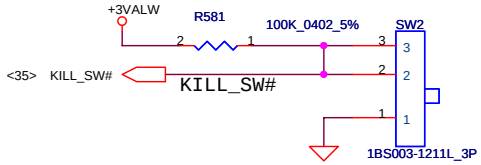
Date: Monday, May 05, 2008 Sheet 42 of 52

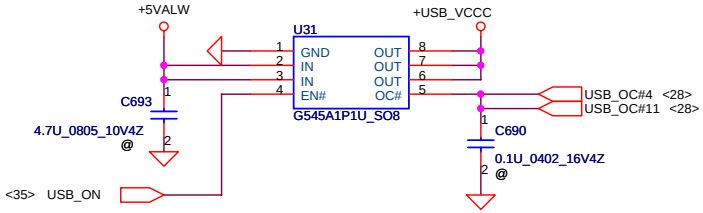


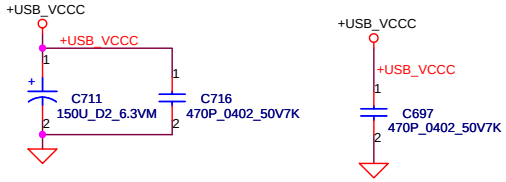
LIFT USB CONN. 1



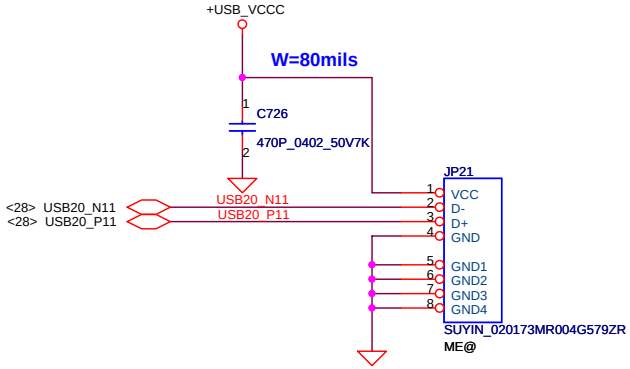
Kill Switch



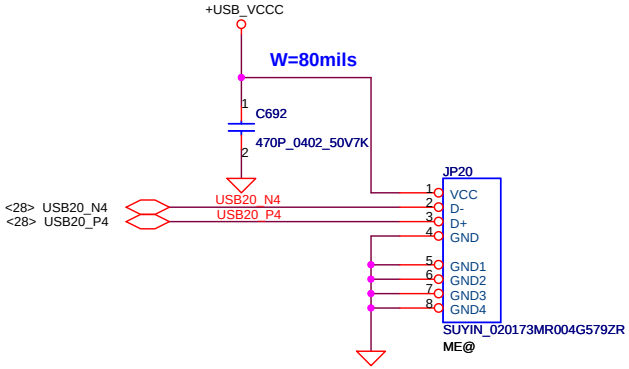




RIGHT USB CONN. 3



RIGHT USB CONN. 2



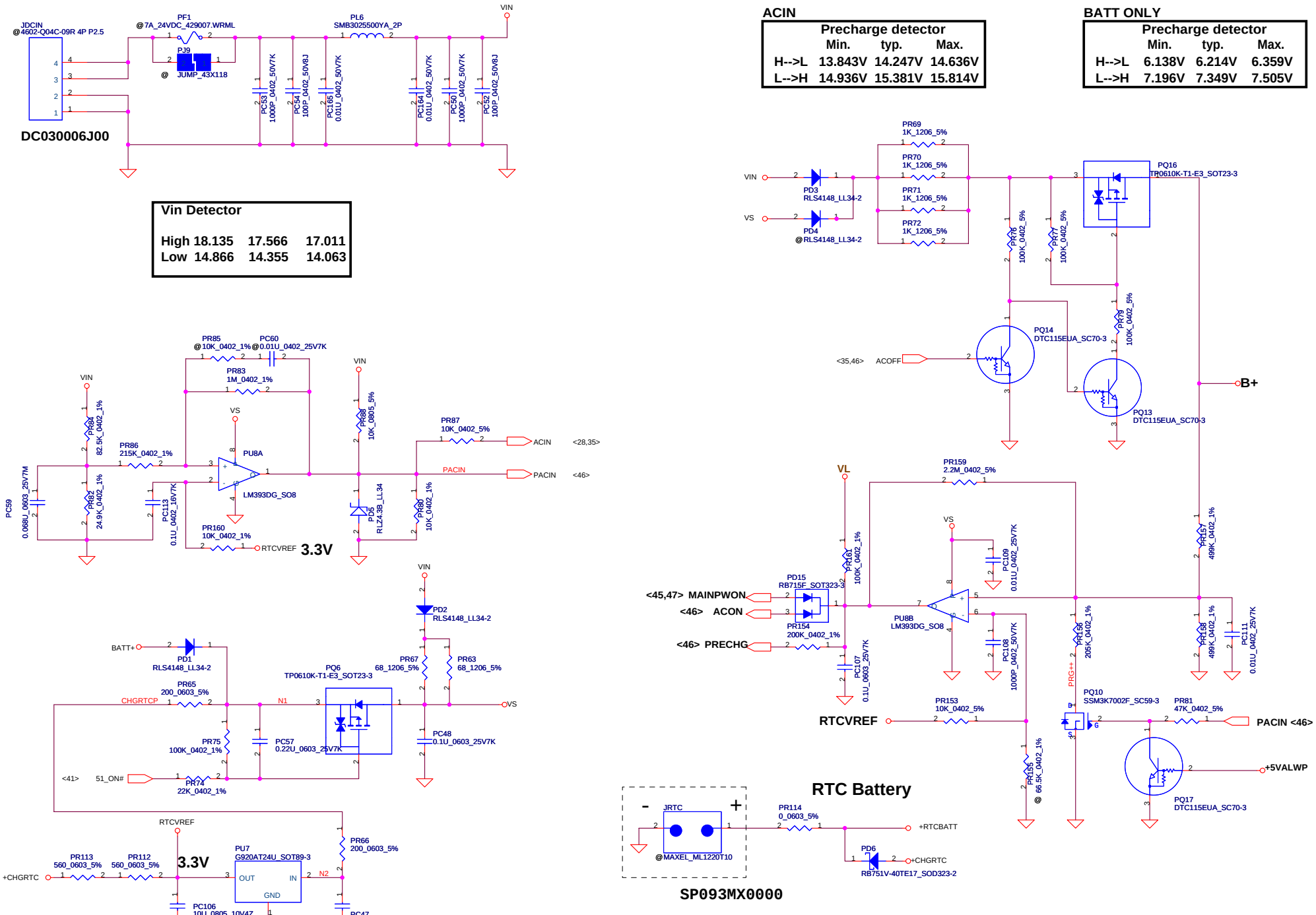
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: Power OK, Reset and RTC Circuit, TP

Size	Document Number	Rev
Custom	LA-3691P	1.0

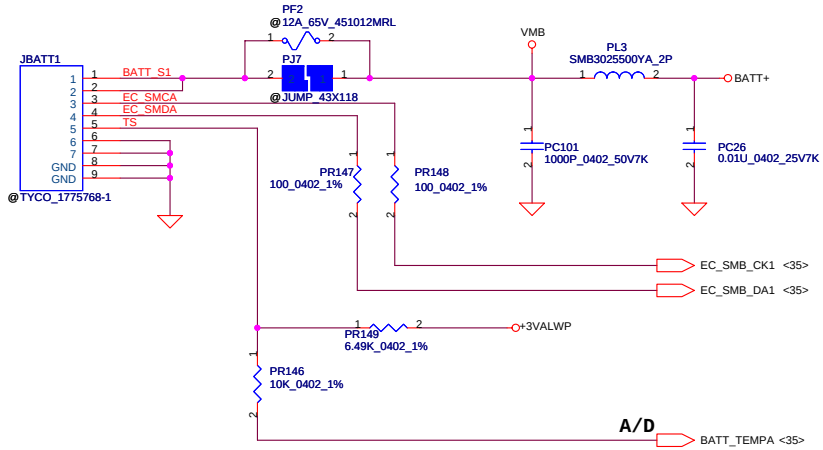
Date: Monday, May 05, 2008 Sheet 43 of 52

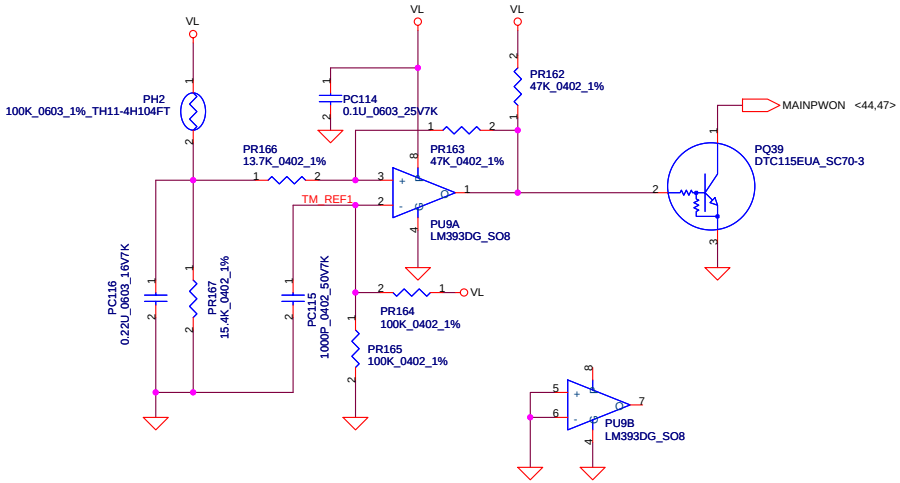


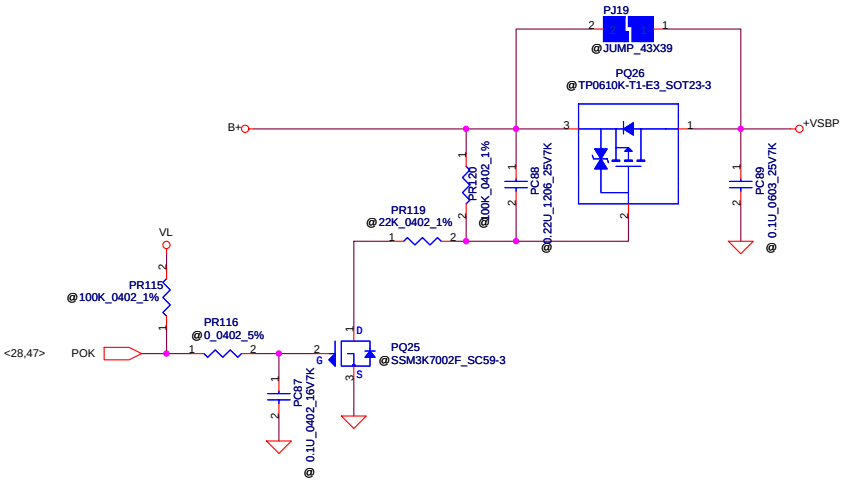
Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

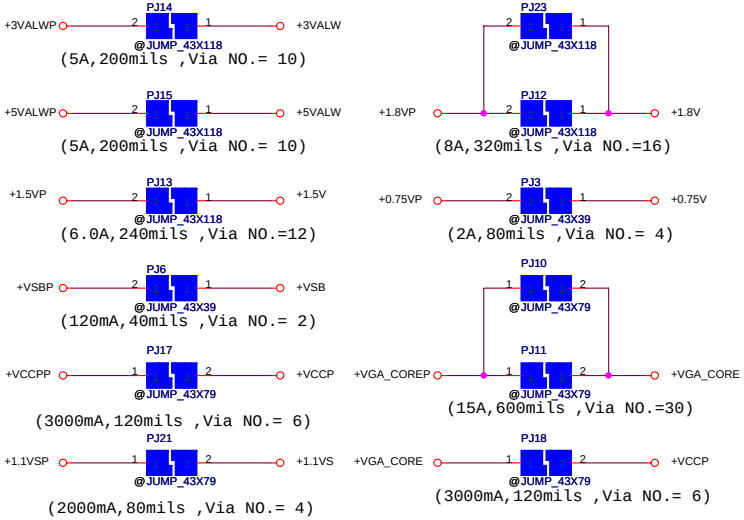
Compal Electronics, Inc.			
Title	DCIN & DETECTOR		
Size	Document Number		Rev 0.1
Date: Friday, May 02, 2008	Sheet 44 of 52		

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C









Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.1

Date: Friday, May 02, 2008 | Sheet 45 of 52

Charger

CP mode
65W: 2.8A
90W: 4.0A

Fosc=14100/Rt=14100/47=300KHz

65W: PR1=49.9K
90W: PR1=31.6K

IREF=0.4~2.88V

LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+

CC=3.6A
(100K/(100K+100K))*2.88V=1.44V
1.44/(20*0.02)=3.6A

Charge voltage
3S CC-CV MODE : 12.6V
SEL is L

Adapter 65W CP Point=2.8A
5V*(10K/(49.9K+10K))=0.835V
0.835V/(20*0.015)=2.78A
Adapter 90W CP Point=4A
5V*(10K/(31.6K+10K))=1.202V
1.202V/(20*0.015)=4.006A

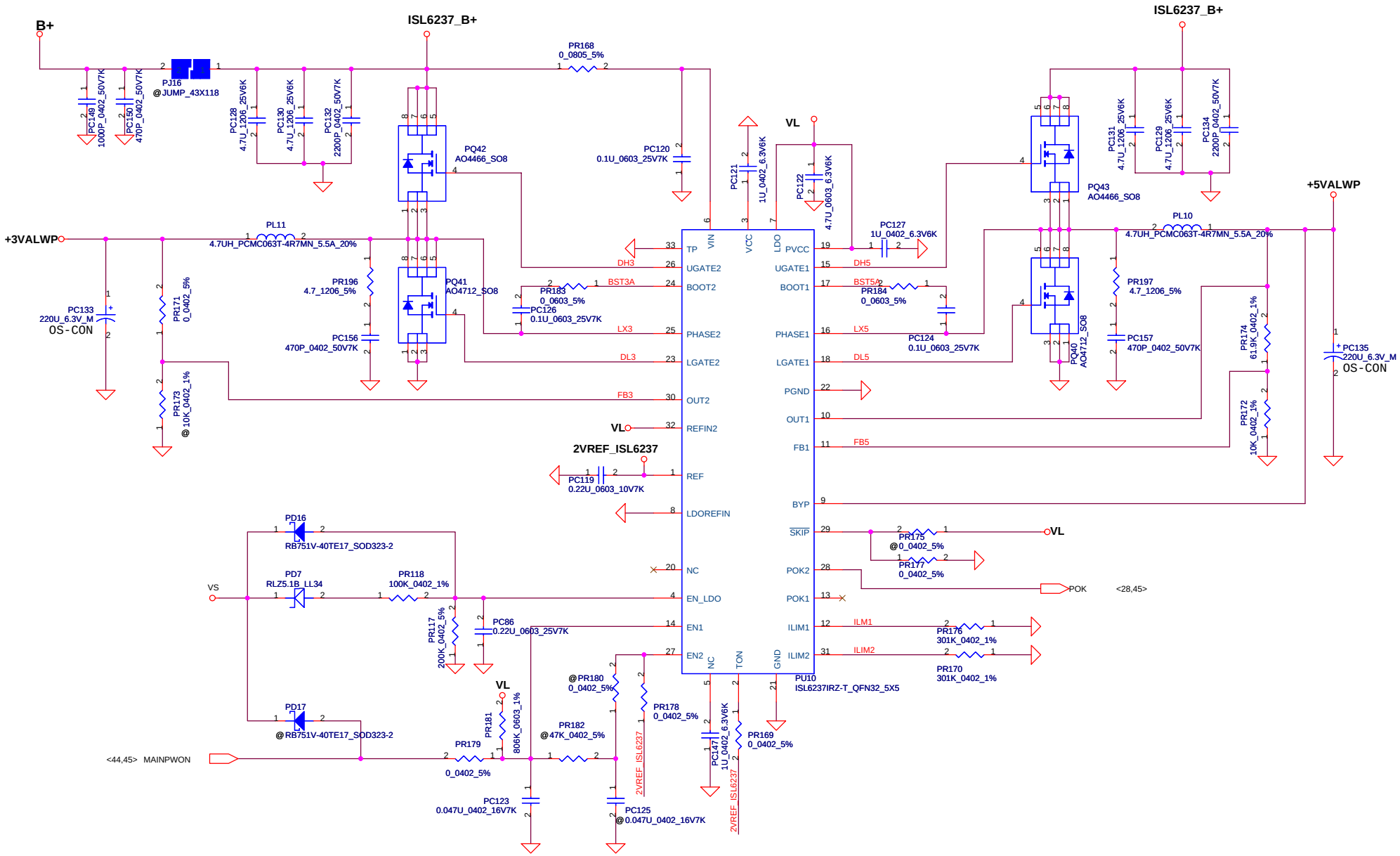
Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

Compal Electronics, Inc.

Title: CHARGER

Size: B | Document Number | Rev: 0.1

Date: Friday, May 02, 2008 | Sheet 46 of 52



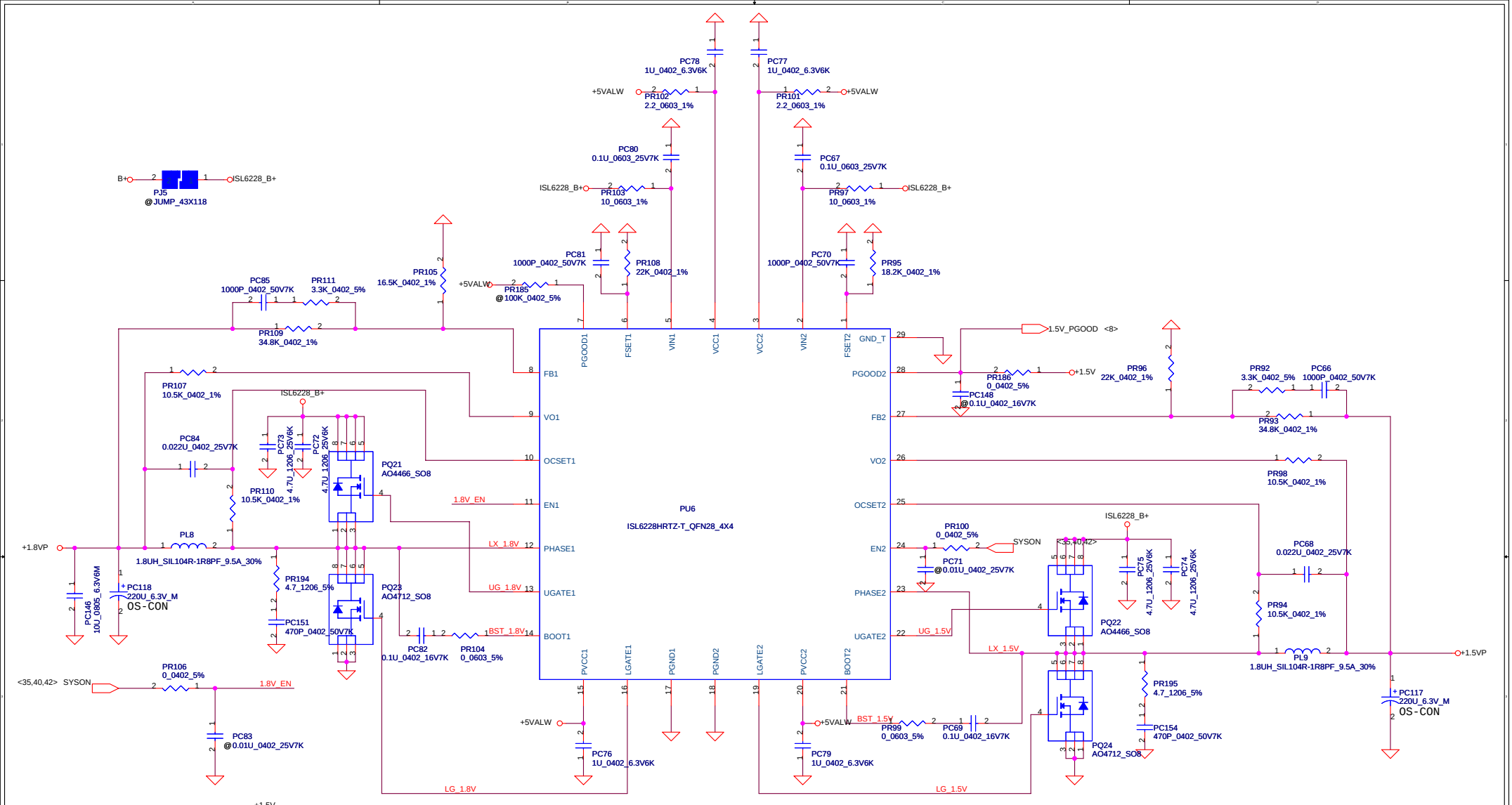
Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

Compal Electronics, Inc.

Title: +5V/+3V

Size: Custom | Document Number | Rev: 0.1

Date: Friday, May 02, 2008 | Sheet 47 of 52



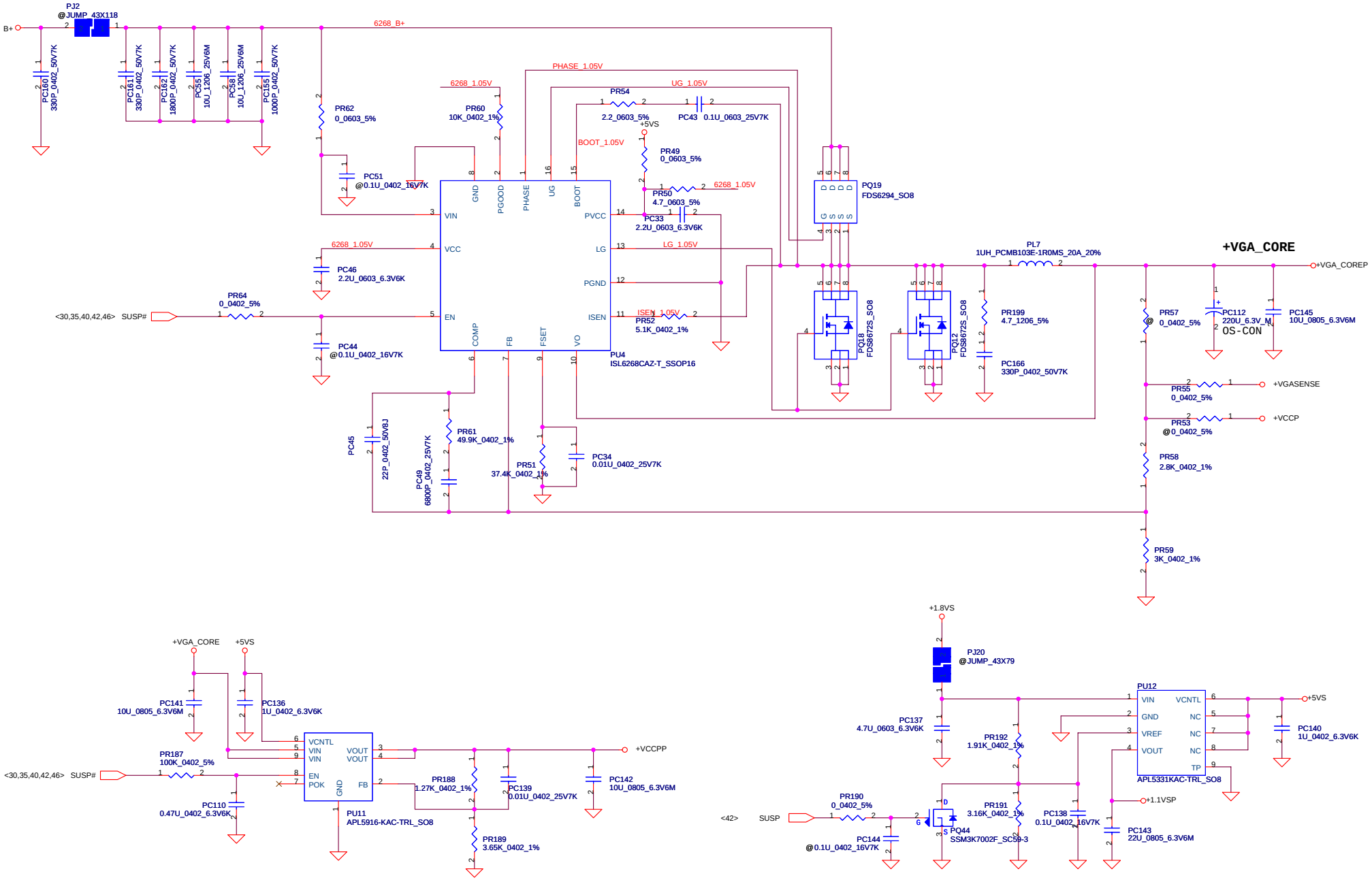
Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

Compal Electronics, Inc.

Title: 1.8V / 1.5V.0.75V

Size	Document Number	Rev
		0.1

Date: Friday, May 02, 2008 | Sheet 48 of 52



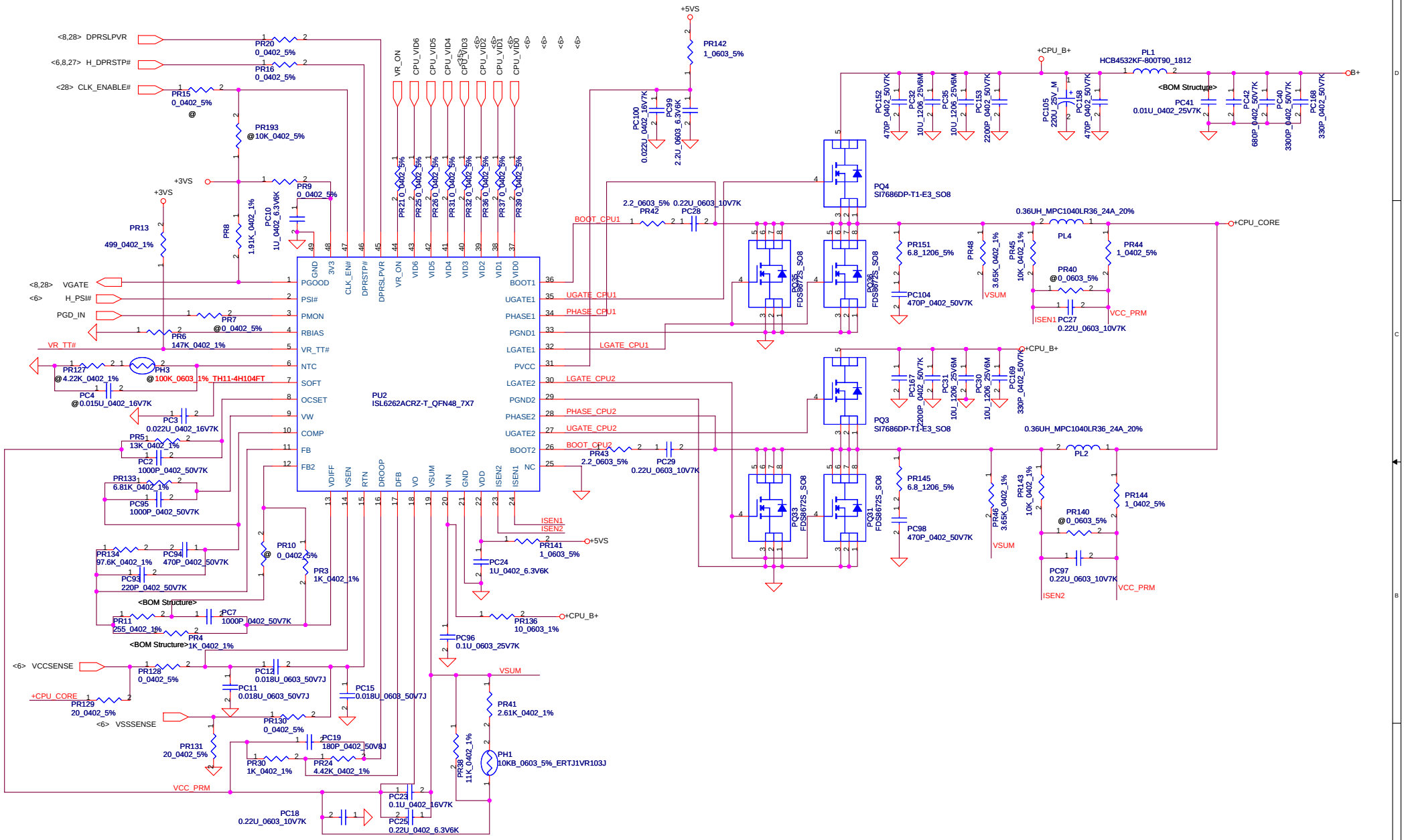
Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: VGA_CORE/VCCP/1.1V

Size	Document Number	Rev
		0.1

Date: Friday, May 02, 2008 | Sheet 49 of 52



Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: +CPU_CORE

Size	Document Number	Rev
Custom		0.1

Date: Friday, May 02, 2008 | Sheet 50 of 52

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	10/12	P48	Add PR185, PR186	Reserve for debug use.
	10/12	P49	Delete PC110	Because HW reserve enough CAP.
	10/17	P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
	10/17	P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V
	11/02	P49	Add PU12, PR190, PR191, PR192, PC137, PC138, PC140, PC143, PC144, PQ44	HW request add VCCIO(1.1V) for VGA use.
	11/12	P47	Add PD16, PD17	To solve 3/5VALW reboot after remove AC.
	11/21	P49	Add PC145	To reduce VGA_CORE ripple.
	11/21	P49	Change PR51 from 44.4k to 37.4k.	To change VGA_CORE frequence to 350KHz
	12/03	P48	Add PC146	To reduce 1.8VP ripple.
	12/03	P47	Add PC147	To reserve for 3/5V IC 2nd source.
	12/17	P48	Change PR105 from 16.9k_0402_1% to 16.5k_0402_1%, PR96 from 16.9k_0402_1% to 22k_0402_1%, PR93 from 25.5k_0402_1% to 34.8k_0402_1%.	Adjust 1.5V to 1.549V, 1.8V to 1.8V to 1.865V
	12/17	P48	Add PC148.	Reserve for HW adjust power sequence.
	12/27	P47, P48, P49, P50	Add PC149, PC150, PC152, PC153, PC155, PC151, PC154, PC156, PC157, PC158, PR194, PR195, PR196, PR197	For EMI request, to decrease power broadband.
	12/31	P49	Change PR58 from 2.8k_0402_1% to 3k_0402_1% PR188 from 1.27k_0402_1% to 1.4k_0402_1%.	For intel request, ES2 NB need adjust VCCP to 1.1V.
	02/29	P46	Add PR198, PC159.	Reserve charger sunbber.
	02/29	P46	Change PR192 from 1.87k_0402_1% to 1.91k_0402_1%.	HW request adjust 1.1V to 1.12V.
	02/29	P49	Change PR64 from 0_0402_5% to 100k_0402_1%, PC44 to 0.47u.	HW adjust power sequence.
	03/11	P44, 46, 49	Add PC160, PC161, PC162, PC163, PC164, PC165.	EMI requesst to solve power broadband.
	03/12	P49	Add PR199, PC166.	Reserve charger sunbber.
	03/11	P44, 46, 49	Add PC160, PC161, PC162, PC163, PC164, PC165.	EMI requesst to solve power broadband.
	03/12	P49	Add PR199, PC166.	Reserve charger sunbber.
	04/29	P50	Add PC167, PC168, PC169	For EMI request, to decrease power broadband.

Security Classification	Compal Secret Data		
Issued Date	2005/06/01	Deciphered Date	2006/06/01

Compal Electronics, Inc.			
Title: Power PIR			
Size	Document Number: LA-4141P		Rev: 0.1
Date: Tuesday, April 29, 2008		Sheet 51 of 51	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	11/12	P24	Change LVDS1 & LVDS2 connect type	
	11/12	P23	Change HDMI channel	
	11/12	P30	Change MDC connect JP8 , Add JP24	
	11/14	P16	Remove R492, R490, R489 & R491 (I2C pull- up resistor) ,Remove R66 (HDCP)	
	11/14	P16	Unstaff R486, R487, R483, R195, R192, R172, R106, R171, C116 & C183 (unused DACB & DACC)	
	11/14	P17	Remove R499 (FB commend14)	
	11/14	P17	Unstaff R87, R90 & C90 (FB_VREF)	
	11/14	P31	MIC P/N CHANGE FROM CY000000S00 TO CYWM64P0110	
	11/15	P18	Add pull down 10kohm (single LVDS signal)	
	11/15	P36	Update U32 for card reader power SW (SA000024X00)	
	11/22	P32	Add D24 , R526 (add WIMAX_LED# of JP22 JP23 42PIN)	
	11/22	P32	delete C737,C735,708,705,C682,C681,680 (for 3G issue)	
	12/05	P23	ADD R636 IN TMDS_B_HPD#	
	12/11	P8	DELETE R502,R498,RR160 (DELETE DDR2 FUNCTION)	
	12/11	P11	R186 CHANGE FROM 0603 TO 0805	
	12/11	P28	ADD R638 CONNECT "WOL_EN" TO 3VALW	
	12/17	P28	GPIO49 add 1k Ohm pulled-down resistor	
	12/17	P7	REMOVE C41	
	12/21	P5	U5 CHANGE FROM ADI TO SMSC (SA00001Z700)	
	12/21	P10	UMA HDMI TMDS CHANGE FROM C306 TO R640 (0OHM)	
	12/21	P16	ADD External Spread Spectrum (ADD U3,R55,C66,R48;DEL R99,R100)	
	12/26	P30	ADD R653,R654 TO EXTERNAL MIC	
	12/27	P43	CHANGE KILL SW POWER FOR +3VS TO +3VALW	
	12/31	P16	UPDATE VGA_HDMI_SCL,VGA_HDMI_SDA FROM I2CD TO I2CE	
	2/13	P8	CHANGE R147 FROM 511ohm TO 499ohm 1%	
	2/13	P23	CHANGE THE D4 LOCATION	
	2/13	P23	ADD D25,D26	
	2/13	P25	ADD D27,D28,D29	
	2/14	P38	CHANGE LED	
	2/14	P29	CHANGE R558,R582 FROM 10ohm TO 100ohm	
	2/14	P29	CHANGE C728,C738 FROM 0.1uF TO 0.1uF	
	2/14	P32	JP22,JP23 PIN37,PIN43 CONNECT TO GROUND	
	2/14	P23	DELETE LEVEL SHIFT CIRCUIT	
	2/14	P23	ADD R659	
	3/3	P10	REMOVE R240,R235 (GHCH_CRT_HSYNC,GHCH_CRT_VSYNC)	
	3/3	P11	REMOVE R186 (+VCCP_PEG)	
	3/3	P11	+1.5VS_TVDAC PULL DOWN	
	3/3	P28	TO USE THE RSMRST CIRCUIT	
	3/3	P28	ADD C804,C805,C806,C807 (ESD REQUESTION)	
	3/17	P16	CHANGE R69,R71 FROM 10Kohm TO 2.2Kohm	
	4/18	P36	change L41,L42 from L to 0ohm	
	5/2	P5	ADD R667,C810 FOR FAN solution RC (R=1Kohm,C=10nF)	
	5/2	P30	ADD R668,C811,R669 FOR MIC solution RC (R=1Kohm,C=10uF) , INT_MIC CONNECT TO U15 PIN23	
	5/2	P42	ADD R670,R671,R672 FOR AO4468 VGS ISSUE solution	

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