1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J41 MLB SCHEMATIC 6.6.0
DVT
4/09/13

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9795	1	SCHEM,MLB,J41	SCH	CRITICAL	
820-3435	1	PCBF,MLB,J41	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Apr 9 19:41:45 2013

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 1 OF 120
SHEET: 1 OF 73

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,MLB_MISC,MLB_DEBUG:ENG,MLB_PROGPARTS
MLB_MISC	PP5V5_DCIN:NO,TBTHV:P15V,EDP,CAM_XTAL:NO,CAM_WAKE:NO,APCLKRQ:ISOL,TPAD_INTWAKE:SHARED,USB_PWR:S3,SD_ON_MLB,VCORE_FETS
MLB_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,DDRVREF_DAC,S0PGOOD_ISL,DBGLED,ISNS:ENG
MLB_DEVEL:PVT	XDP_CONN
MLB_DEBUG:ENG	DEVEL_BOM,XDP,LPCPLUS
MLB_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,XDP,LPCPLUS,ISNS:PROD
MLB_DEBUG:PROD	BKLT:PROD,LPCPLUS,XDP,ISNS:PROD

Current Sensor Configuration

BOM GROUP	BOM OPTIONS
ISNS:ENG	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,P1V05_ISNS:YES,AIRPORT_ISNS:YES,SSD_ISNS:YES,LCDBKLT_ISNS:YES,P3V3SS_ISNS:YES,3V3S0_ISNS:YES,OTHER_HS_ISNS:YES,CAM_ISNS:YES,CPUDDR_ISNS:YES,PANEL_ISNS:YES
ISNS:PROD	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,P1V05_ISNS:NO,AIRPORT_ISNS:NO,SSD_ISNS:YES,LCDBKLT_ISNS:NO,P3V3SS_ISNS:NO,3V3S0_ISNS:NO,OTHER_HS_ISNS:NO,CAM_ISNS:NO,CPUDDR_ISNS:NO,PANEL_ISNS:NO

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:MICRON_4GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:MICRON_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2X3QFN	U2890	CRITICAL	TBTROM:BLANK
341S3802	1	IC,EEPROM,C/R (V23.4) EVT,J41/J41	U2890	CRITICAL	TBTROM:PROG
338S1159	1	IC,SMC12-A3,40MHZ/50DMIPS MCU,9X9,157BGA	U5000	CRITICAL	SMC:BLANK
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_NUM:BLANK
341S3809	1	IC,EFI ROM (V0071) DVT,J41/J43	U6100	CRITICAL	BOOTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4525	1	HSW,SR16M,PRQ,C0,1.3,15W,2+3,1.0,3M,BGA	U0500	CRITICAL	CPU:1.3GHZ
337S4526	1	HSW,SR16L,PRQ,C0,1.4,15W,2+3,1.1,3M,BGA	U0500	CRITICAL	CPU:1.4GHZ
337S4528	1	HSW,SR16H,PRQ,C0,1.7,15W,2+3,1.1,4M,BGA	U0500	CRITICAL	CPU:1.7GHZ
338S1113	1	IC,TBT,CR-4C,B1,PRQ,CIO,288,12X12 FC-CSP	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CAMERA PROCESSOR	U3900	CRITICAL	
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	J41_MLB
946-3892	1	J11/J13 MLB DYMAX ADHESIVE 29993-SC 0.4G	GLUE	CRITICAL	
825-7670	1	LABEL,TEXT,MLB,K21/K78	LABEL		
376S0964	2	MOSFET,N-CH,25V,30A,9.6M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S1104	2	MOSFET,N-CH,25V,30A,6.1M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN
376S1173	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1174	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
900-0090	1		SOLDERPASTE	CRITICAL	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0681	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0676	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0680	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0678	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0666	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0679	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:MICRON_4GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1032	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S0586	152S1301		ALL	Dale/Vishay alt to Cyntec
372S0186	372S0185		ALL	NXP alt to Diodes
197S0479	197S0478		ALL	200uW Epson alt to NDK
376S1053	376S0604		ALL	Diodes alt to Fairchild
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0371	128S0376		ALL	Kemet alt to Sanyo
128S0394	128S0415		ALL	NEC alt to Sanyo
152S1821	152S1757		ALL	Cyntec alt to NEC
197S0480	197S0343		ALL	NDK crystal alt to TXC
197S0481	197S0343		ALL	Epson crystal alt to TXC
107S0254	107S0241		ALL	Cyntec sense R alt to TFT
353S3452	353S1286		ALL	Maxim alt to Microchip
128S0386	128S0284		ALL	Kemet alt to Sanyo
128S0397	128S0325		ALL	Kemet alt to Sanyo
377S0155	377S0104		ALL	OnSemi alt to Infineon
128S0398	128S0220		ALL	Kemet alt to Sanyo
197S0542	197S0544		ALL	NDK alt to TXC
197S0545	197S0544		ALL	Epson alt to TXC
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0841	138S0638		ALL	Murata alt to Samsung
376S1180	376S0761		ALL	Renesas alt to Vishay
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cyntec alt to TFT
107S0250	107S0248		ALL	Cyntec alt to TFT

SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-4118	PCBA,MLB,BEST,HY 4GB,J41:	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-4274	PCBA,MLB,BEST,HY 8GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_8GB
639-4275	PCBA,MLB,BEST,EL 4GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-4276	PCBA,MLB,BEST,EL 8GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_8GB
639-4702	PCBA,MLB,BEST,MI 4GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:MICRON_4GB
639-4434	PCBA,MLB,BETTER,HY 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_4GB
639-4435	PCBA,MLB,BETTER,HY 8GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_8GB
639-4436	PCBA,MLB,BETTER,EL 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_4GB
639-4437	PCBA,MLB,BETTER,EL 8GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_8GB
639-4703	PCBA,MLB,BETTER,MI 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:MICRON_4GB
685-0024	CMN PTS,PCBA,MLB,J41	MLB_COMMON,J41_MLB
985-0017	J41 MLB DEVELOPMENT BOM	MLB_DEVEL:ENG
685-0062	VCORE FET,REN,J41	VCORE_FET:REN
685-0063	VCORE FET,VSHY,J41	VCORE_FET:VSHY

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,SMC:PROG,TBTROM:PROG

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3757	1	IC,SMC-A3 SCPL,EXT,V22.12A18,PROTO 1,J41	U5000	CRITICAL	SMC:PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-0062	685-0063		ALL	Renesas alt to Vishay
333S0704	333S0700		ALL	Elpida CAM DRAM alt to Hynix

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
985-0017	1	J41 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
685-0024	1	CMN PTS,PCBA,MLB,J41	CMNPTS	CRITICAL	MLB_CMNPTS
685-0063	1	VCORE FET,VSHY,J41	VCOREFETS	CRITICAL	VCORE_FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: BOM Variants

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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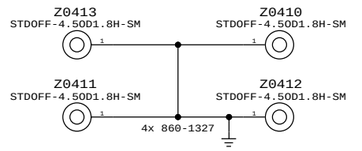
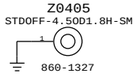
PD Module Parts

806-5107	1	CAN,TOPSIDE,ALT,J41/J43	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-5108	1	CAN,TOPSIDE,COVER,ALT,J41/J43	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
725-1792	1	INSULATOR,CPU,J41/J43	CPU_INSULATOR	CRITICAL	

CPU Heat Sink Mounting Bosses

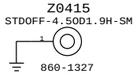


Fan Boss



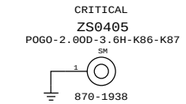
X21 Boss

SSD Boss

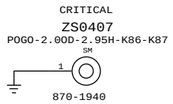


EMI I/O Pogo Pins

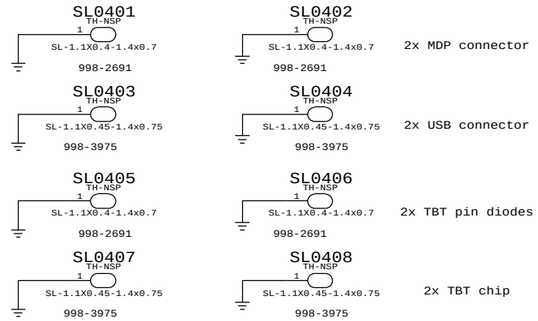
DisplayPort Pogo



USB/SD Card Pogo



Can Slots



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PAGE TITLE: PD Parts

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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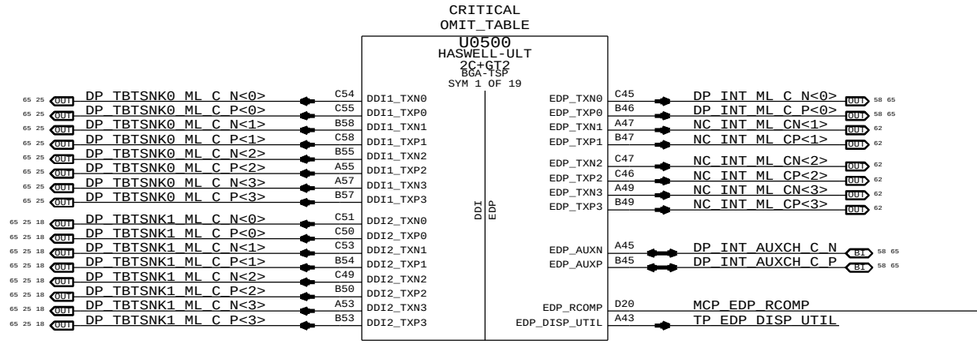
DDI Port Assignments:

TBT Sink 0

TBT Sink 1
(MUXed with HDMI
 if necessary)

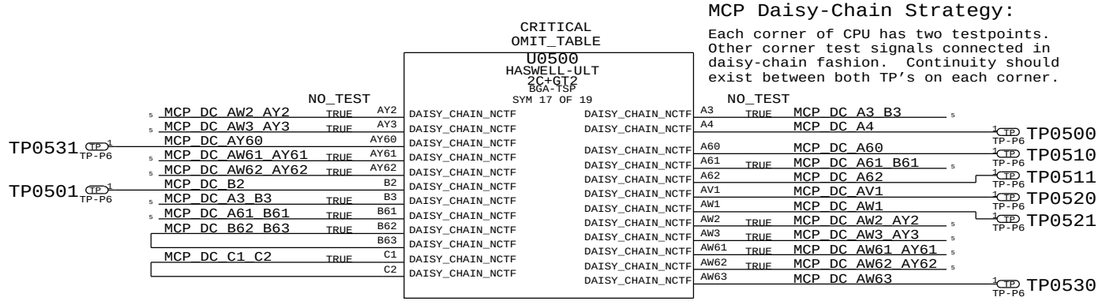


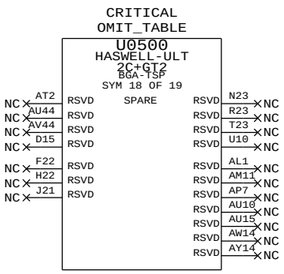
eDP Port Assignment:

Internal panel

MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints.
Other corner test signals connected in
daisy-chain fashion. Continuity should
exist between both TP's on each corner.





SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE: CPU GFX/NCTF/RSVD

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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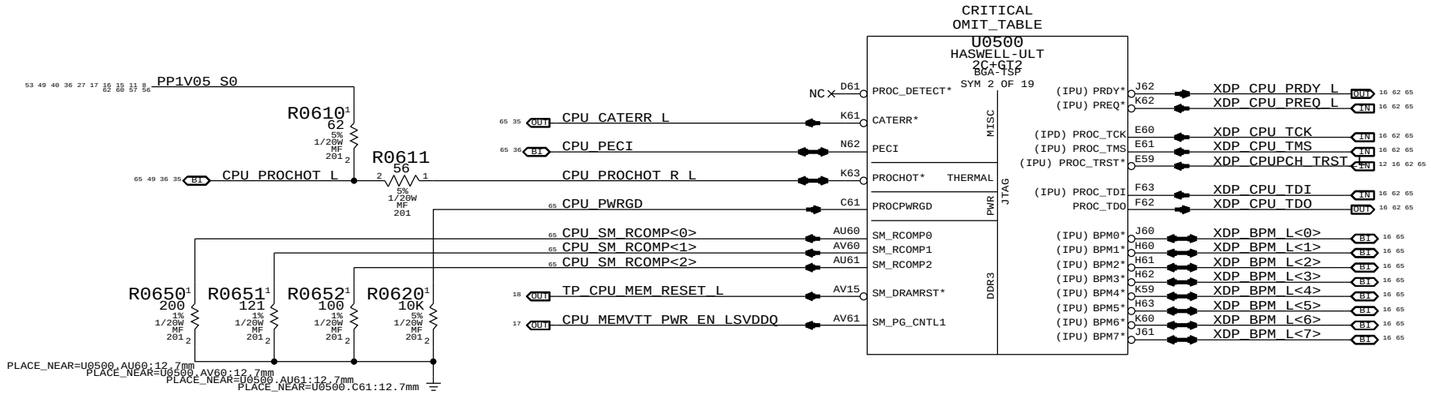
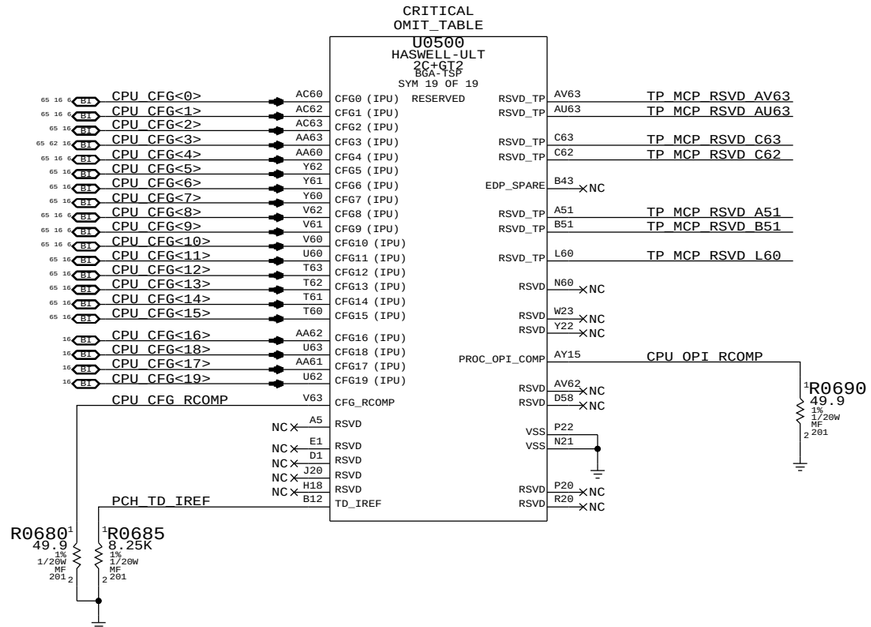
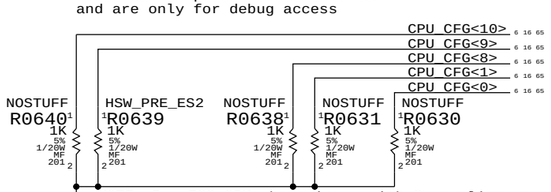


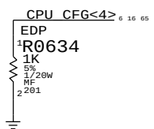


CFG<10>	:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9>	:NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8>	:ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4>	:eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1>	:PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0>	:RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



SYNC_MASTER=WILL_J43	SYNC_DATE=09/13/2012
PAGE TITLE	CPU Misc/JTAG/CFG/RSVD
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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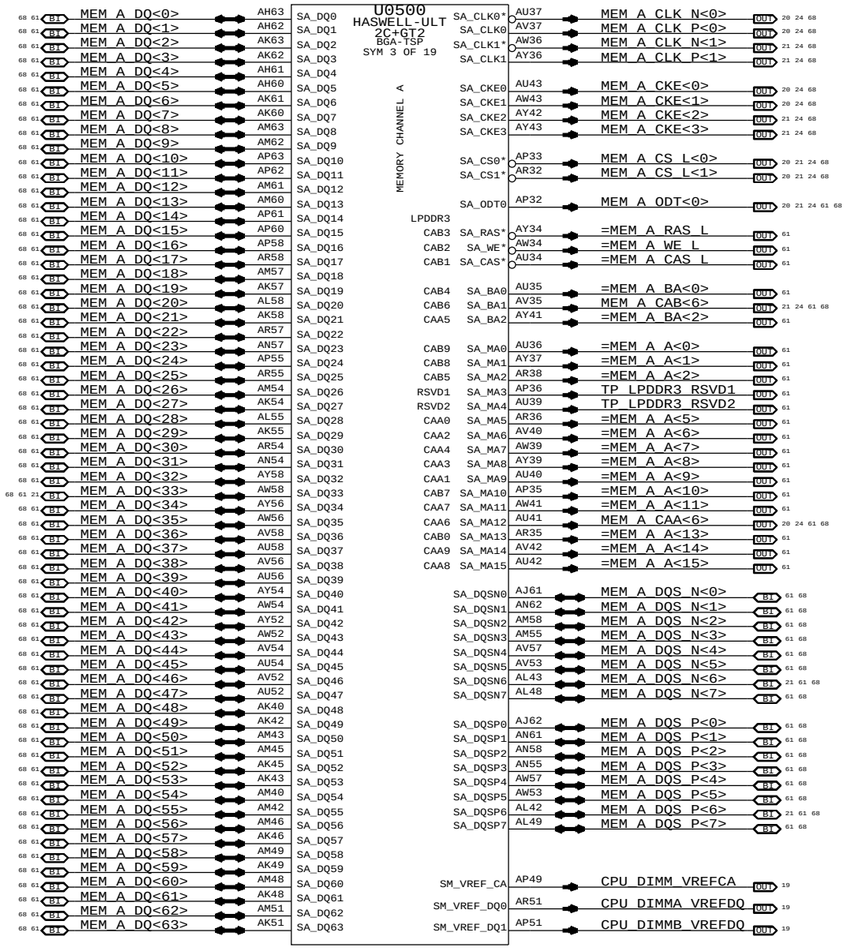

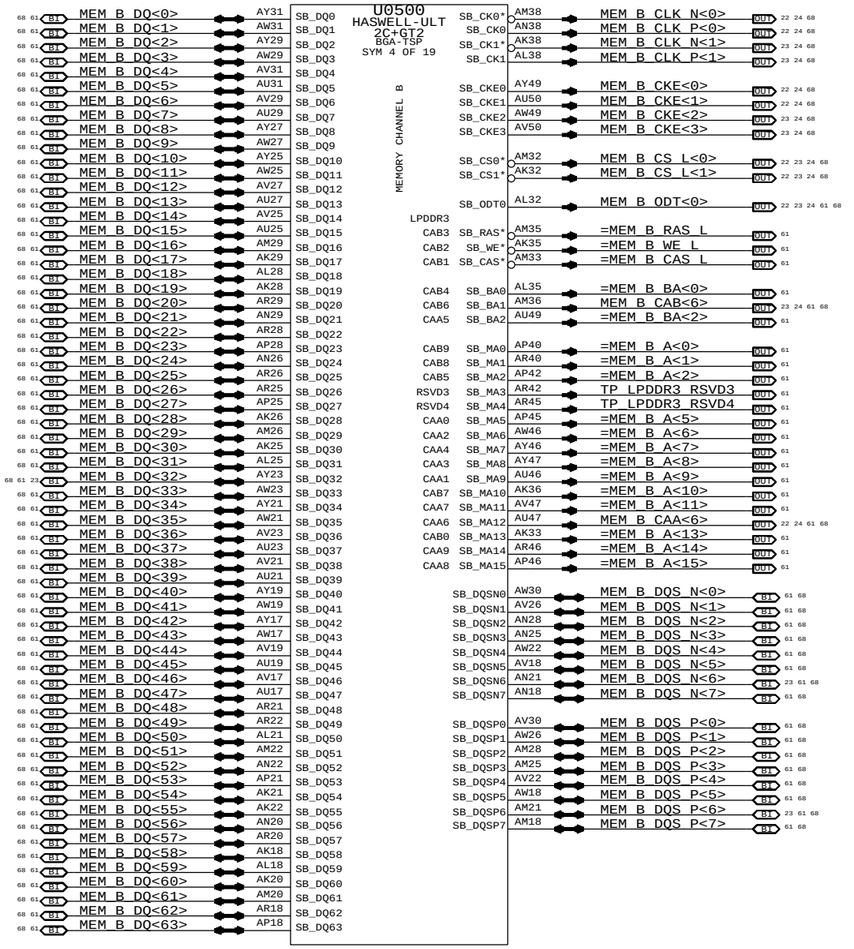

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE_TITLE
CPU DDR3/LPDDR3 Interfaces

Apple Inc.

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REVISION <E4LABEL>
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HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.

CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 12 OF 19
HSW ULT POWER

PPVCC_S0_CPU
32A Max

PPVMEMIO_S0_CPU
1.4A Max (DDR3: 1.5-1.35V)
1.1A Max (LPDDR3: 1.2V)

PPVCC_S0_CPU
R0860 100 5% 1/20W MF 201
PLACE_NEAR=U0500.C50:50.8mm

PP1V05_S0
R0800 75 1% 1/20W MF 201
R0802 130 1% 1/20W MF 201
Max load: 300mA
R0810 43 5% 1/20W MF 201
Max load: 300mA
R0811 0 5% 1/20W MF 0201
R0812 0 5% 1/20W MF 0201
R0802.2: PLACE_NEAR=U0500.L63:2.54mm
R0810.2: PLACE_NEAR=U0500.L62:38.1mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm

CPU_VCCSENSE_P
TP_PPVCCIO_S0_CPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
PPVCOMP_S0_CPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.

CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_VCCST_PWRGD
CPU_VR_EN
CPU_VR_READY
CPU_PWR_DEBUG
TP_CPU_RSVD_P60
TP_CPU_RSVD_P61
TP_CPU_RSVD_N59
TP_CPU_RSVD_N61

PP1V05_S0_SW_PCH_HSIO
1838mA Max
PP1V05_S0
29mA Max[1]
PP1V05_S0_SW_PCH_VCCUSB3PLL
41mA Max
PP1V05_S0_SW_PCH_VCCSATA3PLL
42mA Max
WF: RSVD on Sawtooth Peak rev 1.0
PP1V05_S0_PCH_VCCAPLL_OPI
57mA Max
PP1V5_S0SW_AUDIO_HDA
11mA Max
PP3V3_SUS
59mA Max[1]
PP3V3_S5
114mA Max
PP3V3_S0
40mA Max[1]
PP1V05_S0_PCH_VCC_ICC
VCCCLK: 200mA Max
PP1V05_S0_PCH_VCCACLKPLL
31mA Max
PP1V05_S0
VCCCLK: 200mA Max
WF: RSVD on Sawtooth Peak rev 1.0
PP3V3_SUS
3.3mA Max[1]

CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 13 OF 19
LPT LP POWER

PP3V3_SUS
0.3mA Max[1]
PPVRTC_G3H
PP1V05_S0
???mA Max
PPVOUT_S0_PCH_DCPRTC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
BYPASS=U0500.AE7:6.35mm
C0895 0.1UF 20% 10V CERM 402
PP3V3_SUS
18mA Max
C0892 0.1UF 20% 10V CERM 402
C0891 0.1UF 20% 10V CERM 402
C0890 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG10:6.35mm
BYPASS=U0500.AG10:6.35mm
PP1V05_S0
185mA Max[1]
PP1V05_S0
1499mA Max[1]
PLACE_NEAR=U0500.AG19:2.54mm
R0899 5.11 1% 1/20W MF-LF 201
PPVOUT_S5_PCH_DCPSUSBYP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
Powered in DeepSx
C0899 1UF 10% 6.3V CERM 402
BYPASS=R0899:U0500:2.54mm
PP1V05_S0
473mA Max[1]
PP1V5_S0
3mA Max
PP3V3_S0
1mA Max[1]
PP3V3_S0
17mA Max
WF: RSVD on Sawtooth Peak rev 1.0
PP1V05_S0
213mA Max[1]

SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012
PAGE TITLE: CPU/PCH POWER
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REVISION: <E4LABEL>
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CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
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A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
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AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
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D33	VSS	VSS	H17
D34	VSS	VSS	H57
D35	VSS	VSS	J10
D37	VSS	VSS	J22
D38	VSS	VSS	J59
D39	VSS	VSS	J63
D41	VSS	VSS	K1
D42	VSS	VSS	K12
D43	VSS	VSS	L13
D45	VSS	VSS	L15
D46	VSS	VSS	L17
D47	VSS	VSS	L18
D49	VSS	VSS	L20
D5	VSS	VSS	L58
D50	VSS	VSS	L61
D51	VSS	VSS	L7
D53	VSS	VSS	M22
D54	VSS	VSS	N10
D55	VSS	VSS	N3
D57	VSS	VSS	P59
D59	VSS	VSS	P63
D62	VSS	VSS	R10
D8	VSS	VSS	R22
E11	VSS	VSS	R8
E17	VSS	VSS	T1
F20	VSS	VSS	T58
F26	VSS	VSS	U20
F30	VSS	VSS	U22
F34	VSS	VSS	U61
F38	VSS	VSS	U9
F42	VSS	VSS	V10
F46	VSS	VSS	V3
F50	VSS	VSS	V7
F54	VSS	VSS	W20
F58	VSS	VSS	W22
F61	VSS	VSS	Y10
G18	VSS	VSS	Y59
G22	VSS	VSS	Y63
G3	VSS		
G5	VSS	VSS	V58
G6	VSS	VSS	AH46
G8	VSS	VSS	V23
H13	VSS	VSS_SENSE	E62
		VSS	AH16

CPU_VCCSENSE_N <OUT 49 65>

R0960
100
5%
1/20W
MF
201
PLACE_NEAR=U0500.E62:50.8mm

SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

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All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 1.0 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff

62 60 50 40 8 PPVCC_S0_CPU

NO STUFF C1000 10UF 20% 4V X6S 0402
NO STUFF C1001 10UF 20% 4V X6S 0402
NO STUFF C1002 10UF 20% 4V X6S 0402
NO STUFF C1003 10UF 20% 4V X6S 0402
NO STUFF C1004 10UF 20% 4V X6S 0402
NO STUFF C1005 10UF 20% 4V X6S 0402
NO STUFF C1006 10UF 20% 4V X6S 0402
NO STUFF C1007 10UF 20% 4V X6S 0402
NO STUFF C1008 10UF 20% 4V X6S 0402
NO STUFF C1009 10UF 20% 4V X6S 0402
NO STUFF C1010 10UF 20% 4V X6S 0402
NO STUFF C1011 10UF 20% 4V X6S 0402
NO STUFF C1012 10UF 20% 4V X6S 0402
NO STUFF C1013 10UF 20% 4V X6S 0402
NO STUFF C1014 10UF 20% 4V X6S 0402
NO STUFF C105A 10UF 20% 4V X6S 0402
CRITICAL C105B 10UF 20% 4V X6S 0402
CRITICAL C105C 10UF 20% 4V X6S 0402
NO STUFF C105D 10UF 20% 4V X6S 0402
NO STUFF C105E 10UF 20% 4V X6S 0402
CRITICAL C105F 10UF 20% 4V X6S 0402

NO STUFF C1015 10UF 20% 4V X6S 0402
NO STUFF C1016 10UF 20% 4V X6S 0402
NO STUFF C1017 10UF 20% 4V X6S 0402
NO STUFF C1018 10UF 20% 4V X6S 0402
NO STUFF C1019 10UF 20% 4V X6S 0402
NO STUFF C1020 10UF 20% 4V X6S 0402
NO STUFF C1021 10UF 20% 4V X6S 0402
NO STUFF C1030 10UF 20% 4V X6S 0402
NO STUFF C104A 10UF 20% 4V X6S 0402
NO STUFF C104B 10UF 20% 4V X6S 0402
NO STUFF C104C 10UF 20% 4V X6S 0402
CRITICAL C104D 10UF 20% 4V X6S 0402
NO STUFF C104E 10UF 20% 4V X6S 0402
CRITICAL C104F 10UF 20% 4V X6S 0402
CRITICAL C106A 10UF 20% 4V X6S 0402
NO STUFF C106B 10UF 20% 4V X6S 0402
NO STUFF C106C 10UF 20% 4V X6S 0402
NO STUFF C106D 10UF 20% 4V X6S 0402
NO STUFF C106E 10UF 20% 4V X6S 0402

CRITICAL C1070 10UF 20% 4V X6S 0402
CRITICAL C1071 10UF 20% 4V X6S 0402
NO STUFF C1072 10UF 20% 4V X6S 0402
NO STUFF C1073 10UF 20% 4V X6S 0402
NO STUFF C1074 10UF 20% 4V X6S 0402
NO STUFF C1075 10UF 20% 4V X6S 0402
CRITICAL C1076 10UF 20% 4V X6S 0402
CRITICAL C1077 10UF 20% 4V X6S 0402
NO STUFF C1078 10UF 20% 4V X6S 0402
NO STUFF C1079 10UF 20% 4V X6S 0402
NO STUFF C1080 10UF 20% 4V X6S 0402
NO STUFF C1081 10UF 20% 4V X6S 0402
NO STUFF C1082 10UF 20% 4V X6S 0402
CRITICAL C1083 10UF 20% 4V X6S 0402
CRITICAL C1084 10UF 20% 4V X6S 0402

CRITICAL C1085 10UF 20% 4V X6S 0402
CRITICAL C1086 10UF 20% 4V X6S 0402
CRITICAL C1087 10UF 20% 4V X6S 0402
NO STUFF C1088 10UF 20% 4V X6S 0402
NO STUFF C1089 10UF 20% 4V X6S 0402
NO STUFF C1090 10UF 20% 4V X6S 0402
CRITICAL C1091 10UF 20% 4V X6S 0402
CRITICAL C1092 10UF 20% 4V X6S 0402
NO STUFF C1093 10UF 20% 4V X6S 0402
NO STUFF C1094 10UF 20% 4V X6S 0402
NO STUFF C1095 10UF 20% 4V X6S 0402
NO STUFF C1096 10UF 20% 4V X6S 0402
CRITICAL C1097 10UF 20% 4V X6S 0402

NO STUFF C1022 10UF 20% 4V X6S 0402
NO STUFF C1023 10UF 20% 4V X6S 0402
NO STUFF C1024 10UF 20% 4V X6S 0402
NO STUFF C1025 10UF 20% 4V X6S 0402
NO STUFF C1026 10UF 20% 4V X6S 0402
NO STUFF C1027 10UF 20% 4V X6S 0402
NO STUFF C1028 10UF 20% 4V X6S 0402
NO STUFF C1029 10UF 20% 4V X6S 0402
NO STUFF C1032 10UF 20% 4V X6S 0402
NO STUFF C1033 10UF 20% 4V X6S 0402
NO STUFF C1034 10UF 20% 4V X6S 0402
NO STUFF C1035 10UF 20% 4V X6S 0402
NO STUFF C1036 10UF 20% 4V X6S 0402
NO STUFF C1037 10UF 20% 4V X6S 0402
NO STUFF C1038 10UF 20% 4V X6S 0402

NO STUFF C1039 10UF 20% 4V X6S 0402
NO STUFF C1044 10UF 20% 4V X6S 0402
NO STUFF C1045 10UF 20% 4V X6S 0402
NO STUFF C1046 10UF 20% 4V X6S 0402
NO STUFF C1047 10UF 20% 4V X6S 0402
NO STUFF C1048 10UF 20% 4V X6S 0402
NO STUFF C1049 10UF 20% 4V X6S 0402

NO STUFF C1056 10UF 20% 4V X6S 0402
NO STUFF C1057 10UF 20% 4V X6S 0402
NO STUFF C1058 10UF 20% 4V X6S 0402
NO STUFF C1059 10UF 20% 4V X6S 0402
NO STUFF C1062 10UF 20% 4V X6S 0402
NO STUFF C1063 10UF 20% 4V X6S 0402
NO STUFF C1064 10UF 20% 4V X6S 0402
NO STUFF C1065 10UF 20% 4V X6S 0402
NO STUFF C1066 10UF 20% 4V X6S 0402
NO STUFF C1067 10UF 20% 4V X6S 0402
NO STUFF C1068 10UF 20% 4V X6S 0402
NO STUFF C1069 10UF 20% 4V X6S 0402
NO STUFF C1098 10UF 20% 4V X6S 0402
NO STUFF C1099 10UF 20% 4V X6S 0402
NO STUFF C109A 10UF 20% 4V X6S 0402

NO STUFF C109B 10UF 20% 4V X6S 0402
NO STUFF C109C 10UF 20% 4V X6S 0402
NO STUFF C109D 10UF 20% 4V X6S 0402
NO STUFF C109E 10UF 20% 4V X6S 0402
NO STUFF C109F 10UF 20% 4V X6S 0402
NO STUFF C108A 10UF 20% 4V X6S 0402
NO STUFF C108B 10UF 20% 4V X6S 0402
NO STUFF C108C 10UF 20% 4V X6S 0402
NO STUFF C108D 10UF 20% 4V X6S 0402
NO STUFF C108E 10UF 20% 4V X6S 0402
NO STUFF C108F 10UF 20% 4V X6S 0402
NO STUFF C107A 10UF 20% 4V X6S 0402
NO STUFF C107B 10UF 20% 4V X6S 0402

CRITICAL C1031 470UF-0.0045OHM 20% 2.5V POLY-TANT SM

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 4x 2.2uF 0402, 6x 10uF 0402, 2x 270uF B2 no stuff

40 8 PPVMEMIO_S0_CPU

C1040 2.2UF 20% 6.3V CERM 402-LF
C1041 2.2UF 20% 6.3V CERM 402-LF
C1042 2.2UF 20% 6.3V CERM 402-LF
C1043 2.2UF 20% 6.3V CERM 402-LF

C1050 10UF 20% 6.3V CERM-X5R 0402-1
C1051 10UF 20% 6.3V CERM-X5R 0402-1
C1052 10UF 20% 6.3V CERM-X5R 0402-1
C1053 10UF 20% 6.3V CERM-X5R 0402-1
C1054 10UF 20% 6.3V CERM-X5R 0402-1
C1055 10UF 20% 6.3V CERM-X5R 0402-1

C1060 270UF 20% 2V TANT CASE-B2-SM
NO STUFF C1061 270UF 20% 2V TANT CASE-B2-SM

2x Bulk nostuff per Harris Beach v1.0 schematic

SYNC_MASTER=LABEL_J41 SYNC_DATE=01/11/2013
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BRANCH: <BRANCH>
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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5

NO STUFF
C1200 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH10:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS

NO STUFF
C1202 0.1UF 20% 25V CERM 402
BYPASS=U0500.Y8:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS

C1204 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.AC9:12.7mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS

C1206 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH11:6.35mm

PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0

C1208 1UF 10% 6.3V CERM 402
BYPASS=U0500.U8:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0SW_AUDIO_HDA

C1210 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0

C1212 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.V8:12.7mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0

C1214 0.1UF 20% 25V CERM 402
BYPASS=U0500.K14:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0

NO STUFF
C1250 22UF 20% 6.3V X5R-CERM-1 603
C1251 1UF 10% 6.3V CERM 402
BYPASS=U0500.AE9:12.7mm
BYPASS=U0500.AE9:6.35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0

C1255 10UF 20% 6.3V X5R 603
C1256 1UF 10% 6.3V CERM 402
C1257 1UF 10% 6.3V CERM 402
BYPASS=U0500.J11:12.7mm
BYPASS=U0500.J11:6.35mm
BYPASS=U0500.AE8:6.35mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
PP1V05_S0SW_PCH_HSIO

C1260 1UF 10% 6.3V CERM 402
C1261 1UF 10% 6.3V CERM 402
C1262 10UF 20% 6.3V CERM-X5R 0402-1
BYPASS=U0500.K9:6.35mm
BYPASS=U0500.L10:6.35mm
BYPASS=U0500.M9:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0

C1264 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG16:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0

C1266 1UF 10% 6.3V CERM 402
C1267 1UF 10% 6.3V CERM 402
BYPASS=U0500.J17:6.35mm
BYPASS=U0500.R21:6.35mm

PP1V05_S0
??mA Max

R1270 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603

PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max

C1270 47UF 20% 4V CERM-X5R 0805-1
C1271 47UF 20% 4V CERM-X5R 0805-1
C1272 1UF 10% 10V X5R 402
BYPASS=U0500.A20:12.7mm
BYPASS=U0500.A20:12.7mm
BYPASS=U0500.A20:6.35mm

R1275 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603

PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max

C1275 47UF 20% 4V CERM-X5R 0805-1
C1276 47UF 20% 4V CERM-X5R 0805-1
C1277 1UF 10% 10V X5R 402
BYPASS=U0500.J18:12.7mm
BYPASS=U0500.J18:12.7mm
BYPASS=U0500.J18:6.35mm

R1280 0 5% 1/16W MF-LF 402

CRITICAL
NO STUFF
L1280 2.2UH-240MA-0.221OHM 0603

PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max

NO STUFF C1280 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1281 47UF 20% 4V CERM-X5R 0805-1
C1282 1UF 10% 10V X5R 402
BYPASS=U0500.AA21:12.7mm
BYPASS=U0500.AA21:12.7mm
BYPASS=U0500.AA21:6.35mm

PP1V05_S0SW_PCH_HSIO
83mA Max

CRITICAL
L1290 2.2UH-240MA-0.221OHM 0603

PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max

NO STUFF C1290 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1291 47UF 20% 4V CERM-X5R 0805-1
C1292 1UF 10% 10V X5R 402
BYPASS=U0500.B11:12.7mm
BYPASS=U0500.B11:12.7mm
BYPASS=U0500.B11:6.35mm

CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603

PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max

NO STUFF C1295 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1296 47UF 20% 4V CERM-X5R 0805-1
C1297 1UF 10% 10V X5R 402
BYPASS=U0500.B18:12.7mm
BYPASS=U0500.B18:12.7mm
BYPASS=U0500.B18:6.35mm

LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE: PCH Decoupling

Apple Inc.

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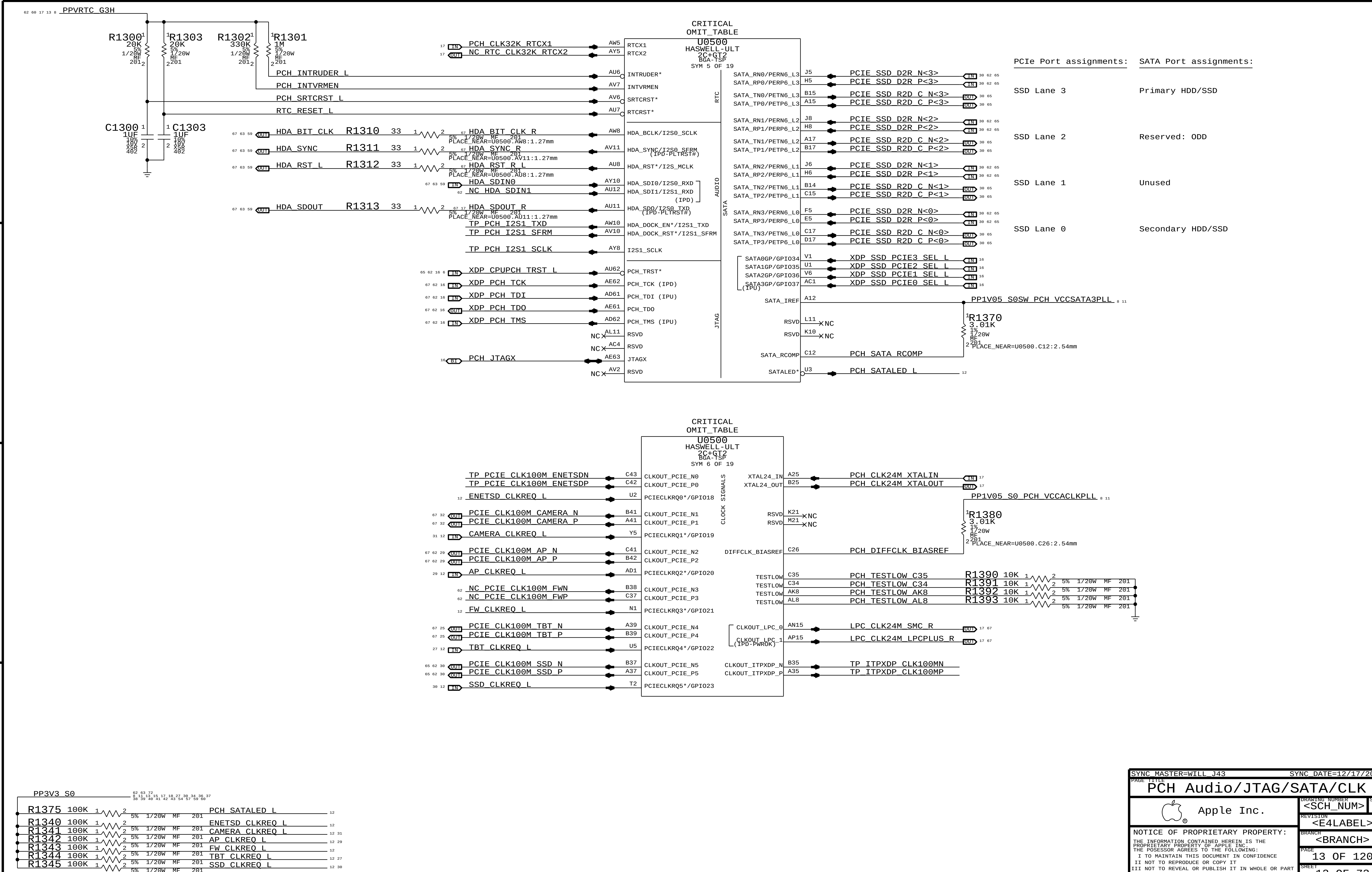

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE

PCH Audio/JTAG/SATA/CLK

Apple Inc.

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REVISION <E4LABEL>

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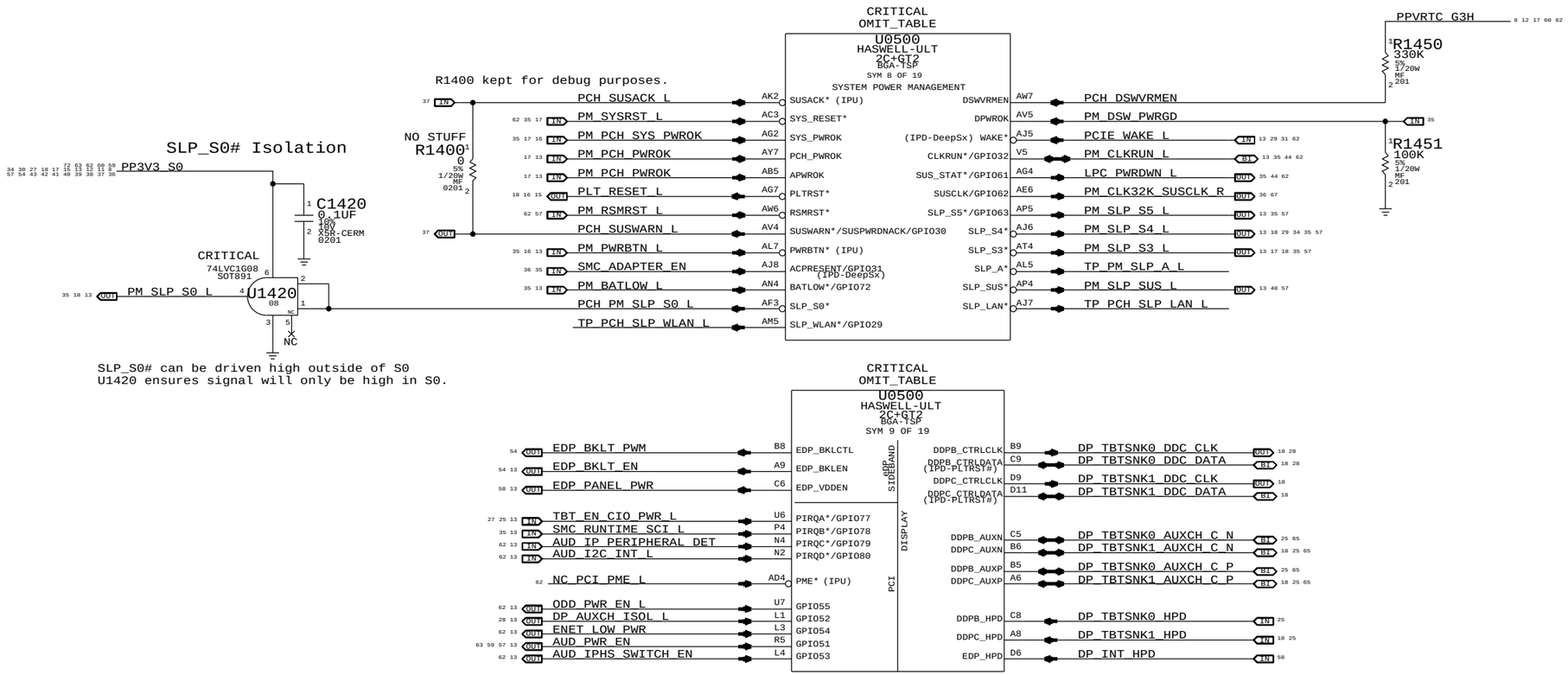

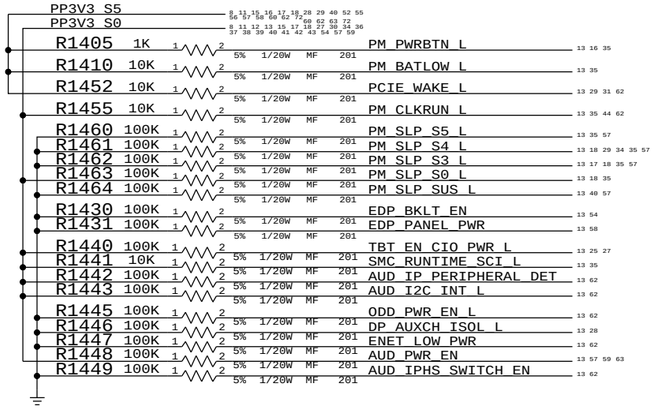

SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE
PCH PM/PCI/GFX

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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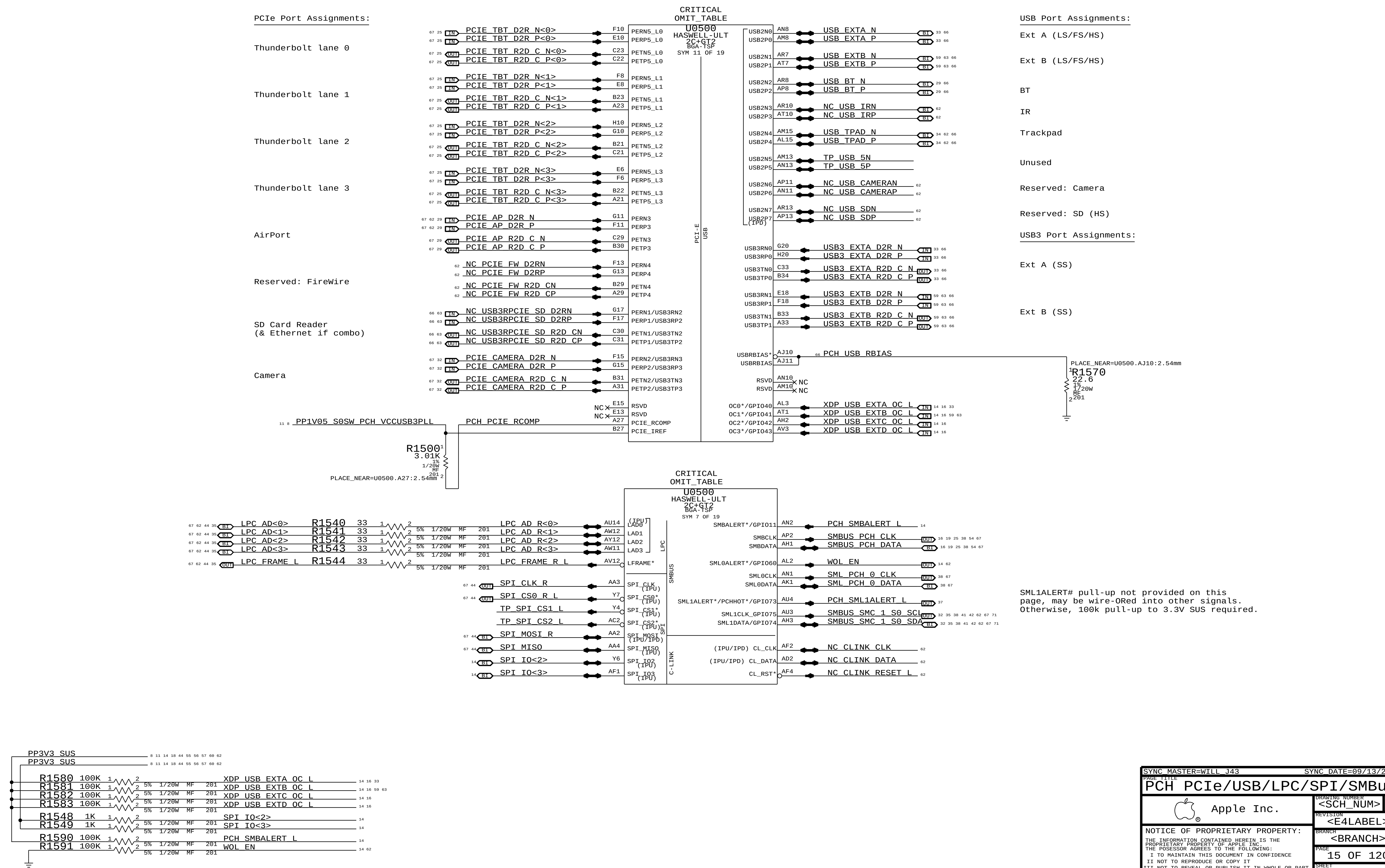


SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

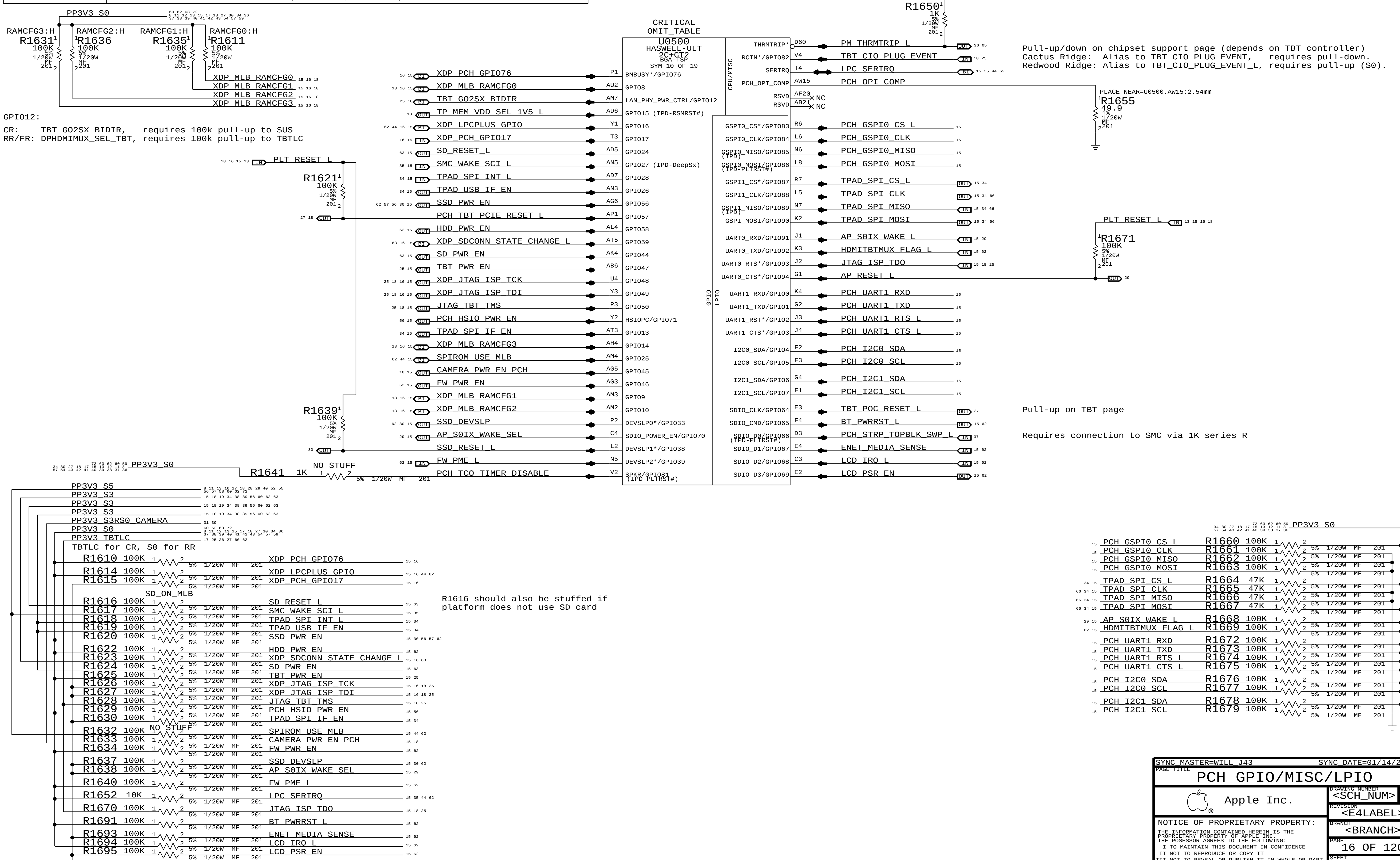
REVISION <E4LABEL>

BRANCH <BRANCH>

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

GPIO12:
CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).



SYNC_MASTER=WILL_J43 SYNC_DATE=01/14/2013

PAGE TITLE
PCH GPIO/MISC/LPIO

Apple Inc.

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BRANCH <BRANCH>

Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807
(TP-P6)

Merged (CPU/PCH) Micro2-XDP

PP1V05_S0

R1830 150 5% 1/16W MF-LF 402

CRITICAL XDP_CONN J1800 DF40RC-60DP-0.4V M-ST-SM1

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	XDP_CPU_PRESENT_L

518S0847

C1804 0.1UF 10V X5R-CERM 0201
C1800 0.1UF 10V X5R-CERM 0201
C1801 0.1UF 10V X5R-CERM 0201
C1806 0.1UF 10V X5R-CERM 0201
R1831 1K 5% 1/16W MF-LF 402

CPU_VCCST_PWRGD → R1800 1K 5% 1/20W MF 201 (PLACE_NEAR=U0500.C61:2.54mm)
PM_PWRBTN_L → R1802 0 5% 1/20W MF 0201 (PLACE_NEAR=U5000.J3:2.54mm)
PM_PCH_SYS_PWROK → R1804 0 5% 1/16W MF-LF 402
XDP_CPU_TCK
PCH_JTAGX → R1835 0 5% 1/20W MF 0201 (PLACE_NEAR=J1800.58:28mm)

PP1V05_S0 → R1810 51 5% 1/20W MF 201 (PLACE_NEAR=U0500.F62:28mm) → XDP_CPU_TDO
PP1V05_S0 → R1813 51 5% 1/20W MF 201 (PLACE_NEAR=U0500.E60:28mm) → XDP_CPU_TCK

TDI and TMS are terminated in CPU.

R1805 1K 5% 1/20W MF 201 (PLACE_NEAR=U0500.AG7:2.54mm): PLT_RESET_L → XDP_CPURST_L

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
XDP_CPU_TDO
XDP_CPUPCH_TRST_L
XDP_CPU_TDI
XDP_CPU_TMS

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563 (PLACE_NEAR=J1800.51:28mm)
CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563 (PLACE_NEAR=J1800.53:28mm)
CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563 (PLACE_NEAR=J1800.55:28mm)
CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563 (PLACE_NEAR=J1800.57:28mm)

XDP_CPUPCH_TRST_L (MAKE_BASE=TRUE) → XDP_CPUPCH_TRST_L, XDP_CPUPCH_TRST_L

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0	TP1870	
XDP_USB_EXTA_OC_L		XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L		XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	TP1873	
XDP_USB_EXTD_OC_L	TP1874	
XDP_SDCONN_STATE_CHANGE_L		XDP_SDCONN_STATE_CHANGE_L
XDP_MLB_RAMCFG1	TP1876	
XDP_MLB_RAMCFG2	TP1877	
XDP_MLB_RAMCFG3	TP1878	
XDP_JTAG_ISP_TCK		XDP_JTAG_ISP_TCK
XDP_SSD_PCIE3_SEL_L	R1881 1K	
XDP_SSD_PCIE2_SEL_L	R1882 1K	NOTE: Must not short XDP pins together!
XDP_SSD_PCIE1_SEL_L	R1883 1K	
XDP_SSD_PCIE0_SEL_L	R1884 1K	SSD_PCIE_SEL_L
XDP_LPCPLUS_GPIO		XDP_LPCPLUS_GPIO
XDP_PCH_GPIO17	TP1886	
XDP_PCH_GPIO76	TP1887	
XDP_JTAG_ISP_TDI		XDP_JTAG_ISP_TDI

(MAKE_BASE=TRUE on the non-XDP signals; R1881–R1884: 1K 5% 1/20W MF 201)

Unused & MLB_RAMCFGx GPIOs have TPs.
USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.
NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.
SSD_PCIEx_SEL_L straps are connected via 1K to common net.
LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
C1845 0.1UF 10V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, NC)
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

PCH_JTAGX	R1899 1K	NO STUFF
XDP_PCH_TDO	R1890 51	XDP
XDP_PCH_TDI	R1891 51	XDP
XDP_PCH_TMS	R1892 51	XDP
XDP_PCH_TCK	R1896 51	NO STUFF
XDP_CPUPCH_TRST_L	R1897 51	NO STUFF

(1K 5% 1/20W MF 201; 51 5% 1/20W MF 201)

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: CPU/PCH Merged XDP

Apple Inc.

DRAWING NUMBER: <SCH_NUM> D
REVISION: <E4LABEL>
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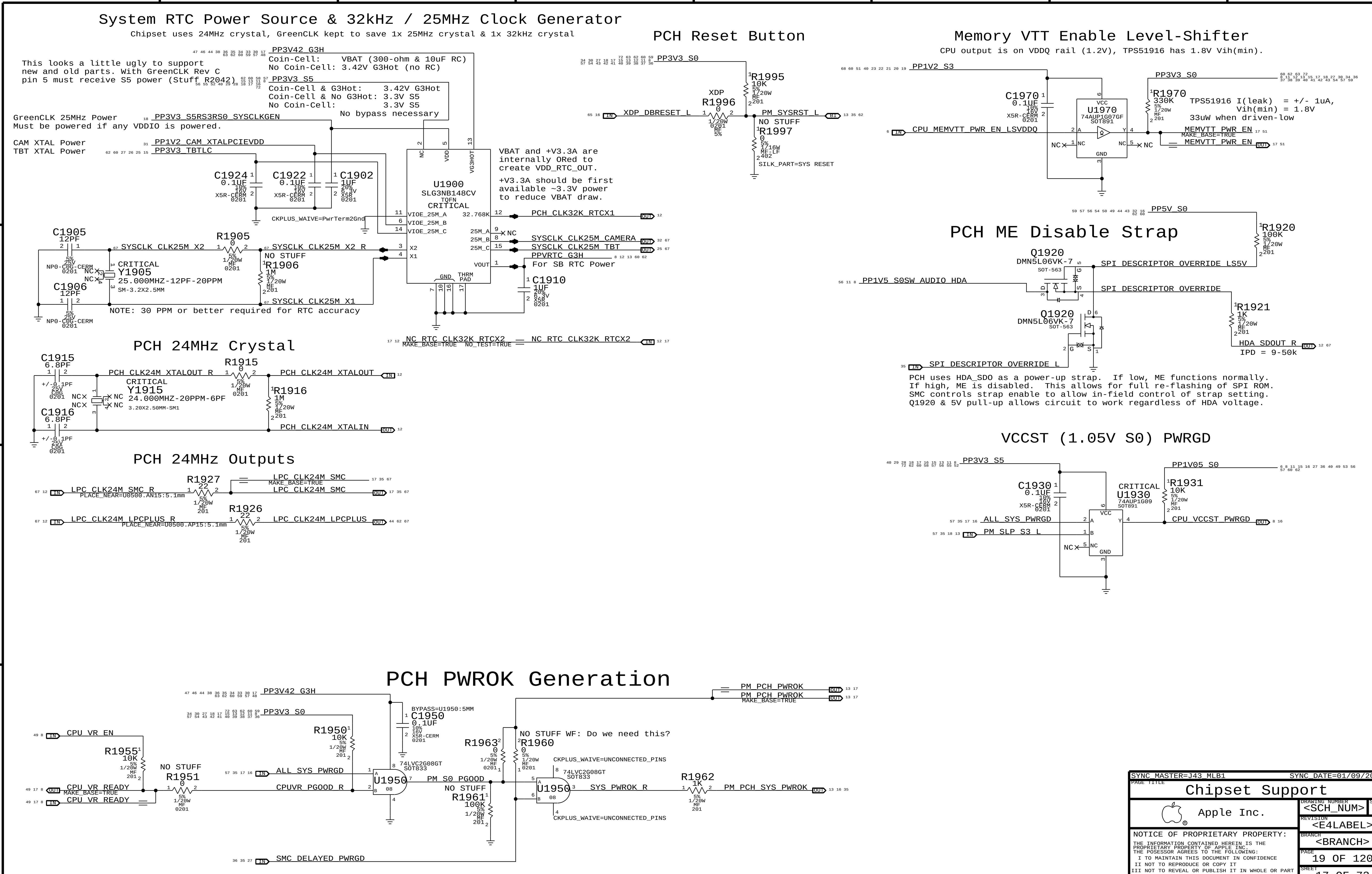
System RTC Power Source & 32kHz / 25MHz Clock Generator
Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal
This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042)
PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)
PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary
GreenCLK 25MHz Power
Must be powered if any VDDIO is powered.
PP3V3_S5RS3RS0_SYSCLKGEN
CAM XTAL Power
TBT XTAL Power
PP1V2_CAM_XTALPCIEVDD
PP3V3_TBTLC
VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.
+V3.3A should be first available ~3.3V power to reduce VBAT draw.
U1900
SLG3NB148CV
TQFN
CRITICAL
CKPLUS_WAIVE=PwrTerm2Gnd
PCH_CLK32K_RTCX1
SYSCLK_CLK25M_CAMERA
SYSCLK_CLK25M_TBT
PPVRTC_G3H
For SB RTC Power
SYSCLK_CLK25M_X2
SYSCLK_CLK25M_X2_R
SYSCLK_CLK25M_X1
NO STUFF
Y1905
25.000MHZ-12PF-20PPM
SM-3.2X2.5MM
NOTE: 30 PPM or better required for RTC accuracy
NC_RTC_CLK32K_RTCX2
MAKE_BASE=TRUE NO_TEST=TRUE
PCH 24MHz Crystal
PCH_CLK24M_XTALOUT_R
PCH_CLK24M_XTALOUT
PCH_CLK24M_XTALIN
Y1915
24.000MHZ-20PPM-6PF
3.20X2.50MM-SM1
PCH 24MHz Outputs
LPC_CLK24M_SMC_R
PLACE_NEAR=U0500.AN15:5.1mm
LPC_CLK24M_SMC
MAKE_BASE=TRUE
LPC_CLK24M_LPCPLUS_R
PLACE_NEAR=U0500.AP15:5.1mm
LPC_CLK24M_LPCPLUS
PCH Reset Button
PP3V3_S0
XDP
XDP_DBRESET_L
PM_SYSRST_L
NO STUFF
SILK_PART=SYS RESET
Memory VTT Enable Level-Shifter
CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).
PP1V2_S3
PP3V3_S0
TPS51916 I(leak) = +/- 1uA,
Vih(min) = 1.8V
33uW when driven-low
U1970
74AUP1G07GF
SOT891
CPU_MEMVTT_PWR_EN_LSVDDQ
MEMVTT_PWR_EN
MAKE_BASE=TRUE
PP5V_S0
PCH ME Disable Strap
Q1920
DMN5L06VK-7
SOT-563
SPI_DESCRIPTOR_OVERRIDE_LS5V
PP1V5_S0SW_AUDIO_HDA
SPI_DESCRIPTOR_OVERRIDE
HDA_SDOUT_R
IPD = 9-50k
SPI_DESCRIPTOR_OVERRIDE_L
PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.
VCCST (1.05V S0) PWRGD
PP3V3_S5
PP1V05_S0
CRITICAL
U1930
74AUP1G09
SOT891
ALL_SYS_PWRGD
PM_SLP_S3_L
CPU_VCCST_PWRGD
PCH PWROK Generation
PP3V42_G3H
PP3V3_S0
BYPASS=U1950:5MM
CPU_VR_EN
CPU_VR_READY
MAKE_BASE=TRUE
NO STUFF
ALL_SYS_PWRGD
CPUVR_PGOOD_R
U1950
74LVC2G08GT
SOT833
PM_S0_PGOOD
NO STUFF
NO STUFF WF: Do we need this?
CKPLUS_WAIVE=UNCONNECTED_PINS
SYS_PWROK_R
PM_PCH_SYS_PWROK
PM_PCH_PWROK
SMC_DELAYED_PWRGD

SYNC_MASTER=J43_MLB1 SYNC_DATE=01/09/2013

PAGE TITLE: Chipset Support

Apple Inc.

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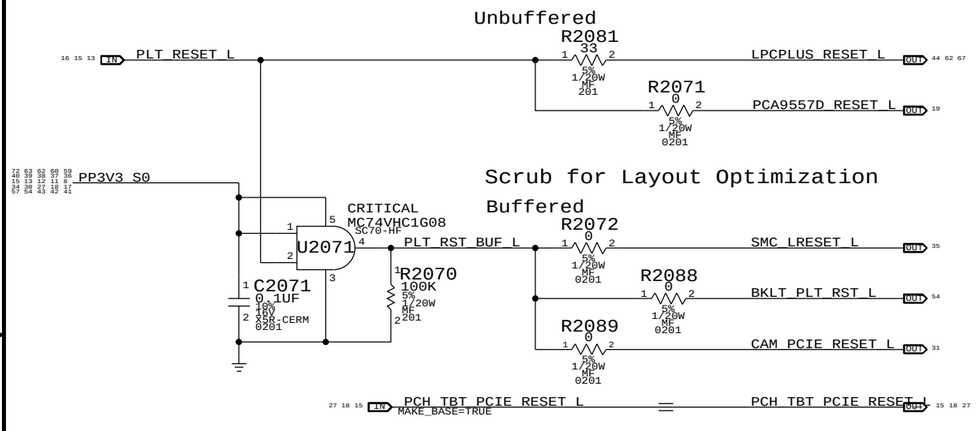
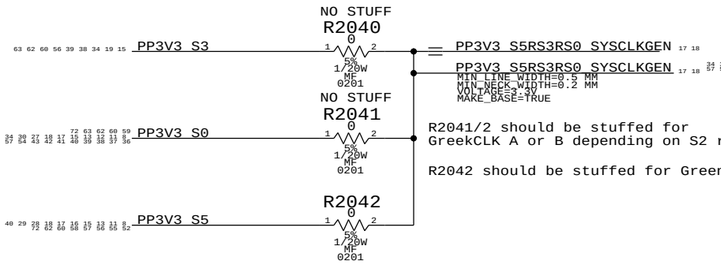
Platform Reset Connections



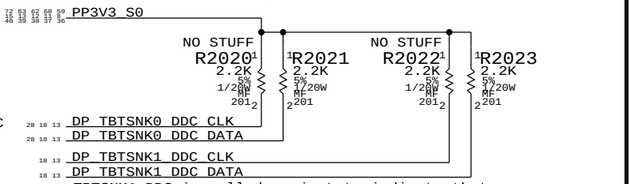
GreenCLK 25MHz Power



DDC Pull-Ups

2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

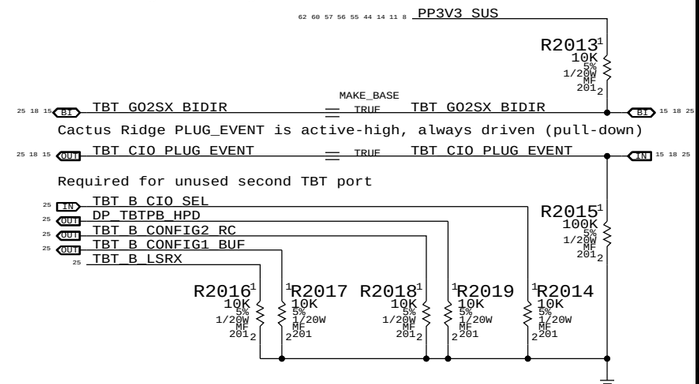


TBTSNK1_DDC is pulled-up just to indicate that
DP port is used. No DDC on this port, AUX-only.

NOTE: Only DDC_DATA is sensed by PCH, so
DDC_CLK pull-ups are unstuffed.

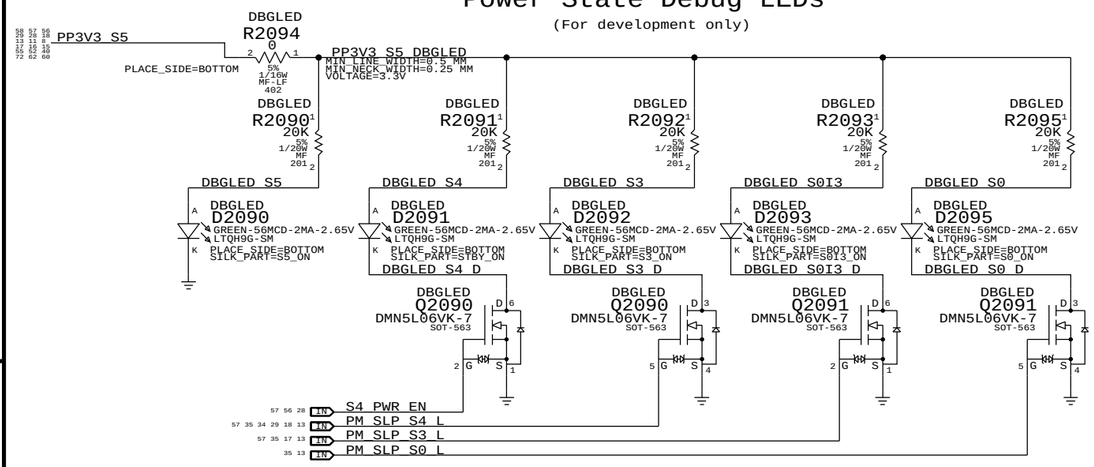
Thunderbolt Pull-up/downs

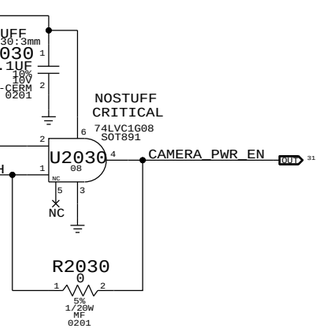
Cactus Ridge GO2SX signal pulled-up to SUS rail



Power State Debug LEDs

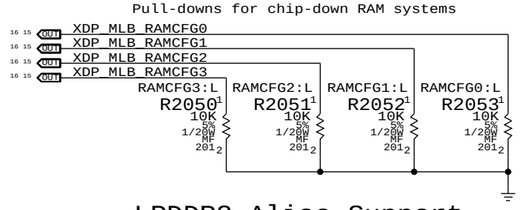
(For development only)



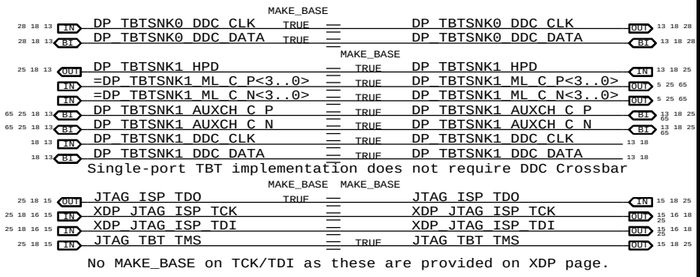


RAM Configuration Straps

Pull-downs for chip-down RAM systems



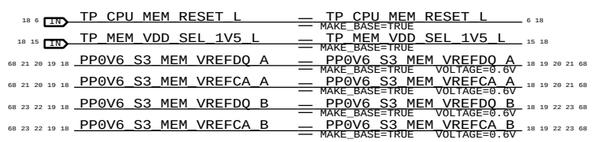
TBT Aliases



Single-port TBT implementation does not require DDC Crossbar

No MAKE_BASE on TCK/TDI as these are provided on XDP page.

LPDDR3 Alias Support



SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

PAGE TITLE: Project Chipset Support

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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining

VRef Dividers

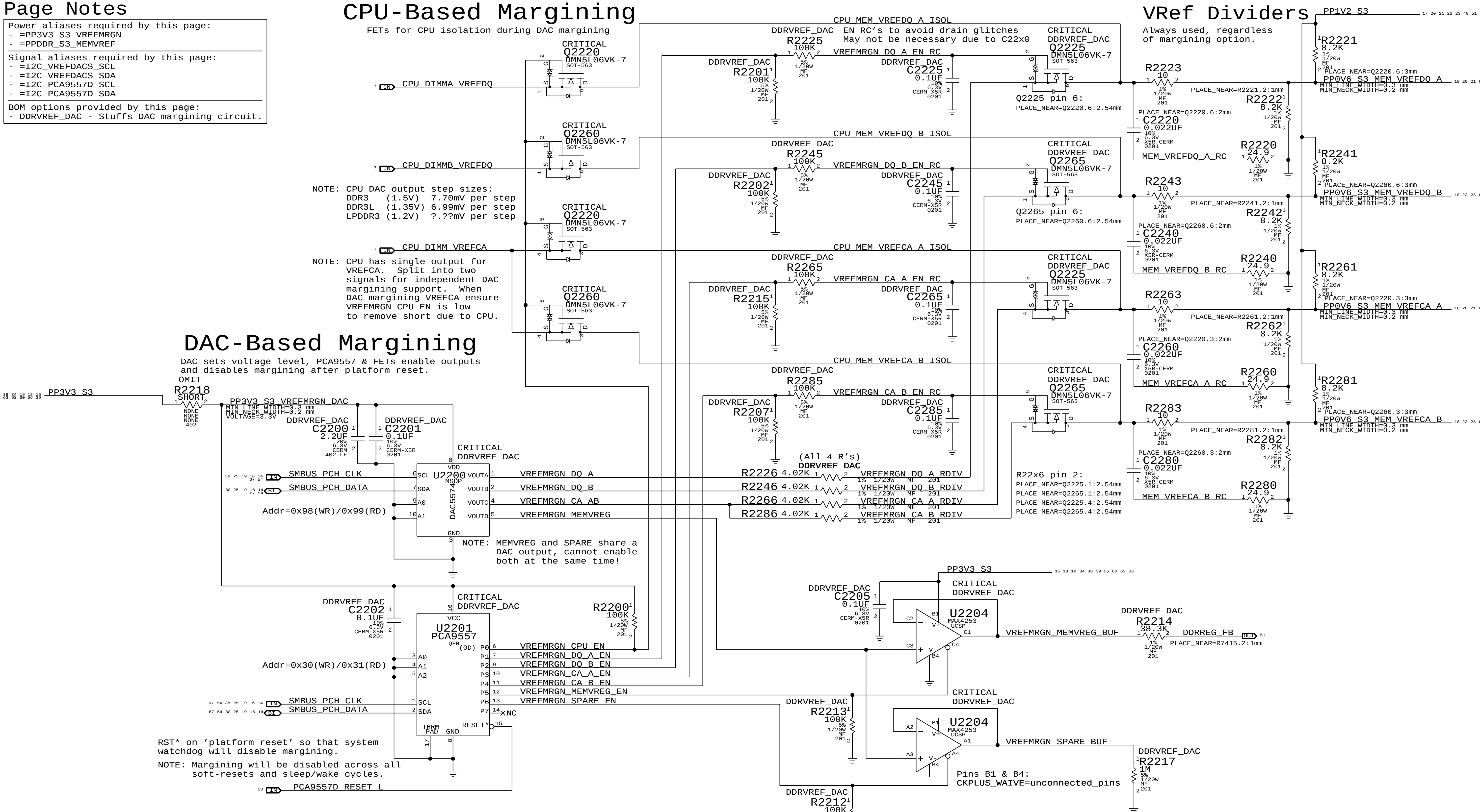
Always used, regardless of margining option.

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.



	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5

	LPDDR3 (1.2V)	DDR3L (1.35V)	LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)	0.675V (DAC: 0x34)	1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)	0.337V - 1.013V (+/- 337.5mV)	0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)	0.000V - 1.354V (0x00 - 0x69)	0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)	+82uA - -82uA (- = sourced)	+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output	6.36mV / step @ output	4.28mV / step @ output	3.53mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=WILL_J43 SYNC_DATE=02/04/2013

PAGE TITLE
DDR3 VREF MARGINING

Apple Inc.

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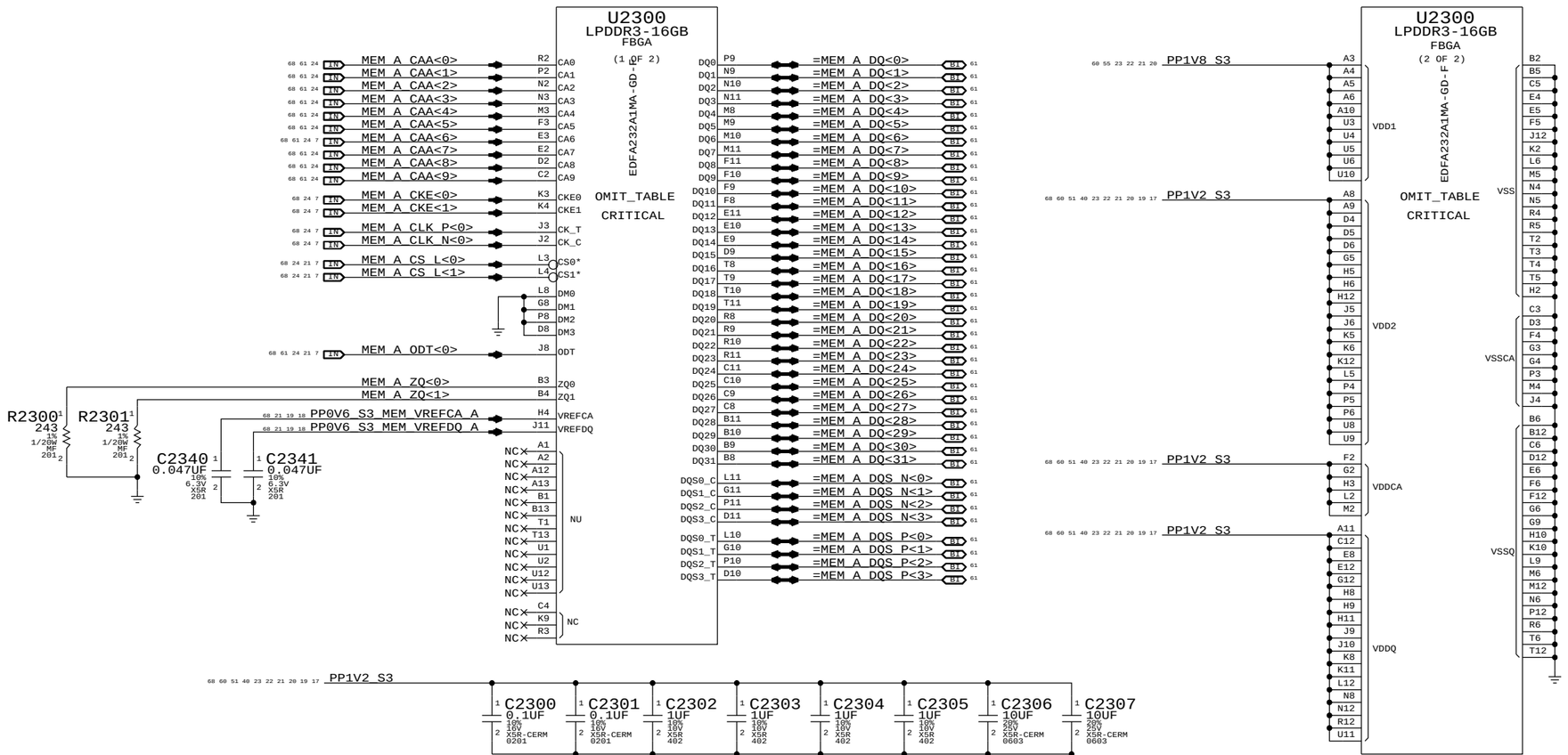
LPDDR3 CHANNEL A (0-31)



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
LPDDR3 DRAM Channel A (0-31)

Apple Inc.

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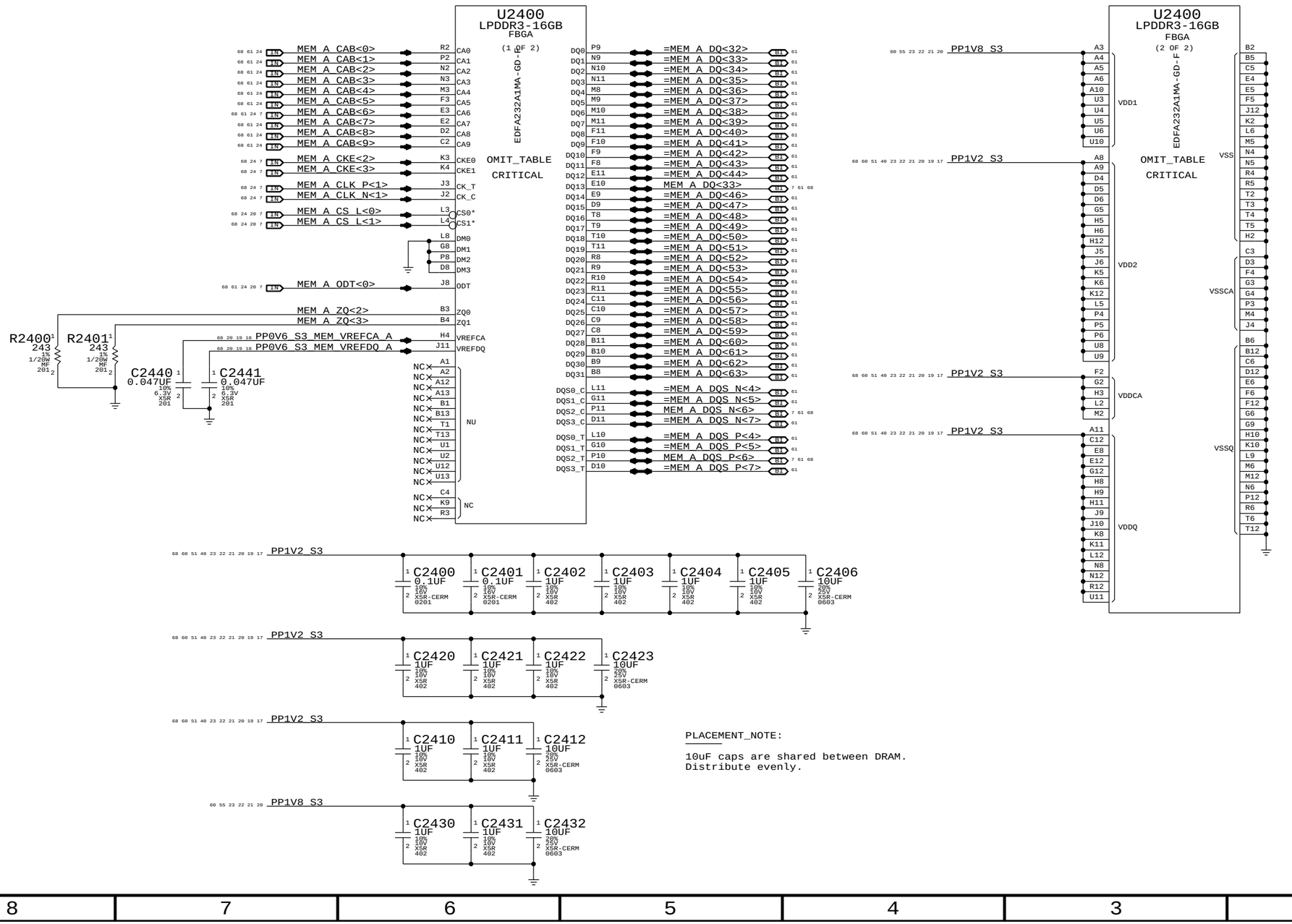
LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

Apple Inc.

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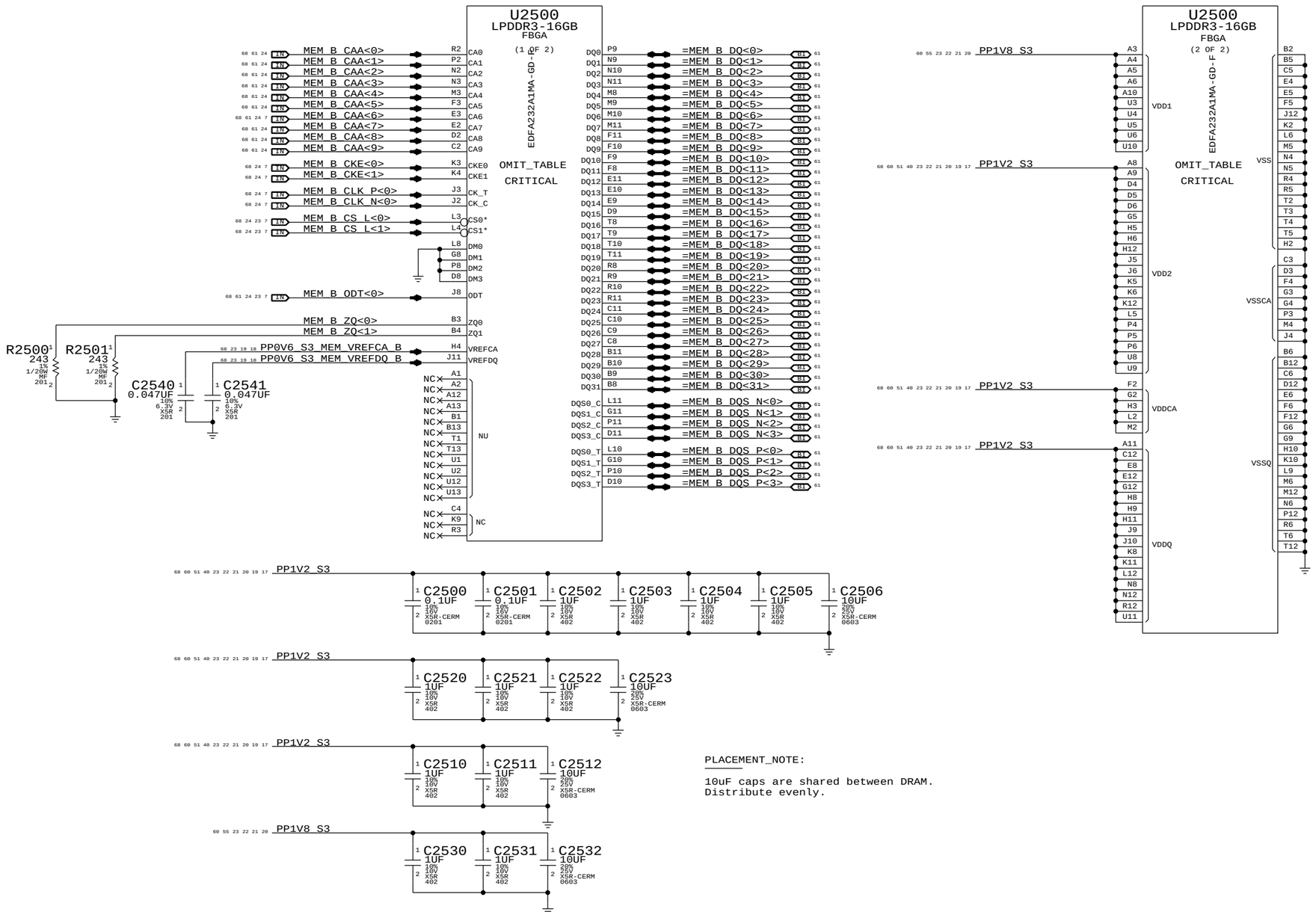
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
LPDDR3 DRAM Channel B (0-31)

Apple Inc.

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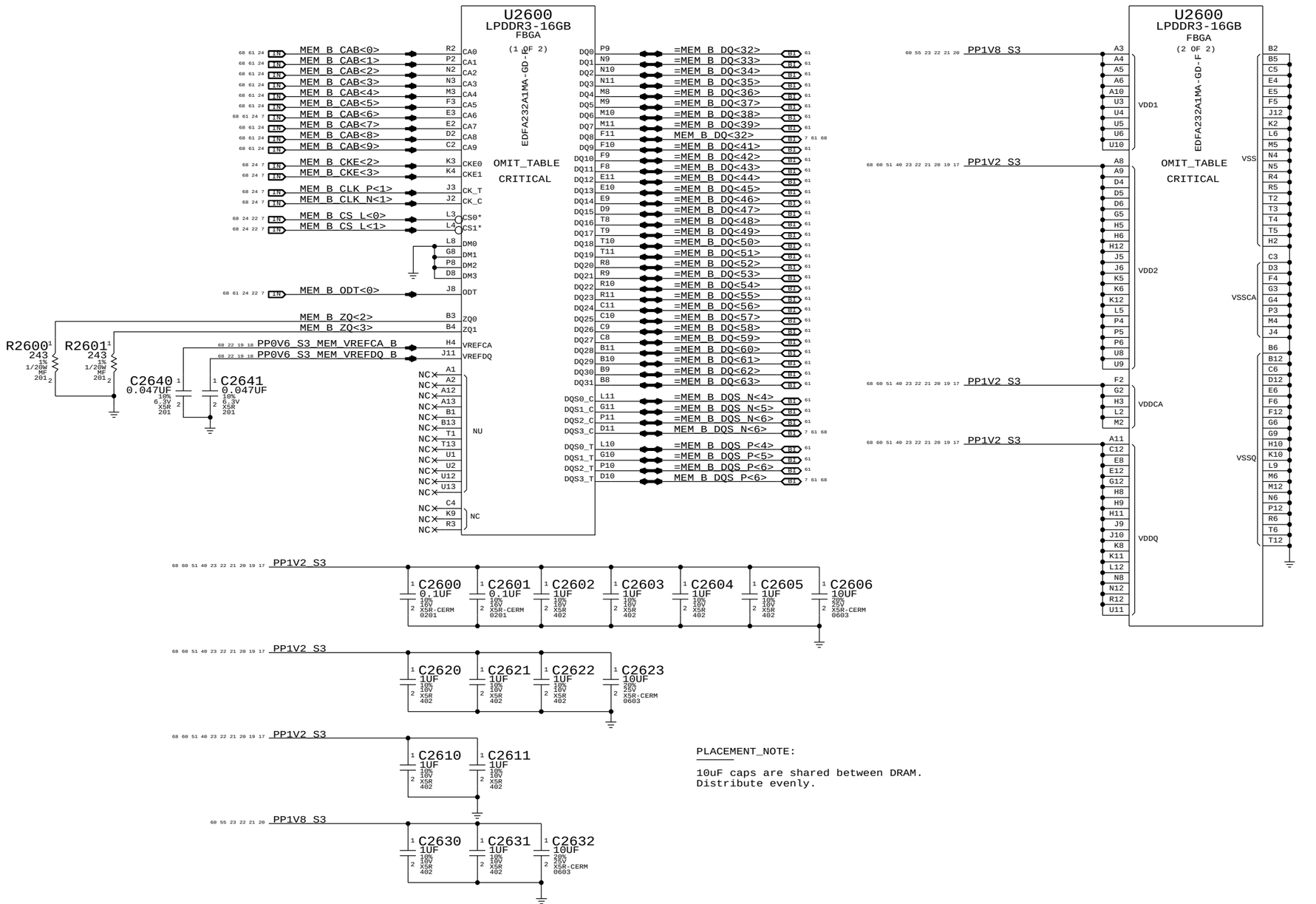
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
LPDDR3 DRAM Channel B (32-63)

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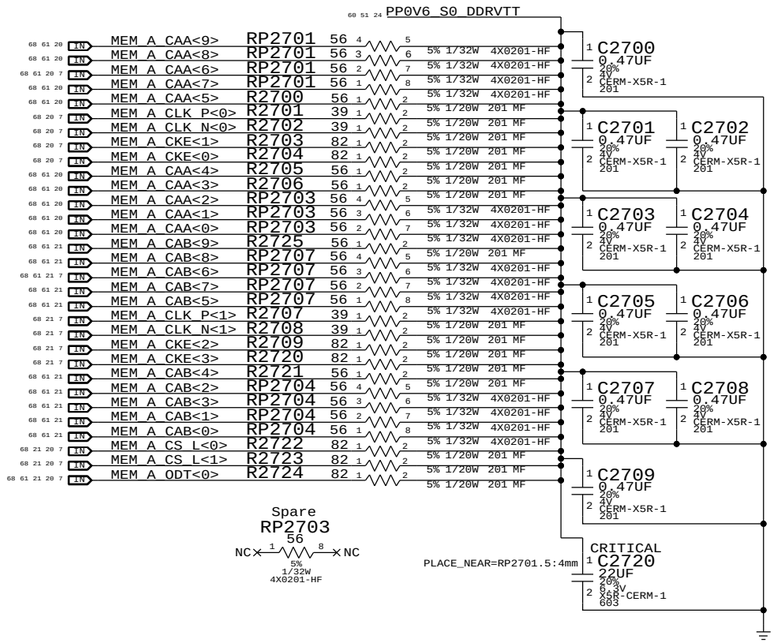
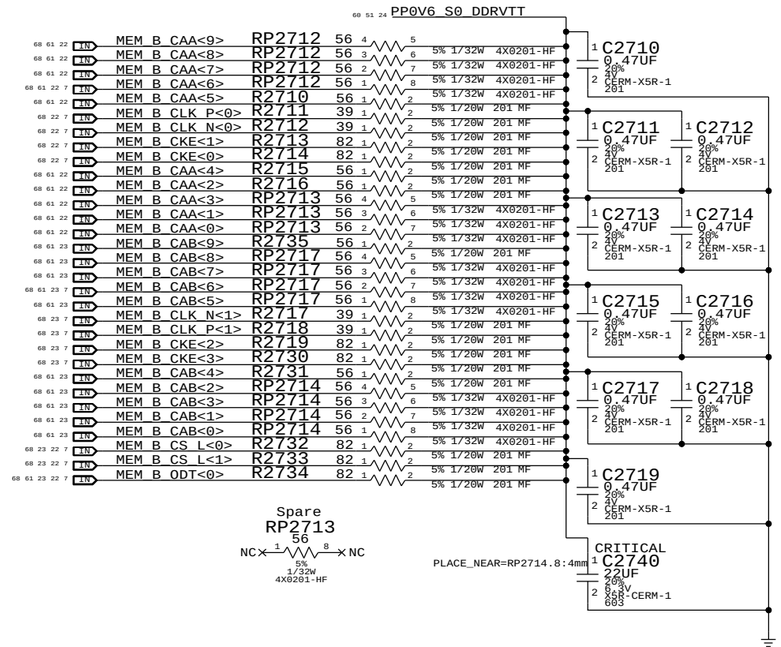
Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





SYNC_MASTER=J43_MLB	SYNC_DATE=09/21/2012
PAGE TITLE	LPDDR3 DRAM Termination
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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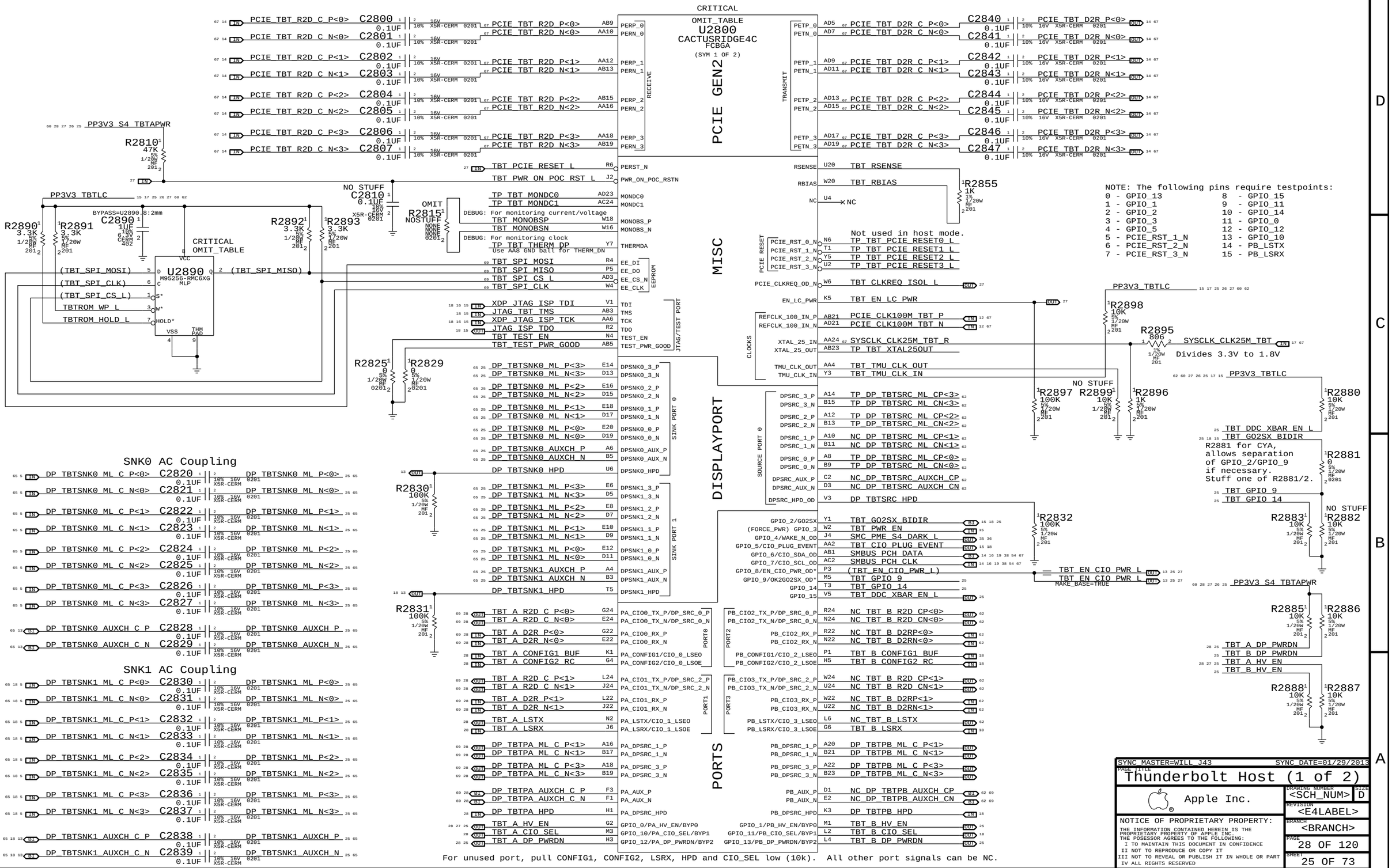
CRITICAL
OMIT_TABLE
U2800
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)
PCIE GEN2
RECEIVE
TRANSMIT
MISC
EEPROM
JTAG/TEST PORT
CLOCKS
DISPLAYPORT
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
PORT0
PORT1
PORT2
PORT3
PORTS
PCIE RESET
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_P<0>
PCIE_TBT_R2D_N<0>
PCIE_TBT_R2D_P<1>
PCIE_TBT_R2D_N<1>
PCIE_TBT_R2D_P<2>
PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_N<3>
PCIE_TBT_D2R_C_P<0>
PCIE_TBT_D2R_C_N<0>
PCIE_TBT_D2R_C_P<1>
PCIE_TBT_D2R_C_N<1>
PCIE_TBT_D2R_C_P<2>
PCIE_TBT_D2R_C_N<2>
PCIE_TBT_D2R_C_P<3>
PCIE_TBT_D2R_C_N<3>
PCIE_TBT_D2R_P<0>
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<1>
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<2>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<3>
PCIE_TBT_D2R_N<3>
PP3V3_S4_TBTAPWR
PP3V3_TBTLC
R2810 47K
TBT_PCIE_RESET_L
TBT_PWR_ON_POC_RST_L
NO STUFF C2810 0.1UF
R2890 3.3K
R2891 3.3K
C2890 1UF
R2892 3.3K
R2893 3.3K
OMIT R2815 NOSTUFF
BYPASS=U2890.8:2mm
CRITICAL
OMIT_TABLE
U2890
M95256-RMC6XG
MLP
(TBT_SPI_MOSI)
(TBT_SPI_CLK)
(TBT_SPI_CS_L)
TBTROM_WP_L
TBTROM_HOLD_L
(TBT_SPI_MISO)
R2825 0
R2829 0
TP_TBT_MONDC0
TP_TBT_MONDC1
DEBUG: For monitoring current/voltage
TBT_MONOBSP
TBT_MONOBSN
DEBUG: For monitoring clock
TP_TBT_THERM_DP
Use AA8 GND ball for THERM_DN
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
XDP_JTAG_ISP_TDI
JTAG_TBT_TMS
XDP_JTAG_ISP_TCK
JTAG_ISP_TDO
TBT_TEST_EN
TBT_TEST_PWR_GOOD
DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_N
DP_TBTSNK0_HPD
R2830 100K
DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_N
DP_TBTSNK1_HPD
R2831 100K
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_CONFIG1_BUF
TBT_A_CONFIG2_RC
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_AUXCH_C_P
DP_TBTPA_AUXCH_C_N
DP_TBTPA_HPD
TBT_A_HV_EN
TBT_A_CIO_SEL
TBT_A_DP_PWRDN
RSENSE
RBIAS
NC
TBT_RSENSE
TBT_RBIAS
R2855 1K
Not used in host mode.
TBT_PCIE_RESET0_L
TBT_PCIE_RESET1_L
TBT_PCIE_RESET2_L
TBT_PCIE_RESET3_L
TBT_CLKREQ_ISOL_L
TBT_EN_LC_PWR
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
SYSCLK_CLK25M_TBT_R
TP_TBT_XTAL25OUT
TBT_TMU_CLK_OUT
TBT_TMU_CLK_IN
TP_DP_TBTSRC_ML_CP<3>
TP_DP_TBTSRC_ML_CN<3>
TP_DP_TBTSRC_ML_CP<2>
TP_DP_TBTSRC_ML_CN<2>
NC_DP_TBTSRC_ML_CP<1>
NC_DP_TBTSRC_ML_CN<1>
TP_DP_TBTSRC_ML_CP<0>
TP_DP_TBTSRC_ML_CN<0>
NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN
DP_TBTSRC_HPD
TBT_GO2SX_BIDIR
TBT_PWR_EN
SMC_PME_S4_DARK_L
TBT_CIO_PLUG_EVENT
SMBUS_PCH_DATA
SMBUS_PCH_CLK
(TBT_EN_CIO_PWR_L)
TBT_GPIO_9
TBT_GPIO_14
TBT_DDC_XBAR_EN_L
NC_TBT_B_R2D_CP<0>
NC_TBT_B_R2D_CN<0>
NC_TBT_B_D2RP<0>
NC_TBT_B_D2RN<0>
TBT_B_CONFIG1_BUF
TBT_B_CONFIG2_RC
NC_TBT_B_R2D_CP<1>
NC_TBT_B_R2D_CN<1>
NC_TBT_B_D2RP<1>
NC_TBT_B_D2RN<1>
NC_TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
NC_DP_TBTPB_AUXCH_CP
NC_DP_TBTPB_AUXCH_CN
DP_TBTPB_HPD
TBT_B_HV_EN
TBT_B_CIO_SEL
TBT_B_DP_PWRDN
TBT_EN_CIO_PWR_L
MAKE_BASE=TRUE
R2832 100K
R2898 10K
R2895 806
SYSCLK_CLK25M_TBT
Divides 3.3V to 1.8V
R2897 100K
R2899 10K
R2896 1K
R2880 10K
TBT_DDC_XBAR_EN_L
TBT_GO2SX_BIDIR
R2881 for CYA,
allows separation
of GPIO_2/GPIO_9
if necessary.
Stuff one of R2881/2.
R2881 0
R2883 10K
R2882 10K
R2885 10K
R2886 10K
R2888 10K
R2887 10K
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
SNK0 AC Coupling
SNK1 AC Coupling
C2820 0.1UF
C2821 0.1UF
C2822 0.1UF
C2823 0.1UF
C2824 0.1UF
C2825 0.1UF
C2826 0.1UF
C2827 0.1UF
C2828 0.1UF
C2829 0.1UF
C2830 0.1UF
C2831 0.1UF
C2832 0.1UF
C2833 0.1UF
C2834 0.1UF
C2835 0.1UF
C2836 0.1UF
C2837 0.1UF
C2838 0.1UF
C2839 0.1UF
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=WILL_J43
SYNC_DATE=01/29/2013
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
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REVISION
<E4LABEL>
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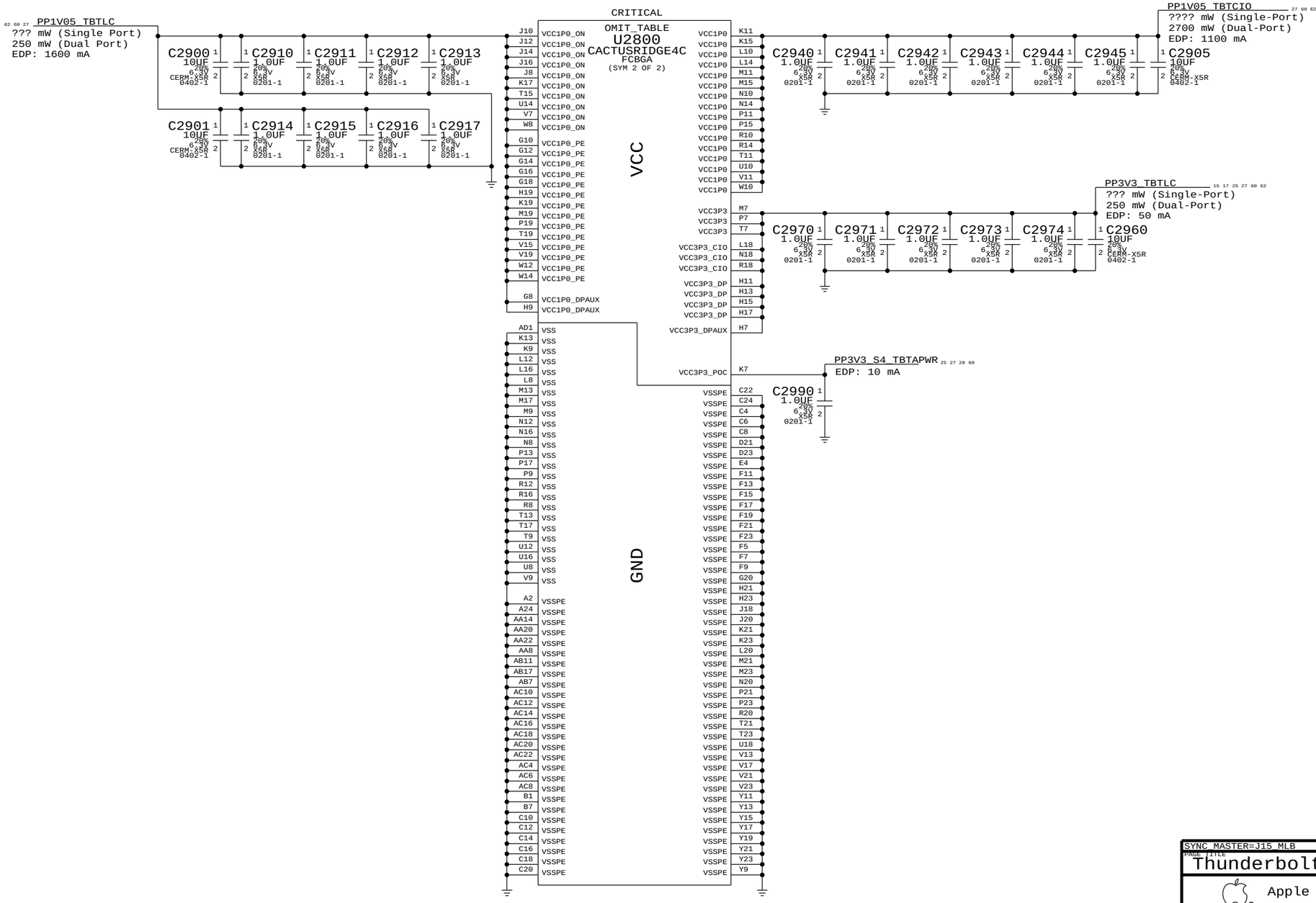

EDP numbers are from 12/22/2011 email from Haim Lustig (Intel) to Paul Baker (Apple)
Power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC_MASTER=J15_MLB SYNC_DATE=07/16/2012

PAGE TITLE
Thunderbolt Host (2 of 2)

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
(NONE)

TBT 15V Boost Regulator

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPBUS_G3H
8-13V Input
Changes required for 2S.

CRITICAL Q3080 SI8409DB BGA

PPVIN_S4SW_TBTBST_FET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

R3080 470K 5% 1/20W MF 201
C3080 0.1UF 10% 16V X5R 402
TBTBST_PWREN_DIV_L
R3081 150K 5% 1/20W MF 201
TBTBST_PWREN_L
Q3005 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
TBT_A_HV_EN

R3091 200K 1% 1/20W MF 201 <R1>
TBTBST_EN_UVLO

C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603

CRITICAL L3095 6.8UH-4.0A PIMB062D-SM

CRITICAL U3090 LT3957 QFN
VIN, SW, SNS1, SNS2, EN/UVLO, INTVCC, VC, RT, SS, SYNC, NC, FBX, SGND, GND

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIOT=TRUE

TBTBST_SNS1
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
R3089 0 5% 1/20W MF 0201

TBTBST_SNS2
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

CRITICAL D3095 POWERDI-123 DFLS230L

PP15V_TBT
Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

XW3095 SM PLACE_NEAR=C3095.1:2 mm

TBTBST_VSNS
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

R3090 49.9K 1% 1/16W MF-LF 402
TBTBST_VSNS_RC
C3088 22PF 5% 50V CERM 0402
R3095 133K 1% 1/16W MF-LF 402 <Ra>
R3096 15.8K 1% 1/16W MF-LF 402 <Rb>
NO STUFF C3089 100PF 5% 50V CERM 402
TBTBST_FBX
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

C3095 10UF 20% 25V X5R-CERM 0603
C3097 10UF 20% 25V X5R-CERM 0603
C3096 10UF 20% 25V X5R-CERM 0603
C3098 10UF 20% 25V X5R-CERM 0603
C3084 10UF 20% 25V X5R-CERM 0603
C309A 10UF 20% 25V X5R-CERM 0603
C3085 10UF 20% 25V X5R-CERM 0603
C309B 10UF 20% 25V X5R-CERM 0603
C3099 0.001UF 10% 50V X7R-CERM 0402

C3081 2.2UF 20% 25V X5R-CERM 402
C3092 2.2UF 20% 25V X5R-CERM 402
C3087 47PF 5% 25V NP0-C0G-CERM 0201
R3093 10K 1% 1/20W MF 201
TBTBST_VC_RC
R3092 73.2K 1% 1/20W MF 201 <R2>
C3082 2.2UF 20% 25V X5R-CERM 402
C3093 3300PF 10% 10V X7R-CERM 0201
R3094 41.2K 1% 1/20W MF 201
C3094 0.33UF 10% 6.3V CERM-X5R 402

TBTBST_INTVCC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
TBTBST_VC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
TBTBST_RT
TBTBST_SS
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

SGND shorted to GND inside package, no XW necessary.

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

Vout = 1.6V * (1 + Ra / Rb)

Q3088 DMN5L06VK-7 SOT-563
Max Vgs: 10V
R3088 330K 5% 1/20W MF 201
TBTBST_SHDN_DIV
R3087 330K 5% 1/20W MF 201
Q3088 DMN5L06VK-7 SOT-563
SMC_DELAYED_PWRGD

Supervisor & CLKREQ# Isolation

PP3V3_S0
R3040 10K 5% 1/20W MF 201
Q3040 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
TBT_EN_LC_PWR
C3000 0.1UF 10% 16V X5R-CERM 0201

CRITICAL U3000 SLG4AP016V TDFN
VDD, SENSE 0.7V, DLY, RESET*, MR*, EN, OUT (OD), IN, GND, THRM PAD

R3007 100K 5% 1/20W MF 201
PP3V3_TBTLC
PP1V05_TBTLC
TBT_PCIE_RESET_L
DLY = 60 ms +/- 20%
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE

PCH_TBT_PCIE_RESET_L
Platform (PCIe) Reset
TBT_CLKREQ_L
Pull-up provided by SB page.

TBT_EN_LC_ISOL
R3011 36.5K 1% 1/20W MF 201
TBT_EN_LC_RC3V3

3.3V TBT "LC" Switch

U3010 TPS22924 CSP
A2, B2, C2, VIN, VOUT, ON, GND, CRITICAL, C1, A1, B1

PP3V3_S0
C3010 1.0UF 20% 6.3V X5R 0201-1
C3011 1.0UF 20% 6.3V X5R 0201-1
PP3V3_TBTLC
Max Current = 2A (85C)

U3010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

R3016 0 5% 1/20W MF 0201
TBT_EN_LC_RC1V05

1.05V TBT "LC" Switch

U3015 TPS22920 CSP
A2, B2, C2, VIN, VOUT, ON, GND, CRITICAL, D1, A1, B1, C1, D2

PP1V05_S0
C3015 1.0UF 20% 6.3V X5R 0201-1
NO STUFF C3016 1.0UF 20% 6.3V X5R 0201-1
PP1V05_TBTLC
Max Current = 4A (85C)

U3015

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	6.1 mOhm Typ 10.4 mOhm Max

TBT "POC" Power-up Reset

PP3V3_S4_TBTAPWR
CRITICAL U3030 TPS3808 QFN
VDD, SENSE, CT, RESET*, MR*, GND, THRM PAD
Pull-up: R2810
TBT_PWR_ON_POC_RST_L
TBTPOCRST_MR_L
TBTPOCRST_CT
C3031 0.0047UF 10% 25V CERM 0402
C3030 0.1UF 10% 16V X5R-CERM 0201
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms
C3025 330PF 10% 16V X7R-CERM 0201
Q3025 DMN5L06VK-7 SOT-563
PP3V3_S0
R3030 100K 5% 1/20W MF 201
TBT_POC_RESET_L

1.05V TBT "CIO" Switch

PP1V05_S0
PP3V3_TBTLC
R3020 100K 5% 1/20W MF 201
TBT_EN_CIO_PWR
Q3025 DMN5L06VK-7 SOT-563
TBT_EN_CIO_PWR_L

U3020 TPS22920 CSP
A2, B2, C2, VIN, VOUT, ON, GND, CRITICAL, D1, A1, B1, C1, D2

C3020 1.0UF 20% 6.3V X5R 0201-1
PP1V05_TBTCIO
Max Current = 4A (85C)

U3020

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	6.1 mOhm Typ 10.4 mOhm Max

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: TBT Power Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt device attach.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5 — CRITICAL C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM; C3280 22UF 20% 6.3V X5R-CERM 603; C3281 0.1UF 10% 16V X5R-CERM 0201

PP15V_TBT 18.9V Max — C3215 4.7UF 10% 25V X5R-CERM 0603; C3210 0.1UF 10% 16V X5R 402

CRITICAL U3210 CD3211A0RGPR QFN

V3P3 (19,20) — V3P3OUT (18) — C3285 0.1UF 10% 16V X5R-CERM 0201

VHV (6,7) — OUT (12,14) — C3286 10UF 20% 6.3V CERM-X5R 0402-1; C3211 0.1UF 10% 25V X5R 402

PP3V3_S4_TBTAPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V

PP3V3RHV_S4_TBTAPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V

Pin	Net
ENHVU (16)	S4_PWR_EN (IN)
EN (5)	TBT_A_HV_EN (IN)
HV_EN (11)	PM_SLP_S3_BUF_L (IN)
S0 (17)	
FAULTZ (4)	
ISET_V3P3 (8)	TBTAPWRSW_ISET_V3P3
ISET_S0 (10)	TBTAPWRSW_ISET_S0
ISET_S3 (9)	TBTAPWRSW_ISET_S3
GND (1,2,3,13,15)	
THRM PAD (21)	

TBTHV:P15V R3210 22.6K 1% 1/20W MF 201 — 12V: See below

TBTHV:P15V R3211 22.6K 1% 1/20W MF 201

R3212 36.5K 1% 1/20W MF 201 <RV3P3>

TBTAPWRSW_ISET_S3_R

TBTAPWRSW_ISET_S0_R

TBTHV:P15V R3213 22.6K 1% 1/20W MF 201 <RHVS3>

TBTHV:P15V R3214 22.6K 1% 1/20W MF 201 <RHVS0>

Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

PP3V3_S4_TBTAPWR — C3220 0.1UF 10% 16V X5R-CERM 0201 — SIGNAL_MODEL=TBT_MUX

CRITICAL U3220 CBTL05024 HVQFN24-COMBO

Pin	Net
VDD (3)	
TB- (7)	TBT_A_D2R_C_N<1>
TB+ (8)	TBT_A_D2R_C_P<1>
AUX- (1)	DP_TBTPA_AUXCH_C_N
AUX+ (2)	DP_TBTPA_AUXCH_C_P
DDC_DAT (4)	DP_TBTSNK0_DDC_DATA
DDC_CLK (5)	DP_TBTSNK0_DDC_CLK
CA_DETOUT (16)	TBT_A_CONFIG1_BUF (OUT)
DP+ (11)	DP_TBTPA_ML_C_P<1>
DP- (10)	DP_TBTPA_ML_C_N<1>
LSTX (IPU) (14)	TBT_A_LSTX (IN)
LSRX (IPD) (13)	TBT_A_LSRX (OUT)
HPDOUT (12)	DP_TBTPA_HPD (OUT)
TB_ENA (15)	TBT_A_CIO_SEL (IN)
AUXIO_EN (24)	DP_AUXCH_ISOL_L (IN)
DP_PD (6)	TBT_A_DP_PWRDN (IN)
(IPU) AUXIO- (23)	TBT_A_D2R1_AUXDDC_N
(IPD) AUXIO+ (22)	TBT_A_D2R1_AUXDDC_P
CA_DET (18)	TBT_A_CONFIG1_RC
DPML0+ (19)	DP_A_LSX_ML_P<1>
DPML0- (20)	DP_A_LSX_ML_N<1>
HPD (17)	TBT_A_HPD
GND THMPAD (9,21,25)	

TBT: RX_1

TBT: LSX_A_R2P/P2R (P/N)

GND_VOID=TRUE (Both C's)

TBT_A_D2R_N<1> — C3277 0.47UF 20% 4V_201 CERM-X5R-1 — TBT_A_D2R_C_N<1>

TBT_A_D2R_P<1> — C3276 0.47UF 20% 4V_201 CERM-X5R-1 — TBT_A_D2R_C_P<1>

DP_TBTPA_AUXCH_C_N — C3230 0.1UF 10% 16V X5R-CERM 0201 — DP_TBTPA_AUXCH_C_N

DP_TBTPA_AUXCH_C_P — C3231 0.1UF 10% 16V X5R-CERM 0201 — DP_TBTPA_AUXCH_P

DP_TBTPA_ML_C_P<1> — C3232 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_P<1>

DP_TBTPA_ML_C_N<1> — C3233 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_N<1>

Thunderbolt Connector A

CRITICAL L3200 FERR-120-OHM-3A 0603 — PP3V3RHV_S4_TBTAPWR_F — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V

C3200 0.01UF 10% 16V X7R-CERM 0402

C3201 0.01UF 10% 16V X7R-CERM 0402

R3201 12 5% 1/20W MF 201

TBTACONN_20_RC — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V

TBT Dir / DP Dir

TBT: RX_0

TBT: Unused

TBT: RX_1

J3200 MDP-J11 F-RT-TH

CRITICAL 514-0818

Pin	Net
HOT_PLUG_DETECT (2)	
CONFIG1 (4)	
CONFIG2 (6)	
GND (13)	
ML_LANE3P (10)	
ML_LANE3N (12)	
GND (14)	
AUX_CHP (16)	
AUX_CHN (18)	
DP_PWR (20)	
GND (1)	
ML_LANE0P (3)	
ML_LANE0N (5)	
GND (7)	
ML_LANE1P (9)	
ML_LANE1N (11)	
GND (8)	
ML_LANE2P (15)	
ML_LANE2N (17)	
RETURN (19)	
SHIELD PINS (28,27,26,25,24,23,22,21)	

TBTACONN_1_C — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V — (0-18.9V)

C3205 0.01UF 10% 25V X5R-CERM 0201 — GND_VOID=TRUE

TBTACONN_7_C — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V — (0-18.9V)

C3206 0.01UF 10% 16V X5R-CERM 0201 — GND_VOID=TRUE

DP Dir / TBT Dir

TBT_A_R2D_P<0> — C3270 0.22UF 20% 6.3V X5R 0201 — TBT_A_R2D_C_P<0>

TBT_A_R2D_N<0> — C3271 0.22UF 20% 6.3V X5R 0201 — TBT_A_R2D_C_N<0>

TBT: TX_0

TBT_A_R2D_P<1> — C3272 0.22UF 20% 6.3V X5R 0201 — TBT_A_R2D_C_P<1>

TBT_A_R2D_N<1> — C3273 0.22UF 20% 6.3V X5R 0201 — TBT_A_R2D_C_N<1>

TBT: TX_1

GND_VOID=TRUE (Both C's)

TBT_A_D2R_P<0> — C3274 0.47UF 20% 4V_201 CERM-X5R-1 — TBT_A_D2R_C_P<0>

TBT_A_D2R_N<0> — C3275 0.47UF 20% 4V_201 CERM-X5R-1 — TBT_A_D2R_C_N<0>

R3294 1K 5% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE

R3295 1K 5% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE

DP_TBTPA_ML_C_P<3> — C3278 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_P<3>

DP_TBTPA_ML_C_N<3> — C3279 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_N<3>

R3279 470K 5% 1/20W MF 201

R3278 470K 5% 1/20W MF 201

TBT_A_D2R1_AUXDDC_P

TBT_A_D2R1_AUXDDC_N

TBT_A_HPD

TBT_A_CONFIG1_RC

TBT_A_CONFIG2_RC (OUT)

R3252 1M 5% 1/20W MF 201

R3251 1M 5% 1/20W MF 201

C3294 330PF 10% 16V X7R-CERM 0201

C3295 330PF 10% 16V X7R-CERM 0201

R3241 100K 5% 1/20W MF 201

C3202 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

R3270 470K 5% 1/20W MF 201 — GND_VOID=TRUE

R3271 470K 5% 1/20W MF 201 — GND_VOID=TRUE

R3272 470K 5% 1/20W MF 201 — GND_VOID=TRUE

R3273 470K 5% 1/20W MF 201 — GND_VOID=TRUE

470K R's for ESD protection on AC-coupled signals.

SYNC_MASTER=J43_MLB SYNC_DATE=09/04/2012

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

Sense resistor on sensor page

PP3V3_WLAN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

PP3V3_WLAN_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

Max Current = 2A (85C)

U3550
TPS22924
CSP
CRITICAL
A1 VOUT
B1
A2 VIN
B2 ON
C2 GND
C1

PP3V3_S5
SMC_WIFI_PWR_EN

C3550
1.0UF
20%
6.3V
X6S
0201-1

C3521
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=J3501:5mm

514S0335
CRITICAL
J3501
SSD-K99
F-RT-SM1

AIRPORT

PCIE_AP_R2D_N → C3531 0.1UF → PCIE_AP_R2D_C_N
PCIE_AP_R2D_P → C3530 0.1UF → PCIE_AP_R2D_C_P
(10% 16V X5R-CERM 0201)

WIFI_EVENT_L (OUT)
PCIE_CLK100M_AP_N (IN)
PCIE_CLK100M_AP_P (IN)
PCIE_AP_D2R_P (OUT)
PCIE_AP_D2R_N (OUT)

PP3V3_S4

C3532
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=J3501:1.5mm

Supervisor & CLKREQ# Isolation

Delay = 130 ms +/- 20%

APCLKRQ:ISOL
R3553 100K 5% 1/20W MF 201
R3554 232K 1% 1/20W MF 201

P3V3WLAN_VMON

U3540
SLG4AP041V
TDFN
CRITICAL
VDD
SENSE
VREF
DLY
RESET*
MR*
EN
OUT (OD)
THRM PAD
GND

PP3V3_S5

C3540
0.1UF
10%
6.3V
CERM-X5R
0201

R3558 0 5% 1/20W MF 0201
AP_RESET_CONN_L → AP_RESET_CONN_R_L → AP_RESET_L (IN)

AP_CLKREQ_Q_L → AP_CLKREQ_R_L

SMC_WIFI_PWR_EN (IN)

R3555 100K 5% 1/20W MF 201

APCLKRQ:ISOL
R3556 0 5% 1/20W MF 0201

APCLKRQ:BIDIR
R3557 0 5% 1/20W MF 0201
AP_CLKREQ_L (BI)

NOSTUFF
R3559 0 5% 1/20W MF 0201

PCIe Wake Muxing

PP3V3_S5

R3561 100K 5% 1/20W MF 201
C3560 0.1UF 10% 6.3V CERM-X5R 0201

U3560
NC7SB3157P6XG
SC70
VER-3
VCC
GND
S
B0
B1
A

SEL	OUTPUT
L	PCIE_WAKE_L (B0)
H	AP_S0IX_WAKE_L (B1)

AP_S0IX_WAKE_SEL (IN)
PCIE_WAKE_L (OUT)
AP_S0IX_WAKE_L (OUT)
AP_PCIE_WAKE_L

NOSTUFF
R3560 0 5% 1/20W MF 0201

PP3V3_S4

BLUETOOTH

U3510
USB3740
DFN
CRITICAL
VDD
DP_2
DM_2
DP_1
DM_1
OE*
S
GND
DP
DM
NC

C3510
0.1UF
10%
6.3V
CERM-X5R
0201

USB_BT_CONN_P
USB_BT_CONN_N
USB_BT_P (BI)
USB_BT_N (BI)
BT_WAKE
PM_SLP_S4_L (IN)

SIGNAL_MODEL=BT_MUX

SEL	OUTPUT
L	BT_WAKE (1)
H	USB_BT (2)

NO_XNET_CONNECTION=TRUE

Q3510
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2
D
G
S

SMC_PME_S4_WAKE_L (OUT)

R3512 15K 1% 1/20W MF 201

SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE
Wireless Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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BRANCH <BRANCH>
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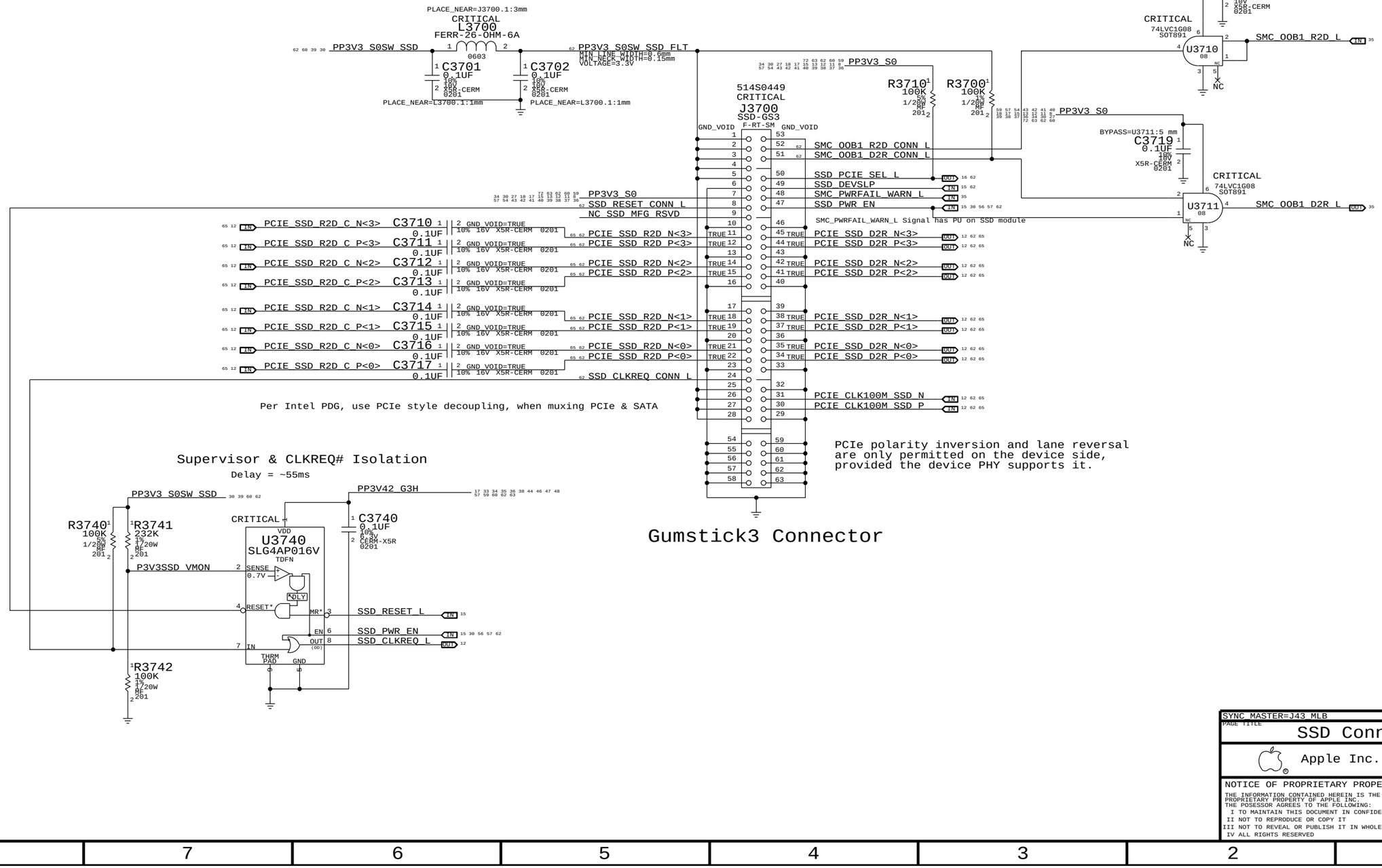

SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE: SSD Connector

Apple Inc.

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REVISION: <E4LABEL>

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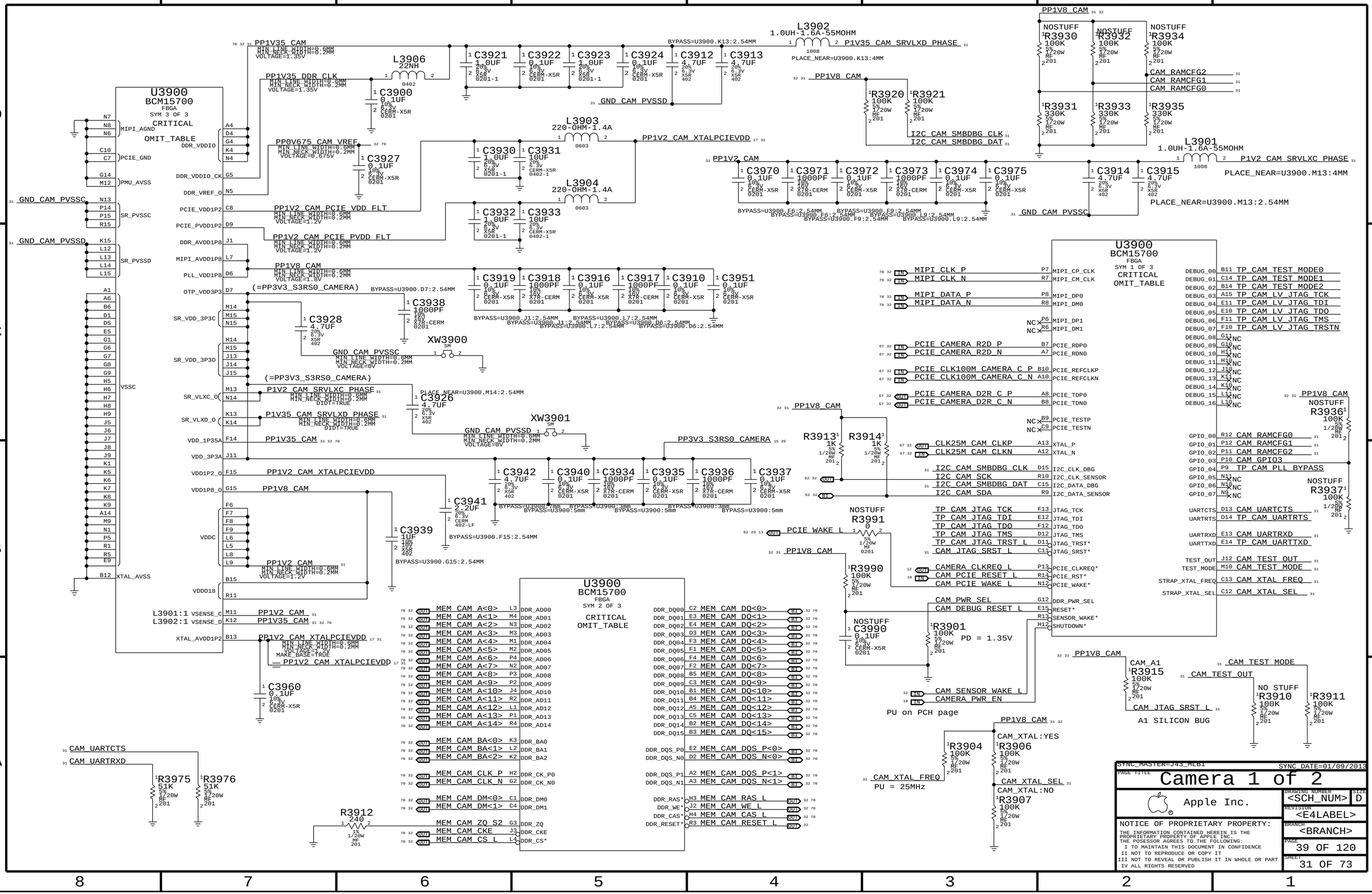
U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE
PP1V35_CAM
PP1V35_DDR_CLK
L3906
22NH
L3902
1.0UH-1.6A-55MOHM
P1V35_CAM_SRVLXD_PHASE
PP1V8_CAM
GND_CAM_PVSSD
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
PP1V2_CAM_XTALPCIEVDD
PP0V675_CAM_VREF
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PCIE_PVDD_FLT
L3901
1.0UH-1.6A-55MOHM
P1V2_CAM_SRVLXC_PHASE
PLACE_NEAR=U3900.M13:4MM
PLACE_NEAR=U3900.M13:2.54MM
GND_CAM_PVSSC
(=PP3V3_S3RS0_CAMERA)
XW3900
XW3901
PP3V3_S3RS0_CAMERA
P1V2_CAM_SRVLXC_PHASE
P1V35_CAM_SRVLXD_PHASE
PP1V2_CAM_XTALPCIEVDD
PP1V8_CAM
PP1V35_CAM
PP1V2_CAM
I2C_CAM_SMBDBG_CLK
I2C_CAM_SMBDBG_DAT
MIPI_CLK_P
MIPI_CLK_N
MIPI_DATA_P
MIPI_DATA_N
PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_N
PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
CLK25M_CAM_CLKP
CLK25M_CAM_CLKN
I2C_CAM_SMBDBG_CLK
I2C_CAM_SCK
I2C_CAM_SMBDBG_DAT
I2C_CAM_SDA
TP_CAM_JTAG_TCK
TP_CAM_JTAG_TDI
TP_CAM_JTAG_TDO
TP_CAM_JTAG_TMS
TP_CAM_JTAG_TRST_L
CAM_JTAG_SRST_L
CAMERA_CLKREQ_L
CAM_PCIE_RESET_L
CAM_PCIE_WAKE_L
CAM_PWR_SEL
CAM_DEBUG_RESET_L
CAM_SENSOR_WAKE_L
CAMERA_PWR_EN
PCIE_WAKE_L
PU on PCH page
CAM_XTAL_FREQ
PU = 25MHz
CAM_XTAL:YES
CAM_XTAL:NO
CAM_XTAL_SEL
CAM_A1
A1 SILICON BUG
CAM_TEST_MODE
CAM_TEST_OUT
NO STUFF
MEM_CAM_A<0>
MEM_CAM_A<1>
MEM_CAM_A<2>
MEM_CAM_A<3>
MEM_CAM_A<4>
MEM_CAM_A<5>
MEM_CAM_A<6>
MEM_CAM_A<7>
MEM_CAM_A<8>
MEM_CAM_A<9>
MEM_CAM_A<10>
MEM_CAM_A<11>
MEM_CAM_A<12>
MEM_CAM_A<13>
MEM_CAM_A<14>
MEM_CAM_BA<0>
MEM_CAM_BA<1>
MEM_CAM_BA<2>
MEM_CAM_CLK_P
MEM_CAM_CLK_N
MEM_CAM_DM<0>
MEM_CAM_DM<1>
MEM_CAM_ZQ_S2
MEM_CAM_CKE
MEM_CAM_CS_L
MEM_CAM_DQ<0>
MEM_CAM_DQS_P<0>
MEM_CAM_DQS_N<0>
MEM_CAM_DQS_P<1>
MEM_CAM_DQS_N<1>
MEM_CAM_RAS_L
MEM_CAM_WE_L
MEM_CAM_CAS_L
MEM_CAM_RESET_L
CAM_UARTCTS
CAM_UARTRXD
CAM_UARTTXD
CAM_UARTRTS
CAM_GPIO3
CAM_RAMCFG0
CAM_RAMCFG1
CAM_RAMCFG2
TP_CAM_PLL_BYPASS
SYNC_MASTER=J43_MLB1
SYNC_DATE=01/09/2013
PAGE TITLE
Camera 1 of 2
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
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REVISION
<E4LABEL>
BRANCH
<BRANCH>
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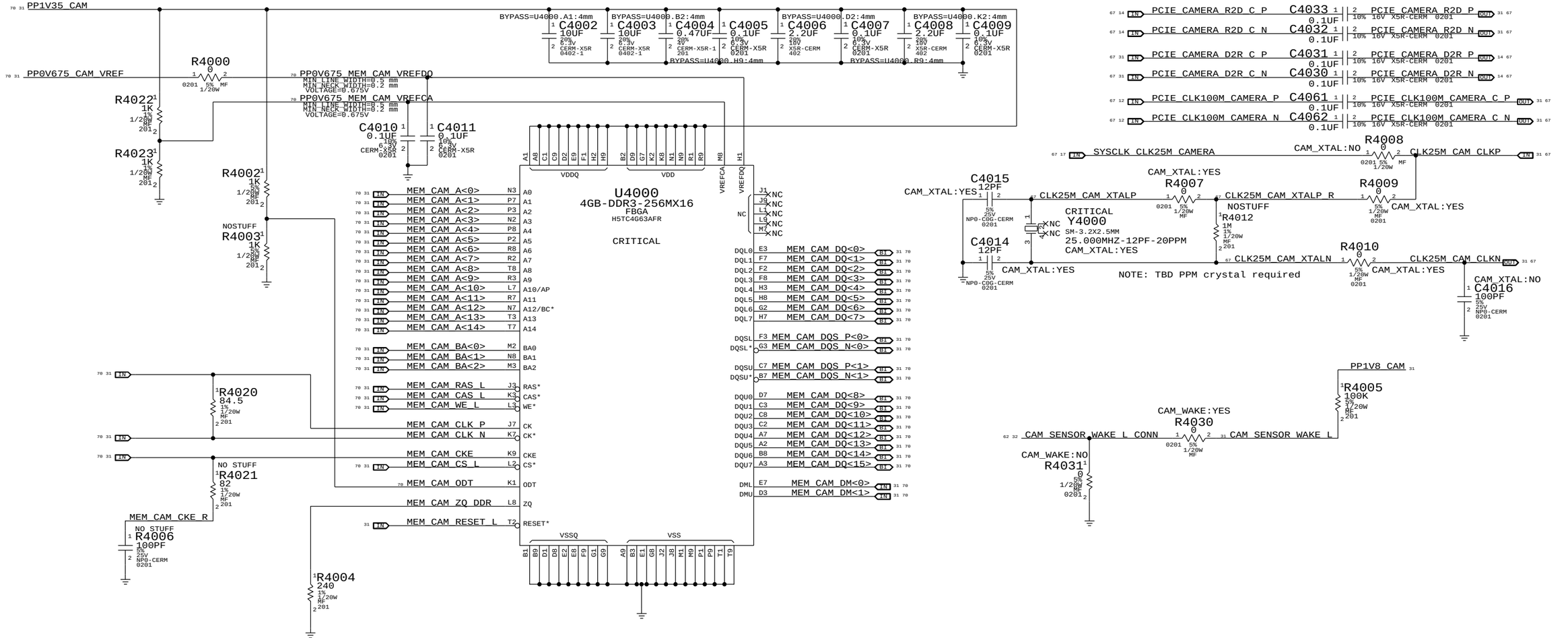

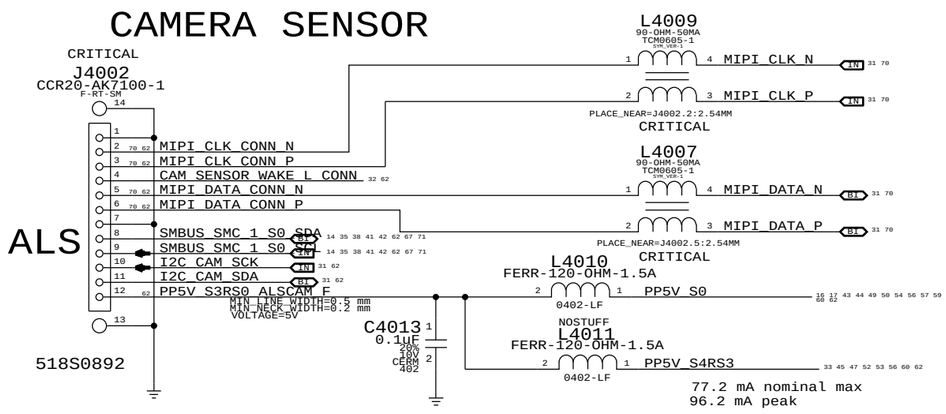

SYNC_MASTER=J43_MLB
SYNC_DATE=09/14/2012

PAGE TITLE: Camera 2 of 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
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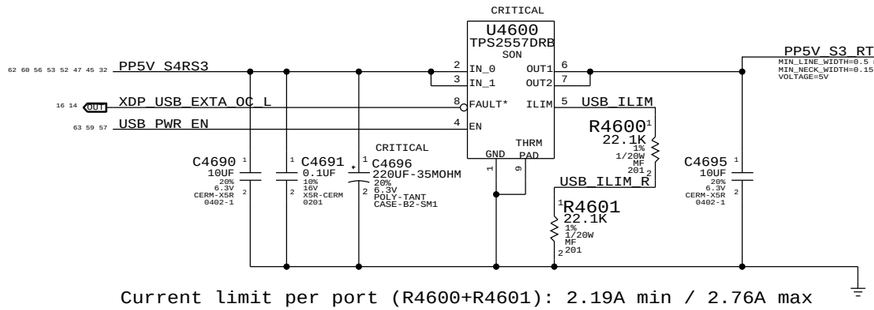
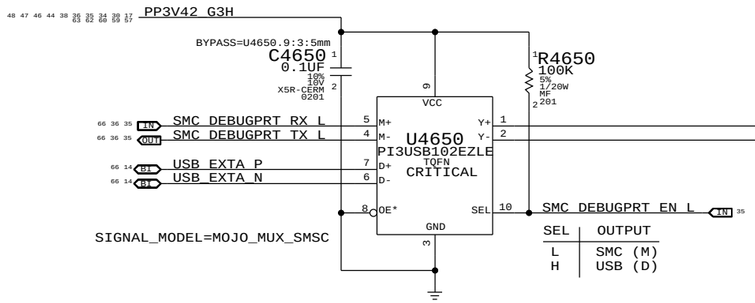
Right USB Port A

USB Port Power Switch

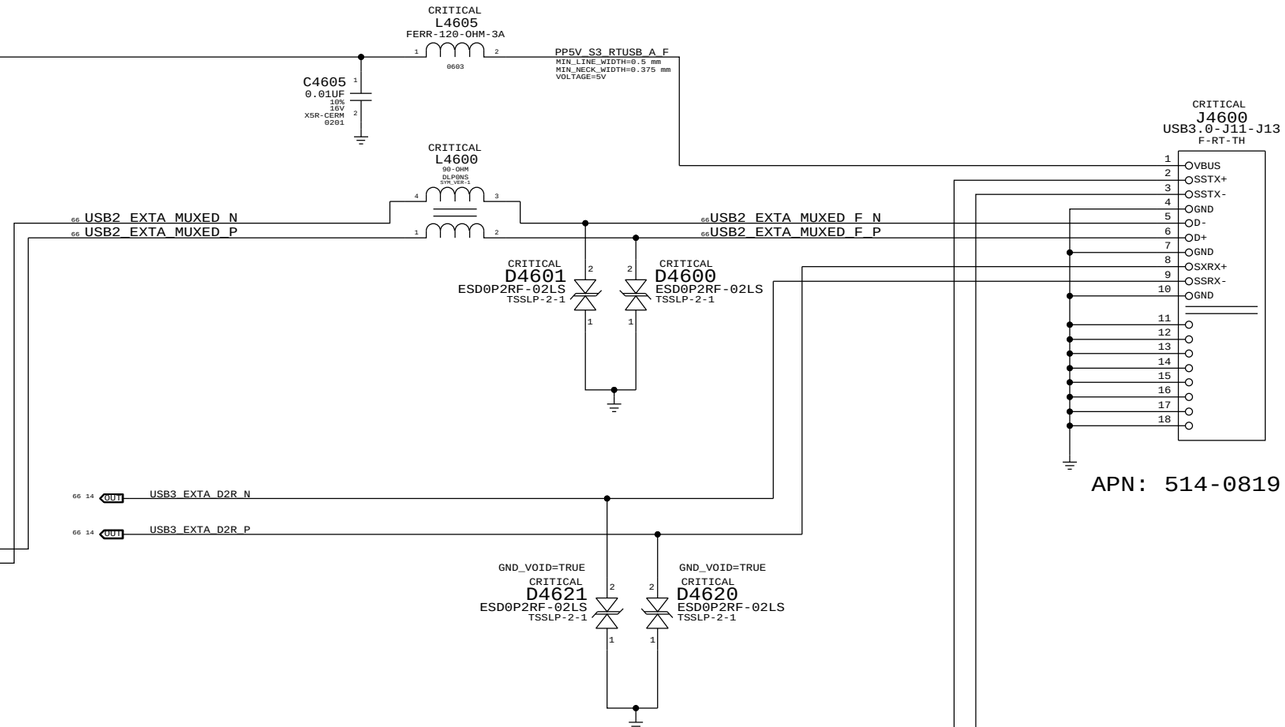


Current limit per port (R4600+R4601): 2.19A min / 2.76A max

Mojo SMC Debug Mux



SEL	OUTPUT
L	SMC (M)
H	USB (D)



APN: 514-0819

SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE
External A USB3 Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 46 OF 120
SHEET 33 OF 73

IPD Flex Connector

PLACE_NEAR=J4800.10:1.5MM
R4830
0
62 60 56 37 36 34 29 PP3V3_S4 — 1 — 2
5% 1/20W MF 0201
C4800 0.1UF 10% 6.3V CERM-X5R 0201
VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.5 mm
BYPASS=J4800.10:1.5MM
PLACE_NEAR=J4800.14:1.5MM
L4820
FERR-120-OHM-1.5A
60 52 51 PP5V_S5 — 1 — 2
0402-LF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
C4810 0.1UF 10% 16V X5R-CERM 0201
PLACE_NEAR=J4800.14:1.5MM
47 46 44 38 36 35 33 30 17 63 62 60 59 57 48 PP3V42_G3H
BYPASS=J4800.10:1.5MM
C4820 0.1UF 10% 6.3V CERM-X5R 0201

TPAD_INTWAKE:SPLIT
PLACE_NEAR=R4844.1:1.5MM
R4841
0
5% 1/20W MF 0201
(TPAD_WAKE_L)

TPAD_INTWAKE:SHARED
R4843
0
5% 1/20W MF 0201
37 35 29 OUT SMC_PME_S4_WAKE_L
To SMC
PLACE_NEAR=R4841.1:1.5MM
(TPAD_SPI_INT_S4_WAKE_L_CONN)

TPAD_INTWAKE:SHARED
R4844
0
5% 1/20W MF 0201
PLACE_NEAR=J4800.8:1.5MM

TPAD_INTWAKE:SHARED
Q4800
DMN32D2LFB4
DFN1006H4-3
SYM_VER_3
63 62 60 56 39 38 34 19 18 15 PP3V3_S3
15 OUT TPAD_SPI_INT_L
To PCH
PLACE_NEAR=R4842.2:5MM

TPAD_INTWAKE:SPLIT
R4842
0
5% 1/20W MF 0201
PLACE_NEAR=R4843.2:1.5MM

62 60 56 37 36 34 29 PP3V3_S4
C4841 0.1UF 10% 16V CERM-X5R 0201
BYPASS=U4810:3mm

CRITICAL
74LVC2G08GT
SOT833
U4810
57 35 34 29 18 13 IN PM_SLP_S4_L
15 IN TPAD_USB_IF_EN
From PCH
(TPAD_USB_IF_EN_CONN)
NOSTUFF
R4810
100K
5% 1/20W MF 201

CKPLUS_WAIVE=UNCONNECTED_PINS
74LVC2G08GT
SOT833
U4810
57 35 34 29 18 13 IN PM_SLP_S4_L
15 IN TPAD_SPI_IF_EN
From PCH
(TPAD_SPI_IF_EN_CONN)
CKPLUS_WAIVE=UNCONNECTED_PINS

63 62 60 56 39 38 34 19 18 15 PP3V3_S3
R4860
100K
5% 1/20W MF 201
Q4860
DMN32D2LFB4
DFN1006H4-3
SYM_VER_3
36 30 27 18 17 15 13 12 11 8 59 57 54 43 42 41 40 39 38 37 PP3V3_S0
15 IN TPAD_SPI_CS_L
TPAD_SPI_CS_CONN_L

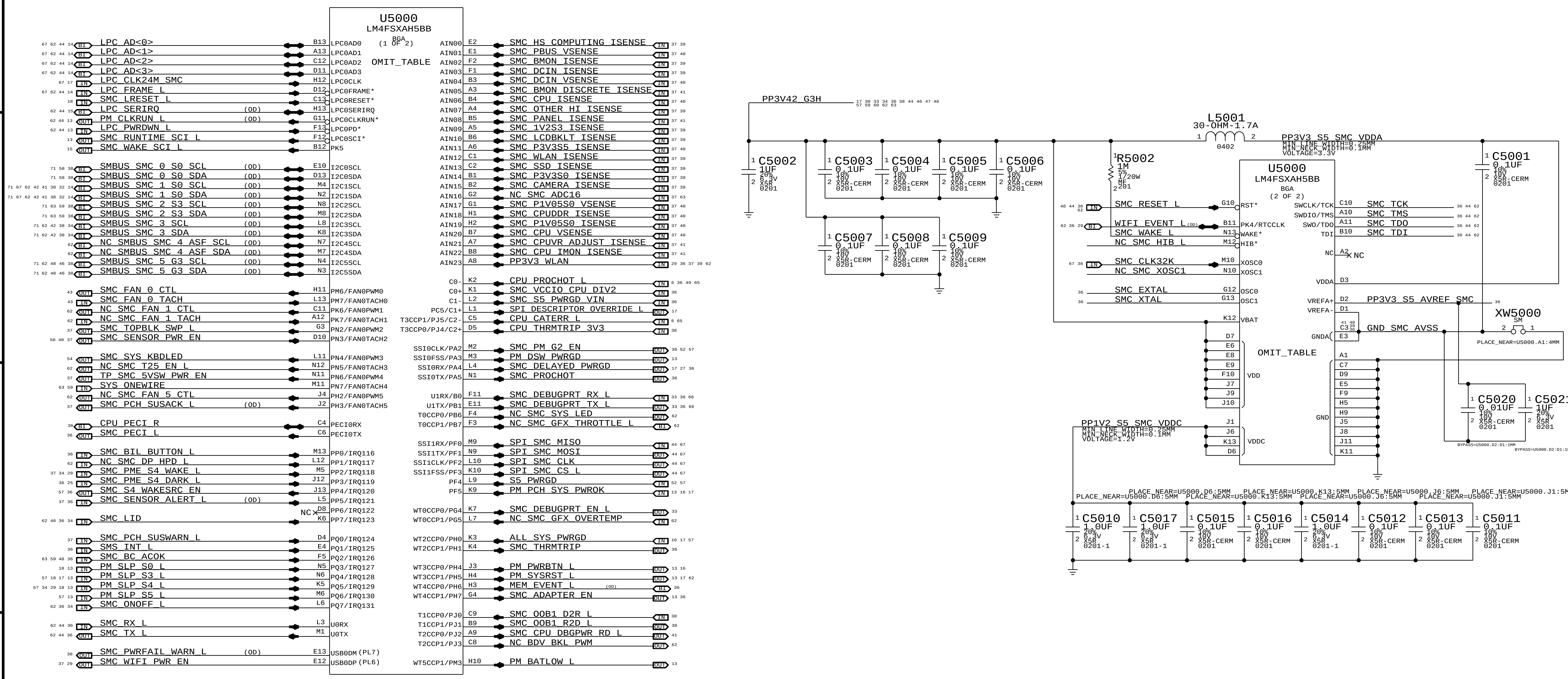
R4850
33
5% 1/20W MF 201
PLACE_NEAR=J4800.2:2.54mm
15 OUT TPAD_SPI_MISO
62 46 36 35 34 IN SMC_LID
62 TPAD_SPI_MISO_R
R4851
33
5% 1/20W MF 201
PLACE_NEAR=J4800.7:2.54mm
15 66 IN TPAD_SPI_CLK
62 TPAD_SPI_CLK_R
R4852
33
5% 1/20W MF 201
PLACE_NEAR=J4800.9:2.54mm
15 66 IN TPAD_SPI_MOSI
62 TPAD_SPI_MOSI_R
R4853
33
5% 1/20W MF 201
PLACE_NEAR=J4800.12:2.54mm
62 TPAD_SPI_CS_R_L
62 TPAD_SPI_IF_EN_CONN
62 TPAD_SPI_INT_S4_WAKE_L_CONN
62 PP5V_S4_IPD
62 TPAD_USB_IF_EN_CONN
71 62 42 38 35 34 BI SMBUS_SMC_3_SDA
71 62 42 38 35 34 BI SMBUS_SMC_3_SCL
62 36 34 OUT SMC_LSOC_RST_L
(=PP3V42_G3H_IPD)
62 36 35 34 OUT SMC_ONOFF_L

CRITICAL
518S0884
J4800
TF13BS-20S-0.4SH
F-RT-SM-1
22
1 SMC_LID
2 TPAD_SPI_MISO_R
3
4 USB_TPAD_P
66 62 14 BI
5 USB_TPAD_N
66 62 14 BI
6
7 TPAD_SPI_CLK_R
8 TPAD_WAKE_L
9 TPAD_SPI_MOSI_R
10 PP3V3_S4_IPD
11 TPAD_SPI_CS_R_L
12 TPAD_SPI_IF_EN_CONN
13 TPAD_SPI_INT_S4_WAKE_L_CONN
14 PP5V_S4_IPD
15 TPAD_USB_IF_EN_CONN
16 SMBUS_SMC_3_SDA
17 SMBUS_SMC_3_SCL
18 SMC_LSOC_RST_L
19 (=PP3V42_G3H_IPD)
20 SMC_ONOFF_L
21

SMBUS_SMC_3_SDA 34 35 38 42 62 71
SMBUS_SMC_3_SCL 34 35 38 42 62 71
SMC_ONOFF_L 34 35 36 62
SMC_LID 34 35 36 46 62
SMC_LSOC_RST_L 34 36 62

NOSTUFF C4832 100PF 5% 25V NP0-CERM 0201 BYPASS=J4800.6:1.5MM
NOSTUFF C4833 100PF 5% 25V NP0-CERM 0201 BYPASS=J4800.5:1.5MM
C4834 100PF 5% 25V NP0-CERM 0201 BYPASS=J4800.4:1.5MM
C4835 100PF 5% 25V NP0-CERM 0201 BYPASS=J4800.3:1.5MM
C4836 100PF 5% 25V NP0-CERM 0201 BYPASS=J4800.1:1.5MM

SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013
PAGE TITLE
IPD Connector
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 48 OF 120
SHEET 34 OF 73


U5000
LM4FSXAH5BB
BGA
(1 OF 2)
OMIT_TABLE
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_CLK24M_SMC
LPC_FRAME_L
SMC_LRESET_L
LPC_SERIRQ
PM_CLKRUN_L
LPC_PWRDWN_L
SMC_RUNTIME_SCI_L
SMC_WAKE_SCI_L
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA
SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA
SMBUS_SMC_2_S3_SCL
SMBUS_SMC_2_S3_SDA
SMBUS_SMC_3_SCL
SMBUS_SMC_3_SDA
NC_SMBUS_SMC_4_ASF_SCL
NC_SMBUS_SMC_4_ASF_SDA
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
SMC_FAN_0_CTL
SMC_FAN_0_TACH
NC_SMC_FAN_1_CTL
NC_SMC_FAN_1_TACH
SMC_TOPBLK_SWP_L
SMC_SENSOR_PWR_EN
SMC_SYS_KBDLED
NC_SMC_T25_EN_L
TP_SMC_5VSW_PWR_EN
SYS_ONEWIRE
NC_SMC_FAN_5_CTL
SMC_PCH_SUSACK_L
CPU_PECI_R
SMC_PECI_L
SMC_BIL_BUTTON_L
NC_SMC_DP_HPD_L
SMC_PME_S4_WAKE_L
SMC_PME_S4_DARK_L
SMC_S4_WAKESRC_EN
SMC_SENSOR_ALERT_L
SMC_LID
SMC_PCH_SUSWARN_L
SMS_INT_L
SMC_BC_ACOK
PM_SLP_S0_L
PM_SLP_S3_L
PM_SLP_S4_L
PM_SLP_S5_L
SMC_ONOFF_L
SMC_RX_L
SMC_TX_L
SMC_PWRFAIL_WARN_L
SMC_WIFI_PWR_EN
SMC_HS_COMPUTING_ISENSE
SMC_PBUS_VSENSE
SMC_BMON_ISENSE
SMC_DCIN_ISENSE
SMC_DCIN_VSENSE
SMC_BMON_DISCRETE_ISENSE
SMC_CPU_ISENSE
SMC_OTHER_HI_ISENSE
SMC_PANEL_ISENSE
SMC_1V2S3_ISENSE
SMC_LCDBKLT_ISENSE
SMC_P3V3S5_ISENSE
SMC_WLAN_ISENSE
SMC_SSD_ISENSE
SMC_P3V3S0_ISENSE
SMC_CAMERA_ISENSE
NC_SMC_ADC16
SMC_P1V05S0_VSENSE
SMC_CPUDDR_ISENSE
SMC_P1V05S0_ISENSE
SMC_CPU_VSENSE
SMC_CPUVR_ADJUST_ISENSE
SMC_CPU_IMON_ISENSE
PP3V3_WLAN
CPU_PROCHOT_L
SMC_VCCIO_CPU_DIV2
SMC_S5_PWRGD_VIN
SPI_DESCRIPTOR_OVERRIDE_L
CPU_CATERR_L
CPU_THRMTRIP_3V3
SMC_PM_G2_EN
PM_DSW_PWRGD
SMC_DELAYED_PWRGD
SMC_PROCHOT
SMC_DEBUGPRT_RX_L
SMC_DEBUGPRT_TX_L
NC_SMC_SYS_LED
NC_SMC_GFX_THROTTLE_L
SPI_SMC_MISO
SPI_SMC_MOSI
SPI_SMC_CLK
SPI_SMC_CS_L
S5_PWRGD
PM_PCH_SYS_PWROK
SMC_DEBUGPRT_EN_L
NC_SMC_GFX_OVERTEMP
ALL_SYS_PWRGD
SMC_THRMTRIP
PM_PWRBTN_L
PM_SYSRST_L
MEM_EVENT_L
SMC_ADAPTER_EN
SMC_OOB1_D2R_L
SMC_OOB1_R2D_L
SMC_CPU_DBGPWR_RD_L
NC_BDV_BKL_PWM
PM_BATLOW_L
PP3V42_G3H
L5001
30-OHM-1.7A
0402
PP3V3_S5_SMC_VDDA
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=3.3V
C5002
1UF
C5003
C5004
C5005
C5006
0.1UF
C5007
C5008
C5009
R5002
1M
U5000
LM4FSXAH5BB
BGA
(2 OF 2)
SMC_RESET_L
WIFI_EVENT_L
SMC_WAKE_L
NC_SMC_HIB_L
SMC_CLK32K
NC_SMC_XOSC1
SMC_EXTAL
SMC_XTAL
SMC_TCK
SMC_TMS
SMC_TDO
SMC_TDI
C5001
0.1UF
PP3V3_S5_AVREF_SMC
XW5000
SM
GND_SMC_AVSS
PLACE_NEAR=U5000.A1:4MM
OMIT_TABLE
C5020
0.01UF
C5021
1UF
PP1V2_S5_SMC_VDDC
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=1.2V
C5010
C5017
C5015
C5016
C5014
C5012
C5013
C5011

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE

SMC

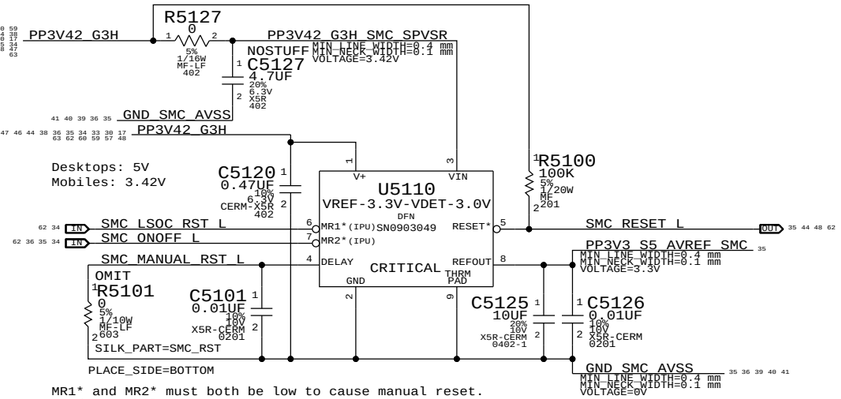
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

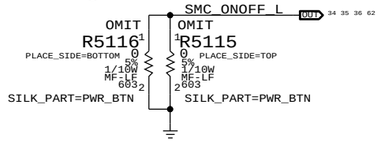
BRANCH <BRANCH>

SMC Reset "Button", Supervisor & AVREF Supply



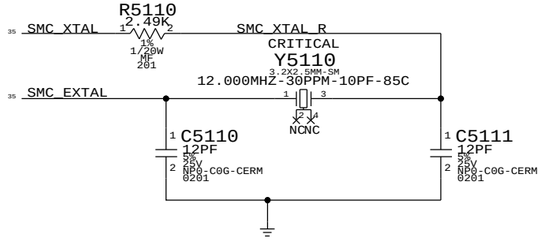
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

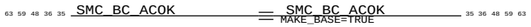
Debug Power "Buttons"

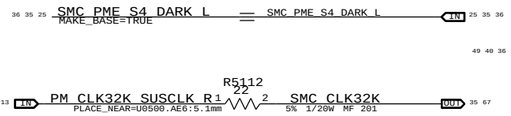


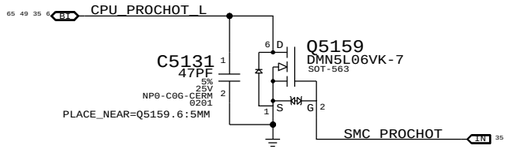
SMC Crystal Circuit

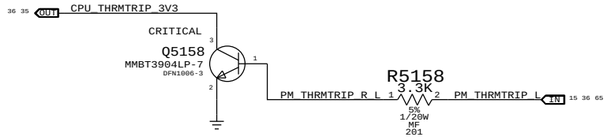
SMC USB Clock require these crystal
values:5,6,8,10,12,16,18,20,24,25 MHz

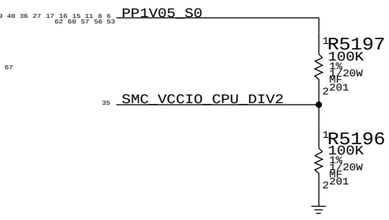




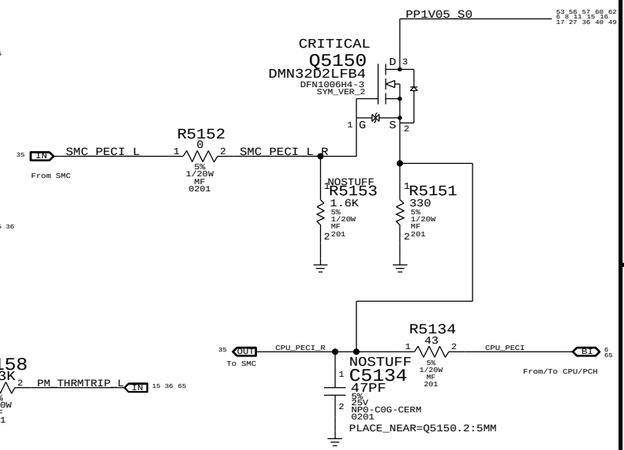


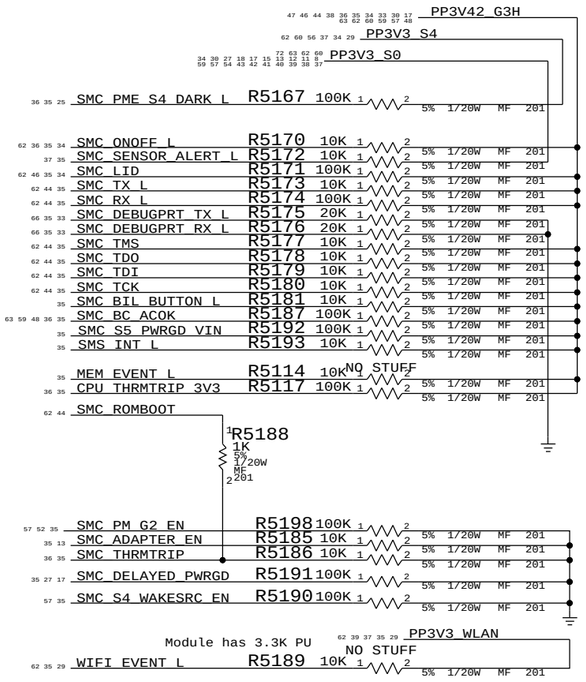






SMC12 PECI Support





SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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BRANCH: <BRANCH>
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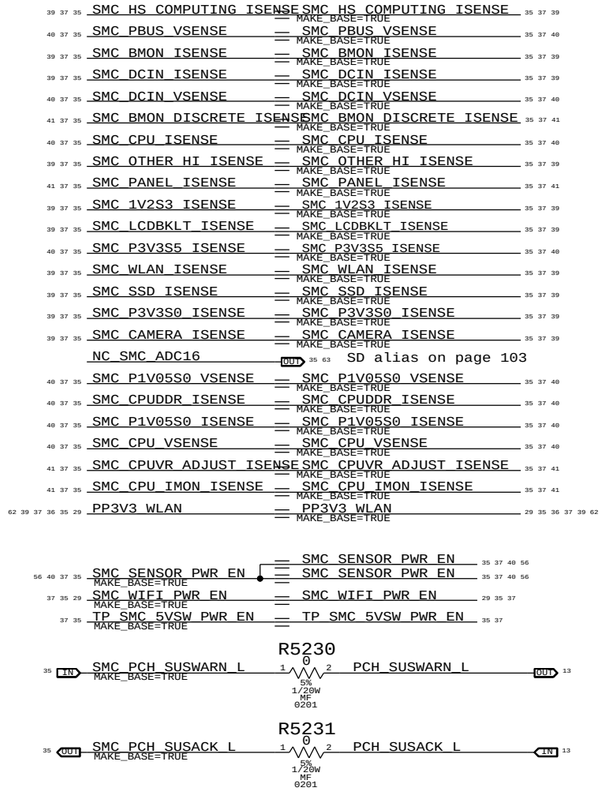
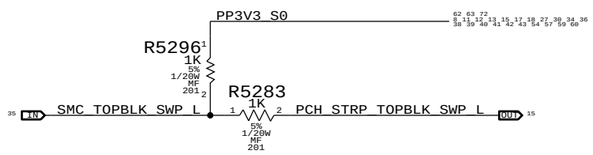
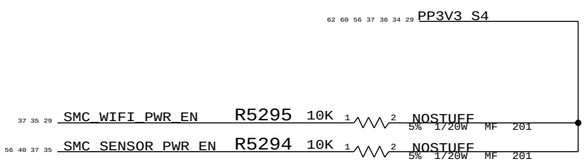
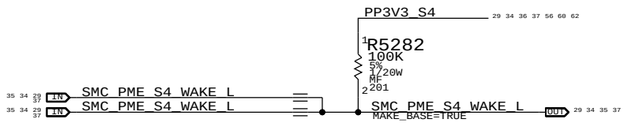
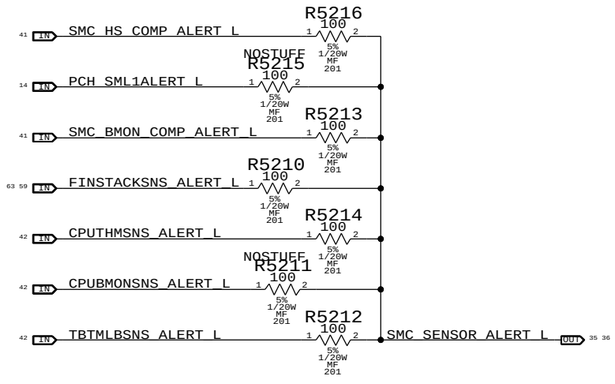


Top-Block Swap









SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE

SMC Project Support

Apple Inc.

DRAWING NUMBER	<SCH_NUM>
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REVISION	<E4LABEL>
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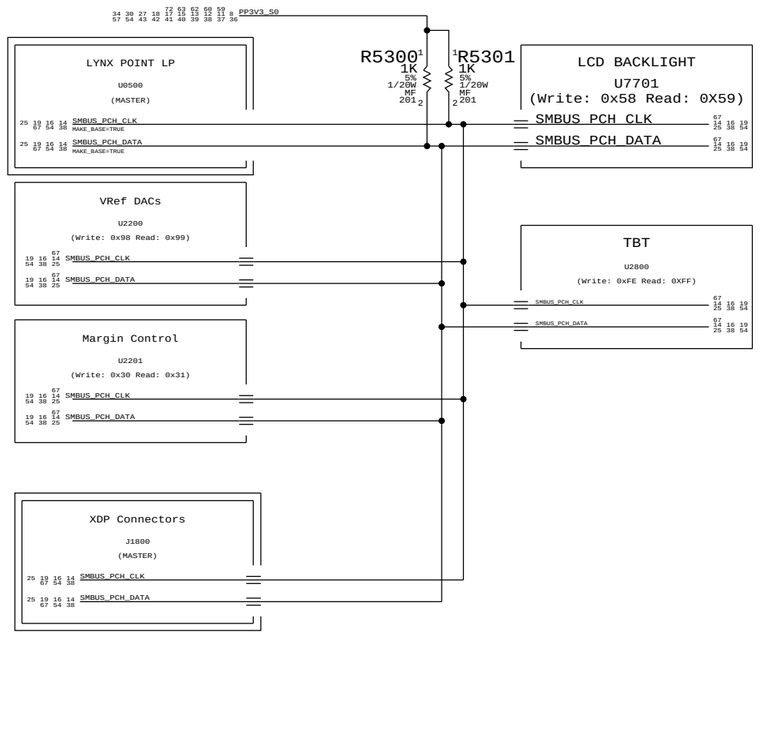
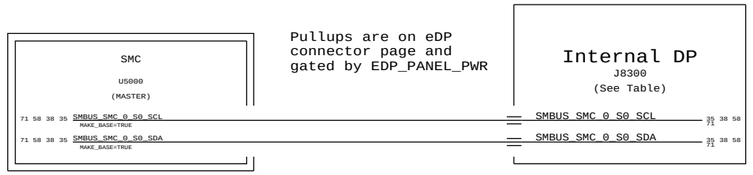
LYNX POINT LP S0 SMBus "0" Connections



SMC "0" SMBus S0 Connections

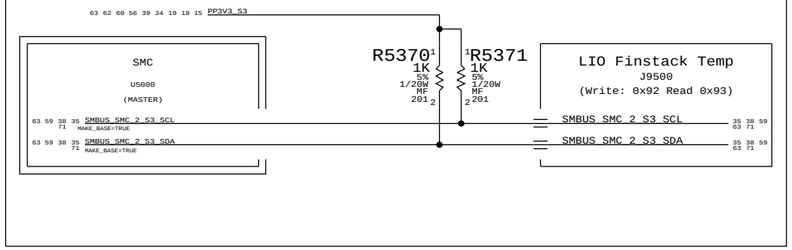


(* = Multiple options)

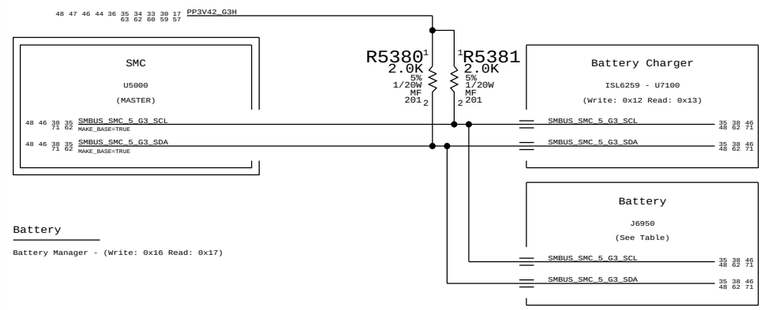
Internal DP

	J43		J41		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

SMC "2" SMBus S3 Connections



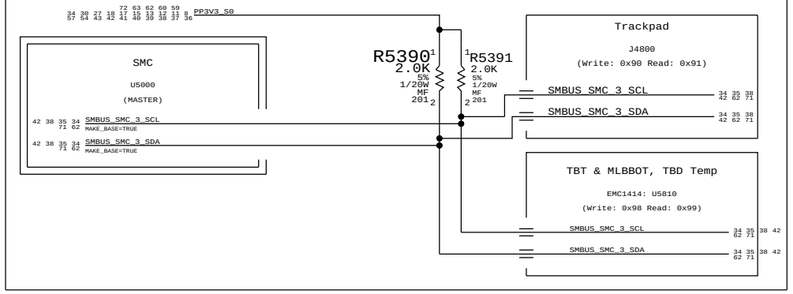
SMC "5" SMBus G3H Connections



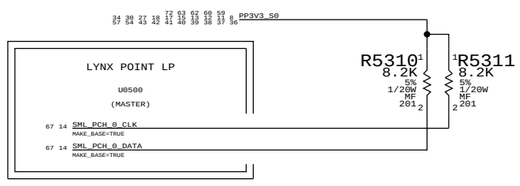
Battery

Battery Manager - (Write: 0x16 Read: 0x17)

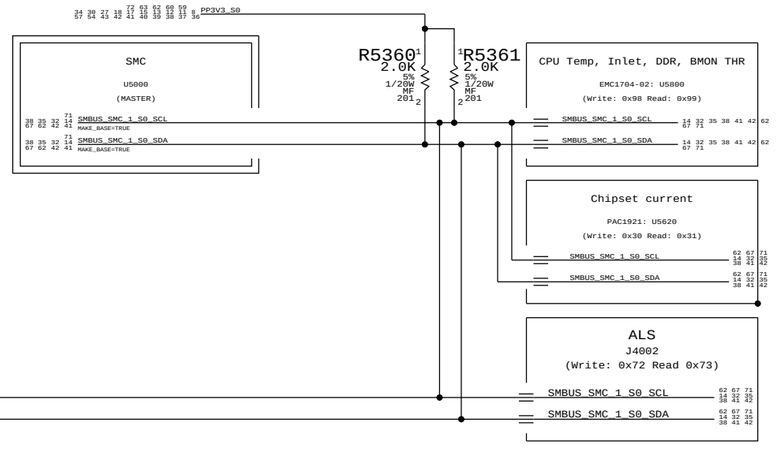
SMC "3" SMBus S0 Connections



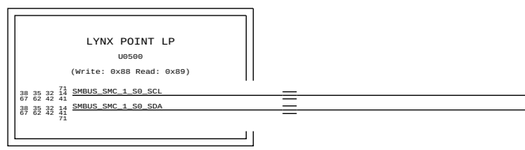
LYNX POINT LP S0 "SMLink 0" Connections



SMC S0 "1" SMBus Connections



LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to
access PCH

SYNC_MASTER=J43_MLB SYNC_DATE=09/28/2012

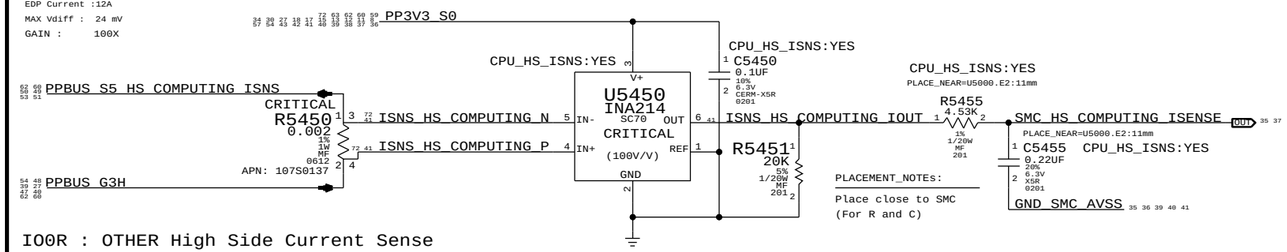
PAGE TITLE
SMBus Connections

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 53 OF 120
SHEET 38 OF 73

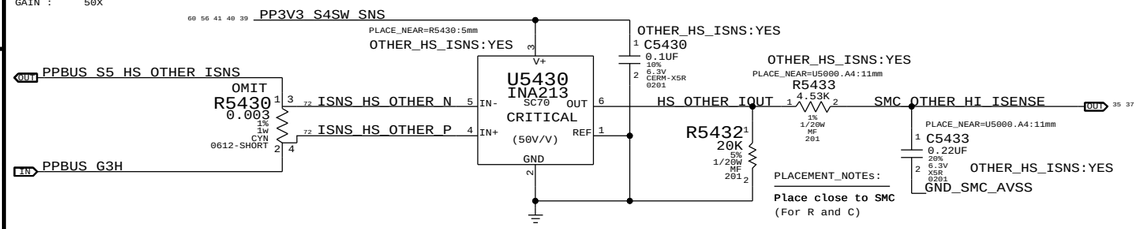
IC0R : COMPUTING High Side Current Sense

EDP Current :12A
MAX Vdiff : 24 mV
GAIN : 100X



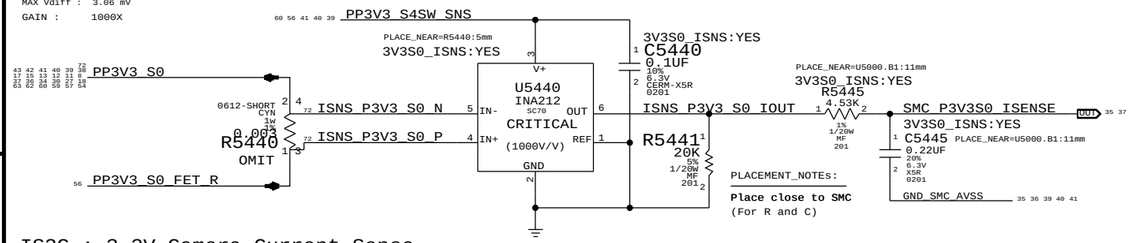
IO0R : OTHER High Side Current Sense

EDP Current :10.75A
MAX Vdiff : 53.75 mV
GAIN : 50X



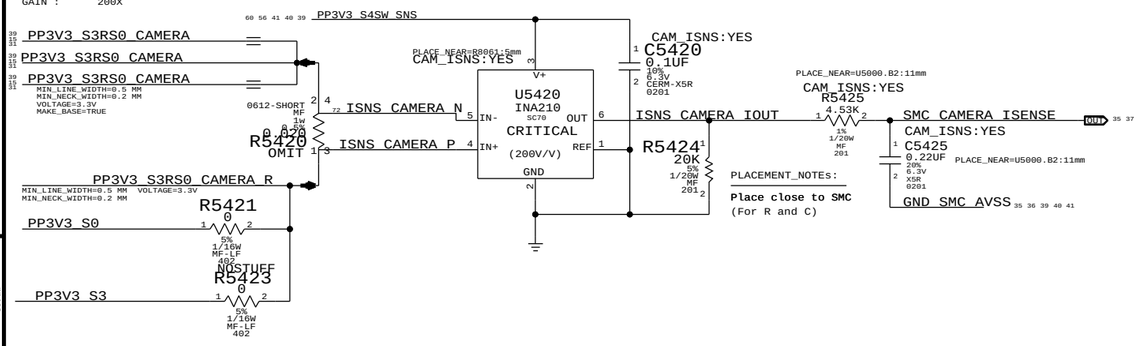
IR0C : 3.3V S0 FET Current Sense

EDP Current :1.02A
MAX Vdiff : 3.06 mV
GAIN : 1000X

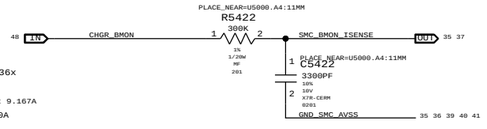


IS2C : 3.3V Camera Current Sense

EDP Current : 0.82A
MAX Vdiff : 16.36 mV
GAIN : 200X

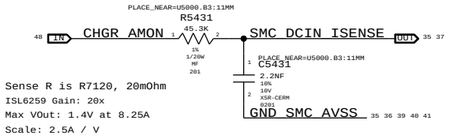


CHARGER BMON High Side Current Sense



ISL6259 Gain: 36x
Scale: 2.78A / V
Max VOut: 3.3V at 9.167A
EDP Current: 310A

DC-IN (AMON) Current Sense

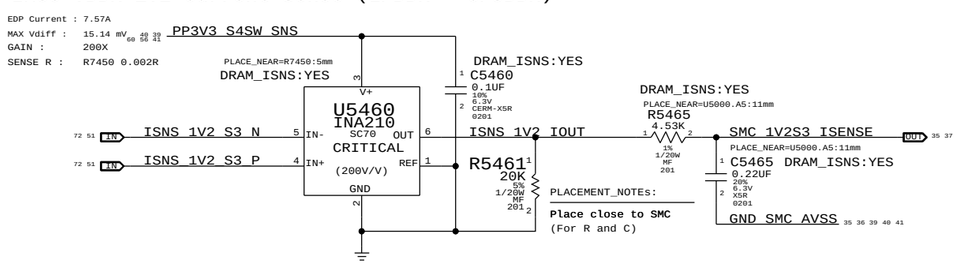


Sense R is R7120, 20mOhm
ISL6259 Gain: 20x
Max VOut: 1.4V at 8.25A
Scale: 2.5A / V
EDP Current: 3.5A

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES,SENSE,0.003OHM,1W,4-TERM,1%,0612,TFT	R5480	CRITICAL	

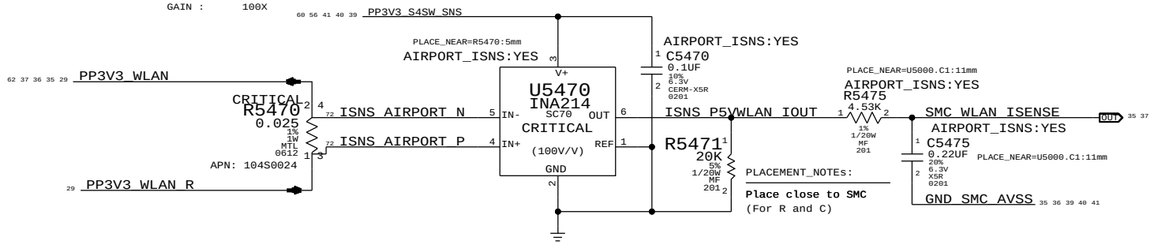
IM3C :DDR 1V2 Current Sense (LPDDR + CPUDDR)

EDP Current : 7.57A
MAX Vdiff : 15.14 mV
GAIN : 200X
SENSE R : R7450 0.002R



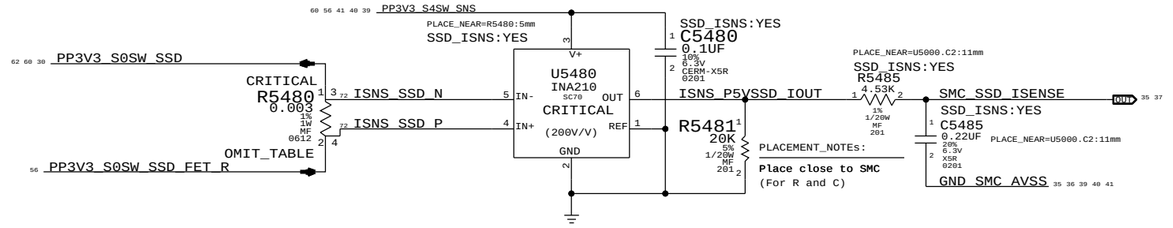
IAPC :AirPort Current Sense

EDP Current : 1.00A
MAX Vdiff : 25 mV
GAIN : 100X



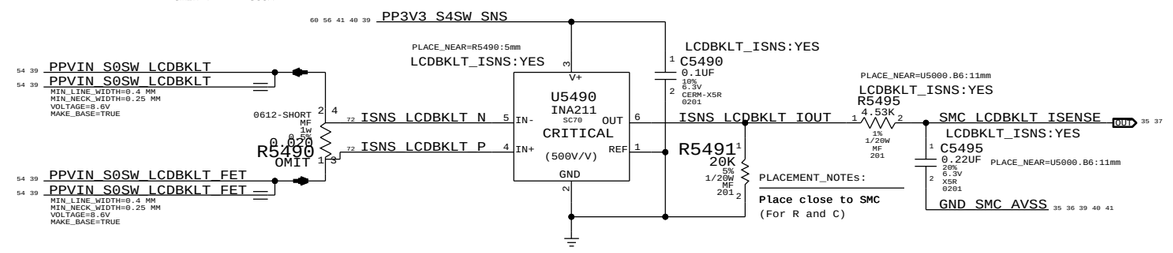
ISDC : SSD Current Sense

EDP Current : 3.00A
MAX Vdiff : 15 mV
GAIN : 200X



IBLC : LCD Backlight Driver Input Current Sense

EDP Current : 0.67A
MAX Vdiff : 0.06 mV
GAIN : 500X



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		SSD_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

SYNC_MASTER=SID J41 SYNC_DATE=02/26/2013
PAGE TITLE: High Side Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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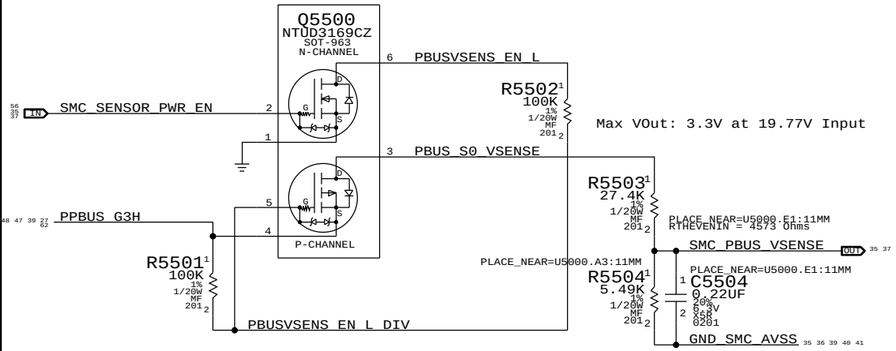
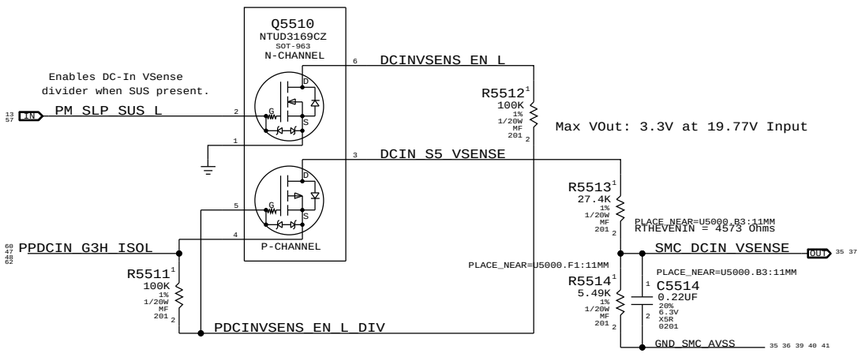
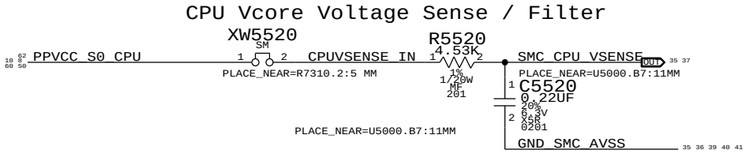
VP0R: PBUS Voltage Sense Enable & Filter



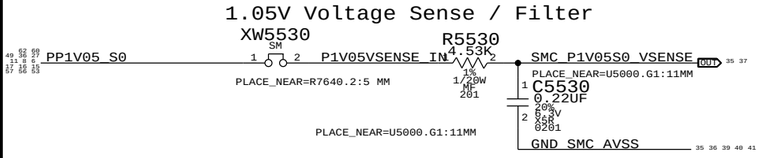
VD0R: DC-In Voltage Sense Enable & Filter



CPU Vcore Voltage Sense / Filter

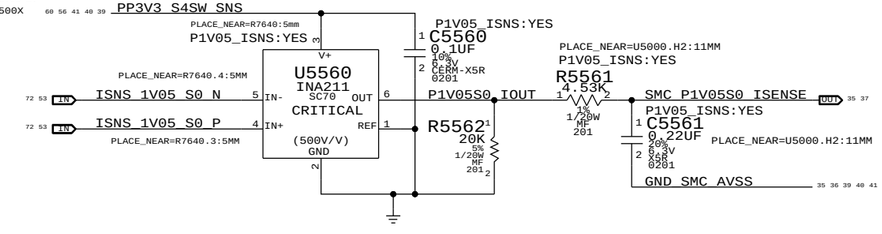


1.05V Voltage Sense / Filter

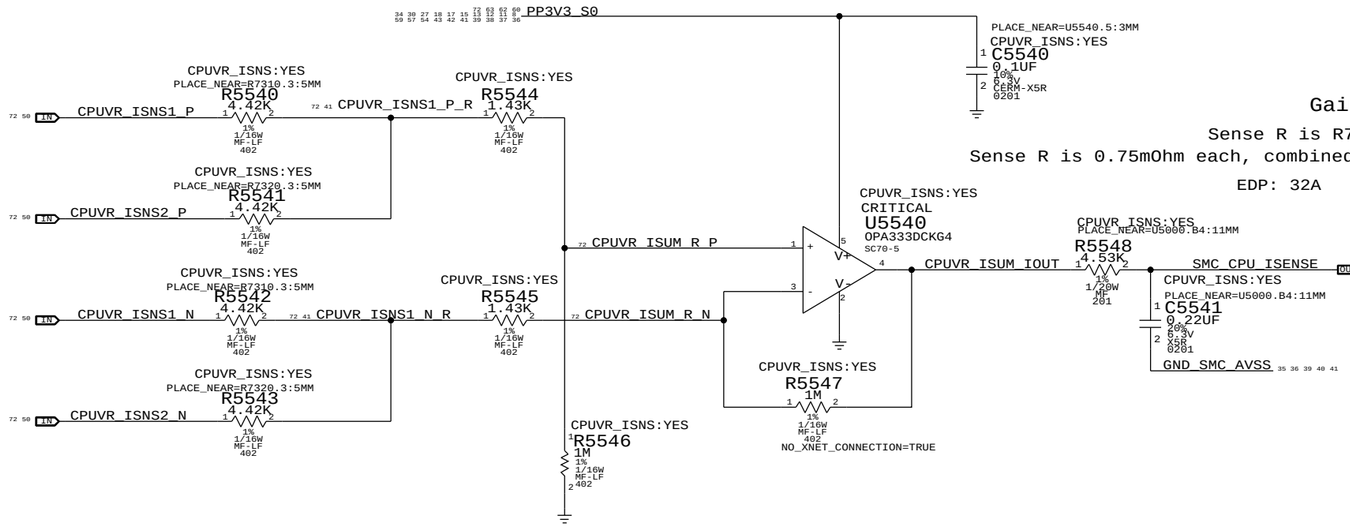


IC1C: 1.05V S0 CURRENT SENSE / FILTER

EDP Current : 1A
MAX Vdiff : 5.65 mV
GAIN : 500X

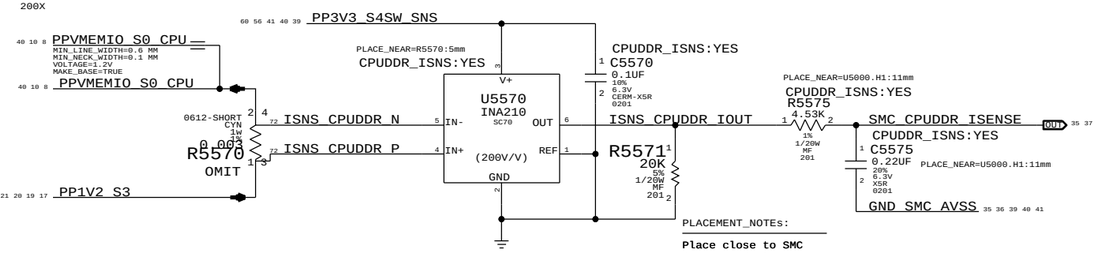


ICS0 : CPU VCore Load Side Current Sense



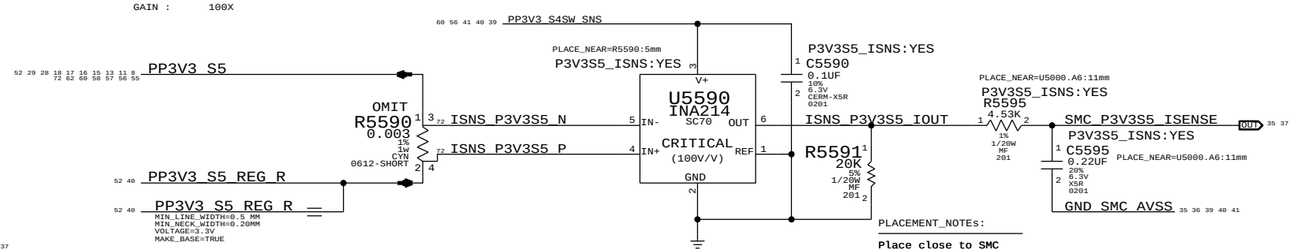
IM0C : CPU DDR Current Sense

EDP Current : 3.00A
MAX Vdiff : 12.60 mV
GAIN : 200X



IR5C :3.3 S5 REG Current Sense

EDP Current : 3.00A
MAX Vdiff : 30.00 mV
GAIN : 100X



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5541		CPUVR_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5561		P1V05_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5595		P3V3S5_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5575		CPUDDR_ISNS:NO

SYNC_MASTER=SID_J41 SYNC_DATE=02/26/2013

PAGE TITLE

Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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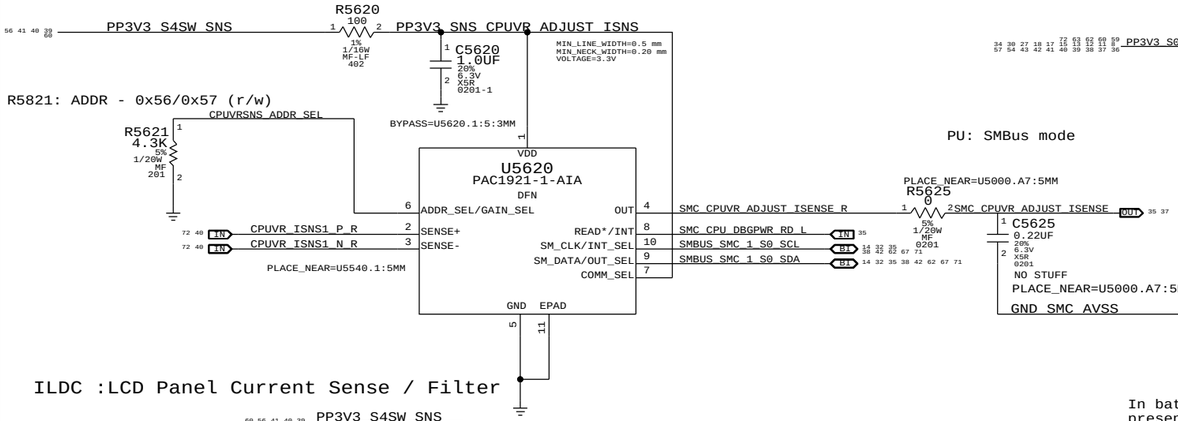
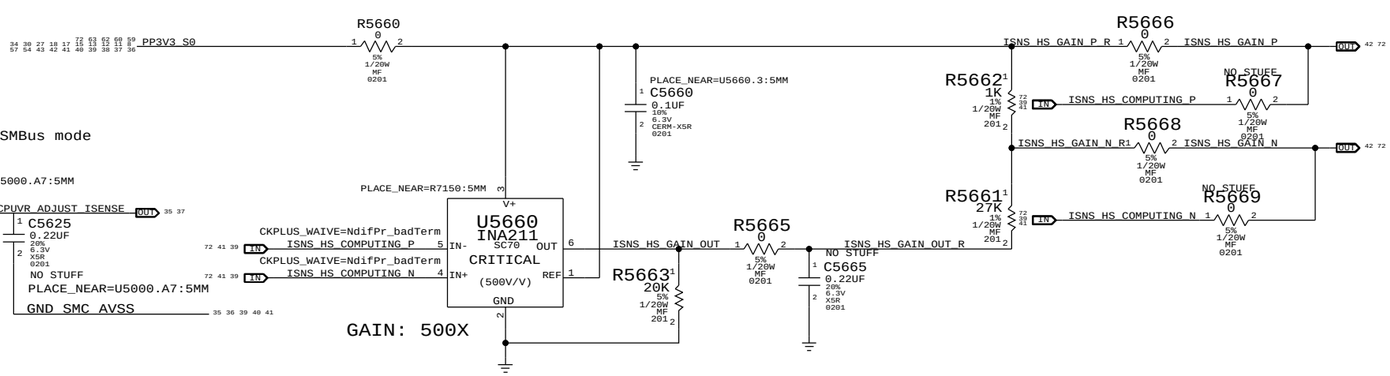
ICS3 : Adjustable Gain CPU VR Current



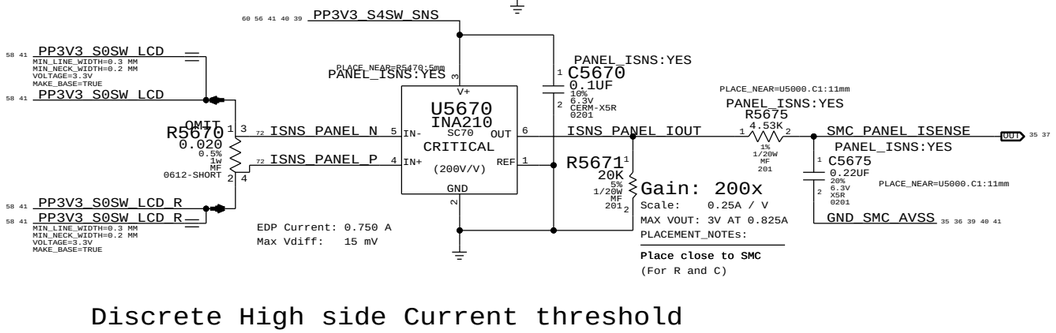
Sense Pins gain stage for U5800 (EMC1704)



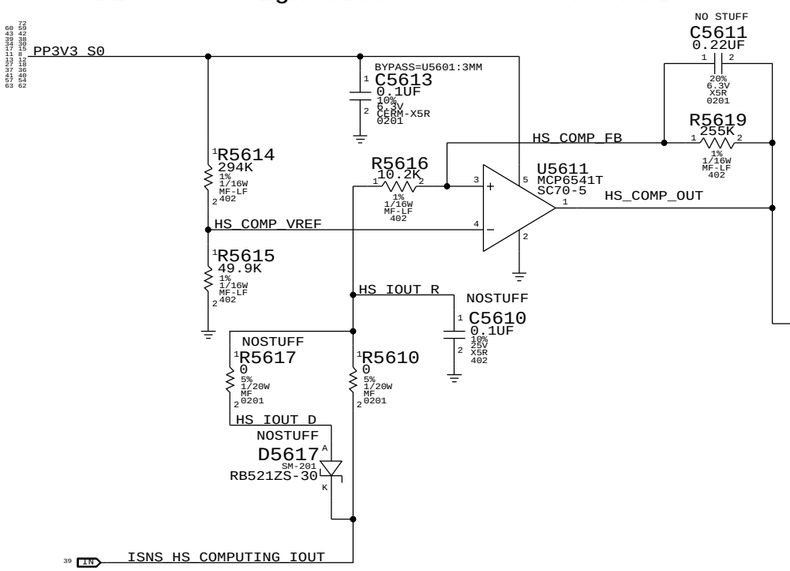
In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

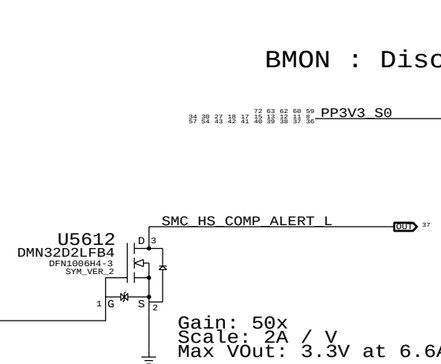
With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800.
This will set the minumum current threshold at 0.100mA

ILDC :LCD Panel Current Sense / Filter



Discrete High side Current threshold

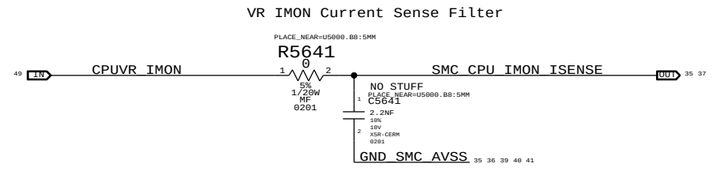




BMON : Discrete BMON Current Sense / Filter

CHGR_CSO_R_P/N are swapped on purpose to measure power into the system

VR IMON Current Sense Filter



Vref = 0.406mV Vth = 0.442 = 1A from Battery
Vtl = 0.290mv = 0.687A from battery
Hysteresis TBD based on RC value changes

Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5675		PANEL_ISNS:NO

SYNC_MASTER=SID_J41 SYNC_DATE=02/26/2013

PAGE TITLE: Debug Sensors 1

Apple Inc.

DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
PAGE	56 OF 120
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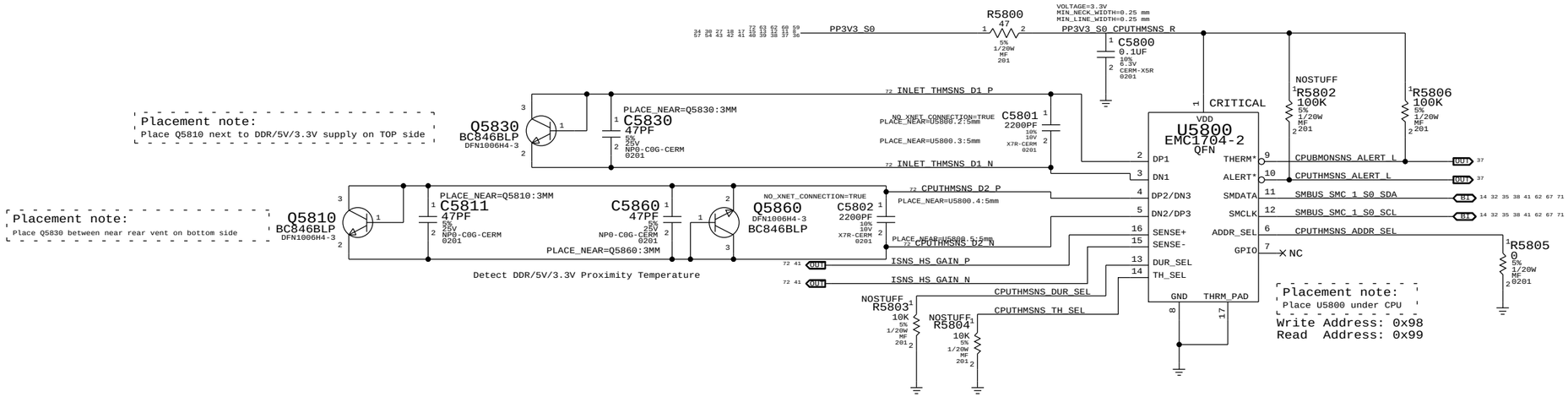
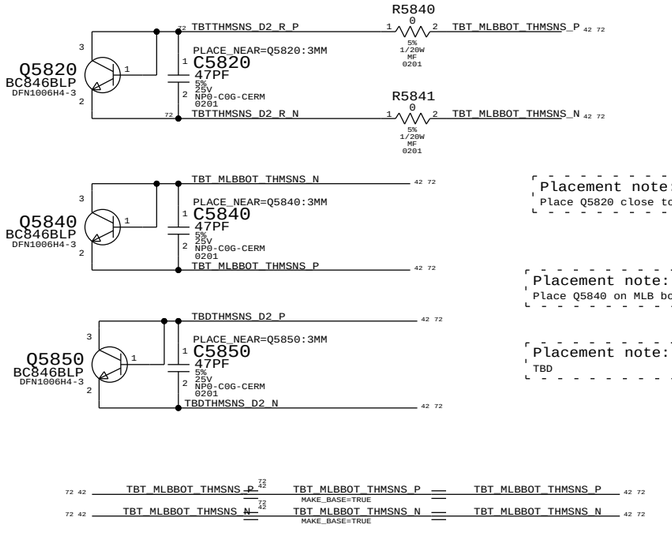
CPU Proximity, Inlet ,DDR and BMON THR Sensor



TBT,MLB Bottom Proximity Sensors

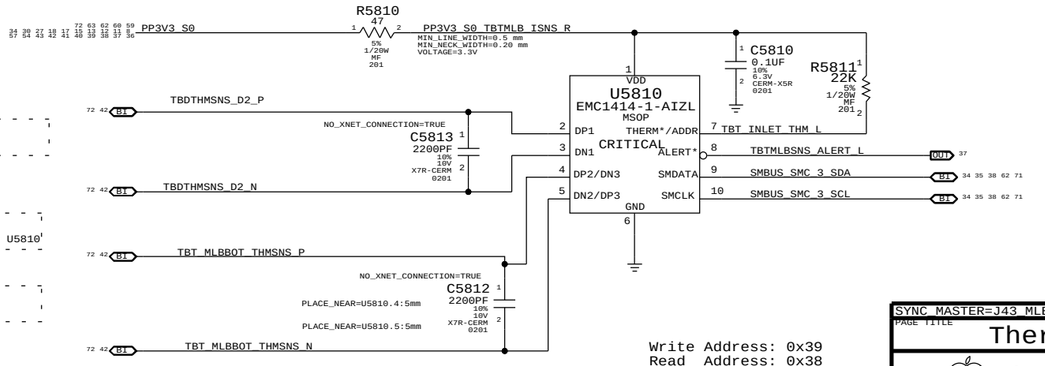


Placement note:
Place Q5820 close to TBT on TOP side

Placement note:
Place Q5840 on MLB bottom side opposite U5810

Placement note:
TBD

TBT, MLBBOT and TBD Temp Sensor



Write Address: 0x39
Read Address: 0x38

SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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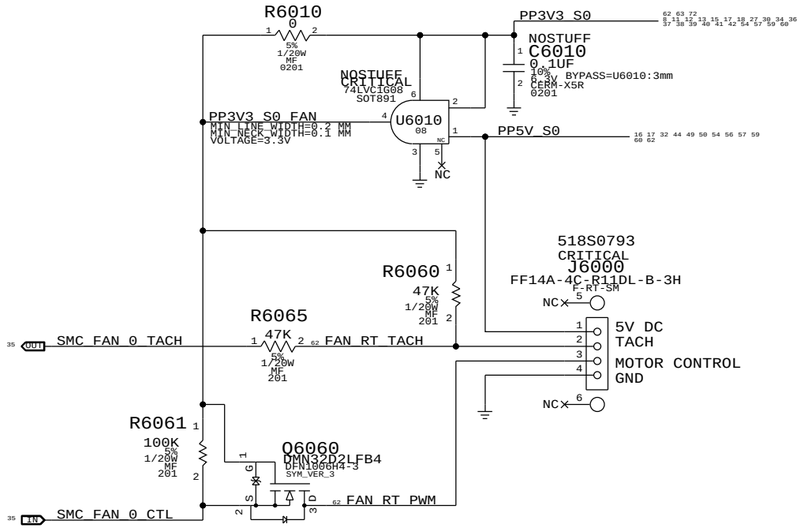
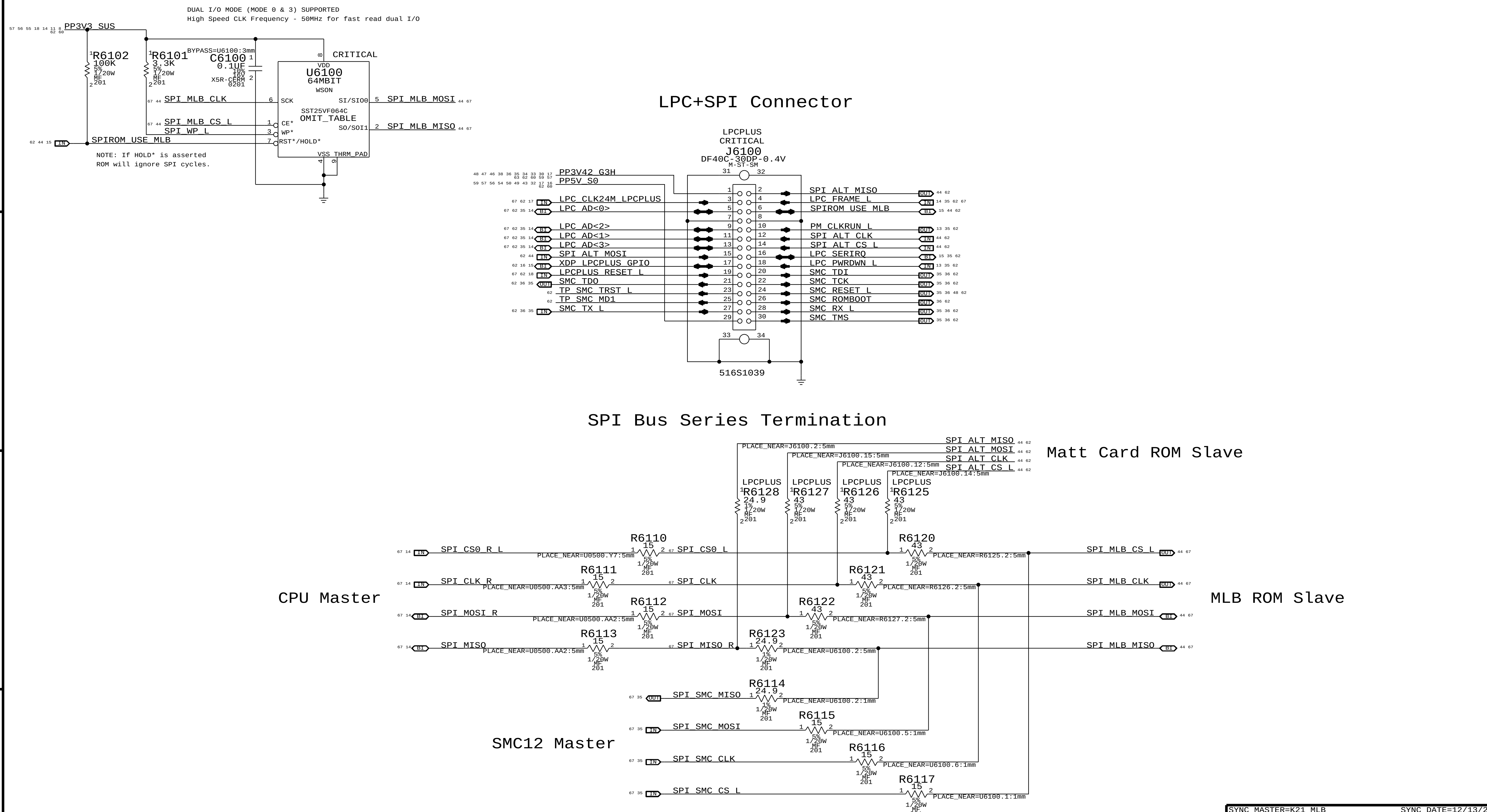
FAN CONNECTOR



SYNC_MASTER=J43_MLB	SYNC_DATE=09/13/2012
PAGE TITLE: Fan	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 60 OF 120
	SHEET: 43 OF 73



DUAL I/O MODE (MODE 0 & 3) SUPPORTED
High Speed CLK Frequency - 50MHz for fast read dual I/O
PP3V3_SUS
R6102 100K 5% 1/20W MF 201
R6101 3.3K 5% 1/20W MF 201
BYPASS=U6100:3mm
C6100 0.1UF 10% 16V X5R-CERM 0201
CRITICAL
U6100 64MBIT WSON
VDD
SCK
CE*
WP*
RST*/HOLD*
SI/SIO0
SO/SOI1
VSS THRM_PAD
SST25VF064C
OMIT_TABLE
SPI_MLB_CLK
SPI_MLB_CS_L
SPI_WP_L
SPIROM_USE_MLB
SPI_MLB_MOSI
SPI_MLB_MISO
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles.
LPC+SPI Connector
LPCPLUS
CRITICAL
J6100
DF40C-30DP-0.4V
M-ST-SM
PP3V42_G3H
PP5V_S0
LPC_CLK24M_LPCPLUS
LPC_AD<0>
LPC_AD<2>
LPC_AD<1>
LPC_AD<3>
SPI_ALT_MOSI
XDP_LPCPLUS_GPIO
LPCPLUS_RESET_L
SMC_TDO
TP_SMC_TRST_L
TP_SMC_MD1
SMC_TX_L
SPI_ALT_MISO
LPC_FRAME_L
SPIROM_USE_MLB
PM_CLKRUN_L
SPI_ALT_CLK
SPI_ALT_CS_L
LPC_SERIRQ
LPC_PWRDWN_L
SMC_TDI
SMC_TCK
SMC_RESET_L
SMC_ROMBOOT
SMC_RX_L
SMC_TMS
516S1039
SPI Bus Series Termination
PLACE_NEAR=J6100.2:5mm
PLACE_NEAR=J6100.15:5mm
PLACE_NEAR=J6100.12:5mm
PLACE_NEAR=J6100.14:5mm
SPI_ALT_MISO
SPI_ALT_MOSI
SPI_ALT_CLK
SPI_ALT_CS_L
Matt Card ROM Slave
LPCPLUS R6128 24.9 1% 1/20W MF 201
LPCPLUS R6127 43 5% 1/20W MF 201
LPCPLUS R6126 43 5% 1/20W MF 201
LPCPLUS R6125 43 5% 1/20W MF 201
CPU Master
SPI_CS0_R_L
SPI_CLK_R
SPI_MOSI_R
SPI_MISO
R6110 15
R6111 15
R6112 15
R6113 15
PLACE_NEAR=U0500.Y7:5mm
PLACE_NEAR=U0500.AA3:5mm
PLACE_NEAR=U0500.AA2:5mm
PLACE_NEAR=U0500.AA2:5mm
SPI_CS0_L
SPI_CLK
SPI_MOSI
SPI_MISO_R
R6120 43
R6121 43
R6122 43
R6123 24.9
PLACE_NEAR=R6125.2:5mm
PLACE_NEAR=R6126.2:5mm
PLACE_NEAR=R6127.2:5mm
PLACE_NEAR=U6100.2:5mm
SPI_MLB_CS_L
SPI_MLB_CLK
SPI_MLB_MOSI
SPI_MLB_MISO
MLB ROM Slave
SMC12 Master
SPI_SMC_MISO
SPI_SMC_MOSI
SPI_SMC_CLK
SPI_SMC_CS_L
R6114 24.9
R6115 15
R6116 15
R6117 15
PLACE_NEAR=U6100.2:1mm
PLACE_NEAR=U6100.5:1mm
PLACE_NEAR=U6100.6:1mm
PLACE_NEAR=U6100.1:1mm

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

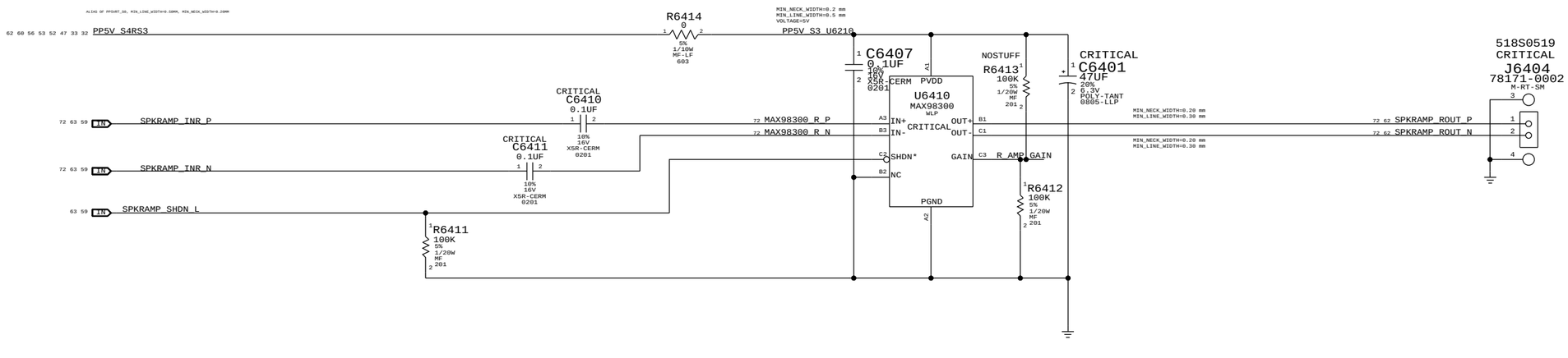
BRANCH <BRANCH>

SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB

Right Speaker Connector



SYNC_MASTER=J43_MLB SYNC_DATE=09/04/2012

PAGE TITLE: Audio: Speaker Amp

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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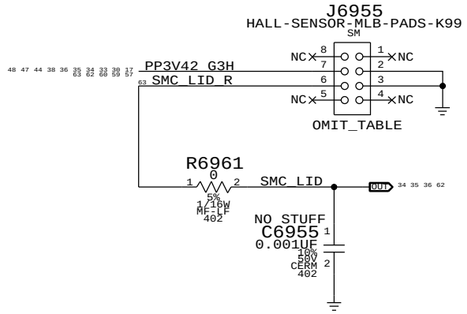
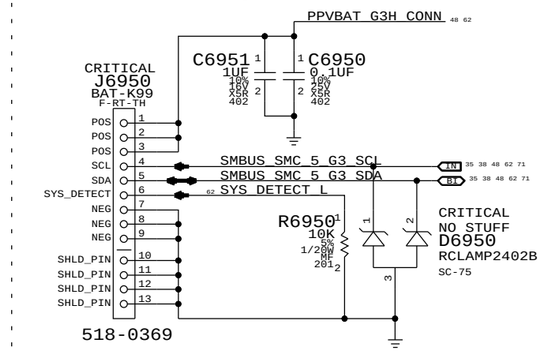
Hall Effect Sensor



11"-Specific Battery Connector



SYNC_MASTER=MASTER	SYNC_DATE=MASTER
PAGE TITLE	Battery Connector & Hall Effect
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 69 OF 120
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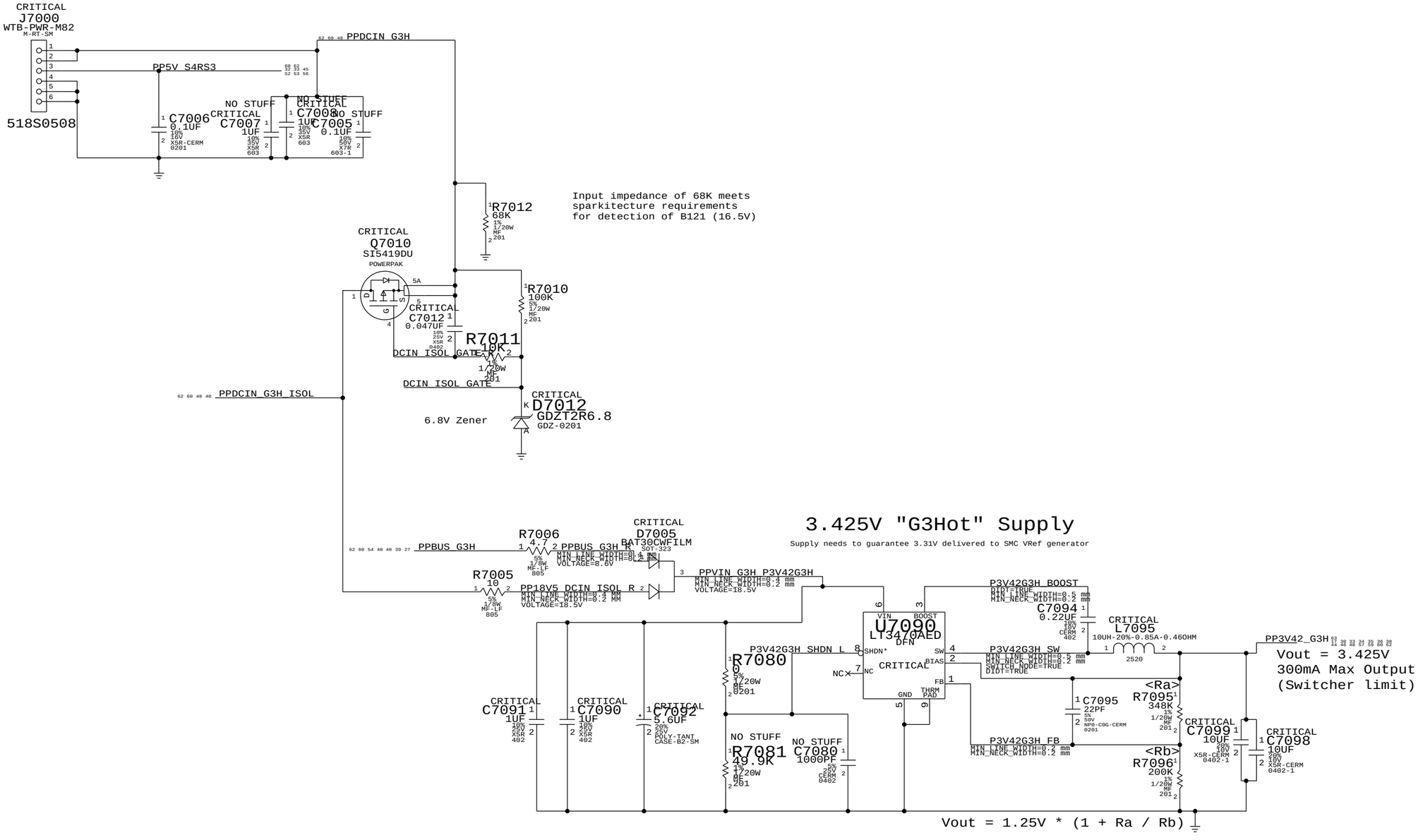
MLB to LIO Power Cable Connector



SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE: DC-In & G3H Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 70 OF 120

SHEET: 47 OF 73

Reverse-Current Protection

Need to stuff R7192 if either PP5V5_DCIN:YES or PP5V5_VDDP are used!

Inrush Limiter

5.5v "G3Hot" Supply
For Erp Lot6 spec

FROM ADAPTER

PPDCIN_G3H

R7185 470K 1/20W MF 201

C7185 0.1UF 10% 25V X5R 402

CRITICAL Q7180 IRF9395TRPBF DIRECTFET-MC

CHGR_AGATE_DIV

R7186 332K 1% 1/20W MF 201

PPDCIN_G3H_INRUSH

R7180 100K 5% 1/20W MF 201

C7184 4.7UF 10% 25V X5R-CERM 0603

CHGR_SGATE_DIV

R7181 62K 5% 1/20W MF 201

PPDCIN_G3H_ISOL

CRITICAL D7105 BAT30CWFILM SOT-323

PPCHGR_DCIN_D_R

PP5V5_DCIN:NO R7105 20 5% 1/10W MF-LF 603

(CHGR_DCIN)

(CHGR_AGATE)

(CHGR_SGATE)

ACIN pin threshold is 3.2V, +/- 50mV

DIVIDER SETS ACIN THRESHOLD AT 13.55V

30mA max load

PP5V1_CHGR_VDD

R7101 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP

C7101 1UF 10% 10V X5R 402

PP3V42_G3H

R7110 130K 1% 1/20W MF 201

NO STUFF R7102 100K 5% 1/20W MF 201

R7100 0 5% 1/20W MF 0201

SMC_RESET_L

U7100 ISL6259 TQFN

VDD	19		
VDDP	20		
VHST	12		
DCIN	2		CHGR_DCIN
SMB_RST_N	13		
SCL	11		SMBUS_SMC_5_G3_SCL
SDA	10		SMBUS_SMC_5_G3_SDA
VFRQ	4		CHGR_VFRQ
CELL	6		CHGR_CELL
ACIN	3		CHGR_ACIN
ICOMP	5		CHGR_ICOMP
VCOMP	7		CHGR_VCOMP
VNEG	8		CHGR_VNEG
CSOP	18		CHGR_CSO_P
CSON	17		CHGR_CSO_N
SGATE	26		CHGR_SGATE
AGATE	1		CHGR_AGATE
CSIP	28		CHGR_CSI_P
CSIN	27		CHGR_CSI_N
BOOT	25		CHGR_BOOT
UGATE	24		CHGR_UGATE
PHASE	23		CHGR_PHASE
LGATE	21		CHGR_LGATE
BGATE	16		CHGR_BGATE
20V/V AMON	9		CHGR_AMON
36V/V BMON	15		CHGR_BMON
(0.8) ACOK	14		SMC_BC_ACOK
(AGND) THRM_PAD	29		
PGND	22		

Float CELL for 1S

R7113 100 5% 1/20W MF 201

R7115 255K 1% 1/20W MF 201

CHGR_VCOMP_R

R7142 1K 5% 1/20W MF 201

R7116 10K 1% 1/20W MF 201

CHGR_ICOMP_R

CHGR_VNEG_R

R7111 46.4K 1% 1/20W MF 201

C7115 470PF 10% 16V X5R-X7R-CERM 0201

C7116 470PF 10% 16V X5R-X7R-CERM 0201

C7150 0.47UF 10% 10V X5R 0402

C7102 1UF 10% 10V X5R 402

XW7100 SM PLACE_NEAR=U7100.22:1mm

C7142 0.1UF 10% 6.3V CERM-X5R 0201

C7111 0.01UF 10% 10V XSR-CERM 0201

C7100 1UF 10% 10V X5R 402-1

C7105 0.22UF 10% 50V X5R-CERM 0603-1

C7126 1000PF 10% 16V X7R-CERM 0201

GND_CHGR_AGND

R7121 10 5% 1/20W MF 201

R7122 10 5% 1/20W MF 201

C7120 0.047UF 10% 16V X7R-CERM 0402

C7122 0.1UF 10% 25V X5R 402

C7121 0.1UF 10% 25V X5R 402

CRITICAL R7120 0.020 0.5% 1W MF-LF 0612

CHGR_CSI_R_P

CHGR_CSI_R_N

PPDCIN_G3H_CHGR

C7125 0.22UF 10% 10V CERM 402

CRITICAL Q7130 RJK03P0DPA WPAK

SWITCH_NODE=TRUE DIDT=TRUE

CRITICAL L7130 4.7UH-17A PIMC104T4R7MN-SM

CRITICAL F7140 8AMP-24V 1206

PPBUS_G3H

TO SYSTEM

Max Current = 8A

f = 400 kHz

PPVBAT_G3H_CHGR_REG

C7140 62UF-0.023OHM 20% 11V TANT-POLY CASE-B2S-1

C7141 62UF-0.023OHM 20% 11V TANT-POLY CASE-B2S-1

C7143 62UF-0.023OHM 20% 11V TANT-POLY CASE-B2S-1

C7145 1000PF 10% 16V X7R-CERM 0201

R7150 0.01 0.5% 1W MF 0612-4

R7151 2.2 5% 1/20W MF 201

R7152 0 5% 1/20W MF 0201

CRITICAL Q7155 SI7137DP SO-8

PPVBAT_G3H_CHGR_R

TO/FROM BATTERY

PPVBAT_G3H_CONN

C7117 10UF 10% 25V X5R 805

C7114 1UF 10% 25V X5R 603-1

C7113 0.1UF 10% 25V X5R 402

C7112 0.01UF 10% 25V X7R 402

* R7151 HAS 2.2OHM TO COMPENSATE UNBALANCED VOLTAGE
DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

PP5V5_DCIN:YES

R7190 0 5% 1/16W MF-LF 402

CHGR_DCIN

PP5V5_VDDP

R7191 0 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP

NO STUFF R7192 0 5% 1/10W MF-LF 603

PPCHGR_DCIN_D_R

CHGR_DCIN_D

NO STUFF C7190 4.7UF 10% 25V X5R-CERM 0603

U7190 LT3470A DFN

VIN BOOST SHDN* SW BIAS NC FB THRM GND PAD

NO STUFF C7194 0.22UF 10% 10V CERM 402

P5V1_BOOST

P5V1_SW

P5V1_FB

CRITICAL L7195 10UH-20%-0.85A-0.46OHM 2520

NO STUFF C7195 22PF 5% 50V NPO-C0G-CERM 0201

NO STUFF <Ra> R7195 681K 1% 1/20W MF 201

NO STUFF <Rb> R7196 200K 1% 1/20W MF 201

Vout = 1.25V * (1 + Ra / Rb)

NO STUFF CRITICAL C7198 10UF 20% 10V X5R 603

NO STUFF CRITICAL C7199 10UF 20% 10V X5R 603

PP5V5_CHGR_VDDP

Vout = 5.50V
200MA MAX OUTPUT
(Switcher limit)

SYNC_MASTER=J43_MLB	SYNC_DATE=09/14/2012
PAGE TITLE	PBus Supply & Battery Charger
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 71 OF 120
	SHEET 48 OF 73

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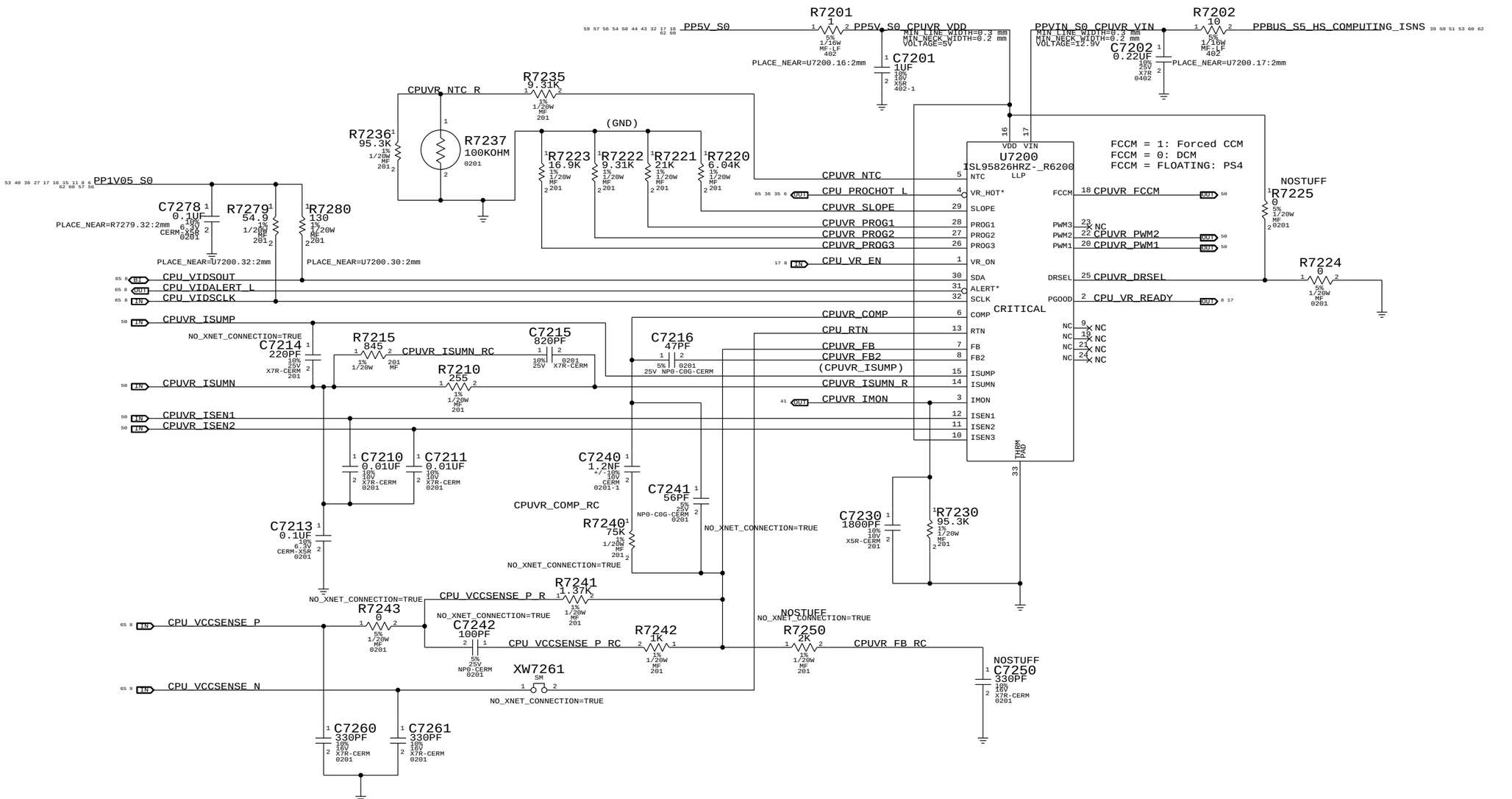
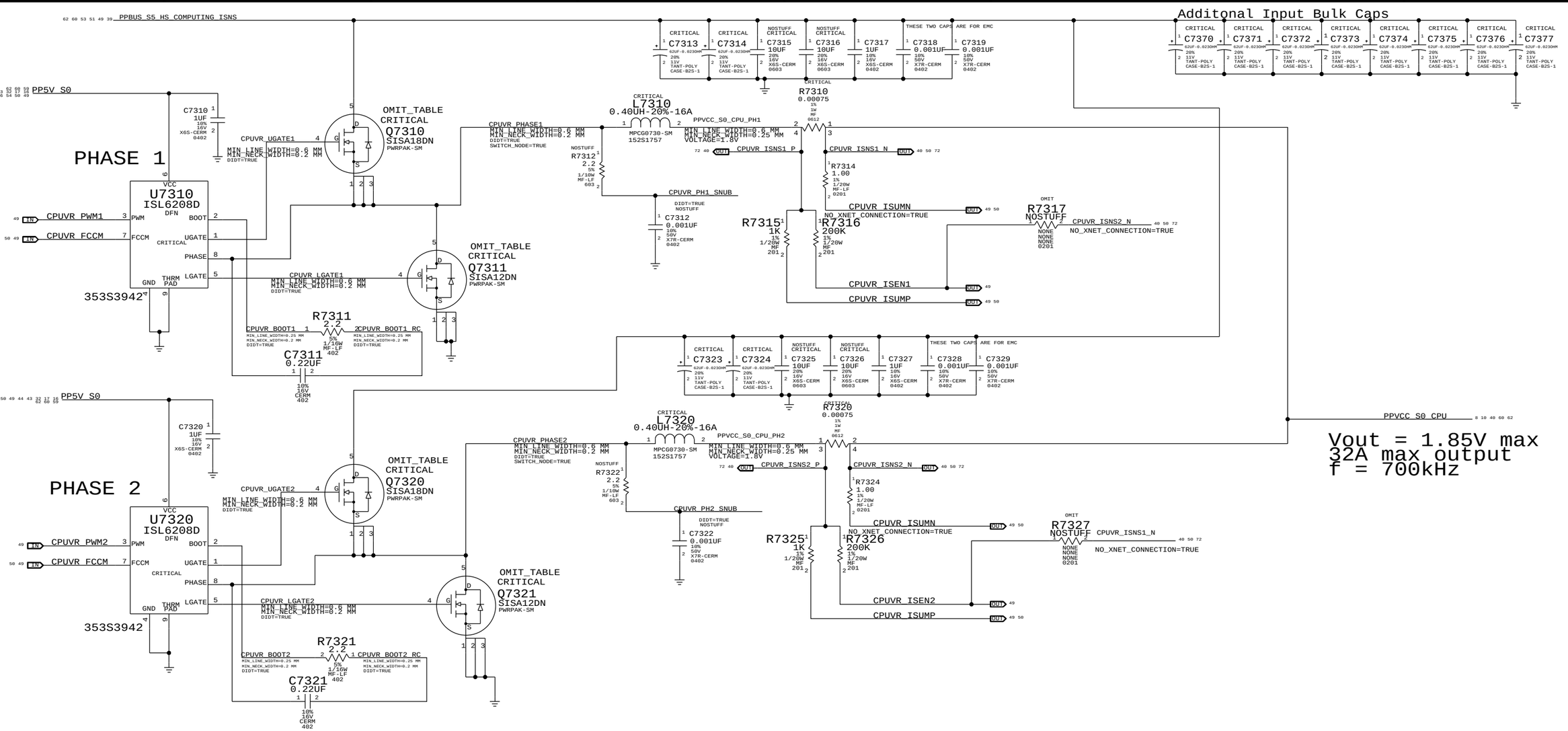


SYNC_MASTER=J43_MLB	SYNC_DATE=10/09/2012
PAGE TITLE	CPU VR12.6 VCC Regulator IC
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 72 OF 120
	SHEET: 49 OF 73



SYNC_MASTER=J43_MLB SYNC_DATE=09/21/2012

PAGE TITLE
CPU VR12.5 VCC Power Stage

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 73 OF 120
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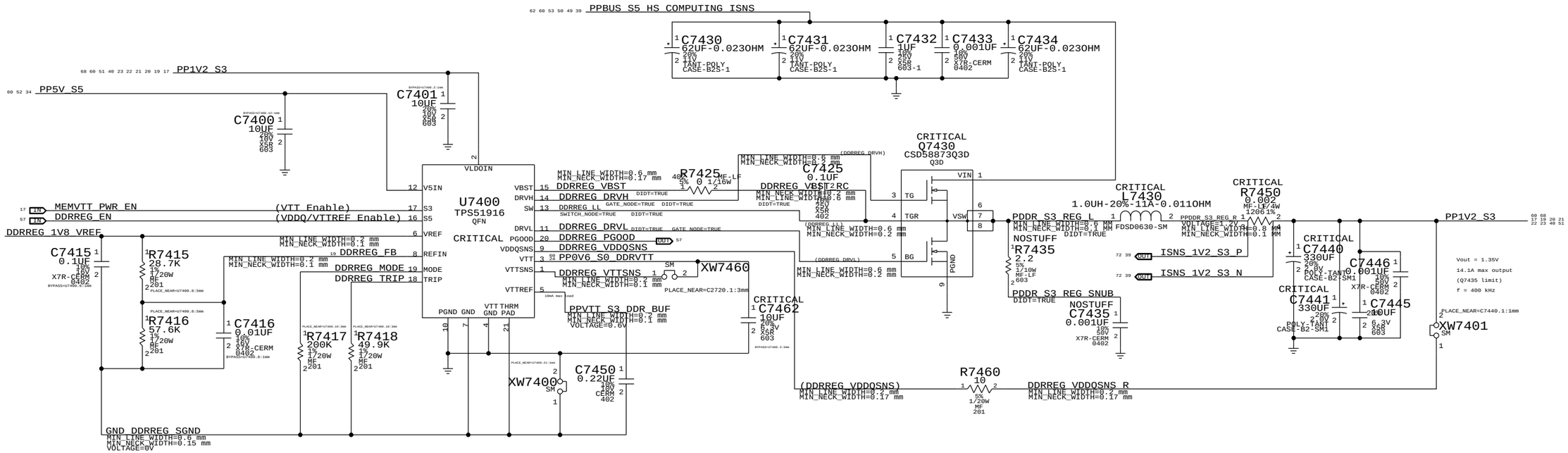

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PAGE TITLE

LPDDR3 Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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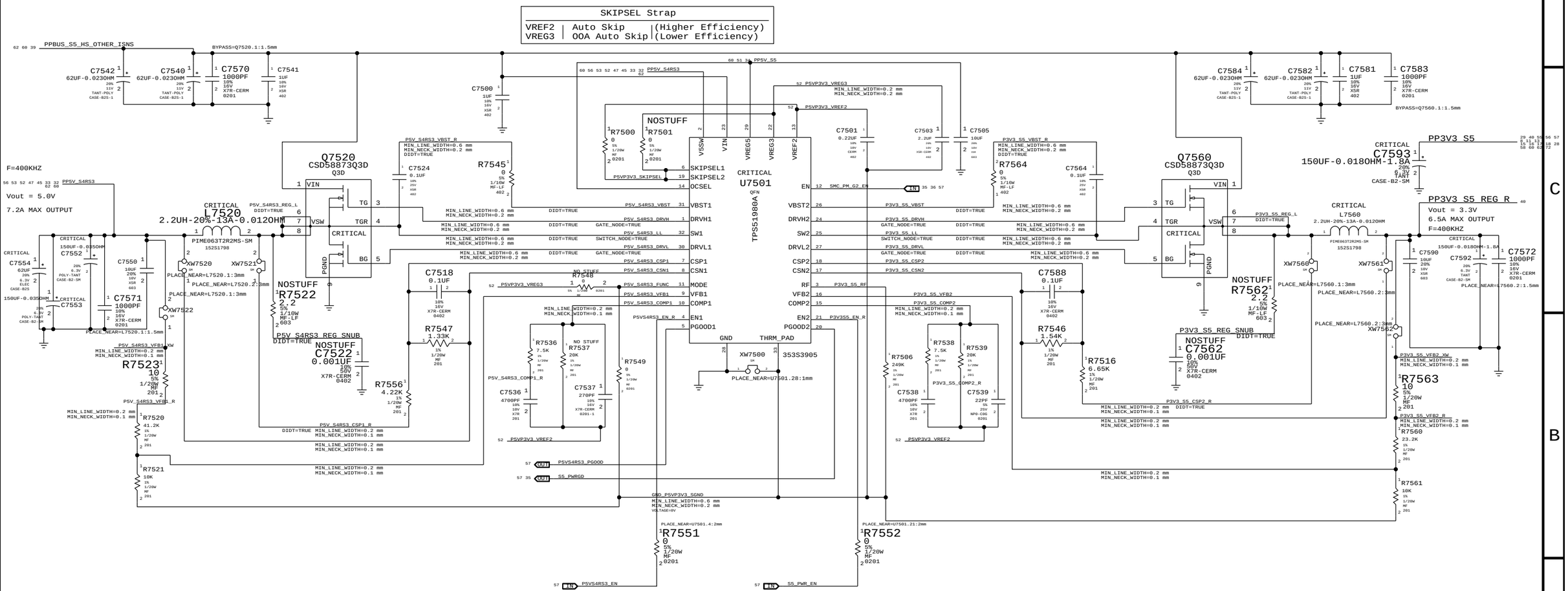
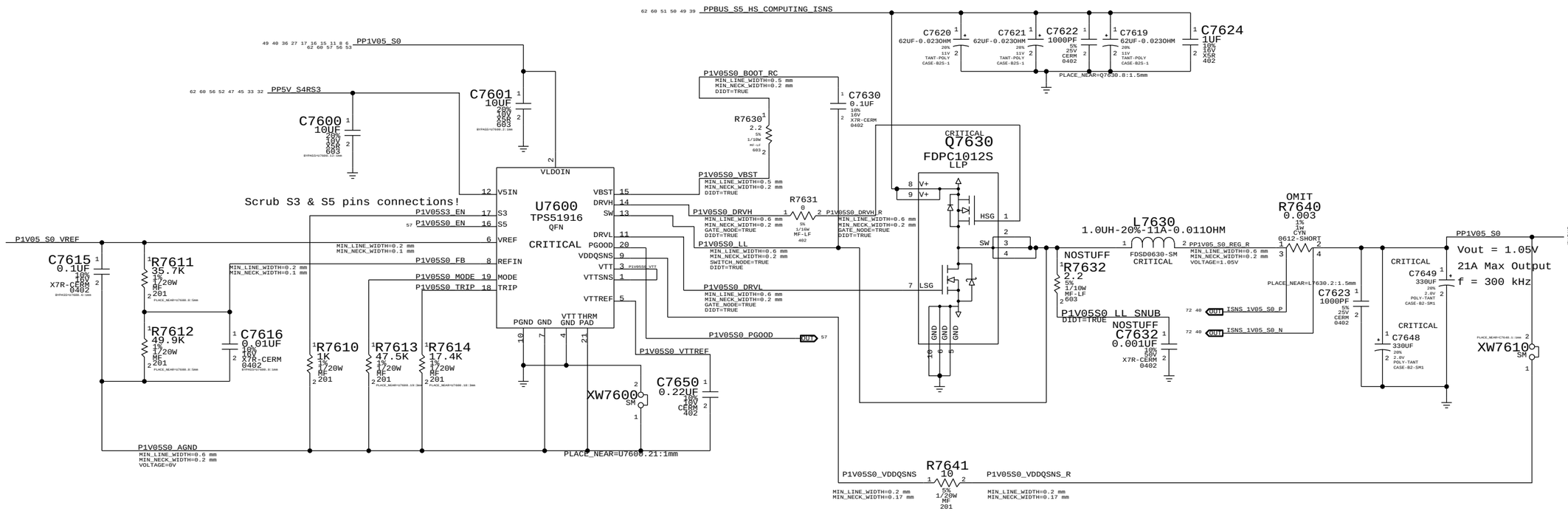
SHEET 51 OF 73

SKIPSEL Strap		
VREF2	Auto Skip	(Higher Efficiency)
VREG3	OOA Auto Skip	(Lower Efficiency)



SYNC_MASTER=J43_MLB	SYNC_DATE=10/02/2012
PAGE TITLE	5V S4RS3 / 3.3V S5 Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 75 OF 120
	SHEET 52 OF 73

1.05V S0 Regulator



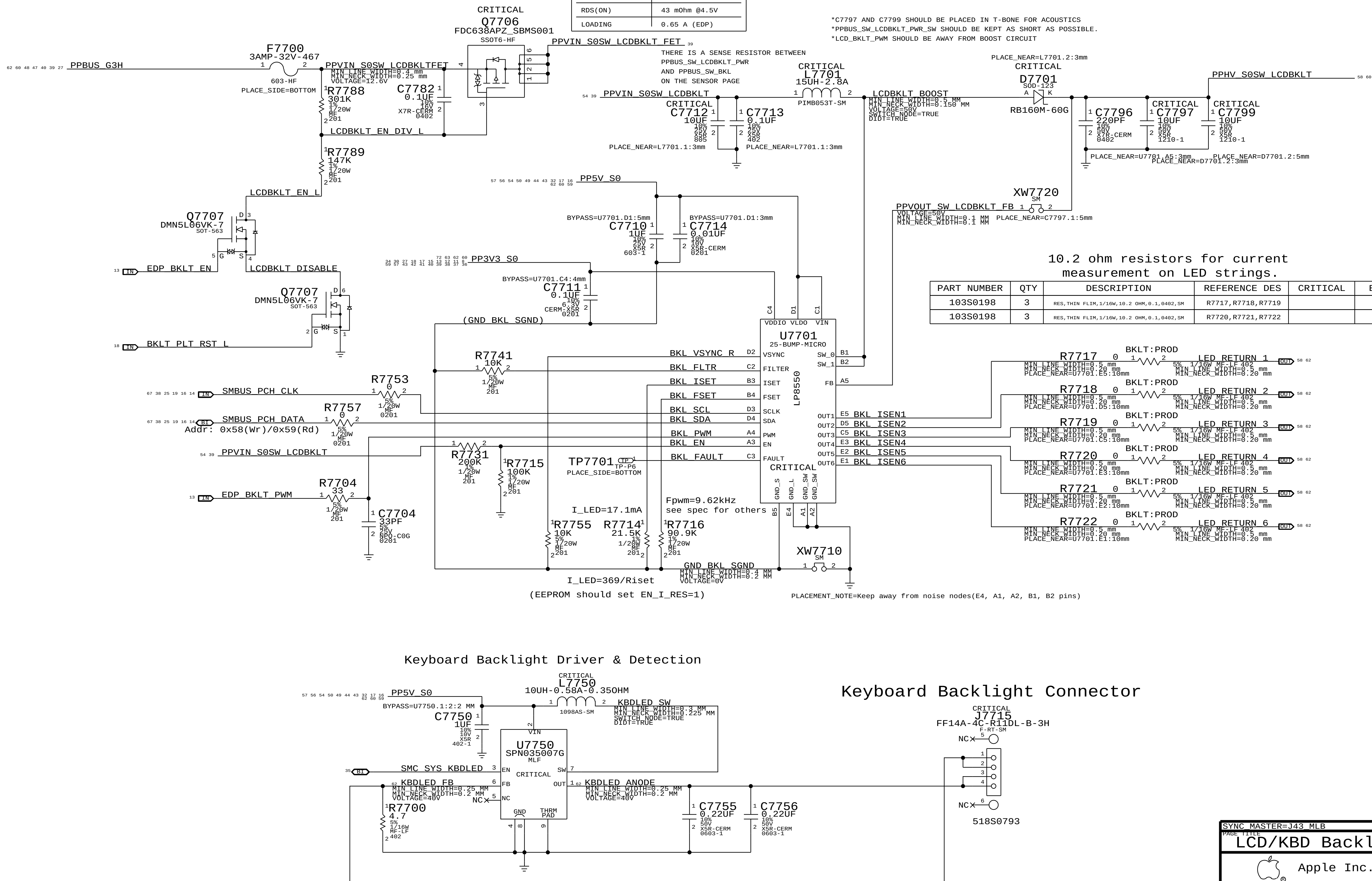
SYNC_MASTER=J43_MLB	SYNC_DATE=09/10/2012
PAGE TITLE	1.05V S0 Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 76 OF 120
	SHEET 53 OF 73

PPBUS S0 LCDBKLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

*C7797 AND C7799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE



10.2 ohm resistors for current measurement on LED strings.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R7717,R7718,R7719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R7720,R7721,R7722		BKLT:ENG

SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE
LCD/KBD Backlight Driver

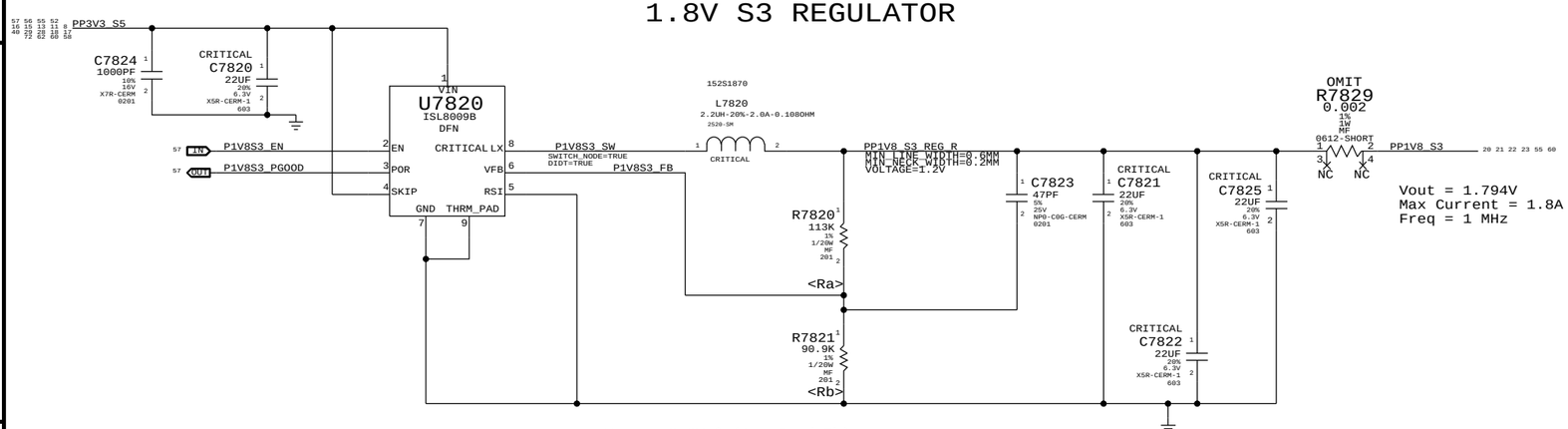
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

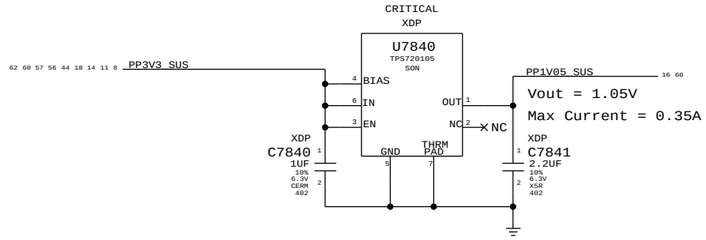
BRANCH <BRANCH>

1.8V S3 REGULATOR

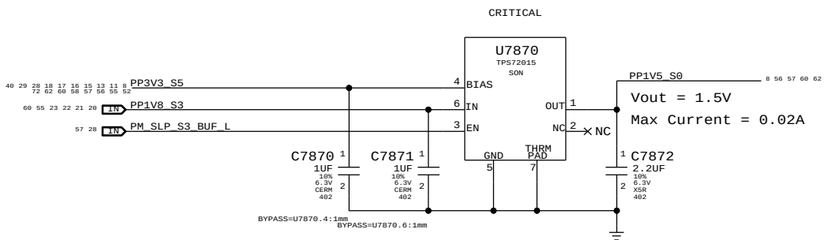


1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



SYNC_MASTER=J43_MLB SYNC_DATE=10/04/2012

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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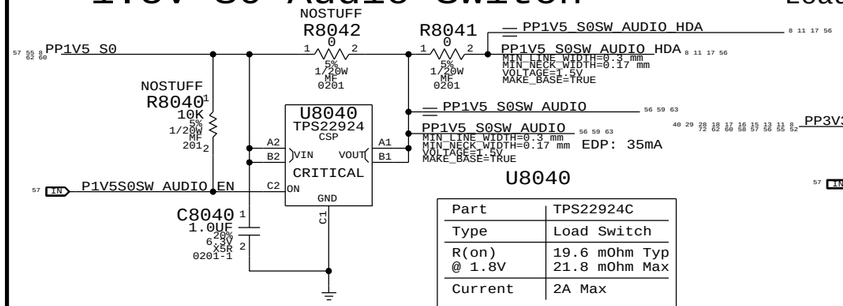
1.5V S0 Audio Switch

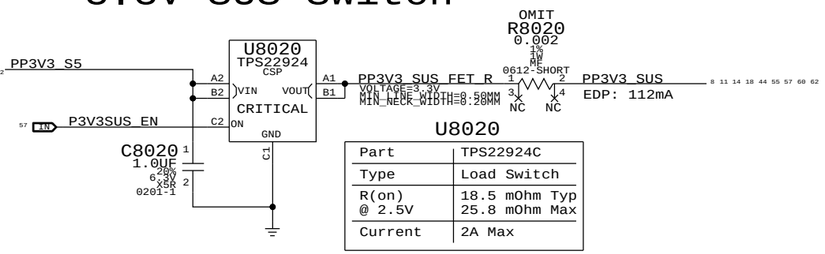
Loading specs per J41/43_PowerBudget_Riviera_rev0.99e



U8040

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

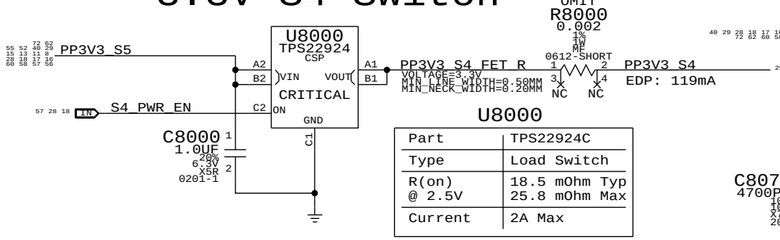
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

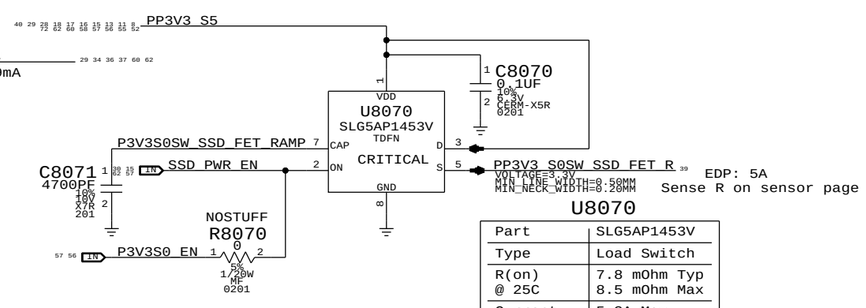
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

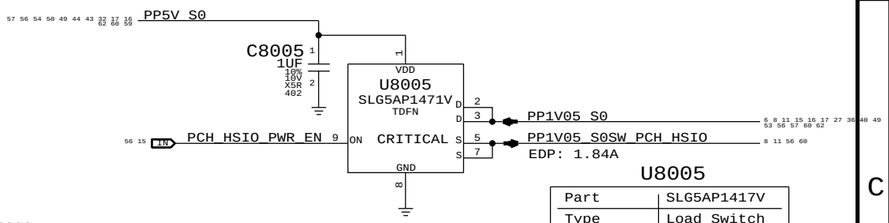
3.3V SSD Switch



U8070

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

1.05V PCH HSIO Switch

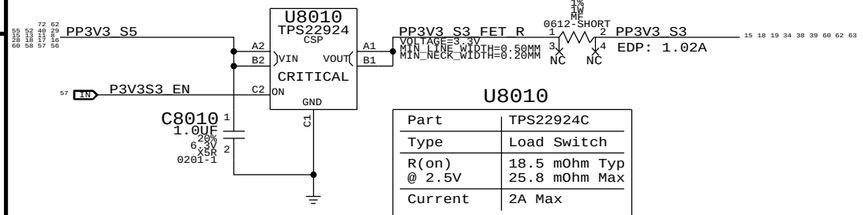


U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

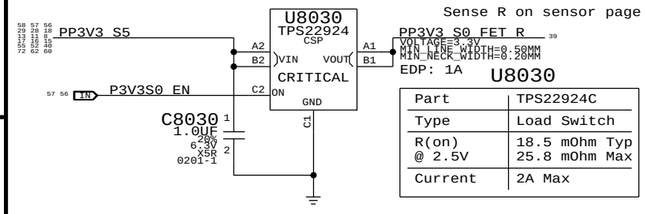
3.3V S3 Switch



U8010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

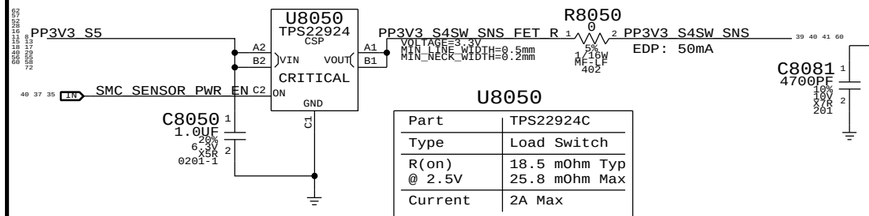
3.3V S0 Switch



U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

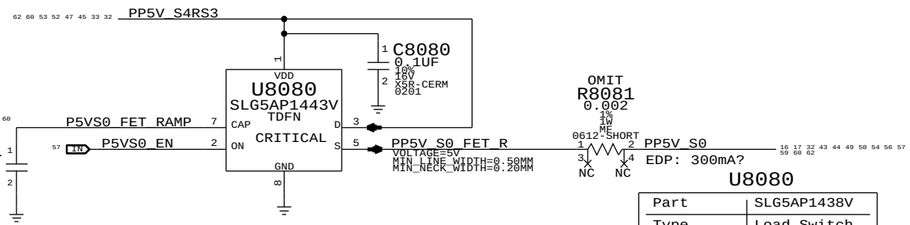
3.3V Sensor Switch



U8050

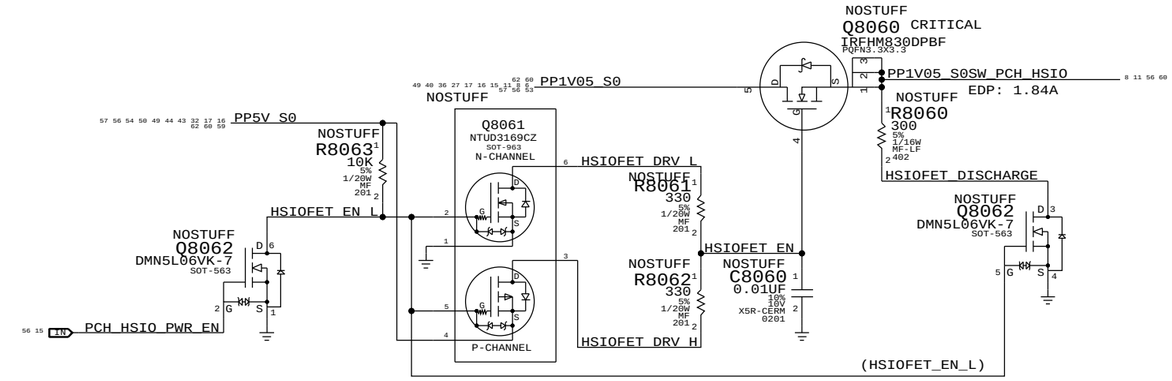
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

5V S0 Switch



U8080

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A



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PAGE TITLE	Power FETs
	Apple Inc.
DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
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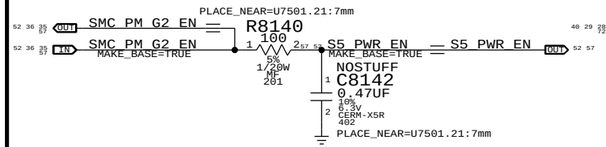
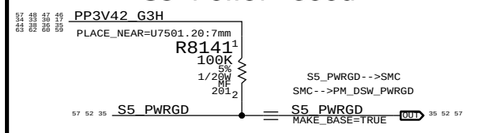
S5 Enables

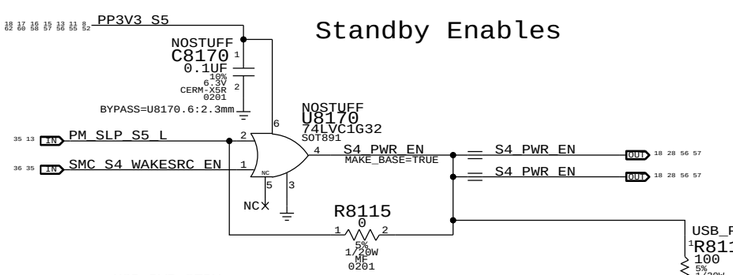


S5 Power Good

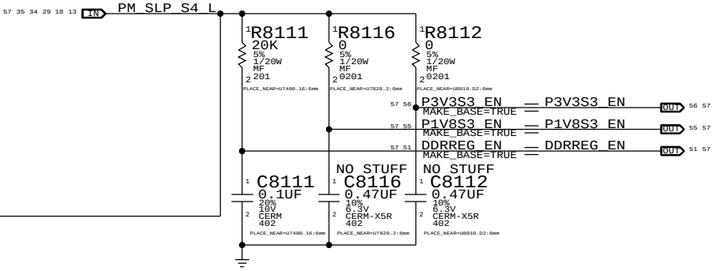


SSD Enable

Standby Enables



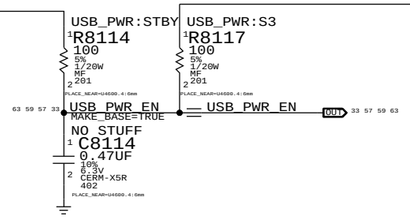
S3 Enables



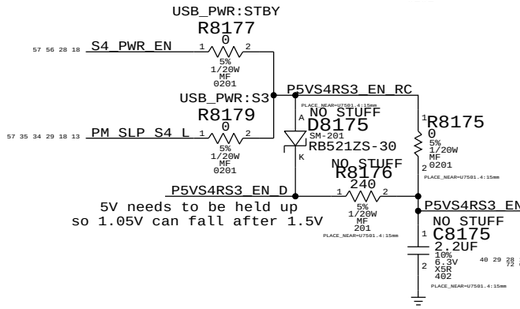
Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

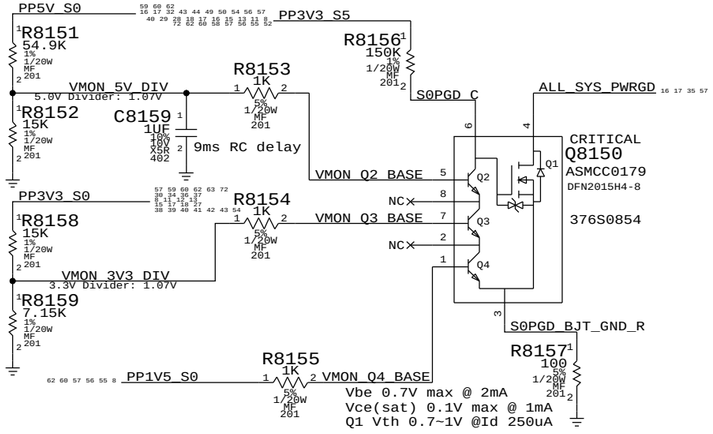
USB_PWR:STBY / USB_PWR:S3



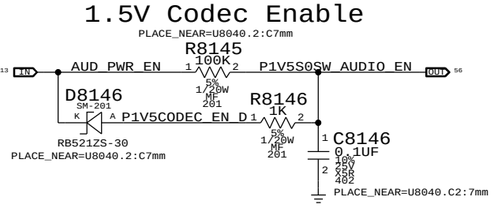
USB_PWR:STBY / USB_PWR:S3 (duplicate)



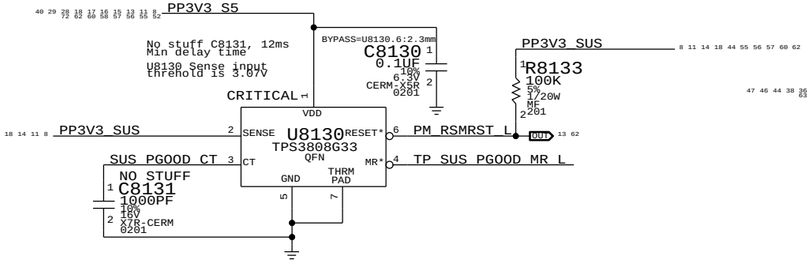
S0 Rail PGOOD (BJT Version)



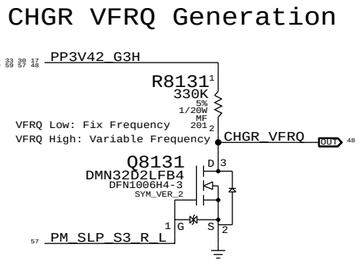
1.5V Codec Enable



3.3V SUS Detect



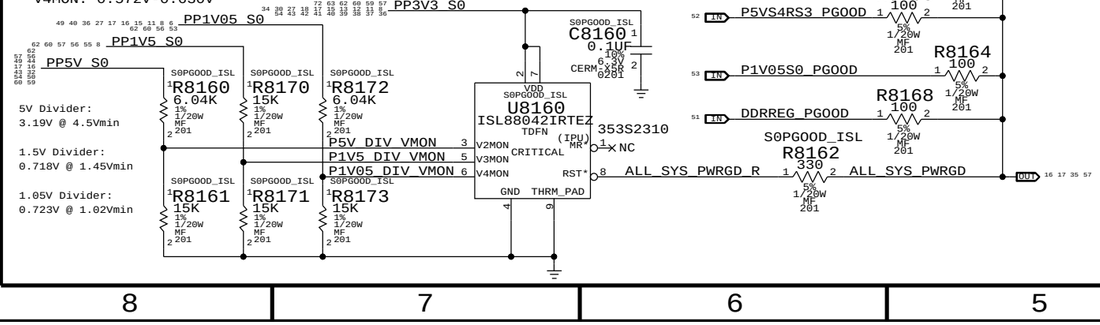
CHGR VFRQ Generation



S0 Rail PGOOD Circuitry

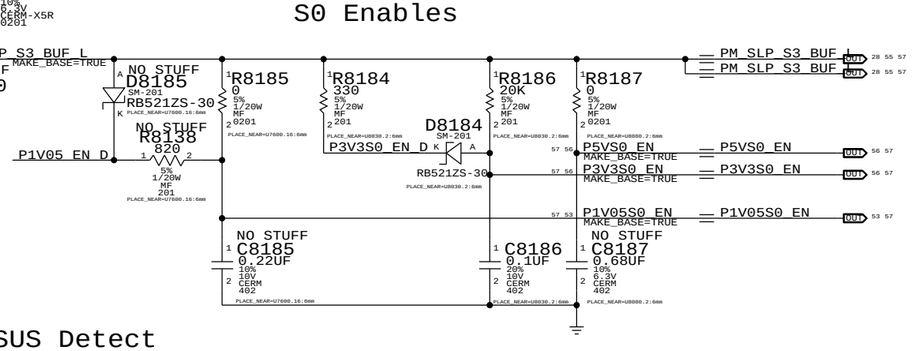
(ISL version used for development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

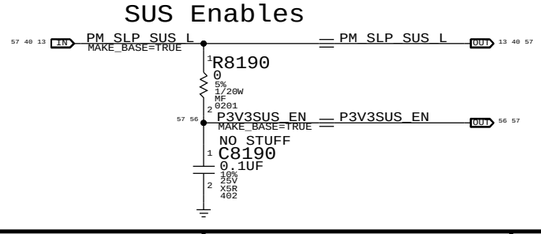


S0 Rail PGOOD Circuitry (duplicate)

S0 Enables



SUS Enables



SYNC_MASTER=J43_MLB SYNC_DATE=09/16/2012

PAGE TITLE

Power Control

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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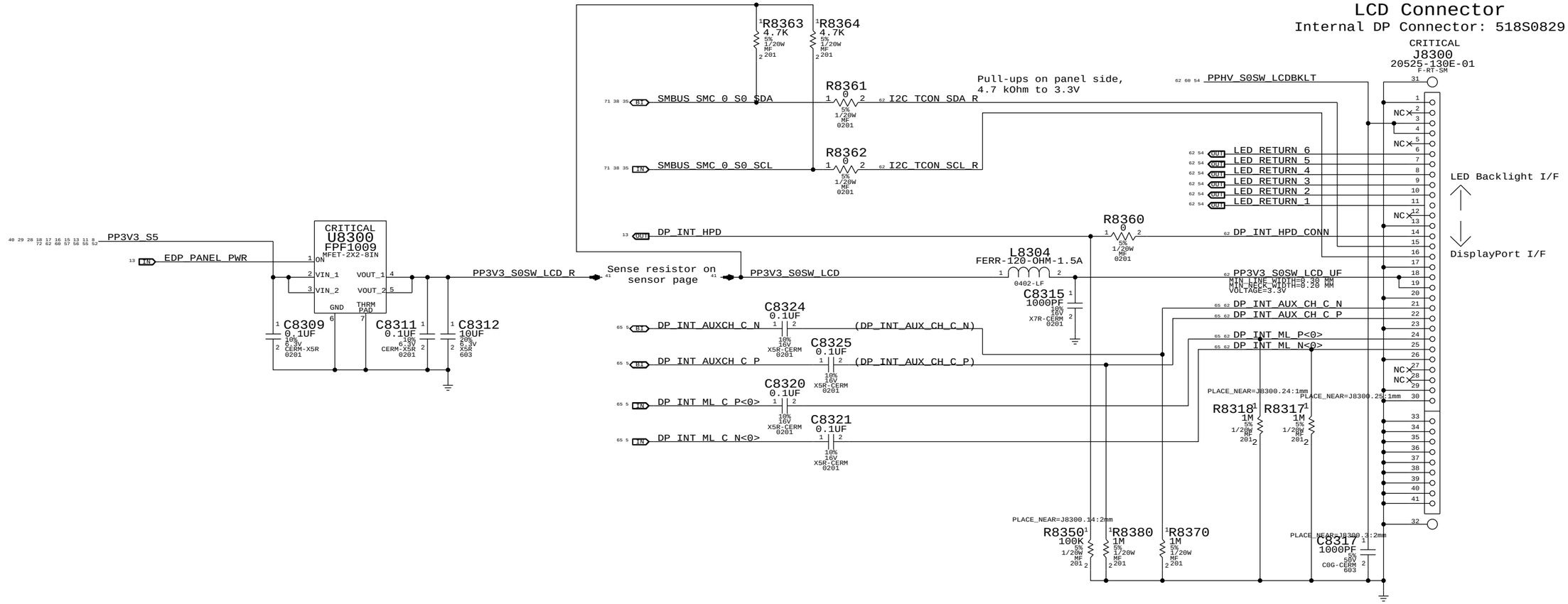

SYNC_MASTER=J43_MLB SYNC_DATE=09/11/2012

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

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LIO Connector

516S1036 (HIROSE 3.0mm RCPT)

CRITICAL

J9500

DF40CG3.0-48DS-0.4V

F-ST-SM

PP5V_S0

NOSTUFF
R9500
0
1/20W 5% MF 0201
VOLTAGE=5V
MIN_LINE_WIDTH=0.1MM
MIN_NECK_WIDTH=0.1MM

63 57 13 IN AUD_PWR_EN
63 PP5V_S0_ALT_AUD_LDO_EN
63 45 OUT SPKRAMP_SHDN_L
63 56 PP1V5_S0SW_AUDIO
PP3V3_S0
72 63 45 OUT SPKRAMP_INR_N
72 63 45 OUT SPKRAMP_INR_P
66 63 OUT USB3_EXTB_D2R_RC_N
66 63 OUT USB3_EXTB_D2R_RC_P
66 63 14 BI USB_EXTB_N
66 63 14 BI USB_EXTB_P
66 63 IN USB3_EXTB_R2D_C_N
66 63 IN USB3_EXTB_R2D_C_P

PP3V42_G3H
SMBUS_SMC_2_S3_SCL IN 35 38 63 71
SMBUS_SMC_2_S3_SDA BI 35 38 63 71
SYS_ONEWIRE BI 35 63
SMC_BC_ACOK OUT 35 36 48 63
XDP_USB_EXTB_OC_L OUT 14 16 63
USB_PWR_EN IN 33 57 63
FINSTACKSNS_ALERT_L OUT 37 63
HDA_SYNC IN 12 63 67
HDA_RST_L IN 12 63 67
HDA_SDOUT IN 12 63 67
HDA_SDIN0 OUT 12 63 67
HDA_BIT_CLK IN 12 63 67

C9510 1 0.1UF 10% 16V X5R-CERM 0201 2
BYPASS=J9500:1.5mm

C9520 1 0.1UF 10% 16V X5R-CERM 0201 2
BYPASS=J9500:1.5mm

C9500 1 0.1UF 10% 16V X5R-CERM 0201 2
BYPASS=J9500:1.5mm

NOSTUFF
C9550 1 10PF 5% 50V C0G-CERM 0402 2

R9510 0 1/20W 5% MF 0201
NOSTUFF C9531 1 5PF 5% 25V NP0-CERM 0201 2
R9520 0 1/20W 5% MF 0201
C9530 1 1UF 10% 16V X5R-CERM 0201 2
C9532 1 1UF 10% 16V X5R-CERM 0201 2

GND_VOID=TRUE

CRITICAL
D9511 ESD0P2RF-02LS TSSLP-2-1
D9510 ESD0P2RF-02LS TSSLP-2-1
D9520 ESD0P2RF-02LS TSSLP-2-1
D9521 ESD0P2RF-02LS TSSLP-2-1

SYNC_MASTER=CLEAN_J41	SYNC_DATE=11/13/2012
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"G3Hot" (Always-Present) Rails

PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

PP3V42_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE

PPVRTC_G3H
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE

5V Rails

PP5V_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4RS3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.175 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

3.3V Rails

PP3V3_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_SUS
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S3
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4SW_SNS
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0SW_SSD
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

1.8V/1.5V/1.2V/1.05V Rails

PP1V8_S3
2A max supply
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V5_S0
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP0V6_S0_DDRVTT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

PP1V05_S0
? mA
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.175 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_S0SW_PCH_HSIO
1.84A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

LCDBKLT Rail

PPHV_S0SW_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=50V
MAKE_BASE=TRUE

TBT Rails (off when no cable)

PP15V_TBT
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.8V
MAKE_BASE=TRUE

PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP1V05_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PPVIN_S4SW_TBTBST_FET
VOLTAGE=8.6V

CPU "VCORE" RAILS

PPVCC_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE
Power Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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LPDDR3 Command/Address

MAKE_BASE

7	=MEM_A_A<5>	TRUE	MEM_A_CAA<0>	20 24 68	
7	=MEM_A_A<9>	TRUE	MEM_A_CAA<1>	20 24 68	
7	=MEM_A_A<6>	TRUE	MEM_A_CAA<2>	20 24 68	
7	=MEM_A_A<8>	TRUE	MEM_A_CAA<3>	20 24 68	
7	=MEM_A_A<7>	TRUE	MEM_A_CAA<4>	20 24 68	
7	=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>	20 24 68	
68 61 24 20 7	MEM_A_CAA<6>	TRUE	MEM_A_CAA<6>	7 20 24 61 68	
7	=MEM_A_A<11>	TRUE	MEM_A_CAA<7>	20 24 68	
7	=MEM_A_A<15>	TRUE	MEM_A_CAA<8>	20 24 68	
7	=MEM_A_A<14>	TRUE	MEM_A_CAA<9>	20 24 68	
7	=MEM_A_A<13>	TRUE	MEM_A_CAB<0>	21 24 68	
7	=MEM_A_CAS_L	TRUE	MEM_A_CAB<1>	21 24 68	
7	=MEM_A_WE_L	TRUE	MEM_A_CAB<2>	21 24 68	
7	=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>	21 24 68	
7	=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>	21 24 68	
7	=MEM_A_A<2>	TRUE	MEM_A_CAB<5>	21 24 68	
68 61 24 21 7	MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>	7 21 24 61 68	
7	=MEM_A_A<10>	TRUE	MEM_A_CAB<7>	21 24 68	
7	=MEM_A_A<1>	TRUE	MEM_A_CAB<8>	21 24 68	
7	=MEM_A_A<0>	TRUE	MEM_A_CAB<9>	21 24 68	
68 61 24 21 20 7	MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>	7 20 21 24 61 68	
61 7	TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1	7 61	
61 7	TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2	7 61	
7	=MEM_B_A<5>	TRUE	MEM_B_CAA<0>	22 24 68	
7	=MEM_B_A<9>	TRUE	MEM_B_CAA<1>	22 24 68	
7	=MEM_B_A<6>	TRUE	MEM_B_CAA<2>	22 24 68	
7	=MEM_B_A<8>	TRUE	MEM_B_CAA<3>	22 24 68	
7	=MEM_B_A<7>	TRUE	MEM_B_CAA<4>	22 24 68	
7	=MEM_B_BA<2>	TRUE	MEM_B_CAA<5>	22 24 68	
68 61 24 22 7	MEM_B_CAA<6>	TRUE	MEM_B_CAA<6>	7 22 24 61 68	
7	=MEM_B_A<11>	TRUE	MEM_B_CAA<7>	22 24 68	
7	=MEM_B_A<15>	TRUE	MEM_B_CAA<8>	22 24 68	
7	=MEM_B_A<14>	TRUE	MEM_B_CAA<9>	22 24 68	
7	=MEM_B_A<13>	TRUE	MEM_B_CAB<0>	23 24 68	
7	=MEM_B_CAS_L	TRUE	MEM_B_CAB<1>	23 24 68	
7	=MEM_B_WE_L	TRUE	MEM_B_CAB<2>	23 24 68	
7	=MEM_B_RAS_L	TRUE	MEM_B_CAB<3>	23 24 68	
7	=MEM_B_BA<0>	TRUE	MEM_B_CAB<4>	23 24 68	
7	=MEM_B_A<2>	TRUE	MEM_B_CAB<5>	23 24 68	
68 61 24 23 7	MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>	7 23 24 61 68	
7	=MEM_B_A<10>	TRUE	MEM_B_CAB<7>	23 24 68	
7	=MEM_B_A<1>	TRUE	MEM_B_CAB<8>	23 24 68	
7	=MEM_B_A<0>	TRUE	MEM_B_CAB<9>	23 24 68	
68 61 24 23 22 7	MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>	7 22 23 24 61 68	
61 7	TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3	7 61	
61 7	TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4	7 61	

Memory Bit/Byte Swizzle

MAKE_BASE

20	=MEM_A_DQ<0>	TRUE	MEM_A_DQ<9>	7 68	
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20	=MEM_A_DQ<10>	TRUE	MEM_A_DQ<2>	7 68	
20	=MEM_A_DQ<11>	TRUE	MEM_A_DQ<7>	7 68	
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21	=MEM_A_DQ<33>	TRUE	MEM_A_DQ<44>	7 68	
21	=MEM_A_DQ<34>	TRUE	MEM_A_DQ<46>	7 68	
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21	=MEM_A_DQ<37>	TRUE	MEM_A_DQ<45>	7 68	
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21	=MEM_A_DQ<39>	TRUE	MEM_A_DQ<43>	7 68	
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21	=MEM_A_DQ<42>	TRUE	MEM_A_DQ<34>	7 68	
21	=MEM_A_DQ<43>	TRUE	MEM_A_DQ<39>	7 68	
21	=MEM_A_DQ<44>	TRUE	MEM_A_DQ<32>	7 68	
68 61 21 7	MEM_A_DQ<33>	TRUE	MEM_A_DQ<33>	7 21 61 68	
21	=MEM_A_DQ<46>	TRUE	MEM_A_DQ<35>	7 68	
21	=MEM_A_DQ<47>	TRUE	MEM_A_DQ<38>	7 68	
21	=MEM_A_DQ<48>	TRUE	MEM_A_DQ<52>	7 68	
21	=MEM_A_DQ<49>	TRUE	MEM_A_DQ<51>	7 68	
21	=MEM_A_DQ<50>	TRUE	MEM_A_DQ<48>	7 68	
21	=MEM_A_DQ<51>	TRUE	MEM_A_DQ<49>	7 68	
21	=MEM_A_DQ<52>	TRUE	MEM_A_DQ<53>	7 68	
21	=MEM_A_DQ<53>	TRUE	MEM_A_DQ<50>	7 68	
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20	=MEM_A_DQS_P<0>	TRUE	MEM_A_DQS_P<1>	7 68	
20	=MEM_A_DQS_N<0>	TRUE	MEM_A_DQS_N<1>	7 68	
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20	=MEM_A_DQS_P<2>	TRUE	MEM_A_DQS_P<3>	7 68	
20	=MEM_A_DQS_N<2>	TRUE	MEM_A_DQS_N<3>	7 68	
20	=MEM_A_DQS_P<3>	TRUE	MEM_A_DQS_P<2>	7 68	
20	=MEM_A_DQS_N<3>	TRUE	MEM_A_DQS_N<2>	7 68	
21	=MEM_A_DQS_P<4>	TRUE	MEM_A_DQS_P<5>	7 68	
21	=MEM_A_DQS_N<4>	TRUE	MEM_A_DQS_N<5>	7 68	
21	=MEM_A_DQS_P<5>	TRUE	MEM_A_DQS_P<4>	7 68	
21	=MEM_A_DQS_N<5>	TRUE	MEM_A_DQS_N<4>	7 68	
68 61 21 7	MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<6>	7 21 61 68	
68 61 21 7	MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<6>	7 21 61 68	
21	=MEM_A_DQS_P<7>	TRUE	MEM_A_DQS_P<7>	7 68	
21	=MEM_A_DQS_N<7>	TRUE	MEM_A_DQS_N<7>	7 68	

MAKE_BASE

22	=MEM_B_DQ<0>	TRUE	MEM_B_DQ<12>	7 68	
22	=MEM_B_DQ<1>	TRUE	MEM_B_DQ<9>	7 68	
22	=MEM_B_DQ<2>	TRUE	MEM_B_DQ<10>	7 68	
22	=MEM_B_DQ<3>	TRUE	MEM_B_DQ<11>	7 68	
22	=MEM_B_DQ<4>	TRUE	MEM_B_DQ<13>	7 68	
22	=MEM_B_DQ<5>	TRUE	MEM_B_DQ<8>	7 68	
22	=MEM_B_DQ<6>	TRUE	MEM_B_DQ<14>	7 68	
22	=MEM_B_DQ<7>	TRUE	MEM_B_DQ<15>	7 68	
22	=MEM_B_DQ<8>	TRUE	MEM_B_DQ<0>	7 68	
22	=MEM_B_DQ<9>	TRUE	MEM_B_DQ<1>	7 68	
22	=MEM_B_DQ<10>	TRUE	MEM_B_DQ<2>	7 68	
22	=MEM_B_DQ<11>	TRUE	MEM_B_DQ<7>	7 68	
22	=MEM_B_DQ<12>	TRUE	MEM_B_DQ<4>	7 68	
22	=MEM_B_DQ<13>	TRUE	MEM_B_DQ<5>	7 68	
22	=MEM_B_DQ<14>	TRUE	MEM_B_DQ<6>	7 68	
22	=MEM_B_DQ<15>	TRUE	MEM_B_DQ<3>	7 68	
22	=MEM_B_DQ<16>	TRUE	MEM_B_DQ<28>	7 68	
22	=MEM_B_DQ<17>	TRUE	MEM_B_DQ<29>	7 68	
22	=MEM_B_DQ<18>	TRUE	MEM_B_DQ<30>	7 68	
22	=MEM_B_DQ<19>	TRUE	MEM_B_DQ<27>	7 68	
22	=MEM_B_DQ<20>	TRUE	MEM_B_DQ<24>	7 68	
22	=MEM_B_DQ<21>	TRUE	MEM_B_DQ<25>	7 68	
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22	=MEM_B_DQ<23>	TRUE	MEM_B_DQ<26>	7 68	
22	=MEM_B_DQ<24>	TRUE	MEM_B_DQ<20>	7 68	
22	=MEM_B_DQ<25>	TRUE	MEM_B_DQ<16>	7 68	
22	=MEM_B_DQ<26>	TRUE	MEM_B_DQ<23>	7 68	
22	=MEM_B_DQ<27>	TRUE	MEM_B_DQ<22>	7 68	
22	=MEM_B_DQ<28>	TRUE	MEM_B_DQ<21>	7 68	
22	=MEM_B_DQ<29>	TRUE	MEM_B_DQ<17>	7 68	
22	=MEM_B_DQ<30>	TRUE	MEM_B_DQ<18>	7 68	
22	=MEM_B_DQ<31>	TRUE	MEM_B_DQ<19>	7 68	
23	=MEM_B_DQ<32>	TRUE	MEM_B_DQ<44>	7 68	
23	=MEM_B_DQ<34>	TRUE	MEM_B_DQ<42>	7 68	
23	=MEM_B_DQ<35>	TRUE	MEM_B_DQ<43>	7 68	
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23	=MEM_B_DQ<37>	TRUE	MEM_B_DQ<40>	7 68	
23	=MEM_B_DQ<38>	TRUE	MEM_B_DQ<46>	7 68	
23	=MEM_B_DQ<39>	TRUE	MEM_B_DQ<47>	7 68	
68 61 23 7	MEM_B_DQ<32>	TRUE	MEM_B_DQ<32>	7 23 61 68	
23	=MEM_B_DQ<41>	TRUE	MEM_B_DQ<33>	7 68	
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23	=MEM_B_DQ<43>	TRUE	MEM_B_DQ<39>	7 68	
23	=MEM_B_DQ<44>	TRUE	MEM_B_DQ<36>	7 68	
23	=MEM_B_DQ<45>	TRUE	MEM_B_DQ<37>	7 68	
23	=MEM_B_DQ<46>	TRUE	MEM_B_DQ<38>	7 68	
23	=MEM_B_DQ<47>	TRUE	MEM_B_DQ<35>	7 68	
23	=MEM_B_DQ<48>	TRUE	MEM_B_DQ<57>	7 68	
23	=MEM_B_DQ<49>	TRUE	MEM_B_DQ<56>	7 68	
23	=MEM_B_DQ<50>	TRUE	MEM_B_DQ<60>	7 68	
23	=MEM_B_DQ<51>	TRUE	MEM_B_DQ<59>	7 68	
23	=MEM_B_DQ<52>	TRUE	MEM_B_DQ<63>	7 68	
23	=MEM_B_DQ<53>	TRUE	MEM_B_DQ<62>	7 68	
23	=MEM_B_DQ<54>	TRUE	MEM_B_DQ<58>	7 68	
23	=MEM_B_DQ<55>	TRUE	MEM_B_DQ<61>	7 68	
23	=MEM_B_DQ<56>	TRUE	MEM_B_DQ<49>	7 68	
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23	=MEM_B_DQ<61>	TRUE	MEM_B_DQ<55>	7 68	
23	=MEM_B_DQ<62>	TRUE	MEM_B_DQ<50>	7 68	
23	=MEM_B_DQ<63>	TRUE	MEM_B_DQ<54>	7 68	
22	=MEM_B_DQS_P<0>	TRUE	MEM_B_DQS_P<1>	7 68	
22	=MEM_B_DQS_N<0>	TRUE	MEM_B_DQS_N<1>	7 68	
22	=MEM_B_DQS_P<1>	TRUE	MEM_B_DQS_P<0>	7 68	
22	=MEM_B_DQS_N<1>	TRUE	MEM_B_DQS_N<0>	7 68	
22	=MEM_B_DQS_P<2>	TRUE	MEM_B_DQS_P<3>	7 68	
22	=MEM_B_DQS_N<2>	TRUE	MEM_B_DQS_N<3>	7 68	
22	=MEM_B_DQS_P<3>	TRUE	MEM_B_DQS_P<2>	7 68	
22	=MEM_B_DQS_N<3>	TRUE	MEM_B_DQS_N<2>	7 68	
23	=MEM_B_DQS_P<4>	TRUE	MEM_B_DQS_P<5>	7 68	
23	=MEM_B_DQS_N<4>	TRUE	MEM_B_DQS_N<5>	7 68	
23	=MEM_B_DQS_P<5>	TRUE	MEM_B_DQS_P<4>	7 68	
23	=MEM_B_DQS_N<5>	TRUE	MEM_B_DQS_N<4>	7 68	
23	=MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<7>	7 68	
23	=MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<7>	7 68	
68 61 23 7	MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>	7 23 61 68	
68 61 23 7	MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>	7 23 61 68	

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Signal Aliases

Apple Inc.

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Functional Test Points

J3501: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN (Need 6 TPs)	29 35 36 37 39
TRUE	WIFI_EVENT_L	29 35 36
TRUE	PCIE_AP_R2D_N	29 67
TRUE	PCIE_AP_R2D_P	29 67
TRUE	PCIE_CLK100M_AP_N	12 29 67
TRUE	PCIE_CLK100M_AP_P	12 29 67
TRUE	PCIE_AP_D2R_P	14 29 67
TRUE	PCIE_AP_D2R_N	14 29 67
TRUE	PCIE_WAKE_L	13 29 31
TRUE	AP_RESET_CONN_L	29
TRUE	AP_CLKREQ_O_L	29
TRUE	USB_BT_CONN_P	29 66
TRUE	USB_BT_CONN_N	29 66
TRUE	PP3V3_S4	29 34 36 37 56 60 62

(Need to add 8 GND TPs)

J3700: SSD Connector

FUNC_TEST

TRUE	PP3V3_S0SW_SSD_FLT (Need 5 TPs)	30
TRUE	PCIE_SSD_R2D_N<3..0>	30 65
TRUE	PCIE_SSD_R2D_P<3..0>	30 65
TRUE	PP3V3_S0	40 41 42 43 54 57 59 11 12 13 15 17 18 27 30 34 36 37 38 39 60 62 63 72
TRUE	SSD_RESET_CONN_L	30
TRUE	SSD_CLKREQ_CONN_L	30
TRUE	SMC_OOB1_R2D_CONN_L	30
TRUE	SMC_OOB1_D2R_CONN_L	30
TRUE	SSD_PCIE_SEL_L	16 30
TRUE	SSD_DEVSLP	15 30
TRUE	SSD_PWRFAIL_WARN_L	
TRUE	SSD_PWR_EN	15 30 56 57
TRUE	PCIE_SSD_D2R_N<3..0>	12 30 65
TRUE	PCIE_SSD_D2R_P<3..0>	12 30 65
TRUE	PCIE_CLK100M_SSD_N	12 30 65
TRUE	PCIE_CLK100M_SSD_P	12 30 65

(Need to add 6 GND TPs)

J4002: Camera Connector

FUNC_TEST

TRUE	MIPI_CLK_CONN_N	32 70
TRUE	MIPI_CLK_CONN_P	32 70
TRUE	CAM_SENSOR_WAKE_L_CONN	32
TRUE	MIPI_DATA_CONN_N	32 70
TRUE	MIPI_DATA_CONN_P	32 70
TRUE	SMBUS_SMC_1_S0_SDA	14 32 35 38 41 42 67 71
TRUE	SMBUS_SMC_1_S0_SCL	14 32 35 38 41 42 67 71
TRUE	I2C_CAM_SCK	31 32
TRUE	I2C_CAM_SDA	31 32
TRUE	PP5V_S3RS0_ALSCAM_F (Need TBD TPs)	32

(Need to add TBD GND TPs)

J6000: Fan Connector

FUNC_TEST

TRUE	PP5V_S0	16 17 32 43 44 49 50 54 56 57 59 60 62
TRUE	FAN_RT_TACH	43
TRUE	FAN_RT_PWM	43

(Need to add 1 GND TP)

J4800: IPD Flex Connector

FUNC_TEST

TRUE	SMC_LID	34 35 36 46
TRUE	TPAD_SPI_MISO_R	34
TRUE	USB_TPAD_P	14 34 66
TRUE	USB_TPAD_N	14 34 66
TRUE	TPAD_SPI_CLK_R	34
TRUE	TPAD_WAKE_L	34
TRUE	TPAD_SPI_MOSI_R	34
TRUE	PP3V3_S4_IPD	34
TRUE	TPAD_SPI_CS_R_L	34
TRUE	TPAD_SPI_IF_EN_CONN	34
TRUE	TPAD_SPI_INT_S4_WAKE_L_CONN	34
TRUE	PP5V_S4_IPD	34
TRUE	TPAD_USB_IF_EN_CONN	34
TRUE	SMBUS_SMC_3_SDA	34 35 38 42 71
TRUE	SMBUS_SMC_3_SCL	34 35 38 42 71
TRUE	SMC_LSOC_RST_L	34 36
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	SMC_ONOFF_L	34 35 36

(Need to add 5 GND TPs)

J7000: DC-In Connector

FUNC_TEST

TRUE	PPDCIN_G3H (Need 4 TPs)	47 48 60 62
TRUE	PP5V_S4RS3 (Need 3 TPs)	32 33 45 47 52 53 56 60

(Need to add 5 GND TPs)

J6404: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_ROUT_P	45 72
TRUE	SPKRAMP_ROUT_N	45 72

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN (Need 4 TPs)	46 48
TRUE	SMBUS_SMC_5_G3_SCL	35 38 46 48 71
TRUE	SMBUS_SMC_5_G3_SDA	35 38 46 48 71
TRUE	SYS_DETECT_L	46

(Need to add 4 GND TPs near J7050 and 1 for shield)

J8300: Internal DP Connector

FUNC_TEST

TRUE	PPHV_S0SW_LCDBKLT (Need 2 TPs)	54 58 60
TRUE	LED_RETURN_6	54 58
TRUE	LED_RETURN_5	54 58
TRUE	LED_RETURN_4	54 58
TRUE	LED_RETURN_3	54 58
TRUE	LED_RETURN_2	54 58
TRUE	LED_RETURN_1	54 58
TRUE	DP_INT_HPD_CONN	58
TRUE	I2C_TCON_SDA_R	58
TRUE	I2C_TCON_SCL_R	58
TRUE	PP3V3_S0SW_LCD_UF (Need 2 TPs)	58
TRUE	DP_INT_AUX_CH_C_N	58 65
TRUE	DP_INT_AUX_CH_C_P	58 65
TRUE	DP_INT_ML_P<0>	58 65
TRUE	DP_INT_ML_N<0>	58 65

(Need to add 5 GND TPs)

J7715: KB BKLT Connector

FUNC_TEST

TRUE	KBDLED_ANODE	54
TRUE	KBDLED_FB	54

(Need to add 2 GND TPs)

J1800: XDP Connector

(Only a subset are needed for FCT HVM test fixture)

FUNC_TEST

TRUE	XDP_CPU_TCK	6 16 65
TRUE	XDP_PCH_TCK	12 16 67
TRUE	XDP_CPU_TDI	6 16 65
TRUE	XDP_CPU_TDO	6 16 65
TRUE	XDP_CPUPCH_TRST_L	6 12 16 65
TRUE	XDP_CPU_TMS	6 16 65
TRUE	XDP_PCH_TMS	12 16 67
TRUE	XDP_PCH_TDI	12 16 67
TRUE	XDP_PCH_TDO	12 16 67
TRUE	XDP_CPU_PREQ_L	6 16 65
TRUE	XDP_CPU_PRDY_L	6 16 65
TRUE	XDP_CPU_VCCST_PWRGD	16
TRUE	PM_RSMRST_L	13 57
TRUE	XDP_SYS_PWROK	16
TRUE	PM_SYSRST_L	13 17 35
TRUE	CPU_CFG<3>	6 16 65
TRUE	PP1V05_S0	6 8 11 15 16 17 27 36 40 49 53 56 57 60 62

(Need to add 2 GND TPs)

J6100: LPC+SPI Connector

FUNC_TEST

TRUE	PP3V42_G3H	62 63
TRUE	PP5V_S0	17 30 33 34 35 36 38 44 46 47 48 59 60 62
TRUE	LPC_CLK24M_LPCPLUS	16 17 32 43 44 49 50 54 56 57 59 60 62 68
TRUE	LPC_AD<3..0>	14 35 44 67
TRUE	SPI_ALT_MOSI	44
TRUE	XDP_LPCPLUS_GPIO	15 16 44
TRUE	LPCPLUS_RESET_L	18 44 67
TRUE	SMC_TDO	35 36 44
TRUE	TP_SMC_TRST_L	44
TRUE	TP_SMC_MD1	44
TRUE	SMC_TX_L	35 36 44
TRUE	SPI_ALT_MISO	44
TRUE	LPC_FRAME_L	14 35 44 67
TRUE	SPIROM_USE_MLB	15 44
TRUE	PM_CLKRUN_L	13 35 44
TRUE	SPI_ALT_CLK	44
TRUE	SPI_ALT_CS_L	44
TRUE	LPC_SERIRQ	15 35 44
TRUE	LPC_PWRDWN_L	13 35 44
TRUE	SMC_TDI	35 36 44
TRUE	SMC_TCK	35 36 44
TRUE	SMC_RESET_L	35 36 44 48
TRUE	SMC_ROMBOOT	36 44
TRUE	SMC_RX_L	35 36 44
TRUE	SMC_TMS	35 36 44

(Need to add 6 GND TPs)

TRUE	GND	

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	27 39 40 47 48 54 60
TRUE	PPVIN_S4SW_TBTBST_FET	27 60
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	39 49 50 51 53 60
TRUE	PPDCIN_G3H	47 48 60 62
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	PPVRTC_G3H	8 12 13 17 60
TRUE	PP3V3_S5	8 11 13 15 16 17 18 28 29 40 52 56 60 67 68 69 72
TRUE	PP3V3_SUS	8 11 14 18 44 55 56 57 60
TRUE	PP3V3_S3	15 18 19 34 38 39 56 60 63
TRUE	PP3V3_S0	60 62 63 72
TRUE	PP3V3_S0SW_SSD	8 11 12 13 15 17 18 27 30 34 36 37 38 39 40 41 42 43 54 57 59
TRUE	PP1V5_S0	30 39 60
TRUE	PP1V05_S0	8 55 56 57 60
TRUE	PP1V05_S0	6 8 11 15 16 17 27 36 40 49 53 56 57 60 62
TRUE	PP15V_TBT	27 28 60
TRUE	PP3V3_TBTLC	15 17 25 26 27 60
TRUE	PP1V05_TBTLC	26 27 60
TRUE	PPVCC_S0_CPU	8 10 40 50 60
TRUE	PP1V05_TBTCIO	26 27 60
TRUE	PPBUS_S5_HS_OTHER_ISNS	39 52 60
TRUE	PPDCIN_G3H_ISOL	40 47 48 60
TRUE	PP3V3_S4	29 34 36 37 56 60 62

(Need to add 27 GND TPs)

NO_TEST Nets

NO_TEST

	MAKE_BASE			
62	NC_PCIE_CLK100M_SDP	TRUE TRUE	NC_PCIE_CLK100M_SDP	62
62	NC_PCIE_CLK100M_SDN	TRUE TRUE	NC_PCIE_CLK100M_SDN	62
62 12	NC_PCIE_CLK100M_FWP	TRUE TRUE	NC_PCIE_CLK100M_FWP	12 62
62 12	NC_PCIE_CLK100M_FWN	TRUE TRUE	NC_PCIE_CLK100M_FWN	12 62
62 14	NC_PCIE_FW_D2RP	TRUE TRUE	NC_PCIE_FW_D2RP	14 62
62 14	NC_PCIE_FW_D2RN	TRUE TRUE	NC_PCIE_FW_D2RN	14 62
62 14	NC_PCIE_FW_R2D_CP	TRUE TRUE	NC_PCIE_FW_R2D_CP	14 62
62 14	NC_PCIE_FW_R2D_CN	TRUE TRUE	NC_PCIE_FW_R2D_CN	14 62
62 14	NC_USB_IRP	TRUE TRUE	NC_USB_IRP	14 62
62 14	NC_USB_IRN	TRUE TRUE	NC_USB_IRN	14 62
62 14	NC_USB_CAMERAP	TRUE TRUE	NC_USB_CAMERAP	14 62
62 14	NC_USB_CAMERAN	TRUE TRUE	NC_USB_CAMERAN	14 62
62 14	NC_USB_SDP	TRUE TRUE	NC_USB_SDP	14 62
62 14	NC_USB_SDN	TRUE TRUE	NC_USB_SDN	14 62
65	DP_INT_ML_C_P<3..1>	TRUE TRUE	NC_INT_ML_CP<3..1>	5
65	DP_INT_ML_C_N<3..1>	TRUE TRUE	NC_INT_ML_CN<3..1>	5
62 12	NC_HDA_SDIN1	TRUE TRUE	NC_HDA_SDIN1	12 62
62 13	NC_PCI_PME_L	TRUE TRUE	NC_PCI_PME_L	13 62
62 14	NC_CLINK_CLK	TRUE TRUE	NC_CLINK_CLK	14 62
62 14	NC_CLINK_DATA	TRUE TRUE	NC_CLINK_DATA	14 62
62 14	NC_CLINK_RESET_L	TRUE TRUE	NC_CLINK_RESET_L	14 62

CPU/PCH

62 35	NC_SMC_SYS_LED	TRUE TRUE	NC_SMC_SYS_LED	35 62
62	NC_IR_RX_OUT_RC	TRUE TRUE	NC_IR_RX_OUT_RC	62
62	NC_USB_SMCP	TRUE TRUE	NC_USB_SMCP	62
62	NC_USB_SMCN	TRUE TRUE	NC_USB_SMCN	62
62 35	NC_SMC_GFX_OVERTEMP	TRUE TRUE	NC_SMC_GFX_OVERTEMP	35 62
62 35	NC_SMC_GFX_THROTTLE_L	TRUE TRUE	NC_SMC_GFX_THROTTLE_L	35 62
62 35	NC_SMC_FAN_1_CTL	TRUE TRUE	NC_SMC_FAN_1_CTL	35 62
62 35	NC_SMC_FAN_1_TACH	TRUE TRUE	NC_SMC_FAN_1_TACH	35 62
62 35	NC_SMC_FAN_5_CTL	TRUE TRUE	NC_SMC_FAN_5_CTL	35 62
62	NC_ENET_ASF_GPIO	TRUE TRUE	NC_ENET_ASF_GPIO	62
62	NC_SMC_MPM5_LED_PWR	TRUE TRUE	NC_SMC_MPM5_LED_PWR	62
62	NC_SMC_MPM5_LED_CHG	TRUE TRUE	NC_SMC_MPM5_LED_CHG	62
62 35	NC_SMC_T25_EN_L	TRUE TRUE	NC_SMC_T25_EN_L	35 62
62 35	NC_SMC_DP_HPD_L	TRUE TRUE	NC_SMC_DP_HPD_L	35 62
62 35	NC_SMBUS_SMC_4_ASF_SCL	TRUE TRUE	NC_SMBUS_SMC_4_ASF_SCL	35 62
62 35	NC_SMBUS_SMC_4_ASF_SDA	TRUE TRUE	NC_SMBUS_SMC_4_ASF_SDA	35 62
62 35	NC_BDV_BKL_PWM	TRUE TRUE	NC_BDV_BKL_PWM	35 62

SMC

69	TBT_B_R2D_C_P<1..0>	TRUE TRUE	NC_TBT_B_R2D_CP<1..0>	25
69	TBT_B_R2D_C_N<1..0>	TRUE TRUE	NC_TBT_B_R2D_CN<1..0>	25
69	TBT_B_D2R_P<1..0>	TRUE TRUE	NC_TBT_B_D2RP<1..0>	25
69	TBT_B_D2R_N<1..0>	TRUE TRUE	NC_TBT_B_D2RN<1..0>	25
62 25	NC_TBT_B_LSTX	TRUE TRUE	NC_TBT_B_LSTX	25 62
69 62	NC_DP_TBTPB_ML_CP<3..1:2>	TRUE TRUE	NC_DP_TBTPB_ML_CP<3..1:2>	62 69
69 62	NC_DP_TBTPB_ML_CN<3..1:2>	TRUE TRUE	NC_DP_TBTPB_ML_CN<3..1:2>	62 69
69 62 25	NC_DP_TBTPB_AUXCH_CP	TRUE TRUE	NC_DP_TBTPB_AUXCH_CP	25 62 69
69 62 25	NC_DP_TBTPB_AUXCH_CN	TRUE TRUE	NC_DP_TBTPB_AUXCH_CN	25 62 69
25	TP_DP_TBTSRC_ML_CP<3>	TRUE TRUE	NC_DP_TBTSRC_ML_CP<3>	
25	TP_DP_TBTSRC_ML_CN<3>	TRUE TRUE	NC_DP_TBTSRC_ML_CN<3>	
25	TP_DP_TBTSRC_ML_CP<2>	TRUE TRUE	NC_DP_TBTSRC_ML_CP<2>	
25	TP_DP_TBTSRC_ML_CN<2>	TRUE TRUE	NC_DP_TBTSRC_ML_CN<2>	
62 25	NC_DP_TBTSRC_ML_CP<1>	TRUE TRUE	NC_DP_TBTSRC_ML_CP<1>	25 62
62 25	NC_DP_TBTSRC_ML_CN<1>	TRUE TRUE	NC_DP_TBTSRC_ML_CN<1>	25 62
25	TP_DP_TBTSRC_ML_CP<0>	TRUE TRUE	NC_DP_TBTSRC_ML_CP<0>	
25	TP_DP_TBTSRC_ML_CN<0>	TRUE TRUE	NC_DP_TBTSRC_ML_CN<0>	
62 25	NC_DP_TBTSRC_AUXCH_CP	TRUE TRUE	NC_DP_TBTSRC_AUXCH_CP	25 62
62 25	NC_DP_TBTSRC_AUXCH_CN	TRUE TRUE	NC_DP_TBTSRC_AUXCH_CN	25 62

TBT

Unused nets with offpage

(Nets with offpages not used on this project)

HDD_PWR_EN	15
WOL_EN	14
BT_PWRRST_L	15
HDMITBTMUX_FLAG_L	15
FW_PWR_EN	15
FW_PME_L	15
ENET_MEDIA_SENSE	15
LCD_PSR_EN	15
LCD_IRQ_L	15
ODD_PWR_EN_L	13
ENET_LOW_PWR	13
AUD_IP_PERIPHERAL_DET	13
AUD_I2C_INT_L	13
AUD_IPHS_SWITCH_EN	13

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: Func Test / No Test

Apple Inc.

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REVISION: <E4LABEL>

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Functional Test Points

J9500: LIO Connector

FUNC_TEST

TRUE	AUD_PWR_EN	13 57 59
TRUE	PP5V_S0_ALT_AUD_LDO_EN	59
TRUE	SPKRAMP_SHDN_L	45 59
TRUE	PP1V5_S0SW_AUDIO	56 59
TRUE	PP3V3_S0	60 62 72 5 11 12 13 15 17 18 27 30 34 36 37 38 39 40 41 42 43 54 57 59
TRUE	SPKRAMP_INR_N	45 59 72
TRUE	SPKRAMP_INR_P	45 59 72
TRUE	USB3_EXTB_D2R_RC_N	59 63 66
TRUE	USB3_EXTB_D2R_RC_P	59 63 66
TRUE	USB_EXTB_N	14 59 66
TRUE	USB_EXTB_P	14 59 66
TRUE	USB3_EXTB_R2D_N	59 63 66
TRUE	USB3_EXTB_R2D_P	59 63 66
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	SMBUS_SMC_2_S3_SCL	35 38 59 71
TRUE	SMBUS_SMC_2_S3_SDA	35 38 59 71
TRUE	SYS_ONEWIRE	35 59
TRUE	SMC_BC_ACOK	35 36 48 59
TRUE	XDP_USB_EXTB_OC_L	14 16 59
TRUE	USB_PWR_EN	33 57 59
TRUE	FINSTACKSNS_ALERT_L	37 59
TRUE	HDA_SYNC	12 59 67
TRUE	HDA_RST_L	12 59 67
TRUE	HDA_SDOUT	12 59 67
TRUE	HDA_SDIN0	12 59 67
TRUE	HDA_BIT_CLK	12 59 67

(Need to add 5 GND TPs)

J6955: HALL EFFECT Connector

FUNC_TEST

TRUE	SMC_LID_R	46
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63

Power Aliases

63 62 60 56 39 38 34 19 18 15 PP3V3_S3 = PP3V3_S3 15 18 19 34 38 39 56 60 62 63

NO_TEST Nets

NO_TEST MAKE_BASE

66 63 14	NC_USB3RPCIE_SD_D2RP	=	TRUE	TRUE	NC_USB3RPCIE_SD_D2RP	14 63 66
66 63 14	NC_USB3RPCIE_SD_D2RN	=	TRUE	TRUE	NC_USB3RPCIE_SD_D2RN	14 63 66
66 63 14	NC_USB3RPCIE_SD_R2D_CP	=	TRUE	TRUE	NC_USB3RPCIE_SD_R2D_CP	14 63 66 CPU/PCH
66 63 14	NC_USB3RPCIE_SD_R2D_CN	=	TRUE	TRUE	NC_USB3RPCIE_SD_R2D_CN	14 63 66
63 37 35	NC_SMC_ADC16	=	TRUE	TRUE	NC_SMC_ADC16	35 63 37 SMC

Bead Probes

66 59 14	USB3_EXTB_D2R_N	1	SM BEAD-PROBE	BPA511
66 59 14	USB3_EXTB_D2R_P	1	SM BEAD-PROBE	BPA510
66 63 59	USB3_EXTB_D2R_RC_N	1	SM BEAD-PROBE	BPA520
66 63 59	USB3_EXTB_D2R_RC_P	1	SM BEAD-PROBE	BPA521
66 59 14	USB3_EXTB_R2D_C_N	1	SM BEAD-PROBE	BPA513
66 59 14	USB3_EXTB_R2D_C_P	1	SM BEAD-PROBE	BPA512
66 63 59	USB3_EXTB_R2D_N	1	SM BEAD-PROBE	BPA523
66 63 59	USB3_EXTB_R2D_P	1	SM BEAD-PROBE	BPA522

Unused nets with offpage

(Nets with offpages not used on this project)

SD_RESET_L 15
XDP_SDCONN_STATE_CHANGE_L 15 16
SD_PWR_EN 15

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Project FCT/NC/Aliases

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J41/J43 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,MEM_TERM	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.110 MM	0.110 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110MM		0.095 MM	0.095 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL2,ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL3,ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL3,ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL4,ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

SYNC_MASTER=J43 MLB SYNC_DATE=10/24/2012

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PCB Rule Definitions

Apple Inc.

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

Note: DisplayPort tables are on Page 113

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	6 36
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
	CPU_45S	CPU_TTP	XDP_DBRESET_L	16 17
	CPU_45S	CPU_TTP	XDP_CPU_PRDY_L	6 16 62
	CPU_45S	CPU_TTP	XDP_CPU_PREQ_L	6 16 62
	CPU_27P4S	CPU_COMP	EDP_COMP	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
	CPU_45S	CPU_TTP	CPU_CFG<11..0>	6 16 62
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 35
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 35 36 49
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	15 36
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU_45S	CPU_TTP	XDP_CPU_TDI	6 16 62
XDP_TDO	CPU_45S	CPU_TTP	XDP_CPU_TDO	6 16 62
XDP_TMS	CPU_45S	CPU_TTP	XDP_CPU_TMS	6 16 62
XDP_TCK	CPU_45S	CPU_TTP	XDP_CPU_TCK	6 16 62
XDP_TRST_L	CPU_45S	CPU_TTP	XDP_CPUPCH_TRST_L	6 12 16 62
XDP_BPM_L	CPU_45S	CPU_TTP	XDP_BPM_L<1..0>	6 16
	CPU_45S	CPU_TTP	XDP_BPM_L<7..2>	6 16
	CPU_45S	CPU_TTP	XDP_OBSDATA_B<3..0>	
	CPU_45S	CPU_TTP	CPU_CFG<15..12>	6 16
(FSB_CPURST_L)	CPU_45S	CPU_TTP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 49
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 49
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 49
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	8 49
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 49
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	12 30
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	12 30
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	30 62
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	30 62
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	12 30 62
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 62
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	5 25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	5 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	5 18 25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	5 18 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	13 18 25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	13 18 25
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	58 62
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	58 62
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 58 62
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 58
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 58
	DP_80D	DP_AUX	DP_INT_AUXCH_P	
	DP_80D	DP_AUX	DP_INT_AUXCH_N	

PCIe SSD

DP

SYNC_MASTER=J43_MLB SYNC_DATE=09/21/2012

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CPU Constraints

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	
USB_BT	USB_80D	USB	USB_BT_P	14 29
USB_BT	USB_80D	USB	USB_BT_N	14 29
	USB_80D	USB	USB_BT_CONN_P	29 62
	USB_80D	USB	USB_BT_CONN_N	29 62
	USB_80D	USB	USB_BT_WAKE_P	
	USB_80D	USB	USB_BT_WAKE_N	
USB_TPAD	USB_80D	USB	USB_TPAD_P	14 34 62
USB_TPAD	USB_80D	USB	USB_TPAD_N	14 34 62
	USB_80D	USB	USB_TPAD_CONN_P	
	USB_80D	USB	USB_TPAD_CONN_N	
	USB_80D	USB	TPAD_SPI_MOSI_USB_P	
	USB_80D	USB	TPAD_SPI_MISO_USB_N	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	
	SPI_45S	SPI	TPAD_SPI_MOSI	15 34
	SPI_45S	SPI	TPAD_SPI_MISO	15 34
	SPI_45S	SPI	TPAD_SPI_CLK	15 34
USB_EXTA	USB_80D	USB	USB_EXTA_P	14 33
USB_EXTA	USB_80D	USB	USB_EXTA_N	14 33
	UART_45S	UART	SMC_DEBUGPRT_TX_L	33 35 36
	UART_45S	UART	SMC_DEBUGPRT_RX_L	33 35 36
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_P	33
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_N	33
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_P	33
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_N	33
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 33
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 33
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	33
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	33
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_P	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_P	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 33
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 33
USB_EXTB	USB_80D	USB	USB_EXTB_P	14 59 63
USB_EXTB	USB_80D	USB	USB_EXTB_N	14 59 63
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_P	14 59 63
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_N	14 59 63
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_P	59 63
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_N	59 63
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P	59 63
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N	59 63
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_P	14 59 63
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_N	14 59 63
USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RP	14 63
USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RN	14 63
USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CP	14 63
USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CN	14 63
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P	
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N	
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P	
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	

USB Hucopyb nets

TP SPI nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

SYNC_MASTER=CLEAN_J41 SYNC_DATE=11/13/2012

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Apple Inc.

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
LPC_AD	LPC_45S	LPC	LPC_AD<3..0> 14 35 44 62
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L 14 35 44 62
	LPC_45S	LPC	LPCPLUS_RESET_L 18 44 62
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC 17 35
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R 12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS 17 44 62
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS_R 12 17
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK 14 16 19 25 38 54
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA 14 16 19 25 38 54
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK 14 38
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA 14 38
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL 14 32 35 38 41 42 62 71
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA 14 32 35 38 41 42 62 71
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK 12 59 63
	HDA_45S	HDA	HDA_BIT_CLK_R 12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC 12 59 63
	HDA_45S	HDA	HDA_SYNC_R 12
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L 12
	HDA_45S	HDA	HDA_RST_L 12 59 63
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0 12 59 63
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT 12 59 63
	HDA_45S	HDA	HDA_SDOUT_R 12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R 13 36
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K 35 36
SPI_CLK	SPI_45S	SPI	SPI_CLK_R 14 44
	SPI_45S	SPI	SPI_CLK 44
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R 14 44
	SPI_45S	SPI	SPI_MOSI 44
SPI_MISO	SPI_45S	SPI	SPI_MISO 14 44
	SPI_45S	SPI	SPI_MISO_R 44
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L 14 44
	SPI_45S	SPI	SPI_CS0_L 44
	SPI_45S	SPI	SPI_SMC_CLK 35 44
	SPI_45S	SPI	SPI_SMC_MOSI 35 44
	SPI_45S	SPI	SPI_SMC_MISO 35 44
	SPI_45S	SPI	SPI_SMC_CS_L 35 44
	SPI_45S	SPI	SPI_MLB_CLK 44
	SPI_45S	SPI	SPI_MLB_MOSI 44
	SPI_45S	SPI	SPI_MLB_MISO 44
	SPI_45S	SPI	SPI_MLB_CS_L 44
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P 29 62
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N 29 62
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P 14 29
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N 14 29
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P 14 29 62
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N 14 29 62
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P 12 29 62
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N 12 29 62
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0> 25
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0> 25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0> 14 25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0> 14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0> 14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0> 14 25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0> 25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0> 25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P 12 25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N 12 25
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N
XDP_TDI	PCH_45S	PCH_TTP	XDP_PCH_TDI 12 16 62
XDP_TDO	PCH_45S	PCH_TTP	XDP_PCH_TDO 12 16 62
XDP_TMS	PCH_45S	PCH_TTP	XDP_PCH_TMS 12 16 62
XDP_TCK	PCH_45S	PCH_TTP	XDP_PCH_TCK 12 16 62
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P 31 32
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N 31 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P 14 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N 14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P 14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N 14 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P 31 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N 31 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P 12 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N 12 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P 31 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N 31 32

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA 17 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP 31 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN 31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT 17 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R 25
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1 17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2 17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R 17
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R
	CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1

SYNC_MASTER=J43_MLB SYNC_DATE=09/14/2012

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_CS_L<1..0>
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_ODT<0>
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_CS_L<1..0>
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_ODT<0>
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_N<7>
		MEM_PWR	PP1V2_S3
		MEM_PWR	PP0V6_S3_MEM_VREFCA_A
		MEM_PWR	PP0V6_S3_MEM_VREFDQ_A
		MEM_PWR	PP0V6_S3_MEM_VREFCA_B
		MEM_PWR	PP0V6_S3_MEM_VREFDQ_B

SYNC_MASTER=CHINMAY_J41 SYNC_DATE=09/07/2012

PAGE TITLE: Memory Constraints

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0> 25 28
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0> 25 28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0> 28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0> 28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1> 25 28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1> 25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3> 25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3> 25 28
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2> 28
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2> 28
	DP_80D	DP_TX	DP_A_LSX_ML_P<1> 28
	DP_80D	DP_TX	DP_A_LSX_ML_N<1> 28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0> 28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0> 28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1> 25 28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1> 25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0> 25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0> 25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P 25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N 25 28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P 28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N 28
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P 28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N 28
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0> 62
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0> 62
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CP<3..1:2> 62
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CN<3..1:2> 62
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0> 62
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0> 62
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CP 25 62
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CN 25 62
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 25
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 25
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 25
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 25

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=CHINMAY_J41 SYNC_DATE=09/07/2012

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 31 32
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 31 32
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 31 32
101	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 31 32
102		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 32
103	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 31 32
104	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 31 32
105	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 31 32
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 31 32
106	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 31 32
107	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 31 32
108	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 31 32
109	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 31 32
110	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 31 32
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 31 32
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 31 32
122	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 31 32
123	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 31 32
124		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 32 62
125		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 32 62
131	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 31 32
132	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 31 32
133		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 32 62
134		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 32 62
140			S2_MEM_PWR	PP1V35_CAM 31 32
141			S2_MEM_PWR	PP0V675_CAM_VREF 31 32
142			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 32
143			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ 32

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
2TO1_DIFFPAIR	*	=STANDARD	0.2 MM	0.1 MM	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL 35 38 58
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA 35 38 58
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL 14 32 35 38 41 42 62 67
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA 14 32 35 38 41 42 62 67
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL 35 38 59 63
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA 35 38 59 63
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL 34 35 38 42 62
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA 34 35 38 42 62
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL 35 38 46 48 62
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA 35 38 46 48 62

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SENSE_DIFFPAIR			CHGR_CSI_P 48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSI_N 48
	2TO1_DIFFPAIR		CHGR_CSI_R_P 48
	2TO1_DIFFPAIR		CHGR_CSI_R_N 48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_P 48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_N 48
	2TO1_DIFFPAIR		CHGR_CSO_R_P 41 48
	2TO1_DIFFPAIR		CHGR_CSO_R_N 41 48

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1TO1_DIFFPAIR	0.200 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
THERM_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SPKR_DIFFPAIR	*	=1TO1_DIFFPAIR	0.300 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P 42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N 42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P 42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N 42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P 42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N 42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_P 42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_N 42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P 42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N 42
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P 40 50
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N 40 50
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_P 40 50
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_N 40 50
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P_R 40 41
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N_R 40 41
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_P 40
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_N 40
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_P 40
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_N 40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_N 40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_P 40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_P 39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_N 39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_N 39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_P 39
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_P 40 53
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_N 40 53
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N 39 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P 39 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N 39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P 39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_N 39 51
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_P 39 51
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N 39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P 39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N 39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P 39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N 39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P 39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_N 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_P 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_N 41 42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_P 41 42
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P 45 59 63
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N 45 59 63
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_P 45
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_N 45
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P 45 62
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N 45 62
		SB_POWER	PP3V3_S5 8 11 13 15 16 17 18 28 29 40 52 55 56 57 58 60 62 63
		SB_POWER	PP3V3_S0 8 11 12 13 15 17 18 27 30 34 36 37 38 39 40 41 42 43 54 57 59
	GND		GND

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<rdar://component/512995> J41 HW EE Schematic | Pre Proto 1
<rdar://component/508412> J41 HW EE Schematic | Proto 1
<rdar://component/508413> J41 HW EE Schematic | EVT
<rdar://component/508414> J41 HW EE Schematic | DVT

Kismet:

afp://kismet.apple.com/Kismet-Projects/J41-J43

Useful Wiki Links:

Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions
Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:

<rdar://component/497591> MobileMac HW | Task
<rdar://component/497587> MobileMac HW | Schematic
<rdar://component/497585> MobileMac HW | New Bugs
<rdar://component/497588> MobileMac HW | Layout
<rdar://component/497590> MobileMac HW | Investigation
<rdar://component/497589> MobileMac HW | Architecture

Other Info:

Page Allocations - <rdar://problem/11791318> 2012 Schematic Page Allocations

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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