1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-02-23

J11 MLB PIB SCHEMATIC
2.6.0
02/23/12

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17	19	PCH DMI/FDI/PM/Graphics	J13_MLB	10/06/2011
18	20	PCH PCI/USB/TP/RSVD	J13_MLB	09/22/2011
19	21	PCH GPIO/MISC/NCTF	J13_MLB	02/23/2012
20	22	PCH POWER	J13_MLB	09/22/2011
21	23	PCH GROUNDS	J13_MLB	08/12/2011
22	24	PCH DECOUPLING	J13_MLB	11/18/2011
23	25	CPU & PCH XDP	J13_MLB	08/04/2011
24	26	USB HUB & MUX	J13_MLB	08/12/2011
25	27	Clock (CK505) and Chipset Support	J13_MLB	08/12/2011
26	28	CPU Memory S3 Support	J13_MLB	11/18/2011
27	29	DDR3 DRAM CHANNEL A (0-31)	J13_MLB	08/29/2011
28	30	DDR3 DRAM CHANNEL A (32-63)	J13_MLB	08/29/2011
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30	32	DDR3 DRAM CHANNEL B (32-63)	J13_MLB	08/29/2011
31	33	FSB/DDR3/FRAMEBUF Vref Margining	J13_MLB	11/18/2011
32	34	DDR3 DRAM Channel B (32-63)	K21_MLB	12/13/2010
33	36	Thunderbolt Host (1 of 2)	J13_MLB	02/22/2012
34	37	Thunderbolt Host (2 of 2)	J13_MLB	09/01/2011
35	38	TBT Power Support	J13_MLB	11/18/2011
36	40	X21 WIRELESS CONNECTOR	J13_MLB	10/06/2011
37	45	SSD CONNECTOR	J13_MLB	11/18/2011
38	46	External A USB3 Connector	J13_MLB	10/06/2011
39	47	LIO CONNECTORS	N/A	N/A
40	49	SMC	J30_MLB	07/26/2011
41	50	SMC Support	J13_MLB	10/06/2011
42	51	LPC+SPI Debug Connector	K21_MLB	12/13/2010
43	52	SMBus Connections	J13_MLB	10/05/2011
44	53	Voltage & Load Side Current Sensing	J13_MLB	09/15/2011
45	54	High Side Current Sensing	J13_MLB	09/15/2011
46	55	Thermal Sensors	J13_MLB	08/30/2011
47	56	Fan	K21_MLB	12/13/2010
48	57	IPD / KBD Backlight	K21_MLB	12/13/2010
49	61	SPI ROM	J13_MLB	10/13/2011
50	62	AUDI0: SPEAKER AMP	K21_MLB	12/13/2010
51	69	DC-In & Battery Connectors	K21_MLB	11/11/2010
52	70	PBus Supply & Battery Charger	J13_MLB	10/10/2011
53	71	System Agent Supply	J13_MLB	09/01/2011
54	72	5V / 3.3V Power Supply	J13_MLB	11/18/2011
55	73	1.5V DDR3 Supply	J13_MLB	10/07/2011
56	74	CPU IMVP7 & AXG VCore Regulator	J13_MLB	09/22/2011
57	75	CPU IMVP7 & AXG VCore Output	K21_MLB	12/13/2010
58	76	CPU VCCIO (1.05V) Power Supply	J13_MLB	09/01/2011
59	77	Misc Power Supplies	K21_MLB	12/13/2010
60	78	Power FETs	K21_MLB	12/13/2010
61	79	Power Control 1/ENABLE	J13_MLB	11/18/2011
62	90	Internal DisplayPort Connector	K21_MLB	12/13/2010
63	94	Thunderbolt Connector A	J13_MLB	11/18/2011
64	97	LCD Backlight Driver	J13_MLB	10/13/2011
65	100	CPU Constraints	CONSTRAINTS	01/11/2012
66	101	Memory Constraints	CONSTRAINTS	01/11/2012
67	102	PCH Constraints 1	CONSTRAINTS	01/11/2012
68	103	PCH Constraints 2	CONSTRAINTS	01/11/2012
69	105	Thunderbolt Constraints	CONSTRAINTS	01/11/2012
70	106	SMC Constraints	CONSTRAINTS	01/11/2012
71	108	Project Specific Constraints	CONSTRAINTS	01/11/2012
72	109	PCB Rule Definitions	CONSTRAINTS	01/11/2012

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9276	1	SCHEM,MLB,J11	SCH	CRITICAL	
820-3208	1	PCBF,MLB,J11	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Thu Feb 23 12:05:40 2012

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE: SCHEM,MLB,J11

Apple Inc.

DRAWING NUMBER: 051-9276 | SIZE: D
REVISION: 2.7.0
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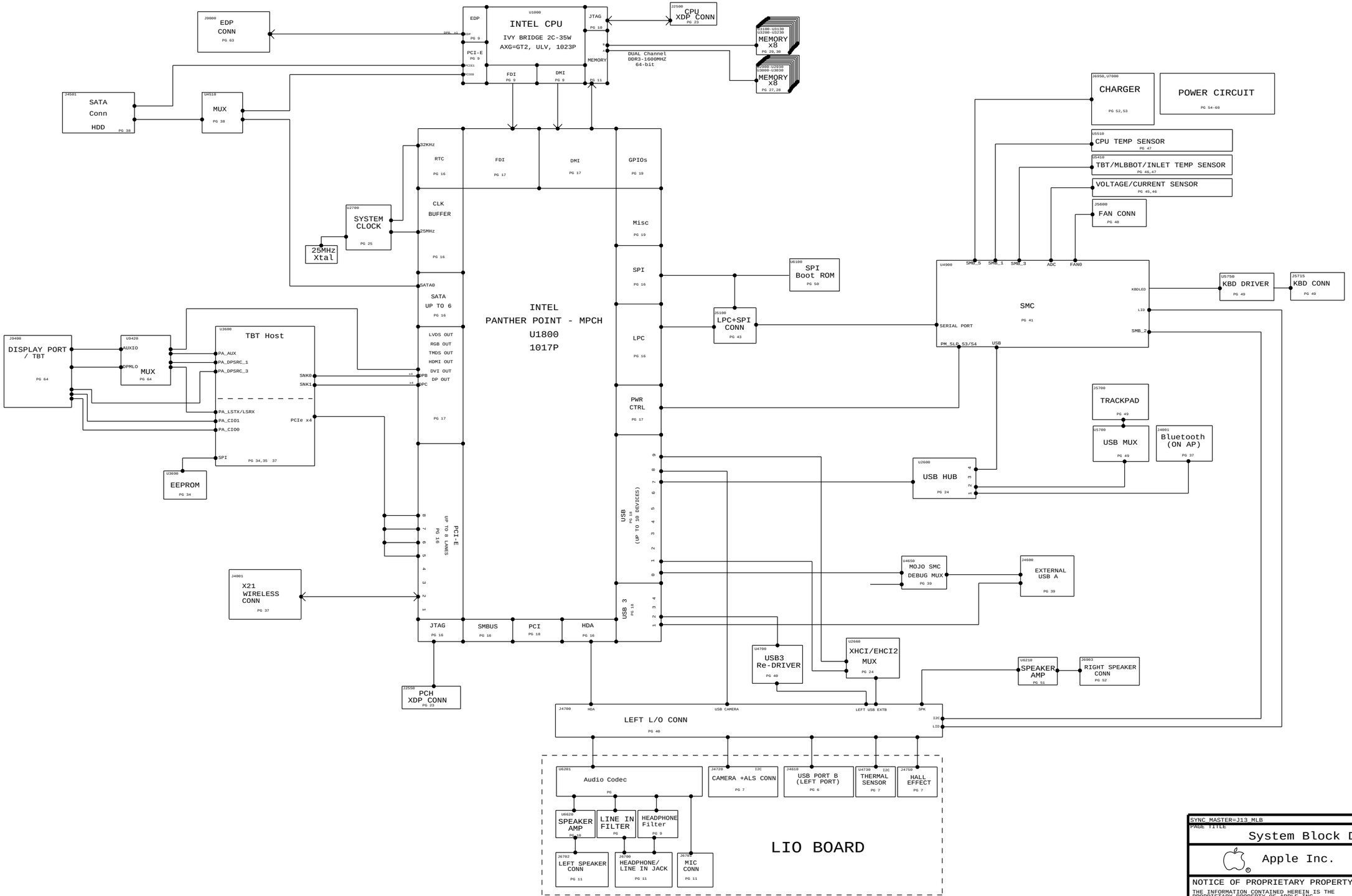

SYNC MASTER=J13_MLB SYNC DATE=11/18/2013

PAGE TITLE

System Block Diagram

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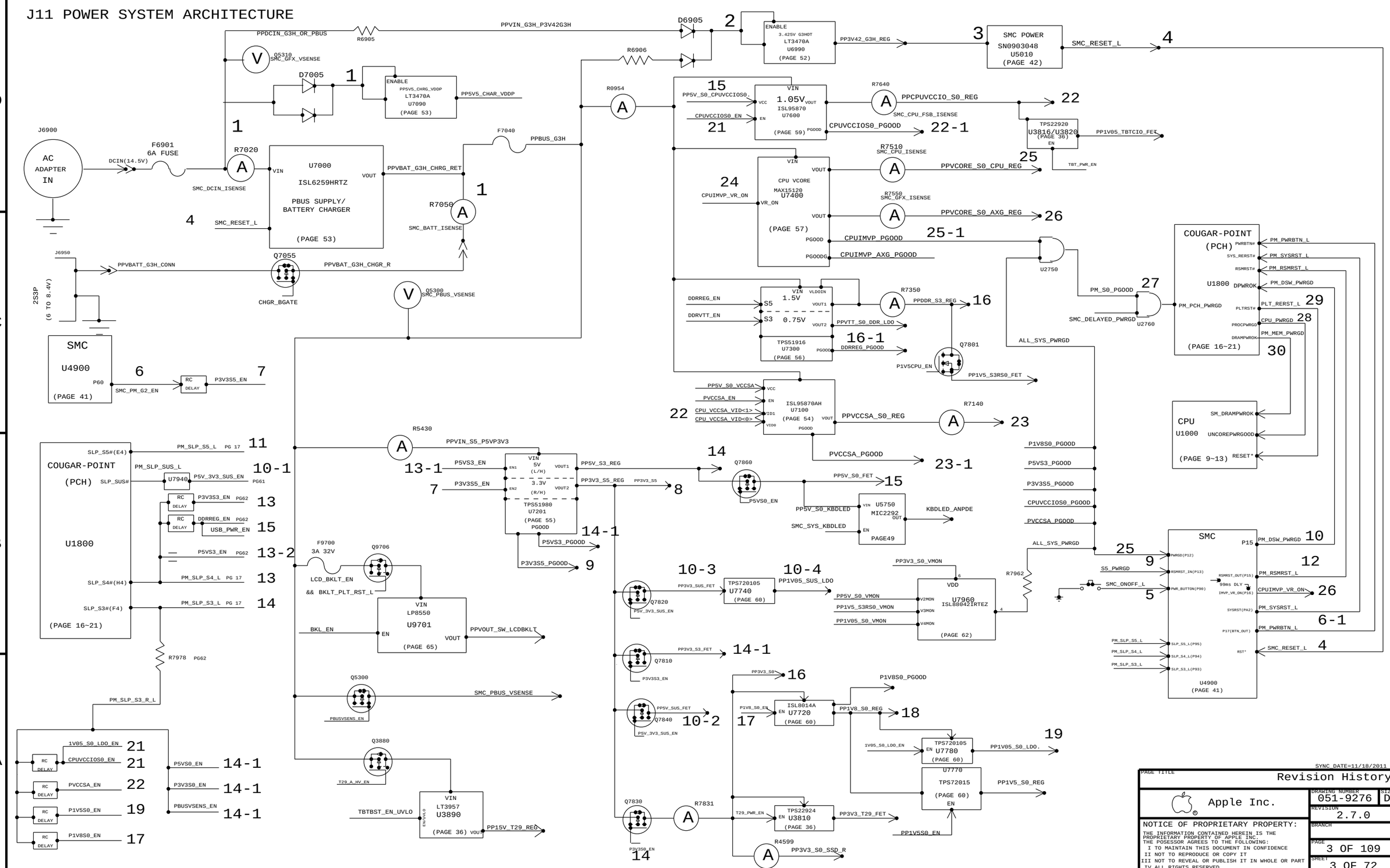
J11 POWER SYSTEM ARCHITECTURE



BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3469	PCBA,MLB,1.5GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKL,DDR3:HYNIX_4GB
639-3470	PCBA,MLB,1.5GHZ,SA 4GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKH,DDR3:SAMSUNG_4GB
639-3473	PCBA,MLB,1.5GHZ,HY 8GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKJ,DDR3:HYNIX_8GB
639-3659	PCBA,MLB,1.5GHZ,EL 8GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:F0V3,DDR3:ELPIDA_8GB
639-3471	PCBA,MLB,1.7GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKK,DDR3:HYNIX_4GB
639-3472	PCBA,MLB,1.7GHZ,SA 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKF,DDR3:SAMSUNG_4GB
639-3775	PCBA,MLB,1.7GHZ,EL 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F27J,DDR3:ELPIDA_4GB
639-3474	PCBA,MLB,1.7GHZ,HY 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKG,DDR3:HYNIX_8GB
639-3774	PCBA,MLB,1.7GHZ,SA 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F27D,DDR3:SAMSUNG_8GB
639-3660	PCBA,MLB,1.7GHZ,EL 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F0V4,DDR3:ELPIDA_8GB
639-3776	PCBA,MLB,2.0GHZ,HY 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27K,DDR3:HYNIX_4GB
639-3778	PCBA,MLB,2.0GHZ,SA 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27G,DDR3:SAMSUNG_4GB
639-3780	PCBA,MLB,2.0GHZ,EL 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27H,DDR3:ELPIDA_4GB
639-3777	PCBA,MLB,2.0GHZ,HY 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27C,DDR3:HYNIX_8GB
639-3779	PCBA,MLB,2.0GHZ,SA 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27F,DDR3:SAMSUNG_8GB
639-3781	PCBA,MLB,2.0GHZ,EL 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F279,DDR3:ELPIDA_8GB
085-3937	J11 MLB DEVELOPMENT BOM	J11_DEVEL:ENG
607-9089	CMN PTS,PCBA,MLB,J11	J11_COMMON
939-0479	PCBA,MLB,1.9GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.9GHZ,EEEE:DYKL,DDR3:HYNIX_4GB

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKL]	CRITICAL	EEEE:DYKL
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKH]	CRITICAL	EEEE:DYKH
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKK]	CRITICAL	EEEE:DYKK
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKF]	CRITICAL	EEEE:DYKF
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKJ]	CRITICAL	EEEE:DYKJ
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKG]	CRITICAL	EEEE:DYKG
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F0V3]	CRITICAL	EEEE:F0V3
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F0V4]	CRITICAL	EEEE:F0V4
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F279]	CRITICAL	EEEE:F279
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27C]	CRITICAL	EEEE:F27C
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27D]	CRITICAL	EEEE:F27D
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27F]	CRITICAL	EEEE:F27F
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27G]	CRITICAL	EEEE:F27G
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27H]	CRITICAL	EEEE:F27H
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27J]	CRITICAL	EEEE:F27J
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27K]	CRITICAL	EEEE:F27K

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3937	1	J11 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9089	1	CMN PTS,PCBA,MLB,J11	CMNPTS	CRITICAL	J11_CMNPTS

SYNC_MASTER=K21_MLB SYNC_DATE=11/16/2010

PAGE TITLE

K78 BOM Variants

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DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

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J11 BOM GROUPS

BOM GROUP	BOM OPTIONS
J11_COMMON	ALTERNATE,COMMON,J11_MISC,J11_DEBUG:ENG,J11_PROGPARTS,USBHUB2513B,EDP:YES,PCH_C1
J11_MISC	HUB_3NONREM,TBT,MPM5:YES,CPUMEM_SLG:NO,PP5VS_DCIN:NO,TPAD_PCH:NO,SKIP_5V3V3:INAUDIBLE,BTPWR:S4,TBTHV:P15V,LVDDR3_HW:YES,AXG_ACOUSTICS:NO
J11_PROGPARTS	BOOTROM_PROG,SMC_PROG,TBTROM:PROG
J11_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,XDP_PCH,DDRVREF_DAC,VREFDQ:M1_M3,VREFCA:LDO_DAC,S0PGOOD_ISL,S3_S0_LED,VCCIOISNS_ENG,AIRPORTISNS_ENG,HDDISNS_ENG,LCDBKLTISNS_ENG
J11_DEVEL:PVT	XDP_CONN
J11_DEBUG:ENG	DEVEL_BOM,MOJO:YES,XDP,XDP_CPU:BPM,LPCPLUS
J11_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,MOJO:YES,XDP,LPCPLUS,VREFDQ:LDO,VREFCA:LDO,XDP_CPU:BPM,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
J11_DEBUG:PROD	BKLT:PROD,MOJO:YES,XDP,LPCPLUS,VREFDQ:LDO,VREFCA:LDO,XDP_CPU:BPM,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2X3QFN	U3690	CRITICAL	TBTROM:BLANK
341S3526	1	IC,EEPROM,Cactus Ridge (V1.2) PIB, J11/J13	U3690	CRITICAL	TBTROM:PROG
338S1098	1	IC,SMC12-A3,40MHZ/50DMIPS MCU,9X9,157BGA	U4900	CRITICAL	SMC_BLANK
341S3434	1	IC,SMC,PIB,J11	U4900	CRITICAL	SMC_PROG
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_BLANK
341S3527	1	IC,EFI ROM,PIB,J11/J13	U6100	CRITICAL	BOOTROM_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
138S0676	138S0691		ALL	Murata alt to Samsung
371S0709	371S0652		ALL	NXP alt to NXP
138S0671	138S0673		ALL	Taiyo alt to Murata
152S1085	152S1307		ALL	Toko alt to Cyntec
152S1462	152S1295		ALL	Toko alt to NEC inductor
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S1493	152S1300		ALL	Coilcraft MA5274 alt to Murata
152S0586	152S1301		ALL	Dale/Vishay alt to Cyntec
353S3238	353S1428		ALL	Intersil alt to OPA2333
372S0186	372S0185		ALL	NXP alt to Diodes
197S0431	197S0432		ALL	200uW Epson alt to NDK
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0903	376S0796		ALL	Fairchild alt to Siliconix
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0333	998-4435		ALL	Sanyo alt to Kemet
128S0357	998-4435		ALL	Sanyo High Voltage Polymer alt
998-4715	998-4435		ALL	Kemet Rectangular Design alt
998-4716	998-4435		ALL	Kemet Flute Design alt

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4197	1	IVB,QBP8,ES2,K0,1.5,17W,2+2,0.95,4M,ULVB	U1000	CRITICAL	CPU:1.5GHZ
337S4299	1	IVB,QC9E,Q5,L1,1.7,17W,2+2,1.05,3M,ULVBG	U1000	CRITICAL	CPU:1.7GHZ
337S4296	1	IVB,QC9B,Q5,L1,2.0,17W,2+2,1.15,4M,ULVBG	U1000	CRITICAL	CPU:2.0GHZ
337S4198	1	IVB,QBTP,ES2,K0,1.5,17W,2+2,0.95,4M,ULVBGA	U1000	CRITICAL	CPU:1.5GHZTDP
337S4299	1	IVB,QC9E,Q5,L1,1.7,17W,2+2,1.05,3M,ULVBG	U1000	CRITICAL	CPU:1.7GHZTDP
337S4296	1	IVB,QC9B,Q5,L1,2.0,17W,2+2,1.15,4M,ULVBG	U1000	CRITICAL	CPU:2.0GHZTDP
337S4297	1	IVB,QC9C,Q5,L1,1.9,17W,2+2,1.15,4M,ULVBG	U1000	CRITICAL	CPU:1.9GHZ
337S4165	1	IC,PCH,PPT-MB,SFF,ES1	U1800	CRITICAL	PCH_ES1
337S4180	1	IC,PCH,PPT-MB,SFF,ES2,B0	U1800	CRITICAL	PCH_ES2
337S4235	1	IC,PCH,PPT-MB,SFF,P-QS,C0	U1800	CRITICAL	PCH_C0
337S4275	1	IC,PCH,PPT-MB,QS77,C1,QS	U1800	CRITICAL	PCH_C1
337S4275	1	IC,PCH,PPT-MB,QS77,C1,QS	U1800	CRITICAL	PCH_C1TDP
338S1108	1	IC,TBT,CR-4C,LP,ES3,288 FCBGA,12X12MM	U3600	CRITICAL	TBT
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GEMMA,78P FPGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GEMMA,78P FPGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GEMMA,78P FPGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GEMMA,78P FPGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_8GB
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	
353S2929	1	IC,ISL6259,BATCHARGER,3%,4C4MM,QFN28	U7000	CRITICAL	
946-3116	1	MLB,DYMAX UV EB 0.22 GRAM,K78	GLUE	CRITICAL	

PD Module Parts

806-3706	1	CAN,TOPSIDE,COVER,ALT,J11/J13	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3705	1	CAN,TOPSIDE,FENCE,ALT,J11/J13	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-3214	1	CAN,TOPSIDE,J11/J13	TBTTOPSIDE_1P	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	

SYNC_MASTER=J11_MLB_NON_POR SYNC_DATE=11/09/2011

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BOM Configuration

Apple Inc.

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Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN_F (Need 6 TPs)	36 41
TRUE	WIFI_EVENT_L	36 40 41
TRUE	PCIE_AP_R2D_N	36 68
TRUE	PCIE_AP_R2D_P	36 68
TRUE	PCIE_CLK100M_AP_N	16 36 68
TRUE	PCIE_CLK100M_AP_P	16 36 68
TRUE	USB_BT_CONN_P	36 67
TRUE	USB_BT_CONN_N	36 67
TRUE	PCIE_AP_D2R_P	16 36 68
TRUE	PCIE_AP_D2R_N	16 36 68
TRUE	PCIE_WAKE_L	17 36
TRUE	AP_RESET_CONN_L	36
TRUE	AP_CLKREQ_O_L	36
TRUE	PP3V3_S3RS4_BT_F	36

(Need to add 8 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST

TRUE	PP3V3_S0_SSD_FLT (Need 5 TPs)	37
TRUE	SATA_SSD_D2R_P	37 67
TRUE	SATA_SSD_D2R_N	37 67
TRUE	SATA_SSD_R2D_N	37 67
TRUE	SATA_SSD_R2D_P	37 67
TRUE	SMC_OOB1_RX_L	37 40
TRUE	SMC_OOB1_TX_L	37 40 41
TRUE	PCIE_SSD_D2R_N<1>	8 37 65
TRUE	PCIE_SSD_D2R_P<1>	8 37 65
TRUE	PCIE_SSD_R2D_N<1>	37 65
TRUE	PCIE_SSD_R2D_P<1>	37 65
TRUE	PCIE_CLK100M_SSD_N	16 37 65
TRUE	PCIE_CLK100M_SSD_P	16 37 65
TRUE	SSD_CLKREQ_L	16 37
TRUE	SSD_RESET_L	25 37
TRUE	SATA_PCIE_SEL	37
TRUE	SSD_P3V3S0_EN	37

(Need to add 6 GND TPs)

J4700: LIO Connector

FUNC_TEST

TRUE	=PP3V42_G3H_ONEWIRE	7 39
TRUE	=PP3V3_S0_AUDIO	7 39
TRUE	=PP3V3R1V5_S0_AUDIO	7 39
TRUE	SYS_ONEWIRE	39 40
TRUE	SMC_BC_ACOK	39 40 41
TRUE	=USB_PWR_EN	38 39 61
TRUE	=I2C_LIO_SDA	39 43
TRUE	=I2C_LIO_SCL	39 43
TRUE	=I2C_MIKEY_SCL	39 43
TRUE	=I2C_MIKEY_SDA	39 43
TRUE	AUD_IPHS_SWITCH_EN	25 39
TRUE	AUD_IP_PERIPHERAL_DET	18 39
TRUE	AUD_I2C_INT_L	18 39
TRUE	AUD_GPIO_3	39 50
TRUE	SPKRAMP_INR_N	39 50 71
TRUE	SPKRAMP_INR_P	39 50 71
TRUE	USB_EXTB_N	24 39 67
TRUE	USB_EXTB_P	24 39 67
TRUE	USB_CAMERA_N	18 39 67
TRUE	USB_CAMERA_P	18 39 67
TRUE	HDA_SDOUT	16 39 68
TRUE	HDA_BIT_CLK	16 39 68
TRUE	HDA_SDIN0	16 39 68
TRUE	USB_EXTB_OC_L	23 39
TRUE	HDA_RST_L	16 39 68
TRUE	HDA_SYNC	16 39 68
TRUE	USB3_EXTB_RX_RC_N	39 67
TRUE	USB3_EXTB_RX_RC_P	39 67
TRUE	USB3_EXTB_TX_C_P	39 67
TRUE	USB3_EXTB_TX_C_N	39 67

(Need to add 5 GND TPs)

J5100: LPC+SPI Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	7 42
TRUE	=PP5V_S0_LPCPLUS	7 42
TRUE	LPC_AD<3..0>	16 40 42 68
TRUE	SPI_ALT_MOSI	42
TRUE	SPI_ALT_MISO	42
TRUE	LPC_FRAME_L	16 40 42 68
TRUE	PM_CLKRUN_L	17 40 42
TRUE	SMC_TMS	40 41 42
TRUE	LPCPLUS_RESET_L	25 42 68
TRUE	SMC_TDO	40 41 42
TRUE	TP_SMC_TRST_L	42
TRUE	TP_SMC_MD1	42
TRUE	SMC_TX_L	40 41 42
TRUE	LPC_CLK33M_LPCPLUS	25 42 68
TRUE	SPIROM_USE_MLB	19 42 49
TRUE	SPI_ALT_CLK	42
TRUE	SPI_ALT_CS_L	42
TRUE	LPC_SERIRQ	16 40 42
TRUE	LPC_PWRDWN_L	17 25 40 42
TRUE	SMC_TDI	40 41 42
TRUE	SMC_TCK	40 41 42
TRUE	SMC_RESET_L	40 41 42 52
TRUE	SMC_ROMBOOT	41 42
TRUE	SMC_RX_L	40 41 42
TRUE	LPCPLUS_GPIO	19 42

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST

TRUE	=PP5V_S0_FAN	7 47
TRUE	FAN_RT_TACH	47
TRUE	FAN_RT_PWM	47

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST

TRUE	SMC_PME_S4_WAKE_L	40 41 48
TRUE	PP5V_TPAD_FILT	48
TRUE	=PP3V42_G3H_TPAD	7 48
TRUE	PP3V3_TPAD_CONN	48
TRUE	USB_TPAD_P	48 67
TRUE	USB_TPAD_N	48 67
TRUE	=I2C_TPAD_SDA	43 48
TRUE	=I2C_TPAD_SCL	43 48
TRUE	SMC_ONOFF_L	40 41 48
TRUE	SMC_LID	40 41 48 51
TRUE	SMC_TPAD_RST_L	41 48

(Need to add 5 GND TPs)

J6900: DC-In Connector

FUNC_TEST

TRUE	=PP18V5_DCIN_CONN	7 51	(Need 4 TPs)
TRUE	=PP5V_S3_LIO_CONN	7 51	(Need 3 TPs)

(Need to add 5 GND TPs)

J6903: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_ROUT_P	50 51 71
TRUE	SPKRAMP_ROUT_N	50 51 71

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	51 52	(Need 4 TPs)
TRUE	=SMBUS_BATT_SCL	43 51	
TRUE	=SMBUS_BATT_SDA	43 51	
TRUE	SYS_DETECT_L	51	

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST

TRUE	PPVOUT_SW_LCDBKLT	62 64	(Need 2 TPs)
TRUE	PP3V3_SW_LCD	62	(Need 2 TPs)
TRUE	I2C_TCON_SDA_R	62	
TRUE	LED_RETURN_6	62 64	
TRUE	LED_RETURN_5	62 64	
TRUE	LED_RETURN_4	62 64	
TRUE	LED_RETURN_3	62 64	
TRUE	LED_RETURN_2	62 64	
TRUE	LED_RETURN_1	62 64	
TRUE	DP_INT_HPD_CONN	62	
TRUE	DP_INT_AUX_CH_C_N	62 65	
TRUE	DP_INT_AUX_CH_C_P	62 65	
TRUE	DP_INT_ML_F_P<0>	62 65	
TRUE	DP_INT_ML_F_N<0>	62 65	
TRUE	I2C_TCON_SCL_R	62	

(Need to add 5 GND TPs)

J5715: KB BKLT Connector

FUNC_TEST

TRUE	KBDLED_FB	48
TRUE	KBDLED_ANODE	48

(Need to add 2 GND TPs)

J6955: HALL EFFECT Connector

FUNC_TEST

TRUE	SMC_LID_R	51
TRUE	=PP3V42_G3H_HALL	7 51

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	7 51
TRUE	PPVIN_SW_TBTBST	7 35
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	7
TRUE	PPDCIN_G3H	7
TRUE	PP3V42_G3H	7
TRUE	PPVRTC_G3H	7
TRUE	PP5V_S5	7
TRUE	PP5V_SUS	7
TRUE	PP3V3_S5	7 71
TRUE	PP3V3_SUS	7
TRUE	PP3V3_S3	7
TRUE	PP1V8_S0	7
TRUE	PP3V3_S0	7 71
TRUE	PP1V5_S3	7 66
TRUE	PP1V5_S3RS0	7 66
TRUE	PP1V5_S0	7
TRUE	PP1V05_S0	7
TRUE	PPVTTDDR_S3	7
TRUE	PP0V75_S0_DDRVTT	7
TRUE	PPVCCSA_S0_CPU	7
TRUE	PP1V05_SUS	7
TRUE	PP15V_TBT	7
TRUE	PP3V3_TBTLC	7
TRUE	PP1V05_TBTLC	7 35
TRUE	PP1V05_S0_PCH_VCCADPLL	7
TRUE	PPVCORE_S0_CPU	7
TRUE	PPVCORE_S0_AXG	7
TRUE	PP1V5_S3_CPU_VCCDQ	7
TRUE	PP1V05_S0_CPU_VCCPQE	7
TRUE	PP1V8_S0_CPU_VCCPLL_R	7
TRUE	PP1V05_TBTCIO	7
TRUE	PPBUS_S5_HS_OTHER_ISNS	7
TRUE	PPDCIN_G3H_ISOL	7
TRUE	PP5V_S3	7
TRUE	PP5V_S0	7
TRUE	PP3V3_S4	7

NC_EDP_TXP<0..3> MAKE_BASE=TRUE	TRUE	TP_EDP_TX_P<0..3>	9
NC_EDP_TXN<0..3> MAKE_BASE=TRUE	TRUE	TP_EDP_TX_N<0..3>	9
NC_EDP_AUXP MAKE_BASE=TRUE	TRUE	TP_EDP_AUX_P	
NC_EDP_AUXN MAKE_BASE=TRUE	TRUE	TP_EDP_AUX_N	
NC_CPU_THERMDA MAKE_BASE=TRUE	TRUE	TP_CPU_THERMDA	
NC_CPU_THERMDC MAKE_BASE=TRUE	TRUE	TP_CPU_THERMDC	
NC_CPU_RSVD<30..45> MAKE_BASE=TRUE	TRUE	TP_CPU_RSVD<30..45>	
NC_CPU_RSVD<8..27> MAKE_BASE=TRUE	TRUE	TP_CPU_RSVD<8..27>	
NC_PEG_R2D_CP<15..2> MAKE_BASE=TRUE	TRUE	=PEG_R2D_C_P<15..2>	9
NC_PEG_R2D_CN<15..2> MAKE_BASE=TRUE	TRUE	=PEG_R2D_C_N<15..2>	9
NC_PEG_D2RP<15..2> MAKE_BASE=TRUE	TRUE	=PEG_D2R_P<15..2>	9
NC_PEG_D2RN<15..2> MAKE_BASE=TRUE	TRUE	=PEG_D2R_N<15..2>	9

(Need to add 27 GND TPs)

NO_TEST Nets

POWER SIGNALS

I64A	TRUE	VCCSAS0_SREF	53
I64B	TRUE	VCCSAS0_SET1_R	53
I64C	TRUE	VCCSAS0_SET0	53
I64D	TRUE	VCCSAS0_SET1	53

NO_TEST

17 TP_CRT_IG_BLUE	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_BLUE
17 TP_CRT_IG_GREEN	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_GREEN
17 TP_CRT_IG_RED	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_RED
17 TP_CRT_IG_DDC_CLK	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK
17 TP_CRT_IG_DDC_DATA	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA
17 TP_CRT_IG_HSYNC	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_HSYNC
17 TP_CRT_IG_VSYNC	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_VSYNC
TP_LVDS_IG_CTRL_CLK	TRUE	MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK
TP_LVDS_IG_CTRL_DATA	TRUE	MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA
TP_PCH_LVDS_VBG	TRUE	MAKE_BASE=TRUE	NC_PCH_LVDS_VBG
16 TP_HDA_SDIN1	TRUE	MAKE_BASE=TRUE	NC_HDA_SDIN1
16 TP_HDA_SDIN2	TRUE	MAKE_BASE=TRUE	NC_HDA_SDIN2
16 TP_HDA_SDIN3	TRUE	MAKE_BASE=TRUE	NC_HDA_SDIN3
18 TP_PCI_PME_L	TRUE	MAKE_BASE=TRUE	NC_PCI_PME_L
18 TP_PCI_CLK33M_OUT3	TRUE	MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3
16 TP_CLINK_CLK	TRUE	MAKE_BASE=TRUE	NC_CLINK_CLK
16 TP_CLINK_DATA	TRUE	MAKE_BASE=TRUE	NC_CLINK_DATA
16 TP_CLINK_RESET_L	TRUE	MAKE_BASE=TRUE	NC_CLINK_RESET_L
16 TP_PCIE_CLK100M_PEBN	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN
16 TP_PCIE_CLK100M_PEBP	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP
17 TP_SDVO_TVCLKINN	TRUE	MAKE_BASE=TRUE	NC_SDVO_TVCLKINN
17 TP_SDVO_TVCLKINP	TRUE	MAKE_BASE=TRUE	NC_SDVO_TVCLKINP
17 TP_SDVO_STALLN	TRUE	MAKE_BASE=TRUE	NC_SDVO_STALLN
17 TP_SDVO_STALLP	TRUE	MAKE_BASE=TRUE	NC_SDVO_STALLP
17 TP_SDVO_INTN	TRUE	MAKE_BASE=TRUE	NC_SDVO_INTN
17 TP_SDVO_INTP	TRUE	MAKE_BASE=TRUE	NC_SDVO_INTP
23 TP_XDP_PCH_OBSFN_A<0..1>	TRUE	MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>
23 TP_XDP_PCH_OBSFN_B<0..1>	TRUE	MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>
23 TP_XDPPCH_HOOK2	TRUE	MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK2
23 TP_XDPPCH_HOOK3	TRUE	MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK3
23 TP_XDP_PCH_OBSFN_D<0..1>	TRUE	MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>
23 TP_XDP_PCH_HOOK4	TRUE	MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4
23 TP_XDP_PCH_HOOK5	TRUE	MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK5
16 TP_PCH_GPIO64_CLKOUTFLEX0	TRUE	MAKE_BASE=TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
16 TP_PCH_GPIO65_CLKOUTFLEX1	TRUE	MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
16 TP_PCH_GPIO66_CLKOUTFLEX2	TRUE	MAKE_BASE=TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
16 TP_PCH_GPIO67_CLKOUTFLEX3	TRUE	MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3
16 TP_PCIE_CLK100M_PE4N	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N
16 TP_PCIE_CLK100M_PE4P	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P
TP_PCIE_CLK100M_PE5N	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P
TP_PCIE_CLK100M_PE6N	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N
TP_PCIE_CLK100M_PE6P	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P
TP_PCIE_CLK100M_PE7N	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7N
TP_PCIE_CLK100M_PE7P	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7P
TP_PSOC_P1_3	TRUE	MAKE_BASE=TRUE	NC_PSOC_P1_3
TP_SATA_B_D2RN	TRUE	MAKE_BASE=TRUE	NC_SATA_B_D2RN
TP_SATA_B_D2RP	TRUE	MAKE_BASE=TRUE	NC_SATA_B_D2RP
TP_SATA_B_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_SATA_B_R2D_CN
TP_SATA_B_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_SATA_B_R2D_CP
16 TP_SATA_D_D2RN	TRUE	MAKE_BASE=TRUE	NC_SATA_D_D2RN
16 TP_SATA_D_D2RP	TRUE	MAKE_BASE=TRUE	NC_SATA_D_D2RP
16 TP_SATA_D_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_SATA_D_R2D_CN
16 TP_SATA_D_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_SATA_D_R2D_CP
16 TP_SATA_E_D2RN	TRUE	MAKE_BASE=TRUE	NC_SATA_E_D2RN
16 TP_SATA_E_D2RP	TRUE	MAKE_BASE=TRUE	NC_SATA_E_D2RP
16 TP_SATA_E_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_SATA_E_R2D_CN
16 TP_SATA_E_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_SATA_E_R2D_CP
16 TP_SATA_F_D2RN	TRUE	MAKE_BASE=TRUE	NC_SATA_F_D2RN
16 TP_SATA_F_D2RP	TRUE	MAKE_BASE=TRUE	NC_SATA_F_D2RP
16 TP_SATA_F_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_SATA_F_R2D_CN
16 TP_SATA_F_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_SATA_F_R2D_CP
TP_PCH_TP18	TRUE	MAKE_BASE=TRUE	NC_PCH_TP18
TP_PCH_TP17	TRUE	MAKE_BASE=TRUE	NC_PCH_TP17
TP_PCH_TP16	TRUE	MAKE_BASE=TRUE	NC_PCH_TP16
TP_PCH_TP15	TRUE	MAKE_BASE=TRUE	NC_PCH_TP15
TP_PCH_TP14	TRUE	MAKE_BASE=TRUE	NC_PCH_TP14
TP_PCH_TP13	TRUE	MAKE_BASE=TRUE	NC_PCH_TP13
TP_PCH_TP12	TRUE	MAKE_BASE=TRUE	NC_PCH_TP12
TP_PCH_TP10	TRUE	MAKE_BASE=TRUE	NC_PCH_TP10
TP_PCH_TP9	TRUE	MAKE_BASE=TRUE	NC_PCH_TP9
TP_PCH_TP8	TRUE	MAKE_BASE=TRUE	NC_PCH_TP8
TP_PCH_TP7	TRUE	MAKE_BASE=TRUE	NC_PCH_TP7
TP_PCH_TP6	TRUE	MAKE_BASE=TRUE	NC_PCH_TP6
TP_PCH_TP5	TRUE	MAKE_BASE=TRUE	NC_PCH_TP5
TP_PCH_TP4	TRUE	MAKE_BASE=TRUE	NC_PCH_TP4
TP_PCH_TP3	TRUE	MAKE_BASE=TRUE	NC_PCH_TP3
TP_PCH_TP2	TRUE	MAKE_BASE=TRUE	NC_PCH_TP2
TP_PCH_TP1	TRUE	MAKE_BASE=TRUE	NC_PCH_TP1
8 TP_LVDS_IG_B_CLKN	TRUE	MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKN
8 TP_LVDS_IG_B_CLKP	TRUE	MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP
TP_LVDS_IG_BKL_PWM	TRUE	MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM
SMC_BS_ALRT_L	TRUE	MAKE_BASE=TRUE	NC_SMC_BS_ALRT_L

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"G3Hot" (Always-Present) Rails

52 =PPBUS_G3H — PPBUS_G3H (6 51)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
- =PPBUS_S0_LCDBKLT 64
- =PPBUS_S0_VSENSE 44
- =PPVIN_SW_TBTBST 35
- =PPVIN_S5_HS_COMPUTING_ISNS_R 8
- =PPVIN_S5_HS_OTHER_ISNS_R 45

35 6 PPVIN_SW_TBTBST
VOLTAGE=12.8V

8 =PPVIN_S5_HS_COMPUTING_ISNS — PPBUS_S5_HS_COMPUTING_ISNS (6)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
- =PPVIN_S0_CPUIMVP 56 57
- =PPVIN_S3_DDRREG 55
- =PPVIN_S0_CPUVCCIOS0 58
- =PPVIN_S0_VCCSAS0 53
- =PPVIN_S0_CPUAXG 57

45 =PPVIN_S5_HS_OTHER_ISNS — PPBUS_S5_HS_OTHER_ISNS (6)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
- =PPVIN_S5_P5VP3V3 54

51 =PP18V5_DCIN_ISOL — PPDCIN_G3H_ISOL (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR_ISOL 52
- =PPDCIN_S5_VSENSE 44

51 6 =PP18V5_DCIN_CONN — PPDCIN_G3H (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR 52

51 =PP3V42_G3H_REG — PP3V42_G3H (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V3_S5_LPCPLUS 6 42
- =PP3V3_S5_SMC 40 41
- =PP3V42_G3H_HALL 6 51
- =PP3V42_G3H_CHGR 52
- =PP3V42_G3H_PWRCTL 61
- =PP3V42_G3H_SMBUS_SMC_BSA 43
- =PP3V42_G3H_SMCUSBMUX 38
- =PP3V42_G3H_TPAD 6 48
- =PPVIN_S5_SMCVREF 41
- =PPVBAT_G3H_SYSCLK 25
- =PP3V42_G3H_ONEWIRE 6 39

25 =PPVRTC_G3_OUT — PPVRTC_G3H (6)
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE
- =PPVRTC_G3_PCH 16 17 20

5V Rails

54 =PP5V_S5_LDO — PP5V_S5 (6)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S5_P1V5DDRFET 60
- =PP5V_S5_P5VSUSFET 60
- =PP5V_S5_TPAD 48

60 =PP5V_SUS_FET — PP5V_SUS (6)
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_SUS_PCH 22

54 =PP5V_S3_REG — PP5V_S3 (6)
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_AUDIO_AMP 50
- =PP5V_S3_DDRREG 55
- =PP5V_S3_MEMRESET 26
- =PP5V_S3_P5VS0FET 60
- =PP5V_S3_RTUSB 38
- =PP5V_S3_LIO_CONN 6 51

60 =PP5V_S0_FET — PP5V_S0 (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_BKL 64
- =PP5V_S0_CPUIMVP 56
- =PP5V_S0_CPUVCCIOS0 58
- =PP5V_S0_FAN 6 47
- =PP5V_S0_LPCPLUS 6 42
- =PP5V_S0_VCCSA 53
- =PP5V_S0_PCH 22 25
- =PP5V_S0_VMON 61
- =PP5V_S0_KBDLED 48

3.3V Rails

54 =PP3V3_S5_REG — PP3V3_S5 (6 71)
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
- =PP3V3_S5_XDP 23
- =PP3V3_S0_P3V3S0FET 60
- =PP3V3_S3_P3V3S3FET 60
- =PP3V3_S5_CPU_VCCDDR 26
- =PP3V3_S5_LCD 62
- =PP3V3_S5_PCH 17
- =PP3V3_S5_PCHPWRGD 25
- =PP3V3_S5_SMCBATLOW 41
- =PP3V3_S5_PCH_VCCDSW 20 22
- =PP3V3_S5_SYSCLK 25
- =PP3V3_S5_VMON 61
- =PP3V3_S5_PWRCTL 61
- =PP3V3_S5_PCH_GPIO 19
- =PP3V3_S5_P3V3SUSFET 60
- =PP3V3_S4_P3V3S4FET 60
- =PP3V3_S4_TBTAPWRSW 63

60 =PP3V3_S4_FET — PP3V3_S4 (6)
MIN_LINE_WIDTH=0.60MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S4_SMC 41
- =PP3V3_S4_TPAD 48
- =PP3V3_S4_BT 36

60 =PP3V3_SUS_FET — PP3V3_SUS (6)
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_SUS_ROM 49
- =PP3V3_SUS_PCH_VCCSUS 20 22
- =PP3V3_SUS_PCH_GPIO 16 17 18 19
- =PP3V3_SUS_PCH 22
- =PP3V3_SUS_PWRCTL 61
- =PP3V3_SUS_P1V05SUSLDO 59
- =PP3V3_SUS_SMC 41
- =PP3V3_SUS_PCH_VCC_SPI 20 22
- =PP3V3_SUS_PCH_VCCSUS_USB 20 22

=PP3V3_S4_TBTAPWR — PP3V3_SW_TBTAPWR (63)
MIN_LINE_WIDTH=0.38 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20 MM MAKE_BASE=TRUE
- =PP3V3_S4_TBT 33 34 35

60 =PP3V3_S3_FET — PP3V3_S3 (6)
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S3_BT 36
- =PP3V3_S3_MEMRESET 26
- =PP3V3_S3_SMBUS_SMC_A_S3 43
- =PP3V3_S3_SMBUS_SMC_MGMT 43
- =PP3V3_S3_USB_HUB 8 24
- =PP3V3_S3_USB_RESET 24
- =PP3V3_S3_VREFMRGN 31
- =PP3V3_S3_WLAN 36
- =PP3V3_S3_WLANISNS 45
- =PP3V3_S3_PCH_GPIO 18 25
- =PP3V3_S3_USBMUX 24
- =PP3V3_S3_1V5S3ISNS 45
- =PP3V3_S3_DBGLEDS 51

60 =PP3V3_S0_FET — PP3V3_S0 (6 71)
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S0_PCH_VCC3_3_CLK 22
- =PP3V3_S0_CPUVCCIOISNS 44
- =PP3V3_S0_AUDIO 6 39
- =PP3V3_S0_BKL_VDDIO 64
- =PP3V3_S0_HS_COMPUTING_ISNS 45
- =PP3V3_S0_CPUTHMSNS 46
- =PP3V3_S0_CPU_VCCIO_SEL 12
- =PP3V3_S0_DP_DDC 8
- =PP3V3_S0_FAN 47
- =PP3V3_S0_P3V3TBTFET 35
- =PP3V3_S0_P1V8S0 59
- =PP3V3_S0_PCH 16 22
- =PP3V3_S0_PCH_GPIO 16 17 18 19 25 35
- =PP3V3_S0_SATAMUX 37
- =PP3V3_S0_PCH_VCC3_3 20 22
- =PP3V3_S0_HS_OTHER_ISNS 45
- =PP3V3_S0_PCH_VCCADAC 22
- =PP3V3_S0_PWRCTL 61
- =PP3V3_S0_RSTBUF 25
- =PP3V3_S0_SB_PM 25
- =PP3V3_S0_SMBUS_PCH 43
- =PP3V3_S0_SMBUS_SMC_0_S0 43
- =PP3V3_S0_SMBUS_SMC_B_S0 43
- =PP3V3_S0_SMC 41
- =PP3V3_S0_SSD 37
- =PP3V3_S0_HDDISNS 45
- =PP3V3_S0_VMON 61
- =PP3V3_S0_P1V5S0 59
- =PP3V3_S0_TBTPWRCTL 35
- =PP3V3_S0_3V3S0ISNS 44
- =PP3V3_S0_P1V05S0LDO 59
- =PP3V3_S0_IMVPISNS 44
- =PP3V3_S0_XDP 23
- =PP3V3_S0_BKLTISNS 45
- =PP3V3_S0_SYSCLKGEN 25
- =PP3V3_S0_SAISNS 44
- =PP3V3_S0_PCH_STRAPS 19

1.8V/1.5V/1.2V/1.05V Rails

59 =PP1V8_S0_REG — PP1V8_S0 (6)
2A max supply
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S0_CPU_VCCPLL 14
- =PP1V8_S0_PCH_VCC_DFTERM 19 20 22
- =PP1V8_S0_P1V05S0LDO 59
- =PP1V8R1V5_S0_PCH_VCCVRM 20
- =PPVDDIO_S0_SBCLK 25
- =PP1V8_S0_P1V5S0 59

55 =PPDDR_S3_REG — PP1V5_S3 (6 66)
MIN_LINE_WIDTH=0.8 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_MEMRESET 26
- =PP1V5_S3_MEM_A 27 28 32
- =PP1V5_S3_MEM_B 29 30 32
- =PP1V5_S3_P1V5S3RS0_FET 60
- =PPVIN_S0_DDRREG_LDO 55
- =PPDDR_S3_MEMVREF 31

60 =PP1V5_S3RS0_FET — PP1V5_S3RS0 (6 66)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_CPU_VCCDDR 10 12 15 26
- =PP1V5_S3RS0_VMON 61

59 =PP1V5_S0_REG — PP1V5_S0 (6)
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP3V3R1V5_S0_AUDIO 6 39
- =PP3V3R1V5_S0_PCH_VCCSUSHDA 20 22 25

55 31 =PPVTT_S3_DDR_BUF — PPVTTDDR_S3 (6)
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

55 =PPVTT_S0_DDR_LDO — PP0V75_S0_DDRVTT (6)
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
- =PP0V75_S0_MEM_VTT_A 32
- =PP0V75_S0_MEM_VTT_B 32
- =PPVTT_S0_VTTCLAMP 26

53 =PPVCCSA_S0_REG — PPVCCSA_S0_CPU (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PPVCCSA_S0_CPU 12 15
- =PPVCCSA_S0_VSENSE 44

59 =PP1V05_SUS_LDO — PP1V05_SUS (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_SUS_PCH_JTAG 23

58 =PPCPUVCCIO_S0_REG — PP1V05_S0 (6)
? mA
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0_CPU_VCCIO 9 10 12 14
- =PP1V05_S0_PCH 16 22
- =PP1V05_S0_PCH_VCCIO 20 22
- =PP1V05_S0_PCH_VCCIO_PCIE 17
- =PP1V05_S0_PCH_VCCIO_SATA 16 22
- =PP1V05_S0_PCH_VCCASW 20 22
- =PP1V05_S0_PCH_VCC_CORE 20 22
- =PP1V05_S0_VMON 61
- =PPVCCIO_S0_CPUIMVP 56
- =PP1V05_S0_PCH_VCCDIFFCLK 16 20 22
- =PP1V05_S0_PCH_VCCSSC 20 22
- =PP1V05_S0_PCH_V_PROC_IO 20 22
- =PP1V05_S0_PCH_VCC_DMI 20 22
- =PPVCCIO_S0_XDP 23
- =PPVCCIO_S0_SMC 41
- =PP1V05_S0_P1V05TBTFET 35

TBT Rails (off when no cable)

35 =PP15V_TBT_REG — PP15V_TBT (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.8V
MAKE_BASE=TRUE
- =PPHV_SW_TBTAPWRSW 63

35 =PP3V3_TBTLC_FET — PP3V3_TBTLC (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PPVDDIO_TBT_CLK 25
- =PP3V3_TBTLC_RTR 33 34 35
- =PP3V3_TBT_PCH_GPIO 19

35 =PP1V05_TBTLC_FET — PP1V05_TBTLC (6 35)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_TBTLC_RTR 34

35 =PP1V05_TBTCIO_FET — PP1V05_TBTCIO (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_TBTCIO_RTR 34

1V05 S0 LDO

59 =PP1V05_S0_LDO — PP1V05_S0_PCH_VCCADPLL (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0_PCH_VCCADPLL 22

Chipset "VCore" Rails

57 =PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU 9 12 14
- =PPCPUVCORE_S0_VSENSE 44

57 =PPVCORE_S0_AXG_REG — PPVCORE_S0_AXG (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU_VCCAXG 9 12 15
- =PPGFXVCORE_S0_VSENSE 44

15 12 =PP1V5_S3_CPU_VCCDQ — PP1V5_S3_CPU_VCCDQ (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

14 12 =PP1V05_S0_CPU_VCCPQE — PP1V05_S0_CPU_VCCPQE (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

14 12 =PP1V8_S0_CPU_VCCPLL_R — PP1V8_S0_CPU_VCCPLL_R (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

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PAGE TITLE
Power Aliases

Apple Inc.

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REVISION 2.7.0
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CPU Heat Sink Mounting Bosses

Z0913 STDOFF-4.50D1.8H-SM
Z0910 STDOFF-4.50D1.8H-SM
Z0911 STDOFF-4.50D1.8H-SM
Z0912 STDOFF-4.50D1.8H-SM
4x 860-1327

Fan Boss

Z0905 STDOFF-4.50D1.8H-SM
860-1327

X21 Boss

Z0914 STDOFF-4.50D1.9H-SM
860-1327

SSD Boss

Z0915 STDOFF-4.50D1.9H-SM
860-1327

EMI I/O Pogo Pins

DisplayPort Pogo

CRITICAL
ZS0905
POGO-2.00D-3.6H-K86-K87
870-1938

USB/SD Card Pogo

CRITICAL
ZS0907
POGO-2.00D-2.95H-K86-K87
870-1940

Can Slots

SL0901 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	SL0902 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	2x MDP connector
SL0903 TH-NSP, SL-1.1X0.45-1.4x0.75, 998-3975	SL0904 TH-NSP, SL-1.1X0.45-1.4x0.75, 998-3975	2x USB connector
SL0905 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	SL0906 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	2x TBT pin diodes
SL0907 TH-NSP, SL-1.1X0.45-1.4x0.75, 998-3975	SL0908 TH-NSP, SL-1.1X0.45-1.4x0.75, 998-3975	2x TBT chip
SL0909 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	SL0910 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	2x CPU Vcore

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

CPU signals

26 MEMVTT_EN (MAKE_BASE=TRUE) — =DDRVTT_EN 26 55

68 33 DP_TBTSNK0_AUXCH_C_P (MAKE_BASE=TRUE)	DPA_IG_AUX_CH_P	17
68 33 DP_TBTSNK0_AUXCH_C_N (MAKE_BASE=TRUE)	DPA_IG_AUX_CH_N	17
16 PCIE_CLK100M_ENET_N (TRUE)	NC_PCIE_CLK100M_ENETN (MAKE_BASE=TRUE)	
16 PCIE_CLK100M_ENET_P (TRUE)	NC_PCIE_CLK100M_ENETP (MAKE_BASE=TRUE)	
16 PCIE_EXCARD_D2R_N (TRUE)	NC_PCIE_EXCARD_D2RN (MAKE_BASE=TRUE)	
16 PCIE_EXCARD_D2R_P (TRUE)	NC_PCIE_EXCARD_D2RP (MAKE_BASE=TRUE)	
16 PCIE_EXCARD_R2D_C_N (TRUE)	NC_PCIE_EXCARD_R2D_CN (MAKE_BASE=TRUE)	
16 PCIE_EXCARD_R2D_C_P (TRUE)	NC_PCIE_EXCARD_R2D_CP (MAKE_BASE=TRUE)	
16 PCIE_CLK100M_EXCARD_N (TRUE)	NC_PCIE_CLK100M_EXCARDN (MAKE_BASE=TRUE)	
16 PCIE_CLK100M_EXCARD_P (TRUE)	NC_PCIE_CLK100M_EXCARDP (MAKE_BASE=TRUE)	
68 16 PEG_CLK100M_P (MAKE_BASE=TRUE)	NC_PEG_CLK100MP (MAKE_BASE=TRUE)	
68 16 PEG_CLK100M_N (MAKE_BASE=TRUE)	NC_PEG_CLK100MN (MAKE_BASE=TRUE)	
16 TP_PCH_CLKOUT_DPN (MAKE_BASE=TRUE)	DPLL_REF_CLK_N	DPLL_REF_CLKN 10 65
16 TP_PCH_CLKOUT_DPP (MAKE_BASE=TRUE)	DPLL_REF_CLK_P	DPLL_REF_CLKP 10 65
MEM_A_CLK_P<1>	TP_MEM_A_CLKP<1> (MAKE_BASE=TRUE)	
66 11 MEM_A_CLK_N<1> (MAKE_BASE=TRUE)	TP_MEM_A_CLKN<1> (MAKE_BASE=TRUE)	
66 11 MEM_B_CLK_P<1> (MAKE_BASE=TRUE)	TP_MEM_B_CLKP<1> (MAKE_BASE=TRUE)	
66 11 MEM_B_CLK_N<1> (MAKE_BASE=TRUE)	TP_MEM_B_CLKN<1> (MAKE_BASE=TRUE)	
18 USB_EXTC_P (TRUE)	NC_USB_EXTCP (MAKE_BASE=TRUE)	
18 USB_EXTC_N (TRUE)	NC_USB_EXTCN (MAKE_BASE=TRUE)	
18 USB3_EXTC_RX_P (TRUE)	NC_USB3_EXTC_RXP (MAKE_BASE=TRUE)	
18 USB3_EXTC_RX_N (TRUE)	NC_USB3_EXTC_RXN (MAKE_BASE=TRUE)	
18 USB3_EXTC_TX_P (TRUE)	NC_USB3_EXTC_TXP (MAKE_BASE=TRUE)	
18 USB3_EXTC_TX_N (TRUE)	NC_USB3_EXTC_TXN (MAKE_BASE=TRUE)	
18 USB3_EXTD_RX_P (TRUE)	NC_USB3_EXTD_RXP (MAKE_BASE=TRUE)	
18 USB3_EXTD_RX_N (TRUE)	NC_USB3_EXTD_RXN (MAKE_BASE=TRUE)	
18 USB3_EXTD_TX_P (TRUE)	NC_USB3_EXTD_TXP (MAKE_BASE=TRUE)	
18 USB3_EXTD_TX_N (TRUE)	NC_USB3_EXTD_TXN (MAKE_BASE=TRUE)	
18 USB_EXTD_EHCI_P (TRUE)	NC_USB_EXTD_EHCIP (MAKE_BASE=TRUE)	
18 USB_EXTD_EHCI_N (TRUE)	NC_USB_EXTD_EHCIN (MAKE_BASE=TRUE)	
TBT_B_R2D_C_P<0> (TRUE)	NC_TBT_B_R2D_CP<0> (MAKE_BASE=TRUE)	
69 33 TBT_B_R2D_C_N<0> (TRUE)	NC_TBT_B_R2D_CN<0> (MAKE_BASE=TRUE)	
69 33 TBT_B_R2D_C_P<1> (TRUE)	NC_TBT_B_R2D_CP<1> (MAKE_BASE=TRUE)	
69 33 TBT_B_R2D_C_N<1> (TRUE)	NC_TBT_B_R2D_CN<1> (MAKE_BASE=TRUE)	
69 33 TBT_B_D2R_P<0> (TRUE)	NC_TBT_B_D2RP<0> (MAKE_BASE=TRUE)	
69 33 TBT_B_D2R_N<0> (TRUE)	NC_TBT_B_D2RN<0> (MAKE_BASE=TRUE)	
69 33 TBT_B_D2R_P<1> (TRUE)	NC_TBT_B_D2RP<1> (MAKE_BASE=TRUE)	
69 33 TBT_B_D2R_N<1> (TRUE)	NC_TBT_B_D2RN<1> (MAKE_BASE=TRUE)	
33 TBT_B_LSTX (TRUE)	NC_TBT_B_LSTX (MAKE_BASE=TRUE)	
69 33 DP_TBTPB_ML_C_P<1>	NC_DP_TBTPB_ML_CP<1> (MAKE_BASE=TRUE)	
69 33 DP_TBTPB_ML_C_N<1>	NC_DP_TBTPB_ML_CN<1> (MAKE_BASE=TRUE)	
69 33 DP_TBTPB_ML_C_P<3>	NC_DP_TBTPB_ML_CP<3> (MAKE_BASE=TRUE)	
69 33 DP_TBTPB_ML_C_N<3>	NC_DP_TBTPB_ML_CN<3> (MAKE_BASE=TRUE)	
16 PCIE_CLK100M_FW_N	NC_PCIE_CLK100M_FWN (MAKE_BASE=TRUE)	
16 PCIE_CLK100M_FW_P	NC_PCIE_CLK100M_FWP (MAKE_BASE=TRUE)	
9 =PEG_D2R_P<1..0>	PCIE_SSD_D2R_P<1..0> (MAKE_BASE=TRUE)	6 37 65
9 =PEG_D2R_N<1..0>	PCIE_SSD_D2R_N<1..0> (MAKE_BASE=TRUE)	6 37 65
9 =PEG_R2D_C_P<1..0>	PCIE_SSD_R2D_C_P<1..0> (MAKE_BASE=TRUE)	37 65
9 =PEG_R2D_C_N<1..0>	PCIE_SSD_R2D_C_N<1..0> (MAKE_BASE=TRUE)	37 65
16 PCIE_ENET_D2R_N (TRUE)	NC_PCIE_ENET_D2RN (MAKE_BASE=TRUE)	
16 PCIE_ENET_D2R_P (TRUE)	NC_PCIE_ENET_D2RP (MAKE_BASE=TRUE)	
16 PCIE_ENET_R2D_C_N (TRUE)	NC_PCIE_ENET_R2D_CN (MAKE_BASE=TRUE)	
16 PCIE_ENET_R2D_C_P (TRUE)	NC_PCIE_ENET_R2D_CP (MAKE_BASE=TRUE)	
16 PCIE_FW_D2R_N (TRUE)	NC_PCIE_FW_D2RN (MAKE_BASE=TRUE)	
16 PCIE_FW_D2R_P (TRUE)	NC_PCIE_FW_D2RP (MAKE_BASE=TRUE)	
16 PCIE_FW_R2D_C_N (TRUE)	NC_PCIE_FW_R2D_CN (MAKE_BASE=TRUE)	
16 PCIE_FW_R2D_C_P (TRUE)	NC_PCIE_FW_R2D_CP (MAKE_BASE=TRUE)	

TBT DP Ports

17 DPB_IG_HPD	DP_TBTSNK1_HPD	33
17 TP_DP_IG_C_MLP<3..0> (MAKE_BASE=TRUE)	DP_TBTSNK1_ML_C_P<3..0> (MAKE_BASE=TRUE)	33 68
17 TP_DP_IG_C_MLN<3..0> (MAKE_BASE=TRUE)	DP_TBTSNK1_ML_C_N<3..0> (MAKE_BASE=TRUE)	33 68
17 DPB_IG_AUX_CH_P (MAKE_BASE=TRUE)	DP_TBTSNK1_AUXCH_C_P (MAKE_BASE=TRUE)	33 68
17 DPB_IG_AUX_CH_N (MAKE_BASE=TRUE)	DP_TBTSNK1_AUXCH_C_N (MAKE_BASE=TRUE)	33 68
17 TP_DP_IG_D_HPD	DP_IG_D_HPD (MAKE_BASE=TRUE)	
69 33 DP_TBTPB_AUXCH_C_P (MAKE_BASE=TRUE)	NC_DP_TBTPB_AUXCH_CP (MAKE_BASE=TRUE)	
69 33 DP_TBTPB_AUXCH_C_N (MAKE_BASE=TRUE)	NC_DP_TBTPB_AUXCH_CN (MAKE_BASE=TRUE)	
17 TP_DP_IG_B_MLP<3..0> (MAKE_BASE=TRUE)	DP_TBTSNK0_ML_C_P<3..0> (MAKE_BASE=TRUE)	33 68
17 TP_DP_IG_B_MLN<3..0> (MAKE_BASE=TRUE)	DP_TBTSNK0_ML_C_N<3..0> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_5_R2D_CP (MAKE_BASE=TRUE)	PCIE_TBT_R2D_C_P<0> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_6_R2D_CP (MAKE_BASE=TRUE)	PCIE_TBT_R2D_C_P<1> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_7_R2D_CP (MAKE_BASE=TRUE)	PCIE_TBT_R2D_C_P<2> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_8_R2D_CP (MAKE_BASE=TRUE)	PCIE_TBT_R2D_C_P<3> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_5_R2D_CN (MAKE_BASE=TRUE)	PCIE_TBT_R2D_C_N<0> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_6_R2D_CN (MAKE_BASE=TRUE)	PCIE_TBT_R2D_C_N<1> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_7_R2D_CN (MAKE_BASE=TRUE)	PCIE_TBT_R2D_C_N<2> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_8_R2D_CN (MAKE_BASE=TRUE)	PCIE_TBT_R2D_C_N<3> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_5_D2RP (MAKE_BASE=TRUE)	PCIE_TBT_D2R_P<0> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_6_D2RP (MAKE_BASE=TRUE)	PCIE_TBT_D2R_P<1> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_7_D2RP (MAKE_BASE=TRUE)	PCIE_TBT_D2R_P<2> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_8_D2RP (MAKE_BASE=TRUE)	PCIE_TBT_D2R_P<3> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_5_D2RN (MAKE_BASE=TRUE)	PCIE_TBT_D2R_N<0> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_6_D2RN (MAKE_BASE=TRUE)	PCIE_TBT_D2R_N<1> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_7_D2RN (MAKE_BASE=TRUE)	PCIE_TBT_D2R_N<2> (MAKE_BASE=TRUE)	33 68
16 NC_PCIE_8_D2RN (MAKE_BASE=TRUE)	PCIE_TBT_D2R_N<3> (MAKE_BASE=TRUE)	33 68

LVDS Aliases

6 TP_LVDS_IG_B_CLKP (MAKE_BASE=TRUE)	LVDS_IG_B_CLK_P
6 TP_LVDS_IG_B_CLKN (MAKE_BASE=TRUE)	LVDS_IG_B_CLK_N
NC_LVDS_IG_B_DATAP<0..3> (MAKE_BASE=TRUE, NO_TEST=TRUE)	LVDS_IG_B_DATA_P<0..3>
NC_LVDS_IG_B_DATAN<0..3> (MAKE_BASE=TRUE, NO_TEST=TRUE)	LVDS_IG_B_DATA_N<0..3>
NC_LVDS_IG_A_DATAP<3> (MAKE_BASE=TRUE, NO_TEST=TRUE)	LVDS_IG_A_DATA_P<3>
NC_LVDS_IG_A_DATAN<3> (MAKE_BASE=TRUE, NO_TEST=TRUE)	LVDS_IG_A_DATA_N<3>
64 LCD_BKLT_PWM (MAKE_BASE=TRUE)	LVDS_IG_BKL_PWM 17
62 LCD_IG_PWR_EN (MAKE_BASE=TRUE)	LVDS_IG_PANEL_PWR 17
64 LCD_BKLT_EN (MAKE_BASE=TRUE)	LVDS_IG_BKL_ON 17

SATA Aliases

Unused SATA ODD Signals

16 IN SATA_ODD_R2D_C_P	NC_SATA_ODD_R2DCP (MAKE_BASE=TRUE, NO_TEST=TRUE)
16 IN SATA_ODD_R2D_C_N	NC_SATA_ODD_R2DCN (MAKE_BASE=TRUE, NO_TEST=TRUE)
16 OUT SATA_ODD_D2R_P	NC_SATA_ODD_D2RP (MAKE_BASE=TRUE, NO_TEST=TRUE)
16 OUT SATA_ODD_D2R_N	NC_SATA_ODD_D2RN (MAKE_BASE=TRUE, NO_TEST=TRUE)

SMC Aliases

Unused SMC Signals

40 IN SMC_SYS_LED	NC_SMC_SYS_LED (MAKE_BASE=TRUE, NO_TEST=TRUE)
40 OUT IR_RX_OUT_RC	NC_IR_RX_OUT_RC (MAKE_BASE=TRUE, NO_TEST=TRUE)

Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE (MAKE_BASE=TRUE)	P1V5S3RS0_RAMP_DONE IN 60
TP_DDRREG_PGOOD (MAKE_BASE=TRUE)	DDRREG_PGOOD IN 55

UNUSED SDCARD USB Aliases

=PP3V3_S3_USB_HUB 24 7

R0901[1] 10K 5% 1/20W MF 201 — R0902[1] 10K 5% 1/20W MF 201

67 24 OUT USB_SDCARD_N
67 24 OUT USB_SDCARD_P

=PP3V3_S0_DP_DDC 8 7

R0920[1] 2.2K 5% 1/20W MF 201 — R0921[1] 2.2K 5% 1/20W MF 201 — R0922[1] 2.2K 5% 1/20W MF 201 NOSTUFF — R0923[1] 2.2K 5% 1/20W MF 201 NOSTUFF

DPB_IG_DDC_CLK 17
DPB_IG_DDC_DATA 17

17 TP_DP_IG_D_CTRL_CLK (MAKE_BASE=TRUE)	DP_IG_D_CTRL_CLK	17
17 TP_DP_IG_D_CTRL_DATA (MAKE_BASE=TRUE)	DP_IG_D_CTRL_DATA	17

R0909[1] 100K 5% 1/20W MF 201

=PP3V3_S0_DP_DDC 8 7

R0924[1] 470K 5% 1/20W MF 201 — R0925[1] 470K 5% 1/20W MF 201

63 DP_TBTSNK0_DDC_CLK (MAKE_BASE=TRUE)	DPA_IG_DDC_CLK	17
63 DP_TBTSNK0_DDC_DATA (MAKE_BASE=TRUE)	DPA_IG_DDC_DATA	17
33 DP_TBTSNK0_HPD (MAKE_BASE=TRUE)	DPA_IG_HPD	17

CRITICAL
R0910 0.01 0.5% 1W MF 0612-1

64 PPBUS_SW_LCDBKLT_PWR (MAKE_BASE=TRUE) — PPBUS_SW_BKL (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.375 MM, VOLTAGE=12.6V, MAKE_BASE=TRUE)
71 45 OUT ISNS_LCDBKLT_P
71 45 OUT ISNS_LCDBKLT_N
=PPBUS_SW_BKL 64

CRITICAL
R0954 0.002 1% MF 1W 0612

7 OUT =PPVIN_S5_HS_COMPUTING_ISNS — =PPVIN_S5_HS_COMPUTING_ISNS_R IN 7
71 45 OUT ISNS_HS_COMPUTING_N
71 45 OUT ISNS_HS_COMPUTING_P

23 19 XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH (MAKE_BASE=TRUE)	ENET_LOW_PWR_PCH	19
23 16 XDP_DC3_PCH_GPIO19_SATARDRVR_EN (MAKE_BASE=TRUE)	SATARDRVR_EN	16

33 TBT_B_CIO_SEL
33 DP_TBTPB_HPD
33 TBT_B_CONFIG2_RC
33 TBT_B_CONFIG1_BUF
33 TBT_B_LSRX

R0916[1] 10K 5% 1/20W MF 201 — R0917[1] 10K 5% 1/20W MF 201 — R0918[1] 10K 5% 1/20W MF 201 — R0919[1] 10K 5% 1/20W MF 201 — R0914[1] 10K 5% 1/20W MF 201

19 MLB_RAMCFG3
19 MLB_RAMCFG2
19 MLB_RAMCFG1
19 MLB_RAMCFG0

RAMCFG3:L R0950[1] 10K 5% 1/20W MF 201 — RAMCFG2:L R0951[1] 10K 5% 1/20W MF 201 — RAMCFG1:L R0952[1] 10K 5% 1/20W MF 201 — RAMCFG0:L R0953[1] 10K 5% 1/20W MF 201

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

PAGE TITLE: Signal Aliases

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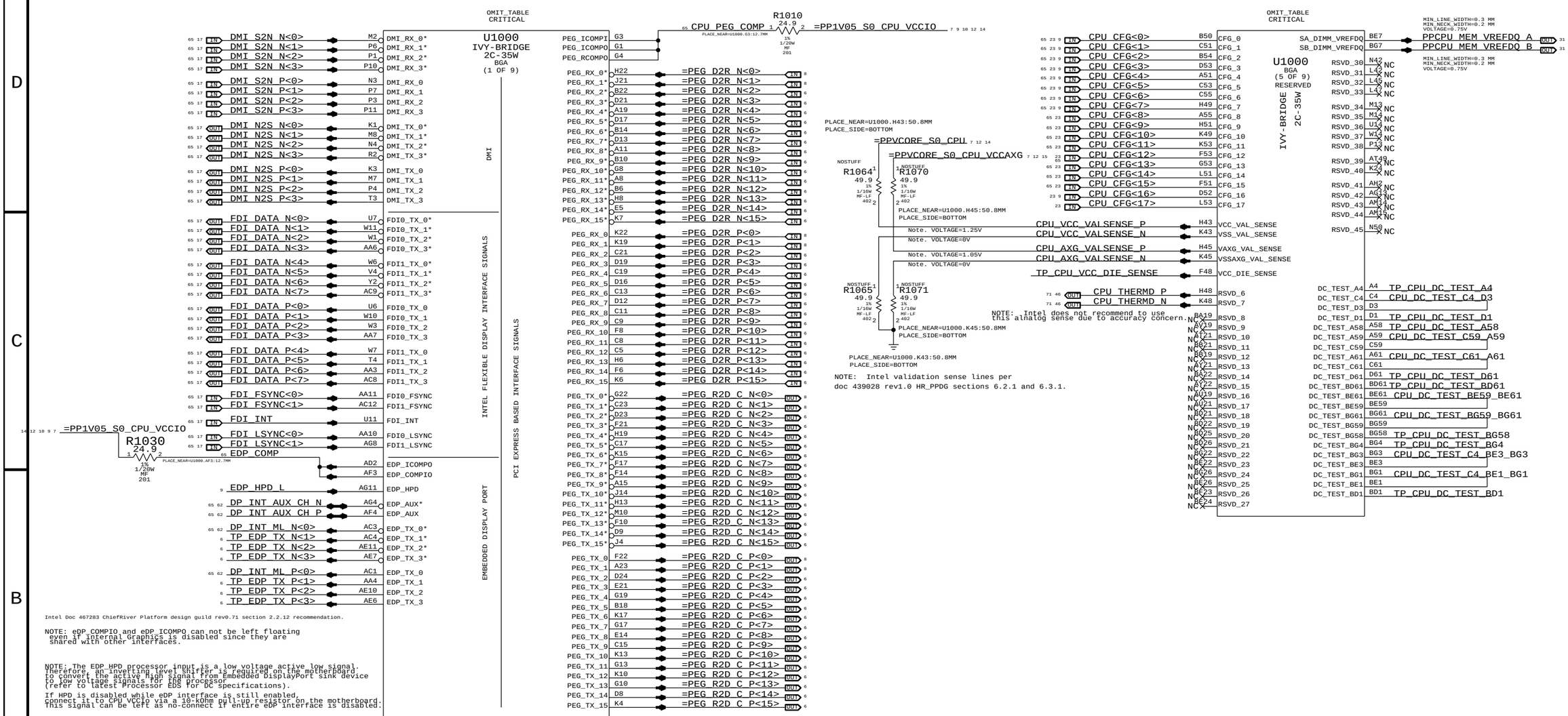
NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.

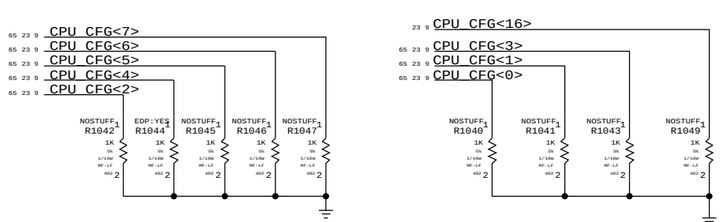


Intel Doc 467283 ChiefRiver Platform design guild rev0.71 section 2.2.12 recommendation.

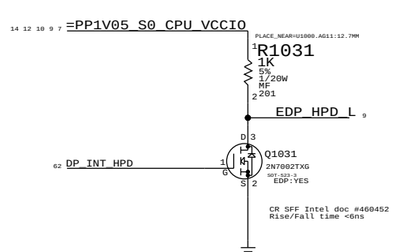
NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU_VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.



These can be Placed close to J2500 and Only for debug access



FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD	00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

SYNC MASTER=J13_MLB SYNC_DATE=10/13/2013

PAGE TITLE

CPU DMI/PEG/FDI/RSVD

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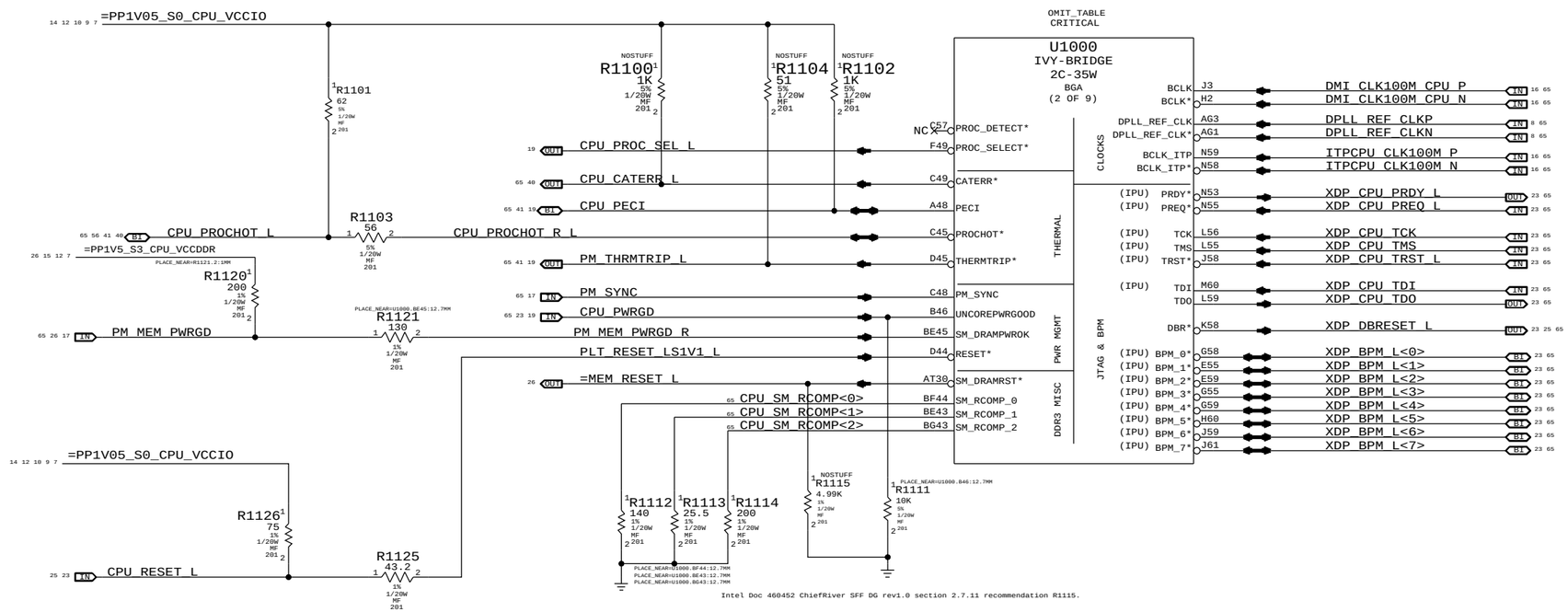

Intel Doc 460452 ChiefRiver SFF DG rev1.0 section 2.7.11 recommendation R1115.

SYNC_MASTER=J13_MLB SYNC_DATE=09/22/2013

PAGE TITLE
CPU CLOCK/MISC/JTAG

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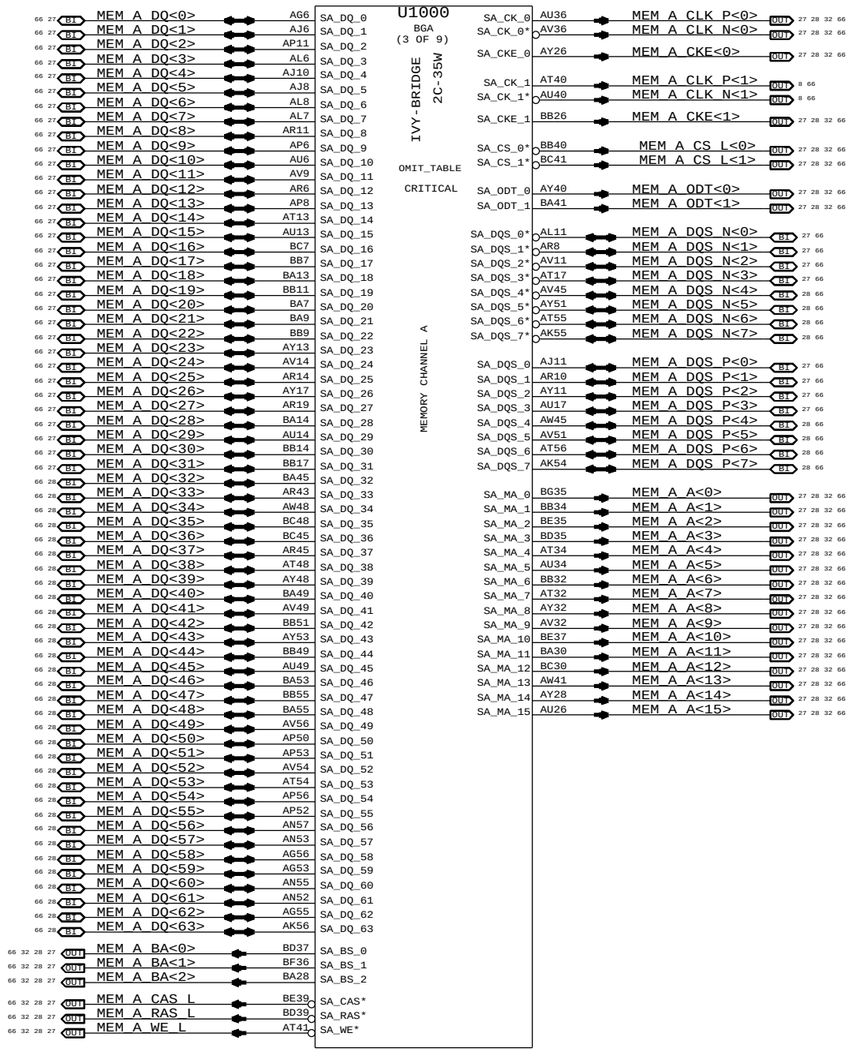

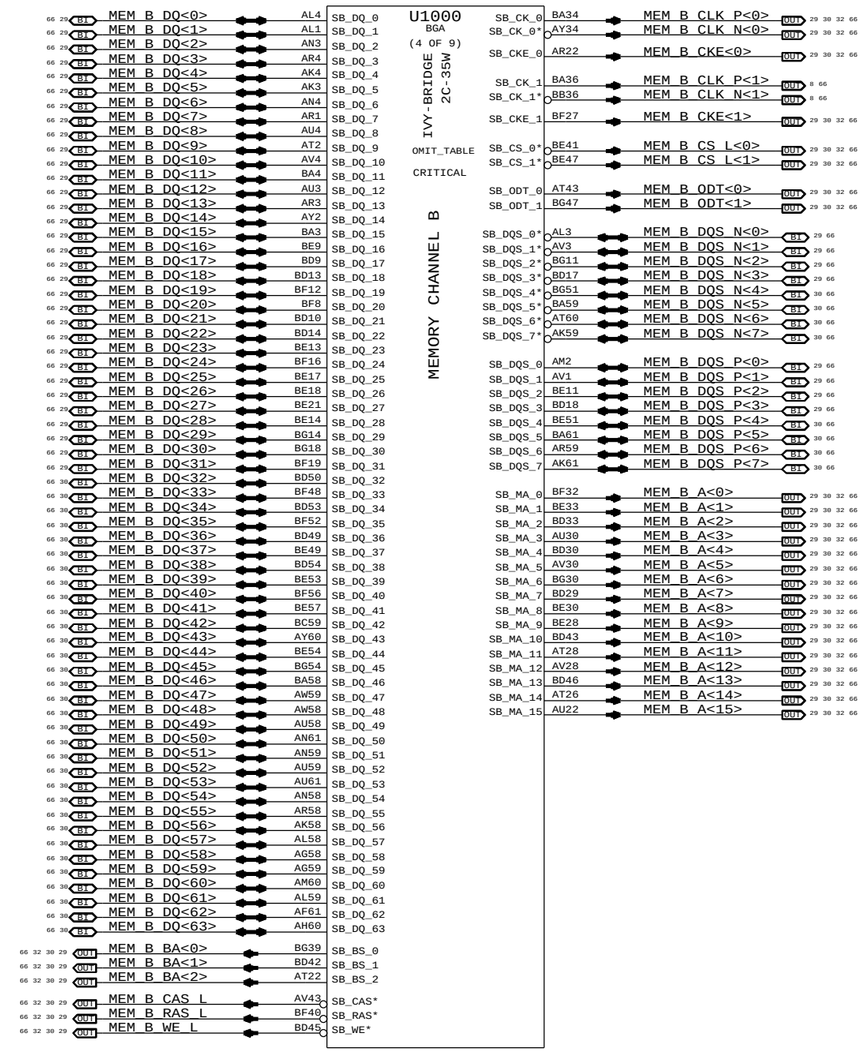

SYNC DATE=12/13/2010

PAGE TITLE
CPU DDR3 INTERFACES

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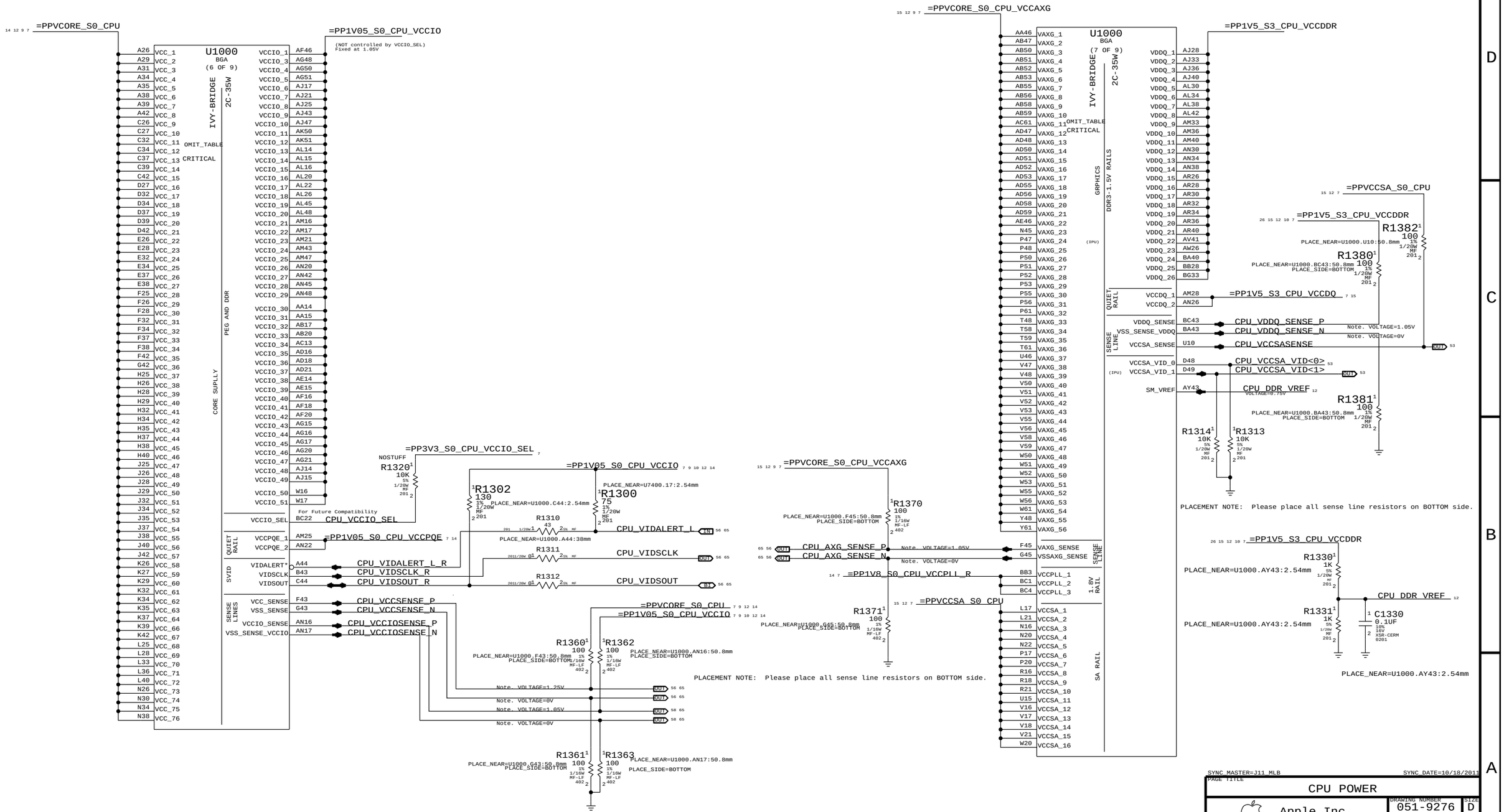

SYNC MASTER=J11_MLB SYNC DATE=10/18/2013

PAGE TITLE: CPU POWER

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DRAWING NUMBER: 051-9276 SIZE: D

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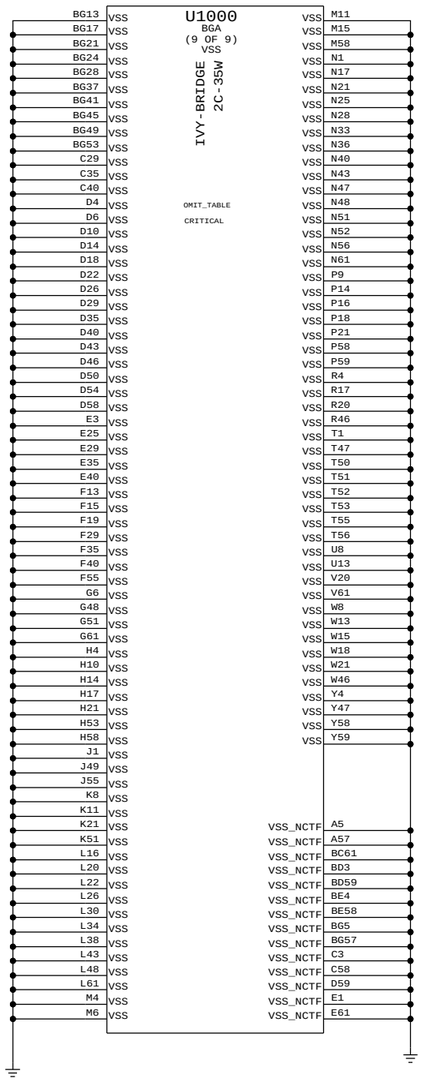

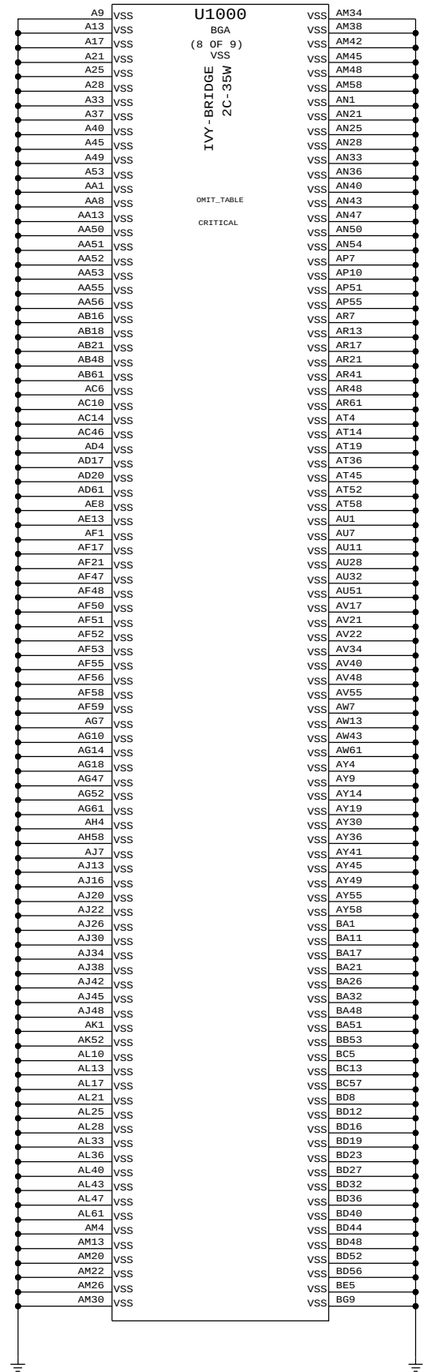

PAGE TITLE

CPU GROUNDS

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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

Processor Load Line : -2.9 mOhms

CPU VCORE DECOUPLING

Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

12 9 7 =PPVCORE_S0_CPU

C1600	C1601	C1602	C1603	C1604	C1605	C1606	C1607	C1608	C1609	C1610	C1611	C1612	C1613	C1614	C1615	C1640	C1641	C1642					
C1616	C1617	C1618	C1619	C1620	C1621	C1622	C1623	C1624	C1625	C1626	C1627	C1628	C1629	C1630	C1631	C1632	C1633	C1634	C1635	C1636	C1637	C1638	C1639

1UF 20% 6.3V X5R 0201 — CRITICAL

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

C1655	C1656	C1657	C1658	C1659	C1660	C1661	C1662	C1663	C1664	C1665	C1666	C1667	C1668	C1669	C1670		

10UF 20% 6.3V CERM-X5R 0402-1 — CRITICAL

PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):

C1680	C1681	C1682	C1683	C1679

270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):

Place on bottom side of U1000

12 10 9 7 =PP1V05_S0_CPU_VCCIO

C1684	C1685	C1686	C1687	C1688	C1689	C1690	C1691	C1692	C1693	C1694	C1695	C1696		
C1697	C1698	C1699	C169A	C169B	C169C	C169D	C169E	C169F	C161A	C161B	C161C	C161D		

1UF 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side

C161E	C161F	C162A	C162B	C162C	C162D	C162E	C167A	C167B	C167C

10UF 20% 6.3V CERM-X5R 0402-1

C167D	C167E	C167G	C167H

270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W 0603 — =PP1V05_S0_CPU_VCCPQE 7 12

C167F 1UF 10V X5R 402 — Note:The smallest 10mOhm available in the library are the 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):
Place near U1000 on top side

7 =PP1V8_S0_CPU_VCCPLL — R1600 0 5% 1/16W MF-LF 402 — =PP1V8_S0_CPU_VCCPLL_R 7 12

C160X 1UF 10V X5R 402 — C160Y 1UF 10V X5R 402 — C160Z 270UF 20% 2V TANT CASE-B2-SM

PLACE_NEAR=U1000.AB2:2.54 mm:NO_VIA

PLACE_NEAR=U1000.BC1:2.54 mm:NO_VIA

CPU VCCPLL Low pass filter

SYNC_MASTER=J13_MLB SYNC_DATE=08/16/2011

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VAXG DECOUPLING

Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

12 9 7 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL: C1700, C1701, C1702, C1703, C1704, C1705, C1706, C1707, C1708, C1709, C1710

1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL: C1711, C1712, C1713, C1714, C1715, C1716

10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL: C1717, C1718, C1719, C1720, C1721, C1722

AXG_ACOUSTICS:NO

22UF 20% 6.3V X5R-CERM1 0603

CRITICAL: C1727, C1728, C1729, C1730, C1731, C1732

AXG_ACOUSTICS:YES

22UF 20% 4V X5R 402

PLACEMENT_NOTE (C1723-C1724):

C1723, C1724, C1725

270UF 20% 2V TANT CASE-B2-SM

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uf, 3x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

12 7 =PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758, C1759, C1760, C1761, C1762

1UF 10% 10V X5R 402

C1763, C1764, C1765, C1766, C1767

10UF 20% 6.3V CERM-X5R 0402-1

C1768

270UF 20% 2V TANT CASE-B2-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

26 12 10 7 =PP1V5_S3_CPU_VCCDDR

Place on bottom side of U1000

C1738, C1739, C1740, C1741, C1742, C1743, C1744, C1745, C1746, C1747

1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748, C1749, C1750, C1751, C1752, C1753, C1754, C1755

10UF 20% 6.3V CERM-X5R 0402-1

C1756

270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702

0.010 1% 1/4W MF 0603

=PP1V5_S3_CPU_VCCDQ 7 12

C1757

1UF 10% 10V X5R 402

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

CPU DECOUPLING-II

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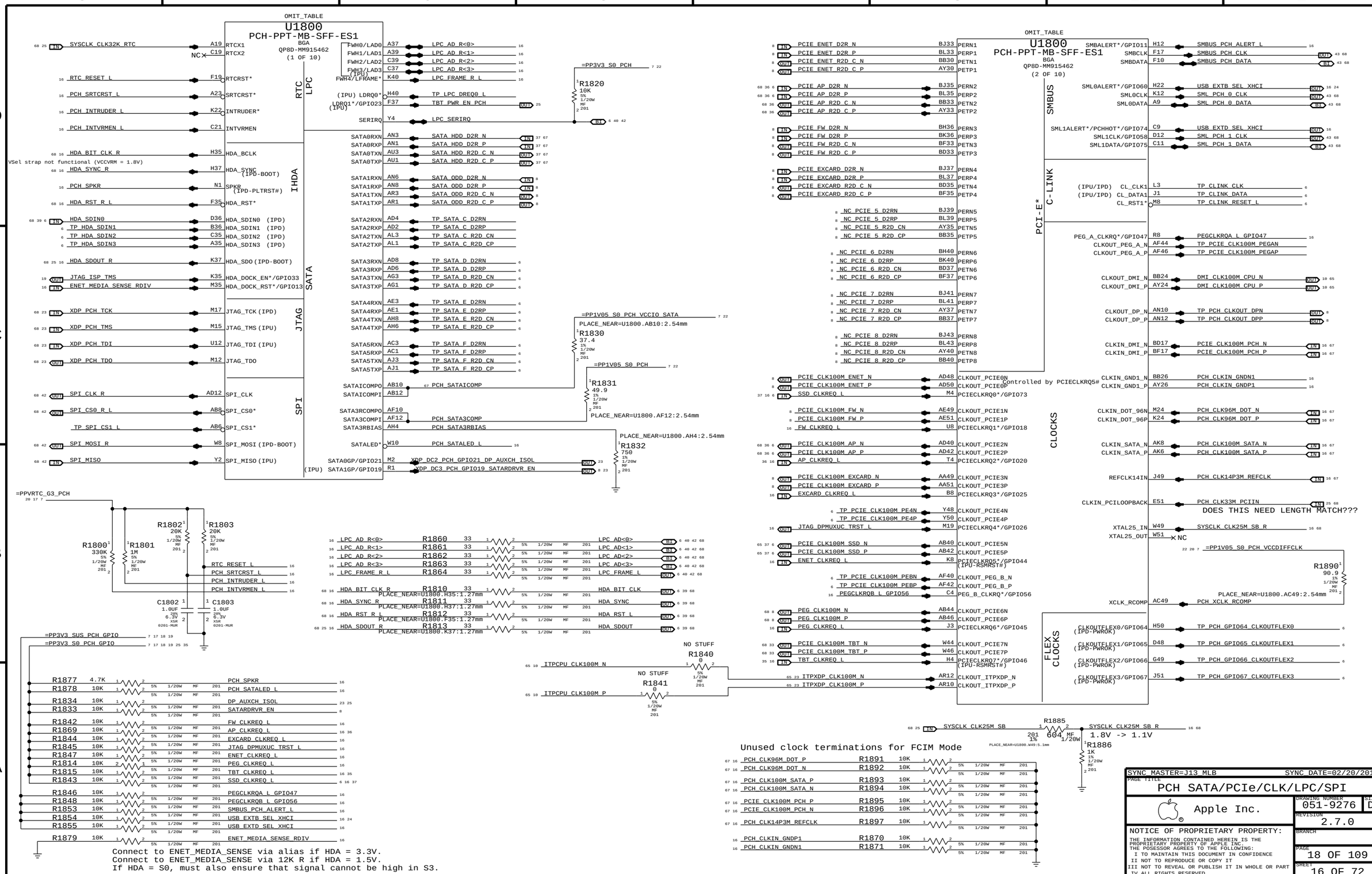
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(1 OF 10)
RTC
LPC
IHDA
SATA
JTAG
SPI
SYSCLK_CLK32K_RTC
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
HDA_BIT_CLK_R
VSel strap not functional (VCCVRM = 1.8V)
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_ISP_TMS
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO
=PP3V3_S0_PCH
R1820
10K
=PP1V05_S0_PCH_VCCIO_SATA
PLACE_NEAR=U1800.AB10:2.54mm
R1830
37.4
=PP1V05_S0_PCH
R1831
49.9
PLACE_NEAR=U1800.AF12:2.54mm
PLACE_NEAR=U1800.AH4:2.54mm
R1832
750
=PPVRTC_G3_PCH
R1800
330K
R1801
1M
R1802
20K
R1803
20K
C1802
1.0UF
6.3V
C1803
1.0UF
6.3V
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
R1877 4.7K PCH_SPKR
R1878 10K PCH_SATALED_L
R1834 10K DP_AUXCH_ISOL
R1833 10K SATARDRVR_EN
R1842 10K FW_CLKREQ_L
R1869 10K AP_CLKREQ_L
R1844 10K EXCARD_CLKREQ_L
R1845 10K JTAG_DPMUXUC_TRST_L
R1847 10K ENET_CLKREQ_L
R1814 10K PEG_CLKREQ_L
R1815 10K TBT_CLKREQ_L
R1843 10K SSD_CLKREQ_L
R1846 10K PEGCLKRQA_L_GPIO47
R1848 10K PEGCLKRQB_L_GPIO56
R1853 10K SMBUS_PCH_ALERT_L
R1854 10K USB_EXTB_SEL_XHCI
R1855 10K USB_EXTD_SEL_XHCI
R1879 10K ENET_MEDIA_SENSE_RDIV
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
R1860 33 LPC_AD<0>
R1861 33 LPC_AD<1>
R1862 33 LPC_AD<2>
R1863 33 LPC_AD<3>
R1864 33 LPC_FRAME_L
R1810 33 HDA_BIT_CLK
R1811 33 HDA_SYNC
R1812 33 HDA_RST_L
R1813 33 HDA_SDOUT
NO STUFF
R1840 0
R1841 0
ITPCPU_CLK100M_N
ITPCPU_CLK100M_P
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(2 OF 10)
SMBUS
C-LINK
PCI-E*
CLOCKS
FLEX CLOCKS
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_FW_D2R_N
PCIE_FW_D2R_P
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
PCIE_EXCARD_D2R_N
PCIE_EXCARD_D2R_P
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P
NC_PCIE_5_D2RN
NC_PCIE_5_D2RP
NC_PCIE_5_R2D_CN
NC_PCIE_5_R2D_CP
NC_PCIE_6_D2RN
NC_PCIE_6_D2RP
NC_PCIE_6_R2D_CN
NC_PCIE_6_R2D_CP
NC_PCIE_7_D2RN
NC_PCIE_7_D2RP
NC_PCIE_7_R2D_CN
NC_PCIE_7_R2D_CP
NC_PCIE_8_D2RN
NC_PCIE_8_D2RP
NC_PCIE_8_R2D_CN
NC_PCIE_8_R2D_CP
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
SSD_CLKREQ_L
PCIE_CLK100M_FW_N
PCIE_CLK100M_FW_P
FW_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
PCIE_CLK100M_EXCARD_N
PCIE_CLK100M_EXCARD_P
EXCARD_CLKREQ_L
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
JTAG_DPMUXUC_TRST_L
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
ENET_CLKREQ_L
TP_PCIE_CLK100M_PEBN
TP_PCIE_CLK100M_PEBP
PEGCLKRQB_L_GPIO56
PEG_CLK100M_N
PEG_CLK100M_P
PEG_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
TBT_CLKREQ_L
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
controlled by PCIECLKRQ5#
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SMBUS_PCH_ALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
USB_EXTB_SEL_XHCI
SML_PCH_0_CLK
SML_PCH_0_DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
USB_EXTD_SEL_XHCI
SML_PCH_1_CLK
SML_PCH_1_DATA
(IPU/IPD) CL_CLK1
(IPU/IPD) CL_DATA1
CL_RST1*
TP_CLINK_CLK
TP_CLINK_DATA
TP_CLINK_RESET_L
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
PEGCLKRQA_L_GPIO47
TP_PCIE_CLK100M_PEGAN
TP_PCIE_CLK100M_PEGAP
CLKOUT_DMI_N
CLKOUT_DMI_P
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
CLKOUT_DP_N
CLKOUT_DP_P
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
CLKIN_DMI_N
CLKIN_DMI_P
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
CLKIN_GND1_N
CLKIN_GND1_P
PCH_CLKIN_GNDN1
PCH_CLKIN_GNDP1
CLKIN_DOT_96N
CLKIN_DOT_96P
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
CLKIN_SATA_N
CLKIN_SATA_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
REFCLK14IN
PCH_CLK14P3M_REFCLK
CLKIN_PCILOOPBACK
PCH_CLK33M_PCIIN
DOES THIS NEED LENGTH MATCH???
XTAL25_IN
XTAL25_OUT
SYSCLK_CLK25M_SB_R
=PP1V05_S0_PCH_VCCDIFFCLK
R1890
90.9
PLACE_NEAR=U1800.AC49:2.54mm
XCLK_RCOMP
PCH_XCLK_RCOMP
CLKOUTFLEX0/GPIO64 (IPD-PWROK)
CLKOUTFLEX1/GPIO65 (IPD-PWROK)
CLKOUTFLEX2/GPIO66 (IPD-PWROK)
CLKOUTFLEX3/GPIO67 (IPD-PWROK)
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
SYSCLK_CLK25M_SB
R1885
604
1.8V -> 1.1V
R1886
1K
Unused clock terminations for FCIM Mode
R1891 10K PCH_CLK96M_DOT_P
R1892 10K PCH_CLK96M_DOT_N
R1893 10K PCH_CLK100M_SATA_P
R1894 10K PCH_CLK100M_SATA_N
R1895 10K PCIE_CLK100M_PCH_P
R1896 10K PCIE_CLK100M_PCH_N
R1897 10K PCH_CLK14P3M_REFCLK
R1870 10K PCH_CLKIN_GNDP1
R1871 10K PCH_CLKIN_GNDN1
SYNC_MASTER=J13_MLB
SYNC_DATE=02/20/2012
PAGE TITLE
PCH SATA/PCIe/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
BRANCH
PAGE 18 OF 109
SHEET 16 OF 72
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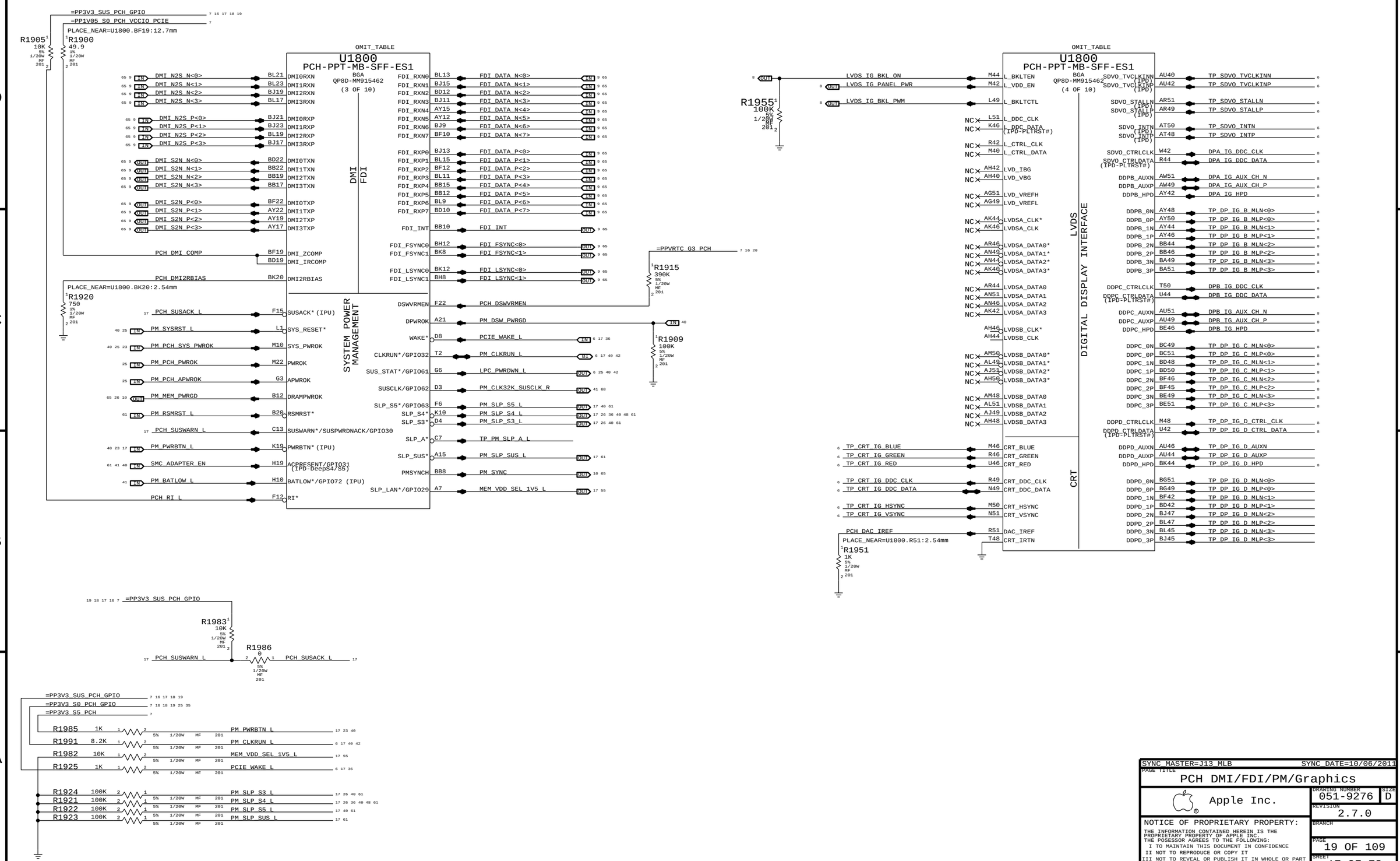

SYNC_MASTER=J13_MLB	SYNC_DATE=10/06/2011
PAGE TITLE: PCH DMI/FDI/PM/Graphics	
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	REVISION: 2.7.0
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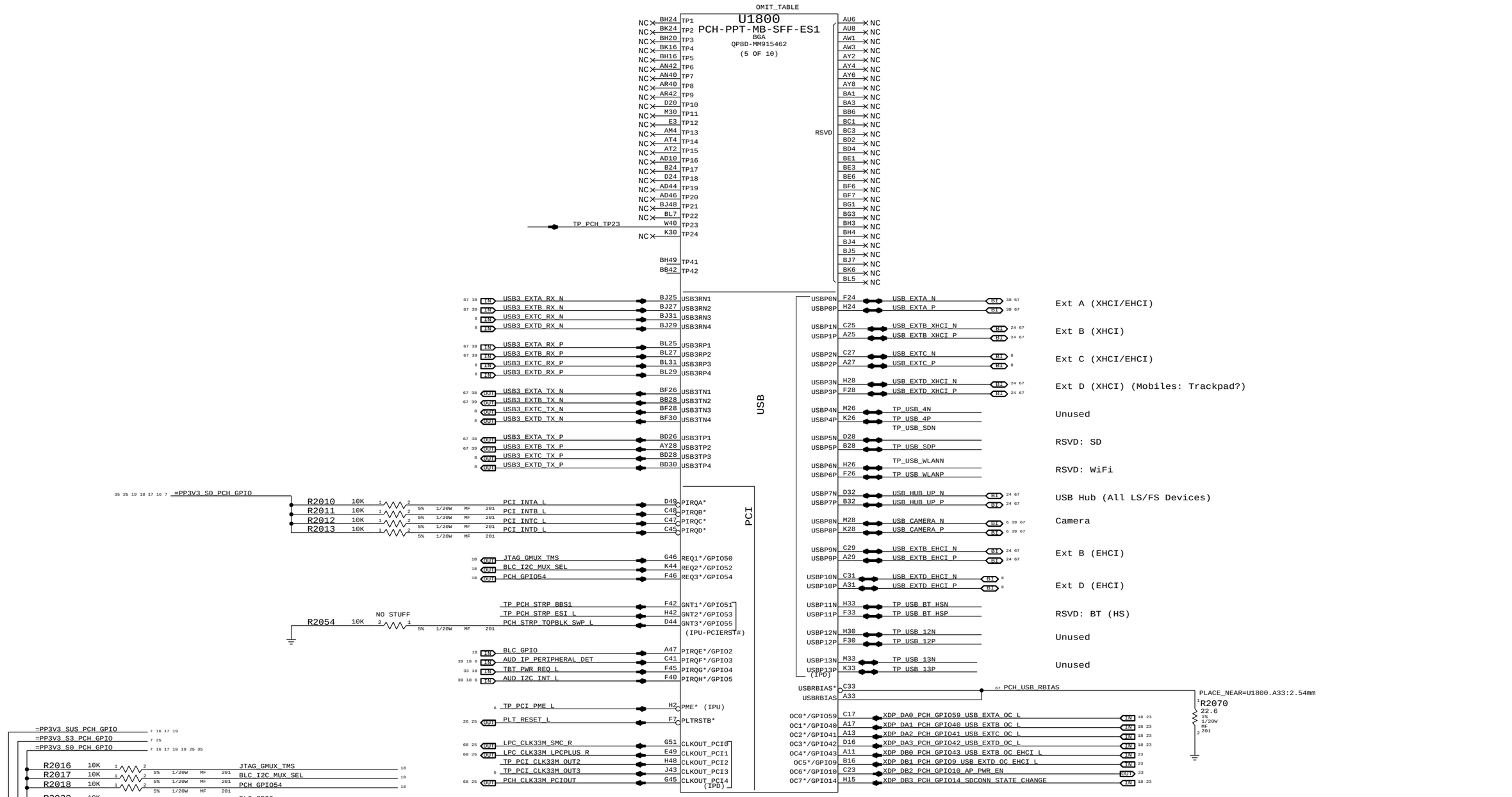
	SHEET: 17 OF 72



SYNC_MASTER=J13_MLB	SYNC_DATE=09/22/2011
PAGE TITLE	PCH PCI/USB/TP/RSVD
Apple Inc.	DRAWING NUMBER 051-9276 SIZE D
	REVISION 2.7.0
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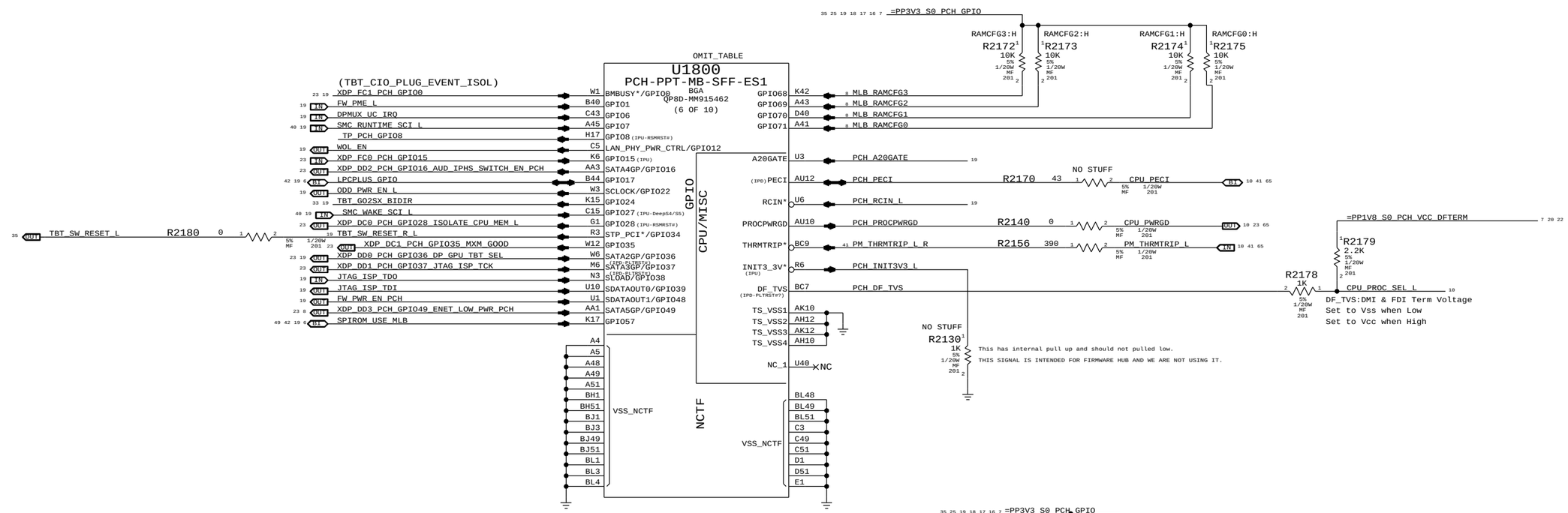
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.



SYNC_MASTER=J13_MLB	SYNC_DATE=02/23/2012
PAGE TITLE	PCH GPIO/MISC/NCTF
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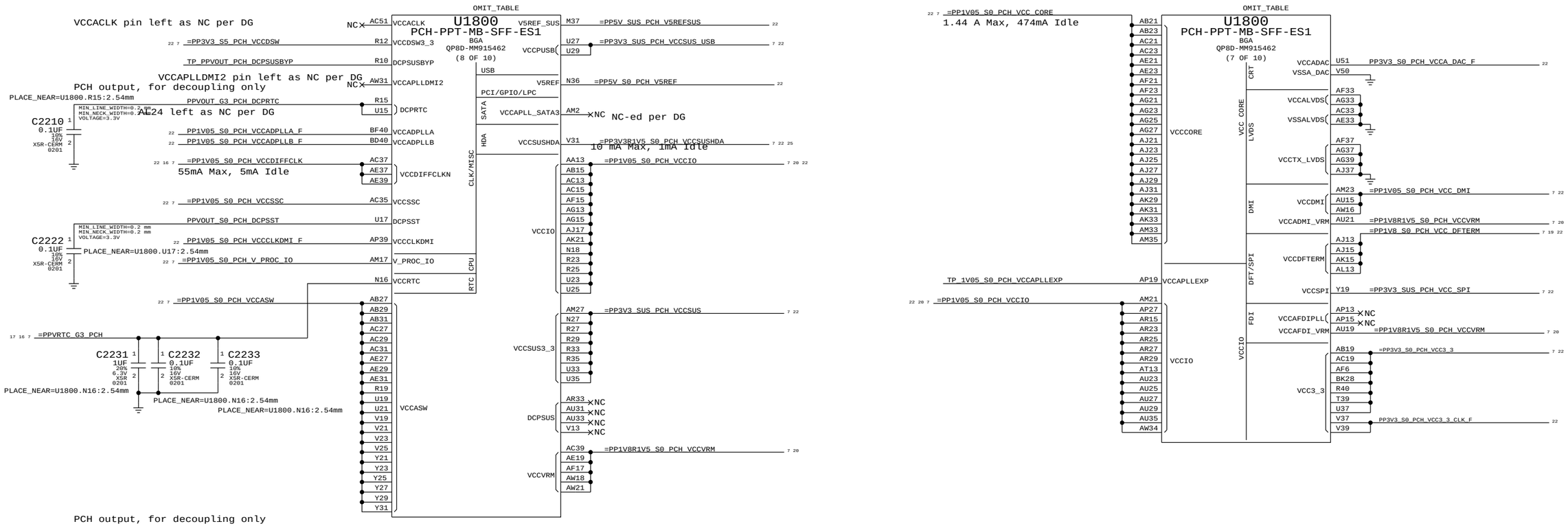

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PAGE TITLE

PCH POWER

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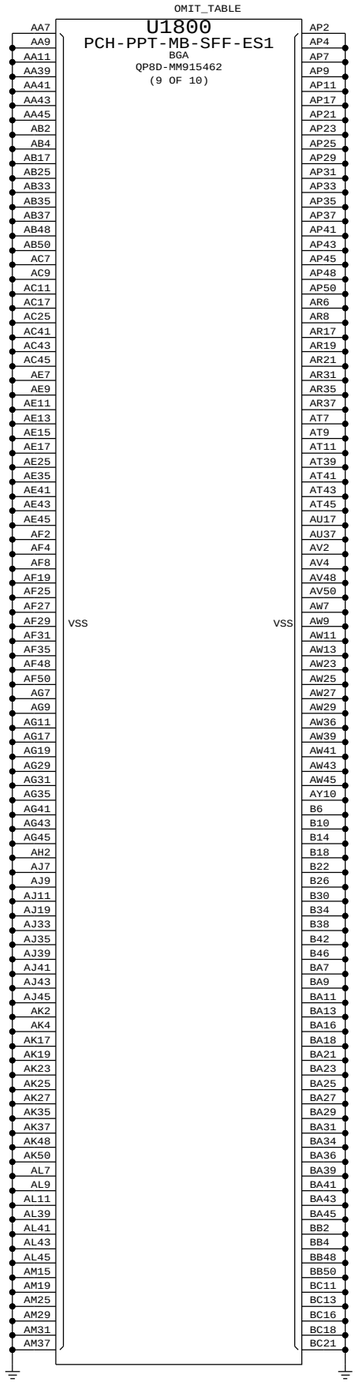

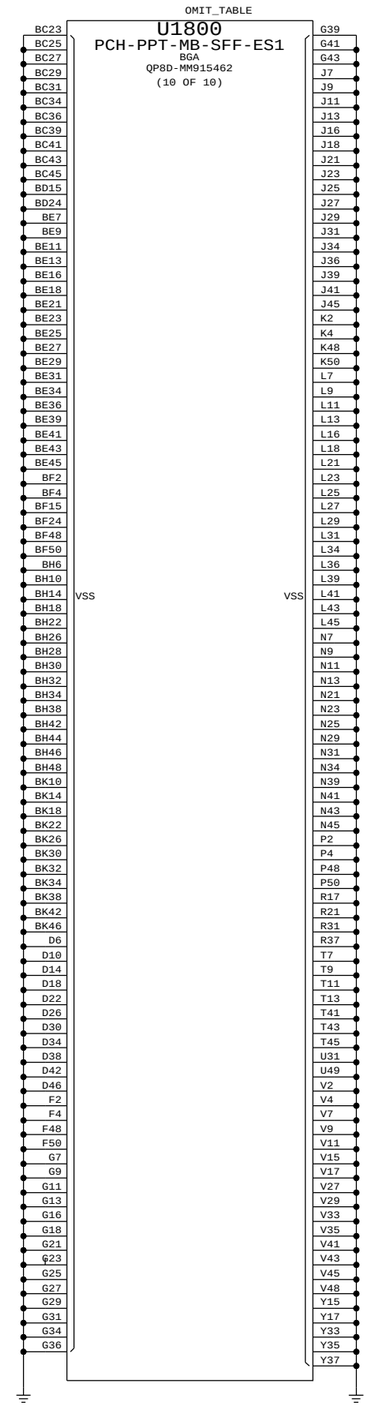

SYNC_MASTER=J13_MLB SYNC_DATE=08/12/2011

PAGE TITLE

PCH GROUNDS

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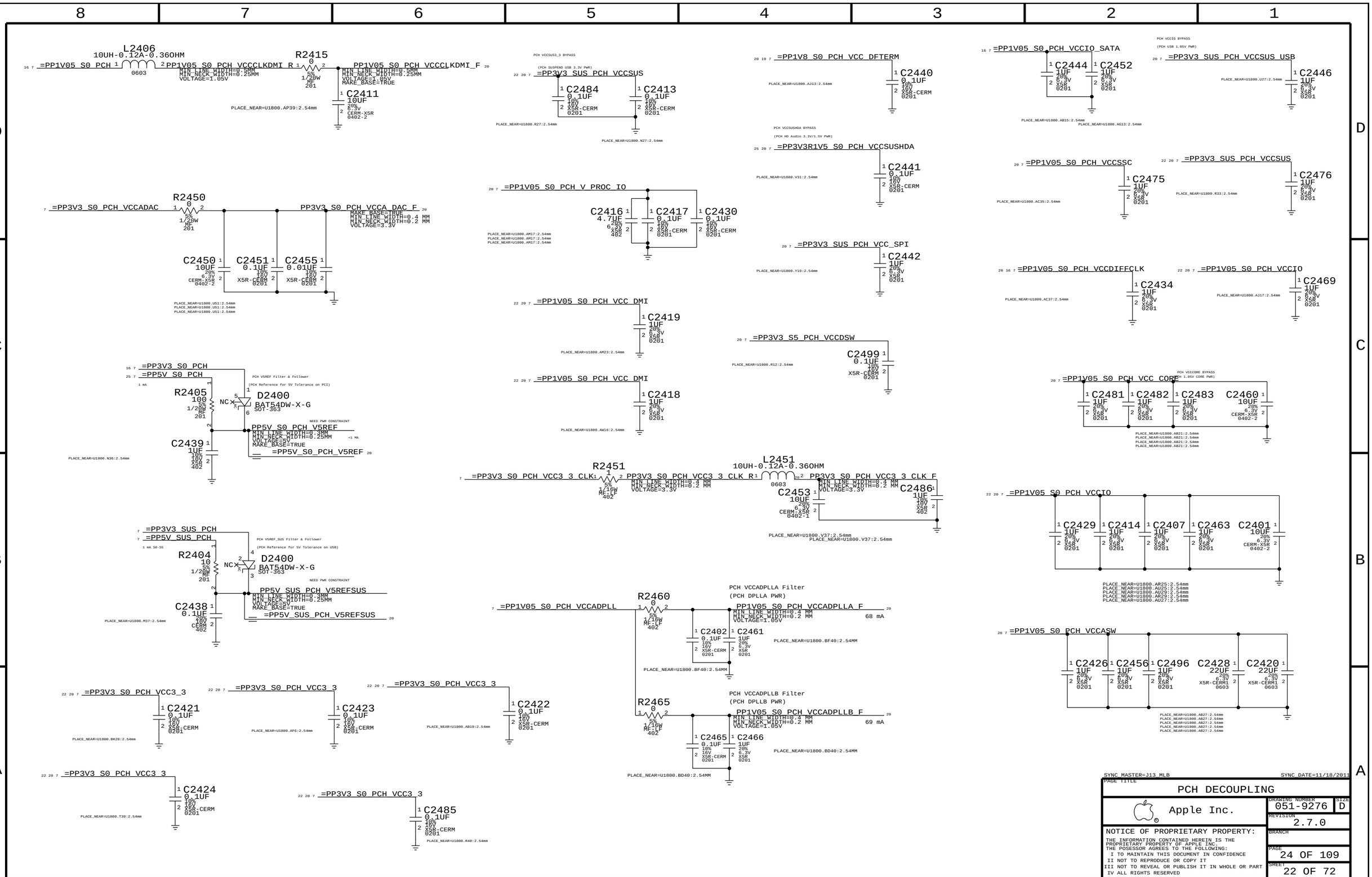

SYNC MASTER=J13_MLB SYNC_DATE=11/18/2013

PAGE TITLE
PCH DECOUPLING

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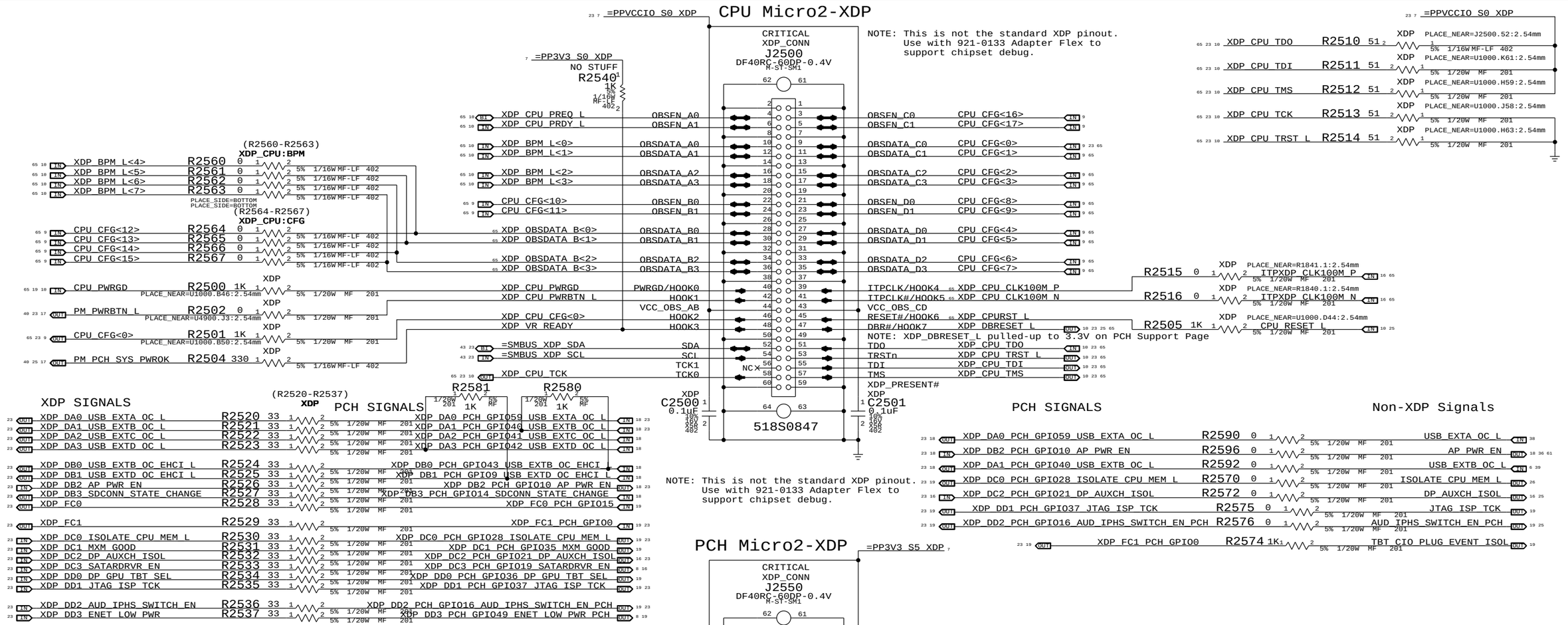
CPU Micro2-XDP



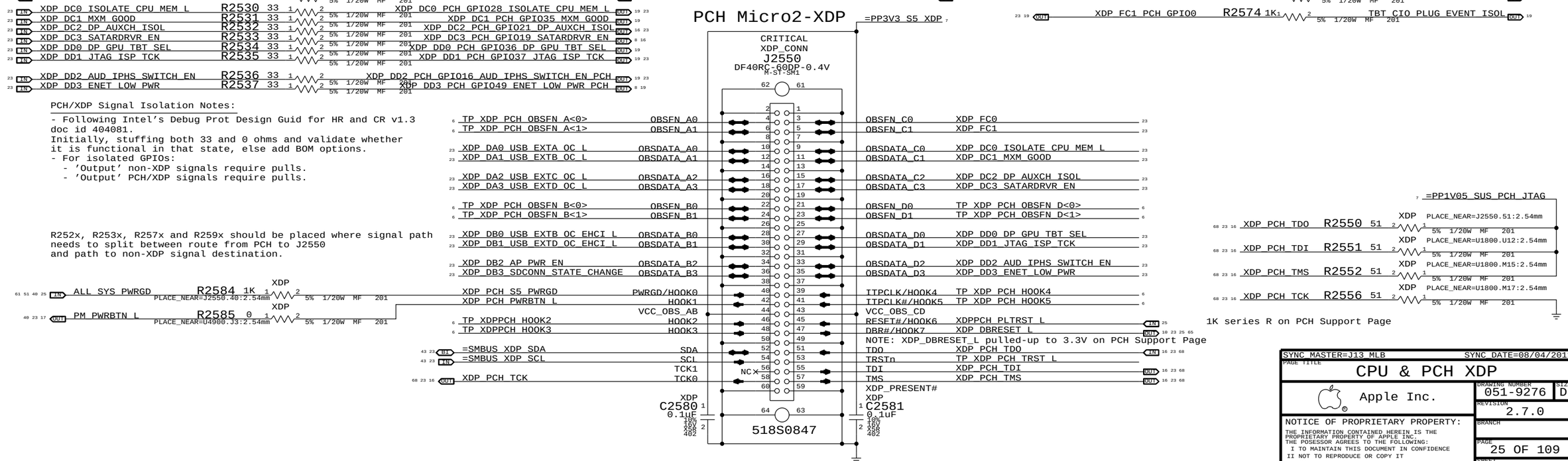
XDP SIGNALS

PCH SIGNALS

PCH SIGNALS

Non-XDP Signals

PCH Micro2-XDP



PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
  Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

SYNC_MASTER=J13_MLB	SYNC_DATE=08/04/2011
PAGE TITLE: CPU & PCH XDP	
Apple Inc.	DRAWING NUMBER: 051-9276 SIZE: D
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	PAGE: 25 OF 109
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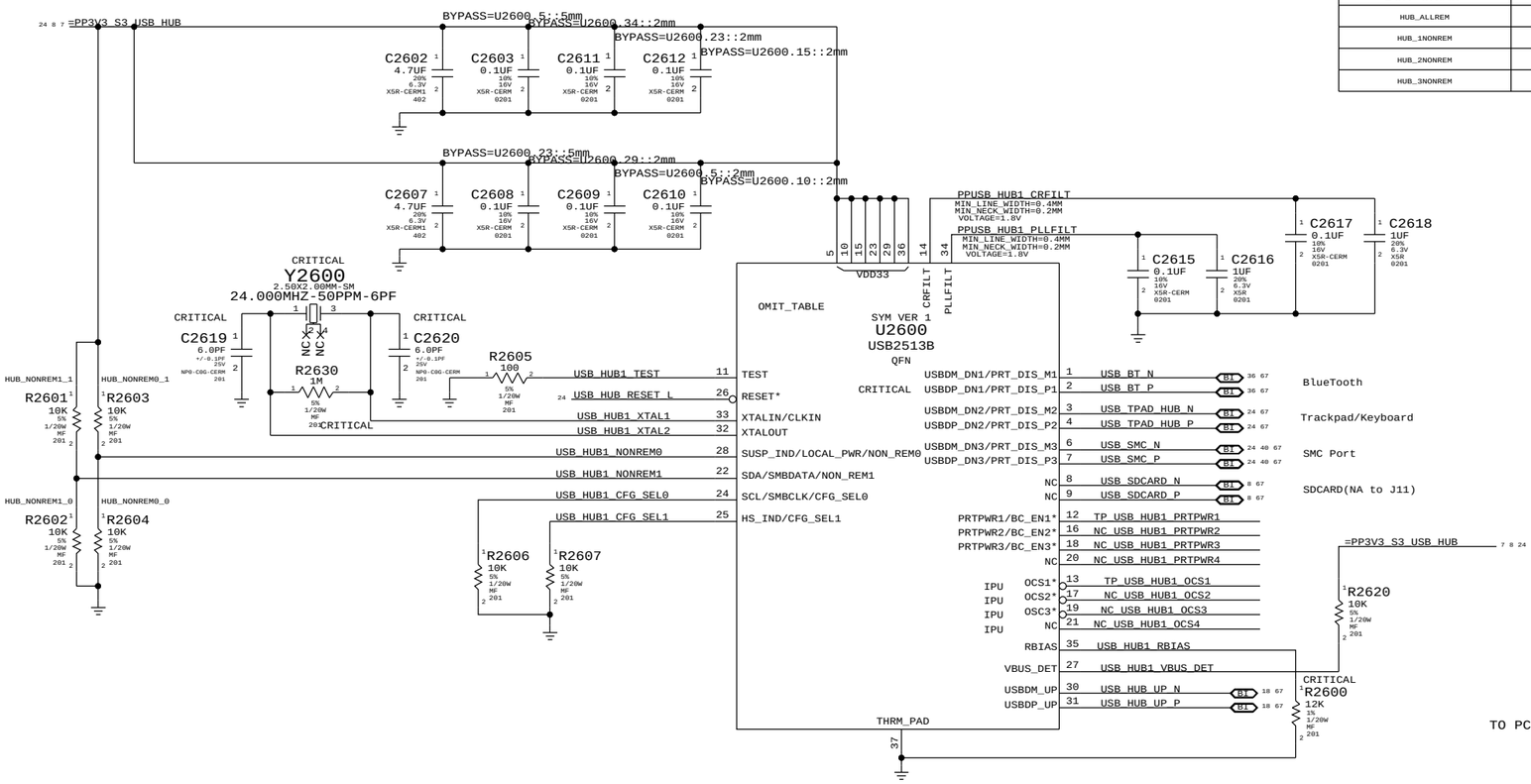
BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

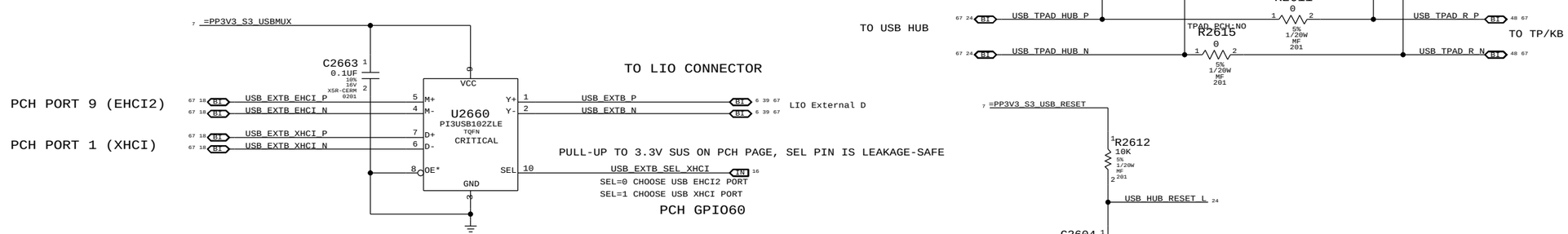
NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0983	1	IC,USB2512B,USB 2.0 HUB CNTRL,36-QFN	U2600	CRITICAL	USBHUB2512B
338S0923	1	IC,USB2513B,USB 2.0,HUB CNTRL,3PRT,36QFN	U2600	CRITICAL	USBHUB2513B



USB XHCI/EHCI2 PORT MUX FOR EXT B



SYNC_MASTER=J13_MLB SYNC_DATE=08/12/2011

PAGE TITLE
USB HUB & MUX

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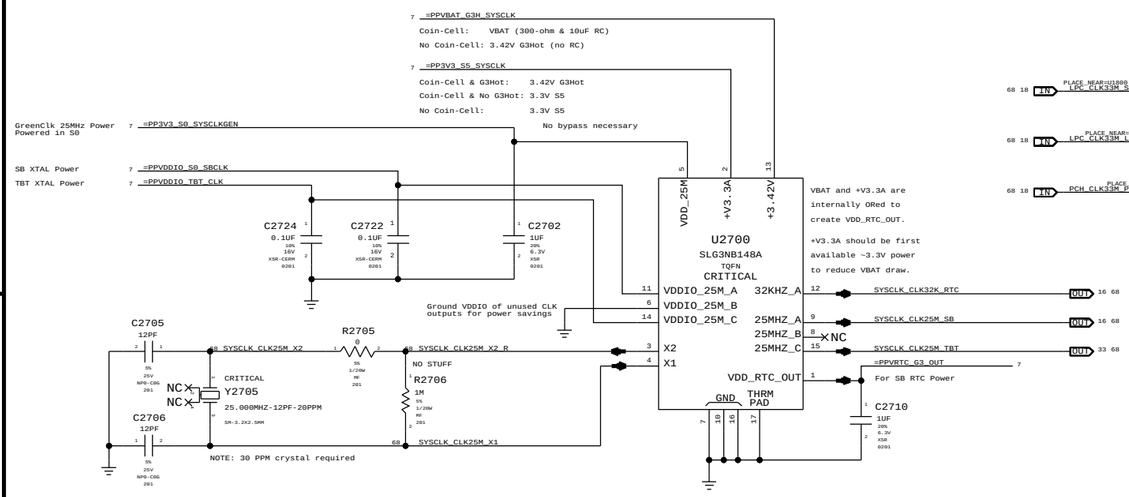
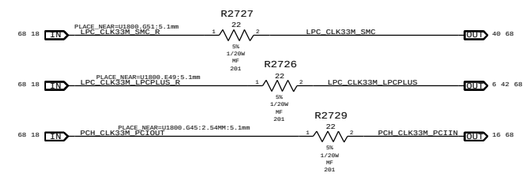
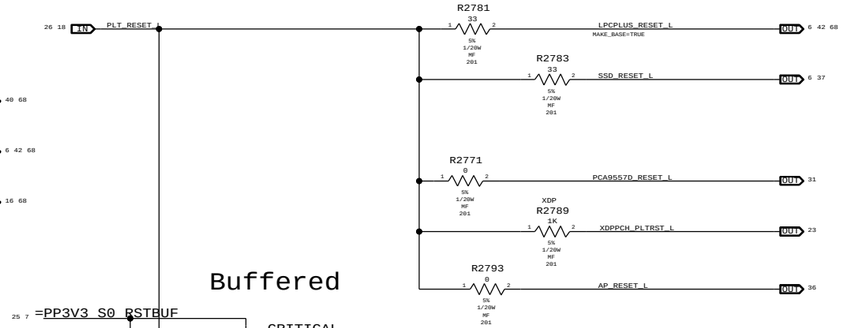
System RTC Power Source & 32kHz / 25MHz Clock Generator



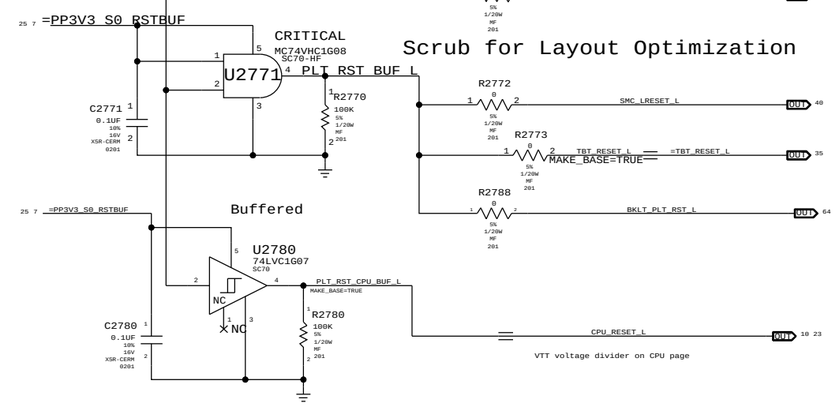


Platform Reset Connections

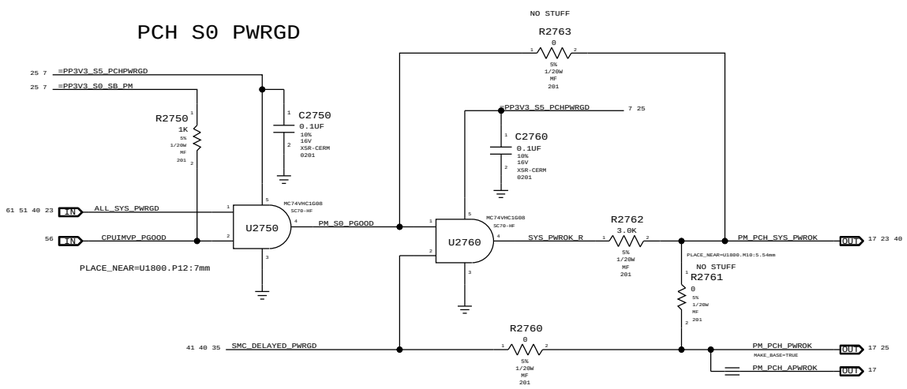
Unbuffered



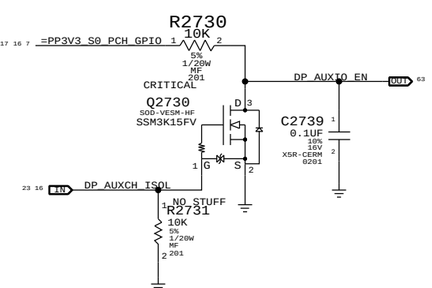
Buffered



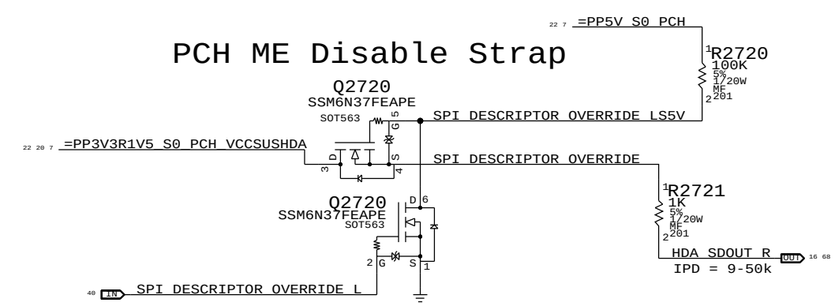
PCH S0 PWRGD



DP_AUXIO_EN Inversion

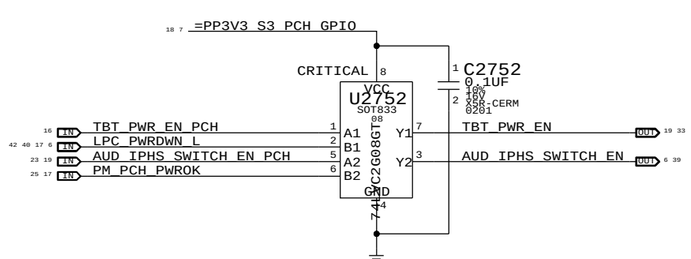


PCH ME Disable Strap

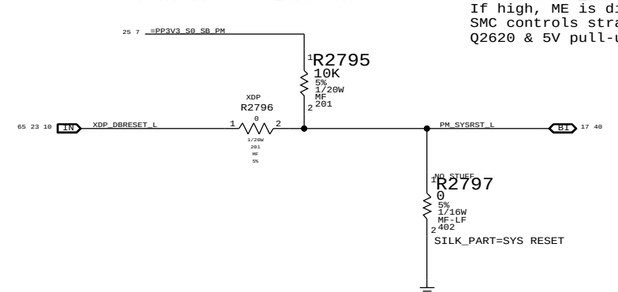


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

GPIO Glitch Prevention



PCH Reset Button



PAGE TITLE	Clock (CK505) and Chipset Support
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D
	REVISION 2.7.0
	BRANCH
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

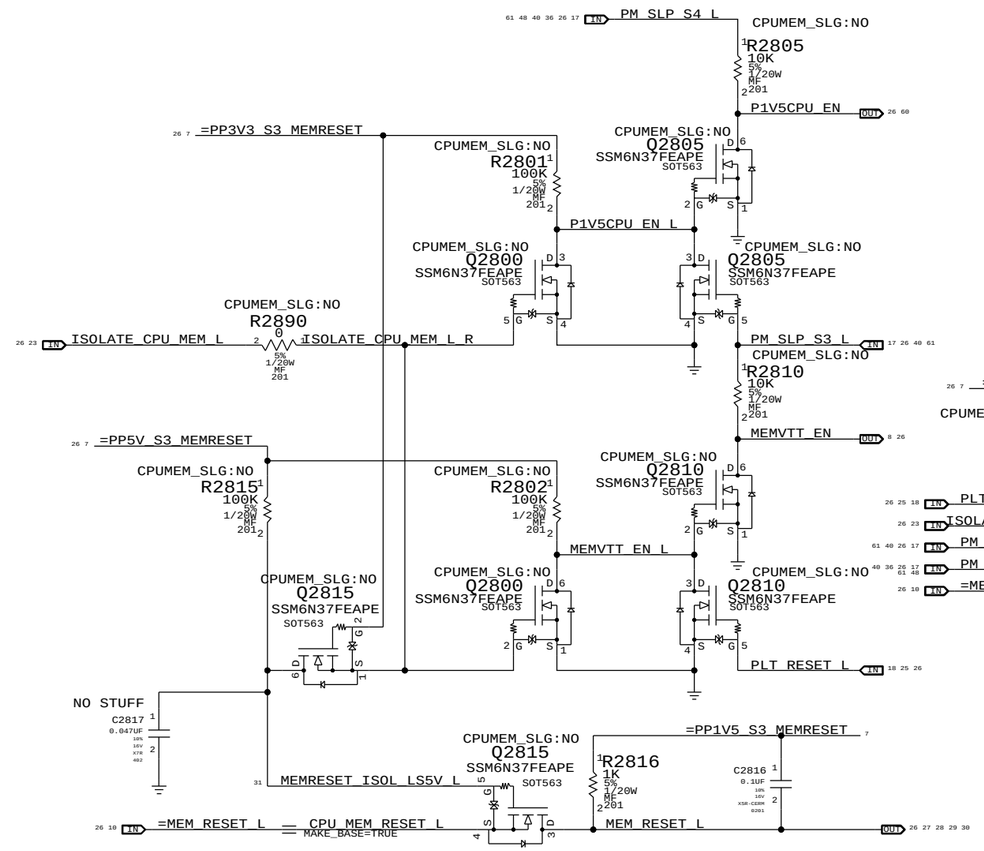
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

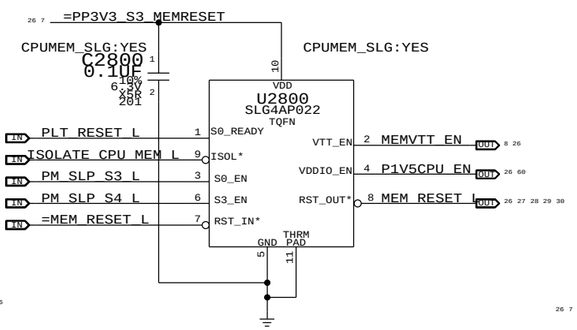
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

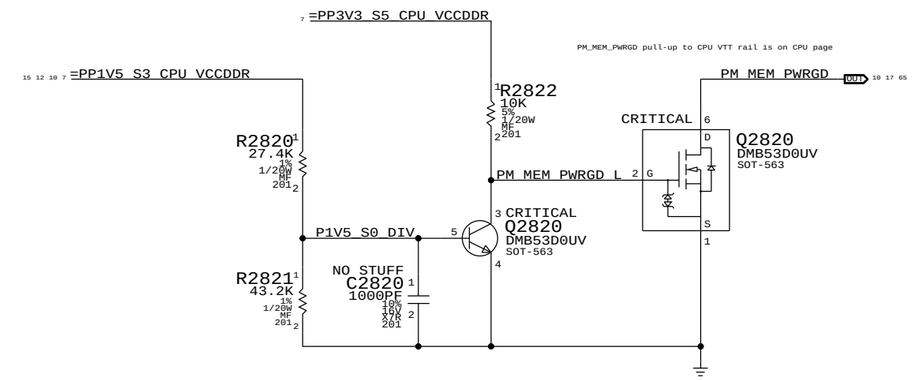
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



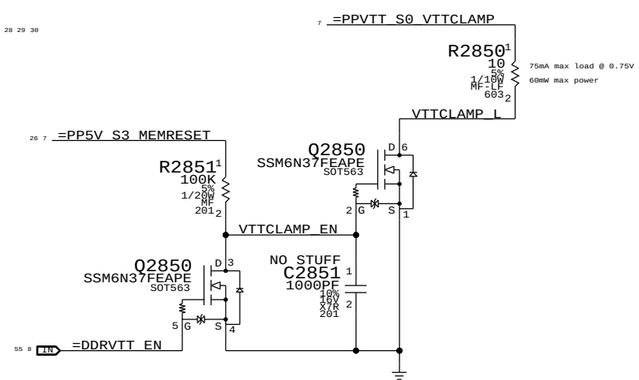


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
S3	4	0	0	1	1	X	1	0	1
	5	0	1	1	1	0 (*)	1	1	1
to	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J13_MLB SYNC_DATE=11/18/2013

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

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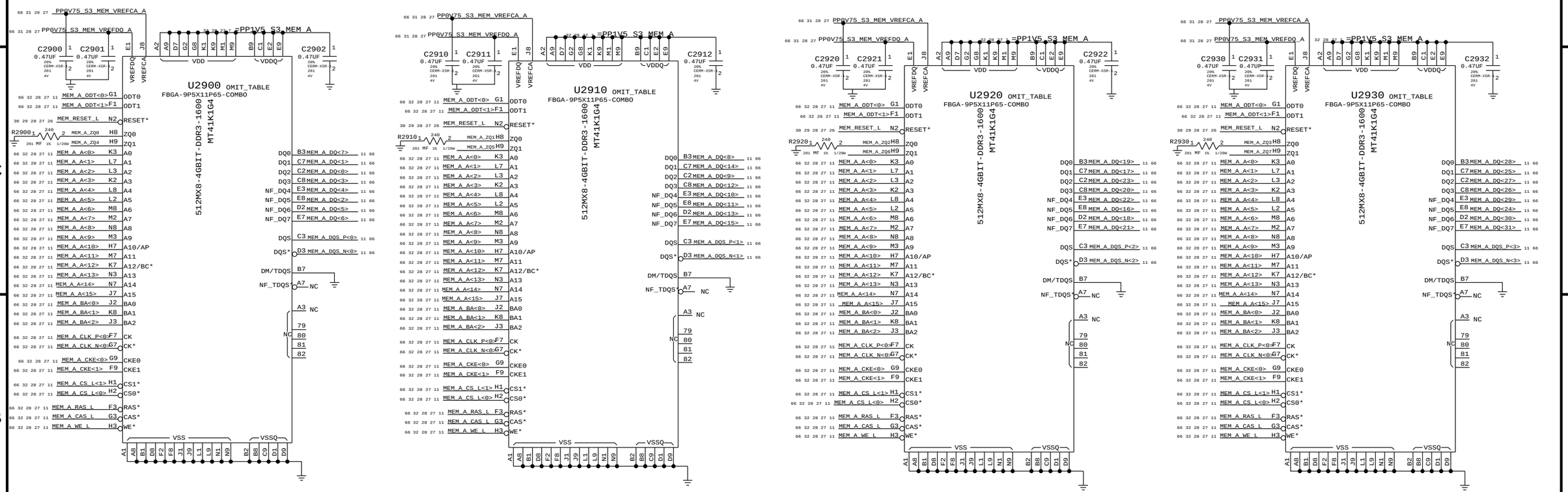
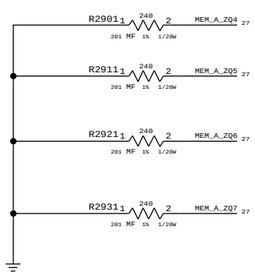


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC_MASTER=J13_MLB SYNC_DATE=08/29/2011

PAGE TITLE
DDR3 DRAM CHANNEL A (0-31)

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
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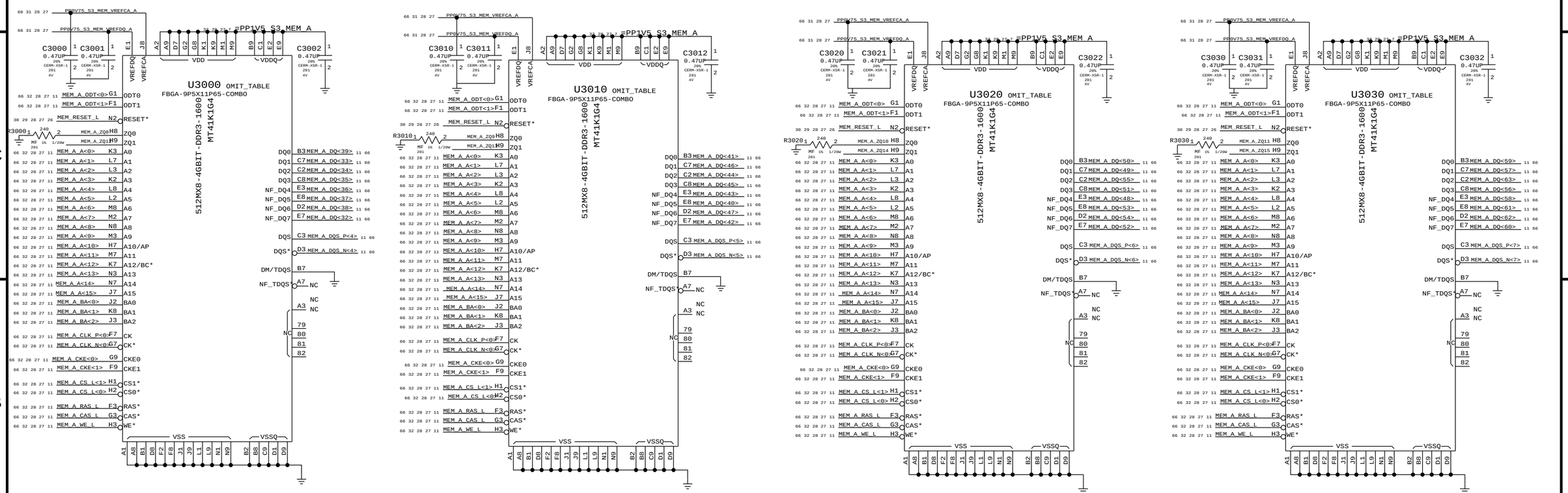
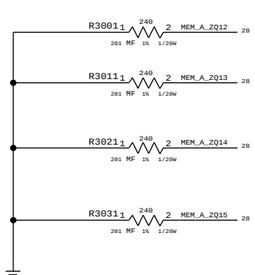


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC MASTER=J13_MLB SYNC DATE=08/29/2013

PAGE TITLE
DDR3 DRAM CHANNEL A (32-63)

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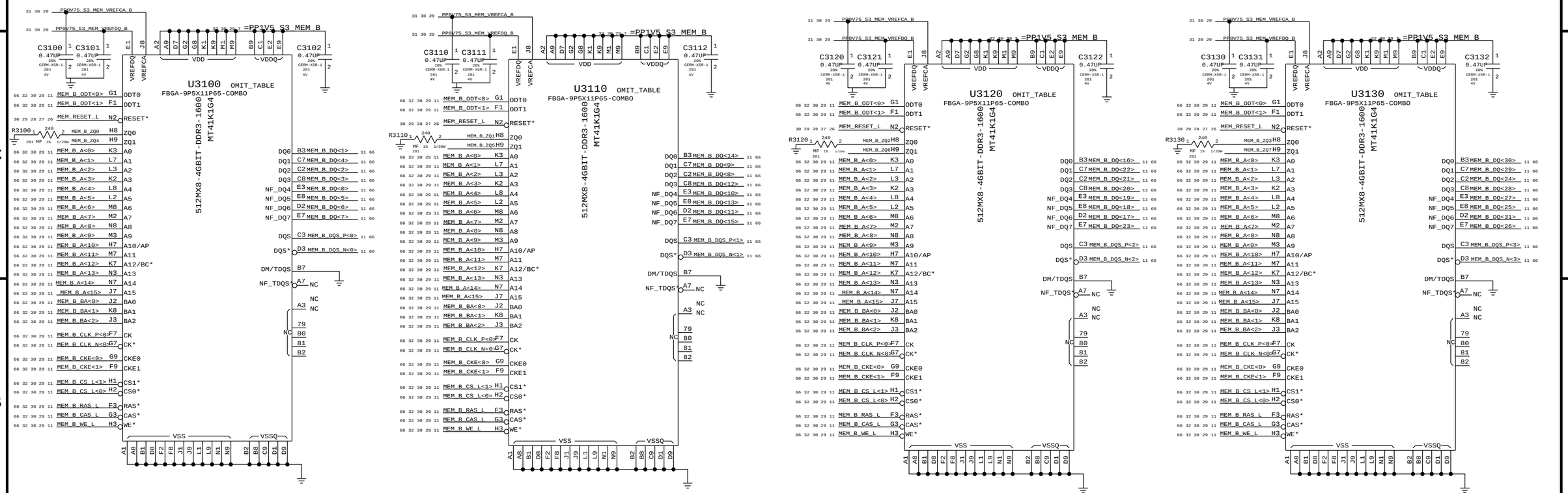
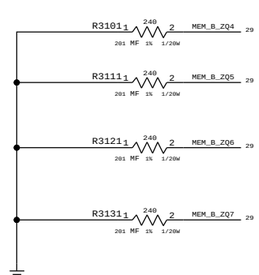


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC_MASTER=J13_MLB SYNC_DATE=08/29/2013

PAGE TITLE
DDR3 DRAM CHANNEL B (0-31)

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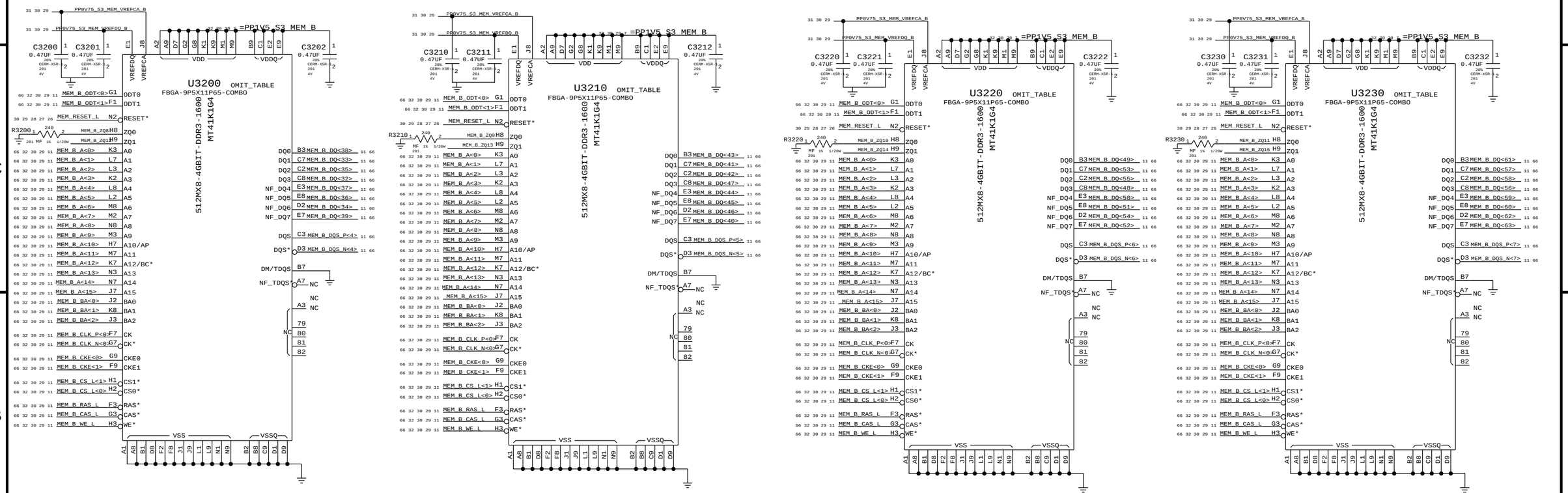
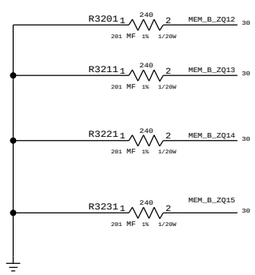


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC_MASTER=J13_MLB SYNC_DATE=08/29/2013

PAGE TITLE
DDR3 DRAM CHANNEL B (32-63)

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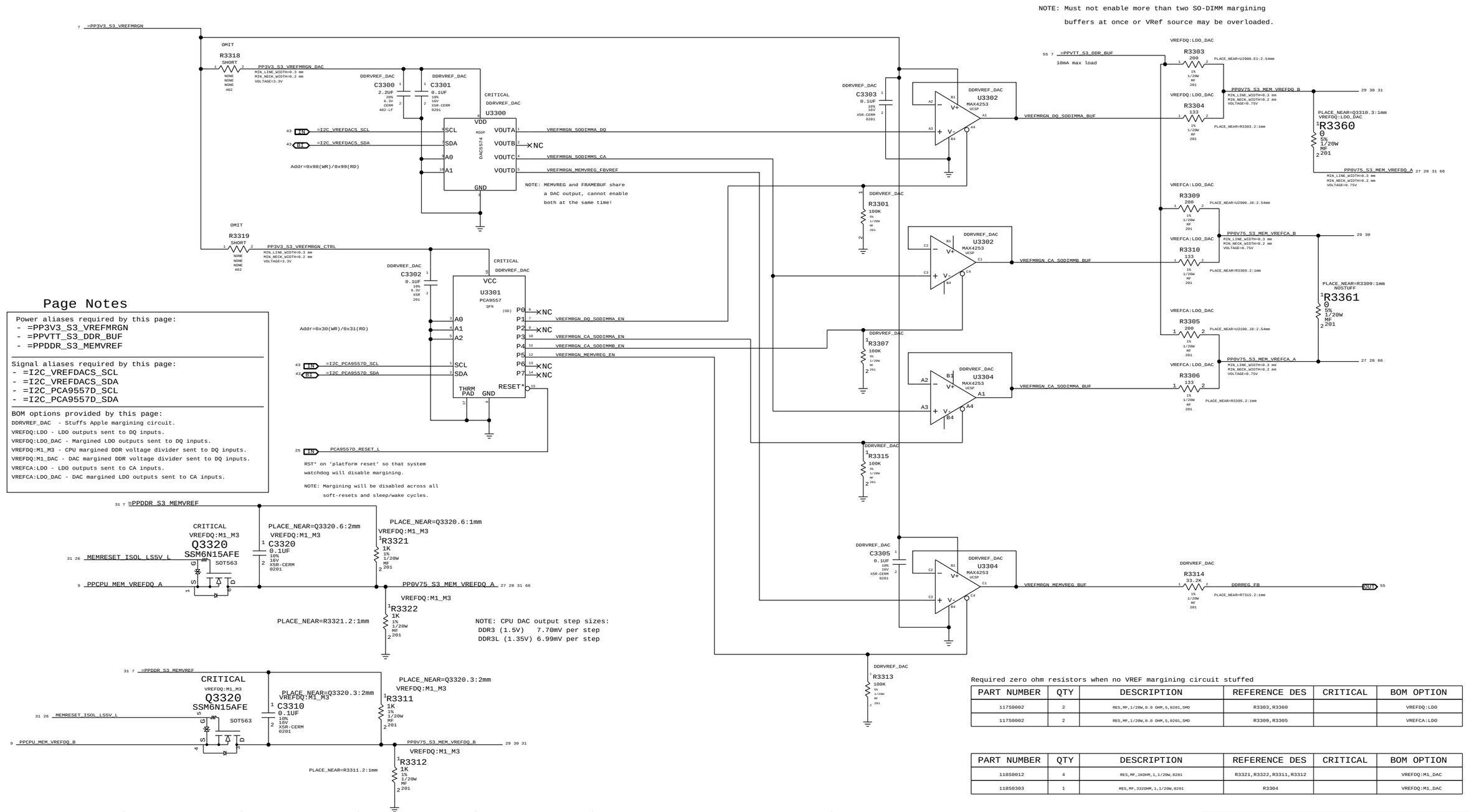

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3303,R3360		VREFDQ:LDO
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3309,R3305		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0012	4	RES,MF,1KOHM,1,1/20W,0201	R3321,R3322,R3311,R3312		VREFDQ:M1_DAC
118S0303	1	RES,MF,332OHM,1,1/20W,0201	R3304		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=J13_MLB SYNC_DATE=11/18/2013

PAGE TITLE
FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
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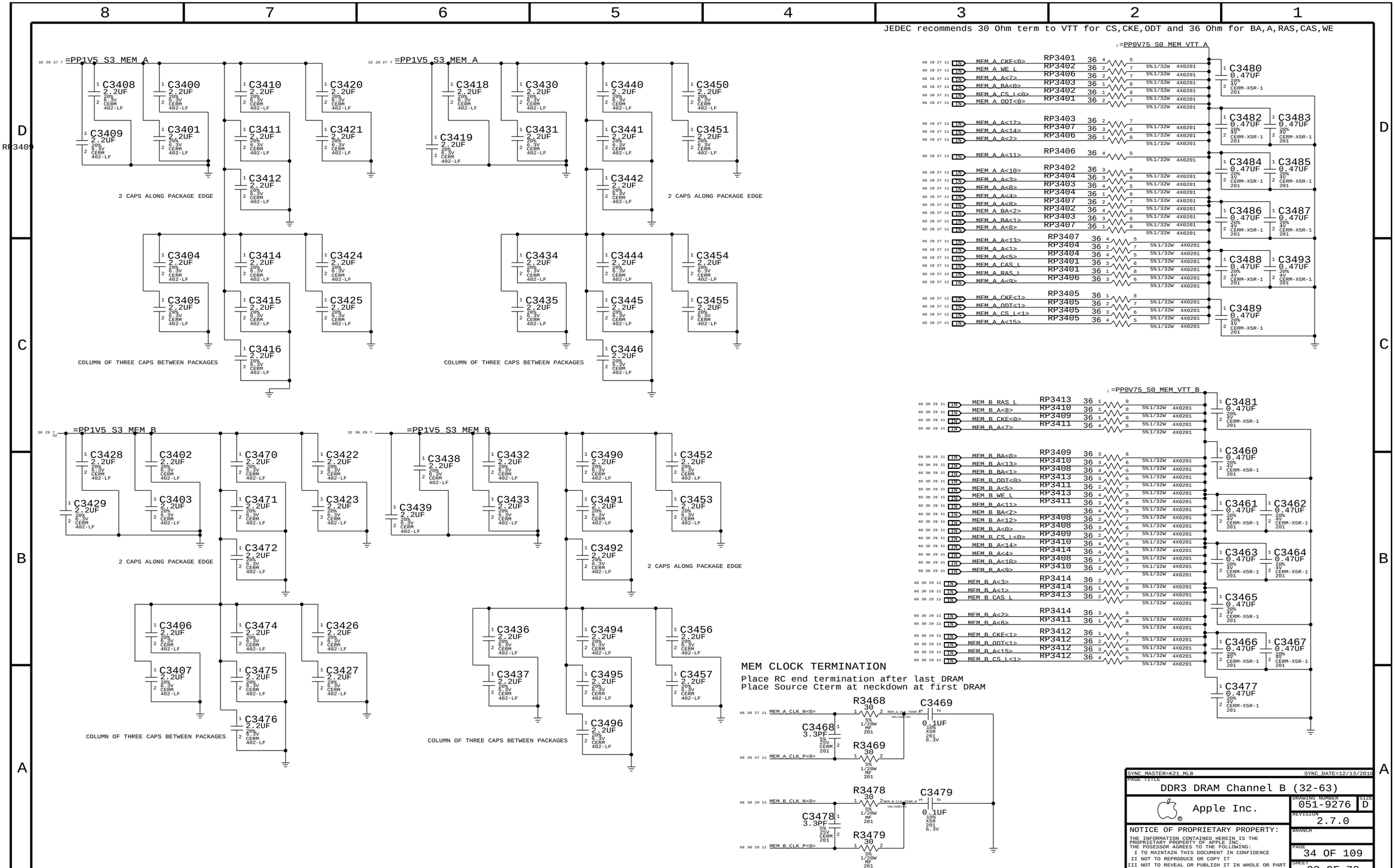
JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE
=PP1V5_S3_MEM_A
2 CAPS ALONG PACKAGE EDGE
COLUMN OF THREE CAPS BETWEEN PACKAGES
=PP1V5_S3_MEM_B
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
MEM CLOCK TERMINATION
Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM
MEM_A_CLK_N<0>
MEM_A_CLK_P<0>
MEM_B_CLK_N<0>
MEM_B_CLK_P<0>
R3468 30
R3469 30
R3478 30
R3479 30
C3468 3.3PF
C3478 3.3PF
C3469 0.1UF
C3479 0.1UF
SYNC_MASTER=K21_MLB
SYNC_DATE=12/13/2010
PAGE TITLE
DDR3 DRAM Channel B (32-63)
Apple Inc.
DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
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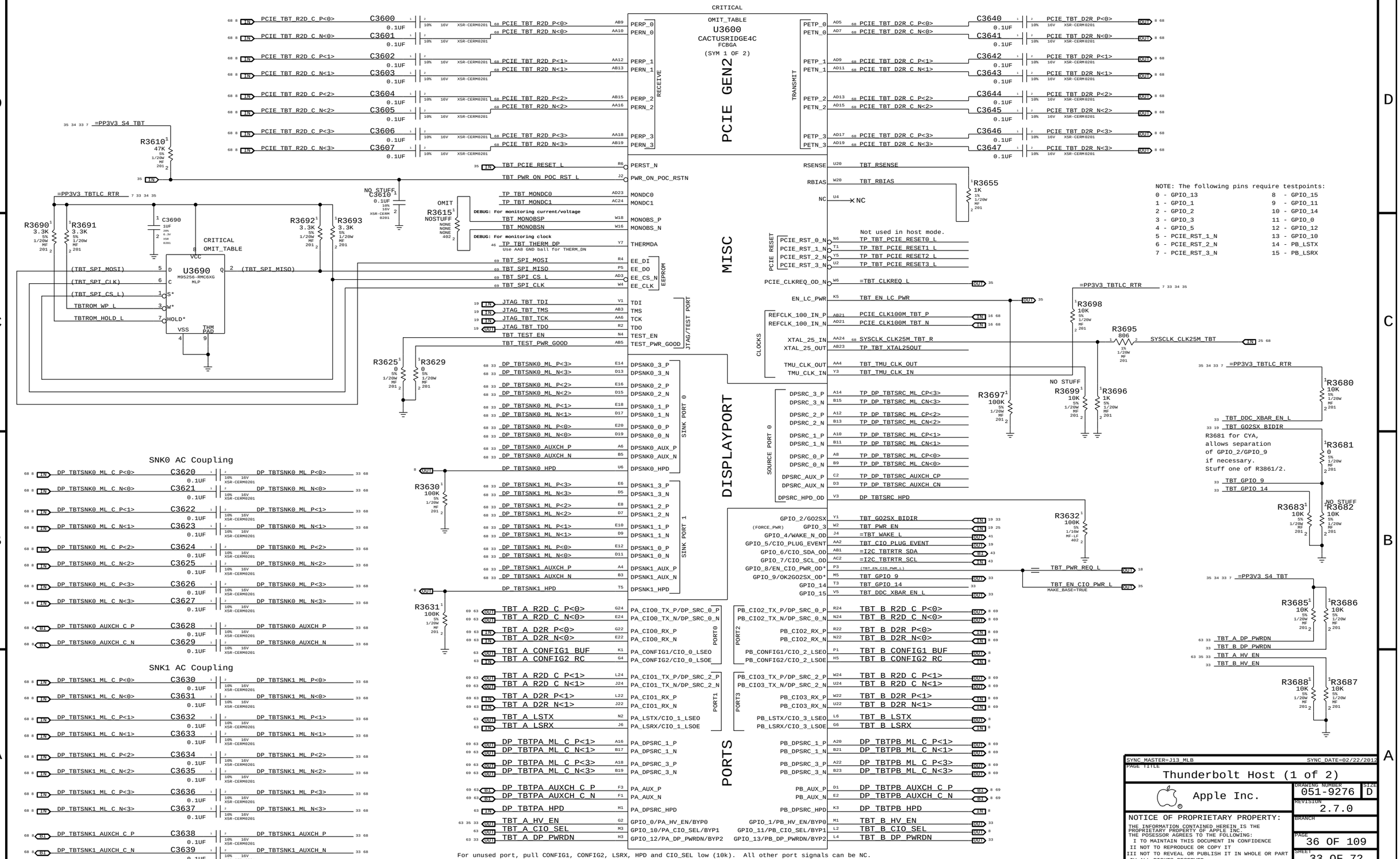

SYNC MASTER=J13_MLB SYNC_DATE=02/22/2012

PAGE TITLE: Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

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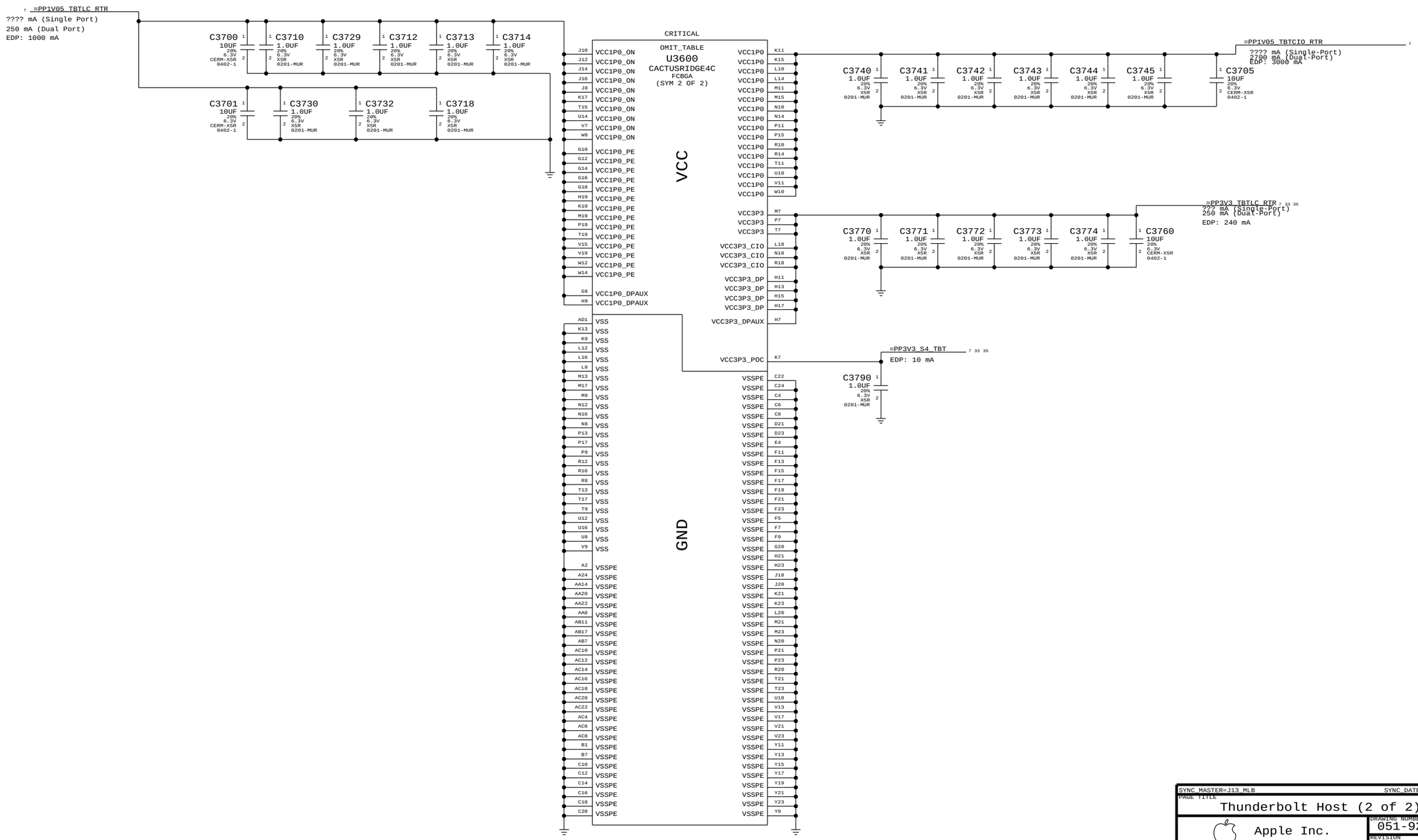

SYNC_MASTER=J13_MLB SYNC_DATE=09/01/2011

PAGE TITLE
Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

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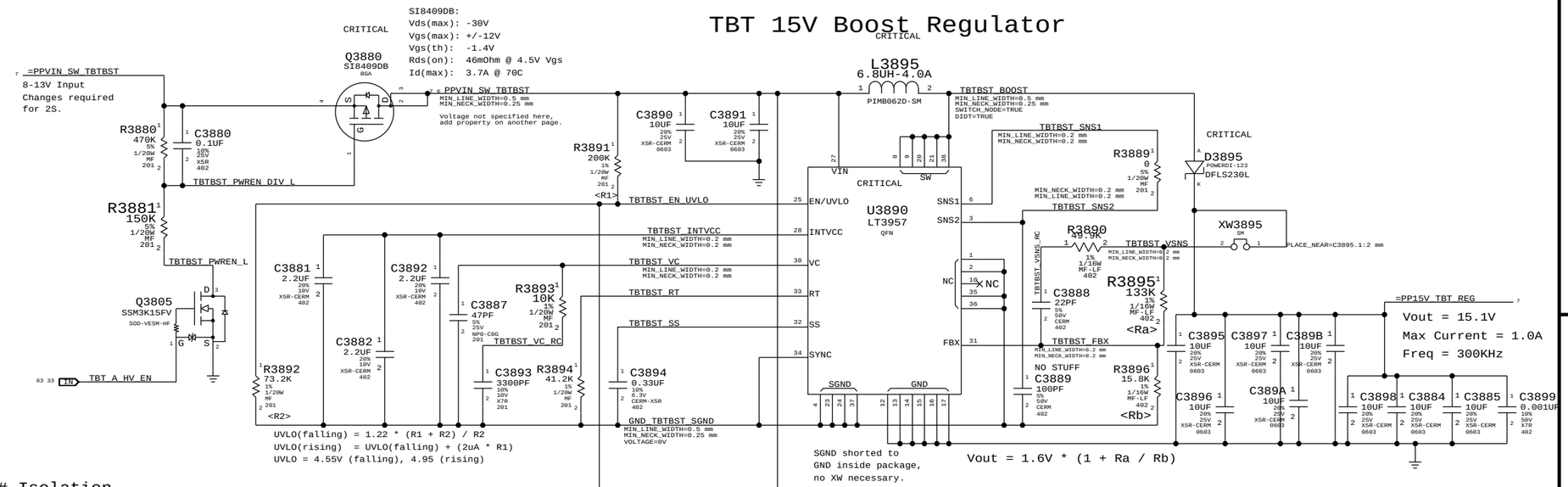
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP18V_TBT_REG (18V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

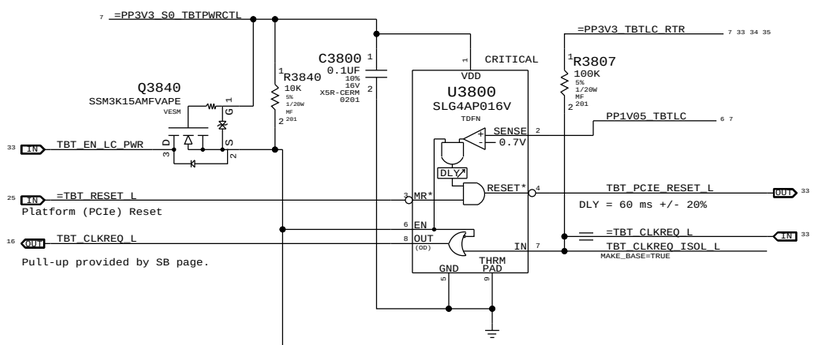
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 18V boost circuitry.

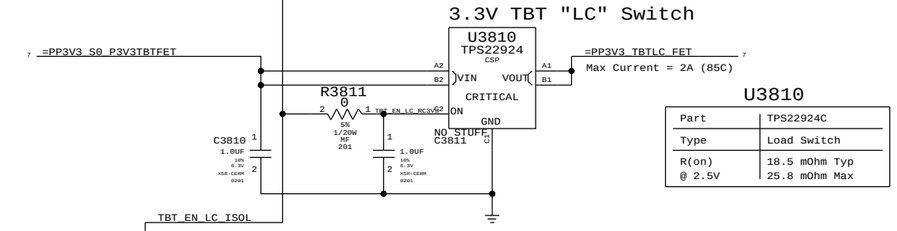
TBT 15V Boost Regulator



Supervisor & CLKREQ# Isolation

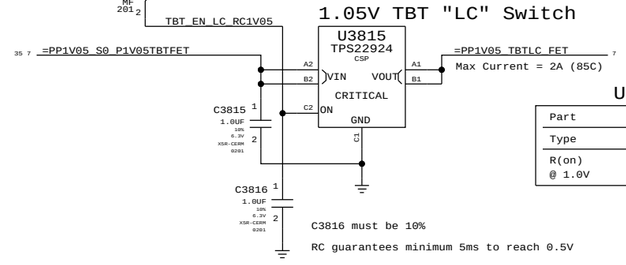


3.3V TBT "LC" Switch



U3810	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

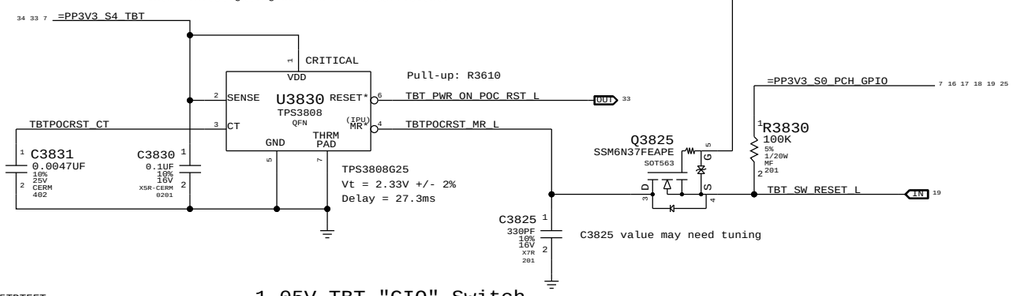
1.05V TBT "LC" Switch



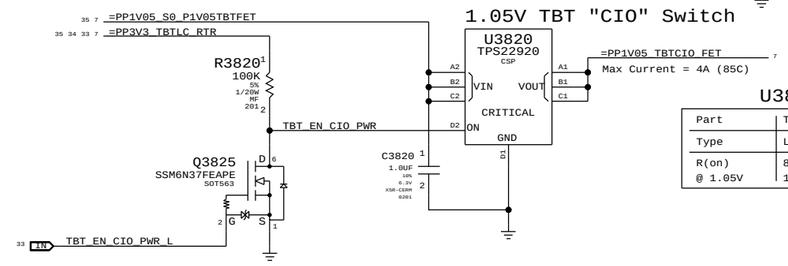
U3815	
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.



1.05V TBT "CIO" Switch



U3820	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=J13_MLB SYNC_DATE=11/18/2011

PAGE TITLE: TBT Power Support

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

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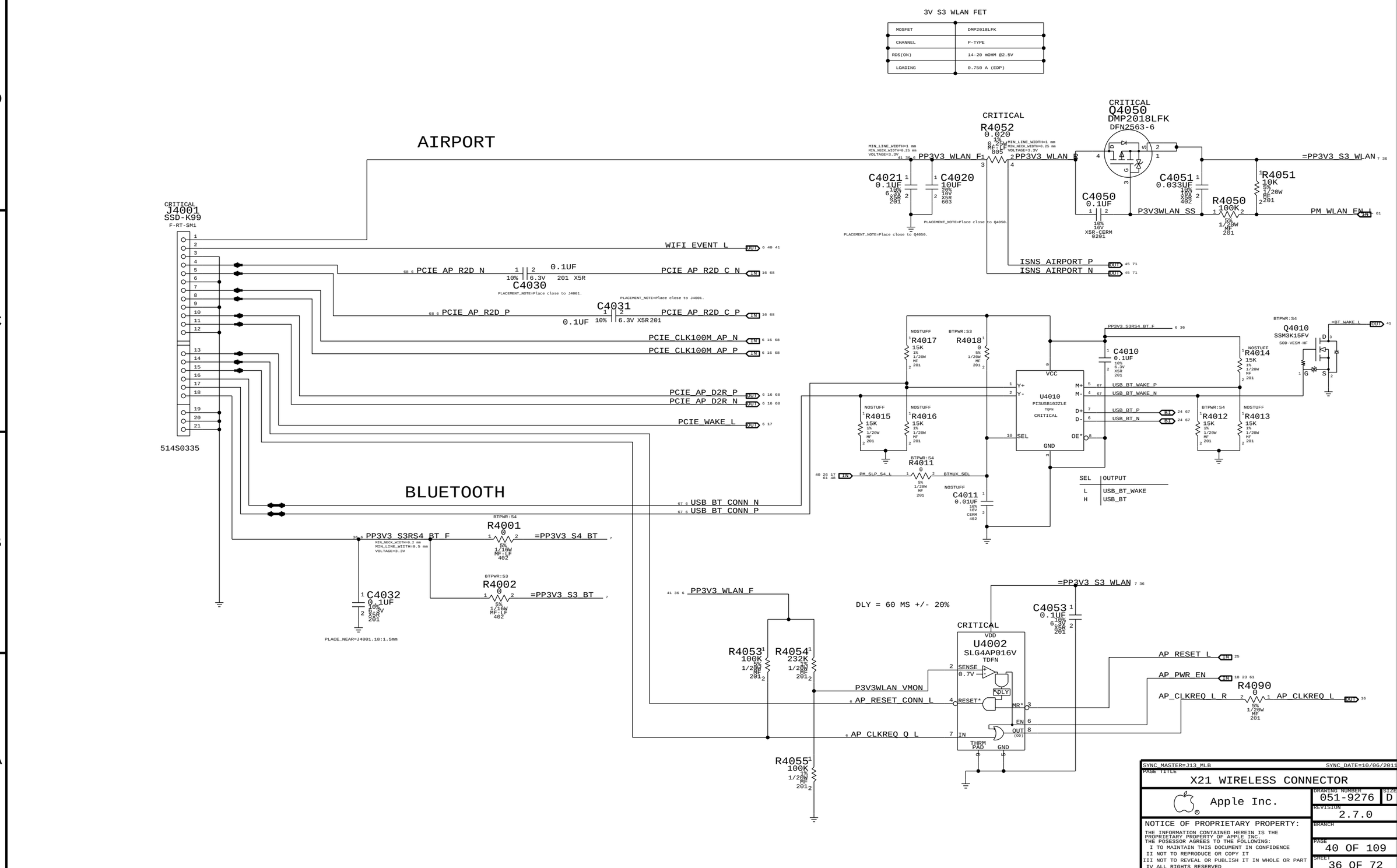
3V S3 WLAN FET
MOSFET DMP2018LFK
CHANNEL P-TYPE
RDS(ON) 14-20 mOHM @2.5V
LOADING 0.750 A (EDP)
AIRPORT
CRITICAL J4001 SSD-K99 F-RT-SM1
514S0335
WIFI EVENT L
PCIE AP R2D N
PCIE AP R2D C N
PCIE AP R2D P
PCIE AP R2D C P
PCIE CLK100M AP N
PCIE CLK100M AP P
PCIE AP D2R P
PCIE AP D2R N
PCIE WAKE L
C4030 0.1UF
C4031 0.1UF
PLACEMENT_NOTE=Place close to J4001.
CRITICAL R4052 0.020
PP3V3 WLAN F
PP3V3 WLAN
C4021 0.1UF
C4020 10UF
CRITICAL Q4050 DMP2018LFK DFN2563-6
C4050 0.1UF
C4051 0.033UF
R4050 100K
R4051 10K
=PP3V3 S3 WLAN
PM WLAN EN L
P3V3WLAN SS
ISNS AIRPORT P
ISNS AIRPORT N
PLACEMENT_NOTE=Place close to Q4050.
BLUETOOTH
USB BT CONN N
USB BT CONN P
PP3V3 S3RS4 BT F
R4001 0
=PP3V3 S4 BT
R4002 0
=PP3V3 S3 BT
C4032 0.1UF
PLACE_NEAR=J4001.18:1.5mm
R4017 15K
R4018 0
R4015 15K
R4016 15K
R4011 0
PM SLP S4 L
BTMUX SEL
C4011 0.01UF
U4010 PI3USB102ZLE TQFN CRITICAL
VCC
GND
SEL
OE*
USB BT WAKE P
USB BT WAKE N
USB BT P
USB BT N
C4010 0.1UF
R4014 15K
R4012 15K
R4013 15K
Q4010 SSM3K15FV SOD-VESM-HF
=BT WAKE L
SEL OUTPUT
L USB_BT_WAKE
H USB_BT
PP3V3 WLAN F
DLY = 60 MS +/- 20%
C4053 0.1UF
CRITICAL U4002 SLG4AP016V TDFN
VDD
SENSE 0.7V
RESET*
DLY
MR*
EN
OUT (OD)
IN
THRM PAD
GND
R4053 100K
R4054 232K
R4055 100K
P3V3WLAN VMON
AP RESET CONN L
AP CLKREQ Q L
AP RESET L
AP PWR EN
AP CLKREQ L R
R4090 0
AP CLKREQ L
SYNC MASTER=J13 MLB
SYNC DATE=10/06/2013
PAGE TITLE
X21 WIRELESS CONNECTOR
Apple Inc.
DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
BRANCH
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SHEET 36 OF 72
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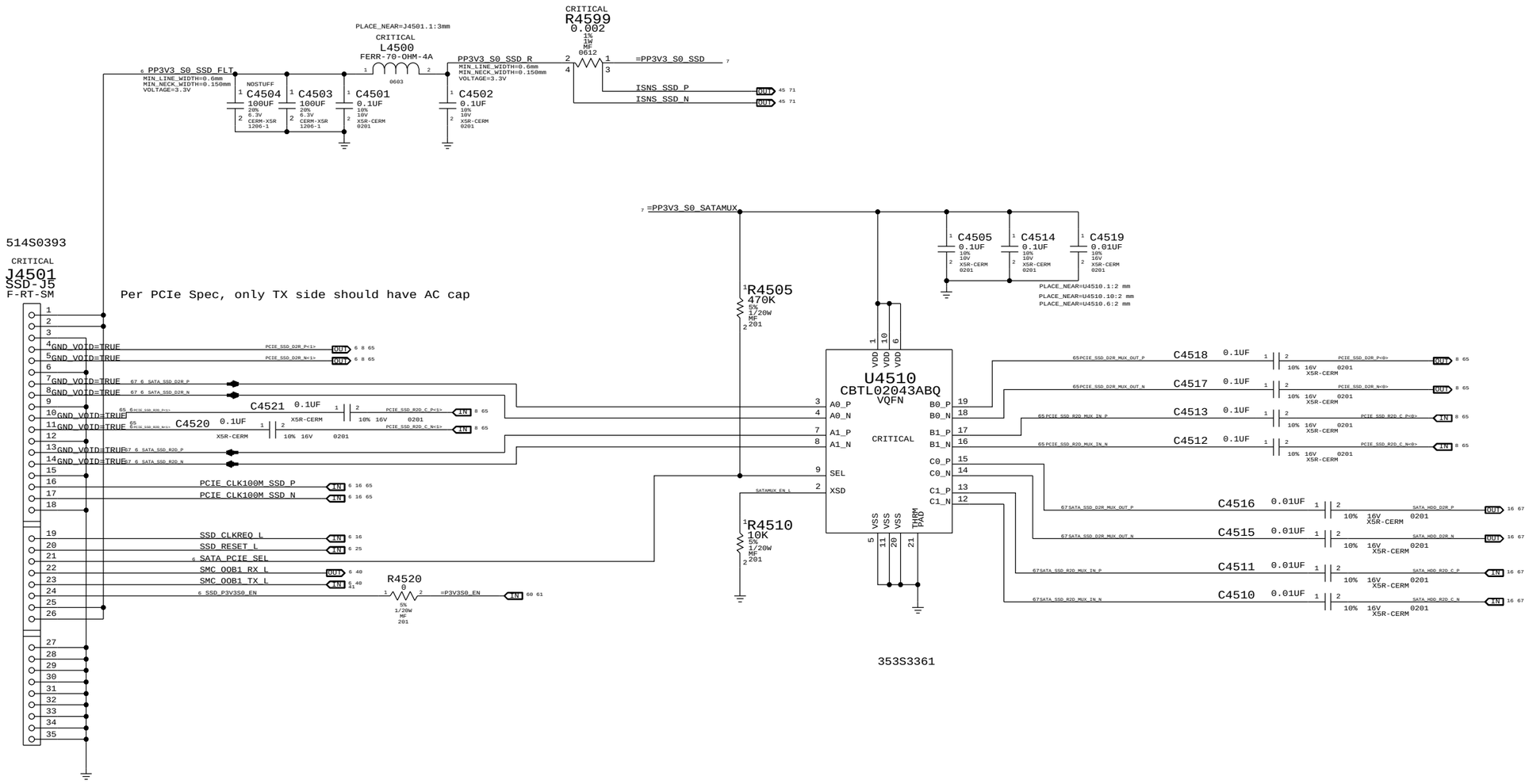

PCIE/SATA GUMSTICK2 CONNECTOR

SYNC MASTER=J13 MLB SYNC DATE=11/18/2013

PAGE TITLE

SSD CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

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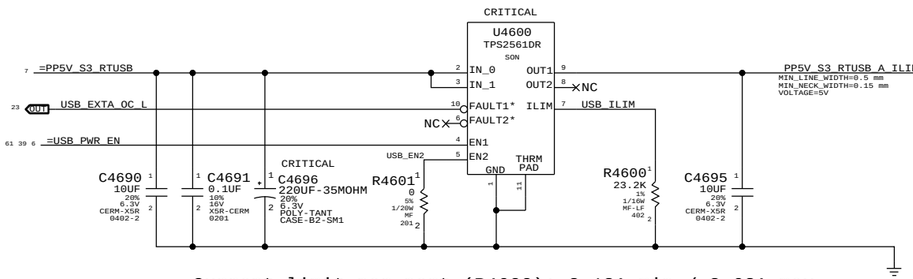
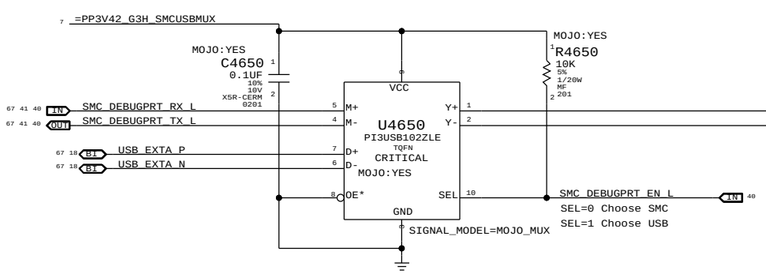
Right USB Port A

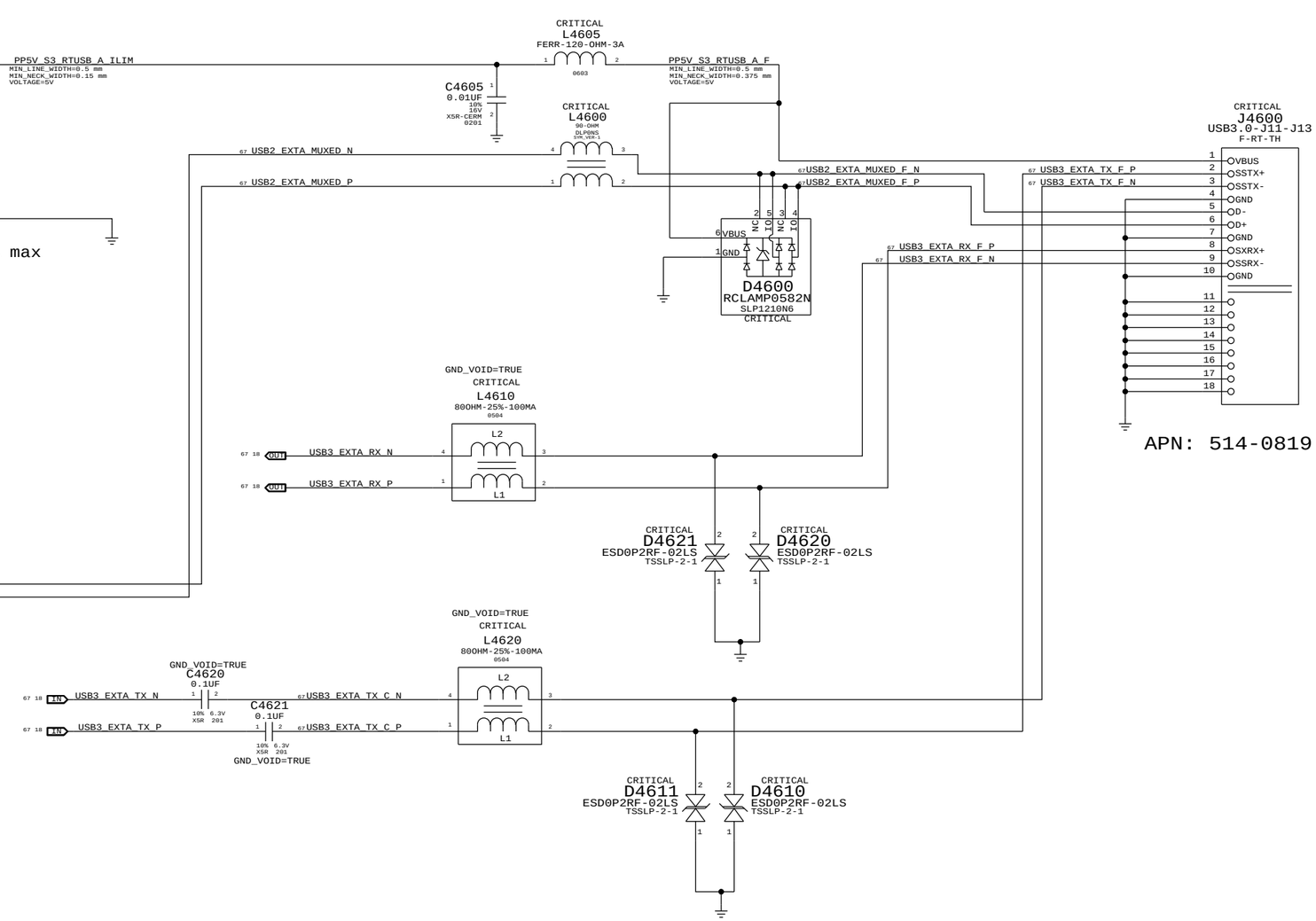
USB Port Power Switch



Current limit per port (R4600): 2.18A min / 2.63A max

Mojo SMC Debug Mux





SYNC_MASTER=J13_MLB	SYNC_DATE=10/06/2011
PAGE TITLE: External A USB3 Connector	
Apple Inc.	DRAWING NUMBER: 051-9276 SIZE: D
	REVISION: 2.7.0
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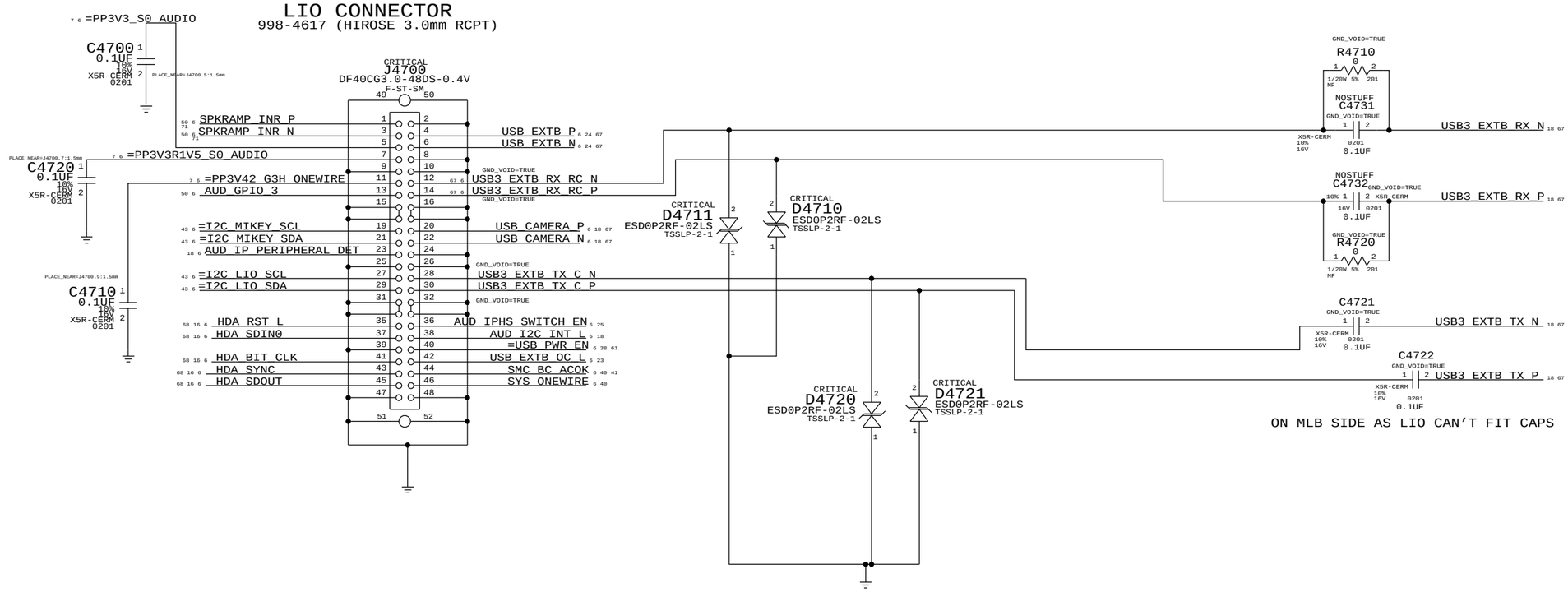
LIO CONNECTOR
998-4617 (HIROSE 3.0mm RCPT)



ON MLB SIDE AS LIO CAN'T FIT CAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
LIO CONNECTORS

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

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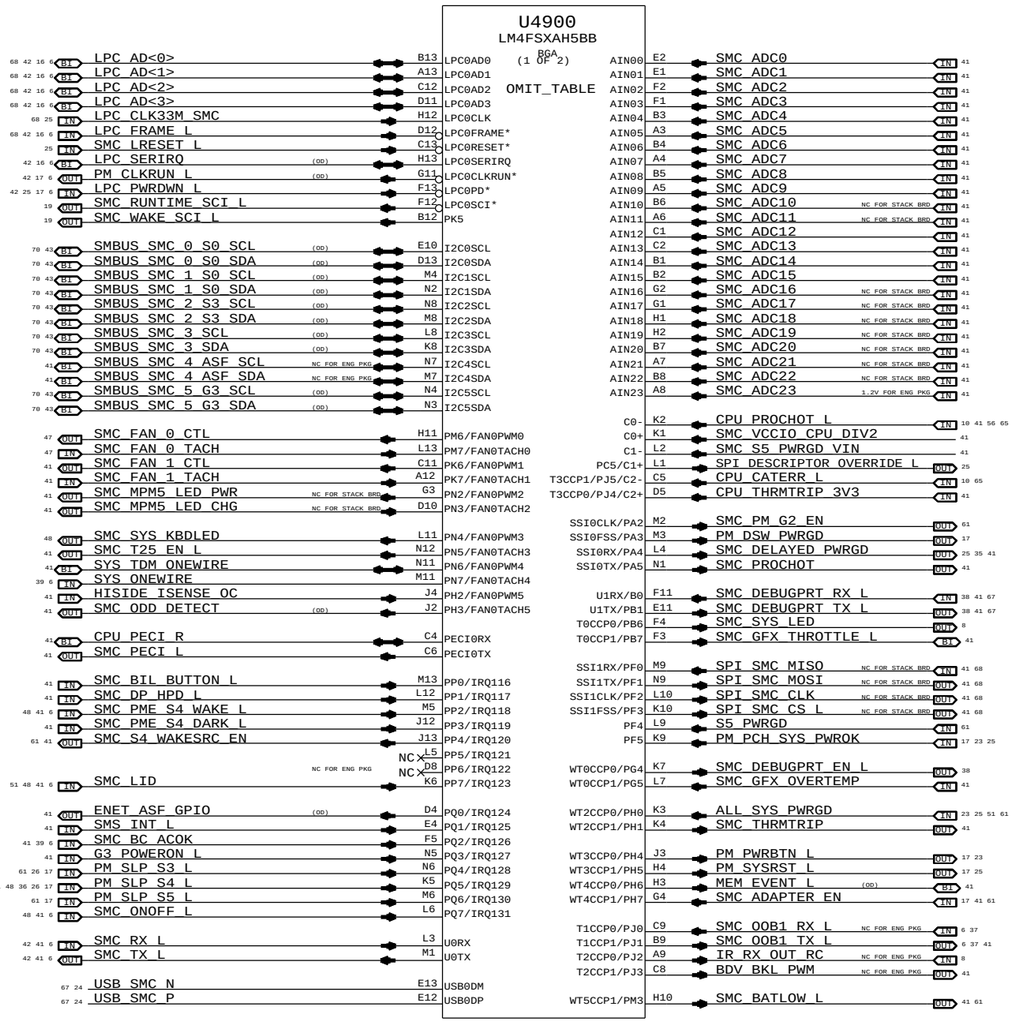

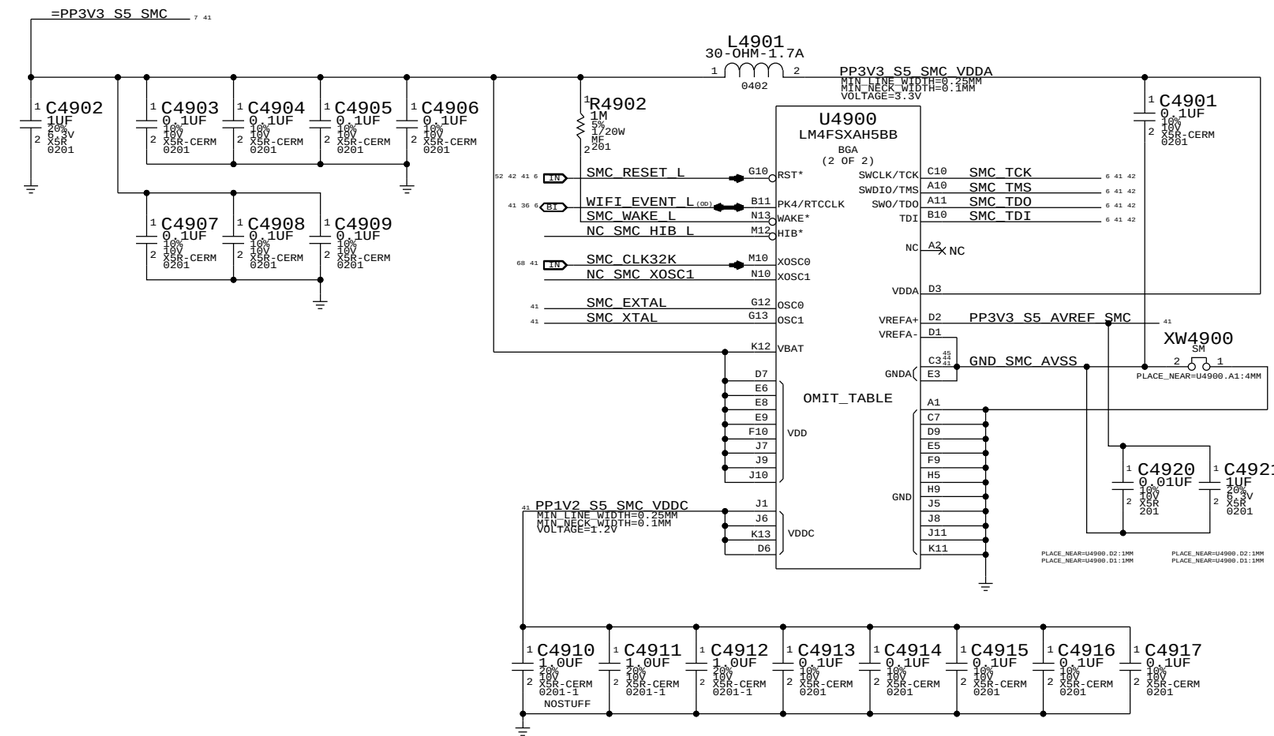

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC MASTER=J30 MLB SYNC DATE=07/26/2011

PAGE TITLE
SMC

Apple Inc.

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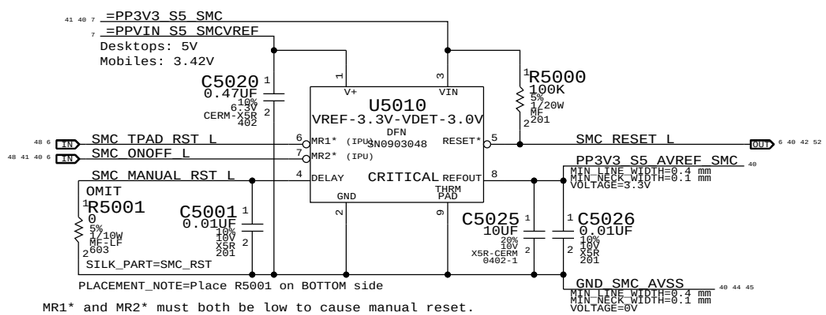
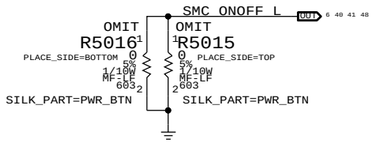
SMC Reset "Button", Supervisor & AVREF Supply



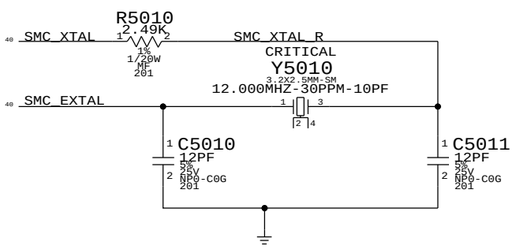
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



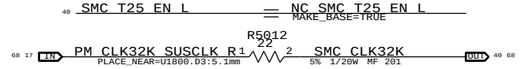
SMC Crystal Circuit

SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz



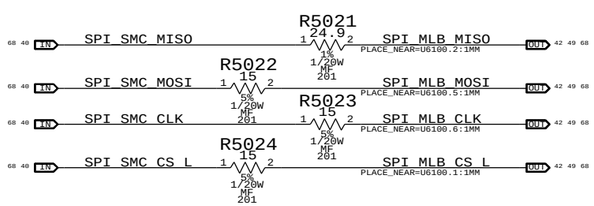
Note:
ADC10 and ADC11 are shared with comparators on Stack Board.

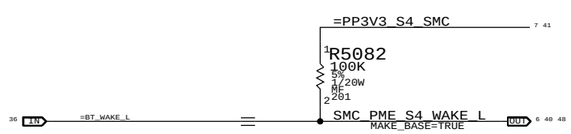
SMC_ADC0	SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_ADC1	SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_ADC2	SMC_VCCSA_VSENSE	MAKE_BASE=TRUE
SMC_ADC3	SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_ADC4	SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_ADC5	SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_ADC6	SMC_HDD_ISENSE	MAKE_BASE=TRUE
SMC_ADC7	SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_ADC8	SMC_HS_COMPUTING_ISENSE	MAKE_BASE=TRUE
SMC_ADC9	SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC10	SMC_1V5S3_ISENSE	MAKE_BASE=TRUE
SMC_ADC11	SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE
SMC_ADC12	SMC_GFX_VSENSE	MAKE_BASE=TRUE
SMC_ADC13	SMC_CPU_SA_ISENSE	MAKE_BASE=TRUE
SMC_ADC14	SMC_3V3S0_ISENSE	MAKE_BASE=TRUE
SMC_ADC15	SMC_WLAN_ISENSE	MAKE_BASE=TRUE
SMC_ADC16	SMC_LCDBKLT_ISENSE	MAKE_BASE=TRUE
SMC_ADC17	NC_SCM_ADC17	MAKE_BASE=TRUE
SMC_ADC18	SMC_GFX_ISENSE	MAKE_BASE=TRUE
SMC_ADC19	NC_SMC_ADC19	MAKE_BASE=TRUE
SMC_ADC20	NC_SMC_ADC20	MAKE_BASE=TRUE
SMC_ADC21	NC_SMC_ADC21	MAKE_BASE=TRUE
SMC_ADC22	NC_SMC_ADC22	MAKE_BASE=TRUE
SMC_ADC23	SMC_ADC23	MAKE_BASE=TRUE
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE
SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE
SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE
ENET_ASF_GPIO	NC_ENET_ASF_GPIO	MAKE_BASE=TRUE
SMC_MPM5_LED_PWR	NC_SMC_MPM5_LED_PWR	MAKE_BASE=TRUE
SMC_MPM5_LED_CHG	NC_SMC_MPM5_LED_CHG	MAKE_BASE=TRUE
SYS_TDM_ONEWIRE	NC_SYS_TDM_ONEWIRE	MAKE_BASE=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE
=CHGR_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE
HISIDE_ISENSE_OC	NC_HISIDE_ISENSE_OC	MAKE_BASE=TRUE
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE
BDV_BKL_PWM	NC_BDV_BKL_PWM	MAKE_BASE=TRUE
SMC_PME_S4_DARK_L	=TBT_WAKE_L	MAKE_BASE=TRUE
SMC_T25_EN_L	NC_SMC_T25_EN_L	MAKE_BASE=TRUE

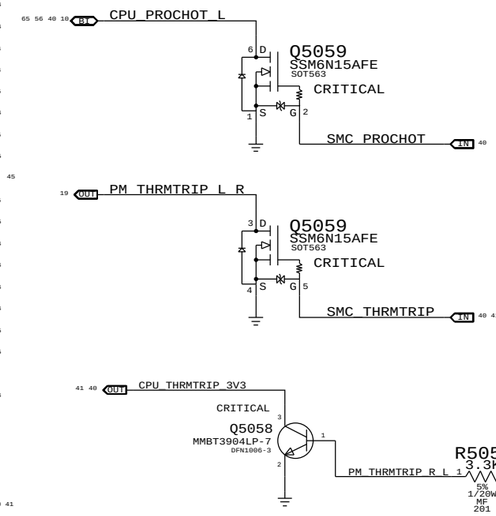


SMC12 SPI Support

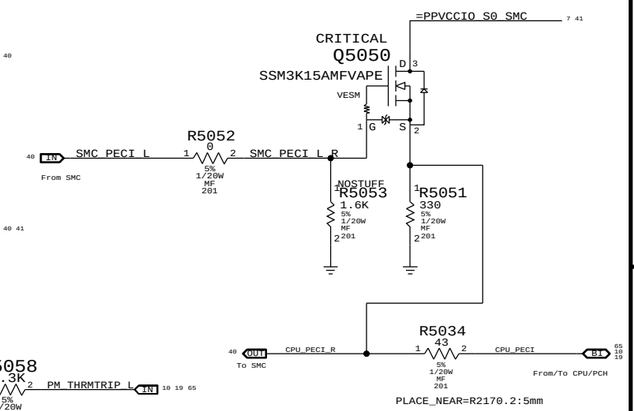
Series resistors are no stuffed until the topology of 2 SPI Masters are verified.





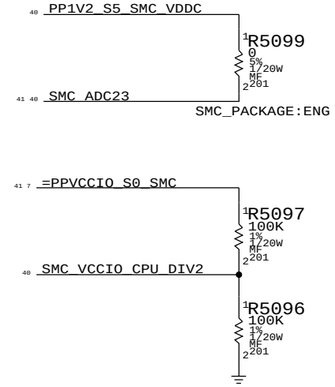


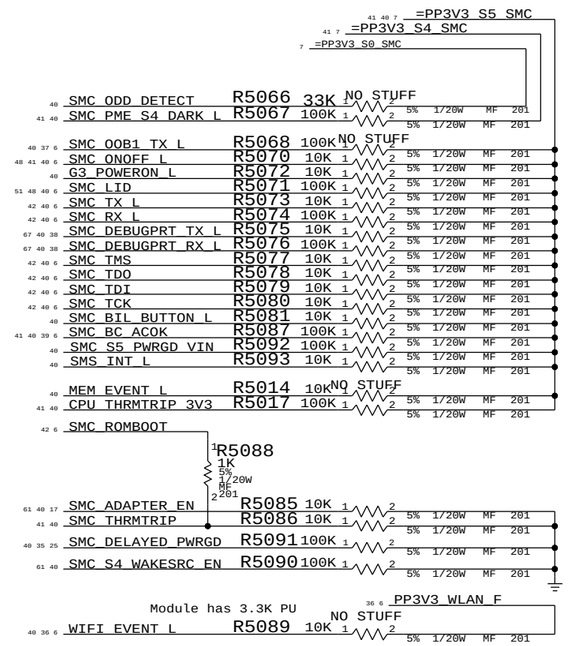
SMC12 PECI Support



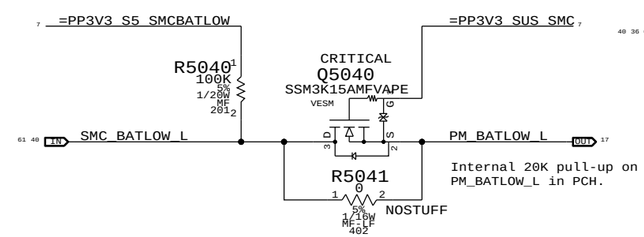
SMC12 Eng Pkg Support

Eng Package requires 1.2V ON SMC_ADC23 pin.





BATLOW# Isolation



Internal 20K pull-up on PM_BATLOW_L in PCH.

SYNC MASTER=J13_MLB	SYNC DATE=10/06/2011
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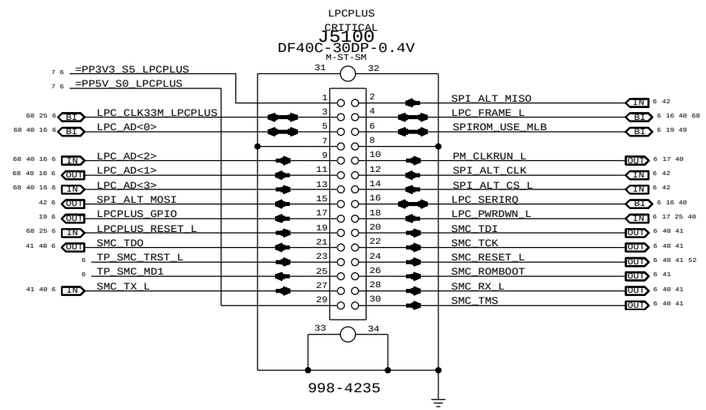
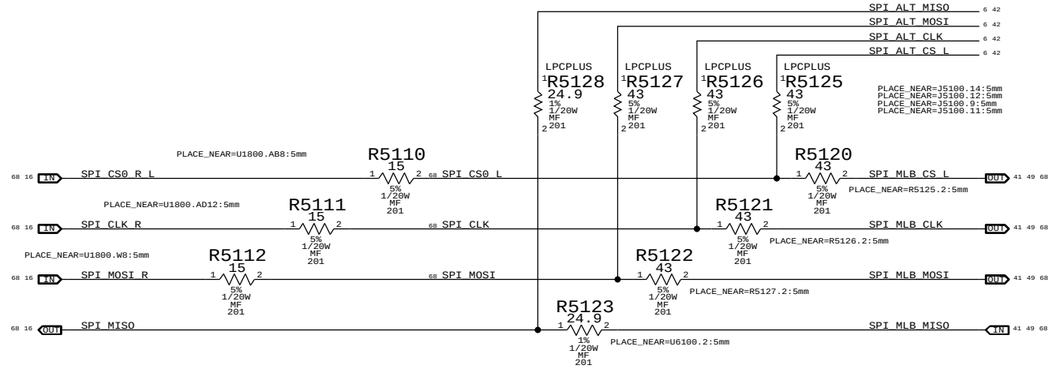
LPC+SPI Connector



SPI Bus Series Termination



SYNC MASTER=K21_MLB SYNC DATE=12/13/2010

PAGE TITLE

LPC+SPI Debug Connector

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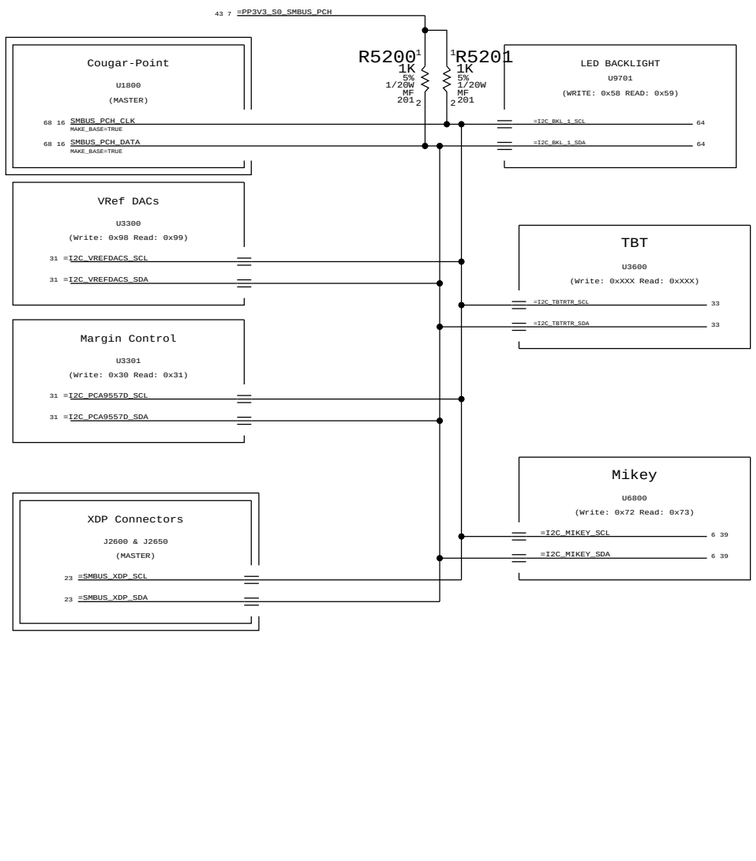
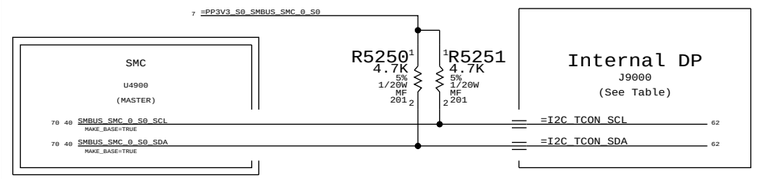
PCH S0 SMBus "0" Connections



SMC "0" SMBus S0 Connections

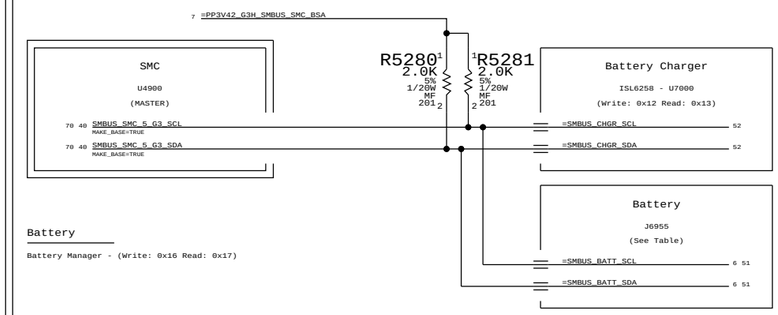


(* = Multiple options)

Internal DP

	K21		K78		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

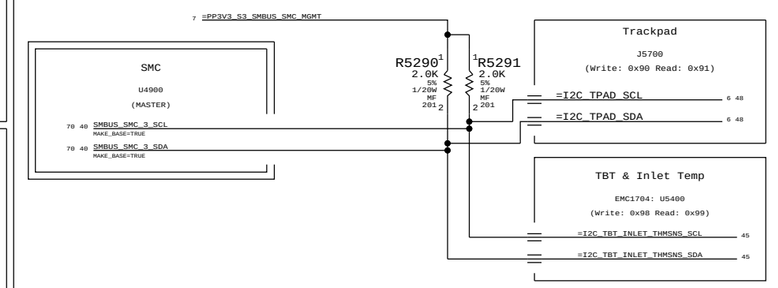
SMC "5" SMBus G3H Connections



Battery

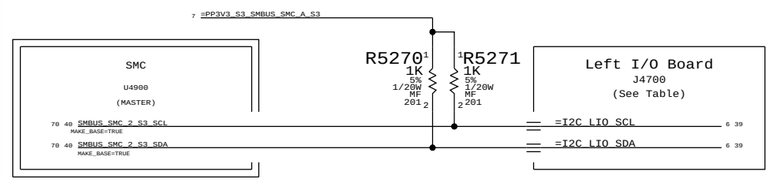
Battery Manager - (Write: 0x16 Read: 0x17)

SMC "3" SMBus S3 Connections



SMC "2" SMBus S3 Connections

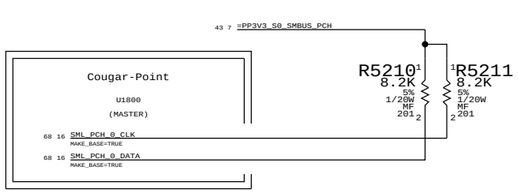
NOTE: SMC RMT bus remains powered and may be active in S3 state



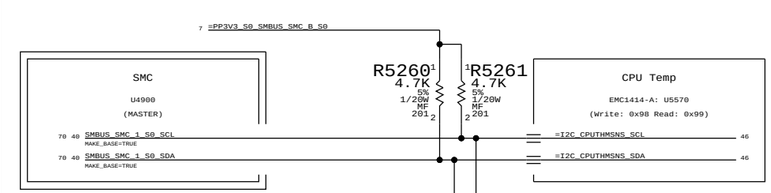
Left I/O Board

ALS - (write: 0x72 Read: 0x73)
Finstack Temp - (Write: 0x92 Read: 0x93)

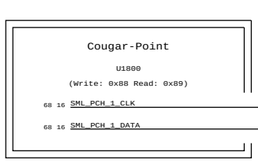
PCH S0 "SMLink 0" Connections



SMC S0 "1" SMBus Connections



PCH S0 "SMLink 1" Connections



SMLink 1 is slave port to access PCH

SYNC_MASTER=J13_MLB SYNC_DATE=10/05/2011

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SMBus Connections

Apple Inc.

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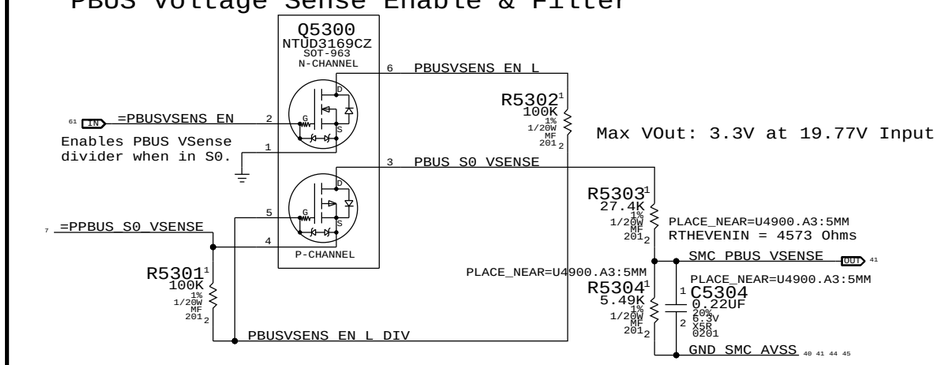
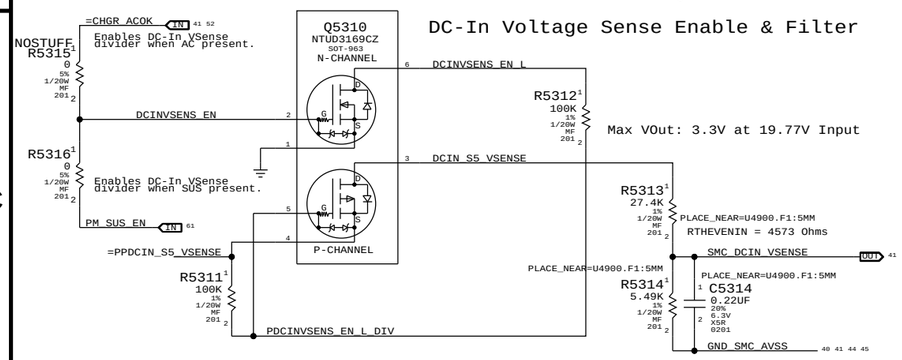
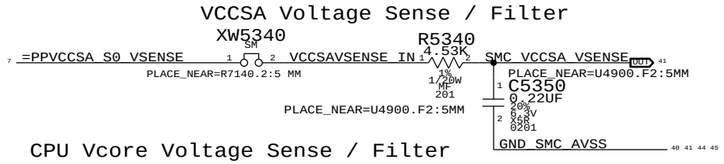
PBUS Voltage Sense Enable & Filter



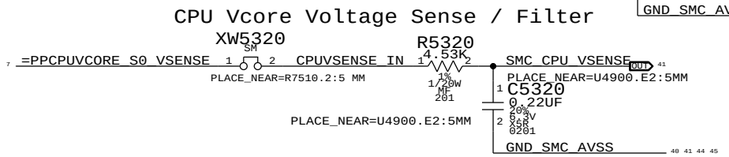
DC-In Voltage Sense Enable & Filter



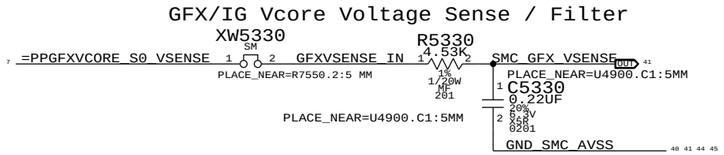
VCCSA Voltage Sense / Filter



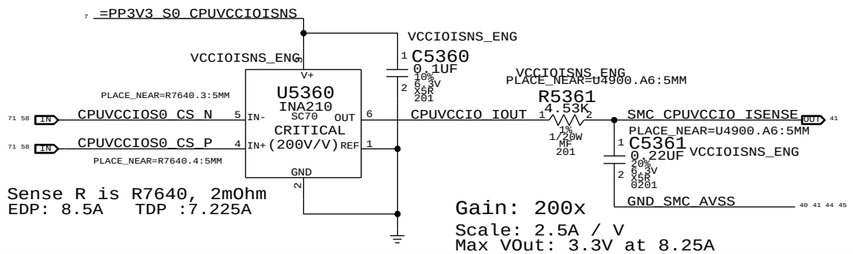
CPU Vcore Voltage Sense / Filter



GFX/IG Vcore Voltage Sense / Filter



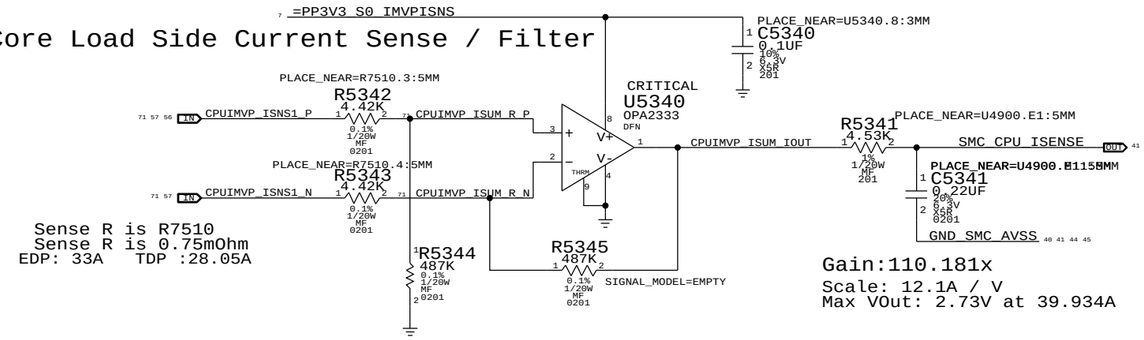
CPU 1.05V VCCIO Current Sense / Filter



Sense R is R7640, 2mOhm
EDP: 8.5A TDP :7.225A

Gain: 200x
Scale: 2.5A / V
Max VOut: 3.3V at 8.25A

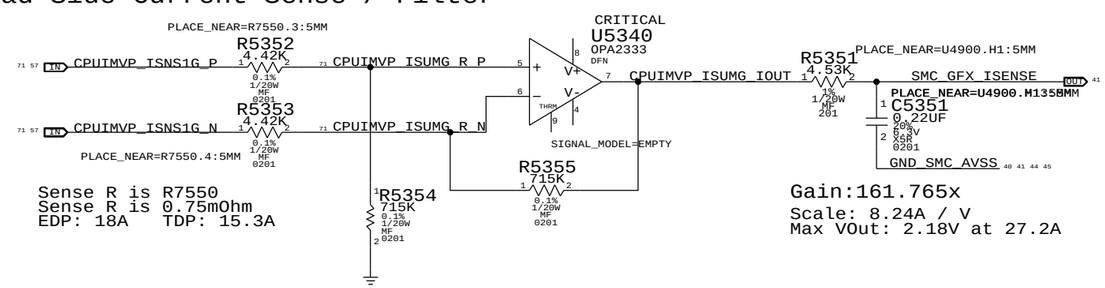
CPU VCore Load Side Current Sense / Filter



Sense R is R7510
Sense R is 0.75mOhm
EDP: 33A TDP :28.05A

Gain:110.181x
Scale: 12.1A / V
Max VOut: 2.73V at 39.934A

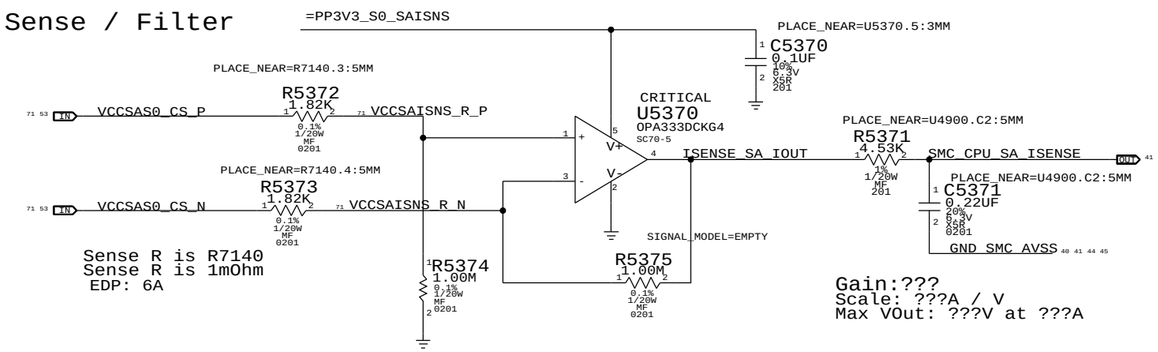
GFX/IG VCore Load Side Current Sense / Filter



Sense R is R7550
Sense R is 0.75mOhm
EDP: 18A TDP: 15.3A

Gain:161.765x
Scale: 8.24A / V
Max VOut: 2.18V at 27.2A

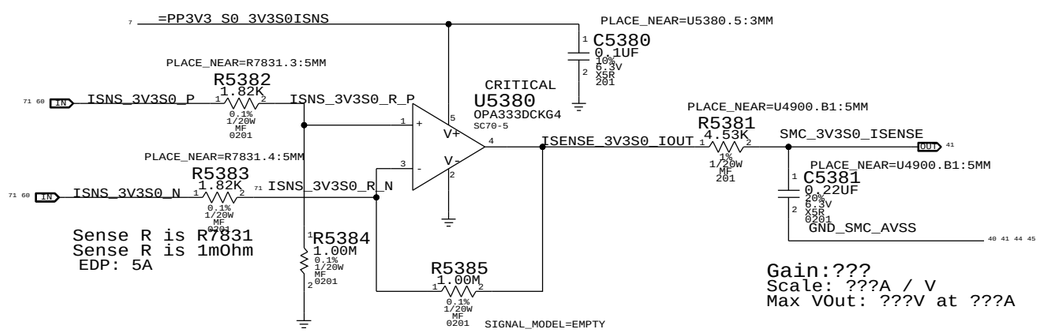
CPU SA Current Sense / Filter



Sense R is R7140
Sense R is 1mOhm
EDP: 6A

Gain:???
Scale: ???A / V
Max VOut: ???V at ???A

3.3V S0 FET Current Sense / Filter



Sense R is R7831
Sense R is 1mOhm
EDP: 5A

Gain:???
Scale: ???A / V
Max VOut: ???V at ???A

SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE
Voltage & Load Side Current Sensing

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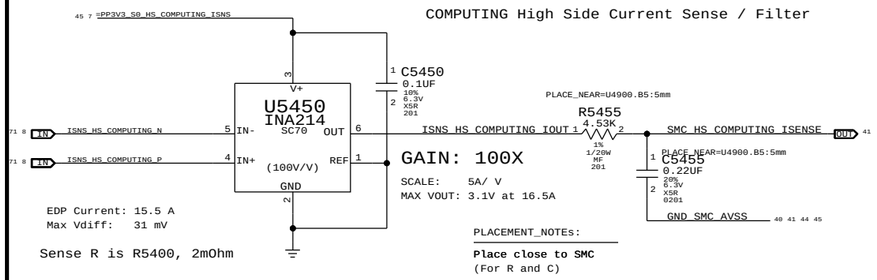
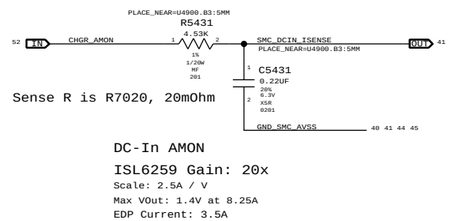
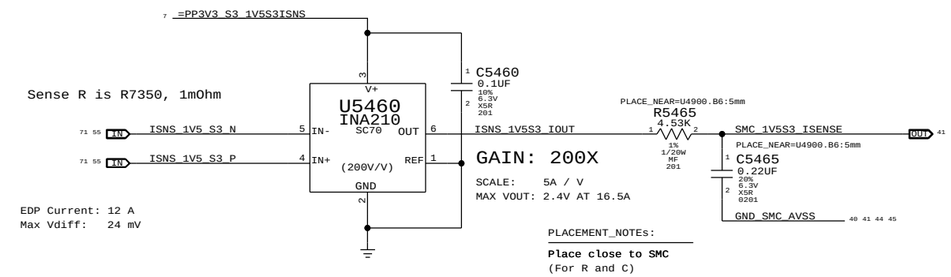
COMPUTING High Side Current Sense / Filter



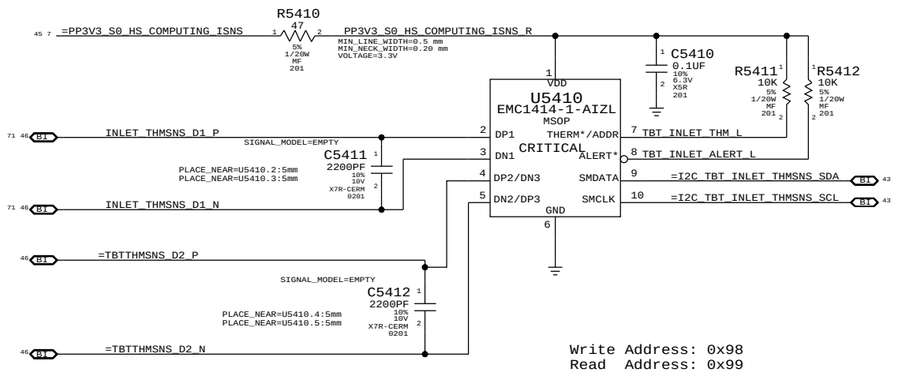
DC-IN (AMON) Current Sense Filter



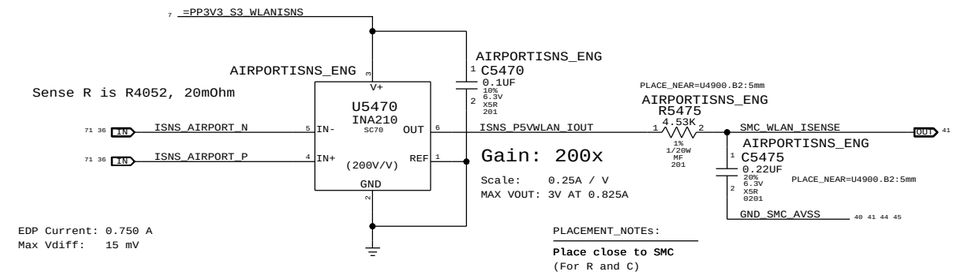
DDR3 1V5R1V35 Current Sense / Filter



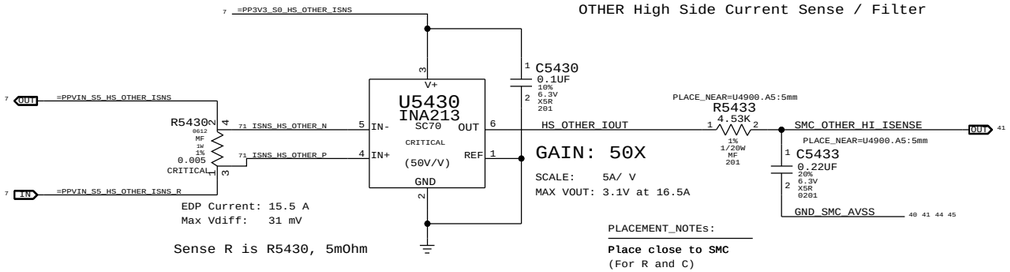
TBT/Inlet Temp Sensor



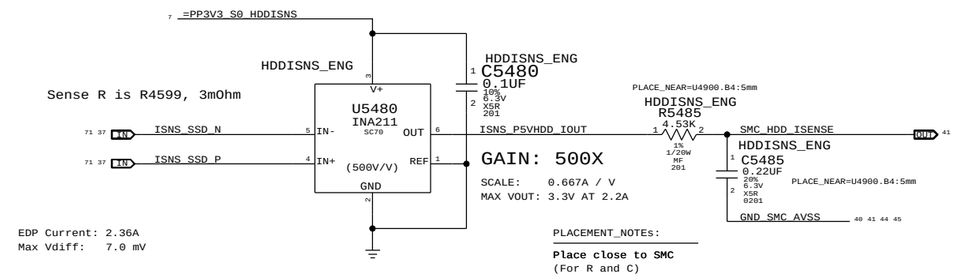
AirPort Current Sense / Filter



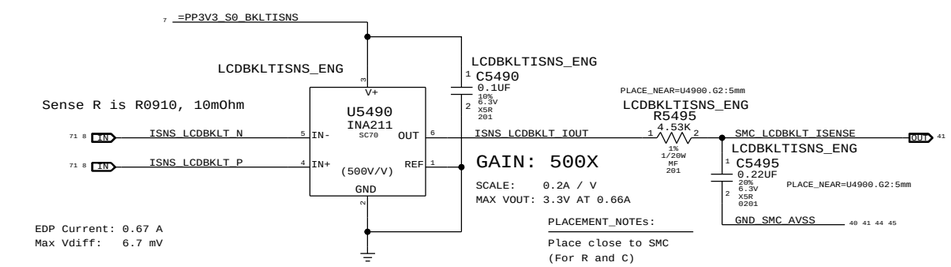
OTHER High Side Current Sense / Filter



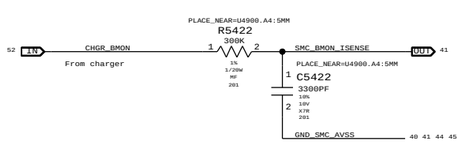
HDD Current Sense / Filter



LCD Backlight Driver Input Current Sense / Filter



CHARGER BMON High Side (BATTERY DISCHAEGE) Current Sense, MUX & Filter



Charger BMON (Production) Solution

ISL6259 Gain: 36x

Scale: 2.78A / V

Max VOut: 3.3V at 9.167A

EDP Current: 310A

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PAGE TITLE: High Side Current Sensing	
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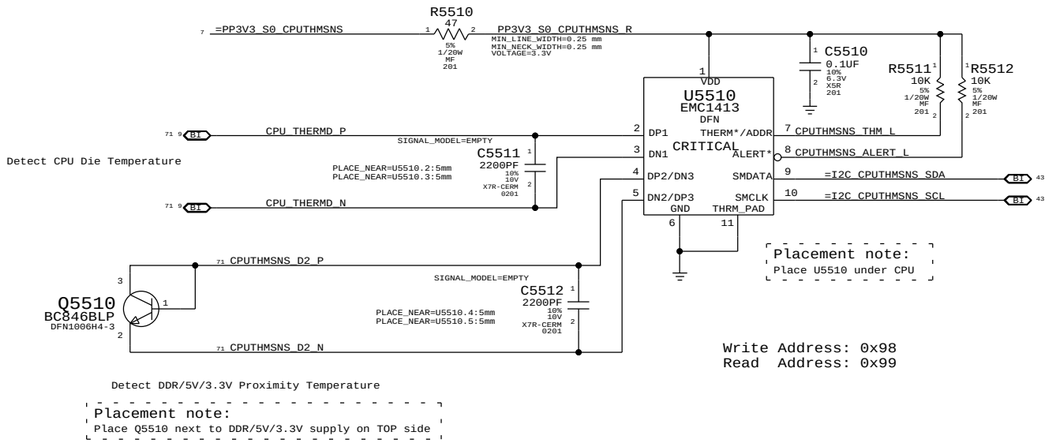
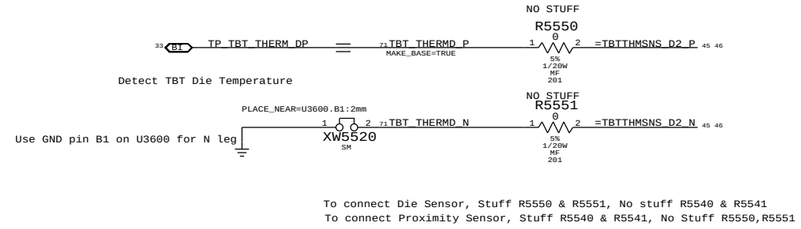
CPU Proximity Sensor



Write Address: 0x98
Read Address: 0x99

TBT Die

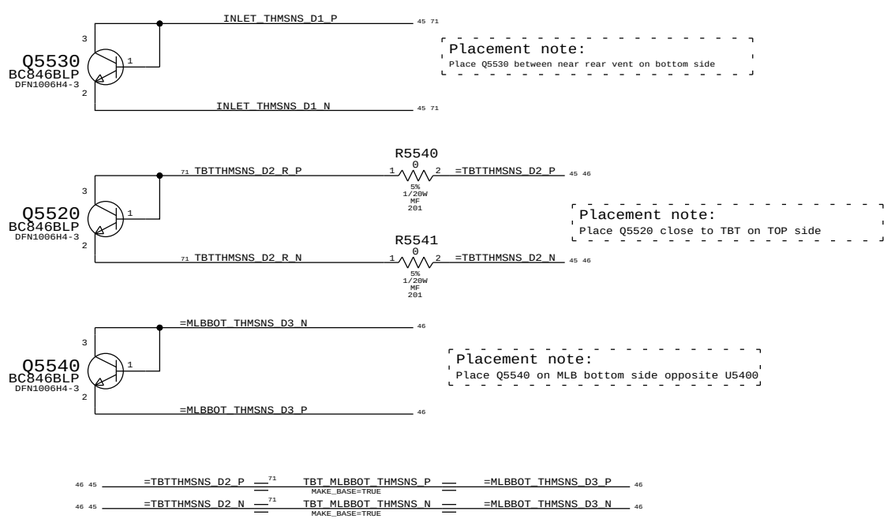


To connect Die Sensor, Stuff R5550 & R5551, No stuff R5540 & R5541
To connect Proximity Sensor, Stuff R5540 & R5541, No Stuff R5550,R5551

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors



SYNC_MASTER=J13_MLB SYNC_DATE=08/30/2011

PAGE TITLE
Thermal Sensors

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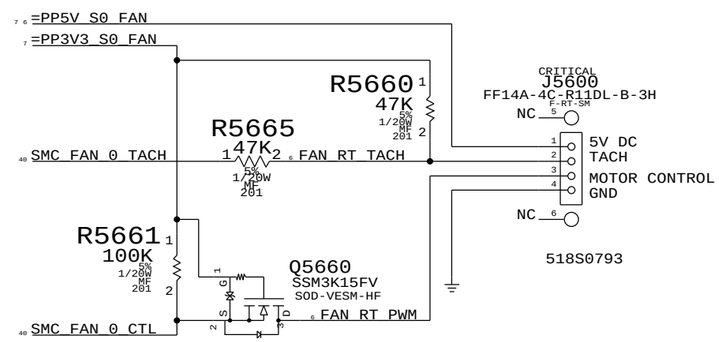
FAN CONNECTOR



SYNC MASTER=K21_MLB SYNC DATE=12/13/2010

PAGE TITLE
Fan

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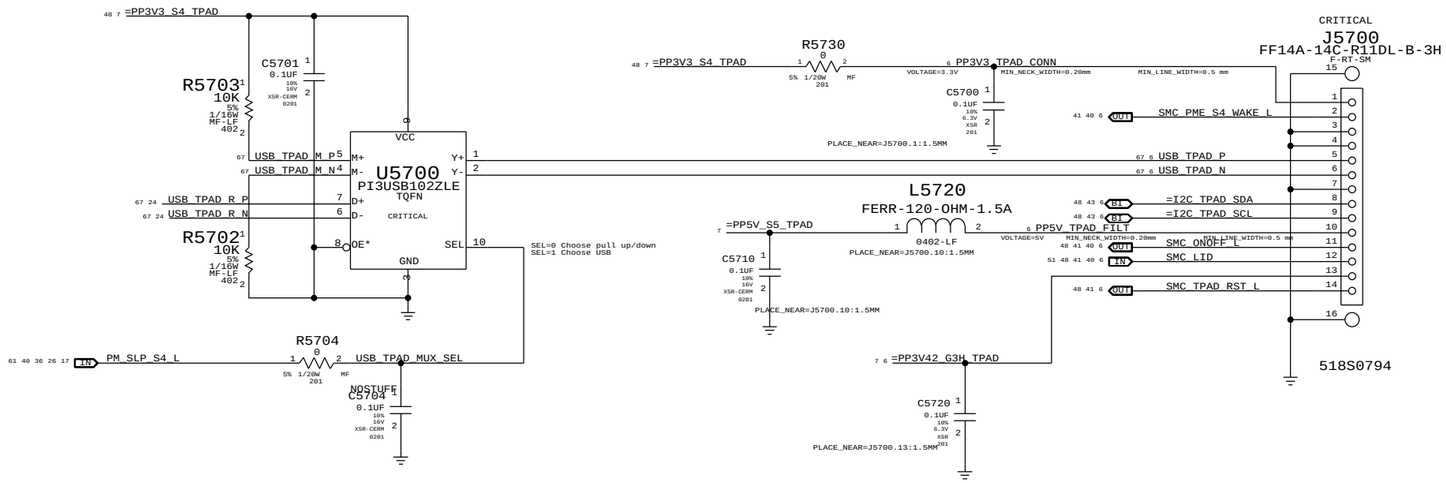
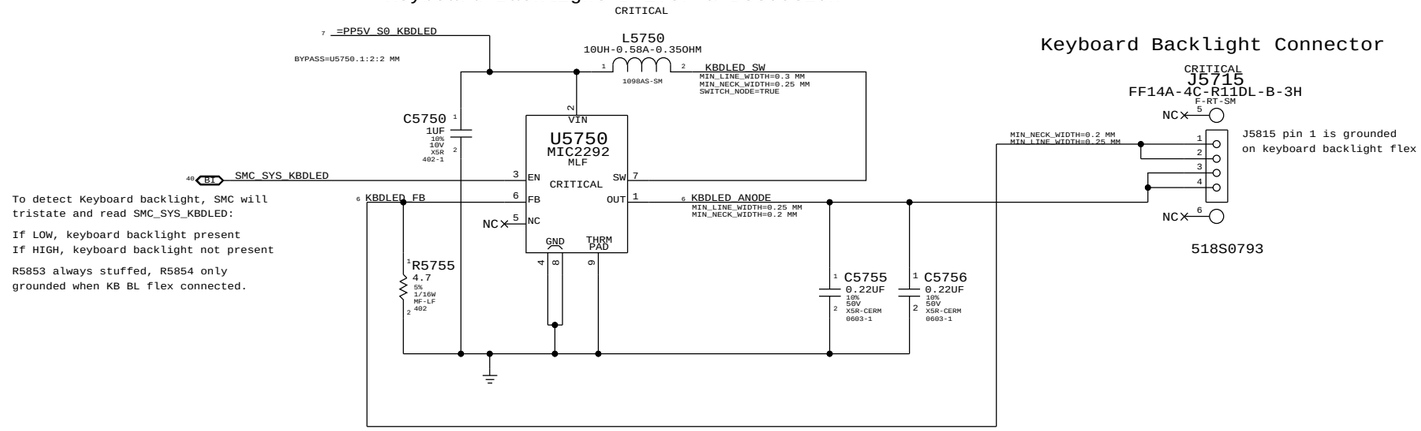
IPD Flex Connector



Keyboard Backlight Driver & Detection



To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

SYNC_MASTER=K21_MLB	SYNC_DATE=12/13/2010
PAGE TITLE: IPD / KBD Backlight	
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	REVISION: 2.7.0
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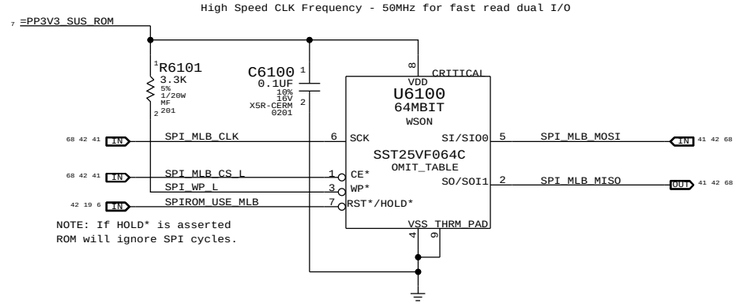
DUAL I/O MODE (MODE 0 & 3) SUPPORTED
High Speed CLK Frequency - 50MHz for fast read dual I/O



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles.

SYNC_MASTER=J13_MLB SYNC_DATE=10/13/2011

PAGE TITLE
SPI ROM

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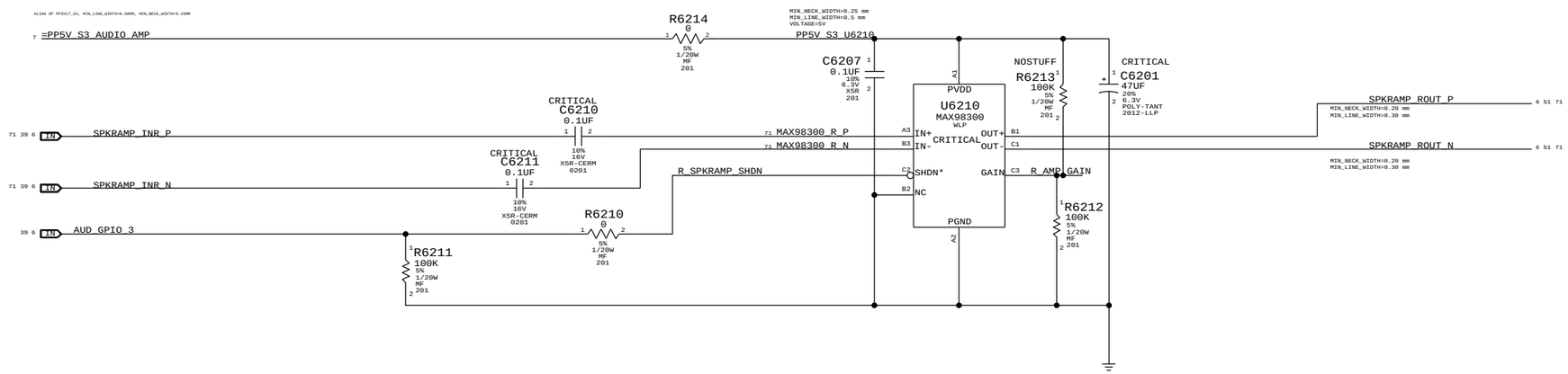
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

AUDI0: SPEAKER AMP

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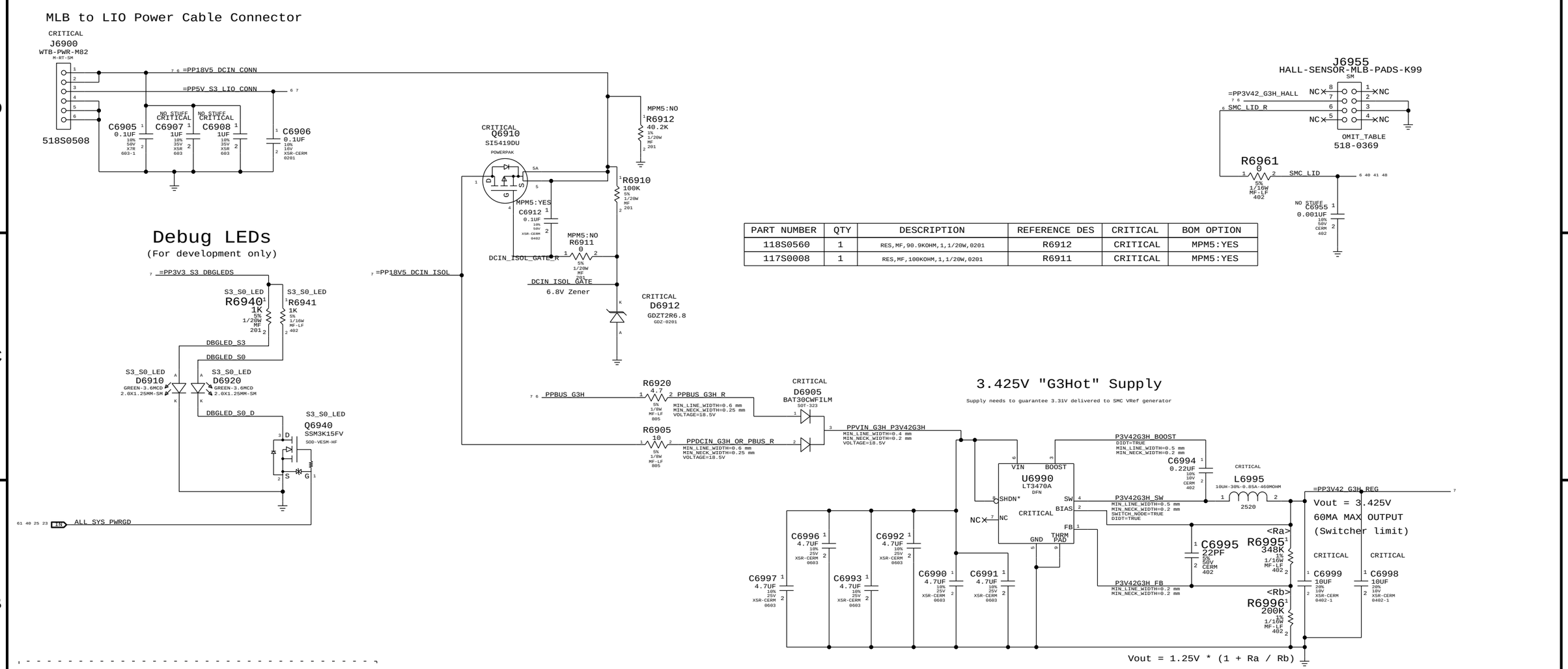

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0560	1	RES,MF,90.9KOHM,1,1/20W,0201	R6912	CRITICAL	MPM5:YES
117S0008	1	RES,MF,100KOHM,1,1/20W,0201	R6911	CRITICAL	MPM5:YES

SYNC_MASTER=K21_MLB SYNC_DATE=11/11/2011

PAGE TITLE

DC-In & Battery Connectors

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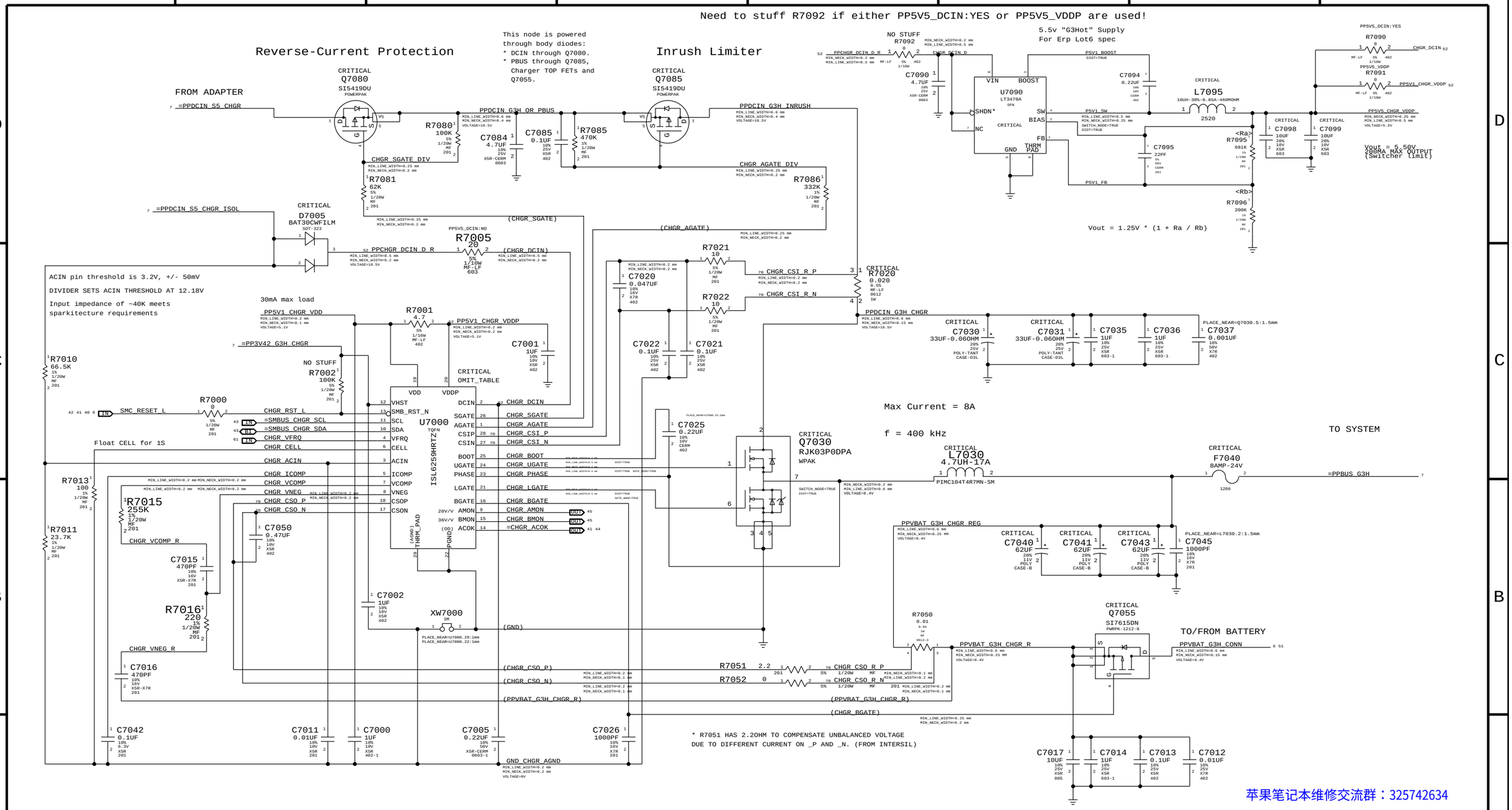

SYNC MASTER=J13 MLB	SYNC DATE=10/10/2013
PAGE TITLE: PBus Supply & Battery Charger	
Apple Inc.	DRAWING NUMBER: 051-9276 SIZE: D
	REVISION: 2.7.0
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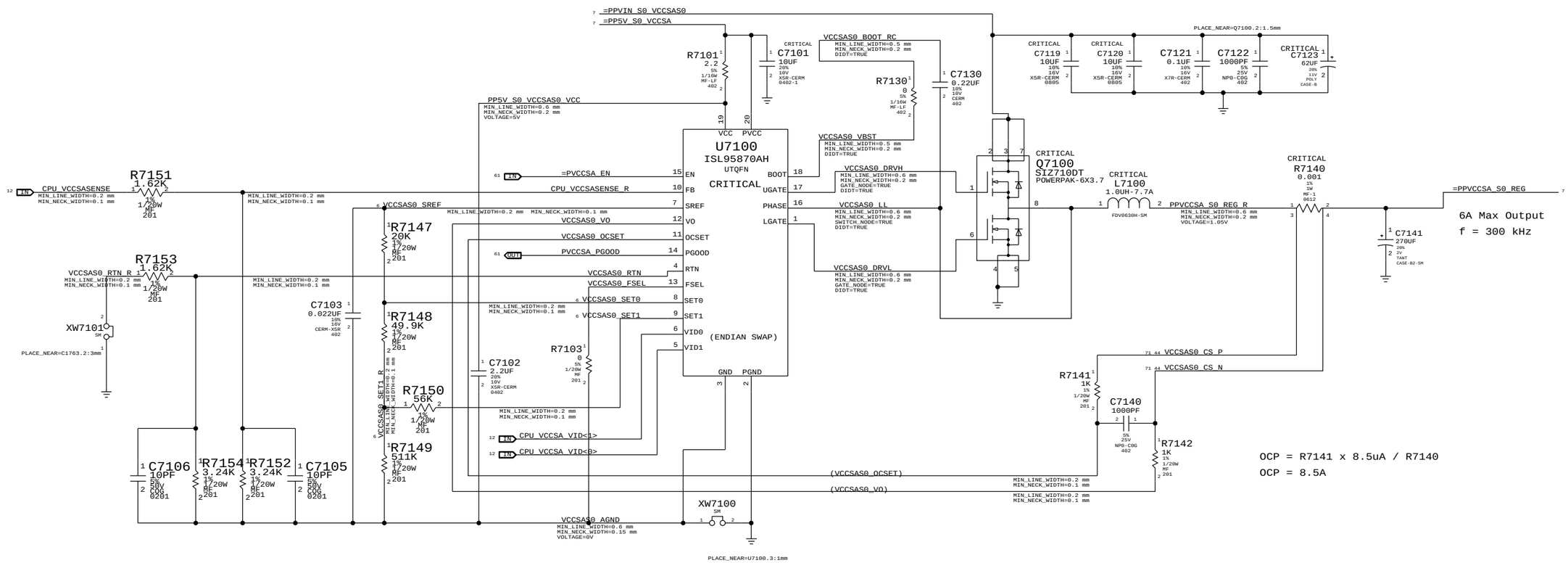

OCP = R7141 x 8.5uA / R7140

OCP = 8.5A

INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC MASTER=J13_MLB SYNC DATE=09/01/2013

PAGE TITLE

System Agent Supply

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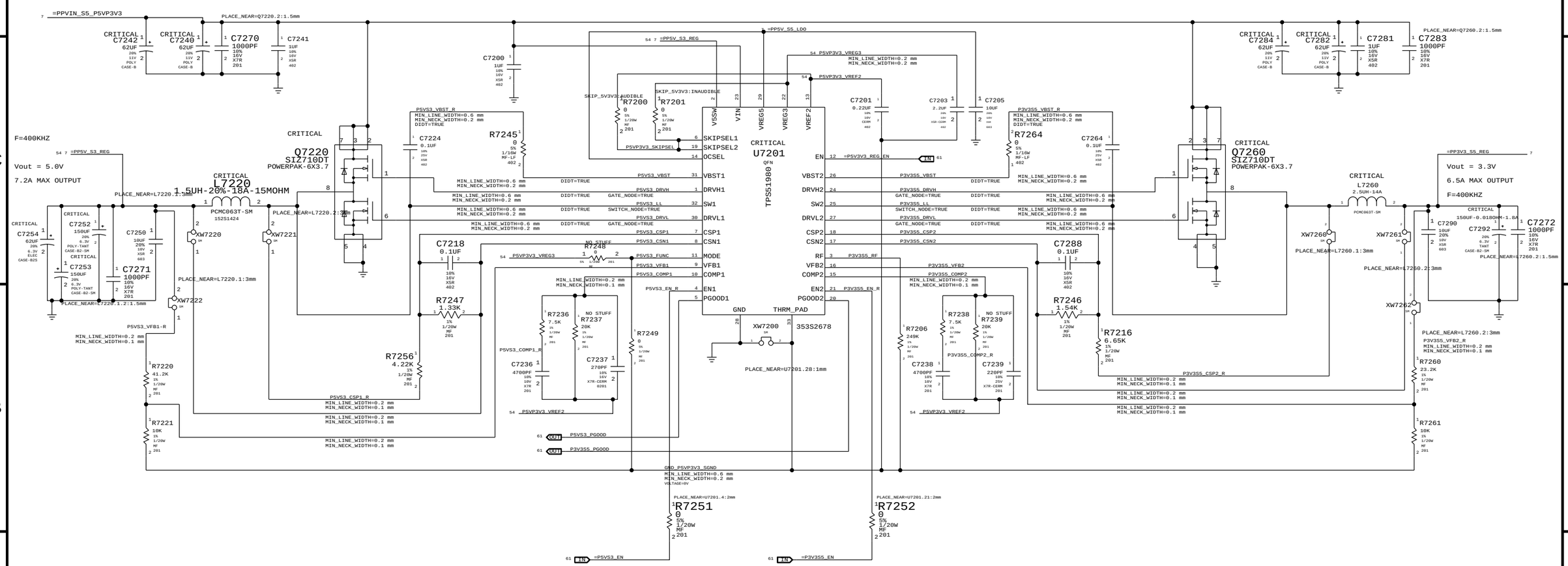

SYNC MASTER=J13_MLB	SYNC DATE=11/18/2013
PAGE TITLE: 5V / 3.3V Power Supply	
Apple Inc.	DRAWING NUMBER: 051-9276 — SIZE: D
	REVISION: 2.7.0
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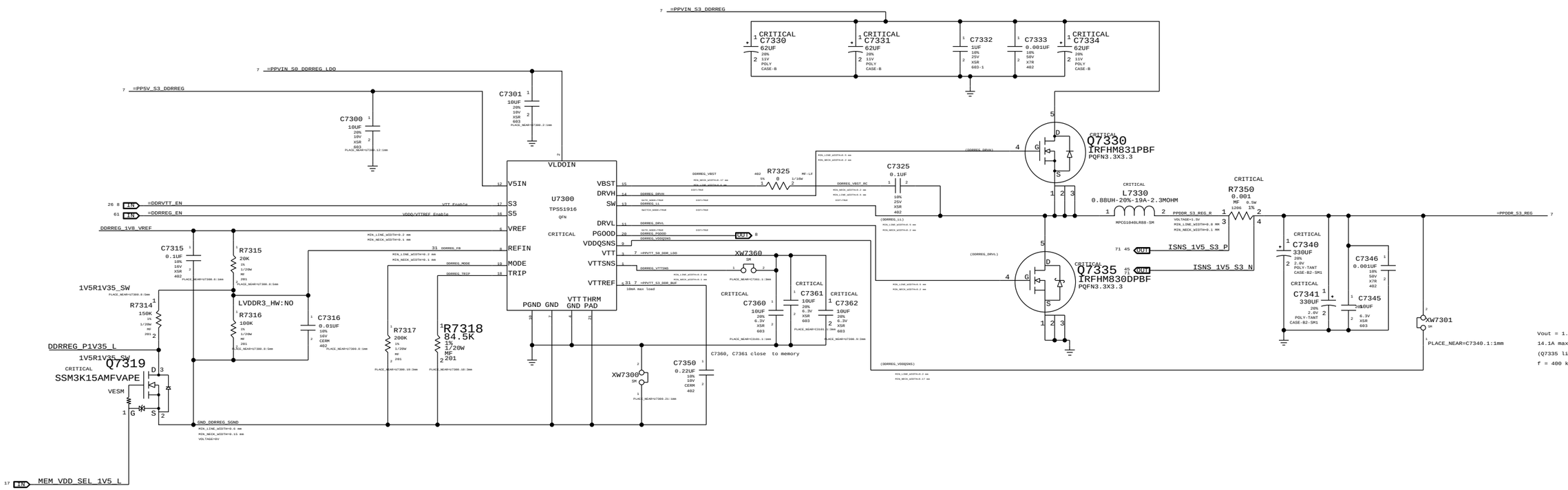

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0460	1	RES,MF,60.4KOHM,1,1/20W,0201	R7316		LVDDR3_HW:YES

If LVDDR3_HW:NO is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35_SW is turned ON

SYNC_MASTER=J13_MLB SYNC_DATE=10/07/2013

PAGE TITLE

1.5V DDR3 Supply

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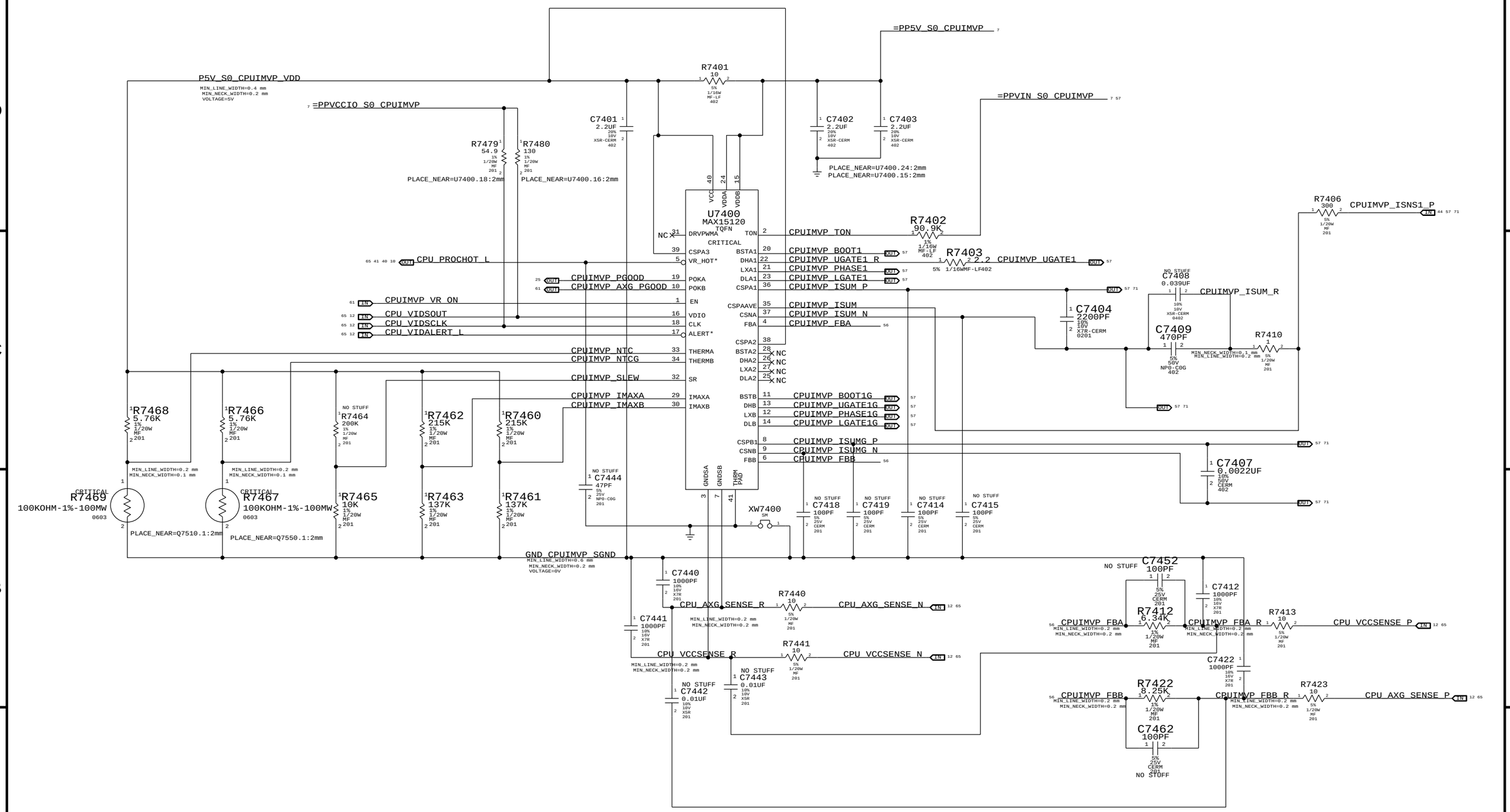

SYNC_MASTER=J13_MLB SYNC_DATE=09/22/2013

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

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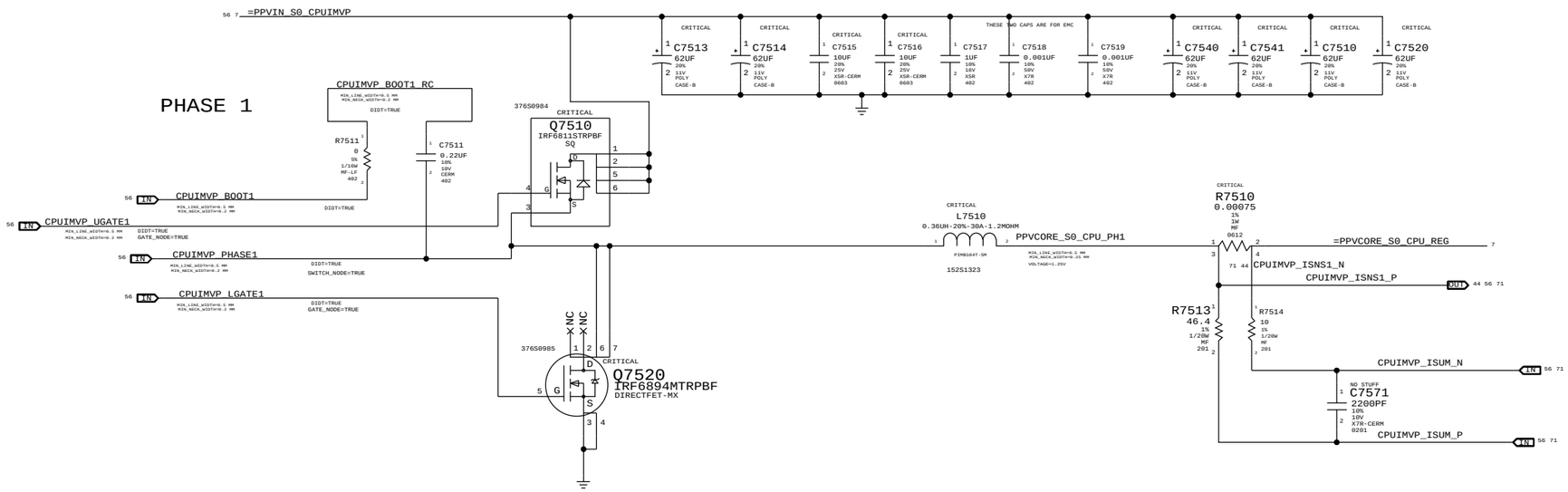
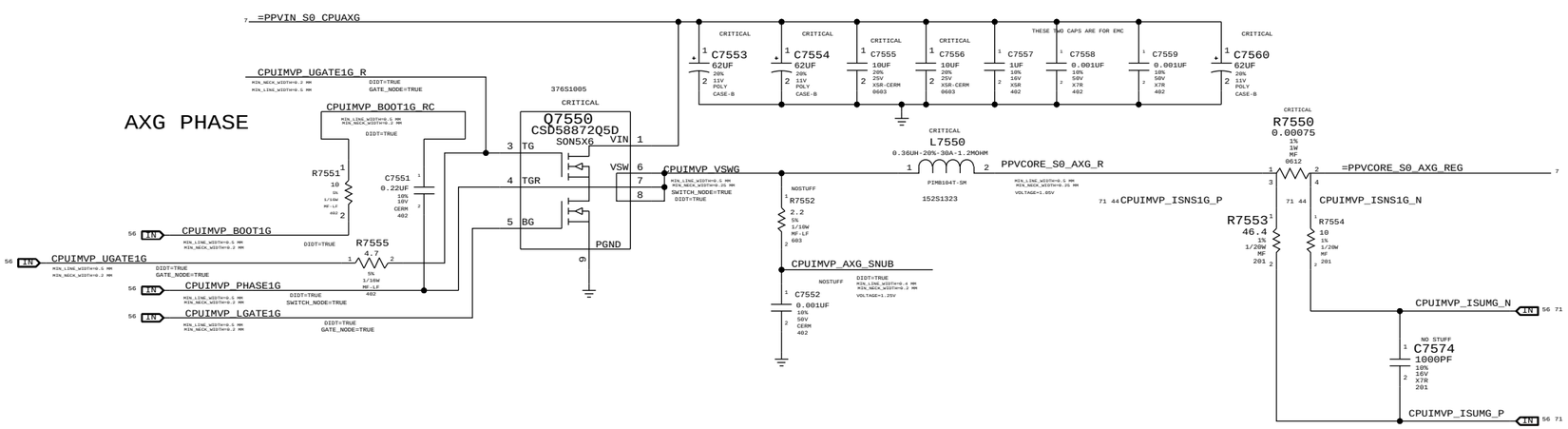
CPU=IV Bridge ULV, AXG=GT2





SYNC_MASTER=M21_MLB	SYNC_DATE=12/13/2010
PAGE TITLE	CPU IMVP7 & AXG VCore Output
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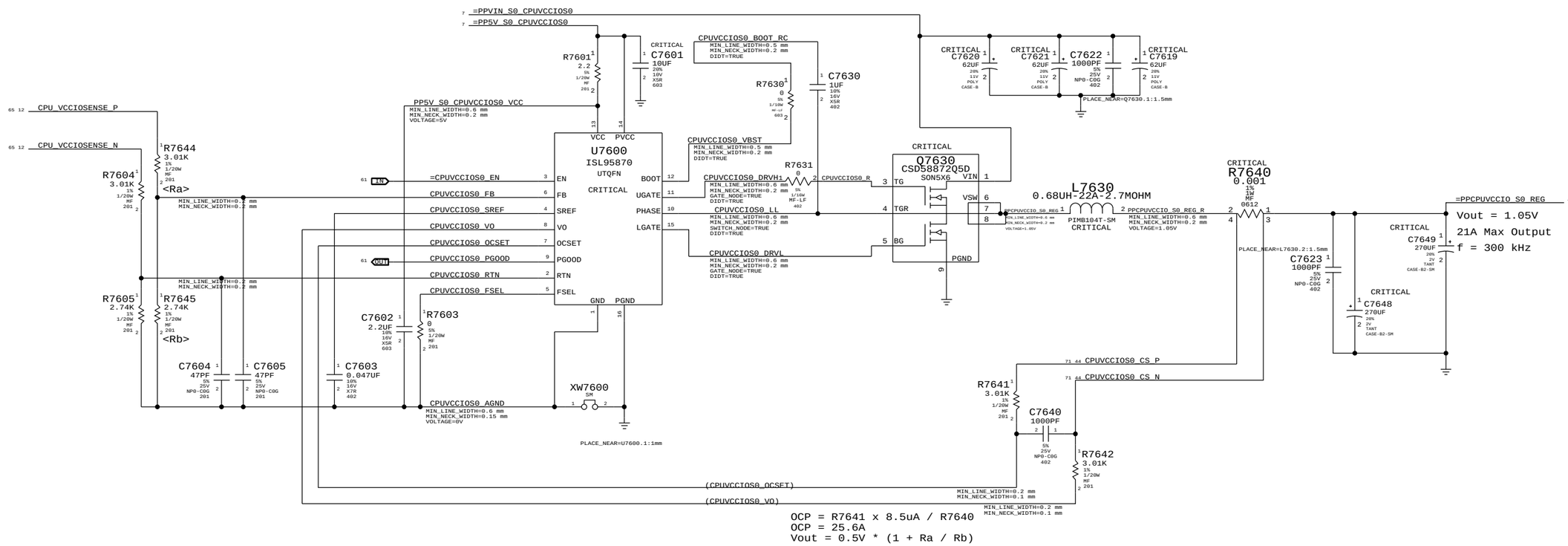
CPU VCCIO (1.05V S0) Regulator



OCP = R7641 x 8.5uA / R7640
OCP = 25.6A
Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=J13_MLB SYNC_DATE=09/01/2011

PAGE TITLE
CPU VCCIO (1.05V) Power Supply

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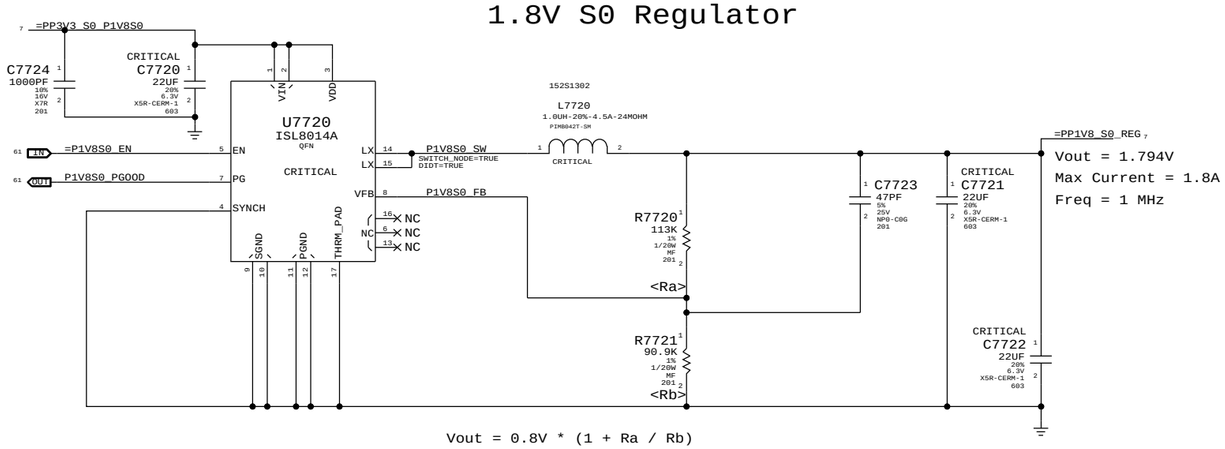
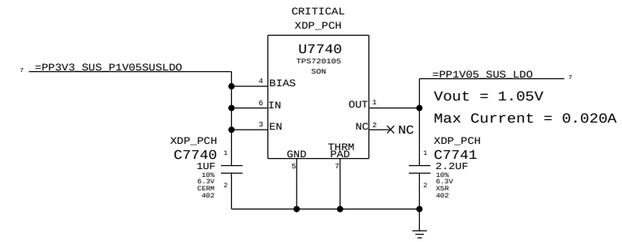
1.8V S0 Regulator



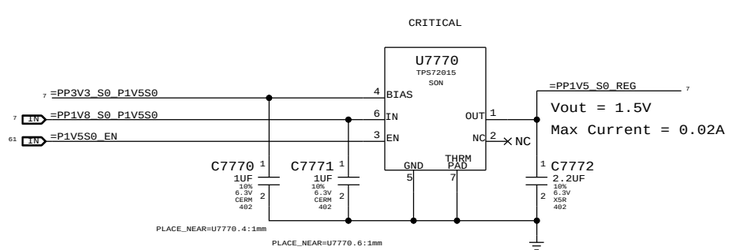
Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

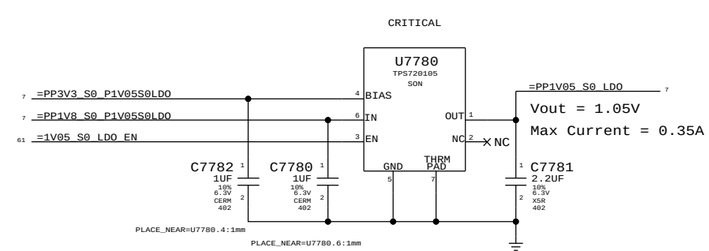
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



1.05V S0 LDO



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
Misc Power Supplies

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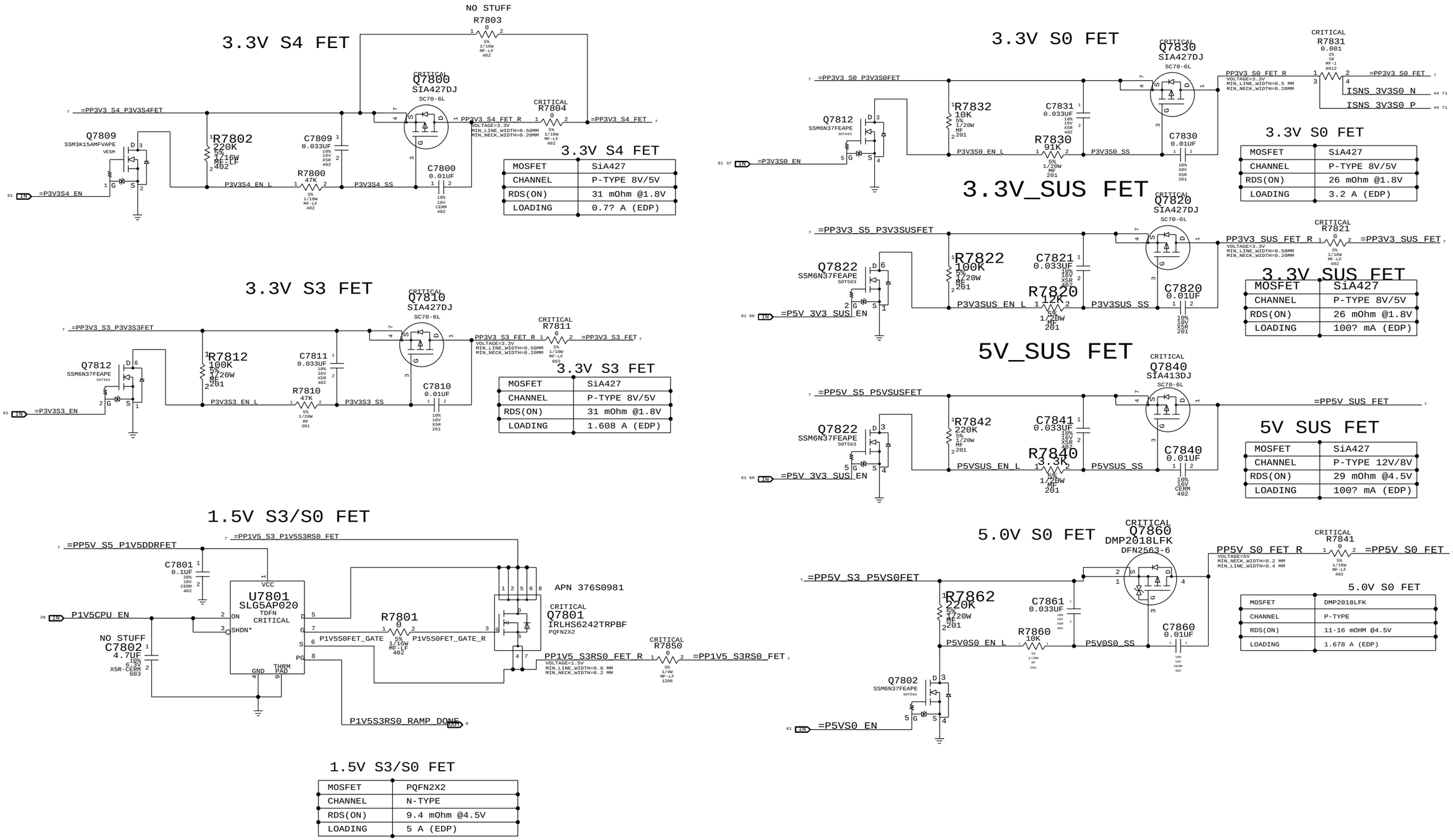

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PAGE TITLE

Power FETs

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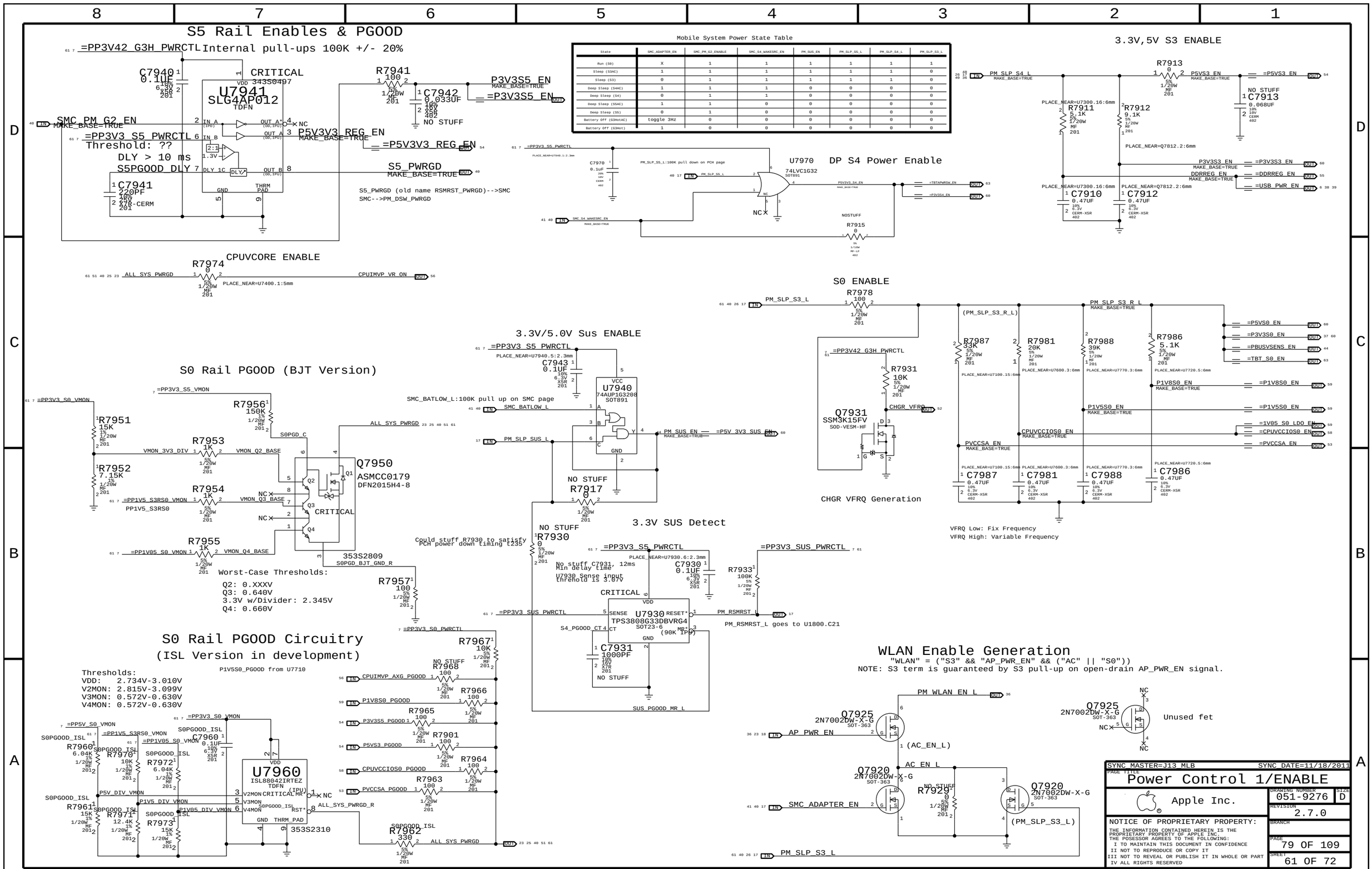
S5 Rail Enables & PGOOD
Internal pull-ups 100K +/- 20%
=PP3V42_G3H_PWRCTL
C7940 0.1UF
CRITICAL
U7941 SLG4AP012 TDFN
SMC_PM_G2_EN
MAKE_BASE=TRUE
=PP3V3_S5_PWRCTL
Threshold: ??
DLY > 10 ms
S5PGOOD_DLY
C7941 220PF
R7941 100
C7942 0.033UF
NO STUFF
P3V3S5_EN
=P3V3S5_EN
P5V3V3_REG_EN
=P5V3V3_REG_EN
S5_PWRGD
S5_PWRGD (old name RSMRST_PWRGD)-->SMC
SMC-->PM_DSW_PWRGD
Mobile System Power State Table
3.3V,5V S3 ENABLE
PM_SLP_S4_L
R7913 0
P5VS3_EN
=P5VS3_EN
NO STUFF
C7913 0.068UF
R7911 5.1K
R7912 9.1K
PLACE_NEAR=U7300.16:6mm
PLACE_NEAR=Q7812.2:6mm
P3V3S3_EN
=P3V3S3_EN
DDRREG_EN
=DDRREG_EN
=USB_PWR_EN
C7910 0.47UF
C7912 0.47UF
U7970 DP S4 Power Enable
74LVC1G32 SOT891
PM_SLP_S5_L:100K pull down on PCH page
PM_SLP_S5_L
SMC_S4_WAKESRC_EN
=PP3V3_S5_PWRCTL
C7970 0.1UF
NC
NOSTUFF
R7915 0
=TBTAPWRSW_EN
=P3V3S4_EN
CPUVCORE ENABLE
R7974 0
ALL_SYS_PWRGD
CPUIMVP_VR_ON
PLACE_NEAR=U7400.1:5mm
S0 ENABLE
R7978 100
PM_SLP_S3_L
(PM_SLP_S3_R_L)
PM_SLP_S3_R_L
MAKE_BASE=TRUE
=PP3V42_G3H_PWRCTL
R7931 10K
CHGR_VFRQ
Q7931 SSM3K15FV SOD-VESM-HF
R7987 33K
R7981 20K
R7988 39K
R7986 5.1K
=P5VS0_EN
=P3V3S0_EN
=PBUSVSENS_EN
=TBT_S0_EN
P1V8S0_EN
=P1V8S0_EN
P1V5S0_EN
=P1V5S0_EN
=1V05_S0_LDO_EN
CPUVCCIOS0_EN
=CPUVCCIOS0_EN
PVCCSA_EN
=PVCCSA_EN
C7987 0.47UF
C7981 0.47UF
C7988 0.47UF
C7986 0.47UF
CHGR VFRQ Generation
VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency
3.3V/5.0V Sus ENABLE
C7943 0.1UF
VCC U7940 74AUP1G3208 SOT891
SMC_BATLOW_L:100K pull up on SMC page
SMC_BATLOW_L
PM_SLP_SUS_L
PM_SUS_EN
=P5V_3V3_SUS_EN
NO STUFF
R7917 0
S0 Rail PGOOD (BJT Version)
=PP3V3_S5_VMON
R7951 15K
R7952 7.15K
R7956 150K
R7953 1K
R7954 1K
R7955 1K
VMON_3V3_DIV
VMON_Q2_BASE
VMON_Q3_BASE
VMON_Q4_BASE
=PP1V5_S3RS0_VMON
PP1V5_S3RS0
=PP1V05_S0_VMON
S0PGD_C
ALL_SYS_PWRGD
Q7950 ASMCC0179 DFN2015H4-8
CRITICAL
353S2809
S0PGD_BJT_GND_R
R7957 100
Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V
3.3V SUS Detect
NO STUFF
R7930 0
Could stuff R7930 to satisfy PCH power down timing t235
No stuff C7931, 12ms Min delay time
U7930 Sense input threhold is 3.07V
C7930 0.1UF
R7933 100K
=PP3V3_SUS_PWRCTL
U7930 TPS3808G33DBVRG4 SOT23-6 (90K IP9)
PM_RSMRST_L
PM_RSMRST_L goes to U1800.C21
S4_PGOOD_CT
C7931 1000PF
SUS_PGOOD_MR_L
S0 Rail PGOOD Circuitry
(ISL Version in development)
Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V
P1V5S0_PGOOD from U7710
U7960 ISL88042IRTEZ TDFN
353S2310
R7967 10K
R7968 100
R7966 100
R7965 100
R7901 100
R7964 100
R7963 100
R7962 330
CPUIMVP_AXG_PGOOD
P1V8S0_PGOOD
P3V3S5_PGOOD
P5VS3_PGOOD
CPUVCCIOS0_PGOOD
PVCCSA_PGOOD
WLAN Enable Generation
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.
PM_WLAN_EN_L
Q7925 2N7002DW-X-G SOT-363
AP_PWR_EN
(AC_EN_L)
AC_EN_L
Q7920 2N7002DW-X-G
R7929 0
SMC_ADAPTER_EN
(PM_SLP_S3_L)
PM_SLP_S3_L
Unused fet
SYNC_MASTER=J13_MLB
SYNC_DATE=11/18/2011
PAGE TITLE
Power Control 1/ENABLE
Apple Inc.
DRAWING NUMBER 051-9276
SIZE D
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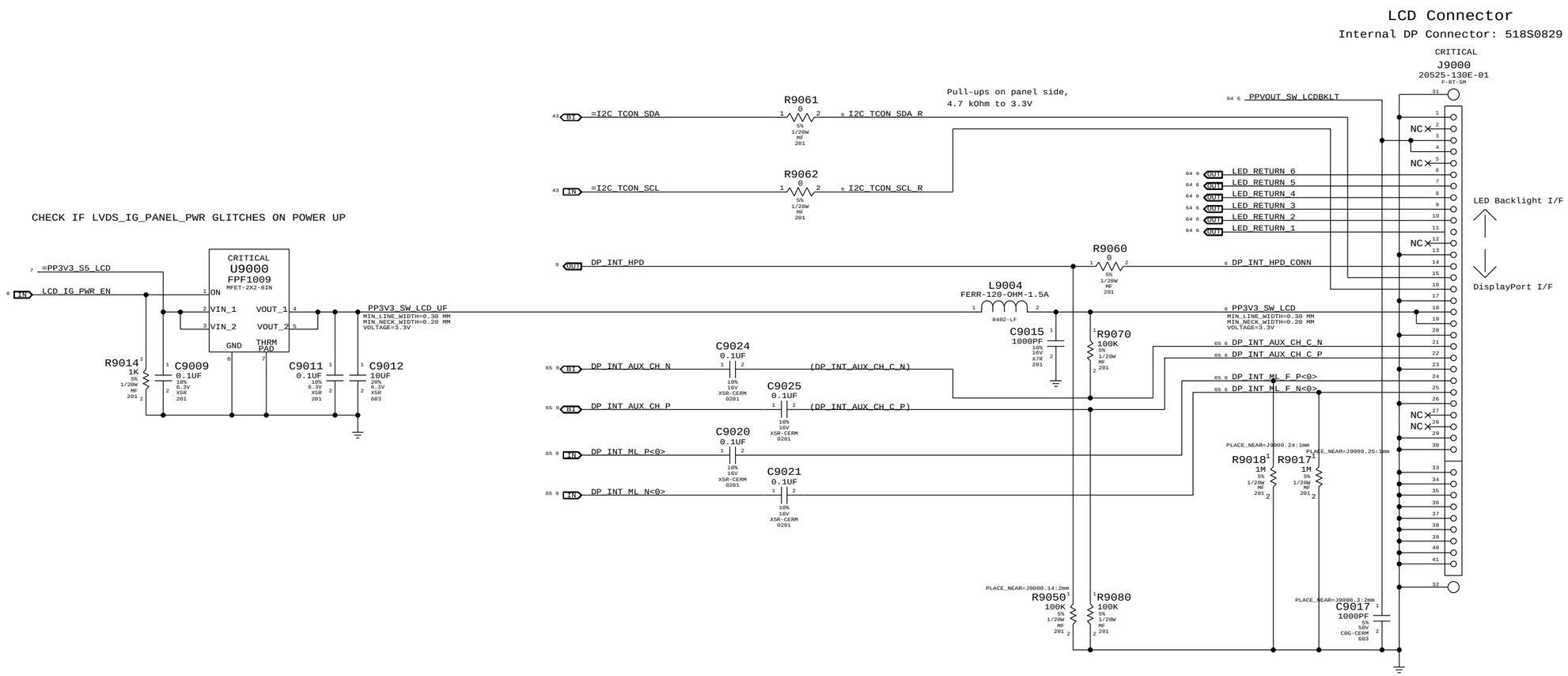

SYNC MASTER=K21_MLB SYNC DATE=12/13/2016

PAGE TITLE
Internal DisplayPort Connector

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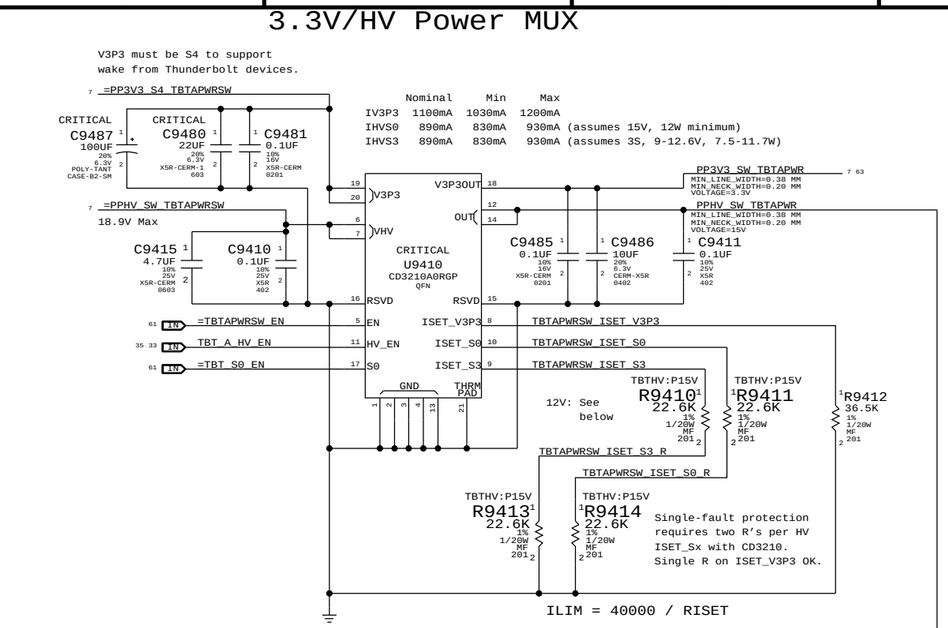
3.3V/HV Power MUX



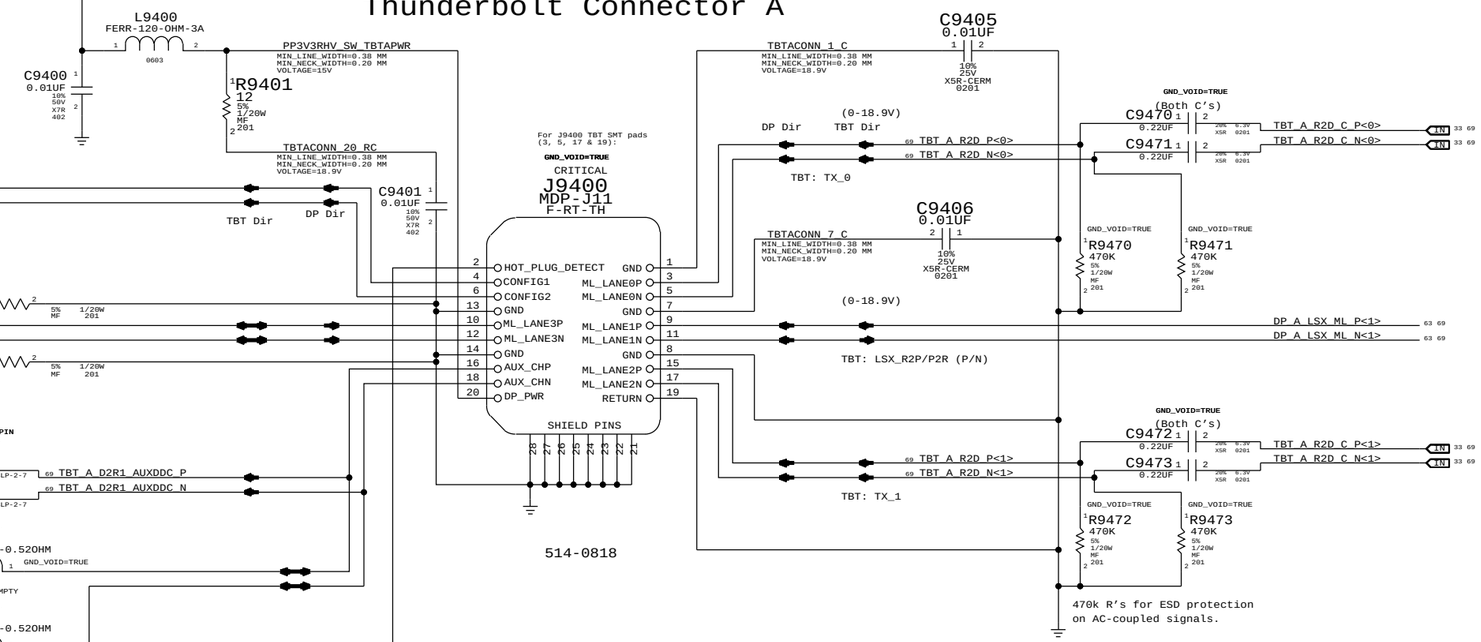
	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MF,1/20W,17.8K,1,0201	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MF,1/20W,17.8K,1,0201	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A



SYNC_MASTER=J13_MLB SYNC_DATE=11/18/2011

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

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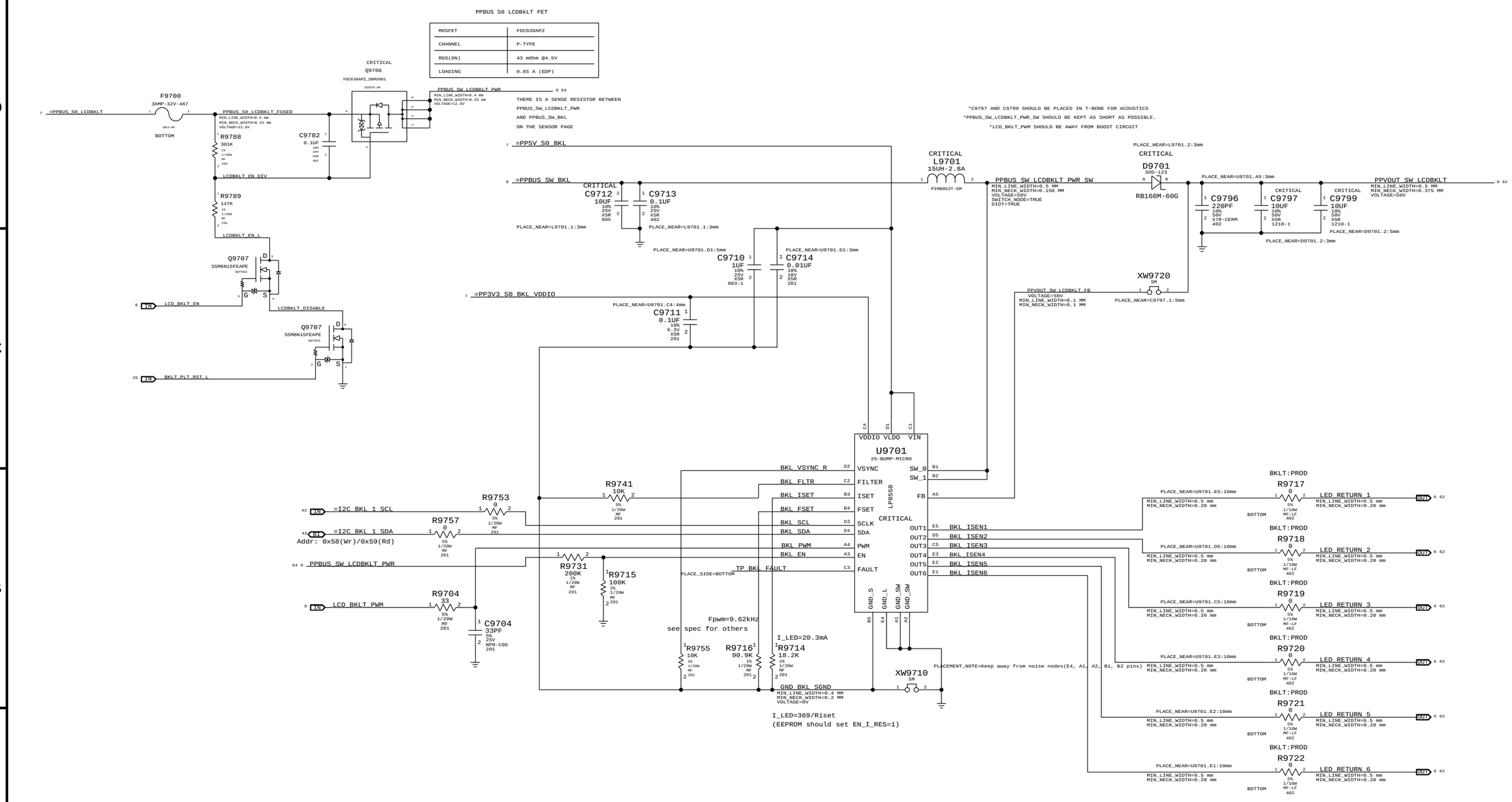

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=J13_MLB SYNC_DATE=10/13/2011

PAGE TITLE

LCD Backlight Driver

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

Note: DisplayPort tables are on Page 103

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET (NET_TYPE) PHYSICAL	SPACING		
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_P<3:0> 9 17
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_N<3:0> 9 17
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_P<3:0> 9 17
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_N<3:0> 9 17
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_P<7:0> 9 17
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_N<7:0> 9 17
	CPU_45S	CPU_AGTL	FDI_FSYNC<1..0> 9 17
	CPU_45S	CPU_AGTL	FDI_LSYNC<1..0> 9 17
	CPU_45S	CPU_AGTL	FDI_INT 9 17
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI 10 19 41
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC 10 17
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD 10 17 26
	CPU_45S	CPU_TTP	XDP_DBRESET_L 10 23 25
	CPU_45S	CPU_TTP	XDP_CPU_PRDY_L 10 23
	CPU_45S	CPU_TTP	XDP_CPU_PREQ_L 10 23
	CPU_27P4S	CPU_COMP	EDP_COMP 9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP 9
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0> 10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1> 10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2> 10
	CPU_45S	CPU_TTP	CPU_CFG<11..0> 9 23
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L 10 40
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL 12
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L 10 40 41 56
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD 10 19 23
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L 10 19 41
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P 10 16
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N 10 16
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP 8 10
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN 8 10
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P 10 16
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N 10 16
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P 16 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N 16 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N 23
XDP_TDI	CPU_45S	CPU_TTP	XDP_CPU_TDI 10 23
XDP_TDO	CPU_45S	CPU_TTP	XDP_CPU_TDO 10 23
XDP_TMS	CPU_45S	CPU_TTP	XDP_CPU_TMS 10 23
XDP_TCK	CPU_45S	CPU_TTP	XDP_CPU_TCK 10 23
XDP_TRST_L	CPU_45S	CPU_TTP	XDP_CPU_TRST_L 10 23
XDP_BPM_L	CPU_45S	CPU_TTP	XDP_BPM_L<3..0> 10 23
XDP_BPM_L_R_CFG	CPU_45S	CPU_TTP	XDP_BPM_L<7..4> 10 23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_TTP	XDP_OBSDATA_B<3..0> 23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_TTP	CPU_CFG<15..12> 9 23
(FSB_CPURST_L)	CPU_45S	CPU_TTP	XDP_CPURST_L 23
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P 12 56
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N 12 56
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P 12 58
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N 12 58
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P 12 56
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N 12 56
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P 12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N 12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P 9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N 9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P 9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N 9
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L 12 56
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK 12 56
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT 12 56
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<0> 8 37
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<0> 8 37
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_P 37
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_N 37
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<0> 8 37
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<0> 8 37
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_P 37
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_N 37
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_P<1> 8 37
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_N<1> 8 37
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<1> 6 37
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<1> 6 37
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<1> 6 8 37
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<1> 6 8 37
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<1>
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<1>
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P 6 16 37
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N 6 16 37
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0> 9 62
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0> 9 62
	DP_80D	DP_TX	DP_INT_ML_F_P<3..0> 6 62
	DP_80D	DP_TX	DP_INT_ML_F_N<3..0> 6 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P 6 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N 6 62
	DP_80D	DP_AUX	DP_INT_AUX_CH_P 9 62
	DP_80D	DP_AUX	DP_INT_AUX_CH_N 9 62

DMI/FDI

PCIe SSD

DP

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	PalPilot Spacing	"Real" Spacing
MEM_DATA2SELF	*	=2x_DIELECTRIC	?	=2x_DIELECTRIC	=2x_DIELECTRIC
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?	=5.7x_DIELECTRIC	=3x_DIELECTRIC
MEM_CMD2CMD	*	=3x_DIELECTRIC	?	=4x_DIELECTRIC	=3x_DIELECTRIC
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?	=4x_DIELECTRIC	=3x_DIELECTRIC
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?	=4x_DIELECTRIC	=3x_DIELECTRIC
MEM_CLK2CLK	*	=6x_DIELECTRIC	?	=8.6x_DIELECTRIC	=6x_DIELECTRIC
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?	=5.7x_DIELECTRIC	=4x_DIELECTRIC
MEM_2PWR	*	=PWR_P2MM	?	=PWR_P2MM	=PWR_P2MM
MEM_2GND	*	=GND_P2MM	?	=GND_P2MM	=GND_P2MM
MEM_2OTHER	*	=6x_DIELECTRIC	?	=8.6x_DIELECTRIC	=6x_DIELECTRIC

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A CKE<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A CS L<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A ODT<3..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A A<15..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A RAS L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A CAS L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A WE L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_45S	MEM_A_DATA_0	MEM A DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_45S	MEM_A_DATA_1	MEM A DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_45S	MEM_A_DATA_2	MEM A DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_45S	MEM_A_DATA_3	MEM A DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_45S	MEM_A_DATA_4	MEM A DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_45S	MEM_A_DATA_5	MEM A DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_45S	MEM_A_DATA_6	MEM A DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_45S	MEM_A_DATA_7	MEM A DQ<63..56>	11 28
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS P<0>	11 27
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS N<0>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS P<1>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS N<1>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS P<2>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS N<2>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS P<3>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS N<3>	11 27
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS P<4>	11 28
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS N<4>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS P<5>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS N<5>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS P<6>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS N<6>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS P<7>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B CKE<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B CS L<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B ODT<3..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B A<15..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B RAS L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B CAS L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B WE L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_45S	MEM_B_DATA_0	MEM B DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_45S	MEM_B_DATA_1	MEM B DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_45S	MEM_B_DATA_2	MEM B DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_45S	MEM_B_DATA_3	MEM B DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_45S	MEM_B_DATA_4	MEM B DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_45S	MEM_B_DATA_5	MEM B DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_45S	MEM_B_DATA_6	MEM B DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_45S	MEM_B_DATA_7	MEM B DQ<63..56>	11 30
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS P<0>	11 29
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS N<0>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS P<1>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS N<1>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS P<2>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS N<2>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS P<3>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS N<3>	11 29
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS P<4>	11 30
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS N<4>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS P<5>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS N<5>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS P<6>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS N<6>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS P<7>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS N<7>	11 30
		MEM_PWR	PP1V5_S3RS0	6 7
		MEM_PWR	PP1V5_S3	6 7
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	27 28 31
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	27 28 31

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	SATA3_PCH_TX	*	SATA3_TX2TX
SATA3_PCH_RX	SATA3_PCH_RX	*	SATA3_RX2RX
SATA3_PCH_TX	*_PCH_TX	*	SATA3_TX2OTHERTX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_RX2OTHERRX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_TX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_RX2TX
SATA3_PCH_TX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*	*	SATA3_2OTHER
SATA3_PCH_RX	*	*	SATA3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	*	=2.5x_DIELECTRIC	?
SATA3_RX2RX	*	=2.5x_DIELECTRIC	?
SATA3_TX2OTHERTX	*	=4x_DIELECTRIC	?
SATA3_RX2OTHERRX	*	=4x_DIELECTRIC	?
SATA3_TX2RX	*	=6x_DIELECTRIC	?
SATA3_RX2TX	*	=6x_DIELECTRIC	?
SATA3_2OTHERHS	*	=4x_DIELECTRIC	?
SATA3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_P	16 37
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_N	16 37
	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_P	37
	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_N	37
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_P	6 37
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_N	6 37
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_P	16 37
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_N	16 37
	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_P	37
	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_N	37
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_P	6 37
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_N	6 37
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	18 24
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	18 24
USB_BT	USB_80D	USB	USB_BT_P	24 36
USB_BT	USB_80D	USB	USB_BT_N	24 36
	USB_80D	USB	USB_BT_CONN_P	6 36
	USB_80D	USB	USB_BT_CONN_N	6 36
	USB_80D	USB	USB_BT_WAKE_P	36
	USB_80D	USB	USB_BT_WAKE_N	36
USB_TPAD	USB_80D	USB	USB_TPAD_P	6 48
USB_TPAD	USB_80D	USB	USB_TPAD_N	6 48
	USB_80D	USB	USB_TPAD_CONN_P	
	USB_80D	USB	USB_TPAD_CONN_N	
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_P	24
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_N	24
	USB_80D	USB	USB_TPAD_R_P	24 48
	USB_80D	USB	USB_TPAD_R_N	24 48
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	48
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	48
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	8 24
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	8 24
USB_SMC	USB_80D	USB	USB_SMC_P	24 40
USB_SMC	USB_80D	USB	USB_SMC_N	24 40
USB_CAMERA	USB_80D	USB	USB_CAMERA_P	6 18 39
USB_CAMERA	USB_80D	USB	USB_CAMERA_N	6 18 39
USB_EXTA	USB_80D	USB	USB_EXTA_P	18 38
USB_EXTA	USB_80D	USB	USB_EXTA_N	18 38
	UART_45S	UART	SMC_DEBUGPRT_TX_L	38 40 41
	UART_45S	UART	SMC_DEBUGPRT_RX_L	38 40 41
	USB_80D	USB	USB2_EXTA_MUXED_P	38
	USB_80D	USB	USB2_EXTA_MUXED_N	38
	USB_80D	USB	USB2_EXTA_MUXED_F_P	38
	USB_80D	USB	USB2_EXTA_MUXED_F_N	38
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_P	18 38
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_N	18 38
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_P	18 38
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_N	18 38
	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_F_P	38
	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_F_N	38
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_F_P	38
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_F_N	38
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_C_P	38
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_C_N	38
USB_EXTB	USB_80D	USB	USB_EXTB_P	6 24 39
USB_EXTB	USB_80D	USB	USB_EXTB_N	6 24 39
	USB_80D	USB	USB_EXTB_EHCI_P	18 24
	USB_80D	USB	USB_EXTB_EHCI_N	18 24
	USB_80D	USB	USB_EXTB_XHCI_P	18 24
	USB_80D	USB	USB_EXTB_XHCI_N	18 24
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_P	18 39
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_N	18 39
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_P	6 39
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_N	6 39
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_P	
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_N	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_P	18 39
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_N	18 39
	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_P	6 39
	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_N	6 39
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_P	18 24
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_N	18 24
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	16
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16

SATA SSD

USB Hub nets

USB Camera nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

Unused USB nets

SYNC_MASTER=CONSTRAINTS SYNC_DATE=01/11/2012

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC AD<3..0>	6 16 40 42
LPC_FRAME_L	LPC_45S	LPC	LPC FRAME L	6 16 40 42
	LPC_45S	LPC	LPCPLUS RESET L	6 25 42
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC CLK33M SMC	25 40
	CLK_LPC_45S	CLK_LPC	LPC CLK33M SMC R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC CLK33M LPCPLUS	6 25 42
	CLK_LPC_45S	CLK_LPC	LPC CLK33M LPCPLUS R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH CLK33M PCIIN	16 25
	CLK_LPC_45S	CLK_LPC	PCH CLK33M PCIOUT	18 25
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS PCH CLK	16 43
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS PCH DATA	16 43
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML PCH 0 CLK	16 43
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML PCH 0 DATA	16 43
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SML PCH 1 CLK	16 43
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SML PCH 1 DATA	16 43
HDA_BIT_CLK	HDA_45S	HDA	HDA BIT CLK	6 16 39
	HDA_45S	HDA	HDA BIT CLK R	16
HDA_SYNC	HDA_45S	HDA	HDA SYNC	6 16 39
	HDA_45S	HDA	HDA SYNC R	16
HDA_RST_L	HDA_45S	HDA	HDA RST R L	16
	HDA_45S	HDA	HDA RST L	6 16 39
HDA_SDIN0	HDA_45S	HDA	HDA SDIN0	6 16 39
HDA_SDOUT	HDA_45S	HDA	HDA SDOUT	6 16 39
	HDA_45S	HDA	HDA SDOUT R	16 25
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM CLK32K SUSCLK R	17 41
	CLK_SLOW_45S	CLK_SLOW	SMC CLK32K	40 41
SPI_CLK	SPI_45S	SPI	SPI CLK R	16 42
	SPI_45S	SPI	SPI CLK	42
SPI_MOSI	SPI_45S	SPI	SPI MOSI R	16 42
	SPI_45S	SPI	SPI MOSI	42
SPI_MISO	SPI_45S	SPI	SPI MISO	16 42
SPI_CS0	SPI_45S	SPI	SPI CS0 R L	16 42
	SPI_45S	SPI	SPI CS0 L	42
	SPI_45S	SPI	SPI SMC CLK	40 41
	SPI_45S	SPI	SPI SMC MOSI	40 41
	SPI_45S	SPI	SPI SMC MISO	40 41
	SPI_45S	SPI	SPI SMC CS L	40 41
	SPI_45S	SPI	SPI MLB CLK	41 42 49
	SPI_45S	SPI	SPI MLB MOSI	41 42 49
	SPI_45S	SPI	SPI MLB MISO	41 42 49
	SPI_45S	SPI	SPI MLB CS L	41 42 49
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D P	6 36
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D N	6 36
	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D C P	16 36
	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D C N	16 36
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R P	6 16 36
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R N	6 16 36
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M AP P	6 16 36
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M AP N	6 16 36
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D P<3..0>	33
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D N<3..0>	33
	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D C P<3..0>	8 33
	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D C N<3..0>	8 33
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R P<3..0>	8 33
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R N<3..0>	8 33
	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R C P<3..0>	33
	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R C N<3..0>	33
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M TBT P	16 33
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M TBT N	16 33
	CLK_PCIE_80D	CLK_PCIE	PEG CLK100M P	8 16
	CLK_PCIE_80D	CLK_PCIE	PEG CLK100M N	8 16
XDP_TDI	PCH_45S	PCH_ITP	XDP PCH TDI	16 23
XDP_TDO	PCH_45S	PCH_ITP	XDP PCH TDO	16 23
XDP_TMS	PCH_45S	PCH_ITP	XDP PCH TMS	16 23
XDP_TCK	PCH_45S	PCH_ITP	XDP PCH TCK	16 23

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK0 ML P<3..0>	33
DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK0 ML N<3..0>	33
	DP_80D	DP_TX	DP TBTSNK0 ML C P<3..0>	8 33
	DP_80D	DP_TX	DP TBTSNK0 ML C N<3..0>	8 33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK0 AUXCH P	33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK0 AUXCH N	33
	DP_80D	DP_AUX	DP TBTSNK0 AUXCH C P	8 33
	DP_80D	DP_AUX	DP TBTSNK0 AUXCH C N	8 33
DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK1 ML P<3..0>	33
DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK1 ML N<3..0>	33
	DP_80D	DP_TX	DP TBTSNK1 ML C P<3..0>	8 33
	DP_80D	DP_TX	DP TBTSNK1 ML C N<3..0>	8 33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK1 AUXCH P	33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK1 AUXCH N	33
	DP_80D	DP_AUX	DP TBTSNK1 AUXCH C P	8 33
	DP_80D	DP_AUX	DP TBTSNK1 AUXCH C N	8 33

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK CLK32K RTC	16 25
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK CLK25M SB	16 25
	CLK_25M_45S	CLK_25M	SYSCLK CLK25M SB R	16
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT	25 33
	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT R	33
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X1	25
	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X2	25
	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X2 R	25

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0>	33 63
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0>	33 63
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0>	63
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0>	63
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1>	33 63
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1>	33 63
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3>	33 63
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3>	33 63
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2>	63
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2>	63
	DP_80D	DP_TX	DP_A_LSX_ML_P<1>	63
	DP_80D	DP_TX	DP_A_LSX_ML_N<1>	63
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0>	63
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0>	63
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1>	33 63
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1>	33 63
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0>	33 63
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0>	33 63
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P	33 63
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N	33 63
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P	63
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N	63
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P	63
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N	63
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P	63
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N	63
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0>	8 33
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0>	8 33
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>	
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>	
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_P<3..1:2>	8 33
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_N<3..1:2>	8 33
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>	
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>	
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>	
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>	
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0>	8 33
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0>	8 33
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_P	8 33
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_N	8 33
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P	
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N	

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	33
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	33
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	33
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	33

Only used on hosts supporting Thunderbolt video-in

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	40 43
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	40 43
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	40 43
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	40 43
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL	40 43
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA	40 43
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	40 43
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	40 43
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	40 43
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	40 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_P	52
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_N	52
	1:1_DIFFPAIR		CHGR_CSI_R_P	52
	1:1_DIFFPAIR		CHGR_CSI_R_N	52
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_P	52
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_N	52
	1:1_DIFFPAIR		CHGR_CSO_R_P	52
	1:1_DIFFPAIR		CHGR_CSO_R_N	52

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1:1_DIFFPAIR	0.200 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SPKR_DIFFPAIR	*	=1:1_DIFFPAIR	0.300 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	45 46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	45 46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_N	46
	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P	46
	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N	46
	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P	46
	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPU_THERMD_P	9 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPU_THERMD_N	9 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	46
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N	44 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P	44 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1_P	44 56 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1_N	44 57
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUM_R_P	44
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUM_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1G_P	44 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1G_N	44 57
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUMG_R_P	44
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUMG_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	VCCSAS0_CS_P	44 53
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	VCCSAS0_CS_N	44 53
	SENSE_1TO1_45S	SENSE	VCCSAISNS_R_P	44
	SENSE_1TO1_45S	SENSE	VCCSAISNS_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_P	44 60
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_N	44 60
	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_R_P	44
	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUMG_P	56 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUMG_N	56 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUM_P	56 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUM_N	56 57
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	8 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	8 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_N	45 55
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_P	45 55
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	36 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	36 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	37 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	37 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	8 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	8 45
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	6 39 50
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	6 39 50
	1:1_DIFFPAIR	AUDIO	MAX98300_R_P	50
	1:1_DIFFPAIR	AUDIO	MAX98300_R_N	50
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	6 50 51
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	6 50 51
		SB_POWER	PP3V3_S5	6 7
		SB_POWER	PP3V3_S0	6 7
		GND	GND	

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Project Specific Constraints

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J11/J13 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL4,ISL9	Y	0.114 MM	0.114 MM		0.150 MM	0.150 MM
72_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

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PCB Rule Definitions

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