

ICH6 GPIO SETTING

Pin	Pin Name	Connect to	Type	Input/Output Set
B7	GPI0/REQ6#	10K Pull +3V	I	fixed as Input only
E8	GPI1 / REQ5#	10K Pull +3V	I	fixed as Input only
D9	GPI2 / PIRQE#	10K Pull +3V	I	fixed as Input only
C7	GPI3 / PIRQF#	10K Pull +3V	I	fixed as Input only
C6	GPI4 / PIRQG#	10K Pull +3V	I	fixed as Input only
M3	GPI5 / PIRQH#	10K Pull +3V	I	fixed as Input only
AD19	GPI6 / BMBUSY#	NB BMBUSY#	I	Input
AE19	GPI7	NC	GPI	fixed as Input only
R1	GPI8	EC KBC_SCI#	GPI	fixed as Input only
C23	GPI9/OC4#	10K Pull +3V	I	Input
D23	GPI10/OC5#	10K Pull +3V	I	Input
W6	GPI11 / SMBALERT#	10K Pull +3V	I	Input
M2	GPI12	NC	GPI	fixed as Input only
R6	GPI13	EC EXTSMI#	GPI	fixed as Input only
C25	GPI14/OC6#	10K Pull +3V	I	Input
C24	GPI15 /OC7#	10K Pull +3V	I	Input
D8	GPO16/GTN6#	NC	O	Output
F6	GPO17 / GNT5#	NC	O	Output
AC21	GPO18 / STP_PC#	Clock GEN STP_PC#	O	Output
AB21	GPO19	WLAN_LED#	GPO	fixed as Output only
AD22	GPO20 / STP_CPU#	STP_CPU#	O	Output
AD20	GPO21	NC	GPO	
NA	GPIO22	NA	NA	NA
AD21	GPO23	NC	GPO	fixed as Output only
V3	GPIO24	3G	I/O	Output
P5	GPIO25	NC	I/O	Output

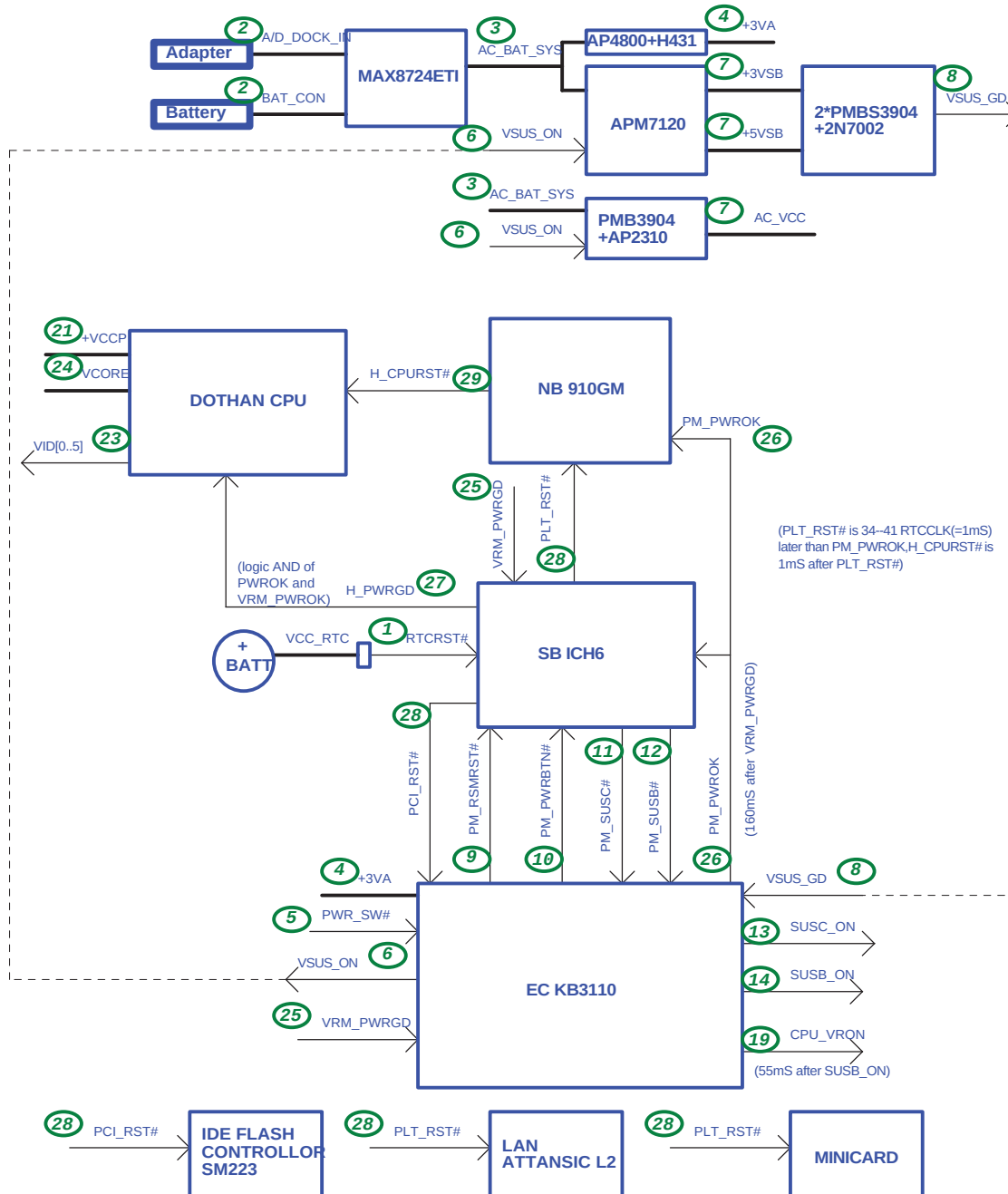
Pin	Pin Name	Connect to	Type	Input/Output Set
AF17	GPI26/SATA0GP	NC	GPI	(GPI)Input
R3	GPIO27	NC	I/O	Output
T3	GPIO28	NC	I/O	Output
AE18	GPI29 / SATA1GP	PCBVER0	GPI	(GPI)Input
AF18	GPI30 / SATA2GP	NC	GPI	(GPI)Input
AG18	GPI31 / SATA3GP	PCBVER1	GPI	(GPI)Input
AF19	GPIO32 / CLKRUN#	10K Pull +3V	I/O	Input
AF20	GPIO33	NC	I/O	Output
AC18	GPIO34	NC	I/O	Output
NA	GPIO35	NA	NA	NA
NA	GPIO36	NA	NA	NA
NA	GPIO37	NA	NA	NA
NA	GPIO38	NA	NA	NA
NA	GPIO39	NA	NA	NA
F7	GPI40 / REQ4#	10K Pull +3V	I	Input
P4	GPI41 / LDRQ1#	NC	I	Input
NA	GPIO42	NA	NA	NA
NA	GPIO43	NA	NA	NA
NA	GPIO44	NA	NA	NA
NA	GPIO45	NA	NA	NA
NA	GPIO46	NA	NA	NA
NA	GPIO47	NA	NA	NA
E7	GPO48 /GNT4#	NC	O	Output
AC25	GPO49 / CPUPWRGD	CPU Power Ok	O	Output

fixed as Output only

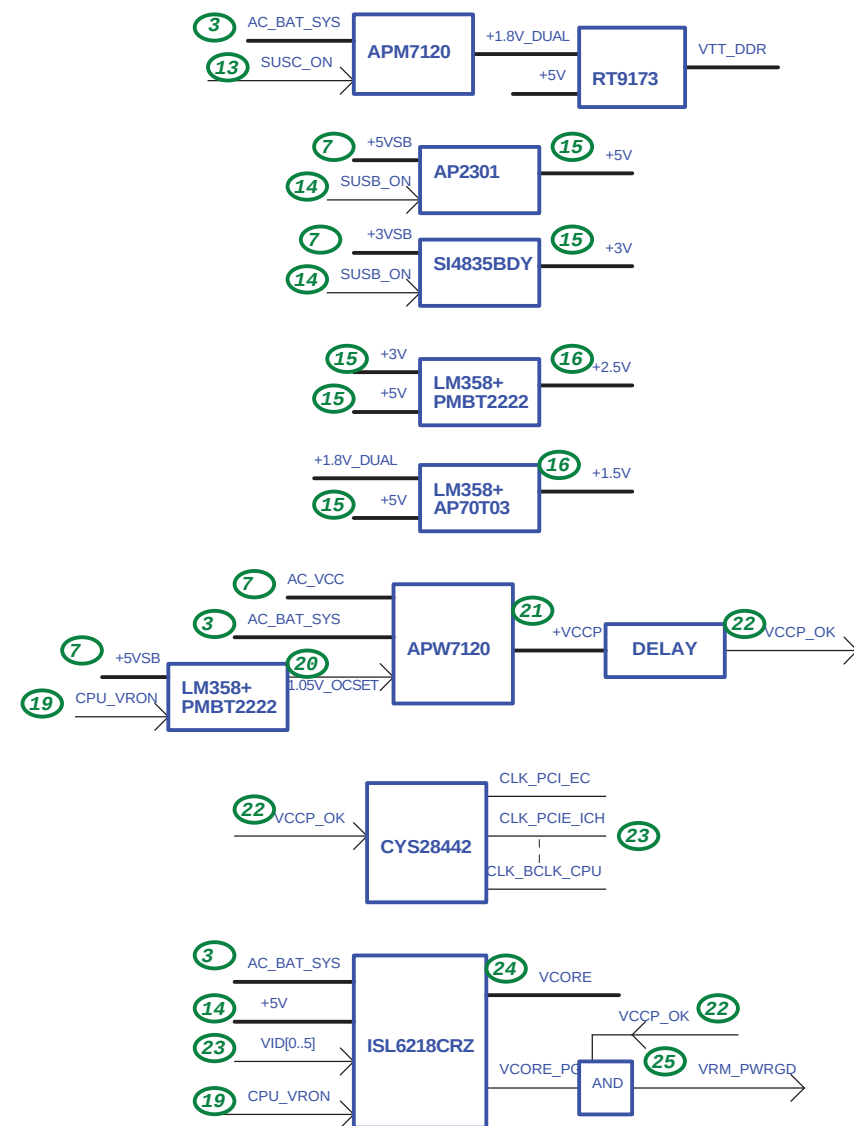
Default Group-A7V8X MX

		Title : System Setting	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A3	Project Name 900SD_MB	Rev R1.0G	
Date: Monday, November 10, 2008		Sheet 2	of 51

*This sequence is for Battery Plug-in and no Adapter,
if Adapter Plug-in, the sequence change to:
A/D_DOCK_IN--->AC_BAT_SYS--->+3VA--->VSUS_ON--->+3VSB & +5VSB
--->VSUS_GD--->PM_REMRST#--->PWR_SW#--->PM_PWRBTN--->PM_SUSC#--->PM_SUSB#



	Signal	S0/S1	S3	S4/S5	Power
Only Battery	VSUS_ON	H	H	L	VSUS
Adapter In	VSUS_ON	H	H	H	VSUS
	SUSB_ON	H	L	L	Main
	SUSC_ON	H	H	L	DUAL



Default Group-A7V8X MX

ASUS		Title : Power Sequence	
ASUSTek Computer INC.		Engineer: Kell Huang	
Size	Project Name	Rev	
A3	900SD_MB	R1.0G	
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EC KB3310 GPIO SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
1	GA20	A20GATE	O	A20GATE
2	KBRST#	RC_IN#	O	KBRST#
6	GPIO04	CTRL_CAMER_PWR	I	Default : High
13	PCIRST#	PCI_RST#	I	PCI Reset
14	GPIO07	N.C	O	Reserved
15	GPIO08	EXTSMIH#	O	EXTSMIH#, 10K Pull +3VSUS
16	GPIO0A	LID_EC#	I	LID_EC#, *
17	GPIO0B	LCD_CSB	O	LCD chip select
18	GPIO0C	LCD_SDA	I/O	LCD Data
19	GPIO0D	DISTP_SW#	I	Touch Pad Disabled,*
20	SCI#	KBC_SCI#	O	KBC_SCI#, 10K Pull +3VSUS
21	PWM1	BL_PWM_DA	O	LCD Light Switch
23	PWM2	LCD_SCL	O	LCD clock
25	GPIO11	PM_PWRBTN#	OD	Power Button to SB, *
26	FANPWM1	FAN0_PWM	O	CPU Fan(Unused)
27	FANPWM2	FAN1_PWM	O	VGA Fan(Unused)
28	FANFB1	FAN0_TACH	I	CPU FanTach(Unused)
29	FANFB2	FAN1_TACH	I	VGA FanTach(Unused)
30	GPIO16	E51_TX	O	RS232 debug port
31	GPIO17	N.C	O	Reserved
32	GPIO18	PWR_SW#	I	power button, *
34	GPIO19	MAIL_LED#	O	Mail LED(Unused)
36	GPIO1A	CTRL_Mincard_PWR	O	Default : High
38	CLKRUN#	N.C	O	Reserved
39	KSO0	KSO0	O	For Keyboard interface
40	KSO1	KSO1	O	For Keyboard interface
41	KSO2	KSO2	O	For Keyboard interface
42	KSO3	KSO3	O	For Keyboard interface
43	KSO4	KSO4	O	For Keyboard interface
44	KSO5	KSO5	O	For Keyboard interface
45	KSO6	KSO6	O	For Keyboard interface
46	KSO7	KSO7	O	For Keyboard interface
47	KSO8	KSO8	O	For Keyboard interface
48	KSO9	KSO9	O	For Keyboard interface
49	KSO10	KSO10	O	For Keyboard interface
50	KSO11	KSO11	O	For Keyboard interface
51	KSO12	KSO12	O	For Keyboard interface
52	KSO13	KSO13	O	For Keyboard interface
53	KSO14	KSO14	O	For Keyboard interface
54	KSO15	KSO15	O	For Keyboard interface
55	KSI0	KSI0	I	For Keyboard interface
56	KSI1	KSI1	I	For Keyboard interface
57	KSI2	KSI2	I	For Keyboard interface
58	KSI3	KSI3	I	For Keyboard interface
59	KSI4	KSI4	I	For Keyboard interface
60	KSI5	KSI5	I	For Keyboard interface
61	KSI6	KSI6	I	For Keyboard interface
62	KSI7	KSI7	I	For Keyboard interface
63	AD0	P_PMON_10	I	Sense Power Loading
64	AD1	BAT_IN	I	sense Battery
65	AD2	N.C	I	Reserved
66	AD3	N.C	I	Reserved
68	GPO3C	DOC	O	Trigger Clock Gen

Pin No.	Pin Name	Signal Name	Type	NOTE
70	GPO3D	LCD_BACKOFF#	O	LCD_BACKOFF#
71	GPO3E	CLK_PWRSERVE#	O	Active when BAT_IN=1 and AC_OK=0(Unused)
72	GPO3F	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K Pull GND
75	GPIO42	N.C	O	Reserved
76	GPIO43	N.C	O	Reserved
77	SCL1	SMB0_CLK	I/OD	4.7K Pull +3VA_EC
78	SDA1	SMB0_DAT	I/OD	4.7K Pull +3VA_EC
79	SCL2	SMB1_CLK	I/OD	10K Pull +3VS
80	SDA2	SMB1_DAT	I/OD	10K Pull +3VS
81	KSO16	N.C	O	Reserved
82	KSO17	N.C	O	Reserved
83	PSCLK1	N.C	O	Reserved
84	PSDAT1	N.C	O	Reserved
85	PSCLK2	N.C	O	Reserved
86	PSDAT2	N.C	O	Reserved
87	PSCLK3	TP_CLK	I/OD	10K Pull +3VS
88	PSDAT3	TP_DAT	I/OD	10K Pull +3VS
89	GPIO50	BATSEL_3S	O	Battery series. Hi:3S, Lo:4S(Unused)
90	GPIO52	CHG_LED_UP#	O	charger LED
91	GPIO53	CTRL_L2_PWR	O	Default : High
92	GPIO54	PWR_LED_UP	O	EC H/W blinking
93	GPIO55	SCRL_LED#	O	EC H/W controls
95	GPIO56	PWR4G_SW#	I	*
97	GPXOA00	SPI_MODE#	O	*HW Strap for SPI Flash deExternal Pull Down 100K ohm to GND"
98	GPXOA01	SUSC_ON	O	
99	GPXOA02	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH8_PWROK	O	
103	GPXOA06	N.C	O	Reserved
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0	BATSEL_2P#	O	Battery parallel. Hi:1P, Lo:2P-3P
110	GPXID1	N.C	O	Reserved
112	GPXID2	THRO_CPU	O	Active if Battery Temperature Is
114	GPXID3	SUSB#	I	Pull Down 100K ohm to GND
115	GPXID4	SUSC#	I	Pull Down 100K ohm to GND
116	GPXID5	CPUPWR_GD	I	10K Pull +3VS
117	GPXID6	VSUS_GD	I	Disabled **
118	GPXID7	N.C	O	Reserved
121	GPIO57	INTERNET#	I	*
126	SPICLK	SPI_CLK	O	SPI Clock
127	GPIO59	N.C	O	Reserved

EC KB3310 Other Pin SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
3	SERIRQ	INT_SERIRQ	I/OD	8.2K Pull +3VS
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	Add 100K ohm to GND
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#	SPI_SO	I	
120	WR#	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	K_V18R		Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#	SPI_CE#	O	

Default Group-A7V8X MX



Title : EC Pin Define

ASUSTek Computer INC.

Engineer: Kell_Huang

Size A3

Project Name 900SD_MB

Rev R1.0G

Date: Monday, November 10, 2008

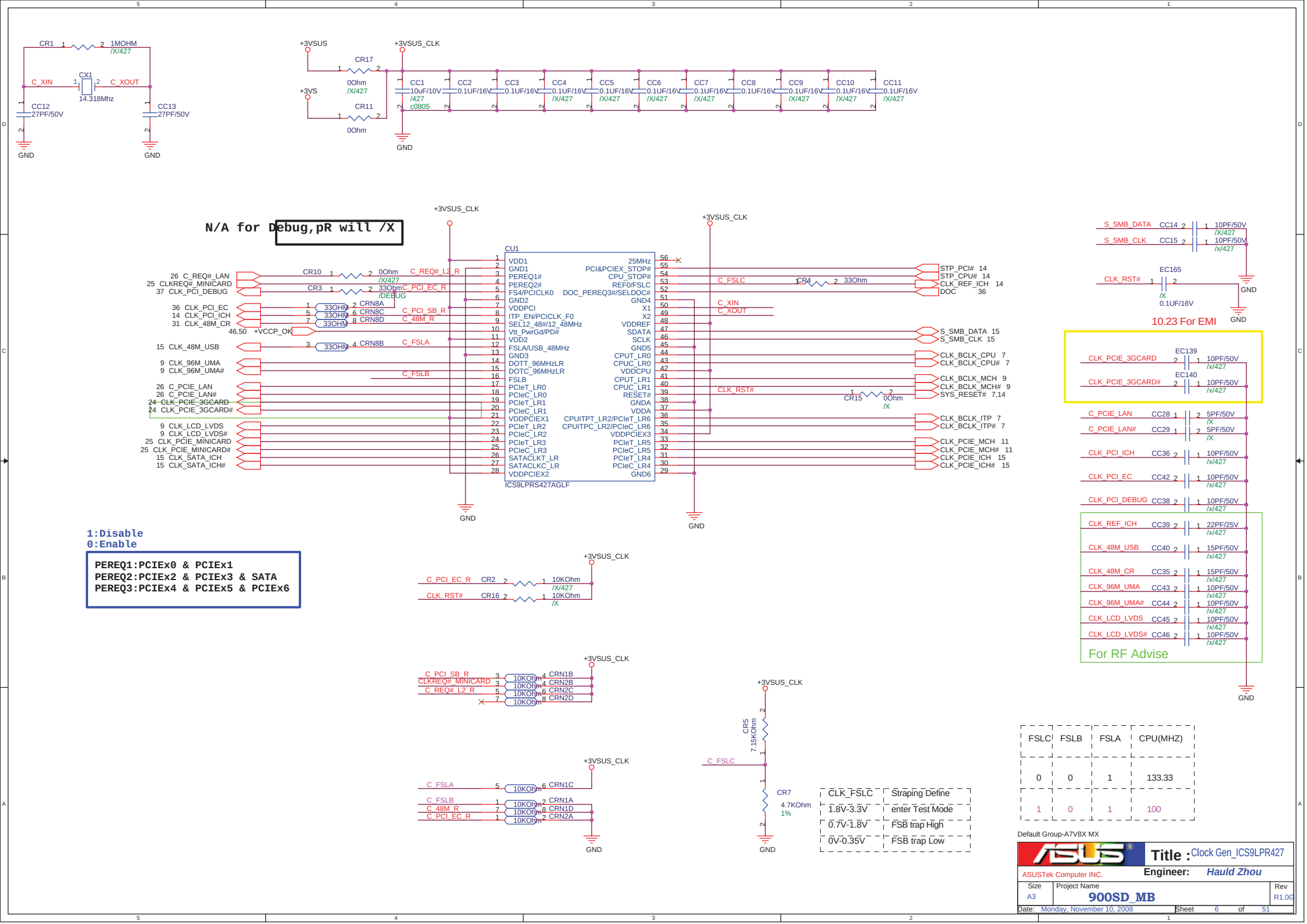
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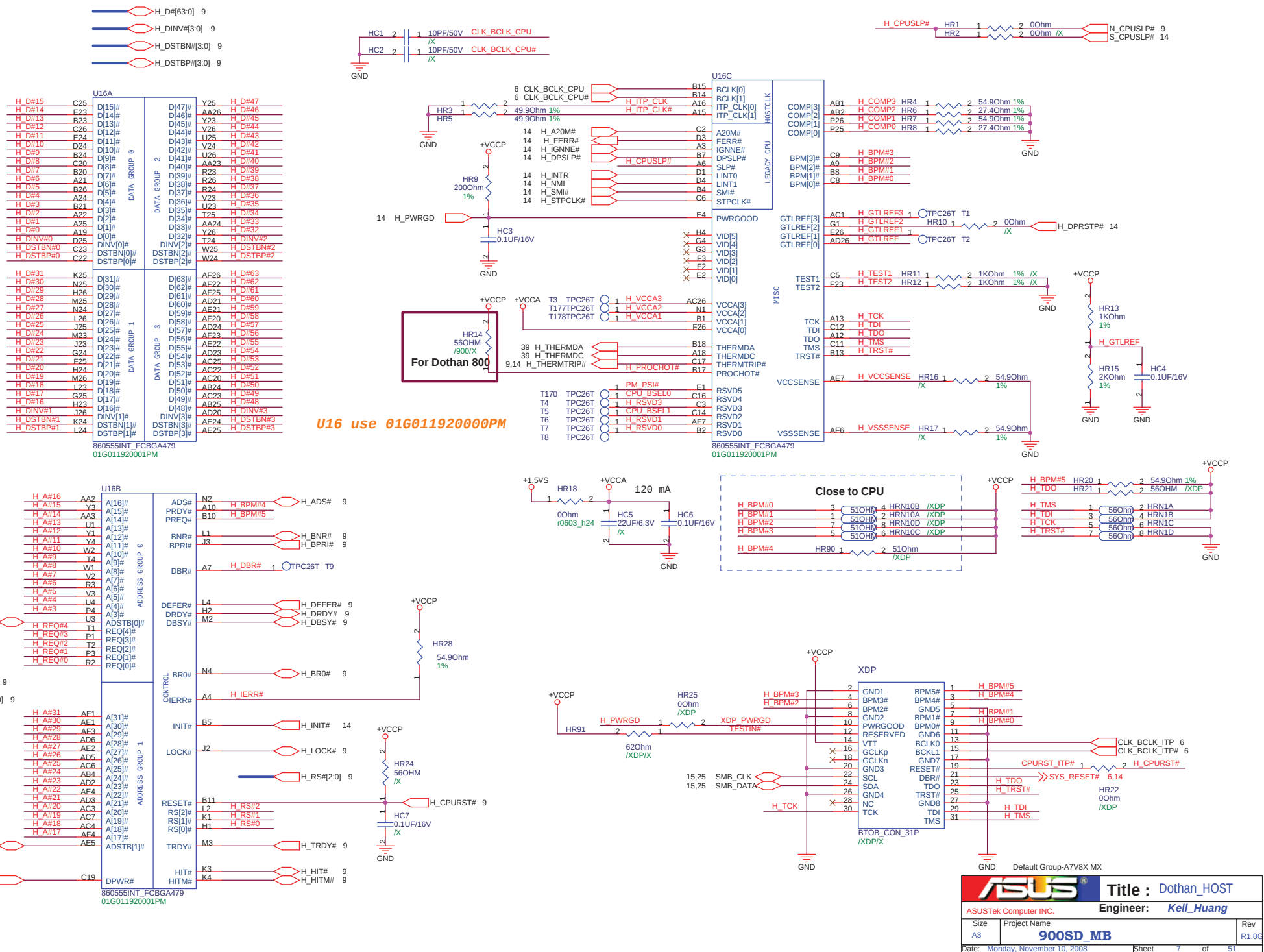
CIRCUIT UPDATED HISTORY

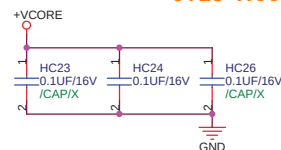
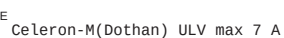
Rev	Date	Description
900SD 1.0G	2008.10.15	Initial Release

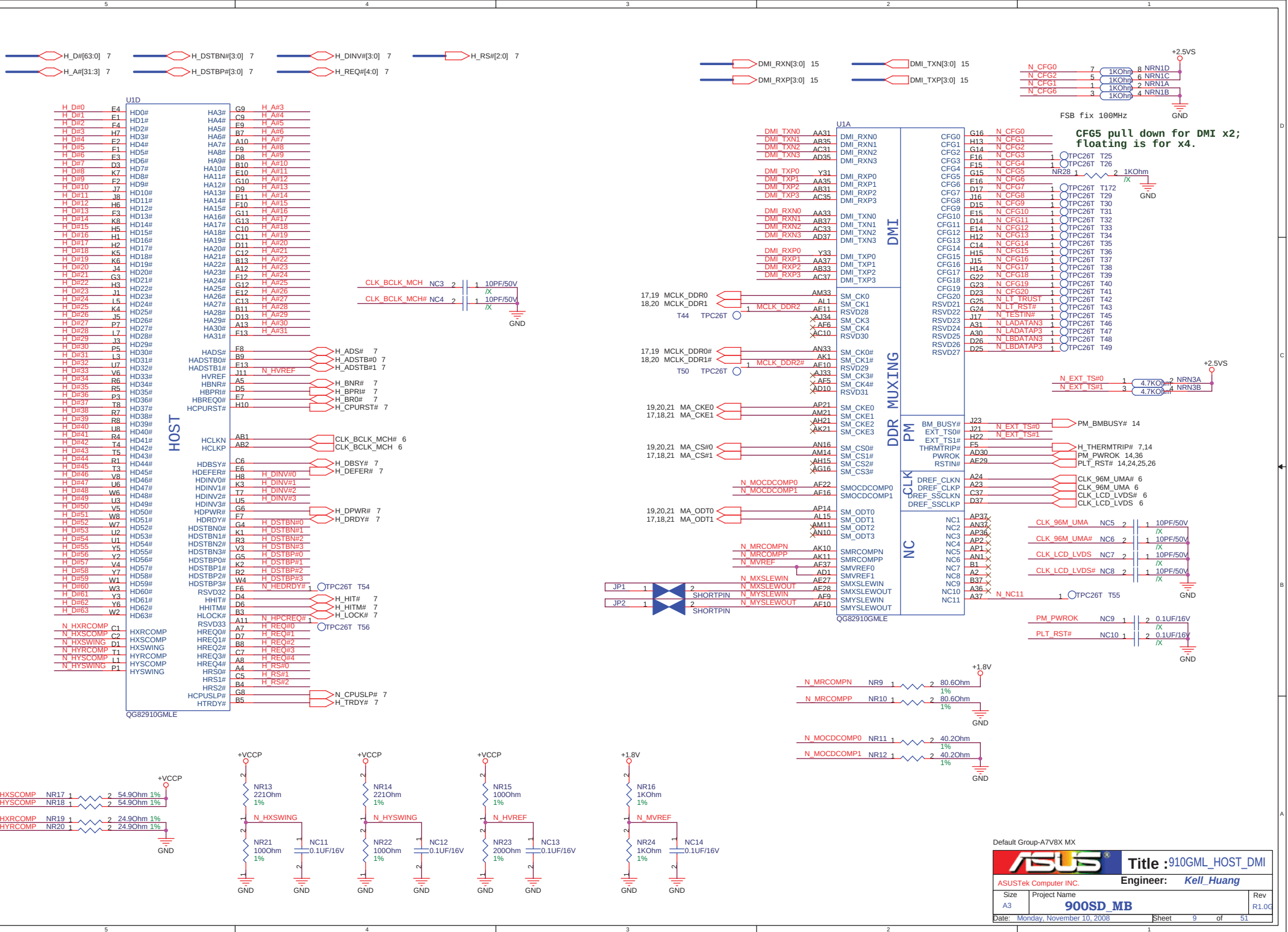
Default Group-A7V8X MX

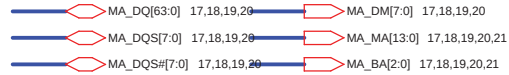












MA_DQ0	AG35	SA_DQ0	SA_BS0	AK15	MA_BA0
MA_DQ1	AH35	SA_DQ1	SA_BS1	AK16	MA_BA1
MA_DQ2	AL35	SA_DQ2	SA_BS2	AL21	MA_BA2
MA_DQ3	AL37	SA_DQ3			
MA_DQ4	AH36	SA_DQ4	SA_DM0	AJ37	MA_DM0
MA_DQ5	AJ35	SA_DQ5	SA_DM1	AP35	MA_DM1
MA_DQ6	AK37	SA_DQ6	SA_DM2	AL29	MA_DM2
MA_DQ7	AL34	SA_DQ7	SA_DM3	AP24	MA_DM3
MA_DQ8	AM36	SA_DQ8	SA_DM4	AP9	MA_DM4
MA_DQ9	AN35	SA_DQ9	SA_DM5	AP4	MA_DM5
MA_DQ10	AP32	SA_DQ10	SA_DM6	AJ2	MA_DM6
MA_DQ11	AM31	SA_DQ11	SA_DM7	AD3	MA_DM7
MA_DQ12	AM34	SA_DQ12			
MA_DQ13	AM35	SA_DQ13	SA_DQS0	AK36	MA_DQS0
MA_DQ14	AL32	SA_DQ14	SA_DQS1	AP33	MA_DQS1
MA_DQ15	AM32	SA_DQ15	SA_DQS2	AN29	MA_DQS2
MA_DQ16	AN31	SA_DQ16	SA_DQS3	AP23	MA_DQS3
MA_DQ17	AP31	SA_DQ17	SA_DQS4	AM8	MA_DQS4
MA_DQ18	AN28	SA_DQ18	SA_DQS5	AM4	MA_DQS5
MA_DQ19	AP28	SA_DQ19	SA_DQS6	AJ1	MA_DQS6
MA_DQ20	AL30	SA_DQ20	SA_DQS7	AE5	MA_DQS7
MA_DQ21	AM30	SA_DQ21			
MA_DQ22	AM28	SA_DQ22	SA_DQS0#	AK35	MA_DQS#0
MA_DQ23	AL28	SA_DQ23	SA_DQS1#	AP34	MA_DQS#1
MA_DQ24	AP27	SA_DQ24	SA_DQS2#	AN30	MA_DQS#2
MA_DQ25	AM27	SA_DQ25	SA_DQS3#	AN23	MA_DQS#3
MA_DQ26	AM23	SA_DQ26	SA_DQS4#	AN8	MA_DQS#4
MA_DQ27	AM22	SA_DQ27	SA_DQS5#	AM5	MA_DQS#5
MA_DQ28	AL23	SA_DQ28	SA_DQS6#	AH1	MA_DQS#6
MA_DQ29	AM24	SA_DQ29	SA_DQS7#	AE4	MA_DQS#7
MA_DQ30	AN22	SA_DQ30			
MA_DQ31	AP22	SA_DQ31	SA_MA0	AL17	MA_MA0
MA_DQ32	AM9	SA_DQ32	SA_MA1	AP17	MA_MA1
MA_DQ33	AL9	SA_DQ33	SA_MA2	AP18	MA_MA2
MA_DQ34	AL6	SA_DQ34	SA_MA3	AM17	MA_MA3
MA_DQ35	AP7	SA_DQ35	SA_MA4	AN18	MA_MA4
MA_DQ36	AP11	SA_DQ36	SA_MA5	AM18	MA_MA5
MA_DQ37	AP10	SA_DQ37	SA_MA6	AL19	MA_MA6
MA_DQ38	AL7	SA_DQ38	SA_MA7	AP20	MA_MA7
MA_DQ39	AM7	SA_DQ39	SA_MA8	AM19	MA_MA8
MA_DQ40	AN5	SA_DQ40	SA_MA9	AL20	MA_MA9
MA_DQ41	AN6	SA_DQ41	SA_MA10	AM16	MA_MA10
MA_DQ42	AN3	SA_DQ42	SA_MA11	AN20	MA_MA11
MA_DQ43	AP3	SA_DQ43	SA_MA12	AM20	MA_MA12
MA_DQ44	AP6	SA_DQ44	SA_MA13	AM15	MA_MA13
MA_DQ45	AM6	SA_DQ45			
MA_DQ46	AL4	SA_DQ46	SA_CAS#	AN15	
MA_DQ47	AM3	SA_DQ47	SA_RAS#	AP16	
MA_DQ48	AK2	SA_DQ48	SA_RCVENIN#	AE29	MA_RCVENIN# 1
MA_DQ49	AK3	SA_DQ49	SA_RCVENOUT#	AE28	MA_RCVENOUT# 1
MA_DQ50	AG2	SA_DQ50	SA_WE#	AP15	
MA_DQ51	AG1	SA_DQ51			
MA_DQ52	AL3	SA_DQ52			
MA_DQ53	AM2	SA_DQ53			
MA_DQ54	AH3	SA_DQ54			
MA_DQ55	AG3	SA_DQ55			
MA_DQ56	AE3	SA_DQ56			
MA_DQ57	AE3	SA_DQ57			
MA_DQ58	AD6	SA_DQ58			
MA_DQ59	AC4	SA_DQ59			
MA_DQ60	AE2	SA_DQ60			
MA_DQ61	AE1	SA_DQ61			
MA_DQ62	AD4	SA_DQ62			
MA_DQ63	AD5	SA_DQ63			

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AE31	SB_DQ0	SB_BS0	AJ15
AE32	SB_DQ1	SB_BS1	AG11
AG32	SB_DQ2	SB_BS2	AG21
AG36	SB_DQ3		
AE34	SB_DQ4		
AE33	SB_DQ5	SB_DM0	AE32
AE31	SB_DQ6	SB_DM1	AK34
AE30	SB_DQ7	SB_DM2	AK27
AH33	SB_DQ8	SB_DM3	AK24
AH32	SB_DQ9	SB_DM4	AJ10
AK31	SB_DQ10	SB_DM5	AE7
AG30	SB_DQ11	SB_DM6	AB7
AG34	SB_DQ12		
AG33	SB_DQ13		
AH31	SB_DQ14	SB_DQS0	AE34
AJ31	SB_DQ15	SB_DQS1	AK32
AK30	SB_DQ16	SB_DQS2	AJ28
AJ30	SB_DQ17	SB_DQS3	AK23
AH29	SB_DQ18	SB_DQS4	AM10
AH28	SB_DQ19	SB_DQS5	AH6
AK29	SB_DQ20	SB_DQS6	AF8
AH30	SB_DQ21	SB_DQS7	AB4
AH27	SB_DQ22		
AG28	SB_DQ23	SB_DQS0#	AE35
AE24	SB_DQ24	SB_DQS1#	AK33
AG23	SB_DQ25	SB_DQS2#	AK28
AJ22	SB_DQ26	SB_DQS3#	AJ23
AK22	SB_DQ27	SB_DQS4#	AL10
AH24	SB_DQ28	SB_DQS5#	AH7
AH23	SB_DQ29	SB_DQS6#	AE7
AG22	SB_DQ30	SB_DQS7#	AB5
AJ21	SB_DQ31		
AG10	SB_DQ32	SB_MA0	AH17
AG9	SB_DQ33	SB_MA1	AK17
AG8	SB_DQ34	SB_MA2	AH18
AH8	SB_DQ35	SB_MA3	AK18
AH11	SB_DQ36	SB_MA4	AJ19
AH10	SB_DQ37	SB_MA5	AK19
AJ9	SB_DQ38	SB_MA6	AH15
AK9	SB_DQ39	SB_MA7	AJ20
AJ7	SB_DQ40	SB_MA8	AH20
AK6	SB_DQ41	SB_MA9	AL16
AJ4	SB_DQ42	SB_MA10	AG19
AH5	SB_DQ43	SB_MA11	AG20
AK8	SB_DQ44	SB_MA12	AG19
AJ8	SB_DQ45	SB_MA13	
AJ5	SB_DQ46		
AK4	SB_DQ47	SB_CAS#	AH14
AG5	SB_DQ48	SB_RAS#	AK14
AG4	SB_DQ49	SB_RCVENIN#	AE15
AD8	SB_DQ50	SB_RCVENOUT#	AE14
AD9	SB_DQ51	SB_WE#	AH16
AH4	SB_DQ52		
AG6	SB_DQ53		
AE8	SB_DQ54		
AD7	SB_DQ55		
AC5	SB_DQ56		
AB8	SB_DQ57		
AB6	SB_DQ58		
AC8	SB_DQ59		
AC7	SB_DQ60		
AA4	SB_DQ61		
AA5	SB_DQ62		
	SB_DQ63		

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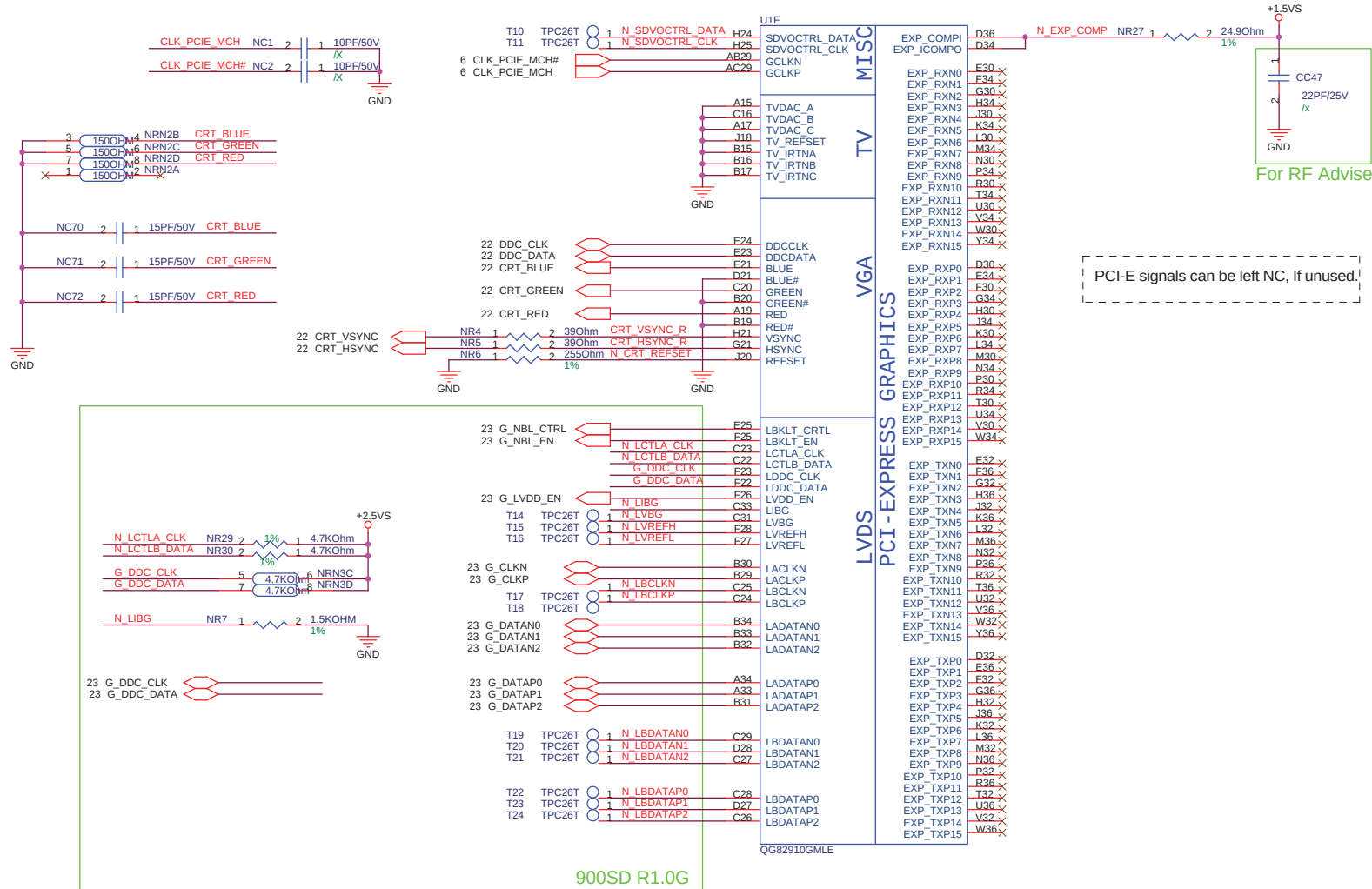
Default Group-A7V8X M2

ASUS		Title : 910GML_DRAM	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name		Rev
A3	900SD_MB		R1.0G
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SDVO SMBus have
internal pull down

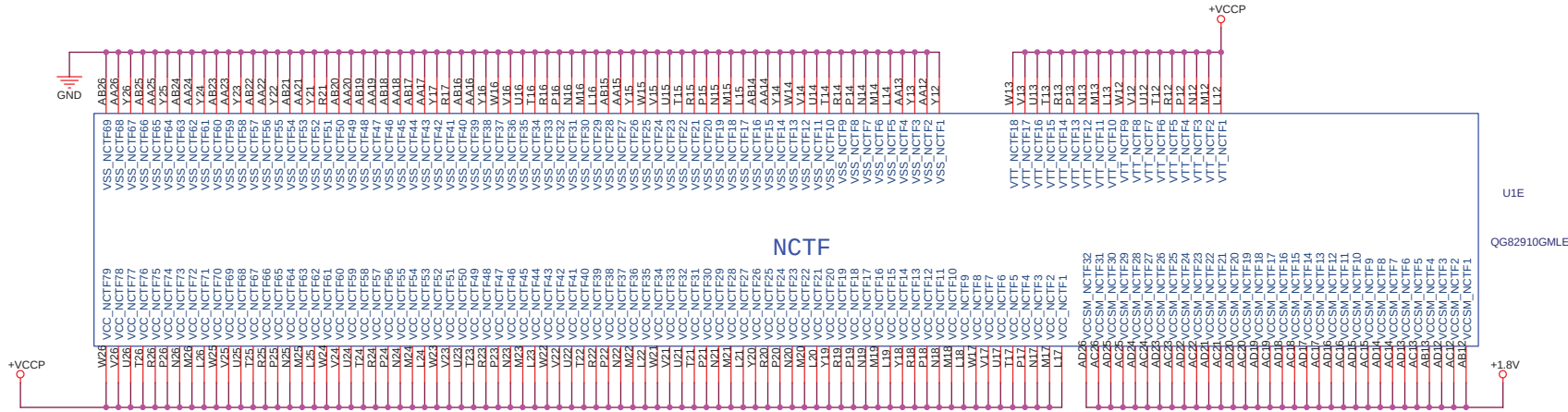
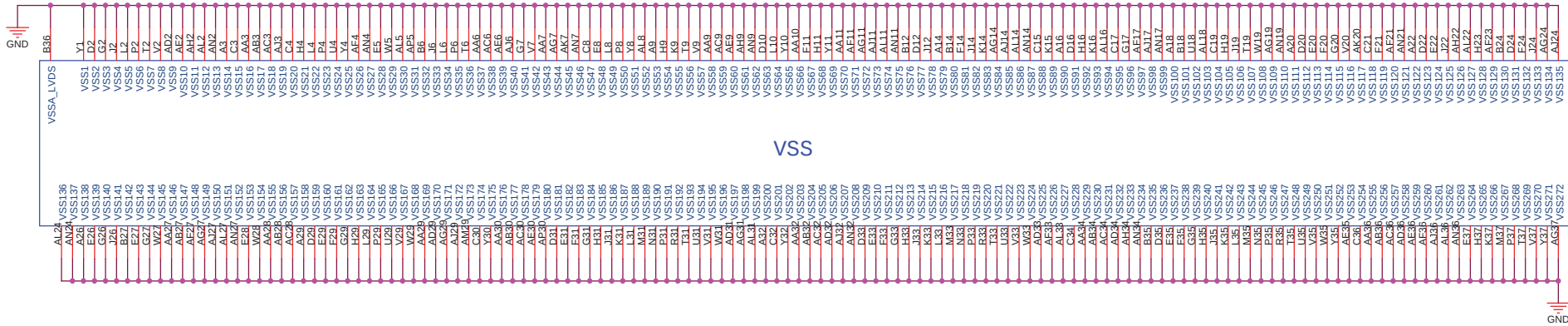
SDVOCTRL_DATA Int PD
0 : No SDVO device
1 : SDVO device present

U1 use 02G010007610



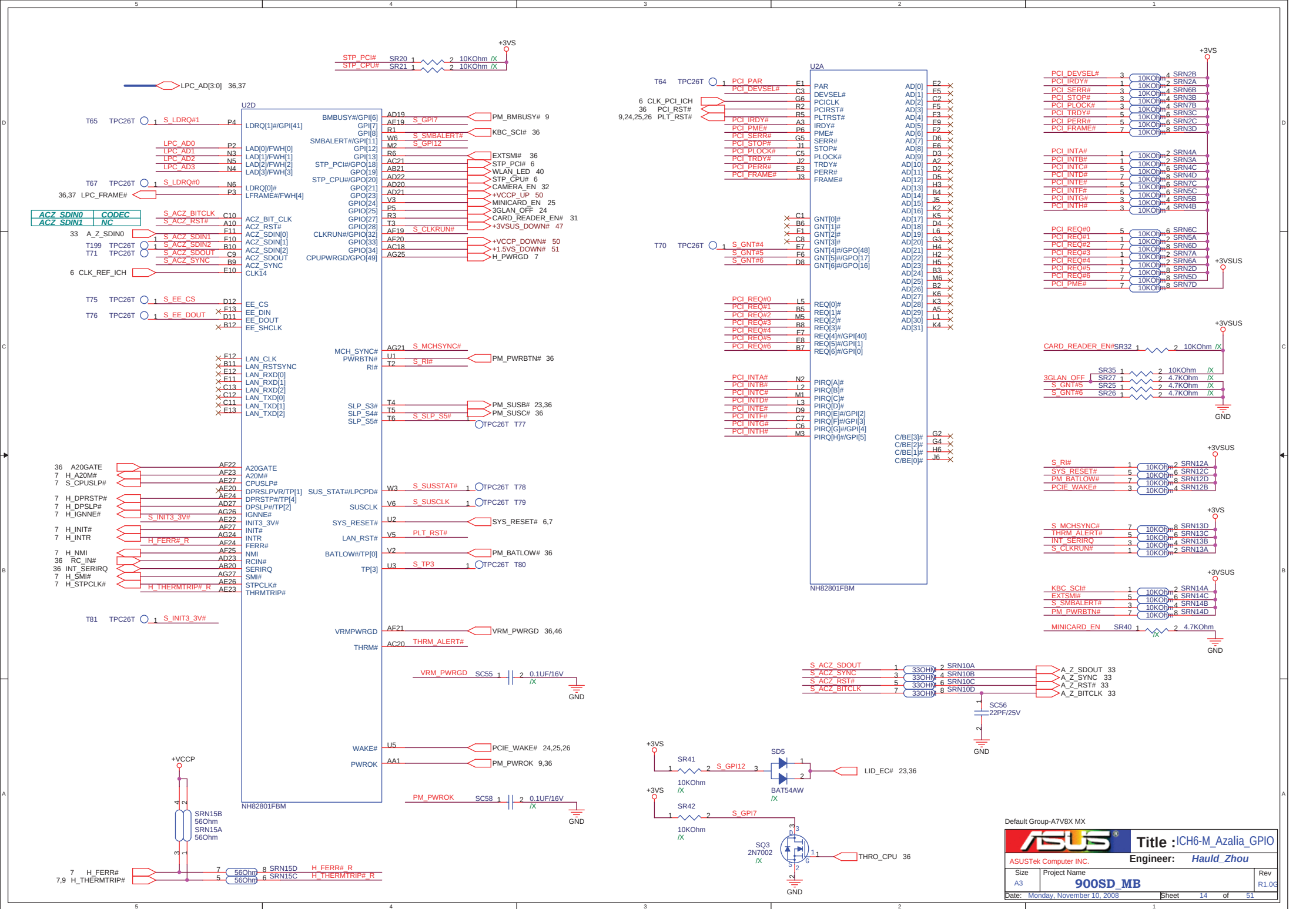
Default Group-A7V8X MX

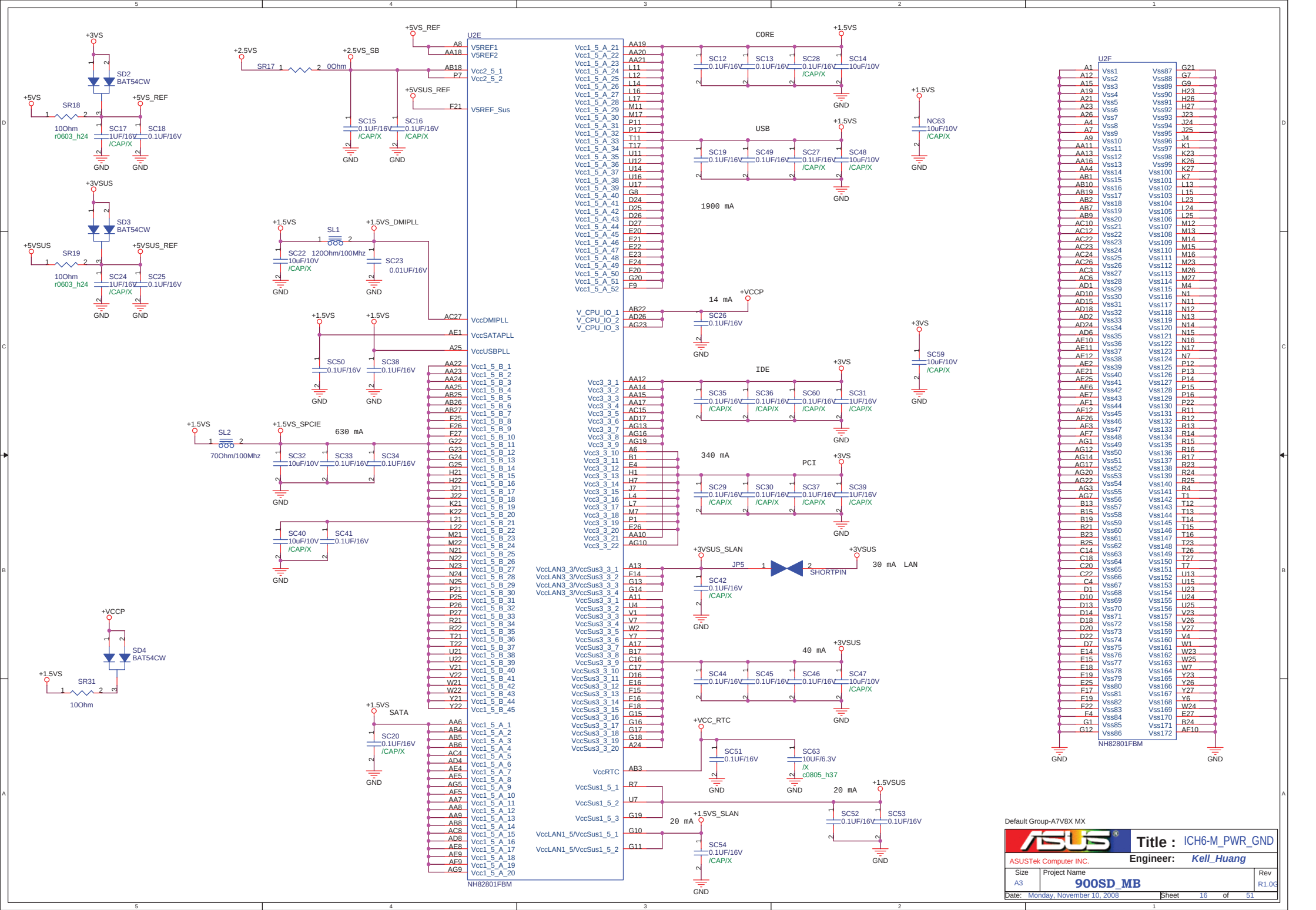
ASUS®		Title :910GML_VGA_LVDS	
ASUSTek Computer INC.		Engineer: Hauld_Zhou	
Size	Project Name		Rev
A3	900SD_MB		R1.0G
Date: Monday, November 10, 2008		Sheet	11 of 51



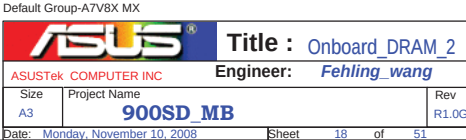
Default Group-A7V8X MX

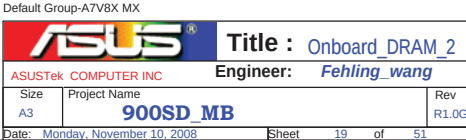
ASUS®		Title : 910GML_GND	
ASUSTek Computer INC.		Engineer: Kell Huang	
Size	Project Name		Rev
A3	900SD_MB		R1.0G
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D

D

C

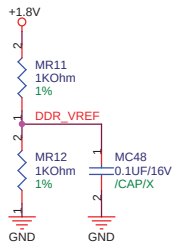
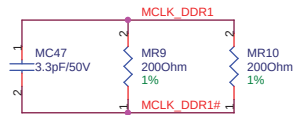
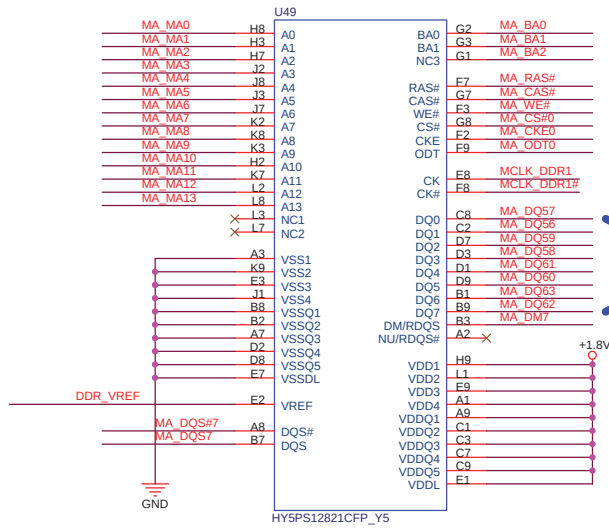
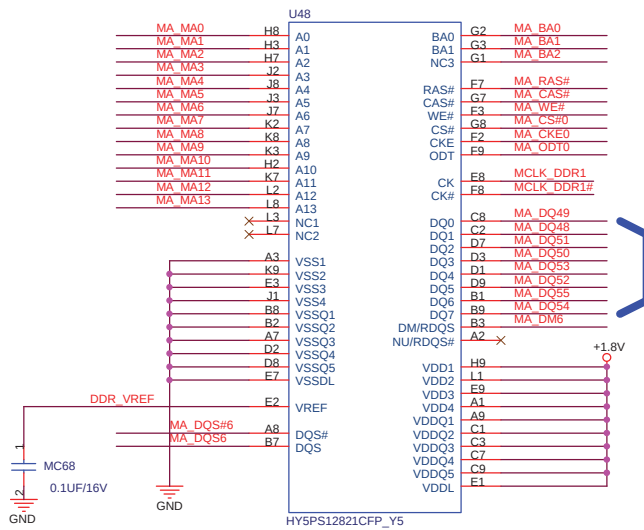
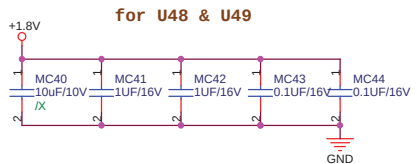
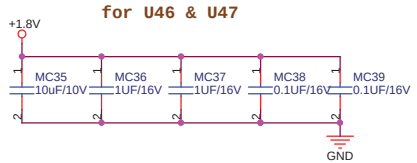
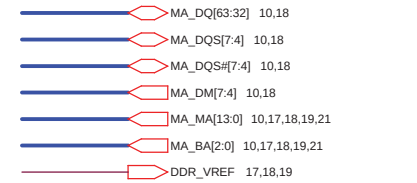
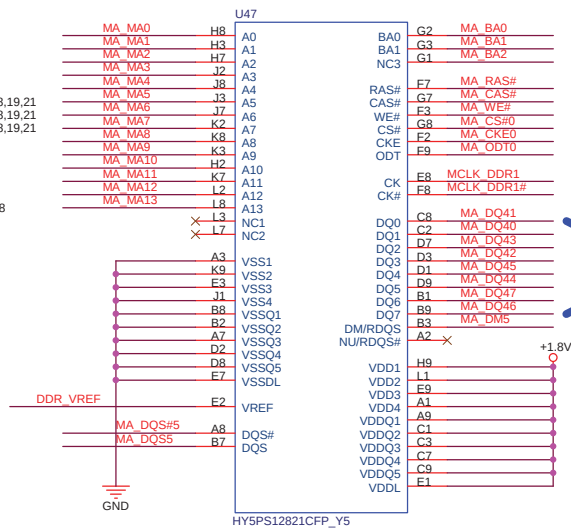
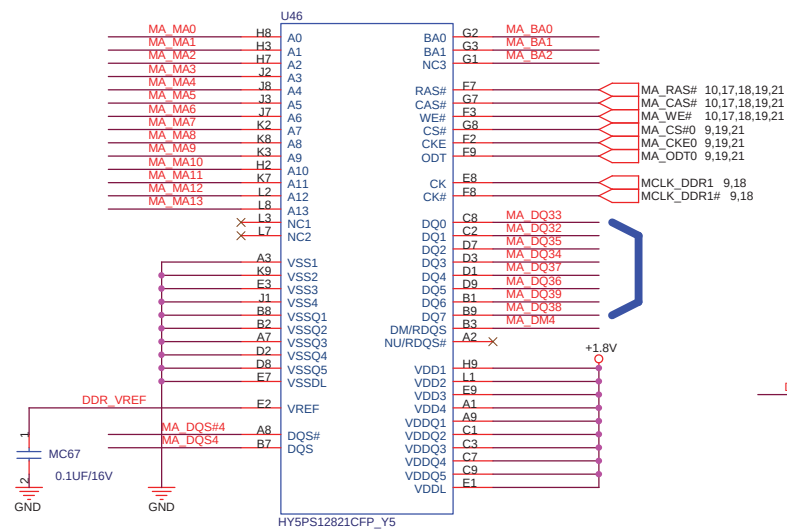
C

B

B

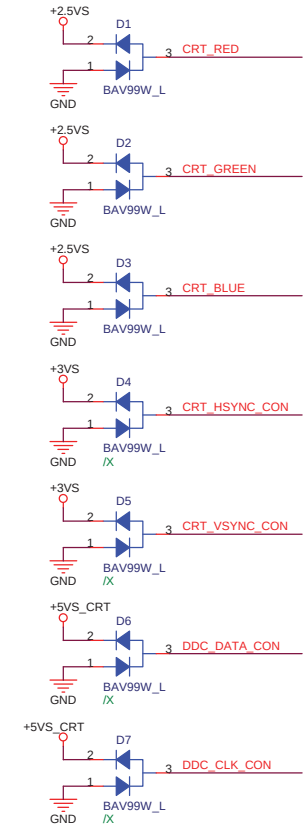
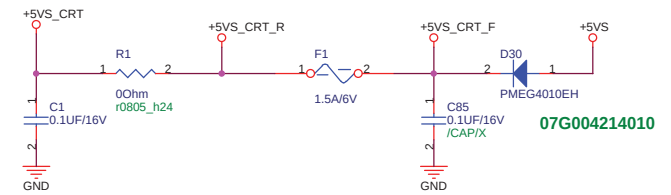
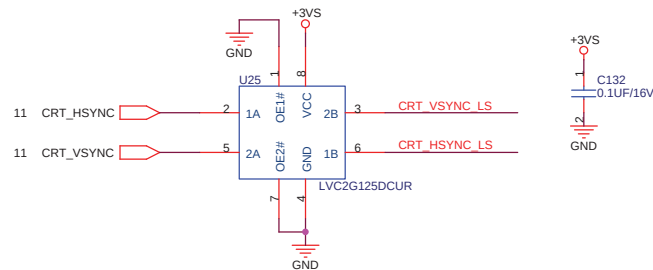
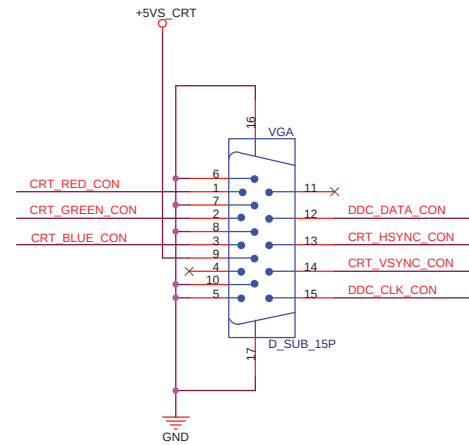
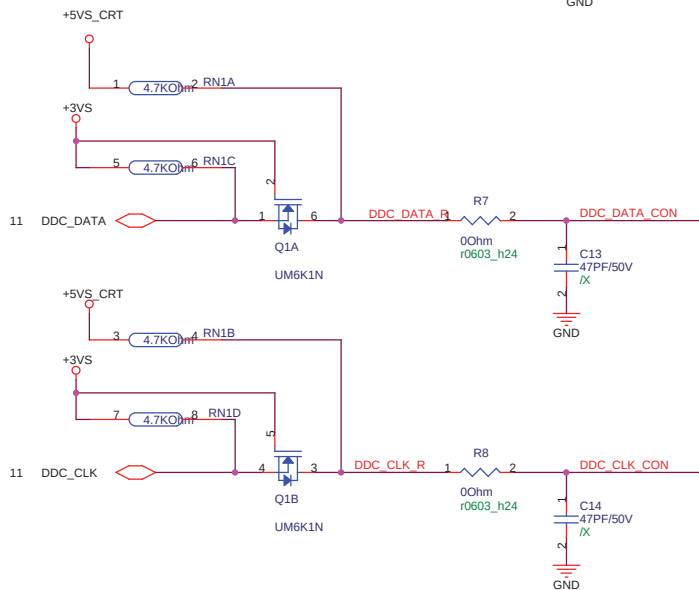
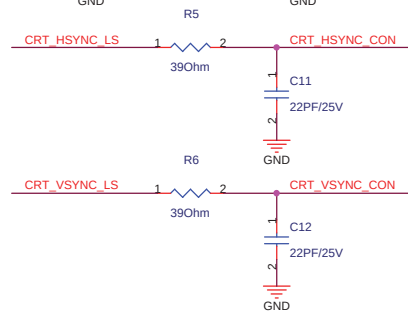
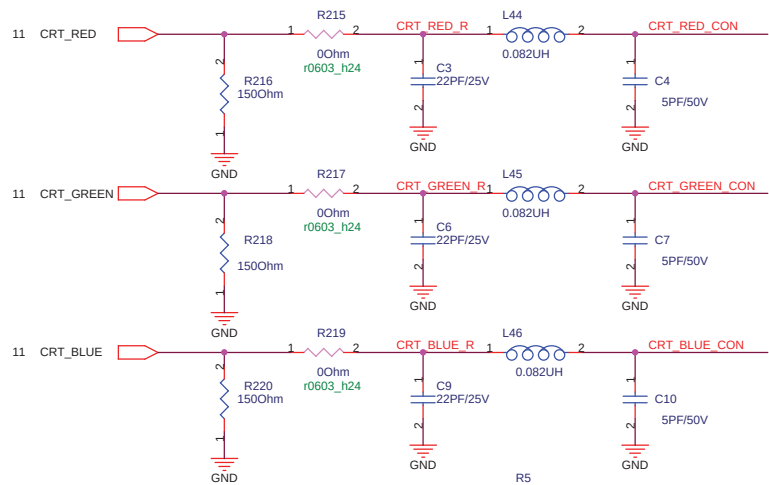
A

A



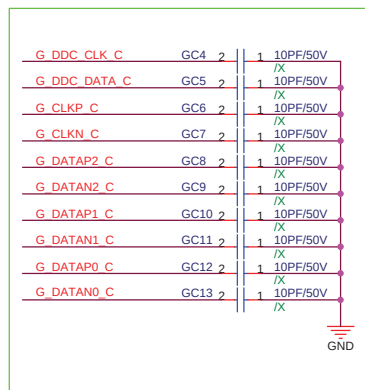
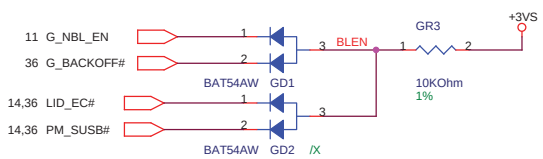
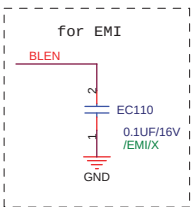
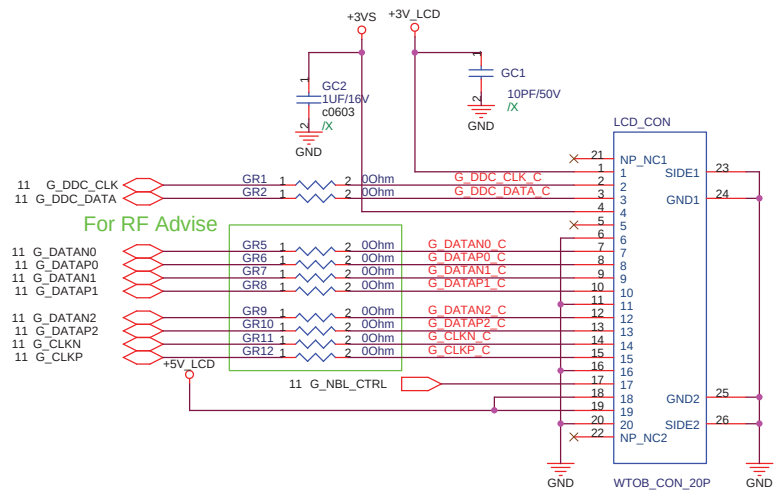
Default Group-A7V8X MX

ASUS		Title : Onboard_DRAM_1	
ASUSTek COMPUTER INC		Engineer: Fehling_wang	
Size	Project Name	Rev	
A3	900SD_MB	R1.0C	
Date: Monday, November 10, 2008		Sheet 20 of 51	

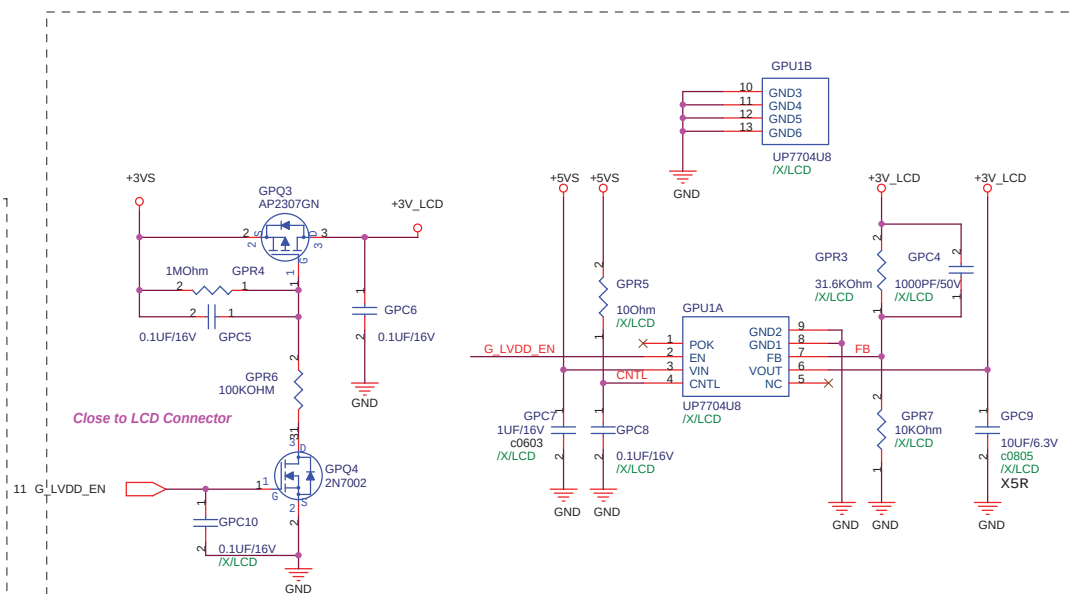
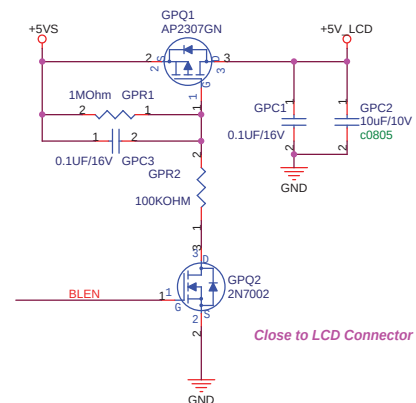
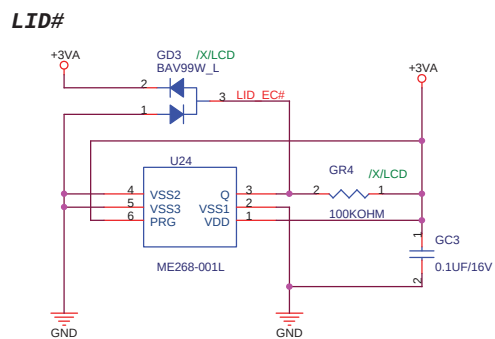


Default Group-A7V8X MX

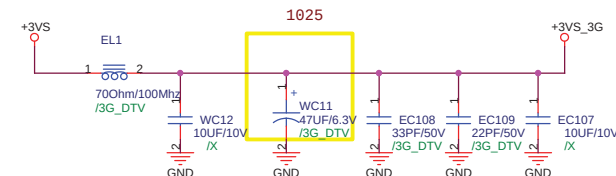
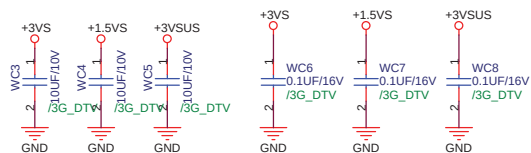
ASUS		Title : Onboard VGA	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name		Rev
A3	900SD_MB		R1.0G
Date: Monday, November 10, 2008		Sheet	22 of 51

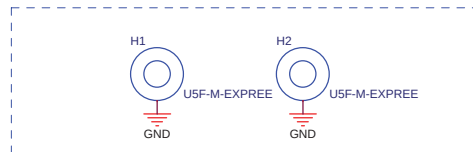
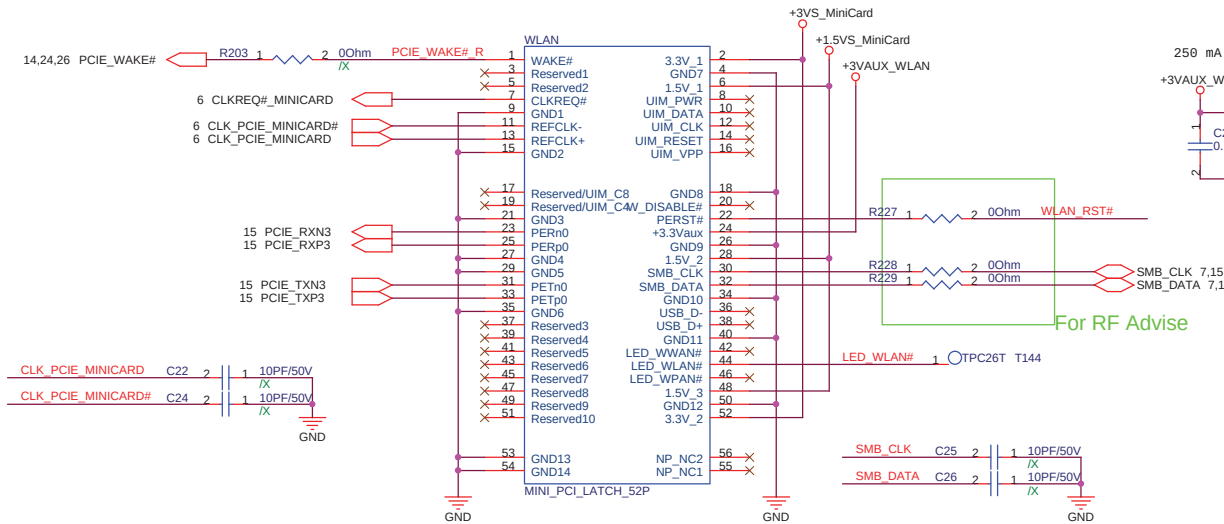


For RF Advise(Close to LCD_CON)

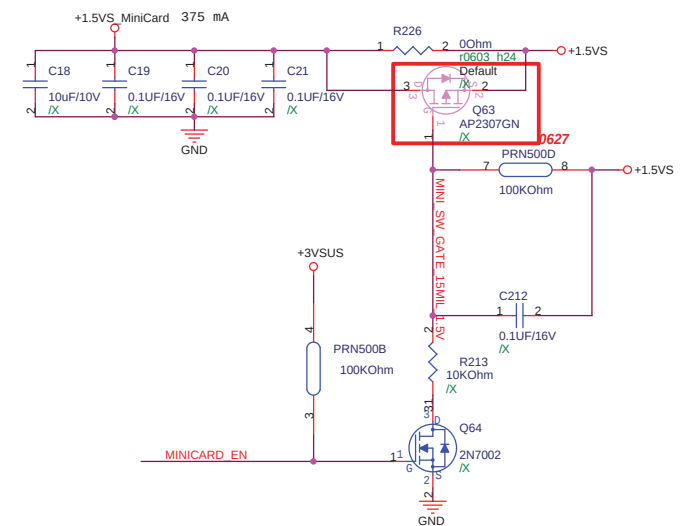
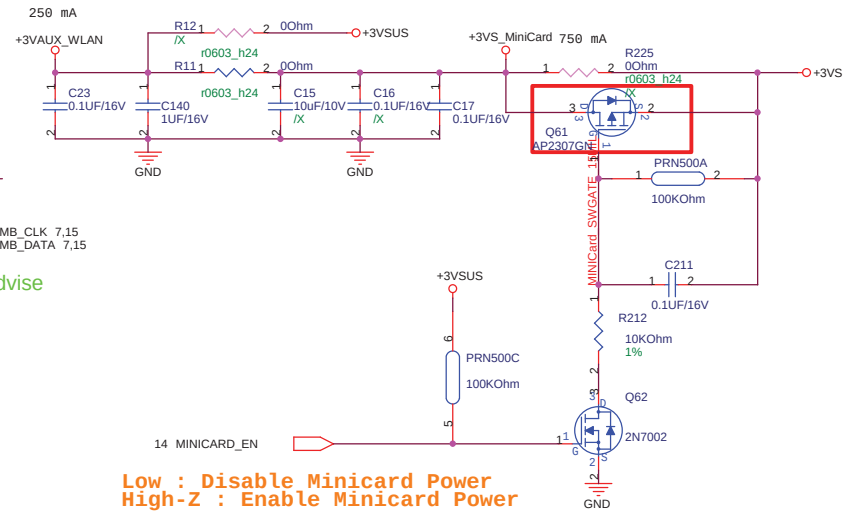
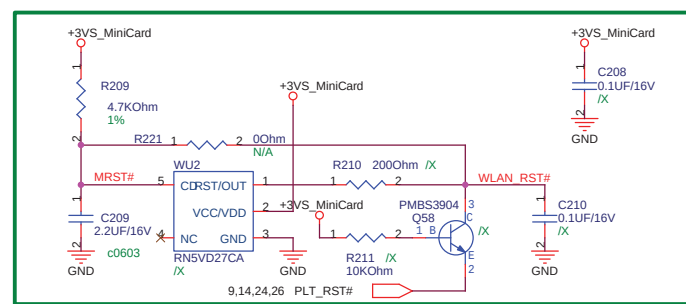
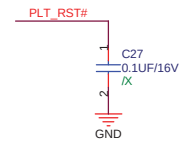


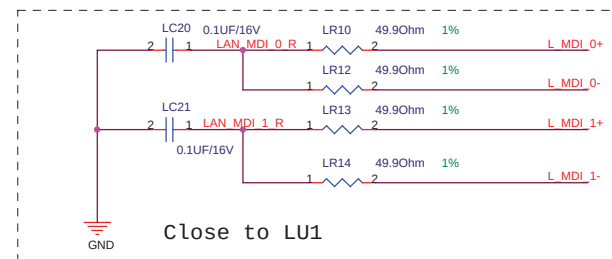
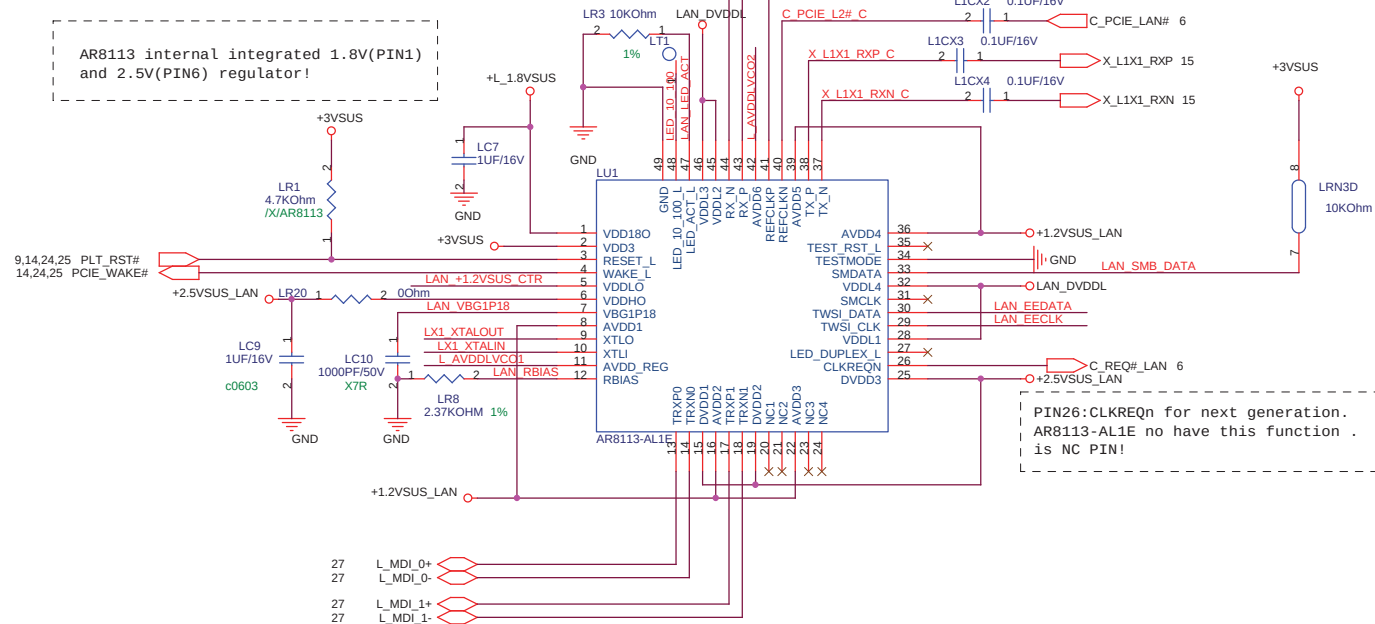
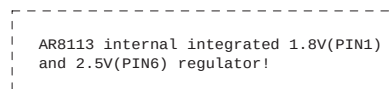
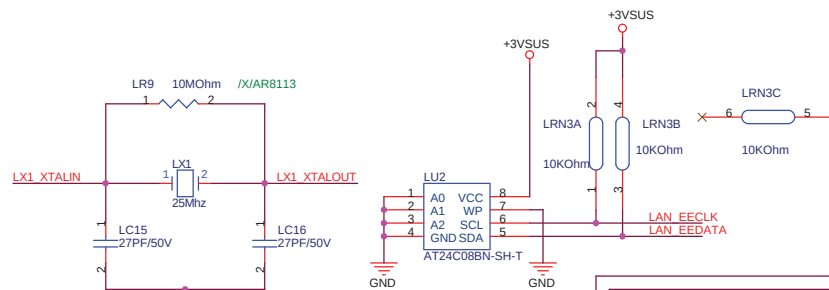
Default Group-A7V8X MX





MINI CARD NUT(1.6mm) *2

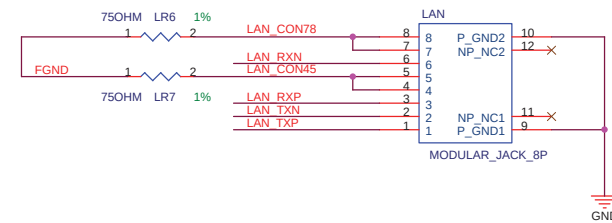
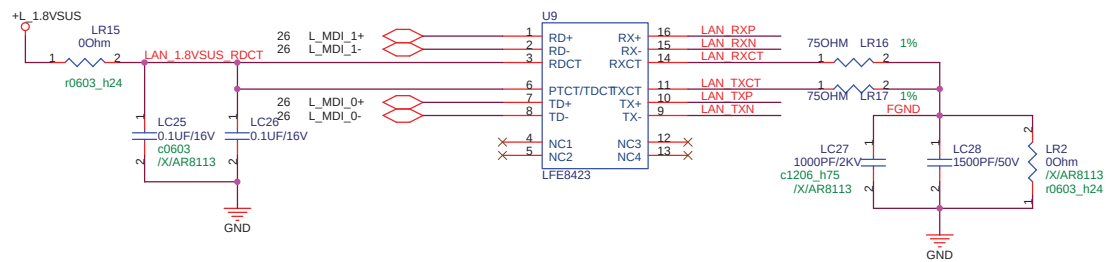


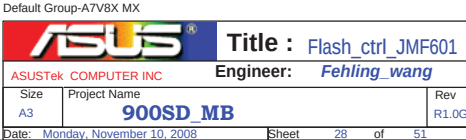


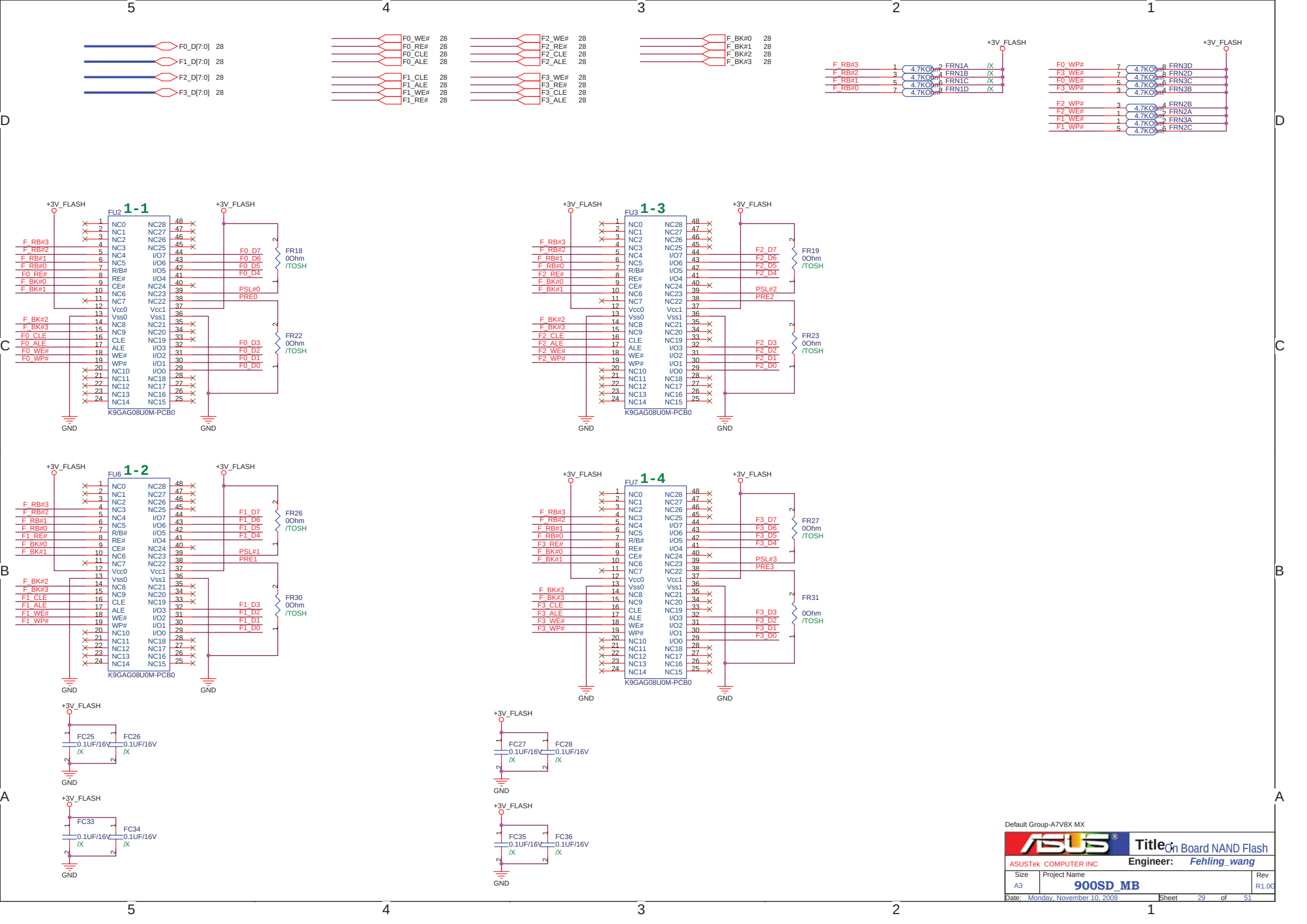
Default Group-A7V8X MX

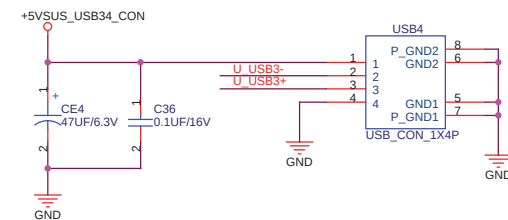
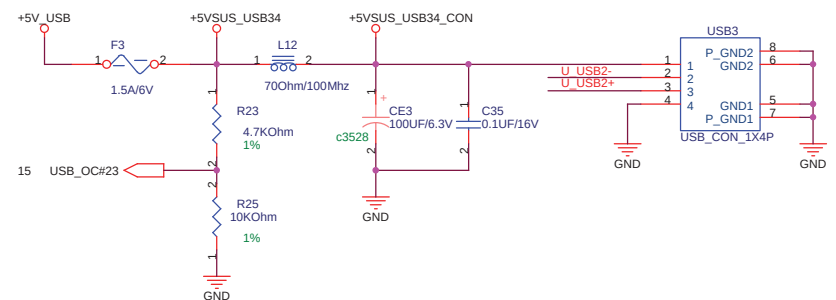
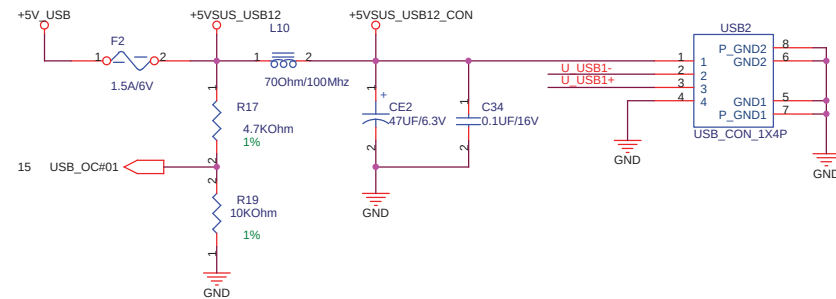
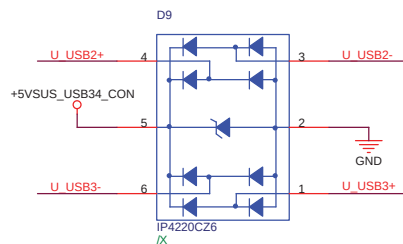
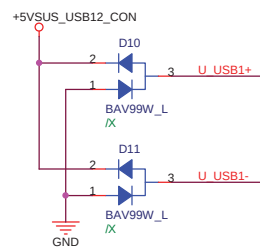


DELETE MODEM



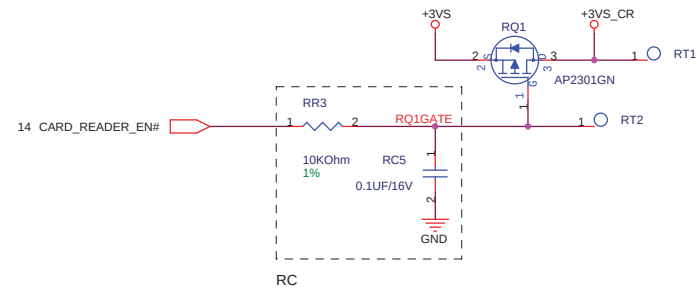
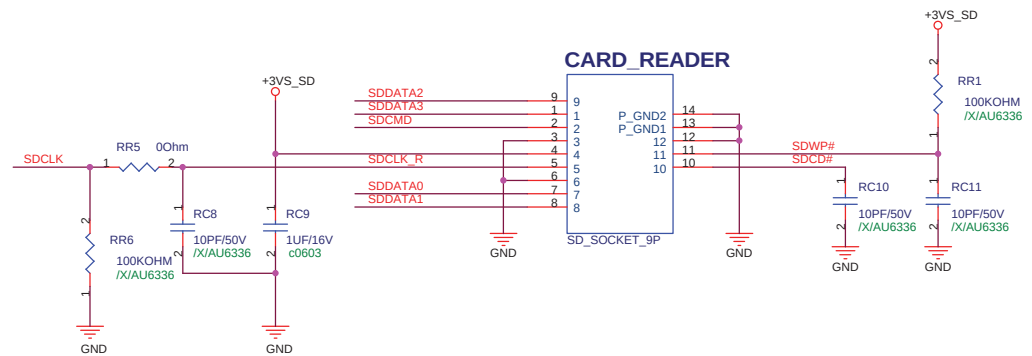


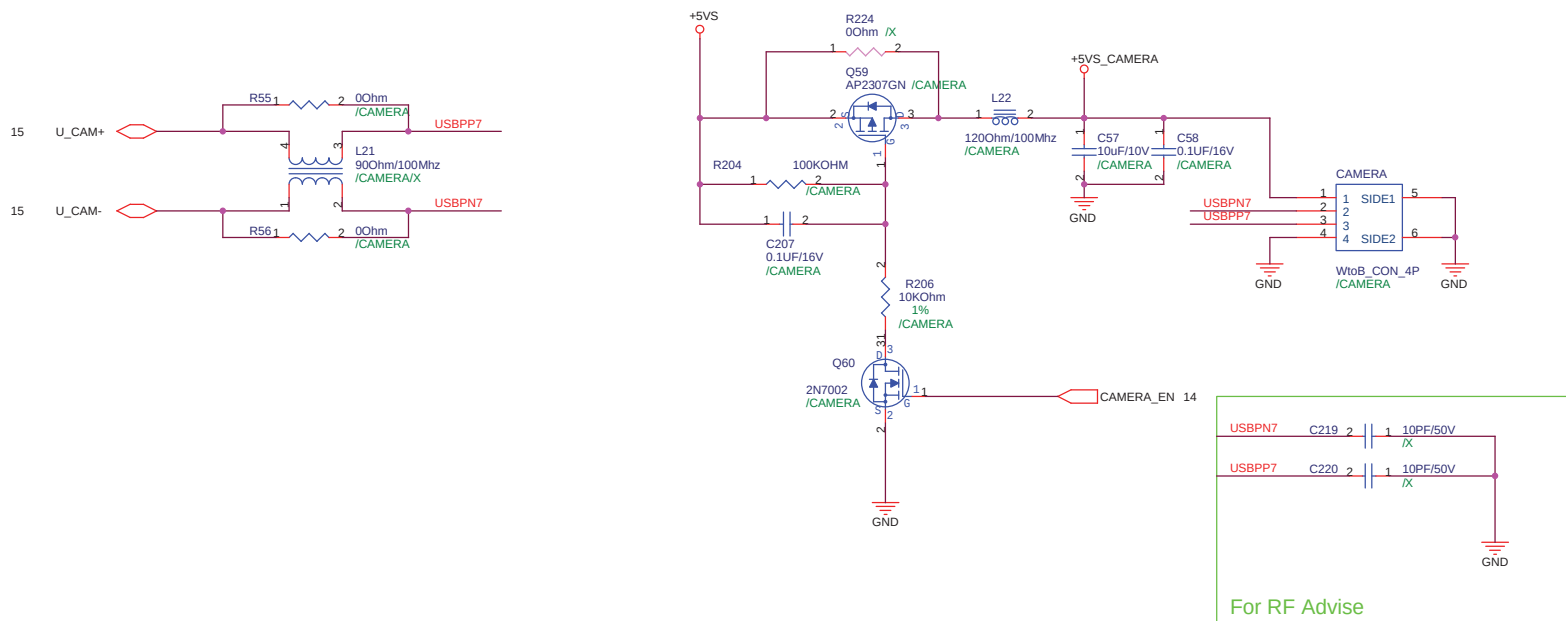




Default Group-A7V8X MX

ASUS		Title : USB Port	
ASUSTek Computer INC.		Engineer: Kell Huang	
Size A3	Project Name 900SD_MB	Date: Monday, November 10, 2008	Rev R1.0G
Sheet 30 of 51			

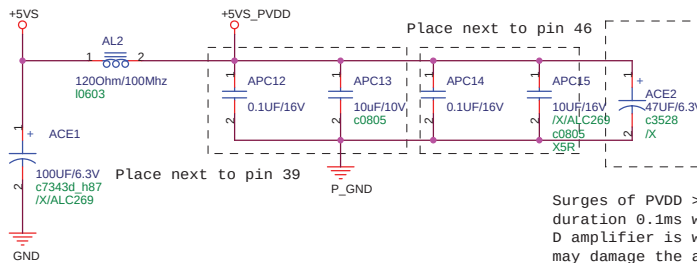
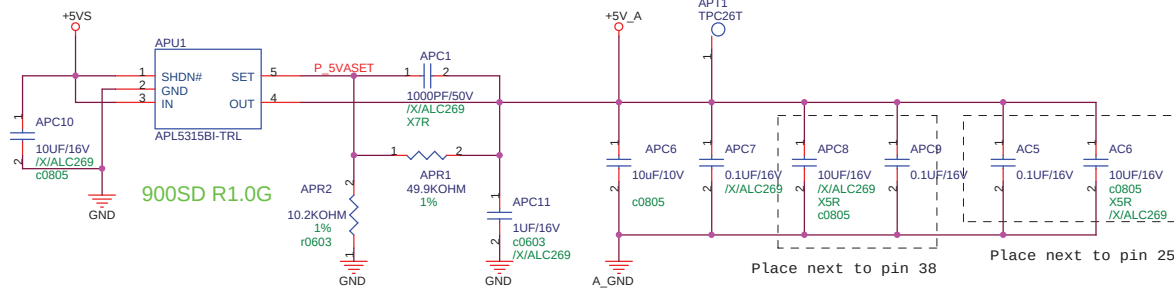




Default Group-A7V8X MX

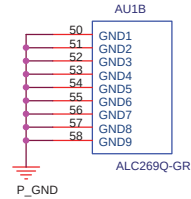
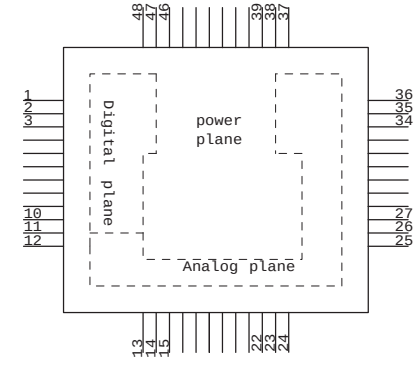
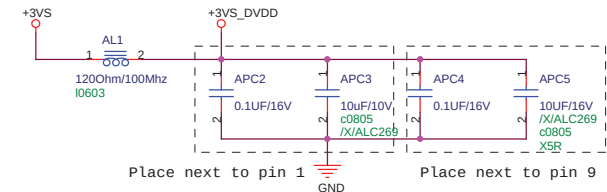
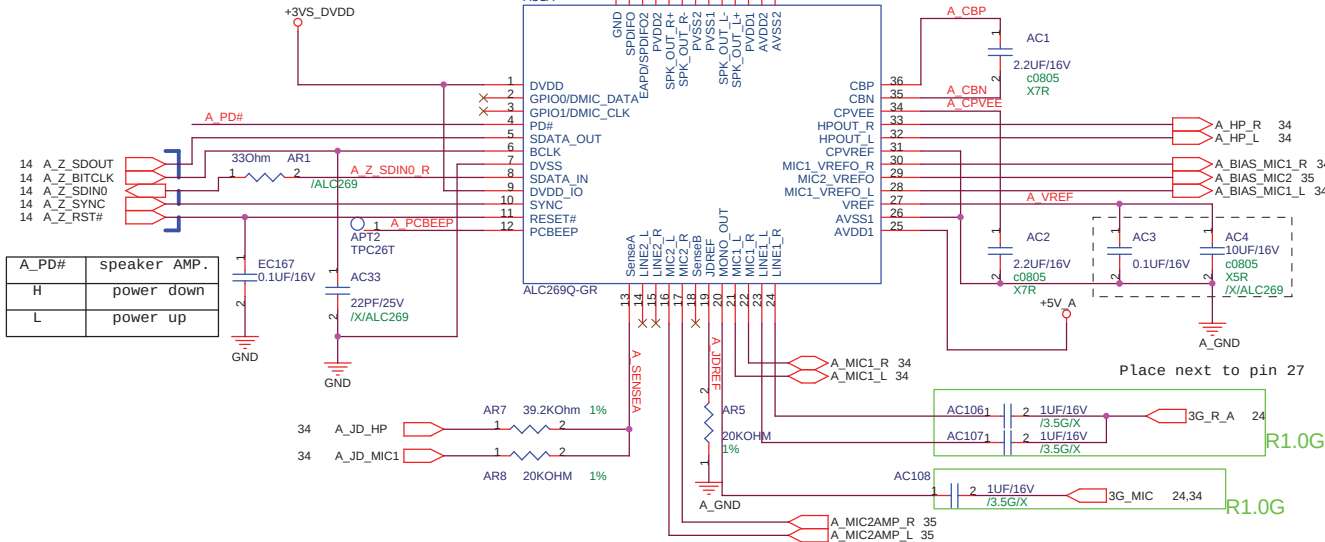
ASUS		Title : Camera Conn	
ASUSTek Computer INC.		Engineer: <i>Kell Huang</i>	
Size A3	Project Name 900SD_MB	Rev R1.0G	
Date: Monday, November 10, 2008	Sheet 32 of 51		

$$V_{out} = 0.8 * (1 + (49.9K / 10.2K))$$

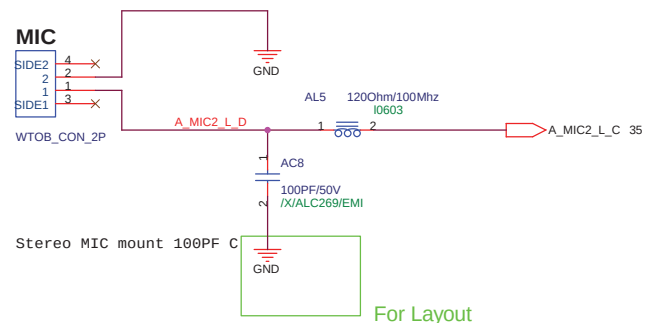


Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to upress the surge.

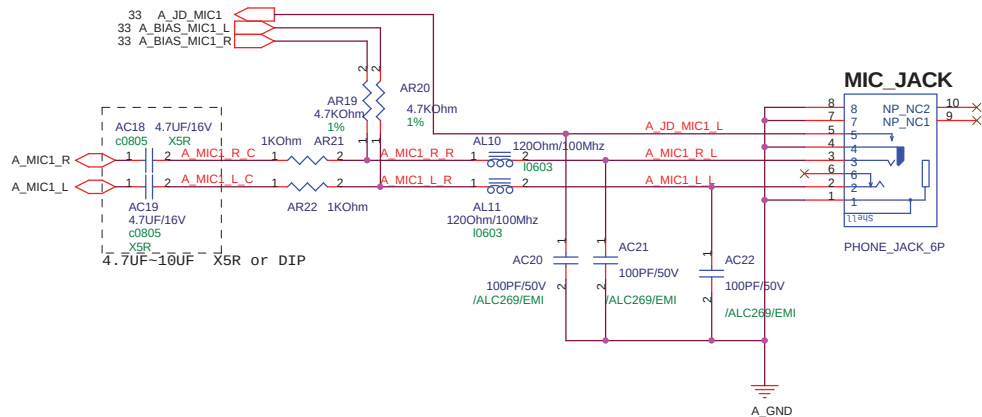
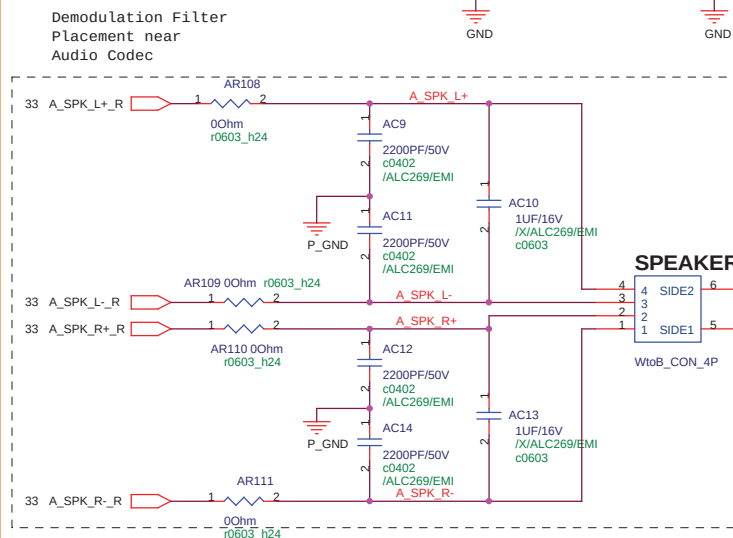
A_PD#	speaker AMP.
H	power down
L	power up



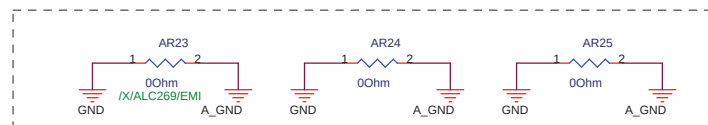
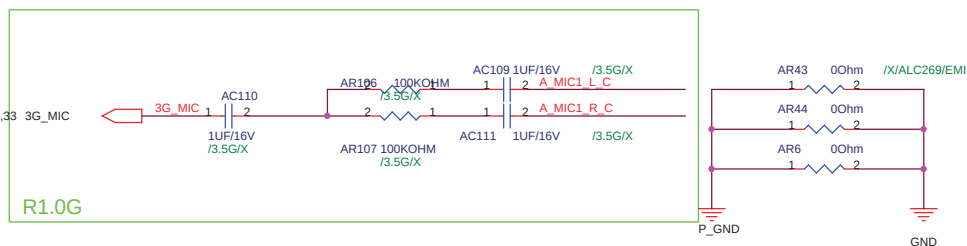
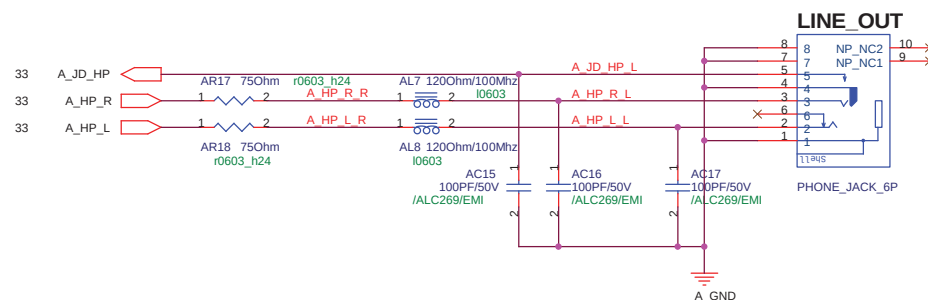
Internal MIC



SPEAKER



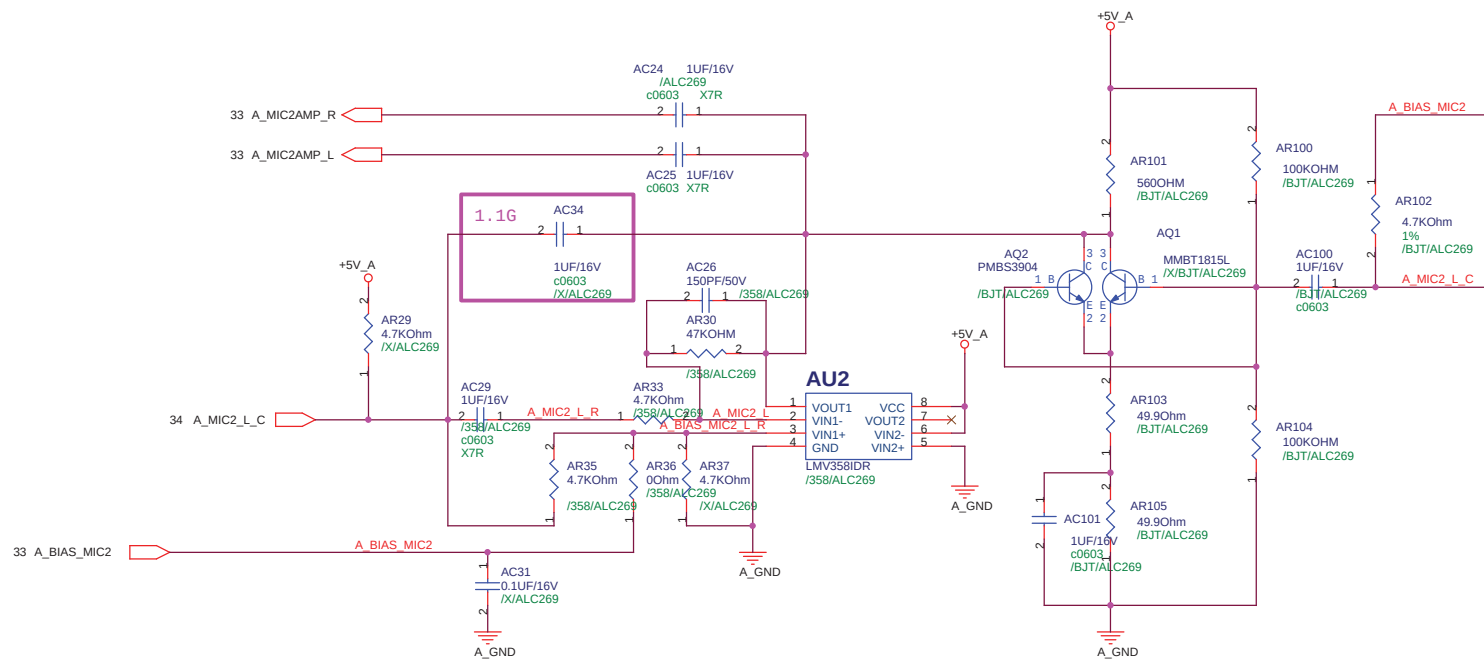
HP



AR24, AR25 can use
0.1uF 11G233310432320
for EMI

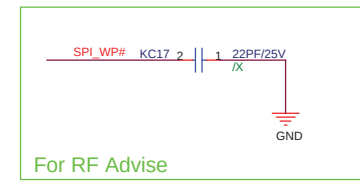
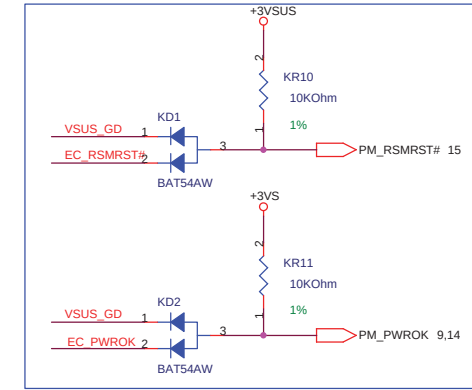
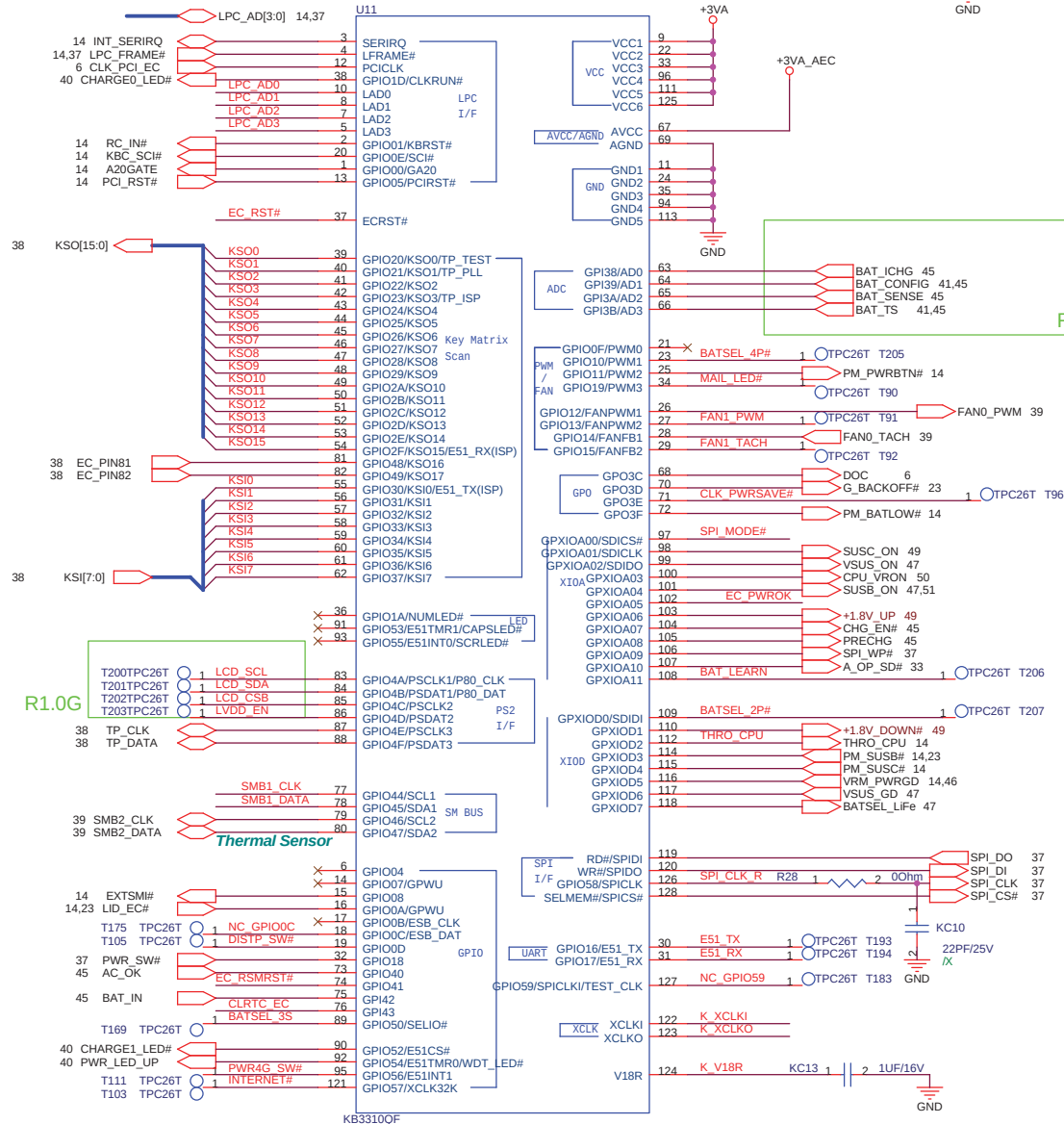
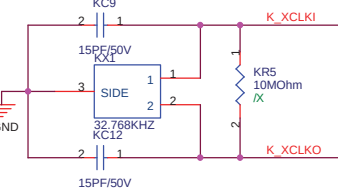
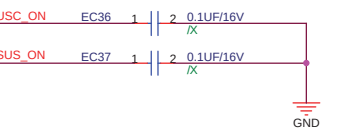
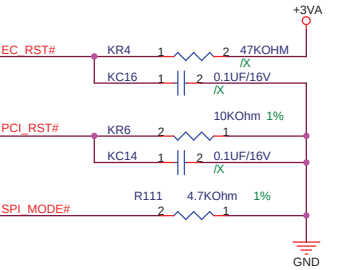
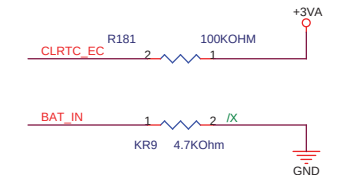
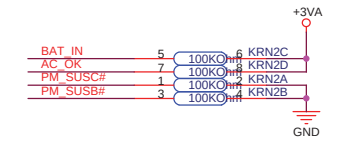
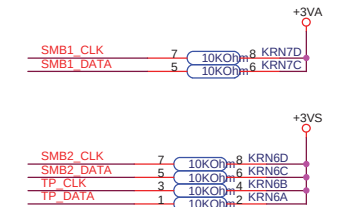
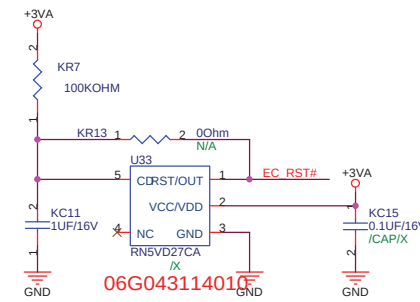
Default Group-A7V8X MX

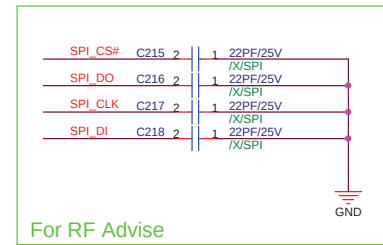
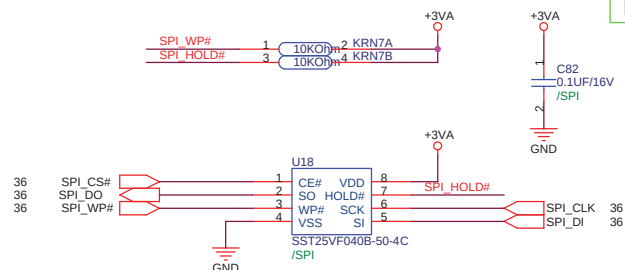
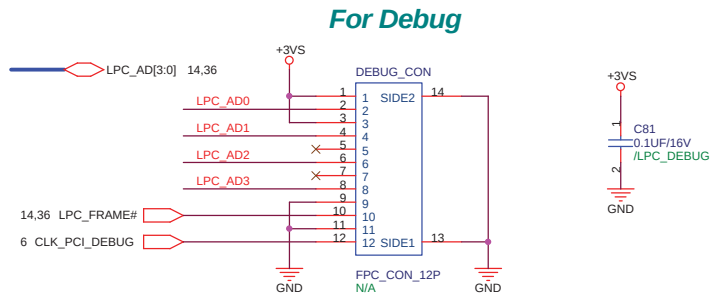
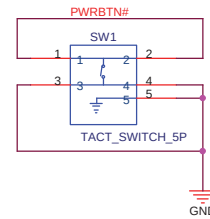
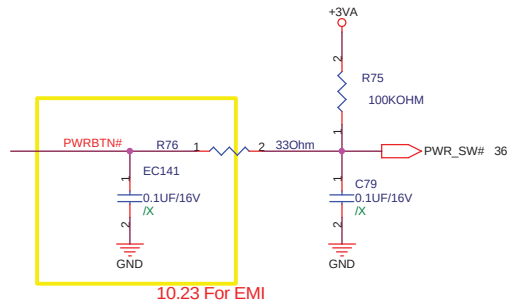
ASUS		Title : ALC269-2(I/O)	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size A3	Project Name 900SD_MB	Rev R1.0G	
Date: Monday, November 10, 2008	Sheet 34 of 51		



Default Group-A7V8X MX

ASUS		Title : ALC269-3(MIC AMP)	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size	Project Name		Rev
A3	900SD_MB		R1.0G
Date: Monday, November 10, 2008		Sheet	35 of 51

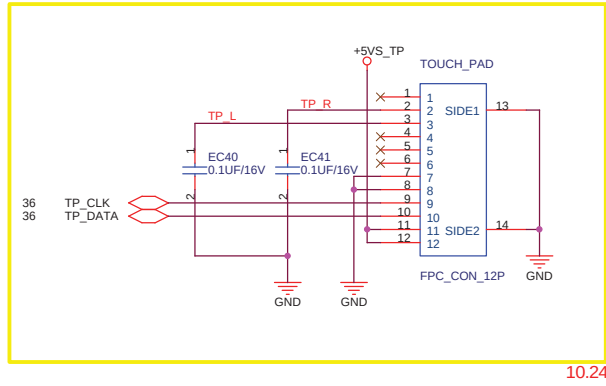
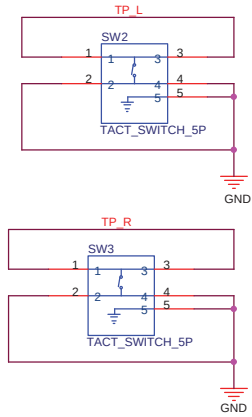




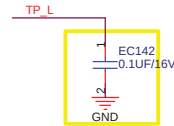
Default Group-A7V8X MX

ASUS		Title : Switch_SPI ROM	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name		Rev
A3	900SD_MB		R1.0G
Date: Monday, November 10, 2008		Sheet	37 of 51

For Touch-Pad

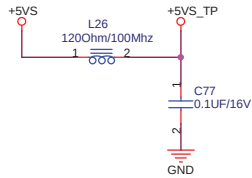


10.24

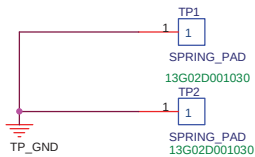
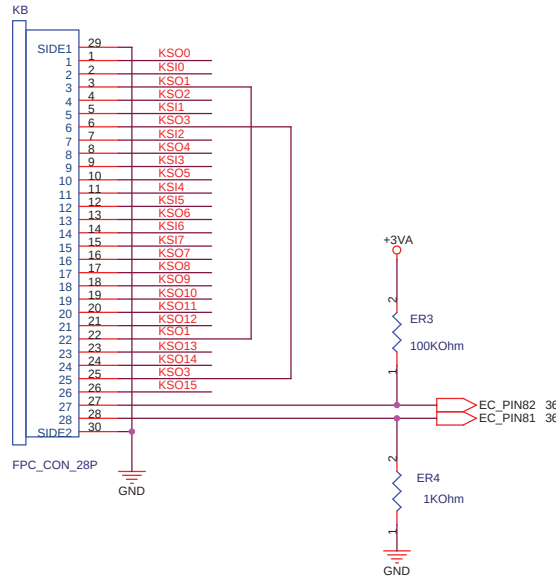


10.23 For EMI

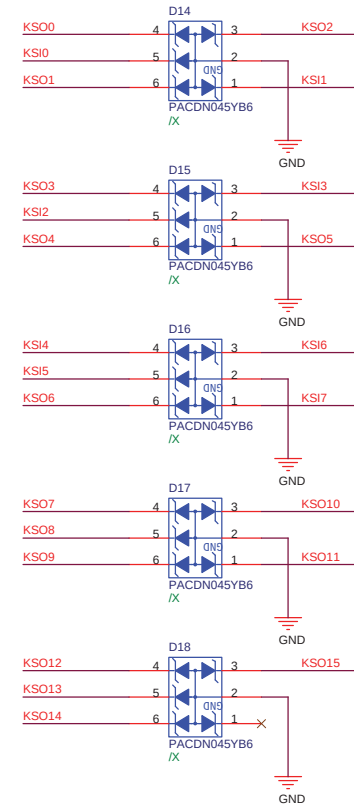
For Keyboard



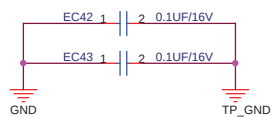
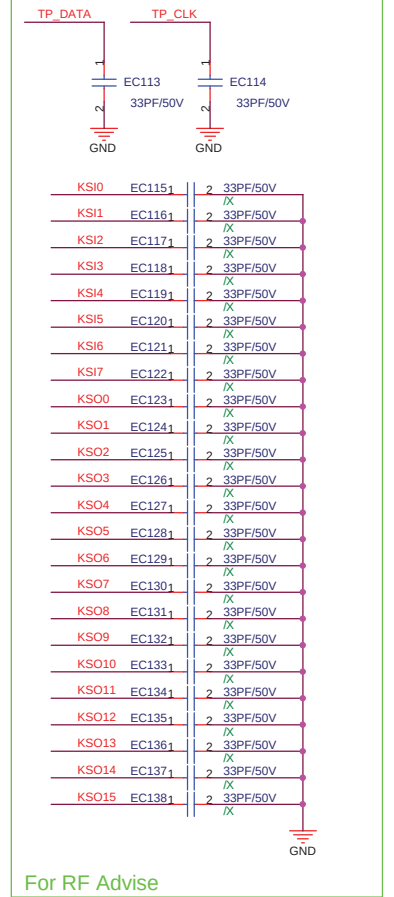
KSO15 1 TPC26T T188
KSI0 1 TPC26T T189
KSO3 1 TPC26T T190



KSO[15:0] 36
KSI[7:0] 36



For RF Advise



Default Group-A7V8X MX

ASUS		Title : KB_Touch Pad	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A3	Project Name 900SD_MB	Rev R1.0G	
Date: Monday, November 10, 2008		Sheet 38 of 51	

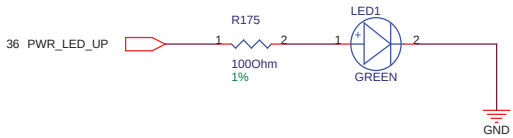


Default Group-A7V8X MX

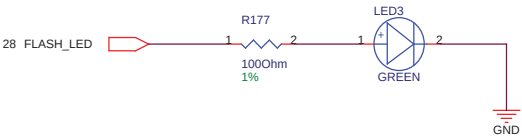


Title : Thermal Sensor_FAN

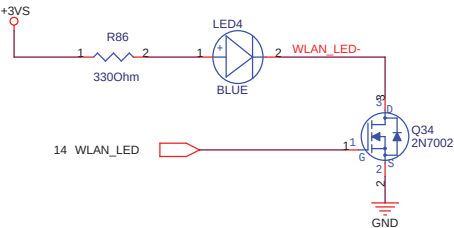
for POWER LED



for FLASH LED

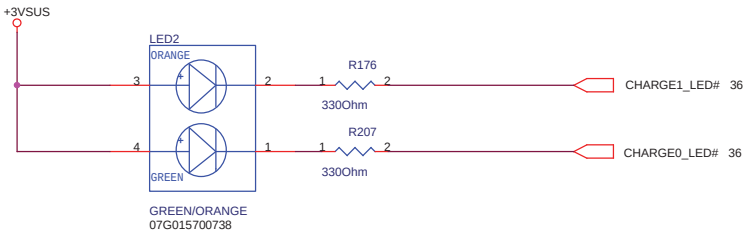


for WLAN LED



R1.0G

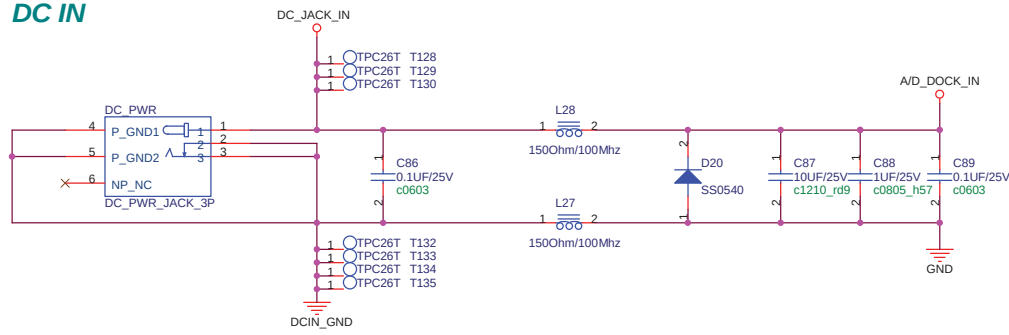
for CHARGE LED



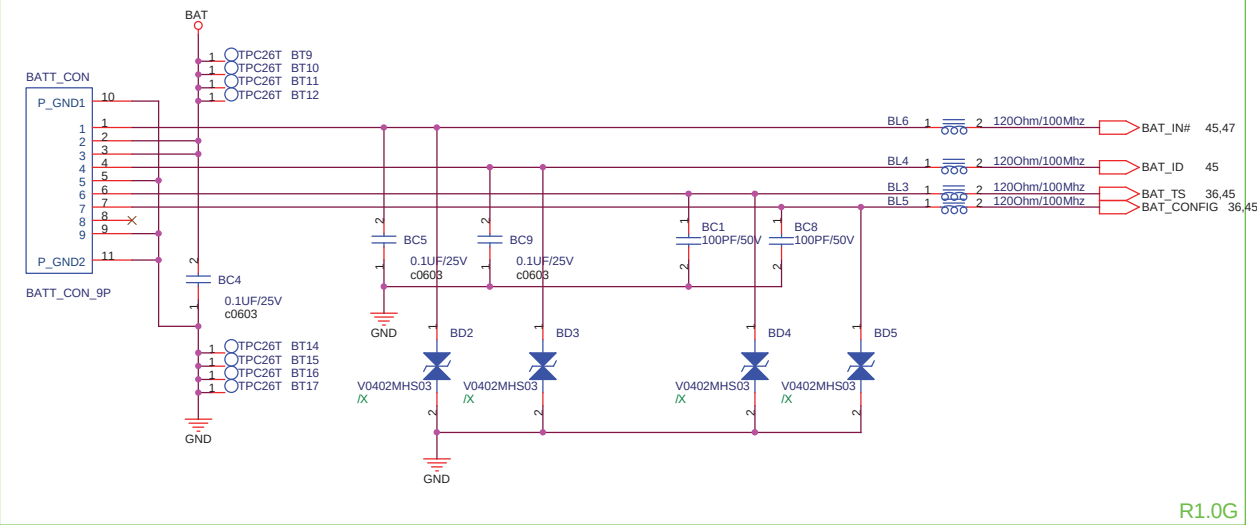
Default Group-A7V8X MX

ASUS		Title : LED	
ASUSTek Computer INC.		Engineer: Hauld_Zhou	
Size A3	Project Name 900SD_MB	Rev R1.0G	
Date: Monday, November 10, 2008		Sheet 40 of 51	

DC IN



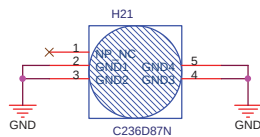
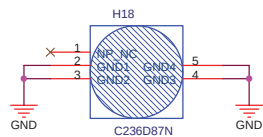
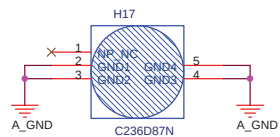
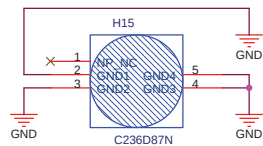
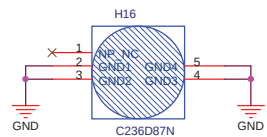
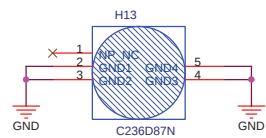
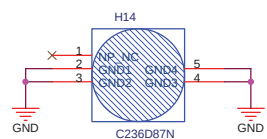
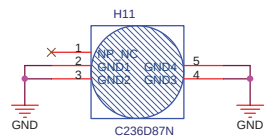
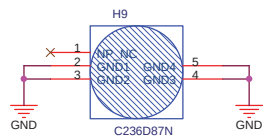
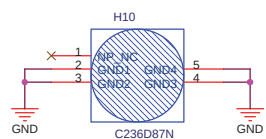
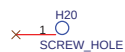
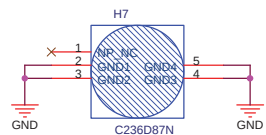
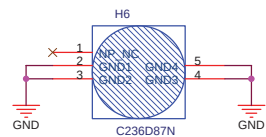
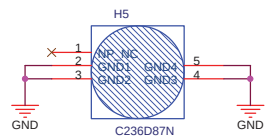
BAT IN

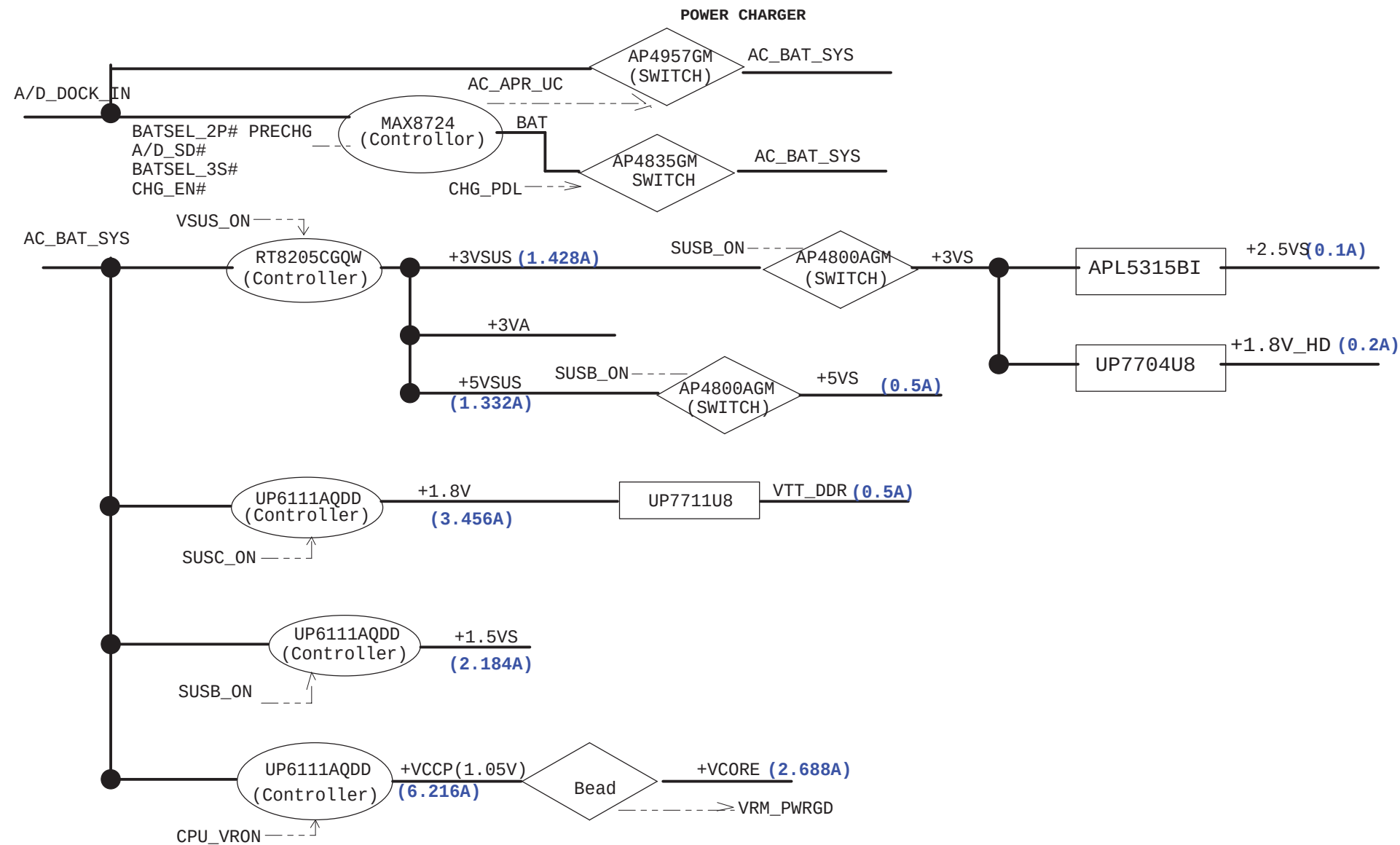


R1.0G

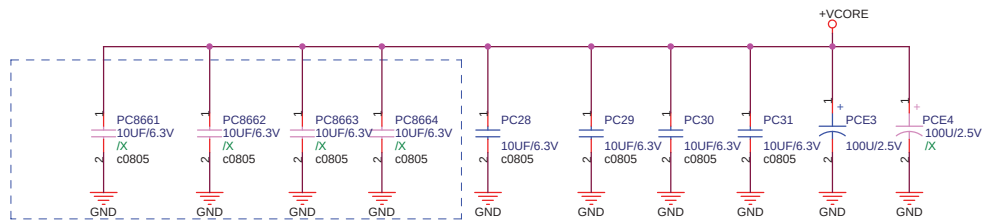
Default Group-A7V8X MX

		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A3	Project Name 900SD_MB		Rev R1.0G
Date: Monday, November 10, 2008	Sheet	41 of 51	

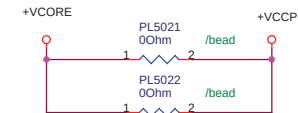
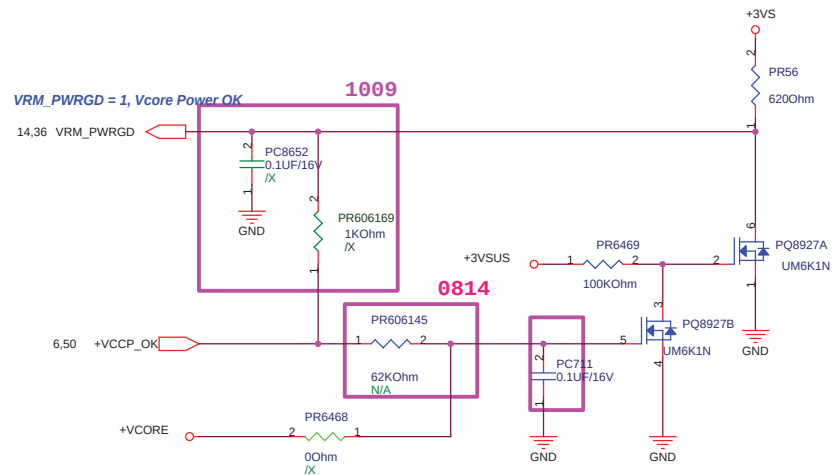




+Vcore / 7A

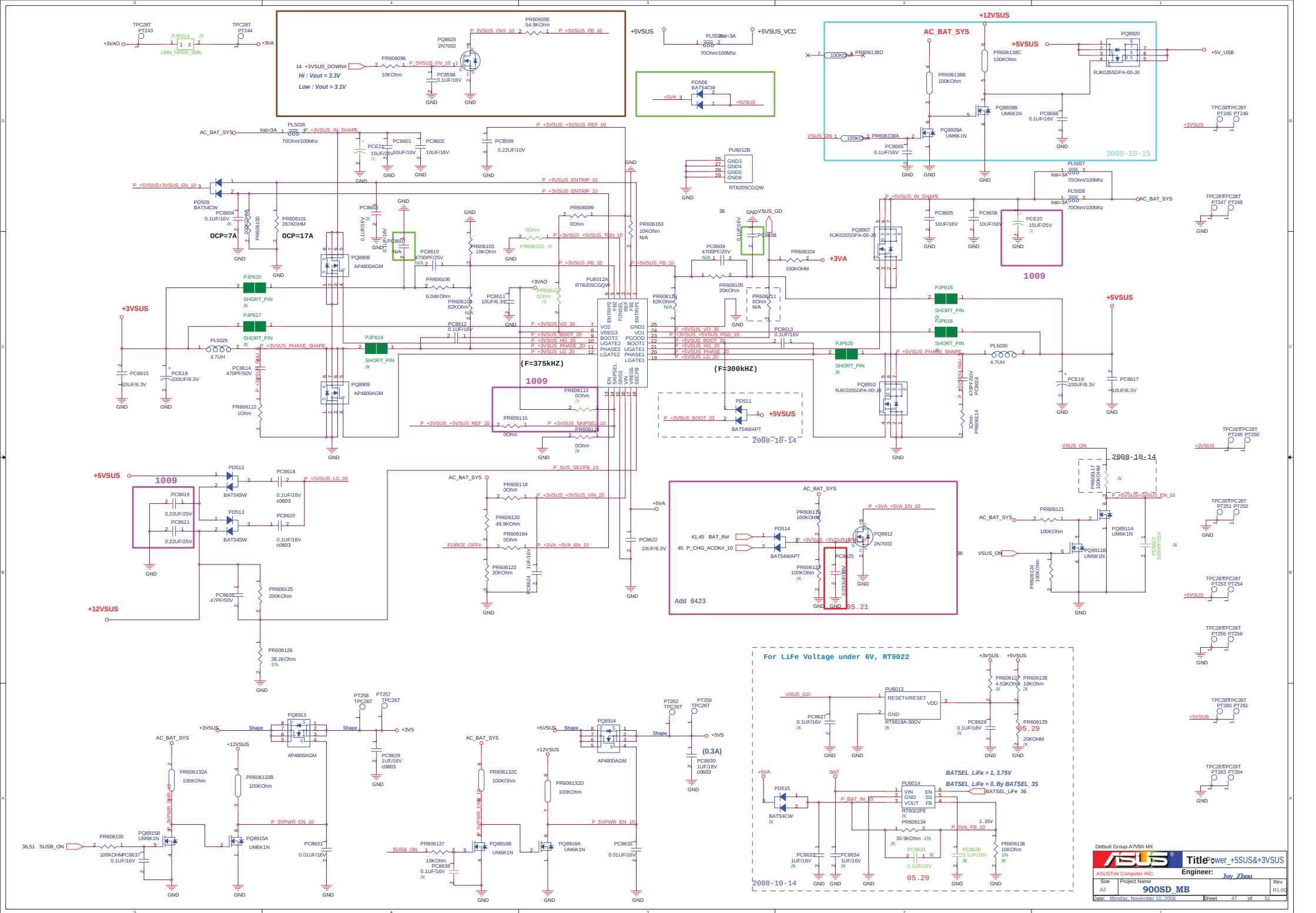


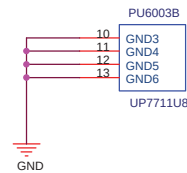
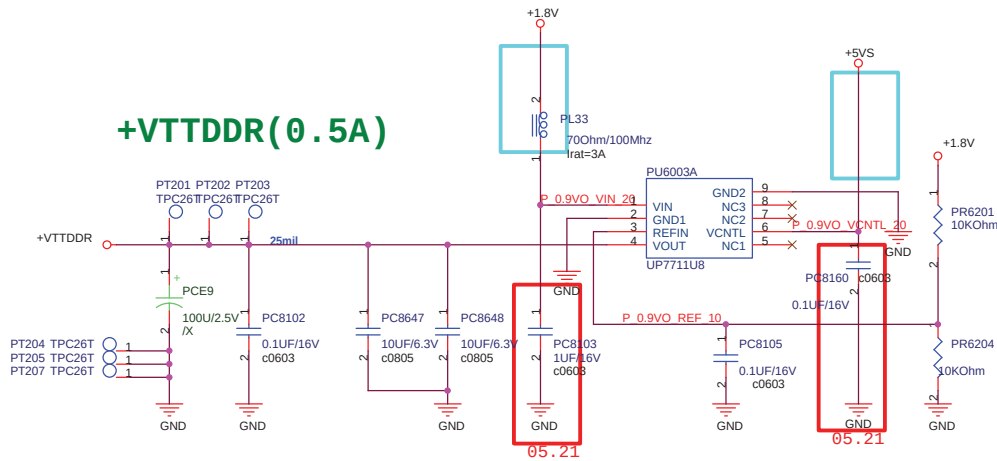
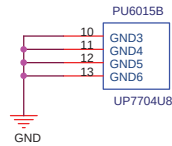
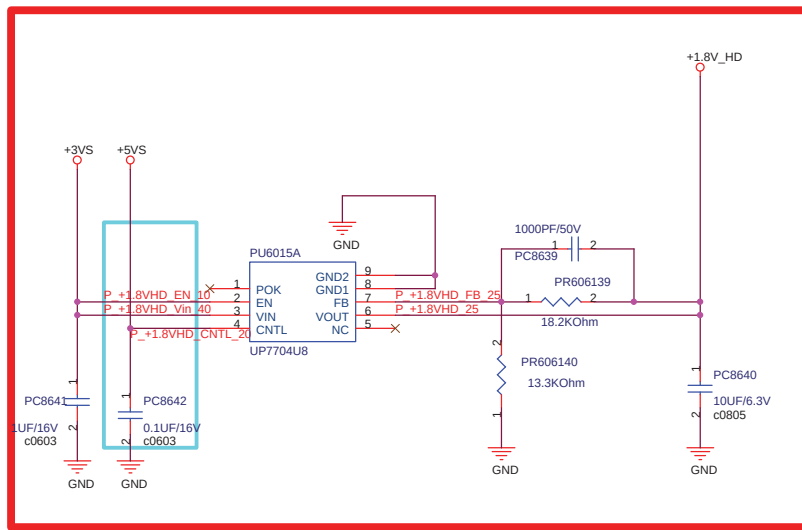
2008-10-15



Default Group-A7V8X MX

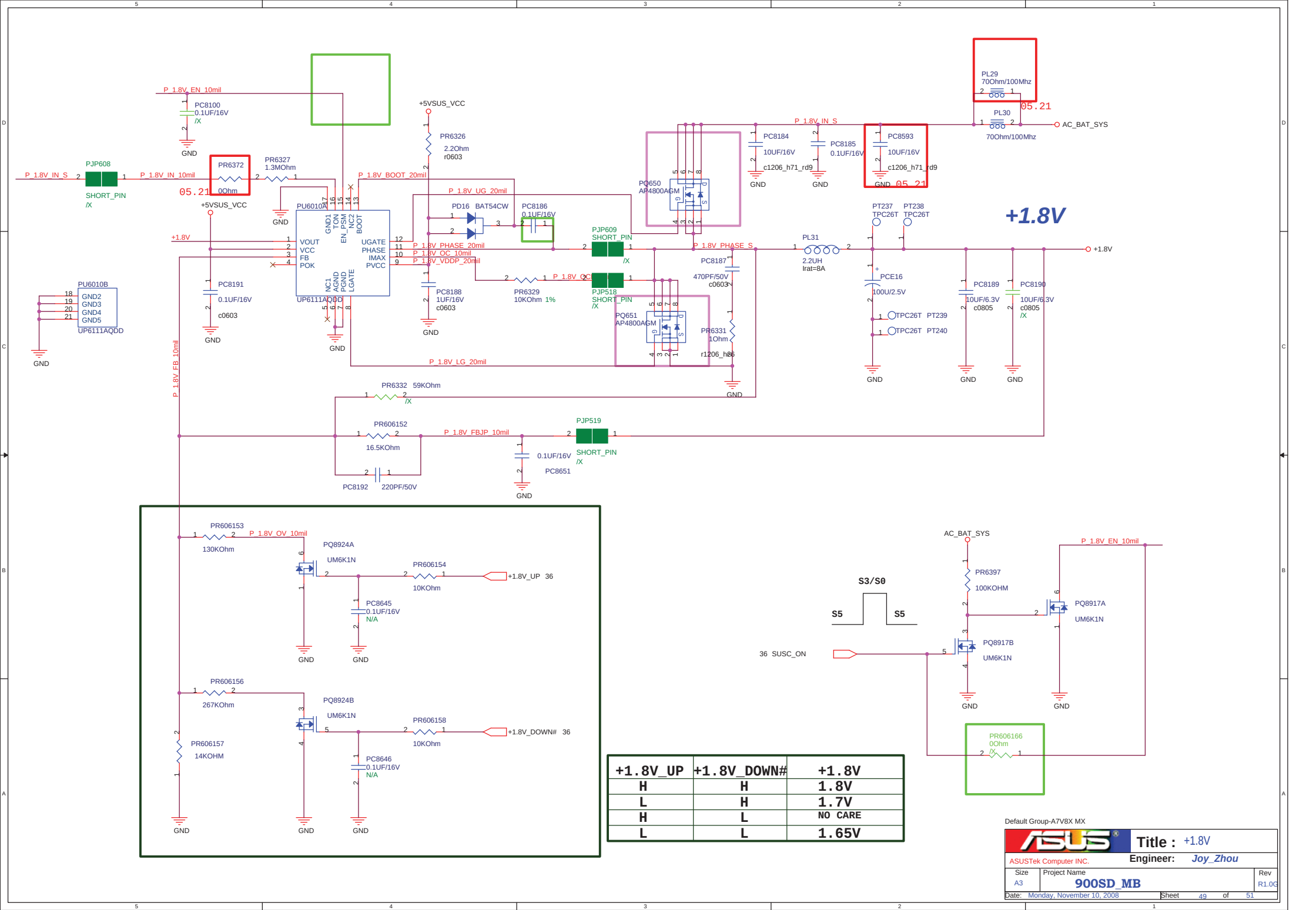


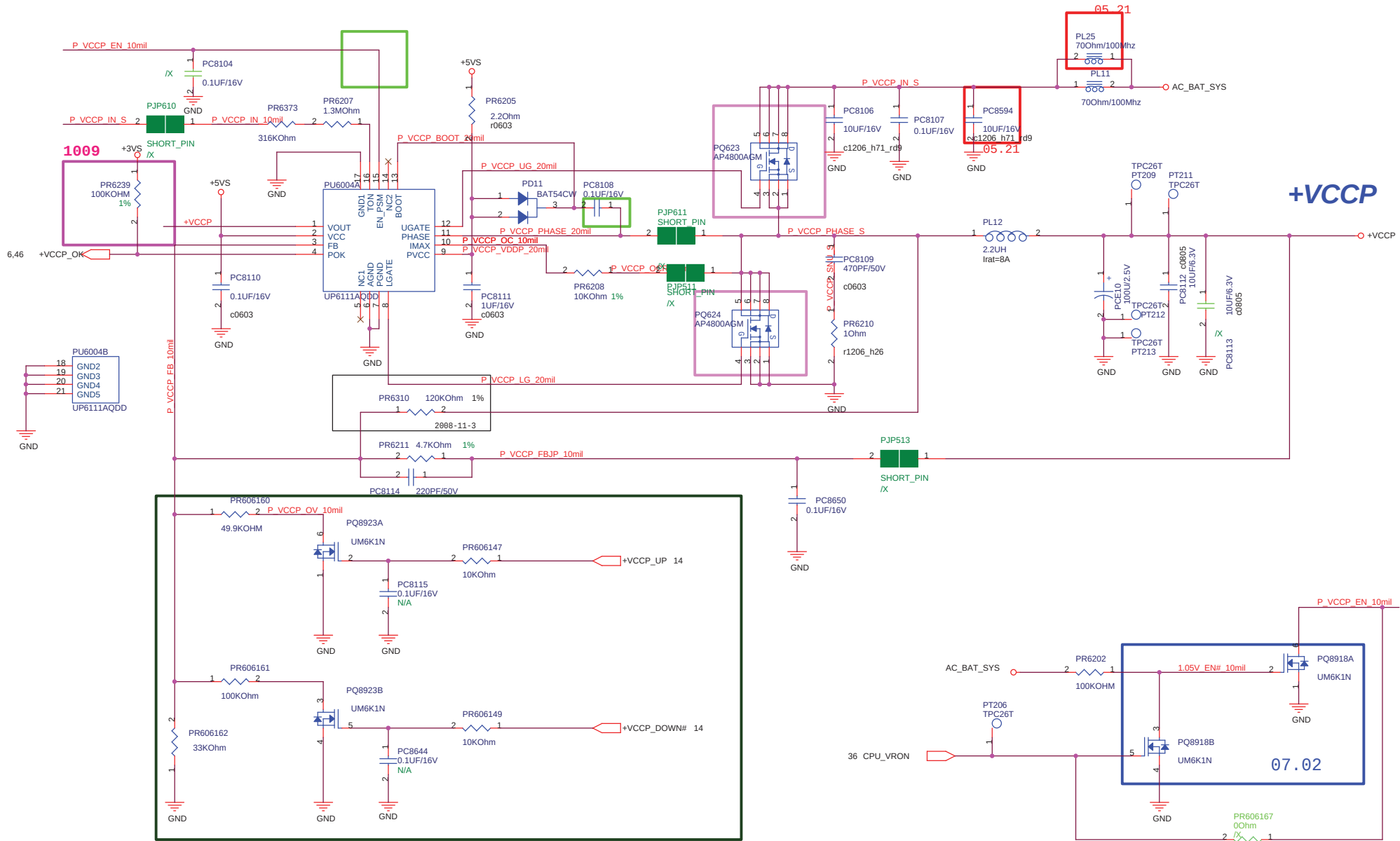




Default Group-A7V8X MX

ASUS		Title : 1.8VHD_VTT_DDR	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size A3	Project Name 900SD_MB	Rev R1.0G	
Date: Monday, November 10, 2008		Sheet 48 of 51	





+VCCP_UP	+VCCP_DOWN#	+VCCP	
H	H	0.96V	0.955V
L	H	0.89V	0.886V
H	L	NO CARE	
L	L	0.85V	0.852V

Default Group-A7V8X MX

ASUS		Title : VCCP	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size A3	Project Name 900SD MB	Rev R1.0G	
Date: Monday, November 10, 2008	Sheet 50	of 51	

