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MS-7B17

ATX

Ver: 11

CFL Platform

CPU:

Coffee lake S

System Chipset:

Z390 PCH_H

Onboard Chip:

HD Audio Codec:ALC1220P

LAN-Intel I219

SIO:NTC6797

Flash ROM: SPI 128 MB X1

Main Memory:

*DDRIV (5000MHz) * 4 (Dual Channel)*

ACPI:

LDO

PWM:

IMVP8 -UPI9521

Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X8) Slot * 1*

*PCI Express (X4) Slot * 1*

*PCI Express (X1) Slot * 3*

*M2 (X4) Slot * 2*

Other:

*SATA3.0 *6*

*USB2.0 *7*

*REAL USB3.0 *5+TYPEC*1*

*FRONT USB3.0 *3+TYPEC*1*

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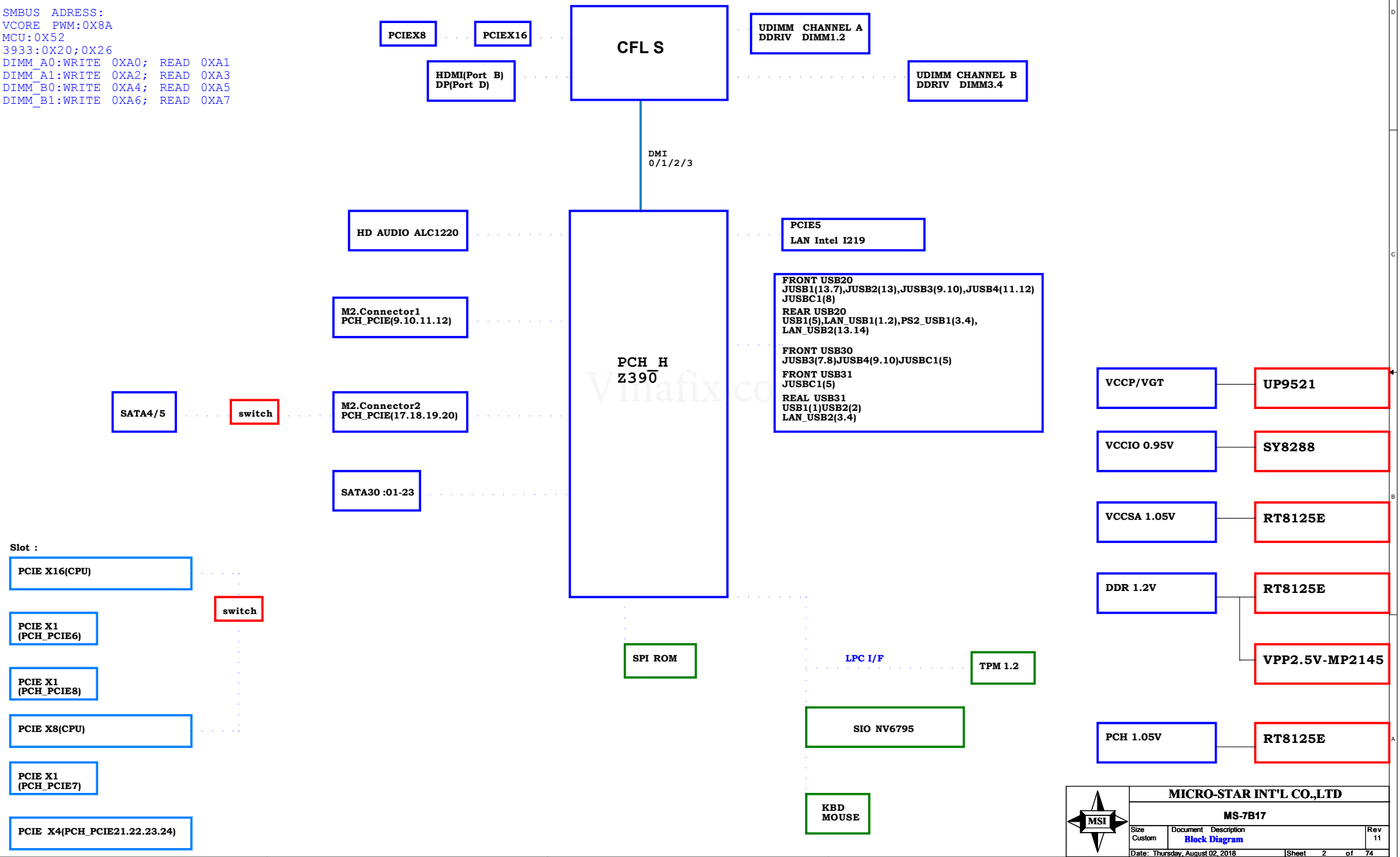
MS-7B17 Block Diagram

SMBUS ADRESS:
VCORE PWM:0X8A
MCU:0X52
3933:0X20;0X26
DIMM_A0:WRITE 0XA0; READ 0XA1
DIMM_A1:WRITE 0XA2; READ 0XA3
DIMM_B0:WRITE 0XA4; READ 0XA5
DIMM_B1:WRITE 0XA6; READ 0XA7



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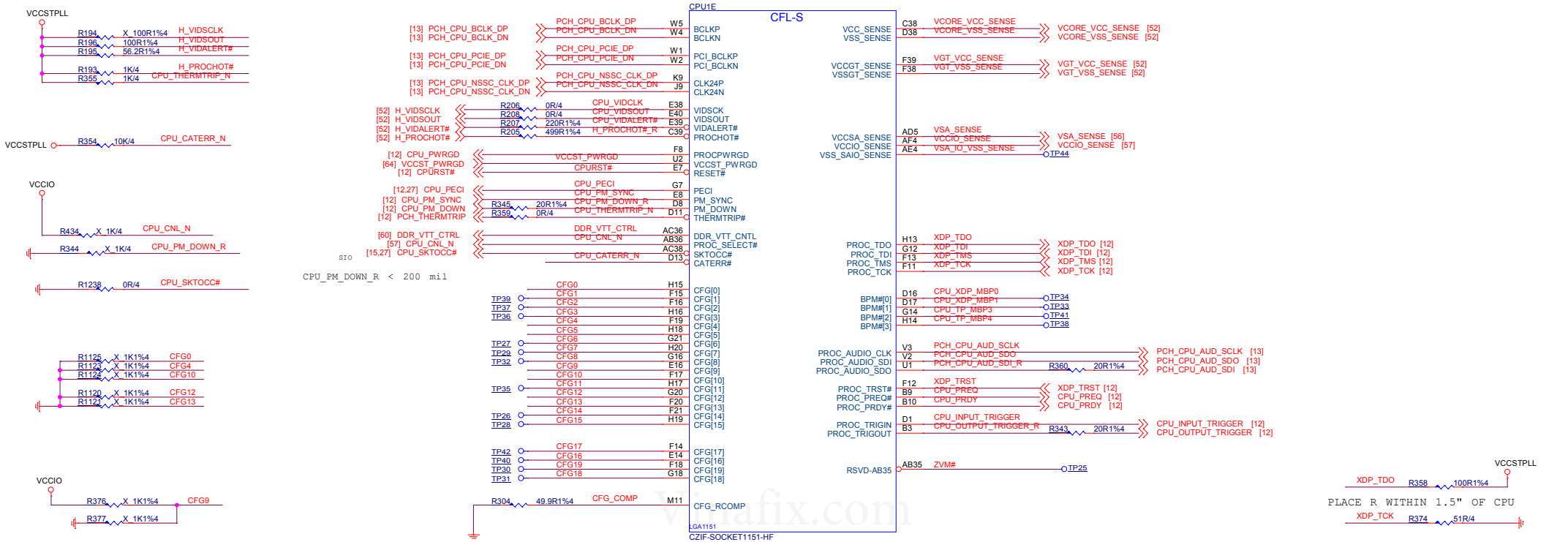
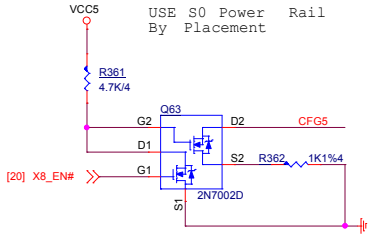
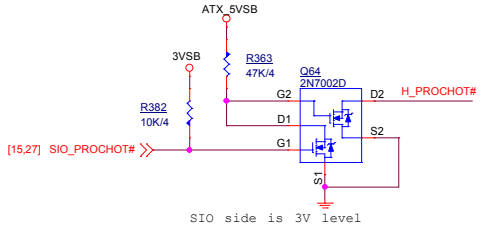


CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	NORM	STALL	EAR
1	NORM	PCHLESS	PCHLESS MODE
2	NORM	REVERSE	PEG LANE REVERSAL
3	ENABLE	DISABLE	DEBUG
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NO PRESENT	SVID NOT PRESENT
10	ACTIVATE	NO ACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI AC
12	SPT	NOT SPT	PCH TYPE
13	SVID	FIXED	VCCSA SVID
14	RSVD		
15	RSVD		





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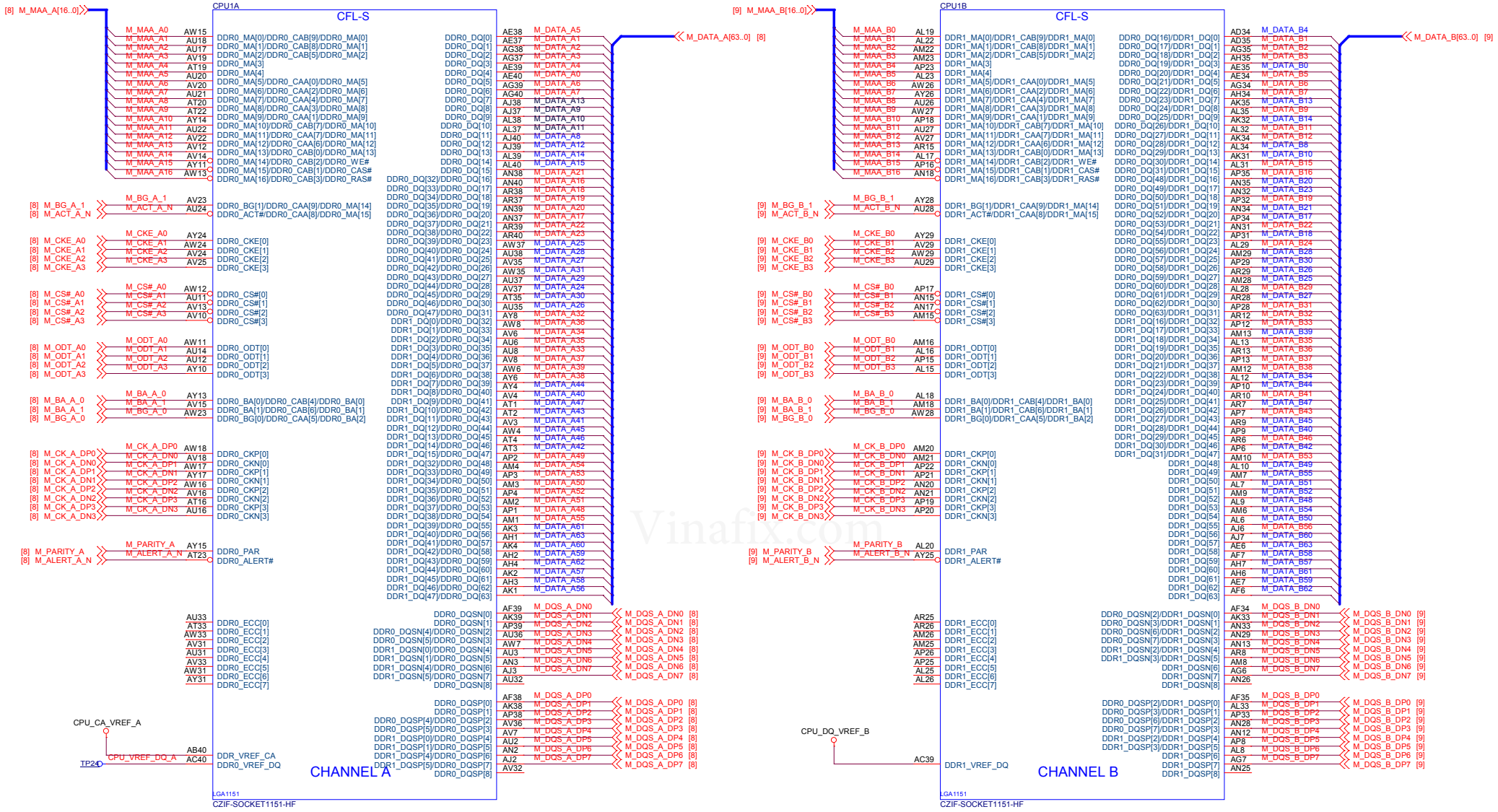
SOCKET PN N12-151A010-L06



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Size	Document Description	Rev
Custom	CPU-Memory	11

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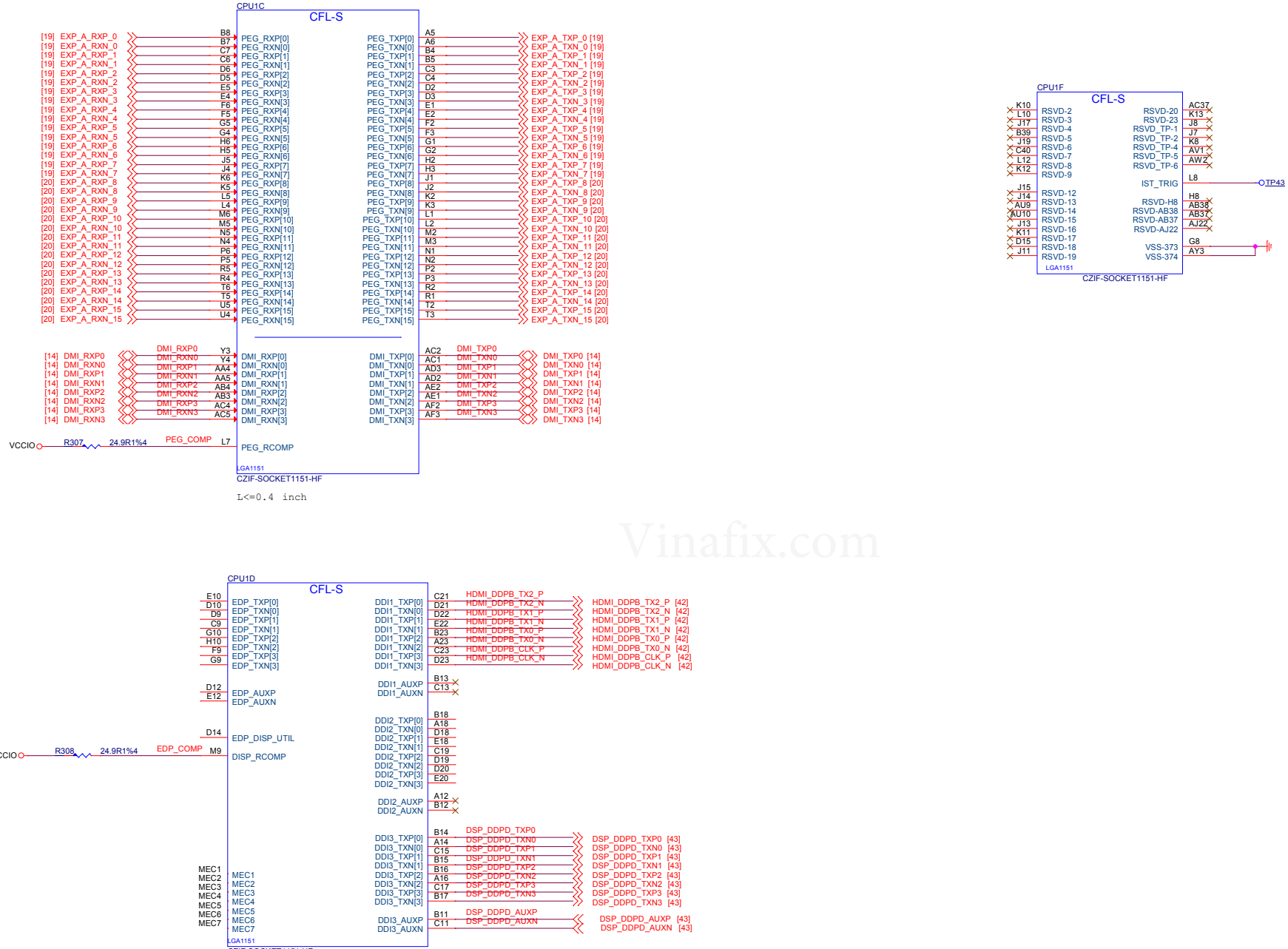

MICRO-STAR INT'L CO.,LTD		
MS-7B17		
Size: Custom	Document Description: CPU-PEG/Display/RSD	Rev: 11
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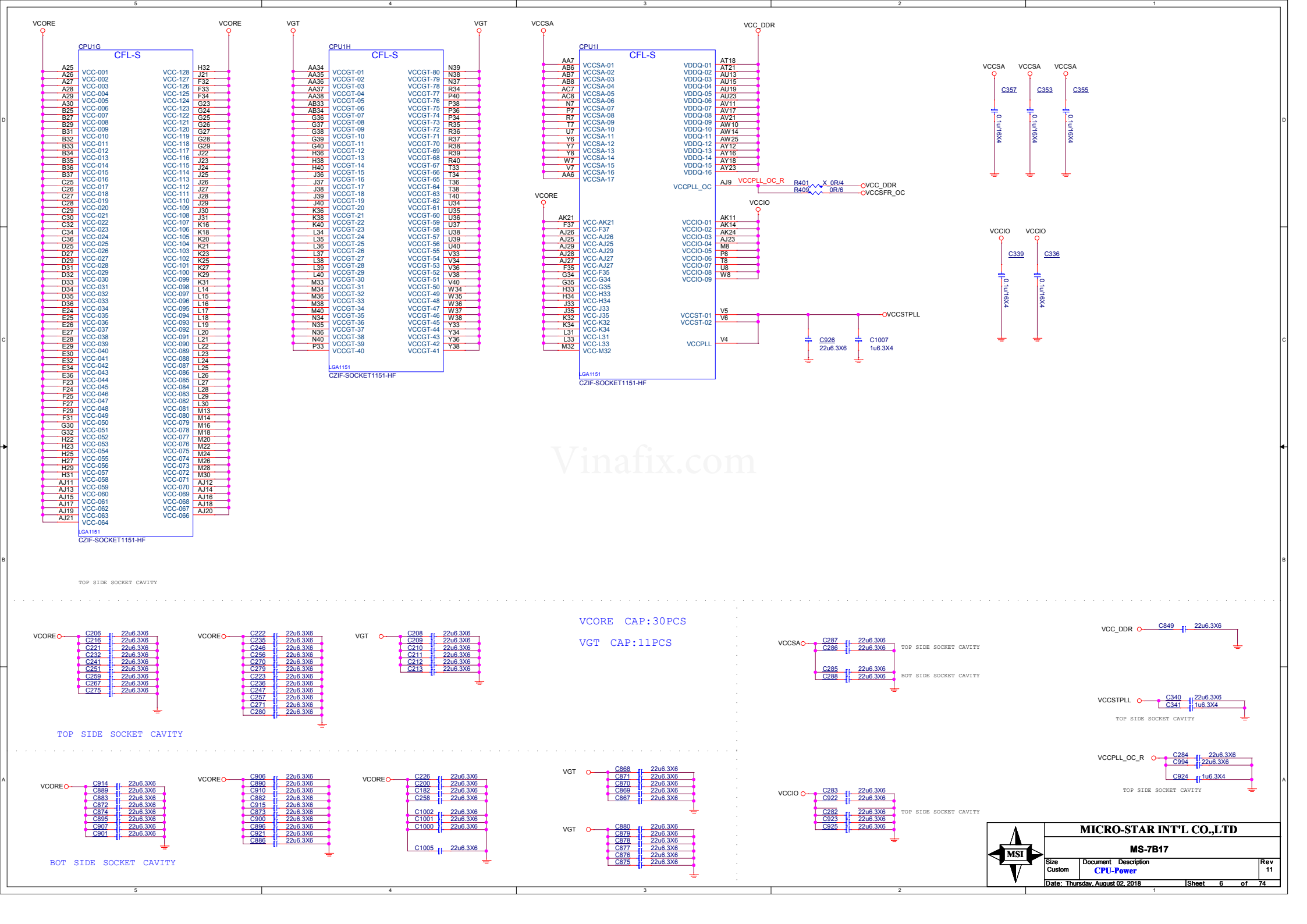
CPU1G
CFL-S
CZIF-SOCKET1151-HF
CPU1H
CFL-S
CZIF-SOCKET1151-HF
CPU1I
CFL-S
CZIF-SOCKET1151-HF
VCORE
VGT
VCCSA
VCC_DDR
VCCIO
VCCPLL_OC_R
R401 X 0R/4
R409 0R/6
VCC_DDR
VCCSFR_OC
C357
C353
C355
C339
C336
C926 22u6.3X6
C1007 1u6.3X4
VCCSTPLL
TOP SIDE SOCKET CAVITY
VCORE CAP:30PCS
VGT CAP:11PCS
BOT SIDE SOCKET CAVITY
C849 22u6.3X6
C340 C341 1u6.3X4
C284 C994 C924
MICRO-STAR INT'L CO.,LTD
MS-7B17
Size Custom
Document Description CPU-Power
Rev 11
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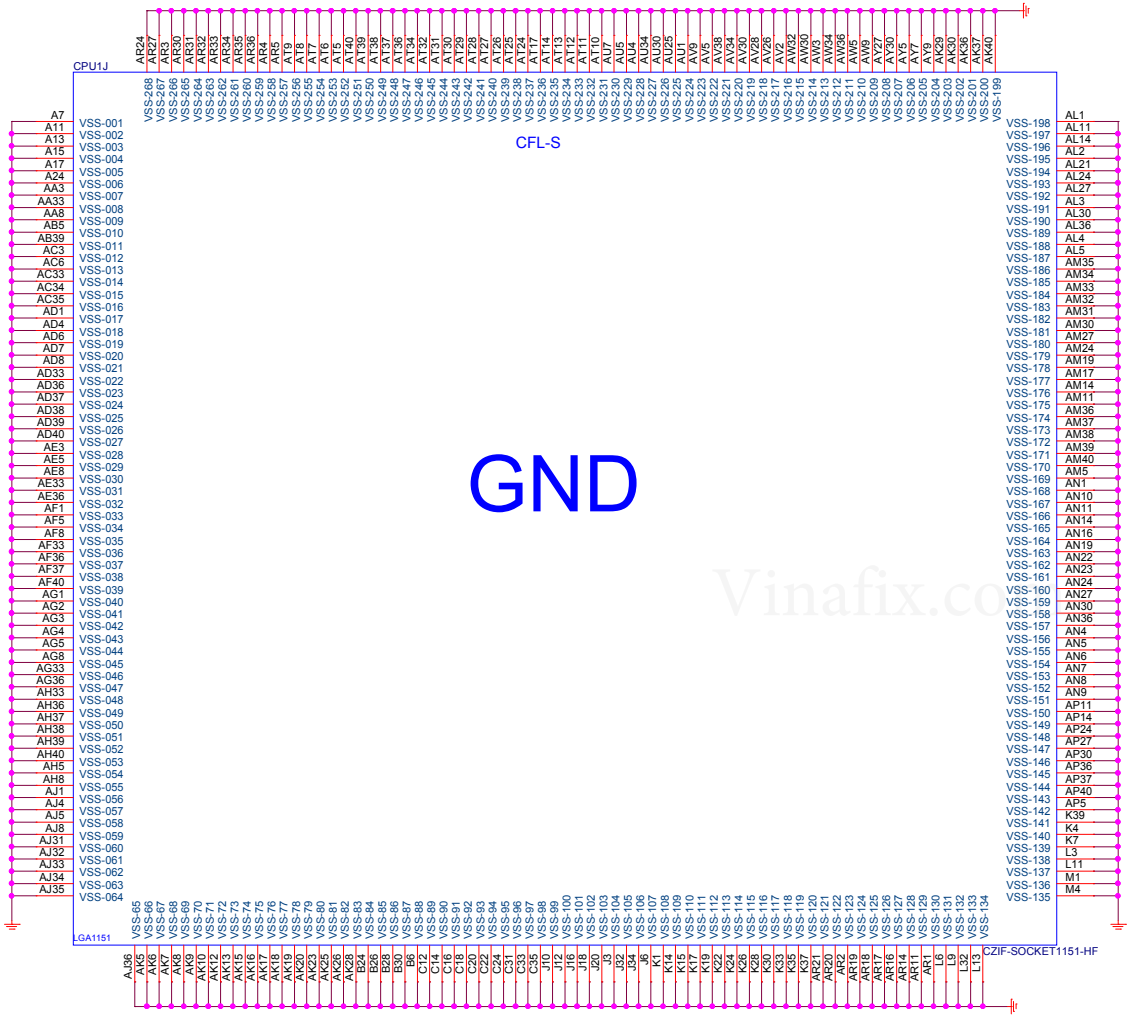

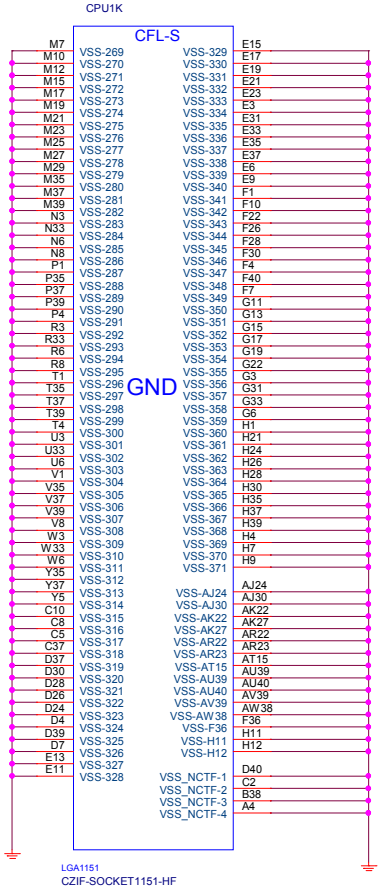

MICRO-STAR INT'L CO.,LTD	
MS-7B17	
Size: Custom	Document Description: CPU-GND
Rev: 11	
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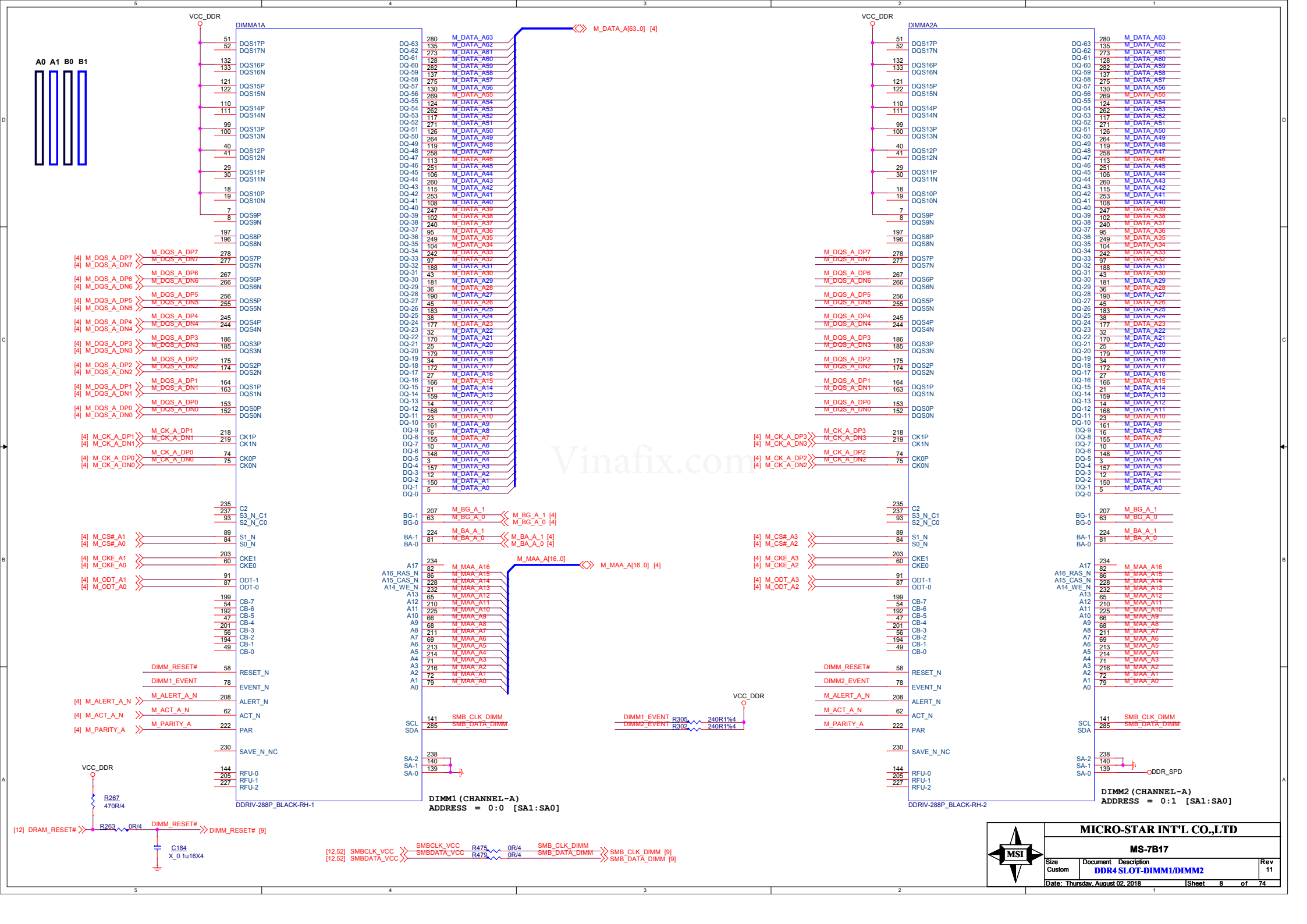
A0 A1 B0 B1
VCC_DDR
DIMMA1A
DDRIV-288P_BLACK-RH-1
M_DATA_A[63..0] [4]
M_MAA_A[16..0]
M_MAA_A[16..0] [4]
DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
VCC_DDR
DIMMA2A
DDRIV-288P_BLACK-RH-2
DDR_SPD
DIMM2 (CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]
R267 470R/4
R263 0R/4
DIMM_RESET#
[12] DRAM_RESET#
DIMM_RESET# [9]
C184 X_0.1u16X4
[12,52] SMBCLK_VCC
[12,52] SMBDATA_VCC
SMBCLK_VCC
SMBDATA_VCC
R475 0R/4
R479 0R/4
SMB_CLK_DIMM
SMB_DATA_DIMM
SMB_CLK_DIMM [9]
SMB_DATA_DIMM [9]
DIMM1_EVENT
DIMM2_EVENT
R305 240R1%4
R302 240R1%4
MICRO-STAR INT'L CO.,LTD
MS-7B17
Size Custom
Document Description
DDR4 SLOT-DIMM1/DIMM2
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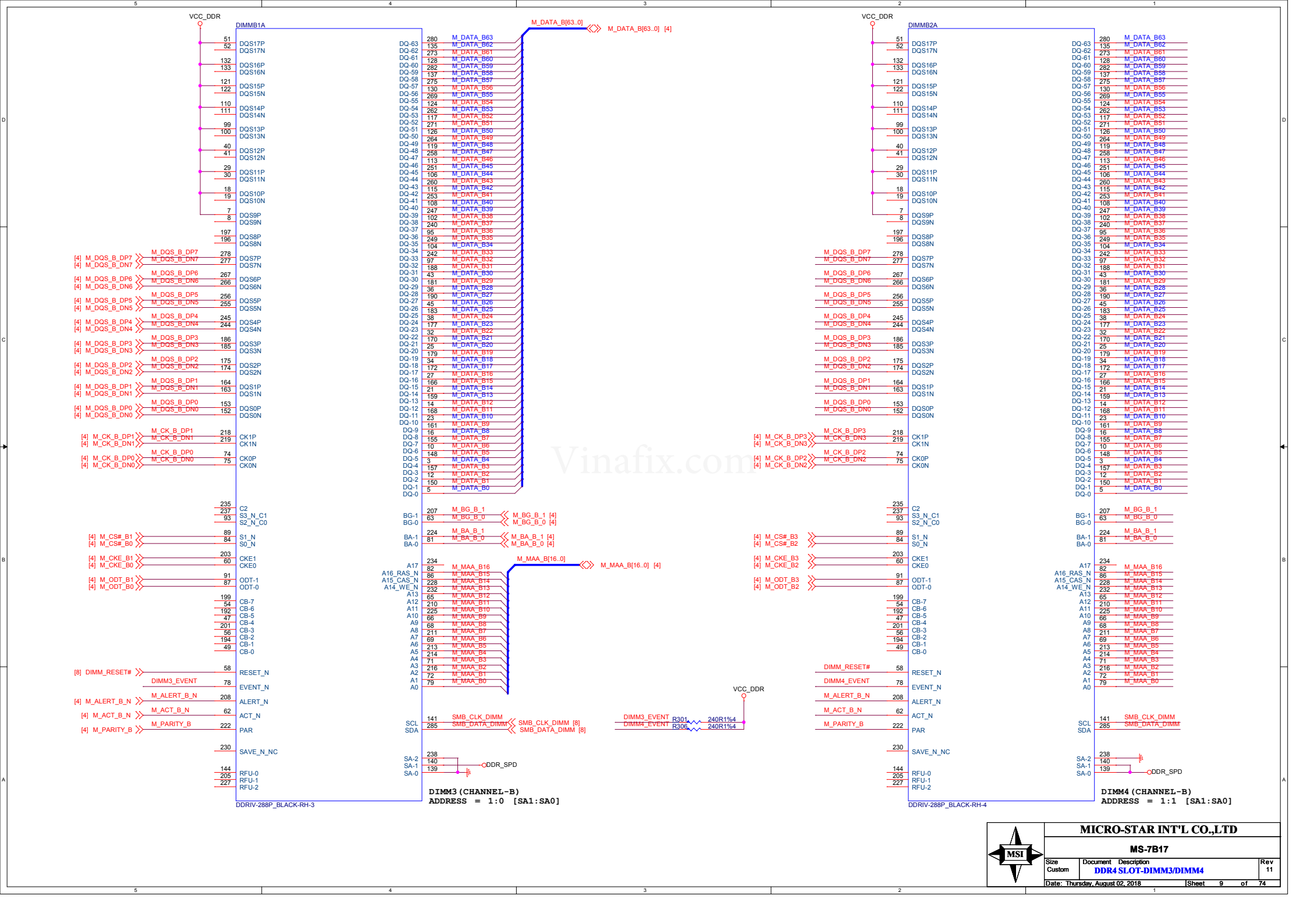
VCC_DDR
DIMMB1A
M_DATA_B[63..0]
M_DATA_B[63..0] [4]
DQS17P
DQS17N
DQS16P
DQS16N
DQS15P
DQS15N
DQS14P
DQS14N
DQS13P
DQS13N
DQS12P
DQS12N
DQS11P
DQS11N
DQS10P
DQS10N
DQS9P
DQS9N
DQS8P
DQS8N
DQS7P
DQS7N
DQS6P
DQS6N
DQS5P
DQS5N
DQS4P
DQS4N
DQS3P
DQS3N
DQS2P
DQS2N
DQS1P
DQS1N
DQS0P
DQS0N
CK1P
CK1N
CK0P
CK0N
C2
S3_N_C1
S2_N_C0
S1_N
S0_N
CKE1
CKE0
ODT-1
ODT-0
CB-7
CB-6
CB-5
CB-4
CB-3
CB-2
CB-1
CB-0
RESET_N
EVENT_N
ALERT_N
ACT_N
PAR
SAVE_N_NC
RFU-0
RFU-1
RFU-2
BG-1
BG-0
BA-1
BA-0
M_BG_B_1
M_BG_B_0
M_BA_B_1
M_BA_B_0
M_MAA_B[16..0]
M_MAA_B[16..0] [4]
A17
A16_RAS_N
A15_CAS_N
A14_WE_N
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
SCL
SDA
SMB_CLK_DIMM
SMB_DATA_DIMM
SMB_CLK_DIMM [8]
SMB_DATA_DIMM [8]
SA-2
SA-1
SA-0
DDR_SPD
DDRIV-288P_BLACK-RH-3
DIMM3 (CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]
DIMM3_EVENT
DIMM4_EVENT
R301
R306
240R1%4
DIMMB2A
DDRIV-288P_BLACK-RH-4
DIMM4 (CHANNEL-B)
ADDRESS = 1:1 [SA1:SA0]
MICRO-STAR INT'L CO.,LTD
MS-7B17
Size
Custom
Document Description
DDR4 SLOT-DIMM3/DIMM4
Rev
11
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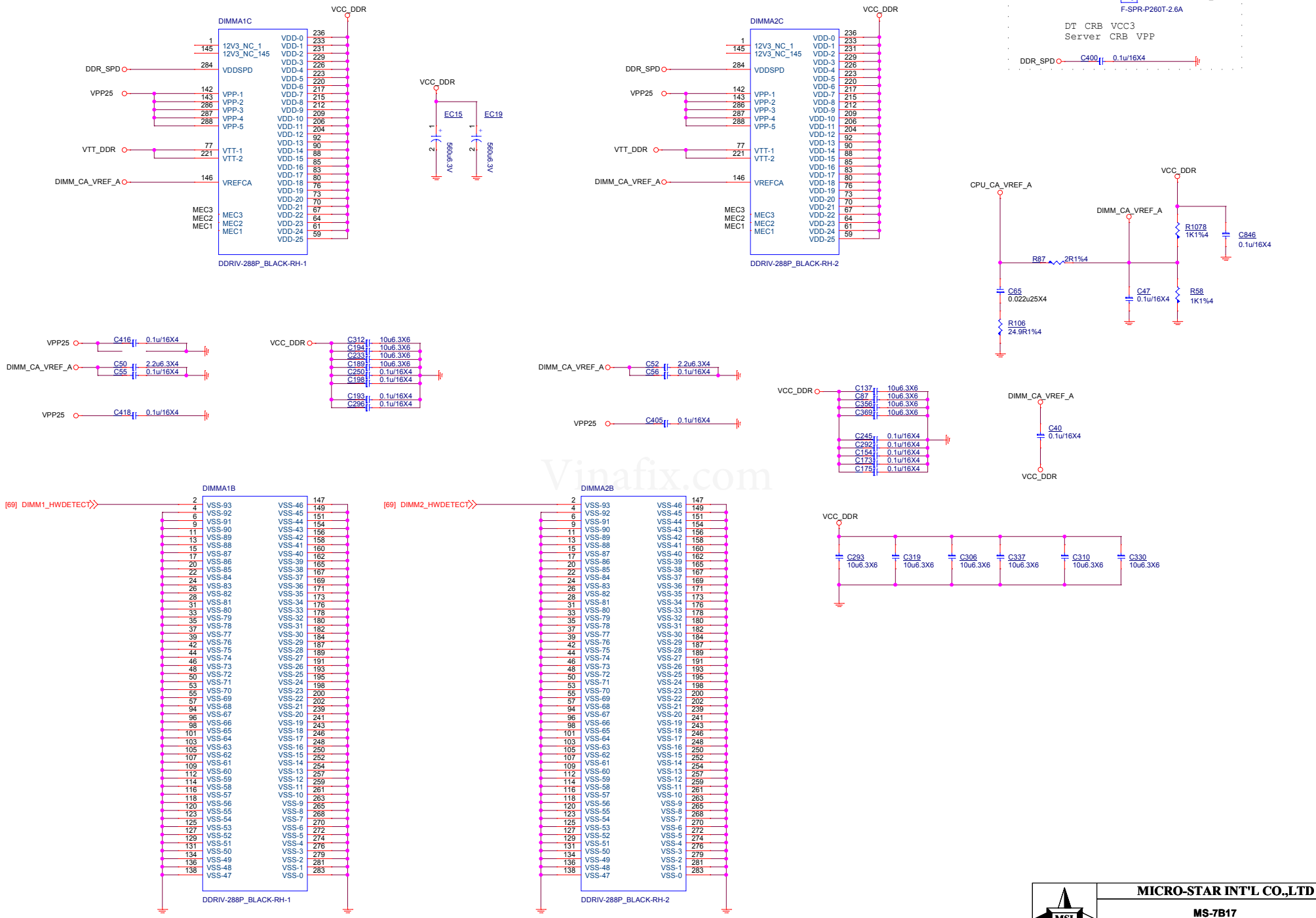

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Size	Document Description	Rev
Custom	DDR4-POWER/GND-1	11

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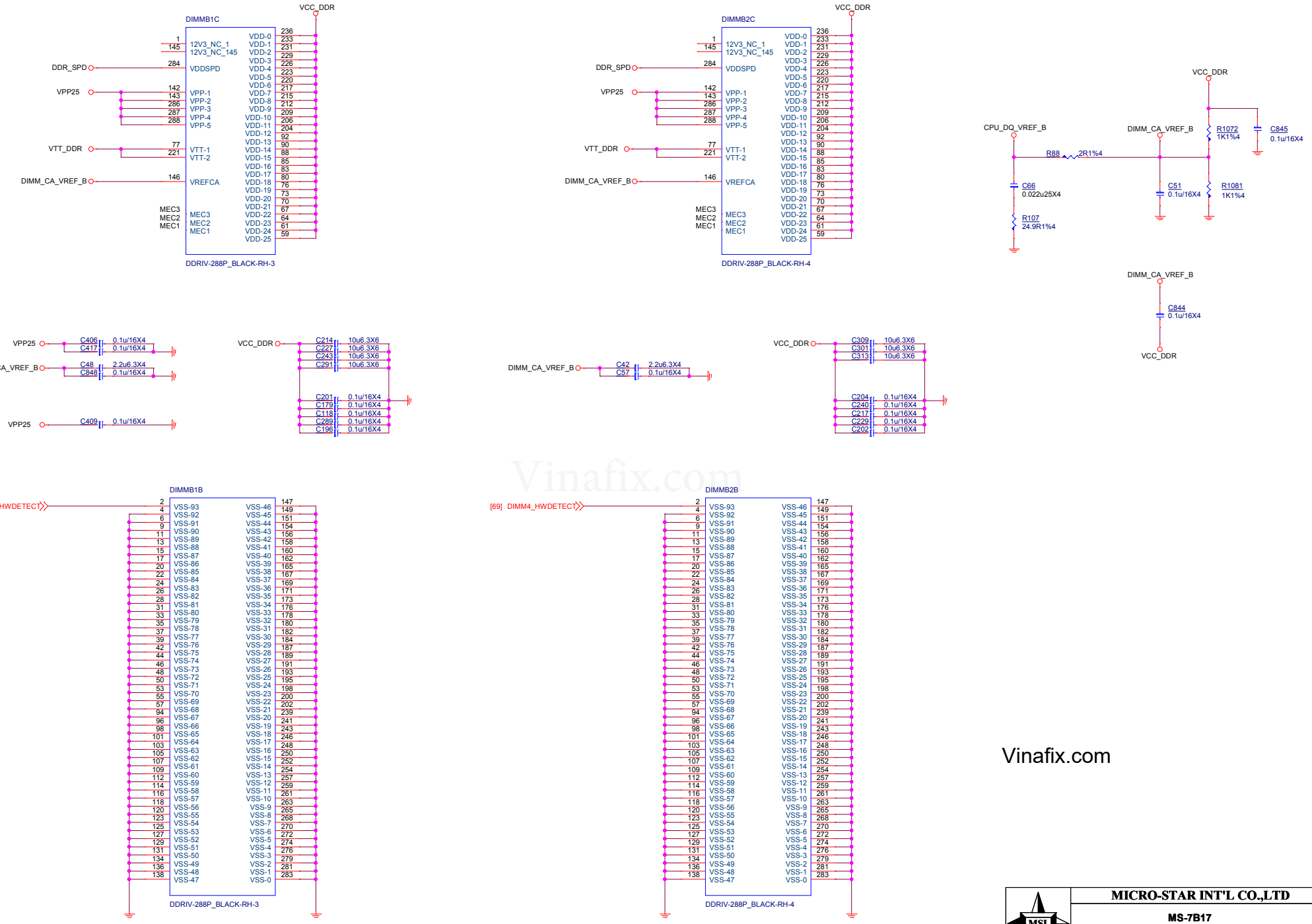
DIMMB1C
DDRIV-288P_BLACK-RH-3
DIMMB2C
DDRIV-288P_BLACK-RH-4
VCC_DDR
DDR_SPD
VPP25
VTT_DDR
DIMM_CA_VREF_B
CPU_DQ_VREF_B
R88 2R1%4
C66 0.022u25X4
R107 24.9R1%4
R1072 1K1%4
C845 0.1u/16X4
C51 0.1u/16X4
R1081 1K1%4
C844 0.1u/16X4
C406 0.1u/16X4
C417 0.1u/16X4
C48 2.2u6.3X4
C848 0.1u/16X4
C409 0.1u/16X4
C214 10u6.3X6
C227 10u6.3X6
C243 10u6.3X6
C291 10u6.3X6
C201 0.1u/16X4
C175 0.1u/16X4
C118 0.1u/16X4
C289 0.1u/16X4
C196 0.1u/16X4
C42 2.2u6.3X4
C57 0.1u/16X4
C309 10u6.3X6
C301 10u6.3X6
C313 10u6.3X6
C204 0.1u/16X4
C240 0.1u/16X4
C217 0.1u/16X4
C229 0.1u/16X4
C202 0.1u/16X4
DIMMB1B
DIMMB2B
[69] DIMM3_HWDETECT
[69] DIMM4_HWDETECT
Vinafix.com
MICRO-STAR INT'L CO.,LTD
MS-7B17
Size Custom
Document Description DDR4-POWER/GND-2
Rev 11
Date: Thursday, August 02, 2018
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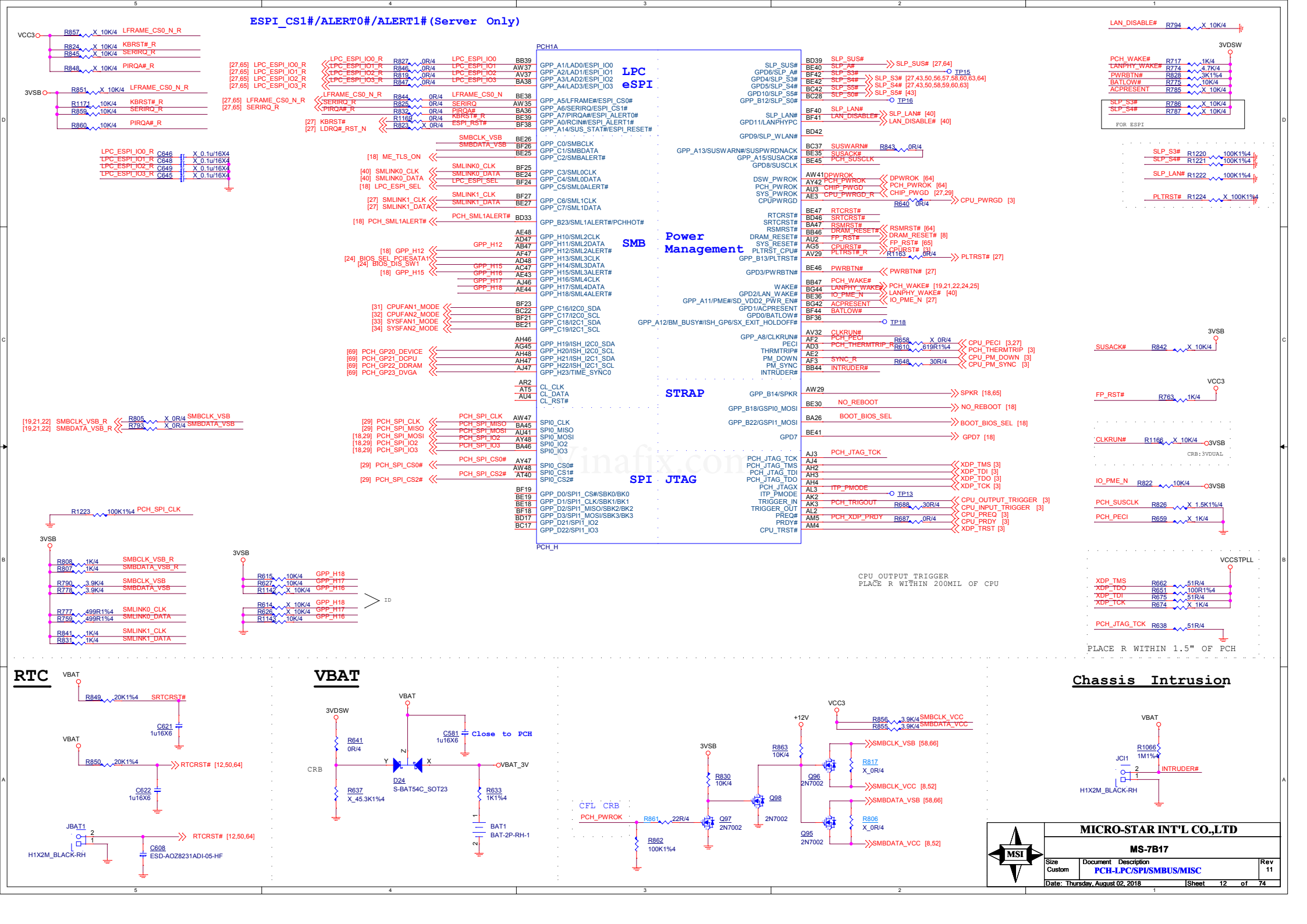
ESPI_CS1#/ALERT0#/ALERT1#(Server Only)
PCH1A
LPC eSPI
SMB
Power Management
STRAP
SPI
JTAG
PCH_H
CPU_OUTPUT_TRIGGER
PLACE R WITHIN 200MIL OF CPU
PLACE R WITHIN 1.5" OF PCH
RTC
VBAT
Close to PCH
CRB
CFL CRB
Chassis Intrusion
MICRO-STAR INT'L CO.,LTD
MS-7B17
PCH-LPC/SPI/SMBUS/MISC
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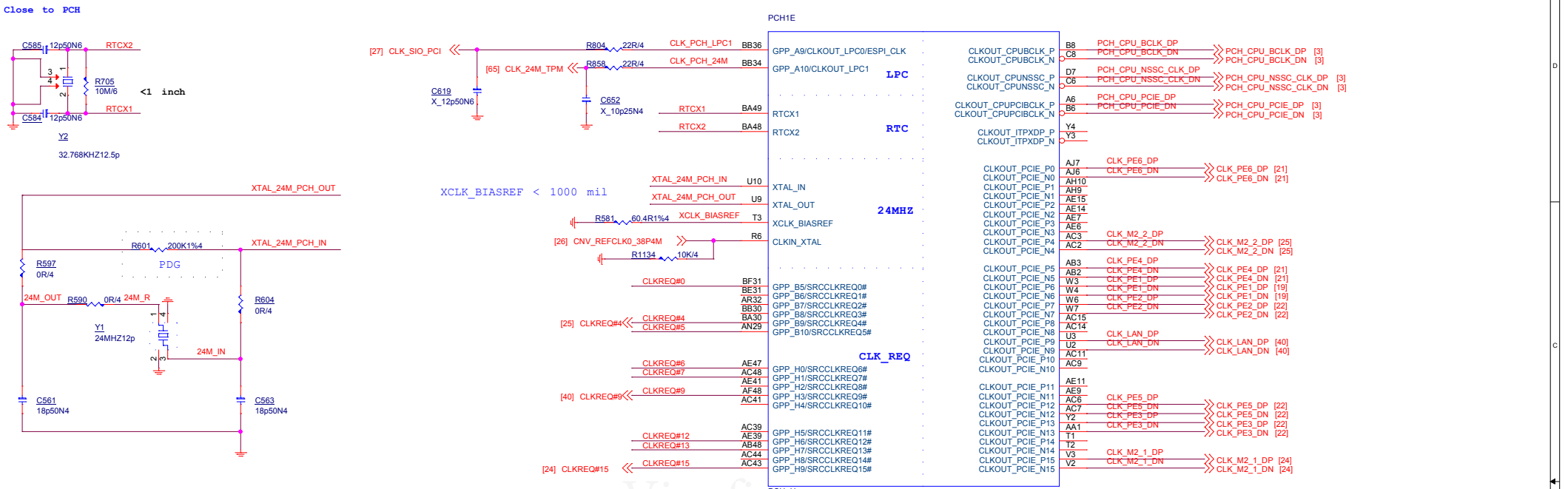
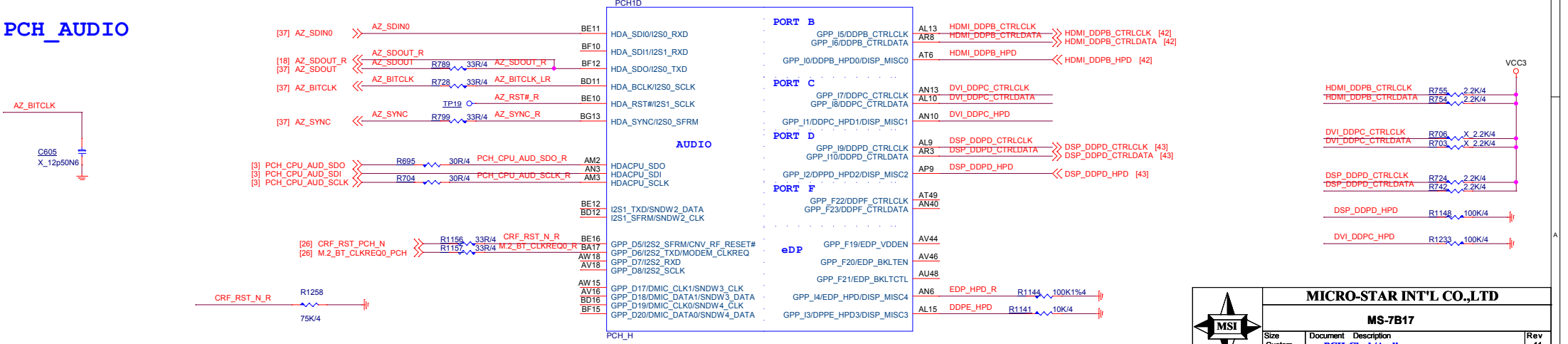
PCH_CLK



PCH_AUDIO



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	PCH-Clock/Audio	11

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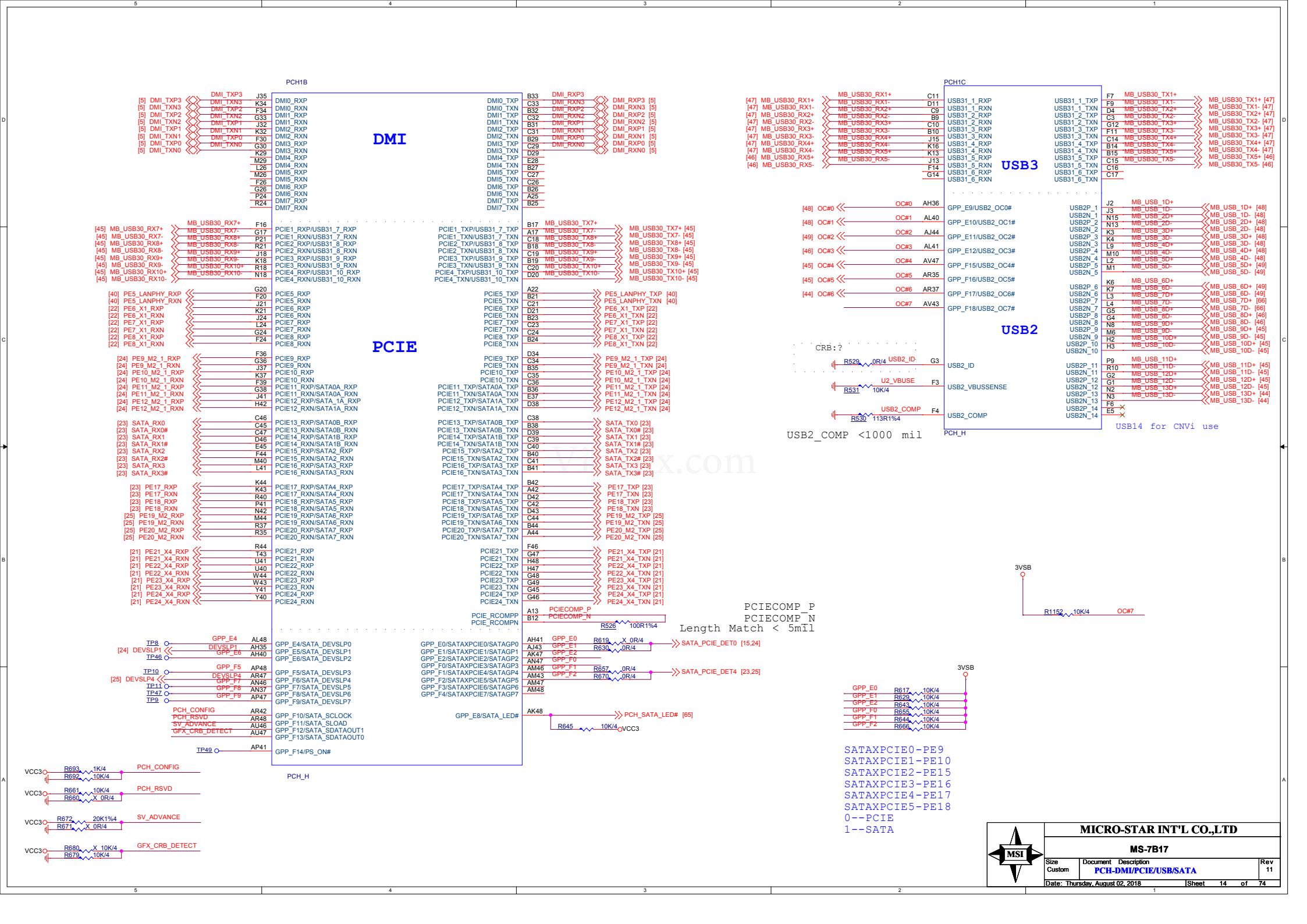
PCH1B
DMI
PCIE
PCH_H
PCH1C
USB3
USB2
PCH_H
CRB:?
USB2_COMP <1000 mil
USB14 for CNVi use
PCIECOMP_P
PCIECOMP_N
Length Match < 5mil
SATAXPCIE0-PE9
SATAXPCIE1-PE10
SATAXPCIE2-PE15
SATAXPCIE3-PE16
SATAXPCIE4-PE17
SATAXPCIE5-PE18
0--PCIE
1--SATA
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MS-7B17
Size Custom
Document Description PCH-DMI/PCIE/USB/SATA
Rev 11
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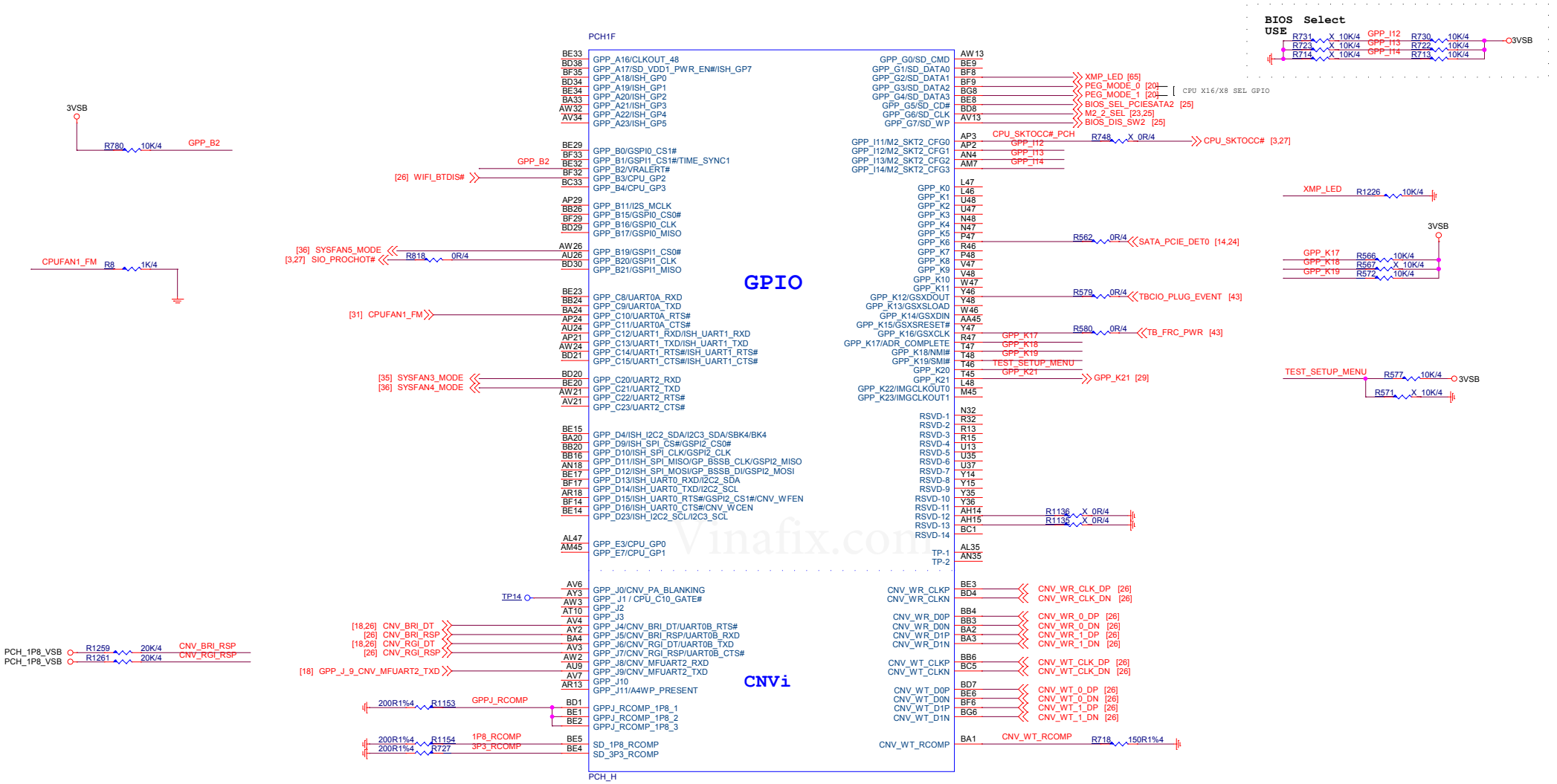

MICRO-STAR INT'L CO.,LTD		
MS-7B17		
Size: Custom	Document Description: PCH-GPIO/RSVD	Rev: 11
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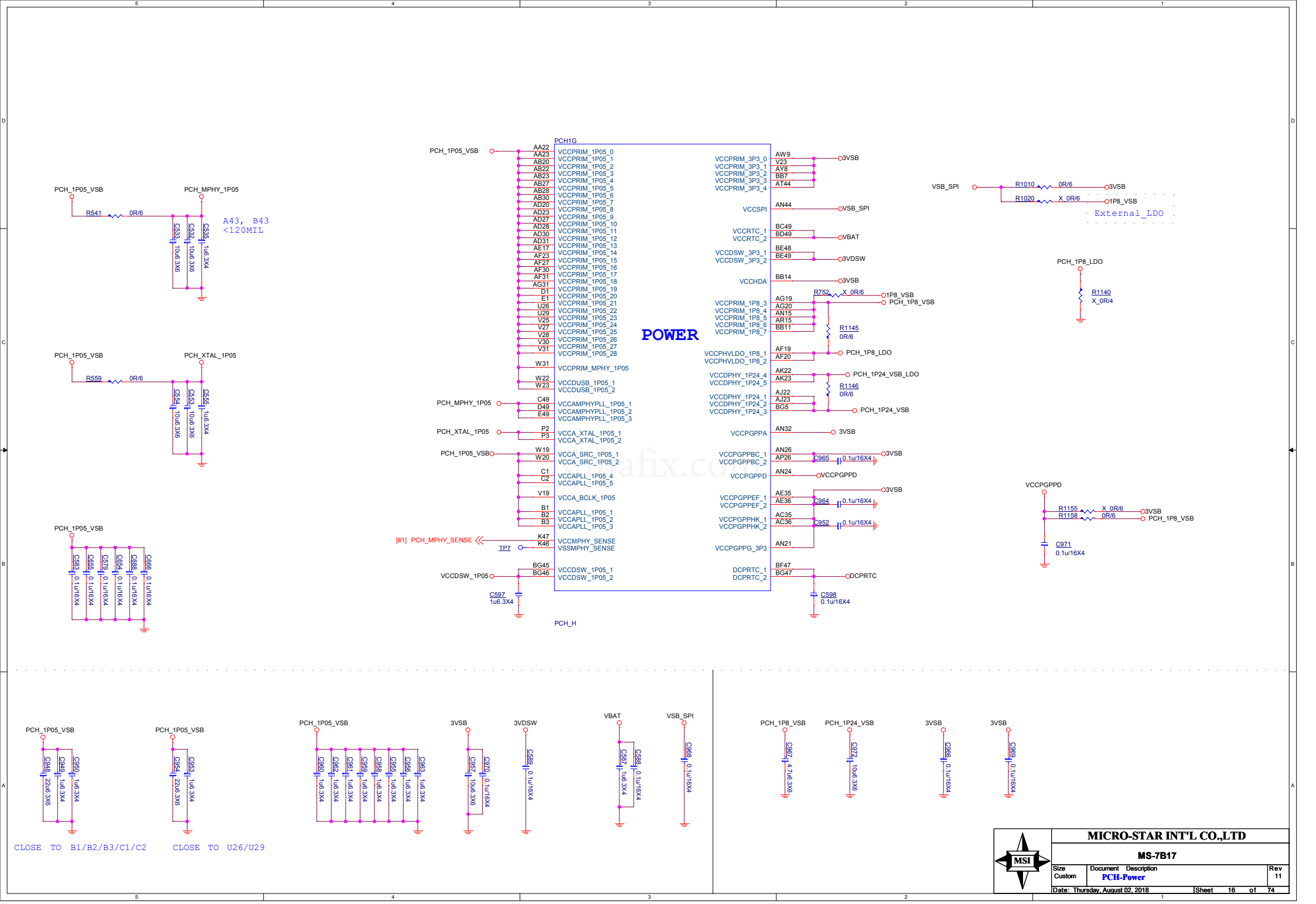
PCH1G
POWER
PCH_1P05_VSB
PCH_MPHY_1P05
PCH_XTAL_1P05
PCH_H
A43, B43
<120MIL
External_LDO
CLOSE TO B1/B2/B3/C1/C2
CLOSE TO U26/U29
MICRO-STAR INT'L CO.,LTD
MS-7B17
PCH-Power
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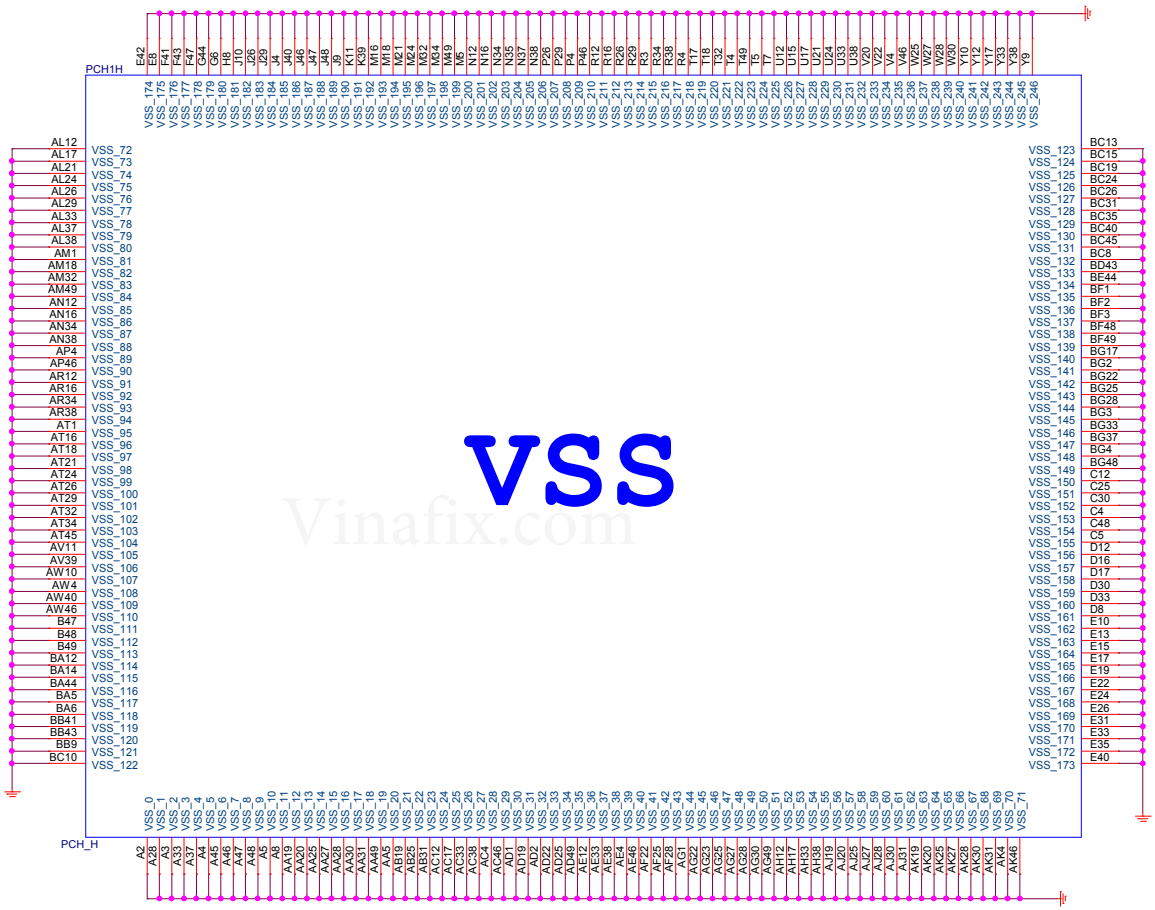

MICRO-STAR INT'L CO.,LTD		
MS-7B17		
Size: Custom	Document Description: PCH-GND	Rev: 11
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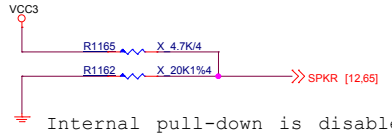
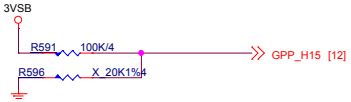
TOP Swap

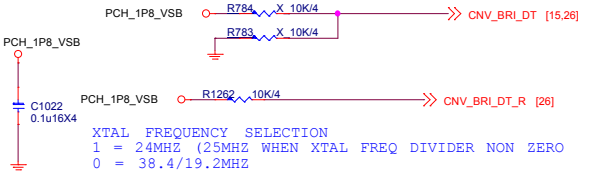


Internal pull-down is disabled after PLTRST#

Reserved

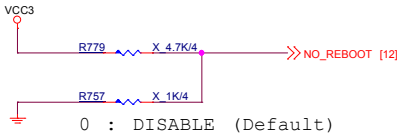


ESPI FLASH SHARING MODE



XTAL FREQUENCY SELECTION
1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO
0 = 38.4/19.2MHZ

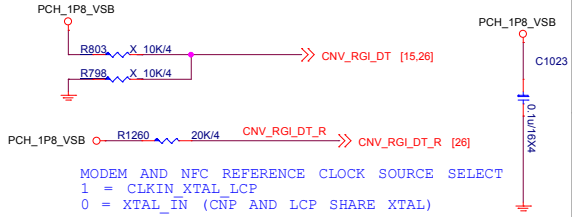
No Reboot



0 : DISABLE (Default)
1 : ENABLE

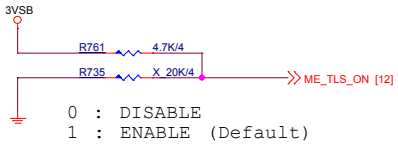
Reserved

Modem Reference Clock Source Select



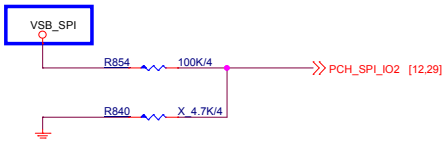
MODEM AND NFC REFERENCE CLOCK SOURCE SELECT
1 = CLKIN_XTAL_LCP
0 = XTAL_IN (CNP AND LCP SHARE XTAL)

AMT and SBA with confidentiality

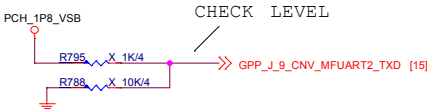


0 : DISABLE
1 : ENABLE (Default)

Reserved



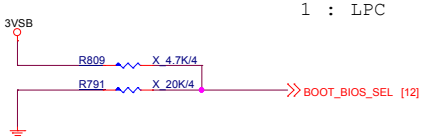
1.8V VCCPSPI



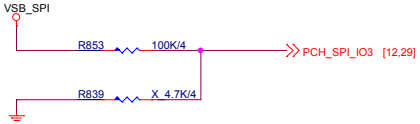
SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE
0 = VCCPSPI IS CONNECTED TO 3.3V RAIL - DEFAULT
1 = VCCPSPI IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD

Boot BIOS

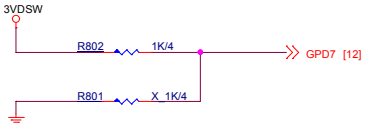
0 : SPI
1 : LPC



Reserved

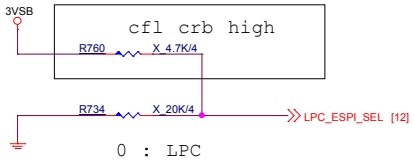


Reserved



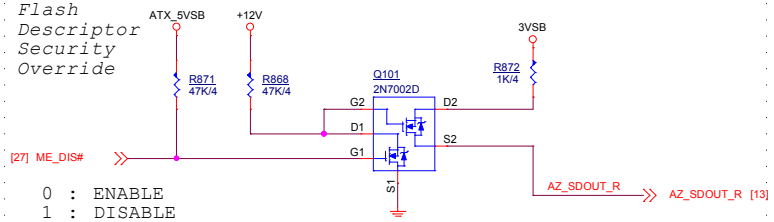
XTAL INPUT MODE
0 = XTAL INPUT IS SINGLE-ENDED
1 = XTAL INPUT IS DIFFERENTIAL
PCH HAS INTERNAL 20K PD

LPC eSPI Mode



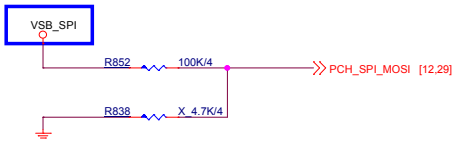
0 : LPC
1 : eSPI

Flash Descriptor Security Override

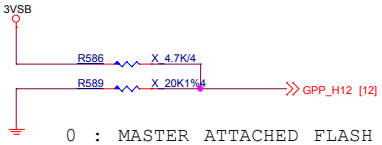


0 : ENABLE
1 : DISABLE

Reserved



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

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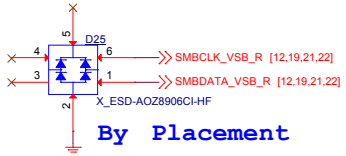
Date: Thursday, August 02, 2018	Sheet 18 of 74	

12V - 5.5A

VCC3 - 3A

3VSB- 375mA

SMBUS ESD



By Placement

Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14

PCI_E1

SLOT-PCI164P_BLACK-2PITCH-RH-51

0901 Modify PCI_E1 PIN X2.X3.X4.X5 Connect to GND

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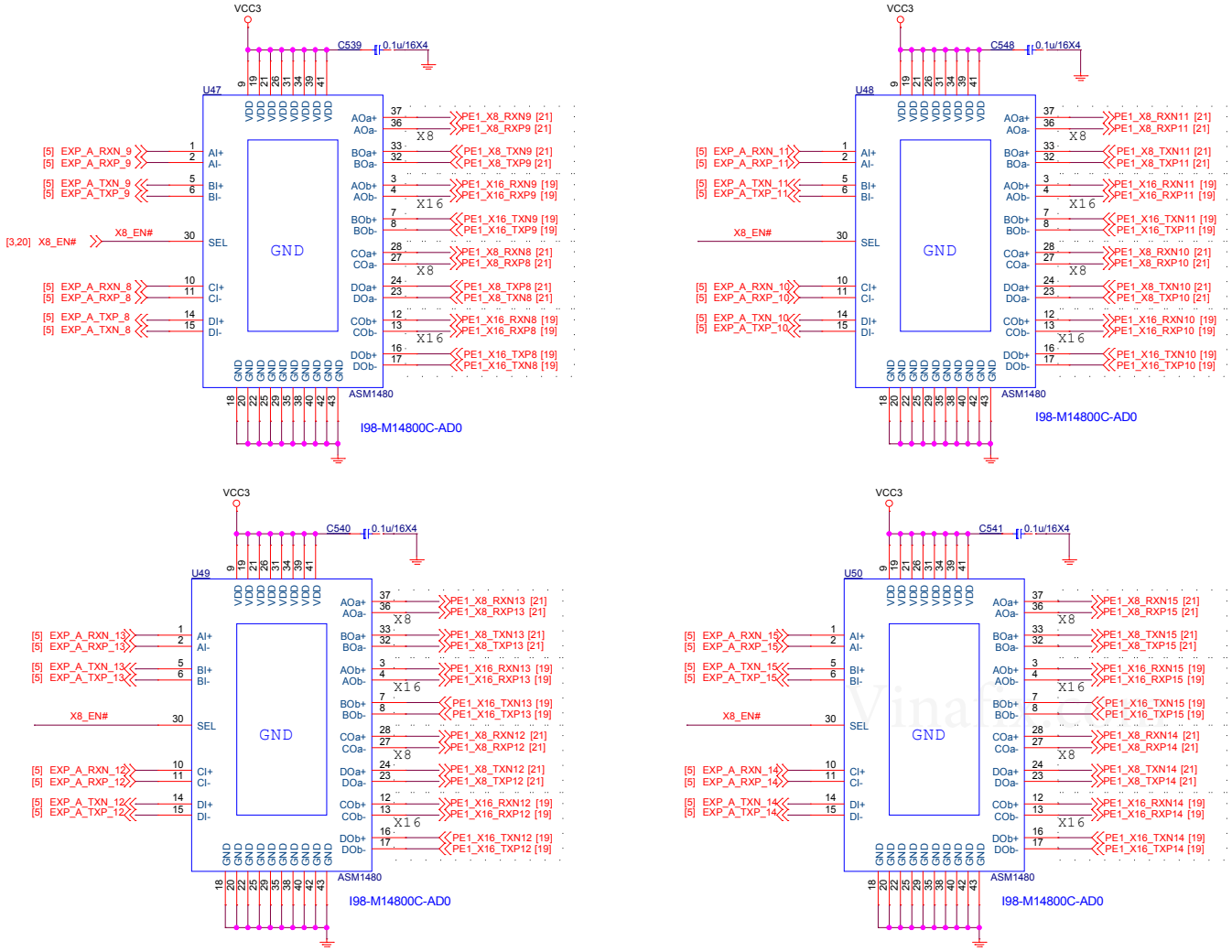
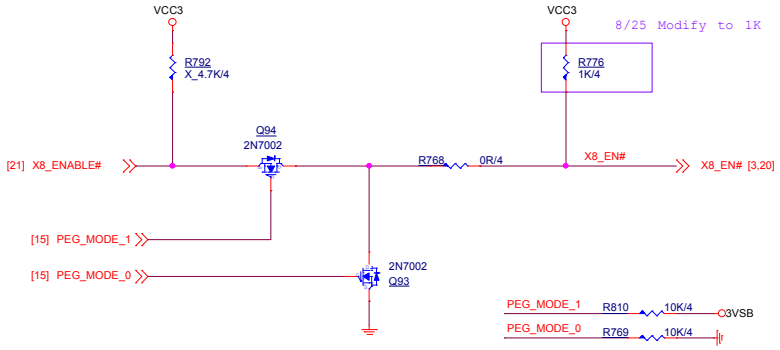
MS-7B17	
Size: Custom	Document Description: PCIE SLOT (X16)
Rev: 11	
Date: Thursday, August 02, 2018	Sheet 19 of 74



Vinafix.com



MODE_1

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0	MODE_1
AUTO	0	1

If USE HW MODE
GPP_G0 & GPP_G1 programming to GPI

If USE BIOS MODE
GPP_G0 & GPP_G1 programming to GPO

BIOS MODE

PCH Status	MODE_0	MODE_1
16,0	0	0
8,8	1	0

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Size: Custom | Document Description: PCIE SWITCH | Rev: 11

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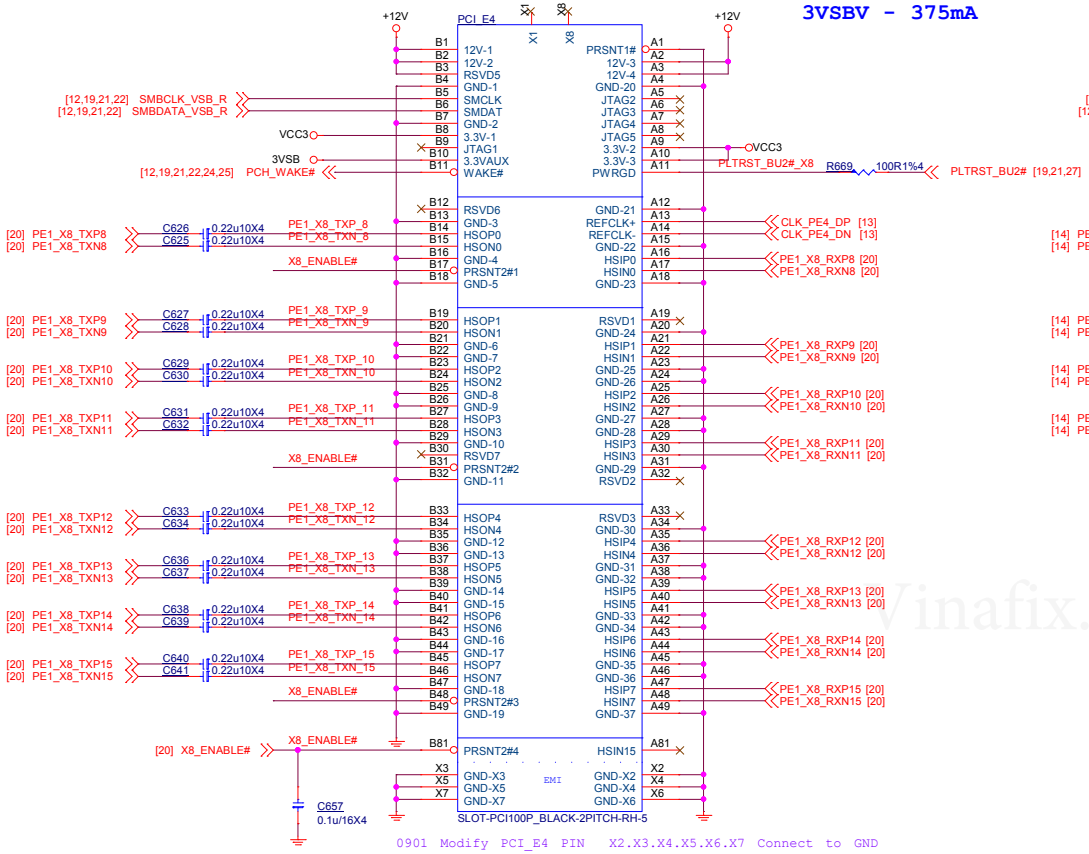
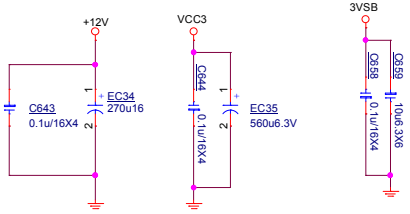
PCI Express X8 Slot

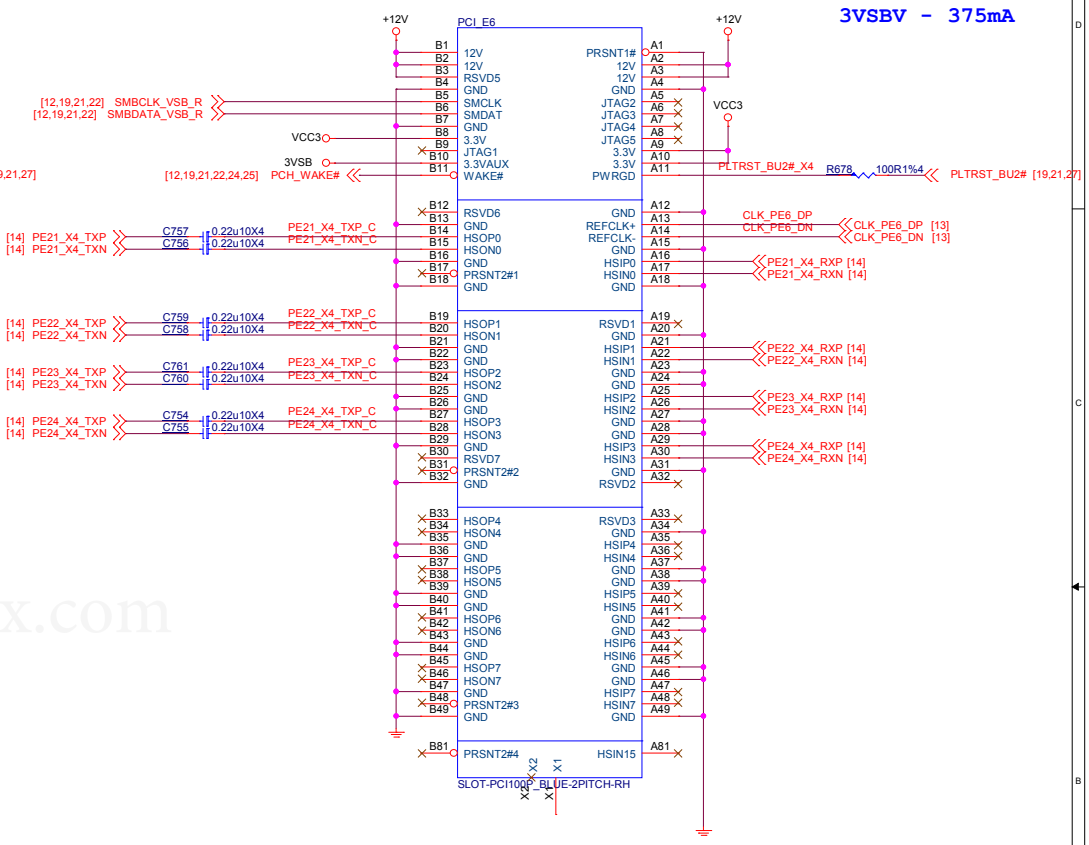
12V - 2.1A
VCC3 - 3A
3VSBV - 375mA

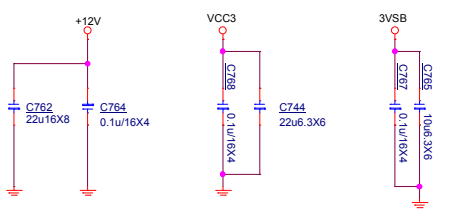




PCI Express X4 Slot

12V - 2.1A
VCC3 - 3A
3VSBV - 375mA





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Size	Document Description	Rev
Custom	PCIE SLOT (X4)	11

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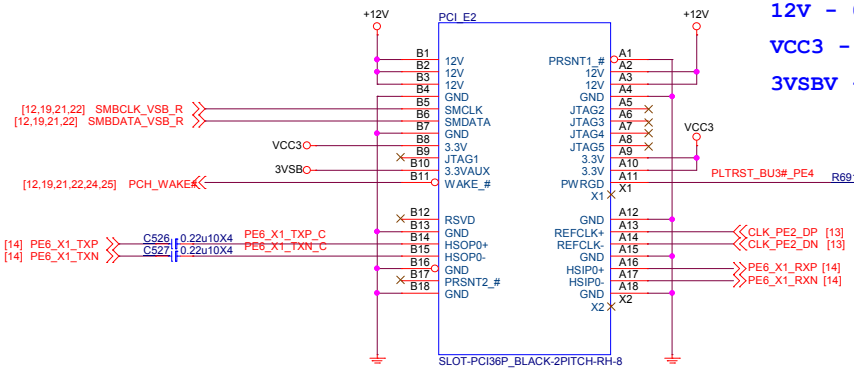
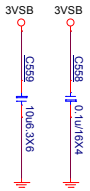
2016.08.25 Modify to N11-0360211-F02

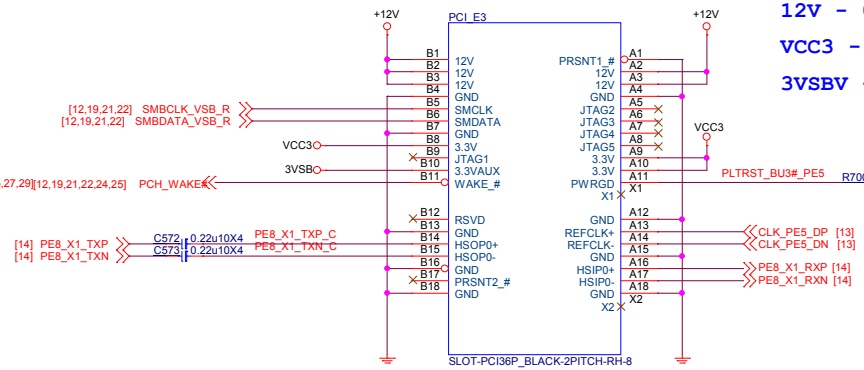
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA

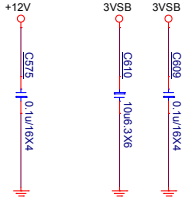




2016.08.25 Modify to N11-0360211-F02

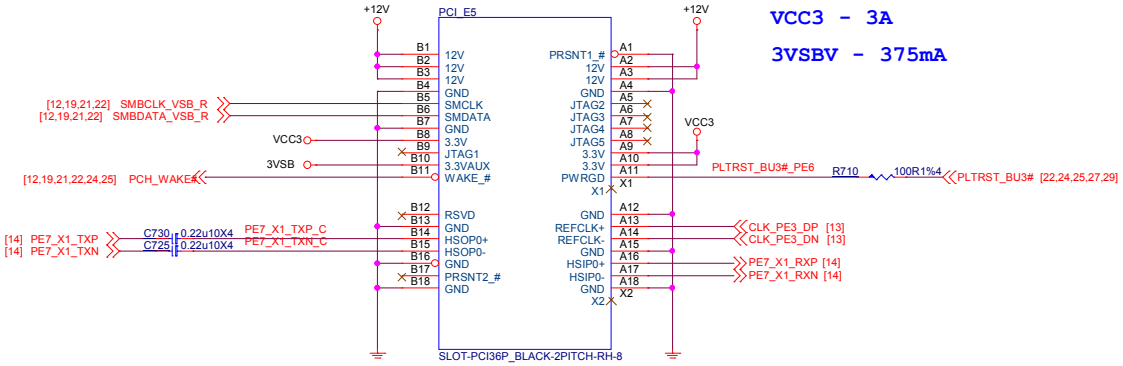
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA

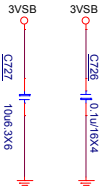




2016.08.25 Modify to N11-0360211-F02

12V - 0.5A
VCC3 - 3A
3VSBV - 375mA





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Custom	PCIE SLOT (X1)	11

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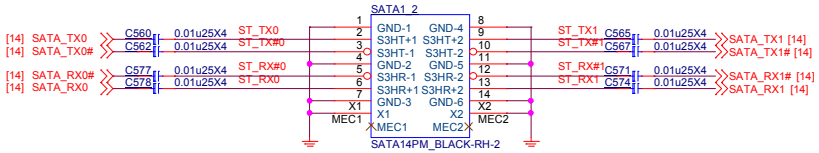
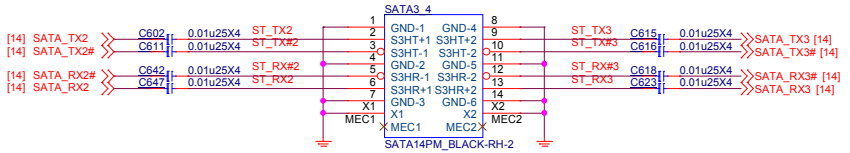
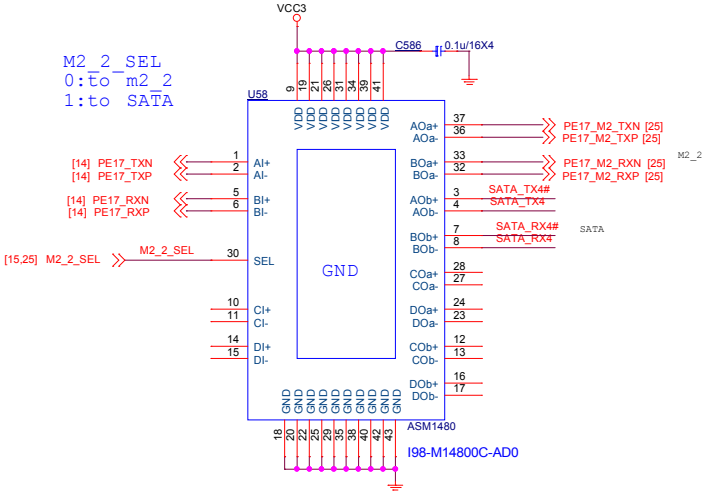
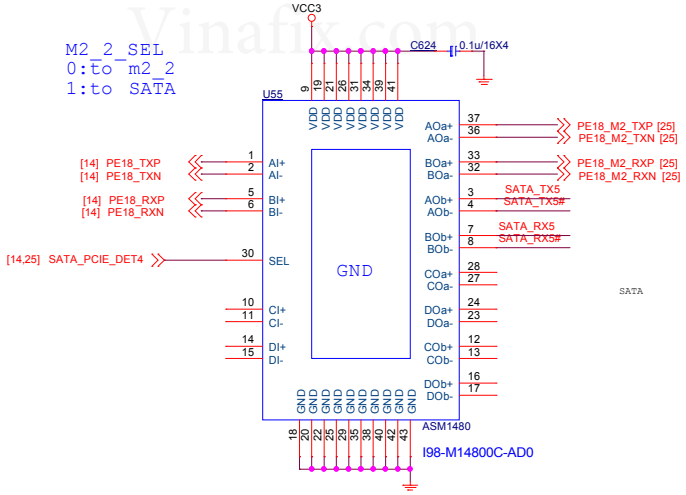
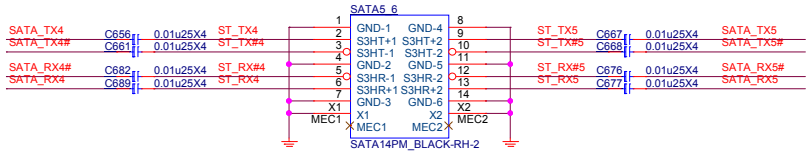
SATA Connector











MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	SATA Connector	11

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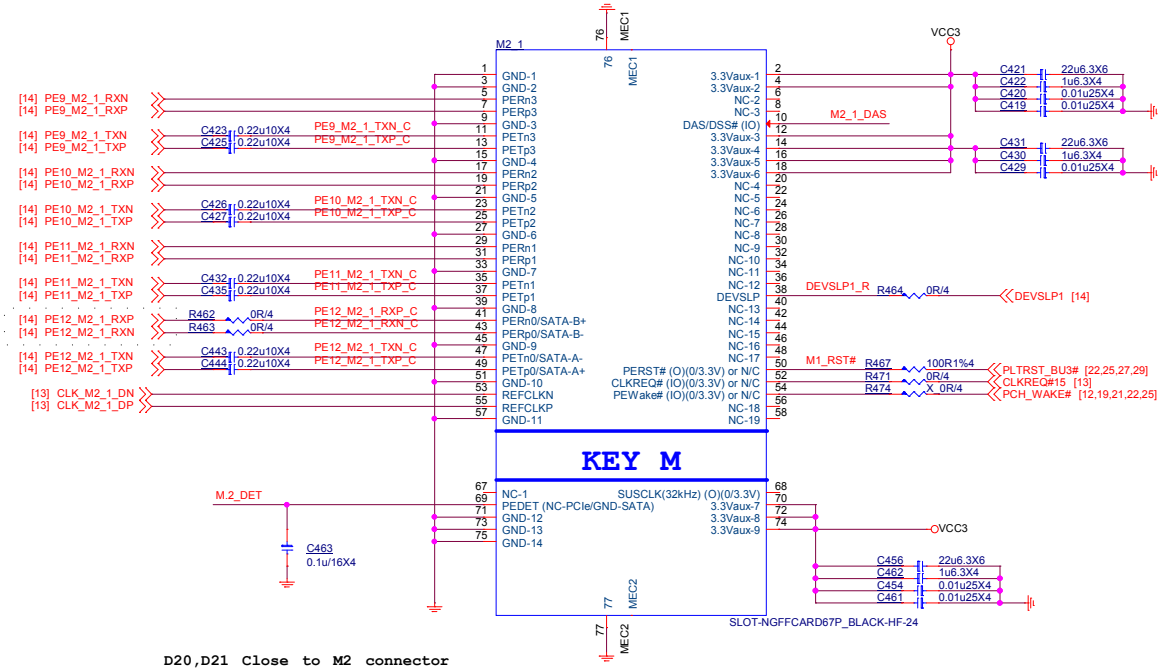
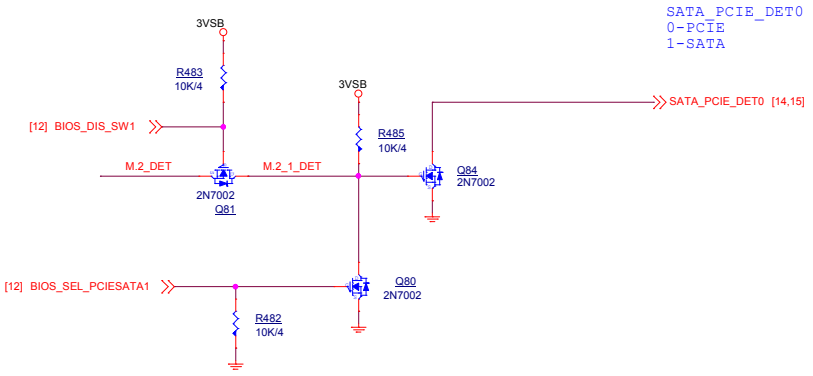
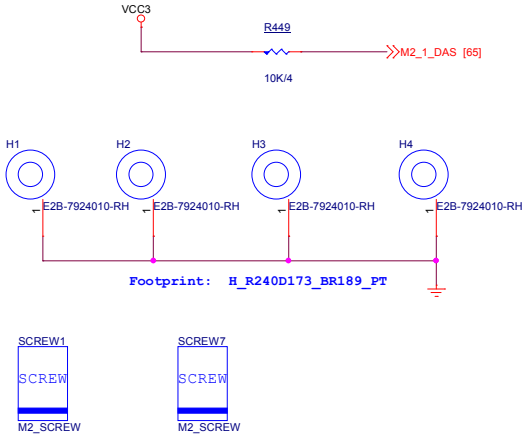


D20,D21 Close to M2 connector





BIOS_MODE

DIS_SW	*M1_SEL_PCIESATA*	*Mode*
0	*1*	*M2-SATA*
0	*0*	*M2-PCIE*
GPI	*GPI*	*AUTO*

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Size: Custom | Document Description: M.2-SLOT1 | Rev: 11

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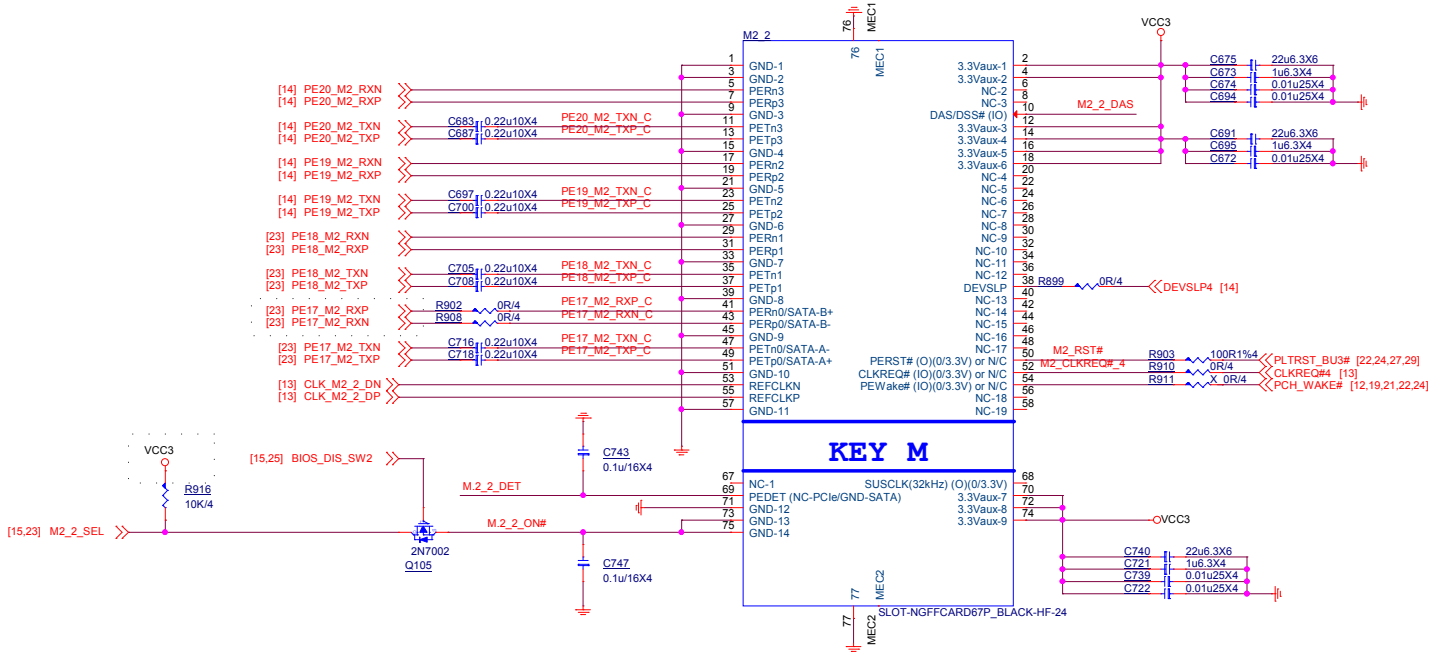

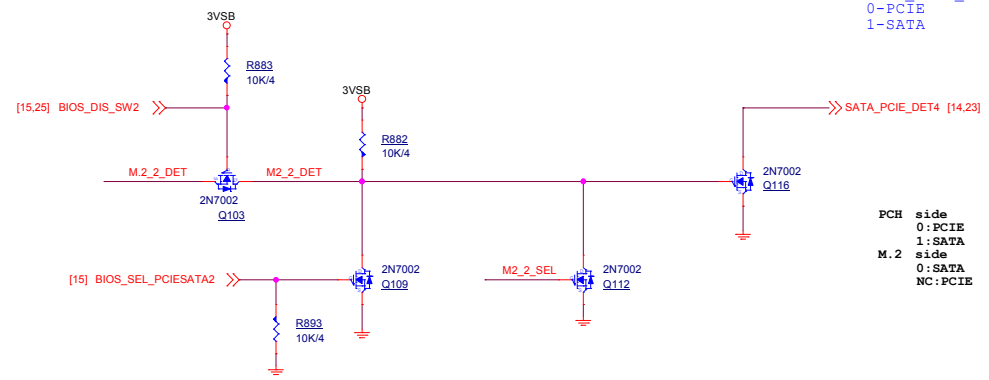

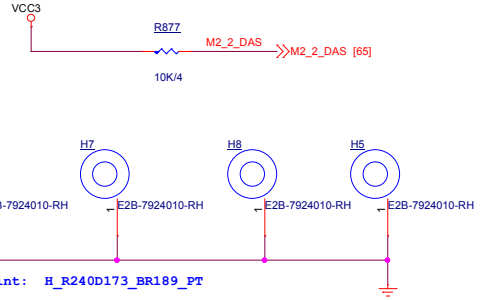

BIOS_MODE

GPP_G7	GPP_G6	GPP_G5	
BIOS_DIS_SW	***M2_2_SEL***	***BIOS_SEL_PCIESATA2***	***Mode***
GPI(1)	***GPI(1)***	***GPI(0)***	***AUTO***
0	***1***	***0***	***SATA5***
0	***0***	***1***	***M2-SATA***
0	***0***	***0***	***M2-PCIE***

SCREW2 SCREW6
SCREW SCREW
M2_SCREW M2_SCREW

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Size: Custom | Document Description: M.2-SLOT2 | Rev: 11

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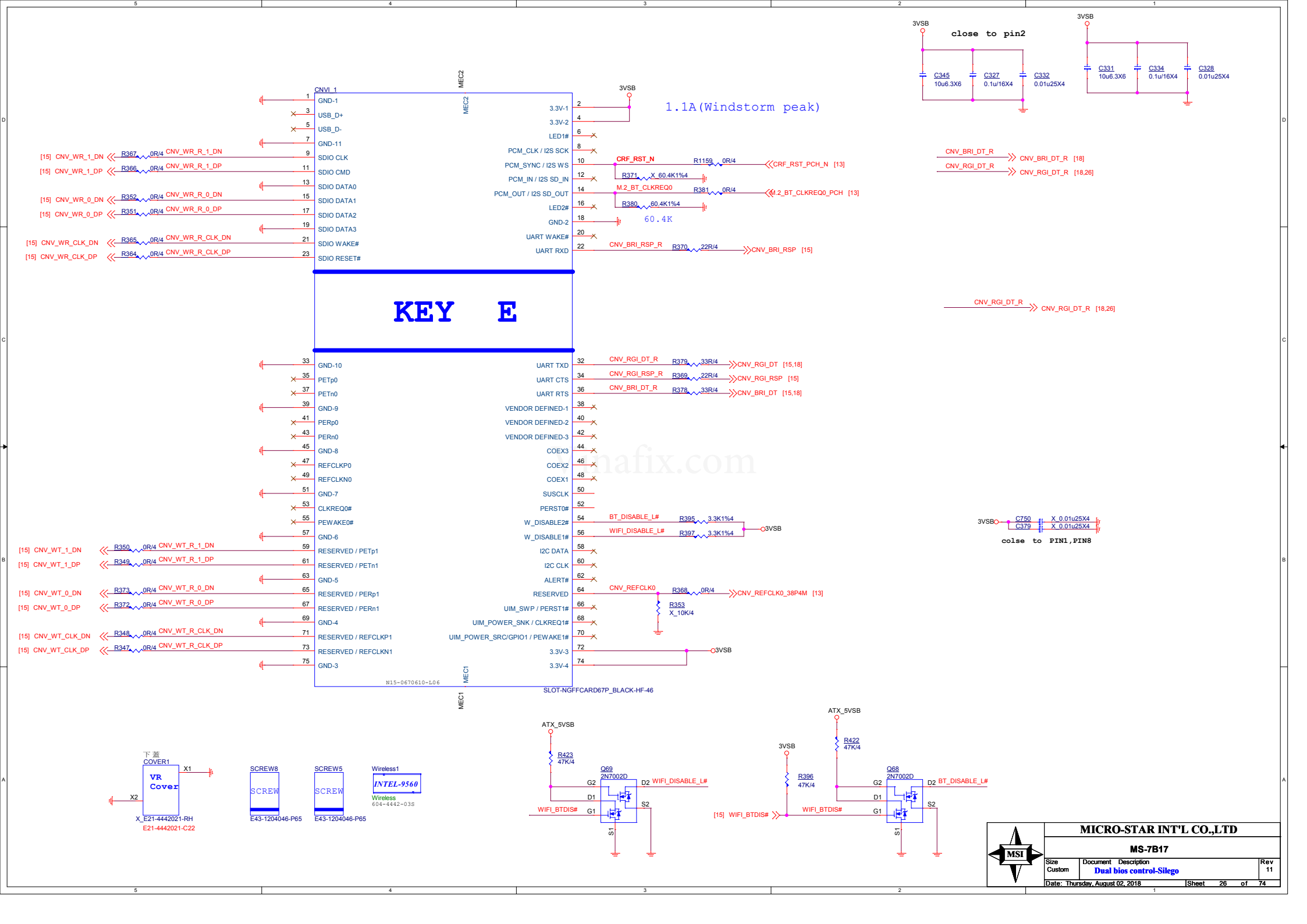
close to pin2
C345 10u6.3X6
C327 0.1u/16X4
C332 0.01u25X4
C331 10u6.3X6
C334 0.1u/16X4
C328 0.01u25X4
1.1A(Windstorm peak)
CNVI_1
MEC2
GND-1
USB_D+
USB_D-
GND-11
SDIO CLK
SDIO CMD
SDIO DATA0
SDIO DATA1
SDIO DATA2
SDIO DATA3
SDIO WAKE#
SDIO RESET#
3.3V-1
3.3V-2
LED1#
PCM_CLK / I2S SCK
PCM_SYNC / I2S WS
PCM_IN / I2S SD_IN
PCM_OUT / I2S SD_OUT
LED2#
GND-2
UART WAKE#
UART RXD
CRF_RST_N
M.2_BT_CLKREQ0
60.4K
KEY E
GND-10
PETp0
PETn0
GND-9
PERp0
PERn0
GND-8
REFCLKP0
REFCLKN0
GND-7
CLKREQ0#
PEWAKE0#
GND-6
RESERVED / PETp1
RESERVED / PETn1
GND-5
RESERVED / PERp1
RESERVED / PERn1
GND-4
RESERVED / REFCLKP1
RESERVED / REFCLKN1
GND-3
UART TXD
UART CTS
UART RTS
VENDOR DEFINED-1
VENDOR DEFINED-2
VENDOR DEFINED-3
COEX3
COEX2
COEX1
SUSCLK
PERST0#
W_DISABLE2#
W_DISABLE1#
I2C DATA
I2C CLK
ALERT#
RESERVED
UIM_SWP / PERST1#
UIM_POWER_SNK / CLKREQ1#
UIM_POWER_SRC/GPIO1 / PEWAKE1#
3.3V-3
3.3V-4
N15-0670610-L06
MEC1
SLOT-NGFFCARD67P_BLACK-HF-46
colse to PIN1,PIN8
COVER1
VR Cover
X_E21-4442021-RH
E21-4442021-C22
SCREW8
SCREW5
E43-1204046-P65
Wireless1
INTEL-9560
Wireless
604-4442-03S
Q69 2N7002D
Q68 2N7002D
WIFI_DISABLE_L#
BT_DISABLE_L#
WIFI_BTDIS#
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Dual bios control-Silego
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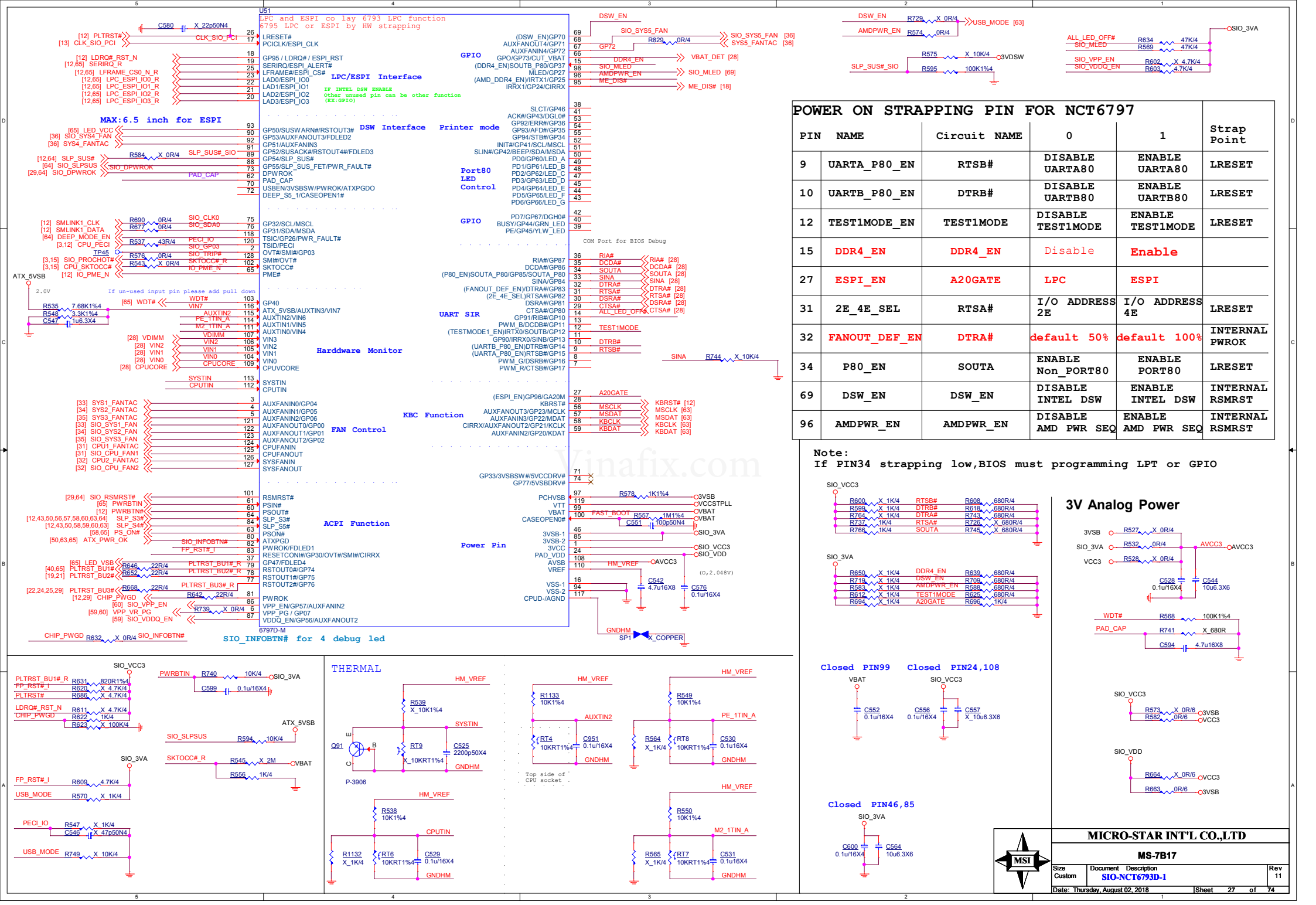
U51
LPC and ESPI co lay 6793 LPC function
6795 LPC or ESPI by HW strapping
LPC/ESPI Interface
IF INTEL DSW ENABLE
Other unused pin can be other function
(EX:GPIO)
MAX:6.5 inch for ESPI
DSW Interface
Printer mode
Port80
LED
Control
GPIO
COM Port for BIOS Debug
UART SIR
Harddware Monitor
KBC Function
FAN Control
ACPI Function
Power Pin
SIO_INFOBTN# for 4 debug led
6797D-M
POWER ON STRAPPING PIN FOR NCT6797
PIN NAME Circuit NAME 0 1 Strap Point
9 UARTA_P80_EN RTSB# DISABLE UARTA80 ENABLE UARTA80 LRESET
10 UARTB_P80_EN DTRB# DISABLE UARTB80 ENABLE UARTB80 LRESET
12 TEST1MODE_EN TEST1MODE DISABLE TEST1MODE ENABLE TEST1MODE LRESET
15 DDR4_EN DDR4_EN Disable Enable
27 ESPI_EN A20GATE LPC ESPI
31 2E_4E_SEL RTSA# I/O ADDRESS 2E I/O ADDRESS 4E LRESET
32 FANOUT_DEF_EN DTRA# default 50% default 100% INTERNAL PWROK
34 P80_EN SOUTA ENABLE Non_PORT80 ENABLE PORT80 LRESET
69 DSW_EN DSW_EN DISABLE INTEL DSW ENABLE INTEL DSW INTERNAL RSMRST
96 AMDPWR_EN AMDPWR_EN DISABLE AMD PWR SEQ ENABLE AMD PWR SEQ INTERNAL RSMRST
Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO
3V Analog Power
Closed PIN99
Closed PIN24,108
Closed PIN46,85
THERMAL
P-3906
Top side of CPU socket
MICRO-STAR INT'L CO.,LTD
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SIO-NCT6793D-1
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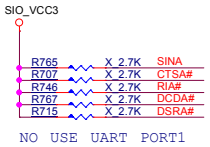
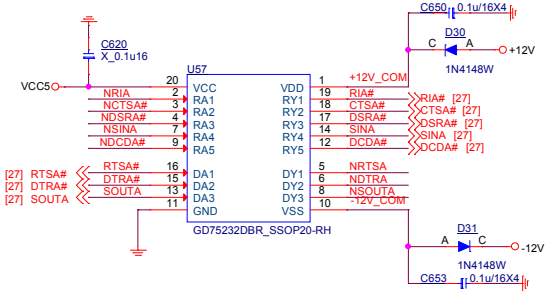
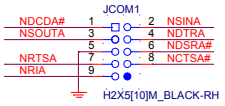
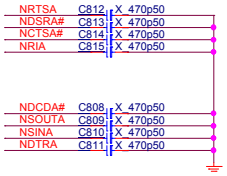
SERIAL PORT 1

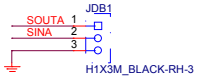






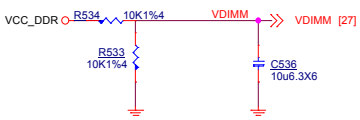


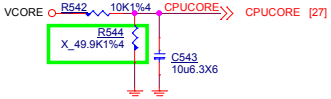
BIOS DEBUG

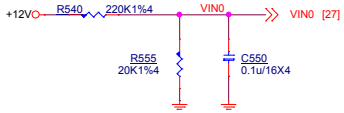


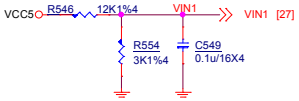
HW Monitor - Voltage

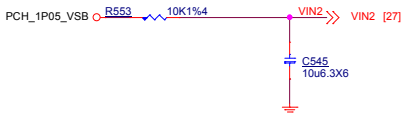
SIO HM Voltage voer 2V will not detect



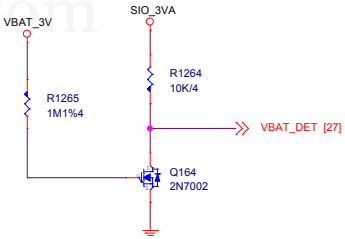








VBAT_DET



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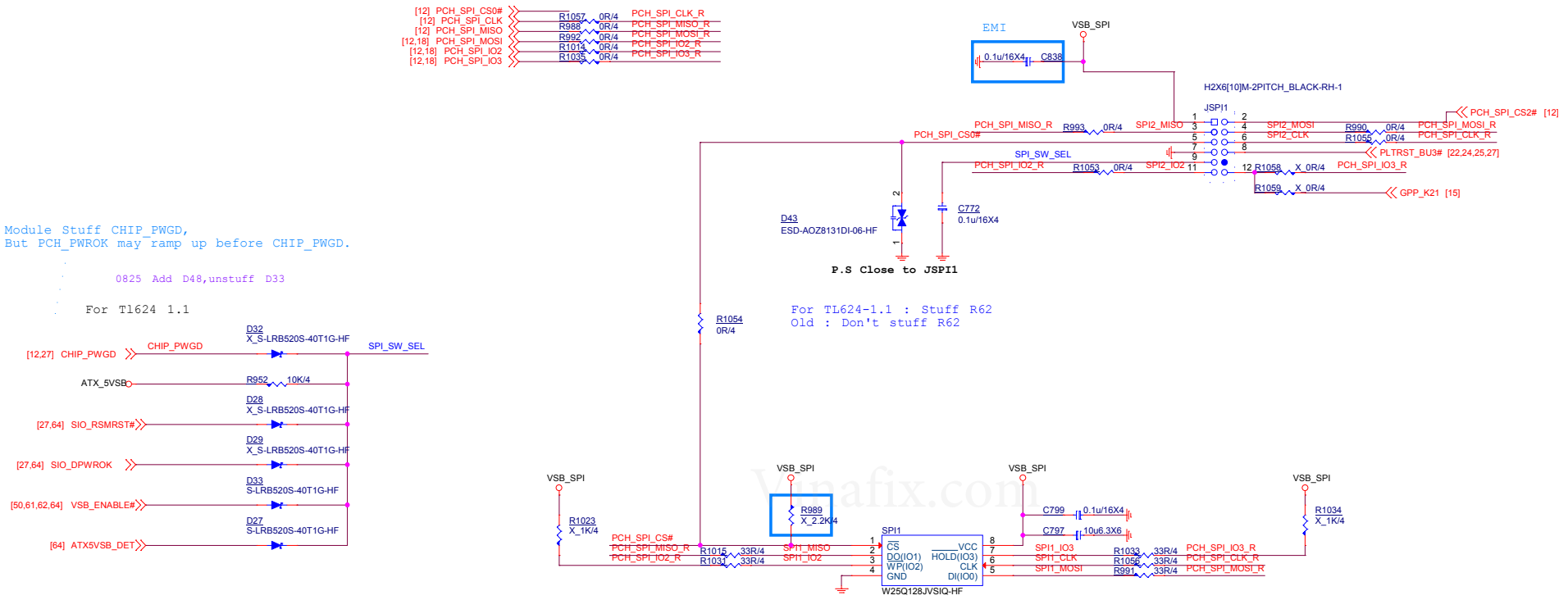

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Size: Custom	Document Description: CLR COMS/CUT VBAT
Rev: 11	
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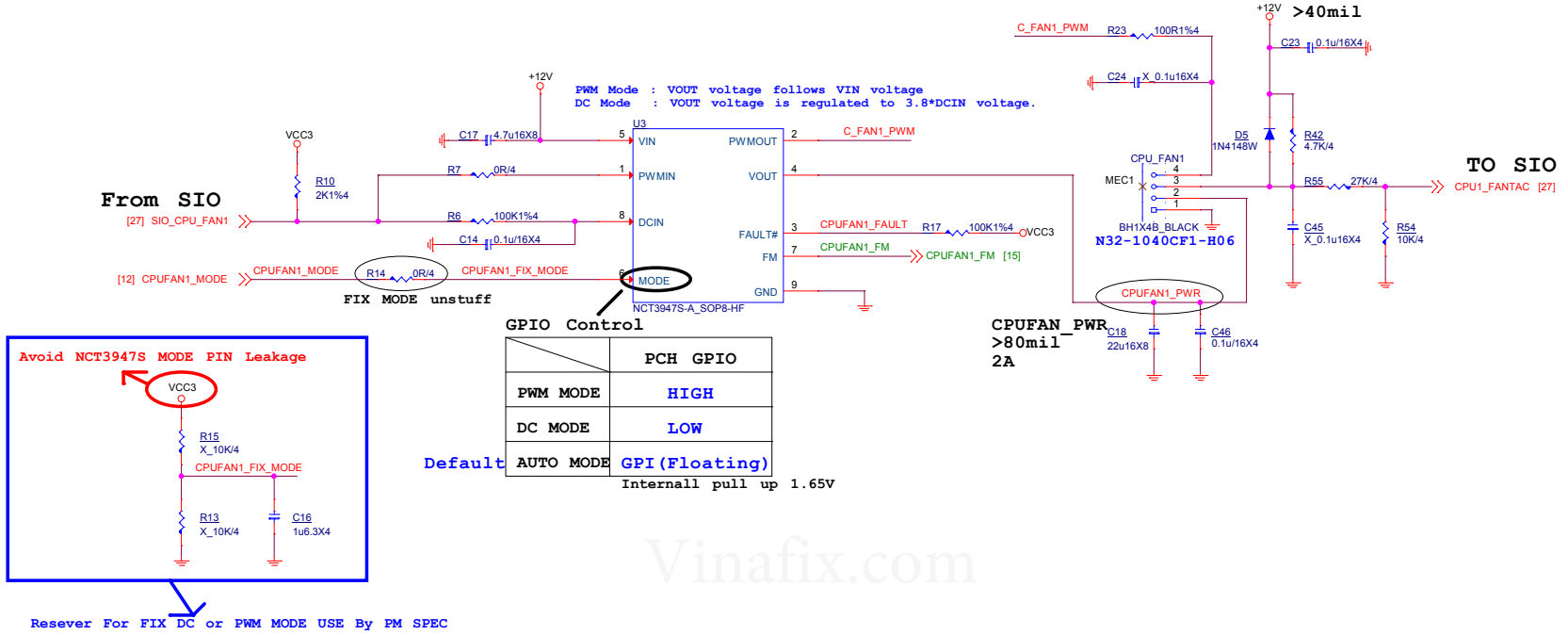
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



MICRO-STAR INT'L CO.,LTD		
MS-7B17		
Size: Custom	Document Description: CPU FAN1	Rev: 11
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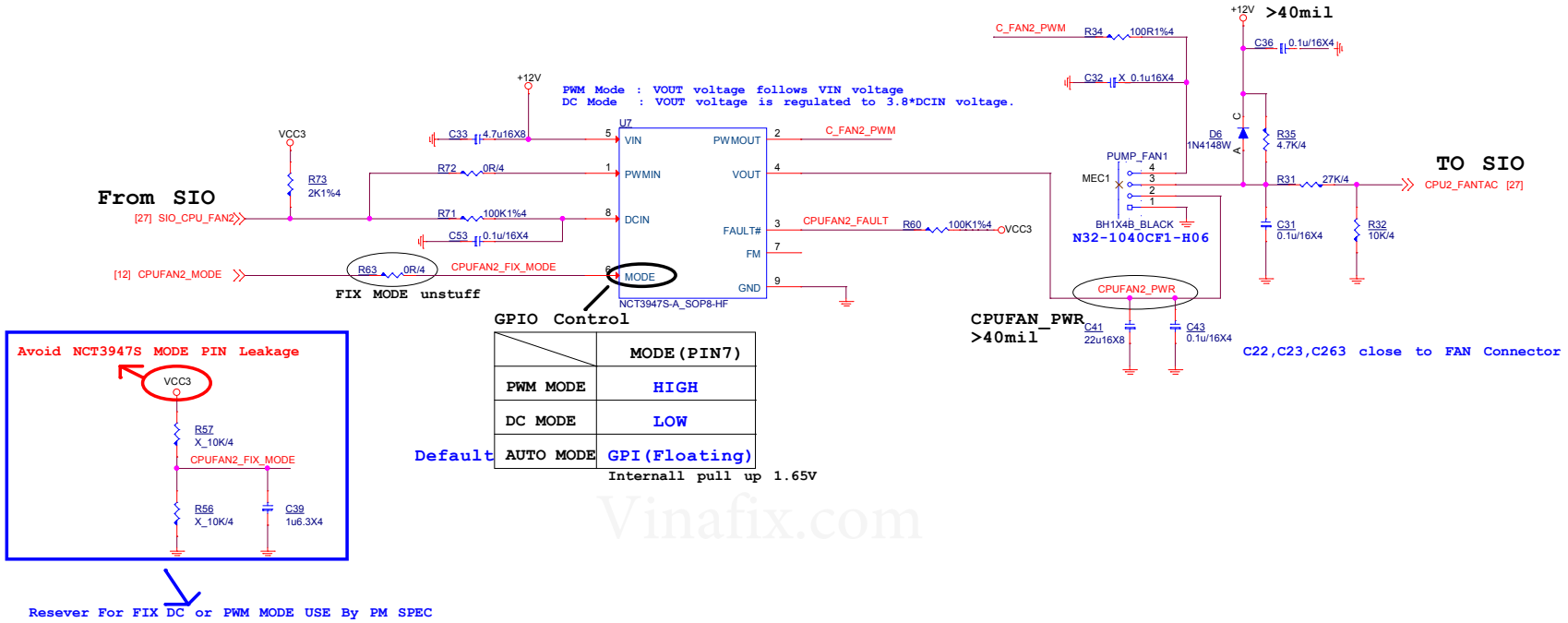
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

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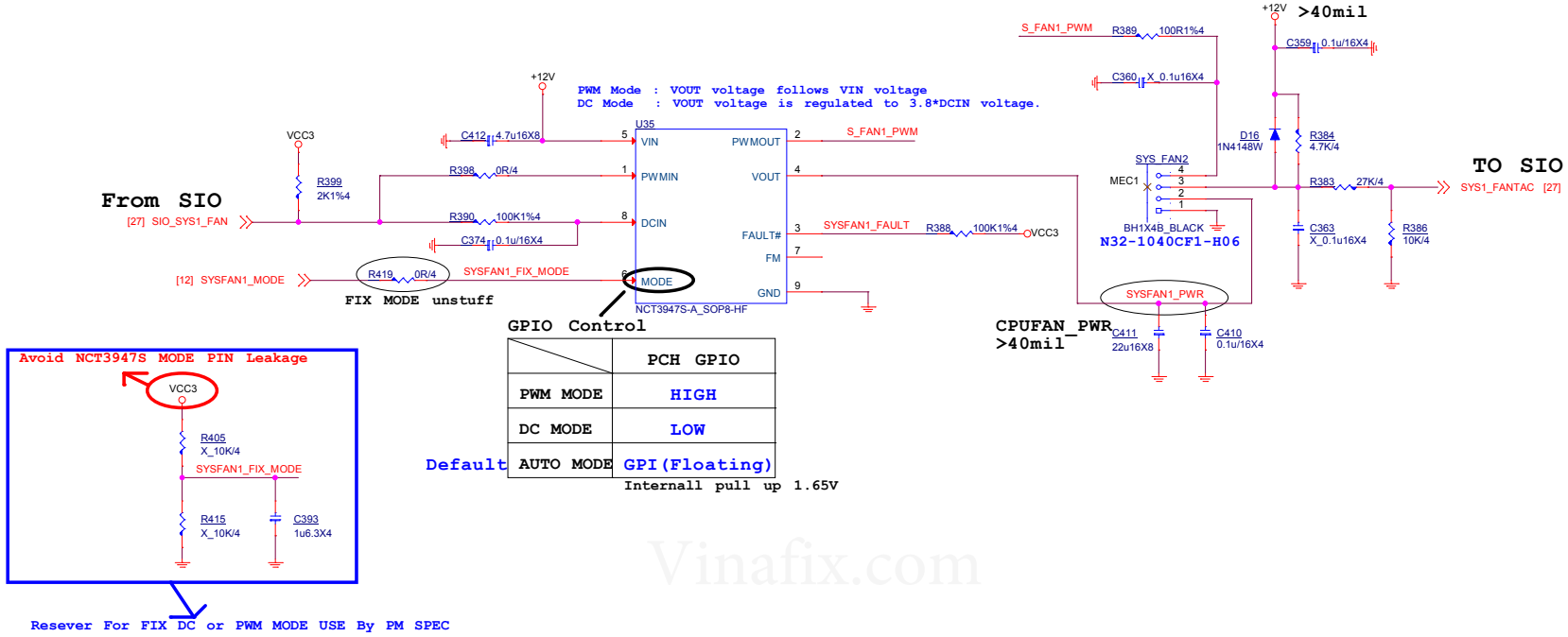

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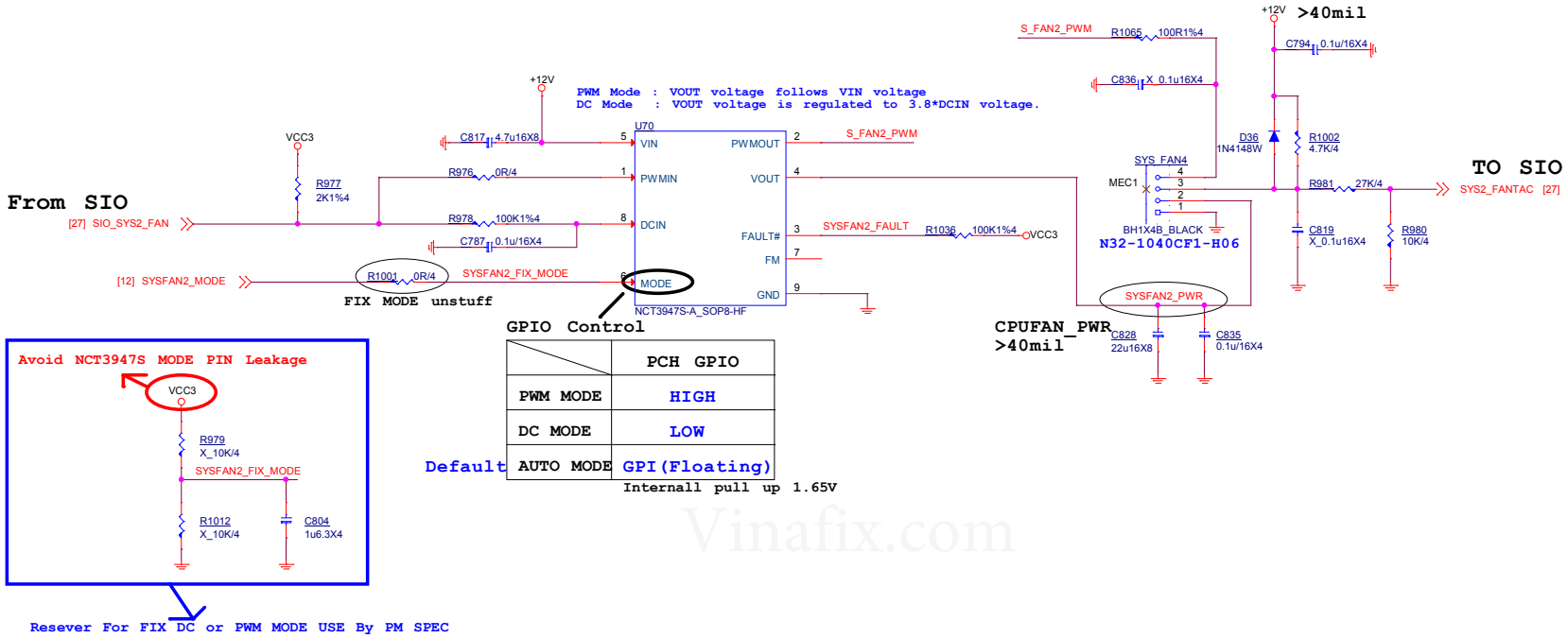
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

Resever For FIX DC or PWM MODE USE By PM SPEC

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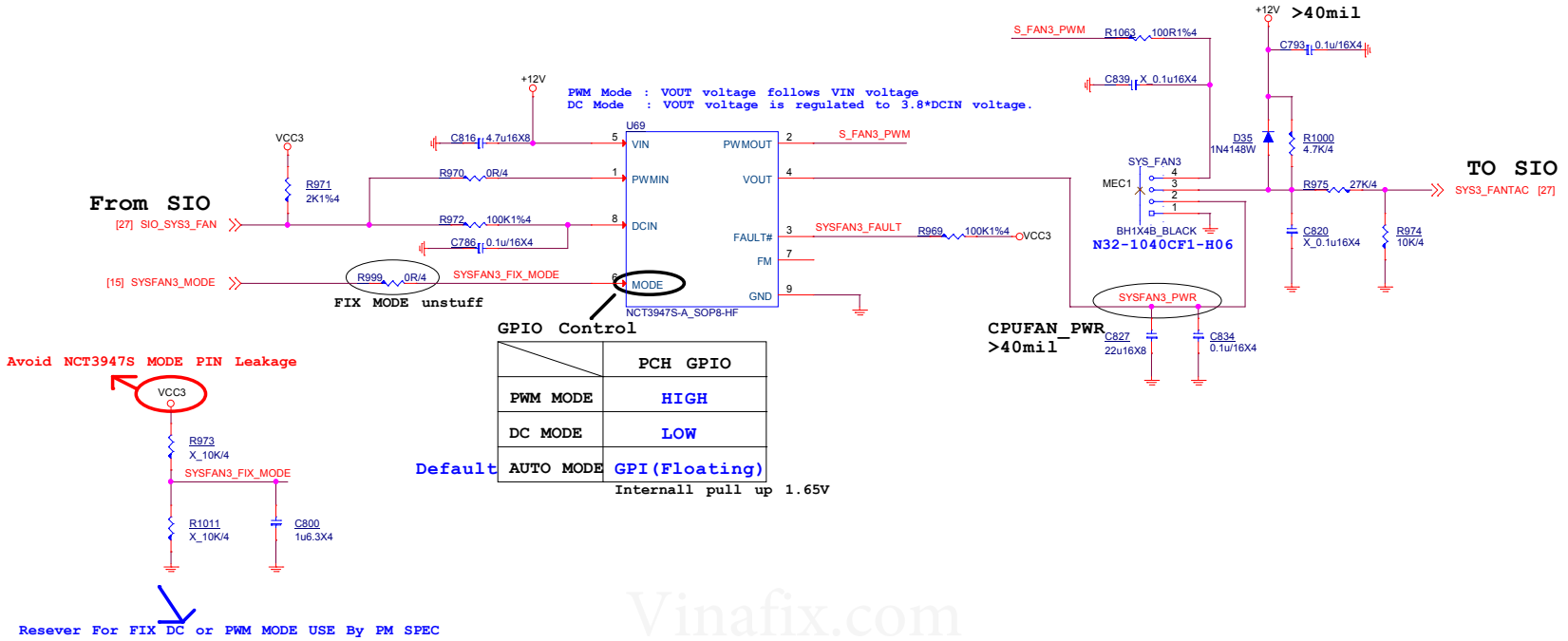
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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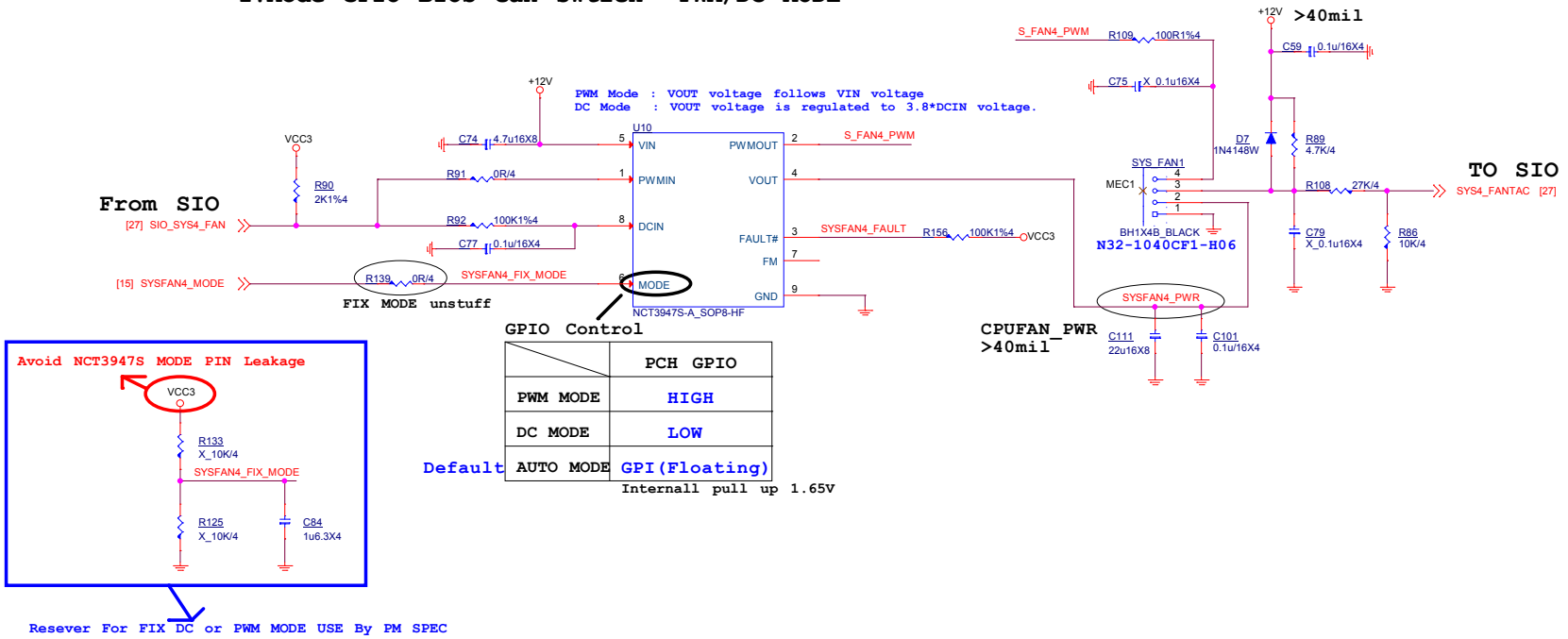
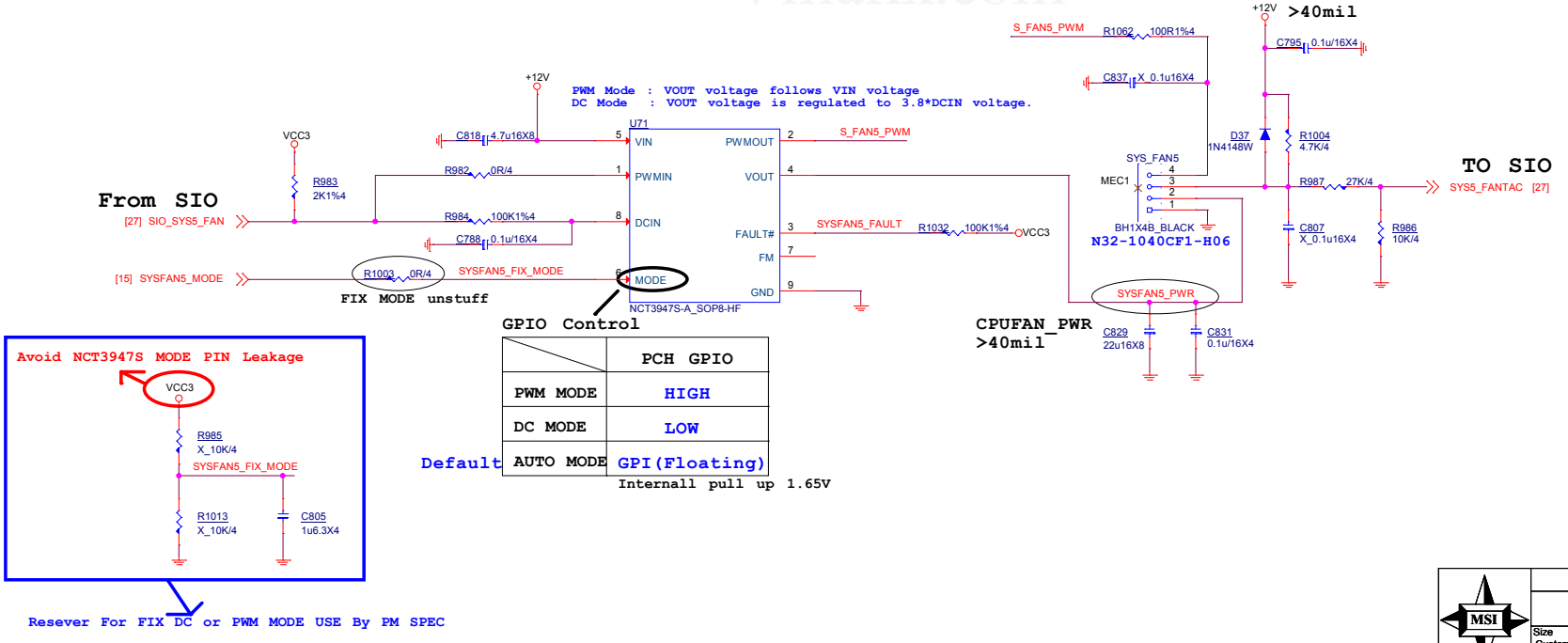
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE





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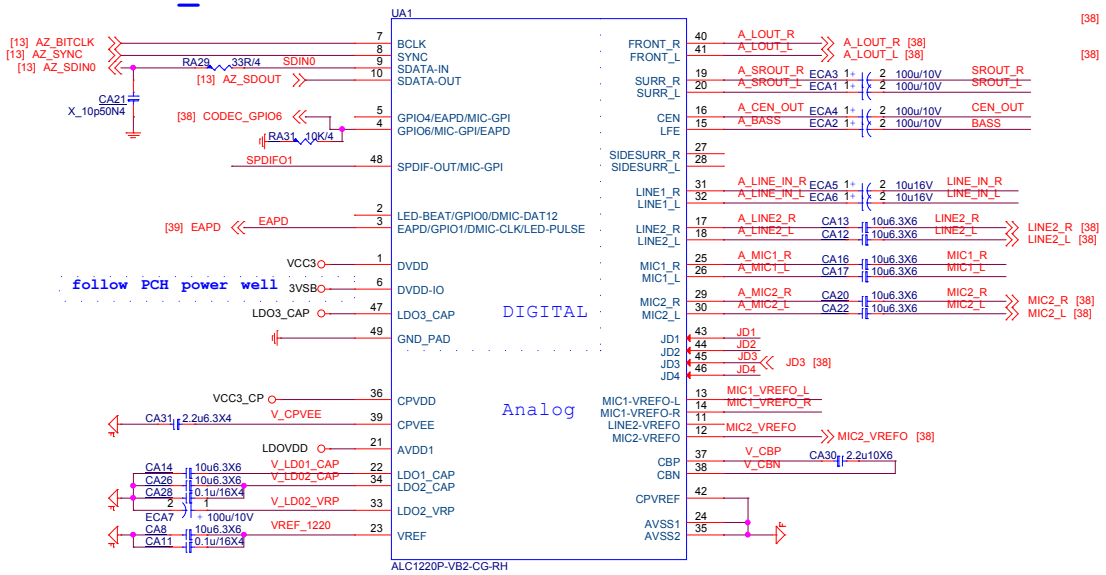
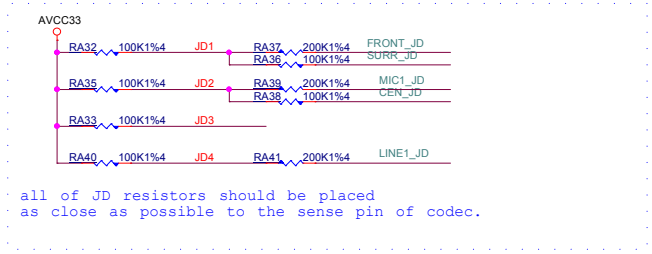
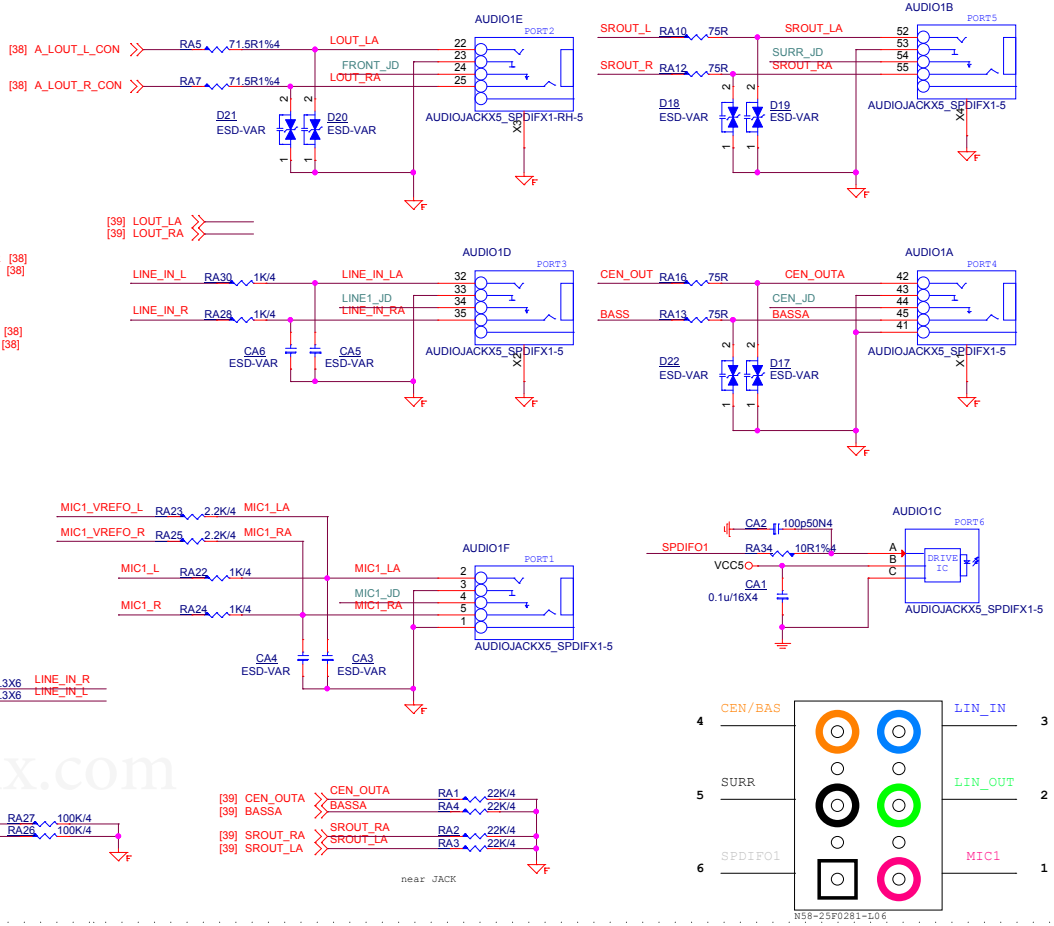
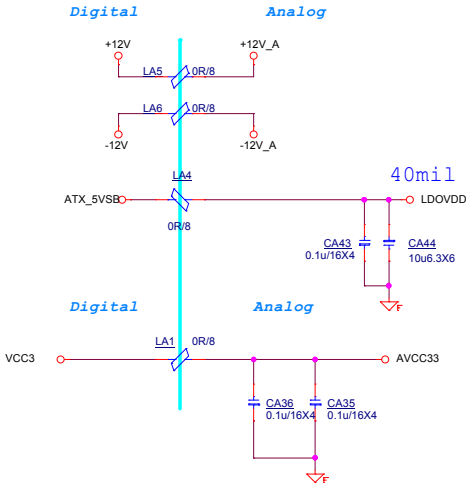
ALC1220P_VB-48PIN

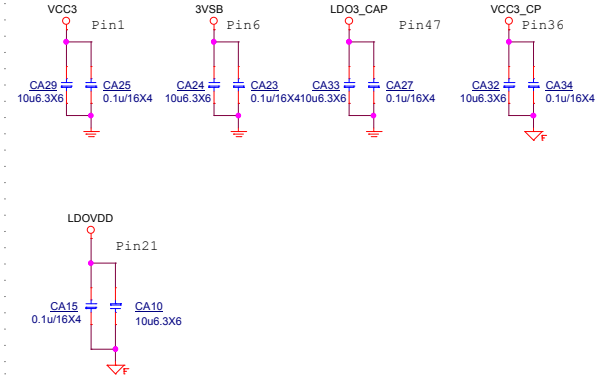




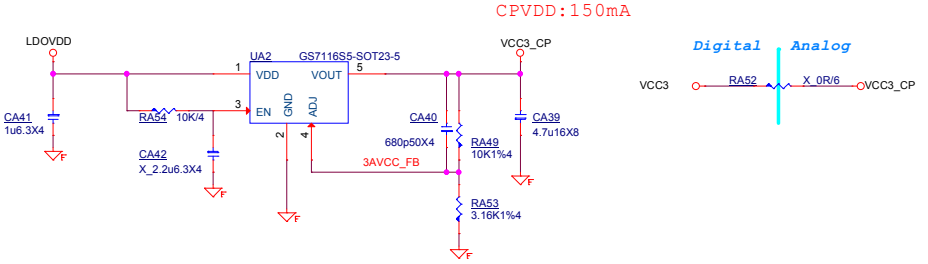


Closed Codec





CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V



EMI

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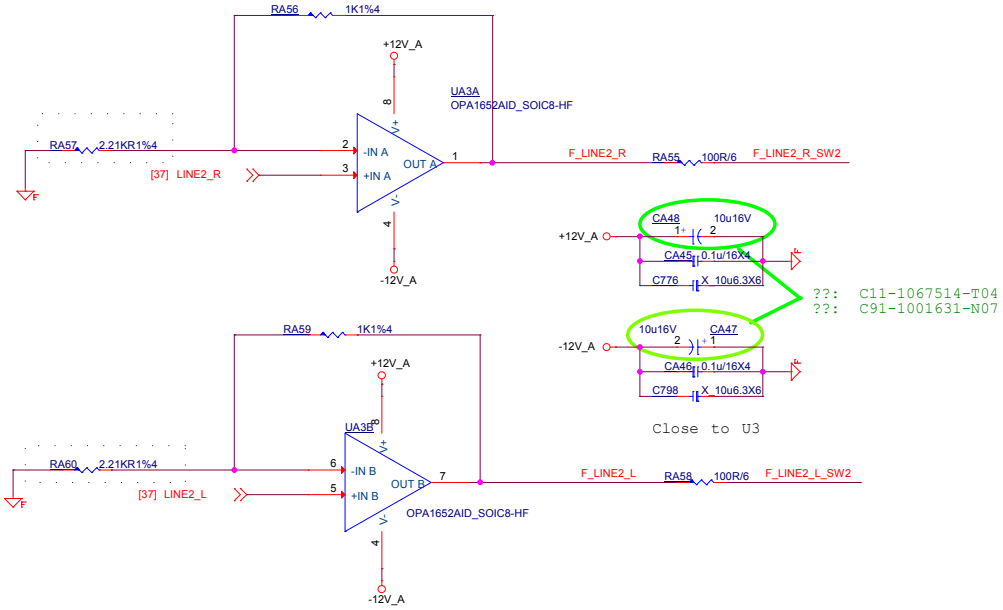
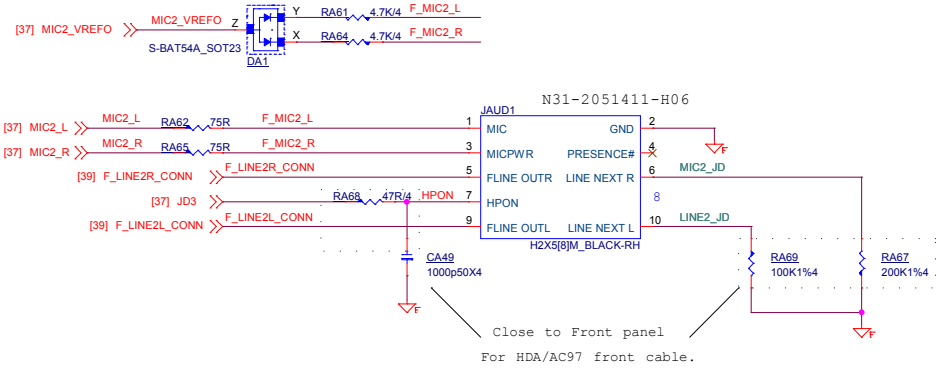
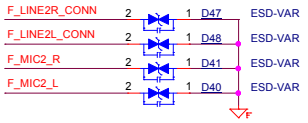
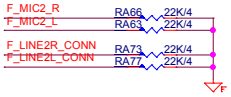




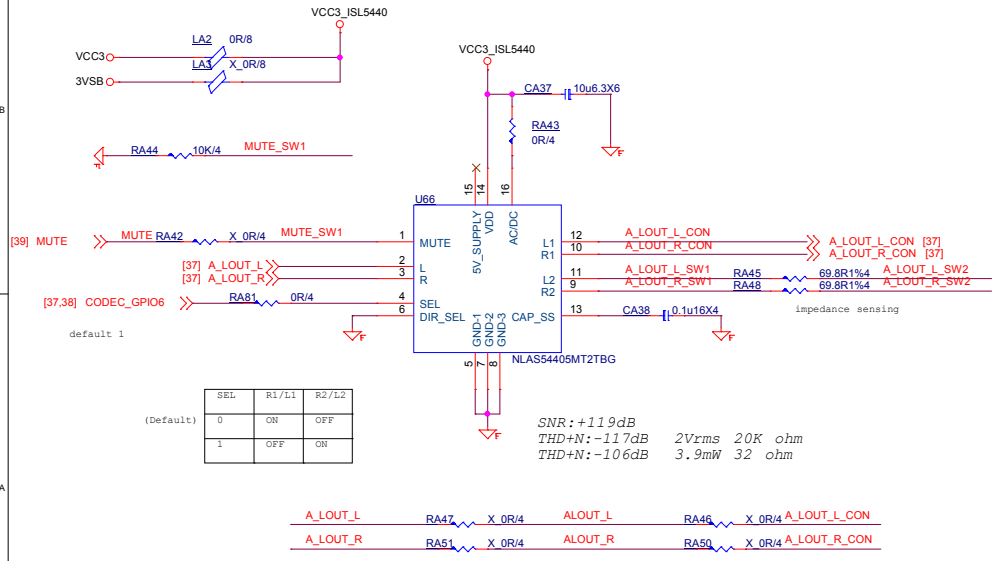
Close to Jack

ESD protect

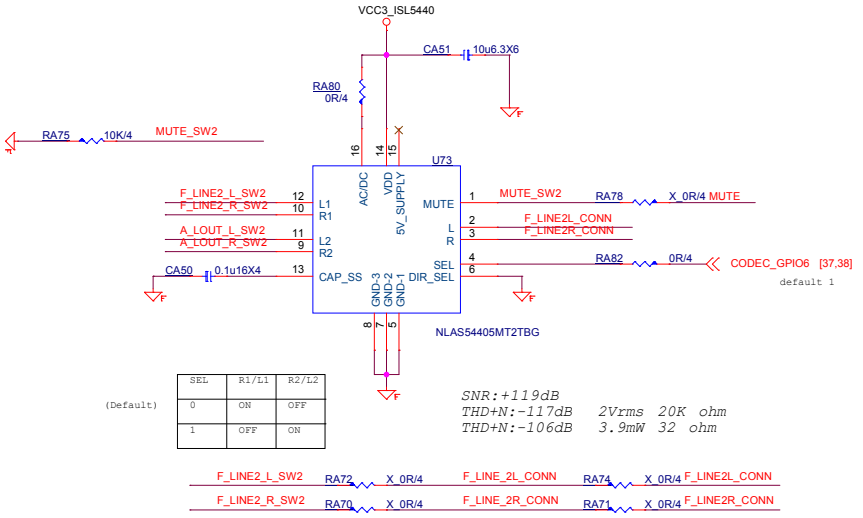




Analong SW1



Analong SW2



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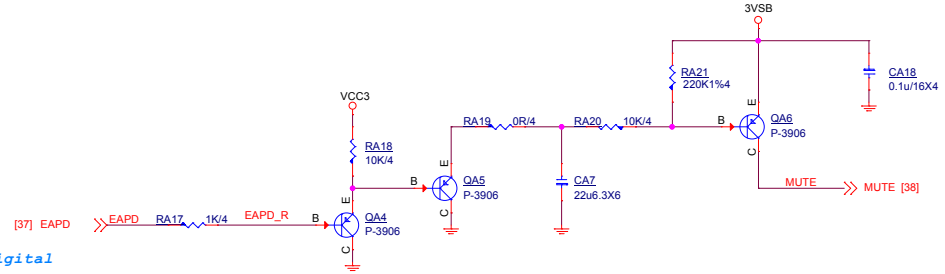
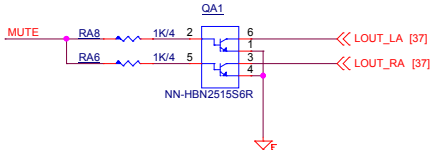
Rear Line OUT De-POP circuit

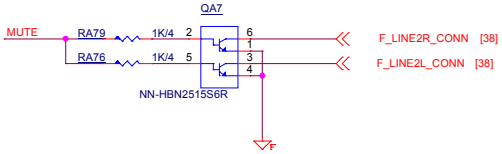
(De-pop circuit for Rear Line out & Front Headphone out)



Digital

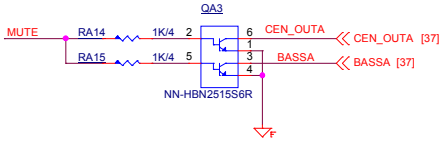
Analog

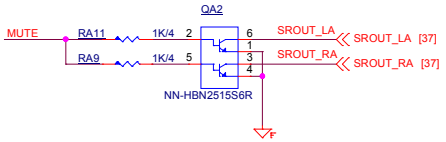




Audio moat is transparent and width 40mil

(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change SROUT_LA,SROUT_RA, CEN_OUTA, BASSA to TVS)





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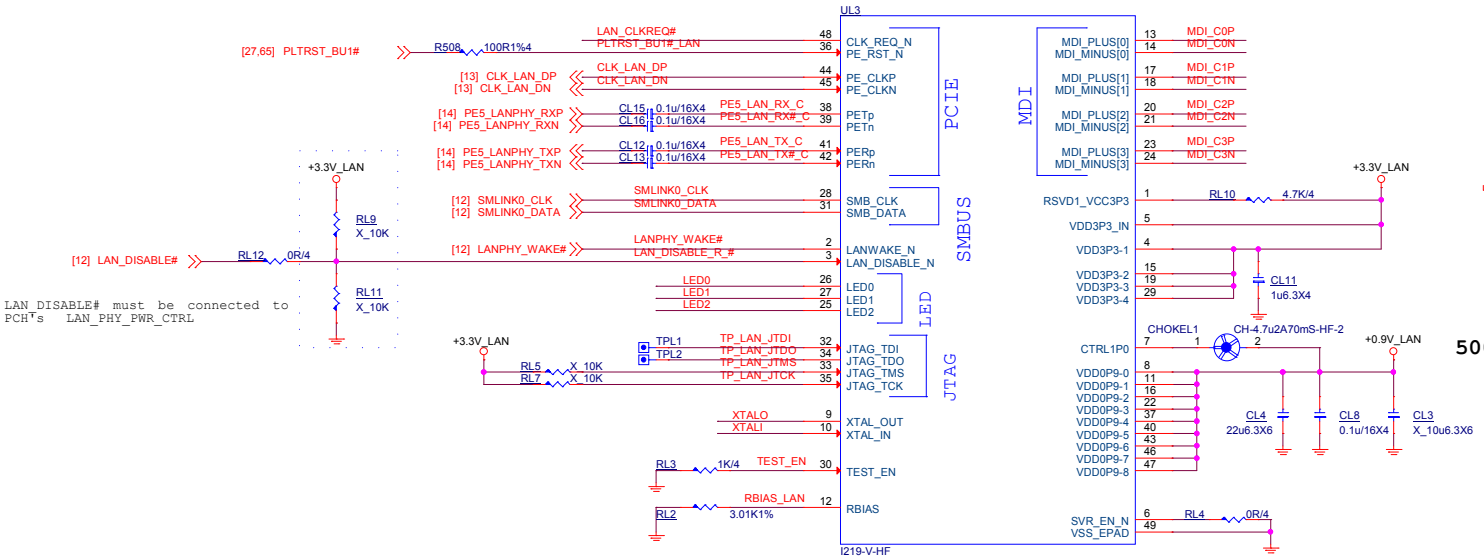
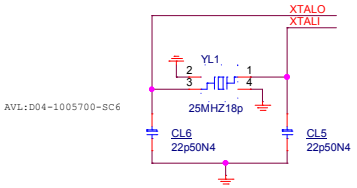
Intel Lan- i219

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

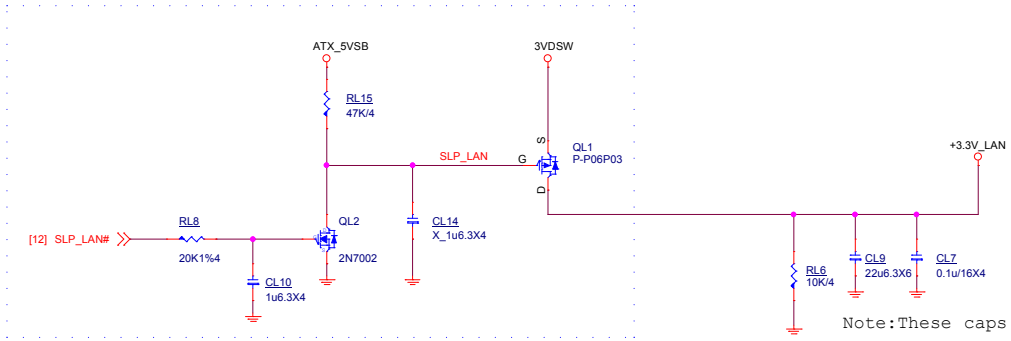


PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN



The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.

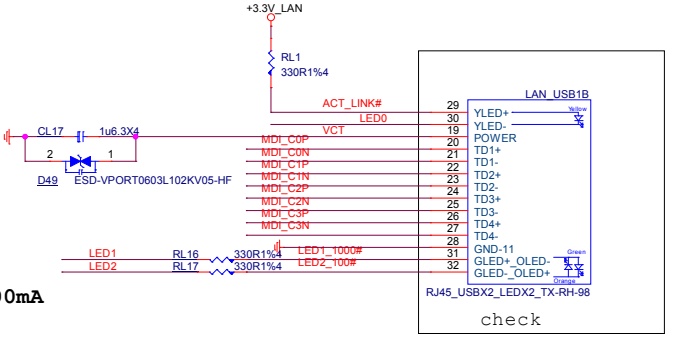


Note:These caps closed to PHY

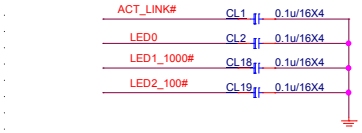
+3.3V_LAN

I218:132mA
I219:542mW

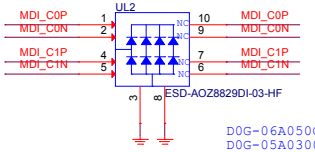
LAN Connector



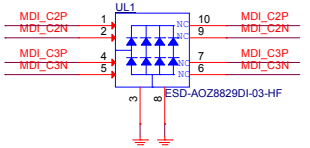
For EMI



UL2&UL3 close to connector



D0G-06A050C-A68
D0G-05A0300-I14



Do not pair MDI0 and MDI1 on the same TVSdevice (avoid LAN POE connecting issue).
Otherpairing combination is ok.

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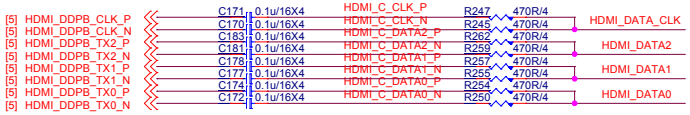
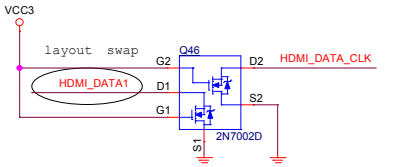
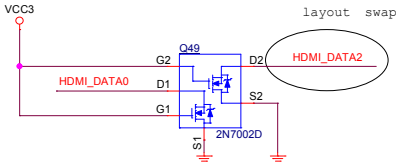
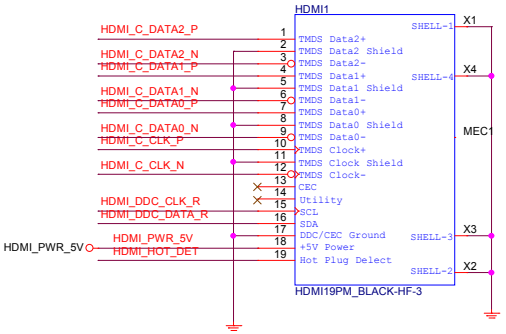
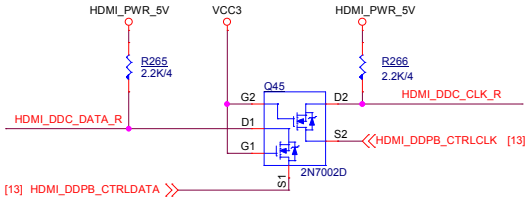
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

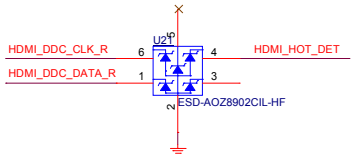


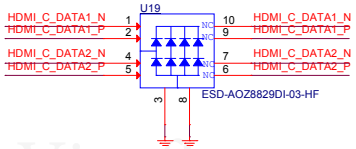


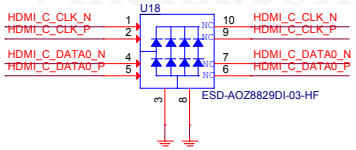


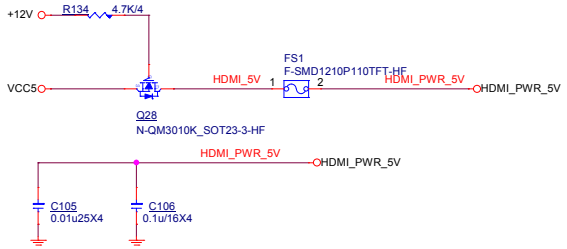


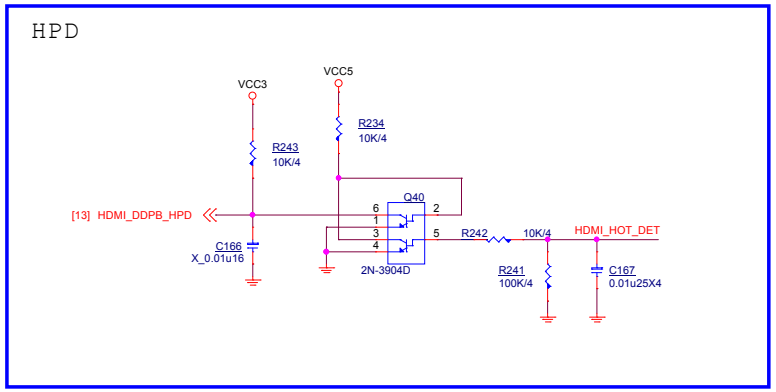


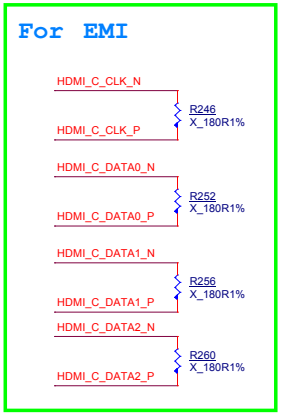












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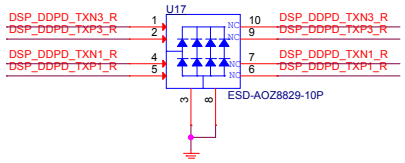
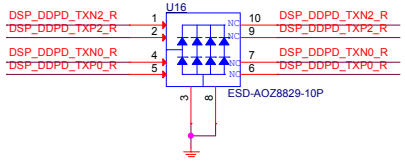
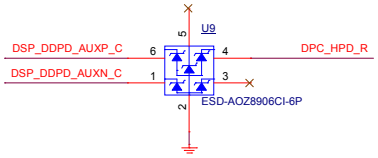
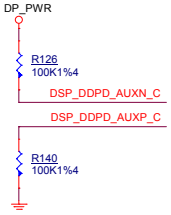
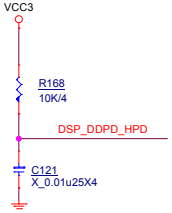
DP

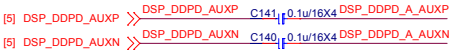


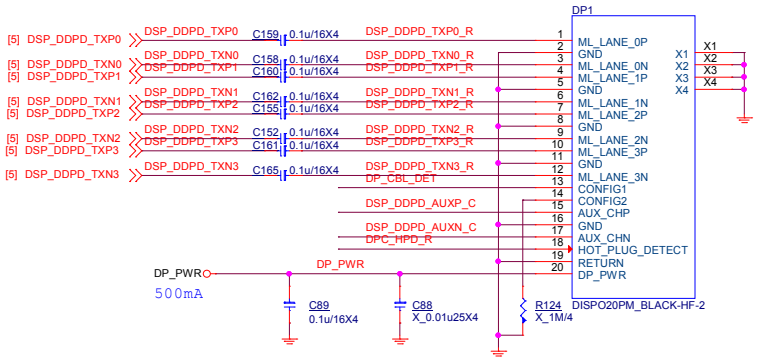




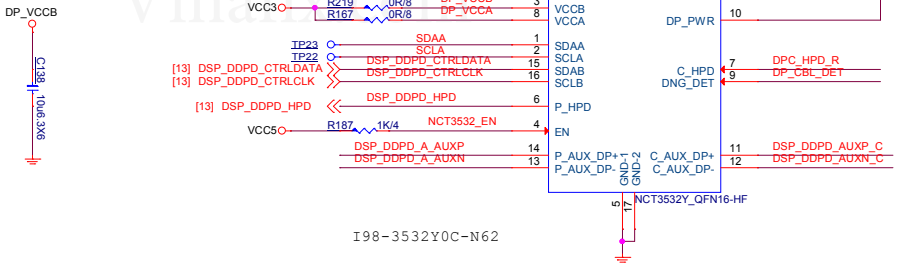


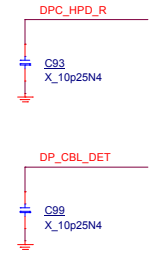




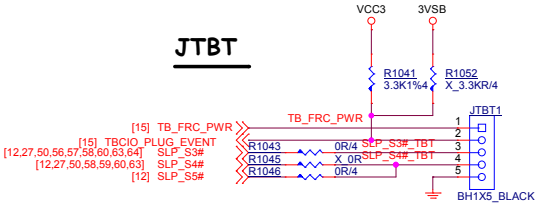


DP_VCCB trace don't less than 30 mil





JTBT



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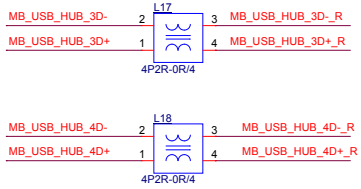
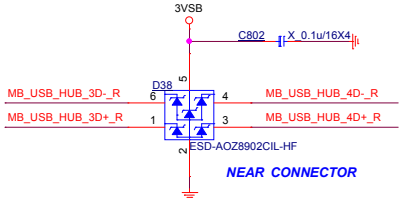
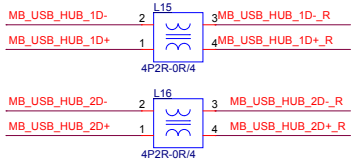
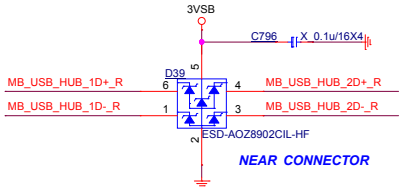
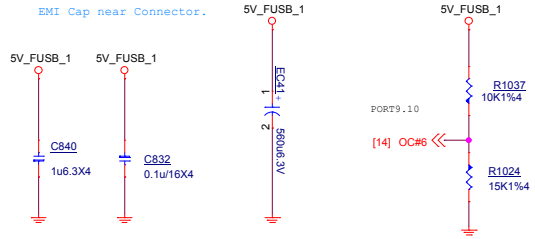


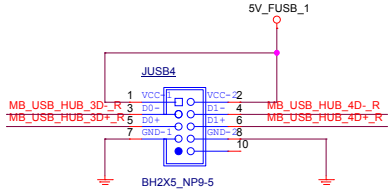


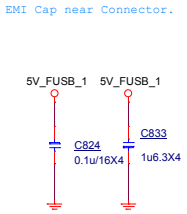




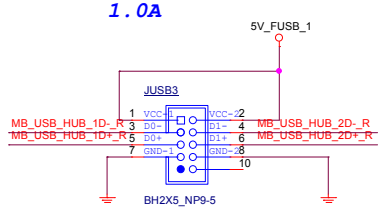
1.0A





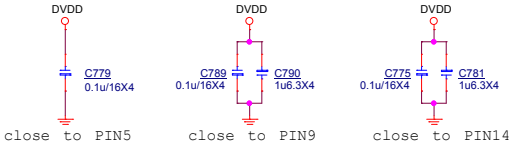


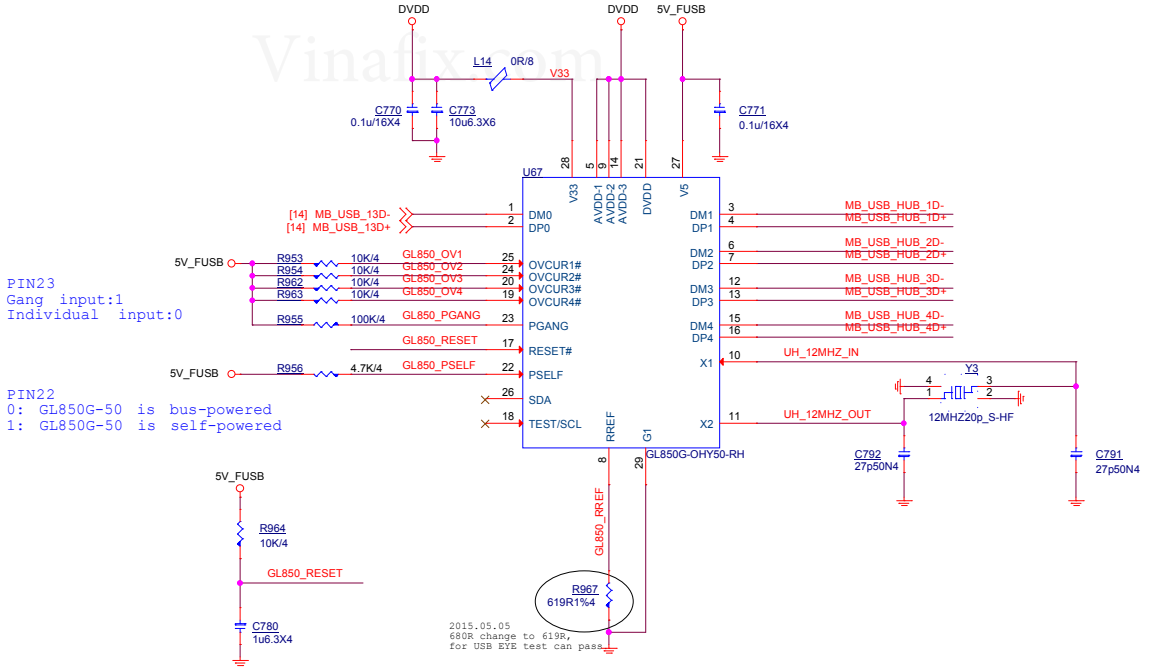
1.0A



USB2.0 HUB

4-port at high-speed mode. --> 58.6mA





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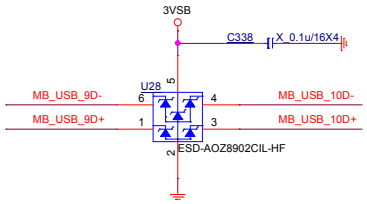

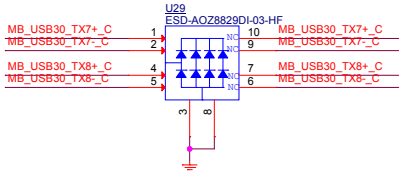

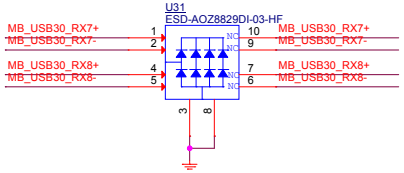

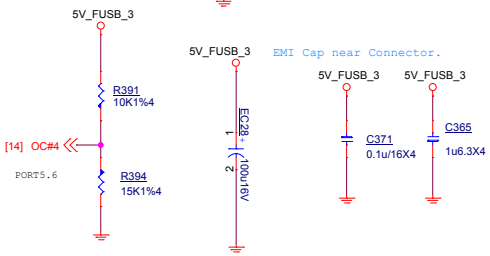

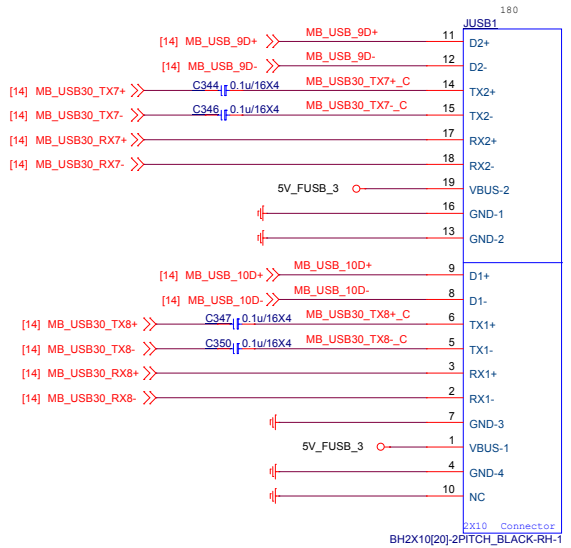

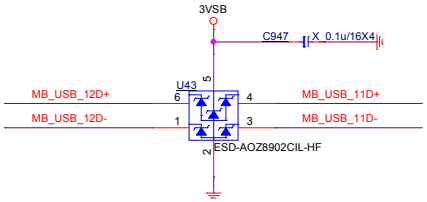

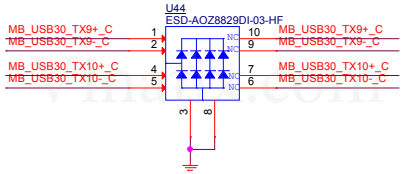

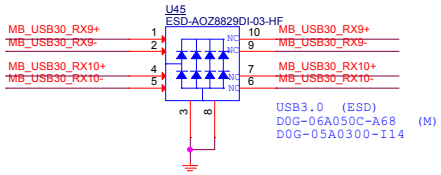

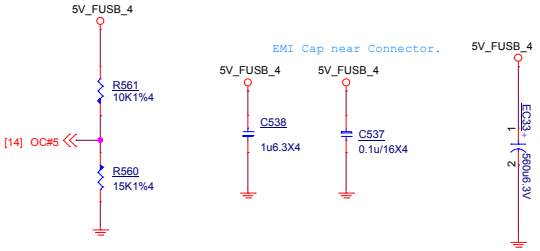

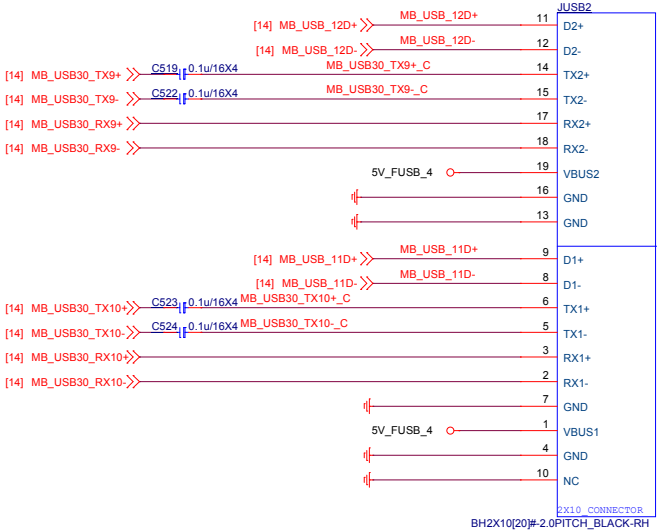

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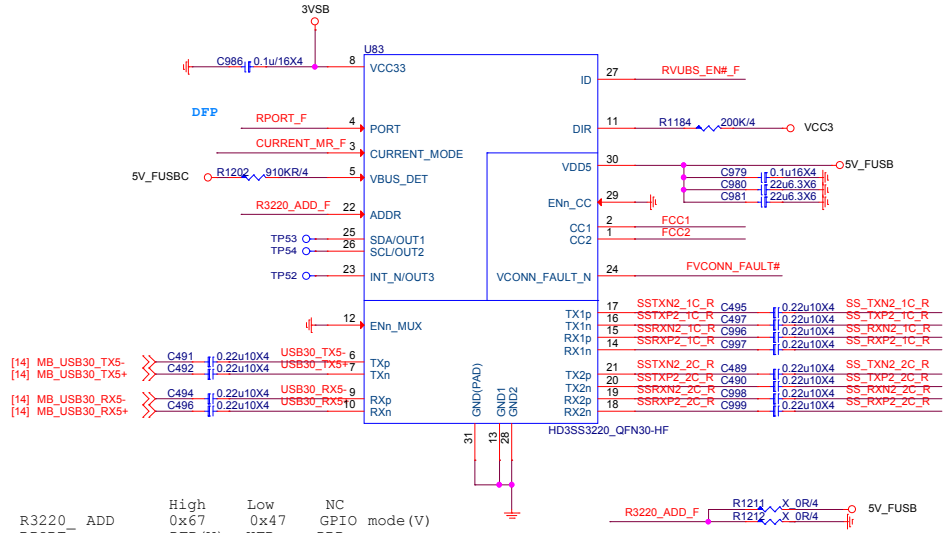
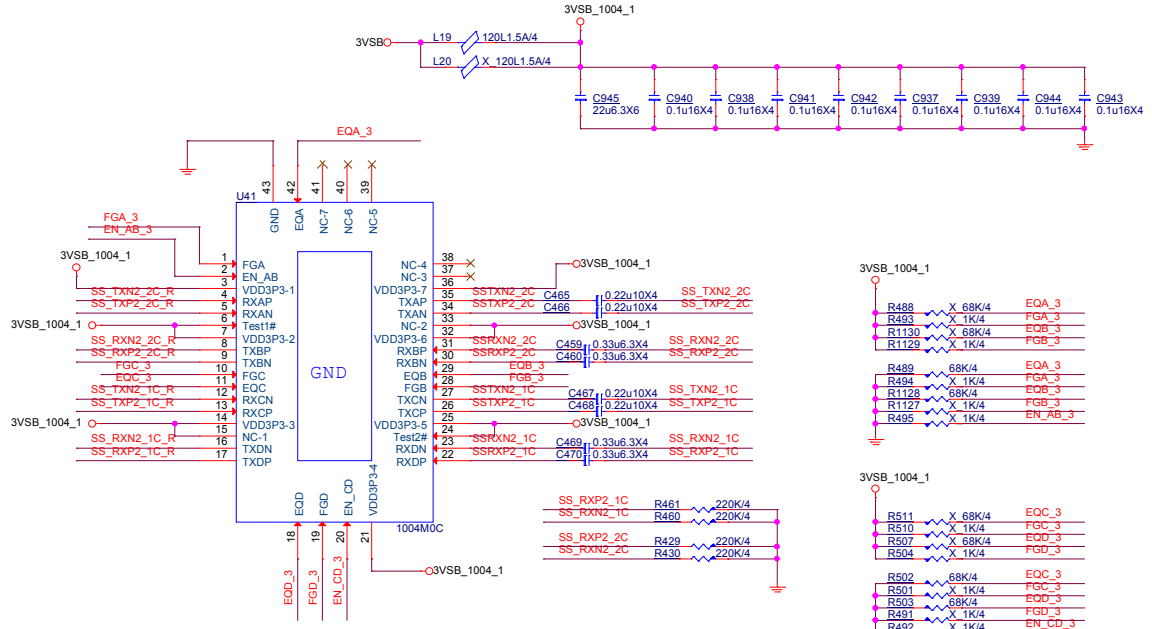


R3220_ ADD	High	Low	NC
RPORT	0x67 DFP(V)	0x47 UFP	GPIO mode(V) DRP

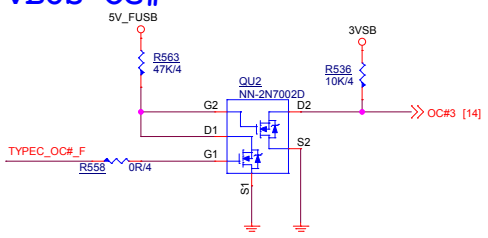


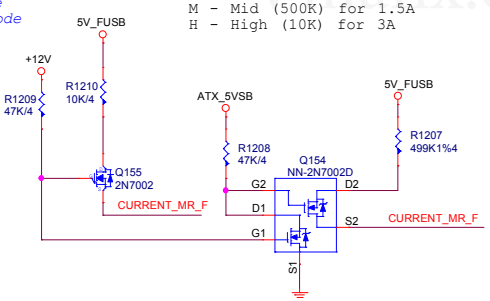
Current Mode

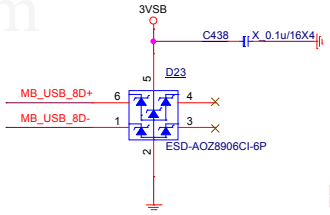
3A under S0 mode
1.5A under S3 mode

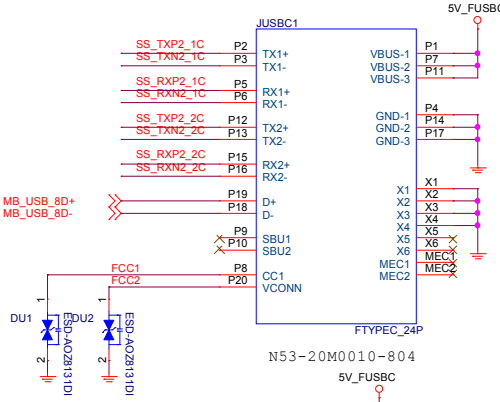
L - Default for 900mA
M - Mid (500K) for 1.5A
H - High (10K) for 3A

VBUS OC#

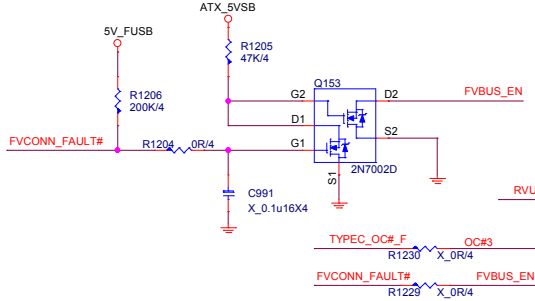






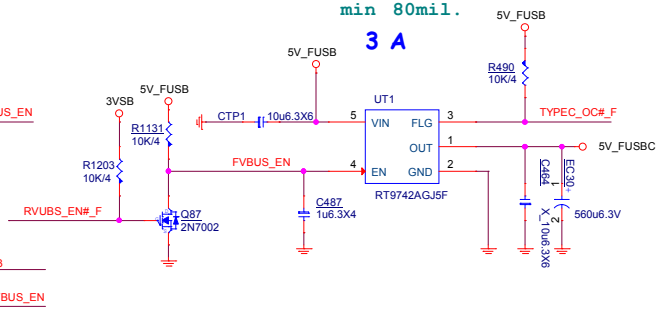


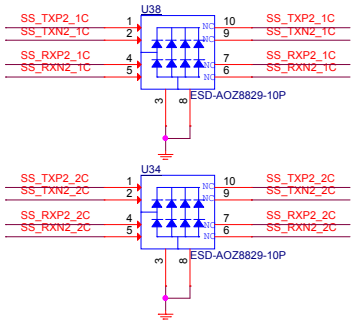
VCONN OC#

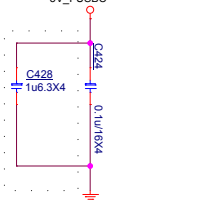


min 80mil.

3 A







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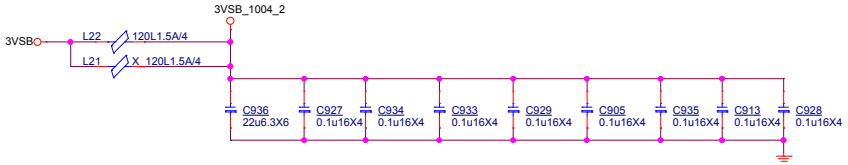
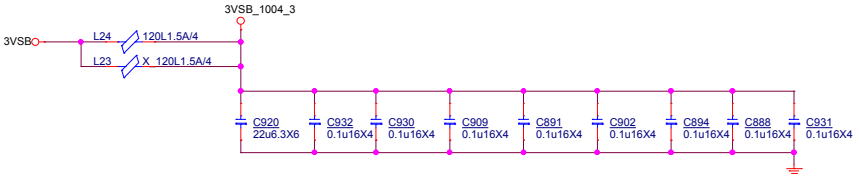
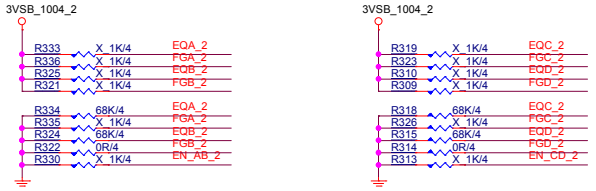
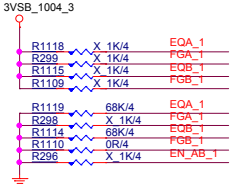
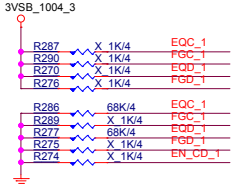
Rear USB3.1 Redriver

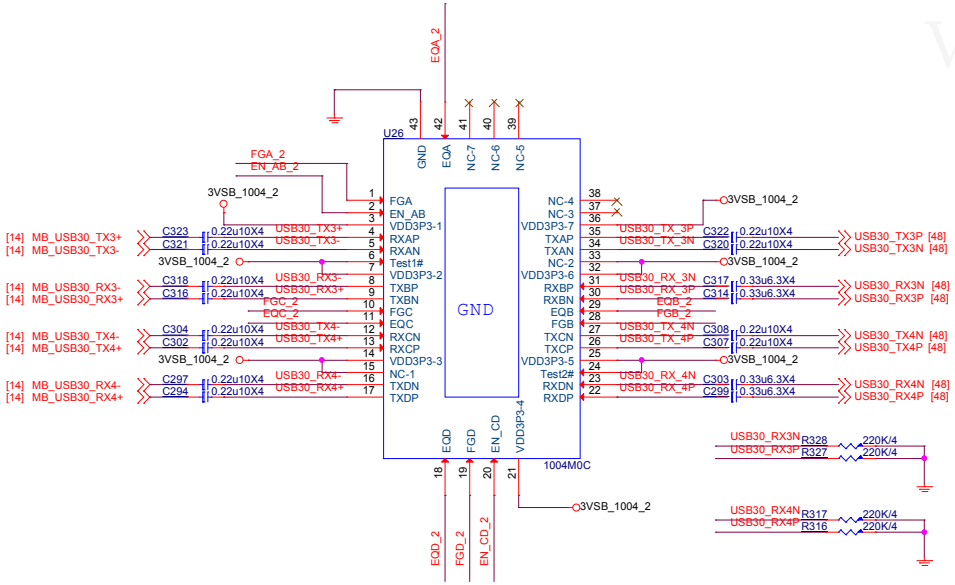


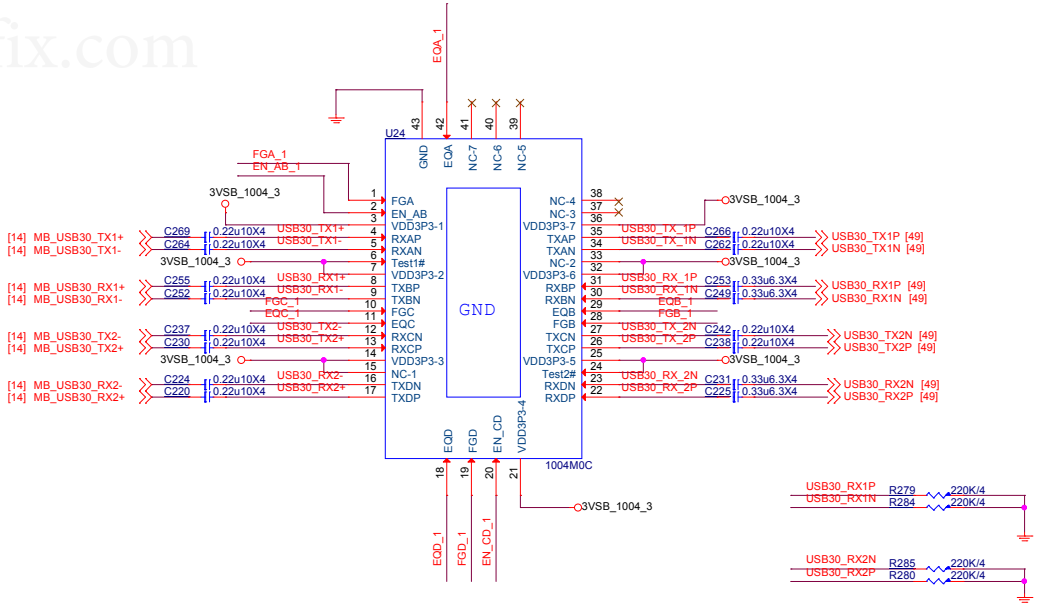












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LAN USB2.0 &3.0

1.8A

[14] MB_USB_2D+
[14] MB_USB_2D-
[14] MB_USB_1D+
[14] MB_USB_1D-
[47] USB30_TX3P
[47] USB30_TX3N
[47] USB30_RX3P
[47] USB30_RX3N
[47] USB30_TX4P
[47] USB30_TX4N
[47] USB30_RX4P
[47] USB30_RX4N

U27
ESD-AOZ8829DI-03-HF
USB30_RX4P
USB30_RX4N
USB30_RX3P
USB30_RX3N

U25
ESD-AOZ8829DI-03-HF
USB30_TX4N
USB30_TX4P
USB30_TX3N
USB30_TX3P

3VSB
C857 X_0.1u/16X4
D15
MB_USB_2D+
MB_USB_2D-
MB_USB_1D+
MB_USB_1D-
ESD-AOZ8902CIL-HF

LAN_USB1A
MB_USB_1D+
MB_USB_1D-
USB30_TX4P
USB30_TX4N
USB30_RX4P
USB30_RX4N
MB_USB_2D+
MB_USB_2D-
USB30_TX3P
USB30_TX3N
USB30_RX3P
USB30_RX3N
D1+
D1-
SSTX1+
SSTX1-
SSRX1+
SSRX1-
UP
D0+
D0-
SSTX0+
SSTX0-
SSRX0+
SSRX0-
DOWN
VBUS-D1
VBUS-D0
GND-D1
GND-01
GND-02
GND-03
GND-04
GND-05
GND-D0
GND-06
GND-07
GND-08
GND-09
GND-10
5V_RUSB_3
RJ45_USBX2_LEDX2_TX-RH-98

5V_RUSB_3
C364 1u6.3X4
C361 0.1u/16X4
EC29 560u6.3V
R424 10K1%4
PORT13.14
[14] OC#0
R436 15K1%4
C274 22u6.3X6

[14] MB_USB_3D-
[14] MB_USB_3D+
L1
4P2R-0R/4
MB_USB_3D-_R
MB_USB_3D+_R
[14] MB_USB_4D-
[14] MB_USB_4D+
L2
4P2R-0R/4
MB_USB_4D-_R
MB_USB_4D+_R

3VSB
C326 0.1u/16X4
D8
MB_USB_3D+_R
MB_USB_3D-_R
MB_USB_4D+_R
MB_USB_4D-_R
ESD-AOZ8902CIL-HF
NEAR CONNECTOR

5V_RUSB_1
PS2_USB1B
MB_USB_3D-_R
MB_USB_3D+_R
MB_USB_4D-_R
MB_USB_4D+_R
VCC-1
USB2-
USB2+
VCC-2
USB1-
USB1+
GND-1
GND-2
MINIDIN_USBX2-RH-8

5V_RUSB_1
C69 1u6.3X4
C68 0.1u/16X4
EC4 560u6.3V
R65 10K1%4
PORT7.8
[14] OC#1
R64 15K1%4

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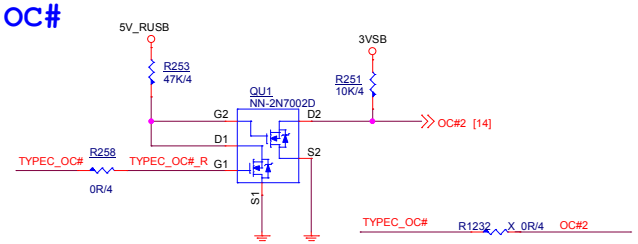
VBUS OC#



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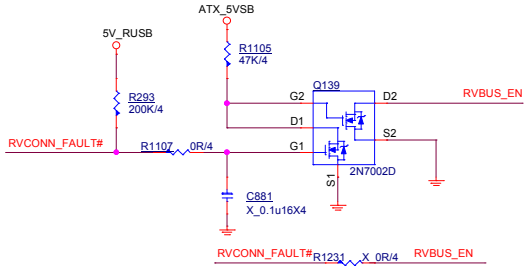
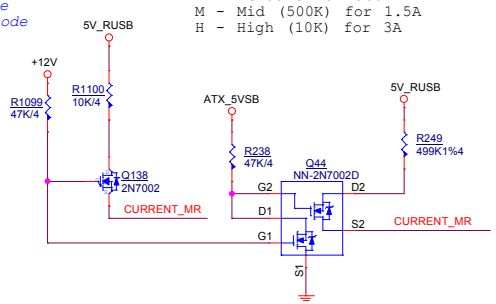
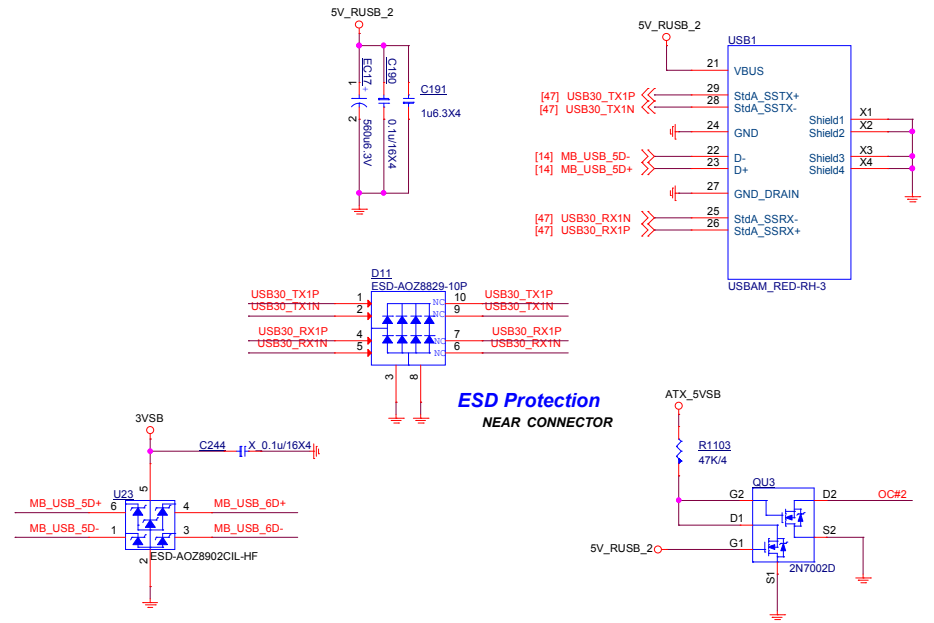


Current Mode

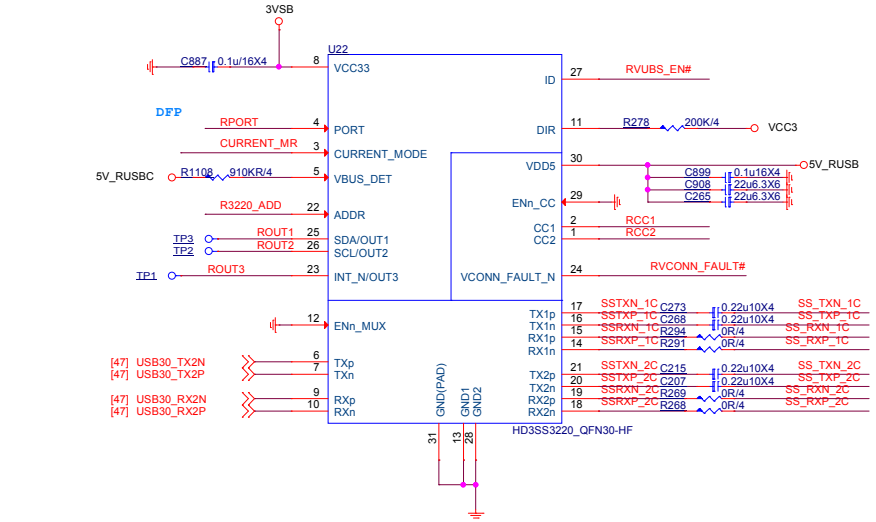
3A under S0 mode
1.5A under S3 mode

L - Default for 900mA
M - Mid (500K) for 1.5A
H - High (10K) for 3A

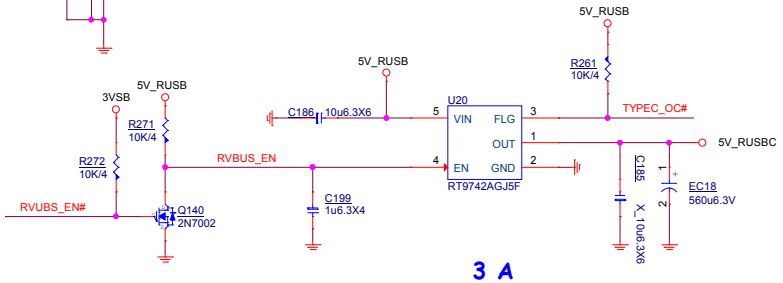




USB Type-C MUX with Configuration Channel (CC)



R3220_ ADD	High	Low	NC
RPORT	0x67	0x47	GPIO mode(V)
	DFP(V)	UFP	DRP

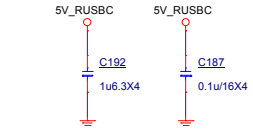


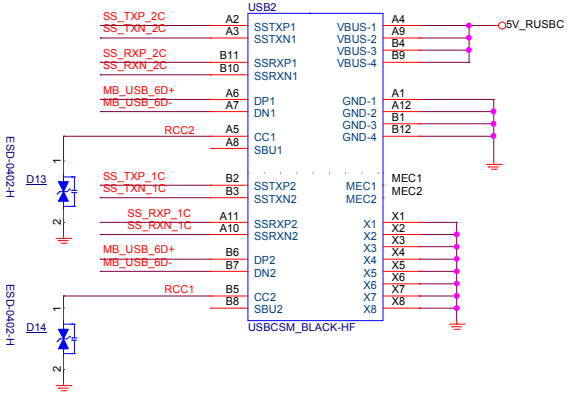
3 A
min 80mil.

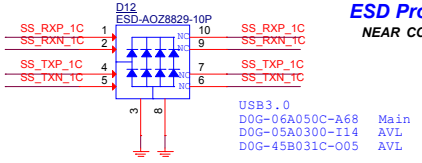
TYPE-C

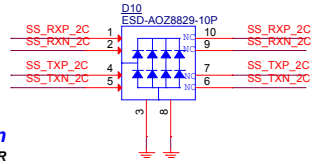
[14] MB_USB_6D+
[14] MB_USB_6D-

close to Type C Connector









ESD Protection
NEAR CONNECTOR

USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-005 AVL

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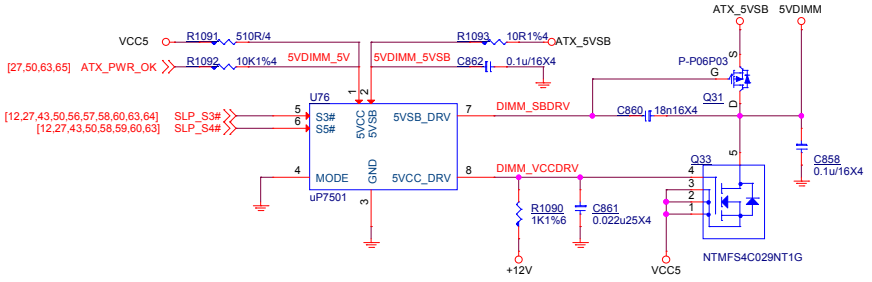
5VDIMM FOR DDR

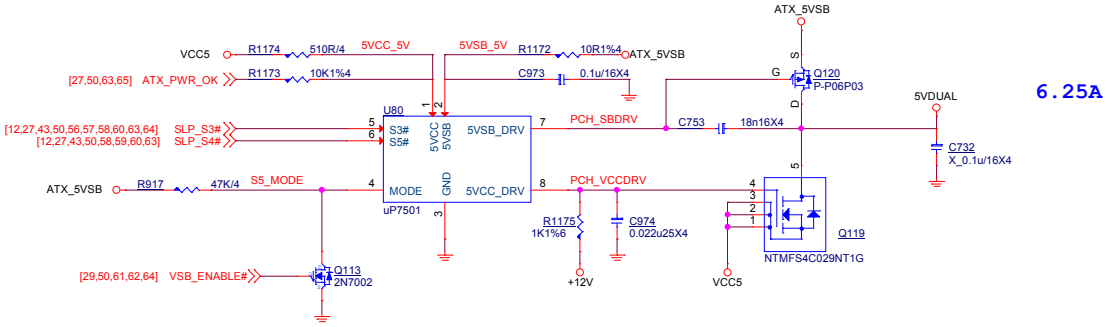
4.8A



7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

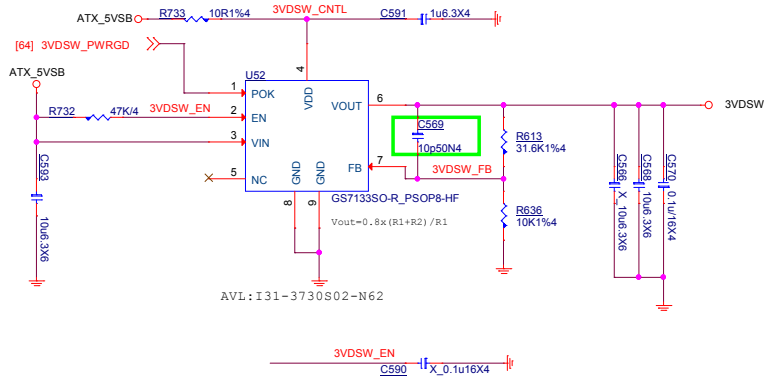
5VDUAL

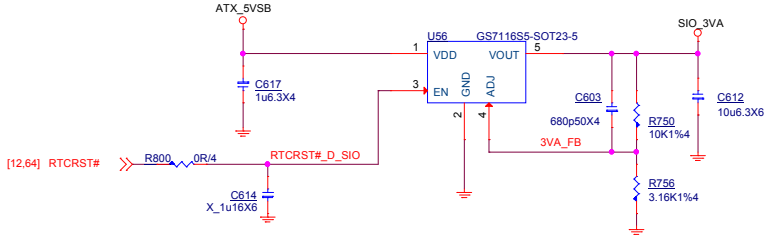
6.25A



3VDSW

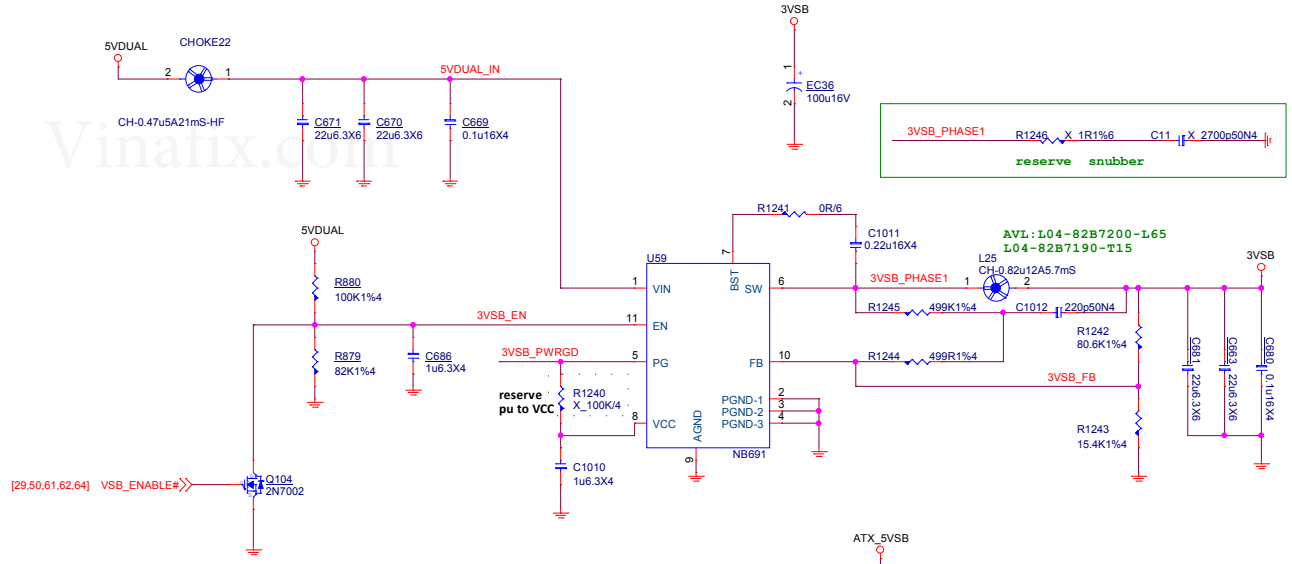
0.512A

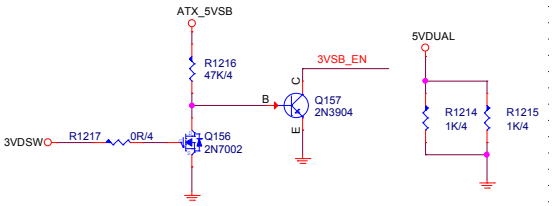


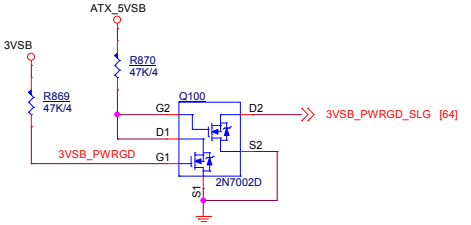


3VSB cost down

4.7A







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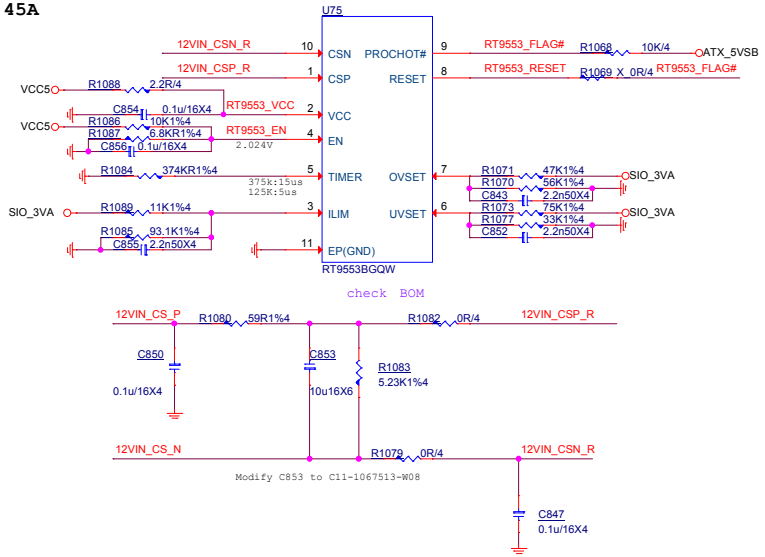
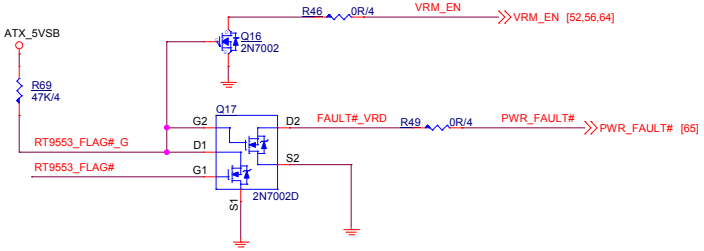
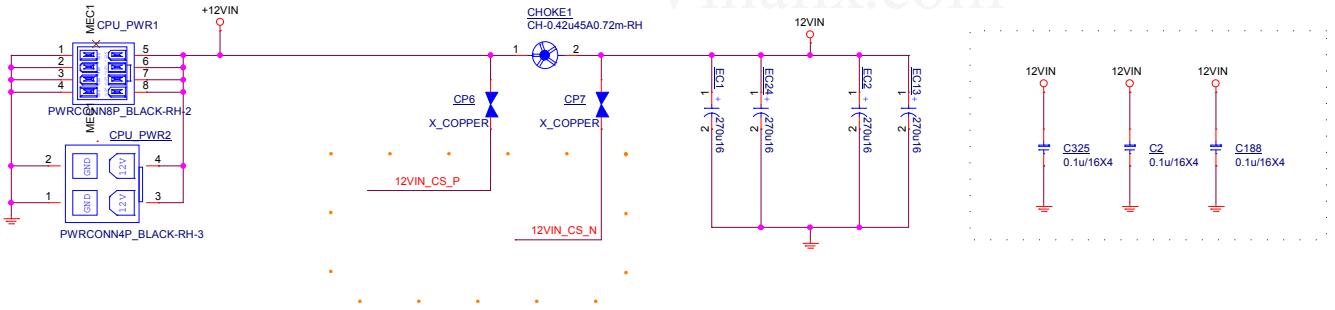
OCP:45A
Real OCP:45A





OCP:45A
Real OCP:45A
R17+R18>100k Vsio_3va= 3.38V Rdcr= 0.5 mohm

I3933_imon*[R17*R18/(R17+R18)]= Istep* Rdcr*100
I3933_imon= 10uA/step
Istep=4.968A



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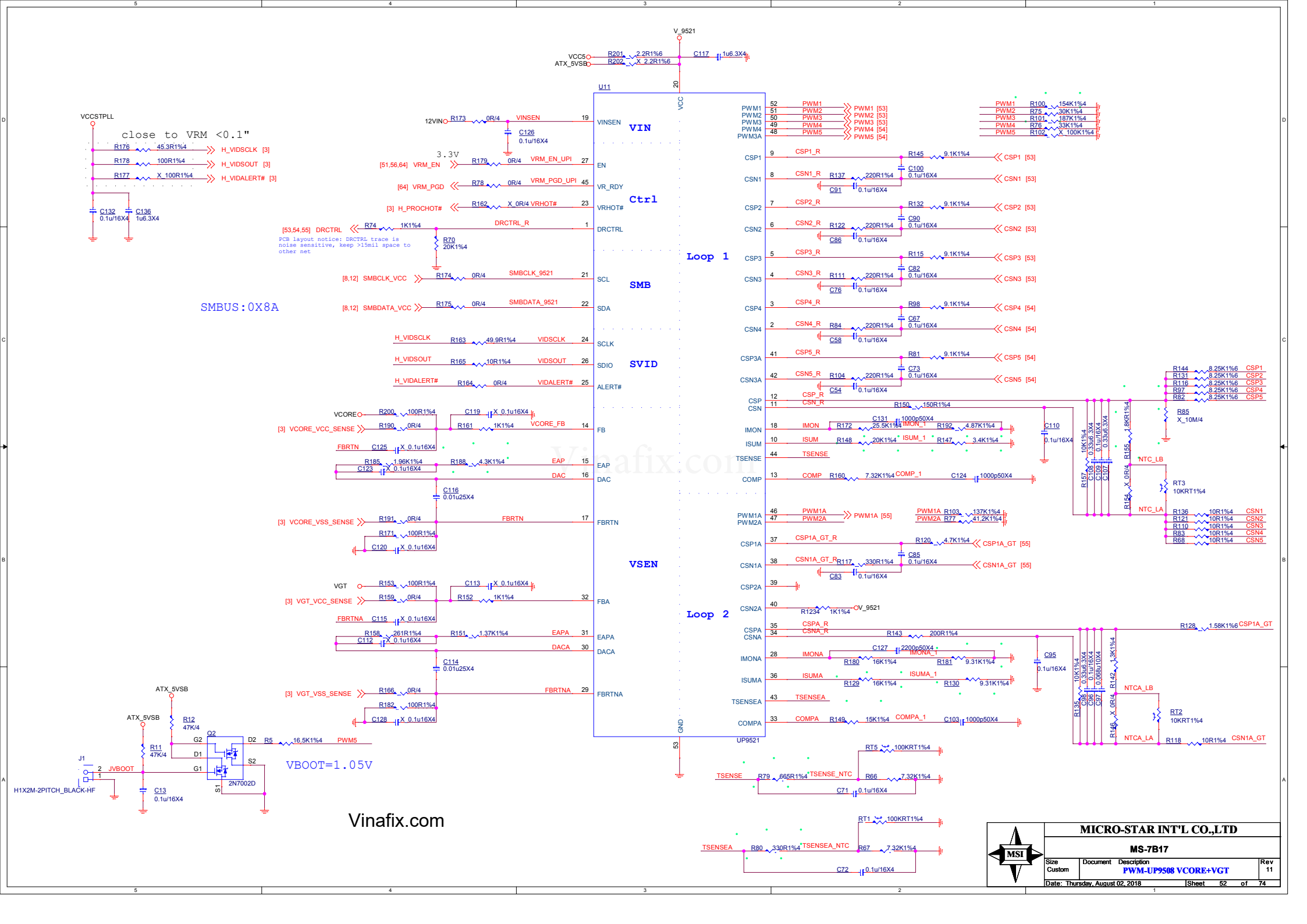
U11
UP9521
VIN
Ctrl
SMB
SVID
VSEN
Loop 1
Loop 2
VINSEN
EN
VR_RDY
VRHOT#
DRCTRL
SCL
SDA
SCLK
SDIO
ALERT#
FB
FBRTN
EAP
DAC
FBA
EAPA
DACA
FBRTNA
IMON
ISUM
TSENSE
COMP
IMONA
ISUMA
TSENSEA
COMPA
CSP1
CSN1
CSP2
CSN2
CSP3
CSN3
CSP4
CSN4
CSP5
CSN5
CSP3A
CSN3A
CSPA
CSNA
CSP1A
CSN1A
CSP2A
CSN2A
PWM1
PWM2
PWM3
PWM4
PWM5
PWM1A
PWM2A
PWM3A
VCC
GND
close to VRM <0.1"
SMBUS:0X8A
VBOOT=1.05V
PCB layout notice: DRCTRL trace is noise sensitive, keep >15mil space to other net
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PWM-UP9508 VCORE+VGT
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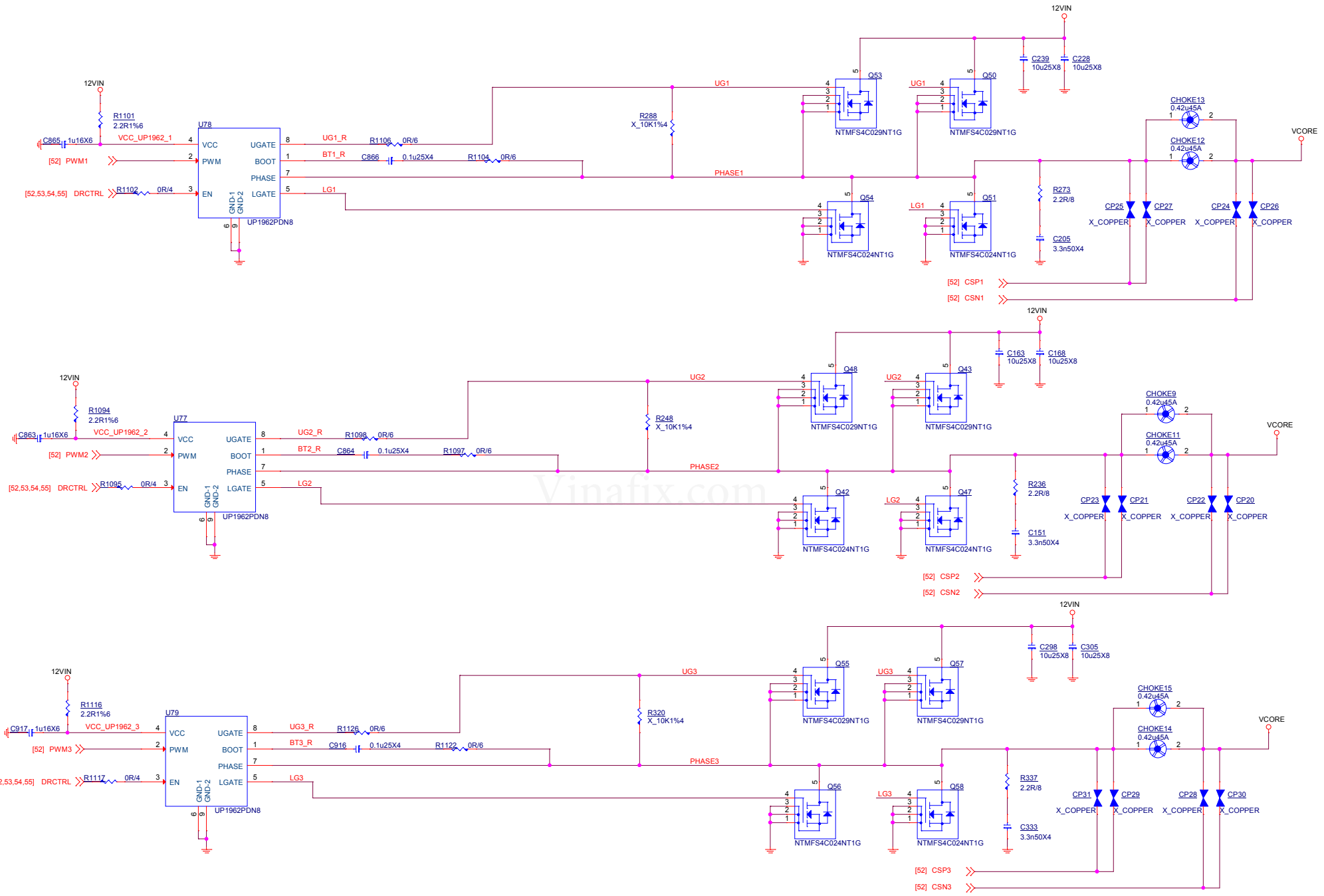
Vinafix.com



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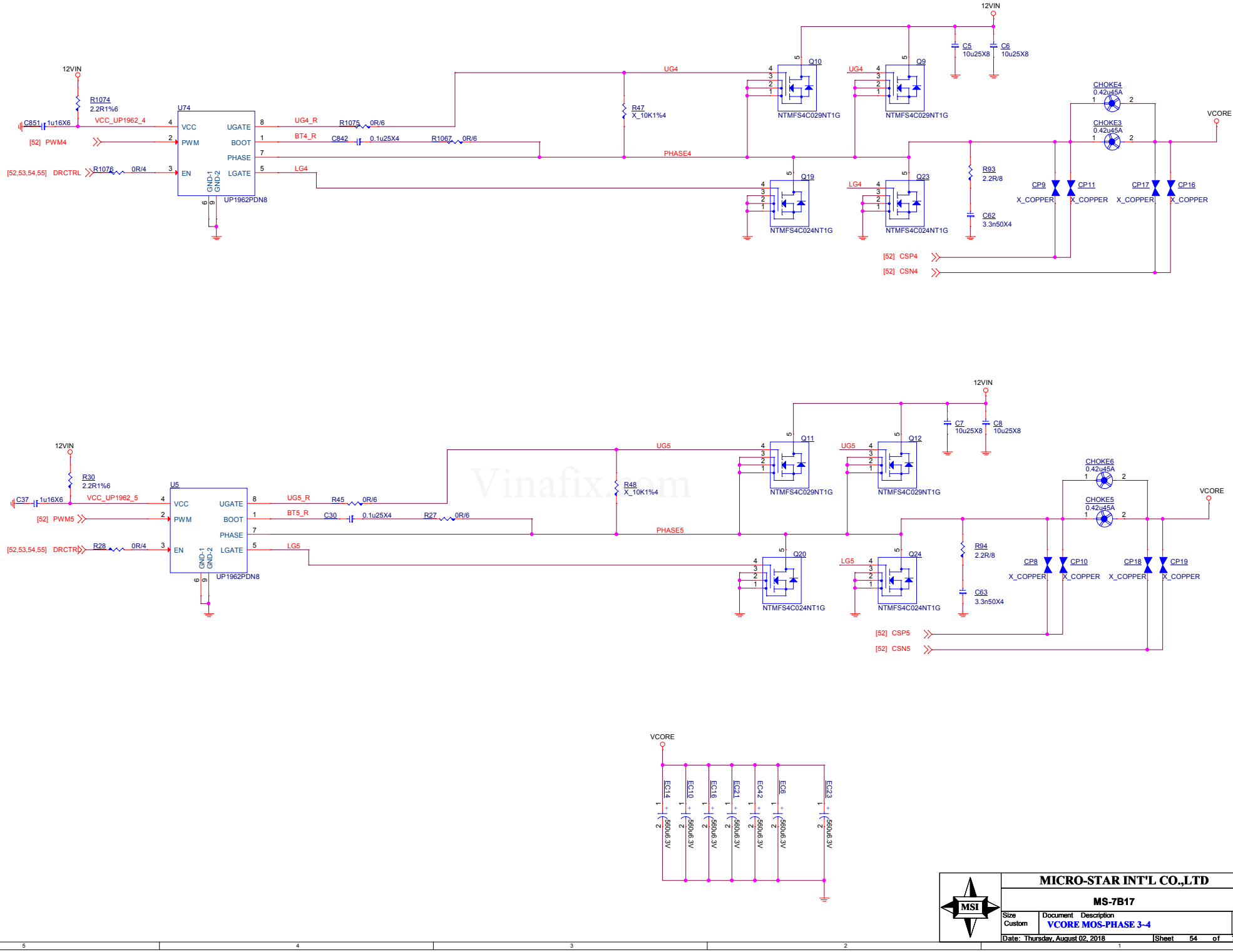
12VIN
R1074
2.2R1%6
C851
1u16X6
VCC_UP1962_4
[52] PWM4
[52,53,54,55] DRCTRL
R1076
0R/4
U74
VCC
PWM
EN
UGATE
BOOT
PHASE
LGATE
GND-1
GND-2
UP1962PDN8
UG4_R
R1075
0R/6
BT4_R
C842
0.1u25X4
R1067
0R/6
LG4
UG4
R47
X_10K1%4
PHASE4
Q10
Q9
NTMFS4C029NT1G
Q19
Q23
NTMFS4C024NT1G
C5
10u25X8
C6
10u25X8
CHOKE4
0.42u45A
CHOKE3
0.42u45A
VCORE
R93
2.2R/8
C62
3.3n50X4
CP9
CP11
CP17
CP16
X_COPPER
[52] CSP4
[52] CSN4
12VIN
R30
2.2R1%6
C37
1u16X6
VCC_UP1962_5
[52] PWM5
[52,53,54,55] DRCTRL
R28
0R/4
U5
VCC
PWM
EN
UGATE
BOOT
PHASE
LGATE
GND-1
GND-2
UP1962PDN8
UG5_R
R45
0R/6
BT5_R
C30
0.1u25X4
R27
0R/6
LG5
UG5
R48
X_10K1%4
PHASE5
Q11
Q12
NTMFS4C029NT1G
Q20
Q24
NTMFS4C024NT1G
C7
10u25X8
C8
10u25X8
CHOKE6
0.42u45A
CHOKE5
0.42u45A
VCORE
R94
2.2R/8
C63
3.3n50X4
CP8
CP10
CP18
CP19
X_COPPER
[52] CSP5
[52] CSN5
VCORE
EC14
EC10
EC16
EC21
EC42
EC8
EC23
560u6.3V
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Custom
Document Description
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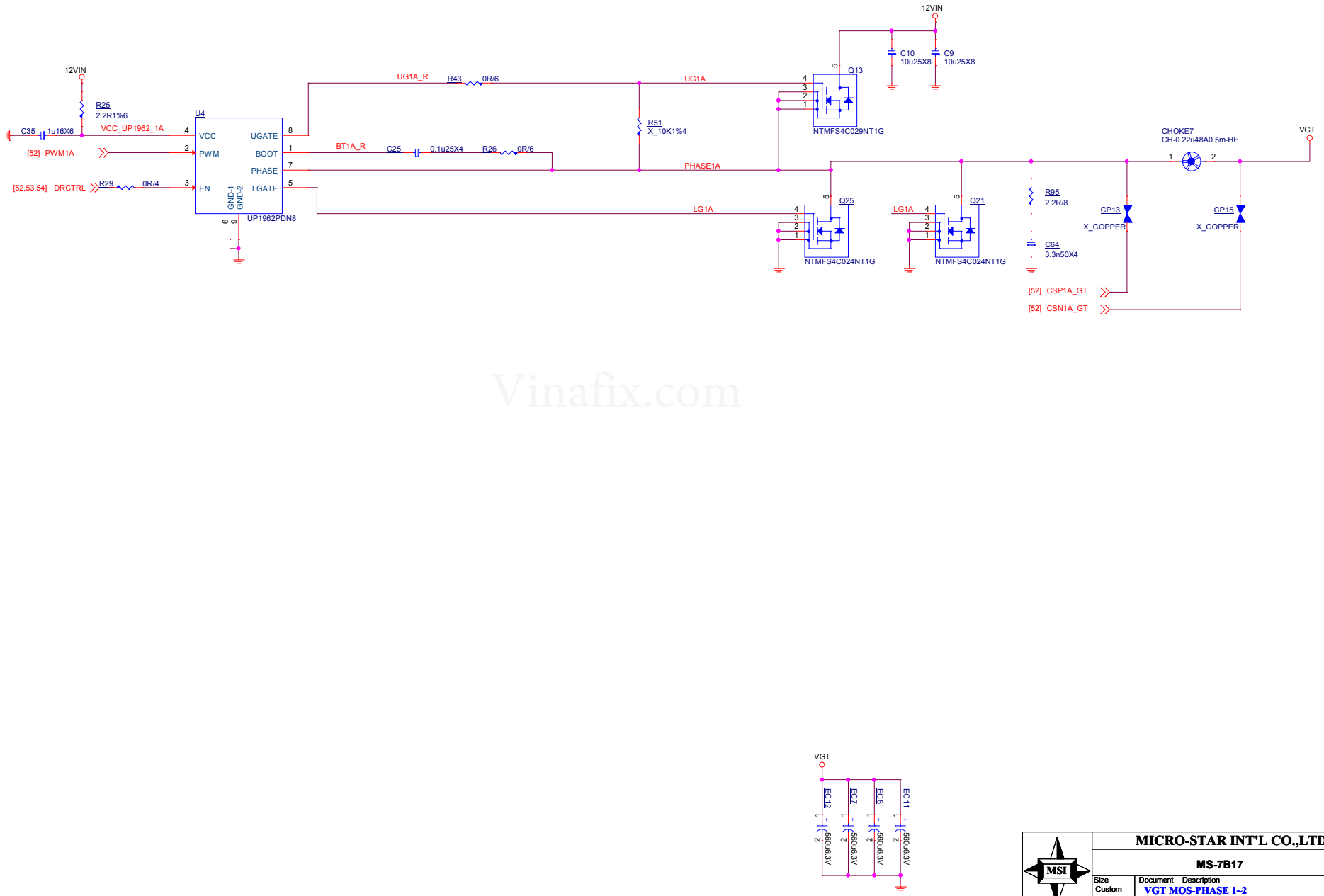
12VIN
R25
2.2R1%6
C35
1u16X6
VCC_UP1962_1A
[52] PWM1A
[52,53,54] DRCTRL
R29
0R/4
U4
VCC
PWM
EN
UGATE
BOOT
PHASE
LGATE
GND-1
GND-2
UP1962PDN8
UG1A_R
R43
0R/6
BT1A_R
C25
0.1u25X4
R26
0R/6
R51
X_10K1%4
UG1A
PHASE1A
LG1A
Q13
NTMFS4C029NT1G
Q25
NTMFS4C024NT1G
Q21
NTMFS4C024NT1G
C10
10u25X8
C9
10u25X8
CHOKE7
CH-0.22u48A0.5m-HF
VGT
R95
2.2R/8
C64
3.3n50X4
CP13
X_COPPER
CP15
X_COPPER
[52] CSP1A_GT
[52] CSN1A_GT
EC12
EC7
EC8
EC11
560u6.3V
Vinafix.com
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Custom
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VGT MOS-PHASE 1~2
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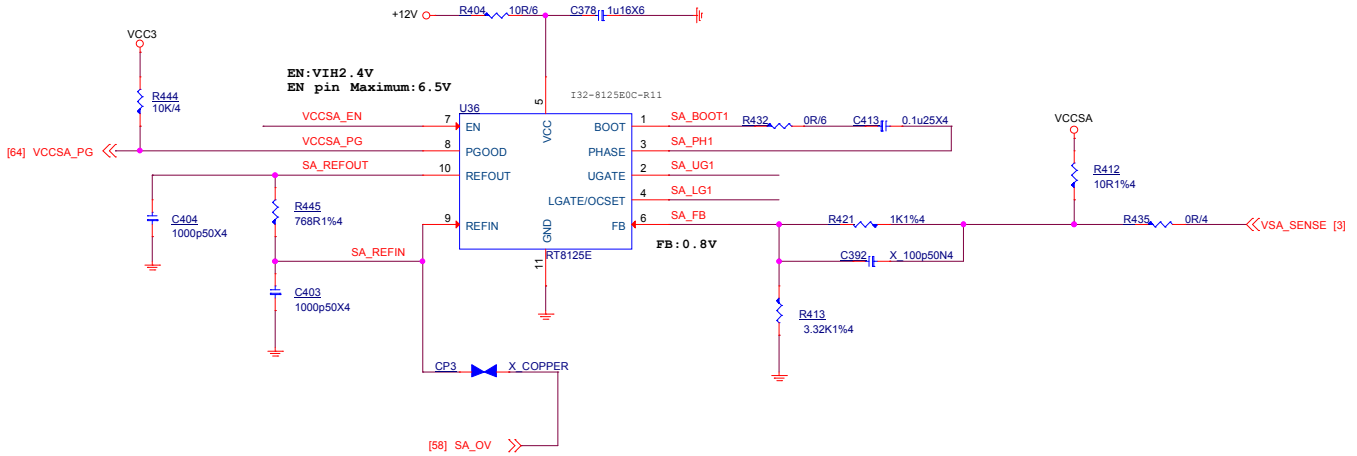
SA Power:1.05V,11.1A

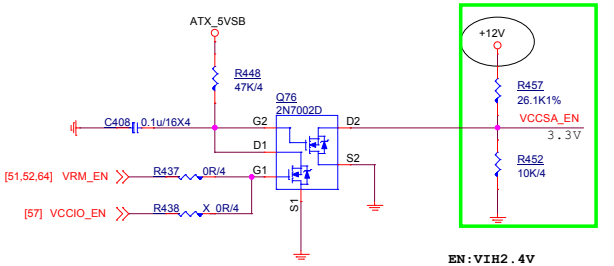
OCP:18A

Rocset = 1.3 * Imax * Rdson(low) / Iocset
= 18.2* 2.8mohm / 10uA
= 5.1K

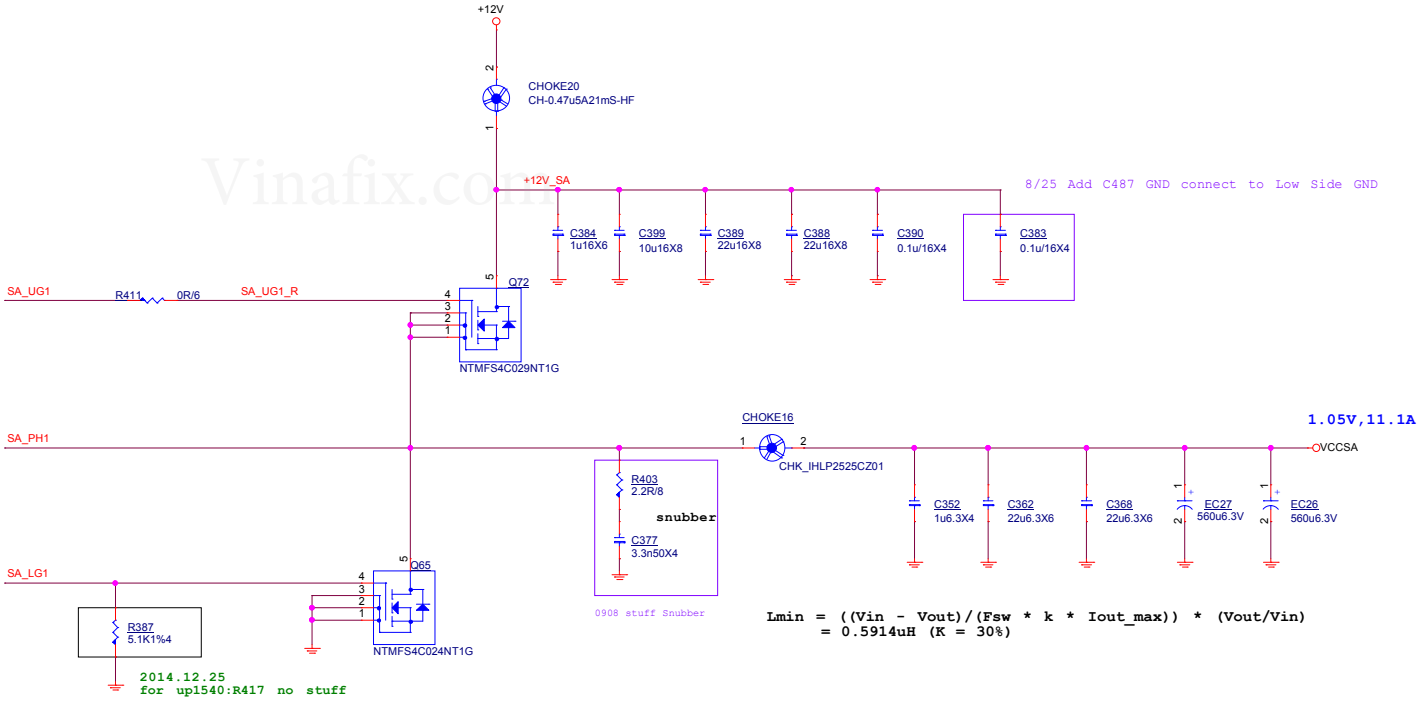
Rdson(low)10V

MOS :2.8mohm

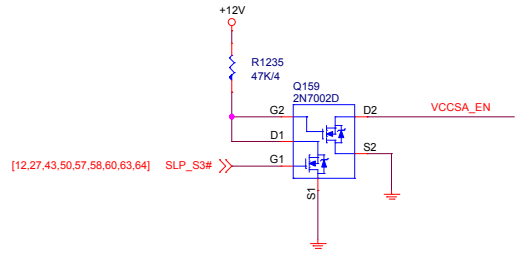




EN:VIH2.4V
EN pin Maximum:6.5V



Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)



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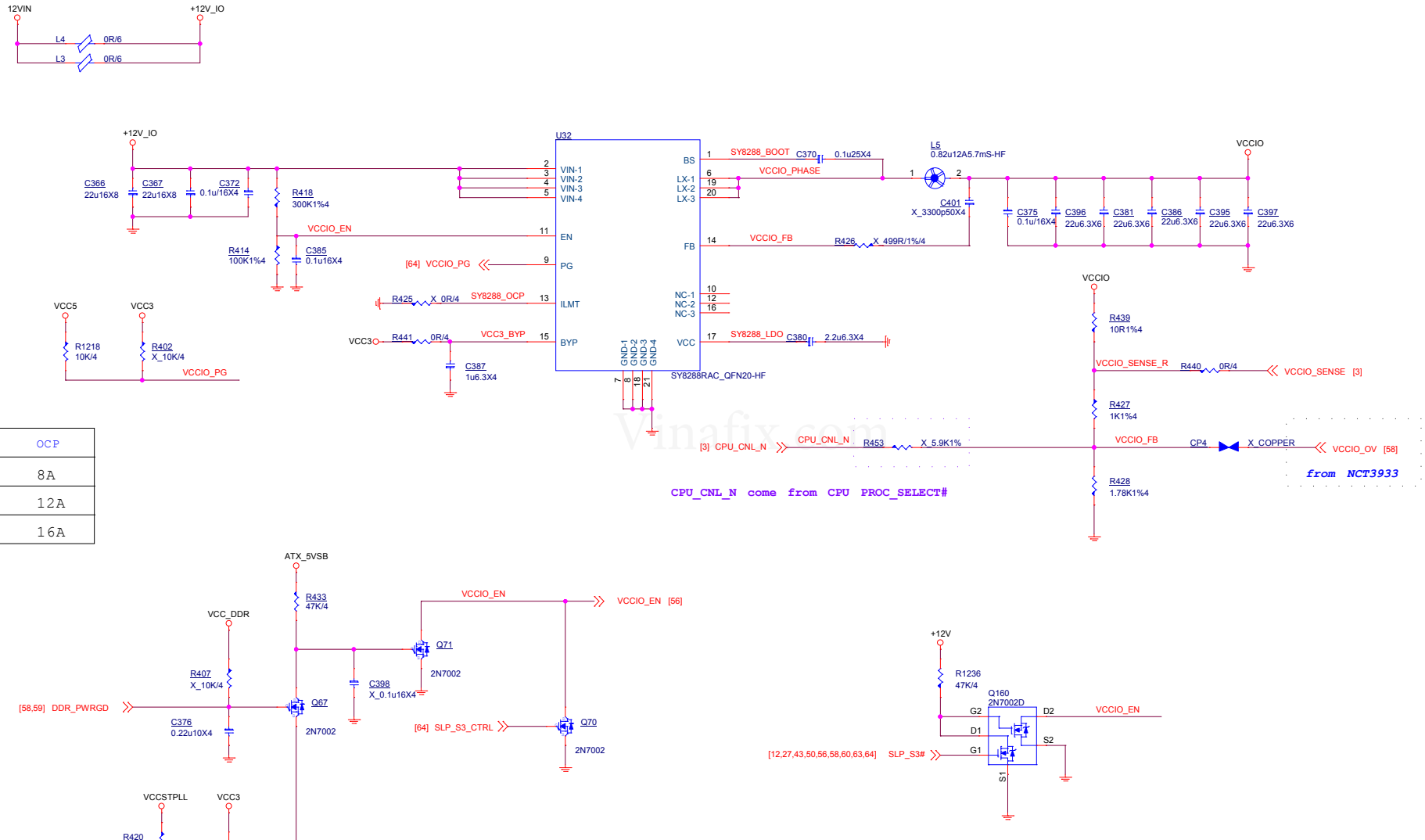
IO Power:0.95V,6.4A

OCP:12A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

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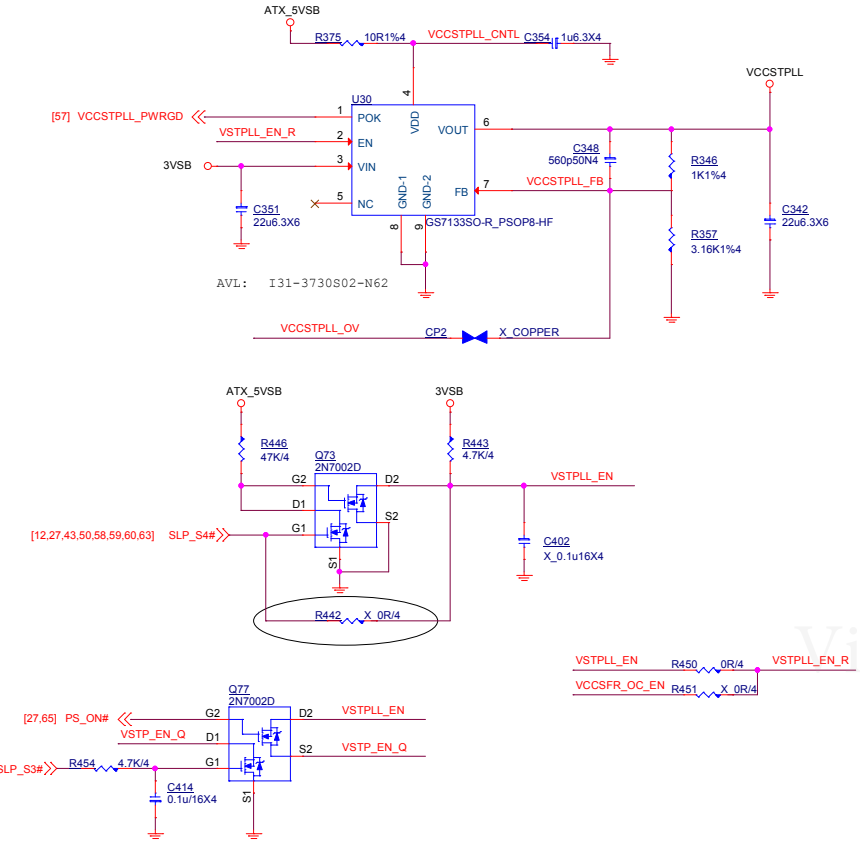
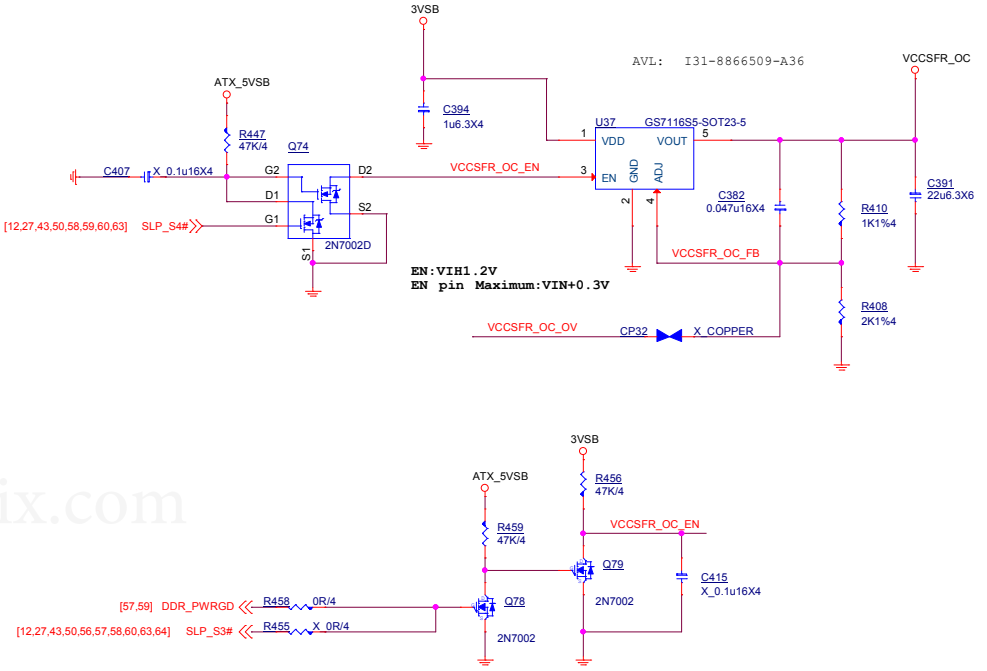
VCCSTPLL

1.05V; 230mA



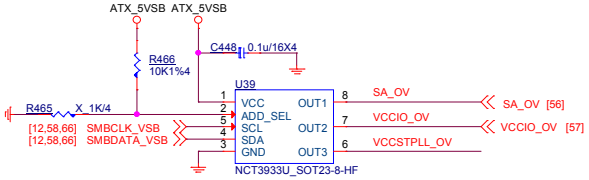
VCCPLL_OC

1.2V; 130mA

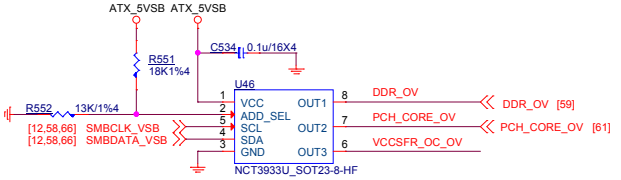


VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN



0x26:RH=18K,RL=13K



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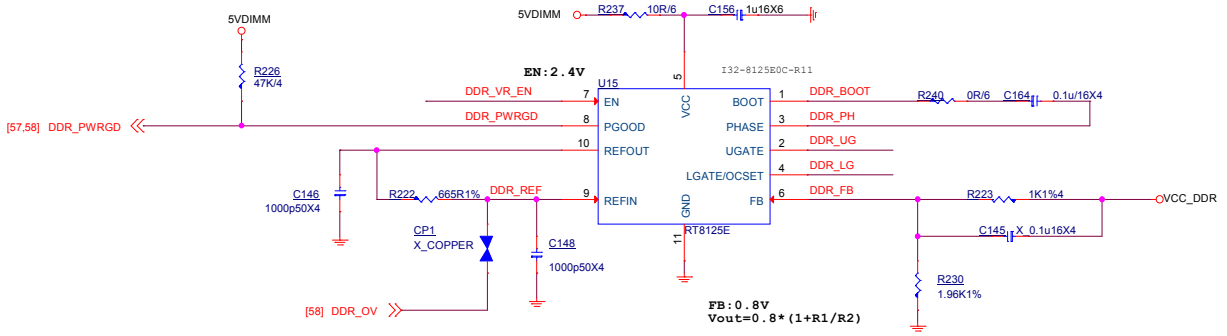
DDR4 Power:1.2V,19.8A *OCP:28A*

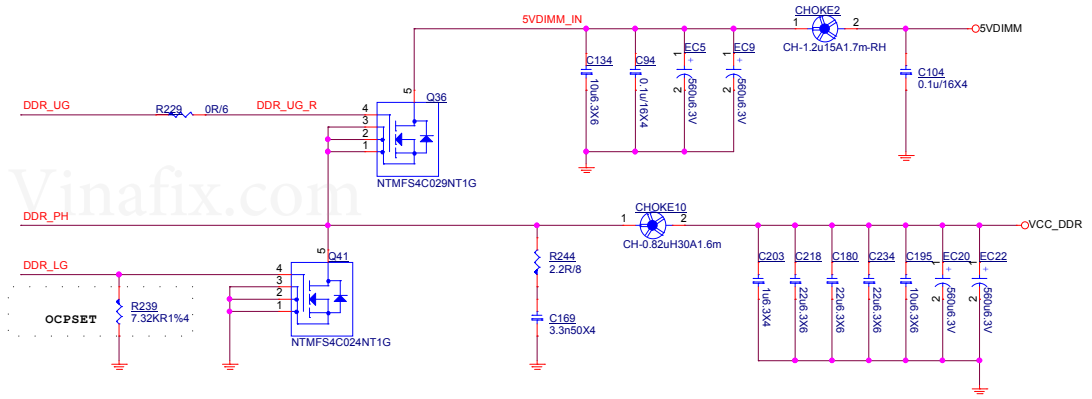
3.3A FOR CPU

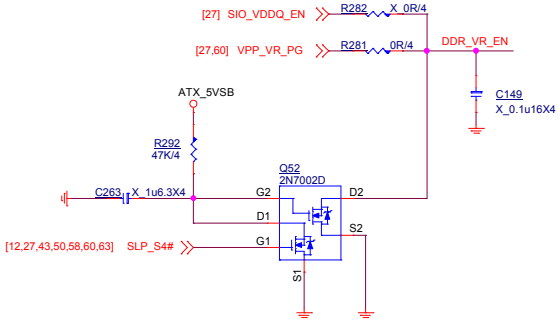
15.7A FOR 4DIMM

0.7A FOR DDR VTT

```
Rocset = 1.3 * Imax * Rdson(low) / Iocset
       = 26* 4mohm / 10uA
       = 10.3K
```







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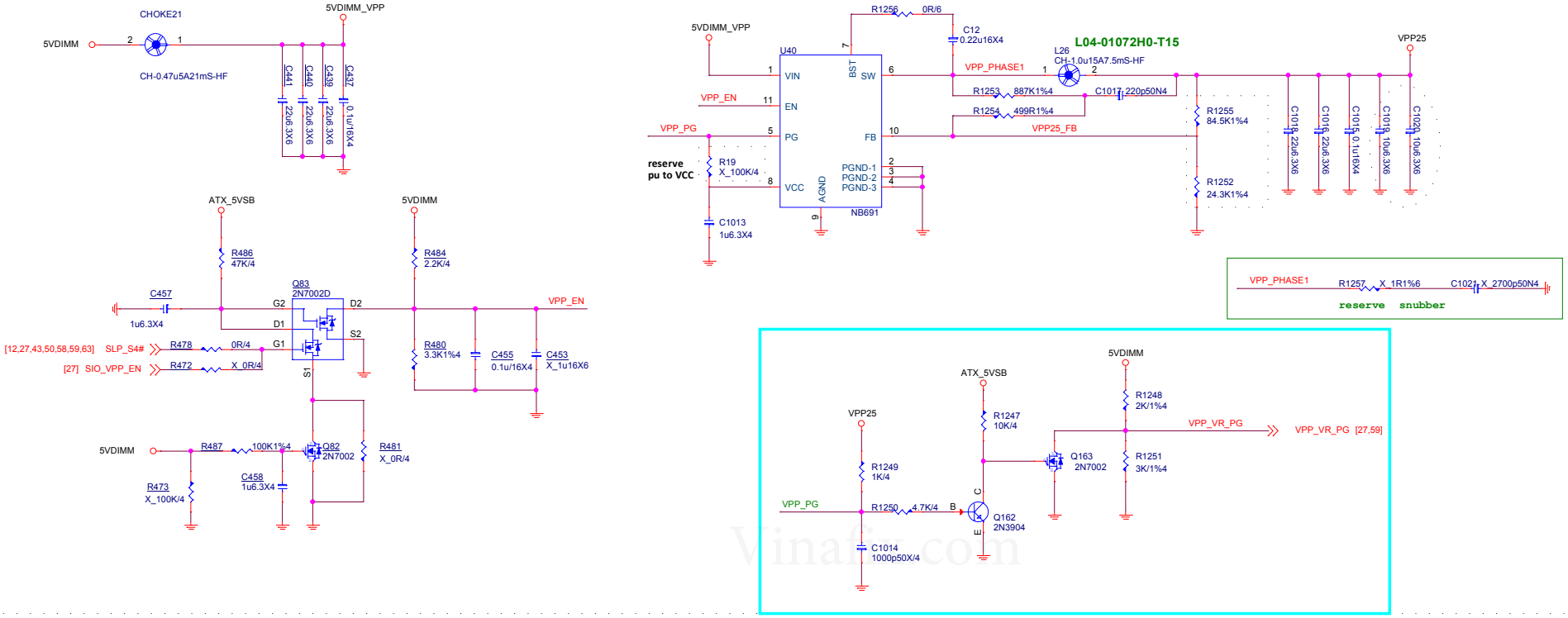
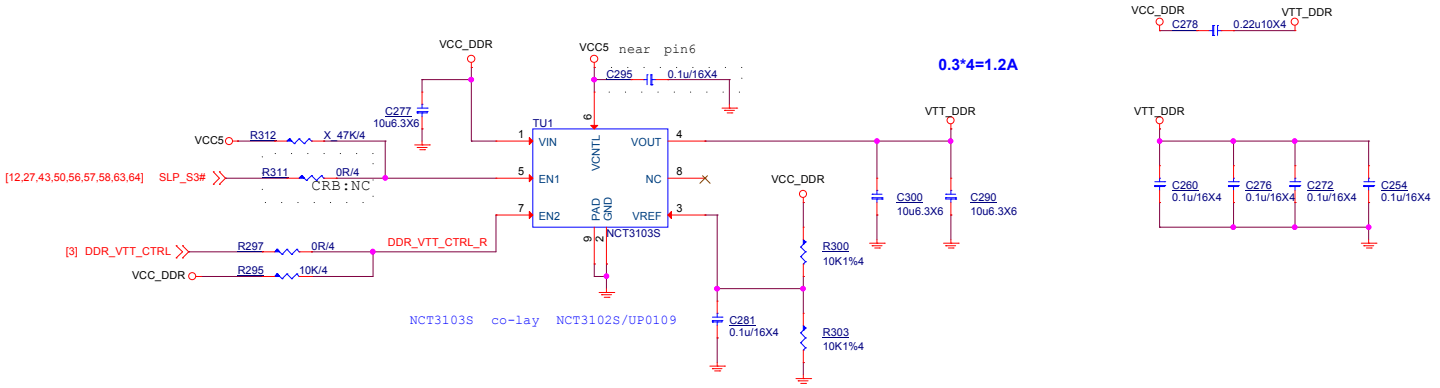
VPP2.5V Power:2.5V,6A

OCP:7.5A



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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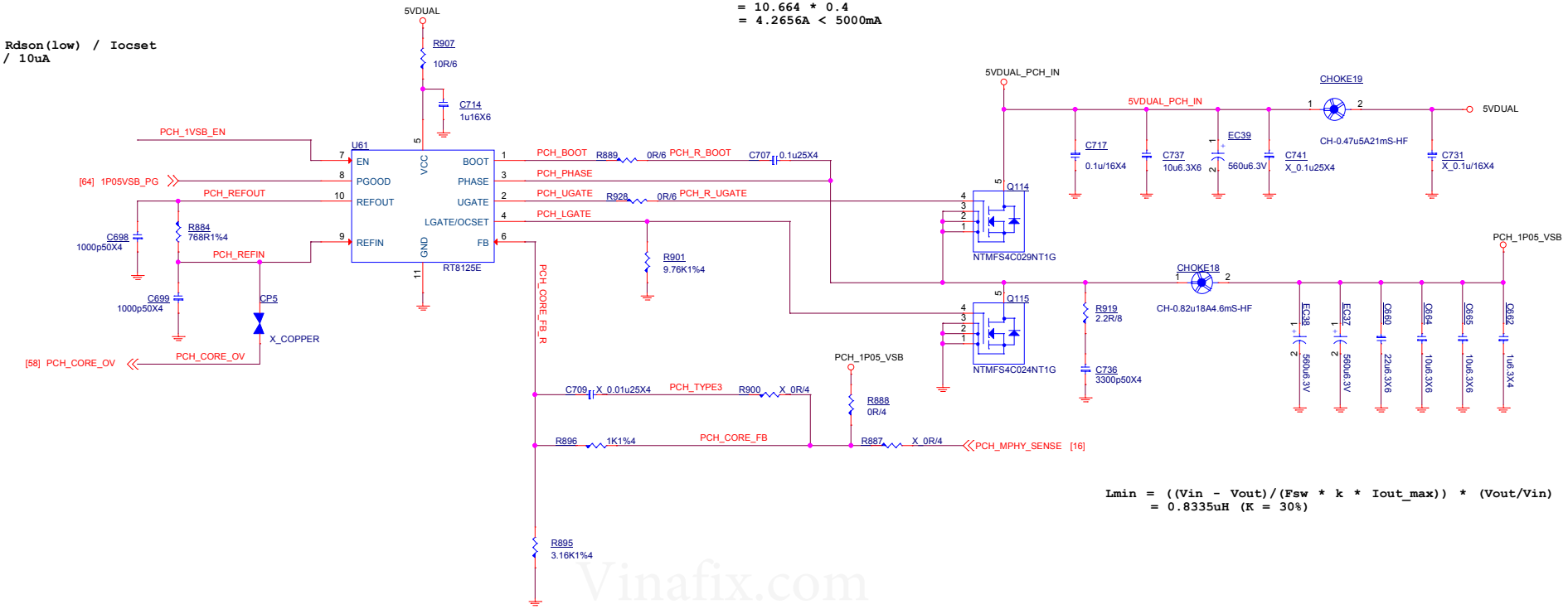
PCH_1VSB Power:1.05V,14A

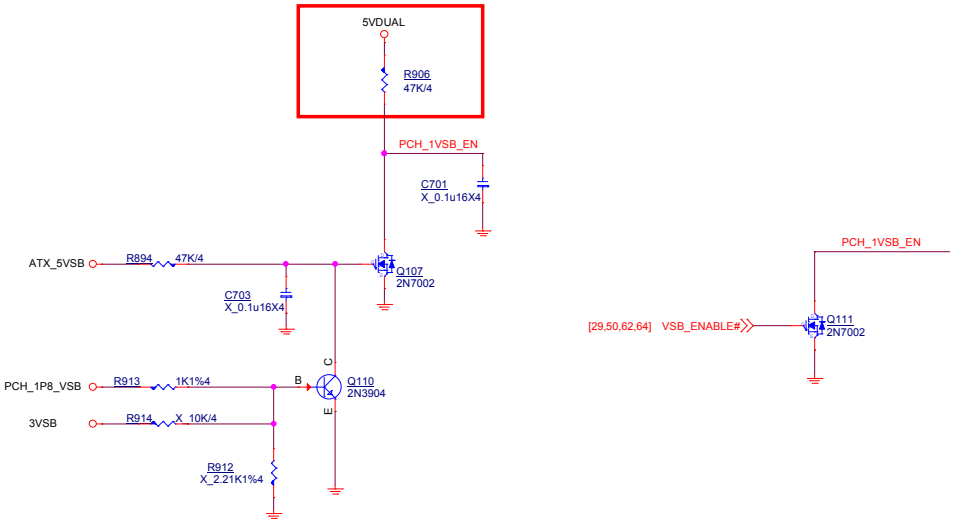
OCP = 18.2A

```
Rocset = 1.3 * Imax * Rdson(low) / Iocset
       = 18.2 * 4mohm / 10uA
       = 7.28K
```

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
     = 10.664 * 0.4
     = 4.2656A < 5000mA
```




```
Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
     = 0.8335uH (K = 30%)
```



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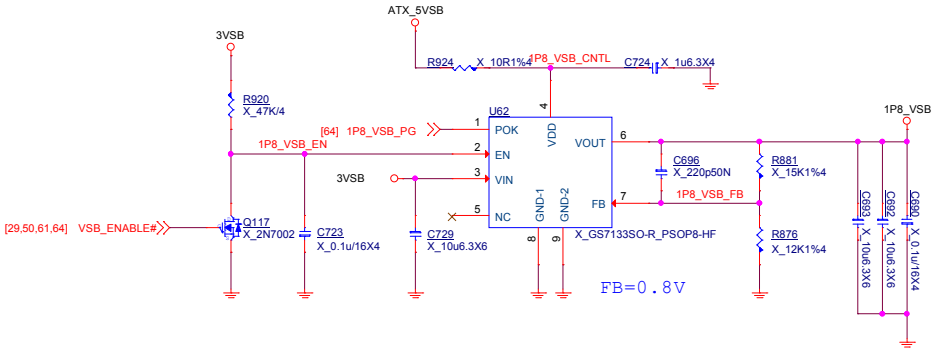

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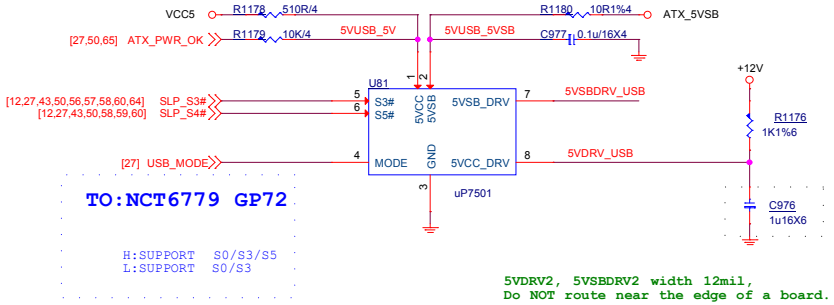
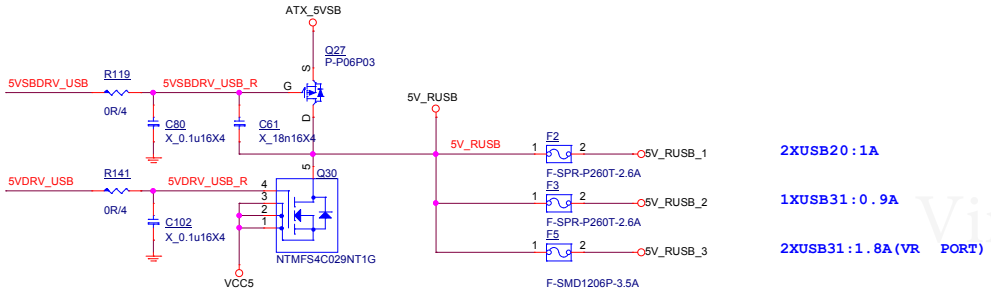
USB POWER



REAR USB PORT POWER

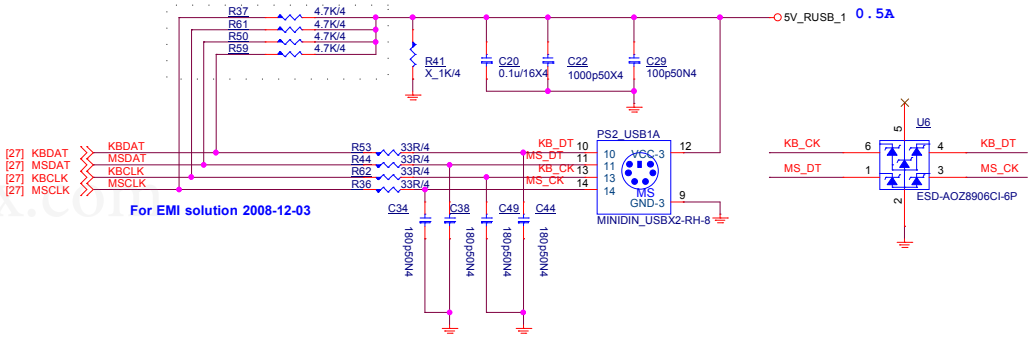


2XUSB20:1A

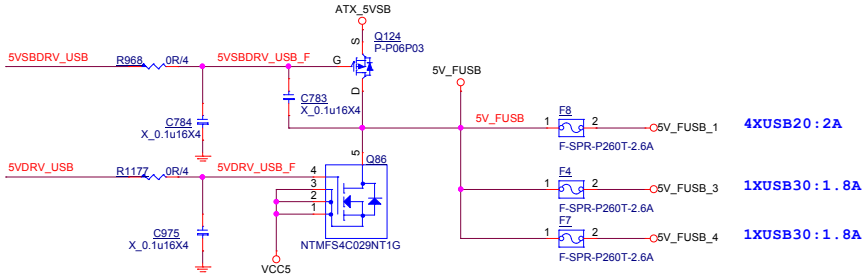
1XUSB31:0.9A

2XUSB31:1.8A(VR PORT)

PS2 KEYBOARD & MOUSE CONNECTOR



FRONT USB PORT POWER



4XUSB20:2A

1XUSB30:1.8A

1XUSB30:1.8A

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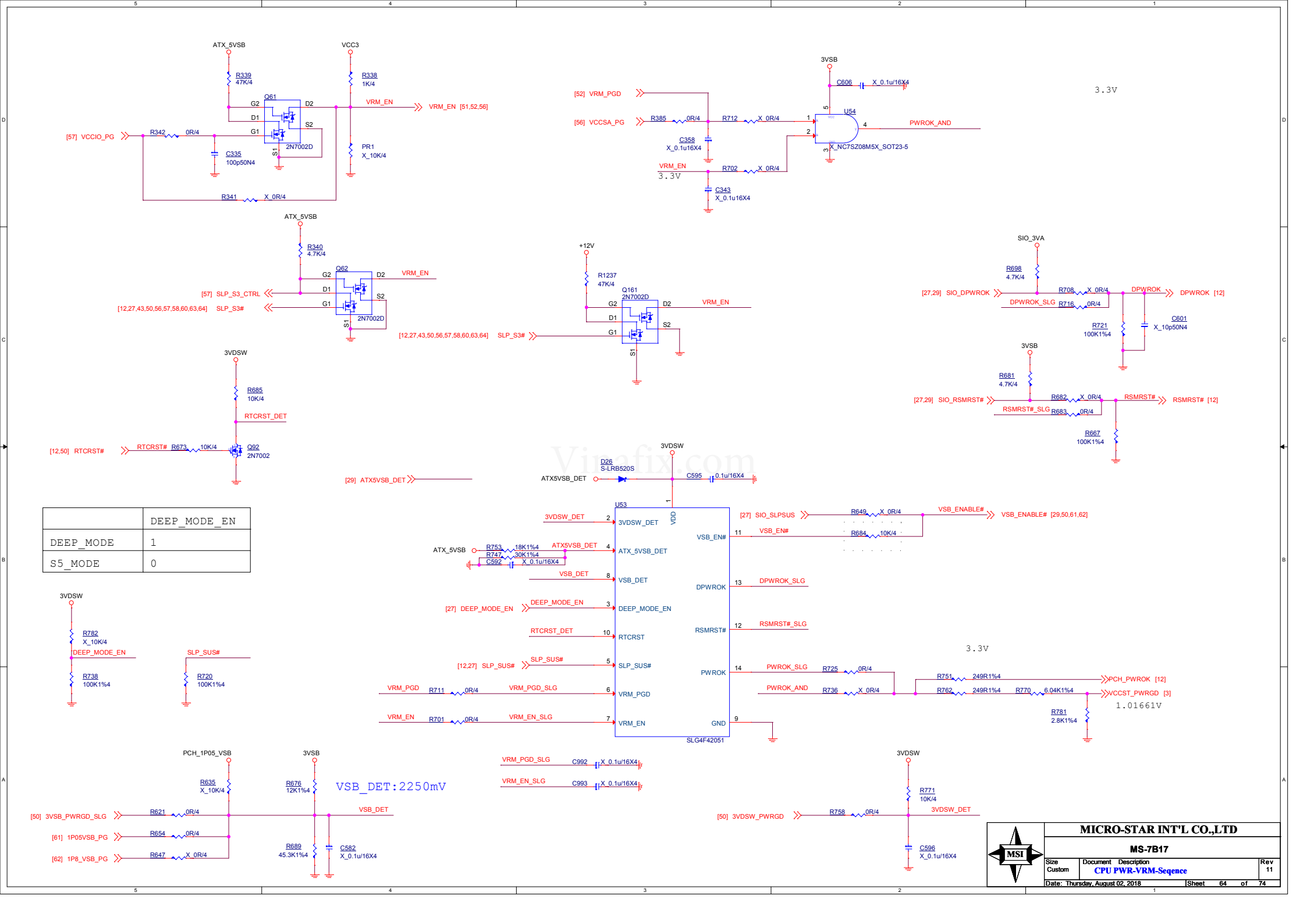

	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0

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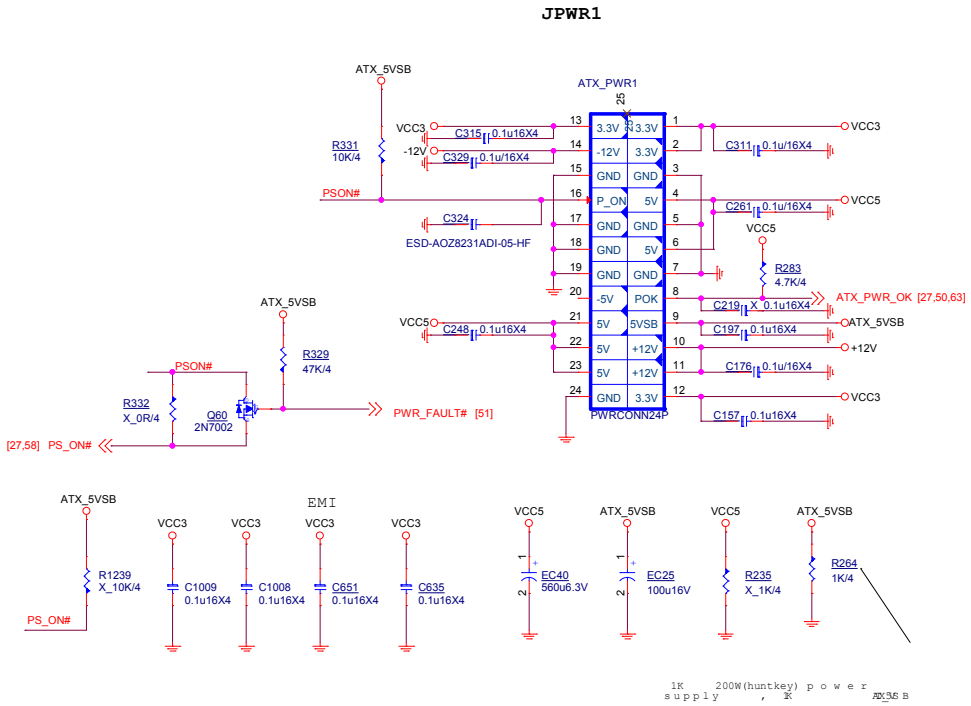
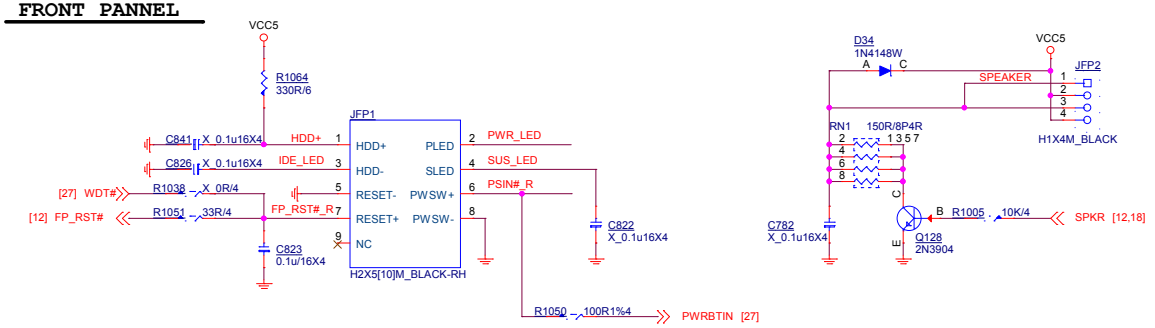
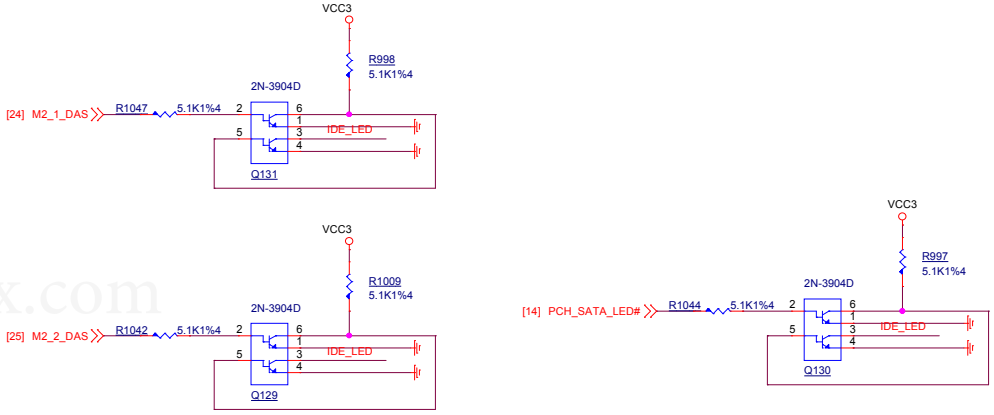
ATX POWER CONNECTOR

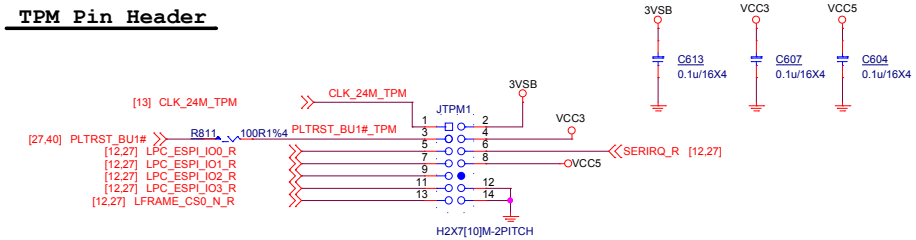


FRONT PANNEL

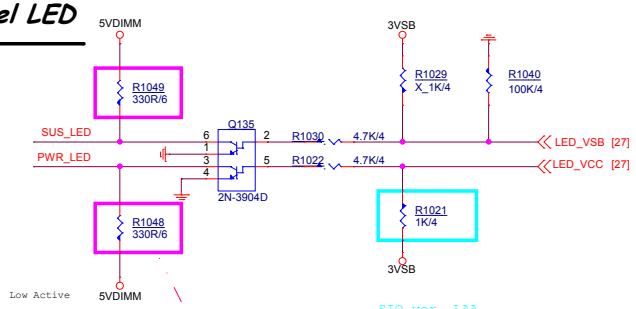




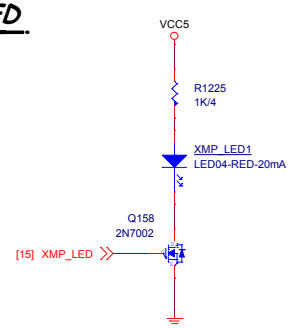
TPM Pin Header



Front Panel LED



XMP LED



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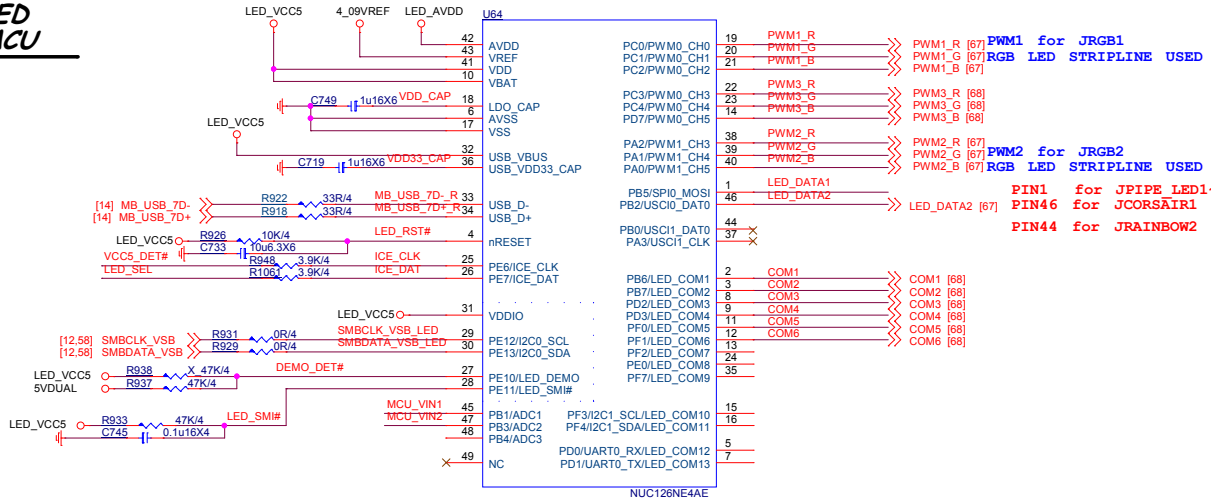
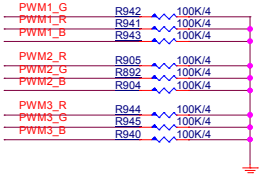
LED MCU

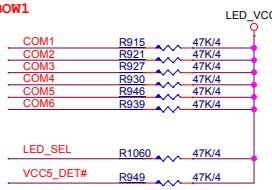


PWM1 for JRGB1
RGB LED STRIPLINE USED

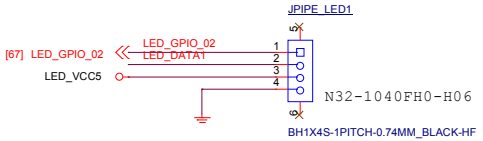
PWM2 for JRGB2
RGB LED STRIPLINE USED

PIN1 for JPIPE_LED1~3 and JRAINBOW1
PIN46 for JCORSAIR1
PIN44 for JRAINBOW2



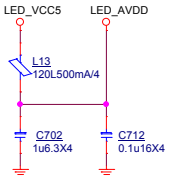


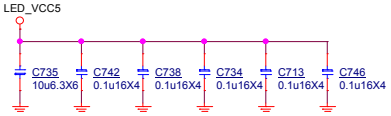
2 AUDIO/IO Cover LED
PCS LED*0.16W=W



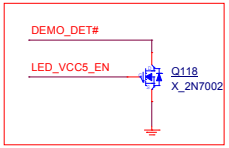
JPIPE:PIN1:output ,PIN2:input
PIN2:MCU IN
PIN1:HEATSINK OUT

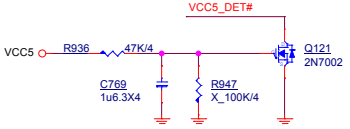
C1811 & C1812 near AVDD Pin.





C930 & C931 near VDD Pin.
C1829 & C1830 near VREF & VBAT Pin.
C1832 & C1832 near VDDIO & USB VBUS Pin.

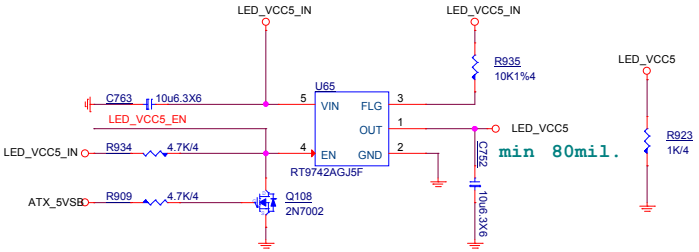




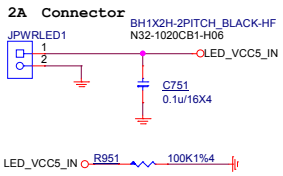
If SPEC hes LED demo function without demo button,
DEMO_DET# must pull up to LED_VCC5,Q319 need to stuff and control by LED_VCC5_EN.
PS. R2069 remove, R2032 and Q319 need to stuff

EXTERNAL POWER INPUT

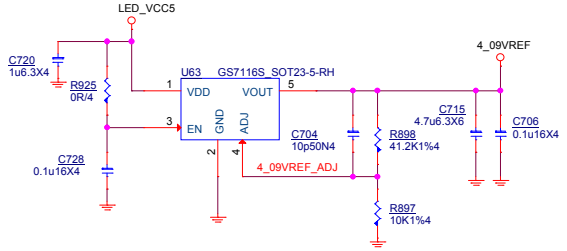
3 A

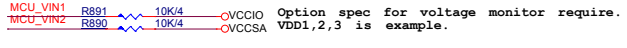


External Power

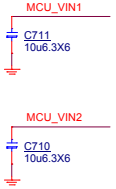


Voltage HW monitor





Option spec for voltage monitor require.
VDD1,2,3 is example.



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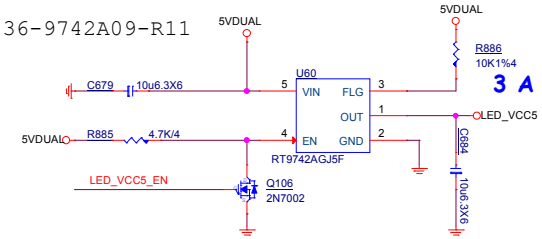
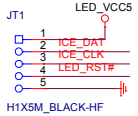


JT1 for FW update

For FW update.



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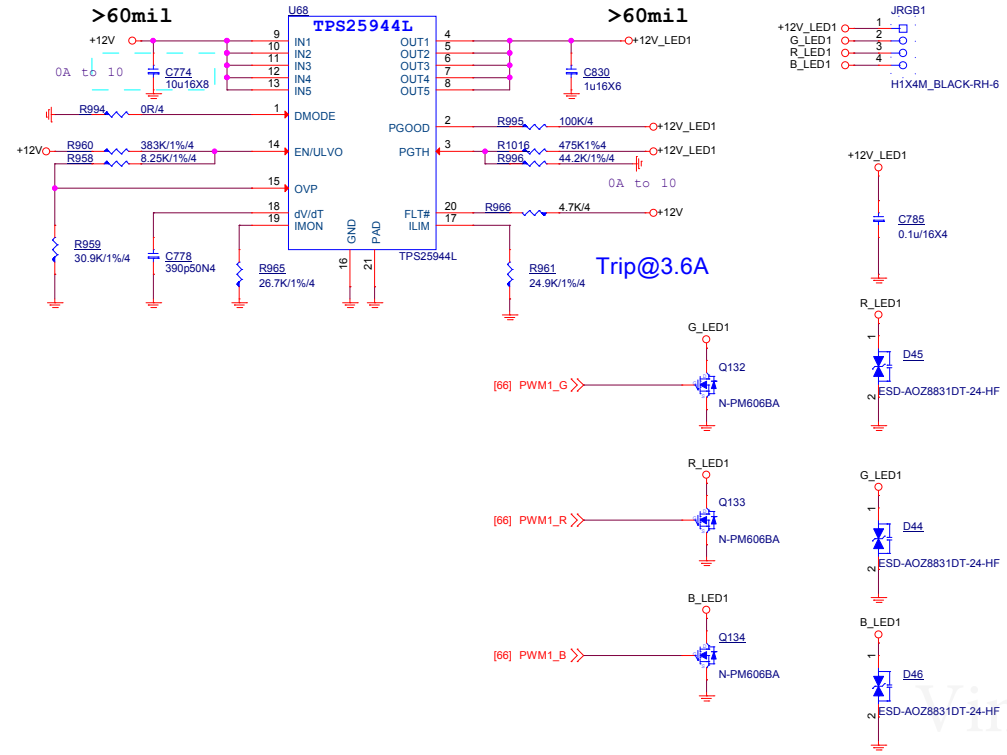
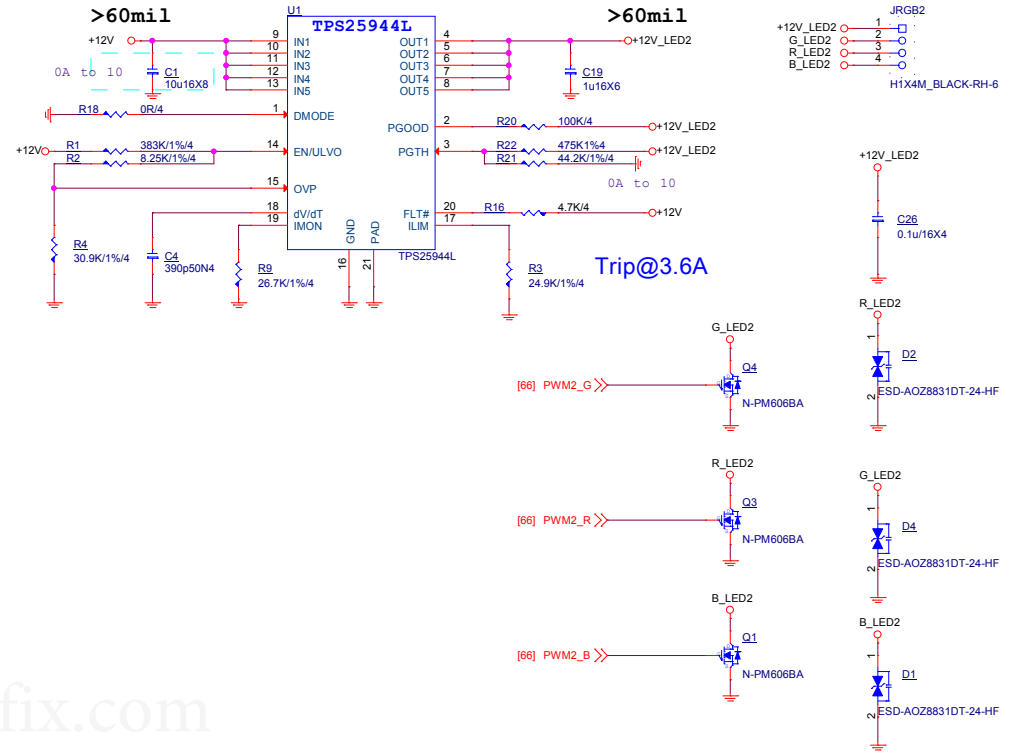
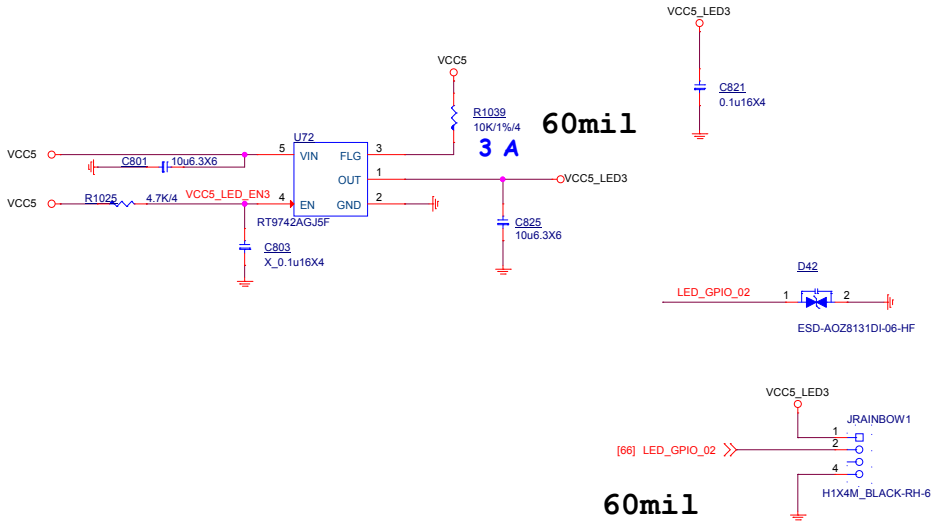
JRGB1



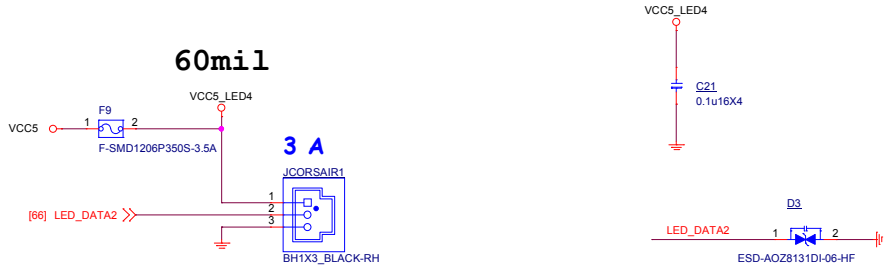
JRGB2



LED STRIPLINE JRAINBOW1



JCORSAIR1



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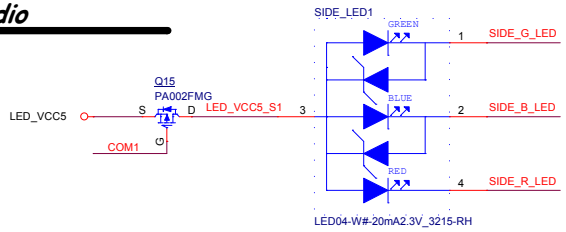
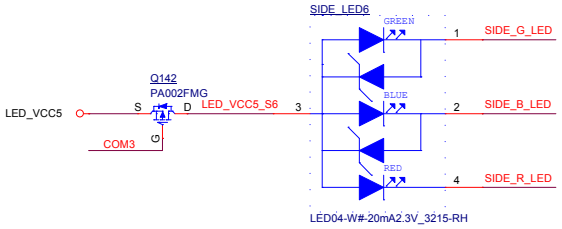
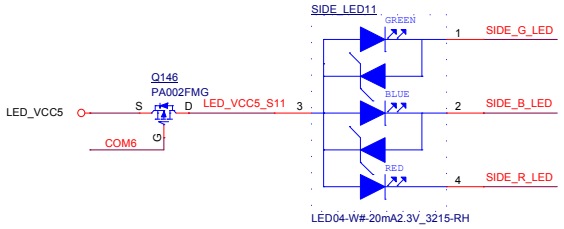
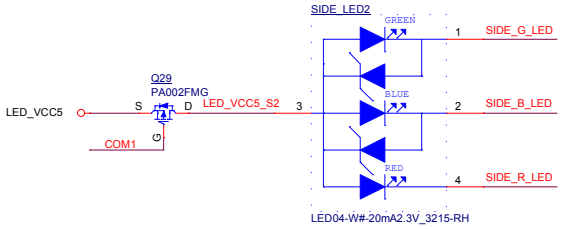
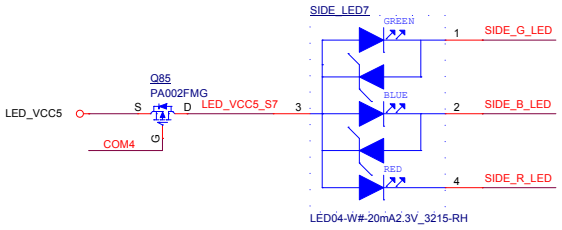
BOARD SIDE LED *8
for Audio

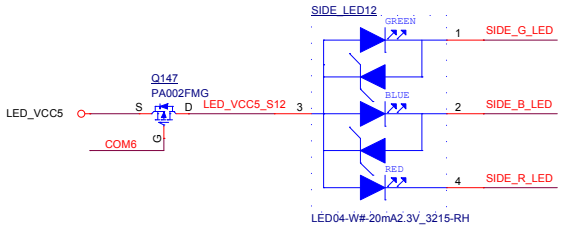


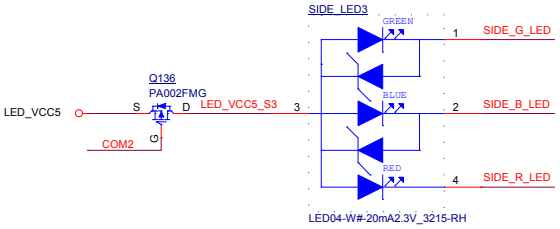


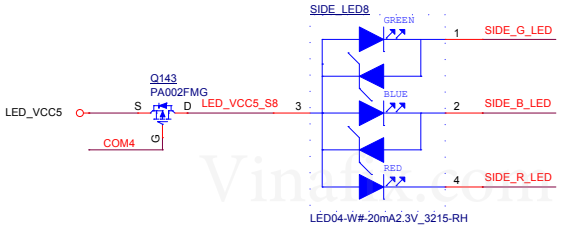


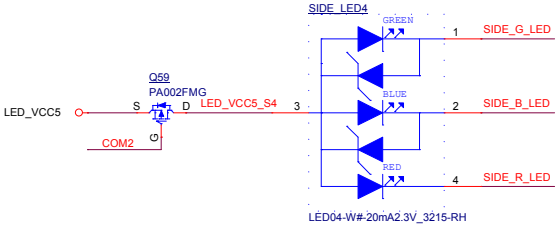


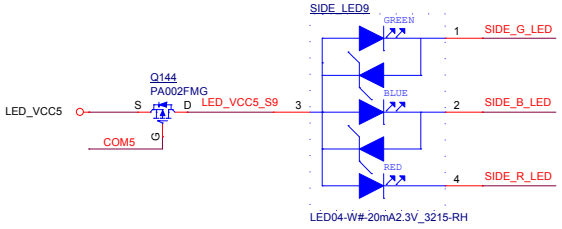


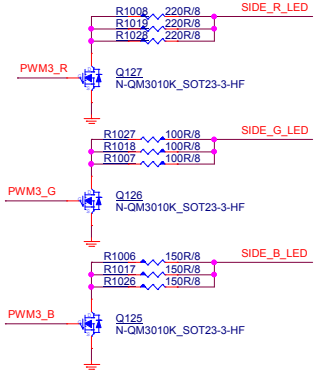


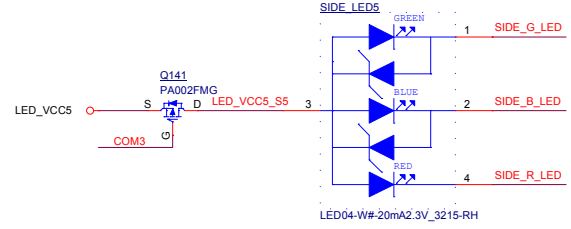


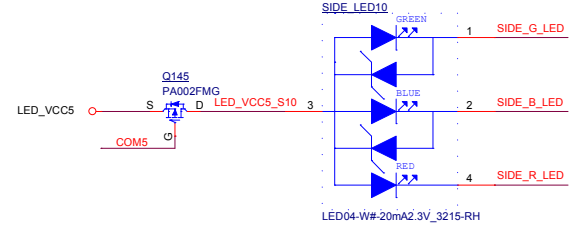












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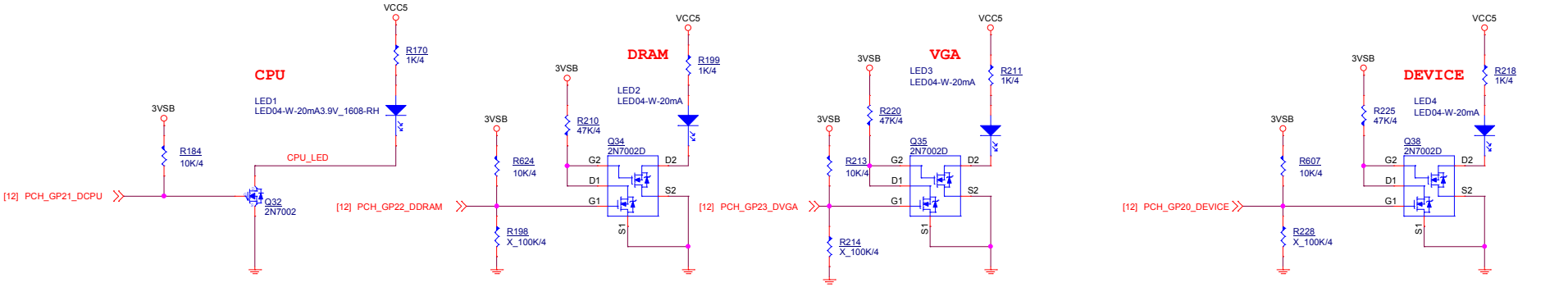
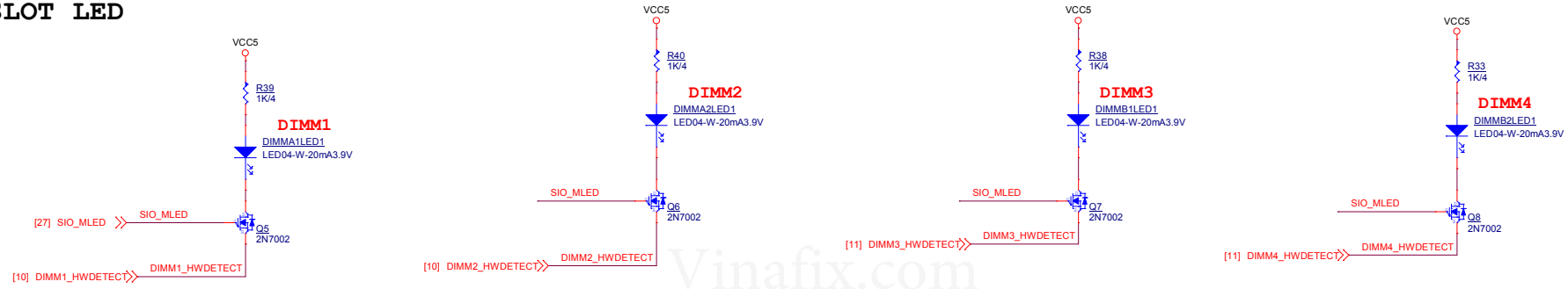


DIMM SLOT LED



SLOT LED

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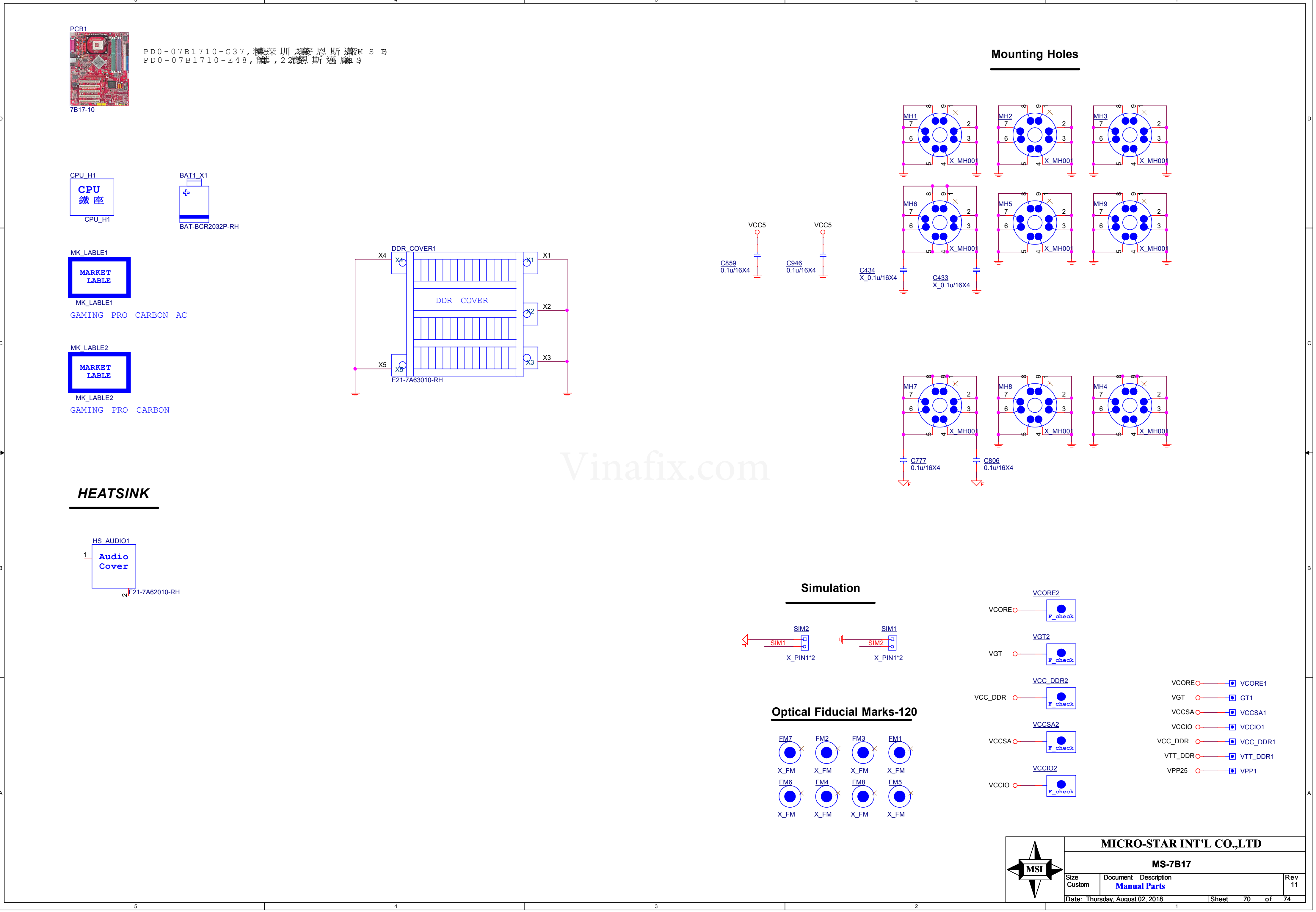

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