1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J43 MLB SCHEMATIC DVT
REV 6.5.0
4/09/13

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9800	1	SCHEM,MLB,J43	SCH	CRITICAL	
820-3437	1	PCBF,MLB,J43	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Apr 9 20:06:04 2013

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB'TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 1 OF 121
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BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,MLB_MISC,MLB_DEBUG:ENG,MLB_PROGPARTS
MLB_MISC	PP5V5_DCIN:NO,TBTHV:P15V,EDP,CAM_XTAL:NO,CAM_WAKE:NO,APCLKRQ:ISOL,TPAD_INTWAKE:SHARED,USB_PWR:S3,SD_ON_MLB,VCORE_FETS
MLB_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,DDRVREF_DAC,S0PGOOD_ISL,DBGLED,ISNS:ENG
MLB_DEVEL:PVT	XDP_CONN
MLB_DEBUG:ENG	DEVEL_BOM,XDP,LPCPLUS
MLB_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,XDP,LPCPLUS,ISNS:PROD
MLB_DEBUG:PROD	BKLT:PROD,LPCPLUS,XDP,ISNS:PROD

Current Sensor Configuration

BOM GROUP	BOM OPTIONS
ISNS:ENG	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,P1V05_ISNS:YES,AIRPORT_ISNS:YES,SSD_ISNS:YES,LCDBKLT_ISNS:YES,P3V3SS_ISNS:YES,3V3S0_ISNS:YES,OTHER_HS_ISNS:YES,CAM_ISNS:YES,CPUDDR_ISNS:YES,PANEL_ISNS:YES
ISNS:PROD	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,P1V05_ISNS:NO,AIRPORT_ISNS:NO,SSD_ISNS:YES,LCDBKLT_ISNS:NO,P3V3SS_ISNS:NO,3V3S0_ISNS:NO,OTHER_HS_ISNS:NO,CAM_ISNS:NO,CPUDDR_ISNS:NO,PANEL_ISNS:NO

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:MICRON_4GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:MICRON_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2X3QFN	U2890	CRITICAL	TBTROM:BLANK
341S3802	1	IC,EEPROM,C/R (V23.4) EVT,J41/J41	U2890	CRITICAL	TBTROM:PROG
338S1159	1	IC,SMC12-A3,40MHZ/50DMIPS MCU,9X9,157BGA	U5000	CRITICAL	SMC:BLANK
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_NUM:BLANK
341S3809	1	IC,EFI ROM (V0071) DVT,J41/J43	U6100	CRITICAL	BOOTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4525	1	HSW,SR16M,PRQ,C0,1.3,15W,2+3,1.0,3M,BGA	U0500	CRITICAL	CPU:1.3GHZ
337S4526	1	HSW,SR16L,PRQ,C0,1.4,15W,2+3,1.1,3M,BGA	U0500	CRITICAL	CPU:1.4GHZ
337S4528	1	HSW,SR16H,PRQ,C0,1.7,15W,2+3,1.1,4M,BGA	U0500	CRITICAL	CPU:1.7GHZ
338S1113	1	IC,TBT,CR-4C,B1,PRQ,CIO,288,12X12 FC-CSP	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CAMERA PROCESSOR	U3900	CRITICAL	
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	J41_MLB
946-3892	1	J11/J13 MLB DYMAX ADHESIVE 29993-SC 0.4G	GLUE	CRITICAL	
825-7670	1	LABEL,TEXT,MLB,K21/K78	LABEL		
376S0964	2	MOSFET,N-CH,25V,30A,9.6M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S1104	2	MOSFET,N-CH,25V,30A,6.1M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN
376S1173	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1174	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
900-0090	1		SOLDERPASTE	CRITICAL	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0681	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0676	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0680	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0678	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0666	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0679	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:MICRON_4GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1032	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S0586	152S1301		ALL	Dale/Vishay alt to Cyntec
372S0186	372S0185		ALL	NXP alt to Diodes
197S0479	197S0478		ALL	200uW Epson alt to NDK
376S1053	376S0604		ALL	Diodes alt to Fairchild
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0371	128S0376		ALL	Kemet alt to Sanyo
128S0394	128S0415		ALL	NEC alt to Sanyo
152S1821	152S1757		ALL	Cyntec alt to NEC
197S0480	197S0343		ALL	NDK crystal alt to TXC
197S0481	197S0343		ALL	Epson crystal alt to TXC
107S0254	107S0241		ALL	Cyntec sense R alt to TFT
353S3452	353S1286		ALL	Maxim alt to Microchip
128S0386	128S0284		ALL	Kemet alt to Sanyo
128S0397	128S0325		ALL	Kemet alt to Sanyo
377S0155	377S0104		ALL	OnSemi alt to Infineon
128S0398	128S0220		ALL	Kemet alt to Sanyo
197S0542	197S0544		ALL	NDK alt to TXC
197S0545	197S0544		ALL	Epson alt to TXC
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0841	138S0638		ALL	Murata alt to Samsung
376S1180	376S0761		ALL	Renesas alt to Vishay
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cyntec alt to TFT
107S0250	107S0248		ALL	Cyntec alt to TFT

SYNC_MASTER=J41_MLB SYNC_DATE=04/09/2013

PAGE TITLE

BOM Configuration

Apple Inc.

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BOM Variants NOTE: All the "GOOD" BOM Configs have been de-activated

BOM NUMBER	BOM NAME	BOM OPTIONS
639-4146	PCBA,MLB,GOOD,HY-4GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_4GB
639-4293	PCBA,MLB,GOOD,HY-8GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_8GB
639-4294	PCBA,MLB,GOOD,EL-4GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_4GB
639-4295	PCBA,MLB,GOOD,EL-8GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_8GB
639-4745	PCBA,MLB,GOOD,MI-4GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:MICRON_4GB
639-4445	PCBA,MLB,BETTER,HY-4GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_4GB
639-4446	PCBA,MLB,BETTER,HY-8GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_8GB
639-4447	PCBA,MLB,BETTER,EL-4GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_4GB
639-4448	PCBA,MLB,BETTER,EL-8GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_8GB
639-4746	PCBA,MLB,BETTER,MI-4GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:MICRON_4GB
639-4755	PCBA,MLB,BEST,HY-4GB,J43	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-4756	PCBA,MLB,BEST,HY-8GB,J43	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_8GB
639-4757	PCBA,MLB,BEST,EL-4GB,J43	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-4758	PCBA,MLB,BEST,EL-8GB,J43	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_8GB
639-4759	PCBA,MLB,BEST,MI-4GB,J43	MLB_CMNPTS,CPU:1.7GHZ,DDR3:MICRON_4GB
685-0025	CMN PTS,PCBA,MLB,J43	MLB_COMMON
985-0018	J43 MLB DEVELOPMENT BOM	MLB_DEVEL:ENG
685-0064	VCORE FET,REN,J43	VCORE_FET:REN
685-0065	VCORE FET,VSHY,J43	VCORE_FET:VSHY

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-0064	685-0065		ALL	Renesas alt for Vishay
333S0704	333S0700		ALL	Elpida CAM DRAM alt to Hynix

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3758	1	IC,SMC-A3 SCPL,EXT,V22.12a19,PROTO 1,J43	U5000	CRITICAL	SMC:PROG

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,SMC:PROG,TBTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S1215	1	IC,GL3219,USB3 SD CARD READER,46P,LQFN	U4500	CRITICAL	

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
985-0018	1	J43 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
685-0025	1	CMN PTS,PCBA,MLB,J43	CMNPTS	CRITICAL	MLB_CMNPTS
685-0065	1	VCORE FET,VSHY,J43	VCOREFETS	CRITICAL	VCORE_FETS

SYNC_MASTER=K21_MLB SYNC_DATE=11/16/2010

PAGE TITLE: BOM Variants

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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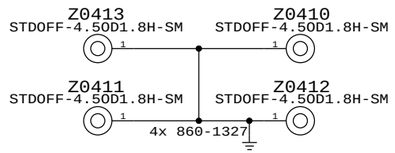
PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-5107	1	CAN,TOPSIDE,ALT,J41/J43	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-5108	1	CAN,TOPSIDE,COVER,ALT,J41/J43	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
725-1792	1	INSULATOR,CPU,J41/J43	CPU_INSULATOR	CRITICAL	

Plated Board Slot

SL0400
TH-NSP
SL-2.3X3.9-2.9X4.5

CPU Heat Sink Mounting Bosses



Fan Boss

Z0405
STDOFF-4.5OD1.8H-SM
860-1327

X21 Boss

Z0414
STDOFF-4.5OD1.9H-SM
860-1327

SSD Boss

Z0415
STDOFF-4.5OD1.9H-SM
860-1327

EMI I/O Pogo Pins

DisplayPort Pogo

CRITICAL
ZS0405
POGO-2.0OD-3.6H-K86-K87
SM
870-1938

USB/SD Card Pogo

CRITICAL
ZS0406
POGO-2.0OD-3.6H-K86-K87
SM
870-1938

Can Slots

SL0401
TH-NSP
SL-1.1X0.4-1.4X0.7

SL0402
TH-NSP
SL-1.1X0.4-1.4X0.7
2x TBT pin diodes

SL0403
TH-NSP
SL-1.1X0.4-1.4X0.7

SL0406
TH-NSP
SL-1.1X0.4-1.4X0.7
2x MDP Connector

SL0405
TH-NSP
SL-1.1X0.45-1.4X0.75

SL0407
TH-NSP
SL-1.1X0.45-1.4X0.75
2x TBT chip

SL0404
TH-NSP
SL-1.1X0.4-1.4X0.7

SL0408
TH-NSP
SL-1.1X0.4-1.4X0.7
2x USB Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
PD PARTS

Apple Inc.

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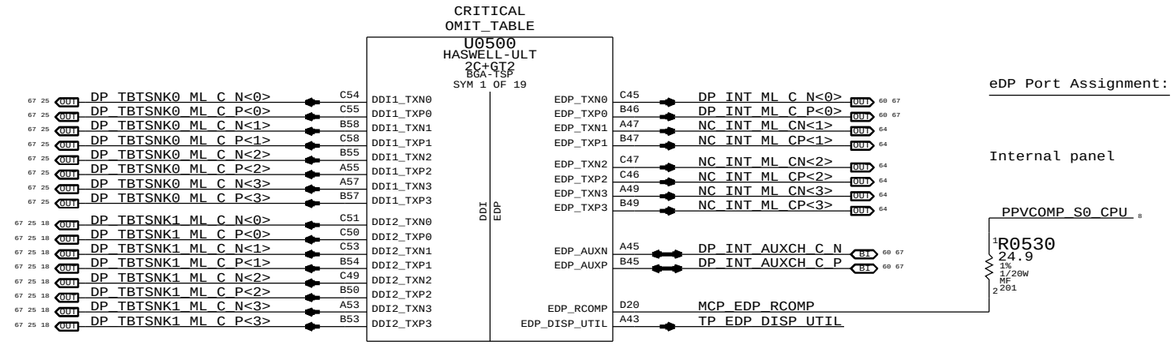
DDI Port Assignments:

TBT Sink 0

TBT Sink 1
(MUXed with HDMI
 if necessary)

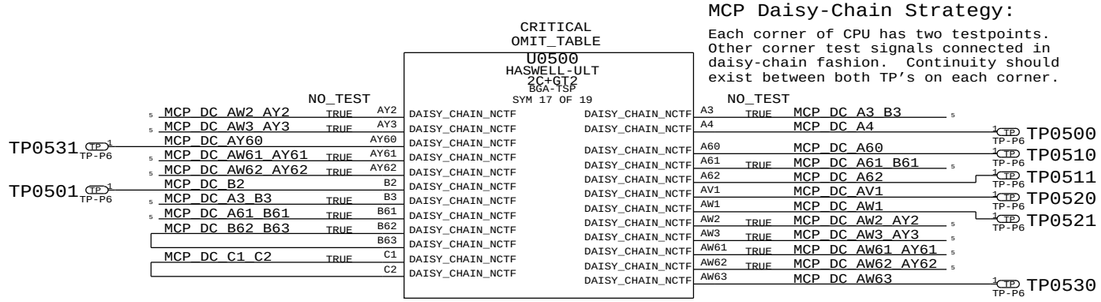


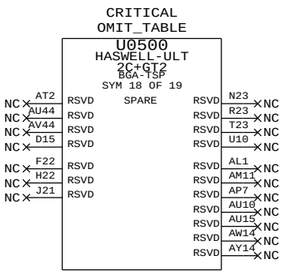
eDP Port Assignment:

Internal panel

MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints.
Other corner test signals connected in
daisy-chain fashion. Continuity should
exist between both TP's on each corner.





SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: CPU GFX/NCTF/RSVD

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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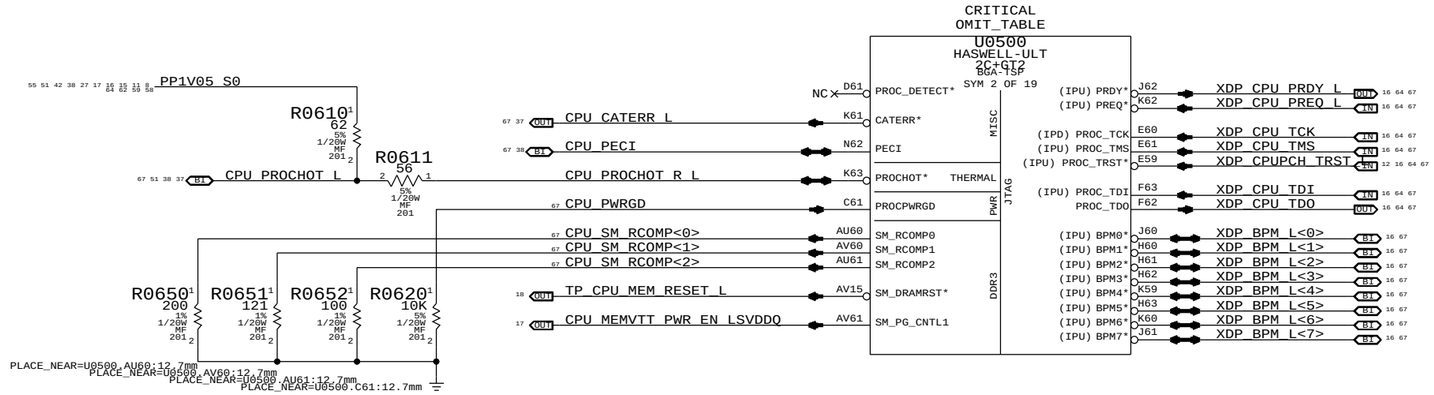
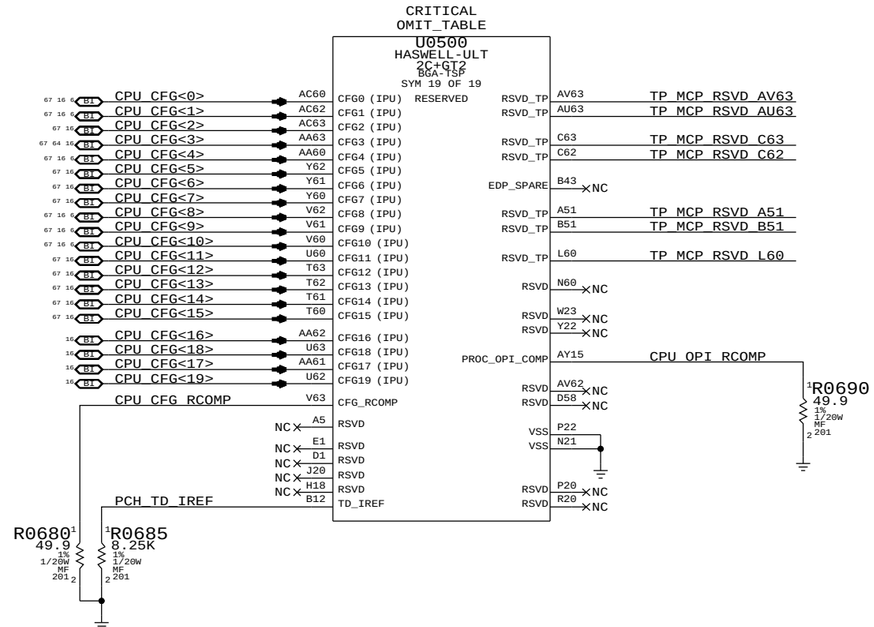
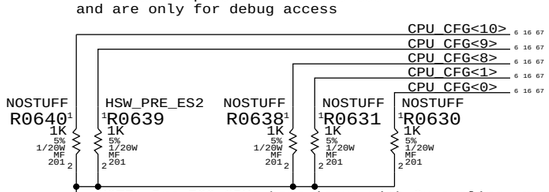


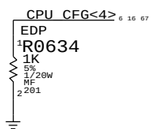


CFG<10>	:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9>	:NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8>	:ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4>	:eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1>	:PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0>	:RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



SYNC_MASTER=J41_MLB SYNC_DATE=04/02/2013

PAGE TITLE: CPU Misc/JTAG/CFG/RSVD

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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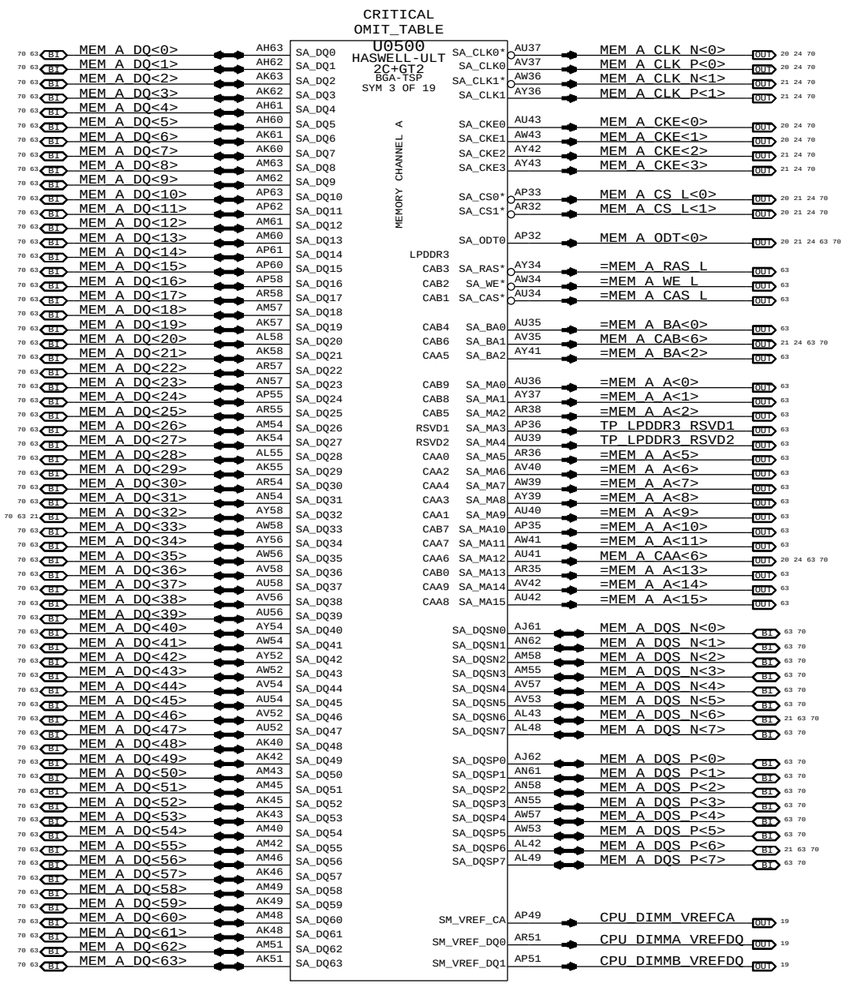

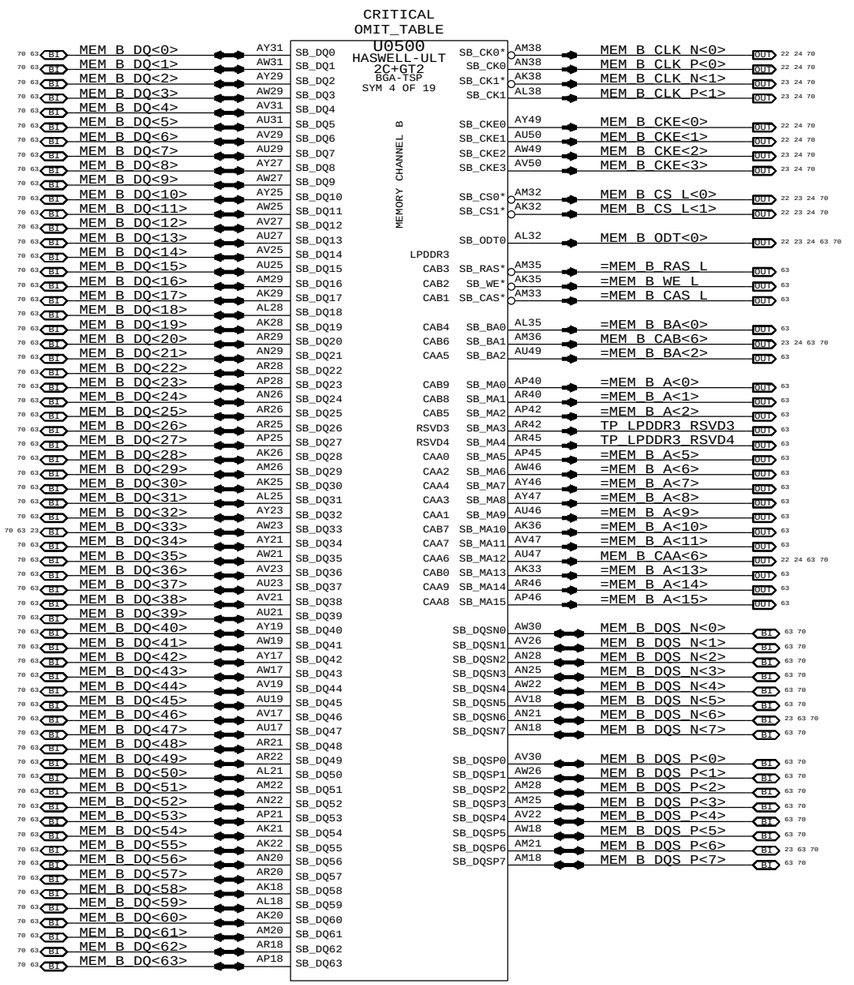

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE

CPU DDR3/LPDDR3 Interfaces

Apple Inc.

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HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.

CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 12 OF 19
HSW ULT POWER

PPVCC_S0_CPU
32A Max

PPVMEMIO_S0_CPU
1.4A Max (DDR3: 1.5-1.35V)
1.1A Max (LPDDR3: 1.2V)

PPVCC_S0_CPU
R0860 100 5% 1/20W MF 201
PLACE_NEAR=U0500.C50:50.8mm

CPU_VCCSENSE_P
TP_PPVCCIO_S0_CPU
PPVCOMP_S0_CPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
NOTE: Aliases not used on CPU supply outputs to avoid any extraneous connections.

PP1V05_S0
R0800 75 1% 1/20W MF 201
R0802 130 1% 1/20W MF 201
Max load: 300mA
Max load: 300mA
R0810 43 5% 1/20W MF 201
R0811 0 5% 1/20W MF 0201
R0812 0 5% 1/20W MF 0201
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
R0802.2: PLACE_NEAR=U0500.L63:2.54mm
R0810.2: PLACE_NEAR=U0500.L62:38.1mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm

CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_VCCST_PWRGD
CPU_VR_EN
CPU_VR_READY
CPU_PWR_DEBUG
TP_CPU_RSVD_P60
TP_CPU_RSVD_P61
TP_CPU_RSVD_N59
TP_CPU_RSVD_N61

PP1V05_S0
???mA Max
PPVRTC_G3H

CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
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LPT LP POWER

PP1V05_S0SW_PCH_HSIO
1838mA Max
PP1V05_S0
29mA Max[1]
PP1V05_S0SW_PCH_VCCUSB3PLL
41mA Max
PP1V05_S0SW_PCH_VCCSATA3PLL
42mA Max
WF: RSVD on Sawtooth Peak rev 1.0
PP1V05_S0_PCH_VCCAPLL_OPI
57mA Max
PP1V5_S0SW_AUDIO_HDA
11mA Max
PP3V3_SUS
59mA Max[1]
PP3V3_S5
114mA Max
PP3V3_S0
40mA Max[1]
PP1V05_S0_PCH_VCC_ICC
VCCCLK: 200mA Max
PP1V05_S0_PCH_VCCACLKPLL
31mA Max
PP1V05_S0
VCCCLK: 200mA Max
WF: RSVD on Sawtooth Peak rev 1.0
PP3V3_SUS
3.3mA Max[1]

PP3V3_SUS
0.3mA Max[1]
PPVOUT_S0_PCH_DCPRTC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
BYPASS=U0500.AE7:6.35mm
C0895 0.1UF 20% 10V CERM 402
PP3V3_SUS
18mA Max
PP1V05_S0
185mA Max[1]
PP1V05_S0
1499mA Max[1]
PLACE_NEAR=U0500.AG19:2.54mm
R0899 5.11 1% 1/20W MF-LF 201
PPVOUT_S5_PCH_DCPSUSBYP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
Powered in DeepSx
C0899 1UF 10% 6.3V CERM 402
BYPASS=R0899:U0500:2.54mm
PP1V05_S0
473mA Max[1]
PP1V5_S0
3mA Max
PP3V3_S0
1mA Max[1]
PP3V3_S0
17mA Max
WF: RSVD on Sawtooth Peak rev 1.0
PP1V05_S0
213mA Max[1]

C0892 1UF 0.1UF 20% 10V CERM 402
C0891 1UF 0.1UF 20% 10V CERM 402
C0890 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG10:6.35mm
BYPASS=U0500.AG10:6.35mm
BYPASS=U0500.AG10:6.35mm

SYNC_MASTER=J41_MLB
SYNC_DATE=04/09/2013
PAGE TITLE
CPU/PCH POWER
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CRITICAL
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U0500
HASWELL-ULT
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A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

CRITICAL
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AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

CRITICAL
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U0500
HASWELL-ULT
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D33	VSS	VSS	H17
D34	VSS	VSS	H57
D35	VSS	VSS	J10
D37	VSS	VSS	J22
D38	VSS	VSS	J59
D39	VSS	VSS	J63
D41	VSS	VSS	K1
D42	VSS	VSS	K12
D43	VSS	VSS	L13
D45	VSS	VSS	L15
D46	VSS	VSS	L17
D47	VSS	VSS	L18
D49	VSS	VSS	L20
D5	VSS	VSS	L58
D50	VSS	VSS	L61
D51	VSS	VSS	L7
D53	VSS	VSS	M22
D54	VSS	VSS	N10
D55	VSS	VSS	N3
D57	VSS	VSS	P59
D59	VSS	VSS	P63
D62	VSS	VSS	R10
D8	VSS	VSS	R22
E11	VSS	VSS	R8
E17	VSS	VSS	T1
F20	VSS	VSS	T58
F26	VSS	VSS	U20
F30	VSS	VSS	U22
F34	VSS	VSS	U61
F38	VSS	VSS	U9
F42	VSS	VSS	V10
F46	VSS	VSS	V3
F50	VSS	VSS	V7
F54	VSS	VSS	W20
F58	VSS	VSS	W22
F61	VSS	VSS	Y10
G18	VSS	VSS	Y59
G22	VSS	VSS	Y63
G3	VSS		
G5	VSS	VSS	V58
G6	VSS	VSS	AH46
G8	VSS	VSS	V23
H13	VSS	VSS_SENSE	E62
		VSS	AH16

CPU_VCCSENSE_N OUT 51 67

R0960
100
5%
1/20W
MF
201
2

PLACE_NEAR=U0500.E62:50.8mm

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

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All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook P[illegible]n Power Delivery Design Guide Rev 1.0 unless stated otherwise

CPU VCC D[illegible]oupling

Intel recommendat[illegible](Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementat[illegible]: 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff

64 62 52 42 8 PPVCC_S0_CPU

CRITICAL C1000 10UF 20% 4V X6S 0402
CRITICAL C1001 10UF 20% 4V X6S 0402
CRITICAL C1002 10UF 20% 4V X6S 0402
CRITICAL C1003 10UF 20% 4V X6S 0402
CRITICAL C1004 10UF 20% 4V X6S 0402
NO STUFF C1005 10UF 20% 4V X6S 0402
NO STUFF C1006 10UF 20% 4V X6S 0402
CRITICAL C1007 10UF 20% 4V X6S 0402
NO STUFF C1008 10UF 20% 4V X6S 0402
NO STUFF C1009 10UF 20% 4V X6S 0402
CRITICAL C1010 10UF 20% 4V X6S 0402
NO STUFF C1011 10UF 20% 4V X6S 0402
CRITICAL C1012 10UF 20% 4V X6S 0402
NO STUFF C1013 10UF 20% 4V X6S 0402
CRITICAL C1014 10UF 20% 4V X6S 0402
NO STUFF C105A 10UF 20% 4V X6S 0402
NO STUFF C105B 10UF 20% 4V X6S 0402
NO STUFF C105C 10UF 20% 4V X6S 0402
NO STUFF C105D 10UF 20% 4V X6S 0402
NO STUFF C105E 10UF 20% 4V X6S 0402
NO STUFF C105F 10UF 20% 4V X6S 0402

NO STUFF C1015 10UF 20% 4V X6S 0402
CRI[illegible] C1016 10UF 20% 4V X6S 0402
CRITICAL C1017 10UF 20% 4V X6S 0402
CRITICAL C1018 10UF 20% 4V X6S 0402
NO STUFF C1019 10UF 20% 4V X6S 0402
NO STUFF C1020 10UF 20% 4V X6S 0402
CRITICAL C1021 10UF 20% 4V X6S 0402
NO STUFF C1030 10UF 20% 4V X6S 0402
NO STUFF C104A 10UF 20% 4V X6S 0402
NO STUFF C104B 10UF 20% 4V X6S 0402
NO STUFF C104C 10UF 20% 4V X6S 0402
NO STUFF C104D 10UF 20% 4V X6S 0402
NO STUFF C104E 10UF 20% 4V X6S 0402
NO STUFF C104F 10UF 20% 4V X6S 0402
NO STUFF C106A 10UF 20% 4V X6S 0402
NO STUFF C106B 10UF 20% 4V X6S 0402
NO STUFF C106C 10UF 20% 4V X6S 0402
NO STUFF C106D 10UF 20% 4V X6S 0402
NO STUFF C106E 10UF 20% 4V X6S 0402

NO STUFF C1070 10UF 20% 4V X6S 0402
NO STUFF C10[illegible] 10UF 20% 4V X6S 0402
NO STUFF C1072 10UF 20% 4V X6S 0402
NO STUFF C1073 10UF 20% 4V X6S 0402
NO STUFF C1074 10UF 20% 4V X6S 0402
NO STUFF C1075 10UF 20% 4V X6S 0402
CRITICAL C1076 10UF 20% 4V X6S 0402
CRITICAL C1077 10UF 20% 4V X6S 0402
NO STUFF C1078 10UF 20% 4V X6S 0402
NO STUFF C1079 10UF 20% 4V X6S 0402
NO STUFF C1080 10UF 20% 4V X6S 0402
NO STUFF C1081 10UF 20% 4V X6S 0402
NO STUFF C1082 10UF 20% 4V X6S 0402
CRITICAL C1083 10UF 20% 4V X6S 0402
CRITICAL C1084 10UF 20% 4V X6S 0402

NO STUFF C1085 10UF 20% 4V X6S 0402
NO STUFF C10[illegible] 10UF 20% 4V X6S 0402
NO STUFF C1087 10UF 20% 4V X6S 0402
CRITICAL C1088 10UF 20% 4V X6S 0402
CRITICAL C1089 10UF 20% 4V X6S 0402
NO STUFF C1090 10UF 20% 4V X6S 0402
NO STUFF C1091 10UF 20% 4V X6S 0402
NO STUFF C1092 10UF 20% 4V X6S 0402
NO STUFF C1093 10UF 20% 4V X6S 0402
NO STUFF C1094 10UF 20% 4V X6S 0402
NO STUFF C1095 10UF 20% 4V X6S 0402
NO STUFF C1096 10UF 20% 4V X6S 0402
NO STUFF C1097 10UF 20% 4V X6S 0402

NO STUFF C1022 10UF 20% 4V X6S 0402
NO STUFF C10[illegible] 10UF 20% 4V X6S 0402
NO STUFF C1024 10UF 20% 4V X6S 0402
NO STUFF C1025 10UF 20% 4V X6S 0402
NO STUFF C1026 10UF 20% 4V X6S 0402
NO STUFF C1027 10UF 20% 4V X6S 0402
NO STUFF C1028 10UF 20% 4V X6S 0402
NO STUFF C1029 10UF 20% 4V X6S 0402
NO STUFF C1032 10UF 20% 4V X6S 0402
NO STUFF C1033 10UF 20% 4V X6S 0402
NO STUFF C1034 10UF 20% 4V X6S 0402
NO STUFF C1035 10UF 20% 4V X6S 0402
NO STUFF C1036 10UF 20% 4V X6S 0402
NO STUFF C1037 10UF 20% 4V X6S 0402
NO STUFF C1038 10UF 20% 4V X6S 0402

NO STUFF C1039 10UF 20% 4V X6S 0402
NO STUFF C10[illegible] 10UF 20% 4V X6S 0402
NO STUFF C1045 10UF 20% 4V X6S 0402
NO STUFF C1046 10UF 20% 4V X6S 0402
NO STUFF C1047 10UF 20% 4V X6S 0402
NO STUFF C1048 10UF 20% 4V X6S 0402
NO STUFF C1049 10UF 20% 4V X6S 0402

NO STUFF C1056 10UF 20% 4V X6S 0402
NO STUFF C10[illegible] 10UF 20% 4V X6S 0402
NO STUFF C1058 10UF 20% 4V X6S 0402
NO STUFF C1059 10UF 20% 4V X6S 0402
NO STUFF C1062 10UF 20% 4V X6S 0402
NO STUFF C1063 10UF 20% 4V X6S 0402
NO STUFF C1064 10UF 20% 4V X6S 0402
NO STUFF C1065 10UF 20% 4V X6S 0402
NO STUFF C1066 10UF 20% 4V X6S 0402
NO STUFF C1067 10UF 20% 4V X6S 0402
NO STUFF C1068 10UF 20% 4V X6S 0402
NO STUFF C1069 10UF 20% 4V X6S 0402
NO STUFF C1098 10UF 20% 4V X6S 0402
NO STUFF C1099 10UF 20% 4V X6S 0402
NO STUFF C109A 10UF 20% 4V X6S 0402

NO STUFF C109B 10UF 20% 4V X6S 0402
NO STUFF C10[illegible] 10UF 20% 4V X6S 0402
NO STUFF C109D 10UF 20% 4V X6S 0402
NO STUFF C109E 10UF 20% 4V X6S 0402
NO STUFF C109F 10UF 20% 4V X6S 0402
NO STUFF C108A 10UF 20% 4V X6S 0402
NO STUFF C108B 10UF 20% 4V X6S 0402
NO STUFF C108C 10UF 20% 4V X6S 0402
NO STUFF C108D 10UF 20% 4V X6S 0402
NO STUFF C108E 10UF 20% 4V X6S 0402
NO STUFF C108F 10UF 20% 4V X6S 0402
NO STUFF C107A 10UF 20% 4V X6S 0402
NO STUFF C107B 10UF 20% 4V X6S 0402

CRITICAL C1031 470UF-0.0045OH 20% 2.5V POLY-TANT SM

CPU VDDQ D[illegible]OUPLING

Intel recommendati[illegible]Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
Apple implementati[illegible]: 4x 2.2uF 0402, 6x 10uF 0402, 2x 270uF B2 no stuff

42 8 PPVMEMIO_S0_CPU

C1040 2.2UF 20% 6.3V CERM 402-LF
C10[illegible] 2.2UF 20% 6.3V CERM 402-LF
C1042 2.2UF 20% 6.3V CERM 402-LF
C1043 2.2UF 20% 6.3V CERM 402-LF

C1050 10UF 20% 6.3V CERM-X5R 0402-1
C1051 10UF 20% 6.3V CERM-X5R 0402-1
C1052 10UF 20% 6.3V CERM-X5R 0402-1
C1053 10UF 20% 6.3V CERM-X5R 0402-1
C1054 10UF 20% 6.3V CERM-X5R 0402-1
C1055 10UF 20% 6.3V CERM-X5R 0402-1

C1060 270UF 20% 2V TANT CASE-B2-SM
NO STUFF C1061 270UF 20% 2V TANT CASE-B2-SM

2x Bulk nostuff per Harris Beach v1.0 schematic

SYNC_MASTER=WILL_J43 SYNC_DATE=01/08/2013
PAGE TITLE: CPU Decoupling
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
NO STUFF
C1200 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH10:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS
NO STUFF
C1202 0.1UF 20% 25V CERM 402
BYPASS=U0500.Y8:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS
C1204 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.AC9:12.7mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
C1206 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH11:6.35mm

PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0
C1208 1UF 10% 6.3V CERM 402
BYPASS=U0500.U8:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0SW_AUDIO_HDA
C1210 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0
C1212 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.V8:12.7mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
C1214 0.1UF 20% 25V CERM 402
BYPASS=U0500.K14:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
NO STUFF
C1250 22UF 20% 6.3V X5R-CERM-1 603
C1251 1UF 10% 6.3V CERM 402
BYPASS=U0500.AE9:12.7mm
BYPASS=U0500.AE9:6.35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C1255 10UF 20% 6.3V X5R 603
C1256 1UF 10% 6.3V CERM 402
C1257 1UF 10% 6.3V CERM 402
BYPASS=U0500.J11:12.7mm
BYPASS=U0500.J11:6.35mm
BYPASS=U0500.AE8:6.35mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
PP1V05_S0SW_PCH_HSIO
C1260 1UF 10% 6.3V CERM 402
C1261 1UF 10% 6.3V CERM 402
C1262 10UF 20% 6.3V CERM-X5R 0402-1
BYPASS=U0500.K9:6.35mm
BYPASS=U0500.L10:6.35mm
BYPASS=U0500.M9:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
C1264 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG16:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0
C1266 1UF 10% 6.3V CERM 402
C1267 1UF 10% 6.3V CERM 402
BYPASS=U0500.J17:6.35mm
BYPASS=U0500.R21:6.35mm

PP1V05_S0
??mA Max
R1270 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603

PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max
C1270 47UF 20% 4V CERM-X5R 0805-1
C1271 47UF 20% 4V CERM-X5R 0805-1
C1272 1UF 10% 10V X5R 402
BYPASS=U0500.A20:12.7mm
BYPASS=U0500.A20:12.7mm
BYPASS=U0500.A20:6.35mm

R1275 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603

PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max
C1275 47UF 20% 4V CERM-X5R 0805-1
C1276 47UF 20% 4V CERM-X5R 0805-1
C1277 1UF 10% 10V X5R 402
BYPASS=U0500.J18:12.7mm
BYPASS=U0500.J18:12.7mm
BYPASS=U0500.J18:6.35mm

R1280 0 5% 1/16W MF-LF 402

CRITICAL
NO STUFF
L1280 2.2UH-240MA-0.221OHM 0603

PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max
NO STUFF C1280 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1281 47UF 20% 4V CERM-X5R 0805-1
C1282 1UF 10% 10V X5R 402
BYPASS=U0500.AA21:12.7mm
BYPASS=U0500.AA21:12.7mm
BYPASS=U0500.AA21:6.35mm

PP1V05_S0SW_PCH_HSIO
83mA Max

CRITICAL
L1290 2.2UH-240MA-0.221OHM 0603

PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max
NO STUFF C1290 47UF 20% 4V CERM-X5R 0805-1
C1291 47UF 20% 4V CERM-X5R 0805-1
C1292 1UF 10% 10V X5R 402
BYPASS=U0500.B11:12.7mm
BYPASS=U0500.B11:12.7mm
BYPASS=U0500.B11:6.35mm

CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603

PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max
NO STUFF C1295 47UF 20% 4V CERM-X5R 0805-1
C1296 47UF 20% 4V CERM-X5R 0805-1
C1297 1UF 10% 10V X5R 402
BYPASS=U0500.B18:12.7mm
BYPASS=U0500.B18:12.7mm
BYPASS=U0500.B18:6.35mm

LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC_MASTER=J41_MLB SYNC_DATE=02/07/2013

PAGE TITLE: PCH Decoupling

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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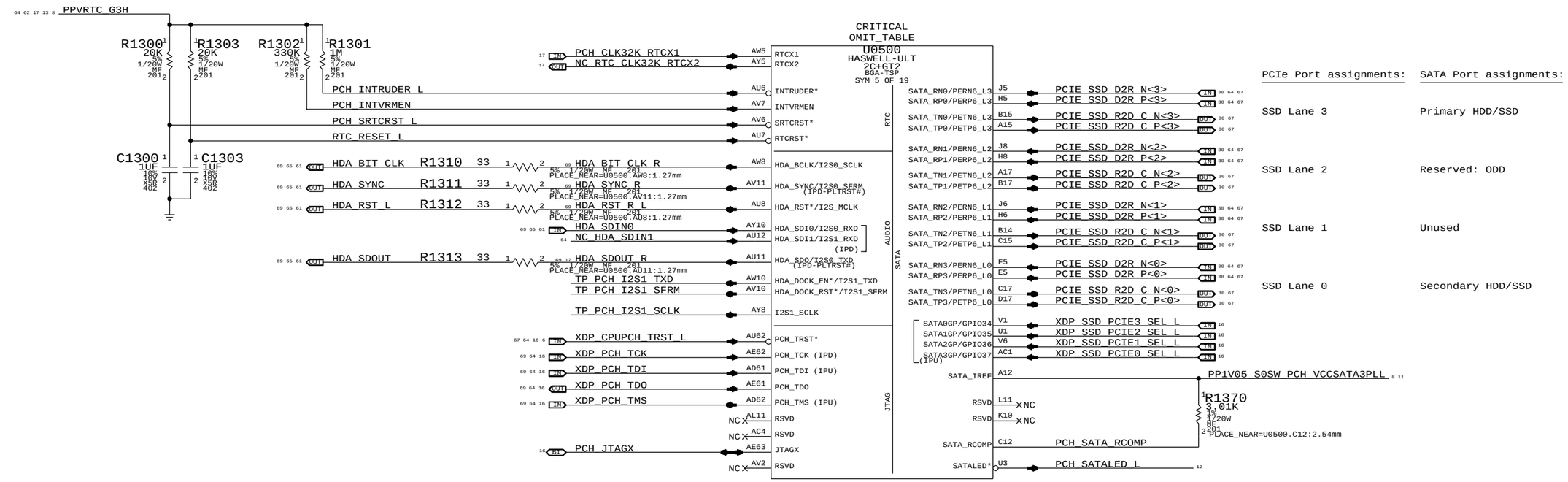
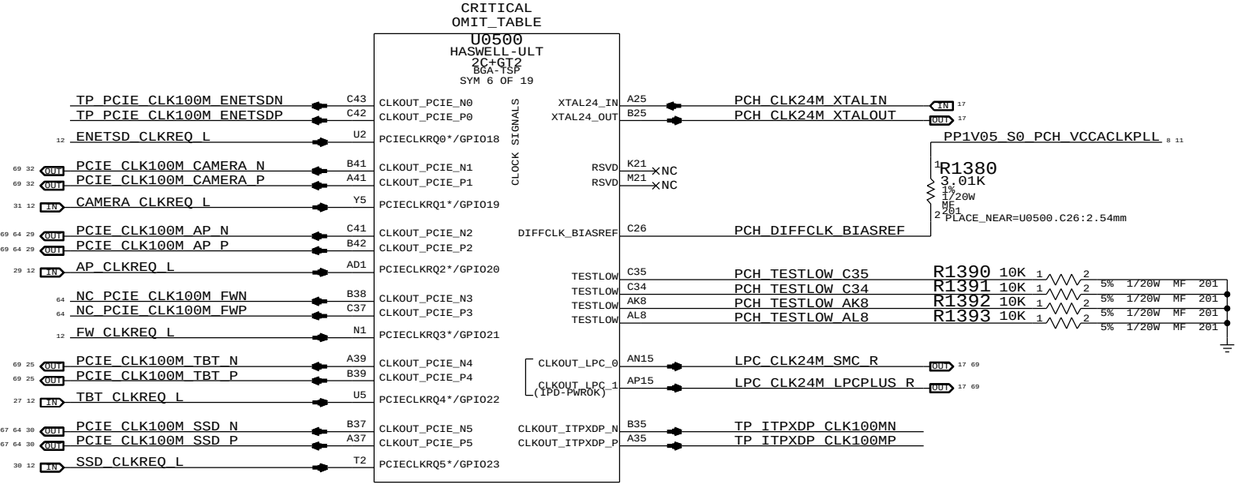
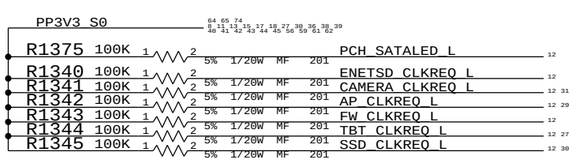
SHEET: 11 OF 76







SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: PCH Audio/JTAG/SATA/CLK

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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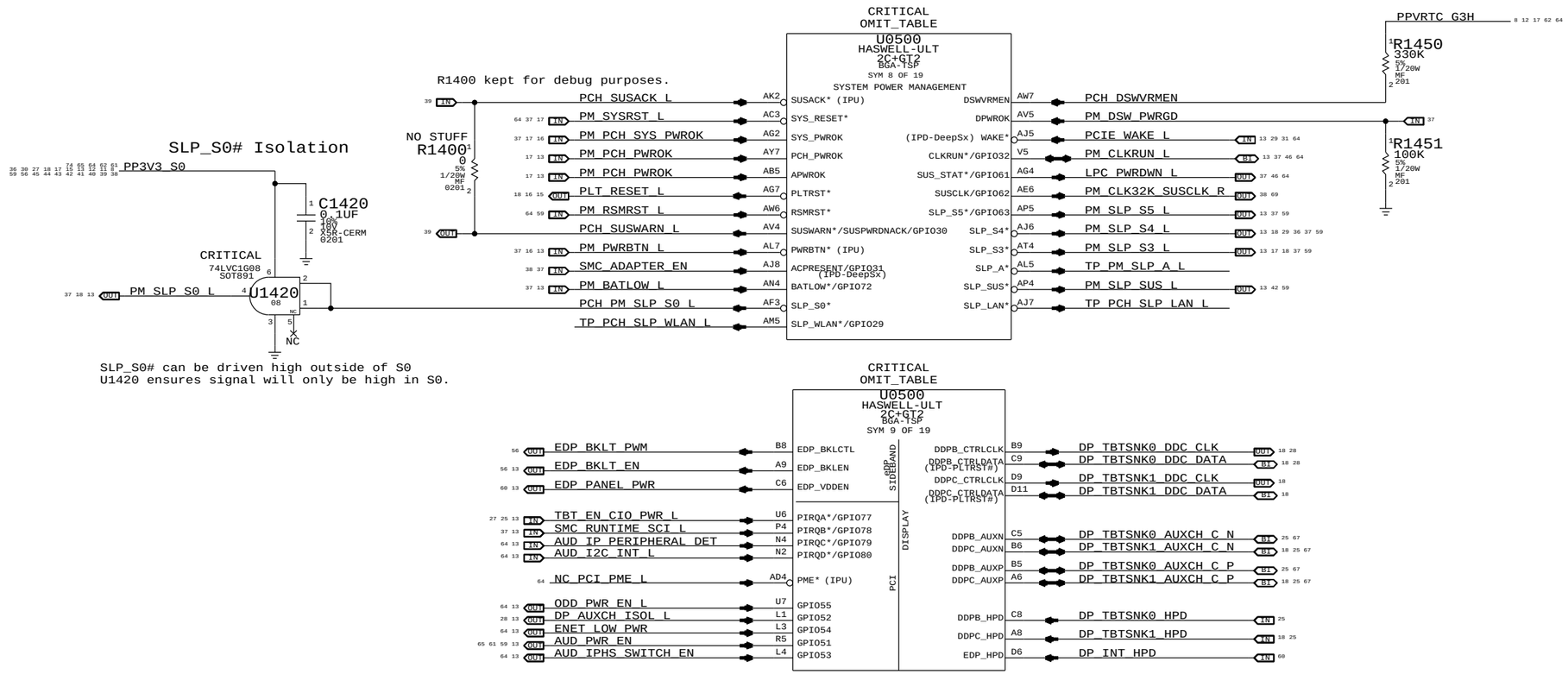

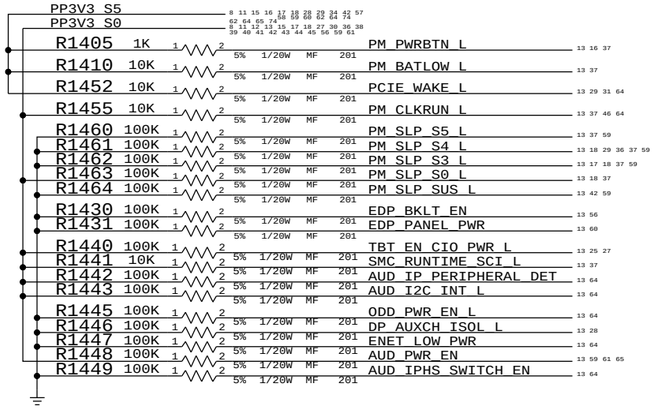

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
PCH PM/PCI/GFX

Apple Inc.

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PCIe Port Assignments:

Thunderbolt lane 0

Thunderbolt lane 1

Thunderbolt lane 2

Thunderbolt lane 3

AirPort

Reserved: FireWire

SD Card Reader
(& Ethernet if combo)

Camera

CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 11 OF 19

PCIE_TBT_D2R_N<0> F10 PERN5_L0
PCIE_TBT_D2R_P<0> E10 PERP5_L0
PCIE_TBT_R2D_C_N<0> C23 PETN5_L0
PCIE_TBT_R2D_C_P<0> C22 PETP5_L0
PCIE_TBT_D2R_N<1> F8 PERN5_L1
PCIE_TBT_D2R_P<1> E8 PERP5_L1
PCIE_TBT_R2D_C_N<1> B23 PETN5_L1
PCIE_TBT_R2D_C_P<1> A23 PETP5_L1
PCIE_TBT_D2R_N<2> H10 PERN5_L2
PCIE_TBT_D2R_P<2> G10 PERP5_L2
PCIE_TBT_R2D_C_N<2> B21 PETN5_L2
PCIE_TBT_R2D_C_P<2> C21 PETP5_L2
PCIE_TBT_D2R_N<3> E6 PERN5_L3
PCIE_TBT_D2R_P<3> F6 PERP5_L3
PCIE_TBT_R2D_C_N<3> B22 PETN5_L3
PCIE_TBT_R2D_C_P<3> A21 PETP5_L3
PCIE_AP_D2R_N G11 PERN3
PCIE_AP_D2R_P F11 PERP3
PCIE_AP_R2D_C_N C29 PETN3
PCIE_AP_R2D_C_P B30 PETP3
NC_PCIE_FW_D2RN F13 PERN4
NC_PCIE_FW_D2RP G13 PERP4
NC_PCIE_FW_R2D_CN B29 PETN4
NC_PCIE_FW_R2D_CP A29 PETP4
USB3_SD_D2R_N G17 PERN1/USB3RN2
USB3_SD_D2R_P F17 PERP1/USB3RP2
USB3_SD_R2D_C_N C30 PETN1/USB3TN2
USB3_SD_R2D_C_P C31 PETP1/USB3TP2
PCIE_CAMERA_D2R_N F15 PERN2/USB3RN3
PCIE_CAMERA_D2R_P G15 PERP2/USB3RP3
PCIE_CAMERA_R2D_C_N B31 PETN2/USB3TN3
PCIE_CAMERA_R2D_C_P A31 PETP2/USB3TP3
NC E15 RSVD
NC E13 RSVD
PP1V05_S0SW_PCH_VCCUSB3PLL → A27 PCH_PCIE_RCOMP
B27 PCIE_IREF

PCI-E
USB

USB2N0 AN8 USB_EXTA_N
USB2P0 AM8 USB_EXTA_P
USB2N1 AR7 USB_EXTB_N
USB2P1 AT7 USB_EXTB_P
USB2N2 AR8 USB_BT_N
USB2P2 AP8 USB_BT_P
USB2N3 AR10 NC_USB_IRN
USB2P3 AT10 NC_USB_IRP
USB2N4 AM15 USB_TPAD_N
USB2P4 AL15 USB_TPAD_P
USB2N5 AM13 TP_USB_5N
USB2P5 AN13 TP_USB_5P
USB2N6 AP11 NC_USB_CAMERAN
USB2P6 AN11 NC_USB_CAMERAP
USB2N7 AR13 NC_USB_SDN
USB2P7 AP13 NC_USB_SDP
(IPD)

USB3RN0 G20 USB3_EXTA_D2R_N
USB3RP0 H20 USB3_EXTA_D2R_P
USB3TN0 C33 USB3_EXTA_R2D_C_N
USB3TP0 B34 USB3_EXTA_R2D_C_P
USB3RN1 E18 USB3_EXTB_D2R_N
USB3RP1 F18 USB3_EXTB_D2R_P
USB3TN1 B33 USB3_EXTB_R2D_C_N
USB3TP1 A33 USB3_EXTB_R2D_C_P

USBRBIAS* AJ10 → PCH_USB_RBIAS
USBRBIAS AJ11
PLACE_NEAR=U0500.AJ10:2.54mm
R1570 22.6 1% 1/20W MF 201

RSVD AN10 NC
RSVD AM10 NC

OC0*/GPIO40 AL3 XDP_USB_EXTA_OC_L
OC1*/GPIO41 AT1 XDP_USB_EXTB_OC_L
OC2*/GPIO42 AH2 XDP_USB_EXTC_OC_L
OC3*/GPIO43 AV3 XDP_USB_EXTD_OC_L

R1500 3.01K 1% 1/20W MF 201
PLACE_NEAR=U0500.A27:2.54mm

USB Port Assignments:

Ext A (LS/FS/HS)

Ext B (LS/FS/HS)

BT

IR

Trackpad

Unused

Reserved: Camera

Reserved: SD (HS)

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
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LPC_AD<0> R1540 33 5% 1/20W MF 201 LPC_AD_R<0>
LPC_AD<1> R1541 33 5% 1/20W MF 201 LPC_AD_R<1>
LPC_AD<2> R1542 33 5% 1/20W MF 201 LPC_AD_R<2>
LPC_AD<3> R1543 33 5% 1/20W MF 201 LPC_AD_R<3>
LPC_FRAME_L R1544 33 5% 1/20W MF 201 LPC_FRAME_R_L

(IPU)
LAD0 AU14
LAD1 AW12
LAD2 AY12
LAD3 AW11
LFRAME* AV12

LPC

SPI_CLK (IPU) AA3
SPI_CS0* (IPU) Y7
SPI_CS1* (IPU) Y4
SPI_CS2* (IPU) AC2
SPI_MOSI (IPU/IPD) AA2
SPI_MISO (IPU) AA4
SPI_IO2 (IPU) Y6
SPI_IO3 (IPU) AF1

SPI

SMBUS

SMBALERT*/GPIO11 AN2 PCH_SMBALERT_L
SMBCLK AP2 SMBUS_PCH_CLK
SMBDATA AH1 SMBUS_PCH_DATA
SML0ALERT*/GPIO60 AL2 WOL_EN
SML0CLK AN1 SML_PCH_0_CLK
SML0DATA AK1 SML_PCH_0_DATA
SML1ALERT*/PCHHOT*/GPIO73 AU4 PCH_SML1ALERT_L
SML1CLK_GPIO75 AU3 SMBUS_SMC_1_S0_SCL
SML1DATA/GPIO74 AH3 SMBUS_SMC_1_S0_SDA

C-LINK

(IPU/IPD) CL_CLK AF2 NC_CLINK_CLK
(IPU/IPD) CL_DATA AD2 NC_CLINK_DATA
CL_RST* AF4 NC_CLINK_RESET_L

SML1ALERT# pull-up not provided on this page, may be wire-ORed into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

PP3V3_SUS
PP3V3_SUS

R1580 100K 5% 1/20W MF 201 XDP_USB_EXTA_OC_L
R1581 100K 5% 1/20W MF 201 XDP_USB_EXTB_OC_L
R1582 100K 5% 1/20W MF 201 XDP_USB_EXTC_OC_L
R1583 100K 5% 1/20W MF 201 XDP_USB_EXTD_OC_L
R1548 1K 5% 1/20W MF 201 SPI_IO<2>
R1549 1K 5% 1/20W MF 201 SPI_IO<3>
R1590 100K 5% 1/20W MF 201 PCH_SMBALERT_L
R1591 100K 5% 1/20W MF 201 WOL_EN

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus

Apple Inc.

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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

PP3V3_S0

RAMCFG3:H	RAMCFG2:H	RAMCFG1:H	RAMCFG0:H
R1631 100K 5% 1/20W MF 201	R1636 100K 5% 1/20W MF 201	R1635 100K 5% 1/20W MF 201	R1611 100K 5% 1/20W MF 201

XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3

GPIO12:

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC

PLT_RESET_L

R1621 100K 5% 1/20W MF 201 → PCH_TBT_PCIE_RESET_L

R1639 100K 5% 1/20W MF 201 → SSD_RESET_L

PP3V3_S0

R1641 1K 5% 1/20W MF 201 — NO STUFF

PP3V3_S5
PP3V3_S3
PP3V3_S0SW_SD
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0
PP3V3_TBTLC

TBTLC for CR, S0 for RR

R1610 100K	XDP_PCH_GPIO76		
R1614 100K	XDP_LPCPLUS_GPIO		
R1615 100K	XDP_PCH_GPIO17		
SD_ON_MLB			
R1616 100K	SD_RESET_L		
R1617 100K	SMC_WAKE_SCI_L		
R1618 100K	TPAD_SPI_INT_L		
R1619 100K	TPAD_USB_IF_EN		
R1620 100K	SSD_PWR_EN		
R1622 100K	HDD_PWR_EN		
R1623 100K	XDP_SDCONN_STATE_CHANGE_L		
R1624 100K	SD_PWR_EN		
R1625 100K	TBT_PWR_EN		
R1626 100K	XDP_JTAG_ISP_TCK		
R1627 100K	XDP_JTAG_ISP_TDI		
R1628 100K	JTAG_TBT_TMS		
R1629 100K	PCH_HSIO_PWR_EN		
R1630 100K	TPAD_SPI_IF_EN		
NO STUFF			
R1632 100K	SPIROM_USE_MLB		
R1633 100K	CAMERA_PWR_EN_PCH		
R1634 100K	FW_PWR_EN		
R1637 100K	SSD_DEVSLP		
R1638 100K	AP_S0IX_WAKE_SEL		
R1640 100K	FW_PME_L		
R1652 10K	LPC_SERIRQ		
R1670 100K	JTAG_ISP_TDO		
R1691 100K	BT_PWRRST_L		
R1693 100K	ENET_MEDIA_SENSE		
R1694 100K	LCD_IRQ_L		
R1695 100K	LCD_PSR_EN		

R1616 should also be stuffed if platform does not use SD card

CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-1SP
SYM 10 OF 19

XDP_PCH_GPIO76	P1	BMBUSY*/GPIO76
XDP_MLB_RAMCFG0	AU2	GPIO8
TBT_GO2SX_BIDIR	AM7	LAN_PHY_PWR_CTRL/GPIO12
TP_MEM_VDD_SEL_1V5_L	AD6	GPIO15 (IPD-RSMRST#)
XDP_LPCPLUS_GPIO	Y1	GPIO16
XDP_PCH_GPIO17	T3	GPIO17
SD_RESET_L	AD5	GPIO24
SMC_WAKE_SCI_L	AN5	GPIO27 (IPD-DeepSx)
TPAD_SPI_INT_L	AD7	GPIO28
TPAD_USB_IF_EN	AN3	GPIO26
SSD_PWR_EN	AG6	GPIO56
PCH_TBT_PCIE_RESET_L	AP1	GPIO57
HDD_PWR_EN	AL4	GPIO58
XDP_SDCONN_STATE_CHANGE_L	AT5	GPIO59
SD_PWR_EN	AK4	GPIO44
TBT_PWR_EN	AB6	GPIO47
XDP_JTAG_ISP_TCK	U4	GPIO48
XDP_JTAG_ISP_TDI	Y3	GPIO49
JTAG_TBT_TMS	P3	GPIO50
PCH_HSIO_PWR_EN	Y2	HSIOPC/GPIO71
TPAD_SPI_IF_EN	AT3	GPIO13
XDP_MLB_RAMCFG3	AH4	GPIO14
SPIROM_USE_MLB	AM4	GPIO25
CAMERA_PWR_EN_PCH	AG5	GPIO45
FW_PWR_EN	AG3	GPIO46
XDP_MLB_RAMCFG1	AM3	GPIO9
XDP_MLB_RAMCFG2	AM2	GPIO10
SSD_DEVSLP	P2	DEVSLP0*/GPIO33
AP_S0IX_WAKE_SEL	C4	SDIO_POWER_EN/GPIO70
SSD_RESET_L	L2	DEVSLP1*/GPIO38
FW_PME_L	N5	DEVSLP2*/GPIO39
PCH_TCO_TIMER_DISABLE	V2	SPKR/GPIO81 (IPD-PLTRST#)

CPU/MISC

THRMTRIP*	D60	PM_THRMTRIP_L
RCIN*/GPIO82	V4	TBT_CIO_PLUG_EVENT
SERIRQ	T4	LPC_SERIRQ
PCH_OPI_COMP	AW15	PCH_OPI_COMP
RSVD	AF20	NC
RSVD	AB21	NC

GPIO / LPIO

GSPI0_CS*/GPIO83	R6	PCH_GSPI0_CS_L
GSPI0_CLK/GPIO84	L6	PCH_GSPI0_CLK
GSPI0_MISO/GPIO85 (IPD)	N6	PCH_GSPI0_MISO
GSPI0_MOSI/GPIO86 (IPD-PLTRST#)	L8	PCH_GSPI0_MOSI
GSPI1_CS*/GPIO87	R7	TPAD_SPI_CS_L
GSPI1_CLK/GPIO88	L5	TPAD_SPI_CLK
GSPI1_MISO/GPIO89 (IPD)	N7	TPAD_SPI_MISO
GSPI_MOSI/GPIO90	K2	TPAD_SPI_MOSI
UART0_RXD/GPIO91	J1	AP_S0IX_WAKE_L
UART0_TXD/GPIO92	K3	HDMITBTMUX_FLAG_L
UART0_RTS*/GPIO93	J2	JTAG_ISP_TDO
UART0_CTS*/GPIO94	G1	AP_RESET_L
UART1_RXD/GPIO0	K4	PCH_UART1_RXD
UART1_TXD/GPIO1	G2	PCH_UART1_TXD
UART1_RST*/GPIO2	J3	PCH_UART1_RTS_L
UART1_CTS*/GPIO3	J4	PCH_UART1_CTS_L
I2C0_SDA/GPIO4	F2	PCH_I2C0_SDA
I2C0_SCL/GPIO5	F3	PCH_I2C0_SCL
I2C1_SDA/GPIO6	G4	PCH_I2C1_SDA
I2C1_SCL/GPIO7	F1	PCH_I2C1_SCL
SDIO_CLK/GPIO64	E3	TBT_POC_RESET_L
SDIO_CMD/GPIO65	F4	BT_PWRRST_L
SDIO_D0/GPIO66 (IPD-PLTRST#)	D3	PCH_STRP_TOPBLK_SWP_L
SDIO_D1/GPIO67	E4	ENET_MEDIA_SENSE
SDIO_D2/GPIO68	C3	LCD_IRQ_L
SDIO_D3/GPIO69	E2	LCD_PSR_EN

PP1V05_S0

R1650 1K 5% 1/20W MF 201 → PM_THRMTRIP_L

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

PLACE_NEAR=U0500.AW15:2.54mm
R1655 49.9 1% 1/20W MF 201

PLT_RESET_L
R1671 100K 5% 1/20W MF 201

Pull-up on TBT page

Requires connection to SMC via 1K series R

PP3V3_S0

PCH_GSPI0_CS_L	R1660 100K	TPAD_SPI_CS_L	R1664 47K
PCH_GSPI0_CLK	R1661 100K	TPAD_SPI_CLK	R1665 47K
PCH_GSPI0_MISO	R1662 100K	TPAD_SPI_MISO	R1666 47K
PCH_GSPI0_MOSI	R1663 100K	TPAD_SPI_MOSI	R1667 47K
AP_S0IX_WAKE_L	R1668 100K	PCH_UART1_RXD	R1672 100K
HDMITBTMUX_FLAG_L	R1669 100K	PCH_UART1_TXD	R1673 100K
PCH_UART1_RTS_L	R1674 100K	PCH_UART1_CTS_L	R1675 100K
PCH_I2C0_SDA	R1676 100K	PCH_I2C1_SDA	R1678 100K
PCH_I2C0_SCL	R1677 100K	PCH_I2C1_SCL	R1679 100K

All: 5% 1/20W MF 201

SYNC_MASTER=J41_MLB SYNC_DATE=04/02/2013

PAGE TITLE: PCH GPIO/MISC/LPIO

Apple Inc.

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Extra BPM Testpoints

XDP_BPM_L<2> — TP1802
XDP_BPM_L<3> — TP1803
XDP_BPM_L<4> — TP1804
XDP_BPM_L<5> — TP1805
XDP_BPM_L<6> — TP1806
XDP_BPM_L<7> — TP1807

(TP-P6)

Merged (CPU/PCH) Micro2-XDP

PP1V05_S0

R1830 150 5% 1/16W MF-LF 402

CRITICAL XDP_CONN J1800 DF40RC-60DP-0.4V M-ST-SM1

518S0847

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
VCC_OBS_AB	HOOK2	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK3	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK		DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	
	TCK0	TMS	
		XDP_PRESENT#	

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

PP1V05_S0 — XDP_CPU_TDO — R1810 51 — XDP — PLACE_NEAR=U0500.F62:28mm
PP1V05_S0 — XDP_CPU_TCK — R1813 51 — XDP — PLACE_NEAR=U0500.E60:28mm

TDI and TMS are terminated in CPU.

CPU_VCCST_PWRGD — R1800 1K — XDP — PLACE_NEAR=U0500.C61:2.54mm
PM_PWRBTN_L — R1802 0 — XDP — PLACE_NEAR=U5000.J3:2.54mm
PM_PCH_SYS_PWROK — R1804 0 — XDP — 5% 1/16W MF-LF 402
XDP_CPU_TCK
PCH_JTAGX — R1835 0 — XDP — 5% 1/20W MF 0201 — PLACE_NEAR=J1800.58:28mm

C1804 0.1UF 10V X5R-CERM 0201 — XDP
R1831 1K 5% 1/16W MF-LF 402 — XDP
C1800 0.1UF 10V X5R-CERM 0201 — XDP
C1801 0.1UF 10V X5R-CERM-X5R 0201 — XDP
C1806 0.1UF 10V X5R-CERM-X5R 0201 — XDP

XDP_CPU_PRESENT_L

R1805 1K — XDP — PLT_RESET_L — PLACE_NEAR=U0500.AG7:2.54mm

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
XDP_CPU_TDO — PLACE_NEAR=J1800.51:28mm
XDP_CPUPCH_TRST_L — MAKE_BASE=TRUE
XDP_CPU_TDI — PLACE_NEAR=J1800.55:28mm
XDP_CPU_TMS — PLACE_NEAR=J1800.57:28mm

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563
CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563
CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563
CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0	TP1870	
XDP_USB_EXTA_OC_L		XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L		XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	TP1873	
XDP_USB_EXTD_OC_L	TP1874	
XDP_SDCONN_STATE_CHANGE_L		XDP_SDCONN_STATE_CHANGE_L
XDP_MLB_RAMCFG1	TP1876	
XDP_MLB_RAMCFG2	TP1877	
XDP_MLB_RAMCFG3	TP1878	
XDP_JTAG_ISP_TCK		XDP_JTAG_ISP_TCK
XDP_SSD_PCIE3_SEL_L	R1881 1K	
XDP_SSD_PCIE2_SEL_L	R1882 1K	NOTE: Must not short XDP pins together!
XDP_SSD_PCIE1_SEL_L	R1883 1K	
XDP_SSD_PCIE0_SEL_L	R1884 1K	SSD_PCIE_SEL_L
XDP_LPCPLUS_GPIO		XDP_LPCPLUS_GPIO
XDP_PCH_GPIO17	TP1886	
XDP_PCH_GPIO76	TP1887	
XDP_JTAG_ISP_TDI		XDP_JTAG_ISP_TDI

Unused & MLB_RAMCFGx GPIOs have TPs.
USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.
NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.
SSD_PCIEx_SEL_L straps are connected via 1K to common net.
LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
C1845 0.1UF 10V X5R-CERM 0201
U1845 74LVC1G07GF SOT891
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

PCH_JTAGX	R1899 1K	NO STUFF
XDP_PCH_TDO	R1890 51	XDP
XDP_PCH_TDI	R1891 51	XDP
XDP_PCH_TMS	R1892 51	XDP
XDP_PCH_TCK	R1896 51	NO STUFF
XDP_CPUPCH_TRST_L	R1897 51	NO STUFF

5% 1/20W MF 201 — PLACE_NEAR=U0500.AG63:28mm / AE61:28mm / AG61:28mm / AG62:28mm / AG62:28mm / AG62:28mm

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System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5

This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042)

No bypass necessary

GreenCLK 25MHz Power Must be powered if any VDDIO is powered. — PP3V3_S5RS3RS0_SYSCLKGEN

CAM XTAL Power — PP1V2_CAM_XTALPCIEVDD

TBT XTAL Power — PP3V3_TBTLC

C1924 0.1UF 10% 16V X5R-CERM 0201
C1922 0.1UF 10% 16V X5R-CERM 0201
C1902 1UF 20% 6.3V X5R 0201

CKPLUS_WAIVE=PwrTerm2Gnd

U1900 SLG3NB148CV TOFN CRITICAL
NC, VDD, VG3HOT

VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

C1905 12PF 5% 25V NP0-C0G-CERM 0201
C1906 12PF 5% 25V NP0-C0G-CERM 0201
Y1905 CRITICAL 25.000MHZ-12PF-20PPM SM-3.2X2.5MM
R1905 0 5% 1/20W MF 0201 — NO STUFF
R1906 1M 5% 1/20W MF 201

SYSCLK_CLK25M_X2 → SYSCLK_CLK25M_X2_R
SYSCLK_CLK25M_X1

NOTE: 30 PPM or better required for RTC accuracy

VIOE_25M_A, VIOE_25M_B, VIOE_25M_C
32.768K → PCH_CLK32K_RTCX1
25M_A NC
25M_B → SYSCLK_CLK25M_CAMERA
25M_C → SYSCLK_CLK25M_TBT
VOUT → PPVRTC_G3H
GND, THRM PAD

C1910 1UF 20% 6.3V X5R 0201 — For SB RTC Power

NC_RTC_CLK32K_RTCX2 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_RTC_CLK32K_RTCX2

PCH Reset Button

PP3V3_S0
R1995 10K 5% 1/20W MF 201
XDP
R1996 0 5% 1/20W MF 0201
XDP_DBRESET_L → PM_SYSRST_L
NO STUFF
R1997 0 5% 1/16W MF-LF 402
SILK_PART=SYS RESET

Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

PP1V2_S3
C1970 0.1UF 10% 16V X5R-CERM 0201
U1970 74AUP1G07GF SOT891
R1970 330K 5% 1/20W MF 201
PP3V3_S0

TPS51916 I(leak) = +/- 1uA, Vih(min) = 1.8V
33uW when driven-low

CPU_MEMVTT_PWR_EN_LSVDDQ
MEMVTT_PWR_EN — MAKE_BASE=TRUE
MEMVTT_PWR_EN

PCH ME Disable Strap

PP5V_S0
R1920 100K 5% 1/20W MF 201
Q1920 DMN5L06VK-7 SOT-563
PP1V5_S0SW_AUDIO_HDA
SPI_DESCRIPTOR_OVERRIDE_LS5V
SPI_DESCRIPTOR_OVERRIDE
R1921 1K 5% 1/20W MF 201
HDA_SDOUT_R — IPD = 9-50k
SPI_DESCRIPTOR_OVERRIDE_L

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

PCH 24MHz Crystal

C1915 6.8PF +/-0.1PF 25V C0G 0201
C1916 6.8PF +/-0.1PF 25V C0G 0201
Y1915 CRITICAL 24.000MHZ-20PPM-6PF 3.20X2.50MM-SM1
R1915 0 5% 1/20W MF 0201
R1916 1M 5% 1/20W MF 201

PCH_CLK24M_XTALOUT_R → PCH_CLK24M_XTALOUT
PCH_CLK24M_XTALIN

PCH 24MHz Outputs

LPC_CLK24M_SMC_R — PLACE_NEAR=U0500.AN15:5.1mm
R1927 22 5% 1/20W MF 201
LPC_CLK24M_SMC — MAKE_BASE=TRUE → LPC_CLK24M_SMC

LPC_CLK24M_LPCPLUS_R — PLACE_NEAR=U0500.AP15:5.1mm
R1926 22 5% 1/20W MF 201
LPC_CLK24M_LPCPLUS

VCCST (1.05V S0) PWRGD

PP3V3_S5
C1930 0.1UF 10% 16V X5R-CERM 0201
U1930 CRITICAL 74AUP1G09 SOT891
R1931 10K 5% 1/20W MF 201
PP1V05_S0

ALL_SYS_PWRGD
PM_SLP_S3_L
CPU_VCCST_PWRGD

PCH PWROK Generation

PP3V42_G3H
PP3V3_S0
BYPASS=U1950:5MM
C1950 0.1UF 10% 16V X5R-CERM 0201

CPU_VR_EN
R1955 10K 5% 1/20W MF 201
NO STUFF
R1951 0 5% 1/20W MF 0201
CPU_VR_READY — MAKE_BASE=TRUE
CPU_VR_READY

R1950 10K 5% 1/20W MF 201
ALL_SYS_PWRGD → CPUVR_PGOOD_R
U1950 74LVC2G08GT SOT833
PM_S0_PGOOD

NO STUFF WF: Do we need this?
R1963 0 5% 1/20W MF 0201
R1960 0 5% 1/20W MF 0201
CKPLUS_WAIVE=UNCONNECTED_PINS
U1950 74LVC2G08GT SOT833
SYS_PWROK_R
CKPLUS_WAIVE=UNCONNECTED_PINS

NO STUFF
R1961 100K 5% 1/20W MF 201

R1962 1K 5% 1/20W MF 201
PM_PCH_SYS_PWROK

PM_PCH_PWROK — MAKE_BASE=TRUE
PM_PCH_PWROK

SMC_DELAYED_PWRGD

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Platform Reset Connections

Unbuffered

PLT_RESET_L (IN) → LPCPLUS_RESET_L (OUT)
- R2081 33 5% 1/10W MF 201

PLT_RESET_L (IN) → PCA9557D_RESET_L (OUT)
- R2071 0 5% 1/20W MF 0201

Scrub for Layout Optimization

Buffered

PP3V3_S0 → U2071 CRITICAL MC74VHC1G08 SC70-HF
- C2071 0.1UF 10% 16V X5R-CERM 0201
- R2070 100K 5% 1/20W MF 201

PLT_RST_BUF_L (OUT) →
- R2072 0 5% 1/20W MF 0201 → SMC_LRESET_L (OUT)
- R2088 0 5% 1/20W MF 0201 → BKLT_PLT_RST_L (OUT)
- R2089 0 5% 1/20W MF 0201 → CAM_PCIE_RESET_L (OUT)

PCH_TBT_PCIE_RESET_L (IN) → PCH_TBT_PCIE_RESET_L (OUT)
MAKE_BASE=TRUE

GreenCLK 25MHz Power

PP3V3_S3 →
- R2040 0 5% 1/20W MF 0201 (NO STUFF) → PP3V3_S5RS3RS0_SYSCLKGEN
- R2041 0 5% 1/20W MF 0201 (NO STUFF) ← PP3V3_S0

PP3V3_S5RS3RS0_SYSCLKGEN
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

R2041/2 should be stuffed for GreekCLK A or B depending on S2 rail

R2042 should be stuffed for GreenCLK C

PP3V3_S5 →
- R2042 0 5% 1/20W MF 0201

DDC Pull-Ups

2.2k pull-ups are required by PCH to indicate active display interface.

DP++ spec violation, should remove!

PP3V3_S0
- R2020 2.2K 5% 1/20W MF 201 (NO STUFF)
- R2021 2.2K 5% 1/20W MF 201
- R2022 2.2K 5% 1/20W MF 201 (NO STUFF)
- R2023 2.2K 5% 1/20W MF 201

DP_TBTSNK0_DDC_CLK
DP_TBTSNK0_DDC_DATA
DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA

TBTSNK1_DDC is pulled-up just to indicate that DP port is used. No DDC on this port, AUX-only.

NOTE: Only DDC_DATA is sensed by PCH, so DDC_CLK pull-ups are unstuffed.

Thunderbolt Pull-up/downs

Cactus Ridge GO2SX signal pulled-up to SUS rail

PP3V3_SUS
- R2013 10K 5% 1/20W MF 201

TBT_GO2SX_BIDIR (BI) — MAKE_BASE TRUE — TBT_GO2SX_BIDIR (BI)

Cactus Ridge PLUG_EVENT is active-high, always driven (pull-down)

TBT_CIO_PLUG_EVENT (OUT) — TRUE — TBT_CIO_PLUG_EVENT (IN)

Required for unused second TBT port

TBT_B_CIO_SEL (IN)
DP_TBTPB_HPD (OUT)
TBT_B_CONFIG2_RC (OUT)
TBT_B_CONFIG1_BUF (OUT)
TBT_B_LSRX
- R2015 100K 5% 1/20W MF 201
- R2016 10K 5% 1/20W MF 201
- R2017 10K 5% 1/20W MF 201
- R2018 10K 5% 1/20W MF 201
- R2019 10K 5% 1/20W MF 201
- R2014 10K 5% 1/20W MF 201

Power State Debug LEDs

(For development only)

PP3V3_S5 → PP3V3_S5_DBGLED
PLACE_SIDE=BOTTOM
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=3.3V
- R2094 0 5% 1/10W MF-LF 402

DBGLED_S5	DBGLED_S4	DBGLED_S3	DBGLED_S0I3	DBGLED_S0	
R2090 20K 5% 1/20W MF 201	R2091 20K 5% 1/20W MF 201	R2092 20K 5% 1/20W MF 201	R2093 20K 5% 1/20W MF 201	R2095 20K 5% 1/20W MF 201	
D2090 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S5_ON	D2091 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S4_ON	D2092 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S3_ON	D2093 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S0I3_ON	D2095 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S0_ON	
DBGLED_S4_D	DBGLED_S3_D	DBGLED_S0I3_D	DBGLED_S0_D		
Q2090 DMN5L06VK-7 SOT-563	Q2090 DMN5L06VK-7 SOT-563	Q2091 DMN5L06VK-7 SOT-563	Q2091 DMN5L06VK-7 SOT-563		

S4_PWR_EN (IN)
PM_SLP_S4_L (IN)
PM_SLP_S3_L (IN)
PM_SLP_S0_L (IN)

RAM Configuration Straps

Pull-downs for chip-down RAM systems

XDP_MLB_RAMCFG0 (OUT)
XDP_MLB_RAMCFG1 (OUT)
XDP_MLB_RAMCFG2 (OUT)
XDP_MLB_RAMCFG3 (OUT)

RAMCFG3:L	RAMCFG2:L	RAMCFG1:L	RAMCFG0:L
R2050 10K 5% 1/20W MF 201	R2051 10K 5% 1/20W MF 201	R2052 10K 5% 1/20W MF 201	R2053 10K 5% 1/20W MF 201

LPDDR3 Alias Support

TP_CPU_MEM_RESET_L (IN) — MAKE_BASE=TRUE — TP_CPU_MEM_RESET_L
TP_MEM_VDD_SEL_1V5_L (IN) — MAKE_BASE=TRUE — TP_MEM_VDD_SEL_1V5_L
PP0V6_S3_MEM_VREFDQ_A — MAKE_BASE=TRUE VOLTAGE=0.6V — PP0V6_S3_MEM_VREFDQ_A
PP0V6_S3_MEM_VREFCA_A — MAKE_BASE=TRUE VOLTAGE=0.6V — PP0V6_S3_MEM_VREFCA_A
PP0V6_S3_MEM_VREFDQ_B — MAKE_BASE=TRUE VOLTAGE=0.6V — PP0V6_S3_MEM_VREFDQ_B
PP0V6_S3_MEM_VREFCA_B — MAKE_BASE=TRUE VOLTAGE=0.6V — PP0V6_S3_MEM_VREFCA_B

TBT Aliases

MAKE_BASE

DP_TBTSNK0_DDC_CLK (IN) — TRUE — DP_TBTSNK0_DDC_CLK (OUT)
DP_TBTSNK0_DDC_DATA (BI) — TRUE — DP_TBTSNK0_DDC_DATA (BI)

MAKE_BASE

DP_TBTSNK1_HPD (OUT) — TRUE — DP_TBTSNK1_HPD (IN)
=DP_TBTSNK1_ML_C_P<3..0> (IN) — TRUE — DP_TBTSNK1_ML_C_P<3..0> (OUT)
=DP_TBTSNK1_ML_C_N<3..0> (IN) — TRUE — DP_TBTSNK1_ML_C_N<3..0> (OUT)
DP_TBTSNK1_AUXCH_C_P (BI) — TRUE — DP_TBTSNK1_AUXCH_C_P (BI)
DP_TBTSNK1_AUXCH_C_N (BI) — TRUE — DP_TBTSNK1_AUXCH_C_N (BI)
DP_TBTSNK1_DDC_CLK (IN) — TRUE — DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA (BI) — TRUE — DP_TBTSNK1_DDC_DATA

Single-port TBT implementation does not require DDC Crossbar

MAKE_BASE MAKE_BASE

JTAG_ISP_TDO (OUT) — TRUE — JTAG_ISP_TDO (IN)
XDP_JTAG_ISP_TCK (IN) — XDP_JTAG_ISP_TCK (OUT)
XDP_JTAG_ISP_TDI (IN) — XDP_JTAG_ISP_TDI (OUT)
JTAG_TBT_TMS (IN) — TRUE — JTAG_TBT_TMS (OUT)

No MAKE_BASE on TCK/TDI as these are provided on XDP page.

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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining

CPU_DIMMA_VREFDQ
CPU_DIMMB_VREFDQ
CPU_DIMM_VREFCA

CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

CPU MEM VREFDQ A ISOL
CPU MEM VREFDQ B ISOL
CPU MEM VREFCA A ISOL
CPU MEM VREFCA B ISOL

DDRVREF_DAC R2225 100K 5% 1/20W MF 201 — VREFMRGN_DQ_A_EN_RC
DDRVREF_DAC R2201 100K 5% 1/20W MF 201
DDRVREF_DAC C2225 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
Q2225 pin 6: PLACE_NEAR=Q2220.6:2.54mm

DDRVREF_DAC R2245 100K — VREFMRGN_DQ_B_EN_RC
DDRVREF_DAC R2202 100K
DDRVREF_DAC C2245 0.1UF
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
Q2265 pin 6: PLACE_NEAR=Q2260.6:2.54mm

DDRVREF_DAC R2265 100K — VREFMRGN_CA_A_EN_RC
DDRVREF_DAC R2215 100K
DDRVREF_DAC C2265 0.1UF
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563

DDRVREF_DAC R2285 100K — VREFMRGN_CA_B_EN_RC
DDRVREF_DAC R2207 100K
DDRVREF_DAC C2285 0.1UF
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
R22x6 pin 2:
PLACE_NEAR=Q2225.1:2.54mm
PLACE_NEAR=Q2265.1:2.54mm
PLACE_NEAR=Q2225.4:2.54mm
PLACE_NEAR=Q2265.4:2.54mm

(All 4 R's) DDRVREF_DAC
R2226 4.02K 1% 1/20W MF 201 — VREFMRGN_DQ_A_RDIV
R2246 4.02K — VREFMRGN_DQ_B_RDIV
R2266 4.02K — VREFMRGN_CA_A_RDIV
R2286 4.02K — VREFMRGN_CA_B_RDIV

VRef Dividers

Always used, regardless of margining option.

PP1V2_S3

R2223 10 1% 1/20W MF 201 — PLACE_NEAR=Q2220.6:2mm
C2220 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFDQ_A_RC
R2221 8.2K 1% 1/20W MF 201 — PLACE_NEAR=Q2220.6:3mm
R2222 8.2K — PLACE_NEAR=R2221.2:1mm
R2220 24.9 — PLACE_NEAR=Q2220.6:2.54mm
PP0V6_S3_MEM_VREFDQ_A MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm

R2243 10 — PLACE_NEAR=Q2260.6:2mm
C2240 0.022UF — MEM_VREFDQ_B_RC
R2241 8.2K — PLACE_NEAR=Q2260.6:3mm
R2242 8.2K — PLACE_NEAR=R2241.2:1mm
R2240 24.9 — PLACE_NEAR=Q2240.6:2.54mm
PP0V6_S3_MEM_VREFDQ_B MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm

R2263 10 — PLACE_NEAR=Q2220.3:2mm
C2260 0.022UF — MEM_VREFCA_A_RC
R2261 8.2K — PLACE_NEAR=Q2220.3:3mm
R2262 8.2K — PLACE_NEAR=R2261.2:1mm
R2260 24.9 — PLACE_NEAR=Q2260.6:2.54mm
PP0V6_S3_MEM_VREFCA_A MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm

R2283 10 — PLACE_NEAR=Q2260.3:2mm
C2280 0.022UF — MEM_VREFCA_B_RC
R2281 8.2K — PLACE_NEAR=Q2260.3:3mm
R2282 8.2K — PLACE_NEAR=R2281.2:1mm
R2280 24.9 — PLACE_NEAR=Q2280.6:2.54mm
PP0V6_S3_MEM_VREFCA_B MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

PP3V3_S3
OMIT R2218 SHORT
PP3V3_S3_VREFMRGN_DAC MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC

U2200 DAC5574 MSOP
SMBUS_PCH_CLK — SCL
SMBUS_PCH_DATA — SDA
Addr=0x98(WR)/0x99(RD)
VOUTA — VREFMRGN_DQ_A
VOUTB — VREFMRGN_DQ_B
VOUTC — VREFMRGN_CA_AB
VOUTD — VREFMRGN_MEMVREG

NOTE: MEMVREG and SPARE share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
R2200 100K 5% 1/20W MF 201

U2201 PCA9557 QFN (OD)
Addr=0x30(WR)/0x31(RD)
SMBUS_PCH_CLK
SMBUS_PCH_DATA
P0 — VREFMRGN_CPU_EN
P1 — VREFMRGN_DQ_A_EN
P2 — VREFMRGN_DQ_B_EN
P3 — VREFMRGN_CA_A_EN
P4 — VREFMRGN_CA_B_EN
P5 — VREFMRGN_MEMVREG_EN
P6 — VREFMRGN_SPARE_EN
P7 — NC
RESET* — PCA9557D_RESET_L
THRM PAD, GND

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PP3V3_S3
DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R2214 38.3K 1% 1/20W MF 201 — DDRREG_FB — PLACE_NEAR=R7415.2:1mm

DDRVREF_DAC R2213 100K
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_SPARE_BUF
DDRVREF_DAC R2217 1M
Pins B1 & B4: CKPLUS_WAIVE=unconnected_pins

DDRVREF_DAC R2212 100K

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output	3.53mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=J41_MLB SYNC_DATE=02/12/2013

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

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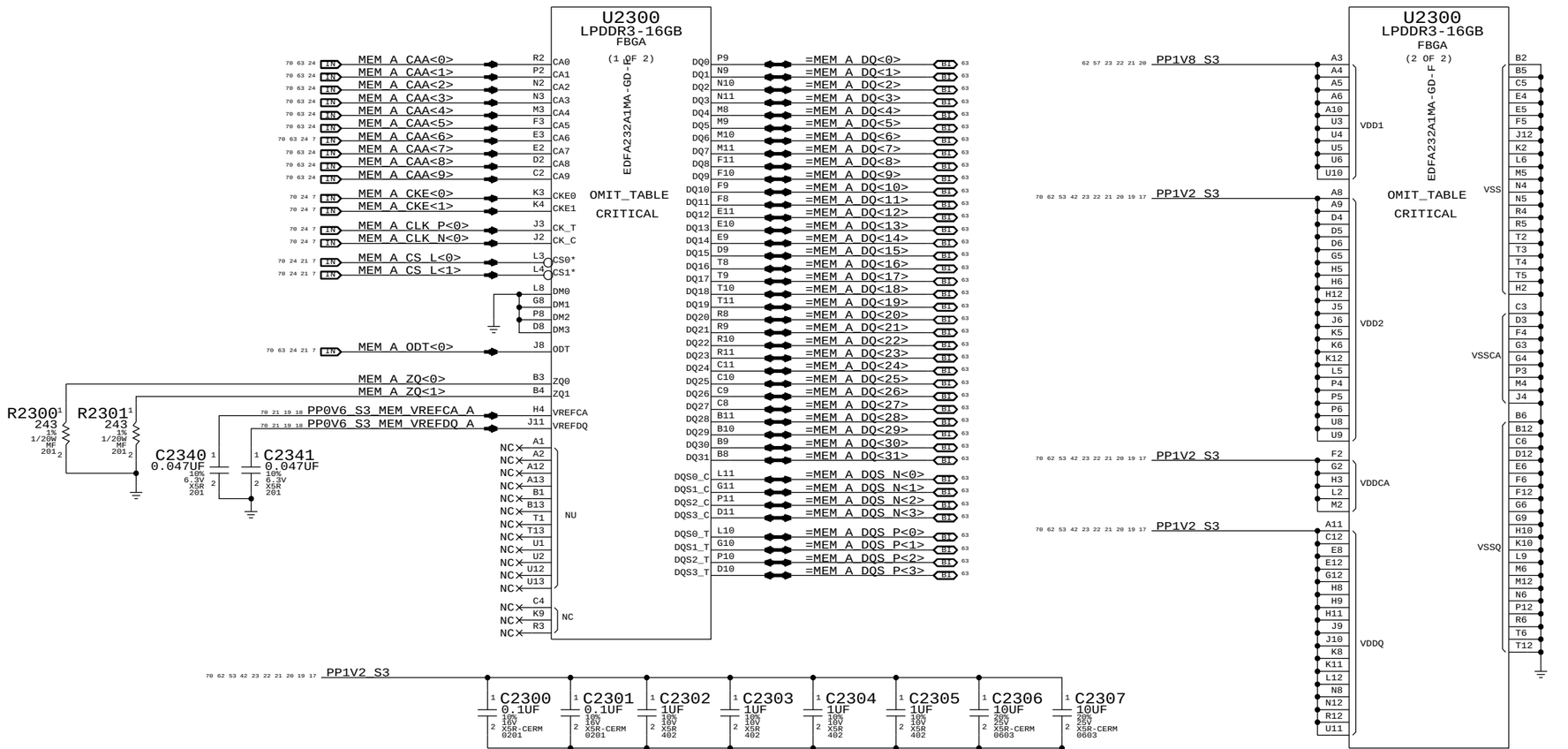
LPDDR3 CHANNEL A (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
LPDDR3 DRAM Channel A (0-31)

Apple Inc.

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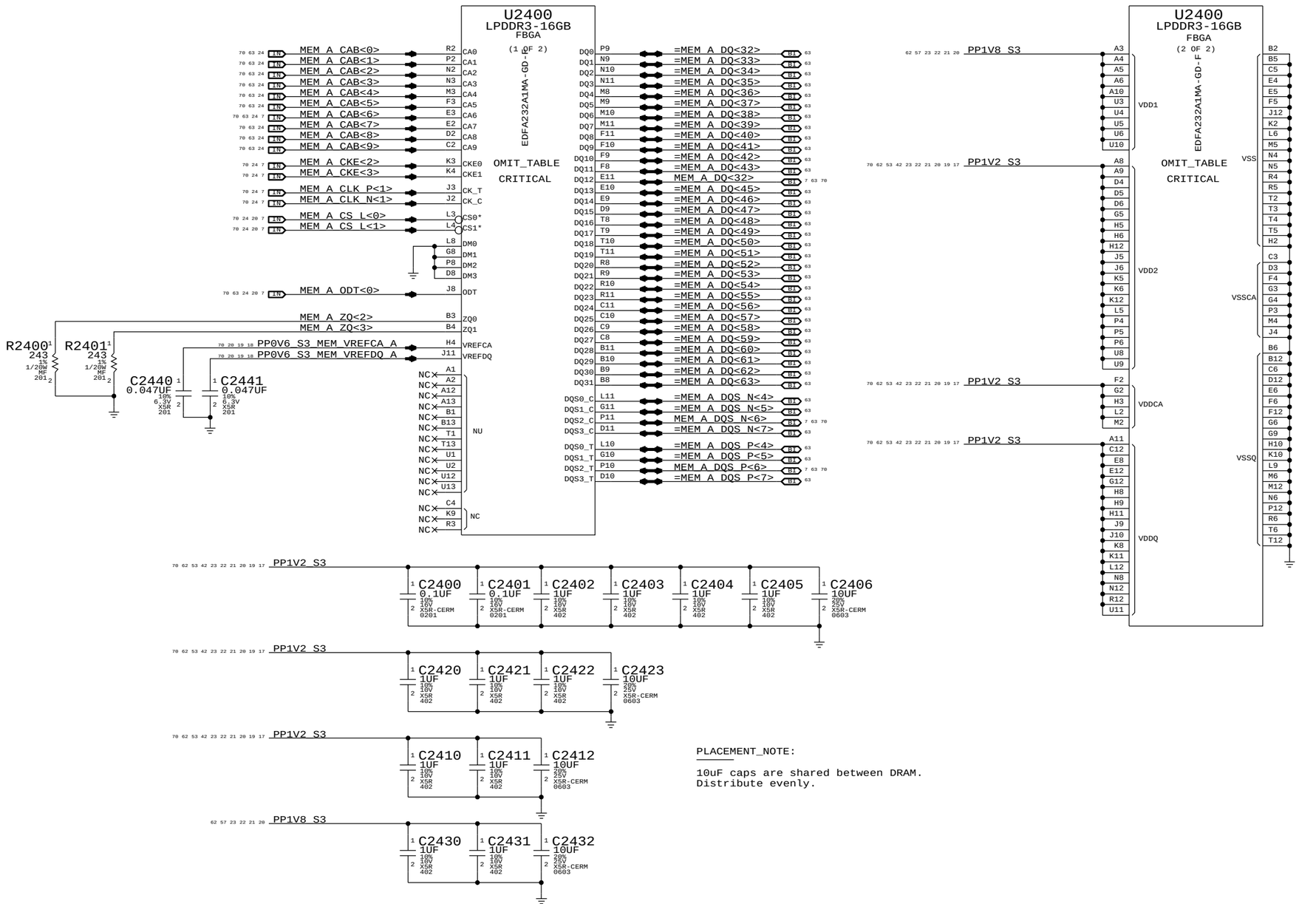
LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

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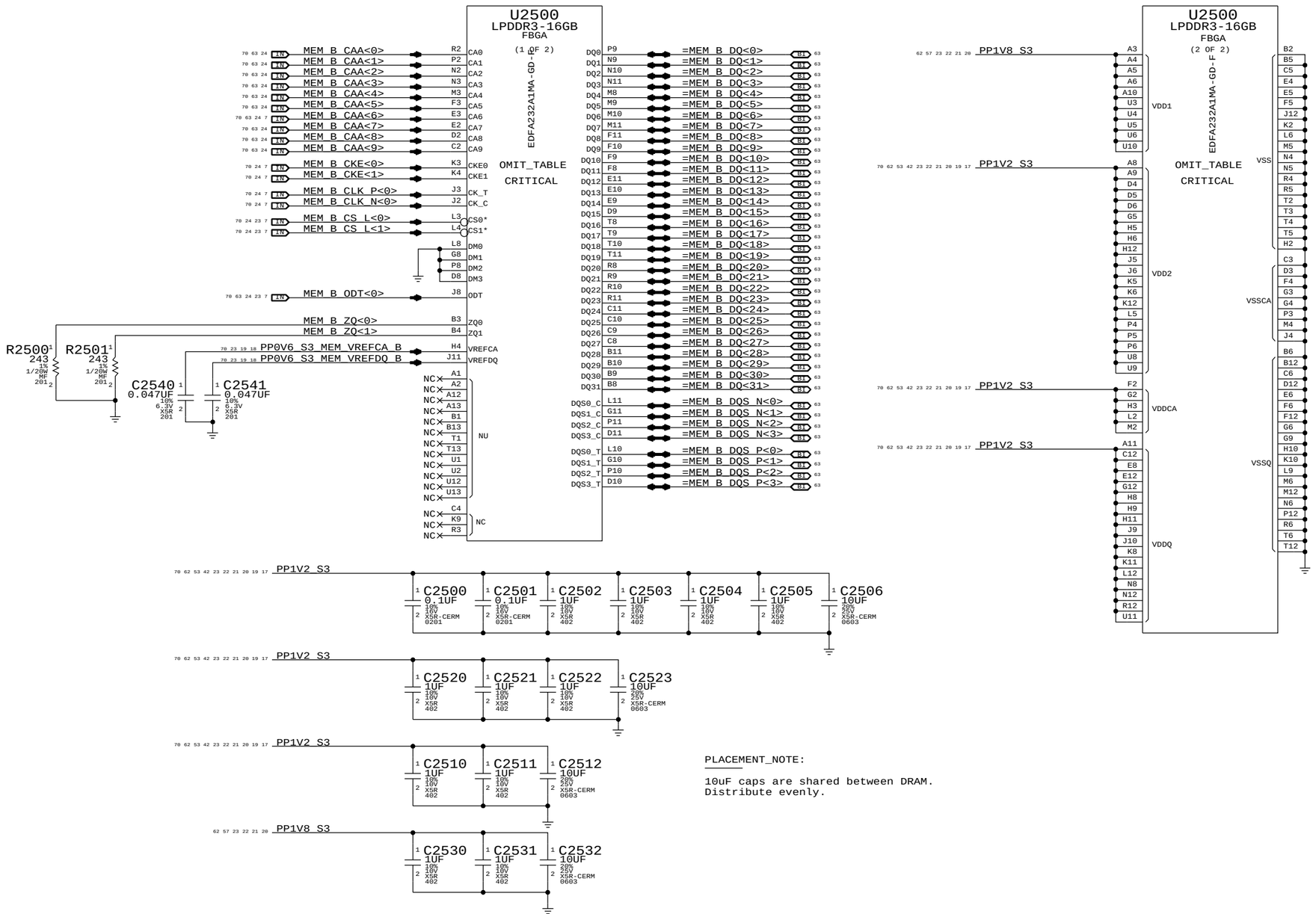
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
LPDDR3 DRAM Channel B (0-31)

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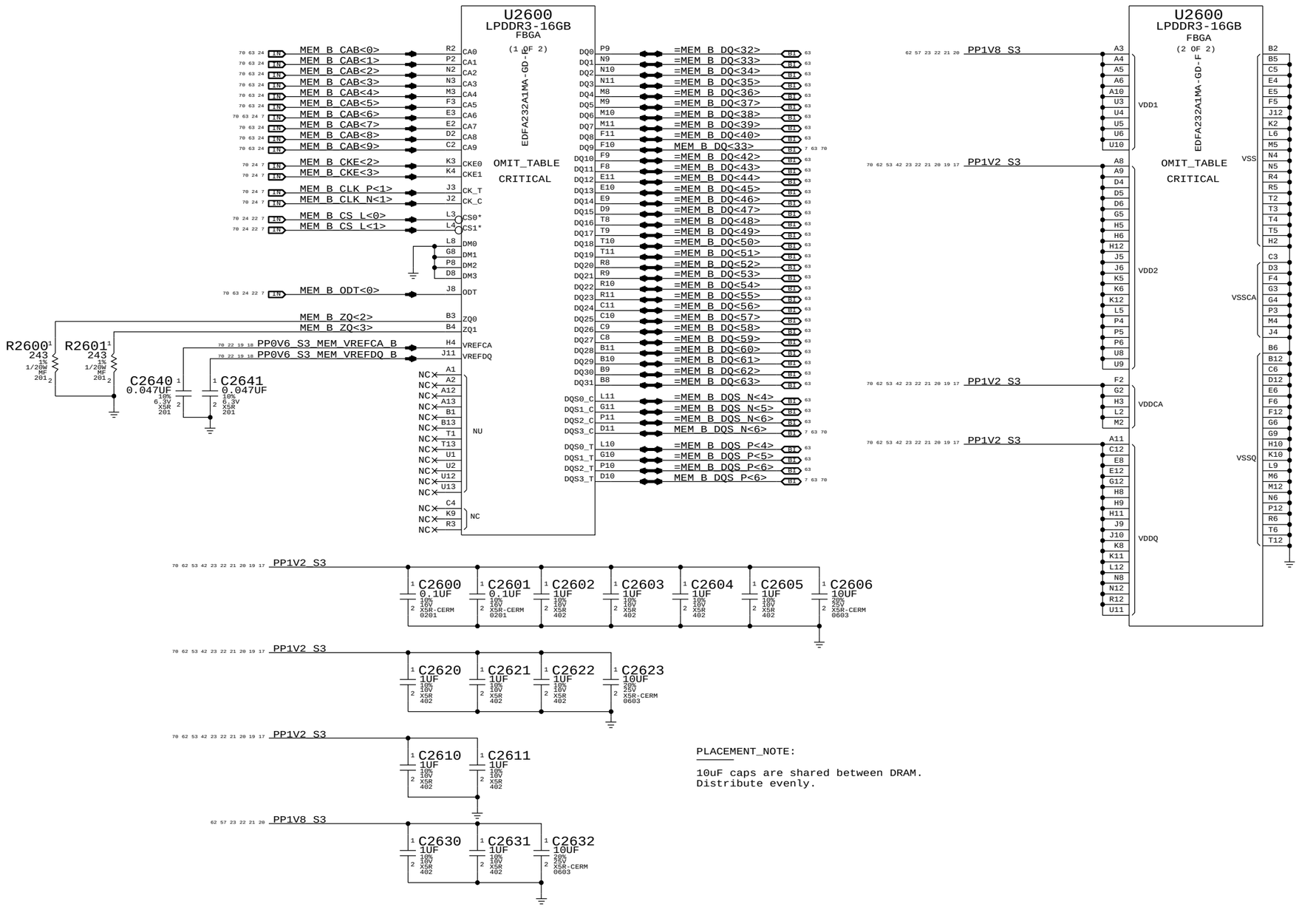
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
LPDDR3 DRAM Channel B (32-63)

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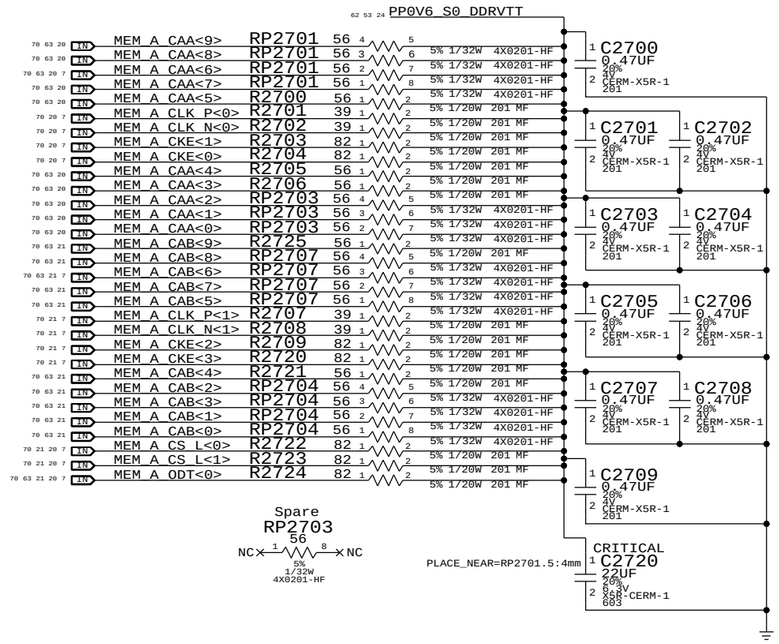
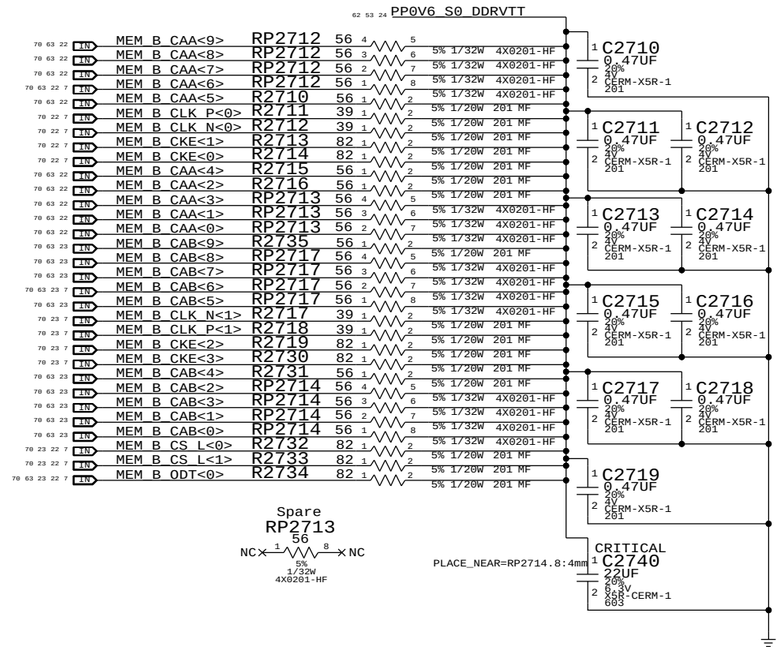
Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/KE, 38 Ohm for CLK





SYNC_MASTER=J41_MLB	SYNC_DATE=02/06/2013
PAGE TITLE	LPDDR3 DRAM Termination
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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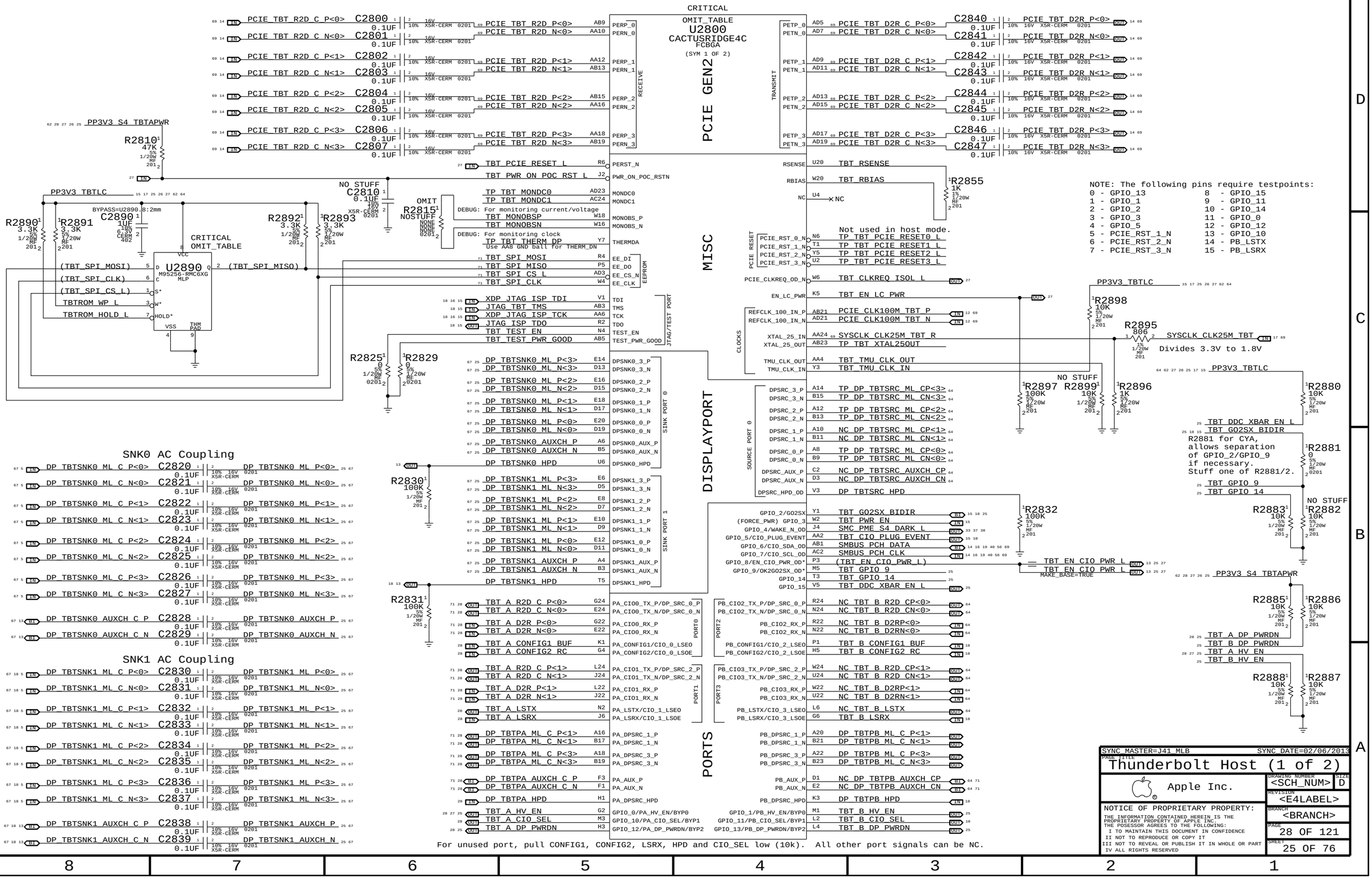
CRITICAL
OMIT_TABLE
U2800
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)
PCIE GEN2
RECEIVE
TRANSMIT
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_P<0>
PCIE_TBT_R2D_N<0>
PCIE_TBT_R2D_P<1>
PCIE_TBT_R2D_N<1>
PCIE_TBT_R2D_P<2>
PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_N<3>
PCIE_TBT_D2R_C_P<0>
PCIE_TBT_D2R_C_N<0>
PCIE_TBT_D2R_C_P<1>
PCIE_TBT_D2R_C_N<1>
PCIE_TBT_D2R_C_P<2>
PCIE_TBT_D2R_C_N<2>
PCIE_TBT_D2R_C_P<3>
PCIE_TBT_D2R_C_N<3>
PCIE_TBT_D2R_P<0>
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<1>
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<2>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<3>
PCIE_TBT_D2R_N<3>
PERST_N
PWR_ON_POC_RSTN
MONDC0
MONDC1
MONOBS_P
MONOBS_N
THERMDA
EE_DI
EE_DO
EE_CS_N
EE_CLK
EEPROM
TDI
TMS
TCK
TDO
TEST_EN
TEST_PWR_GOOD
JTAG/TEST PORT
MISC
RSENSE
RBIAS
NC
TBT_RSENSE
TBT_RBIAS
Not used in host mode.
PCIE RESET
PCIE_RST_0_N
PCIE_RST_1_N
PCIE_RST_2_N
PCIE_RST_3_N
TP_TBT_PCIE_RESET0_L
TP_TBT_PCIE_RESET1_L
TP_TBT_PCIE_RESET2_L
TP_TBT_PCIE_RESET3_L
PCIE_CLKREQ_OD_N
TBT_CLKREQ_ISOL_L
EN_LC_PWR
TBT_EN_LC_PWR
CLOCKS
REFCLK_100_IN_P
REFCLK_100_IN_N
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
XTAL_25_IN
XTAL_25_OUT
SYSCLK_CLK25M_TBT_R
TP_TBT_XTAL25OUT
TMU_CLK_OUT
TMU_CLK_IN
TBT_TMU_CLK_OUT
TBT_TMU_CLK_IN
DISPLAYPORT
SOURCE PORT 0
DPSRC_3_P
DPSRC_3_N
DPSRC_2_P
DPSRC_2_N
DPSRC_1_P
DPSRC_1_N
DPSRC_0_P
DPSRC_0_N
DPSRC_AUX_P
DPSRC_AUX_N
DPSRC_HPD_OD
TP_DP_TBTSRC_ML_CP<3>
TP_DP_TBTSRC_ML_CN<3>
TP_DP_TBTSRC_ML_CP<2>
TP_DP_TBTSRC_ML_CN<2>
NC_DP_TBTSRC_ML_CP<1>
NC_DP_TBTSRC_ML_CN<1>
TP_DP_TBTSRC_ML_CP<0>
TP_DP_TBTSRC_ML_CN<0>
NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN
DP_TBTSRC_HPD
SINK PORT 0
DPSNK0_3_P
DPSNK0_3_N
DPSNK0_2_P
DPSNK0_2_N
DPSNK0_1_P
DPSNK0_1_N
DPSNK0_0_P
DPSNK0_0_N
DPSNK0_AUX_P
DPSNK0_AUX_N
DPSNK0_HPD
SINK PORT 1
DPSNK1_3_P
DPSNK1_3_N
DPSNK1_2_P
DPSNK1_2_N
DPSNK1_1_P
DPSNK1_1_N
DPSNK1_0_P
DPSNK1_0_N
DPSNK1_AUX_P
DPSNK1_AUX_N
DPSNK1_HPD
DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_N
DP_TBTSNK0_HPD
DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_N
DP_TBTSNK1_HPD
PORT0
PORT2
PORT1
PORT3
PORTS
PA_CIO0_TX_P/DP_SRC_0_P
PA_CIO0_TX_N/DP_SRC_0_N
PA_CIO0_RX_P
PA_CIO0_RX_N
PA_CONFIG1/CIO_0_LSEO
PA_CONFIG2/CIO_0_LSOE
PA_CIO1_TX_P/DP_SRC_2_P
PA_CIO1_TX_N/DP_SRC_2_N
PA_CIO1_RX_P
PA_CIO1_RX_N
PA_LSTX/CIO_1_LSEO
PA_LSRX/CIO_1_LSOE
PA_DPSRC_1_P
PA_DPSRC_1_N
PA_DPSRC_3_P
PA_DPSRC_3_N
PA_AUX_P
PA_AUX_N
PA_DPSRC_HPD
GPIO_0/PA_HV_EN/BYP0
GPIO_10/PA_CIO_SEL/BYP1
GPIO_12/PA_DP_PWRDN/BYP2
PB_CIO2_TX_P/DP_SRC_0_P
PB_CIO2_TX_N/DP_SRC_0_N
PB_CIO2_RX_P
PB_CIO2_RX_N
PB_CONFIG1/CIO_2_LSEO
PB_CONFIG2/CIO_2_LSOE
PB_CIO3_TX_P/DP_SRC_2_P
PB_CIO3_TX_N/DP_SRC_2_N
PB_CIO3_RX_P
PB_CIO3_RX_N
PB_LSTX/CIO_3_LSEO
PB_LSRX/CIO_3_LSOE
PB_DPSRC_1_P
PB_DPSRC_1_N
PB_DPSRC_3_P
PB_DPSRC_3_N
PB_AUX_P
PB_AUX_N
PB_DPSRC_HPD
GPIO_1/PB_HV_EN/BYP0
GPIO_11/PB_CIO_SEL/BYP1
GPIO_13/PB_DP_PWRDN/BYP2
GPIO_2/GO2SX
(FORCE_PWR) GPIO_3
GPIO_4/WAKE_N_OD
GPIO_5/CIO_PLUG_EVENT
GPIO_6/CIO_SDA_OD
GPIO_7/CIO_SCL_OD
GPIO_8/EN_CIO_PWR_OD*
GPIO_9/OK2GO2SX_OD*
GPIO_14
GPIO_15
TBT_GO2SX_BIDIR
TBT_PWR_EN
SMC_PME_S4_DARK_L
TBT_CIO_PLUG_EVENT
SMBUS_PCH_DATA
SMBUS_PCH_CLK
(TBT_EN_CIO_PWR_L)
TBT_GPIO_9
TBT_GPIO_14
TBT_DDC_XBAR_EN_L
TBT_EN_CIO_PWR_L
MAKE_BASE=TRUE
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
PP3V3_S4_TBTAPWR
PP3V3_TBTLC
PP3V3_TBTLC
PP3V3_S4_TBTAPWR
PP3V3_TBTLC
R2810 47K
R2890 3.3K
R2891 3.3K
C2890 1UF
R2892 3.3K
R2893 3.3K
C2810 0.1UF
R2815 NOSTUFF
R2855 1K
R2898 10K
R2895 806
R2897 100K
R2899 NO STUFF
R2896 1K
R2880 10K
R2825 0
R2829 0
R2830 100K
R2831 100K
R2832 100K
R2881 0
R2883 10K
R2882 10K
R2885 10K
R2886 10K
R2888 10K
R2887 10K
U2890
M95256-RMC6XG
MLP
(TBT_SPI_MOSI)
(TBT_SPI_CLK)
(TBT_SPI_CS_L)
TBTROM_WP_L
TBTROM_HOLD_L
(TBT_SPI_MISO)
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
XDP_JTAG_ISP_TDI
JTAG_TBT_TMS
XDP_JTAG_ISP_TCK
JTAG_ISP_TDO
TBT_TEST_EN
TBT_TEST_PWR_GOOD
Divides 3.3V to 1.8V
R2881 for CYA,
allows separation
of GPIO_2/GPIO_9
if necessary.
Stuff one of R2881/2.
SNK0 AC Coupling
SNK1 AC Coupling
DP_TBTSNK0_ML_C_P<0>
DP_TBTSNK0_ML_C_N<0>
DP_TBTSNK0_ML_C_P<1>
DP_TBTSNK0_ML_C_N<1>
DP_TBTSNK0_ML_C_P<2>
DP_TBTSNK0_ML_C_N<2>
DP_TBTSNK0_ML_C_P<3>
DP_TBTSNK0_ML_C_N<3>
DP_TBTSNK0_AUXCH_C_P
DP_TBTSNK0_AUXCH_C_N
DP_TBTSNK1_ML_C_P<0>
DP_TBTSNK1_ML_C_N<0>
DP_TBTSNK1_ML_C_P<1>
DP_TBTSNK1_ML_C_N<1>
DP_TBTSNK1_ML_C_P<2>
DP_TBTSNK1_ML_C_N<2>
DP_TBTSNK1_ML_C_P<3>
DP_TBTSNK1_ML_C_N<3>
DP_TBTSNK1_AUXCH_C_P
DP_TBTSNK1_AUXCH_C_N
C2820
C2821
C2822
C2823
C2824
C2825
C2826
C2827
C2828
C2829
C2830
C2831
C2832
C2833
C2834
C2835
C2836
C2837
C2838
C2839
0.1UF
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=J41_MLB
SYNC_DATE=02/06/2013
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
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REVISION
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BRANCH
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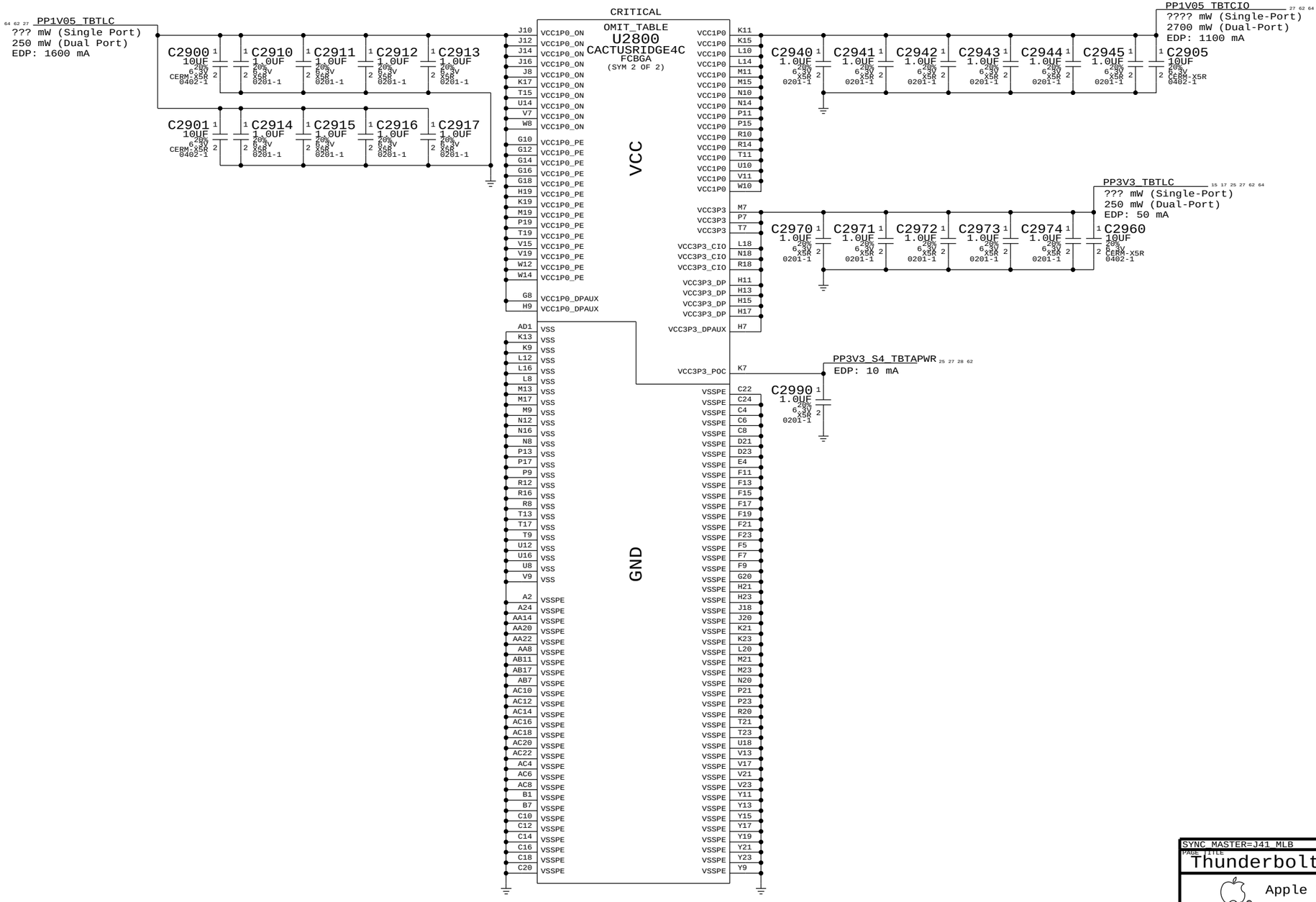

EDP numbers are from 12/22/2011 email from Haim Lustig (Intel) to Paul Baker (Apple)
Power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
Thunderbolt Host (2 of 2)

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
(NONE)

TBT 15V Boost Regulator

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL Q3080 SI8409DB BGA

PPBUS_G3H — 8-13V Input. Changes required for 2S.

PPVIN_S4SW_TBTBST_FET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

R3080 470K 5% 1/20W MF 201
C3080 0.1UF 10% 16V X5R 402
TBTBST_PWREN_DIV_L
R3081 150K 5% 1/20W MF 201
TBTBST_PWREN_L
Q3005 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
TBT_A_HV_EN

C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603
R3091 200K 1% 1/20W MF 201 <R1>

CRITICAL L3095 6.8UH-4.0A PIMB062D-SM

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIOT=TRUE

TBTBST_SNS1
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
R3089 0 5% 1/20W MF 0201

TBTBST_SNS2
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

CRITICAL D3095 POWERDI-123 DFLS230L

PP15V_TBT
Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

XW3095 SM PLACE_NEAR=C3095.1:2 mm

TBTBST_VSNS
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

CRITICAL U3090 LT3957 QFN
VIN, SW, EN/UVLO, INTVCC, VC, RT, SS, SYNC, SNS1, SNS2, NC, FBX

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
GND_TBTBST_SGND
SGND shorted to GND inside package, no XW necessary.

C3081 2.2UF 20% 25V X5R-CERM 402
C3092 2.2UF 20% 25V X5R-CERM 402
C3087 47PF 5% 25V NP0-C0G-CERM 0201
R3093 10K 1% 1/20W MF 201
TBTBST_VC_RC
R3092 73.2K 1% 1/20W MF 201 <R2>
C3082 2.2UF 20% 25V X5R-CERM 402
C3093 3300PF 10% 10V X7R-CERM 0201
R3094 41.2K 1% 1/20W MF 201
C3094 0.33UF 10% 6.3V CERM-X5R 402

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

R3090 49.9K 1% 1/16W MF-LF 402
TBTBST_VSNS_RC
C3088 22PF 5% 50V CERM 0402
R3095 133K 1% 1/16W MF-LF 402 <Ra>
C3089 100PF 5% 50V CERM 402 NO STUFF
R3096 15.8K 1% 1/16W MF-LF 402 <Rb>
TBTBST_FBX

C3095 10UF 20% 25V X5R-CERM 0603
C3097 10UF 20% 25V X5R-CERM 0603
C3096 10UF 20% 25V X5R-CERM 0603
C3098 10UF 20% 25V X5R-CERM 0603
C3084 10UF 20% 25V X5R-CERM 0603
C309A 10UF 20% 25V X5R-CERM 0603
C3085 10UF 20% 25V X5R-CERM 0603
C309B 10UF 20% 25V X5R-CERM 0603
C3099 0.001UF 10% 50V X7R-CERM 0402

Vout = 1.6V * (1 + Ra / Rb)

Q3088 DMN5L06VK-7 SOT-563
R3088 330K 5% 1/20W MF 201
TBTBST_SHDN_DIV
R3087 330K 5% 1/20W MF 201
Q3088 DMN5L06VK-7 SOT-563
Max Vgs: 10V
SMC_DELAYED_PWRGD

Supervisor & CLKREQ# Isolation

PP3V3_S0
R3040 10K 5% 1/20W MF 201
Q3040 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
TBT_EN_LC_PWR
C3000 0.1UF 10% 16V X5R-CERM 0201

CRITICAL U3000 SLG4AP016V TDFN
PP3V3_TBTLC
R3007 100K 5% 1/20W MF 201
PP1V05_TBTLC
SENSE 0.7V
DLY2
RESET*
TBT_PCIE_RESET_L
DLY = 60 ms +/- 20%
PCH_TBT_PCIE_RESET_L
Platform (PCIe) Reset
EN
OUT (OD)
IN
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE
TBT_CLKREQ_L
Pull-up provided by SB page.
GND, THRM PAD

TBT_EN_LC_ISOL
R3011 36.5K 1% 1/20W MF 201
TBT_EN_LC_RC3V3

3.3V TBT "LC" Switch

PP3V3_S0
U3010 TPS22924 CSP
A2 VIN, B2 VIN, C2 ON, A1 VOUT, B1 VOUT, C1 GND
CRITICAL
PP3V3_TBTLC
Max Current = 2A (85C)
C3010 1.0UF 20% 6.3V X5R 0201-1
C3011 1.0UF 20% 6.3V X5R 0201-1

U3010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

R3016 0 5% 1/20W MF 0201
TBT_EN_LC_RC1V05

1.05V TBT "LC" Switch

PP1V05_S0
U3015 TPS22920 CSP
A2 VIN, B2 VIN, C2 ON, A1 VOUT, B1 VOUT, C1 GND
CRITICAL
PP1V05_TBTLC
Max Current = 4A (85C)
C3015 1.0UF 20% 6.3V X5R 0201-1
NO STUFF C3016 1.0UF 20% 6.3V X5R 0201-1

U3015

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	6.1 mOhm Typ 10.4 mOhm Max

TBT "POC" Power-up Reset

PP3V3_S4_TBTAPWR
CRITICAL U3030 TPS3808 QFN
Pull-up: R2810
SENSE, CT, GND, THRM PAD, RESET*, MR* (IPU)
TBT_PWR_ON_POC_RST_L
TBTPOCRST_MR_L
TBTPOCRST_CT
C3031 0.0047UF 10% 25V CERM 0402
C3030 0.1UF 10% 16V X5R-CERM 0201
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms
C3025 330PF 10% 16V X7R-CERM 0201
Q3025 DMN5L06VK-7 SOT-563
PP3V3_S0
R3030 100K 5% 1/20W MF 201
TBT_POC_RESET_L

1.05V TBT "CIO" Switch

PP1V05_S0
PP3V3_TBTLC
R3020 100K 5% 1/20W MF 201
TBT_EN_CIO_PWR
Q3025 DMN5L06VK-7 SOT-563
TBT_EN_CIO_PWR_L
U3020 TPS22920 CSP
A2 VIN, B2 VIN, C2 ON, A1 VOUT, B1 VOUT, C1 GND
CRITICAL
PP1V05_TBTCIO
Max Current = 4A (85C)
C3020 1.0UF 20% 6.3V X5R 0201-1

U3020

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	6.1 mOhm Typ 10.4 mOhm Max

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: TBT Power Support

Apple Inc.

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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt device attach.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
PP15V_TBT 18.9V Max
C3287 CRITICAL 100UF 20% 6.3V POLY TANT CASE-B2-SM
C3280 22UF 20% 6.3V X5R-CERM 603
C3281 0.1UF 10% 16V X5R-CERM 0201
C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 16V X5R 402
U3210 CRITICAL CD3211A0RGPR QFN
V3P3 V3P3OUT VHV OUT ENHVU FAULTZ EN ISET_V3P3 HV_EN ISET_S0 S0 ISET_S3 GND THRM PAD
C3285 0.1UF 10% 16V X5R-CERM 0201
C3286 10UF 20% 6.3V CERM-X5R 0402-1
C3211 0.1UF 10% 25V X5R 402
PP3V3_S4_TBTAPWR
PP3V3RHV_S4_TBTAPWR
S4_PWR_EN
TBT_A_HV_EN
PM_SLP_S3_BUF_L
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V
12V: See below
R3210 22.6K 1% 1/20W MF 201
R3211 22.6K 1% 1/20W MF 201
R3212 36.5K 1% 1/20W MF 201 <RV3P3>
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R3213 22.6K 1% 1/20W MF 201 <RHVS3>
R3214 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

PP3V3_S4_TBTAPWR
C3220 0.1UF 10% 16V X5R-CERM 0201
U3220 CRITICAL CBTL05024 HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX
GND_VOID=TRUE (Both C's)
C3277 0.47UF 20% 4V_201 CERM-X5R-1
C3276 0.47UF 20% 4V_201 CERM-X5R-1
C3230 0.1UF 10% 16V X5R-CERM 0201
C3231 0.1UF 10% 16V X5R-CERM 0201
C3232 0.22UF 20% 6.3V X5R 0201
C3233 0.22UF 20% 6.3V X5R 0201
TBT_A_D2R_N<1> / TBT_A_D2R_P<1>
TBT_A_D2R_C_N<1> / TBT_A_D2R_C_P<1>
DP_TBTPA_AUXCH_C_N / DP_TBTPA_AUXCH_C_P
DP_TBTPA_AUXCH_N / DP_TBTPA_AUXCH_P
DP_TBTSNK0_DDC_DATA / DP_TBTSNK0_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1> / DP_TBTPA_ML_C_N<1>
DP_TBTPA_ML_P<1> / DP_TBTPA_ML_N<1>
TBT_A_LSTX / TBT_A_LSRX
DP_TBTPA_HPD
TBT_A_CIO_SEL
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N / TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
TBT_A_DP_HPD
TBT_A_LSX_ML_P<1> / TBT_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)

Thunderbolt Connector A

CRITICAL L3200 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTAPWR_F
C3200 0.01UF 10% 50V X7R-CERM 0402
C3201 0.01UF 10% 50V X7R-CERM 0402
R3201 12 5% 1/20W MF 201
TBTACONN_20_RC
J3200 MDP-J11 F-RT-TH
CRITICAL 514-0818
HOT_PLUG_DETECT, CONFIG1, CONFIG2, GND, ML_LANE3P, ML_LANE3N, AUX_CHP, AUX_CHN, DP_PWR, ML_LANE0P, ML_LANE0N, ML_LANE1P, ML_LANE1N, ML_LANE2P, ML_LANE2N, RETURN
SHIELD PINS
TBTACONN_1_C
TBTACONN_7_C
C3205 0.01UF 10% 25V X5R-CERM 0201 (0-18.9V)
C3206 0.01UF 10% 25V X5R-CERM 0201 (0-18.9V)
C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201
TBT_A_R2D_C_P<0> / TBT_A_R2D_C_N<0>
TBT_A_R2D_C_P<1> / TBT_A_R2D_C_N<1>
TBT_A_R2D_P<0> / TBT_A_R2D_N<0>
TBT_A_R2D_P<1> / TBT_A_R2D_N<1>
TBT: TX_0
TBT: TX_1
DP_A_LSX_ML_P<1> / DP_A_LSX_ML_N<1>
470K R's for ESD protection on AC-coupled signals.
TBT_A_D2R_P<0> / TBT_A_D2R_N<0>
TBT_A_D2R_C_P<0> / TBT_A_D2R_C_N<0>
R3294 1K 5% 1/20W MF 201
R3295 1K 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
DP_TBTPA_ML_C_P<3> / DP_TBTPA_ML_C_N<3>
C3278 0.22UF 20% 6.3V X5R 0201
C3279 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<3> / DP_TBTPA_ML_N<3>
R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201
TBT: Unused
TBT_A_D2R1_AUXDDC_P / TBT_A_D2R1_AUXDDC_N
TBT: RX_0
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R-CERM 0201
C3295 330PF 10% 16V X7R-CERM 0201
R3241 100K 5% 1/20W MF 201
C3202 0.01UF 10% 16V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=J41_MLB SYNC_DATE=02/07/2013

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

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3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

Sense resistor on sensor page

PP3V3_WLAN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

PP3V3_WLAN_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
Max Current = 2A (85C)

U3550
TPS22924
CSP
CRITICAL
A1 VOUT
B1
A2 VIN
B2 ON
C2 GND
C1

PP3V3_S5
SMC_WIFI_PWR_EN

C3550
1.0UF
20%
6.3V
X6S
0201-1

C3521
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=J3501:5mm

514S0335
CRITICAL
J3501
SSD-K99
F-RT-SM1

AIRPORT

PCIE_AP_R2D_N → C3531 0.1UF → PCIE_AP_R2D_C_N
PCIE_AP_R2D_P → C3530 0.1UF → PCIE_AP_R2D_C_P
(10% 6.3V X5R-CERM 0201)

WIFI_EVENT_L (OUT)
PCIE_CLK100M_AP_N (IN)
PCIE_CLK100M_AP_P (IN)
PCIE_AP_D2R_P (OUT)
PCIE_AP_D2R_N (OUT)

PP3V3_S4
C3532
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=J3501:1.5mm

Supervisor & CLKREQ# Isolation

Delay = 130 ms +/- 20%

APCLKRQ:ISOL
R3553 100K 5% 1/20W MF 201
R3554 232K 1% 1/20W MF 201

P3V3WLAN_VMON

U3540
SLG4AP041V
TDFN
CRITICAL
VDD
SENSE
VREF
RESET*
MR*
EN
OUT (OD)
IN
THRM PAD
GND
DLY

PP3V3_S5
C3540
0.1UF
10%
6.3V
CERM-X5R
0201

R3558
0
5%
1/20W
MF
0201

AP_RESET_CONN_L
AP_RESET_CONN_R_L
AP_RESET_L
SMC_WIFI_PWR_EN
AP_CLKREQ_R_L
AP_CLKREQ_Q_L

R3555
100K
5%
1/20W
MF
201

APCLKRQ:ISOL
R3556
0
5%
1/20W
MF
0201

APCLKRQ:BIDIR
R3557
0
5%
1/20W
MF
0201
AP_CLKREQ_L

NOSTUFF
R3559
0
5%
1/20W
MF
0201

PCIe Wake Muxing

PP3V3_S5
R3561 100K 5% 1/20W MF 201
C3560 0.1UF 10% 6.3V CERM-X5R 0201
AP_PCIE_WAKE_L

U3560
NC7SB3157P6XG
SC70
VER-3
VCC
GND
S
B0
B1
A

SEL	OUTPUT
L	PCIE_WAKE_L (B0)
H	AP_S0IX_WAKE_L (B1)

AP_S0IX_WAKE_SEL (IN)
PCIE_WAKE_L (OUT)
AP_S0IX_WAKE_L (OUT)

NOSTUFF
R3560
0
5%
1/20W
MF
0201

BLUETOOTH

PP3V3_S4
C3510
0.1UF
10%
6.3V
CERM-X5R
0201

U3510
USB3740
DFN
CRITICAL
VDD
DP_2
DM_2
DP_1
DM_1
OE*
S
GND
NC

USB_BT_CONN_P
USB_BT_CONN_N
USB_BT_P
USB_BT_N
BT_WAKE
PM_SLP_S4_L

SEL	OUTPUT
L	BT_WAKE (1)
H	USB_BT (2)

SIGNAL_MODEL=BT_MUX

NO_XNET_CONNECTION=TRUE
Q3510
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2

R3512
15K
1%
1/20W
MF
201

SMC_PME_S4_WAKE_L

SYNC_MASTER=J41_MLB
SYNC_DATE=02/06/2013

PAGE TITLE
Wireless Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM>
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PLACE_NEAR=J3700.1:3mm
CRITICAL
L3700
FERR-26-OHM-6A
0603
64 62 41 30 PP3V3_S0SW_SSD
64 PP3V3_S0SW_SSD_FLT
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.15mm
VOLTAGE=3.3V
C3701 0.1UF 10% 10V X5R-CERM 0201
C3702 0.1UF 10% 10V X5R-CERM 0201
PLACE_NEAR=L3700.1:1mm
PLACE_NEAR=L3700.1:1mm

514S0449
CRITICAL
J3700
SSD-GS3
F-RT-SM

36 30 27 18 17 15 13 12 11 8 7 74 65 64 62 61 59 56 45 44 43 42 41 40 39 38 PP3V3_S0
R3710 100K 5% 1/20W MF 201
R3700 100K 5% 1/20W MF 201
61 59 56 45 44 43 42 41 40 39 38 74 65 64 62 PP3V3_S0

GND_VOID	1	53	GND_VOID		
	2	52	64 SMC_OOB1_R2D_CONN_L		
	3	51	64 SMC_OOB1_D2R_CONN_L		
	4				
	5	50	SSD_PCIE_SEL_L	OUT	16 64
	6	49	SSD_DEVSLP	IN	15 64
	7	48	SMC_PWRFAIL_WARN_L	IN	37
	8	47	SSD_PWR_EN	IN	15 30 58 59 64
	9				
	10	46	SMC_PWRFAIL_WARN_L Signal has PU on SSD module		
	11	45 TRUE	PCIE_SSD_D2R_N<3>	OUT	12 64 67
	12	44 TRUE	PCIE_SSD_D2R_P<3>	OUT	12 64 67
	13	43			
	14	42 TRUE	PCIE_SSD_D2R_N<2>	OUT	12 64 67
	15	41 TRUE	PCIE_SSD_D2R_P<2>	OUT	12 64 67
	16	40			
	17	39			
	18	38 TRUE	PCIE_SSD_D2R_N<1>	OUT	12 64 67
	19	37 TRUE	PCIE_SSD_D2R_P<1>	OUT	12 64 67
	20	36			
	21	35 TRUE	PCIE_SSD_D2R_N<0>	OUT	12 64 67
	22	34 TRUE	PCIE_SSD_D2R_P<0>	OUT	12 64 67
	23	33			
	24				
	25	32			
	26	31	PCIE_CLK100M_SSD_N	IN	12 64 67
	27	30	PCIE_CLK100M_SSD_P	IN	12 64 67
	28	29			
	54	59			
	55	60			
	56	61			
	57	62			
	58	63			

PP3V3_S0
SSD_RESET_CONN_L
NC_SSD_MFG_RSVD

67 12 PCIE_SSD_R2D_C_N<3> C3710 0.1UF 10% 16V X5R-CERM 0201 2 GND_VOID=TRUE 67 64 PCIE_SSD_R2D_N<3>
67 12 PCIE_SSD_R2D_C_P<3> C3711 0.1UF 10% 16V X5R-CERM 0201 2 GND_VOID=TRUE 67 64 PCIE_SSD_R2D_P<3>
67 12 PCIE_SSD_R2D_C_N<2> C3712 0.1UF 10% 16V X5R-CERM 0201 2 GND_VOID=TRUE 67 64 PCIE_SSD_R2D_N<2>
67 12 PCIE_SSD_R2D_C_P<2> C3713 0.1UF 10% 16V X5R-CERM 0201 2 GND_VOID=TRUE 67 64 PCIE_SSD_R2D_P<2>
67 12 PCIE_SSD_R2D_C_N<1> C3714 0.1UF 10% 16V X5R-CERM 0201 2 GND_VOID=TRUE 67 64 PCIE_SSD_R2D_N<1>
67 12 PCIE_SSD_R2D_C_P<1> C3715 0.1UF 10% 16V X5R-CERM 0201 2 GND_VOID=TRUE 67 64 PCIE_SSD_R2D_P<1>
67 12 PCIE_SSD_R2D_C_N<0> C3716 0.1UF 10% 16V X5R-CERM 0201 2 GND_VOID=TRUE 67 64 PCIE_SSD_R2D_N<0>
67 12 PCIE_SSD_R2D_C_P<0> C3717 0.1UF 10% 16V X5R-CERM 0201 2 GND_VOID=TRUE 67 64 PCIE_SSD_R2D_P<0>
64 SSD_CLKREQ_CONN_L

Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

PCIe polarity inversion and lane reversal
are only permitted on the device side,
provided the device PHY supports it.

Gumstick3 Connector

OOB Isolation

64 62 41 30 PP3V3_S0SW_SSD
BYPASS=U3710:5 mm
C3718 0.1UF 10% 10V X5R-CERM 0201
CRITICAL
74LVC1G08 SOT891
U3710 08
SMC_OOB1_R2D_L IN 37
NC

36 30 27 18 17 15 13 12 11 8 7 74 65 64 62 61 59 56 45 44 43 42 41 40 39 38 PP3V3_S0
BYPASS=U3711:5 mm
C3719 0.1UF 10% 10V X5R-CERM 0201
CRITICAL
74LVC1G08 SOT891
U3711 08
SMC_OOB1_D2R_L OUT 37
NC

Supervisor & CLKREQ# Isolation

Delay = ~55ms

PP3V3_S0SW_SSD 30 41 62 64
PP3V42_G3H 17 35 36 37 38 40 46 49 50 59 61 62 64 65
R3740 100K 5% 1/20W MF 201
R3741 232K 1% 1/20W MF 201
P3V3SSD_VMON
CRITICAL
U3740 SLG4AP016V TDFN
VDD
C3740 0.1UF 10% 6.3V CERM-X5R 0201
SENSE 0.7V
DLY
RESET*
MR*
EN
IN
OUT (OD)
THRM PAD
GND
SSD_RESET_L IN 15
SSD_PWR_EN IN 15 30 58 59 64
SSD_CLKREQ_L OUT 12
R3742 100K 1% 1/20W MF 201

SYNC_MASTER=J41_MLB	SYNC_DATE=04/09/2013
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Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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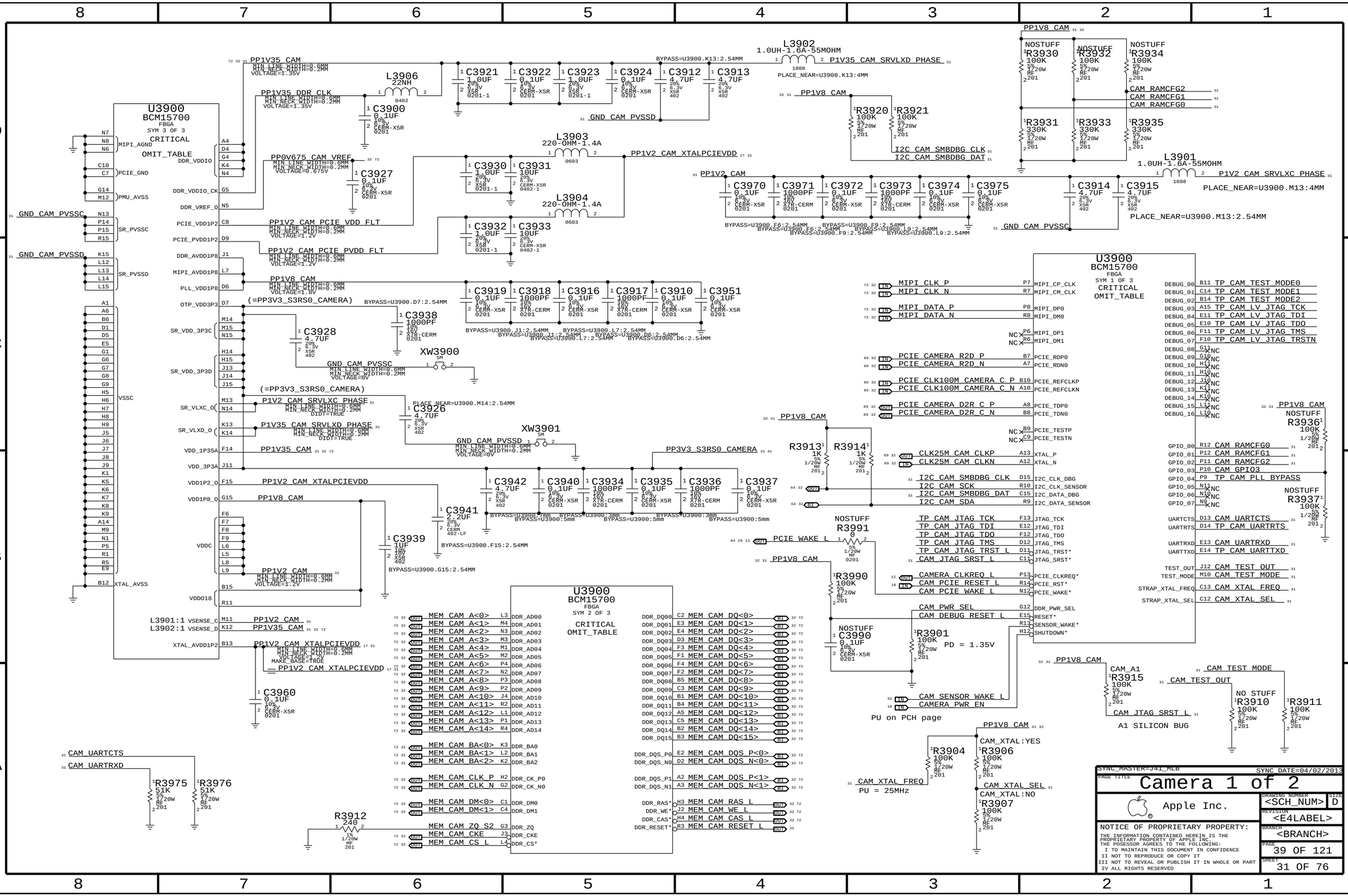
U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE
PP1V35_CAM
PP1V35_DDR_CLK
L3906
22NH
L3902
1.0UH-1.6A-55MOHM
P1V35_CAM_SRVLXD_PHASE
PP1V8_CAM
R3930 100K
R3932 100K
R3934 100K
R3931 330K
R3933 330K
R3935 330K
CAM_RAMCFG2
CAM_RAMCFG1
CAM_RAMCFG0
R3920 100K
R3921 100K
I2C_CAM_SMBDBG_CLK
I2C_CAM_SMBDBG_DAT
L3901
1.0UH-1.6A-55MOHM
P1V2_CAM_SRVLXC_PHASE
PLACE_NEAR=U3900.M13:4MM
PLACE_NEAR=U3900.M13:2.54MM
GND_CAM_PVSSC
GND_CAM_PVSSD
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
PP1V2_CAM_XTALPCIEVDD
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PCIE_PVDD_FLT
PP0V675_CAM_VREF
PP1V2_CAM
(=PP3V3_S3RS0_CAMERA)
XW3900
XW3901
P1V2_CAM_SRVLXC_PHASE
P1V35_CAM_SRVLXD_PHASE
PP3V3_S3RS0_CAMERA
PP1V2_CAM_XTALPCIEVDD
PP1V8_CAM
R3913 1K
R3914 1K
NOSTUFF R3991 0
PCIE_WAKE_L
R3990 100K
NOSTUFF C3990 0.1UF
R3901 100K
PD = 1.35V
PU on PCH page
CAM_SENSOR_WAKE_L
CAMERA_PWR_EN
MIPI_CLK_P
MIPI_CLK_N
MIPI_DATA_P
MIPI_DATA_N
PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_N
PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
CLK25M_CAM_CLKP
CLK25M_CAM_CLKN
I2C_CAM_SMBDBG_CLK
I2C_CAM_SCK
I2C_CAM_SMBDBG_DAT
I2C_CAM_SDA
TP_CAM_JTAG_TCK
TP_CAM_JTAG_TDI
TP_CAM_JTAG_TDO
TP_CAM_JTAG_TMS
TP_CAM_JTAG_TRST_L
CAM_JTAG_SRST_L
CAMERA_CLKREQ_L
CAM_PCIE_RESET_L
CAM_PCIE_WAKE_L
CAM_PWR_SEL
CAM_DEBUG_RESET_L
R3904 100K
R3906 100K
CAM_XTAL:YES
CAM_XTAL_SEL
CAM_XTAL:NO
R3907 100K
CAM_XTAL_FREQ
PU = 25MHz
CAM_A1
R3915 100K
CAM_JTAG_SRST_L
A1 SILICON BUG
CAM_TEST_MODE
CAM_TEST_OUT
NO STUFF R3910 100K
R3911 100K
NOSTUFF R3936 100K
NOSTUFF R3937 100K
CAM_UARTCTS
CAM_UARTRXD
R3975 51K
R3976 51K
R3912 240
MEM_CAM_A<0>
MEM_CAM_A<1>
MEM_CAM_A<2>
MEM_CAM_A<3>
MEM_CAM_A<4>
MEM_CAM_A<5>
MEM_CAM_A<6>
MEM_CAM_A<7>
MEM_CAM_A<8>
MEM_CAM_A<9>
MEM_CAM_A<10>
MEM_CAM_A<11>
MEM_CAM_A<12>
MEM_CAM_A<13>
MEM_CAM_A<14>
MEM_CAM_BA<0>
MEM_CAM_BA<1>
MEM_CAM_BA<2>
MEM_CAM_CLK_P
MEM_CAM_CLK_N
MEM_CAM_DM<0>
MEM_CAM_DM<1>
MEM_CAM_ZQ_S2
MEM_CAM_CKE
MEM_CAM_CS_L
MEM_CAM_DQ<0>
MEM_CAM_DQ<1>
MEM_CAM_DQ<2>
MEM_CAM_DQ<3>
MEM_CAM_DQ<4>
MEM_CAM_DQ<5>
MEM_CAM_DQ<6>
MEM_CAM_DQ<7>
MEM_CAM_DQ<8>
MEM_CAM_DQ<9>
MEM_CAM_DQ<10>
MEM_CAM_DQ<11>
MEM_CAM_DQ<12>
MEM_CAM_DQ<13>
MEM_CAM_DQ<14>
MEM_CAM_DQ<15>
MEM_CAM_DQS_P<0>
MEM_CAM_DQS_N<0>
MEM_CAM_DQS_P<1>
MEM_CAM_DQS_N<1>
MEM_CAM_RAS_L
MEM_CAM_WE_L
MEM_CAM_CAS_L
MEM_CAM_RESET_L
SYNC_MASTER=J41_MLB
SYNC_DATE=04/02/2013
PAGE TITLE
Camera 1 of 2
Apple Inc.
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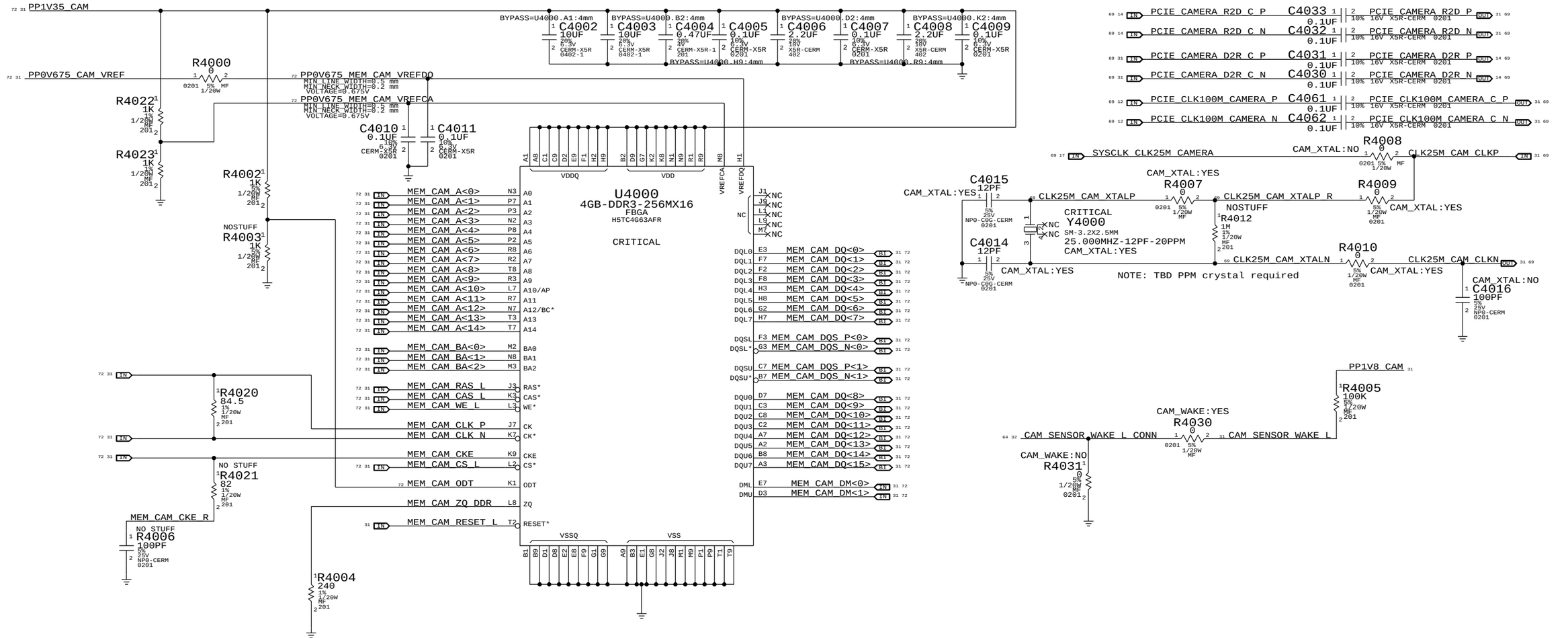

SYNC_MASTER=J41_MLB
SYNC_DATE=03/20/2013

PAGE TITLE: Camera 2 of 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM>
SIZE: D
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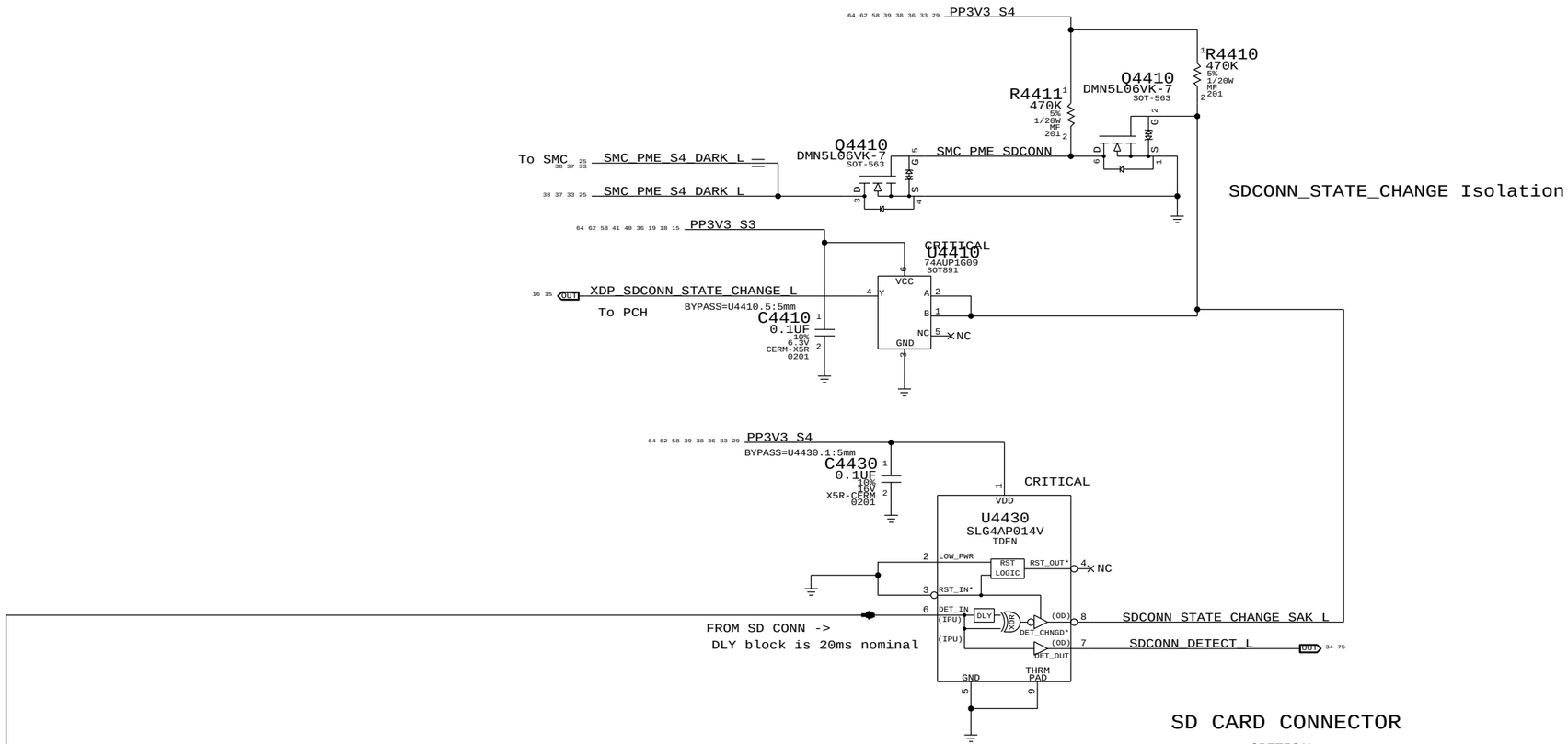

SYNC_MASTER=MASTER SYNC_DATE=07/01/2011

PAGE TITLE
SD READER CONNECTOR

Apple Inc.

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3.3V S3 SD Card Switch

PP3V3_S5

NOSTUFF
R4555 10K 5% 1/20W MF 201

SD_PWR_EN

U4550 SLG5AP1443V TDFN CRITICAL
VDD CAP ON GND D S
P3V3_SD_FET_RAMP

BYPASS=U4550.A2:5mm
C4560 1.0UF 20% 6.3V X5R 0201-1
C4561 4700PF 10% 16V X7R 201

PP3V3_S0SW_SD
MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.20MM VOLTAGE=3.3V MAKE_BASE=TRUE

U4550 EDP: 1.05A

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

CRITICAL
L4500 FERR-1000-OHM-450MA 0402

PP1V2_S0_SD_AVDD12
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.2V

BYPASS=U4500.46:5mm BYPASS=U4500.3:5mm
C4523 0.1UF 10% 16V X5R-CERM 0201
C4524 0.1UF 10% 16V X5R-CERM 0201
C4525 1.0UF 10% 6.3V X5R-CERM 0201-1
BYPASS=U4500.3:5mm

PP3V3_S0_SD_AVDD33
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V

BYPASS=U4500.43:5mm
C4526 0.1UF 10% 16V X5R-CERM 0201
C4527 0.1UF 10% 16V X5R-CERM 0201
C4528 2.2UF 20% 6.3V CERM 402-LF
BYPASS=U4500.9:5mm
BYPASS=U4500.43:5mm

CRITICAL
L4501 FERR-1000-OHM-450MA 0402

PP1V2_S3_SD_DVDD12
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.2V

BYPASS=U4500.42:5mm
C4519 0.1UF 10% 16V X5R-CERM 0201
BYPASS=U4500.21:5mm
C4520 2.2UF 20% 4V X5R-CERM 0201

PP3V3_S0_SD_CONN
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.20MM VOLTAGE=3.3V MAKE_BASE=TRUE
900mA max
BYPASS=U4500.39:5mm
C4550 4.7UF 20% 6.3V X5R 402

NO USB_2.0 INTERFACE
USB_SD_DM
R4580 0 5% 1/20W MF 0201
USB_SD_DP

U4500 GL3219 LQFN CRITICAL OMIT_TABLE

39	PMOS33		
3	AVDD12		
46	AVDD12		
9	AVDD33		
43	AVDD33		
21	DVDD12		
42	DVDD12		
31	DVDD33		
38	DVDD33		
40	DVDD33		
22	V33IN		
30	VUHSI		
45	DM		
44	DP		
7	X1		
8	X2		
4	RXN	TXN	USB3_SD_D2R_C_N
5	RXP	TXP	USB3_SD_D2R_C_P
10	RTERM		
41	RSTZ* (IPU)		
11	NC	SD_CLK	SDCONN_CLK
12	NC	SD_WP (IPU)	SDCONN_WP
13	NC	SD_CMD	SDCONN_CMD
14	NC	SD_CDZ (IPU)	SDCONN_DETECT_L
15	NC	SPI_CK	SD_SPI_CLK
16	NC	SPI_CS	SD_SPI_CS_L
17	NC	SPI_SI	SD_SPI_MOSI
18	NC	SPI_SO	SD_SPI_MISO
19	NC	LED	NC
32	NC		
6	GND		
47	THRM PAD		

PP1V2_S0_SD_VUHS1
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.8V

C4529 47PF 5% 25V NP0-C0G-CERM 0201
C4530 100PF 5% 25V NP0-CERM 0201
C4531 1.0UF 10% 6.3V X5R-CERM 0201-1
BYPASS=U4500.30:5mm
BYPASS=U4500.30:5mm

BYPASS=U4500.38:5mm
C4521 4.7UF 20% 6.3V X5R 402
BYPASS=U4500.22:5mm
C4522 1.0UF 10% 6.3V X5R-CERM 0201-1
C4518 0.1UF 10% 16V X5R-CERM 0201
BYPASS=U4500.31:5mm

SD_D1 SDCONN_DATA<1>
SD_D0 SDCONN_DATA<0>
SD_D2 SDCONN_DATA<2>
SD_D3 SDCONN_DATA<3>
(B1) 33 75

PLACE_NEAR=U4500.4:5mm
USB3_SD_R2D_C_N → C4510 0.1UF 10% 16V X5R-CERM 0201 GND VOID=TRUE → USB3_SD_R2D_N
USB3_SD_R2D_C_P → C4511 0.1UF 10% 16V X5R-CERM 0201 GND VOID=TRUE → USB3_SD_R2D_P
PLACE_NEAR=U4500.5:5mm

PLACE_NEAR=U4500.1:5mm
C4512 0.1UF 10% 16V X5R-CERM 0201 GND VOID=TRUE → USB3_SD_D2R_N
C4513 0.1UF 10% 16V X5R-CERM 0201 GND VOID=TRUE → USB3_SD_D2R_P
PLACE_NEAR=U4500.2:5mm

SD_RESET_L → R4570 3.3K 5% 1/20W MF 201 → SD_RESET_R_L

C4570 0.047UF 10% 6.3V X5R 201
R4500 680 1% 1/20W MF 201

U4590 512KB USON W25X05CL CRITICAL NOSTUFF
VCC DIO(IO0) DO(IO1) CLK CS* WP* HOLD* THRM PAD GND

SD_SPI_WP_L
SD_SPI_HOLD_L

NOSTUFF
R4590 3.3K 5% 1/20W MF 201
R4591 3.3K 5% 1/20W MF 201

C4590 1.0UF 10% 6.3V X5R-CERM 0201-1 NOSTUFF
BYPASS=U4590.8:5mm

USING ON CHIP CLOCK SOURCE MODE (CRYSTAL AS BACK-UP)

C4580 12PF 5% 25V NP0-C0G-CERM 0201
C4581 12PF 5% 25V NP0-C0G-CERM 0201
CRITICAL
Y4580 25.000MHZ-12PF-20PPM SM-3.2X2.5MM
R4581 0 5% 1/20W MF 0201
R4582 1M 5% 1/20W MF 201
SDCLK_CLK25M_X2 → SDCLK_CLK25M_X2_R
SDSCLK_CLK25M_X1

PAGE TITLE
SD CONTROLLER (GL3219)

Apple Inc.

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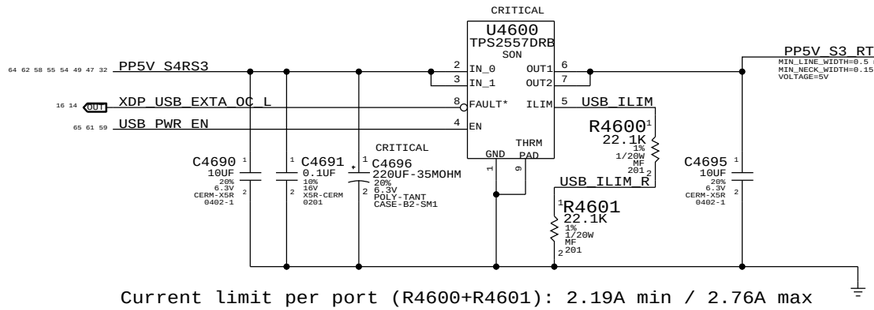
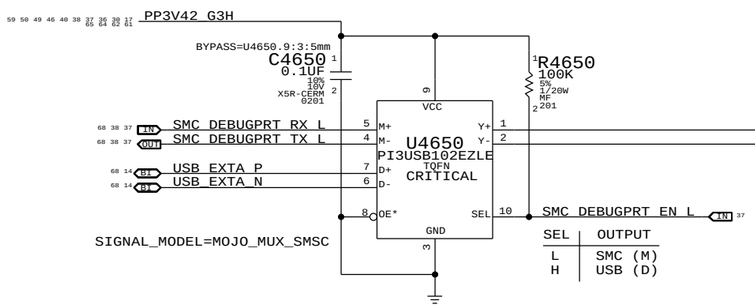
Right USB Port A

USB Port Power Switch

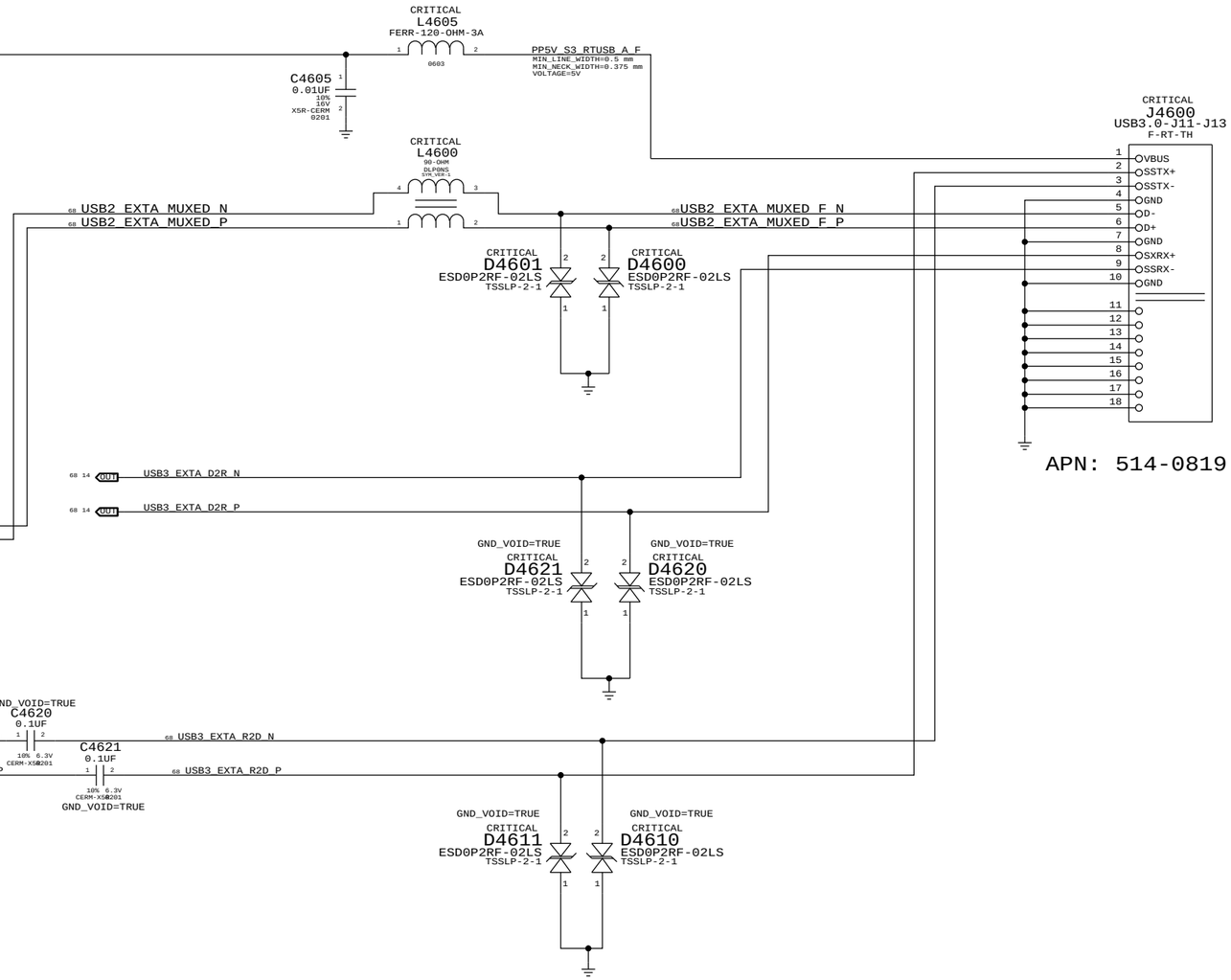


Current limit per port (R4600+R4601): 2.19A min / 2.76A max

Mojo SMC Debug Mux



SEL	OUTPUT
L	SMC (M)
H	USB (D)



APN: 514-0819

SYNC_MASTER=J41_MLB SYNC_DATE=02/07/2013

PAGE TITLE
External A USB3 Connector

Apple Inc.

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IPD Flex Connector

PLACE_NEAR=J4800.10:1.5MM
R4830
0
64 62 58 39 38 36 33 29 PP3V3_S4
5% 1/20W MF 0201
C4800
0.1UF
10% 6.3V CERM-X5R 0201
VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.5 mm
BYPASS=J4800.10:1.5MM
PLACE_NEAR=J4800.14:1.5MM
L4820
FERR-120-OHM-1.5A
62 54 53 PP5V_S5
0402-LF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
C4810
0.1UF
10% 16V X5R-CERM 0201
PLACE_NEAR=J4800.14:1.5MM
50 49 46 40 38 37 35 30 17 65 64 62 61 59 PP3V42_G3H
BYPASS=J4800.10:1.5MM
C4820
0.1UF
10% 6.3V CERM-X5R 0201

TPAD_INTWAKE:SPLIT
PLACE_NEAR=R4844.1:1.5MM
R4841
0
5% 1/20W MF 0201
(TPAD_WAKE_L)

TPAD_INTWAKE:SHARED
R4843
0
5% 1/20W MF 0201
39 37 29 OUT SMC_PME_S4_WAKE_L
To SMC
PLACE_NEAR=R4841.1:1.5MM
(TPAD_SPI_INT_S4_WAKE_L_CONN)

TPAD_INTWAKE:SHARED
Q4800
DMN32D2LFB4
DFN1006H4-3
SYM_VER_3
64 62 58 41 40 36 33 19 18 15 PP3V3_S3
15 OUT TPAD_SPI_INT_L
To PCH
PLACE_NEAR=R4842.2:5MM

TPAD_INTWAKE:SPLIT
R4842
0
5% 1/20W MF 0201
PLACE_NEAR=R4843.2:1.5MM

TPAD_INTWAKE:SHARED
R4844
0
5% 1/20W MF 0201
PLACE_NEAR=J4800.8:1.5MM

64 62 58 39 38 36 33 29 PP3V3_S4
C4841
0.1UF
10% 6.3V CERM-X5R 0201
BYPASS=U4810:3mm

CRITICAL
74LVC2G08GT
SOT833
U4810
59 37 36 29 18 13 IN PM_SLP_S4_L
15 IN TPAD_USB_IF_EN
From PCH
(TPAD_USB_IF_EN_CONN)
NOSTUFF
R4810
100K
5% 1/20W MF 201

CKPLUS_WAIVE=UNCONNECTED_PINS
74LVC2G08GT
SOT833
U4810
59 37 36 29 18 13 IN PM_SLP_S4_L
15 IN TPAD_SPI_IF_EN
From PCH
(TPAD_SPI_IF_EN_CONN)
CKPLUS_WAIVE=UNCONNECTED_PINS

64 62 58 41 40 36 33 19 18 15 PP3V3_S3
R4860
100K
5% 1/20W MF 201
38 30 27 18 17 15 13 12 11 8 61 59 56 45 44 43 42 41 40 39 74 66 64 62 PP3V3_S0
Q4860
DMN32D2LFB4
DFN1006H4-3
SYM_VER_3
15 IN TPAD_SPI_CS_L
TPAD_SPI_CS_CONN_L

R4850
33
65 64 61 38 37 36 IN SMC_LID
15 68 OUT TPAD_SPI_MISO
5% 1/20W MF 201
PLACE_NEAR=J4800.2:2.54mm
64 TPAD_SPI_MISO_R
68 64 14 BI USB_TPAD_P
68 64 14 BI USB_TPAD_N
R4851
15 68 IN TPAD_SPI_CLK
5% 1/20W MF 201
PLACE_NEAR=J4800.7:2.54mm
64 TPAD_SPI_CLK_R
64 TPAD_WAKE_L
R4852
15 68 IN TPAD_SPI_MOSI
5% 1/20W MF 201
PLACE_NEAR=J4800.9:2.54mm
64 TPAD_SPI_MOSI_R
64 PP3V3_S4_IPD
R4853
5% 1/20W MF 201
PLACE_NEAR=J4800.12:2.54mm
64 TPAD_SPI_CS_R_L
64 TPAD_SPI_IF_EN_CONN
64 TPAD_SPI_INT_S4_WAKE_L_CONN
64 PP5V_S4_IPD
64 TPAD_USB_IF_EN_CONN
73 64 44 40 37 36 BI SMBUS_SMC_3_SDA
73 64 44 40 37 36 BI SMBUS_SMC_3_SCL
64 38 36 OUT SMC_LSOC_RST_L
(=PP3V42_G3H_IPD)
64 38 37 36 OUT SMC_ONOFF_L

CRITICAL
518S0884
J4800
TF13BS-20S-0.4SH
F-RT-SM-1
22
1 SMC_LID
2 TPAD_SPI_MISO_R
3
4 USB_TPAD_P
5 USB_TPAD_N
6
7 TPAD_SPI_CLK_R
8 TPAD_WAKE_L
9 TPAD_SPI_MOSI_R
10 PP3V3_S4_IPD
11 TPAD_SPI_CS_R_L
12 TPAD_SPI_IF_EN_CONN
13 TPAD_SPI_INT_S4_WAKE_L_CONN
14 PP5V_S4_IPD
15 TPAD_USB_IF_EN_CONN
16 SMBUS_SMC_3_SDA
17 SMBUS_SMC_3_SCL
18 SMC_LSOC_RST_L
19 (=PP3V42_G3H_IPD)
20 SMC_ONOFF_L
21

SMBUS_SMC_3_SDA 36 37 40 44 64 73
SMBUS_SMC_3_SCL 36 37 40 44 64 73
SMC_ONOFF_L 36 37 38 64
SMC_LID 36 37 38 61 64 65
SMC_LSOC_RST_L 36 38 64

NOSTUFF C4832 100PF 5% 25V NP0-CERM 0201 BYPASS=J4800.6:1.5MM
NOSTUFF C4833 100PF 5% 25V NP0-CERM 0201 BYPASS=J4800.5:1.5MM
C4834 100PF 5% 25V NP0-CERM 0201 BYPASS=J4800.4:1.5MM
C4835 100PF 5% 25V NP0-CERM 0201 BYPASS=J4800.3:1.5MM
C4836 100PF 5% 25V NP0-CERM 0201 BYPASS=J4800.1:1.5MM

SYNC_MASTER=J41_MLB SYNC_DATE=02/12/2013
PAGE TITLE
IPD Connector
Apple Inc.
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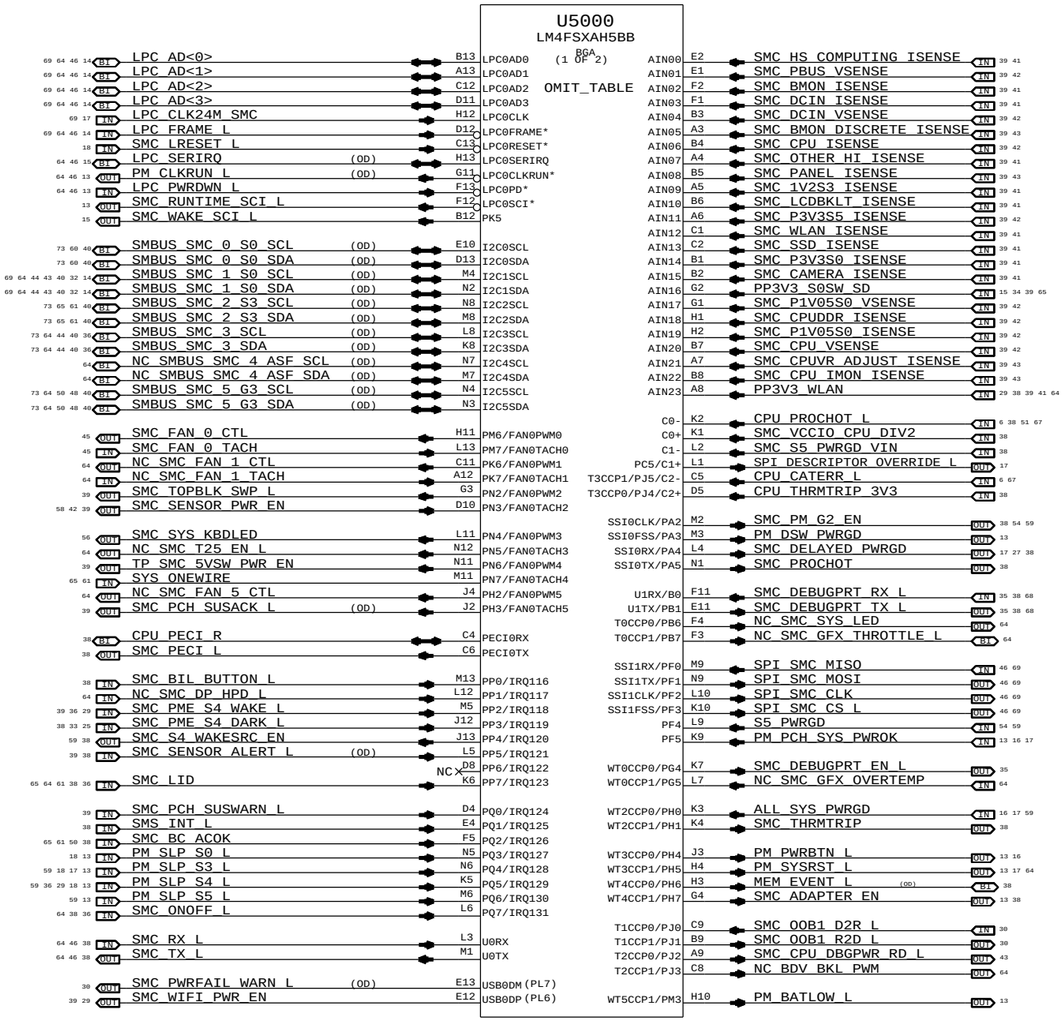

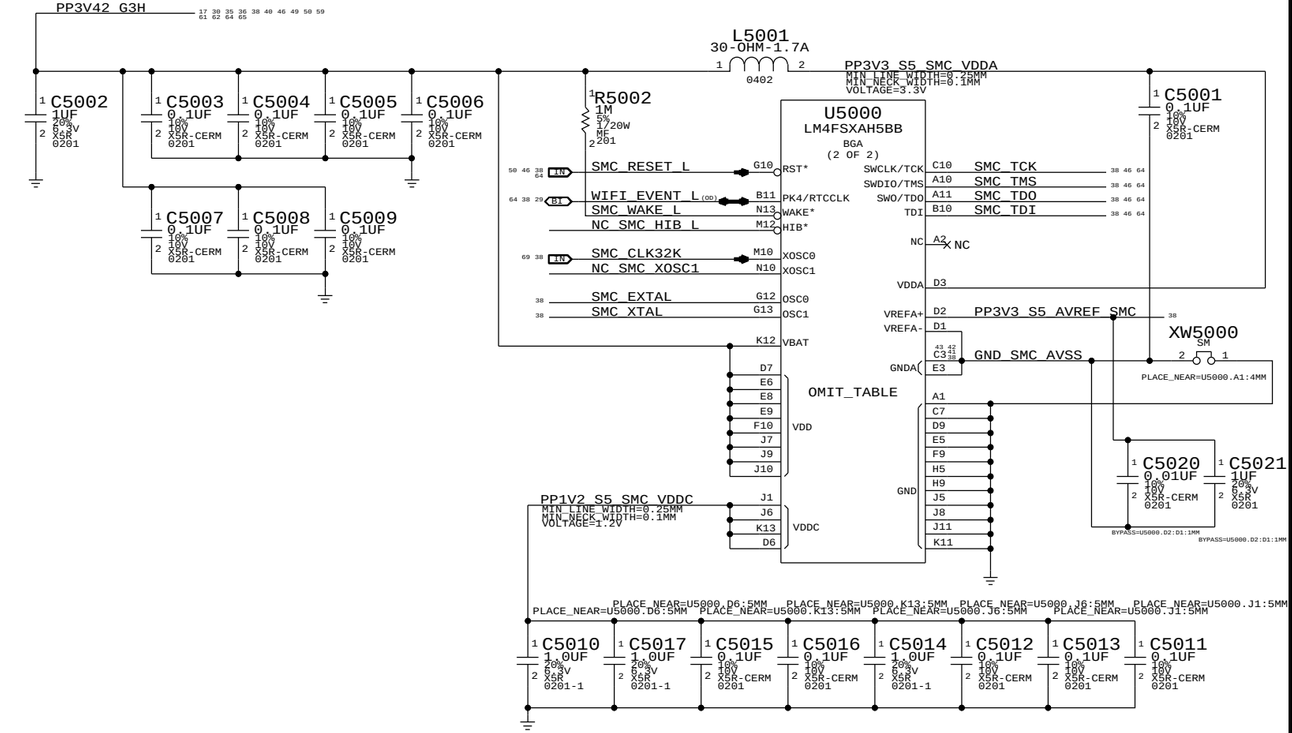

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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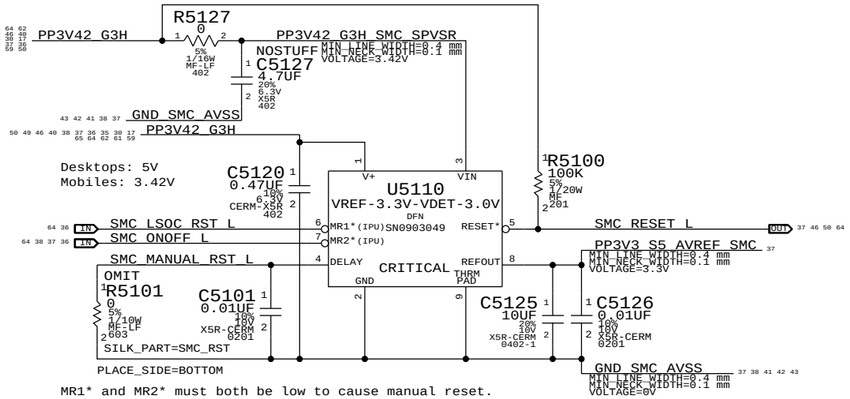
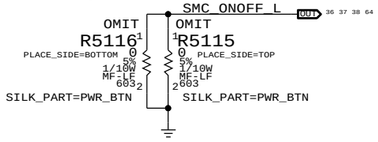
SMC Reset "Button", Supervisor & AVREF Supply



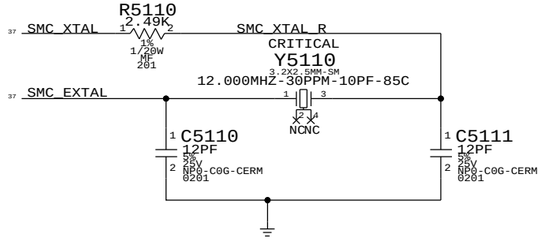
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

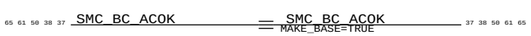
Debug Power "Buttons"

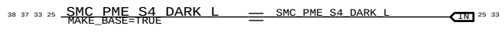


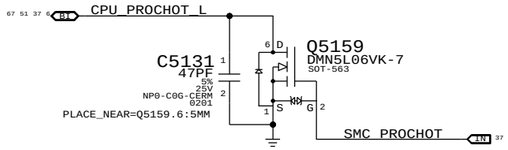
SMC Crystal Circuit

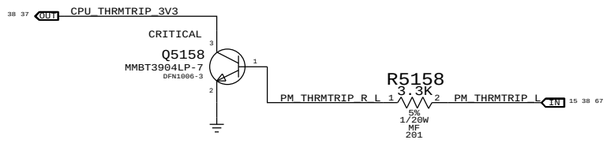
SMC USB Clock require these crystal
values:5,6,8,10,12,16,18,20,24,25 MHz

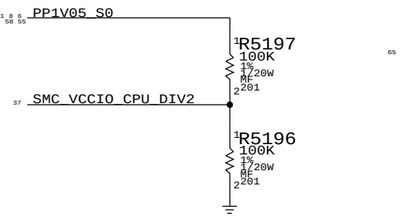




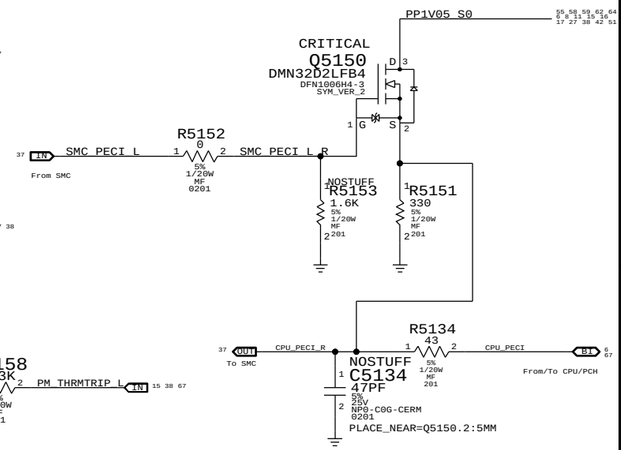


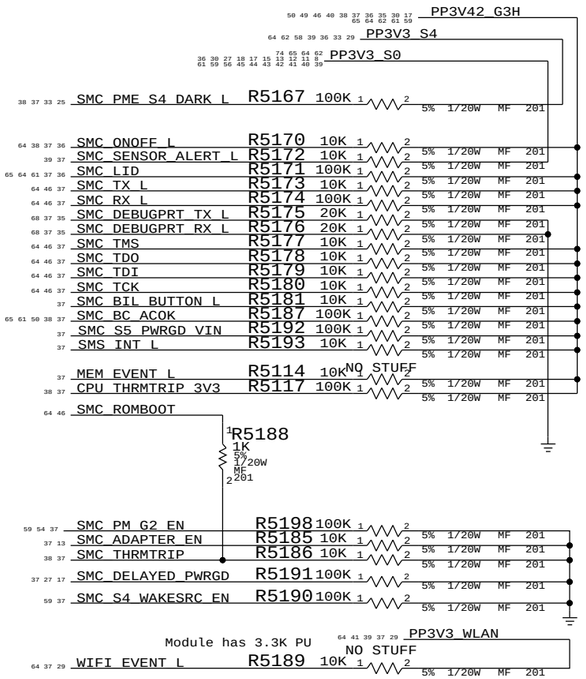






SMC12 PECI Support





SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

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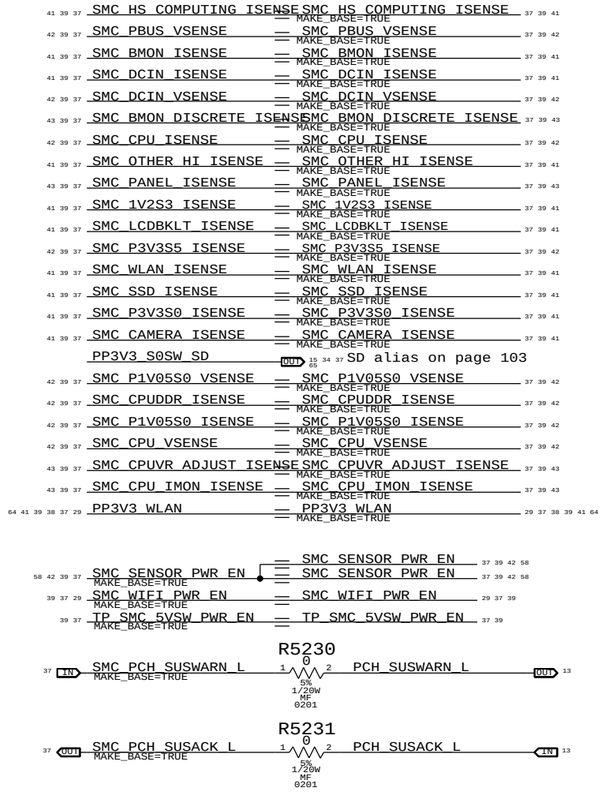
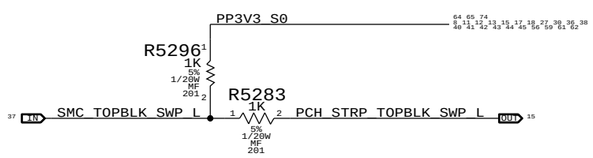
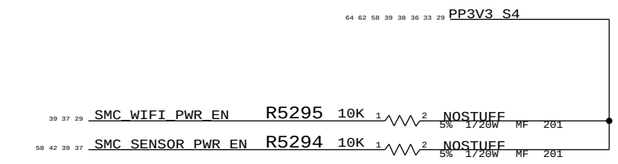
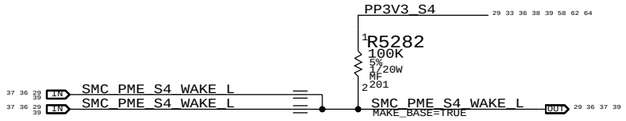
8	7	6	5	4	3	2	1

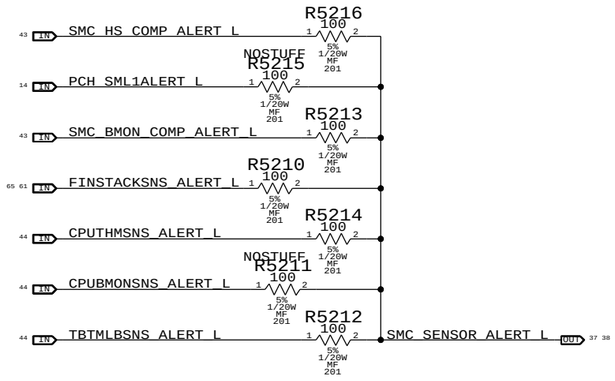


Top-Block Swap









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SMC Project Support

Apple Inc.

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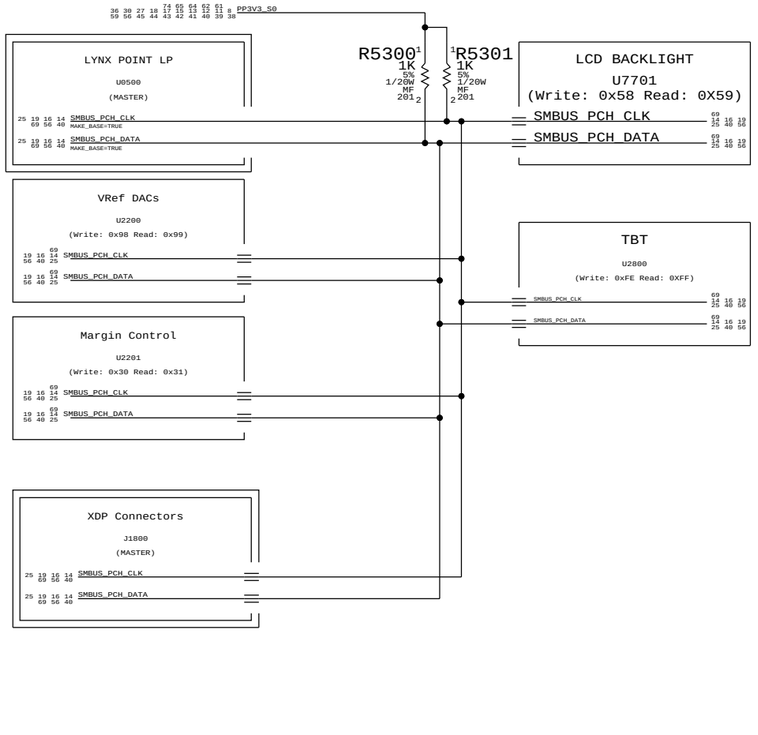
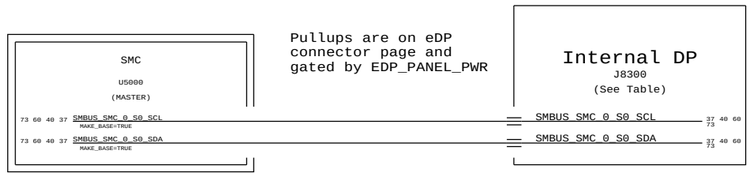
LYNX POINT LP S0 SMBus "0" Connections



SMC "0" SMBus S0 Connections

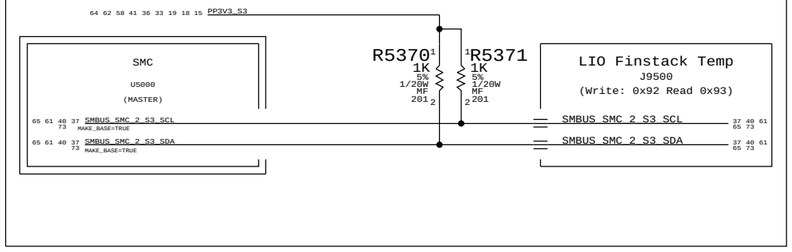


(* = Multiple options)

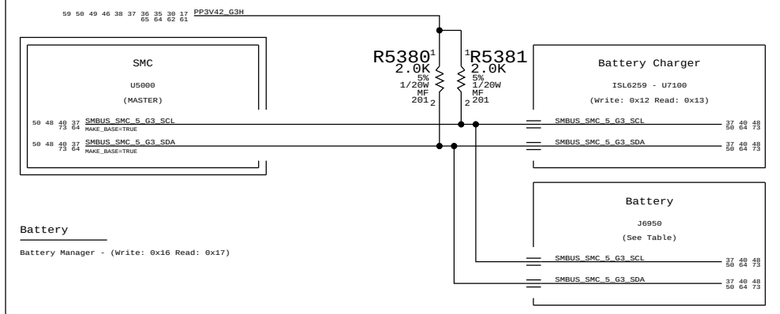
Internal DP

	J43		J41		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

SMC "2" SMBus S3 Connections



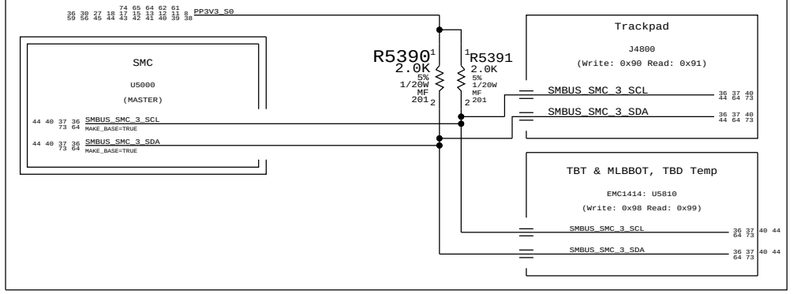
SMC "5" SMBus G3H Connections



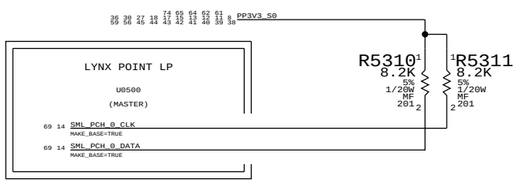
Battery

Battery Manager - (Write: 0x16 Read: 0x17)

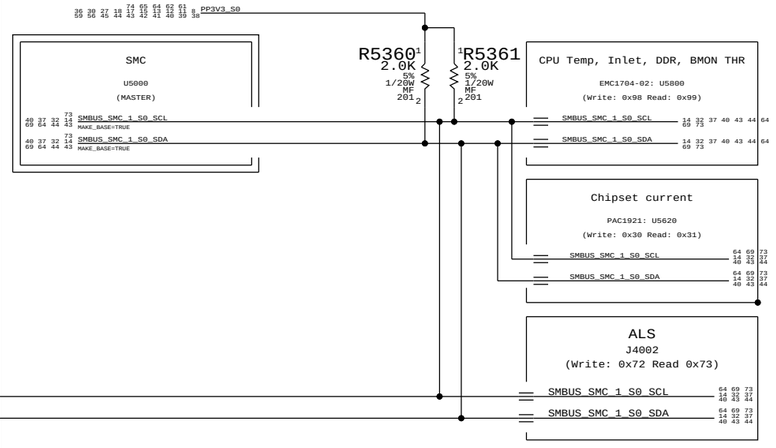
SMC "3" SMBus S0 Connections



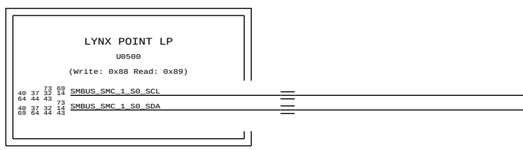
LYNX POINT LP S0 "SMLink 0" Connections



SMC S0 "1" SMBus Connections



LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to
access PCH

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SMBus Connections

Apple Inc.

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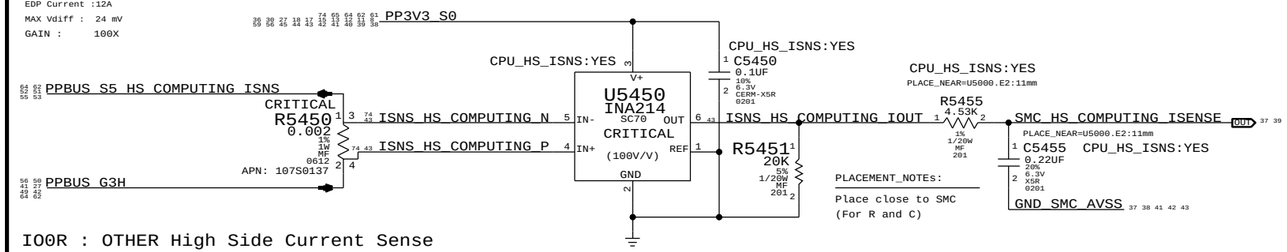
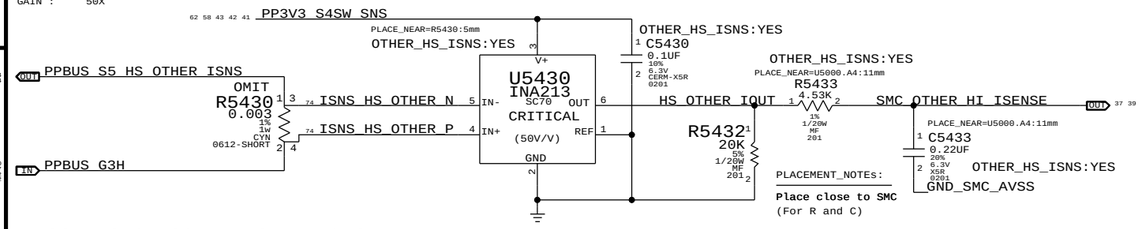
IC0R : COMPUTING High Side Current Sense

EDP Current :12A
MAX Vdiff : 24 mV
GAIN : 100X



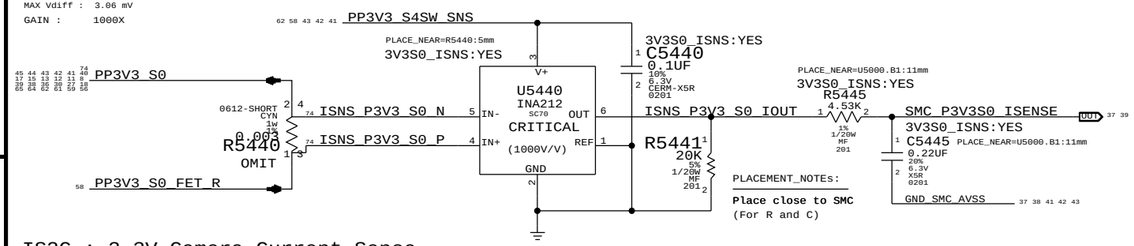
IO0R : OTHER High Side Current Sense

EDP Current :10.75A
MAX Vdiff : 53.75 mV
GAIN : 50X



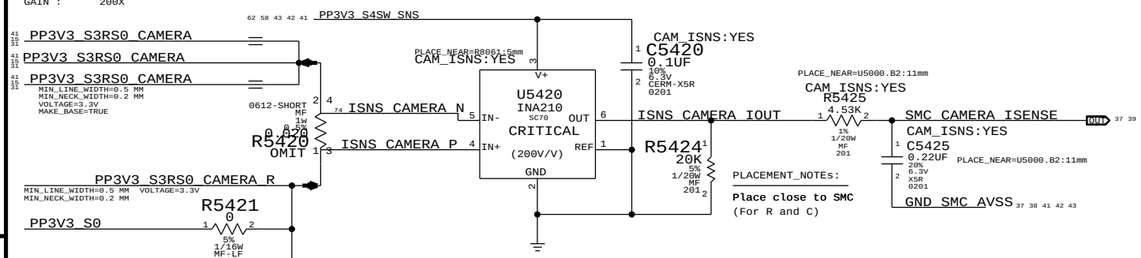
IR0C : 3.3V S0 FET Current Sense

EDP Current :1.02A
MAX Vdiff : 3.06 mV
GAIN : 1000X

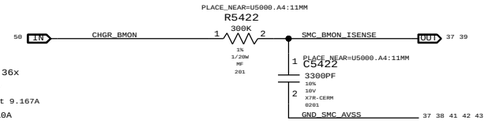


IS2C : 3.3V Camera Current Sense

EDP Current : 0.82A
MAX Vdiff : 16.36 mV
GAIN : 200X

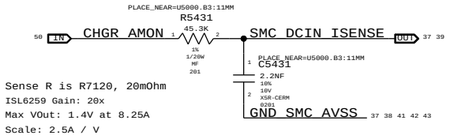


CHARGER BMON High Side Current Sense



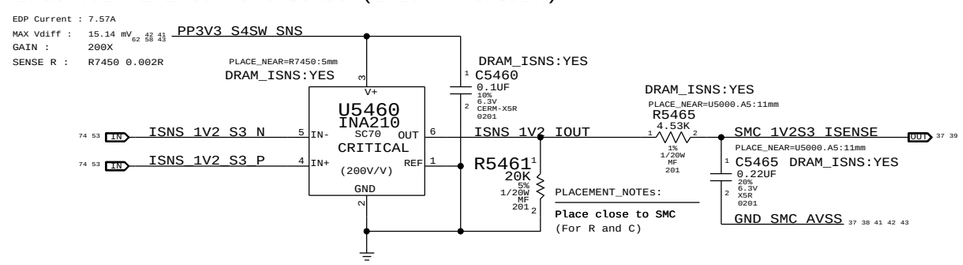
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES,SENSE,0.003OHM,1W,4-TERM,1%,0612,TFT	R5480	CRITICAL	

DC-IN (AMON) Current Sense



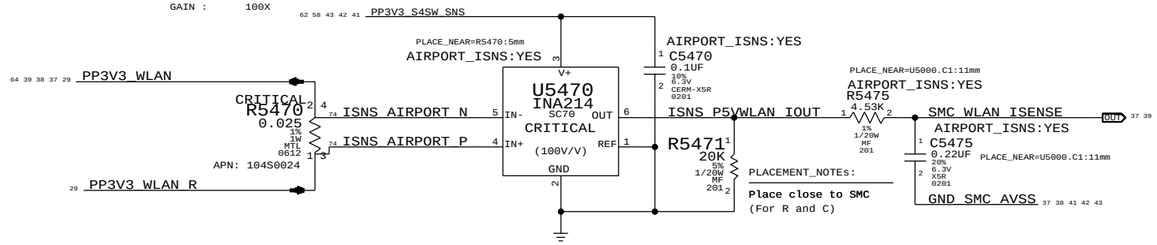
IM3C :DDR 1V2 Current Sense (LPDDR + CPUDDR)

EDP Current : 7.57A
MAX Vdiff : 15.14 mV
GAIN : 200X
SENSE R : R7450 0.002R



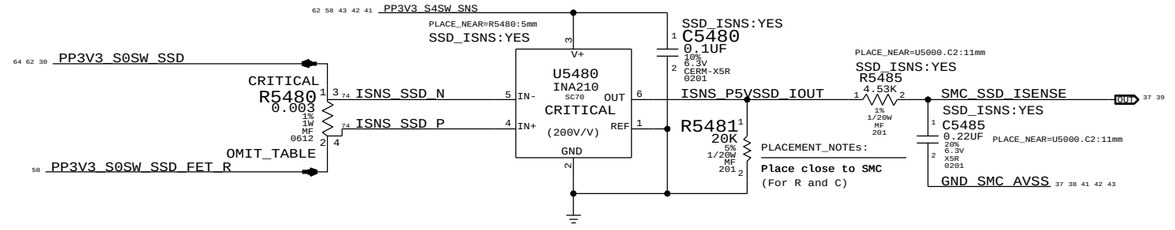
IAPC :AirPort Current Sense

EDP Current : 1.00A
MAX Vdiff : 25 mV
GAIN : 100X



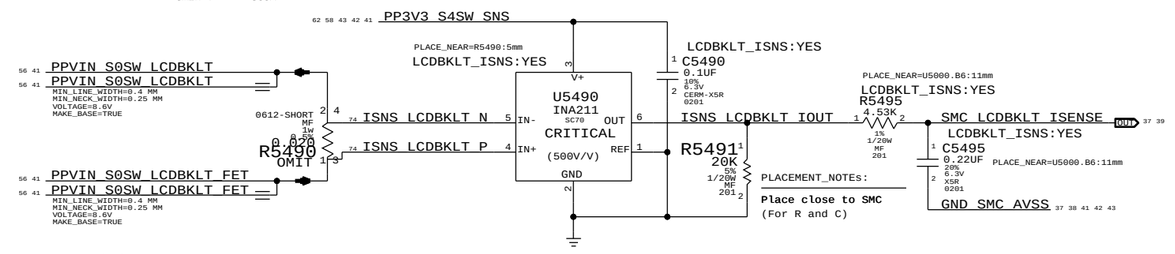
ISDC : SSD Current Sense

EDP Current : 3.00A
MAX Vdiff : 15 mV
GAIN : 200X



IBLC : LCD Backlight Driver Input Current Sense

EDP Current : 0.67A
MAX Vdiff : 0.06 mV
GAIN : 500X



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		SSD_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

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High Side Current Sensing

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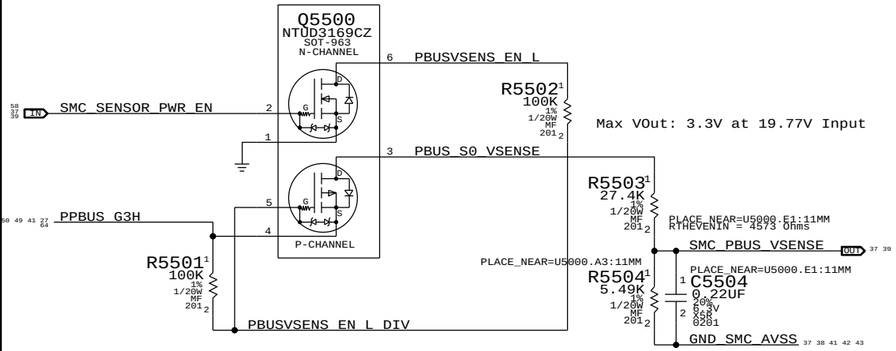
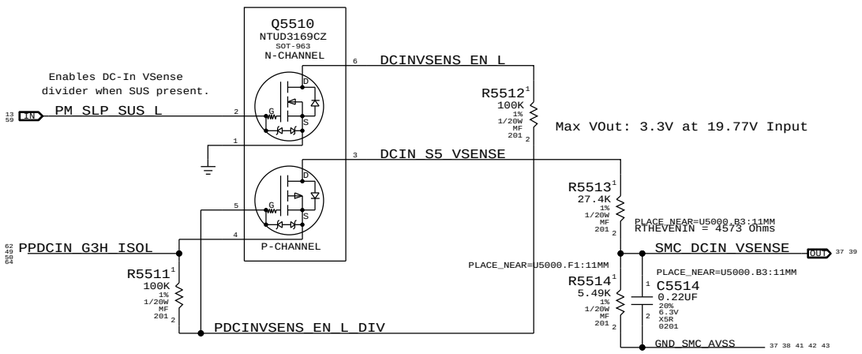
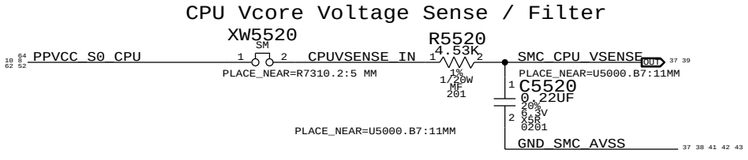
VP0R: PBUS Voltage Sense Enable & Filter



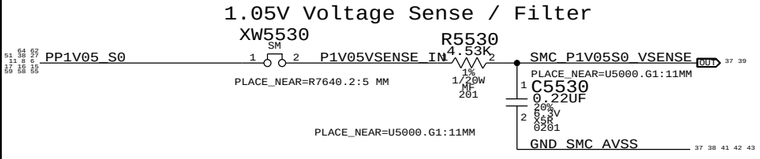
VD0R: DC-In Voltage Sense Enable & Filter



CPU Vcore Voltage Sense / Filter

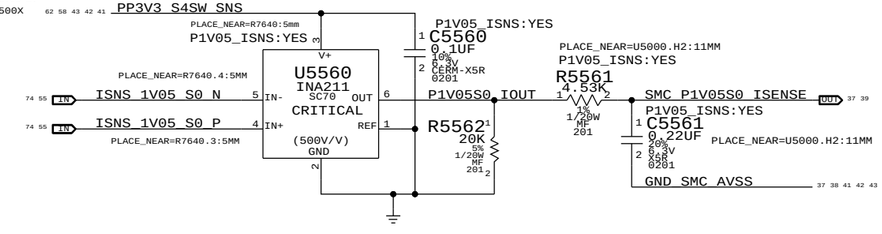


1.05V Voltage Sense / Filter

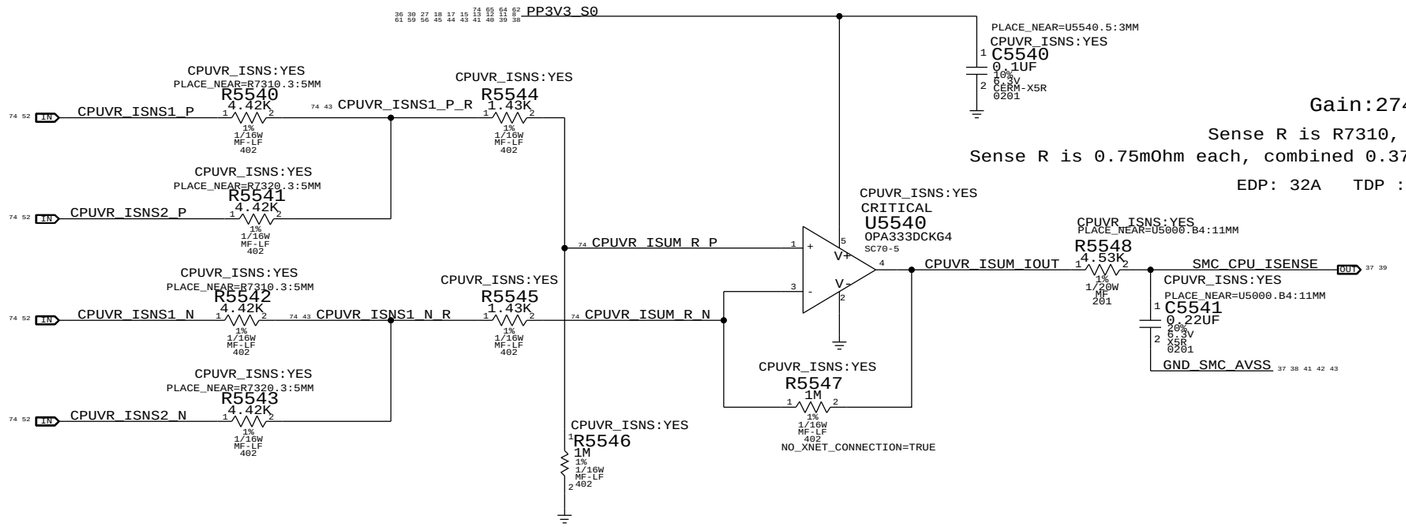


IC1C: 1.05V S0 CURRENT SENSE / FILTER

EDP Current : 1A
MAX Vdiff : 5.65 mV
GAIN : 500X

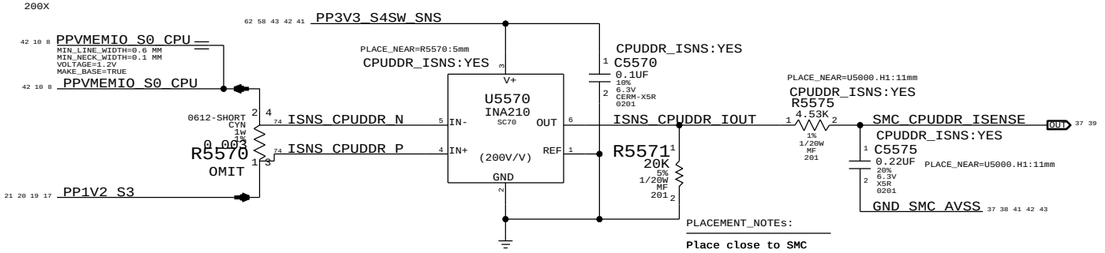


ICS0 : CPU VCore Load Side Current Sense



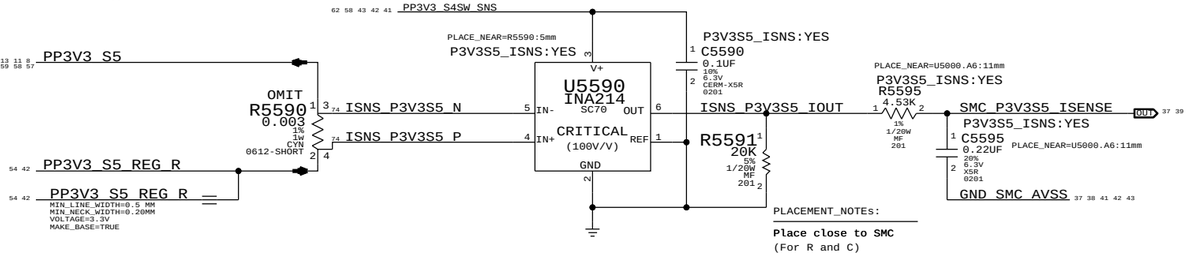
IM0C : CPU DDR Current Sense

EDP Current : 3.00A
MAX Vdiff : 12.60 mV
GAIN : 200X



IR5C :3.3 S5 REG Current Sense

EDP Current : 3.00A
MAX Vdiff : 30.00 mV
GAIN : 100X



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5541		CPUVR_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5561		P1V05_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5595		P3V3S5_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5575		CPUDDR_ISNS:NO

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Voltage & Load Side Current Sensing

Apple Inc.

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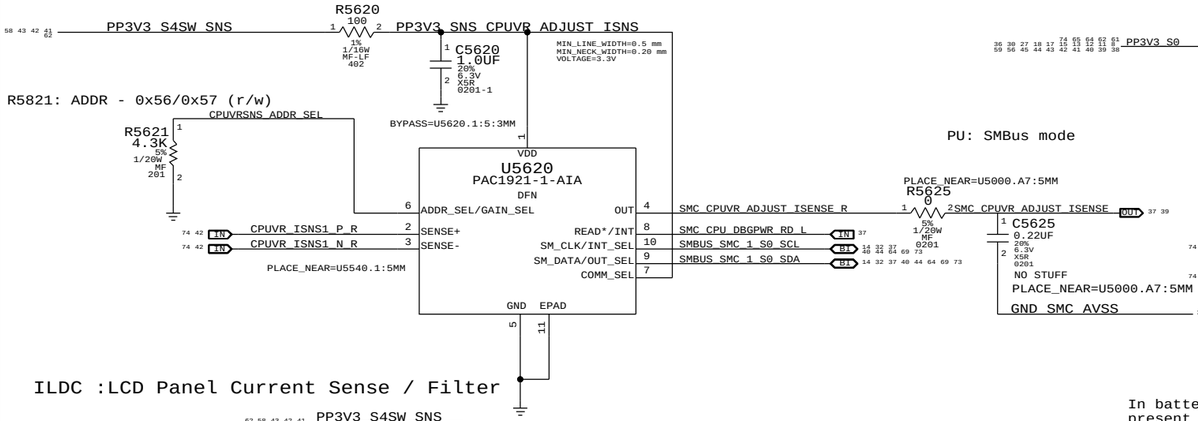
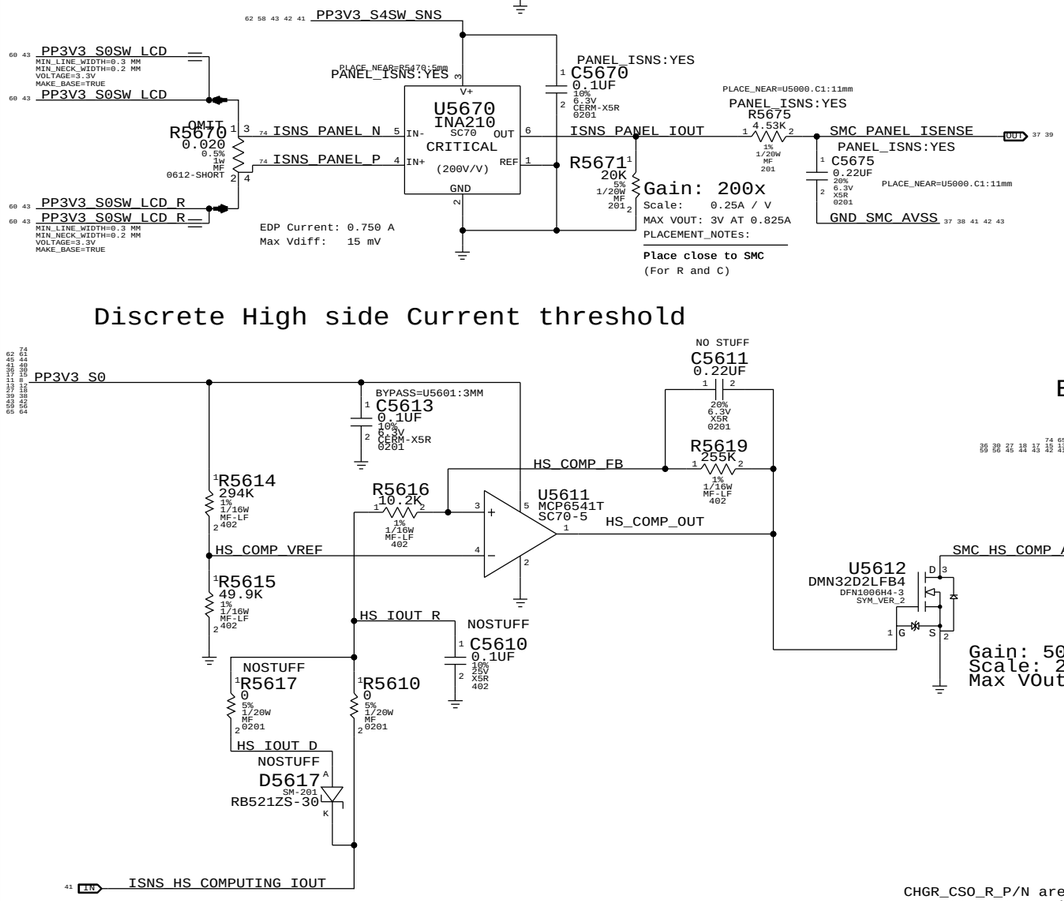
ICS3 : Adjustable Gain CPU VR Current



ILDC :LCD Panel Current Sense / Filter

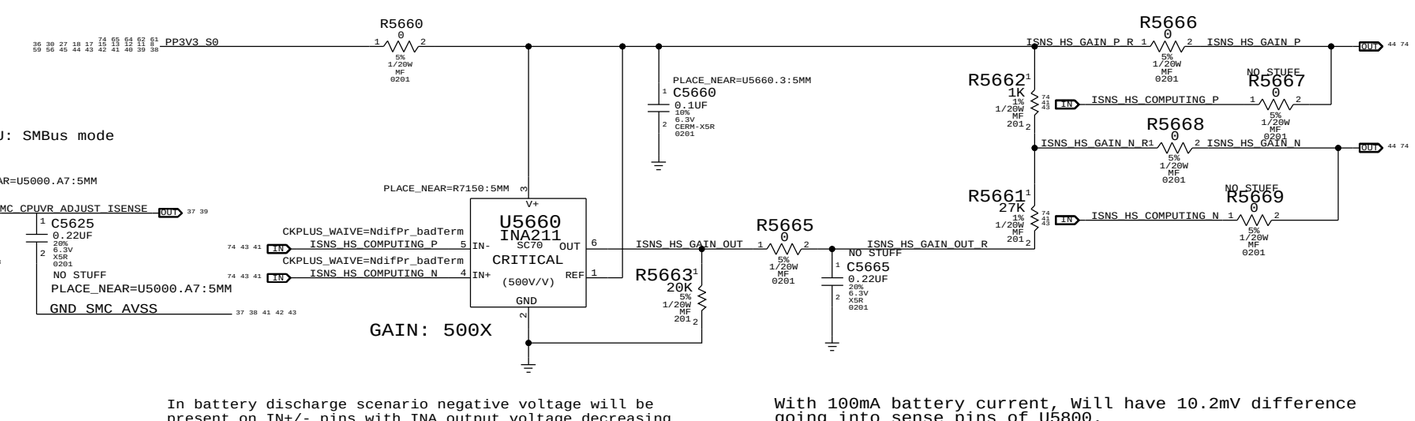


Discrete High side Current threshold

Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5675		PANEL_ISNS:NO

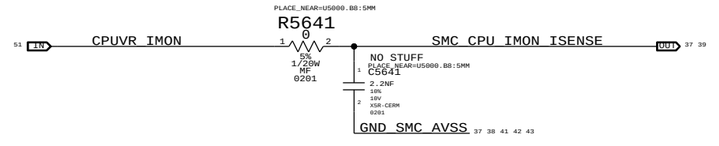
Sense Pins gain stage for U5800 (EMC1704)



In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

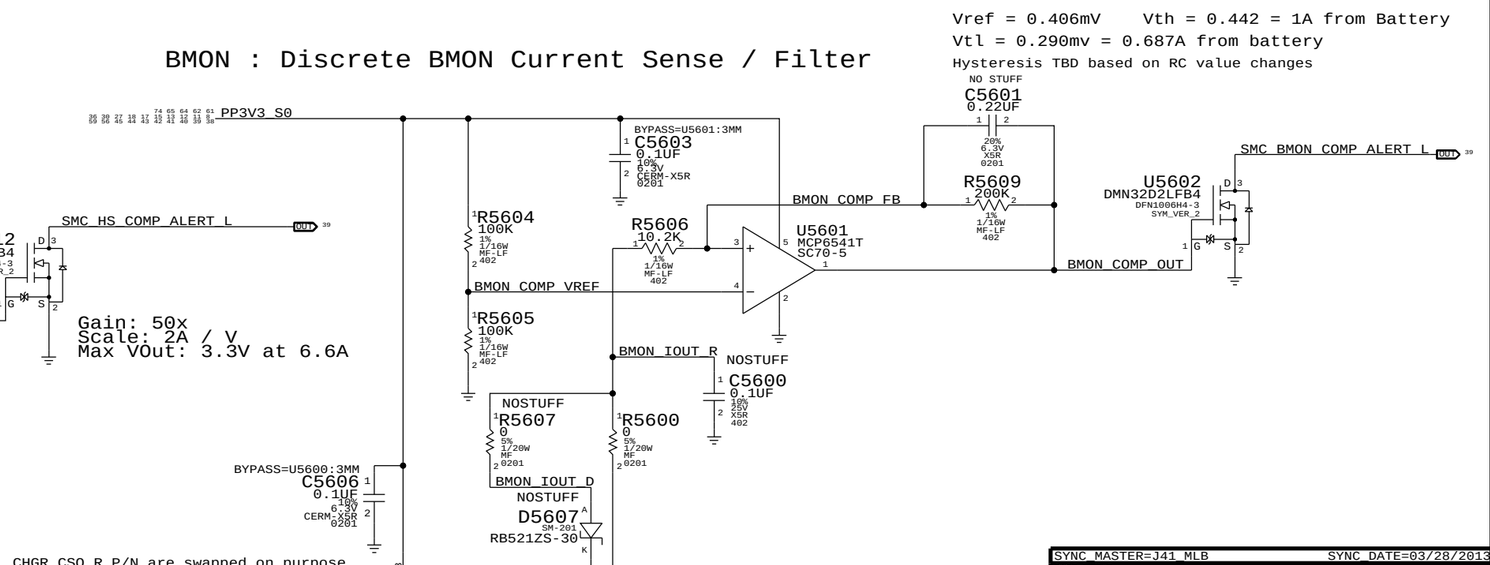
With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800.
This will set the minumum current threshold at 0.100mA

VR IMON Current Sense Filter



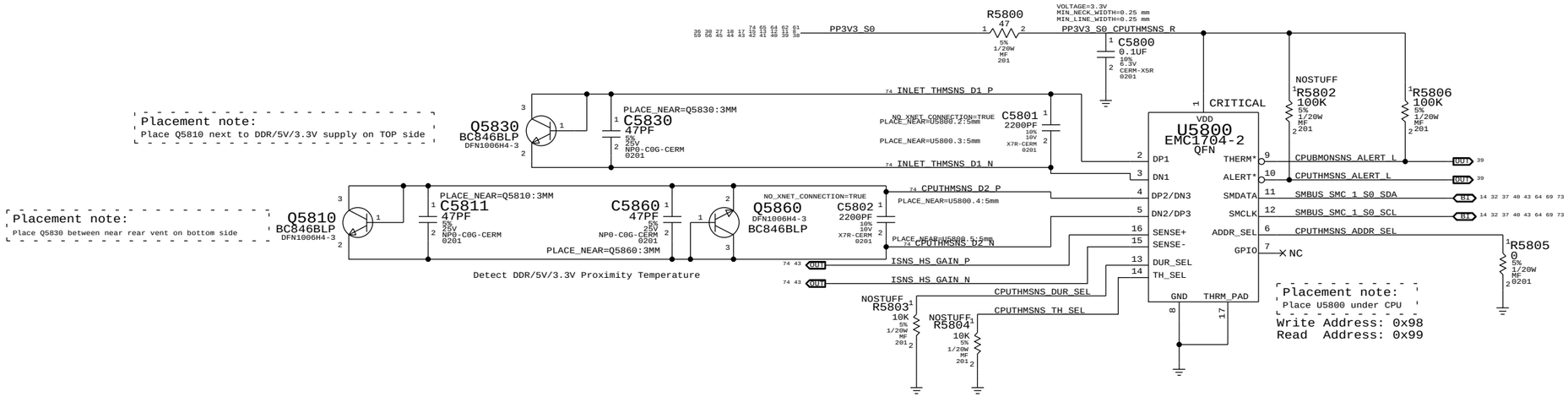
Vref = 0.406mV Vth = 0.442 = 1A from Battery
Vtl = 0.290mv = 0.687A from battery
Hysteresis TBD based on RC value changes

BMON : Discrete BMON Current Sense / Filter

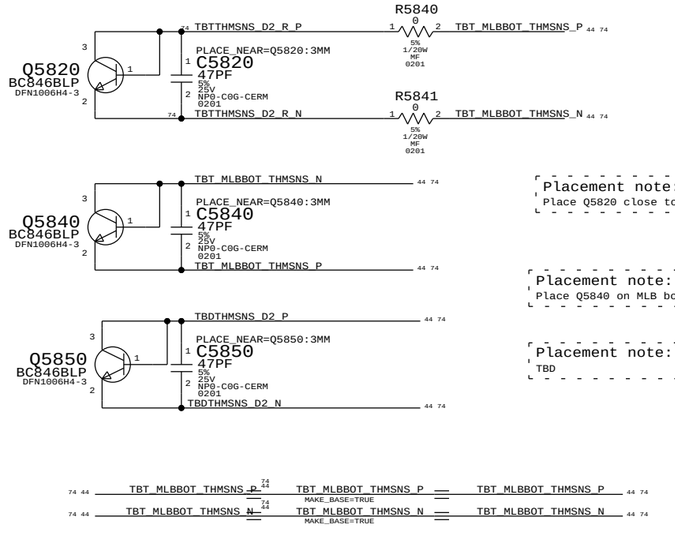


SYNC_MASTER=J41_MLB	SYNC_DATE=03/28/2013
PAGE TITLE	Debug Sensors 1
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 56 OF 121
	SHEET 43 OF 76

CPU Proximity, Inlet ,DDR and BMON THR Sensor



TBT,MLB Bottom Proximity Sensors



Placement note:
Place Q5820 close to TBT on TOP side

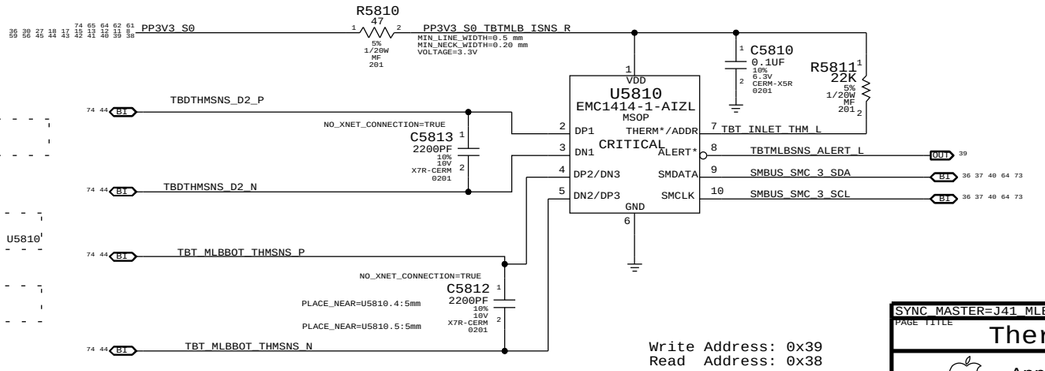
Placement note:
Place Q5840 on MLB bottom side opposite U5810

Placement note:
TBD

TBT_MLBBOT_THMSNS_P — MAKE_BASE=TRUE — TBT_MLBBOT_THMSNS_P

TBT_MLBBOT_THMSNS_N — MAKE_BASE=TRUE — TBT_MLBBOT_THMSNS_N

TBT, MLBBOT and TBD Temp Sensor



Write Address: 0x39
Read Address: 0x38

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

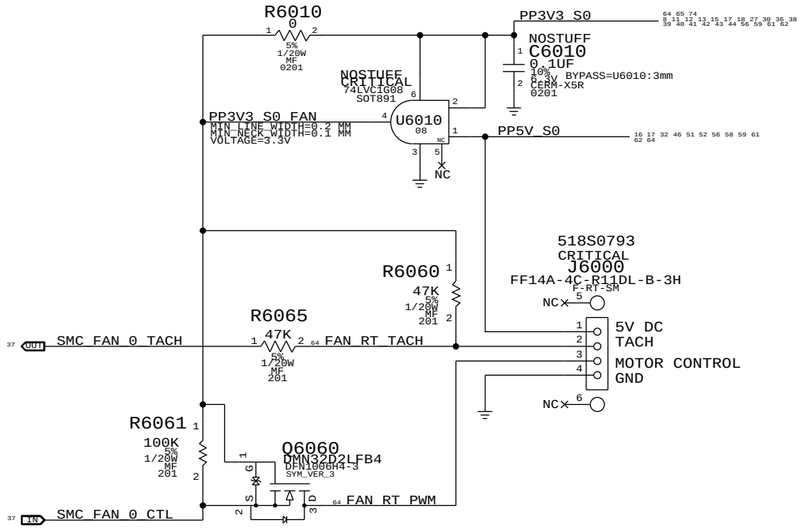
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 58 OF 121

SHEET: 44 OF 76

FAN CONNECTOR



SYNC_MASTER=J41_MLB	SYNC_DATE=02/06/2013
PAGE TITLE: Fan	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 60 OF 121
	SHEET: 45 OF 76

DUAL I/O MODE (MODE 0 & 3) SUPPORTED
High Speed CLK Frequency - 50MHz for fast read dual I/O

PP3V3_SUS

R6102 100K 5% 1/20W MF 201

R6101 3.3K 5% 1/20W MF 201

C6100 0.1UF 10% 16V X5R-CERM 0201 (BYPASS=U6100:3mm)

U6100 64MBIT WSON
SST25VF064C
OMIT_TABLE
VDD, VSS, THRM_PAD

- SPI_MLB_CLK → SCK
- SPI_MLB_CS_L → CE*
- SPI_WP_L → WP*
- SPIROM_USE_MLB → RST*/HOLD*
- SI/SIO0 → SPI_MLB_MOSI
- SO/SOI1 → SPI_MLB_MISO

NOTE: If HOLD* is asserted
ROM will ignore SPI cycles.

LPC+SPI Connector

LPCPLUS CRITICAL
J6100 DF40C-30DP-0.4V M-ST-SM

PP3V42_G3H	31	32	
PP5V_S0	33	34	
LPC_CLK24M_LPCPLUS	3	4	LPC_FRAME_L
LPC_AD<0>	5	6	SPIROM_USE_MLB
LPC_AD<2>	9	10	PM_CLKRUN_L
LPC_AD<1>	11	12	SPI_ALT_CLK
LPC_AD<3>	13	14	SPI_ALT_CS_L
SPI_ALT_MOSI	15	16	LPC_SERIRQ
XDP_LPCPLUS_GPIO	17	18	LPC_PWRDWN_L
LPCPLUS_RESET_L	19	20	SMC_TDI
SMC_TDO	21	22	SMC_TCK
TP_SMC_TRST_L	23	24	SMC_RESET_L
TP_SMC_MD1	25	26	SMC_ROMBOOT
SMC_TX_L	27	28	SMC_RX_L
	29	30	SMC_TMS

516S1039

SPI Bus Series Termination

CPU Master

SPI_CS0_R_L	R6110 15	SPI_CS0_L	PLACE_NEAR=U0500.Y7:5mm
SPI_CLK_R	R6111 15	SPI_CLK	PLACE_NEAR=U0500.AA3:5mm
SPI_MOSI_R	R6112 15	SPI_MOSI	PLACE_NEAR=U0500.AA2:5mm
SPI_MISO	R6113 15	SPI_MISO_R	PLACE_NEAR=U0500.AA2:5mm

Matt Card ROM Slave

SPI_ALT_MISO	R6128 24.9	PLACE_NEAR=J6100.2:5mm
SPI_ALT_MOSI	R6127 43	PLACE_NEAR=J6100.15:5mm
SPI_ALT_CLK	R6126 43	PLACE_NEAR=J6100.12:5mm
SPI_ALT_CS_L	R6125 43	PLACE_NEAR=J6100.14:5mm

MLB ROM Slave

SPI_CS0_L	R6120 43	PLACE_NEAR=R6125.2:5mm → SPI_MLB_CS_L
SPI_CLK	R6121 43	PLACE_NEAR=R6126.2:5mm → SPI_MLB_CLK
SPI_MOSI	R6122 43	PLACE_NEAR=R6127.2:5mm → SPI_MLB_MOSI
SPI_MISO_R	R6123 24.9	PLACE_NEAR=U6100.2:5mm → SPI_MLB_MISO

SMC12 Master

SPI_SMC_MISO	R6114 24.9	PLACE_NEAR=U6100.2:1mm
SPI_SMC_MOSI	R6115 15	PLACE_NEAR=U6100.5:1mm
SPI_SMC_CLK	R6116 15	PLACE_NEAR=U6100.6:1mm
SPI_SMC_CS_L	R6117 15	PLACE_NEAR=U6100.1:1mm

SYNC_MASTER=J41_MLB SYNC_DATE=04/02/2013

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

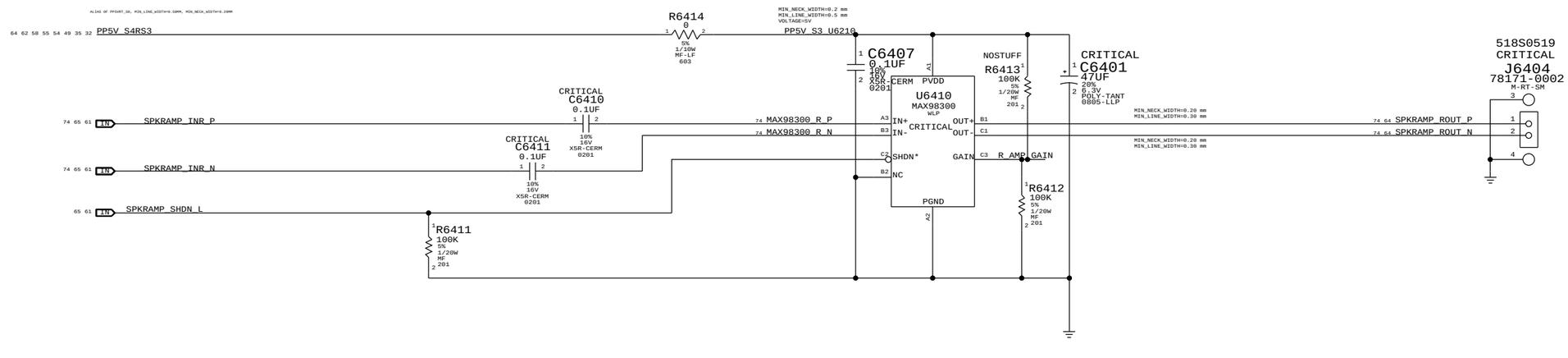
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 61 OF 121
SHEET: 46 OF 76

SPEAKER AMPLIFIERS

APN:353S2888

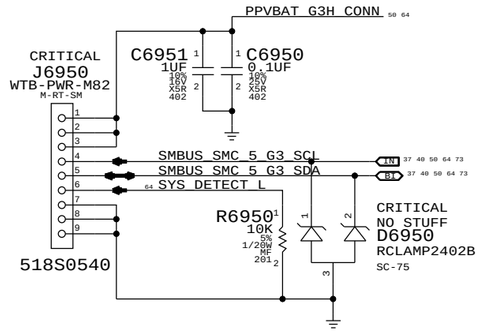
SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB

Right Speaker Connector



SYNC_MASTER=J41_MLB	SYNC_DATE=02/06/2013
PAGE TITLE	Audio: Speaker Amp
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 64 OF 121
	SHEET 47 OF 76

13" SPECIFIC
Battery Connector



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Battery Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 69 OF 121
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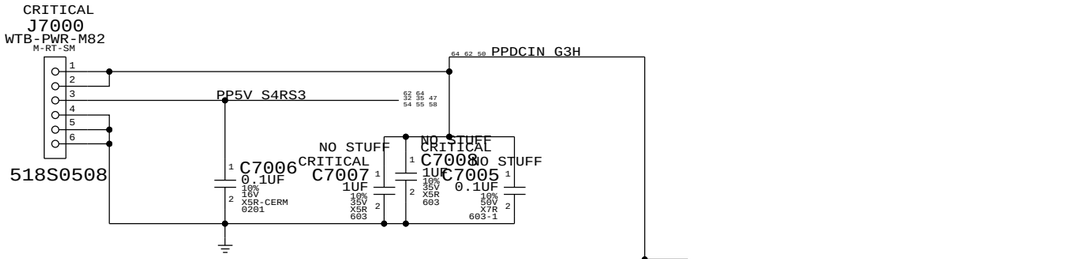
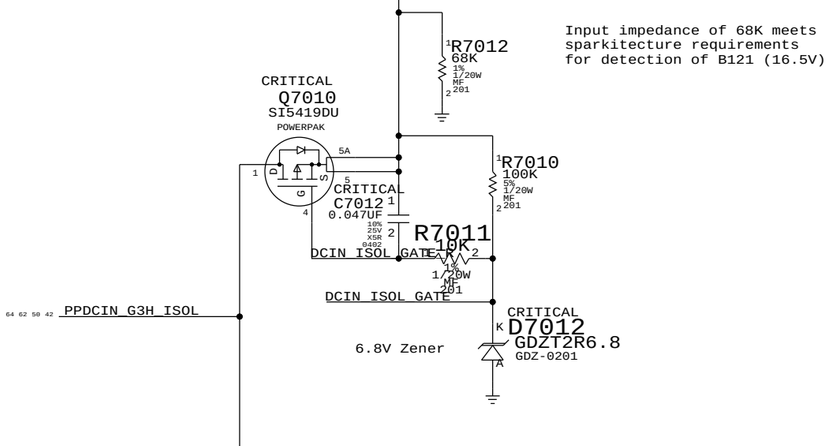
MLB to LIO Power Cable Connector





SYNC_MASTER=J41_MLB	SYNC_DATE=02/06/2013
PAGE TITLE	DC-In & G3H Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 70 OF 121
	SHEET 49 OF 76

Reverse-Current Protection

Need to stuff R7192 if either PP5V5_DCIN:YES or PP5V5_VDDP are used!

Inrush Limiter

FROM ADAPTER

64 62 49 PPDCIN_G3H

R7185 470K 1/20W MF 201

C7185 0.1UF 10% 25V X5R 402

CRITICAL Q7180 IRF9395TRPBF DIRECTFET-MC

CHGR_AGATE_DIV

R7186 332K 1% 1/20W MF 201

64 62 49 42 PPDCIN_G3H_ISOL

CRITICAL D7105 BAT30CWFILM SOT-323

MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm

PPDCIN_G3H_INRUSH

MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=18.5V

R7180 100K 5% 1/20W MF 201

C7184 4.7UF 10% 25V X5R-CERM 0603

CHGR_SGATE_DIV

MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm

R7181 62K 5% 1/20W MF 201

(CHGR_AGATE)

(CHGR_SGATE)

MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm

PP5V5_DCIN:NO

R7105 20 5% 1/10W MF-LF 603

50 PPCHGR_DCIN_D_R

MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=18.5V

(CHGR_DCIN)

MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.2 mm

ACIN pin threshold is 3.2V, +/- 50mV

DIVIDER SETS ACIN THRESHOLD AT 13.55V

30mA max load

PP5V1_CHGR_VDD

MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm VOLTAGE=5.1V

R7101 4.7 5% 1/16W MF-LF 402

48 PP5V1_CHGR_VDDP

MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=5.1V

C7101 1UF 10% 10V X5R 402

59 49 46 40 38 37 36 35 30 17 65 64 62 61 PP3V42_G3H

R7110 130K 1% 1/20W MF 201

NO STUFF R7102 100K 5% 1/20W MF 201

R7100 0 5% 1/20W MF 0201

64 46 38 37 SMC_RESET_L

CHGR_RST_L

SMBUS_SMC_5_G3_SCL

SMBUS_SMC_5_G3_SDA

CHGR_VFRQ

CHGR_CELL

Float CELL for 1S

CHGR_ACIN

R7113 100 5% 1/20W MF 201

R7115 255K 1% 1/20W MF 201

CHGR_VCOMP_R

R7111 46.4K 1% 1/20W MF 201

C7115 470PF 10% 16V X5R-X7R-CERM 0201

R7142 1K 5% 1/20W MF 201

CHGR_ICOMP_R

R7116 10K 1% 1/20W MF 201

CHGR_VNEG_R

C7116 470PF 10% 16V X5R-X7R-CERM 0201

C7142 0.1UF 10% 6.3V CERM-X5R 0201

C7150 0.47UF 10% 10V X5R 0402

C7111 0.01UF 10% 10V X5R-CERM 0201

C7100 1UF 10% 10V X5R 402-1

C7105 0.22UF 10% 50V X5R-CERM 0603-1

C7126 1000PF 10% 16V X7R-CERM 0201

GND_CHGR_AGND

MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

U7100 ISL6259 TQFN

19	VDD		
20	VDDP		
12	VHST	DCIN	2
13	SMB_RST_N		
11	SCL		
10	SDA		
4	VFRQ		
6	CELL		
3	ACIN		
5	ICOMP		
7	VCOMP		
8	VNEG		
18	CSOP		
17	CSON		
26	SGATE		
1	AGATE		
28	CSIP		
27	CSIN		
25	BOOT		
24	UGATE		
23	PHASE		
21	LGATE		
16	BGATE		
9	AMON		
15	BMON		
14	ACOK		
29	(AGND) THRM_PAD		
22	PGND		

CHGR_RST_L
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
CHGR_VFRQ
CHGR_CELL
CHGR_ACIN
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
73 CHGR_CSO_P
73 CHGR_CSO_N
CHGR_DCIN
CHGR_SGATE
CHGR_AGATE
73 CHGR_CSI_P
73 CHGR_CSI_N
CHGR_BOOT
CHGR_UGATE
CHGR_PHASE
CHGR_LGATE
CHGR_BGATE
CHGR_AMON
CHGR_BMON
SMC_BC_ACOK

20V/V AMON
36V/V BMON
(0.08) ACOK

C7150 0.47UF 10% 10V X5R 0402

C7102 1UF 10% 10V X5R 402

XW7100 SM

PLACE_NEAR=U7100.22:1mm

(GND)

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

R7151 2.2 5% 1/20W MF 201

R7152 0 5% 1/20W MF 0201

73 43 CHGR_CSO_R_P

73 43 CHGR_CSO_R_N

MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm

* R7151 HAS 2.2OHM TO COMPENSATE UNBALANCED VOLTAGE
DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

R7121 10 5% 1/20W MF 201

R7122 10 5% 1/20W MF 201

C7120 0.047UF 10% 16V X7R-CERM 0402

C7122 0.1UF 10% 25V X5R 402

C7121 0.1UF 10% 25V X5R 402

CRITICAL R7120 0.020 0.5% 1W MF-LF 0612

PPDCIN_G3H_CHGR

MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.15 mm VOLTAGE=18.5V

C7125 0.22UF 10% 10V CERM 402

CRITICAL Q7130 RJK03P0DPA WPAK

SWITCH_NODE=TRUE DIDT=TRUE

MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.6 mm VOLTAGE=8.6V

CRITICAL L7130 4.7UH-17A PIMC104T4R7MN-SM

CRITICAL F7140 8AMP-24V 1206

PPBUS_G3H

27 41 42 49 56 62 64

TO SYSTEM

Max Current = 8A

f = 400 kHz

5.5v "G3Hot" Supply For Erp Lot6 spec

50 PPCHGR_DCIN_D_R

NO STUFF R7192 0 5% 1/10W 402

CHGR_DCIN_D

NO STUFF C7190 4.7UF 10% 25V X5R-CERM 0603

U7190 LT3470A DFN

VIN BOOST SHDN* SW BIAS NC FB THRM GND PAD

NO STUFF

CRITICAL

P5V1_BOOST DIDT=TRUE

NO STUFF C7194 0.22UF 10% 16V CERM 402

P5V1_SW

MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm SWITCH_NODE=TRUE DIDT=TRUE

CRITICAL NO STUFF L7195 10UH-20%-0.85A-0.46OHM 2520

P5V1_FB

NO STUFF C7195 22PF 5% 50V NPO-C0G-CERM 0201

NO STUFF <Ra> R7195 681K 1% 1/20W MF 201

NO STUFF <Rb> R7196 200K 1% 1/20W MF 201

Vout = 1.25V * (1 + Ra / Rb)

NO STUFF CRITICAL C7198 10UF 20% 10V X5R 603

NO STUFF CRITICAL C7199 10UF 20% 10V X5R 603

PP5V5_DCIN:YES

R7190 0 5% 1/16W MF-LF 402

CHGR_DCIN 50

PP5V5_VDDP

R7191 0 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP 50

PP5V5_CHGR_VDDP

MIN_NECK_WIDTH=0.25 mm MIN_LINE_WIDTH=0.5 mm VOLTAGE=5.5V

Vout = 5.50V
200MA MAX OUTPUT
(Switcher limit)

Q7155 TO/FROM BATTERY

CRITICAL Q7155 SI7137DP SO-8

R7150 0.01 0.5% 1W MF 0612-4

PPVBAT_G3H_CHGR_R

MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 MM VOLTAGE=8.6V

PPVBAT_G3H_CHGR_REG

MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 MM VOLTAGE=8.6V

PPVBAT_G3H_CONN

48 64

MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.15 mm VOLTAGE=8.6V

C7140 62UF-0.023OHM 20% 11V TANT-POLY CASE-B2S-1

C7141 62UF-0.023OHM 20% 11V TANT-POLY CASE-B2S-1

C7143 62UF-0.023OHM 20% 11V TANT-POLY CASE-B2S-1

C7145 1000PF 10% 16V X7R-CERM 0201

BYPASS=L7130:Q7130:1.5mm

C7135 1UF 10% 25V X5R 603-1

C7136 1UF 10% 25V X5R 603-1

C7137 0.001UF 10% 50V X7R-CERM 0402

BYPASS=Q7130:1.5mm

C7130 33UF-0.060OHM 20% 25V POLY-TANT CASE-D3L

C7131 33UF-0.060OHM 20% 25V POLY-TANT CASE-D3L

C7117 10UF 10% 25V X5R 805

C7114 1UF 10% 25V X5R 603-1

C7113 0.1UF 10% 25V X5R 402

C7112 0.01UF 10% 50V X7R 402

SYNC_MASTER=J41_MLB SYNC_DATE=02/09/2013

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

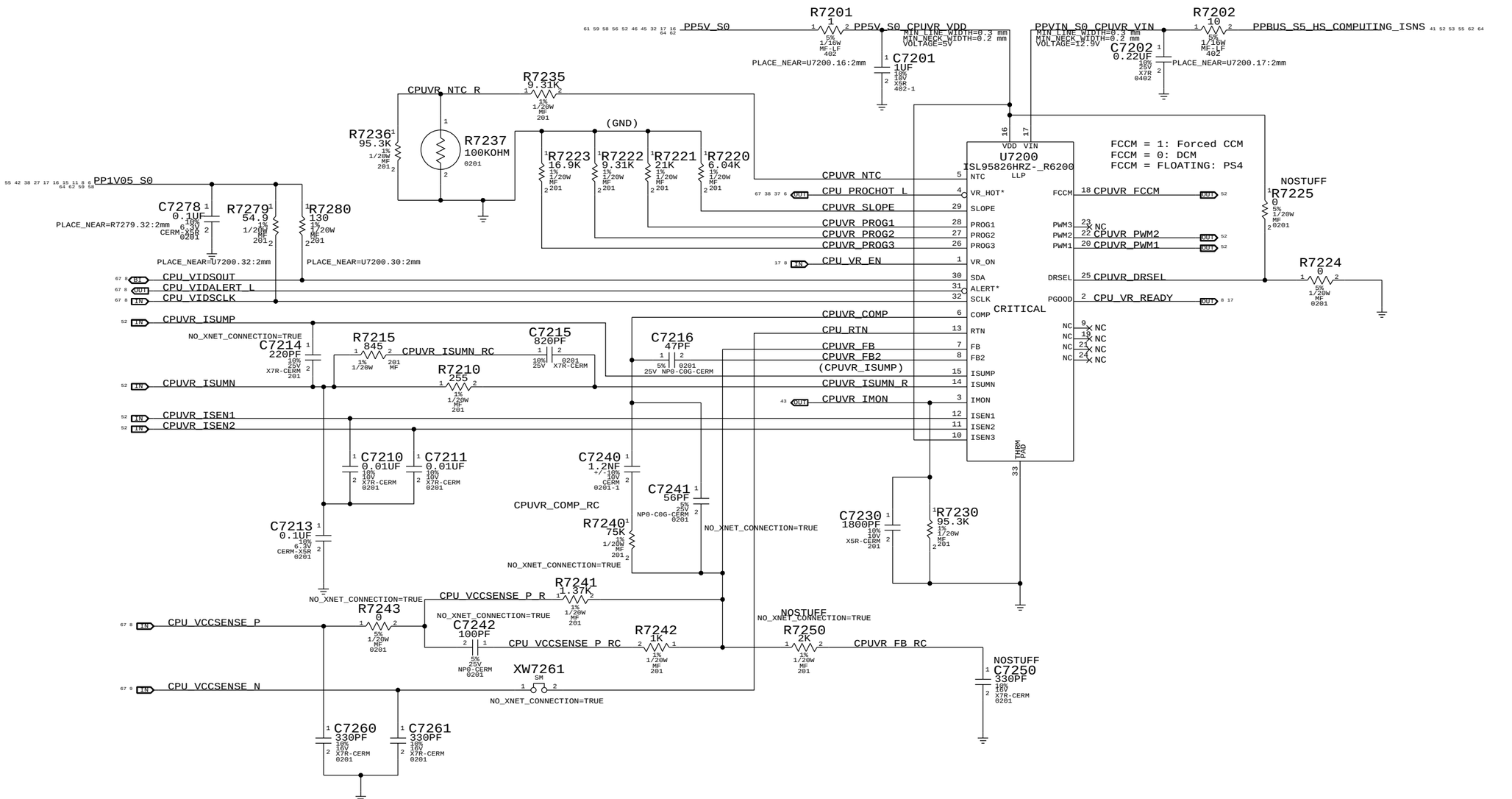
DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 71 OF 121

SHEET: 50 OF 76

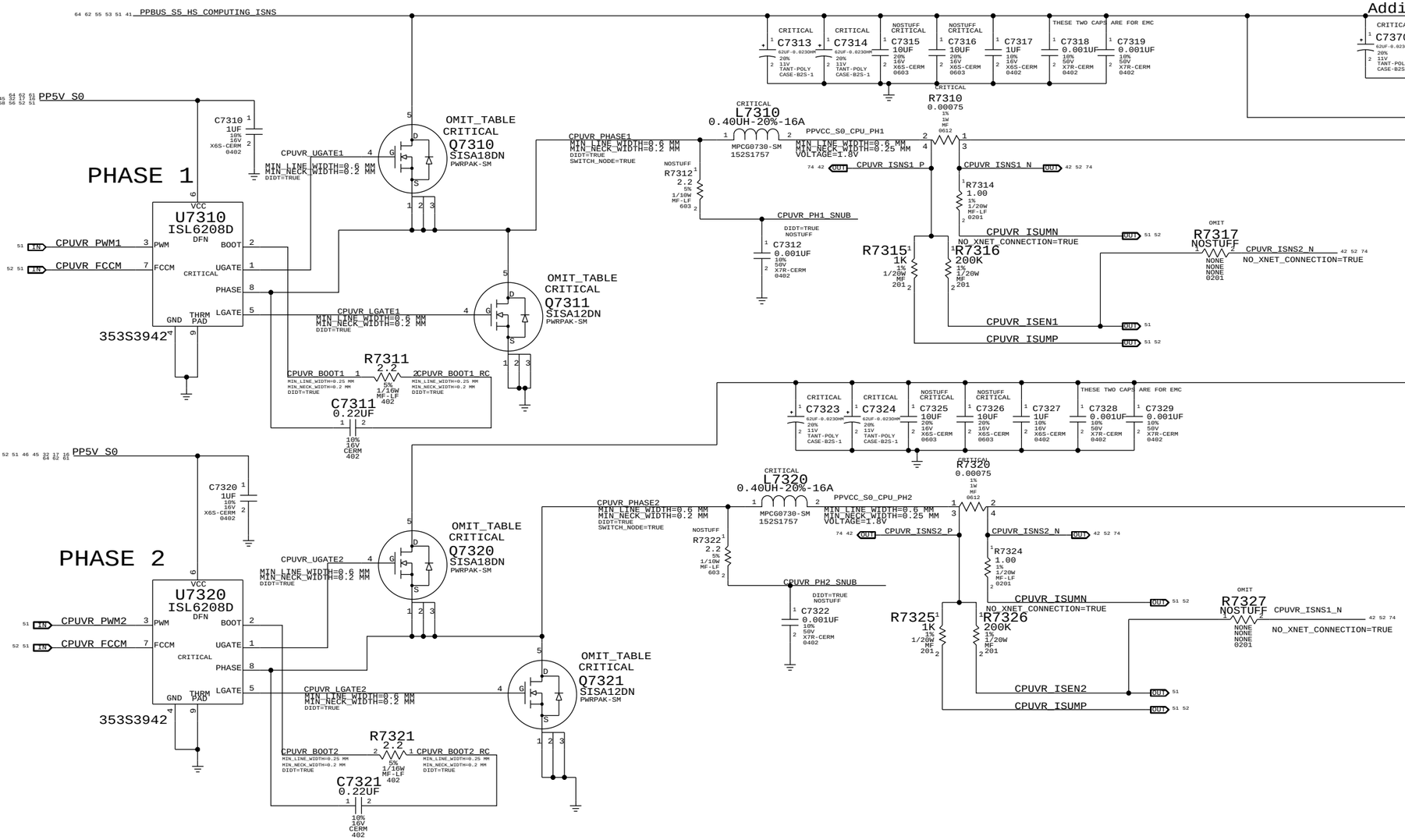


SYNC_MASTER=J41_MLB SYNC_DATE=04/09/2013

PAGE TITLE
CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 72 OF 121
SHEET 51 OF 76

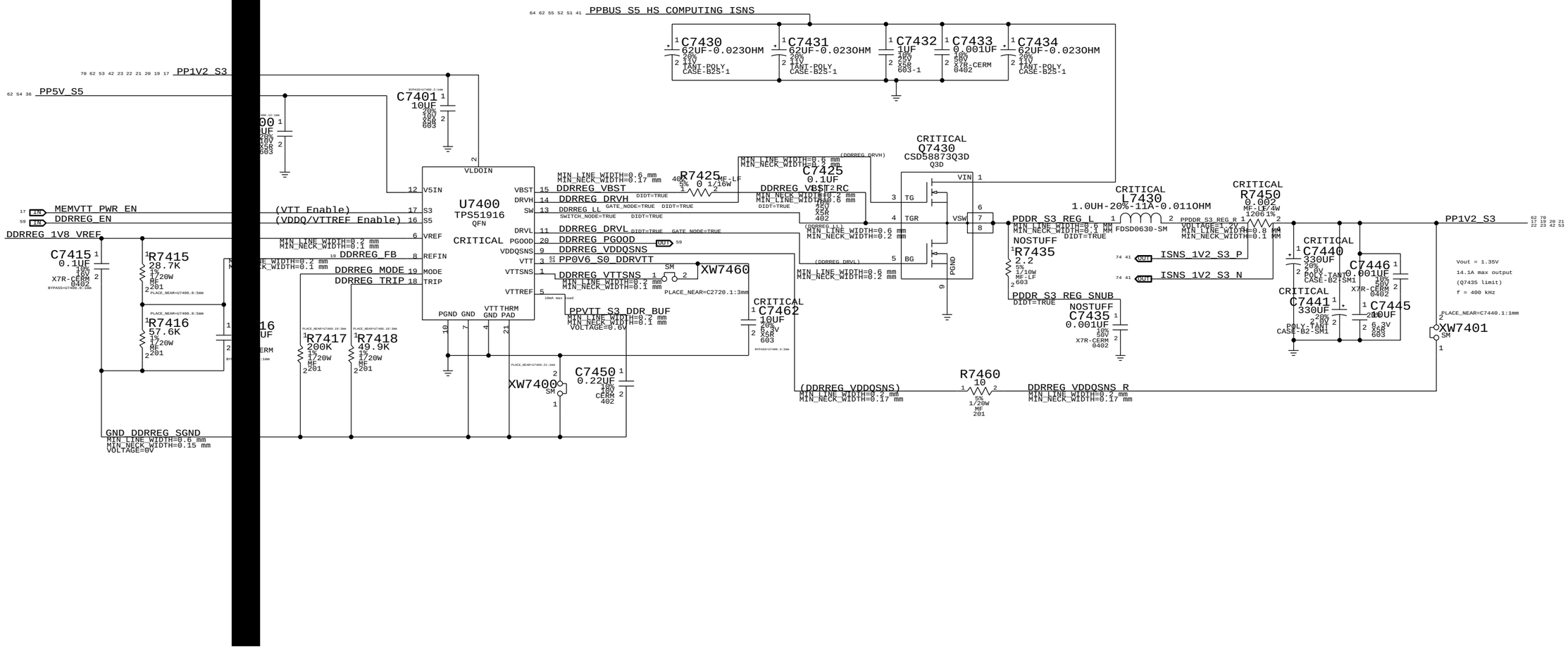


SYNC_MASTER=J41_MLB SYNC_DATE=04/09/2013

PAGE TITLE
CPU VR12.5 VCC Power Stage

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 73 OF 121
SHEET 52 OF 76



SYNC_MASTER=J41_MLB	SYNC_DATE=02/09/2013
PAGE TITLE	LPDDR3 Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 74 OF 121
	SHEET 53 OF 76

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SKIPSEL Strap		
VREF2	Auto Skip	(Higher Efficiency)
VREG3	0OA Auto Skip	(Lower Efficiency)

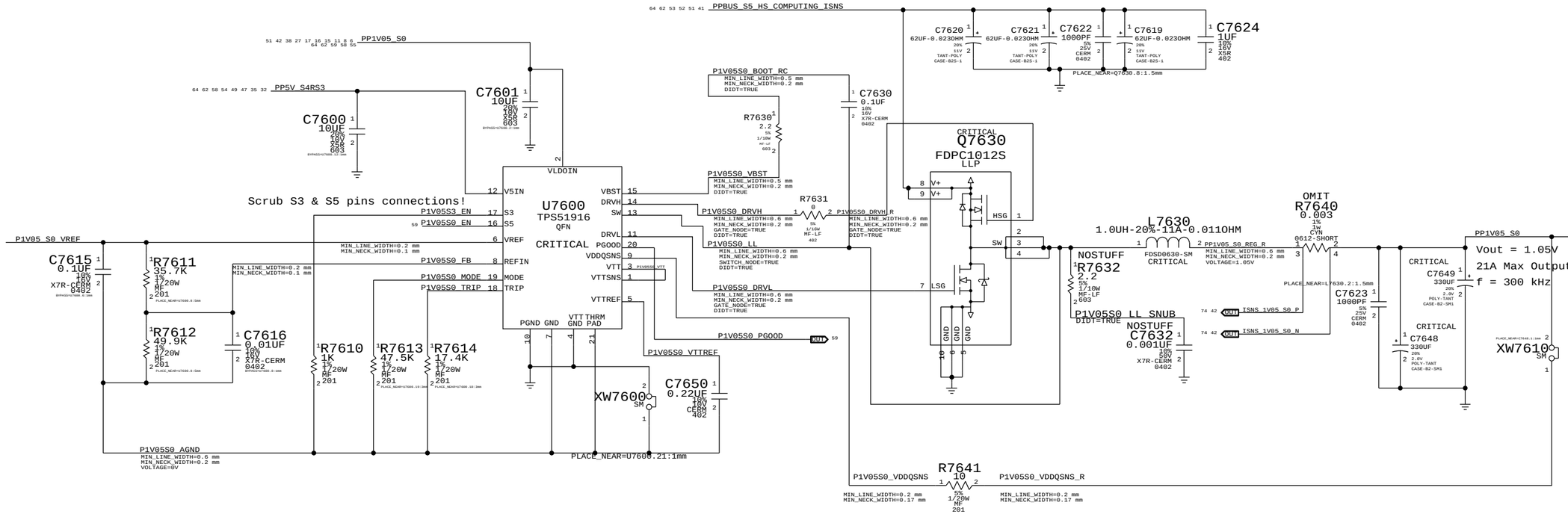
F=400KHZ
Vout = 5.0V
7.2A MAX OUTPUT

Vout = 3.3V
6.5A MAX OUTPUT
F=400KHZ

SYNC_MASTER=J41_MLB	SYNC_DATE=09/17/2012
PAGE TITLE	5V S4RS3 / 3.3V S5 Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 75 OF 121
	SHEET 54 OF 76

Power

1.05V S0 Regulator



SYNC_MASTER=J41_MLB	SYNC_DATE=03/28/2013
PAGE TITLE	1.05V S0 Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 76 OF 121
	SHEET 55 OF 76

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

PPBUS S0 LCDBkLT FET

*C7797 AND C7799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

10.2 ohm resistors for current measurement on LED strings.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R7717,R7718,R7719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R7720,R7721,R7722		BKLT:ENG

Keyboard Backlight Driver & Detection

Keyboard Backlight Connector

PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)

SYNC_MASTER=J41 MLB	SYNC_DATE=02/06/2013
PAGE TITLE	LCD/KBD Backlight Driver
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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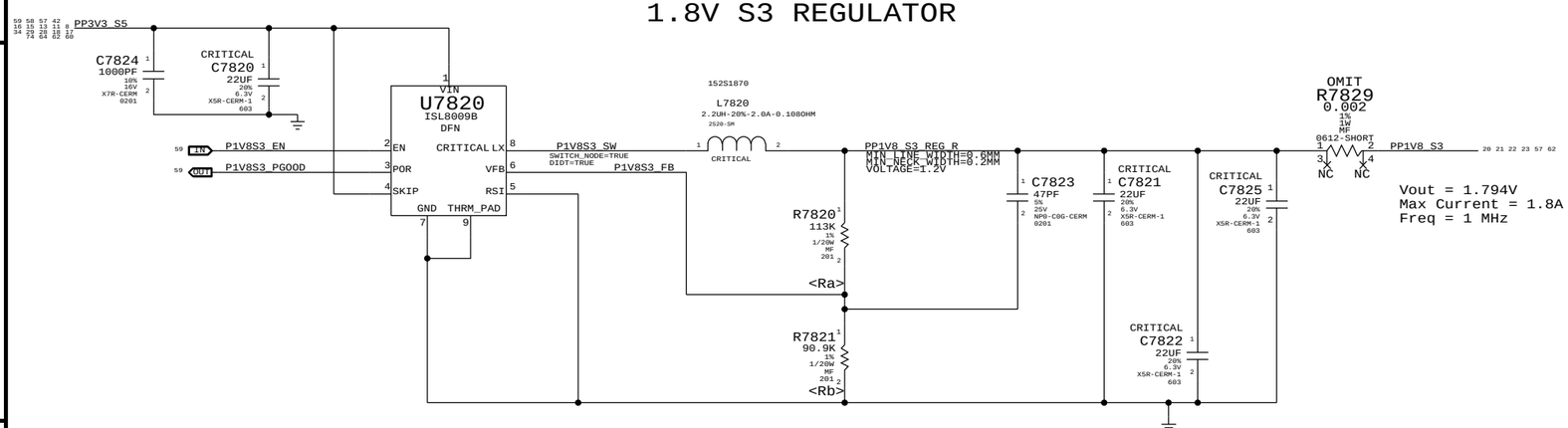
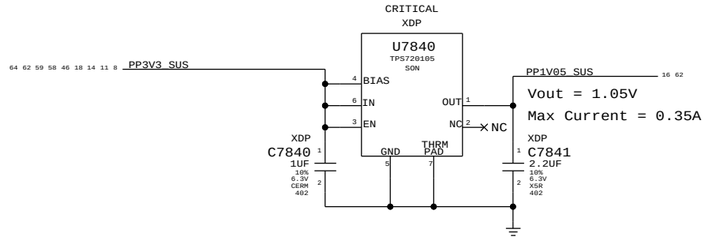
1.8V S3 REGULATOR

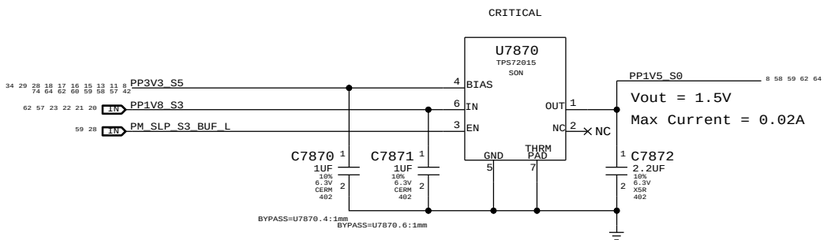


1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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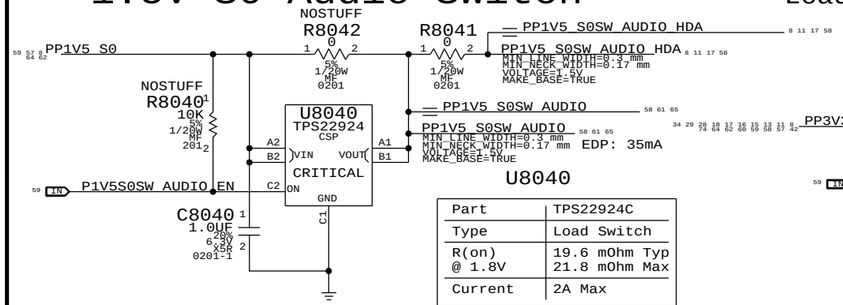
SHEET: 57 OF 76

1.5V S0 Audio Switch

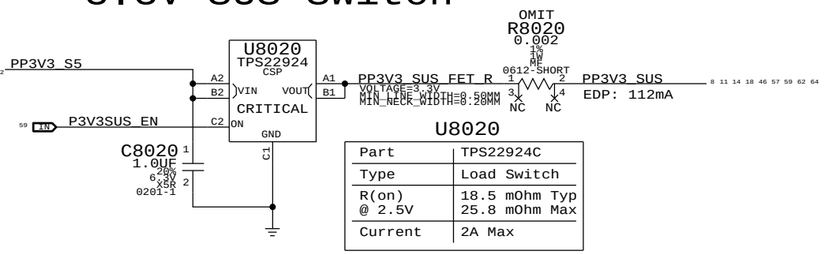
Loading specs per J41/43_PowerBudget_Riviera_rev0.99e



U8040

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

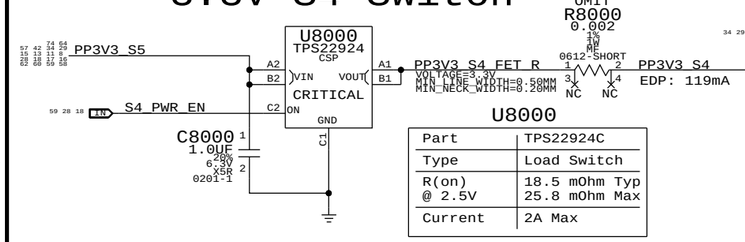
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

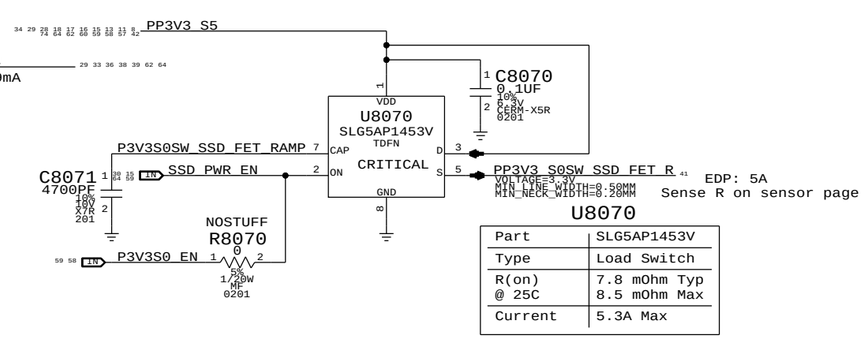
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

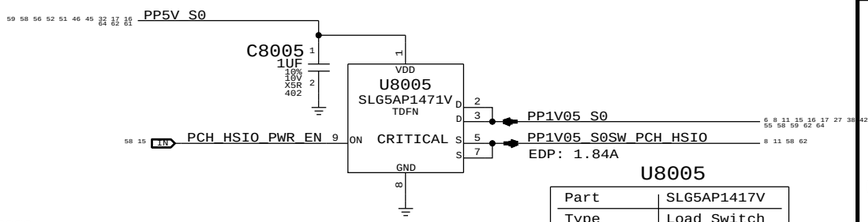
3.3V SSD Switch



U8070

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

1.05V PCH HSIO Switch

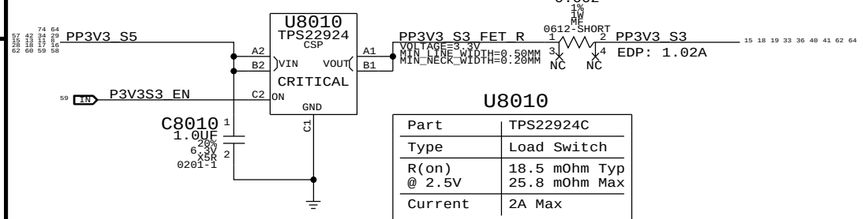


HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

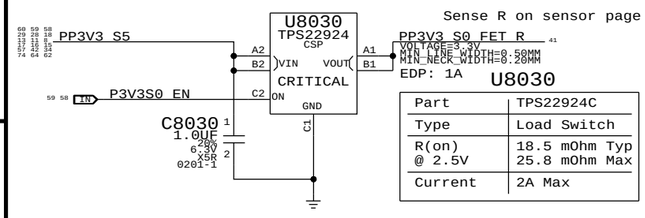
3.3V S3 Switch



U8010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

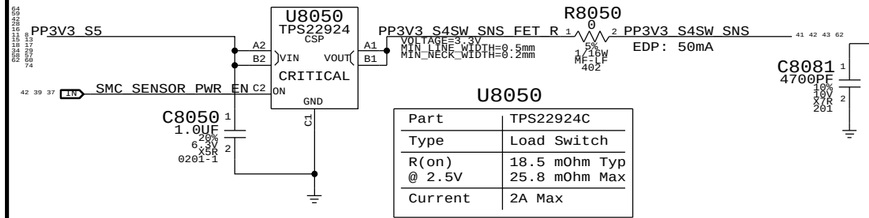
3.3V S0 Switch



U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

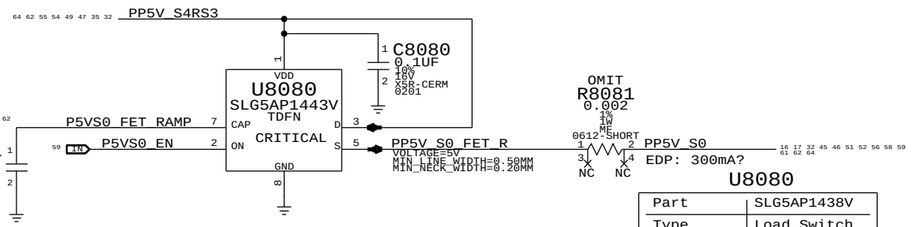
3.3V Sensor Switch



U8050

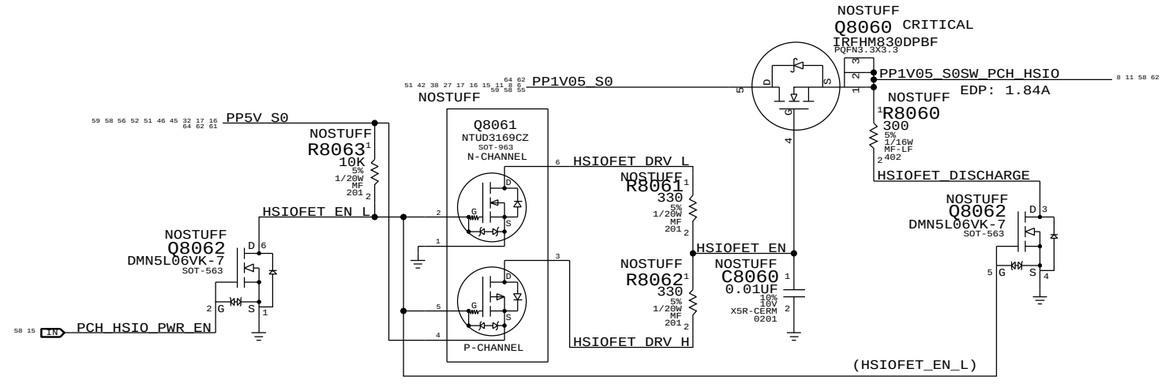
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

5V S0 Switch



U8080

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A



SYNC_MASTER=J41_MLB	SYNC_DATE=02/06/2013
PAGE TITLE	Power FETs
	Apple Inc.
DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
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S5 Enables

SMC_PM_G2_EN (OUT) → R8140 100 → S5_PWR_EN (MAKE_BASE=TRUE) → S5_PWR_EN (OUT)
PLACE_NEAR=U7501.21:7mm
NOSTUFF C8142 0.47UF 10% 6.3V CERM-X5R 402
PLACE_NEAR=U7501.21:7mm

S5 Power Good

PP3V42_G3H
PLACE_NEAR=U7501.20:7mm
R8141 100K 5% 1/20W MF 201
S5_PWRGD-->SMC
SMC-->PM_DSW_PWRGD
S5_PWRGD → S5_PWRGD (MAKE_BASE=TRUE) (OUT)

SSD Enable

SSD_PWR_EN (IN) → SSD_PWR_EN (MAKE_BASE=TRUE) (OUT)

Standby Enables

PP3V3_S5
NOSTUFF C8170 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U8170.6:2.3mm
NOSTUFF U8170 74LVC1G32 SOT891
PM_SLP_S5_L (IN)
SMC_S4_WAKESRC_EN (IN)
S4_PWR_EN (MAKE_BASE=TRUE) → S4_PWR_EN (OUT) ×2
NCX
R8115 0 1/20W MF 0201

S3 Enables

PM_SLP_S4_L (IN)
R8111 20K 5% 1/20W MF 201
R8116 0 5% 1/20W MF 0201
R8112 0 5% 1/20W MF 0201
P3V3S3_EN (MAKE_BASE=TRUE) → P3V3S3_EN (OUT)
P1V8S3_EN (MAKE_BASE=TRUE) → P1V8S3_EN (OUT)
DDRREG_EN (MAKE_BASE=TRUE) → DDRREG_EN (OUT)
C8111 0.1UF 20% 10V CERM 402
NO STUFF C8116 0.47UF 10% 6.3V CERM-X5R 402
NO STUFF C8112 0.47UF 10% 6.3V CERM-X5R 402

USB_PWR:STBY R8114 100 5% 1/20W MF 201
USB_PWR:S3 R8117 100 5% 1/20W MF 201
USB_PWR_EN (MAKE_BASE=TRUE) → USB_PWR_EN (OUT)
NO STUFF C8114 0.47UF 10% 6.3V CERM-X5R 402

USB_PWR:STBY R8177 0 5% 1/20W MF 0201
S4_PWR_EN
USB_PWR:S3 R8179 0 5% 1/20W MF 0201
PM_SLP_S4_L
P5VS4RS3_EN_RC
NO STUFF D8175 SM-201 RB521ZS-30
R8175 0 5% 1/20W MF 0201
NO STUFF R8176 240 5% 1/20W MF 201
P5VS4RS3_EN_D
5V needs to be held up so 1.05V can fall after 1.5V
P5VS4RS3_EN (OUT)
NO STUFF C8175 2.2UF 10% 6.3V X6R 402

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

S0 Rail PGOOD (BJT Version)

PP5V_S0
R8151 54.9K 1% 1/20W MF 201
VMON_5V_DIV
5.0V Divider: 1.07V
R8152 15K 1% 1/20W MF 201
R8153 1K 5% 1/20W MF 201
C8159 1UF 10% 10V X5R 402
9ms RC delay
PP3V3_S0
R8158 15K 1% 1/20W MF 201
VMON_3V3_DIV
3.3V Divider: 1.07V
R8159 7.15K 1% 1/20W MF 201
R8154 1K 5% 1/20W MF 201
R8156 150K 1% 1/20W MF 201
PP3V3_S5
S0PGD_C
ALL_SYS_PWRGD (OUT)
CRITICAL Q8150 ASMCC0179 DFN2015H4-8 376S0854
VMON_Q2_BASE
VMON_Q3_BASE
NC
NC
S0PGD_BJT_GND_R
R8157 100 5% 1/20W MF 201
PP1V5_S0
R8155 1K 5% 1/20W MF 201
VMON_Q4_BASE
Vbe 0.7V max @ 2mA
Vce(sat) 0.1V max @ 1mA
Q1 Vth 0.7~1V @Id 250uA

1.5V Codec Enable

PLACE_NEAR=U8040.2:C7mm
AUD_PWR_EN (IN)
R8145 100K 5% 1/20W MF 201
P1V5S0SW_AUDIO_EN (OUT)
D8146 SM-201 RB521ZS-30
P1V5CODEC_EN_D
R8146 1K 5% 1/20W MF 201
C8146 0.1UF 10% 25V X5R 402
PLACE_NEAR=U8040.2:C7mm

3.3V SUS Detect

PP3V3_S5
BYPASS=U8130.6:2.3mm
C8130 0.1UF 10% 6.3V CERM-X5R 0201
No stuff C8131, 12ms Min delay time'
U8130 Sense input threhold is 3.07V
CRITICAL
PP3V3_SUS
U8130 TPS3808G33 QFN
VDD SENSE CT GND THRM PAD RESET* MR*
PM_RSMRST_L (OUT)
TP_SUS_PGOOD_MR_L
SUS_PGOOD_CT
NO STUFF C8131 1000PF 10% 16V X7R-CERM 0201
PP3V3_SUS
R8133 100K 5% 1/20W MF 201

CHGR VFRQ Generation

PP3V42_G3H
R8131 330K 5% 1/20W MF 201
VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency
CHGR_VFRQ (OUT)
Q8131 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
PM_SLP_S3_R_L

S0 Rail PGOOD Circuitry (ISL version used for development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

PP1V05_S0
PP1V5_S0
PP5V_S0
PP3V3_S0
S0PGOOD_ISL
R8160 6.04K 1% 1/20W MF 201
R8170 15K 1% 1/20W MF 201
R8172 6.04K 1% 1/20W MF 201
5V Divider: 3.19V @ 4.5Vmin
1.5V Divider: 0.718V @ 1.45Vmin
1.05V Divider: 0.723V @ 1.02Vmin
R8161 15K 1% 1/20W MF 201
R8171 15K 1% 1/20W MF 201
R8173 15K 1% 1/20W MF 201
C8160 0.1UF 10% 6.3V CERM-X5R 0201
U8160 ISL88042IRTEZ TDFN (IPU) CRITICAL 353S2310
VDD V2MON V3MON V4MON GND THRM_PAD MR RST*
P5V_DIV_VMON
P1V5_DIV_VMON
P1V05_DIV_VMON
NC
ALL_SYS_PWRGD_R
R8162 330 1% 1/20W MF 201
ALL_SYS_PWRGD (OUT)

P1V8S3_PGOOD (IN) → R8166 100
P5VS4RS3_PGOOD (IN) → R8165 100
P1V05S0_PGOOD (IN) → R8164 100
DDRREG_PGOOD (IN) → R8168 100
R8167 10K 5% 1/20W MF 201

S0 Enables

PP3V3_S5
BYPASS=U8180.6:3mm
C8180 0.1UF 10% 6.3V CERM-X5R 0201
PM_SLP_S3_L (IN)
R8178 100 5% 1/20W MF 201
PM_SLP_S3_R_L
MC74VHC1G08 SC70-HF U8180
PM_SLP_S3_BUF_L (MAKE_BASE=TRUE)
NOSTUFF R8180 330K 5% 1/20W MF 201
PM_SLP_S3_BUF_L (OUT) ×2

NO STUFF D8185 SM-201 RB521ZS-30
R8185 0 5% 1/20W MF 0201
NO STUFF R8138 820 5% 1/20W MF 201
P1V05_EN_D
R8184 330 5% 1/20W MF 201
D8184 SM-201 RB521ZS-30
P3V3S0_EN_D
R8186 20K 5% 1/20W MF 201
R8187 0 5% 1/20W MF 201
P5VS0_EN (MAKE_BASE=TRUE) → P5VS0_EN (OUT)
P3V3S0_EN (MAKE_BASE=TRUE) → P3V3S0_EN (OUT)
P1V05S0_EN (MAKE_BASE=TRUE) → P1V05S0_EN (OUT)
NO STUFF C8185 0.22UF 10% 10V CERM 402
C8186 0.1UF 20% 10V CERM 402
NO STUFF C8187 0.68UF 10% 6.3V CERM 402

SUS Enables

PM_SLP_SUS_L (IN)
PM_SLP_SUS_L (MAKE_BASE=TRUE) → PM_SLP_SUS_L (OUT)
R8190 0 5% 1/20W MF 0201
P3V3SUS_EN (MAKE_BASE=TRUE) → P3V3SUS_EN (OUT)
NO STUFF C8190 0.1UF 10% 25V X5R 402

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013
PAGE TITLE: Power Control
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REVISION: <E4LABEL>
BRANCH: <BRANCH>
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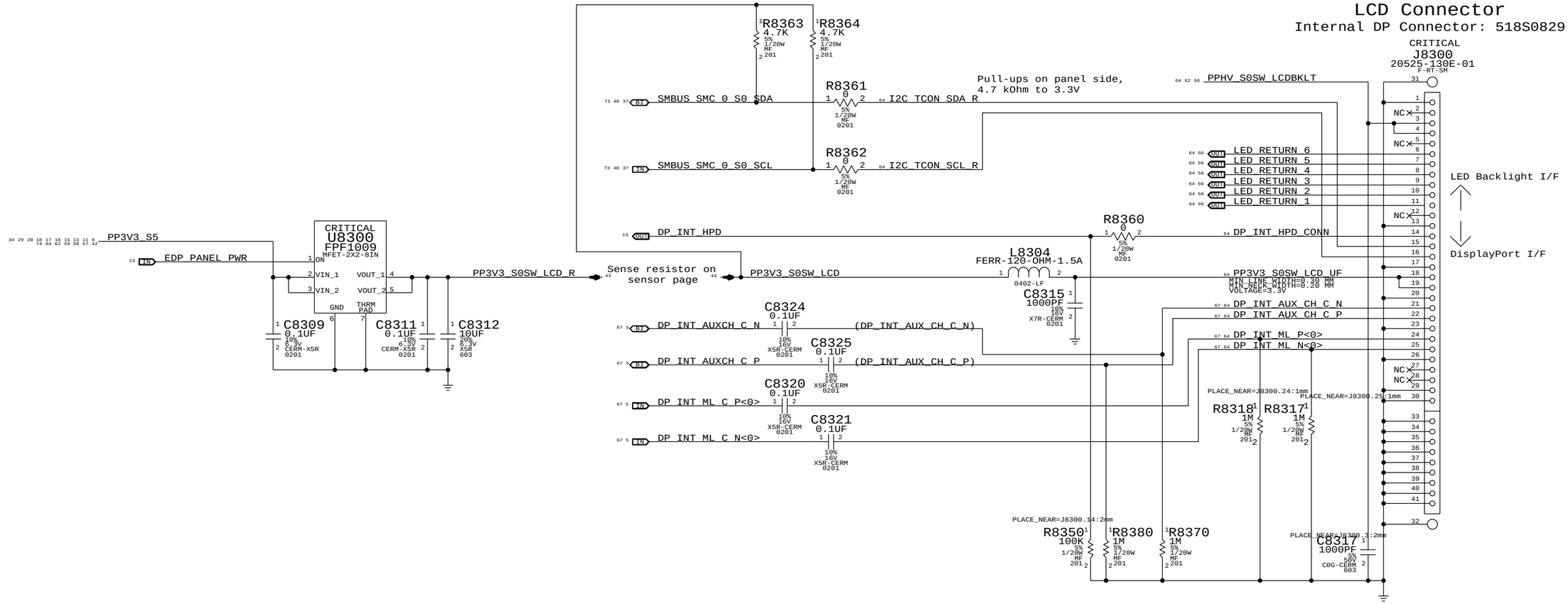

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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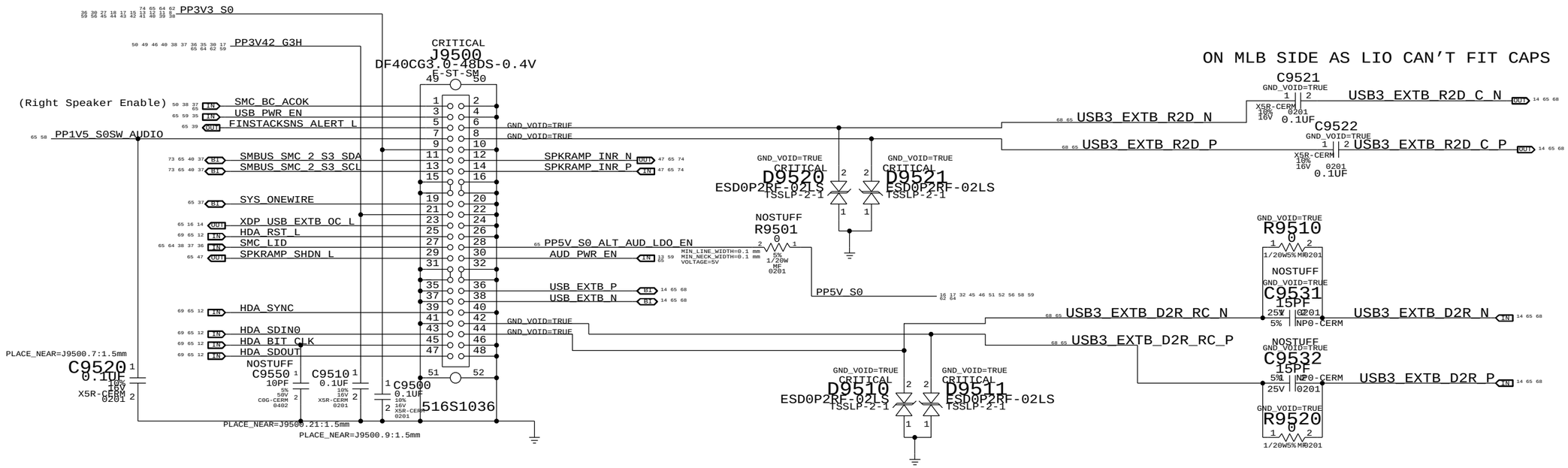

IO Ports

SYNC_MASTER=CLEAN_J43 SYNC_DATE=11/13/2012

PAGE TITLE
Left I/O (LIO) Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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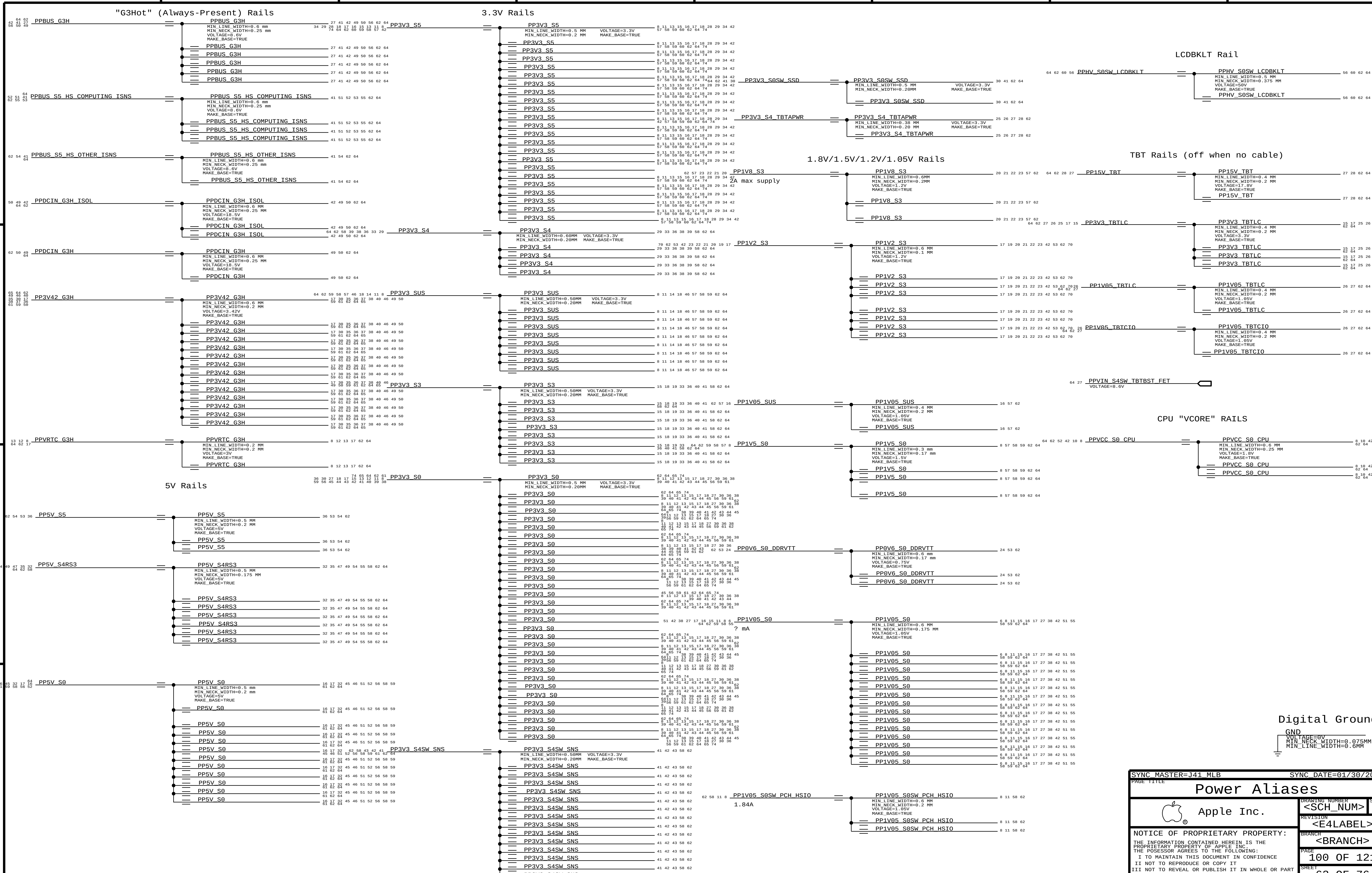

SYNC_MASTER=J41_MLB SYNC_DATE=01/30/2013

PAGE TITLE

Power Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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Memory Bit/Byte Swizzle

LPDDR3 Command/Address

MAKE_BASE

7	=MEM_A_A<5>	TRUE	MEM_A_CAA<0>	20 24 70	
7	=MEM_A_A<9>	TRUE	MEM_A_CAA<1>	20 24 70	
7	=MEM_A_A<6>	TRUE	MEM_A_CAA<2>	20 24 70	
7	=MEM_A_A<8>	TRUE	MEM_A_CAA<3>	20 24 70	
7	=MEM_A_A<7>	TRUE	MEM_A_CAA<4>	20 24 70	
7	=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>	20 24 70	
70 63 24 20 7	MEM_A_CAA<6>	TRUE	MEM_A_CAA<6>	7 20 24 63 70	
7	=MEM_A_A<11>	TRUE	MEM_A_CAA<7>	20 24 70	
7	=MEM_A_A<15>	TRUE	MEM_A_CAA<8>	20 24 70	
7	=MEM_A_A<14>	TRUE	MEM_A_CAA<9>	20 24 70	
7	=MEM_A_A<13>	TRUE	MEM_A_CAB<0>	21 24 70	
7	=MEM_A_CAS_L	TRUE	MEM_A_CAB<1>	21 24 70	
7	=MEM_A_WE_L	TRUE	MEM_A_CAB<2>	21 24 70	
7	=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>	21 24 70	
7	=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>	21 24 70	
7	=MEM_A_A<2>	TRUE	MEM_A_CAB<5>	21 24 70	
70 63 24 21 7	MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>	7 21 24 63 70	
7	=MEM_A_A<10>	TRUE	MEM_A_CAB<7>	21 24 70	
7	=MEM_A_A<1>	TRUE	MEM_A_CAB<8>	21 24 70	
7	=MEM_A_A<0>	TRUE	MEM_A_CAB<9>	21 24 70	
70 63 24 21 20 7	MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>	7 20 21 24 63 70	
63 7	TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1	7 63	
63 7	TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2	7 63	
7	=MEM_B_A<5>	TRUE	MEM_B_CAA<0>	22 24 70	
7	=MEM_B_A<9>	TRUE	MEM_B_CAA<1>	22 24 70	
7	=MEM_B_A<6>	TRUE	MEM_B_CAA<2>	22 24 70	
7	=MEM_B_A<8>	TRUE	MEM_B_CAA<3>	22 24 70	
7	=MEM_B_A<7>	TRUE	MEM_B_CAA<4>	22 24 70	
7	=MEM_B_BA<2>	TRUE	MEM_B_CAA<5>	22 24 70	
70 63 24 22 7	MEM_B_CAA<6>	TRUE	MEM_B_CAA<6>	7 22 24 63 70	
7	=MEM_B_A<11>	TRUE	MEM_B_CAA<7>	22 24 70	
7	=MEM_B_A<15>	TRUE	MEM_B_CAA<8>	22 24 70	
7	=MEM_B_A<14>	TRUE	MEM_B_CAA<9>	22 24 70	
7	=MEM_B_A<13>	TRUE	MEM_B_CAB<0>	23 24 70	
7	=MEM_B_CAS_L	TRUE	MEM_B_CAB<1>	23 24 70	
7	=MEM_B_WE_L	TRUE	MEM_B_CAB<2>	23 24 70	
7	=MEM_B_RAS_L	TRUE	MEM_B_CAB<3>	23 24 70	
7	=MEM_B_BA<0>	TRUE	MEM_B_CAB<4>	23 24 70	
7	=MEM_B_A<2>	TRUE	MEM_B_CAB<5>	23 24 70	
70 63 24 23 7	MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>	7 23 24 63 70	
7	=MEM_B_A<10>	TRUE	MEM_B_CAB<7>	23 24 70	
7	=MEM_B_A<1>	TRUE	MEM_B_CAB<8>	23 24 70	
7	=MEM_B_A<0>	TRUE	MEM_B_CAB<9>	23 24 70	
70 63 24 23 22 7	MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>	7 22 23 24 63 70	
63 7	TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3	7 63	
63 7	TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4	7 63	

MAKE_BASE

20	=MEM_A_DQ<0>	TRUE	MEM_A_DQ<9>	7 70	
20	=MEM_A_DQ<1>	TRUE	MEM_A_DQ<12>	7 70	
20	=MEM_A_DQ<2>	TRUE	MEM_A_DQ<10>	7 70	
20	=MEM_A_DQ<3>	TRUE	MEM_A_DQ<11>	7 70	
20	=MEM_A_DQ<4>	TRUE	MEM_A_DQ<8>	7 70	
20	=MEM_A_DQ<5>	TRUE	MEM_A_DQ<13>	7 70	
20	=MEM_A_DQ<6>	TRUE	MEM_A_DQ<14>	7 70	
20	=MEM_A_DQ<7>	TRUE	MEM_A_DQ<15>	7 70	
20	=MEM_A_DQ<8>	TRUE	MEM_A_DQ<0>	7 70	
20	=MEM_A_DQ<9>	TRUE	MEM_A_DQ<1>	7 70	
20	=MEM_A_DQ<10>	TRUE	MEM_A_DQ<2>	7 70	
20	=MEM_A_DQ<11>	TRUE	MEM_A_DQ<7>	7 70	
20	=MEM_A_DQ<12>	TRUE	MEM_A_DQ<4>	7 70	
20	=MEM_A_DQ<13>	TRUE	MEM_A_DQ<5>	7 70	
20	=MEM_A_DQ<14>	TRUE	MEM_A_DQ<3>	7 70	
20	=MEM_A_DQ<15>	TRUE	MEM_A_DQ<6>	7 70	
20	=MEM_A_DQ<16>	TRUE	MEM_A_DQ<29>	7 70	
20	=MEM_A_DQ<17>	TRUE	MEM_A_DQ<28>	7 70	
20	=MEM_A_DQ<18>	TRUE	MEM_A_DQ<27>	7 70	
20	=MEM_A_DQ<19>	TRUE	MEM_A_DQ<31>	7 70	
20	=MEM_A_DQ<20>	TRUE	MEM_A_DQ<24>	7 70	
20	=MEM_A_DQ<21>	TRUE	MEM_A_DQ<25>	7 70	
20	=MEM_A_DQ<22>	TRUE	MEM_A_DQ<26>	7 70	
20	=MEM_A_DQ<23>	TRUE	MEM_A_DQ<30>	7 70	
20	=MEM_A_DQ<24>	TRUE	MEM_A_DQ<18>	7 70	
20	=MEM_A_DQ<25>	TRUE	MEM_A_DQ<21>	7 70	
20	=MEM_A_DQ<26>	TRUE	MEM_A_DQ<16>	7 70	
20	=MEM_A_DQ<27>	TRUE	MEM_A_DQ<23>	7 70	
20	=MEM_A_DQ<28>	TRUE	MEM_A_DQ<20>	7 70	
20	=MEM_A_DQ<29>	TRUE	MEM_A_DQ<19>	7 70	
20	=MEM_A_DQ<30>	TRUE	MEM_A_DQ<22>	7 70	
20	=MEM_A_DQ<31>	TRUE	MEM_A_DQ<17>	7 70	
21	=MEM_A_DQ<32>	TRUE	MEM_A_DQ<41>	7 70	
21	=MEM_A_DQ<33>	TRUE	MEM_A_DQ<44>	7 70	
21	=MEM_A_DQ<34>	TRUE	MEM_A_DQ<46>	7 70	
21	=MEM_A_DQ<35>	TRUE	MEM_A_DQ<47>	7 70	
21	=MEM_A_DQ<36>	TRUE	MEM_A_DQ<40>	7 70	
21	=MEM_A_DQ<37>	TRUE	MEM_A_DQ<45>	7 70	
21	=MEM_A_DQ<38>	TRUE	MEM_A_DQ<42>	7 70	
21	=MEM_A_DQ<39>	TRUE	MEM_A_DQ<43>	7 70	
21	=MEM_A_DQ<40>	TRUE	MEM_A_DQ<36>	7 70	
21	=MEM_A_DQ<41>	TRUE	MEM_A_DQ<37>	7 70	
21	=MEM_A_DQ<42>	TRUE	MEM_A_DQ<34>	7 70	
21	=MEM_A_DQ<43>	TRUE	MEM_A_DQ<39>	7 70	
70 63 21 7	MEM_A_DQ<32>	TRUE	MEM_A_DQ<32>	7 21 63 70	
21	=MEM_A_DQ<45>	TRUE	MEM_A_DQ<33>	7 70	
21	=MEM_A_DQ<46>	TRUE	MEM_A_DQ<35>	7 70	
21	=MEM_A_DQ<47>	TRUE	MEM_A_DQ<38>	7 70	
21	=MEM_A_DQ<48>	TRUE	MEM_A_DQ<52>	7 70	
21	=MEM_A_DQ<49>	TRUE	MEM_A_DQ<51>	7 70	
21	=MEM_A_DQ<50>	TRUE	MEM_A_DQ<48>	7 70	
21	=MEM_A_DQ<51>	TRUE	MEM_A_DQ<49>	7 70	
21	=MEM_A_DQ<52>	TRUE	MEM_A_DQ<53>	7 70	
21	=MEM_A_DQ<53>	TRUE	MEM_A_DQ<50>	7 70	
21	=MEM_A_DQ<54>	TRUE	MEM_A_DQ<54>	7 70	
21	=MEM_A_DQ<55>	TRUE	MEM_A_DQ<55>	7 70	
21	=MEM_A_DQ<56>	TRUE	MEM_A_DQ<58>	7 70	
21	=MEM_A_DQ<57>	TRUE	MEM_A_DQ<62>	7 70	
21	=MEM_A_DQ<58>	TRUE	MEM_A_DQ<60>	7 70	
21	=MEM_A_DQ<59>	TRUE	MEM_A_DQ<61>	7 70	
21	=MEM_A_DQ<60>	TRUE	MEM_A_DQ<59>	7 70	
21	=MEM_A_DQ<61>	TRUE	MEM_A_DQ<63>	7 70	
21	=MEM_A_DQ<62>	TRUE	MEM_A_DQ<57>	7 70	
21	=MEM_A_DQ<63>	TRUE	MEM_A_DQ<56>	7 70	
20	=MEM_A_DQS_P<0>	TRUE	MEM_A_DQS_P<1>	7 70	
20	=MEM_A_DQS_N<0>	TRUE	MEM_A_DQS_N<1>	7 70	
20	=MEM_A_DQS_P<1>	TRUE	MEM_A_DQS_P<0>	7 70	
20	=MEM_A_DQS_N<1>	TRUE	MEM_A_DQS_N<0>	7 70	
20	=MEM_A_DQS_P<2>	TRUE	MEM_A_DQS_P<3>	7 70	
20	=MEM_A_DQS_N<2>	TRUE	MEM_A_DQS_N<3>	7 70	
20	=MEM_A_DQS_P<3>	TRUE	MEM_A_DQS_P<2>	7 70	
20	=MEM_A_DQS_N<3>	TRUE	MEM_A_DQS_N<2>	7 70	
21	=MEM_A_DQS_P<4>	TRUE	MEM_A_DQS_P<5>	7 70	
21	=MEM_A_DQS_N<4>	TRUE	MEM_A_DQS_N<5>	7 70	
21	=MEM_A_DQS_P<5>	TRUE	MEM_A_DQS_P<4>	7 70	
21	=MEM_A_DQS_N<5>	TRUE	MEM_A_DQS_N<4>	7 70	
70 63 21 7	MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<6>	7 21 63 70	
70 63 21 7	MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<6>	7 21 63 70	
21	=MEM_A_DQS_P<7>	TRUE	MEM_A_DQS_P<7>	7 70	
21	=MEM_A_DQS_N<7>	TRUE	MEM_A_DQS_N<7>	7 70	

MAKE_BASE

22	=MEM_B_DQ<0>	TRUE	MEM_B_DQ<12>	7 70	
22	=MEM_B_DQ<1>	TRUE	MEM_B_DQ<9>	7 70	
22	=MEM_B_DQ<2>	TRUE	MEM_B_DQ<10>	7 70	
22	=MEM_B_DQ<3>	TRUE	MEM_B_DQ<11>	7 70	
22	=MEM_B_DQ<4>	TRUE	MEM_B_DQ<13>	7 70	
22	=MEM_B_DQ<5>	TRUE	MEM_B_DQ<8>	7 70	
22	=MEM_B_DQ<6>	TRUE	MEM_B_DQ<14>	7 70	
22	=MEM_B_DQ<7>	TRUE	MEM_B_DQ<15>	7 70	
22	=MEM_B_DQ<8>	TRUE	MEM_B_DQ<0>	7 70	
22	=MEM_B_DQ<9>	TRUE	MEM_B_DQ<1>	7 70	
22	=MEM_B_DQ<10>	TRUE	MEM_B_DQ<2>	7 70	
22	=MEM_B_DQ<11>	TRUE	MEM_B_DQ<7>	7 70	
22	=MEM_B_DQ<12>	TRUE	MEM_B_DQ<4>	7 70	
22	=MEM_B_DQ<13>	TRUE	MEM_B_DQ<5>	7 70	
22	=MEM_B_DQ<14>	TRUE	MEM_B_DQ<6>	7 70	
22	=MEM_B_DQ<15>	TRUE	MEM_B_DQ<3>	7 70	
22	=MEM_B_DQ<16>	TRUE	MEM_B_DQ<28>	7 70	
22	=MEM_B_DQ<17>	TRUE	MEM_B_DQ<29>	7 70	
22	=MEM_B_DQ<18>	TRUE	MEM_B_DQ<30>	7 70	
22	=MEM_B_DQ<19>	TRUE	MEM_B_DQ<27>	7 70	
22	=MEM_B_DQ<20>	TRUE	MEM_B_DQ<24>	7 70	
22	=MEM_B_DQ<21>	TRUE	MEM_B_DQ<25>	7 70	
22	=MEM_B_DQ<22>	TRUE	MEM_B_DQ<31>	7 70	
22	=MEM_B_DQ<23>	TRUE	MEM_B_DQ<26>	7 70	
22	=MEM_B_DQ<24>	TRUE	MEM_B_DQ<20>	7 70	
22	=MEM_B_DQ<25>	TRUE	MEM_B_DQ<16>	7 70	
22	=MEM_B_DQ<26>	TRUE	MEM_B_DQ<23>	7 70	
22	=MEM_B_DQ<27>	TRUE	MEM_B_DQ<22>	7 70	
22	=MEM_B_DQ<28>	TRUE	MEM_B_DQ<21>	7 70	
22	=MEM_B_DQ<29>	TRUE	MEM_B_DQ<17>	7 70	
22	=MEM_B_DQ<30>	TRUE	MEM_B_DQ<18>	7 70	
22	=MEM_B_DQ<31>	TRUE	MEM_B_DQ<19>	7 70	
23	=MEM_B_DQ<32>	TRUE	MEM_B_DQ<44>	7 70	
23	=MEM_B_DQ<33>	TRUE	MEM_B_DQ<41>	7 70	
23	=MEM_B_DQ<34>	TRUE	MEM_B_DQ<42>	7 70	
23	=MEM_B_DQ<35>	TRUE	MEM_B_DQ<43>	7 70	
23	=MEM_B_DQ<36>	TRUE	MEM_B_DQ<45>	7 70	
23	=MEM_B_DQ<37>	TRUE	MEM_B_DQ<40>	7 70	
23	=MEM_B_DQ<38>	TRUE	MEM_B_DQ<46>	7 70	
23	=MEM_B_DQ<39>	TRUE	MEM_B_DQ<47>	7 70	
23	=MEM_B_DQ<40>	TRUE	MEM_B_DQ<32>	7 70	
70 63 23 7	MEM_B_DQ<33>	TRUE	MEM_B_DQ<33>	7 23 63 70	
23	=MEM_B_DQ<42>	TRUE	MEM_B_DQ<34>	7 70	
23	=MEM_B_DQ<43>	TRUE	MEM_B_DQ<39>	7 70	
23	=MEM_B_DQ<44>	TRUE	MEM_B_DQ<36>	7 70	
23	=MEM_B_DQ<45>	TRUE	MEM_B_DQ<37>	7 70	
23	=MEM_B_DQ<46>	TRUE	MEM_B_DQ<38>	7 70	
23	=MEM_B_DQ<47>	TRUE	MEM_B_DQ<35>	7 70	
23	=MEM_B_DQ<48>	TRUE	MEM_B_DQ<57>	7 70	
23	=MEM_B_DQ<49>	TRUE	MEM_B_DQ<56>	7 70	
23	=MEM_B_DQ<50>	TRUE	MEM_B_DQ<60>	7 70	
23	=MEM_B_DQ<51>	TRUE	MEM_B_DQ<59>	7 70	
23	=MEM_B_DQ<52>	TRUE	MEM_B_DQ<63>	7 70	
23	=MEM_B_DQ<53>	TRUE	MEM_B_DQ<62>	7 70	
23	=MEM_B_DQ<54>	TRUE	MEM_B_DQ<58>	7 70	
23	=MEM_B_DQ<55>	TRUE	MEM_B_DQ<61>	7 70	
23	=MEM_B_DQ<56>	TRUE	MEM_B_DQ<49>	7 70	
23	=MEM_B_DQ<57>	TRUE	MEM_B_DQ<51>	7 70	
23	=MEM_B_DQ<58>	TRUE	MEM_B_DQ<48>	7 70	
23	=MEM_B_DQ<59>	TRUE	MEM_B_DQ<53>	7 70	
23	=MEM_B_DQ<60>	TRUE	MEM_B_DQ<52>	7 70	
23	=MEM_B_DQ<61>	TRUE	MEM_B_DQ<55>	7 70	
23	=MEM_B_DQ<62>	TRUE	MEM_B_DQ<50>	7 70	
23	=MEM_B_DQ<63>	TRUE	MEM_B_DQ<54>	7 70	
22	=MEM_B_DQS_P<0>	TRUE	MEM_B_DQS_P<1>	7 70	
22	=MEM_B_DQS_N<0>	TRUE	MEM_B_DQS_N<1>	7 70	
22	=MEM_B_DQS_P<1>	TRUE	MEM_B_DQS_P<0>	7 70	
22	=MEM_B_DQS_N<1>	TRUE	MEM_B_DQS_N<0>	7 70	
22	=MEM_B_DQS_P<2>	TRUE	MEM_B_DQS_P<3>	7 70	
22	=MEM_B_DQS_N<2>	TRUE	MEM_B_DQS_N<3>	7 70	
22	=MEM_B_DQS_P<3>	TRUE	MEM_B_DQS_P<2>	7 70	
22	=MEM_B_DQS_N<3>	TRUE	MEM_B_DQS_N<2>	7 70	
23	=MEM_B_DQS_P<4>	TRUE	MEM_B_DQS_P<5>	7 70	
23	=MEM_B_DQS_N<4>	TRUE	MEM_B_DQS_N<5>	7 70	
23	=MEM_B_DQS_P<5>	TRUE	MEM_B_DQS_P<4>	7 70	
23	=MEM_B_DQS_N<5>	TRUE	MEM_B_DQS_N<4>	7 70	
23	=MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<7>	7 70	
23	=MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<7>	7 70	
70 63 23 7	MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>	7 23 63 70	
70 63 23 7	MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>	7 23 63 70	

SYNC_MASTER=J41_MLB SYNC_DATE=08/30/2012

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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Functional Test Points

J3501: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN	(Need 6 TPs)	29 37 38 39 41
TRUE	WIFI_EVENT_L		29 37 38
TRUE	PCIE_AP_R2D_N		29 69
TRUE	PCIE_AP_R2D_P		29 69
TRUE	PCIE_CLK100M_AP_N		12 29 69
TRUE	PCIE_CLK100M_AP_P		12 29 69
TRUE	PCIE_AP_D2R_P		14 29 69
TRUE	PCIE_AP_D2R_N		14 29 69
TRUE	PCIE_WAKE_L		13 29 31
TRUE	AP_RESET_CONN_L		29
TRUE	AP_CLKREQ_O_L		29
TRUE	USB_BT_CONN_P		29 68
TRUE	USB_BT_CONN_N		29 68
TRUE	PP3V3_S4		29 33 36 38 39 58 62 63

(Need to add 8 GND TPs)

J3700: SSD Connector

FUNC_TEST

TRUE	PP3V3_S0SW_SSD_FLT	(Need 5 TPs)	30
TRUE	PCIE_SSD_R2D_N<3..0>		30 67
TRUE	PCIE_SSD_R2D_P<3..0>		30 67
TRUE	PP3V3_S0		42 43 44 45 56 59 61 62 64 65 74
TRUE	SSD_RESET_CONN_L		30
TRUE	SSD_CLKREQ_CONN_L		30
TRUE	SMC_OOB1_R2D_CONN_L		30
TRUE	SMC_OOB1_D2R_CONN_L		30
TRUE	SSD_PCIE_SEL_L		16 30
TRUE	SSD_DEVSLP		15 30
TRUE	SSD_PWRFAIL_WARN_L		
TRUE	SSD_PWR_EN		15 30 58 59
TRUE	PCIE_SSD_D2R_N<3..0>		12 30 67
TRUE	PCIE_SSD_D2R_P<3..0>		12 30 67
TRUE	PCIE_CLK100M_SSD_N		12 30 67
TRUE	PCIE_CLK100M_SSD_P		12 30 67

(Need to add 6 GND TPs)

J4002: Camera Connector

FUNC_TEST

TRUE	MIPI_CLK_CONN_N		32 72
TRUE	MIPI_CLK_CONN_P		32 72
TRUE	CAM_SENSOR_WAKE_L_CONN		32
TRUE	MIPI_DATA_CONN_N		32 72
TRUE	MIPI_DATA_CONN_P		32 72
TRUE	SMBUS_SMC_1_S0_SDA		14 32 37 40 43 44 69 73
TRUE	SMBUS_SMC_1_S0_SCL		14 32 37 40 43 44 69 73
TRUE	I2C_CAM_SCK		31 32
TRUE	I2C_CAM_SDA		31 32
TRUE	PP5V_S3RS0_ALSCAM_F	(Need TBD TPs)	32

(Need to add TBD GND TPs)

J6100: LPC+SPI Connector

FUNC_TEST

TRUE	PP3V42_G3H	65
TRUE	PP5V_S0	17 30 35 36 37 39 46 49 50 56 58 59 61 62 64
TRUE	LPC_CLK24M_LPCPLUS	17 46 69
TRUE	LPC_AD<3..0>	14 37 46 69
TRUE	SPI_ALT_MOSI	46
TRUE	XDP_LPCPLUS_GPIO	15 16 46
TRUE	LPCPLUS_RESET_L	18 46 69
TRUE	SMC_TDO	37 38 46
TRUE	TP_SMC_TRST_L	46
TRUE	TP_SMC_MD1	46
TRUE	SMC_TX_L	37 38 46
TRUE	SPI_ALT_MISO	46
TRUE	LPC_FRAME_L	14 37 46 69
TRUE	SPIROM_USE_MLB	15 46
TRUE	PM_CLKRUN_L	13 37 46
TRUE	SPI_ALT_CLK	46
TRUE	SPI_ALT_CS_L	46
TRUE	LPC_SERIRQ	15 37 46
TRUE	LPC_PWRDWN_L	13 37 46
TRUE	SMC_TDI	37 38 46
TRUE	SMC_TCK	37 38 46
TRUE	SMC_RESET_L	37 38 46 50
TRUE	SMC_ROMBOOT	38 46
TRUE	SMC_RX_L	37 38 46
TRUE	SMC_TMS	37 38 46

(Need to add 6 GND TPs)

J6000: Fan Connector

FUNC_TEST

TRUE	PP5V_S0		16 17 32 45 46 51 52 56 58 59 61 62 64
TRUE	FAN_RT_TACH		45
TRUE	FAN_RT_PWM		45

(Need to add 1 GND TP)

J4800: IPD Flex Connector

FUNC_TEST

TRUE	SMC_LID	36 37 38 61 65
TRUE	TPAD_SPI_MISO_R	36
TRUE	USB_TPAD_P	14 36 68
TRUE	USB_TPAD_N	14 36 68
TRUE	TPAD_SPI_CLK_R	36
TRUE	TPAD_WAKE_L	36
TRUE	TPAD_SPI_MOSI_R	36
TRUE	PP3V3_S4_IPD	36
TRUE	TPAD_SPI_CS_R_L	36
TRUE	TPAD_SPI_IF_EN_CONN	36
TRUE	TPAD_SPI_INT_S4_WAKE_L_CONN	36
TRUE	PP5V_S4_IPD	36
TRUE	TPAD_USB_IF_EN_CONN	36
TRUE	SMBUS_SMC_3_SDA	36 37 40 44 73
TRUE	SMBUS_SMC_3_SCL	36 37 40 44 73
TRUE	SMC_LSOC_RST_L	36 38
TRUE	PP3V42_G3H	17 30 35 36 37 38 40 46 49 50 59 61 62 64 65
TRUE	SMC_ONOFF_L	36 37 38

(Need to add 5 GND TPs)

J7000: DC-In Connector

FUNC_TEST

TRUE	PPDCIN_G3H	(Need 4 TPs)	42 50 62 64
TRUE	PP5V_S4RS3	(Need 3 TPs)	32 35 47 49 54 55 58 62

(Need to add 5 GND TPs)

J6404: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_ROUT_P	47 74
TRUE	SPKRAMP_ROUT_N	47 74

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	(Need 4 TPs)	48 50
TRUE	SMBUS_SMC_5_G3_SCL		37 40 48 50 73
TRUE	SMBUS_SMC_5_G3_SDA		37 40 48 50 73
TRUE	SYS_DETECT_L		48

(Need to add 4 GND TPs near J7050 and 1 for shield)

J8300: Internal DP Connector

FUNC_TEST

TRUE	PPHV_S0SW_LCDBKLT	(Need 2 TPs)	56 60 62
TRUE	LED_RETURN_6		56 60
TRUE	LED_RETURN_5		56 60
TRUE	LED_RETURN_4		56 60
TRUE	LED_RETURN_3		56 60
TRUE	LED_RETURN_2		56 60
TRUE	LED_RETURN_1		56 60
TRUE	DP_INT_HPD_CONN		60
TRUE	I2C_TCON_SDA_R		60
TRUE	I2C_TCON_SCL_R		60
TRUE	PP3V3_S0SW_LCD_UF	(Need 2 TPs)	60
TRUE	DP_INT_AUX_CH_C_N		60 67
TRUE	DP_INT_AUX_CH_C_P		60 67
TRUE	DP_INT_ML_P<0>		60 67
TRUE	DP_INT_ML_N<0>		60 67

(Need to add 5 GND TPs)

J7715: KB BKLT Connector

FUNC_TEST

TRUE	KBDLED_ANODE	56
TRUE	KBDLED_FB	56

(Need to add 2 GND TPs)

J1800: XDP Connector

(Only a subset are needed for FCT HVM test fixture)

FUNC_TEST

H776	TRUE	XDP_CPU_TCK	6 16 67
H777	TRUE	XDP_PCH_TCK	12 16 69
H778	TRUE	XDP_CPU_TDI	6 16 67
H779	TRUE	XDP_CPU_TDO	6 16 67
H780	TRUE	XDP_CPUPCH_TRST_L	6 12 16 67
H781	TRUE	XDP_CPU_TMS	6 16 67
H782	TRUE	XDP_PCH_TMS	12 16 69
H783	TRUE	XDP_PCH_TDI	12 16 69
H784	TRUE	XDP_PCH_TDO	12 16 69
H785	TRUE	XDP_CPU_PREQ_L	6 16 67
H786	TRUE	XDP_CPU_PRDY_L	6 16 67
H787	TRUE	XDP_CPU_VCCST_PWRGD	16
H788	TRUE	PM_RSMRST_L	13 59
H789	TRUE	XDP_SYS_PWROK	16
H790	TRUE	PM_SYSRST_L	13 17 37
H791	TRUE	CPU_CFG<3>	6 16 67
H792	TRUE	PP1V05_S0	6 8 11 15 16 17 27 38 42 51 55 58 59 62 64

(Need to add 2 GND TPs)

H765 TRUE GND

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	27 41 42 49 50 56 62
TRUE	PPVIN_S4SW_TBTBST_FET	27 62
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	41 51 52 53 55 62
TRUE	PPDCIN_G3H	49 50 62 64
TRUE	PP3V42_G3H	17 30 35 36 37 38 40 46 49 50 59 61 62 64 65
TRUE	PPVRTC_G3H	8 12 13 17 62
TRUE	PP3V3_S5	8 11 13 15 16 17 18 28 29 34 42 57 58 59 60 62 74
TRUE	PP3V3_SUS	8 11 14 18 46 57 58 59 62
TRUE	PP3V3_S3	15 18 19 33 36 40 41 58 62
TRUE	PP3V3_S0	62 64 65 74
TRUE	PP3V3_S0SW_SSD	8 11 12 13 15 17 18 27 30 36 38 39 40 41 42 43 44 45 56 59 61
TRUE	PP1V5_S0	30 41 62
TRUE	PP1V05_S0	8 57 58 59 62
TRUE	PP15V_TBT	6 8 11 15 16 17 27 38 42 51 55 58 59 62 64
TRUE	PP3V3_TBTLC	27 28 62
TRUE	PP1V05_TBTLC	15 17 25 26 27 62
TRUE	PPVCC_S0_CPU	26 27 62
TRUE	PP1V05_TBTCIO	8 10 42 52 62
TRUE	PPBUS_S5_HS_OTHER_ISNS	26 27 62
TRUE	PPDCIN_G3H_ISOL	41 54 62
TRUE	PP3V3_S4	42 49 50 62

(Need to add 27 GND TPs)

NO_TEST Nets

NO_TEST MAKE_BASE

64	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	64
64	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	64
64 12	NC_PCIE_CLK100M_FWP	TRUE	TRUE	NC_PCIE_CLK100M_FWP	12 64
64 12	NC_PCIE_CLK100M_FWN	TRUE	TRUE	NC_PCIE_CLK100M_FWN	12 64
64 14	NC_PCIE_FW_D2RP	TRUE	TRUE	NC_PCIE_FW_D2RP	14 64
64 14	NC_PCIE_FW_D2RN	TRUE	TRUE	NC_PCIE_FW_D2RN	14 64
64 14	NC_PCIE_FW_R2D_CP	TRUE	TRUE	NC_PCIE_FW_R2D_CP	14 64
64 14	NC_PCIE_FW_R2D_CN	TRUE	TRUE	NC_PCIE_FW_R2D_CN	14 64
64 14	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP	14 64
64 14	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN	14 64
64 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14 64
64 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14 64
64 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14 64
64 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14 64
67	DP_INT_ML_C_P<3..1>	TRUE	TRUE	NC_INT_ML_CP<3..1>	5
67	DP_INT_ML_C_N<3..1>	TRUE	TRUE	NC_INT_ML_CN<3..1>	5
64 12	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	12 64
64 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13 64
64 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14 64
64 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14 64
64 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14 64
64 37	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	37 64
64	NC_IR_RX_OUT_RC	TRUE	TRUE	NC_IR_RX_OUT_RC	64
64	NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP	64
64	NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN	64
64 37	NC_SMC_GFX_OVERTEMP	TRUE	TRUE	NC_SMC_GFX_OVERTEMP	37 64
64 37	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	37 64
64 37	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	37 64
64 37	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	37 64
64 37	NC_SMC_FAN_5_CTL	TRUE	TRUE	NC_SMC_FAN_5_CTL	37 64
64	NC_ENET_ASF_GPIO	TRUE	TRUE	NC_ENET_ASF_GPIO	64
64	NC_SMC_MPM5_LED_PWR	TRUE	TRUE	NC_SMC_MPM5_LED_PWR	64
64	NC_SMC_MPM5_LED_CHG	TRUE	TRUE	NC_SMC_MPM5_LED_CHG	64
64 37	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	37 64
64 37	NC_SMC_DP_HPD_L	TRUE	TRUE	NC_SMC_DP_HPD_L	37 64
64 37	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	37 64
64 37	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	37 64
64 37	NC_BDV_BKL_PWM	TRUE	TRUE	NC_BDV_BKL_PWM	37 64
71	TBT_B_R2D_C_P<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CP<1..0>	25
71	TBT_B_R2D_C_N<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CN<1..0>	25
71	TBT_B_D2R_P<1..0>	TRUE	TRUE	NC_TBT_B_D2RP<1..0>	25
71	TBT_B_D2R_N<1..0>	TRUE	TRUE	NC_TBT_B_D2RN<1..0>	25
64 25	NC_TBT_B_LSTX	TRUE	TRUE	NC_TBT_B_LSTX	25 64
71 64	NC_DP_TBTPB_ML_CP<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CP<3..1:2>	64 71
71 64	NC_DP_TBTPB_ML_CN<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CN<3..1:2>	64 71
71 64 25	NC_DP_TBTPB_AUXCH_CP	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CP	25 64 71
71 64 25	NC_DP_TBTPB_AUXCH_CN	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CN	25 64 71
25	TP_DP_TBTSRC_ML_CP<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3>	
25	TP_DP_TBTSRC_ML_CN<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3>	
25	TP_DP_TBTSRC_ML_CP<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<2>	
25	TP_DP_TBTSRC_ML_CN<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<2>	
64 25	NC_DP_TBTSRC_ML_CP<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<1>	25 64
64 25	NC_DP_TBTSRC_ML_CN<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<1>	25 64
25	TP_DP_TBTSRC_ML_CP<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<0>	
25	TP_DP_TBTSRC_ML_CN<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<0>	
64 25	NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP	25 64
64 25	NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN	25 64

CPU/PCH

SMC

TBT

Unused nets with offpage

(Nets with offpages not used on this project)

HDD_PWR_EN	15
WOL_EN	14
BT_PWRRST_L	15
HDMITBTMUX_FLAG_L	15
FW_PWR_EN	15
FW_PME_L	15
ENET_MEDIA_SENSE	15
LCD_PSR_EN	15
LCD_IRQ_L	15
ODD_PWR_EN_L	13
ENET_LOW_PWR	13
AUD_IP_PERIPHERAL_DET	13
AUD_I2C_INT_L	13
AUD_IPHS_SWITCH_EN	13

SYNC_MASTER=J41_MLB SYNC_DATE=02/01/2013

PAGE TITLE: Func Test / No Test

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Functional Test Points

J9500: LIO Connector

FUNC_TEST			
TRUE	PP3V42_G3H	17 30 35 36 37 38 40 46 49 50 59 61 62 64	
TRUE	PP3V3_S0	8 11 12 13 15 17 18 27 30 36 38 39 40 41 42 43 44 45 56 59 61	
TRUE	PP1V5_S0SW_AUDIO	58 61	
TRUE	SYS_ONEWIRE	37 61	
TRUE	SMC_BC_ACOK	37 38 50 61	
TRUE	USB_PWR_EN	35 59 61	
TRUE	SMBUS_SMC_2_S3_SDA	37 40 61 73	
TRUE	SMBUS_SMC_2_S3_SCL	37 40 61 73	
TRUE	SPKRAMP_SHDN_L	47 61	
TRUE	FINSTACKSNS_ALERT_L	39 61	
TRUE	SPKRAMP_INR_N	47 61 74	
TRUE	SPKRAMP_INR_P	47 61 74	
TRUE	USB_EXTB_N	14 61 68	
TRUE	USB_EXTB_P	14 61 68	
TRUE	PP5V_S0_ALT_AUD_LDO_EN	61	
TRUE	SMC_lID	36 37 38 61 64	
TRUE	HDA_SDOUT	12 61 69	
TRUE	HDA_BIT_CLK	12 61 69	
TRUE	HDA_SDIN0	12 61 69	
TRUE	XDP_USB_EXTB_OC_L	14 16 61	
TRUE	HDA_RST_L	12 61 69	
TRUE	HDA_SYNC	12 61 69	
TRUE	USB3_EXTB_D2R_RC_P	61 65 68	
TRUE	USB3_EXTB_D2R_RC_N	61 65 68	
TRUE	USB3_EXTB_R2D_P	61 65 68	
TRUE	USB3_EXTB_R2D_N	61 65 68	
TRUE	AUD_PWR_EN	13 59 61	

(Need to add 5 GND TPs)

SD Card Aliases

		MAKE_BASE		
68 65 34 14	USB3_SD_D2R_P	TRUE	USB3_SD_D2R_P	14 34 65 68
68 65 34 14	USB3_SD_D2R_N	TRUE	USB3_SD_D2R_N	14 34 65 68
68 65 34 14	USB3_SD_R2D_C_P	TRUE	USB3_SD_R2D_C_P	14 34 65 68
68 65 34 14	USB3_SD_R2D_C_N	TRUE	USB3_SD_R2D_C_N	14 34 65 68
65 39 37 34 15	PP3V3_S0SW_SD		PP3V3_S0SW_SD	15 34 37 39 65

(MAKE_BASE=TRUE on page 45)

Bead Probes

68 61 14	USB3_EXTB_D2R_N	BEAD-PROBE	BPA511
68 61 14	USB3_EXTB_D2R_P	BEAD-PROBE	BPA510
68 65 61	USB3_EXTB_D2R_RC_N	BEAD-PROBE	BPA520
68 65 61	USB3_EXTB_D2R_RC_P	BEAD-PROBE	BPA521
68 61 14	USB3_EXTB_R2D_C_N	BEAD-PROBE	BPA513
68 61 14	USB3_EXTB_R2D_C_P	BEAD-PROBE	BPA512
68 65 61	USB3_EXTB_R2D_N	BEAD-PROBE	BPA523
68 65 61	USB3_EXTB_R2D_P	BEAD-PROBE	BPA522

SYNC_MASTER=J41_MLB SYNC_DATE=09/13/2012

PAGE TITLE: Project FCT/NC/Aliases

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J41/J43 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,MEM_TERM	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.110 MM	0.110 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110MM		0.095 MM	0.095 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL2,ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL3,ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL3,ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL4,ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

SYNC MASTER=CONSTRAINTS SYNC DATE=10/24/2012

PAGE TITLE

PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI 6 38
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD
	CPU_45S	CPU_TTP	XDP_DBRESET_L 16 17
	CPU_45S	CPU_TTP	XDP_CPU_PRDY_L 6 16 64
	CPU_45S	CPU_TTP	XDP_CPU_PREQ_L 6 16 64
	CPU_27P4S	CPU_COMP	EDP_COMP
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0> 6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1> 6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2> 6
	CPU_45S	CPU_TTP	CPU_CFG<11..0> 6 16 64
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L 6 37
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L 6 37 38 51
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD 6
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L 15 38
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N
XDP_TDI	CPU_45S	CPU_TTP	XDP_CPU_TDI 6 16 64
XDP_TDO	CPU_45S	CPU_TTP	XDP_CPU_TDO 6 16 64
XDP_TMS	CPU_45S	CPU_TTP	XDP_CPU_TMS 6 16 64
XDP_TCK	CPU_45S	CPU_TTP	XDP_CPU_TCK 6 16 64
XDP_TRST_L	CPU_45S	CPU_TTP	XDP_CPUPCH_TRST_L 6 12 16 64
XDP_BPM_L	CPU_45S	CPU_TTP	XDP_BPM_L<1..0> 6 16
	CPU_45S	CPU_TTP	XDP_BPM_L<7..2> 6 16
	CPU_45S	CPU_TTP	XDP_OBSDATA_B<3..0>
	CPU_45S	CPU_TTP	CPU_CFG<15..12> 6 16
(FSB_CPURST_L)	CPU_45S	CPU_TTP	XDP_CPURST_L 16
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P 8 51
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N 9 51
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L 8 51
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK 8 51
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT 8 51
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0> 12 30
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0> 12 30
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0> 30 64
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0> 30 64
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0> 12 30 64
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0> 12 30 64
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P 12 30 64
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N 12 30 64
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0> 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0> 25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0> 5 25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0> 5 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N 25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P 13 25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N 13 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0> 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0> 25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0> 5 18 25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0> 5 18 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N 25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P 13 18 25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N 13 18 25
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0> 60 64
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0> 60 64
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0> 5 60 64
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0> 5 60 64
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P 60 64
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N 60 64
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P 5 60
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N 5 60
	DP_80D	DP_AUX	DP_INT_AUXCH_P
	DP_80D	DP_AUX	DP_INT_AUXCH_N

PCIe SSD

DP

Note: DisplayPort tables are on Page 113

SYNC_MASTER=CONSTRAINTS SYNC_DATE=09/25/2012

PAGE TITLE: CPU Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	
USB_BT	USB_80D	USB	USB_BT_P	14 29
USB_BT	USB_80D	USB	USB_BT_N	14 29
	USB_80D	USB	USB_BT_CONN_P	29 64
	USB_80D	USB	USB_BT_CONN_N	29 64
	USB_80D	USB	USB_BT_WAKE_P	
	USB_80D	USB	USB_BT_WAKE_N	
USB_TPAD	USB_80D	USB	USB_TPAD_P	14 36 64
USB_TPAD	USB_80D	USB	USB_TPAD_N	14 36 64
	USB_80D	USB	USB_TPAD_CONN_P	
	USB_80D	USB	USB_TPAD_CONN_N	
	USB_80D	USB	TPAD_SPI_MOSI_USB_P	
	USB_80D	USB	TPAD_SPI_MISO_USB_N	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	
	SPI_45S	SPI	TPAD_SPI_MOSI	15 36
	SPI_45S	SPI	TPAD_SPI_MISO	15 36
	SPI_45S	SPI	TPAD_SPI_CLK	15 36
USB_EXTA	USB_80D	USB	USB_EXTA_P	14 35
USB_EXTA	USB_80D	USB	USB_EXTA_N	14 35
	UART_45S	UART	SMC_DEBUGPRT_TX_L	35 37 38
	UART_45S	UART	SMC_DEBUGPRT_RX_L	35 37 38
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_P	35
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_N	35
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_P	35
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_N	35
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 35
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 35
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	35
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	35
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_P	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_P	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 35
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 35
USB_EXTB	USB_80D	USB	USB_EXTB_P	14 61 65
USB_EXTB	USB_80D	USB	USB_EXTB_N	14 61 65
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_P	14 61 65
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_N	14 61 65
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_P	61 65
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_N	61 65
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P	61 65
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N	61 65
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_P	14 61 65
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_N	14 61 65
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3_SD_D2R_P	14 34 65
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3_SD_D2R_N	14 34 65
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_R2D_C_P	14 34 65
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_R2D_C_N	14 34 65
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P	34
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N	34
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P	34
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N	34
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	

USB Hucopyb nets

TP SPI nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

SYNC_MASTER=CLEAN_J43 SYNC_DATE=11/13/2012

PAGE TITLE: PCH Constraints 1

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DRAWING NUMBER: <SCH_NUM> SIZE: D

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
LPC_AD	LPC_45S	LPC	LPC_AD<3..0> 14 37 46 64
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L 14 37 46 64
	LPC_45S	LPC	LPCPLUS_RESET_L 18 46 64
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC 17 37
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R 12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS 17 46 64
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS_R 12 17
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK 14 16 19 25 40 56
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA 14 16 19 25 40 56
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK 14 40
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA 14 40
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL 14 32 37 40 43 44 64 73
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA 14 32 37 40 43 44 64 73
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK 12 61 65
	HDA_45S	HDA	HDA_BIT_CLK_R 12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC 12 61 65
	HDA_45S	HDA	HDA_SYNC_R 12
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L 12
	HDA_45S	HDA	HDA_RST_L 12 61 65
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0 12 61 65
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT 12 61 65
	HDA_45S	HDA	HDA_SDOUT_R 12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R 13 38
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K 37 38
SPI_CLK	SPI_45S	SPI	SPI_CLK_R 14 46
	SPI_45S	SPI	SPI_CLK 46
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R 14 46
	SPI_45S	SPI	SPI_MOSI 46
SPI_MISO	SPI_45S	SPI	SPI_MISO 14 46
	SPI_45S	SPI	SPI_MISO_R 46
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L 14 46
	SPI_45S	SPI	SPI_CS0_L 46
	SPI_45S	SPI	SPI_SMC_CLK 37 46
	SPI_45S	SPI	SPI_SMC_MOSI 37 46
	SPI_45S	SPI	SPI_SMC_MISO 37 46
	SPI_45S	SPI	SPI_SMC_CS_L 37 46
	SPI_45S	SPI	SPI_MLB_CLK 46
	SPI_45S	SPI	SPI_MLB_MOSI 46
	SPI_45S	SPI	SPI_MLB_MISO 46
	SPI_45S	SPI	SPI_MLB_CS_L 46
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P 29 64
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N 29 64
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P 14 29
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N 14 29
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P 14 29 64
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N 14 29 64
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P 12 29 64
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N 12 29 64
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0> 25
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0> 25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0> 14 25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0> 14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0> 14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0> 14 25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0> 25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0> 25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P 12 25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N 12 25
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N
XDP_TDI	PCH_45S	PCH_TTP	XDP_PCH_TDI 12 16 64
XDP_TDO	PCH_45S	PCH_TTP	XDP_PCH_TDO 12 16 64
XDP_TMS	PCH_45S	PCH_TTP	XDP_PCH_TMS 12 16 64
XDP_TCK	PCH_45S	PCH_TTP	XDP_PCH_TCK 12 16 64
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P 31 32
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N 31 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P 14 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N 14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P 14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N 14 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P 31 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N 31 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P 12 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N 12 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P 31 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N 31 32

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA 17 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP 31 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN 31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT 17 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R 25
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1 17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2 17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R 17
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2 34
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R 34 75
	CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1 34

SYNC_MASTER=J41_MLB SYNC_DATE=12/14/2012

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Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_CS_L<1..0>
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_ODT<0>
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_CS_L<1..0>
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_ODT<0>
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_N<7>
		MEM_PWR	PP1V2_S3
		MEM_PWR	PP0V6_S3_MEM_VREFCA_A
		MEM_PWR	PP0V6_S3_MEM_VREFDQ_A
		MEM_PWR	PP0V6_S3_MEM_VREFCA_B
		MEM_PWR	PP0V6_S3_MEM_VREFDQ_B

SYNC_MASTER=CONSTRAINTS SYNC_DATE=09/25/2012

PAGE TITLE: Memory Constraints

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0> 25 28
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0> 25 28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0> 28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0> 28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1> 25 28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1> 25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3> 25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3> 25 28
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2> 28
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2> 28
	DP_80D	DP_TX	DP_A_LSX_ML_P<1> 28
	DP_80D	DP_TX	DP_A_LSX_ML_N<1> 28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0> 28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0> 28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1> 25 28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1> 25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0> 25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0> 25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P 25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N 25 28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P 28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N 28
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P 28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N 28
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0> 64
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0> 64
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CP<3..1:2> 64
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CN<3..1:2> 64
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0> 64
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0> 64
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CP 25 64
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CN 25 64
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 25
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 25
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 25
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 25

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=CONSTRAINTS SYNC_DATE=09/25/2012

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 31 32
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 31 32
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 31 32
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 31 32
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 32 64
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 32 64
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 31 32
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 32 64
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 32 64
		S2_MEM_PWR	PP1V35_CAM 31 32
		S2_MEM_PWR	PP0V675_CAM_VREF 31 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ 32

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
2TO1_DIFFPAIR	*	=STANDARD	0.2 MM	0.1 MM	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL 37 40 60
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA 37 40 60
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL 14 32 37 40 43 44 64 69
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA 14 32 37 40 43 44 64 69
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL 37 40 61 65
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA 37 40 61 65
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL 36 37 40 44 64
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA 36 37 40 44 64
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL 37 40 48 50 64
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA 37 40 48 50 64

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SENSE_DIFFPAIR			CHGR_CSI_P 50
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSI_N 50
	2TO1_DIFFPAIR		CHGR_CSI_R_P 50
	2TO1_DIFFPAIR		CHGR_CSI_R_N 50
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_P 50
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_N 50
	2TO1_DIFFPAIR		CHGR_CSO_R_P 43 50
	2TO1_DIFFPAIR		CHGR_CSO_R_N 43 50

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1TO1_DIFFPAIR	0.200 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
THERM_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SPKR_DIFFPAIR	*	=1TO1_DIFFPAIR	0.300 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	44
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	44
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P	44
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N	44
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_N	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P	44
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N	44
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_P	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_N	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	44
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P	42 52
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N	42 52
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_P	42 52
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_N	42 52
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P_R	42 43
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N_R	42 43
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_P	42
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_N	42
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_P	42
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_N	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_N	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_P	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_P	41
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_P	42 55
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_N	42 55
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	41 43
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	41 43
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_N	41 53
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_P	41 53
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_N	43
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_P	43
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_N	43 44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_P	43 44
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	47 61 65
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	47 61 65
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_P	47
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_N	47
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	47 64
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	47 64
		SB_POWER	PP3V3_S5	8 11 13 15 16 17 18 28 29 34 42 57 58 59 60 62 64 65
		SB_POWER	PP3V3_S0	8 11 12 13 15 17 18 27 30 36 38 39 40 41 42 43 44 45 56 59 61
	GND		GND	

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE		

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE SPACING		
I344 SDDATA	SD_45SE		SDCONN_DATA<0..3>	33 34
I345 SDCLK	SD_45SE		SDCONN_CLK	33 34
I346	SD_45SE		SDCONN_WP	33 34
I347	SD_45SE		SDCONN_CMD	33 34
I348	SD_45SE		SDCONN_DETECT_L	33 34
I350	SD_45SE	SPI	SD_SPI_CLK	34
I351	SD_45SE	SPI	SD_SPI_CS_L	34
I352	SD_45SE	SPI	SD_SPI_MOSI	34
I353	SD_45SE	SPI	SD_SPI_MISO	34
I354	CLK_25M_45S		SDSCLK_CLK_25M_X1	
I355	CLK_25M_45S		SDCLK_CLK25M_X2_R	34 69

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<RDAR://COMPONENT/508934> J43 HW EE SCHEMATIC | PROTO 0
<RDAR://COMPONENT/508937> J43 HW EE SCHEMATIC | PROTO 1
<RDAR://COMPONENT/508941> J43 HW EE SCHEMATIC | EVT
<RDAR://COMPONENT/508945> J43 HW EE SCHEMATIC | DVT

Kismet:

afp://kismet.apple.com/Kismet-Projects/J41-J43

Useful Wiki Links:

Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions
Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:

<rdar://component/497591> MobileMac HW | Task
<rdar://component/497587> MobileMac HW | Schematic
<rdar://component/497585> MobileMac HW | New Bugs
<rdar://component/497588> MobileMac HW | Layout
<rdar://component/497590> MobileMac HW | Investigation
<rdar://component/497589> MobileMac HW | Architecture

Other Info:

Page Allocations - <rdar://problem/11791318> 2012 Schematic Page Allocations

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