1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-10-12

SCHEM,FLYING_DUTCHMAN,MLB,K91F

REV B RELEASE, 01/31/11

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8620	1	SCHEM,MLB,K91	SCH	CRITICAL	
820-2915	1	PCBF,MLB,K91	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Jan 31 12:49:37 2011

DRAWING TITLE: SCHEM,MLB,K91

Apple Inc.

DRAWING NUMBER: SIZE D

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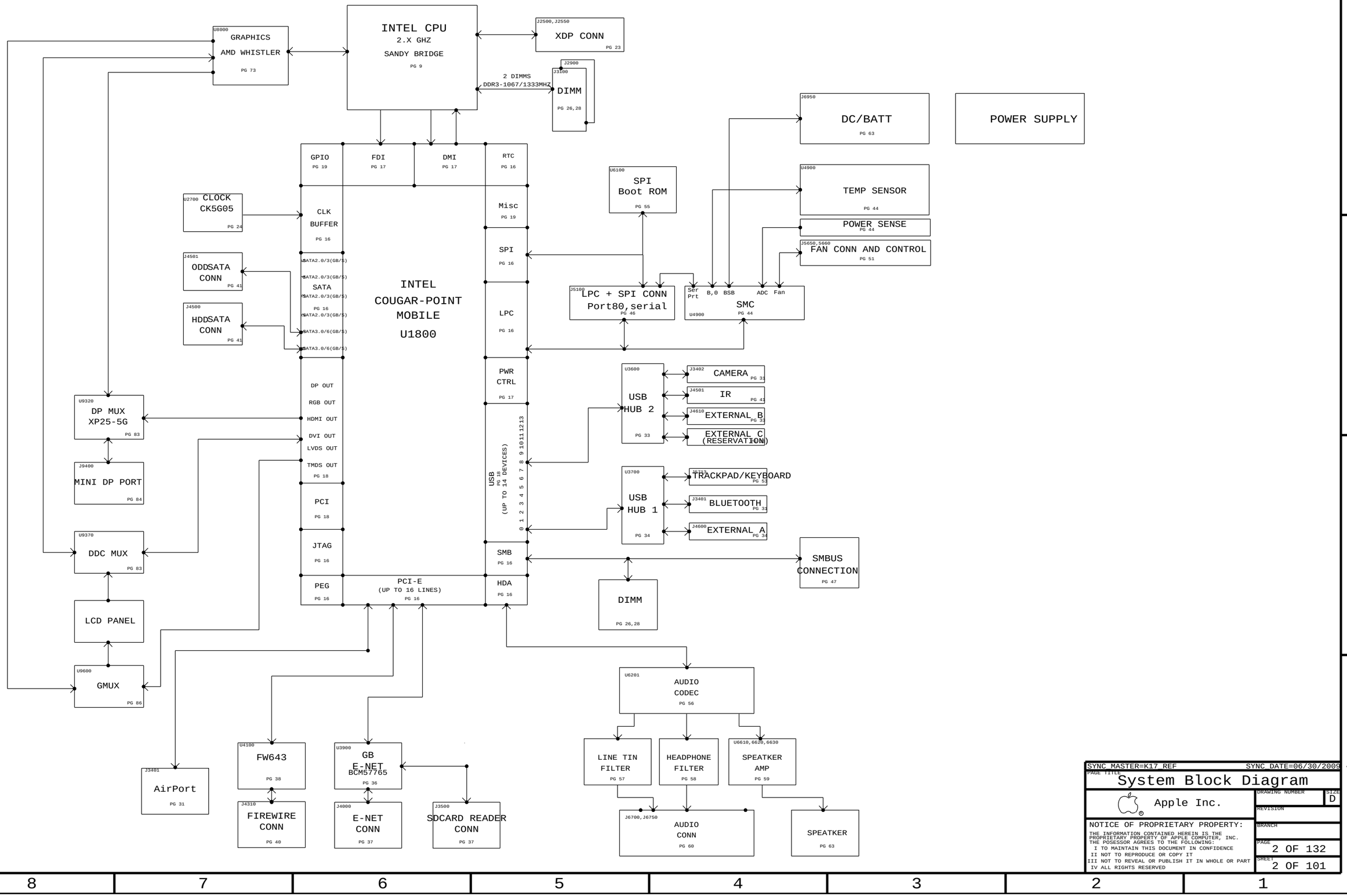

SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

PAGE TITLE

System Block Diagram

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K91 POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN
DCIN(16.5V)
F6905 6A FUSE
PP18V5_DCIN_CONN
R6990
D6990
PPBUS_G3H
F7040 8A FUSE
R7020
SMC_DCIN_ISENSE
U7000 ISL6259HRTZ PBUS SUPPLY/ BATTERY CHARGER (PAGE 64)
SMC_RESET_L
PPVBAT_G3H
R7050
SMC_BATT_ISENSE
J6950 3S2P (9 TO 12.6V)
PPVBATT_G3H_CONN
Q7055
CHGR_BGATE
PPVBAT_G3H_CHGR_R
SMC_PBUS_VSENSE
Q5315
ENABLE 3.425V G3HOT PM6640 U6990 (PAGE 62)
PP3V42_G3H
SMC PWRGD NCP303LSN U5000 (PAGE 45)
SMC_RESET_L
SMC AVREF SUPPLY REF3333 (PAGE 45)
PP3V3_S5_AVREF_SMC
PP3V3_S5_SMC
SMC_TPAD_RST_L
SMC_ONOFF_L
U5001
PP5V_S3_GFXIMVP6_VDD
GPU VCORE ISL6263C U8900 (PAGE 82)
R5388/U5388
GPUVCORE_EN
GPUVCORE_PGOOD
SMC_GPU_VSENSE
U5410
SMC_GPU_ISENSE
PPVCORE_GPU
PP5V_S0_CPUVTTS0
1.05V ISL95870 U7600 (PAGE 70)
CPUVTTS0_EN
CPUVTTS0_PGOOD
R7640
PPCPUVTT_S0
SMC_CPU_FSB_ISENSE
TPS22924 U4202 (PAGE 39)
PP1V0_FW_FWPHY
FW_PWR_EN
SMC_CPU_VSENSE
SMC_CPU_HI_ISENSE
CPU VCORE ISL95831 U7400 (PAGE 67)
CPUIMVP7_VR_ON
SMC_CPU_ISENSE
PPVCORE_S0_CPU
CPUIMVP7_AXG_PGOOD
PM_PCH_PWRGD
U2850
COUGAR_POINT U1800 (PAGE 16~21)
PM_PWRBTN_L
PLT_RERST_L
CPU_PWRGD
PM_MEM_PWRGD
GMUX U9600 XP25-5 (PAGE 86)
EG_RAIL1_EN → P1V1GPU_EN
EG_RAIL2_EN → P3V3GPU_EN
EG_RAIL3_EN → GPUVCORE_EN
EG_RAIL4_EN
PM_ALL_GPU_PGOOD
SMC U4900 (PAGE 44)
P60
SMC_PM_G2_EN
RC DELAY
P3V3S5_EN
PP5V_S3_DDRREG
U5440
SMC_CPU_DDR_VSENSE
R7350
SMC_DDR_ISENSE
PPDDR_S3_REG
PP1V5_S3
P1V0GPU_EN
P1V5FB_EN
1.003V(L/H) 1.503V(R/H) ISL6236 U9500 (PAGE 85)
PP1V0_S0GPU_REG
R5413
PP1V5_GPU_REG
SMC_GPU_1V8_ISENSE
P1V0GPU_PGOOD
P1V5FB_PGOOD
DDRREG_EN
DDRVTT_EN
1.5V S5 / 0.75V S3 TPS51116 U7300 (PAGE 66)
PPVTT_S0_DDR_LDO
DDRREG_PGOOD
4.5V MAX8840 U6200
PP3V3_S0
PP4V5_AUDIO_ANALOG
P1V5CPU_EN
SLG5AP020 U7801
Q7801
PP1V5_S3RS0
P1V5S0FET_GATE
Q7860
PP5V_S0
P5V_S0_EN
COUGAR-POINT MOBILE U1800 (PAGE 16~21)
SLP_S5#(L4)
SLP_S4#(H7)
SLP_S3#(P12)
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
R7978
PM_SLP_S3_L_R
P1V8S0_EN
P1V2S0_EN
CPUVTTS0_EN
P1V5CPU_EN
P5VS0_EN
P3V3S0_EN
PBUSVSENS_EN
P5VS3_EN
P3V3S5_EN
5V (L/H) 3.3V (R/H) TPS51125 U7201 (PAGE 65)
PP5V_S3
PP3V3_S5
PGOOD
P5V3V3_PGOOD
BKLT_PLT_RST_L && LCD_BKLT_NO
BKLT_EN
VIN LP8550 U9701 (PAGE 87)
PPVOUT_S0_LCDBKLT
Q9806
Q4260
PFWBOOST
SMC_ADAPTER_EN&&PM_SLP_S3_L
Q7870
PP3V3_S0GPU
P3V3GPU_EN
Q7810
PP3V3_S3
P3V3S3_EN
Q7830
PP3V3_S0_FET
P3V3S0_EN
Q7922
PP3V3_ENET
PP3V3_S0_PWRCTL
P1V8S0_PGOOD
P5V3V3_PGOOD
S0PGOOD_PWROK
PM_SLP_S3_L&&WOL_EN||SMC_ADAPTER_EN
TPS22924 U4201 (PAGE 39)
PP3V3_FW_FWPHY
FW_PWR_EN
P1V8_S0
P1V8FB_EN
SLG5AP020 U7880
Q7880
PP1V8_GPUIFPX
P1V8GPUIFPXFET_GATE
U7980
PM_ALL_GPU_PGOOD
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
99ms DLY
SMC
SMC_ADAPTER_EN
PM_RSMRST_L
CPUIMVP_VR_ON
PM_SYSRST_L
PM_PWRBTN_L
SMC_RESET_L
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
H8S2117 U4900 (PAGE 45)
P1V8S0_EN
P1V8_S0_EN
ISL8014A U7720 (PAGE 70)
PP1V8_S0
P1V8S0_PGOOD
PP3V3_S0
PP1V5_S0
PP1V05_S0
U7971 ISL88042IRTJJZ (PAGE 72)
TRST = 200mS
Q7850
PP1V2_S0
P1V2S0_EN
P1V2ENET_EN
ISL8014A U7760 (PAGE 70)
PP1V2_ENET
P1V2ENET_PGOOD
CPU U1000 (PAGE 9~14)
SM_DRAMPWROK
VCCCPUPWRGD
RESET#

SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

PAGE TITLE: Power Block Diagram

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Revision History

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1468	PCBA,MLB,K91F,DG64	K91_COMMON,SODIMM:FOXCONN,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DG64
639-1972	PCBA,MLB,K91F,DL83	K91_COMMON,SODIMM:HYBRID,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL83
639-1971	PCBA,MLB,K91F,DL82	K91_COMMON,SODIMM:MOLEX,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL82
639-1469	PCBA,MLB,K91F,DG65	K91_COMMON,SODIMM:FOXCONN,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DG65
639-1970	PCBA,MLB,K91F,DL86	K91_COMMON,SODIMM:HYBRID,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL86
639-1956	PCBA,MLB,K91F,DL7W	K91_COMMON,SODIMM:MOLEX,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL7W
639-1470	PCBA,MLB,K91F,DG66	K91_COMMON,SODIMM:FOXCONN,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DG66
639-1974	PCBA,MLB,K91F,DL87	K91_COMMON,SODIMM:HYBRID,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL87
639-1976	PCBA,MLB,K91F,DL88	K91_COMMON,SODIMM:MOLEX,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL88
639-1471	PCBA,MLB,K91F,DG67	K91_COMMON,SODIMM:FOXCONN,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DG67
639-1973	PCBA,MLB,K91F,DL81	K91_COMMON,SODIMM:HYBRID,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL81
639-1954	PCBA,MLB,K91F,DL7T	K91_COMMON,SODIMM:MOLEX,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL7T
639-1573	PCBA,MLB,K91,DHMV	K91_COMMON,SODIMM:FOXCONN,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DHMV
639-1945	PCBA,MLB,K91,DL7Q	K91_COMMON,SODIMM:HYBRID,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DL7Q
639-1953	PCBA,MLB,K91,DL7R	K91_COMMON,SODIMM:MOLEX,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DL7R
639-1574	PCBA,MLB,K91,DHMW	K91_COMMON,SODIMM:FOXCONN,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DHMW
639-1959	PCBA,MLB,K91,DL80	K91_COMMON,SODIMM:HYBRID,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DL80
639-1960	PCBA,MLB,K91,DL7Y	K91_COMMON,SODIMM:MOLEX,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DL7Y
085-1901	K91/K91F DEVELOPMENT BOM	K91_DEVEL:ENG

K91 BOM GROUPS

BOM GROUP	BOM OPTIONS
K91_COMMON	ALTERNATE,COMMON,K91_COMMON1,K91_COMMON2,K91_PROGPARTS,K91_PROGPARTS1,UVGLUE_K91_K91F,K91_PVT
K91_COMMON1	CPUMEM_S0,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_2NONREM,USBHUB_2513B
K91_COMMON2	GPUVID_1P11V,KB_BL,T29:YES,ENET_SD:B0,T29BST:Y,SDRV_PD,SDRVI2C:MCU,T29_DP_HPD:ALL_OR
K91_PVT	BMON:PROD,VREFMRGN_NOT,XDP,XDP_CPU_BPM,BKLT:PROD,ISNS_ON:NO,LPCPLUS_R:YES
K91_PROGPARTS	GMUX_PROG,IR_PROG,TPAD_PROG:PVT,ENETROM_PROG:PVT,T29ROM:PROG,T29MCU:PROG
K91_PROGPARTS1	SMC_PROG:PVT,BOOTROM_PROG:PVT
K91_DEVEL:ENG	SNB_CPT_XDP,BMON:ENG,GMUX_JTAG_CONN,VREFMRGN,LPCPLUS_CONN:YES,LPCPLUS_R:YES,BKLT:ENG,S0PGOOD_ISL,CPURIPPLE_ENG,IMVPISNS_ENG,ISNS_ON:YES,DEBUG_ADC,DIGI_MIC
K91_DEVEL:PVT	SNB_CPT_XDP,LPCPLUS_CONN:YES,LPCPLUS_R:YES
SNB_CPT_XDP	XDP,XDP_CONN,XDP_CPU_BPM,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4031	1	IC,CPU,SNB,SR030,PRQ,D2,2.0,45W,4+2,1.20,6M,BGA	U1000	CRITICAL	CPU:2_0GHZ
337S4032	1	IC,CPU,SNB,SR00W,PRQ,D2,2.2,45W,4+2,1.30,6M,BGA	U1000	CRITICAL	CPU:2_2GHZ
337S4033	1	IC,CPU,SNB,SR00U,PRQ,D2,2.3,45W,4+2,1.30,8M,BGA	U1000	CRITICAL	CPU:2_3GHZ
337S4029	1	IC,PCH,COUGARPOINT,SLH9D,PRQ,BD82HM65	U1800	CRITICAL	
337S3936	1	IC,GPU,AMD,WHISTLER,962FCBGA,40NM,ES	U8000	CRITICAL	GPU:WHISTLER
337S3979	1	IC,GPU,AMD,SEYMOUR,M2 LP,ES1,962BGA	U8000	CRITICAL	GPU:SEYMOUR
338S0945	1	IC,ASSP,LIGHTRIDGE,S LHAJ,PRQ,FCBGA,15X15MM	U3600	CRITICAL	T29:YES
343S0534	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN8X8,B0	U3900	CRITICAL	ENET_SD:B0
343S0494	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN8X8,A0	U3900	CRITICAL	ENET_SD:A0
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
333S0543	4	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_512_SAMSUNG
333S0564	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8400,U8450,U8500,U8550	CRITICAL	FB_512_HYNIX
333S0571	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,C-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_SAMSUNG
333S0572	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,M-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX
333S0543	2	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8500,U8550	CRITICAL	FB_256_SAMSUNG
333S0564	2	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8500,U8550	CRITICAL	FB_256_HYNIX
353S3055	1	IC,PI3VEDP212,X2 DISPLAYPORT 2:1 MUX,QFN	U9390	CRITICAL	
725-1479	1	MLB LOCTITE UV EB CPU,PCH,T29,GPU,K91	UV_GLUE_K91_K91F	CRITICAL	UVGLUE_K91_K91F
516S0806	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,FOXCONN	J3100	CRITICAL	SODIMM:FOXCONN
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:FOXCONN
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:MOLEX
516-0245	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,MOLEX	J2900	CRITICAL	SODIMM:MOLEX
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:HYBRID
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:HYBRID

ETHERNET ROM

335S0663	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENETROM_BLANK
341S2685	1	IC,ENET,1MBITFLASH,CIV REV01,K74/K75,K40	U3990	CRITICAL	ENETROM_PROG:A0_SD
341S2973	1	IC,ENET,1MBITFLASH,CIV REV01,K60/K62	U3990	CRITICAL	ENETROM_PROG:B0_SD
341S3026	1	IC,ENET,1MBITFLASH,CIV REV01,K901/K91/K92	U3990	CRITICAL	ENETROM_PROG:EVT
341S3096	1	IC,ENET ROM,1MBIT,DVT,PVT,K901/K91x	U3990	CRITICAL	ENETROM_PROG:PVT

Alternate Parts

(Alternate) (Primary)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
353S2805	353S2603		ALL	Fairchild wafer option
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
353S3085	353S1658		ALL	ST Micro alt to LT
376S0972	376S0612		ALL	ROHM alt to Toshiba N-FET
376S0855	376S0613		ALL	Diodes alt to Toshiba dual N-FET
138S0676	138S0691		ALL	Murata alt to Samsung cap
138S0652	138S0648		ALL	Samsung / Murata alt for Taiyo Yuden
138S0681	138S0638		ALL	Taiyo Yuden alt for Samsung
152S0685	152S0796		ALL	Dale/Vishay/TDK alt for Cyntec
376S0977	376S0859		ALL	Diodes alt for Rohm
353S2592	353S3199		ALL	1024x1 24BIT CBRIC OLD REV IC ALTERNATE FOR NEW REV
335S0550	335S0777		ALL	add 4K byte as alternative to 2K
371S0679	371S0652		ALL	NXP alternate for pin diodes
138S0671	138S0673		ALL	Taiyo Yuden alt for Murata 10 uF caps

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DDKG]	CRITICAL	EEEE:DDKG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG63]	CRITICAL	EEEE:DG63
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG64]	CRITICAL	EEEE:DG64
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG65]	CRITICAL	EEEE:DG65
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG66]	CRITICAL	EEEE:DG66
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG67]	CRITICAL	EEEE:DG67
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DHMV]	CRITICAL	EEEE:DHMV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DHMW]	CRITICAL	EEEE:DHMW
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL81]	CRITICAL	EEEE:DL81
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL82]	CRITICAL	EEEE:DL82
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL83]	CRITICAL	EEEE:DL83
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL84]	CRITICAL	EEEE:DL84
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL85]	CRITICAL	EEEE:DL85
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL86]	CRITICAL	EEEE:DL86
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL87]	CRITICAL	EEEE:DL87
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL88]	CRITICAL	EEEE:DL88
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL89]	CRITICAL	EEEE:DL89
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7Q]	CRITICAL	EEEE:DL7Q
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7R]	CRITICAL	EEEE:DL7R
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7T]	CRITICAL	EEEE:DL7T
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7V]	CRITICAL	EEEE:DL7V
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7W]	CRITICAL	EEEE:DL7W
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7Y]	CRITICAL	EEEE:DL7Y
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL80]	CRITICAL	EEEE:DL80

Programmables - All Builds

341S2830	1	IC,CPLD,LATTICE,GMUX,K91/K91F	U9600	CRITICAL	GMUX_PROG
336S0042	1	IC,PLD,LATTICE,LFXP2-5E-5,132 BALL CSBGA	U9600	CRITICAL	GMUX_BLANK
341S2384	1	IR,ENCORE II,CY7C63833-LFXC	U4800	CRITICAL	IR_PROG
341S3129	1	IC,T29 EEPROM,PVT,K9x	U3690	CRITICAL	T29ROM:PROG
335S0777	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	T29ROM:BLANK
341S3128	1	IC,PROGRMD,LPC1112A,T29 PORT MCU,PVT,HVQFN25	U9330	CRITICAL	T29MCU:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2957	1	IC,GPU ROM,K91/F,K92,PROG	U8701	CRITICAL	GPUROM:PROG
335S0724	1	IC,GPU ROM,K91/F,K92,BLANK	U8701	CRITICAL	GPUROM:BLANK

SMC

338S0895	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2854	1	IC,SMC,DEVELOPMENT-PROTO0,K91	U4900	CRITICAL	SMC_PROG:PROTO0
341S2935	1	IC,SMC,DEVELOPMENT-PROTO1,K91	U4900	CRITICAL	SMC_PROG:PROTO1
341S2994	1	IC,SMC,DEVELOPMENT-PROTO2,K91	U4900	CRITICAL	SMC_PROG:PROTO2
341S2861	1	IC,SMC,DEVELOPMENT-EVT,K91	U4900	CRITICAL	SMC_PROG:EVT
341S2864	1	IC,SMC,DEVELOPMENT-DVT,K91	U4900	CRITICAL	SMC_PROG:DVT
341S2867	1	IC,SMC,DEVELOPMENT-PVT,K91	U4900	CRITICAL	SMC_PROG:PVT

EFI ROM

335S0740	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341S2893	1	IC,EFI,ROM,PROTO0, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S2934	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S2991	1	IC,EFI,ROM,PROTO2, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S2894	1	IC,EFI,ROM,EVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:EVT
341S2895	1	IC,EFI,ROM,DVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:DVT
341S2896	1	IC,EFI,ROM,PVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PVT

PSOC

341S2902	1	IC,TP PSOC,K9x,PROTO0	U5701	CRITICAL	TPAD_PROG:PROTO0
341S2940	1	IC,TP PSOC,K9x,PROTO1	U5701	CRITICAL	TPAD_PROG:PROTO1
341S3001	1	IC,TP PSOC,K9x,PROTO2	U5701	CRITICAL	TPAD_PROG:PROTO2
341S3024	1	IC,TP PSOC,K9x,EVT	U5701	CRITICAL	TPAD_PROG:EVT
341S3099	1	IC,TP PSOC,K9x,DVT,PVT	U5701	CRITICAL	TPAD_PROG:PVT

SYNC_MASTER=K17_REF SYNC_DATE=05/28/2009

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Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST

TRUE	PP5V S0	101	3 TPs per Fan
TRUE	FAN LT PWM	51	
TRUE	FAN LT TACH	51	

J5660 (RIGHT FAN CONN)

TRUE	PP5V S0	101	2 TPs
TRUE	FAN RT PWM	51	
TRUE	FAN RT TACH	51	
TRUE	GND		5 TPs per Fan

J6780 (MIC CONN)

TRUE	BI MIC N	60 61	
TRUE	BI MIC SHIELD	60 61	
TRUE	BI MIC P	60 61	

J6781 & J6782 (SPEAKERS CONN)

TRUE	SPKRCONN L OUT P	59 60 98
TRUE	SPKRCONN L OUT N	59 60 98
TRUE	SPKRCONN R OUT P	59 60 98
TRUE	SPKRCONN R OUT N	59 60 98
TRUE	SPKRCONN S OUT P	59 60 98
TRUE	SPKRCONN S OUT N	59 60 98

J9000 (LVDS CONN)

TRUE	PP3V3 SW LCD	82	
TRUE	PP3V3 S0	84 87 88 89 90 82	
TRUE	PPVOUT S0 LCDBKLT	82 88 100	2 TP needed
TRUE	LVDS DDC CLK	82 83	
TRUE	LVDS DDC DATA	82 83	
TRUE	LVDS CONN A DATA P<0>	82 83 97	
TRUE	LVDS CONN A DATA N<0>	82 83 97	
TRUE	LVDS CONN A DATA P<1>	82 83 97	
TRUE	LVDS CONN A DATA N<1>	82 83 97	
TRUE	LVDS CONN A DATA P<2>	82 83 97	
TRUE	LVDS CONN A DATA N<2>	82 83 97	
TRUE	LVDS CONN A CLK F P	82 97	
TRUE	LVDS CONN A CLK F N	82 97	
TRUE	LVDS CONN B DATA P<0>	82 83 97	
TRUE	LVDS CONN B DATA N<0>	82 83 97	
TRUE	LVDS CONN B DATA P<1>	82 83 97	
TRUE	LVDS CONN B DATA N<1>	82 83 97	
TRUE	LVDS CONN B DATA P<2>	82 83 97	
TRUE	LVDS CONN B DATA N<2>	82 83 97	
TRUE	LVDS CONN B CLK F P	82 97	
TRUE	LVDS CONN B CLK F N	82 97	
TRUE	LED RETURN 1	82 88	
TRUE	LED RETURN 2	82 88	
TRUE	LED RETURN 3	82 88	
TRUE	LED RETURN 4	82 88	
TRUE	LED RETURN 5	82 88	
TRUE	LED RETURN 6	82 88	
TRUE	GND		4 TPs

J4500 (SATA ODD CONN)

TRUE	PP5V SW ODD	41	3 TPs
TRUE	SMC ODD DETECT	41 44	
TRUE	SATA ODD D2R C P	41	
TRUE	SATA ODD D2R C N	41	
TRUE	SATA ODD R2D P	41 92	
TRUE	SATA ODD R2D N	41 92	
TRUE	SATA ODD D2R UF P	41 92	
TRUE	SATA ODD D2R UF N	41 92	
TRUE	GND		5 TPs

J4501 (SATA HDD CONN)

TRUE	PP5V S0 HDD FLT	41
TRUE	SATA HDD R2D P	41 92
TRUE	SATA HDD R2D N	41 92
TRUE	SATA HDD D2R C N	41 92
TRUE	SATA HDD D2R C P	41 92
TRUE	GND	

J5815 (KBD BACKLIGHT CONN)

TRUE	KBDLED ANODE	53
TRUE	SMC KDBLED PRESENT L	53
TRUE	GND	

FUNC_TEST

TRUE	GND	
TRUE	GND	6 TPs

USB PORTS

TRUE	PP5V S3 RTUSB A F	42	
TRUE	USB2 LT1 N	42 98	
TRUE	USB2 LT1 P	42 98	
TRUE	GND		3 TPs per Fan
TRUE	PP5V S3 RTUSB B F	42	
TRUE	USB LT2 N	42 98	
TRUE	USB LT2 P	42 98	
TRUE	GND		2 TPs

J3401 & J3402 (AIRPORT/BT/CAMERA CONN)

TRUE	PCIE AP D2R P	16 31 93
TRUE	PCIE AP D2R N	16 31 93
TRUE	PCIE AP R2D P	31 93
TRUE	PCIE AP R2D N	31 93
TRUE	PCIE CLK100M AP CONN_P	31 98
TRUE	PCIE CLK100M AP CONN_N	31 98
TRUE	AP CLKREQ Q L	31
TRUE	PCIE WAKE L	17 25 31 84
TRUE	WIFI EVENT L	31 44 45
TRUE	AP RESET CONN L	31
TRUE	PP3V3 WLAN	31 45
TRUE	PP5V S3 ALSCAMERA F	31
TRUE	SMBUS SMC A S3 SDA	6 31 44 47 53 54 96
TRUE	SMBUS SMC A S3 SCL	6 31 44 47 53 54 96
TRUE	USB CAMERA CONN P	31 92
TRUE	USB CAMERA CONN N	31 92
TRUE	CONN USB2 BT P	98
TRUE	CONN USB2 BT N	98
TRUE	SMBUS SMC 0 S0 SCL	31 44 47 59 79 96
TRUE	SMBUS SMC 0 S0 SDA	31 44 47 59 79 96

J6950 (BAT CONN)

TRUE	SYS DETECT L	62

J5800 (IPD FLEX CONN)

TRUE	PP18V5 S4	53
TRUE	Z2 HOST INTN	52 53
TRUE	Z2 MOSI	52 53
TRUE	Z2 CS L	52 53
TRUE	Z2 DEBUG3	52 53
TRUE	Z2 MISO	52 53
TRUE	Z2 BOOST EN	53
TRUE	Z2 SCLK	52 53
TRUE	Z2 CLKIN	52 53
TRUE	Z2 KEY ACT L	52 53
TRUE	Z2 RESET	52 53
TRUE	PSOC F CS L	52 53
TRUE	PICKB L	52 53
TRUE	PSOC MISO	52 53
TRUE	PSOC MOSI	52 53
TRUE	PSOC SCLK	52 53
TRUE	SMBUS SMC A S3 SCL	6 31 44 47 53 54 96
TRUE	SMBUS SMC A S3 SDA	6 31 44 47 53 54 96

J6900 (DC POWER CONN)

TRUE	ADAPTER SENSE	62
TRUE	PP18V5 DCIN FUSE	62
TRUE	GND	

J6950 (MAIN BATT CONN)

TRUE	PPVBAT G3H CONN	62 63
TRUE	SMBUS SMC BSA SCL	6 44 47 62 63 96
TRUE	SMBUS SMC BSA SDA	6 44 47 62 63 96
TRUE	NC SMC BS ALRT L	6
TRUE	GND	

J6995 (BAT LED CONN)

TRUE	PP3V42 G3H	6 7 25 42 44 45 46 47 52 62 63 72
TRUE	SMBUS SMC BSA SDA	6 44 47 62 63 96
TRUE	SMBUS SMC BSA SCL	6 44 47 62 63 96
TRUE	SMC BIL BUTTON L	44 45 62
TRUE	GND	

J5713 (KEY BOARD CONN)

TRUE	PP3V3 S3	21 72 87
TRUE	PP3V42 G3H	21 72 87 48 51 72 78 79 80 82 84 87 88 89 90
TRUE	WS KBD1	52
TRUE	WS KBD2	52
TRUE	WS KBD3	52
TRUE	WS KBD4	52
TRUE	WS KBD5	52
TRUE	WS KBD6	52
TRUE	WS KBD7	52
TRUE	WS KBD8	52
TRUE	WS KBD9	52
TRUE	WS KBD10	52
TRUE	WS KBD11	52
TRUE	WS KBD12	52
TRUE	WS KBD13	52
TRUE	WS KBD14	52
TRUE	WS KBD15 CAP	52
TRUE	WS KBD16 NUM	52
TRUE	WS KBD17	52
TRUE	WS KBD18	52
TRUE	WS KBD19	52
TRUE	WS KBD20	52
TRUE	WS KBD21	52
TRUE	WS KBD22	52
TRUE	WS KBD23	52
TRUE	WS KBD ONOFF L	52
TRUE	WS LEFT SHIFT KBD	52
TRUE	WS LEFT OPTION KBD	52
TRUE	WS CONTROL KBD	52

J6950 (BIL CABLE CONN)

TRUE	PP5V S3 IR R	41
TRUE	SMC LID R	62
TRUE	IR RX OUT	41 43
TRUE	SYS LED ANODE	41 45
TRUE	GND	

FUNC_TEST

TRUE	BKLT EN	
TRUE	TP ISSP SCLK P1_1	8 52
TRUE	TP ISSP SDATA P1_0	8 52
TRUE	LCD BKLT PWM	87 88
TRUE	LPCPLUS GPIO	19 46
TRUE	LPCPLUS RESET L	25 46 87 93
TRUE	LPC AD<0..3>	16 44 46 87 93
TRUE	LPC CLK33M LPCPLUS	25 46 93
TRUE	LPC FRAME L	16 44 46 87 93
TRUE	LPC PWRDWN L	17 44 46
TRUE	LPC SERIRQ	16 44 46
TRUE	PM CLKRUN L	17 44 46
TRUE	PM SYSRST L	17 25 44
TRUE	SMC MD1	44 46
TRUE	SMC NMI	44 46
TRUE	SMC ONOFF L	44 45 52
TRUE	SMC RESET L	42 44 45 46 63
TRUE	SMC RX L	42 44 45 46
TRUE	SMC TCK	44 45 46
TRUE	SMC TDI	44 45 46
TRUE	SMC TDO	44 45 46
TRUE	SMC TMS	44 45 46
TRUE	SMC TRST L	44 46
TRUE	SMC TX L	42 44 45 46
TRUE	SPIROM USE MLB	19 46 55
TRUE	SPI ALT CLK	46
TRUE	SPI ALT CS L	46
TRUE	SPI ALT MISO	46
TRUE	SPI ALT MOSI	46
TRUE	SYS LED ANODE R	41

NO_TEST=TRUE

TRUE	T29 D2R P<1..0>	33 84 95
TRUE	T29 D2R N<1..0>	33 84 95
TRUE	T29 D2R C P<1..0>	84 85 95
TRUE	T29 D2R C N<1..0>	84 85 95
TRUE	T29 R2D C P<1..0>	33 84 95
TRUE	T29 R2D C N<1..0>	33 84 95
TRUE	T29 R2D P<1..0>	84 95
TRUE	T29 R2D N<1..0>	84 95
TRUE	T29DPA ML P<3..0>	84 85 95
TRUE	T29DPA ML N<3..0>	84 85 95
TRUE	DP T29SNK0 AUXCH C P	33 78 95
TRUE	DP T29SNK0 AUXCH C N	33 78 95
TRUE	DP T29SNK0 AUXCH P	33 95
TRUE	DP T29SNK0 AUXCH N	33 95
TRUE	DP T29SNK0 ML C P<3..0>	33 78 95
TRUE	DP T29SNK0 ML C N<3..0>	33 78 95
TRUE	DP T29SNK0 ML P<3..0>	33 95
TRUE	DP T29SNK0 ML N<3..0>	33 95
TRUE	DP T29SNK1 AUXCH C P	33 78 95
TRUE	DP T29SNK1 AUXCH C N	33 78 95
TRUE	DP T29SNK1 AUXCH P	33 95
TRUE	DP T29SNK1 AUXCH N	33 95
TRUE	DP T29SNK1 ML C P<3..0>	33 78 95
TRUE	DP T29SNK1 ML C N<3..0>	33 78 95
TRUE	DP T29SNK1 ML P<3..0>	33 95
TRUE	DP T29SNK1 ML N<3..0>	33 95
TRUE	TP DP T29SRC AUXCH CN	33
TRUE	TP DP T29SRC AUXCH CP	33
TRUE	TP DP T29SRC ML CP<3..0>	33
TRUE	TP DP T29SRC ML CN<3..0>	33
TRUE	DP SDRVA ML C P<0>	84 95
TRUE	DP SDRVA ML C N<0>	84 95
TRUE	DP SDRVA ML C P<2>	84 95
TRUE	DP SDRVA ML C N<2>	84 95
TRUE	DP SDRVA ML P<0>	84 95
TRUE	DP SDRVA ML N<0>	84 95
TRUE	DP SDRVA ML P<2>	84 95
TRUE	DP SDRVA ML N<2>	84 95
TRUE	TP T29 PCIE RESET0 L	33
TRUE	TP T29 PCIE RESET1 L	33
TRUE	TP T29 PCIE RESET2 L	33
TRUE	TP T29 PCIE RESET3 L	33
TRUE	T29DPA D2R1 AUXCH N	85 95
TRUE	T29DPA D2R1 AUXCH P	85 95
TRUE	T29 D2R1 BIAS	

POWER RAILS

FUNC_TEST

TRUE	PM SLP S3 L	17 29 44
TRUE	PP0V75 S0 DDRVTT	66 72 26 28 29
TRUE	PP18V5 S3	44 67 69
TRUE	PP1V05 S0	17 26 72
TRUE	PP1V05 S0GPU	23 35 39
TRUE	PP1V05 S5	72 103
TRUE	PP1V0 FW FWPHY	7 38 39
TRUE	PP1V2 ENET	7 36 70
TRUE	PP1V2 S0	7 70 87
TRUE	PP1V5 S3	7 26 28 29
TRUE	PP1V5 S3RS0	66 71 98
TRUE	PP1V8R1V55 S0GPU_ISNS	
TRUE	PP1V8R1V55 S0GPU_ISNS_R	
TRUE	PP1V8 GPUIFPX	7 71 100
TRUE	PP1V8 S0	71 87
TRUE	PP3V3 ENET	7 14 17 20 22 25 70
TRUE	PP3V3 FW FWPHY	80 88 89 83
TRUE	PP3V3 S0	53 56 60 45 47 48 67 72 73
TRUE	PP3V3 S0GPU	8 12 16 39 41 49 50 51 61 73 72 84 87 88
TRUE	PP3V3 S3	7 26 28 29 66 71 84 87 88
TRUE	PP3V3 S5 AVREF SMC	44
TRUE	PP3V42 G3H	20 37 47 48 25 42 48
TRUE	PP5V S0	72 86 88 53 64 67 68 69 71
TRUE	PP5V S3	53 64 67 68 69 71 101
TRUE	PP5V S5	7 53 65 71
TRUE	PPBUS G3H	63 88 48 49 62 39
TRUE	PPDCIN G3H	7 48 62 63
TRUE	PPVCORE GPU	7 48 74 81
TRUE	PPVCORE S0 CPU	7 12 14 48 68 101
TRUE	PPVCORE S0 GFX	
TRUE	PPVP FW	7 39 40
TRUE	PPVTTDDR S3	7 30 66

NC NO_TESTS

NO_TEST

TRUE	TP FW643 NAND TREE	38
TRUE	TP FW643 OCR10 CTL	38
TRUE	TP FW643 SCIFCLK	38
TRUE	TP FW643 SCIFDAIN	38
TRUE	TP FW643 SCIFDOUT	38
TRUE	TP FW643 SCIFMC	38
TRUE	TP FW643 SDA	38
TRUE	TP FW643 SE	38
TRUE	TP FW643 SM	38
TRUE	TP FW643 CE	38
TRUE	TP FW643 FW620 L	38
TRUE	TP FW643 JASI EN	38
TRUE	DMI S2N N<1>	90 97
TRUE	DMI S2N P<1>	90 97
TRUE	FDI DATA N<1>	90 97
TRUE	FDI DATA P<1>	90 97
TRUE	FDI FSYNC<1..0>	90 97
TRUE	FDI LSYNC<1..0>	90 97
TRUE	FDI INT	9 97 98
TRUE	TP FW643 VAUX ENABLE	38
TRUE	TP FW643 VBUF	38
TRUE	TP FW643 TCK	38
TRUE	TP FW643 TDO	38
TRUE	TP FW643 TMS	38
TRUE	TP SMC P10	44 45
TRUE	TP P7 7	52
TRUE	TP PSOC SCL	52
TRUE	TP PSOC SDA	52
TRUE	TP SMC P24	44 45
TRUE	DC TEST BH1 BG2	12
TRUE	DC TEST BH3 BJ2	12
TRUE	TP USB HUB1 OCS1	24
TRUE	TP USB HUB1 PRTPWR1	24
TRUE	TP USB HUB2 OCS1	24
TRUE	TP USB HUB2 PRTPWR1	24
TRUE	TP DC TEST A62	12
TRUE	TP DC TEST D65	12
TRUE	TP SMC PF5	44 45

ICT Test Points

CPU NO_TESTS

NO_TEST

TP CPU RSVD<65..62>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD<65..62>
TP CPU RSVD<58..45>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD<58..45>
TP CPU RSVD<43..32>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD<43..32>
TP CPU RSVD<27..26>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD<27..26>
TP CPU RSVD<24..15>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD<24..15>
TP CPU RSVD<2..1>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD<2..1>
TP CPU RSVD NCTF<8..5>	TRUE	MAKE_BASE=TRUE	NC TP CPU RSVD NCTF<8..5>

NC NO_TESTS

NO_TEST

NC CRT IG BLUE	TRUE	MAKE_BASE=TRUE	NC CRT IG BLUE
NC CRT IG GREEN	TRUE	MAKE_BASE=TRUE	NC CRT IG GREEN
NC CRT IG RED	TRUE	MAKE_BASE=TRUE	NC CRT IG RED
NC CRT IG DDC CLK	TRUE	MAKE_BASE=TRUE	NC CRT IG DDC CLK
NC CRT IG DDC DATA	TRUE	MAKE_BASE=TRUE	NC CRT IG DDC DATA
NC CRT IG HSYNC	TRUE	MAKE_BASE=TRUE	NC CRT IG HSYNC
NC CRT IG VSYNC	TRUE	MAKE_BASE=TRUE	NC CRT IG VSYNC
NC LVDS IG CTRL CLK	TRUE	MAKE_BASE=TRUE	NC LVDS IG CTRL CLK
NC LVDS IG CTRL DATA	TRUE	MAKE_BASE=TRUE	NC LVDS IG CTRL DATA
NC PCH LVDS VBG	TRUE	MAKE_BASE=TRUE	NC PCH LVDS VBG
NC HDA SDIN1	TRUE	MAKE_BASE=TRUE	NC HDA SDIN1
NC HDA SDIN2	TRUE	MAKE_BASE=TRUE	NC HDA SDIN2
NC HDA SDIN3	TRUE	MAKE_BASE=TRUE	NC HDA SDIN3

NC NO_TESTS

NO_TEST

TRUE	TP AUD GPIO 2	56
TRUE	TP AUD GPIO 1	56
TRUE	TP AUD LO1 L N	56
TRUE	TP AUD LO1 L P	56
TRUE	TP BKL FAULT	88
TRUE	TP SPI DESCRIPTOR OVERRIDE L	44
TRUE	TP XDPPCH HOOK2	23
TRUE	TP XDPPCH HOOK3	23
TRUE	TP GMUX PL6B	87
TRUE	PM RSMRST L	17 72
TRUE	CPUIMVP BOOT1	67 68
TRUE	CPUIMVP BOOT2	67 68
TRUE	CPUIMVP UGATE2	67 68
TRUE	TP 1V05 S0 PCH VCCAPLLEXP	20

NC PCI PME L	TRUE	MAKE_BASE=TRUE	NC PCI PME L
NC PCI CLK33M OUT3	TRUE	MAKE_BASE=TRUE	NC PCI CLK33M OUT3
NC PCIE CLK100M PE4N	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE4N
NC PCIE CLK100M PE4P	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE4P
NC PCIE CLK100M PE5N	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE5N
NC PCIE CLK100M PE5P	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE5P
NC PCIE CLK100M PE6N	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE6N
NC PCIE CLK100M PE6P	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE6P
NC PCIE CLK100M PE7N	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE7N
NC PCIE CLK100M PE7P	TRUE	MAKE_BASE=TRUE	NC PCIE CLK100M PE7P
NC PSOC P1 3	TRUE	MAKE_BASE=TRUE	NC PSOC P1 3
NC SATA B D2RN	TRUE	MAKE_BASE=TRUE	NC SATA B D2RN
NC SATA B D2RP	TRUE	MAKE_BASE=TRUE	NC SATA B D2RP
NC SATA B R2D CN	TRUE	MAKE_BASE=TRUE	NC SATA B R2D CN
NC SATA B R2D CP	TRUE	MAKE_BASE=TRUE	NC SATA B R2D CP
NC SATA D D2RN	TRUE	MAKE_BASE=TRUE	NC SATA D D2RN
NC SATA D D2RP	TRUE	MAKE_BASE=TRUE	NC SATA D D2RP
NC SATA D R2D CN	TRUE	MAKE_BASE=TRUE	NC SATA D R2D CN
NC SATA D R2D CP	TRUE	MAKE_BASE=TRUE	NC SATA D R2D CP
NC SATA E D2RN	TRUE	MAKE_BASE=TRUE	NC SATA E D2RN
NC SATA E D2RP	TRUE	MAKE_BASE=TRUE	NC SATA E D2RP
NC SATA E R2D CN	TRUE	MAKE_BASE=TRUE	NC SATA E R2D CN
NC SATA E R2D CP	TRUE	MAKE_BASE=TRUE	NC SATA E R2D CP
NC SATA F D2RN	TRUE	MAKE_BASE=TRUE	NC SATA F D2RN
NC SATA F D2RP	TRUE	MAKE_BASE=TRUE	NC SATA F D2RP
NC SATA F R2D CN	TRUE	MAKE_BASE=TRUE	NC SATA F R2D CN
NC SATA F R2D CP	TRUE	MAKE_BASE=TRUE	NC SATA F R2D CP
TP SMC P41	TRUE	MAKE_BASE=TRUE	NC SMC P41

PCH ALIASES

NC LPC DREQ0 L		NC LPC DREQ0 L
NC CLINK CLK	TRUE	NC CLINK CLK
NC CLINK DATA	MAKE_BASE=TRUE	NC CLINK DATA
NC CLINK RESET L	TRUE	NC CLINK RESET L
NC PCIE CLK100M PEBN	MAKE_BASE=TRUE	NC PCIE CLK100M PEBN
NC PCIE CLK100M PEBP	TRUE	NC PCIE CLK100M PEBP
	MAKE_BASE=TRUE	

NC NO_TESTS

NO_TEST

TRUE	NC SMC FAN 3 TACH	44 45	
TRUE	NC SMC FAN 3 CTL	44 45	
TRUE	NC SMC FAN 2 TACH	44 45	
TRUE	NC SMC FAN 2 CTL	44 45	
TRUE	NC FW2 TPBP	38 40	
TRUE	NC FW2 TPBN	38 40	
TRUE	NC FW2 TPBIAS	38 40	
TRUE	NC FW2 TPAP	38 40	
TRUE	NC FW2 TPAN	38 40	
TRUE	NC FW0 TPBP	38 40 94	
TRUE	NC FW0 TPBN	38 40 94	
TRUE	NC FW0 TPAP	38 40 94	
TRUE	NC ESTARLDO EN		
TRUE	NC ALS GAIN		
TRUE	NC FW643 AVREG		NC FW643 AVREG
TRUE	NC FW643 TDI		NC FW643 TDI
TRUE	NC DP IG C HPD		NC DP IG C HPD
TRUE	NC DP IG C CTRL CLK		NC DP IG C CTRL CLK
TRUE	NC DP IG C CTRL DATA		NC DP IG C CTRL DATA
TRUE	TP DP IG C MLP<3..0>		NC DP IG C MLP<3..0>
TRUE	TP DP IG C MLN<3..0>		NC DP IG C MLN<3..0>
TRUE	NC DP IG C AUXP		NC DP IG C AUXP
TRUE	NC DP IG C AUXN		NC DP IG C AUXN
TRUE	NC DP IG D HPD		NC DP IG D HPD
TRUE	NC DP IG D CTRL CLK		NC DP IG D CTRL CLK
TRUE	NC DP IG D CTRL DATA		NC DP IG D CTRL DATA
TRUE	TP DP IG D MLP<3..0>		NC DP IG D MLP<3..0>
TRUE	TP DP IG D MLN<3..0>		NC DP IG D MLN<3..0>
TRUE	NC DP IG D AUXP		NC DP IG D AUXP
TRUE	NC DP IG D AUXN		NC DP IG D AUXN
TRUE	NC SDVO TVCLKINN		NC SDVO TVCLKINN
TRUE	NC SDVO TVCLKINP		NC SDVO TVCLKINP
TRUE	NC SDVO STALLN		NC SDVO STALLN
TRUE	NC SDVO STALLP		NC SDVO STALLP
TRUE	NC SDVO INTN		NC SDVO INTN
TRUE	NC SDVO INTP		NC SDVO INTP
TRUE	NC GPU BUFRST L		NC GPU BUFRST L
TRUE	TP GPU GSTATE<0>		NC GPU GSTATE<0>
TRUE	NC GPU GSTATE<1>		NC GPU GSTATE<1>
TRUE	TP GPU MIOA D<9..0>		NC GPU MIOA D<9..0>
TRUE	NC GPU MIOA DE		NC GPU MIOA DE
TRUE	NC LVDS EG BKL PWM		NC LVDS EG BKL PWM
TRUE	TP LVDS IG B CLKN		NC LVDS IG B CLKN
TRUE	TP LVDS IG B CLKP		NC LVDS IG B CLKP
TRUE	TP LVDS IG BKL PWM		NC LVDS IG BKL PWM
TRUE	NC SMC BS ALRT L		NC SMC BS ALRT L
TRUE	MEM A BA<2..0>	11 26 91	MEM B BA<2..0> 11 28 91
TRUE	MEM A CKE<1..0>	11 26 91	MEM B CKE<1..0> 11 28 91
TRUE	MEM A CLK N<1..0>	11 26	MEM B CLK N<1..0> 11 28
TRUE	MEM A CLK P<1..0>	91 11 26	MEM B CLK P<1..0> 11 28 91
TRUE	MEM A CS L<1..0>	11 26 91	MEM B CS L<1..0> 11 28 91
TRUE	MEM A ODT<1..0>	11 26 91	MEM B ODT<1..0> 11 28 91
TRUE	MEM A SA<1..0>	26	MEM B SA<1..0> 28
TRUE	MEM A DQ<63..0>	11 26 27 28 91	MEM B DQ<63..0> 11 27 28 91
TRUE	MEM A DQS N<7..0>	11 26 27 91	MEM B DQS N<7..0> 11 27 28 91
TRUE	MEM A DQS P<7..0>	11 26 27 91	MEM B DQS P<7..0> 11 27 28 91
TRUE	FB A0 DQ<31..0>	75 76 97	FB B0 DQ<31..0> 75 77 97
TRUE	FB A0 A<8..0>	75 76 97	FB B0 A<8..0> 75 77 97
TRUE	FB A0 ABI L	75 76 97	FB B0 ABI L 75 77 97
TRUE	FB A0 EDC<3..0>	75 76 97	FB B0 EDC<3..0> 75 77 97
TRUE	FB A0 WCLK N<1..0>	75 76 97	FB B0 WCLK N<1..0> 75 77 97
TRUE	FB A0 WCLK P<1..0>	75 76 97	FB B0 WCLK P<1..0> 75 77 97
TRUE	FB A0 DBI L<3..0>	75 76 97	FB B0 DBI L<3..0> 75 77 97
TRUE	FB A1 DQ<31..0>	75 76 97	FB B1 DQ<31..0> 75 77 97
TRUE	FB A1 A<8..0>	75 76 97	FB B1 A<8..0> 75 77 97
TRUE	FB A1 ABI L	75 76 97	FB B1 ABI L 75 77 97
TRUE	FB A1 EDC<3..0>	75 76 97	FB B1 EDC<3..0> 75 77 97
TRUE	FB A1 WCLK N<1..0>	75 76 97	FB B1 WCLK N<1..0> 75 77 97
TRUE	FB A1 WCLK P<1..0>	75 76 97	FB B1 WCLK P<1..0> 75 77 97
TRUE	FB A1 DBI L<3..0>	75 76 97	FB B1 DBI L<3..0> 75 77 97
TRUE	MEM A A<15..0>	11 26 91	MEM B A<15..0> 11 28 91
TRUE	MEM A CAS L	11 26 91	MEM B CAS L 11 28 91
TRUE	MEM A RAS L	11 26 91	MEM B RAS L 11 28 91
TRUE	MEM A WE L	11 26 91	MEM B WE L 11 28 91

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

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Functional / ICT Test

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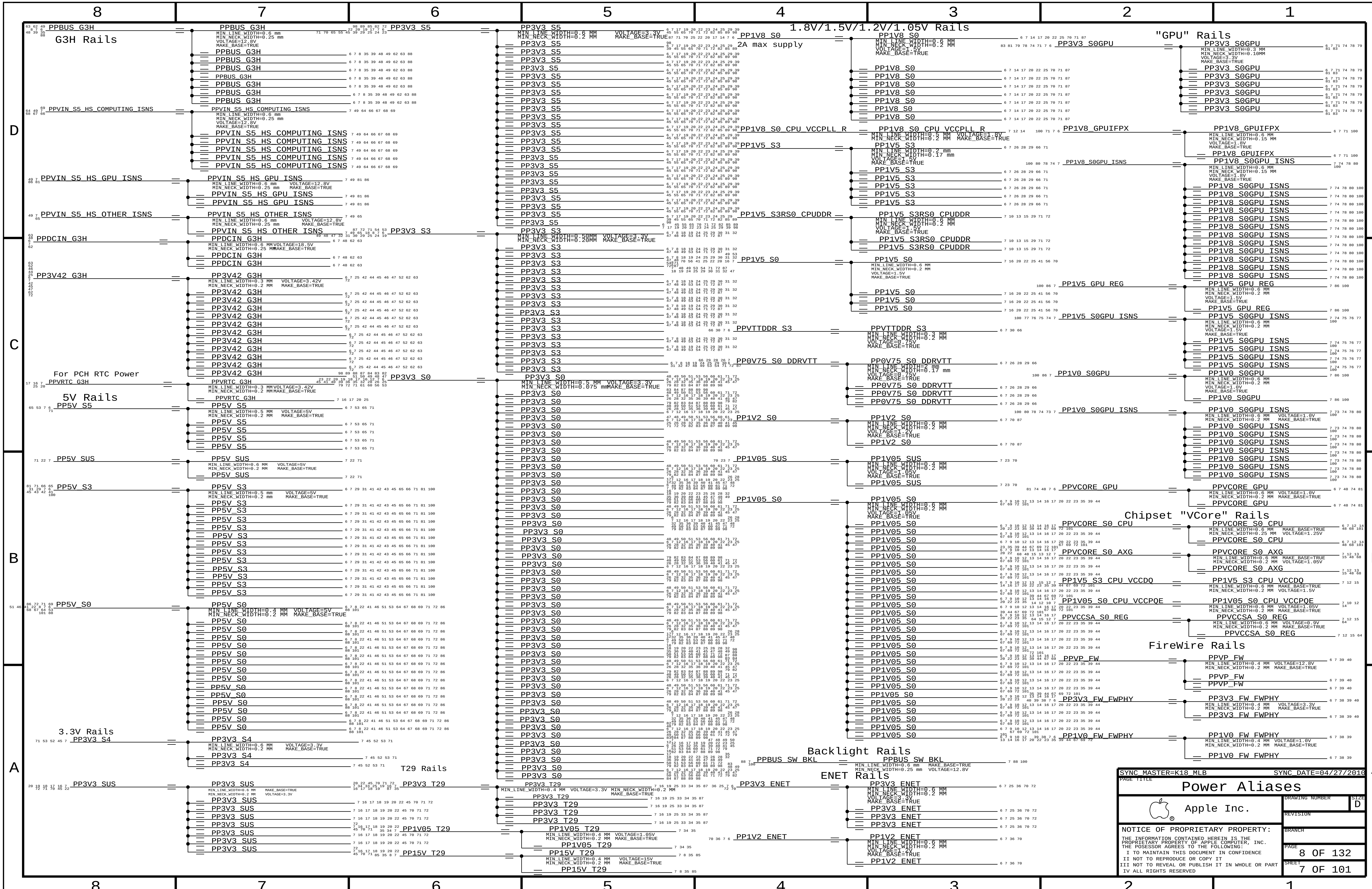

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

Power Aliases

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH

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Thermal Module Holes

ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0987 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0980 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0985 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0986 STDOFF-4.5OD.98H-1.1-3.48-TH

Fan Holes

ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0989 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0991 STDOFF-4.5OD.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 GND
ZT0940 3R2P5 GND
ZT0950 TH GND SL-3.1X2.7-6CIR-NSP
ZT0960 3R2P5 GND
ZT0990 3R2P5 GND

Left Speaker Holes

ZT0934 STDOFF-4.0OD3.0H-TH
ZT0935 STDOFF-4.0OD3.0H-TH

Keyboard / IPD Conn Protect

ZT0952 4.0OD1.85H-M1.6X0.35
ZT0953 4.0OD1.85H-M1.6X0.35

Tall EMI pogo pins

SH0902 POGO-2.0OD-3.5H-K86-K87
SH0903 POGO-2.0OD-3.5H-K86-K87
SH0904 POGO-2.0OD-3.5H-K86-K87
SH0900 POGO-2.0OD-3.5H-K86-K87
SH0916 POGO-2.0OD-3.5H-K86-K87

Short (IO Row) EMI pogo pins

SH0910 1.4DIA-SHORT-SILVER-K99
SH0912 1.4DIA-SHORT-SILVER-K99
SH0901 1.4DIA-SHORT-SILVER-K99
SH0914 1.4DIA-SHORT-SILVER-K99
SH0911 1.4DIA-SHORT-SILVER-K99
SH0913 1.4DIA-SHORT-SILVER-K99
SH0917 1.4DIA-SHORT-SILVER-K99
GND_CHASSIS_AUDIO_JACK

Heat spreader mounting boss for T29 router

SH0920 STDOFF-4.0OD1.85H-SM
SH0923 STDOFF-4.0OD1.85H-SM

Heat spreader mounting boss for PCH

SH0921 STDOFF-4.0OD2.23H-SM
SH0922 STDOFF-4.0OD2.23H-SM

R0921 51 5% 1/20W MF 201 — T29 A BIAS R — T29 A BIAS R2D P0 — C0901 0.01UF 10% 10V X5R 201
R0922 51 5% 1/20W MF 201 — T29 A BIAS R — T29 A BIAS R2D N0 — C0902 0.01UF 10% 10V X5R 201
R0923 51 5% 1/20W MF 201 — T29 A BIAS R — T29 A BIAS R2D P1 — C0903 0.01UF 10% 10V X5R 201
R0924 51 5% 1/20W MF 201 — T29 A BIAS R — T29 A BIAS R2D N1 — C0904 0.01UF 10% 10V X5R 201

T29 / GMUX JTAG Signals

JTAG_ISP_TCK — JTAG_ISP_TCK
JTAG_ISP_TDI — JTAG_ISP_TDI
JTAG_ISP_TDO — JTAG_ISP_TDO
T29_LSEO_LSOE3 — T29_LSEO_LSOE3 (MAKE_BASE=TRUE, NO_TEST=TRUE) — T29_LSEO_LSOE3
T29_LSEO_LSOE2 — T29_LSEO_LSOE2 (MAKE_BASE=TRUE, NO_TEST=TRUE) — T29_LSEO_LSOE2

GMUX ALIASES

PM_ALL_GPU_PGOOD — PM_ALL_GPU_PGOOD
TP_LVDS_MUX_SEL_EG — TP_LVDS_MUX_SEL_EG (NO_TEST=TRUE)
EG_RESET_L — EG_RESET_L
LVDS_IG_BKL_ON — LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR — LVDS_IG_PANEL_PWR
PPVOUT_S0_LCDBKLT — PPVOUT_S0_LCDBKLT
GMUX_VSYNC — GMUX_VSYNC
PEX_CLKREQ_L — PEX_CLKREQ_L
PEG_CLKREQ_L — PEG_CLKREQ_L
PM_ENET_EN — PM_ENET_EN

FW_PLUG_DET_L — FW_PLUG_DET_L
FW643_WAKE_L — FW643_WAKE_L
TP_SMC_EXCARD_PWR_EN — TP_SMC_EXCARD_PWR_EN
NC_PCIE_EXCARD_D2R_N — NC_PCIE_EXCARD_D2R_N
NC_PCIE_EXCARD_D2R_P — NC_PCIE_EXCARD_D2R_P
NC_PCIE_EXCARD_R2D_C_N — NC_PCIE_EXCARD_R2D_C_N
NC_PCIE_EXCARD_R2D_C_P — NC_PCIE_EXCARD_R2D_C_P
NC_PCIE_CLK100M_EXCARD_N — NC_PCIE_CLK100M_EXCARD_N
NC_PCIE_CLK100M_EXCARD_P — NC_PCIE_CLK100M_EXCARD_P
NC_PEG_B_CLKRQ_L_GPIO56 — NC_PEG_B_CLKRQ_L_GPIO56
NC_PCIECLKRQ4_L_GPIO26 — NC_PCIECLKRQ4_L_GPIO26
TP_ISSP_SCLK_P1_1 — TP_ISSP_SCLK_P1_1
TP_ISSP_SDATA_P1_0 — TP_ISSP_SDATA_P1_0

GND
GND
GND
GND
GND

NC_PCH_CLKOUT_DPN — NC_PCH_CLKOUT_DPN
NC_PCH_CLKOUT_DPP — NC_PCH_CLKOUT_DPP
NC_PCH_GPIO64_CLKOUTFLEX0 — NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1 — NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2 — NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3 — NC_PCH_GPIO67_CLKOUTFLEX3

NC_FSB_CLK133M_PCHP — NC_FSB_CLK133M_PCHP
NC_FSB_CLK133M_PCHN — NC_FSB_CLK133M_PCHN
NC_LT_GAIN_TP — NC_LT_GAIN_TP
NC_RT_GAIN_TP — NC_RT_GAIN_TP
NC_SW_GAIN_TP — NC_SW_GAIN_TP

PP5V_S0 — XW0901 — PP5V_S0_AUDIO — XW0902 — PP5V_S0_AUDIO_AMP_L — XW0903 — PP5V_S0_AUDIO_AMP_R

CPU signals

CPU_VID<0..6> — CPUIMVP_VID<0..6>
GFX_VID<0..6> — GFXIMVP_VID<0..6>
MEMVTT_EN — MEMVTT_EN

Unused PEG signals

NC_PEG_D2R_P<15..12> — =PEG_D2R_P<15..12>
NC_PEG_D2R_N<15..12> — =PEG_D2R_N<15..12>
NC_PEG_R2D_C_P<15..12> — =PEG_R2D_C_P<15..12>
NC_PEG_R2D_C_N<15..12> — =PEG_R2D_C_N<15..12>

T29 Signals Through PEG

PCIE_T29_D2R_P<3..0> — =PEG_D2R_P<11..8>
PCIE_T29_D2R_N<3..0> — =PEG_D2R_N<11..8>
PCIE_T29_R2D_C_P<3..0> — =PEG_R2D_C_P<11..8>
PCIE_T29_R2D_C_N<3..0> — =PEG_R2D_C_N<11..8>

GPU signals

PEG_D2R_P<7..0> — =PEG_D2R_P<7..0>
PEG_D2R_N<7..0> — =PEG_D2R_N<7..0>
PEG_R2D_C_P<7..0> — =PEG_R2D_C_P<7..0>
PEG_R2D_C_N<7..0> — =PEG_R2D_C_N<7..0>

Unused T29 Ports

T29_D2R_P<3..2> — NC_T29_D2RP<3..2>
T29_D2R_N<3..2> — NC_T29_D2RN<3..2>
T29_R2D_C_P<3..2> — NC_T29_R2D_CP<3..2>
T29_R2D_C_N<3..2> — NC_T29_R2D_CN<3..2>

DP_EG_AUXCH_N — DP_EG_AUXCH_N
DP_EG_AUXCH_P — DP_EG_AUXCH_P
NC_DPB_EG_AUX_CHN — NC_DPB_EG_AUX_CHN
NC_DPB_EG_AUX_CHP — NC_DPB_EG_AUX_CHP
NC_DPB_EG_DDC_CLK — NC_DPB_EG_DDC_CLK
NC_DPB_EG_DDC_DATA — NC_DPB_EG_DDC_DATA
NC_DPB_EG_MLN<3..0> — DPB_EG_ML_N<3..0>
NC_DPB_EG_MLP<3..0> — DPB_EG_ML_P<3..0>

LCD_BKLT_EN
R0901 4.7K 5% 1/16W MF-LF 402

T29BST:N — R0950 0 5% 1/8W MF-LF 805 — PPBUS_G3H — PP15V_T29

TP_CPU_VTT_SELECT — TP_CPU_VTT_SELECT

TP_LVDS_IG_B_CLKP — TP_LVDS_IG_B_CLKP
TP_LVDS_IG_B_CLKN — TP_LVDS_IG_B_CLKN
TP_LVDS_IG_BKL_PWM — TP_LVDS_IG_BKL_PWM
NC_GPU_XTALOUT — NC_GPU_XTALOUT
NC_LVDS_IG_A_DATAP<3> — NC_LVDS_IG_A_DATAP<3>
NC_LVDS_IG_A_DATAN<3> — NC_LVDS_IG_A_DATAN<3>
NC_LVDS_IG_B_DATAP<3> — NC_LVDS_IG_B_DATAP<3>
NC_LVDS_IG_B_DATAN<3> — NC_LVDS_IG_B_DATAN<3>

NC_USB_HUB1_OCS4 — NC_USB_HUB1_OCS4
NC_USB_HUB2_OCS4 — NC_USB_HUB2_OCS4

PP3V3_S3
NOSTUFF R0903 10K 5% 1/16W MF-LF 402 — R0904 10K 5% 1/16W MF-LF 402
USB_EXTC_N
USB_EXTC_P

PP3V3_S3
NOSTUFF R0913 10K 5% 1/16W MF-LF 402 — R0914 10K 5% 1/16W MF-LF 402
USB_SDCARD_P — USB_SDCARD_P
USB_SDCARD_N — USB_SDCARD_N

PP3V3_S3
R0915 10K 5% 1/16W MF-LF 402 — R0916 10K 5% 1/16W MF-LF 402
USB_T29A_N
USB_T29A_P

DP_A_BIAS2
DP_A_BIAS0
C0905 0.01UF 10% 10V X5R 201 — C0908 0.01UF 10% 10V X5R 201
GND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.095 mm
VOLTAGE=0V

DP_IG_MLP<3..0> — TP_DP_IG_B_MLP<3..0>
DP_IG_MLN<3..0> — TP_DP_IG_B_MLN<3..0>
DP_IG_AUX_CH_P — DP_IG_AUX_CH_P
DP_IG_AUX_CH_N — DP_IG_AUX_CH_N
DP_IG_DDC_CLK — DP_IG_DDC_CLK
DP_IG_DDC_DATA — DP_IG_DDC_DATA
DP_IG_HPD — DP_IG_HPD

Digital Ground

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010
PAGE TITLE: Signal Aliases
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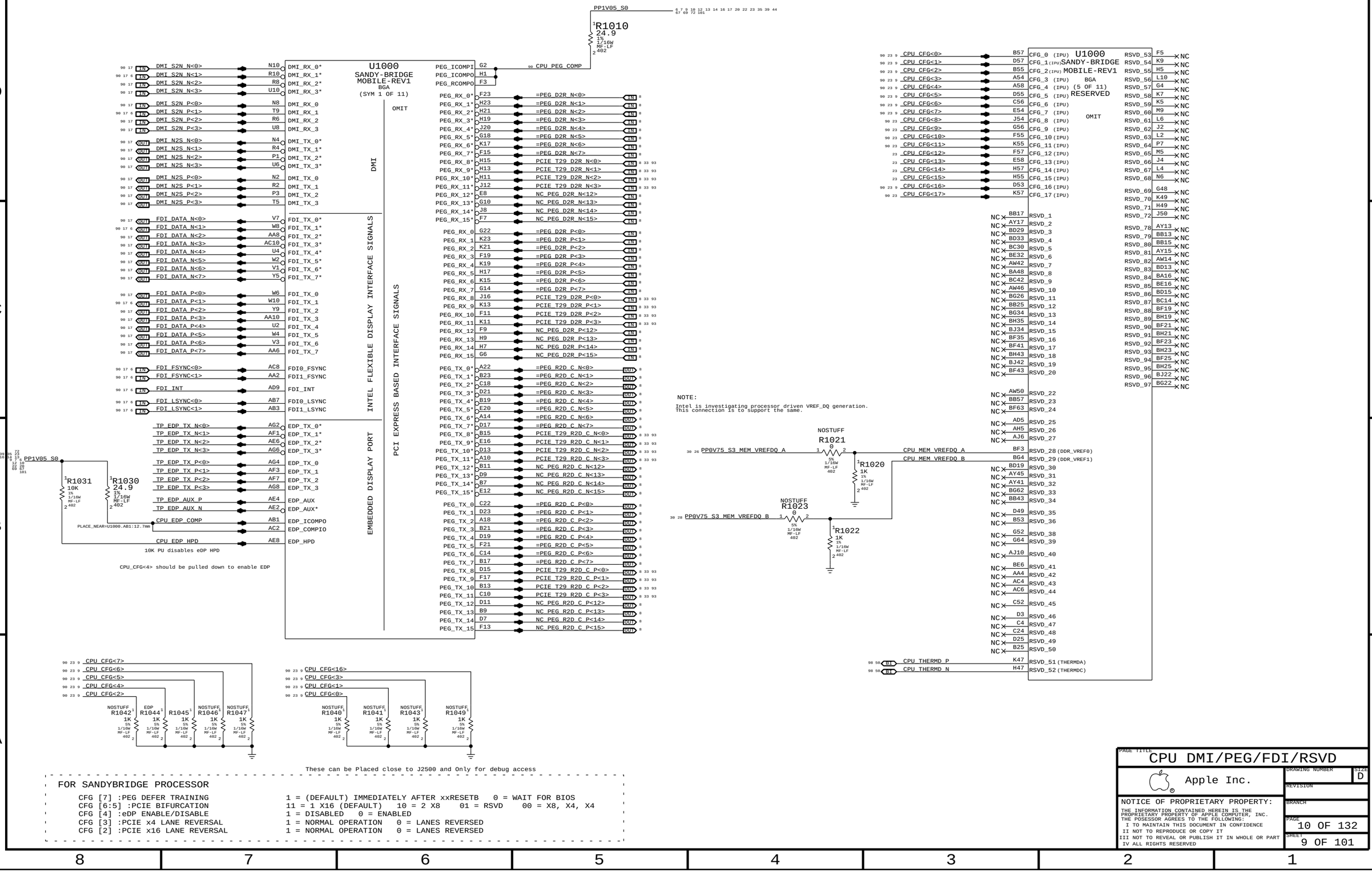
PP1V05_S0
R1010 24.9 1% 1/16W MF-LF 402
U1000
SANDY-BRIDGE
MOBILE-REV1
BGA
(SYM 1 OF 11)
OMIT
DMI
INTEL FLEXIBLE DISPLAY INTERFACE SIGNALS
PCI EXPRESS BASED INTERFACE SIGNALS
EMBEDDED DISPLAY PORT
DMI_S2N_N<0>
DMI_S2N_N<1>
DMI_S2N_N<2>
DMI_S2N_N<3>
DMI_S2N_P<0>
DMI_S2N_P<1>
DMI_S2N_P<2>
DMI_S2N_P<3>
DMI_N2S_N<0>
DMI_N2S_N<1>
DMI_N2S_N<2>
DMI_N2S_N<3>
DMI_N2S_P<0>
DMI_N2S_P<1>
DMI_N2S_P<2>
DMI_N2S_P<3>
FDI_DATA_N<0>
FDI_DATA_N<1>
FDI_DATA_N<2>
FDI_DATA_N<3>
FDI_DATA_N<4>
FDI_DATA_N<5>
FDI_DATA_N<6>
FDI_DATA_N<7>
FDI_DATA_P<0>
FDI_DATA_P<1>
FDI_DATA_P<2>
FDI_DATA_P<3>
FDI_DATA_P<4>
FDI_DATA_P<5>
FDI_DATA_P<6>
FDI_DATA_P<7>
FDI_FSYNC<0>
FDI_FSYNC<1>
FDI_INT
FDI_LSYNC<0>
FDI_LSYNC<1>
TP_EDP_TX_N<0>
TP_EDP_TX_N<1>
TP_EDP_TX_N<2>
TP_EDP_TX_N<3>
TP_EDP_TX_P<0>
TP_EDP_TX_P<1>
TP_EDP_TX_P<2>
TP_EDP_TX_P<3>
TP_EDP_AUX_P
TP_EDP_AUX_N
CPU_EDP_COMP
CPU_EDP_HPD
PLACE_NEAR=U1000.AB1:12.7mm
10K PU disables eDP HPD
CPU_CFG<4> should be pulled down to enable EDP
R1031 10K 1% 1/16W MF-LF 402
R1030 24.9 1% 1/16W MF-LF 402
PEG_ICOMPI
PEG_ICOMPO
PEG_RCOMPO
CPU_PEG_COMP
PEG_RX_0*
PEG_RX_1*
PEG_RX_2*
PEG_RX_3*
PEG_RX_4*
PEG_RX_5*
PEG_RX_6*
PEG_RX_7*
PEG_RX_8*
PEG_RX_9*
PEG_RX_10*
PEG_RX_11*
PEG_RX_12*
PEG_RX_13*
PEG_RX_14*
PEG_RX_15*
PEG_RX_0
PEG_RX_1
PEG_RX_2
PEG_RX_3
PEG_RX_4
PEG_RX_5
PEG_RX_6
PEG_RX_7
PEG_RX_8
PEG_RX_9
PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15
PEG_TX_0*
PEG_TX_1*
PEG_TX_2*
PEG_TX_3*
PEG_TX_4*
PEG_TX_5*
PEG_TX_6*
PEG_TX_7*
PEG_TX_8*
PEG_TX_9*
PEG_TX_10*
PEG_TX_11*
PEG_TX_12*
PEG_TX_13*
PEG_TX_14*
PEG_TX_15*
PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15
NOTE:
Intel is investigating processor driven VREF_DQ generation.
This connection is to support the same.
NOSTUFF R1021 0 5% 1/16W MF-LF 402
R1020 1K 1% 1/16W MF-LF 402
NOSTUFF R1023 0 5% 1/16W MF-LF 402
R1022 1K 1% 1/16W MF-LF 402
PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFDQ_B
CPU_MEM_VREFDQ_A
CPU_MEM_VREFDQ_B
U1000
SANDY-BRIDGE
MOBILE-REV1
BGA
(5 OF 11)
RESERVED
OMIT
CPU_CFG<0>
CPU_CFG<1>
CPU_CFG<2>
CPU_CFG<3>
CPU_CFG<4>
CPU_CFG<5>
CPU_CFG<6>
CPU_CFG<7>
CPU_CFG<8>
CPU_CFG<9>
CPU_CFG<10>
CPU_CFG<11>
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>
CPU_CFG<16>
CPU_CFG<17>
CPU_THERMD_P
CPU_THERMD_N
NOSTUFF R1042 1K 5% 1/16W MF-LF 402
EDP R1044 1K 5% 1/16W MF-LF 402
R1045 1K 5% 1/16W MF-LF 402
NOSTUFF R1046 1K 5% 1/16W MF-LF 402
NOSTUFF R1047 1K 5% 1/16W MF-LF 402
NOSTUFF R1040 1K 5% 1/16W MF-LF 402
NOSTUFF R1041 1K 5% 1/16W MF-LF 402
NOSTUFF R1043 1K 5% 1/16W MF-LF 402
NOSTUFF R1049 1K 5% 1/16W MF-LF 402
These can be Placed close to J2500 and Only for debug access
FOR SANDYBRIDGE PROCESSOR
CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
PAGE TITLE
CPU DMI/PEG/FDI/RSVD
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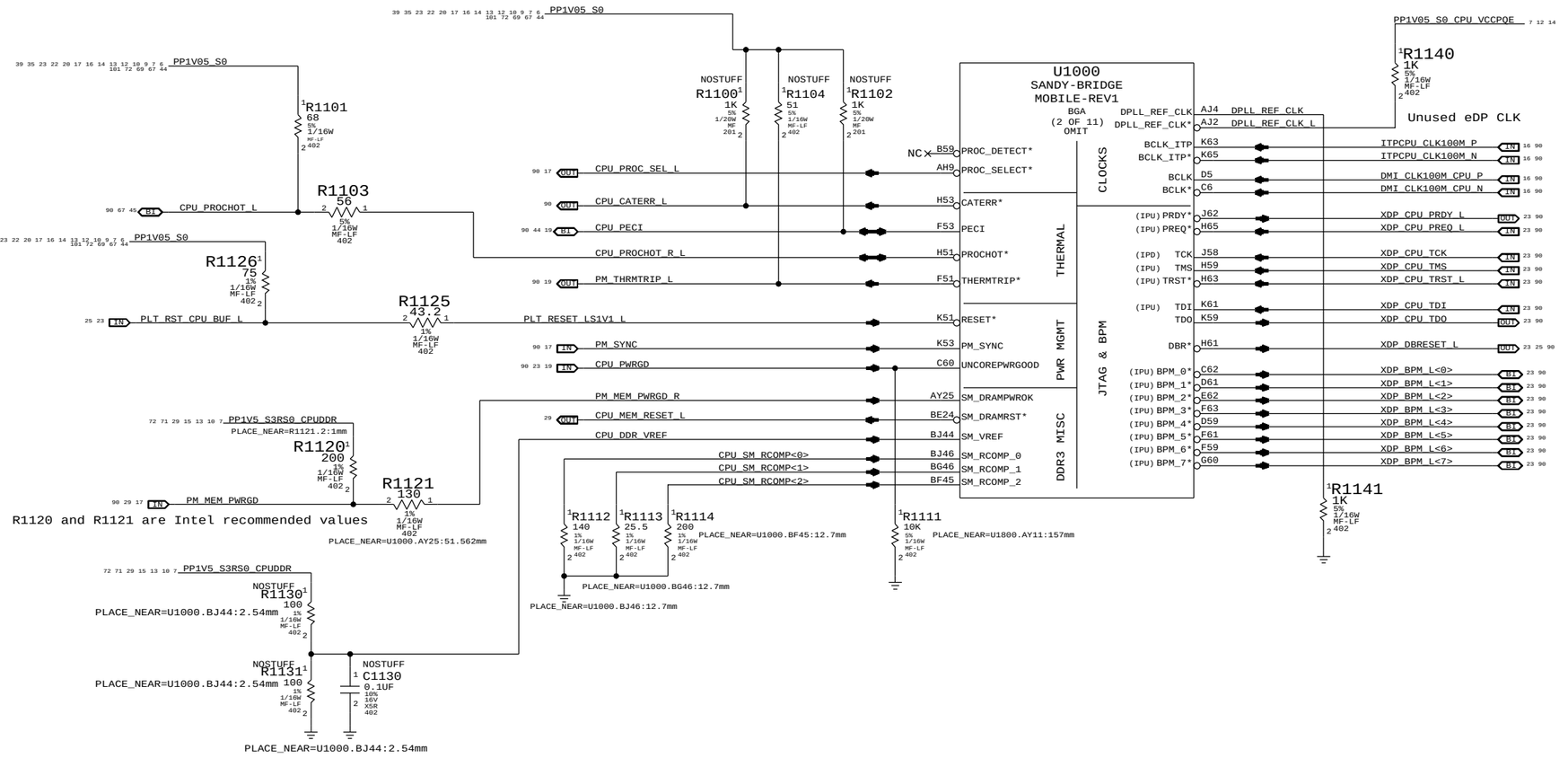

PAGE TITLE
CPU CLOCK/MISC/JTAG

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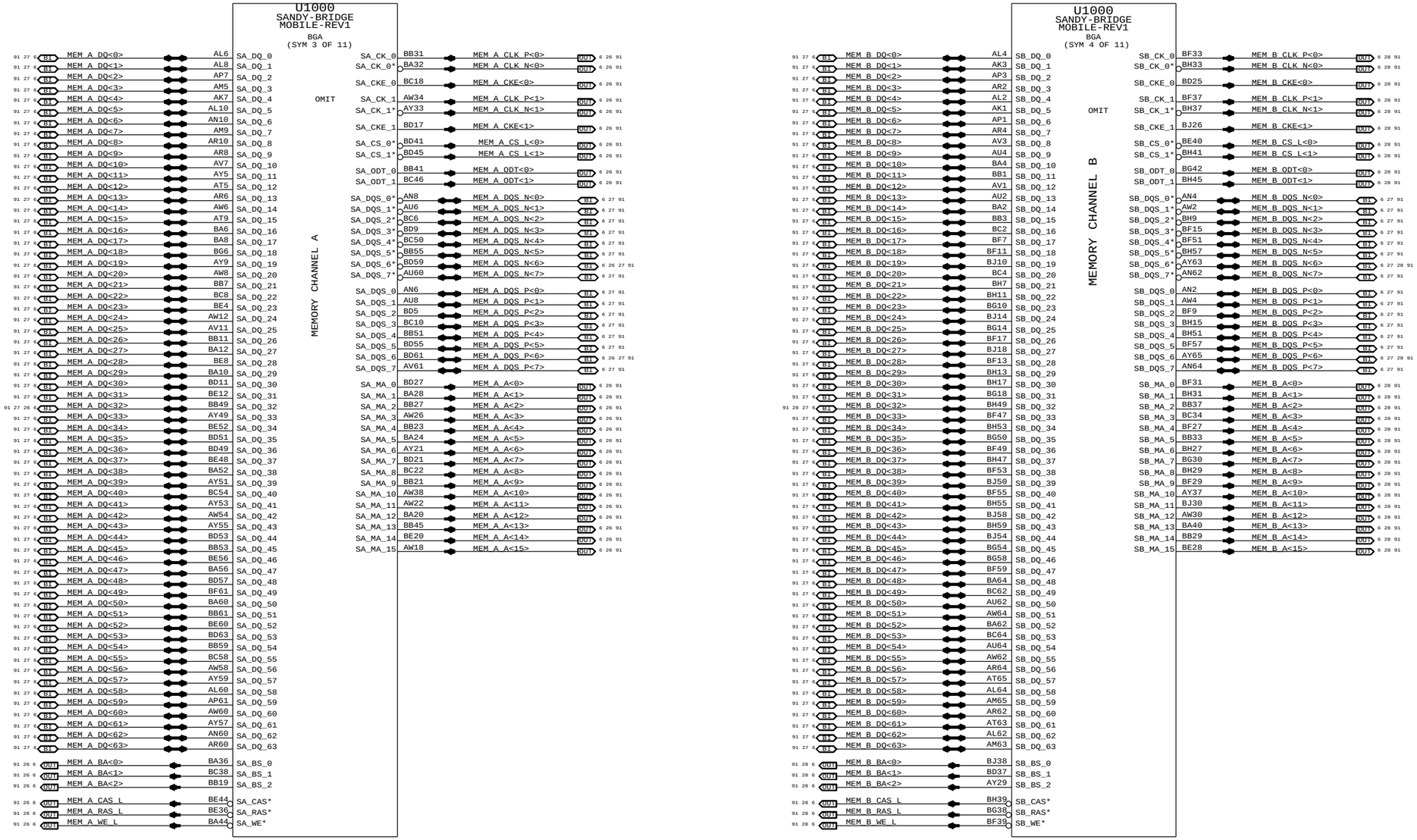
U1000
SANDY-BRIDGE
MOBILE-REV1
BGA
(SYM 3 OF 11)
MEMORY CHANNEL A
OMIT
SA_DQ_0 AL6
SA_DQ_1 AL8
SA_DQ_2 AP7
SA_DQ_3 AM5
SA_DQ_4 AK7
SA_DQ_5 AL10
SA_DQ_6 AN10
SA_DQ_7 AM9
SA_DQ_8 AR10
SA_DQ_9 AR8
SA_DQ_10 AV7
SA_DQ_11 AY5
SA_DQ_12 AT5
SA_DQ_13 AR6
SA_DQ_14 AW6
SA_DQ_15 AT9
SA_DQ_16 BA6
SA_DQ_17 BA8
SA_DQ_18 BG6
SA_DQ_19 AY9
SA_DQ_20 AW8
SA_DQ_21 BB7
SA_DQ_22 BC8
SA_DQ_23 BE4
SA_DQ_24 AW12
SA_DQ_25 AV11
SA_DQ_26 BB11
SA_DQ_27 BA12
SA_DQ_28 BE8
SA_DQ_29 BA10
SA_DQ_30 BD11
SA_DQ_31 BE12
SA_DQ_32 BB49
SA_DQ_33 AY49
SA_DQ_34 BE52
SA_DQ_35 BD51
SA_DQ_36 BD49
SA_DQ_37 BE48
SA_DQ_38 BA52
SA_DQ_39 AY51
SA_DQ_40 BC54
SA_DQ_41 AY53
SA_DQ_42 AW54
SA_DQ_43 AY55
SA_DQ_44 BD53
SA_DQ_45 BB53
SA_DQ_46 BE56
SA_DQ_47 BA56
SA_DQ_48 BD57
SA_DQ_49 BF61
SA_DQ_50 BA60
SA_DQ_51 BB61
SA_DQ_52 BE60
SA_DQ_53 BD63
SA_DQ_54 BB59
SA_DQ_55 BC58
SA_DQ_56 AW58
SA_DQ_57 AY59
SA_DQ_58 AL60
SA_DQ_59 AP61
SA_DQ_60 AW60
SA_DQ_61 AY57
SA_DQ_62 AN60
SA_DQ_63 AR60
SA_BS_0 BA36
SA_BS_1 BC38
SA_BS_2 BB19
SA_CAS* BE44
SA_RAS* BE36
SA_WE* BA44
SA_CK_0 BB31
SA_CK_0* BA32
SA_CKE_0 BC18
SA_CK_1 AW34
SA_CK_1* AY33
SA_CKE_1 BD17
SA_CS_0* BD41
SA_CS_1* BD45
SA_ODT_0 BB41
SA_ODT_1 BC46
SA_DQS_0* AN8
SA_DQS_1* AU6
SA_DQS_2* BC6
SA_DQS_3* BD9
SA_DQS_4* BC50
SA_DQS_5* BB55
SA_DQS_6* BD59
SA_DQS_7* AU60
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SA_DQS_1 AU8
SA_DQS_2 BD5
SA_DQS_3 BC10
SA_DQS_4 BB51
SA_DQS_5 BD55
SA_DQS_6 BD61
SA_DQS_7 AV61
SA_MA_0 BD27
SA_MA_1 BA28
SA_MA_2 BB27
SA_MA_3 AW26
SA_MA_4 BB23
SA_MA_5 BA24
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SA_MA_7 BD21
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SANDY-BRIDGE
MOBILE-REV1
BGA
(SYM 4 OF 11)
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SB_DQ_2 AP3
SB_DQ_3 AR2
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SB_CKE_1 BJ26
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SB_CS_1* BH41
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SB_ODT_1 BH45
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SB_DQS_1* AW2
SB_DQS_2* BH9
SB_DQS_3* BF15
SB_DQS_4* BF51
SB_DQS_5* BH57
SB_DQS_6* AY63
SB_DQS_7* AN62
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SB_DQS_1 AW4
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SB_DQS_4 BH51
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CPU DDR3 INTERFACES
Apple Inc.
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SIZE
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REVISION
BRANCH
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11 OF 101
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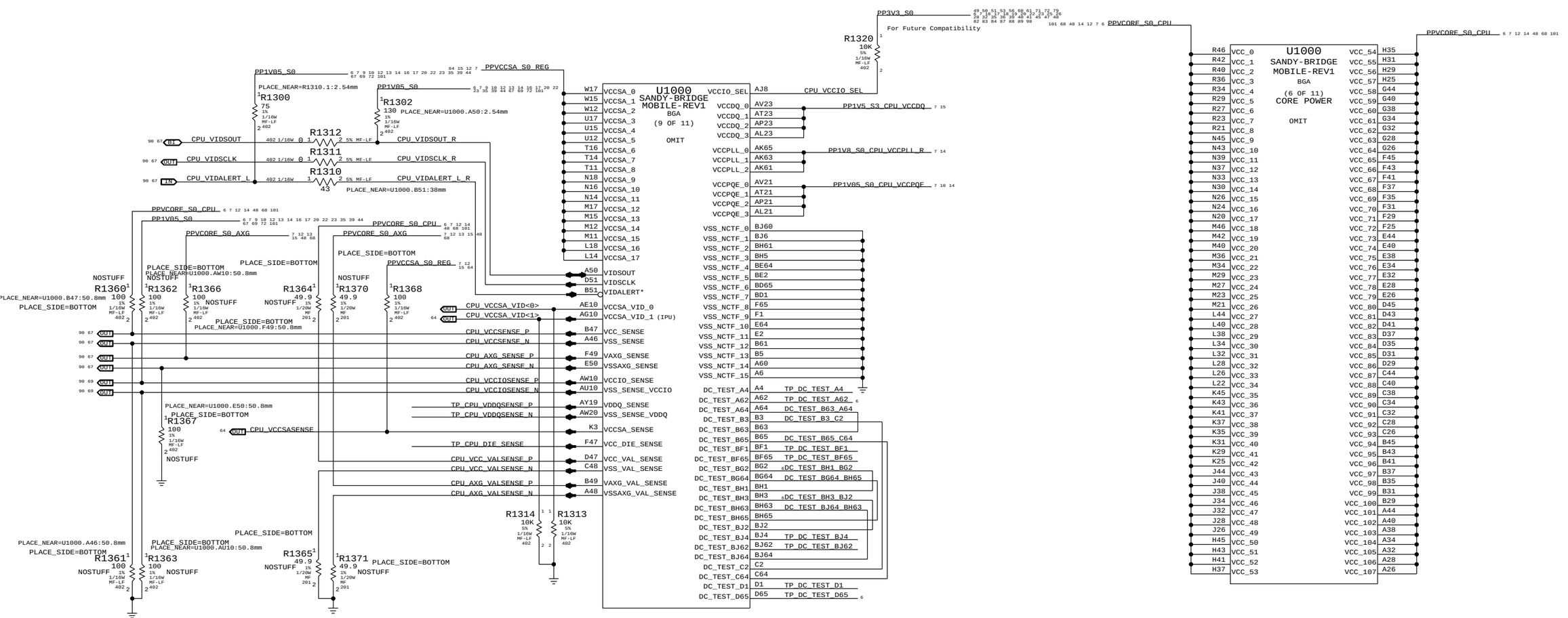

PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.
NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

SYNC_MASTER=K92_MLB SYNC_DATE=08/03/2010

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REVISION:

BRANCH:

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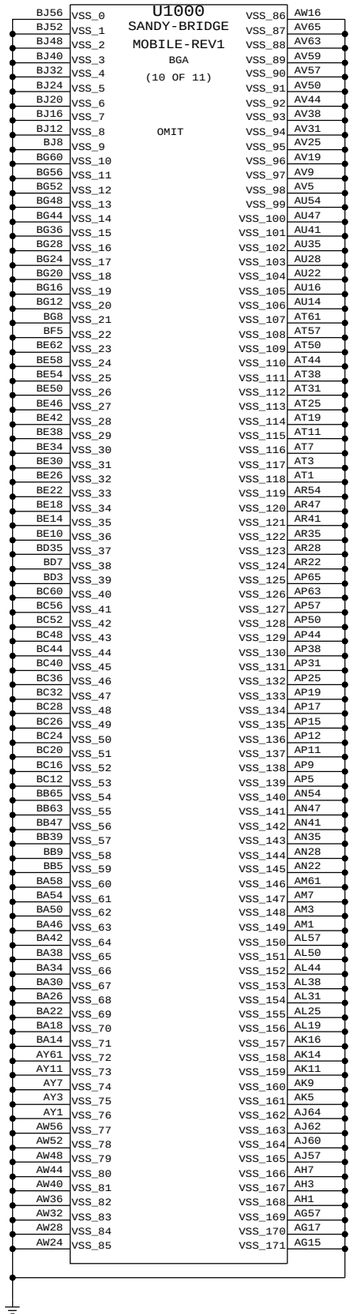

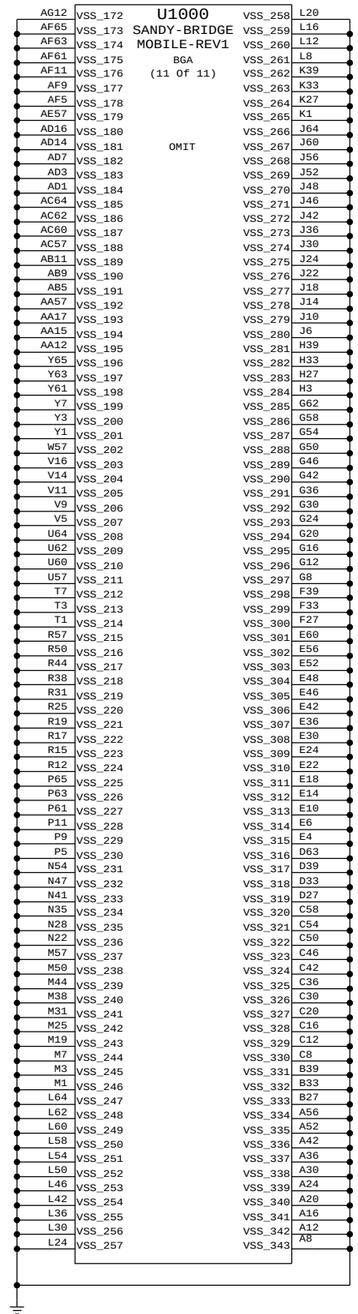

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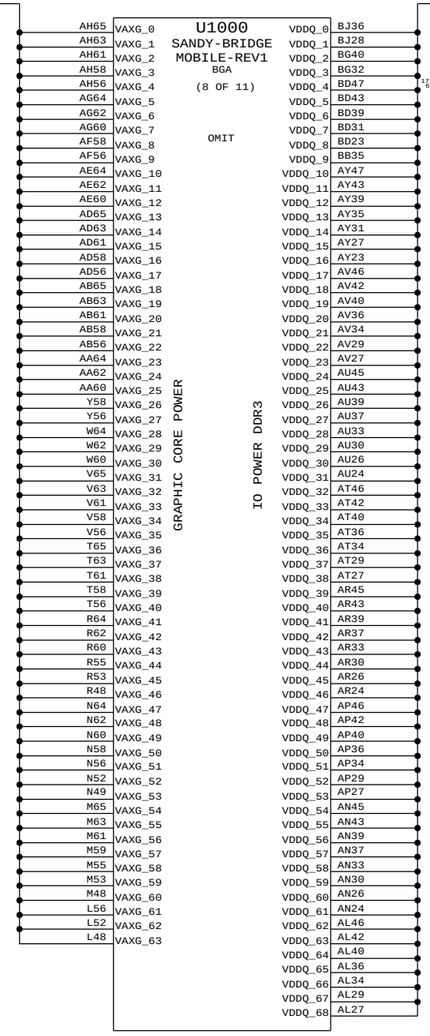
68 48 15 12 7



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PP1V05_S0
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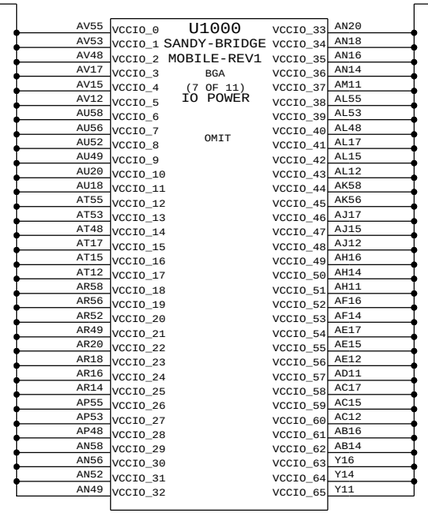
69 67 44 39 35 23 22 20



PP1V05_S0
67 69 72 103
17 20 22 23 33 38 39 44

PP1V05_S0
68 70 71 104
17 20 22 23 33 38 39 44

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CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

101 68 48 12 7 6 PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 20% 10V X5R 402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 6.3V X5R 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 6.3V X5R 0201

PLACEMENT_NOTE (C1620-C1623):
Place near U1000 on bottom side

CRITICAL C1620 C1621 C1622 C1623
10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side.

CRITICAL C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
22UF 20% 6.3V X5M CERM1 0603

NOSTUFF C16D0 C16D1 C16D2 C16D3 C16D4 C16D5
22UF 20% 6.3V X5M CERM1 0603

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

CRITICAL C1640 C1641 C1642 C1643
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

NOSTUFF C1644
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

39 35 23 16 15 14 9 5 PP1V05_S0

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
1UF 20% 10V X5R 402

C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 20% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

CRITICAL C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 6.3V X5R 603

Place near inductors on bottom side

CRITICAL C1682 C1683
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601
0.010
1% 1/4W MF 0603

PP1V05_S0_CPU_VCCPQE 7 10 12

C1684
1UF 10% 16V X5R 402

87 71 70 25 22 20 17 7 6 PP1V8_S0

CPU VCCPLL DECOUPLING

R1600
0
5% 1/16W MF-LF 402

PP1V8_S0_CPU_VCCPLL_R 7 12

PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA

C1685 C1686
1UF 10% 16V X5R 402

CRITICAL C1687
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA
PLACE_NEAR=U1000.AK61:5 mm

CPU VCCPLL Low pass filter

SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2010

PAGE TITLE
CPU DECOUPLING-I

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VAXG DECOUPLING

Intel recommendation: 2x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

68 48 13 12 7 PPVCORE_S0_AXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 1UF 10% 10V X5R 402
C1701 1UF 10% 10V X5R 402
C1702 1UF 10% 10V X5R 402
C1703 1UF 10% 10V X5R 402
C1704 1UF 10% 10V X5R 402
C1705 1UF 10% 10V X5R 402
C1706 1UF 10% 10V X5R 402
C1707 1UF 10% 10V X5R 402
C1708 1UF 10% 10V X5R 402
NOSTUFF C1709 1UF 10% 10V X5R 402
NOSTUFF C1710 1UF 10% 10V X5R 402
NOSTUFF C1711 1UF 10% 10V X5R 402
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NOSTUFF C1714 1UF 10% 10V X5R 402
NOSTUFF C1715 1UF 10% 10V X5R 402
NOSTUFF C1716 1UF 10% 10V X5R 402
NOSTUFF C1717 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 10UF 20% 6.3V CERM-X5R 0402-1
C1719 10UF 20% 6.3V CERM-X5R 0402-1
C1720 10UF 20% 6.3V CERM-X5R 0402-1
C1721 10UF 20% 6.3V CERM-X5R 0402-1
C1722 10UF 20% 6.3V CERM-X5R 0402-1
C1723 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1724 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1725 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 22UF 20% 6.3V X5R-CERM1 0603
C1727 22UF 20% 6.3V X5R-CERM1 0603
C1728 22UF 20% 6.3V X5R-CERM1 0603
C1729 22UF 20% 6.3V X5R-CERM1 0603
C1730 22UF 20% 6.3V X5R-CERM1 0603
C1731 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1732 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1733 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1734-C1735):
Place near inductors on bottom side.

C1734 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
C1735 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
NOSTUFF C1737 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

PLACEMENT_NOTE (C1738-C1747):

72 71 29 13 10 7 PP1V5_S3RS0_CPUDDR

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V X5R 603
C1749 10UF 20% 6.3V X5R 603
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V X5R 603
C1752 10UF 20% 6.3V X5R 603
C1753 10UF 20% 6.3V X5R 603
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V X5R 603

Place near inductors on bottom side

C1756 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700 0.010 1% 1/4W MF 0603

PP1V5_S3_CPU_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

PLACEMENT_NOTE (C1758-C1762):

64 12 7 PPVCCSA_S0_REG

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V X5R 603
C1764 10UF 20% 6.3V X5R 603
C1765 10UF 20% 6.3V X5R 603
C1766 10UF 20% 6.3V X5R 603
C1767 10UF 20% 6.3V X5R 603

C1768 270UF 20% 2V TANT CASE-B4-SM

SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2010

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

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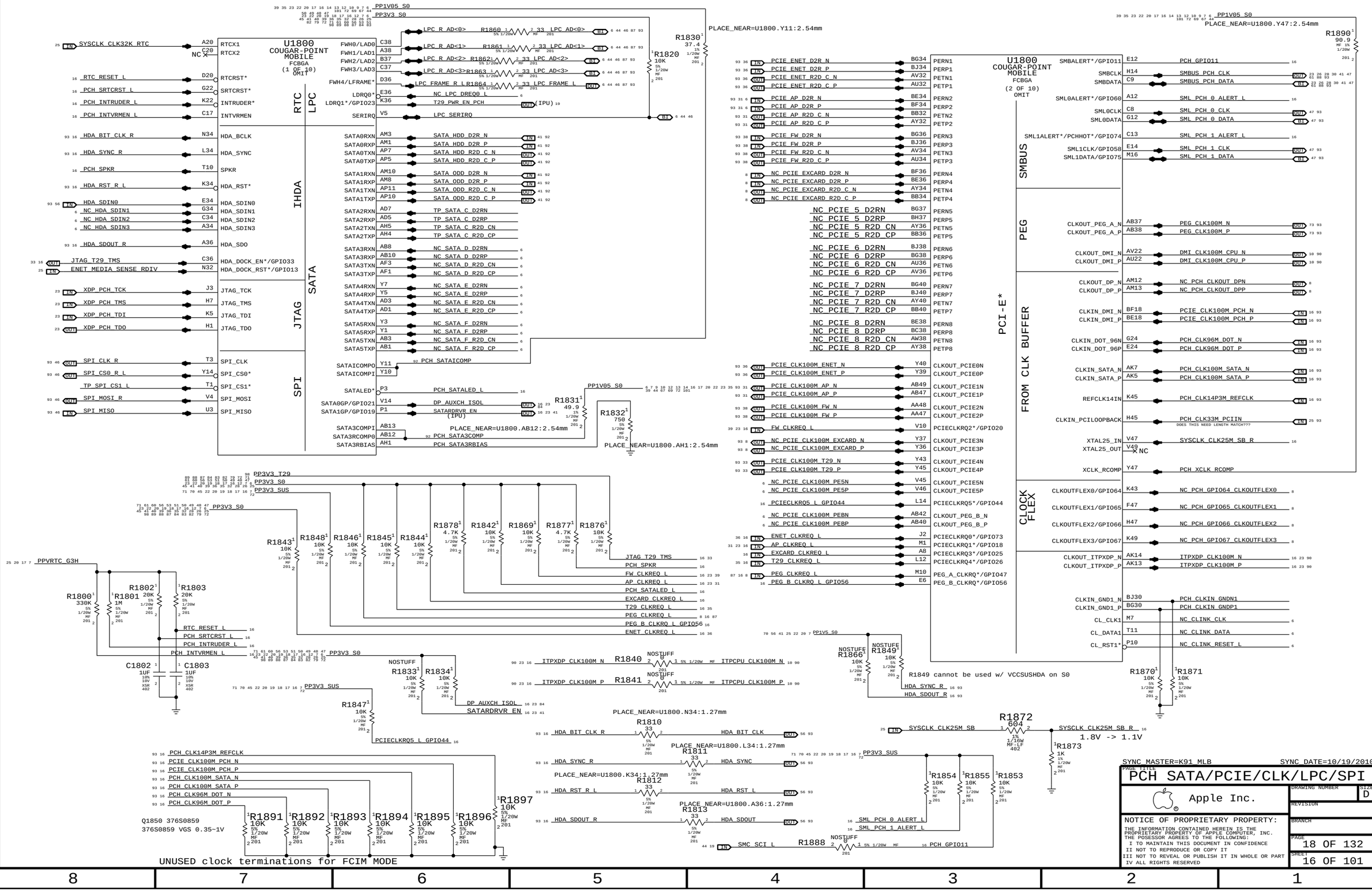
U1800
COUGAR-POINT MOBILE
FCBGA
(1 OF 10)
OMIT
RTC
LPC
IHDA
SATA
JTAG
SPI
SMBUS
PEG
FROM CLK BUFFER
PCI-E*
CLOCK FLEX
SYSCLK_CLK32K_RTC
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
HDA_BIT_CLK_R
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
NC_HDA_SDIN1
NC_HDA_SDIN2
NC_HDA_SDIN3
HDA_SDOUT_R
JTAG_T29_TMS
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO
LPC_R_AD<0>
LPC_R_AD<1>
LPC_R_AD<2>
LPC_R_AD<3>
LPC_FRAME_R_L
LDRQ0*
LDRQ1*/GPIO23
SERIRQ
T29_PWR_EN_PCH
LPC_SERIRQ
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATALED*
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA3COMPI
SATA3RCOMP0
SATA3RBIAS
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA_ODD_D2R_N
SATA_ODD_D2R_P
SATA_ODD_R2D_C_N
SATA_ODD_R2D_C_P
TP_SATA_C_D2RN
TP_SATA_C_D2RP
TP_SATA_C_R2D_CN
TP_SATA_C_R2D_CP
NC_SATA_D_D2RN
NC_SATA_D_D2RP
NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP
NC_SATA_E_D2RN
NC_SATA_E_D2RP
NC_SATA_E_R2D_CN
NC_SATA_E_R2D_CP
NC_SATA_F_D2RN
NC_SATA_F_D2RP
NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP
PCH_SATAICOMP
PCH_SATALED_L
DP_AUXCH_ISOL
SATARDRVR_EN
(IPU)
PCH_SATA3COMP
PCH_SATA3RBIAS
PLACE_NEAR=U1800.AB12:2.54mm
PLACE_NEAR=U1800.AH1:2.54mm
PLACE_NEAR=U1800.Y11:2.54mm
PLACE_NEAR=U1800.Y47:2.54mm
PLACE_NEAR=U1800.N34:1.27mm
PLACE_NEAR=U1800.L34:1.27mm
PLACE_NEAR=U1800.K34:1.27mm
PLACE_NEAR=U1800.A36:1.27mm
R1830 37.4
R1820 10K
R1890 90.9
R1831 49.9
R1832 750
PP1V05_S0
PP3V3_S0
PP3V3_SUS
PP3V3_T29
PPVRTC_G3H
R1800 330K
R1801 1M
R1802 20K
R1803 20K
C1802 1UF
C1803 1UF
R1843 10K
R1848 10K
R1846 10K
R1845 10K
R1844 10K
R1878 4.7K
R1842 10K
R1869 10K
R1877 4.7K
R1876 10K
R1840 0
R1841 0
R1833 10K
R1834 10K
R1847 10K
R1810 33
R1811 33
R1812 33
R1813 33
R1891 10K
R1892 10K
R1893 10K
R1894 10K
R1895 10K
R1896 10K
R1897 10K
R1866 10K
R1849 10K
R1888 0
R1854 10K
R1855 10K
R1853 10K
R1872 604
R1873 1K
R1870 10K
R1871 10K
NOSTUFF
R1849 cannot be used w/ VCCSUSHDA on S0
Q1850 376S0859
376S0859 VGS 0.35~1V
UNUSED clock terminations for FCIM MODE
1.8V -> 1.1V
SYNC_MASTER=K91_MLB
SYNC_DATE=10/19/2010
PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI
Apple Inc.
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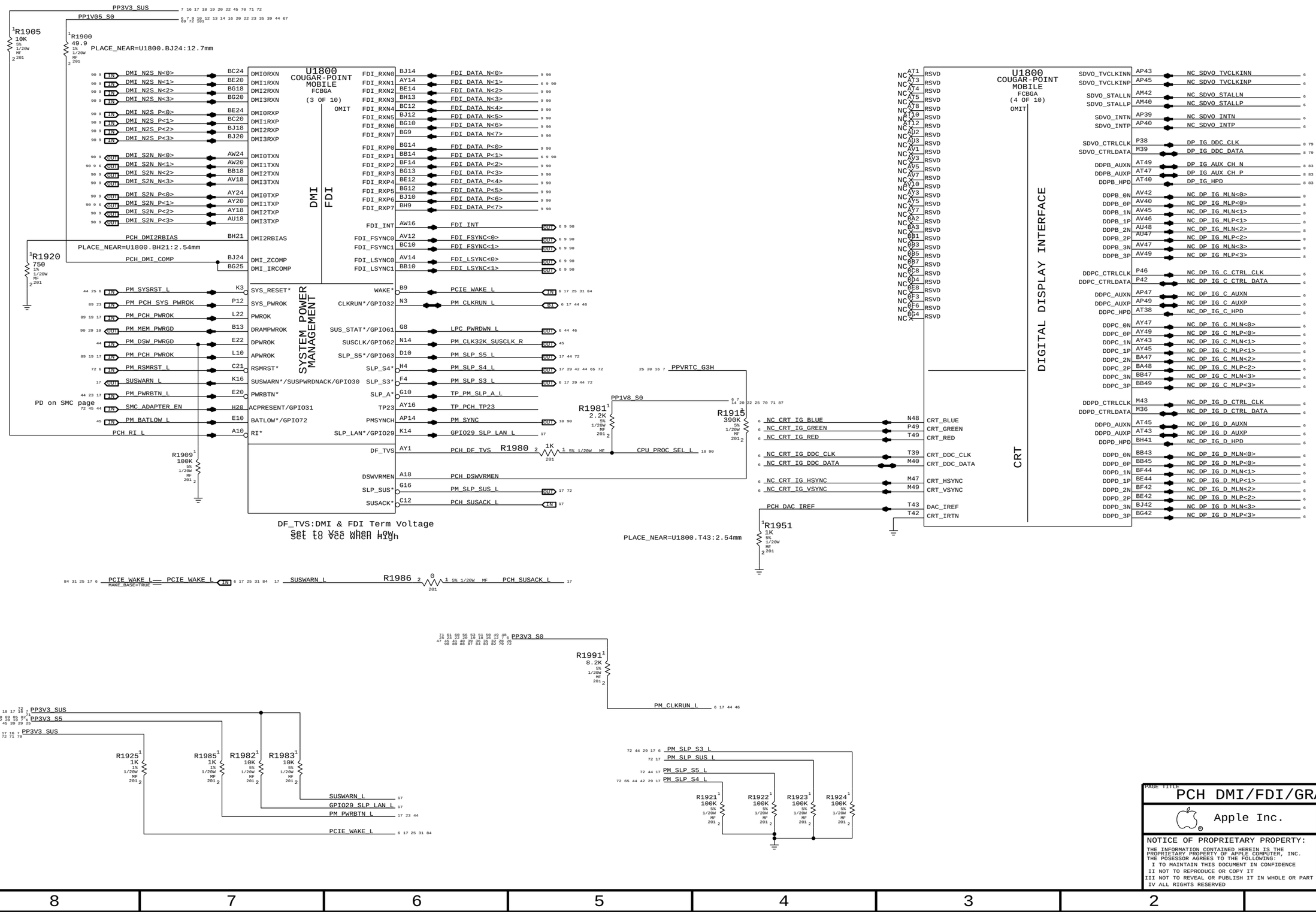
U1800
COUGAR-POINT
MOBILE
FCBGA
(3 OF 10)
OMIT
DMI
FDI
SYSTEM POWER MANAGEMENT
DMI_N2S_N<0>
DMI_N2S_N<1>
DMI_N2S_N<2>
DMI_N2S_N<3>
DMI_N2S_P<0>
DMI_N2S_P<1>
DMI_N2S_P<2>
DMI_N2S_P<3>
DMI_S2N_N<0>
DMI_S2N_N<1>
DMI_S2N_N<2>
DMI_S2N_N<3>
DMI_S2N_P<0>
DMI_S2N_P<1>
DMI_S2N_P<2>
DMI_S2N_P<3>
PCH_DMI2RBIAS
PLACE_NEAR=U1800.BH21:2.54mm
PCH_DMI_COMP
FDI_DATA_N<0>
FDI_DATA_N<1>
FDI_DATA_N<2>
FDI_DATA_N<3>
FDI_DATA_N<4>
FDI_DATA_N<5>
FDI_DATA_N<6>
FDI_DATA_N<7>
FDI_DATA_P<0>
FDI_DATA_P<1>
FDI_DATA_P<2>
FDI_DATA_P<3>
FDI_DATA_P<4>
FDI_DATA_P<5>
FDI_DATA_P<6>
FDI_DATA_P<7>
FDI_INT
FDI_FSYNC<0>
FDI_FSYNC<1>
FDI_LSYNC<0>
FDI_LSYNC<1>
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PM_MEM_PWRGD
PM_DSW_PWRGD
PM_RSMRST_L
SUSWARN_L
PM_PWRBTN_L
SMC_ADAPTER_EN
PM_BATLOW_L
PCH_RI_L
PD on SMC page
PCIE_WAKE_L
PM_CLKRUN_L
LPC_PWRDWN_L
PM_CLK32K_SUSCLK_R
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PM_SLP_A_L
TP_PCH_TP23
PM_SYNC
GPIO29_SLP_LAN_L
PCH_DF_TVS
PPVRTC_G3H
PP1V8_S0
CPU_PROC_SEL_L
PCH_DSWVRMEN
PM_SLP_SUS_L
PCH_SUSACK_L
DF_TVS:DMI & FDI Term Voltage
Set to Vss when low
Set to Vcc when high
PLACE_NEAR=U1800.T43:2.54mm
SUSWARN_L
PCH_SUSACK_L
PP3V3_SUS
PP1V05_S0
PP3V3_S0
PP3V3_S5
PM_SLP_S3_L
PM_SLP_SUS_L
PM_SLP_S5_L
PM_SLP_S4_L
DIGITAL DISPLAY INTERFACE
CRT
NC_CRT_IG_BLUE
NC_CRT_IG_GREEN
NC_CRT_IG_RED
NC_CRT_IG_DDC_CLK
NC_CRT_IG_DDC_DATA
NC_CRT_IG_HSYNC
NC_CRT_IG_VSYNC
PCH_DAC_IREF
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_VSYNC
DAC_IREF
CRT_IRTN
SDVO_TVCLKINN
SDVO_TVCLKINP
SDVO_STALLN
SDVO_STALLP
SDVO_INTN
SDVO_INTP
SDVO_CTRLCLK
SDVO_CTRLDATA
DDPB_AUXN
DDPB_AUXP
DDPB_HPD
DDPB_0N
DDPB_0P
DDPB_1N
DDPB_1P
DDPB_2N
DDPB_2P
DDPB_3N
DDPB_3P
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPC_AUXN
DDPC_AUXP
DDPC_HPD
DDPC_0N
DDPC_0P
DDPC_1N
DDPC_1P
DDPC_2N
DDPC_2P
DDPC_3N
DDPC_3P
DDPD_CTRLCLK
DDPD_CTRLDATA
DDPD_AUXN
DDPD_AUXP
DDPD_HPD
DDPD_0N
DDPD_0P
DDPD_1N
DDPD_1P
DDPD_2N
DDPD_2P
DDPD_3N
DDPD_3P
NC_SDVO_TVCLKINN
NC_SDVO_TVCLKINP
NC_SDVO_STALLN
NC_SDVO_STALLP
NC_SDVO_INTN
NC_SDVO_INTP
DP_IG_DDC_CLK
DP_IG_DDC_DATA
DP_IG_AUX_CH_N
DP_IG_AUX_CH_P
DP_IG_HPD
NC_DP_IG_MLN<0>
NC_DP_IG_MLP<0>
NC_DP_IG_MLN<1>
NC_DP_IG_MLP<1>
NC_DP_IG_MLN<2>
NC_DP_IG_MLP<2>
NC_DP_IG_MLN<3>
NC_DP_IG_MLP<3>
NC_DP_IG_C_CTRL_CLK
NC_DP_IG_C_CTRL_DATA
NC_DP_IG_C_AUXN
NC_DP_IG_C_AUXP
NC_DP_IG_C_HPD
NC_DP_IG_C_MLN<0>
NC_DP_IG_C_MLP<0>
NC_DP_IG_C_MLN<1>
NC_DP_IG_C_MLP<1>
NC_DP_IG_C_MLN<2>
NC_DP_IG_C_MLP<2>
NC_DP_IG_C_MLN<3>
NC_DP_IG_C_MLP<3>
NC_DP_IG_D_CTRL_CLK
NC_DP_IG_D_CTRL_DATA
NC_DP_IG_D_AUXN
NC_DP_IG_D_AUXP
NC_DP_IG_D_HPD
NC_DP_IG_D_MLN<0>
NC_DP_IG_D_MLP<0>
NC_DP_IG_D_MLN<1>
NC_DP_IG_D_MLP<1>
NC_DP_IG_D_MLN<2>
NC_DP_IG_D_MLP<2>
NC_DP_IG_D_MLN<3>
NC_DP_IG_D_MLP<3>
PAGE TITLE
PCH DMI/FDI/GRAPHICS
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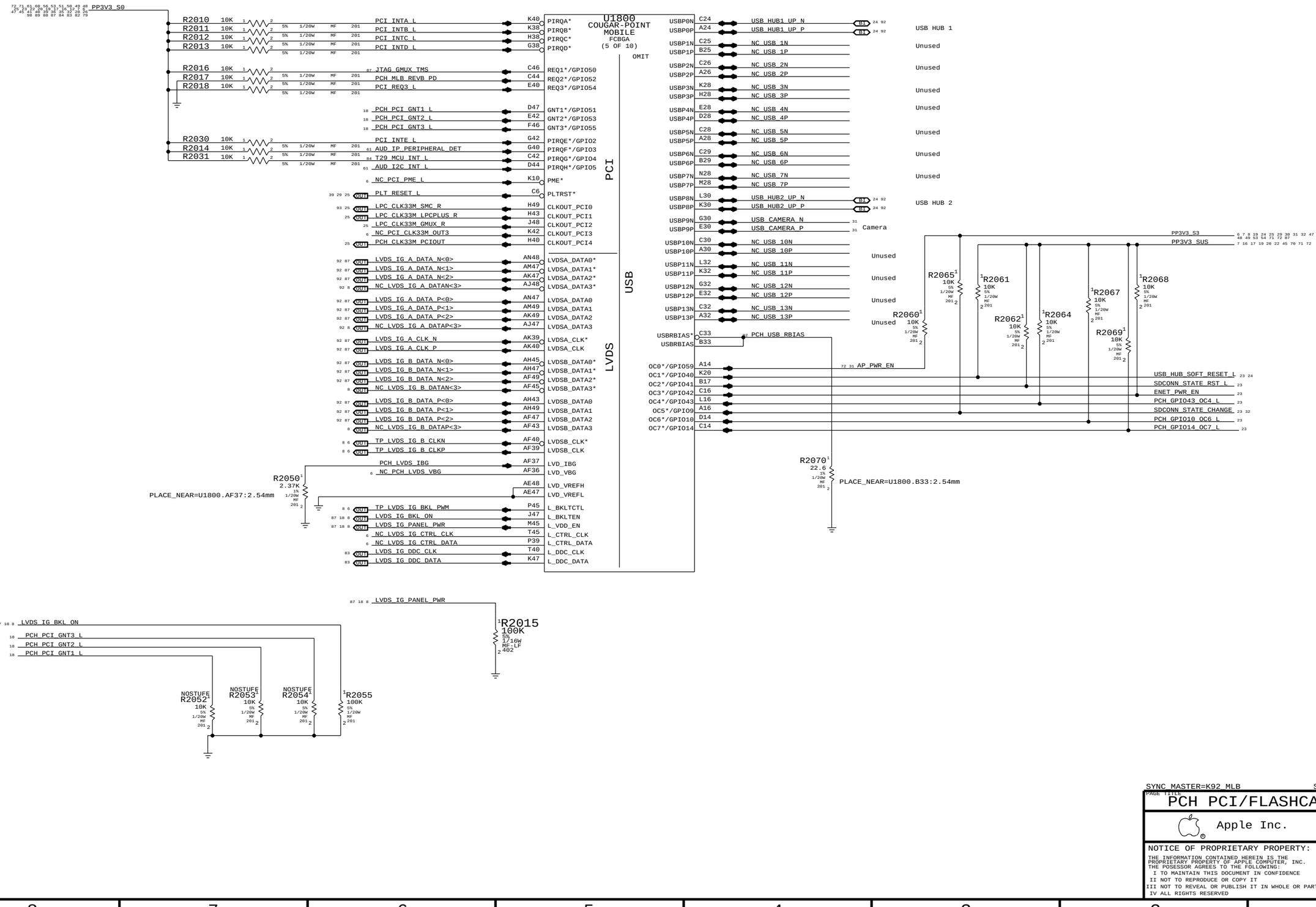

SYNC_MASTER=K92_MLB SYNC_DATE=07/06/2010

PAGE TITLE
PCH PCI/FLASHCACHE/USB

Apple Inc.

DRAWING NUMBER
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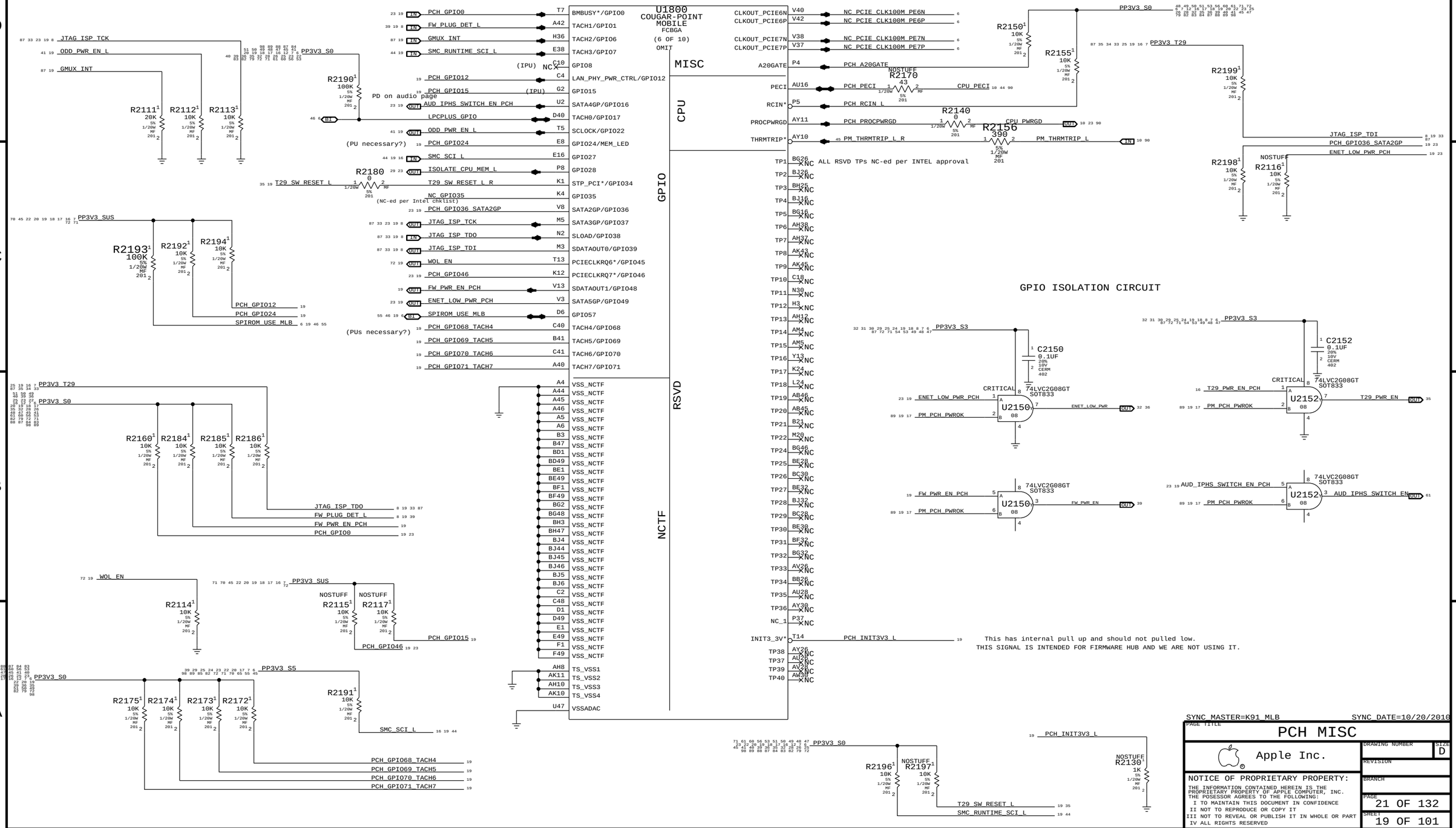

SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE: PCH MISC

Apple Inc.

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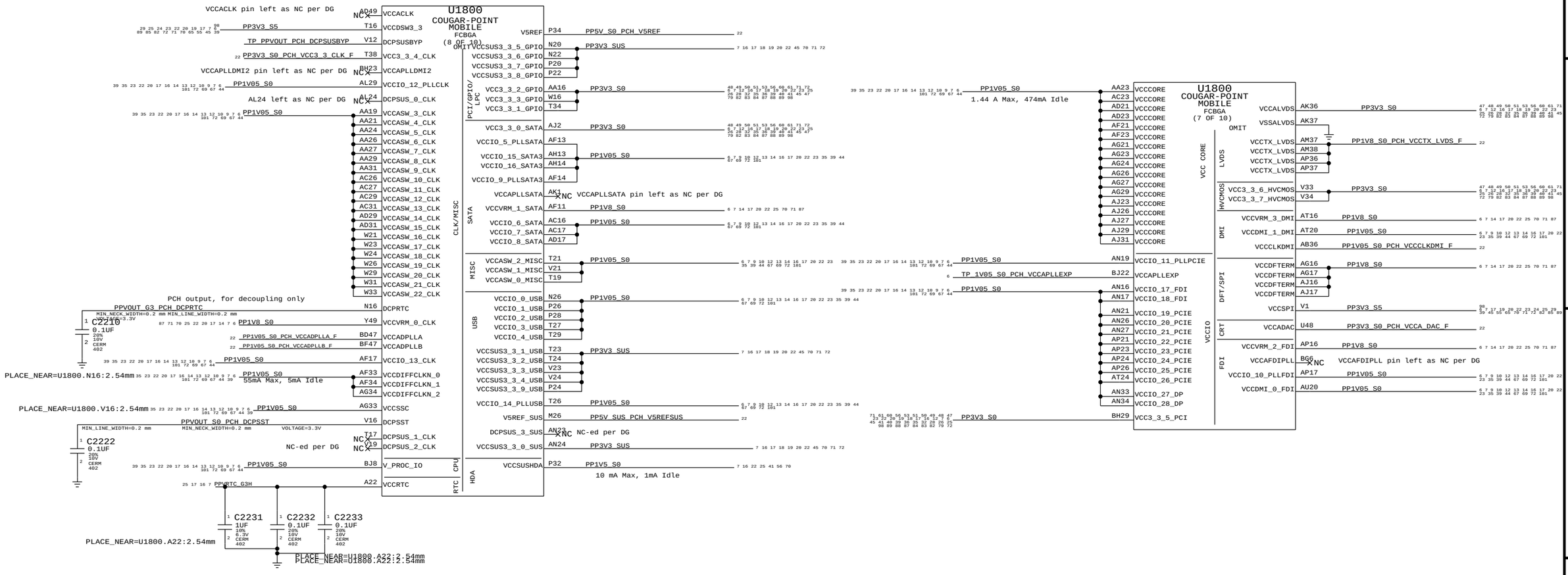

PAGE TITLE: PCH POWER

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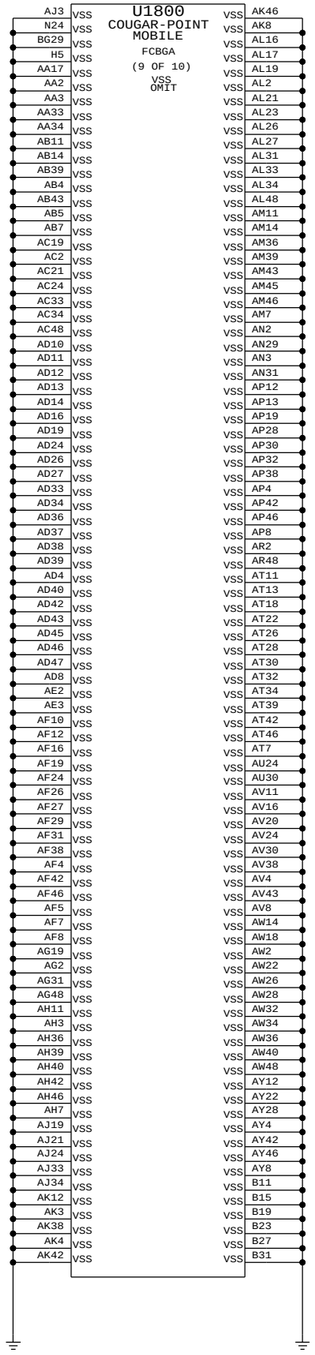

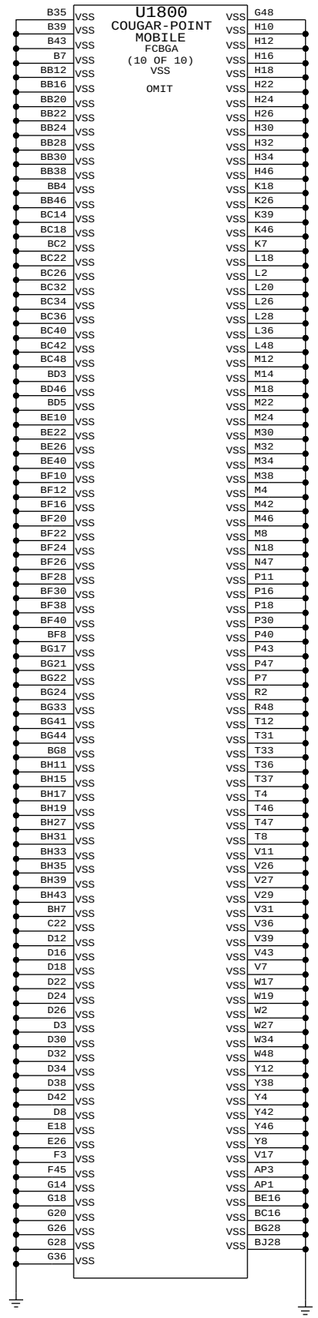

SYNC_MASTER=K92_MLB SYNC_DATE=04/30/2010

PAGE TITLE

PCH GROUNDS

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DRAWING NUMBER

SIZE D

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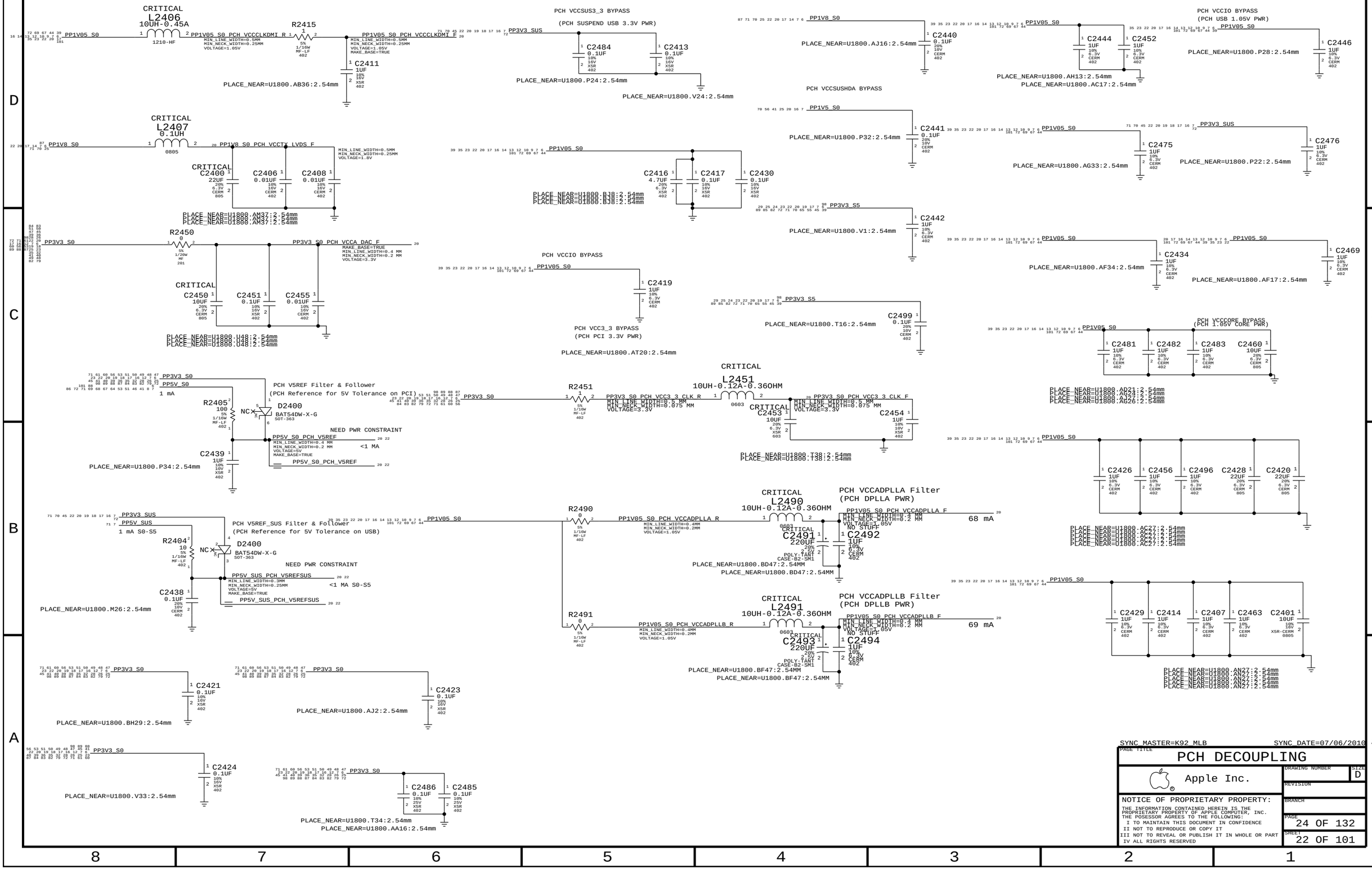
CRITICAL
L2406
10UH-0.45A
1210-HF
PP1V05_S0
PP1V05_S0_PCH_VCCCLKDMI_R
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
R2415
1/16W
MF-LF
402
PP1V05_S0_PCH_VCCCLKDMI_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
C2411
1UF
PLACE_NEAR=U1800.AB36:2.54mm
PCH VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)
PP3V3_SUS
C2484
0.1UF
C2413
0.1UF
PLACE_NEAR=U1800.P24:2.54mm
PLACE_NEAR=U1800.V24:2.54mm
PP1V8_S0
C2440
0.1UF
PLACE_NEAR=U1800.AJ16:2.54mm
PCH VCCIO BYPASS
(PCH USB 1.05V PWR)
PP1V05_S0
C2444
1UF
C2452
1UF
PLACE_NEAR=U1800.AH13:2.54mm
PLACE_NEAR=U1800.AC17:2.54mm
C2446
1UF
PLACE_NEAR=U1800.P28:2.54mm
CRITICAL
L2407
0.1UH
0805
PP1V8_S0_PCH_VCCTX_LVDS_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.8V
CRITICAL
C2400
22UF
C2406
0.01UF
C2408
0.01UF
PLACE_NEAR=U1800.AM37:2.54mm
PLACE_NEAR=U1800.AM37:2.54mm
PLACE_NEAR=U1800.AM37:2.54mm
PCH VCCSUSHDA BYPASS
PP1V5_S0
C2441
0.1UF
PLACE_NEAR=U1800.P32:2.54mm
PP1V05_S0
C2416
4.7UF
C2417
0.1UF
C2430
0.1UF
PLACE_NEAR=U1800.BJ8:2.54mm
PLACE_NEAR=U1800.BJ8:2.54mm
PLACE_NEAR=U1800.BJ8:2.54mm
PP1V05_S0
C2475
1UF
PLACE_NEAR=U1800.AG33:2.54mm
PP3V3_SUS
C2476
1UF
PLACE_NEAR=U1800.P22:2.54mm
PP3V3_S5
C2442
1UF
PLACE_NEAR=U1800.V1:2.54mm
R2450
0
PP3V3_S0
PP3V3_S0_PCH_VCCA_DAC_F
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
CRITICAL
C2450
10UF
C2451
0.1UF
C2455
0.01UF
PLACE_NEAR=U1800.U48:2.54mm
PLACE_NEAR=U1800.U48:2.54mm
PLACE_NEAR=U1800.U48:2.54mm
PCH VCCIO BYPASS
PP1V05_S0
C2419
1UF
PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)
PLACE_NEAR=U1800.AT20:2.54mm
PP1V05_S0
C2434
1UF
PLACE_NEAR=U1800.AF34:2.54mm
C2469
1UF
PLACE_NEAR=U1800.AF17:2.54mm
PP3V3_S5
C2499
0.1UF
PLACE_NEAR=U1800.T16:2.54mm
PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C2481
1UF
C2482
1UF
C2483
1UF
C2460
10UF
PLACE_NEAR=U1800.AD21:2.54mm
PLACE_NEAR=U1800.AG24:2.54mm
PLACE_NEAR=U1800.AG25:2.54mm
PLACE_NEAR=U1800.AG26:2.54mm
PP3V3_S0
PP5V_S0
1 mA
PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)
R2405
100
NC
D2400
BAT54DW-X-G
SOT-363
NEED PWR CONSTRAINT
PP5V_S0_PCH_V5REF
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 MA
PP5V_S0_PCH_V5REF
C2439
1UF
PLACE_NEAR=U1800.P34:2.54mm
PP3V3_S0
PP3V3_S0_PCH_VCC3_3_CLK_R
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=3.3V
R2451
CRITICAL
L2451
10UH-0.12A-0.36OHM
0603
PP3V3_S0_PCH_VCC3_3_CLK_F
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=3.3V
CRITICAL
C2453
10UF
C2454
1UF
PLACE_NEAR=U1800.T38:2.54mm
PLACE_NEAR=U1800.T38:2.54mm
PP1V05_S0
C2426
1UF
C2456
1UF
C2496
1UF
C2428
22UF
C2420
22UF
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PP3V3_SUS
PP5V_SUS
1 mA S0-S5
PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)
R2404
10
NC
D2400
BAT54DW-X-G
SOT-363
NEED PWR CONSTRAINT
PP5V_SUS_PCH_V5REFSUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 MA S0-S5
PP5V_SUS_PCH_V5REFSUS
C2438
0.1UF
PLACE_NEAR=U1800.M26:2.54mm
PP1V05_S0
PP1V05_S0_PCH_VCCADPLLA_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
R2490
0
CRITICAL
L2490
10UH-0.12A-0.36OHM
0603
PP1V05_S0_PCH_VCCADPLLA_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
68 mA
PCH VCCADPLLA Filter
(PCH DPLLA PWR)
NO STUFF
CRITICAL
C2491
220UF
POLY-TANT
CASE-B2-SM1
C2492
1UF
PLACE_NEAR=U1800.BD47:2.54MM
PLACE_NEAR=U1800.BD47:2.54MM
PP1V05_S0
PP1V05_S0_PCH_VCCADPLLB_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
R2491
0
CRITICAL
L2491
10UH-0.12A-0.36OHM
0603
PP1V05_S0_PCH_VCCADPLLB_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
69 mA
PCH VCCADPLLB Filter
(PCH DPLLB PWR)
NO STUFF
CRITICAL
C2493
220UF
POLY-TANT
CASE-B2-SM1
C2494
1UF
PLACE_NEAR=U1800.BF47:2.54MM
PLACE_NEAR=U1800.BF47:2.54MM
PP1V05_S0
C2429
1UF
C2414
1UF
C2407
1UF
C2463
1UF
C2401
10UF
X5R-CERM
0805
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PP3V3_S0
C2421
0.1UF
PLACE_NEAR=U1800.BH29:2.54mm
PP3V3_S0
C2423
0.1UF
PLACE_NEAR=U1800.AJ2:2.54mm
PP3V3_S0
C2424
0.1UF
PLACE_NEAR=U1800.V33:2.54mm
PP3V3_S0
C2486
0.1UF
C2485
0.1UF
PLACE_NEAR=U1800.T34:2.54mm
PLACE_NEAR=U1800.AA16:2.54mm
SYNC_MASTER=K92_MLB
SYNC_DATE=07/06/2010
PAGE TITLE
PCH DECOUPLING
Apple Inc.
DRAWING NUMBER
SIZE
D
REVISION
BRANCH
PAGE
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SHEET
22 OF 101
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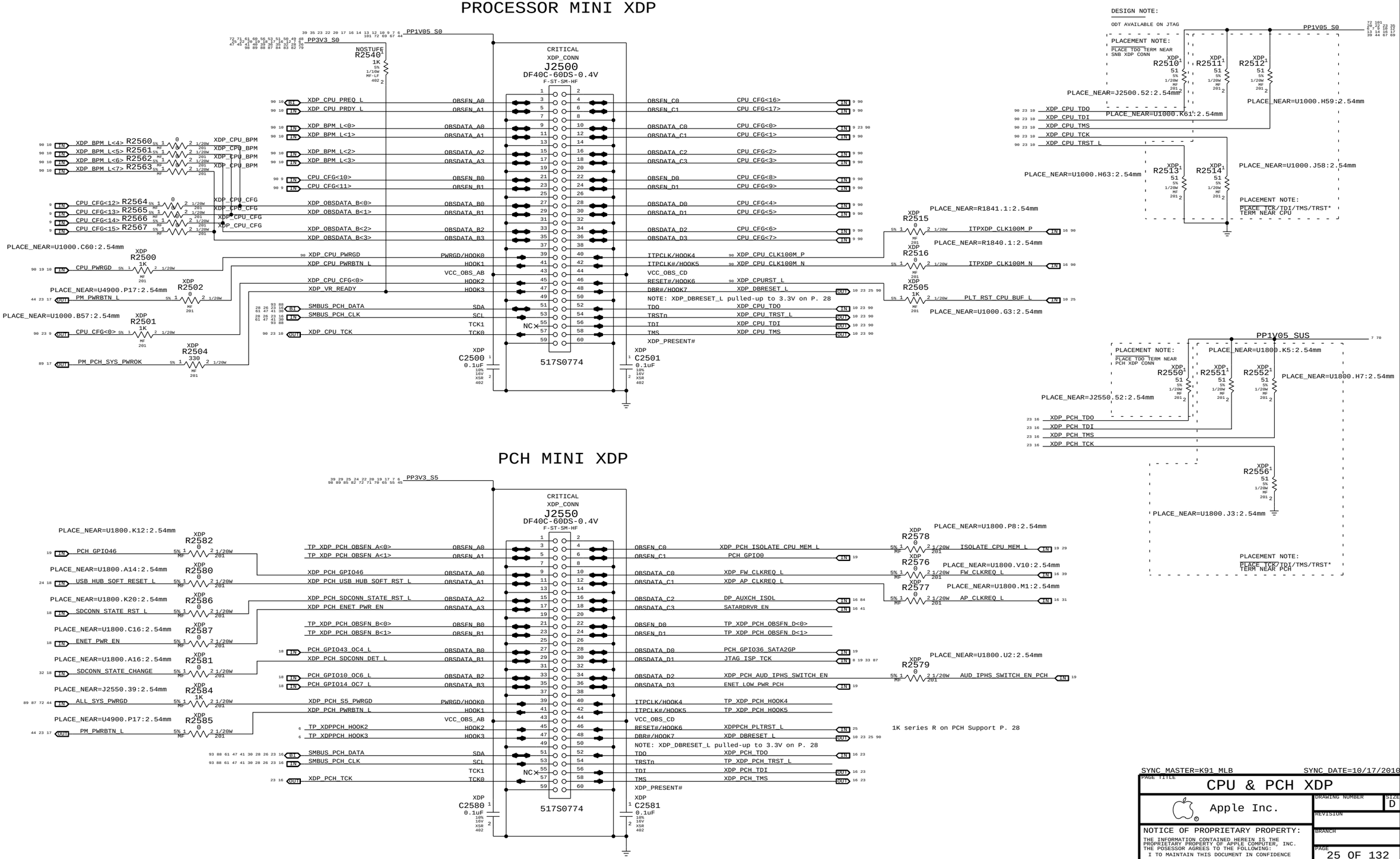
PROCESSOR MINI XDP



PCH MINI XDP

SYNC_MASTER=K91_MLB SYNC_DATE=10/17/2010

PAGE TITLE: CPU & PCH XDP

Apple Inc.

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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600,U2650	CRITICAL	USBHUB_2061
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B

T29 - no longer used, pulled up to 3V3 S0

IR Receiver

External B

External C

Bluetooth

Trackpad/Keyboard

External A

SD Card/Express Card

SYNC MASTER=K91_ERIC SYNC DATE=10/08/2010

PAGE TITLE: USB HUBS

Apple Inc.

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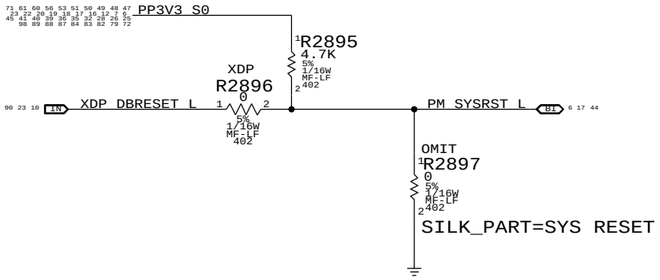
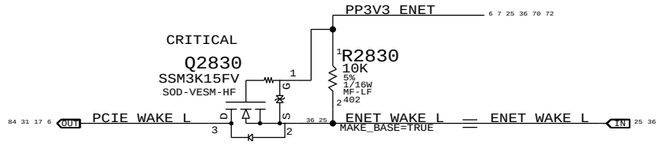
PCH Reset Button

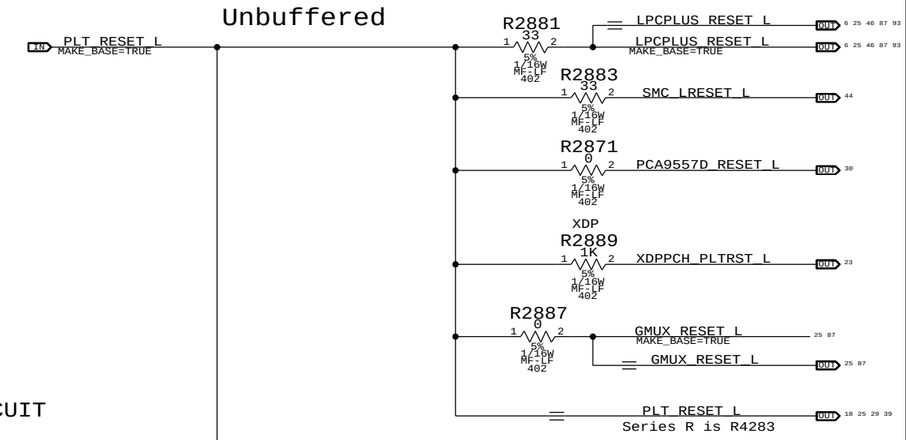


Ethernet WAKE# Isolation



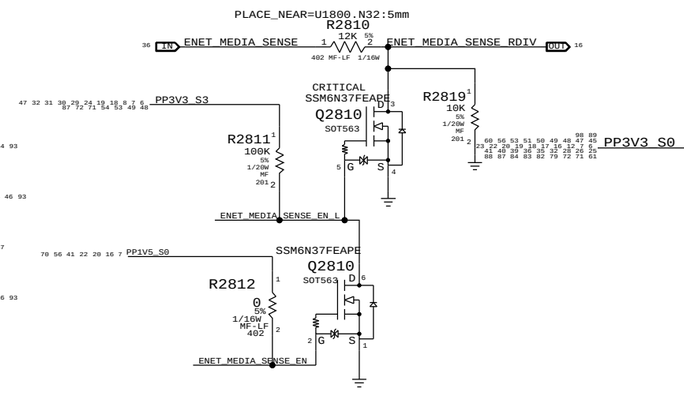
Platform Reset Connections

Unbuffered



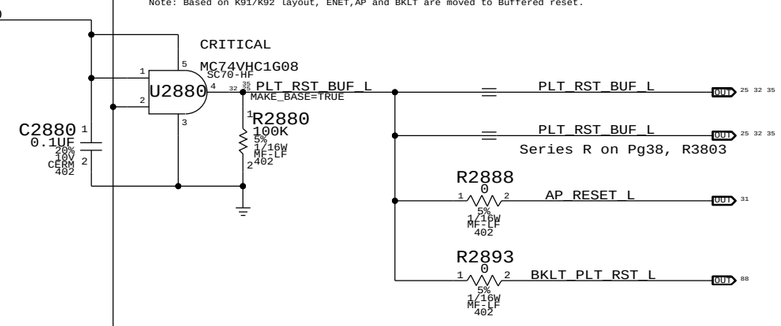
Series R is R4283

ENET_MEDIA_SENSE ISOLATION CIRCUIT



Buffered

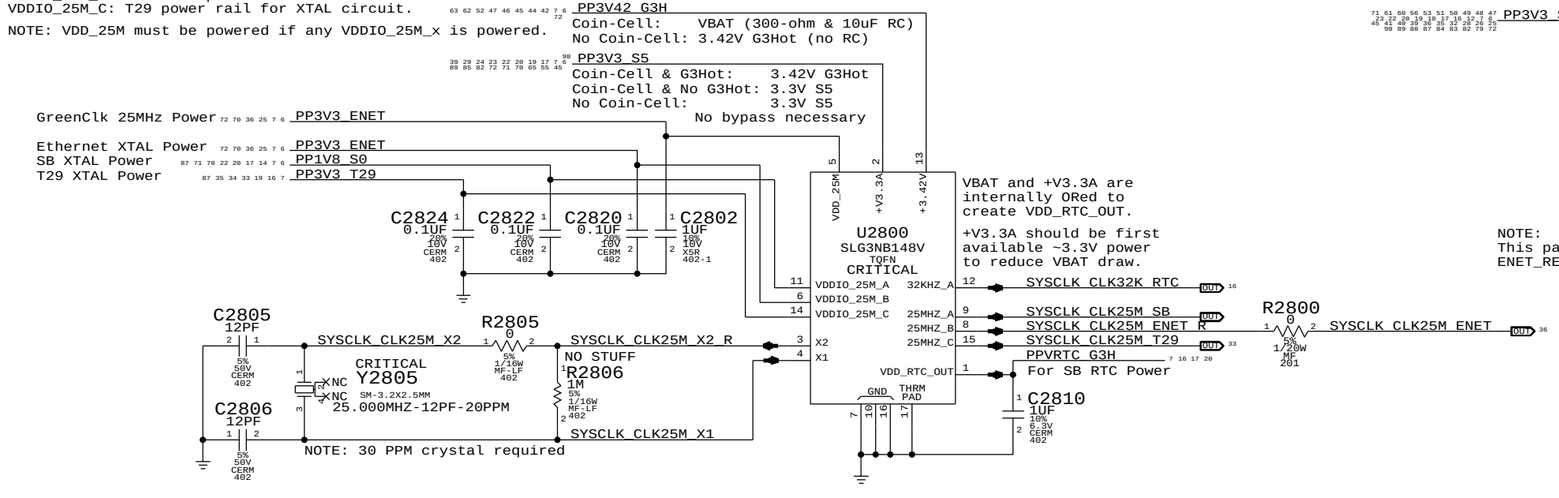
Note: Based on K91/K92 layout, ENET,AP and BKLT are moved to Buffered reset.

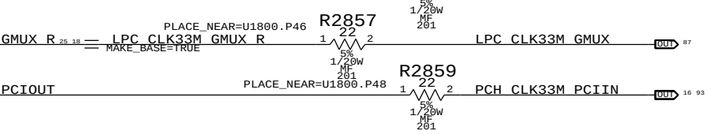


System RTC Power Source & 32kHz / 25MHz Clock Generator

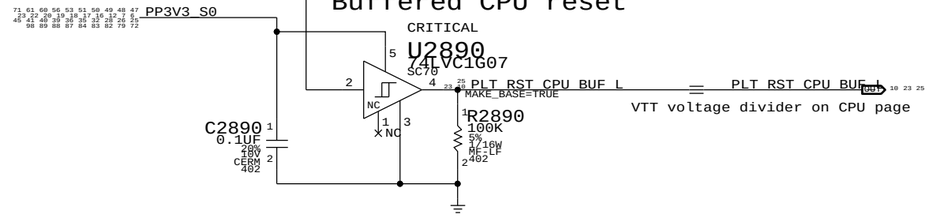
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.





Buffered CPU reset



NOTE:
This page is different for K92.
ENET_RESET_L hooked up differently on both the projects.

SYNC_MASTER=K92_MLB SYNC_DATE=07/06/2010

PAGE TITLE: Chipset Support

Apple Inc.

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_A_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C2900 10UF 20% 6.3V X6S 603 — PLACE_NEAR=J2900.75:2.54mm
C2901 10UF 20% 6.3V X6S 603 — PLACE_NEAR=J2900.75:2.54mm

C2910 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2911 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2912 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2913 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2914 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2915 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2916 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2917 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2918 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2919 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2920 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2921 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2922 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2923 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm

PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFCA_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

PP3V3_S0

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

PP0V75_S0_DDRVTT

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

J2900 — DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2) — F-RT-THB

OMIT_TABLE

KEY

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204

NC× on pins 77, 125, 122

MEM_A_CKE<0> MEM_A_CKE<1>
MEM_A_BA<2> MEM_A_A<15> MEM_A_A<14>
MEM_A_A<12> MEM_A_A<11>
MEM_A_A<9> MEM_A_A<7>
MEM_A_A<8> MEM_A_A<6>
MEM_A_A<5> MEM_A_A<4>
MEM_A_A<3> MEM_A_A<2>
MEM_A_A<1> MEM_A_A<0>
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MEM_A_CLK_N<0> MEM_A_CLK_N<1>
MEM_A_A<10> MEM_A_BA<1>
MEM_A_BA<0> MEM_A_RAS_L
MEM_A_WE_L MEM_A_CS_L<0>
MEM_A_CAS_L MEM_A_ODT<0>
MEM_A_A<13> MEM_A_ODT<1>
MEM_A_CS_L<1>

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MEM_A_DQS_P<4>
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MEM_A_DQS_P<6>
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MEM_A_DQ<59>
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MEM_A_DQS_N<7>
MEM_A_DQS_P<7>
MEM_A_DQ<62>
MEM_A_DQ<63>
MEM_EVENT_L
SMBUS_PCH_DATA
SMBUS_PCH_CLK

MEM_A_SA<0>
MEM_A_SA<1>

516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

J2900 — DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2) — CRITICAL — F-RT-THB

OMIT_TABLE

KEY

1	VREFDQ	VSS	2
3	VSS	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS	8
9	VSS	DQS0*	10
11	DM0	DQS0	12
13	VSS	VSS	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS	VSS	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS	VSS	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS	VSS	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS	VSS	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS	VSS	44
45	DQS2*	DM2	46
47	DQS2	VSS	48
49	VSS	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS	54
55	VSS	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS	60
61	VSS	DQS3*	62
63	DM3	DQS3	64
65	VSS	VSS	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS	VSS	72

MEM_A_DQ<0> MEM_A_DQ<4>
MEM_A_DQ<1> MEM_A_DQ<5>
MEM_A_DQ<2> MEM_A_DQS_N<0>
MEM_A_DQ<3> MEM_A_DQS_P<0>
MEM_A_DQ<8> MEM_A_DQ<6>
MEM_A_DQ<9> MEM_A_DQ<7>
MEM_A_DQS_N<1> MEM_A_DQ<12>
MEM_A_DQS_P<1> MEM_A_DQ<13>
MEM_A_DQ<10> MEM_RESET_L
MEM_A_DQ<11> MEM_A_DQ<14>
MEM_A_DQ<16> MEM_A_DQ<15>
MEM_A_DQ<17>
MEM_A_DQS_N<2> MEM_A_DQ<20>
MEM_A_DQS_P<2> MEM_A_DQ<21>
MEM_A_DQ<18>
MEM_A_DQ<19> MEM_A_DQ<22>
MEM_A_DQ<24> MEM_A_DQ<23>
MEM_A_DQ<25>
MEM_A_DQ<28>
MEM_A_DQ<29>
MEM_A_DQS_N<3>
MEM_A_DQS_P<3>
MEM_A_DQ<26> MEM_A_DQ<30>
MEM_A_DQ<27> MEM_A_DQ<31>

See CSA05 BOM table

"Factory" (top) slot

SYNC_MASTER=K92_SUMA	SYNC_DATE=06/23/2010
PAGE TITLE: DDR3 SO-DIMM Connector A	
Apple Inc.	DRAWING NUMBER — SIZE: D
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	BRANCH
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	SHEET: 26 OF 101

CPU CHANNEL A DQS 0 -> DIMM A DQS 0

91 11 6	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	26
91 11 6	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	26
91 11 6	MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	26
91 11 6	MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	26
91 11 6	MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	26
91 11 6	MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	26
91 11 6	MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	26
91 11 6	MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	26
91 11 6	MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	26
91 11 6	MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	26

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

91 11 6	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	26
91 11 6	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	26
91 11 6	MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	26
91 11 6	MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	26
91 11 6	MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	26
91 11 6	MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	26
91 11 6	MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	26
91 11 6	MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	26
91 11 6	MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	26
91 11 6	MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	26

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

91 11 6	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	26
91 11 6	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	26
91 11 6	MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	26
91 11 6	MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	26
91 11 6	MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	26
91 11 6	MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	26
91 11 6	MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	26
91 11 6	MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	26
91 11 6	MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	26
91 11 6	MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	26

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

91 11 6	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	26
91 11 6	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	26
91 11 6	MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	26
91 11 6	MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	26
91 11 6	MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	26
91 11 6	MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	26
91 11 6	MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	26
91 11 6	MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	26
91 11 6	MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	26
91 11 6	MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	26

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

91 11 6	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	26
91 11 6	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	26
91 11 6	MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	26
91 11 6	MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	26
91 11 6	MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	26
91 11 6	MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	26
91 11 6	MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	26
91 11 6	MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	26
91 11 6	MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	26
91 27 26 11 6	MEM_A_DQ<32>	MAKE_BASE=TRUE	MEM_A_DQ<32>	6 11 26 27 91

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

91 11 6	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	26
91 11 6	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	26
91 11 6	MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	26
91 11 6	MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	26
91 11 6	MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	26
91 11 6	MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	26
91 11 6	MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	26
91 11 6	MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	26
91 11 6	MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	26
91 11 6	MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	26

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

91 27 26 11 6	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	MEM_A_DQS_N<6>	6 11 26 27 91
91 27 26 11 6	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	MEM_A_DQS_P<6>	6 11 26 27 91
91 11 6	MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	26
91 11 6	MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	26
91 11 6	MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	26
91 11 6	MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	26
91 11 6	MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	26
91 11 6	MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	26
91 11 6	MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	26
91 11 6	MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	26

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

91 11 6	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	26
91 11 6	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	26
91 11 6	MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	26
91 11 6	MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	26
91 11 6	MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	26
91 11 6	MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	26
91 11 6	MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	26
91 11 6	MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	26
91 11 6	MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	26
91 11 6	MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	26

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

91 11 6	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	28
91 11 6	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	28
91 11 6	MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	28
91 11 6	MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	28
91 11 6	MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	28
91 11 6	MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	28
91 11 6	MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	28
91 11 6	MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	28
91 11 6	MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	28
91 11 6	MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	28

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

91 11 6	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	28
91 11 6	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	28
91 11 6	MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	28
91 11 6	MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	28
91 11 6	MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	28
91 11 6	MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	28
91 11 6	MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	28
91 11 6	MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	28
91 11 6	MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	28
91 11 6	MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	28

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

91 11 6	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	28
91 11 6	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	28
91 11 6	MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	28
91 11 6	MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	28
91 11 6	MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	28
91 11 6	MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	28
91 11 6	MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	28
91 11 6	MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	28
91 11 6	MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	28
91 11 6	MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	28

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

91 11 6	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	28
91 11 6	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	28
91 11 6	MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	28
91 11 6	MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	28
91 11 6	MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	28
91 11 6	MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	28
91 11 6	MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	28
91 11 6	MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	28
91 11 6	MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	28
91 11 6	MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	28

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

91 11 6	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	28
91 11 6	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	28
91 11 6	MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	28
91 11 6	MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	28
91 11 6	MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	28
91 11 6	MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	28
91 11 6	MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	28
91 11 6	MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	28
91 11 6	MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	28
27 11 6 91 28	MEM_B_DQ<32>	MAKE_BASE=TRUE	MEM_B_DQ<32>	6 11 27 28 91

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

91 11 6	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	28
91 11 6	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	28
91 11 6	MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	28
91 11 6	MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	28
91 11 6	MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	28
91 11 6	MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	28
91 11 6	MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	28
91 11 6	MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	28
91 11 6	MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	28
91 11 6	MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	28

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

27 11 6 91 28	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	MEM_B_DQS_N<6>	6 11 27 28 91
27 11 6 91 28	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	MEM_B_DQS_P<6>	6 11 27 28 91
91 11 6	MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	28
91 11 6	MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	28
91 11 6	MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	28
91 11 6	MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	28
91 11 6	MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	28
91 11 6	MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	28
91 11 6	MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	28
91 11 6	MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	28

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

91 11 6	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	28
91 11 6	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	28
91 11 6	MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	28
91 11 6	MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	28
91 11 6	MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	28
91 11 6	MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	28
91 11 6	MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	28
91 11 6	MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	28
91 11 6	MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	28
91 11 6	MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	28

SYNC_MASTER=K92_SUMA SYNC_DATE=05/10/2010

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C3100 10UF 20% 6.3V X6S CERM 603
C3101 10UF 20% 6.3V X6S CERM 603
PLACE_NEAR=J3100.75:2.54mm

C3110 C3111 C3112 C3113 C3114 C3115 C3116 C3117 C3118 C3119 C3120 C3121 C3122 C3123
0.1UF 20% 10V CERM 402
PLACE_NEAR=J3100.75:2.54mm
PLACE_NEAR=J3100.75:2.54mm

PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFCA_B

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

PP3V3_S0

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

PP0V75_S0_DDRVTT

C3150 C3151 C3152 C3153
1UF 10% 10V X5R 402

J3100 DDR3-SODIMM (2 OF 2)

OMIT_TABLE

73	CKE0		74	CKE1	
75	VDD		76	VDD	
77	NC	NC×	78	A15	MEM_B_A<15>
79	BA2	MEM_B_BA<2>	80	A14	MEM_B_A<14>
81	VDD		82	VDD	
83	A12/BC*	MEM_B_A<12>	84	A11	MEM_B_A<11>
85	A9	MEM_B_A<9>	86	A7	MEM_B_A<7>
87	VDD		88	VDD	
89	A8	MEM_B_A<8>	90	A6	MEM_B_A<6>
91	A5	MEM_B_A<5>	92	A4	MEM_B_A<4>
93	VDD		94	VDD	
95	A3	MEM_B_A<3>	96	A2	MEM_B_A<2>
97	A1	MEM_B_A<1>	98	A0	MEM_B_A<0>
99	VDD		100	VDD	
101	CK0	MEM_B_CLK_P<0>	102	CK1	MEM_B_CLK_P<1>
103	CK0*	MEM_B_CLK_N<0>	104	CK1*	MEM_B_CLK_N<1>
105	VDD		106	VDD	
107	A10/AP	MEM_B_A<10>	108	BA1	MEM_B_BA<1>
109	BA0	MEM_B_BA<0>	110	RAS*	MEM_B_RAS_L
111	VDD		112	VDD	
113	WE*	MEM_B_WE_L	114	S0*	MEM_B_CS_L<0>
115	CAS*	MEM_B_CAS_L	116	ODT0	MEM_B_ODT<0>
117	VDD		118	VDD	
119	A13	MEM_B_A<13>	120	ODT1	MEM_B_ODT<1>
121	S1*	MEM_B_CS_L<1>	122	NC	×NC
123	VDD		124	VDD	
125	TEST	NC×	126	VREFCA	
127	VSS		128	VSS	
129	DQ32	MEM_B_DQ<32>	130	DQ36	MEM_B_DQ<36>
131	DQ33	MEM_B_DQ<33>	132	DQ37	MEM_B_DQ<37>
133	VSS		134	VSS	
135	DQS4*	MEM_B_DQS_N<4>	136	DM4	
137	DQS4	MEM_B_DQS_P<4>	138	VSS	
139	VSS		140	DQ38	MEM_B_DQ<38>
141	DQ34	MEM_B_DQ<34>	142	DQ39	MEM_B_DQ<39>
143	DQ35	MEM_B_DQ<35>	144	VSS	
145	VSS		146	DQ44	MEM_B_DQ<44>
147	DQ40	MEM_B_DQ<40>	148	DQ45	MEM_B_DQ<45>
149	DQ41	MEM_B_DQ<41>	150	VSS	
151	VSS		152	DQS5*	MEM_B_DQS_N<5>
153	DM5		154	DQS5	MEM_B_DQS_P<5>
155	VSS		156	VSS	
157	DQ42	MEM_B_DQ<42>	158	DQ46	MEM_B_DQ<46>
159	DQ43	MEM_B_DQ<43>	160	DQ47	MEM_B_DQ<47>
161	VSS		162	VSS	
163	DQ48	MEM_B_DQ<48>	164	DQ52	MEM_B_DQ<52>
165	DQ49	MEM_B_DQ<49>	166	DQ53	MEM_B_DQ<53>
167	VSS		168	VSS	
169	DQS6*	MEM_B_DQS_N<6>	170	DM6	
171	DQS6	MEM_B_DQS_P<6>	172	VSS	
173	VSS		174	DQ54	MEM_B_DQ<54>
175	DQ50	MEM_B_DQ<50>	176	DQ55	MEM_B_DQ<55>
177	DQ51	MEM_B_DQ<51>	178	VSS	
179	VSS		180	DQ60	MEM_B_DQ<60>
181	DQ56	MEM_B_DQ<56>	182	DQ61	MEM_B_DQ<61>
183	DQ57	MEM_B_DQ<57>	184	VSS	
185	VSS		186	DQS7*	MEM_B_DQS_N<7>
187	DM7		188	DQS7	MEM_B_DQS_P<7>
189	VSS		190	VSS	
191	DQ58	MEM_B_DQ<58>	192	DQ62	MEM_B_DQ<62>
193	DQ59	MEM_B_DQ<59>	194	DQ63	MEM_B_DQ<63>
195	VSS		196	VSS	
197	SA0	MEM_B_SA<0>	198	EVENT*	MEM_EVENT_L
199	VDDSPD		200	SDA	SMBUS_PCH_DATA
201	SA1	MEM_B_SA<1>	202	SCL	SMBUS_PCH_CLK
203	VTT		204	VTT	PP0V75_S0_DDRVTT
205	MTG PIN		206	MTG PIN	
207	MTG PIN		208	MTG PIN	
209	MTG PIN		210	MTG PIN	
211	MTG PIN		212	MTG PIN	

MTG PINS

516S0806
SPD ADDR=0xA4(WR)/0xA5(RD)

J3100 DDR3-SODIMM (1 OF 2)

CRITICAL

OMIT_TABLE

1	VREFDQ		2	VSS	
3	VSS		4	DQ4	=MEM_B_DQ<4>
5	DQ0	=MEM_B_DQ<0>	6	DQ5	=MEM_B_DQ<5>
7	DQ1	=MEM_B_DQ<1>	8	VSS	
9	VSS		10	DQS0*	=MEM_B_DQS_N<0>
11	DM0		12	DQS0	=MEM_B_DQS_P<0>
13	VSS		14	VSS	
15	DQ2	=MEM_B_DQ<2>	16	DQ6	=MEM_B_DQ<6>
17	DQ3	=MEM_B_DQ<3>	18	DQ7	=MEM_B_DQ<7>
19	VSS		20	VSS	
21	DQ8	=MEM_B_DQ<8>	22	DQ12	=MEM_B_DQ<12>
23	DQ9	=MEM_B_DQ<9>	24	DQ13	=MEM_B_DQ<13>
25	VSS		26	VSS	
27	DQS1*	=MEM_B_DQS_N<1>	28	DM1	
29	DQS1	=MEM_B_DQS_P<1>	30	RESET*	MEM_RESET_L
31	VSS		32	VSS	
33	DQ10	=MEM_B_DQ<10>	34	DQ14	=MEM_B_DQ<14>
35	DQ11	=MEM_B_DQ<11>	36	DQ15	=MEM_B_DQ<15>
37	VSS		38	VSS	
39	DQ16	=MEM_B_DQ<16>	40	DQ20	=MEM_B_DQ<20>
41	DQ17	=MEM_B_DQ<17>	42	DQ21	=MEM_B_DQ<21>
43	VSS		44	VSS	
45	DQS2*	=MEM_B_DQS_N<2>	46	DM2	
47	DQS2	=MEM_B_DQS_P<2>	48	VSS	
49	VSS		50	DQ22	=MEM_B_DQ<22>
51	DQ18	=MEM_B_DQ<18>	52	DQ23	=MEM_B_DQ<23>
53	DQ19	=MEM_B_DQ<19>	54	VSS	
55	VSS		56	DQ28	=MEM_B_DQ<28>
57	DQ24	=MEM_B_DQ<24>	58	DQ29	=MEM_B_DQ<29>
59	DQ25	=MEM_B_DQ<25>	60	VSS	
61	VSS		62	DQS3*	=MEM_B_DQS_N<3>
63	DM3		64	DQS3	=MEM_B_DQS_P<3>
65	VSS		66	VSS	
67	DQ26	=MEM_B_DQ<26>	68	DQ30	=MEM_B_DQ<30>
69	DQ27	=MEM_B_DQ<27>	70	DQ31	=MEM_B_DQ<31>
71	VSS		72	VSS	

516S0806

"Expansion" (bottom) slot

SYNC_MASTER=K92_SUMA SYNC_DATE=06/23/2010

PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

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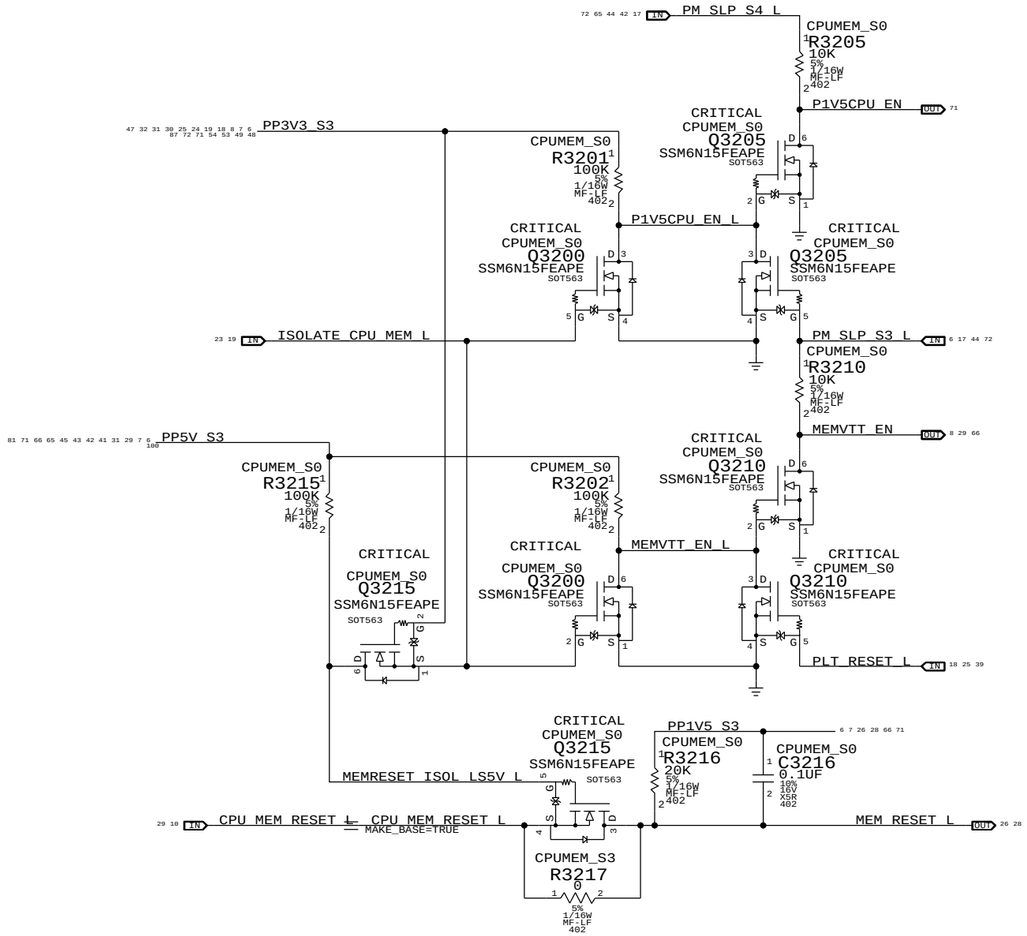
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

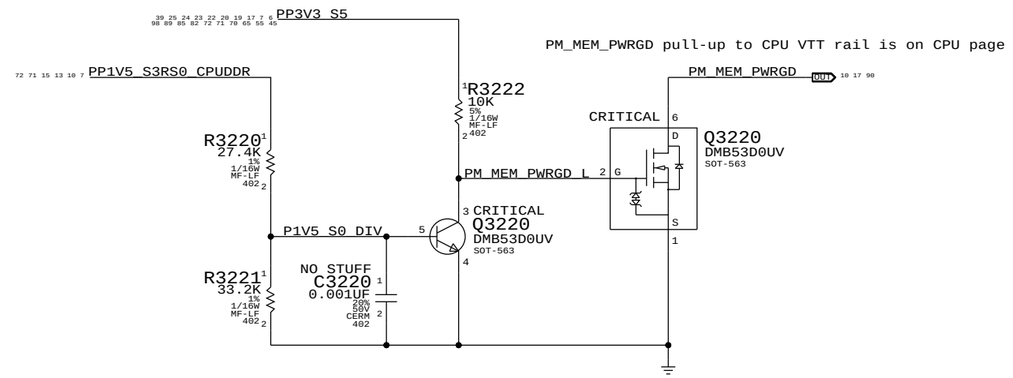


	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
to	4	0	0	1	1	X	1	0	1
S0	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

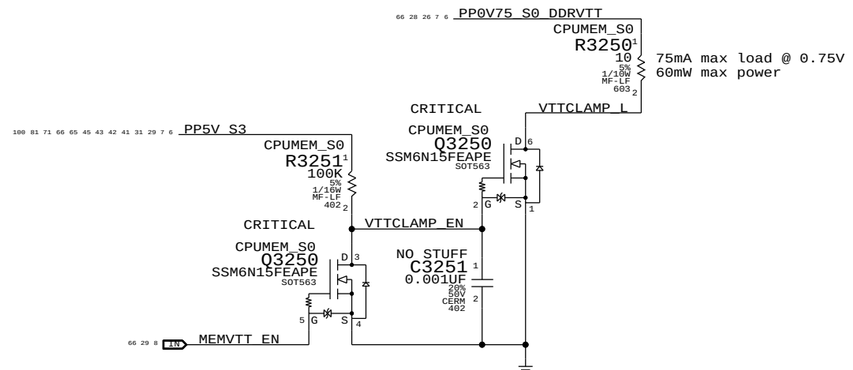
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

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Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L3470,L3471,L3473,L3474		

3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

AIRPORT

BLUETOOTH

ALS CAMERA

Supervisor & CLKFREG # Isolation

Delay = 60 ms +/- 20%

275 mA peak
206 mA nominal max

SYNC_MASTER=K91_MARY SYNC_DATE=10/08/2016

PAGE TITLE

X19/ALS/CAMERA CONNECTOR

Apple Inc.

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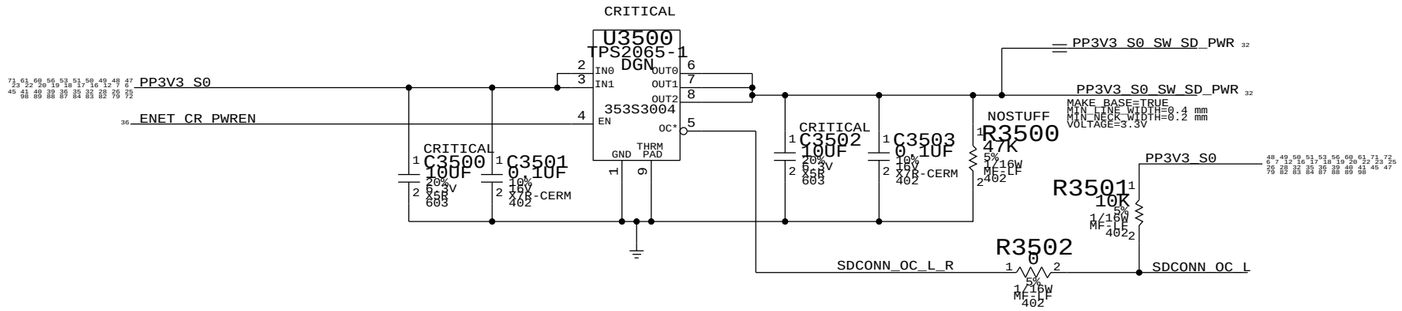
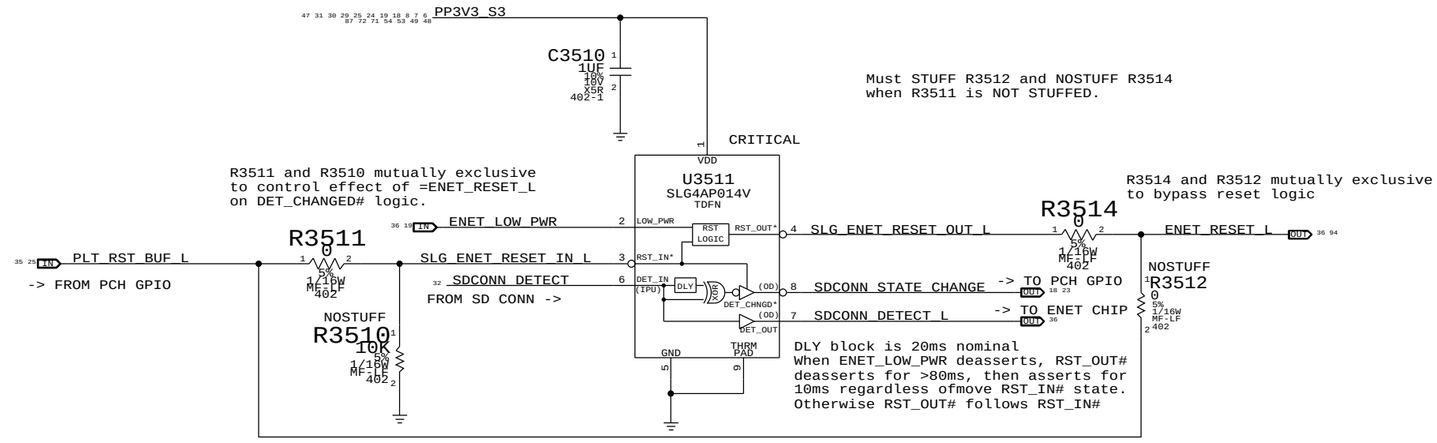
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

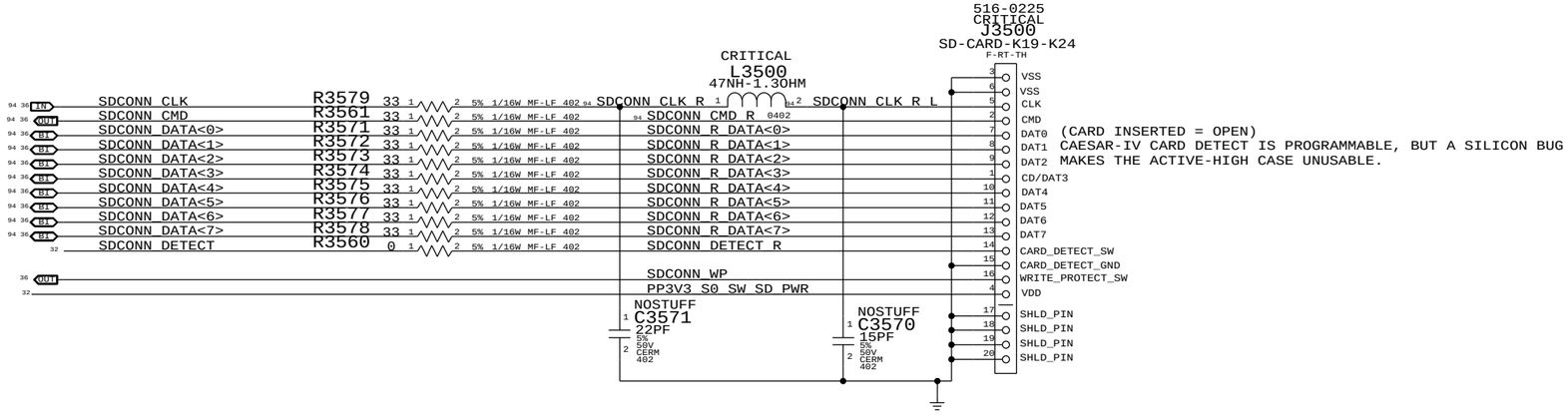
TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO LATCH CIRCUIT



SD CARD CONNECTOR



SYNC MASTER=K91_ERIC SYNC DATE=10/08/2010

PAGE TITLE

SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER

SIZE D

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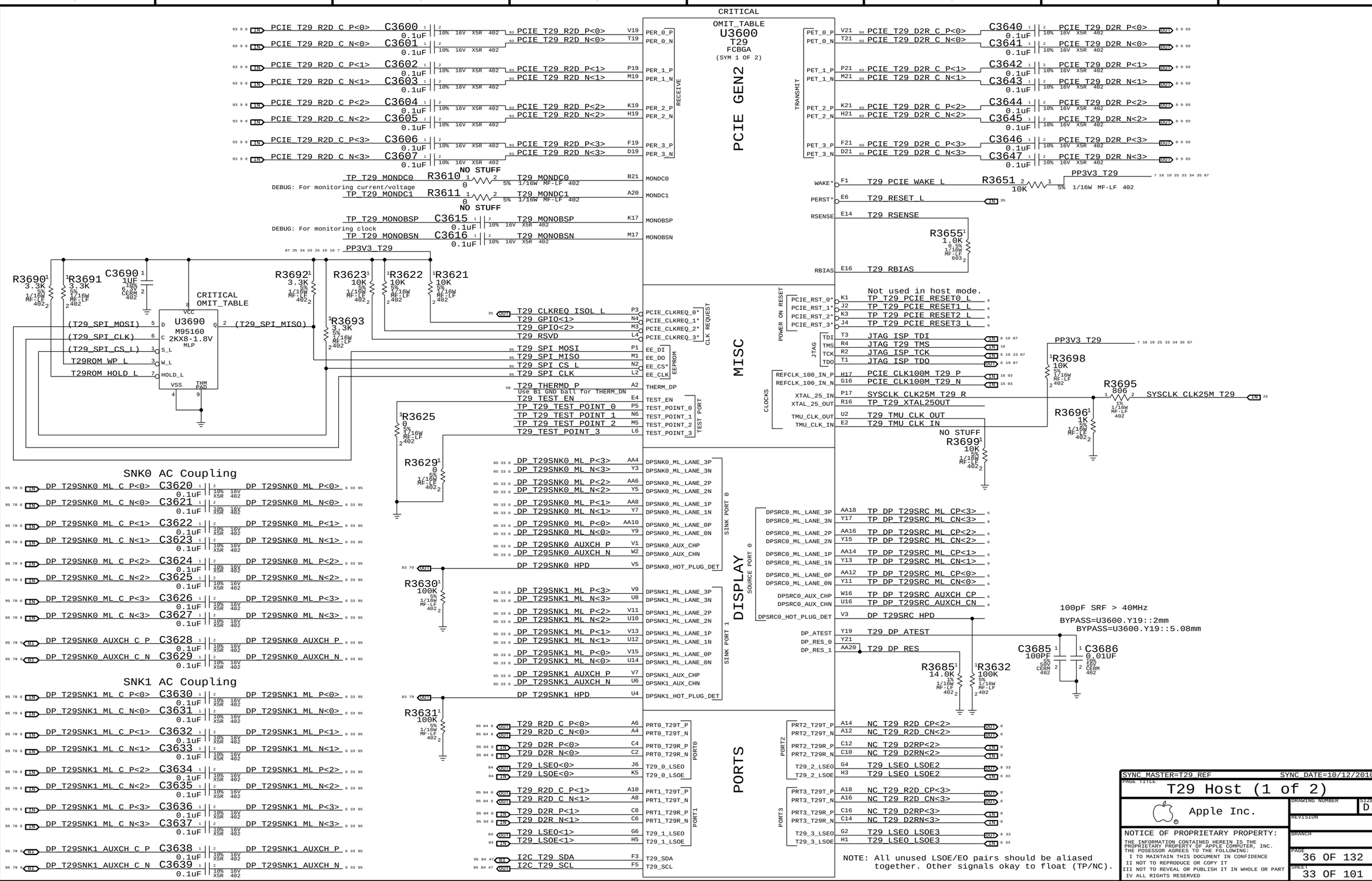
CRITICAL
OMIT_TABLE
U3600
T29
FCBGA
(SYM 1 OF 2)
PCIE GEN2
RECEIVE
TRANSMIT
PCIE T29 R2D C P<0>
PCIE T29 R2D C N<0>
PCIE T29 R2D C P<1>
PCIE T29 R2D C N<1>
PCIE T29 R2D C P<2>
PCIE T29 R2D C N<2>
PCIE T29 R2D C P<3>
PCIE T29 R2D C N<3>
PCIE T29 R2D P<0>
PCIE T29 R2D N<0>
PCIE T29 R2D P<1>
PCIE T29 R2D N<1>
PCIE T29 R2D P<2>
PCIE T29 R2D N<2>
PCIE T29 R2D P<3>
PCIE T29 R2D N<3>
PCIE T29 D2R C P<0>
PCIE T29 D2R C N<0>
PCIE T29 D2R C P<1>
PCIE T29 D2R C N<1>
PCIE T29 D2R C P<2>
PCIE T29 D2R C N<2>
PCIE T29 D2R C P<3>
PCIE T29 D2R C N<3>
PCIE T29 D2R P<0>
PCIE T29 D2R N<0>
PCIE T29 D2R P<1>
PCIE T29 D2R N<1>
PCIE T29 D2R P<2>
PCIE T29 D2R N<2>
PCIE T29 D2R P<3>
PCIE T29 D2R N<3>
NO STUFF
R3610
R3611
TP T29 MONDC0
TP T29 MONDC1
T29 MONDC0
T29 MONDC1
DEBUG: For monitoring current/voltage
TP T29 MONOBSP
TP T29 MONOBSN
T29 MONOBSP
T29 MONOBSN
DEBUG: For monitoring clock
PP3V3 T29
WAKE*
PERST*
RSENSE
RBIAS
T29 PCIE WAKE L
T29 RESET L
T29 RSENSE
T29 RBIAS
R3651
R3655
MISC
CLK REQUEST
EEPROM
TEST PORT
POWER ON RESET
JTAG
CLOCKS
Not used in host mode.
TP T29 PCIE RESET0 L
TP T29 PCIE RESET1 L
TP T29 PCIE RESET2 L
TP T29 PCIE RESET3 L
JTAG T29 TMS
JTAG T29 TDI
JTAG T29 TDO
JTAG ISP TCK
JTAG ISP TDI
JTAG ISP TDO
PCIE CLK100M T29 P
PCIE CLK100M T29 N
SYSCLK CLK25M T29 R
SYSCLK CLK25M T29
TP T29 XTAL25OUT
T29 TMU CLK OUT
T29 TMU CLK IN
R3698
R3695
R3696
R3699
T29 CLKREQ ISOL L
T29 GPIO<1>
T29 GPIO<2>
T29 RSVD
T29 SPI MOSI
T29 SPI MISO
T29 SPI CS L
T29 SPI CLK
T29 THERMD P
Use B1 GND ball for THERM_DN
T29 TEST EN
TP T29 TEST POINT 0
TP T29 TEST POINT 1
TP T29 TEST POINT 2
T29 TEST POINT 3
R3625
R3629
DP T29SNK0 ML P<3>
DP T29SNK0 ML N<3>
DP T29SNK0 ML P<2>
DP T29SNK0 ML N<2>
DP T29SNK0 ML P<1>
DP T29SNK0 ML N<1>
DP T29SNK0 ML P<0>
DP T29SNK0 ML N<0>
DP T29SNK0 AUXCH P
DP T29SNK0 AUXCH N
DP T29SNK0 HPD
R3630
DP T29SNK1 ML P<3>
DP T29SNK1 ML N<3>
DP T29SNK1 ML P<2>
DP T29SNK1 ML N<2>
DP T29SNK1 ML P<1>
DP T29SNK1 ML N<1>
DP T29SNK1 ML P<0>
DP T29SNK1 ML N<0>
DP T29SNK1 AUXCH P
DP T29SNK1 AUXCH N
DP T29SNK1 HPD
R3631
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
DISPLAY
TP DP T29SRC ML CP<3>
TP DP T29SRC ML CN<3>
TP DP T29SRC ML CP<2>
TP DP T29SRC ML CN<2>
TP DP T29SRC ML CP<1>
TP DP T29SRC ML CN<1>
TP DP T29SRC ML CP<0>
TP DP T29SRC ML CN<0>
TP DP T29SRC AUXCH CP
TP DP T29SRC AUXCH CN
T29 DP T29SRC HPD
100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm
T29 DP ATEST
T29 DP RES
R3685
R3632
C3685
C3686
PORT0
PORT1
PORT2
PORT3
PORTS
T29 R2D C P<0>
T29 R2D C N<0>
T29 R2D P<0>
T29 R2D N<0>
T29 LSEO<0>
T29 LSOE<0>
T29 R2D C P<1>
T29 R2D C N<1>
T29 R2D P<1>
T29 R2D N<1>
T29 LSEO<1>
T29 LSOE<1>
I2C T29 SDA
I2C T29 SCL
NC T29 R2D CP<2>
NC T29 R2D CN<2>
NC T29 D2RP<2>
NC T29 D2RN<2>
T29 LSEO LSOE2
T29 LSOE LSOE2
NC T29 R2D CP<3>
NC T29 R2D CN<3>
NC T29 D2RP<3>
NC T29 D2RN<3>
T29 LSEO LSOE3
T29 LSOE LSOE3
NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).
SNK0 AC Coupling
SNK1 AC Coupling
R3690
R3691
C3690
R3692
R3693
R3623
R3622
R3621
CRITICAL
OMIT_TABLE
U3690
M95160
2KX8-1.8V
MLP
(T29_SPI_MOSI)
(T29_SPI_CLK)
(T29_SPI_CS_L)
T29ROM_WP_L
T29ROM_HOLD_L
(T29_SPI_MISO)
SYNC_MASTER=T29_REF
SYNC_DATE=10/12/2010
PAGE TITLE
T29 Host (1 of 2)
Apple Inc.
DRAWING NUMBER
SIZE
D
REVISION
BRANCH
PAGE
36 OF 132
SHEET
33 OF 101
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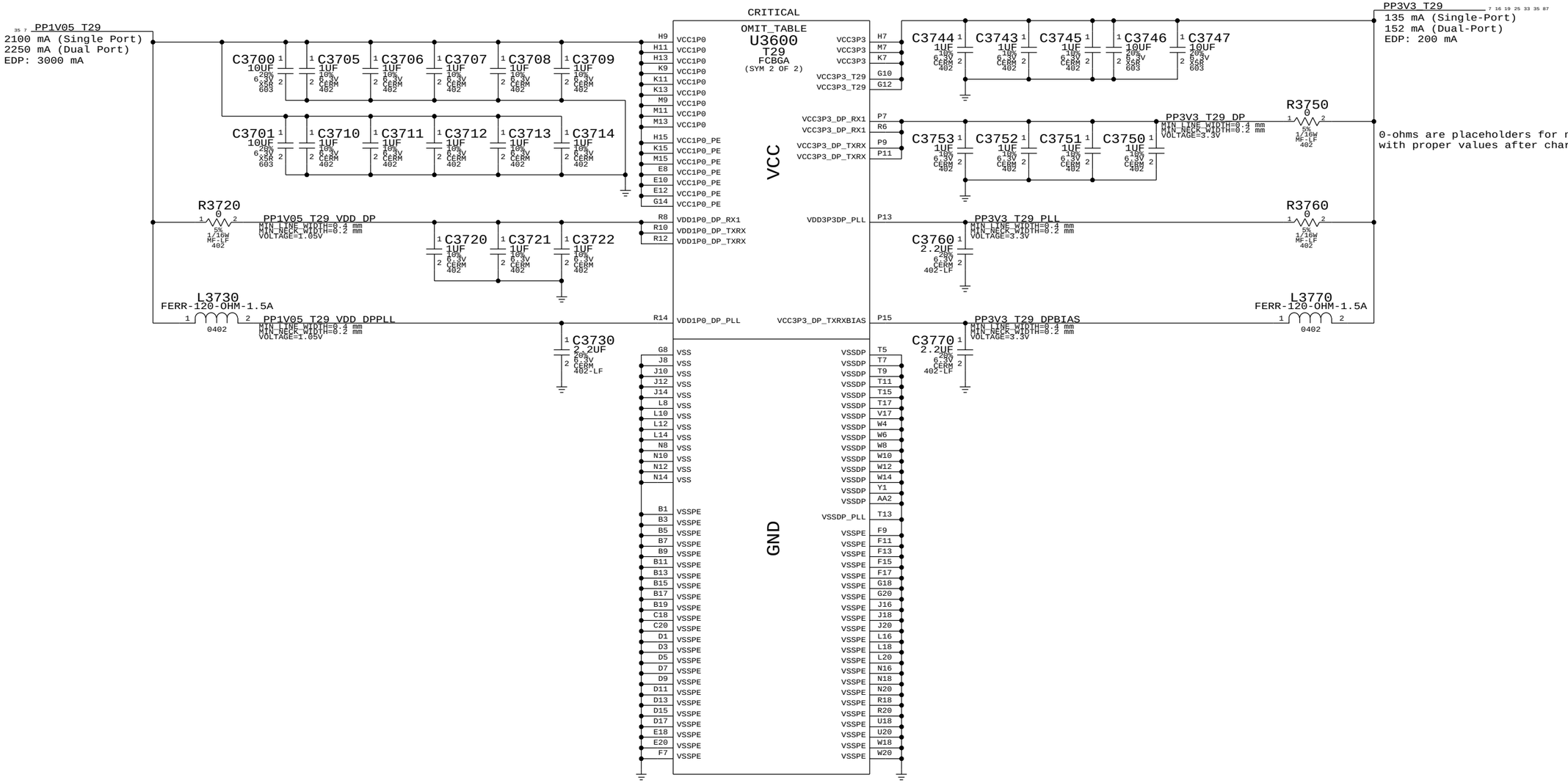

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_REF SYNC_DATE=10/12/2010

PAGE TITLE: T29 Host (2 of 2)

Apple Inc.

DRAWING NUMBER | SIZE: D

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

T29 15V Boost Regulator

PPBUS_G3H
8-13V Input
Changes required for 2S.

CRITICAL T29BST:Y Q3880 SI8409DB 8A

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_T29BST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

CRITICAL T29BST:Y L3895 10UH-4A-68-MOHM PCMB063T-100MS

T29BST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL T29BST:Y U3890 LT3957 QFN

T29BST_SNS1
T29BST_SNS2
T29BST_VSNS
T29BST_INTVCC
T29BST_VC
T29BST_RT
T29BST_SS
T29BST_VC_RC
T29BST_FBX
T29BST_EN_UVLO
GND_T29BST_SGND
SGND
GND

CRITICAL T29BST:Y D3895 POWERDI-123 DFLS230L

XW3895 SM PLACE_NEAR=C3895.1:2 mm

PP15V_T29
Vout = 15V
Max Current = 0.8A
Freq = 300KHz

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

Supervisor & CLKREQ# Isolation

PP3V3_S0

Platform (PCIe) Reset
PLT_RST_BUF_L

CRITICAL U3800 SLG4AP016V TDFN

PP3V3_T29
PP1V05_T29
T29_RESET_L
DLY = 60 ms +/- 20%
T29_CLKREQ_ISOL_L
MAKE_BASE=TRUE

Open-Drain GPIO
T29_SW_RESET_L

T29_CLKREQ_L
Pull-up provided by SB page.

3.3V T29 Switch

U3810 TPS22924 CSP CRITICAL

PP3V3_S0
PP3V3_T29
Max Current = 1.7A (85C)

U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch

U3815 TPS22924 CSP CRITICAL

PP1V05_S0
PP1V05_T29
Max Current = 3.4A (85C)

U3816 TPS22924 CSP CRITICAL

T29_PWR_EN
Pull-up provided by SB page.

U3816.A2: PLACE_NEAR=U3815.B2:3 mm

SYNC_MASTER=T29_REF	SYNC_DATE=10/12/2010
PAGE_TITLE: T29 Power Support	
Apple Inc.	DRAWING_NUMBER: D; SIZE: D
	REVISION:
	BRANCH:
	PAGE: 38 OF 132
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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT_REG

CRITICAL L3900 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_XTALVDDH — C3900 0.1UF
CRITICAL L3905 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_BIASVDDH — C3905 0.1UF
CRITICAL L3910 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_AVDDH — R3910 4.7K, C3910 0.1UF, C3911 0.1UF

R3940 4.7K, R3941 4.7K
C3915 4.7UF, C3916 0.1UF

ENET_SR_LX
PP1V2_ENET

Internal 1.2V Switching Regulator pins.

CRITICAL L3920 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_AVDDL — C3921 0.1UF, C3920 4.7UF
CRITICAL L3925 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_PCIEPLL — C3926 0.1UF, C3925 4.7UF
CRITICAL L3930 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_GPHYPLL — C3931 0.1UF, C3930 4.7UF
C3936 0.1UF, CRITICAL C3935 10UF

PP1V2_ENET
???mA (1000base-T, Caesar V)

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

PP3V3_S0
R3942 1K Current Limiting Resistor
C3950 0.1uF, C3951 0.1uF, C3955 0.1uF, C3956 0.1uF, R3943 0

OMIT
U3900
BCM57765B0
QFN-8X8

PCIE_ENET_D2R_N	58 VMAIN_PRSNT(IPD)	ENET_VMAIN_PRSNT
PCIE_ENET_D2R_P	27 PCIE_TXD_N	PCIE_ENET_D2R_C_N
PCIE_ENET_R2D_C_P	28 PCIE_TXD_P	PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_C_N	33 PCIE_RXD_P	PCIE_ENET_R2D_P
ENET_WAKE_L (See note)	34 PCIE_RXD_N	PCIE_ENET_R2D_N
	31 PCIE_REFCLK_P	PCIE_CLK100M_ENET_P
	30 PCIE_REFCLK_N	PCIE_CLK100M_ENET_N
	11 PERST* (IPD)	ENET_RESET_L
	12 CLKREQ* (OD)	ENET_CLKREQ_L
	3 WAKE* (OD)	ENET_WAKE_R_L
	4 LOW_PWR (IPD)	ENET_LOW_PWR
	6 SMB_CLK	BCM57765_SMB_CLK
	10 SMD_DATA (IPD)	BCM57765_SMB_DATA
	66 SCLK	BCM57765_SCLK
	64 SI/LINKLED*	BCM57765_MISO
	65 SO	BCM57765_MOSI
	63 CS*	BCM57765_CS_L
	2 SPD100LED*/SERIAL_DO (OD)	TP_BCM57765_SPD100LED_L
	67 TRAFFICLED*/SERIAL_DI (OD)	TP_BCM57765_TRAFFICLED_L
	18 XTALI	SYSCLK_CLK25M_ENET
	19 XTALO	NC
	38 RDAC	BCM57765_RDAC
	69 THRM_PAD	

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

R3965 1.24K

TRD0_P	40	ENET_MDI_P<0>
TRD0_N	41	ENET_MDI_N<0>
TRD1_P	44	ENET_MDI_P<1>
TRD1_N	43	ENET_MDI_N<1>
TRD2_P	46	ENET_MDI_P<2>
TRD2_N	47	ENET_MDI_N<2>
TRD3_P	50	ENET_MDI_P<3>
TRD3_N	49	ENET_MDI_N<3>
GPIO_0	5	NC
GPIO_1/CR_BUS_PWR	8	
RE*/GPIO_2	9	ENET_MEDIA_SENSE
(IPU) DETECT/WE*	1	SDCONN_DETECT_L
(IPU) CR_CMD/CLE	26	SDCONN_CMD
CR_CLK/RY_BY*	21	SDCONN_CLK
CR_DATA0	25	SDCONN_DATA<0>
CR_DATA1	24	SDCONN_DATA<1>
CR_DATA2	23	SDCONN_DATA<2>
CR_DATA3	22	SDCONN_DATA<3>
CR_DATA4	52	SDCONN_DATA<4>
CR_DATA5	53	SDCONN_DATA<5>
CR_DATA6	54	SDCONN_DATA<6>
CR_DATA7	55	SDCONN_DATA<7>
CE*/MS_INS*	59	TP_CE_L_MS_INS_L
CR_LED/ALE	60	ENET_CR_PWREN
CR_WP*/XD_WP*	57	SDCONN_WP
XD_DETECT	68	BDM57765_SR_DISABLE

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

R3980 1K 5% 1/16W MF-LF 402

BCM57765 supports both active-levels for WP.

SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.

PP3V3R1V8_ENET_LR_OUT_REG
PP3V3R1V8_ENET_LR_OUT_REG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C3970 4.7UF, C3971 0.1UF, C3972 0.1UF

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)

PP3V3_ENET
C3990 0.1UF
U3990 AT45DB011D SOIC-8S1 OMIT
BCM57765_SCLK, BCM57765_CS_L, BCM57765_MOSI, BCM57765_MISO
NOSTUFF R3990 4.7K, R3997 4.7K

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K91_ERIC SYNC_DATE=10/11/2010
PAGE TITLE
ETHERNET PHY (CAESAR IV)

Apple Inc.

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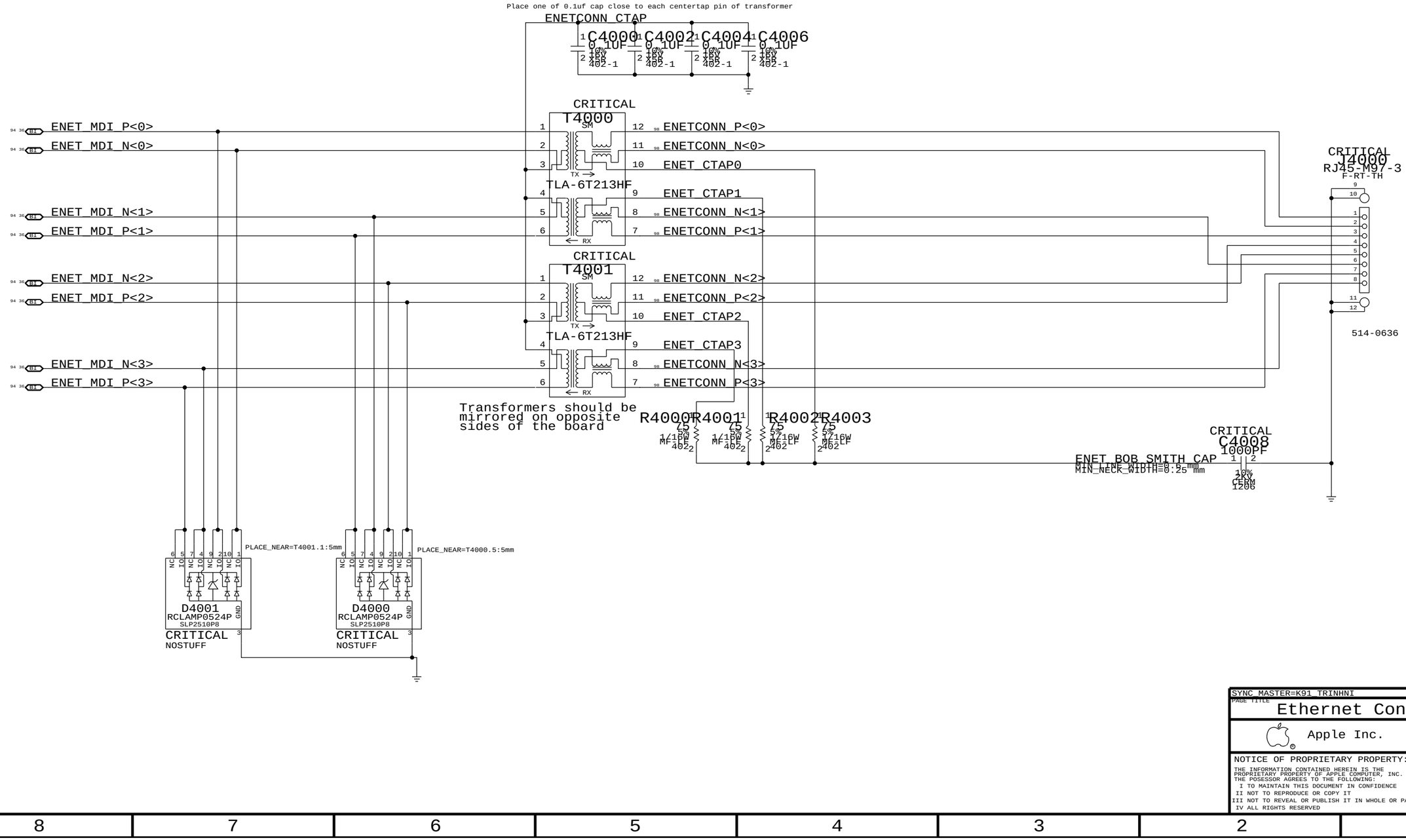
Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K91_TRINHNI SYNC_DATE=05/26/2010

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER | SIZE: D

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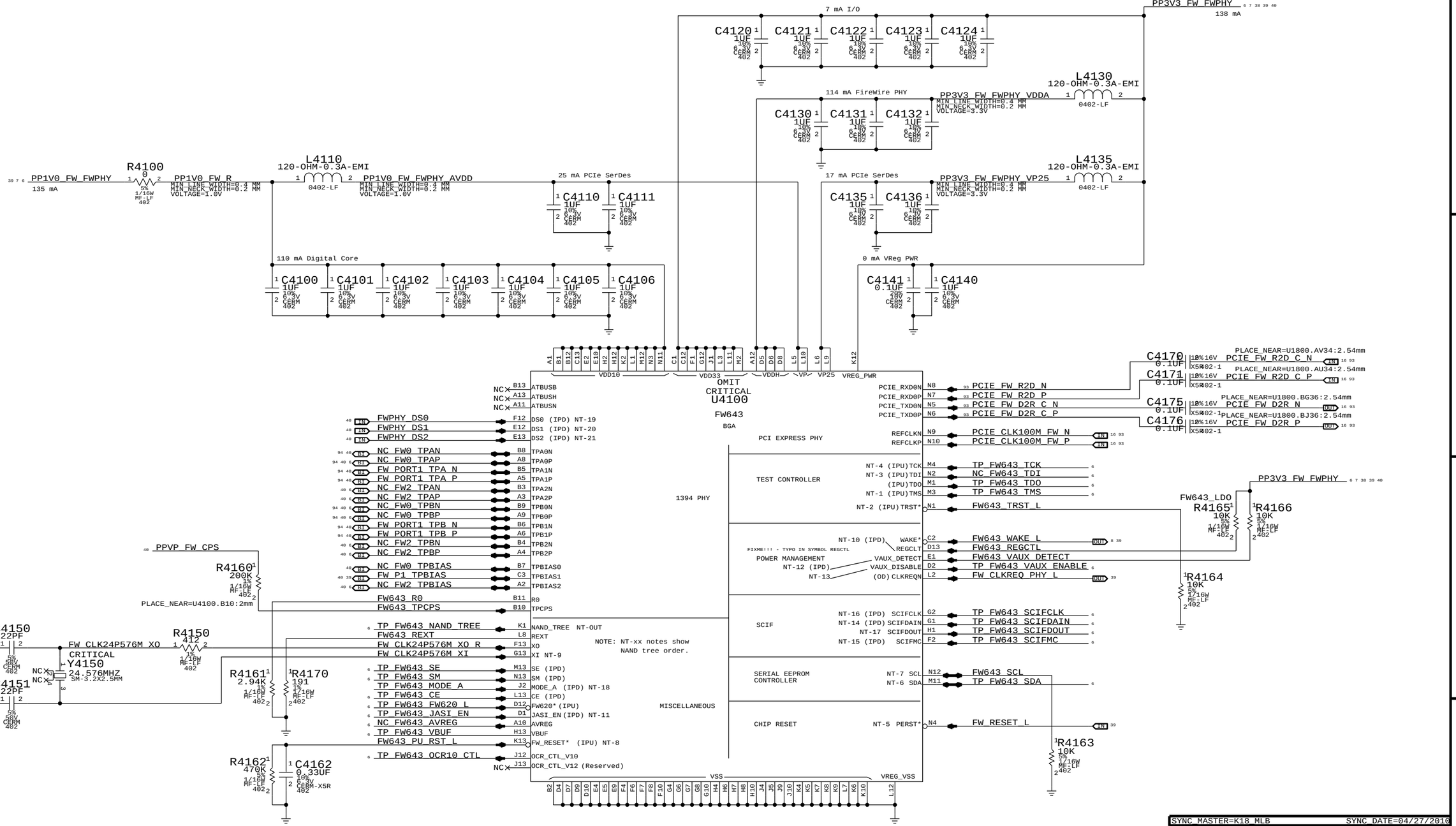
PAGE: 40 OF 132

SHEET: 37 OF 101


PP1V0_FW_FWPHY
135 mA
R4100 0 5% 1/10W MF-LF 402
PP1V0_FW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
L4110 120-OHM-0.3A-EMI 0402-LF
PP1V0_FW_FWPHY_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
25 mA PCIe SerDes
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402
110 mA Digital Core
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402
7 mA I/O
C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402
PP3V3_FW_FWPHY
138 mA
L4130 120-OHM-0.3A-EMI 0402-LF
114 mA FireWire PHY
PP3V3_FW_FWPHY_VDDA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402
L4135 120-OHM-0.3A-EMI 0402-LF
17 mA PCIe SerDes
PP3V3_FW_FWPHY_VP25
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402
0 mA VReg PWR
C4141 0.1UF 20% 16V CERM 402
C4140 1UF 10% 6.3V CERM 402
VDD10
VDD33
VDDH
VP
VP25
VREG_PWR
OMIT CRITICAL
U4100
FW643
BGA
ATBUSB
ATBUSH
ATBUSN
FWPHY_DS0
FWPHY_DS1
FWPHY_DS2
DS0 (IPD) NT-19
DS1 (IPD) NT-20
DS2 (IPD) NT-21
NC_FW0_TPAN
NC_FW0_TPAP
FW_PORT1_TPA_N
FW_PORT1_TPA_P
NC_FW2_TPAN
NC_FW2_TPAP
NC_FW0_TPBN
NC_FW0_TPBP
FW_PORT1_TPB_N
FW_PORT1_TPB_P
NC_FW2_TPBN
NC_FW2_TPBP
TPA0N
TPA0P
TPA1N
TPA1P
TPA2N
TPA2P
TPB0N
TPB0P
TPB1N
TPB1P
TPB2N
TPB2P
PCI EXPRESS PHY
PCIE_RXD0N
PCIE_RXD0P
PCIE_TXD0N
PCIE_TXD0P
PCIE_FW_R2D_N
PCIE_FW_R2D_P
PCIE_FW_D2R_C_N
PCIE_FW_D2R_C_P
C4170 0.1UF 10% 16V X5R 402-1
C4171 0.1UF 10% 16V X5R 402-1
C4175 0.1UF 10% 16V X5R 402-1
C4176 0.1UF 10% 16V X5R 402-1
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
PCIE_FW_D2R_N
PCIE_FW_D2R_P
PLACE_NEAR=U1800.AV34:2.54mm
PLACE_NEAR=U1800.AU34:2.54mm
PLACE_NEAR=U1800.BG36:2.54mm
PLACE_NEAR=U1800.BJ36:2.54mm
REFCLKN
REFCLKP
PCIE_CLK100M_FW_N
PCIE_CLK100M_FW_P
1394 PHY
TEST CONTROLLER
NT-4 (IPU) TCK
NT-3 (IPU) TDI
(IPU) TDO
NT-1 (IPU) TMS
NT-2 (IPU) TRST*
TP_FW643_TCK
NC_FW643_TDI
TP_FW643_TDO
TP_FW643_TMS
FW643_TRST_L
POWER MANAGEMENT
FIXME!!! - TYPO IN SYMBOL REGCTL
NT-10 (IPD) WAKE*
REGCLT
VAUX_DETECT
VAUX_DISABLE
(OD) CLKREQN
NT-12 (IPD)
NT-13
FW643_WAKE_L
FW643_REGCTL
FW643_VAUX_DETECT
TP_FW643_VAUX_ENABLE
FW_CLKREQ_PHY_L
SCIF
NT-16 (IPD) SCIFCLK
NT-14 (IPD) SCIFDAIN
NT-17 SCIFDOUT
NT-15 (IPD) SCIFMC
TP_FW643_SCIFCLK
TP_FW643_SCIFDAIN
TP_FW643_SCIFDOUT
TP_FW643_SCIFMC
SERIAL EEPROM CONTROLLER
NT-7 SCL
NT-6 SDA
FW643_SCL
TP_FW643_SDA
CHIP RESET
NT-5 PERST*
FW_RESET_L
FW643_LDO
R4165 10K 5% 1/16W MF-LF 402
R4166 10K 5% 1/16W MF-LF 402
R4164 10K 5% 1/16W MF-LF 402
R4163 10K 5% 1/16W MF-LF 402
PP3V3_FW_FWPHY
PPVP_FW_CPS
R4160 200K 1% 1/16W MF-LF 402
PLACE_NEAR=U4100.B10:2mm
C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO
CRITICAL
Y4150 24.576MHZ SM-3.2X2.5MM
R4150 412 1% 1/16W MF-LF 402
R4161 2.94K 1% 1/16W MF-LF 402
R4170 191 1% 1/16W MF-LF 402
R4162 470K 5% 1/16W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402
NAND_TREE NT-OUT
REXT
XO
XI NT-9
SE (IPD)
SM (IPD)
MODE_A (IPD) NT-18
CE (IPD)
FW620* (IPU)
JASI_EN (IPD) NT-11
AVREG
VBUF
FW_RESET* (IPU) NT-8
OCR_CTL_V10
OCR_CTL_V12 (Reserved)
TP_FW643_NAND_TREE
FW643_REXT
FW_CLK24P576M_XO_R
FW_CLK24P576M_XI
TP_FW643_SE
TP_FW643_SM
TP_FW643_MODE_A
TP_FW643_CE
TP_FW643_FW620_L
TP_FW643_JASI_EN
NC_FW643_AVREG
TP_FW643_VBUF
FW643_PU_RST_L
TP_FW643_OCR10_CTL
NOTE: NT-xx notes show NAND tree order.
MISCELLANEOUS
VSS
VREG_VSS
SYNC_MASTER=K18_MLB
SYNC_DATE=04/27/2010
PAGE TITLE
FireWire LLC/PHY (FW643)
Apple Inc.
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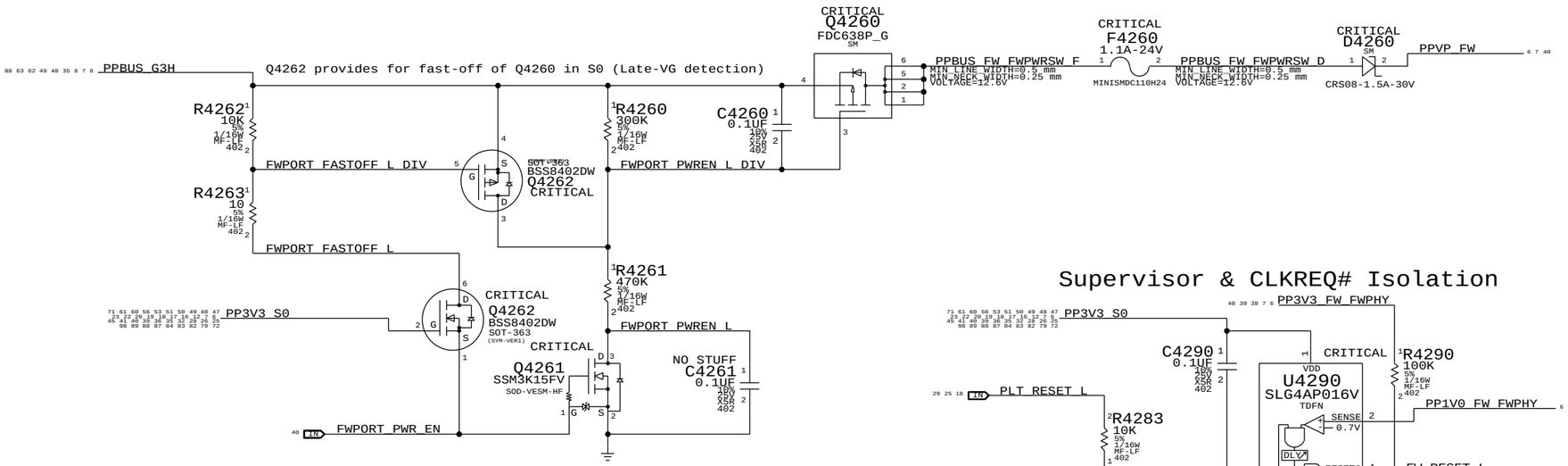
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

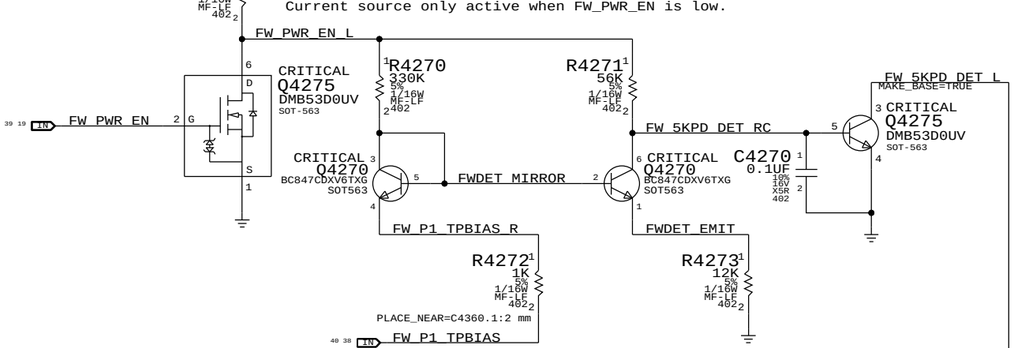
FireWire Port Power Switch



Supervisor & CLKREQ# Isolation

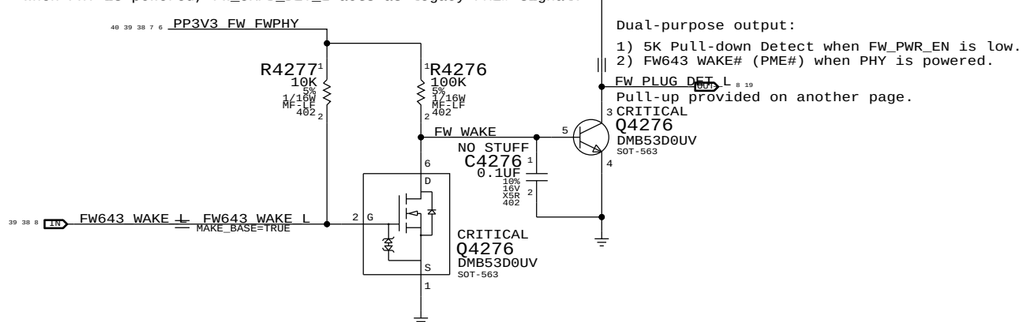
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.

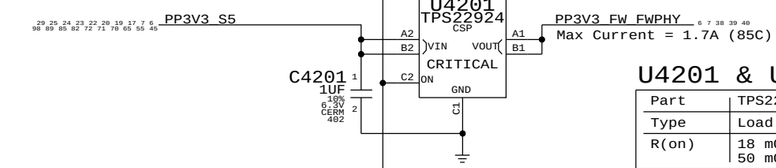


FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.



3.3V FW Switch

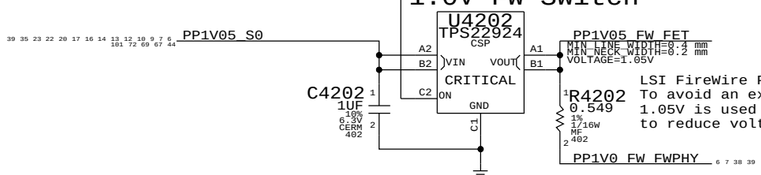


U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

SYNC_MASTER=T27_REF SYNC_DATE=06/10/2010

PAGE TITLE
FireWire Port & PHY Power

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

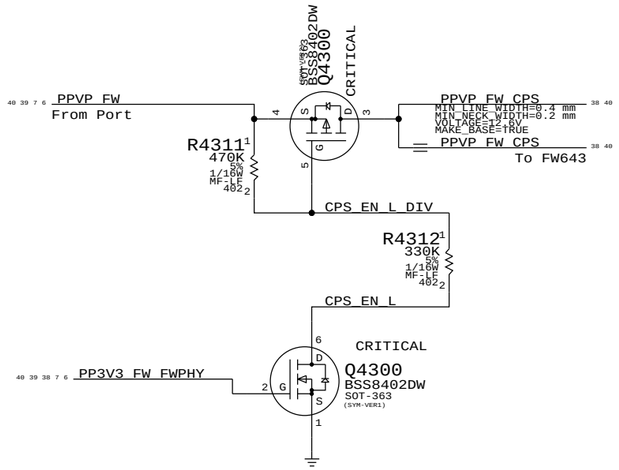
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

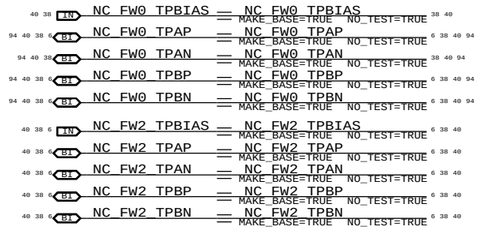
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



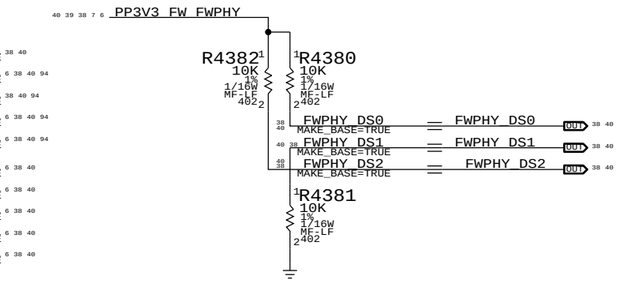
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



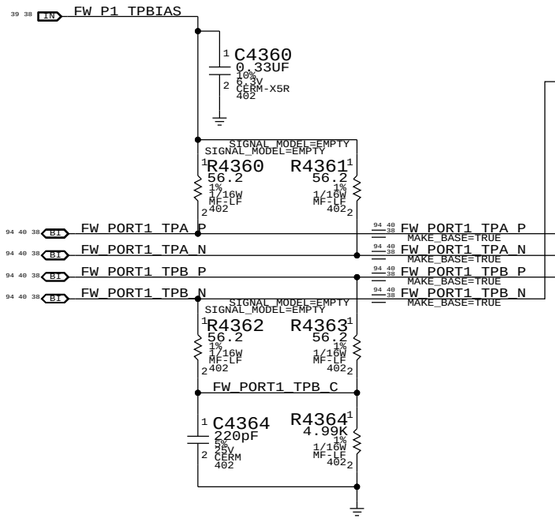
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

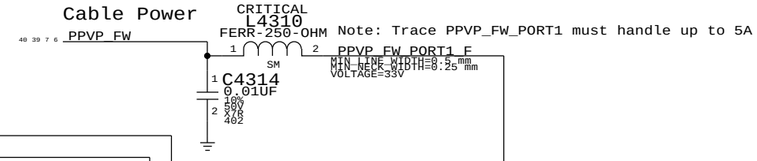


Termination

Place close to FireWire PHY

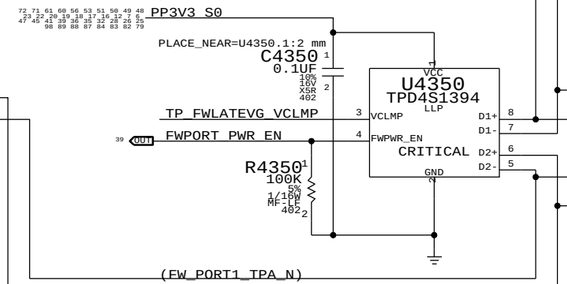


Cable Power



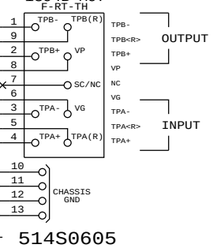
Note: Trace PPVP_FW_PORT1 must handle up to 5A

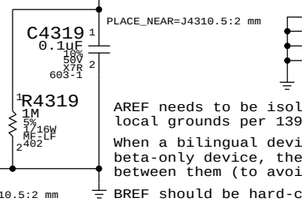
"Snapback" & "Late VG" Protection



PORT 1

BILINGUAL





AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

SYNC_MASTER=T27_REF SYNC_DATE=06/10/2010

PAGE TITLE: FireWire Connector

Apple Inc.

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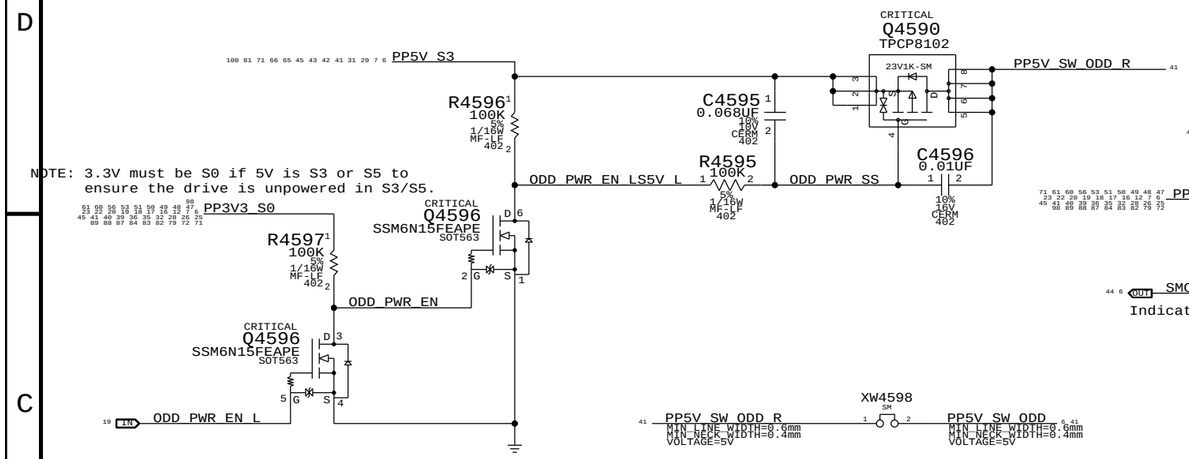
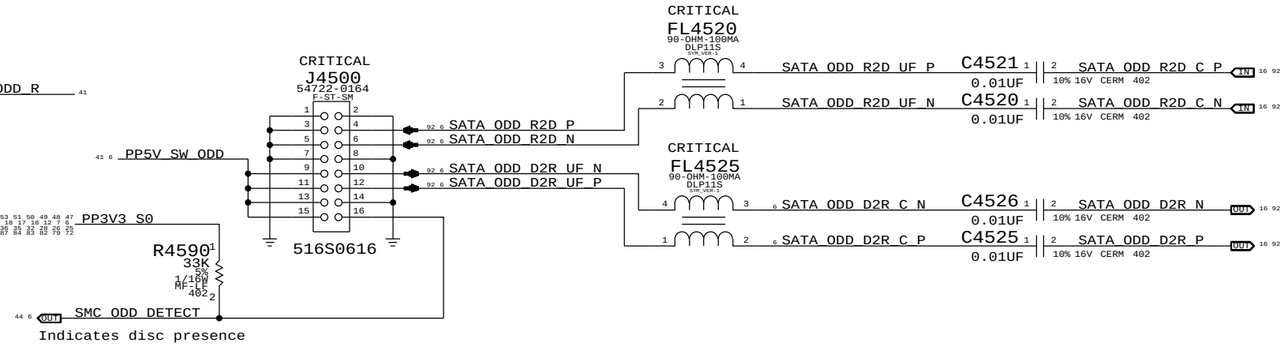
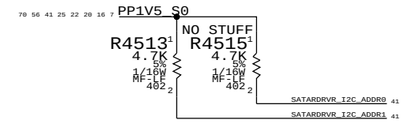
ODD Power Control



SATA ODD Connector

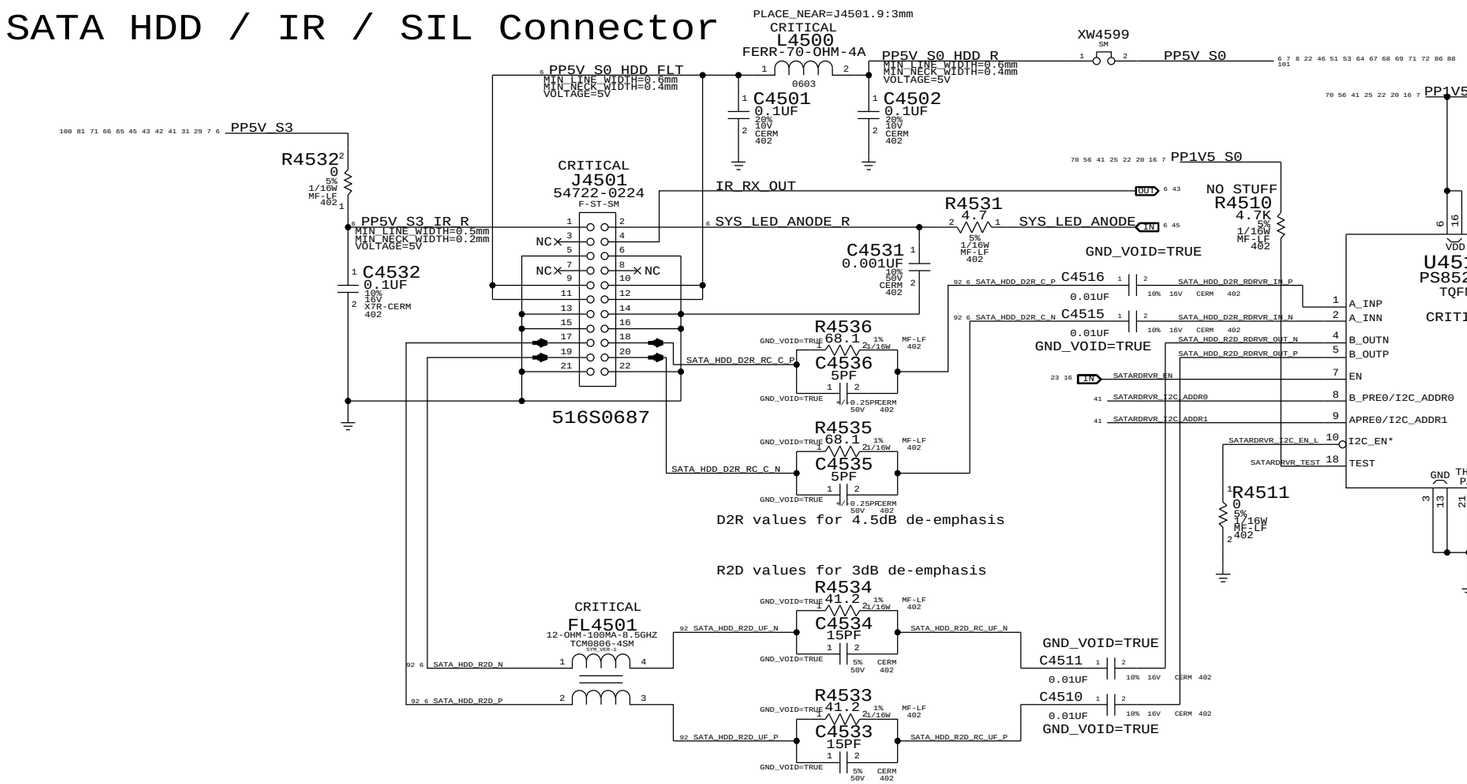




Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SATA HDD / IR / SIL Connector



SYNC_MASTER=K91_ERIC SYNC_DATE=11/08/2010

PAGE TITLE
SATA/IR/SIL Connectors

Apple Inc.

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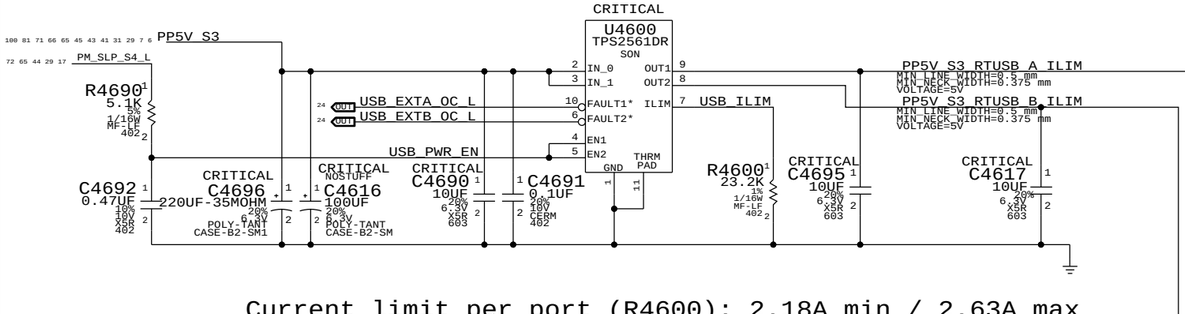
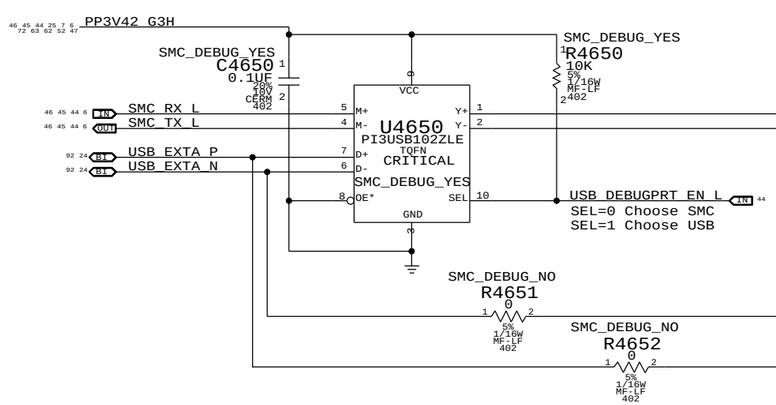
USB Port Power Switch

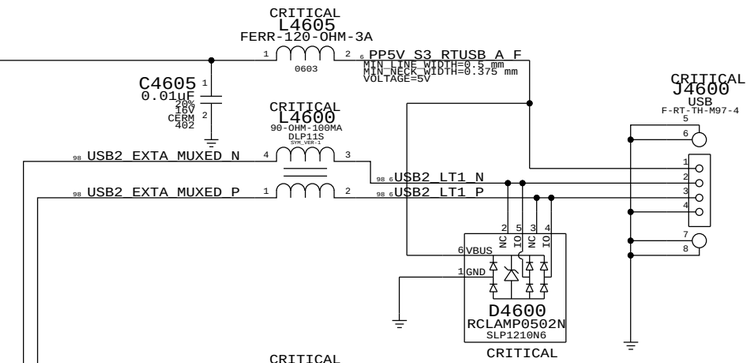


Current limit per port (R4600): 2.18A min / 2.63A max

USB/SMC Debug Mux

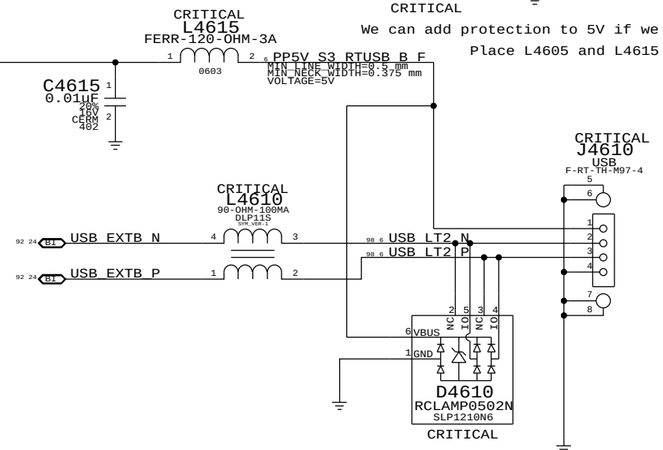


Left USB Port A



We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin



Left USB Port B

SYNC_MASTER=K91_ERIC	SYNC_DATE=10/08/2010
PAGE TITLE: External USB Connectors	
Apple Inc.	DRAWING NUMBER: D; SIZE: D
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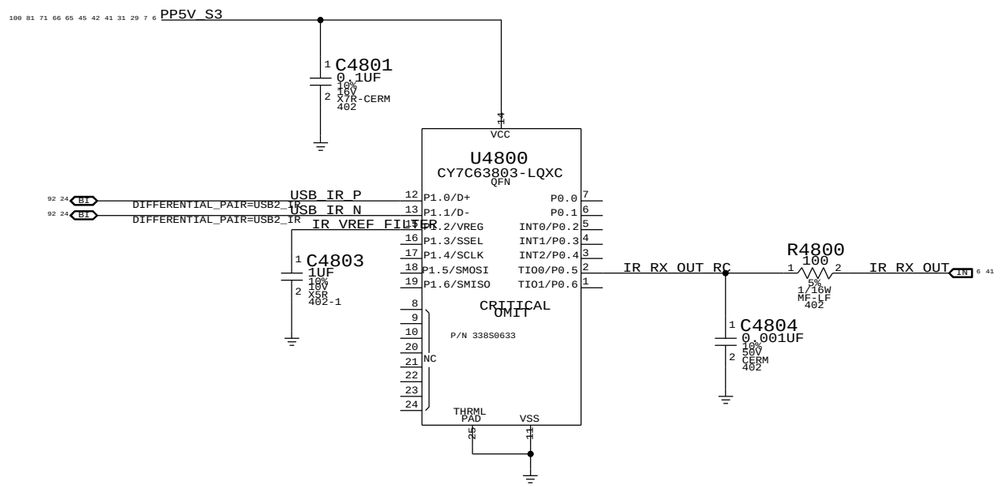
IR SUPPORT



SYNC_MASTER=K18_MLB	SYNC_DATE=04/27/2010
PAGE TITLE: Front Flex Support	
Apple Inc.	DRAWING NUMBER / SIZE: D
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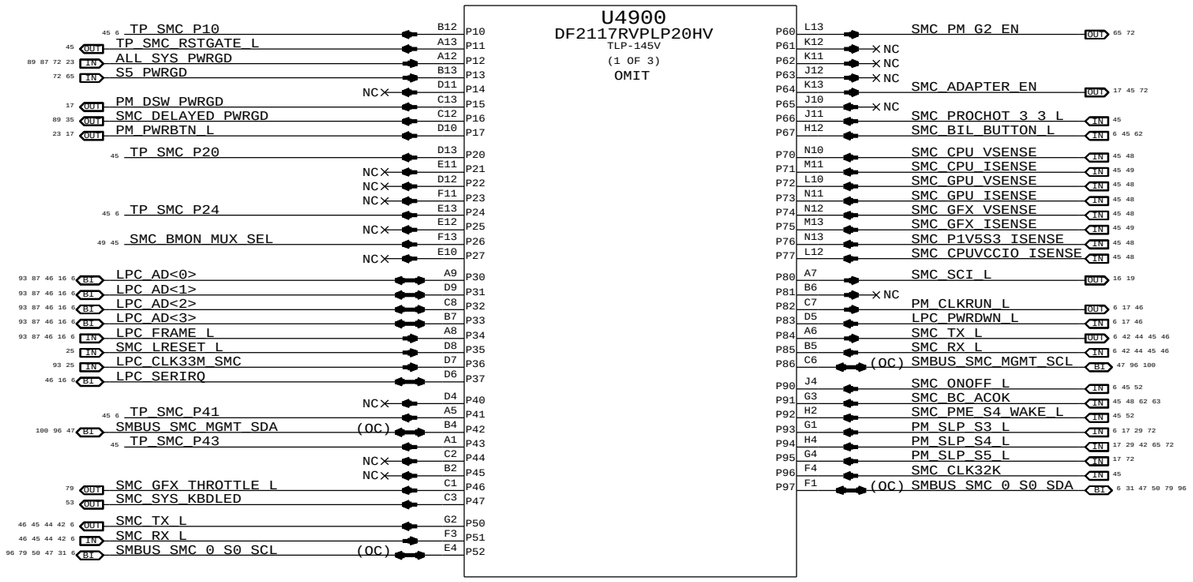
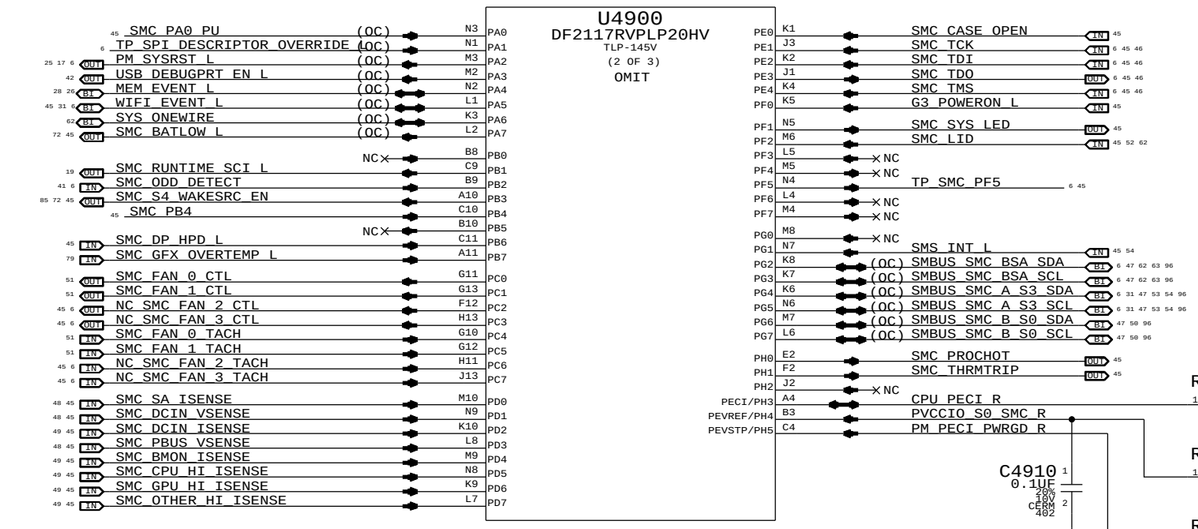
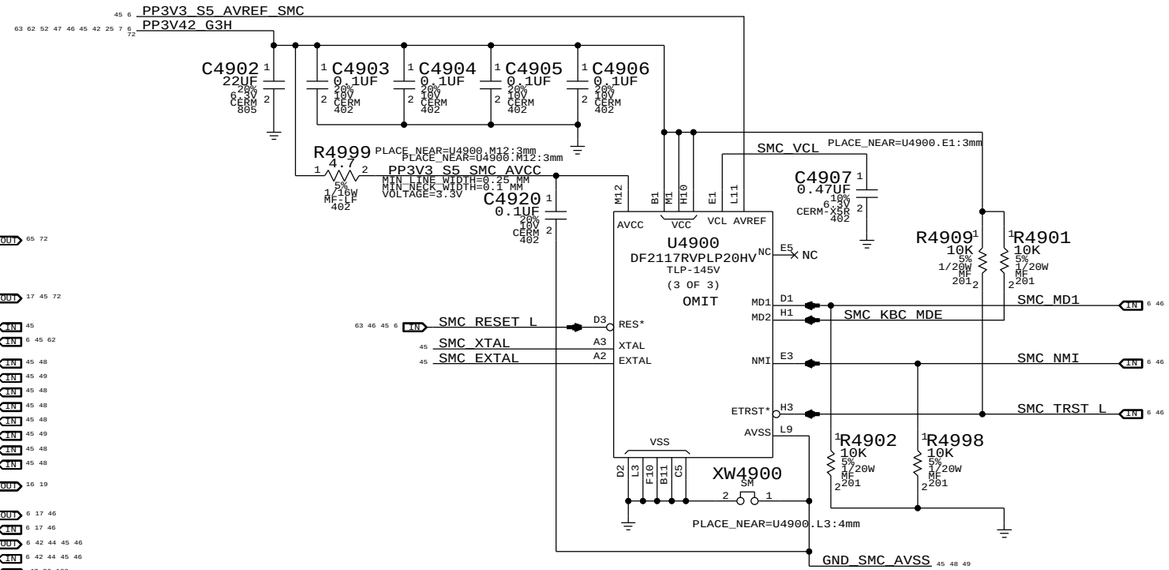
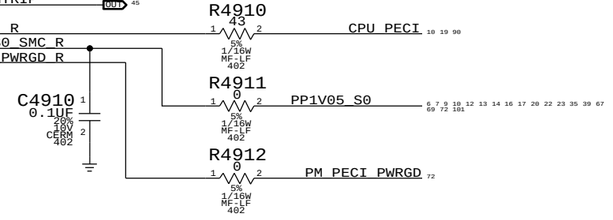
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.









NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

PAGE TITLE: SMC

Apple Inc.

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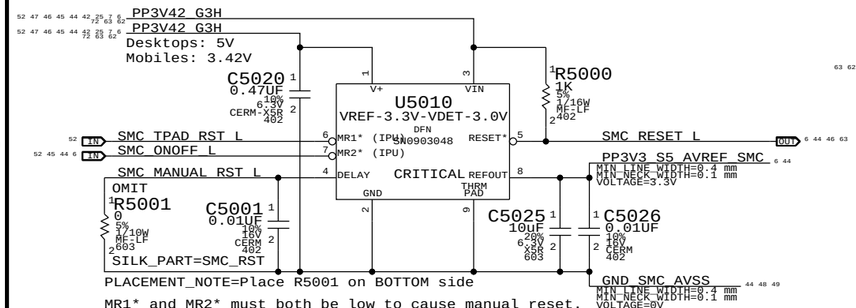
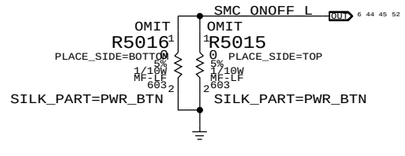
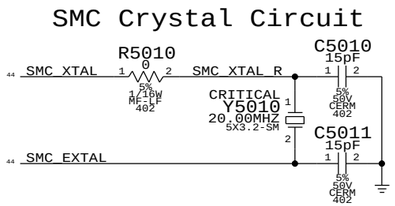
SMC Reset "Button", Supervisor & AVREF Supply



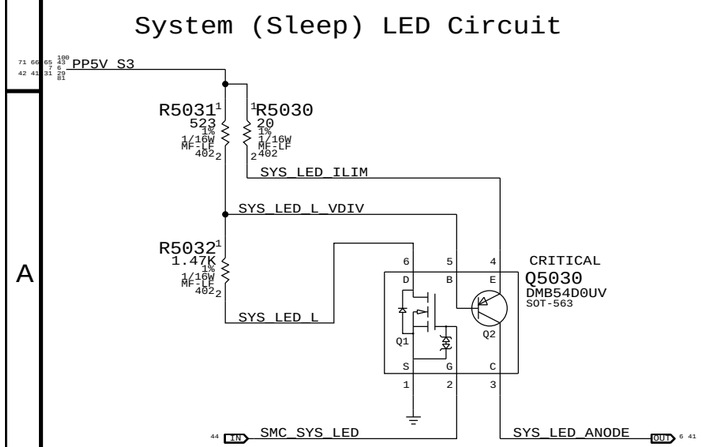
Debug Power "Buttons"



SMC Crystal Circuit



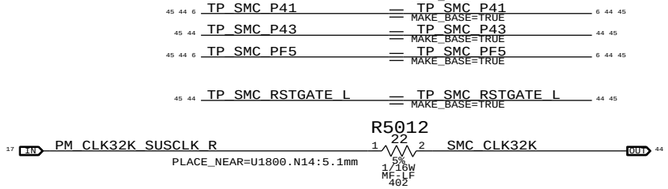
System (Sleep) LED Circuit

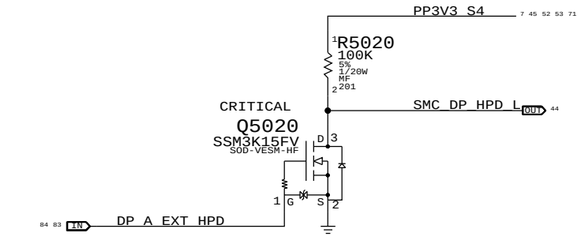


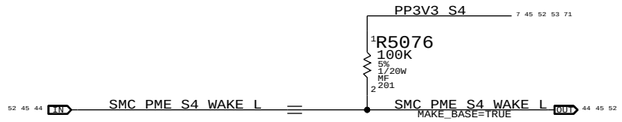
SMC Signal Connections

NC_SMC_FAN_2_CTL	=	NC_SMC_FAN_2_CTL
NC_SMC_FAN_2_TACH	=	NC_SMC_FAN_2_TACH
NC_SMC_FAN_3_CTL	=	NC_SMC_FAN_3_CTL
NC_SMC_FAN_3_TACH	=	NC_SMC_FAN_3_TACH
SMC_BC_ACOK	=	SMC_BC_ACOK
SMS_INT_L	=	SMS_INT_L
SMC_CPU_VSENSE	=	SMC_CPU_VSENSE
SMC_CPU_ISENSE	=	SMC_CPU_ISENSE
SMC_GPU_VSENSE	=	SMC_GPU_VSENSE
SMC_GPU_ISENSE	=	SMC_GPU_ISENSE
SMC_GFX_VSENSE	=	SMC_GFX_VSENSE
SMC_GFX_ISENSE	=	SMC_GFX_ISENSE
SMC_P1V5S3_ISENSE	=	SMC_P1V5S3_ISENSE
SMC_CPUVCCIO_ISENSE	=	SMC_CPUVCCIO_ISENSE
SMC_SA_ISENSE	=	SMC_SA_ISENSE
SMC_DCIN_VSENSE	=	SMC_DCIN_VSENSE
SMC_DCIN_ISENSE	=	SMC_DCIN_ISENSE
SMC_PBUS_VSENSE	=	SMC_PBUS_VSENSE
SMC_BMON_ISENSE	=	SMC_BMON_ISENSE
SMC_CPU_HI_ISENSE	=	SMC_CPU_HI_ISENSE
SMC_GPU_HI_ISENSE	=	SMC_GPU_HI_ISENSE
SMC_OTHER_HI_ISENSE	=	SMC_OTHER_HI_ISENSE
TP_SMC_P10	=	TP_SMC_P10
TP_SMC_P20	=	TP_SMC_P20
TP_SMC_P24	=	TP_SMC_P24
SMC_BMON_MUX_SEL	=	SMC_BMON_MUX_SEL
TP_SMC_P41	=	TP_SMC_P41
TP_SMC_P43	=	TP_SMC_P43
TP_SMC_PF5	=	TP_SMC_PF5
TP_SMC_RSTGATE_L	=	TP_SMC_RSTGATE_L

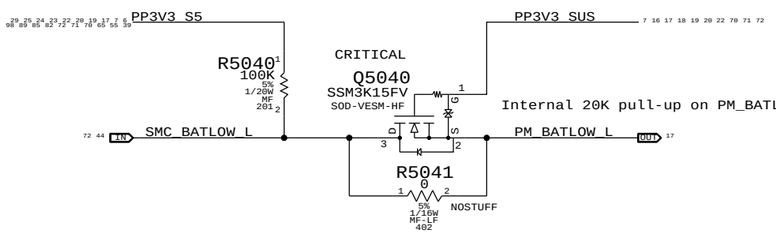
All: MAKE_BASE=TRUE



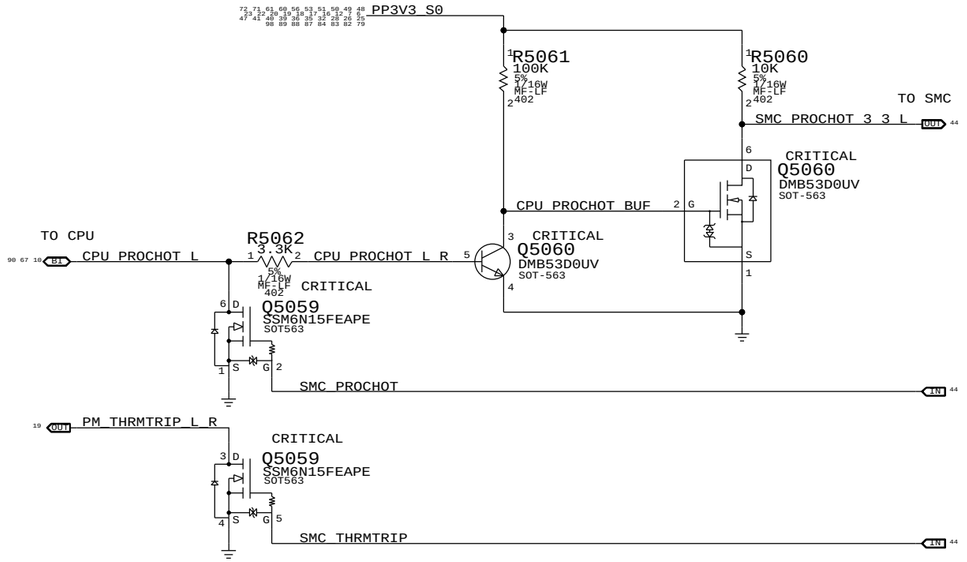




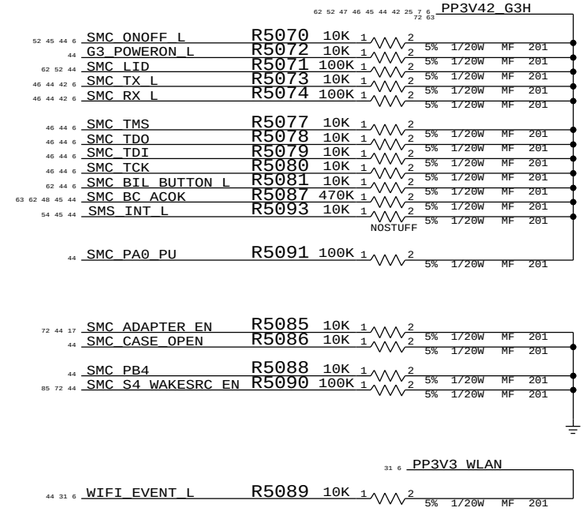
BATLOW# Isolation



SMC FSB to 3.3V Level Shifting



Pull-ups



SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: | SIZE: D

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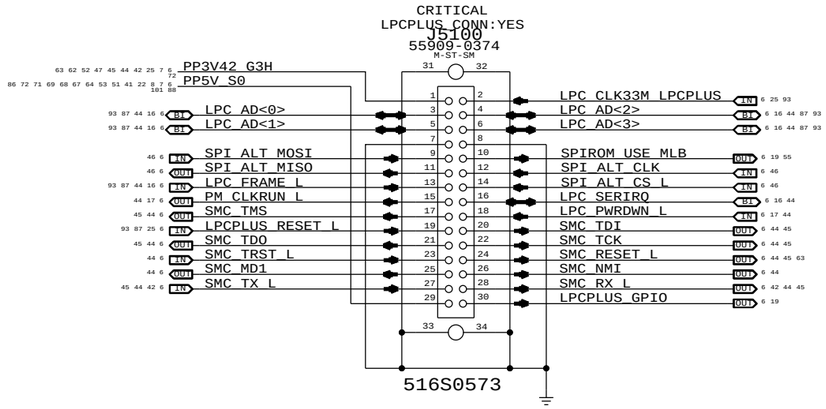
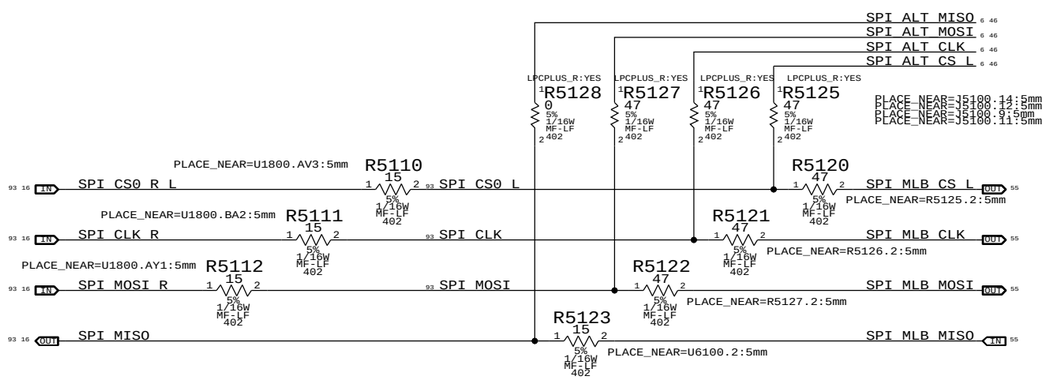
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: LPC+SPI Debug Connector

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PCH SMBus "0" Connections

PP3V3_S0

R5200 1K 5% 1/16W MF-LF 402
R5201 1K 5% 1/16W MF-LF 402

Cougar Point
U1800
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA
MAKE_BASE=TRUE

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

VRef DACs
U3300
(Write: 0x98 Read: 0x99)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SO-DIMM "B"
J3100
(Write: 0xA4 Read: 0xA5)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control
U3301
(Write: 0x30 Read: 0x31)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SATA Redriver
U4510
(Write: 0xB6 Read: 0xB7)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

LED BACKLIGHT
U9701
(WRITE: 0x58 READ: 0x59)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors
J2500 & J2550
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Mikey
U6880
(Write: 0x72 Read: 0x73)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SDRVI2C:SB
R5237 0 5% 1/16W MF-LF 402

SDRVI2C:SB
R5236 0 5% 1/16W MF-LF 402

DP SDRV "A"
U9310
(Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL
- I2C_DPSDRVA_SDA
MAKE_BASE=TRUE

PCH "SMLink 0" Connections

PP3V3_S0

R5210 8.2K 5% 1/16W MF-LF 402
R5211 8.2K 5% 1/16W MF-LF 402

Cougar Point
U1800
(MASTER)
- SML_PCH_0_CLK
- SML_PCH_0_DATA
MAKE_BASE=TRUE

PCH "SMLink 1" Connections

PP3V3_S0

NO STUFF
R5220 8.2K 5% 1/16W MF-LF 402

NO STUFF
R5221 8.2K 5% 1/16W MF-LF 402

R5223 0 5% 1/16W MF-LF 402

R5222 0 5% 1/16W MF-LF 402

Cougar Point
U1800
(Write: 0x88 Read: 0x89)
- SML_PCH_1_CLK
- SML_PCH_1_DATA
MAKE_BASE=TRUE

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

R5250 4.7K 5% 1/16W MF-LF 402

R5251 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

GPU Temp (Int)
Whistler: U8000
(Write: 0x82 Read: 0x83)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

X19
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

R5270 1K 5% 1/16W MF-LF 402

R5271 1K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA
MAKE_BASE=TRUE

Trackpad
J5800
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

J3401
ALS
(Write: 0x72 Read: 0x73)
Lid Angle Detect
(Write: 0x32 Read: 0x33)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

Digital SMS
LIS331DLH: U5920
(Write: 0x30 Read: 0x31)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMC "B" SMBus Connections

PP3V3_S0

R5260 4.7K 5% 1/16W MF-LF 402

R5261 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA
MAKE_BASE=TRUE

CPU Temp
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

T29 Temp
EMC1412-A: U5520
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

SMC "Battery A" SMBus Connections

PP3V42_G3H

R5280 2.0K 5% 1/16W MF-LF 402

R5281 2.0K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA
MAKE_BASE=TRUE

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery
J6955
(See Table)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x92 Read: 0x93)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S3

R5290 4.7K 5% 1/16W MF-LF 402

R5291 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA
MAKE_BASE=TRUE

Sensor ADC A
U5930
(Write: 0x10 Read: 0x11)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

T29 SMBus Connections

PP3V3_S0

R5230 4.7K 5% 1/16W MF-LF 402

R5231 4.7K 5% 1/16W MF-LF 402

T29 IC
U3600
(MASTER)
- I2C_T29_SCL
- I2C_T29_SDA
MAKE_BASE=TRUE

T29 Port A MCU
J9330
(Write: 0x26 Read: 0x27)
- I2C_T29_SCL
- I2C_T29_SDA

SDRVI2C:MCU
R5234 0 5% 1/16W MF-LF 402

SDRVI2C:MCU
R5235 0 5% 1/16W MF-LF 402

DP SDRV "A"
U9310
(Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL
- I2C_DPSDRVA_SDA
MAKE_BASE=TRUE

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE
SMBus Connections

Apple Inc.

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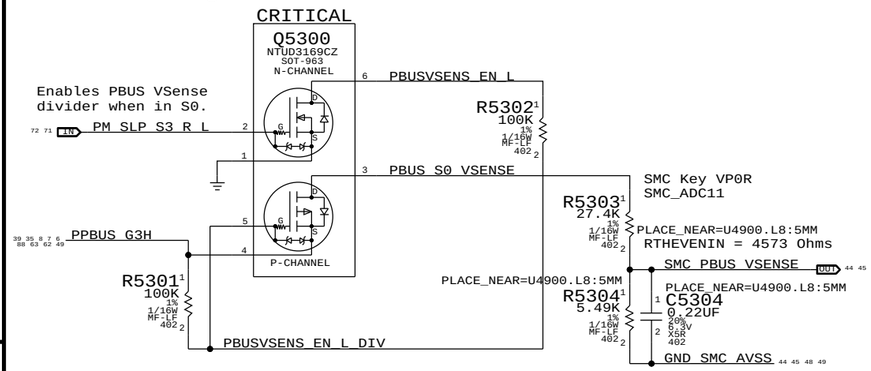
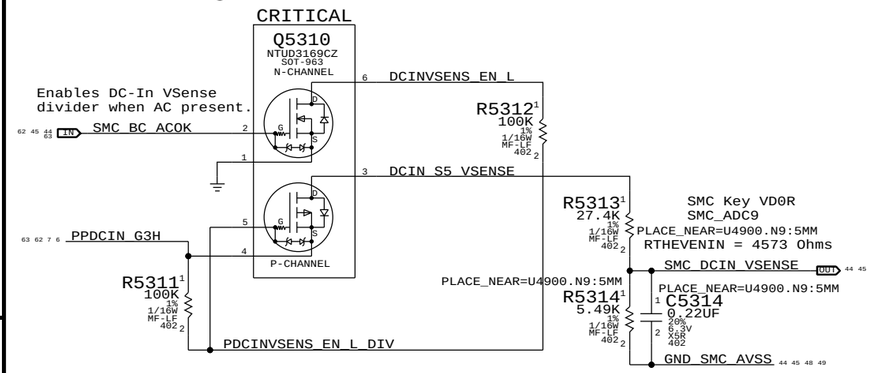
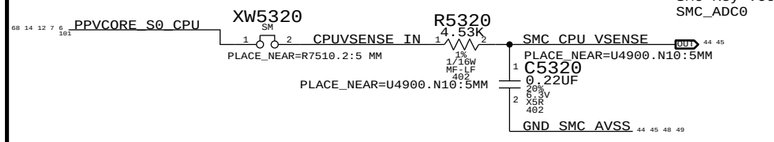
PBUS Voltage Sense Enable & Filter



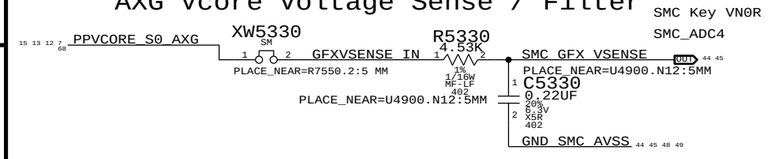
DC-In Voltage Sense Enable & Filter



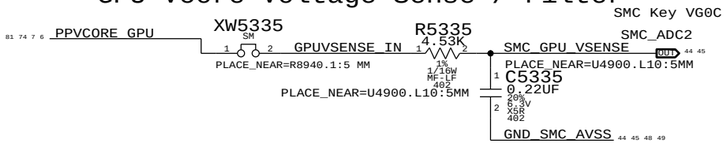
CPU Vcore Voltage Sense / Filter



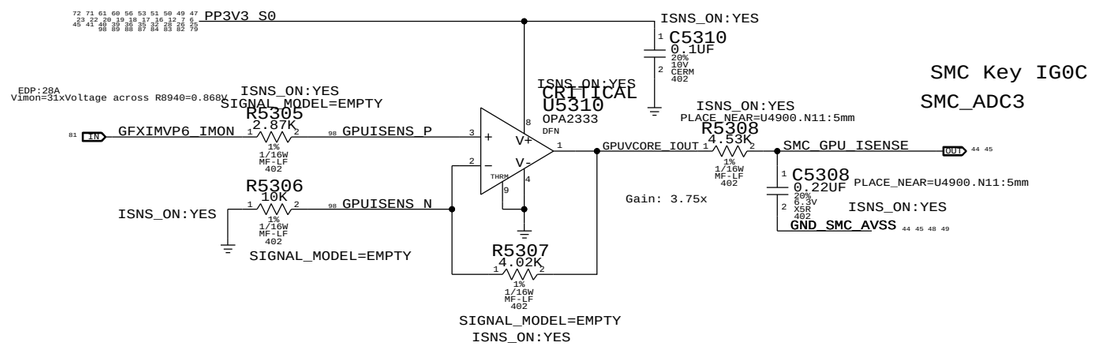
AXG Vcore Voltage Sense / Filter



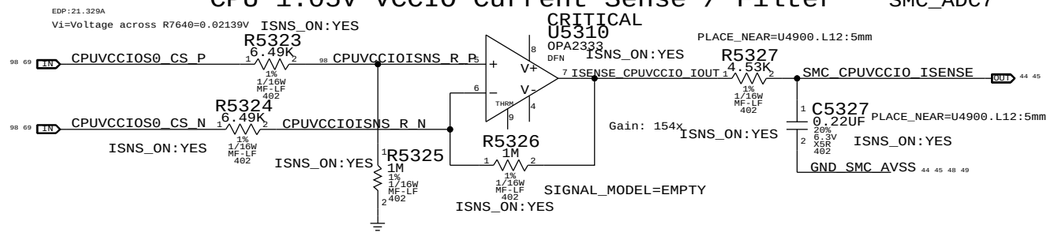
GPU Vcore Voltage Sense / Filter



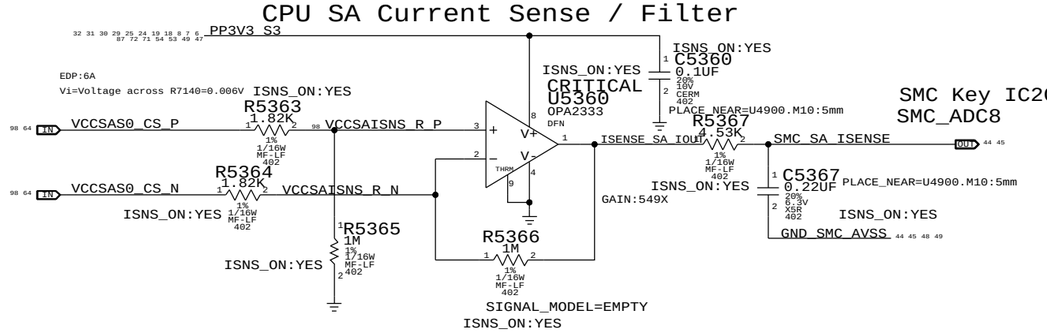
GPU VCore Load Side Current Sense / Filter



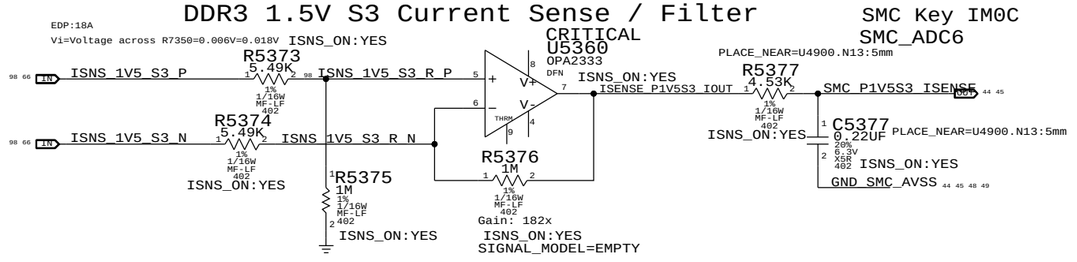
CPU 1.05V VCCIO Current Sense / Filter



CPU SA Current Sense / Filter



DDR3 1.5V S3 Current Sense / Filter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	4	RES, 00HM, 0402	C5308,C5327,C5367,C5377		ISNS_ON:NO

SYNC_MASTER=K91_DINESH SYNC_DATE=08/16/2010

PAGE TITLE: Voltage & Load Side Current Sensing

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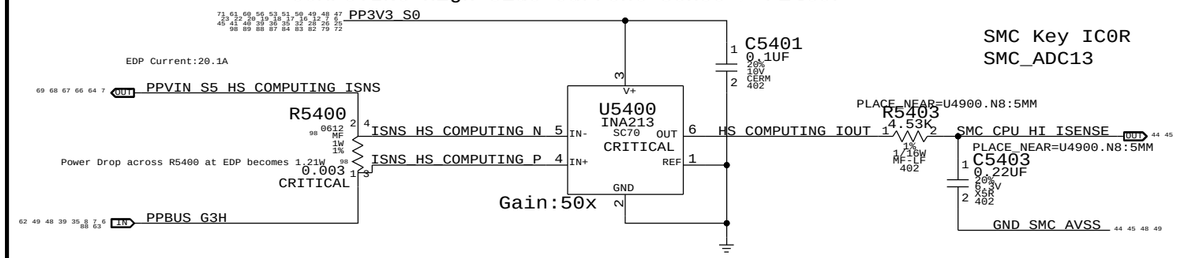
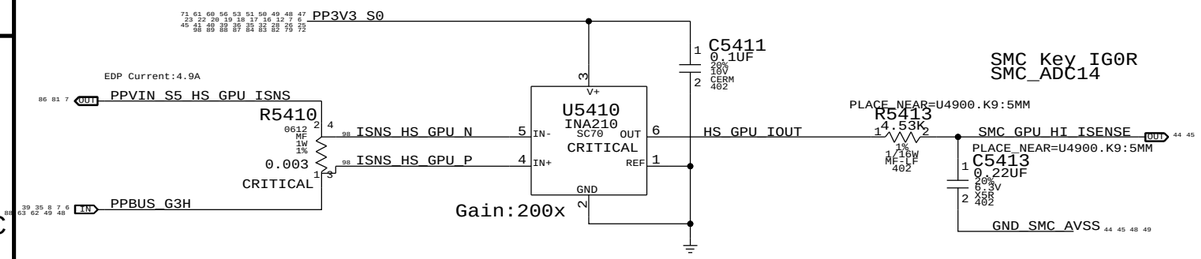
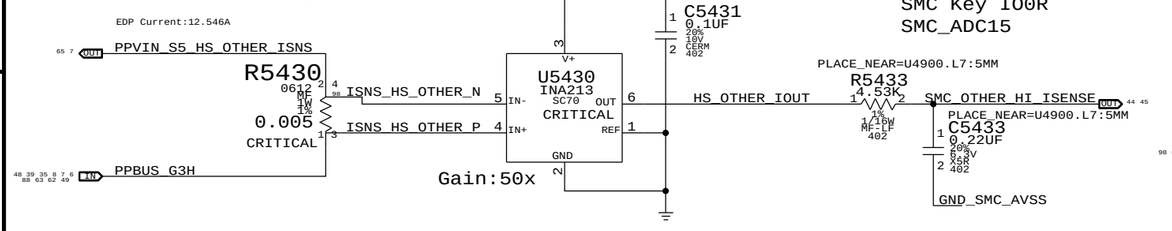
COMPUTING High Side Current Sense / Filter



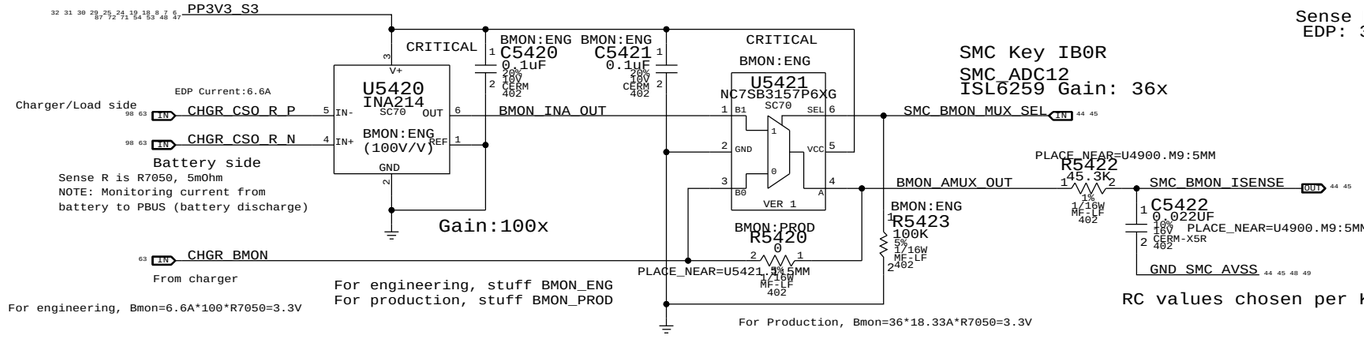
GRAPHICS High Side Current Sense / Filter



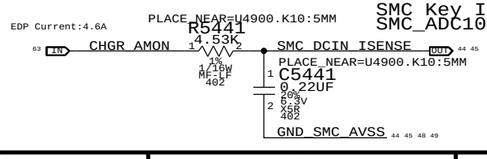
OTHER High Side Current Sense / Filter



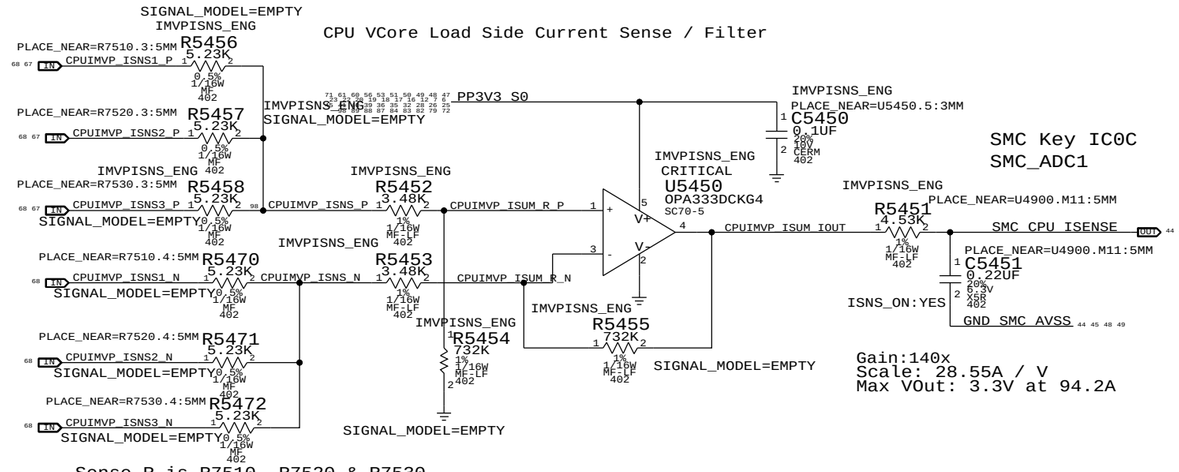
CHARGER BMON High Side (BATTERY DISCHARGE) Current Sense, MUX & Filter



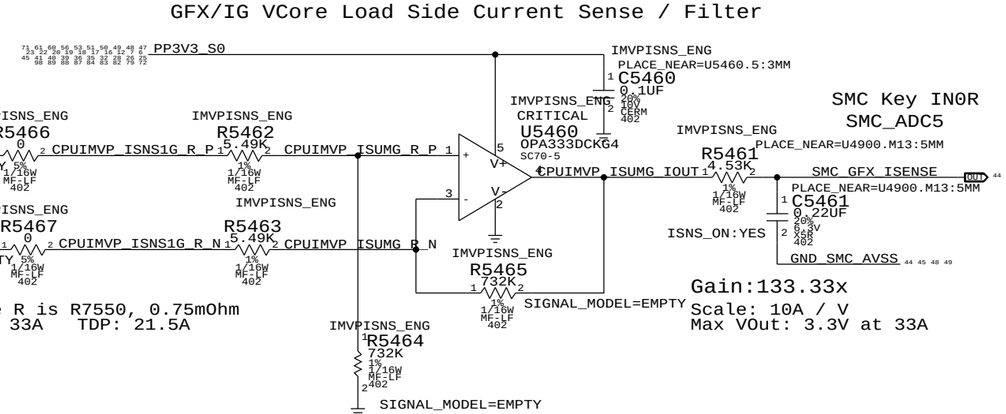
DC-IN (AMON) Current Sense Filter



CPU VCore Load Side Current Sense / Filter



GFX/IG VCore Load Side Current Sense / Filter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	2	RES, 0OHM, 0402	C5451,C5461		ISNS_ON:NO

RC values chosen per K17 Radar 7337775

SYNC_MASTER=K91_DINESH SYNC_DATE=10/29/2016

PAGE TITLE: High Side and CPU/AXG Current Sensing

Apple Inc.

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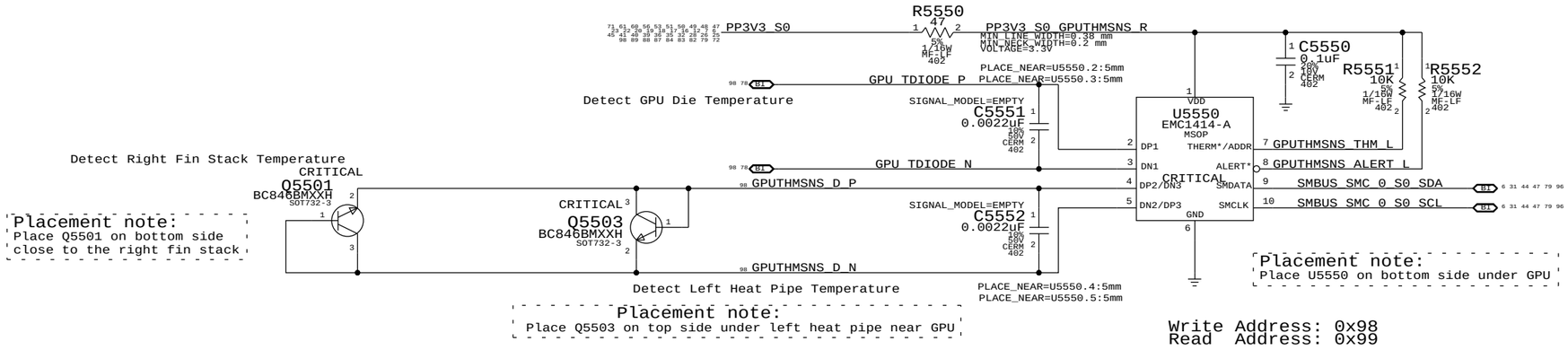
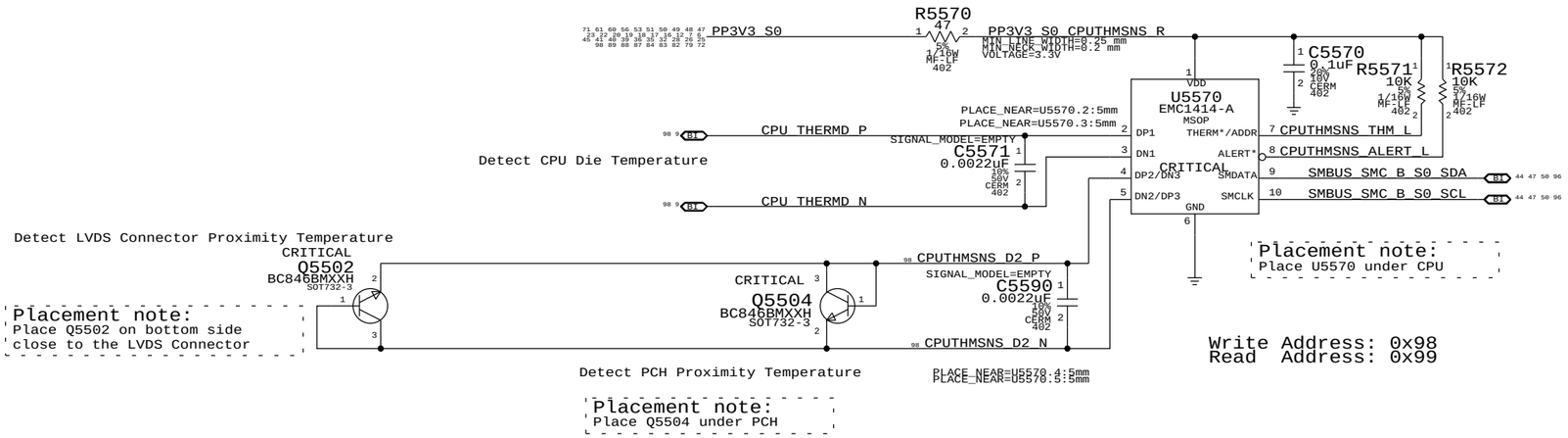
GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack

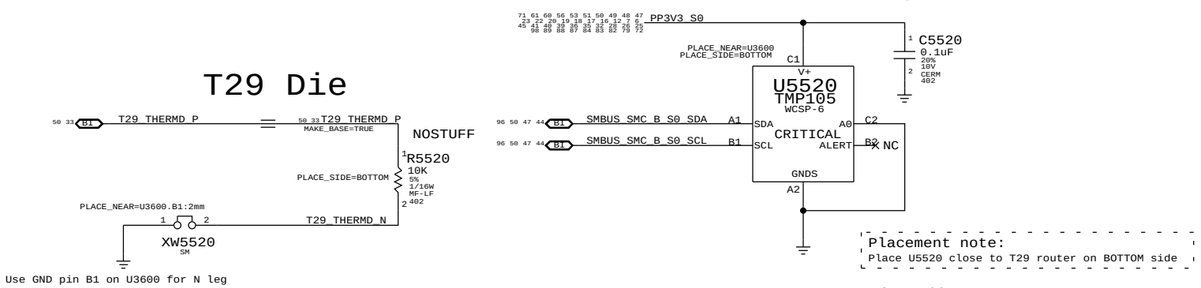


CPU Proximity/CPU Die/PCH Proximity/LVDS Connector Proximity



Note: EMC1414 can perform Beta Compensation for External Diode 1 only

T29 Proximity



SYNC_MASTER=K91_DINESH	SYNC_DATE=09/22/2010
PAGE TITLE: Thermal Sensors	
Apple Inc.	DRAWING NUMBER / SIZE: D
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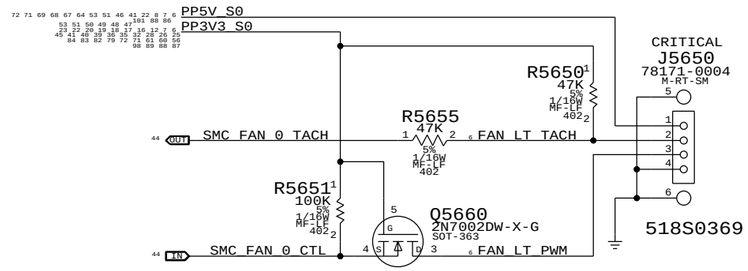
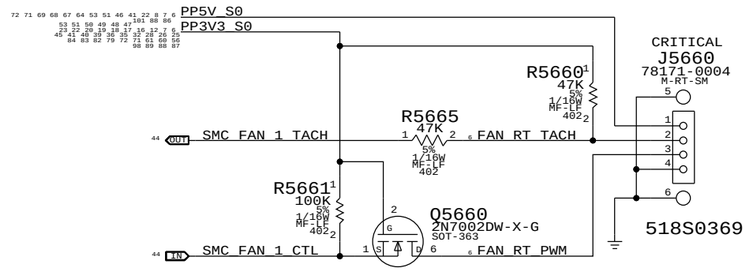
Left Fan



Right Fan



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: Fan Connectors

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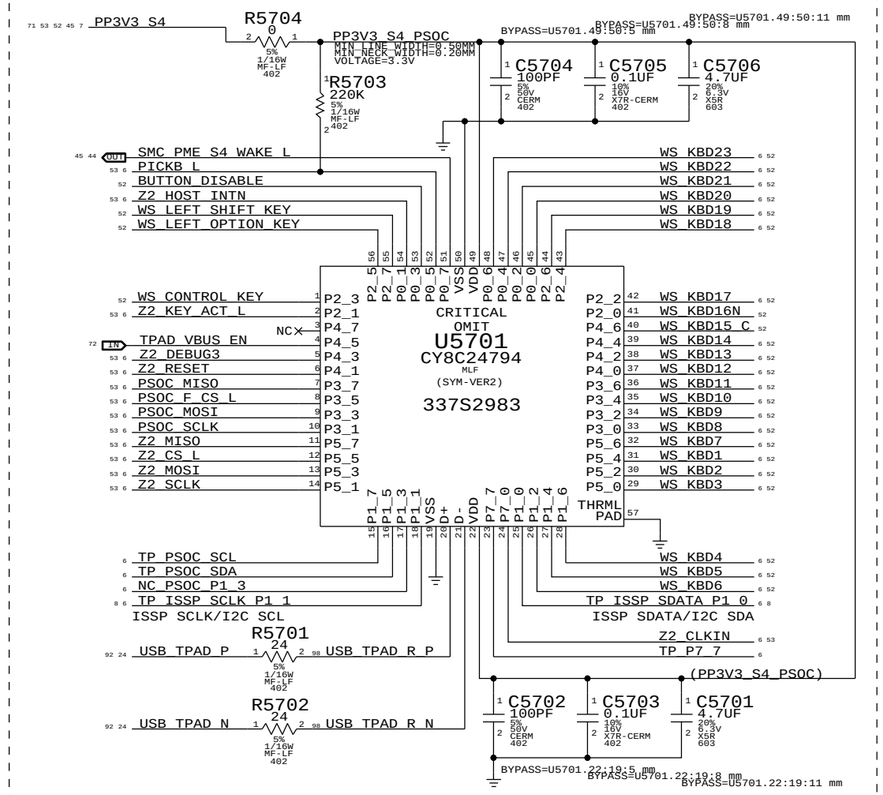
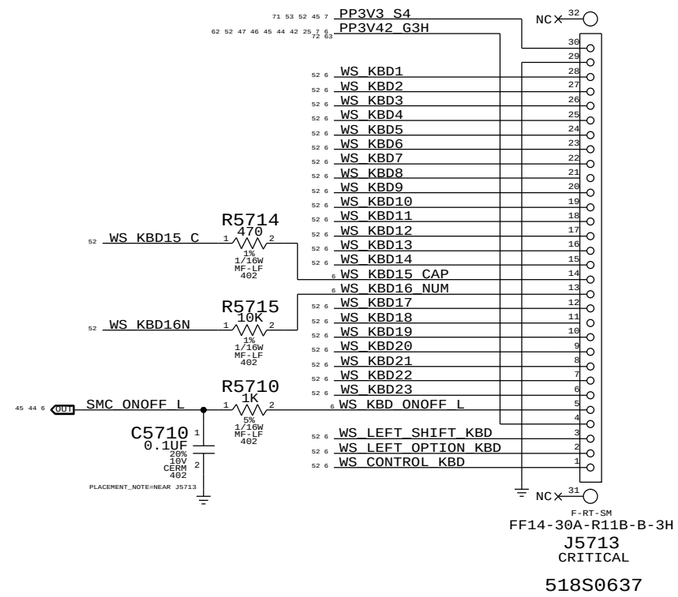
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



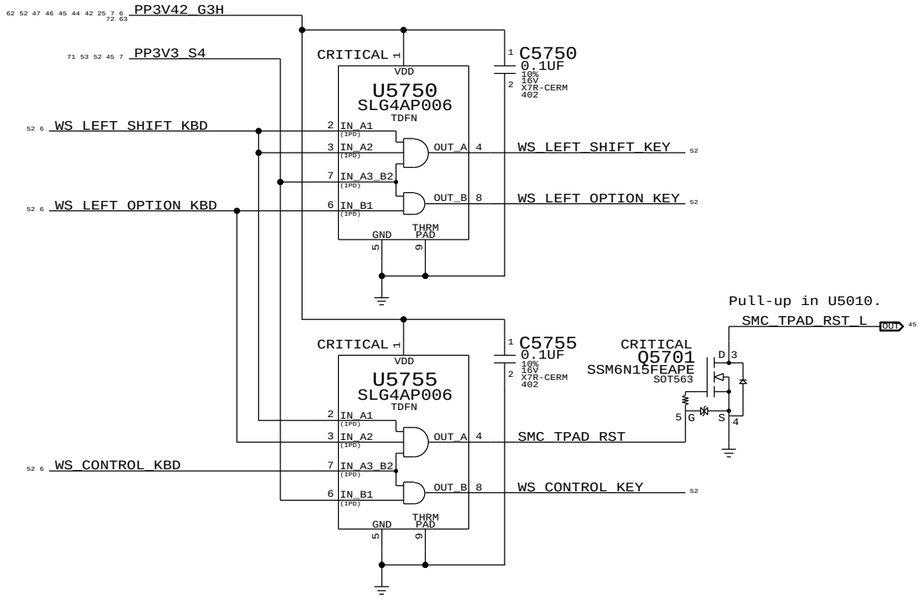
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector

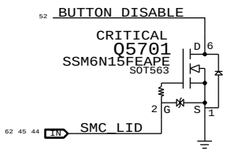


SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: WELLSPRING 1

Apple Inc.

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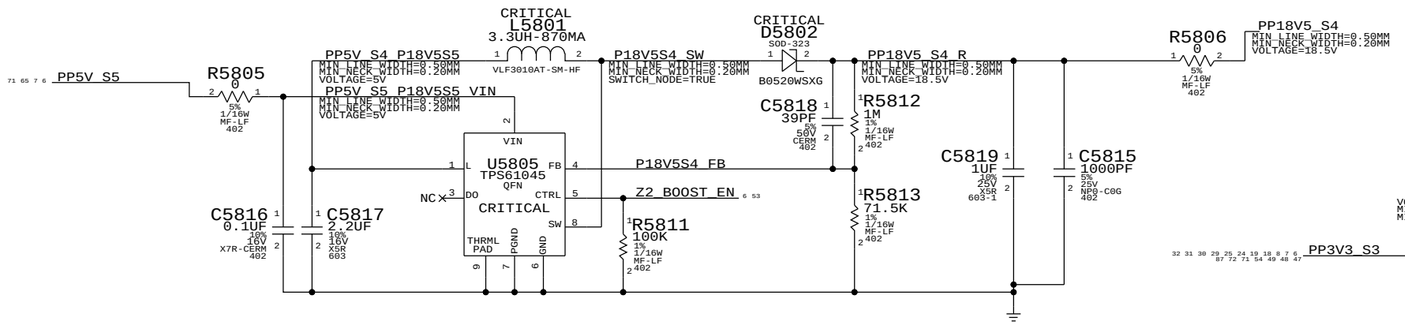
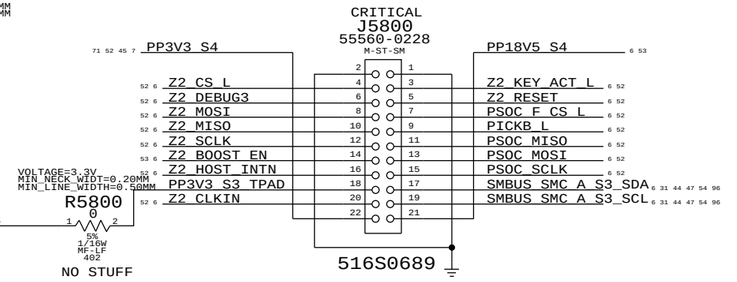
BOOSTER +18.5VDC FOR SENSORS

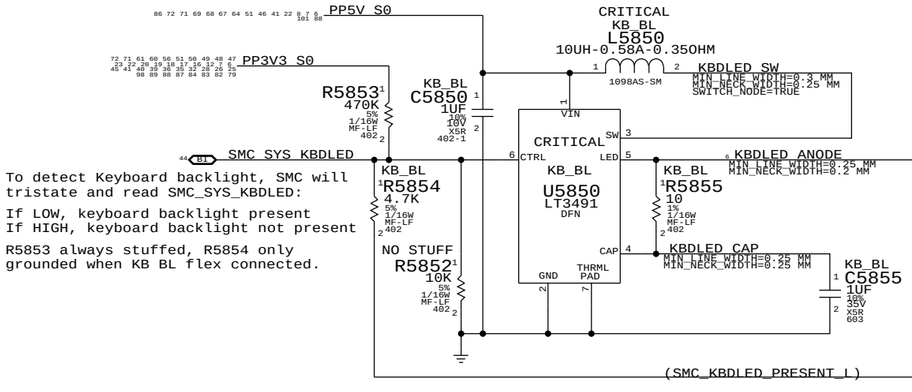
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

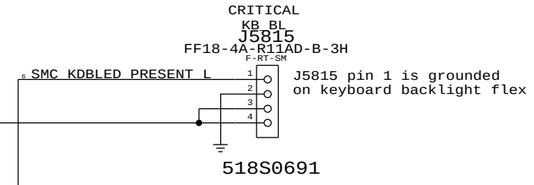


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



SYNC_MASTER=K91_ERIC	SYNC_DATE=07/14/2010
PAGE TITLE: WELLSPRING 2	
Apple Inc.	DRAWING NUMBER / SIZE: D
	REVISION
	BRANCH
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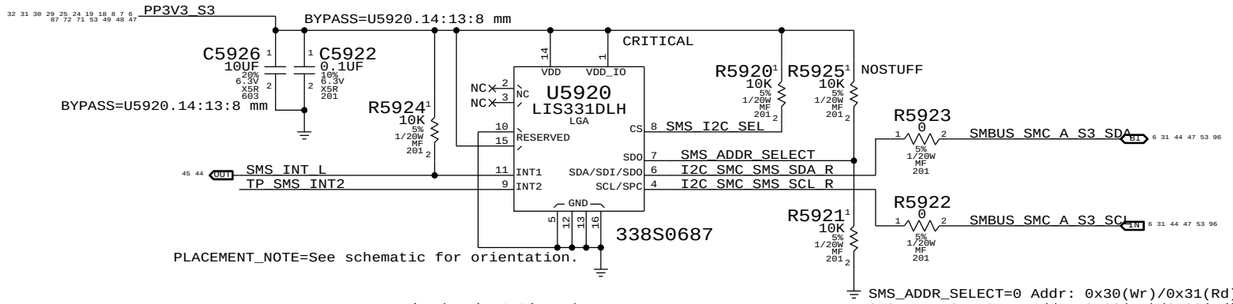

SYNC_MASTER=K91_DINESH SYNC_DATE=08/06/2010

PAGE TITLE
Digital Accelerometer

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

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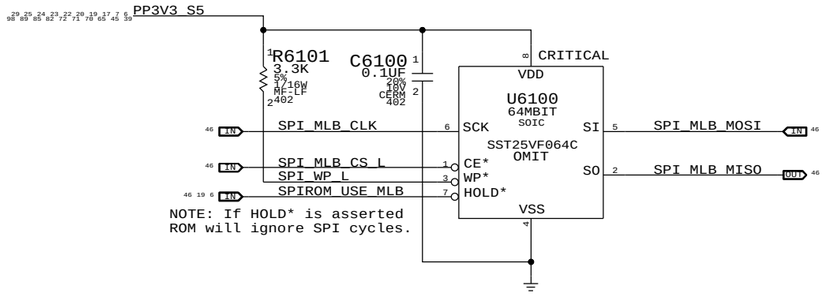

SYNC_MASTER=K91_BEN SYNC_DATE=06/08/2010

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

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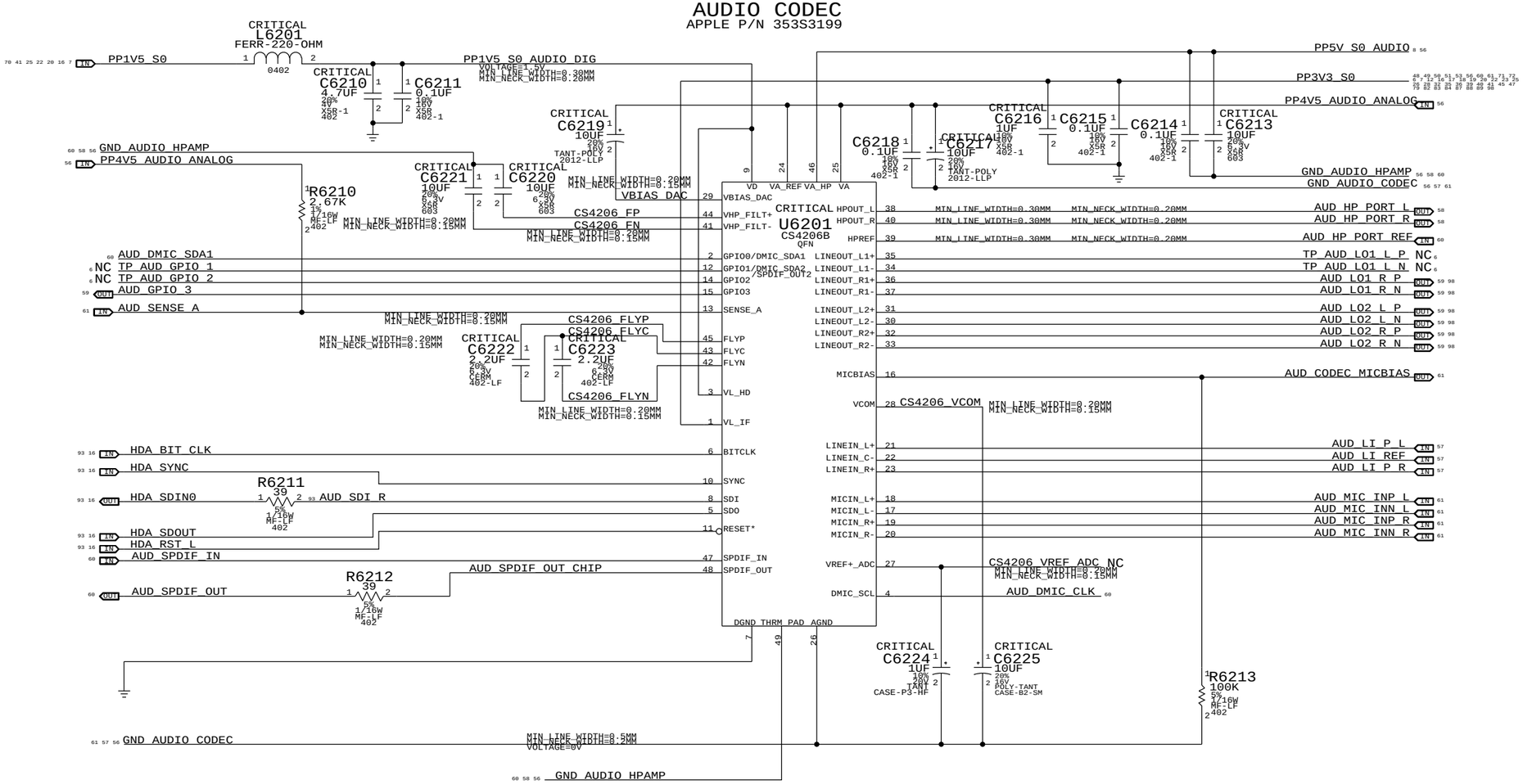
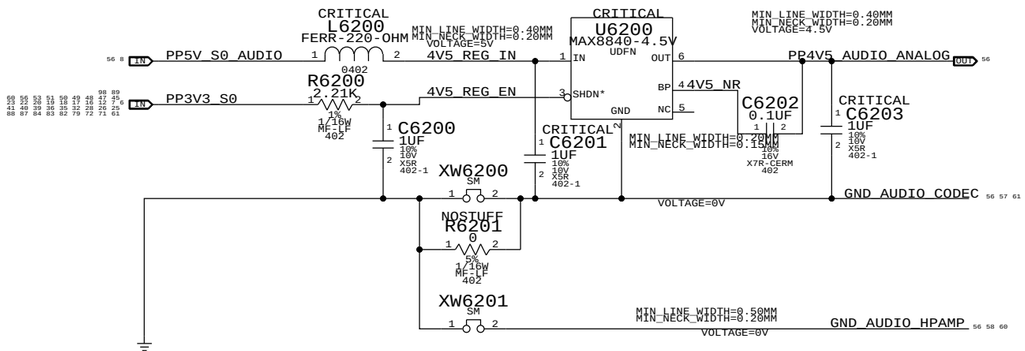
SHEET 55 OF 101

AUDIO CODEC
APPLE P/N 353S3199



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2234



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=K91_AUDIO SYNC_DATE=09/30/2010

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

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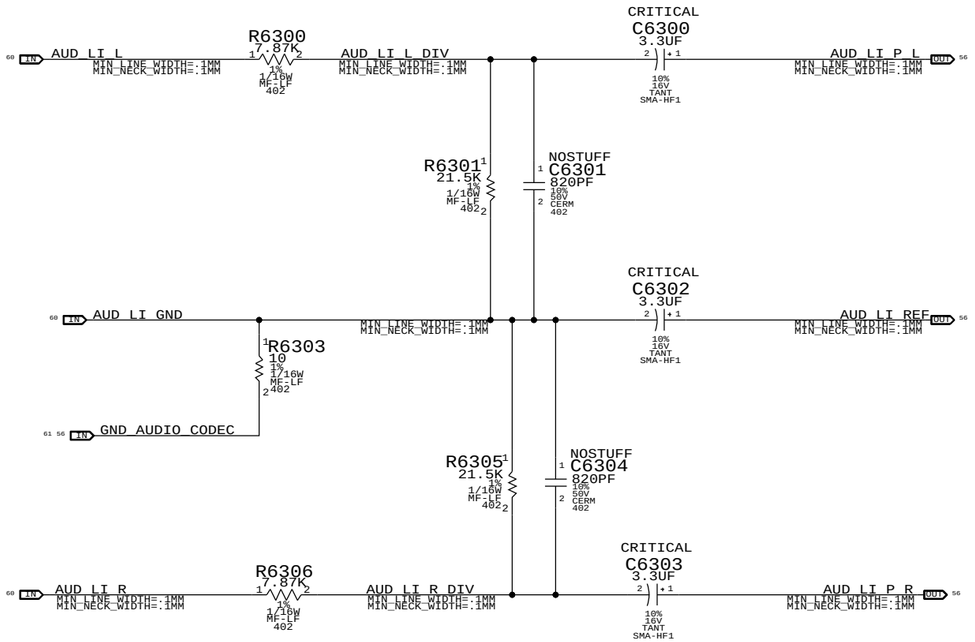
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



SYNC_MASTER=K91_AUDIO SYNC_DATE=07/12/2010

PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

DRAWING NUMBER
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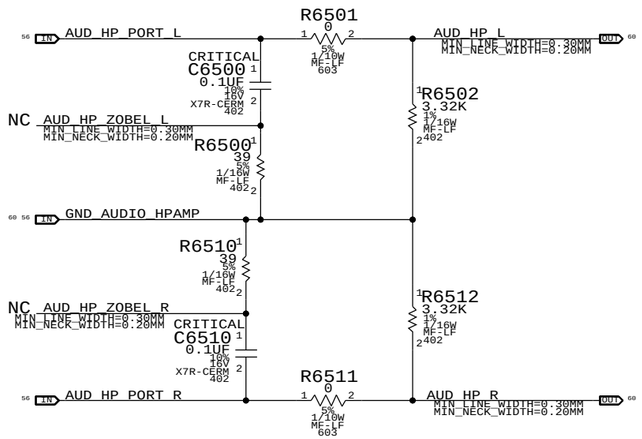
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=K91_AUDIO SYNC_DATE=07/12/2010

PAGE TITLE
AUDIO: HEADPHONE FILTER

Apple Inc.

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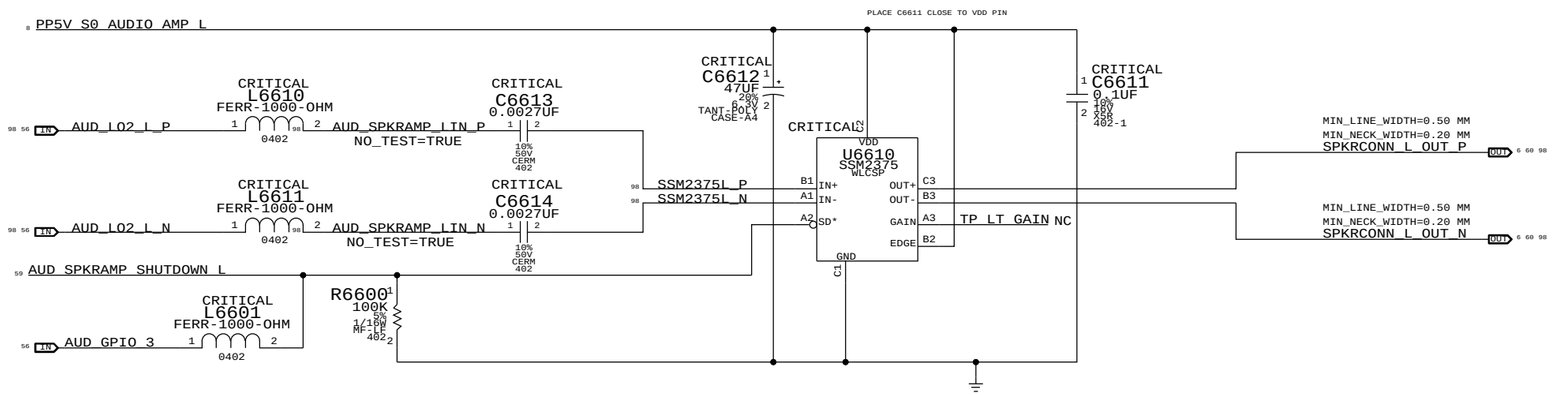
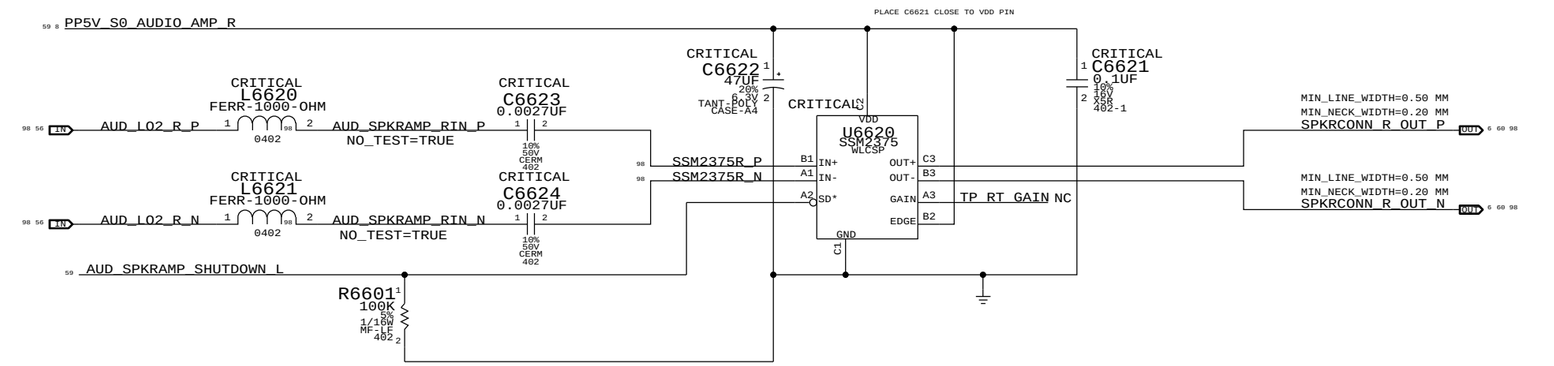
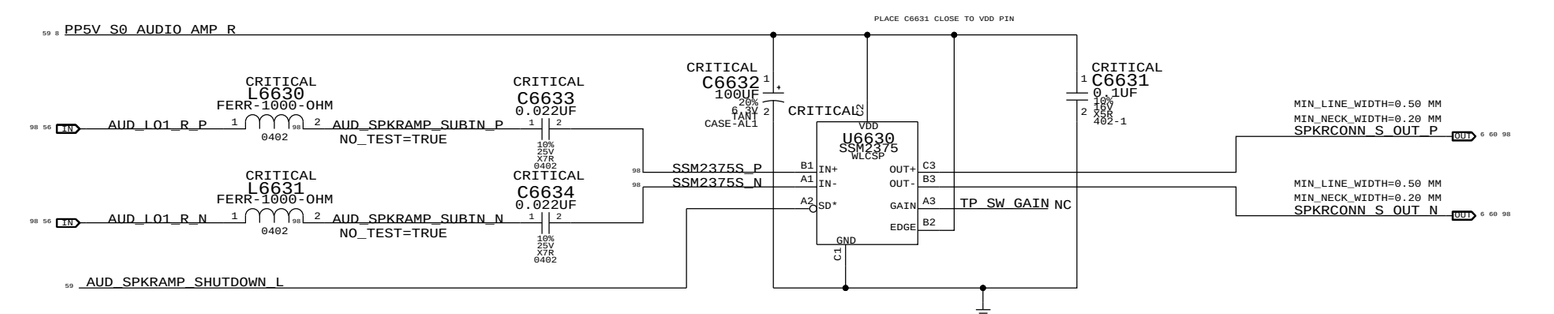
3X MONO SPEAKER AMPLIFIERS (SSM2375)
APN: 353S2958

GAIN = +3 DB
1ST ORDER FC (L&R) = ~737 HZ
1ST ORDER FC (SUB) = ~90 HZ







SYNC_MASTER=K91_AUDIO SYNC_DATE=07/12/2010

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER | SIZE: D
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MIC CONNECTOR
Dual DMIC removed.Added single analog mic like K18.
Sept 21st 2010

AUDIO JACK 1 LO/HP JACK, SPDIF TX

PP3V3_S0
APN: 514-0671
CRITICAL
J6700
SPDIF-TXRX-K24
F-RT-TH
AUDIO
POF
OPERATING VOLTAGE 3.3
SHELL
SHIELD PINS
C6700 0.1UF 10% 10V X5R 402-1
C6701 2.2UF 20% 6.3V CERM 402-LF
AUD_SPDIF_OUT
L6703 FERR-1000-OHM CRITICAL 0402
HS_MIC_P
L6702 FERR-1000-OHM CRITICAL 0402
HS_MIC_N
L6707 CRITICAL FERR-220-OHM 0402
AUD_HP_PORT_REF
L6701 CRITICAL FERR-220-OHM-2.5A 0603
GND_AUDIO_HPAMP
L6704 CRITICAL FERR-220-OHM 0402
AUD_HP_R
L6706 CRITICAL FERR-220-OHM 0402
AUD_HP_L
R6700 10K 5% 1/16W MF-LF 402
AUD_J1_SLEEVEDET_R
L6705 FERR-1000-OHM CRITICAL 0402
AUD_J1_TIPDET_R
DZ6703 CRITICAL 6.8V-100PF 402
DZ6704 CRITICAL 6.8V-100PF 402
DZ6700 CRITICAL 6.8V-100PF 402
DZ6706 CRITICAL 6.8V-100PF 402
DZ6701 CRITICAL 6.8V-100PF 402
C6705 100PF 5% 50V CERM 402
AUD_CONNJ1_SLEEVE2
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING
AUD_CONNJ1_SLEEVE
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V
GND_CHASSIS_AUDIO_JACK

XW6701 SM
XW6702 SM
GND PATCH
R6701 0 5% 1/16W MF-LF 402
GND_CHASSIS_AUDIO_JACK

AUDIO JACK 2 LINE IN JACK, SPDIF RX

PP3V3_S0
APN: 514-0635
CRITICAL
J6750
AUDIO-RCVR-M97
F-RT-TH5
AUDIO
POF
OPERATING VOLTAGE 3.3
SHELL
SHIELD PINS
C6750 1UF 10% 10V X5R 402-1
AUD_J2_OPT_OUT
R6749 4.7 5% 1/10W MF-LF 402
AUD_SPDIF_IN
AUD_CONNJ2_TIPDET
AUD_CONNJ2_RING
AUD_CONNJ2_TIP
AUD_CONNJ2_SLEEVE
L6754 CRITICAL FERR-1000-OHM 0402
AUD_LI_R
L6756 CRITICAL FERR-1000-OHM 0402
AUD_LI_L
L6758 CRITICAL 600-OHM-300MA 0402
AUD_LI_GND
L6752 CRITICAL FERR-1000-OHM 0402
AUD_J2_TIPDET_R
DZ6757 CRITICAL ESDALC5-1BM2 SOD882
DZ6758 CRITICAL ESDALC5-1BM2 SOD882
DZ6754 CRITICAL 6.8V-100PF 402
DZ6756 CRITICAL 6.8V-100PF 402
C6756 100PF 5% 50V CERM 402
GND_CHASSIS_AUDIO_JACK

MIC CONNECTOR

Place this in place of DMIC connector J6780

CRITICAL
J6780
78171-0003
M-RT-SM
BI_MIC_N
BI_MIC_SHIELD
BI_MIC_P

DIGI_MIC CRITICAL L6783 600-OHM-300MA 0402
AUD_DMIC_CLK
CON_DMIC_CLK
DIGI_MIC CRITICAL L6784 600-OHM-300MA 0402
AUD_DMIC_SDA1
CON_DMIC_SDA
DIGI_MIC CRITICAL L6785 600-OHM-300MA 0402
PP3V3_S0
CON_DMIC_PWR
DIGI_MIC CRITICAL J6783 78171-0004 M-RT-SM

SPEAKER CONNECTOR

APN: 518S0519
CRITICAL
J6781
78171-0002
M-RT-SM
SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
CRITICAL
J6782
78171-0004
M-RT-SM

APN: 518S0521
SPKRCONN_S_OUT_P
SPKRCONN_S_OUT_N
SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
NOSTUFF CRITICAL C6781 33PF 5% 50V CERM 402
NOSTUFF CRITICAL C6782 33PF 5% 50V CERM 402
NOSTUFF CRITICAL C6783 33PF 5% 50V CERM 402
NOSTUFF CRITICAL C6784 33PF 5% 50V CERM 402

SYNC_MASTER=K91_AUDIO
SYNC_DATE=09/30/2010
PAGE TITLE: AUDIO: JACKS
Apple Inc.
DRAWING NUMBER
SIZE: D
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BRANCH
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SHEET: 60 OF 101

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

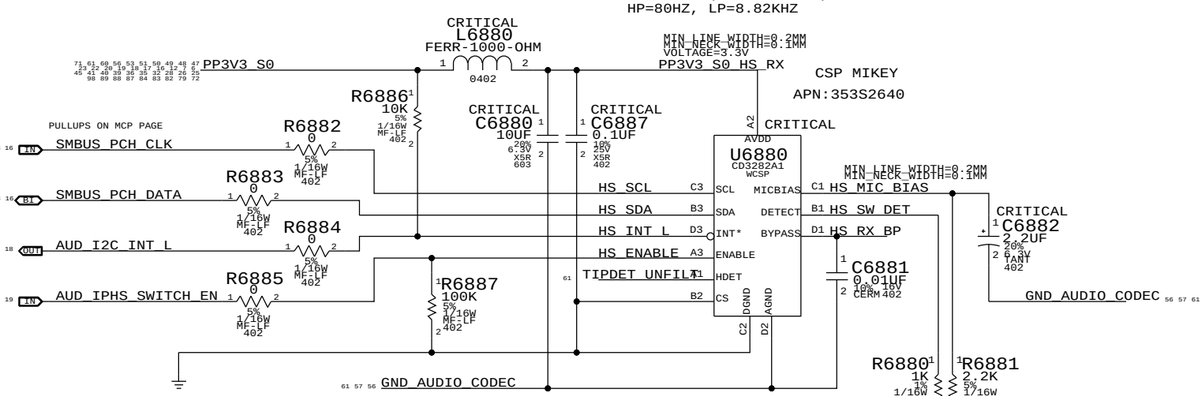
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

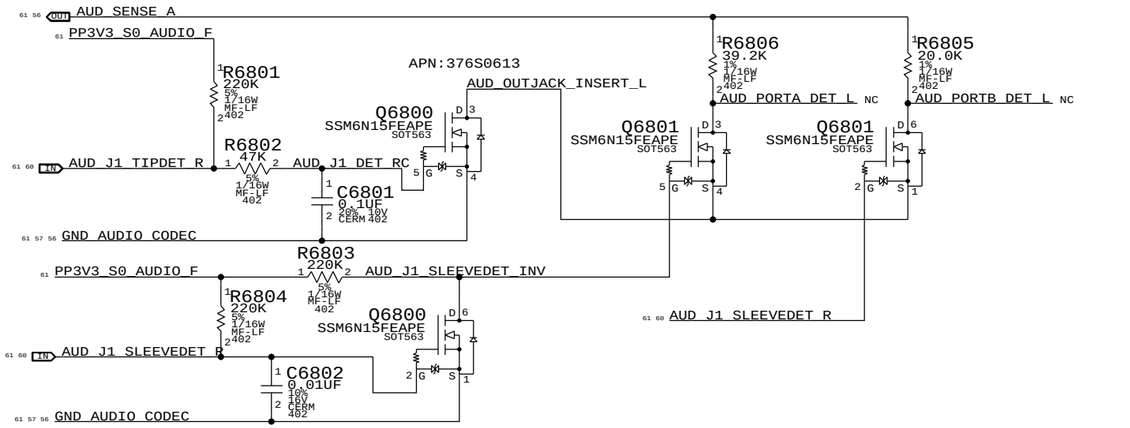
SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

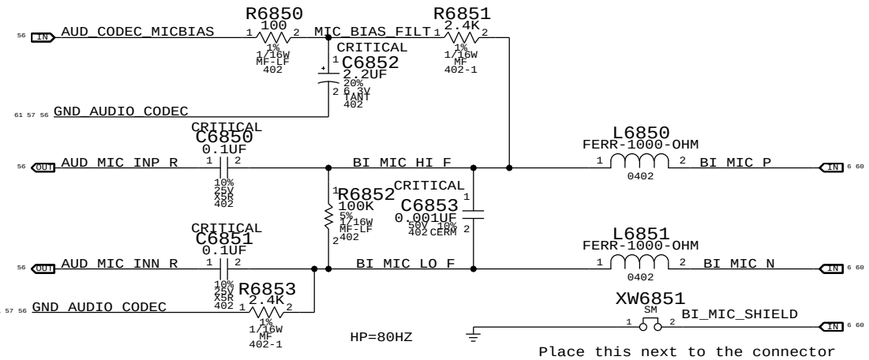
PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



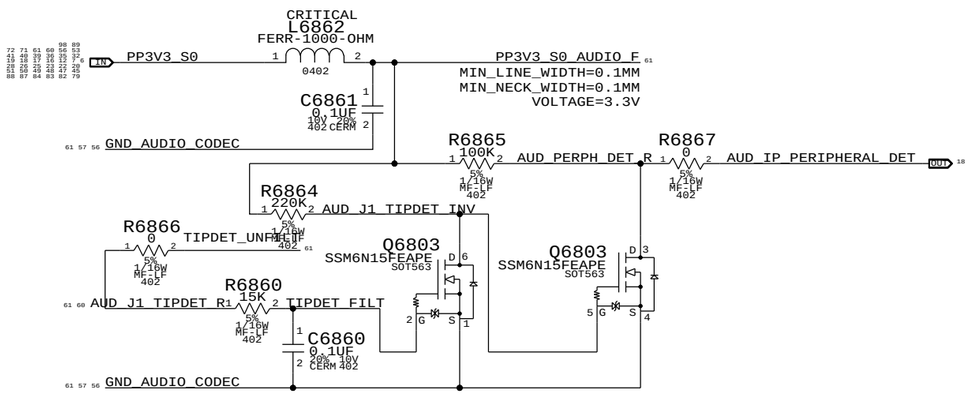
PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)



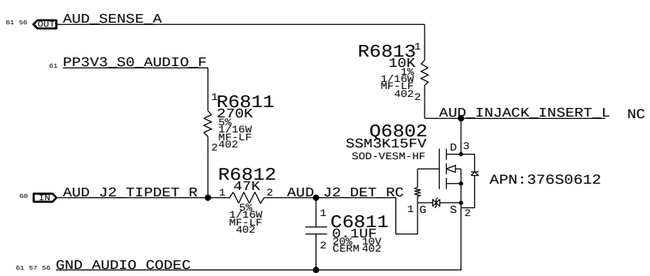
PORT B RIGHT(BUILT-IN MIC)

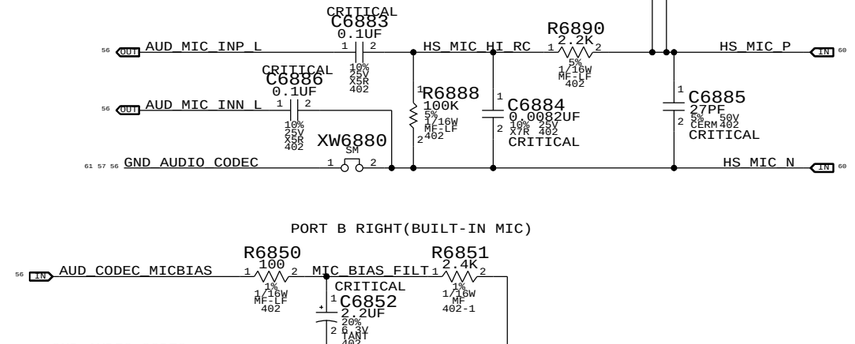


EXTRACTION NOTIFICATION



PORT C DETECT (LINE-IN)





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PAGE TITLE	AUDIO: JACK TRANSLATORS
Apple Inc.	DRAWING NUMBER: — SIZE: D
	REVISION:
	BRANCH:
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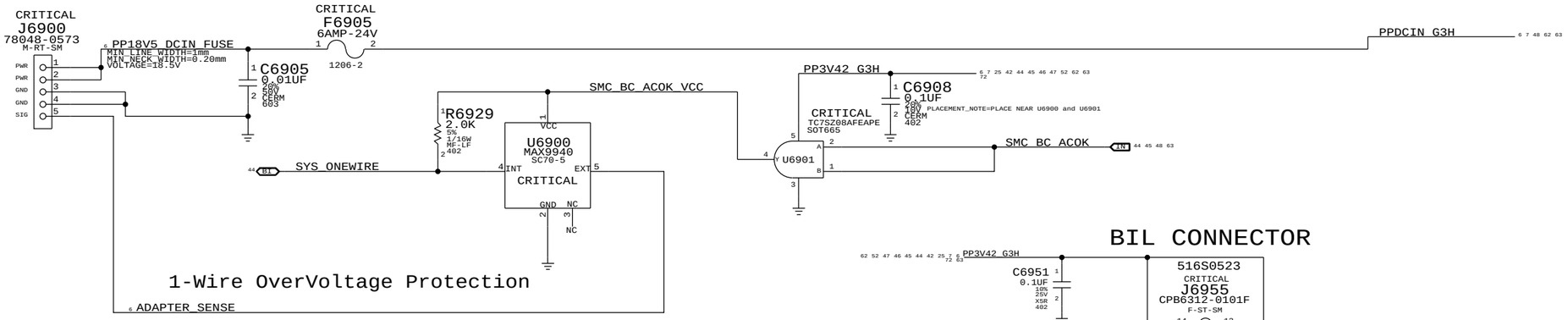
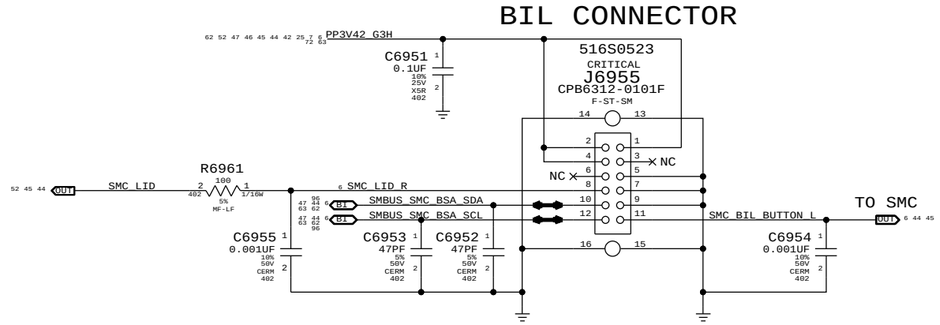
MagSafe DC Power Jack



1-Wire OverVoltage Protection

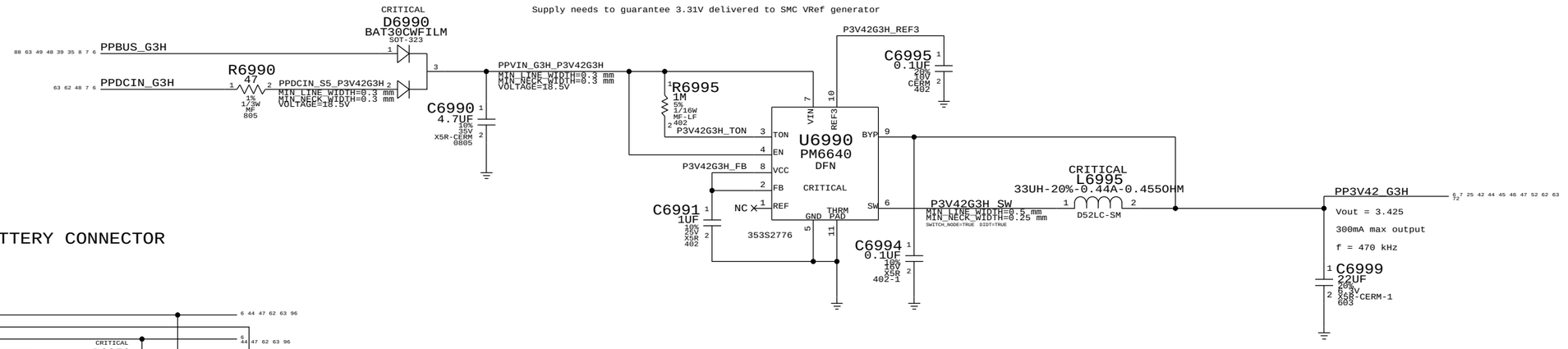
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

BIL CONNECTOR

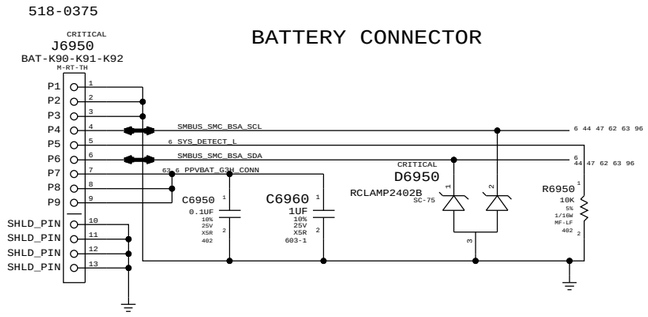


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



SYNC_MASTER=K91_ERIC	SYNC_DATE=10/08/2010
PAGE TITLE: DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER: SIZE D
	REVISION:
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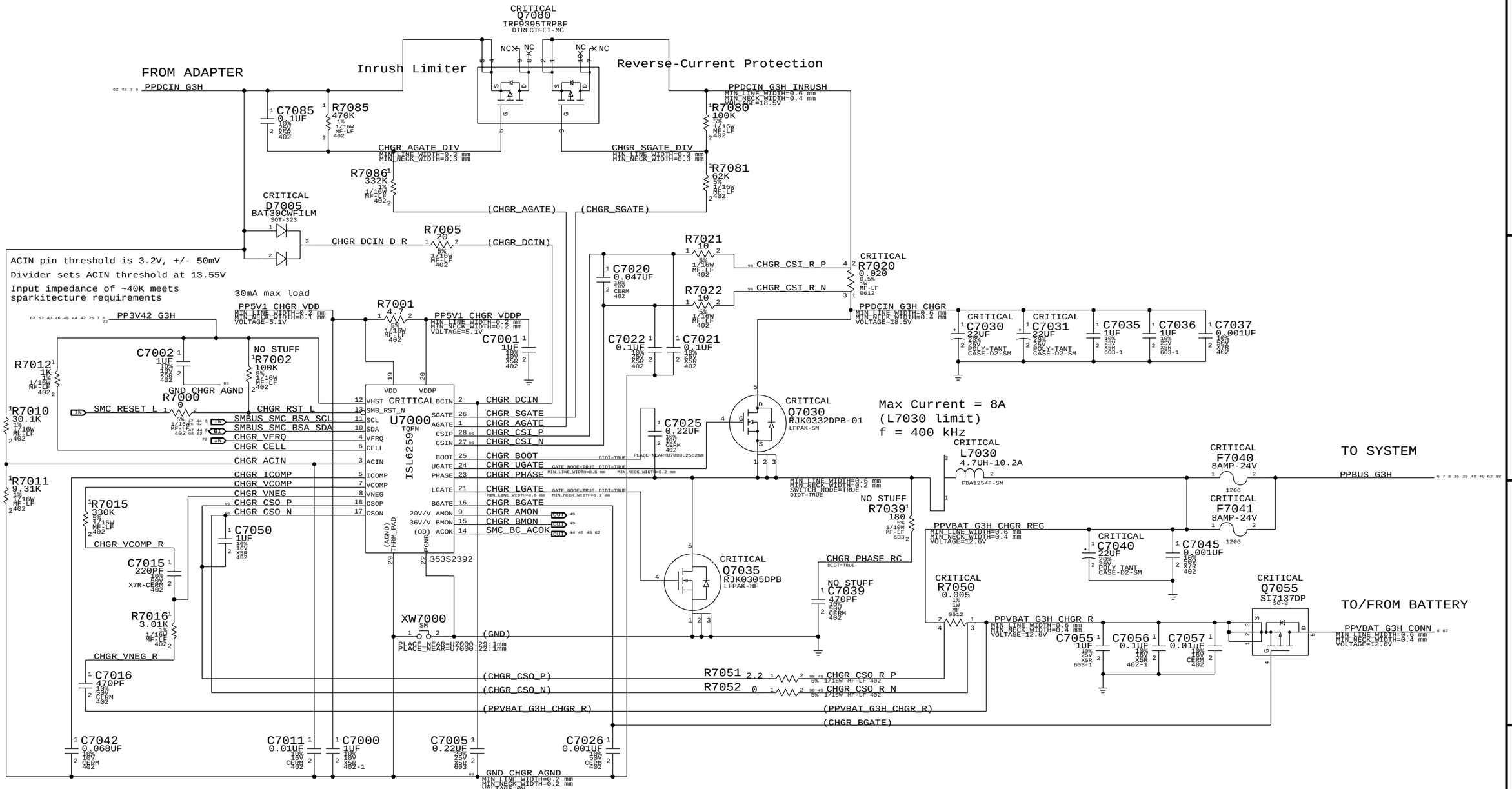
	PAGE: 69 OF 132
	SHEET: 62 OF 101



SYNC_MASTER=K91_CHANG SYNC_DATE=07/20/2016

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER — SIZE D

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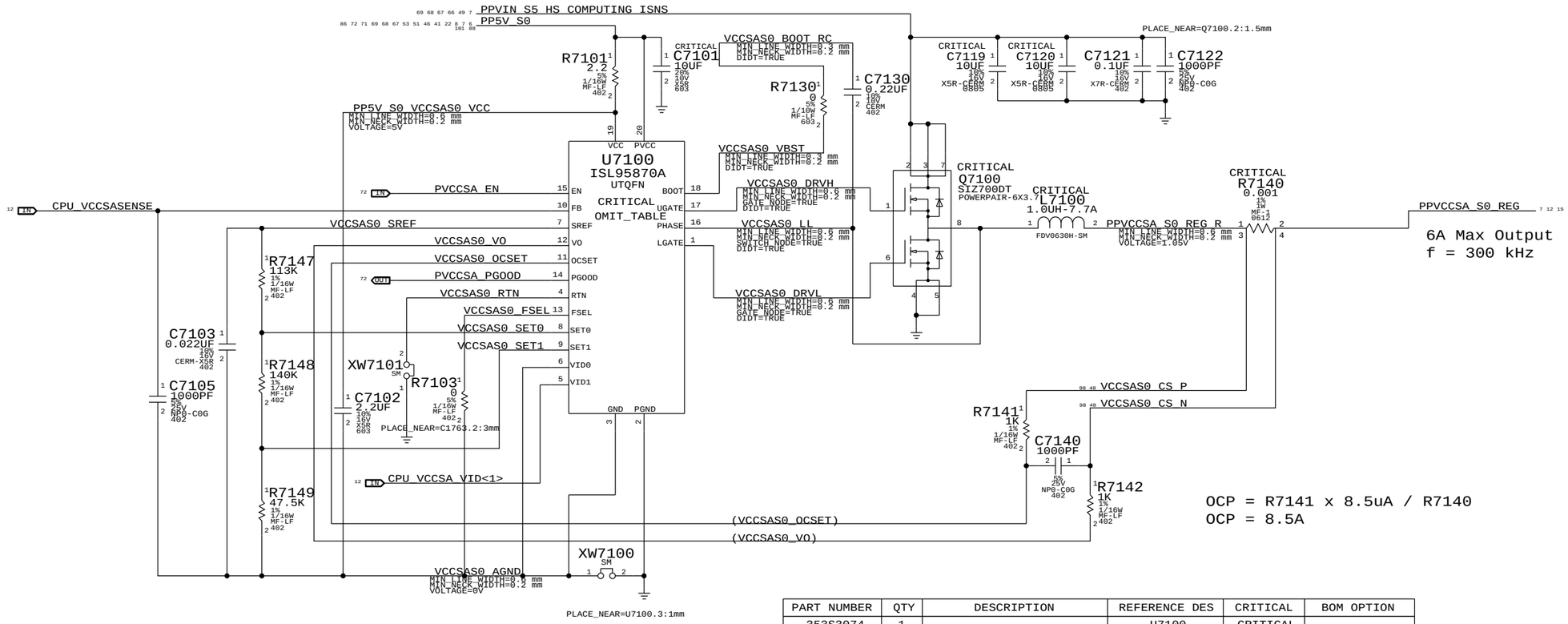

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1	IC,ISL95870A,PWM,2BIT-VID,RMOT-SNSE,20P	U7100	CRITICAL	

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER | SIZE: D

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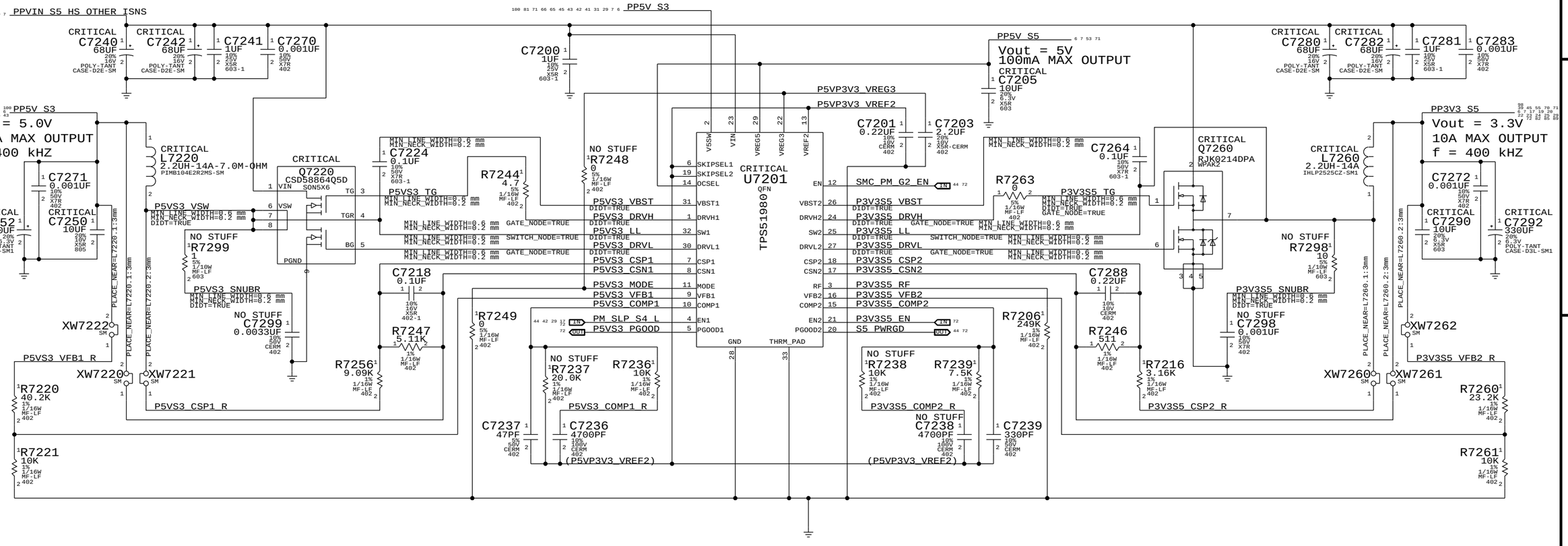

SYNC_MASTER=K91_ERIC	SYNC_DATE=10/08/2010
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER · SIZE D
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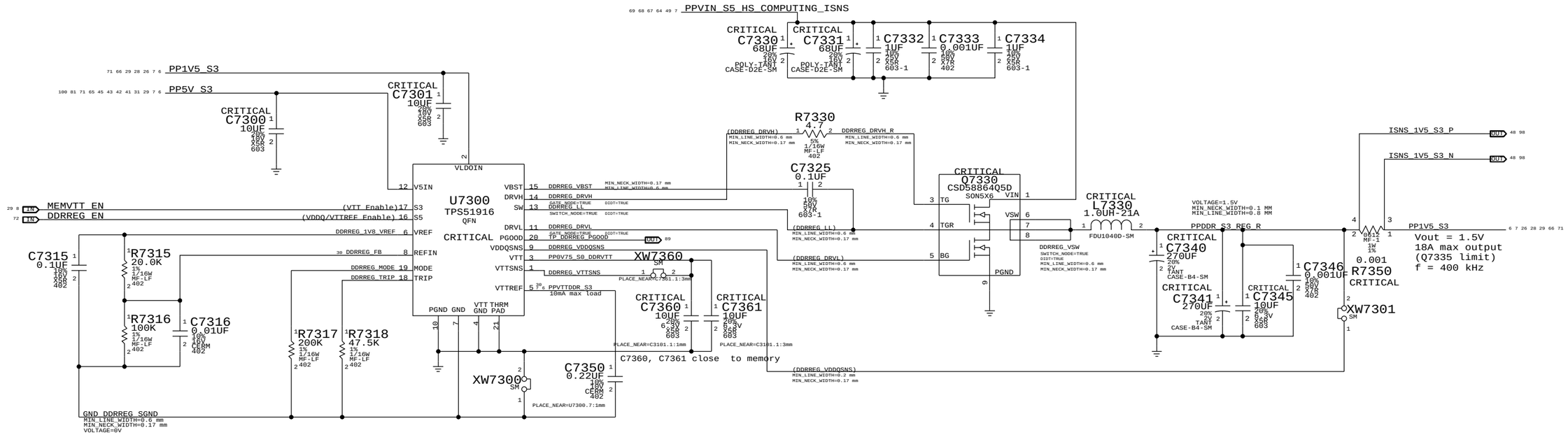

SYNC_MASTER=K91_ERIC	SYNC_DATE=10/08/2010
PAGE TITLE	1.5V DDR3 Supply
Apple Inc.	DRAWING NUMBER: D
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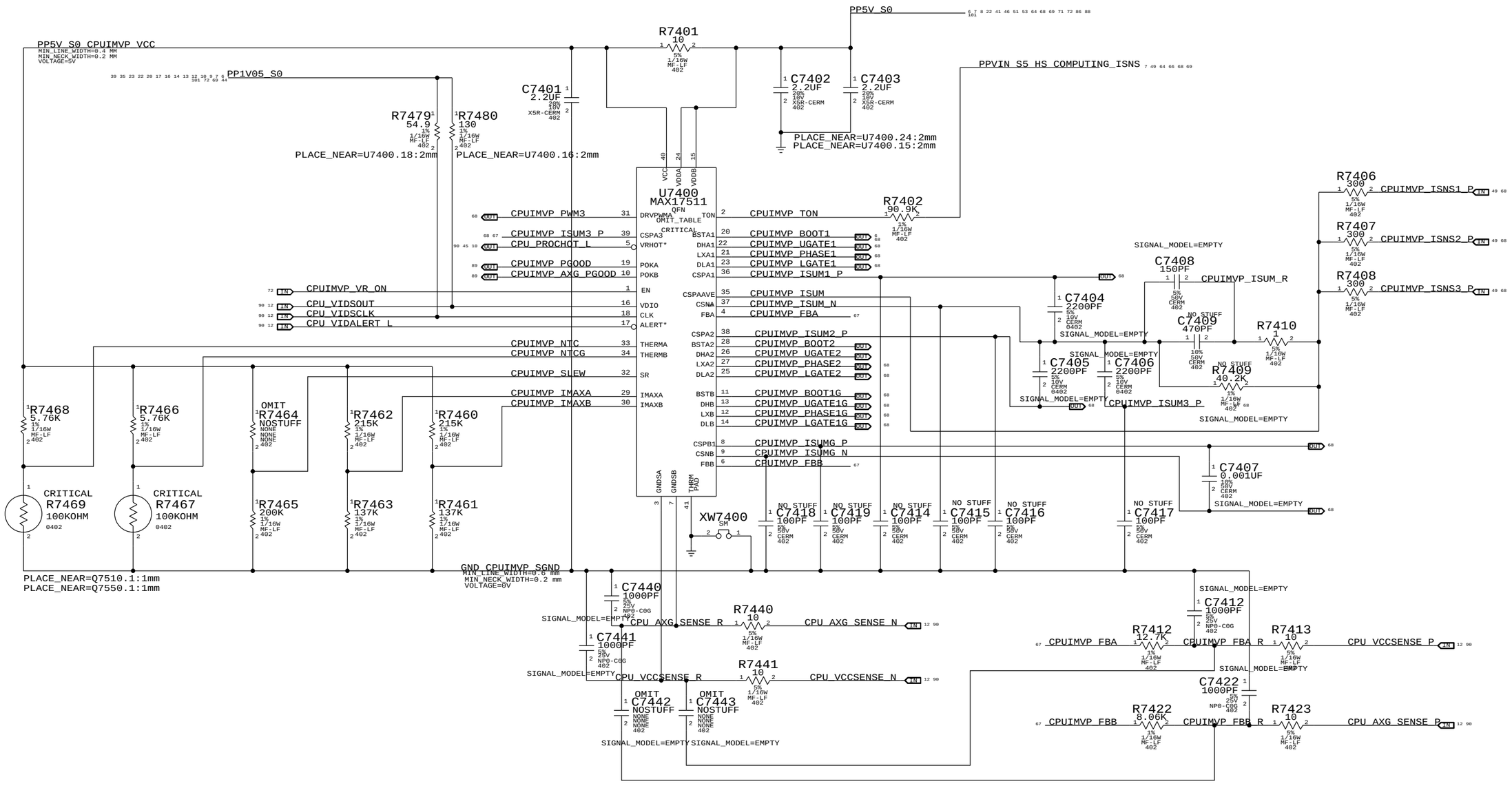
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3259	1	IC,MAX15092,3+1PH CPU REG,IMVP7,5X5QFN40	U7400	CRITICAL	



SYNC_MASTER=K91_ERIC	SYNC_DATE=10/08/2010
PAGE TITLE	CPU IMVP7 & AXG VCore Regulator
Apple Inc.	DRAWING NUMBER: SIZE D
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PHASE 1

PPVIN_S5_HS_COMPUTING_ISNS

376S0872

CRITICAL Q7510 IRF6723M2DPBF DIRECTFET-MA

CRITICAL L7510 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7510 0.00075 1% 1W MF 0612

THESE TWO CAPS ARE FOR EMC

CRITICAL C7513 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7514 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7515 10UF 10% 16V X5R-CERM 0805

CRITICAL C7516 10UF 10% 16V X5R-CERM 0805

CRITICAL C7517 1UF 10% 16V X5R 402

CRITICAL C7518 0.001UF 10% 50V X7R 402

C7519 0.001UF 10% 50V X7R 402

CPUIMVP_BOOT1_RC MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE

R7511 0 5% 1/16W MF-LF 402

C7511 0.22UF 10% 16V CERM 402

CPUIMVP_BOOT1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

CPUIMVP_UGATE1 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_PHASE1 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE SWITCH_NODE=TRUE

CPUIMVP_LGATE1 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

376S0930

CRITICAL Q7515 IRF6798MTRPBF DIRECTFET-MX

NOSTUFF R7512 2.2 5% 1/10W MF-LF 603

CPUIMVP_PH1_SNUB DIDT=TRUE

NOSTUFF C7512 0.001UF 10% 50V CERM 402

PPVCORE_S0_CPU_PH1_L

PPVCORE_S0_CPU_PH1

PPVCORE_S0_CPU

CPUIMVP_ISNS1_P

CPUIMVP_ISNS1_N

R7513 46.4 1% 1/10W MF-LF 402

R7514 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUM_N

NOSTUFF C7571 330PF 10% 50V CERM 402

CPUIMVP_ISUM1_P

PHASE 2

376S0872

CRITICAL Q7510 IRF6723M2DPBF DIRECTFET-MA

CRITICAL L7520 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7520 0.00075 1% 1W MF 0612

THESE TWO CAPS ARE FOR EMC

CRITICAL C7523 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7524 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7525 10UF 10% 16V X5R-CERM 0805

CRITICAL C7526 10UF 10% 16V X5R-CERM 0805

CRITICAL C7527 1UF 10% 16V X5R 402

CRITICAL C7528 0.001UF 10% 50V X7R 402

C7529 0.001UF 10% 50V X7R 402

CPUIMVP_BOOT2_RC MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE

R7521 0 5% 1/16W MF-LF 402

C7521 0.22UF 10% 16V CERM 402

CPUIMVP_BOOT2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

CPUIMVP_UGATE2 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_PHASE2 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE SWITCH_NODE=TRUE

CPUIMVP_LGATE2 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

376S0930

CRITICAL Q7525 IRF6798MTRPBF DIRECTFET-MX

NOSTUFF R7522 2.2 5% 1/10W MF-LF 603

CPUIMVP_PH2_SNUB DIDT=TRUE

NOSTUFF C7522 0.001UF 10% 50V CERM 402

PPVCORE_S0_CPU_PH2_L

PPVCORE_S0_CPU_PH2

PPVCORE_S0_CPU

CPUIMVP_ISNS2_P

CPUIMVP_ISNS2_N

R7523 46.4 1% 1/10W MF-LF 402

R7524 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUM_N

NOSTUFF C7572 330PF 10% 50V CERM 402

CPUIMVP_ISUM2_P

PHASE 3

376S0772

CRITICAL Q7530 IRF6710 S1

CRITICAL L7530 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7530 0.00075 1% 1W MF 0612

THESE TWO CAPS ARE FOR EMC

CRITICAL C7533 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7534 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7535 10UF 10% 16V X5R-CERM 0805

CRITICAL C7536 10UF 10% 16V X5R-CERM 0805

CRITICAL C7537 1UF 10% 16V X5R 402

CRITICAL C7538 0.001UF 10% 50V X7R 402

C7539 0.001UF 10% 50V X7R 402

CPUIMVP_BOOT3_RC MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE

R7531 0 5% 1/16W MF-LF 402

C7531 0.22UF 10% 16V CERM 402

CPUIMVP_BOOT3 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

CPUIMVP_UGATE3 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_PHASE3 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE SWITCH_NODE=TRUE

CPUIMVP_LGATE3 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

376S0930

CRITICAL Q7535 IRF6798MTRPBF DIRECTFET-MX

NOSTUFF R7532 2.2 5% 1/10W MF-LF 603

CPUIMVP_PH3_SNUB DIDT=TRUE

NOSTUFF C7532 0.001UF 10% 50V CERM 402

SWITCH_NODE=TRUE

PPVCORE_S0_CPU_PH3_L

PPVCORE_S0_CPU_PH3

PPVCORE_S0_CPU

CPUIMVP_ISNS3_P

CPUIMVP_ISNS3_N

R7533 46.4 1% 1/10W MF-LF 402

R7534 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUM_N

NOSTUFF C7573 330PF 10% 50V CERM 402

CPUIMVP_ISUM3_P

PP5V_S0

R7547 10K 5% 1/16W MF-LF 402

C7541 1UF 10% 16V X5R 402

U7541 MAX17491 TQFN CRITICAL

VDD PWN SKIP* BST DH LX DL GND THRM PAD

CPUIMVP_PWM3

CPUIMVP_SKIP

CPUIMVP_BOOT3

CPUIMVP_UGATE3

CPUIMVP_PHASE3

CPUIMVP_LGATE3

Additonal Input Bulk Caps

CRITICAL C7561 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7562 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7563 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7564 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7565 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7566 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7567 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7568 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7569 68UF 20% 16V POLY-TANT CASE-D2E-SM

AXG PHASE

PPVIN_S5_HS_COMPUTING_ISNS

THESE TWO CAPS ARE FOR EMC

CRITICAL C7553 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7554 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7555 10UF 10% 16V X5R-CERM 0805

CRITICAL C7556 10UF 10% 16V X5R-CERM 0805

CRITICAL C7557 1UF 10% 16V X5R 402

CRITICAL C7558 0.001UF 10% 50V X7R 402

C7559 0.001UF 10% 50V X7R 402

CRITICAL Q7550 CSD58864Q5D SON5X6

CRITICAL L7550 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7550 0.00075 1% 1W MF 0612

R7556 0 5% 1/16W MF-LF 402

CPUIMVP_BOOT1G_R MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

C7551 0.22UF 10% 16V CERM 402

R7555 4.7 5% 1/10W MF-LF 402

CPUIMVP_UGATE1G_R MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_BOOT1G MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

CPUIMVP_UGATE1G MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_PHASE1G MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE SWITCH_NODE=TRUE

CPUIMVP_LGATE1G MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

376S0906

CPUIMVP_VSWG MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM SWITCH_NODE=TRUE

NOSTUFF R7552 2.2 5% 1/10W MF-LF 603

CPUIMVP_AXG_SNUB DIDT=TRUE

NOSTUFF C7552 0.001UF 10% 50V CERM 402

PPVCORE_S0_AXG_L

PPVCORE_S0_AXG

CPUIMVP_ISNS1G_P

CPUIMVP_ISNS1G_N

R7553 46.4 1% 1/10W MF-LF 402

R7554 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUMG_N

NOSTUFF C7574 330PF 10% 50V CERM 402

CPUIMVP_ISUMG_P

SYNC_MASTER=K91_ERIC	SYNC_DATE=09/22/2010
PAGE TITLE: CPU IMVP7 & AXG VCore Output	
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	BRANCH:
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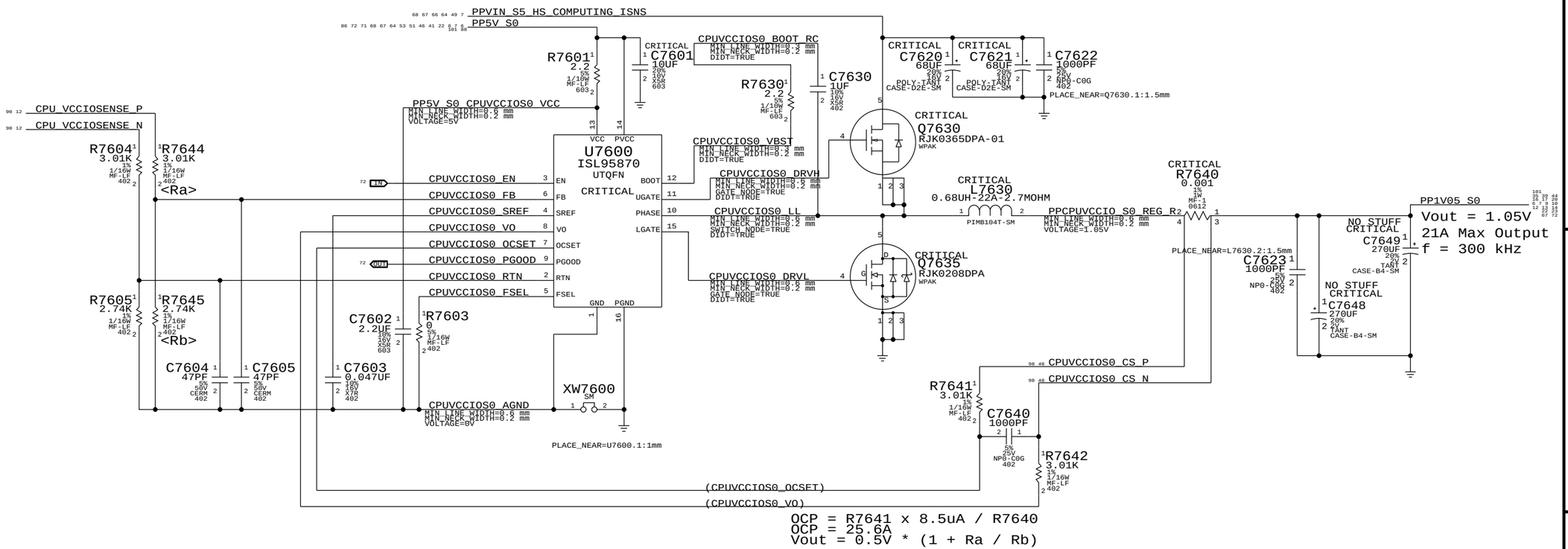
CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE

CPU VCCIO (1.05V) Power Supply

Apple Inc.

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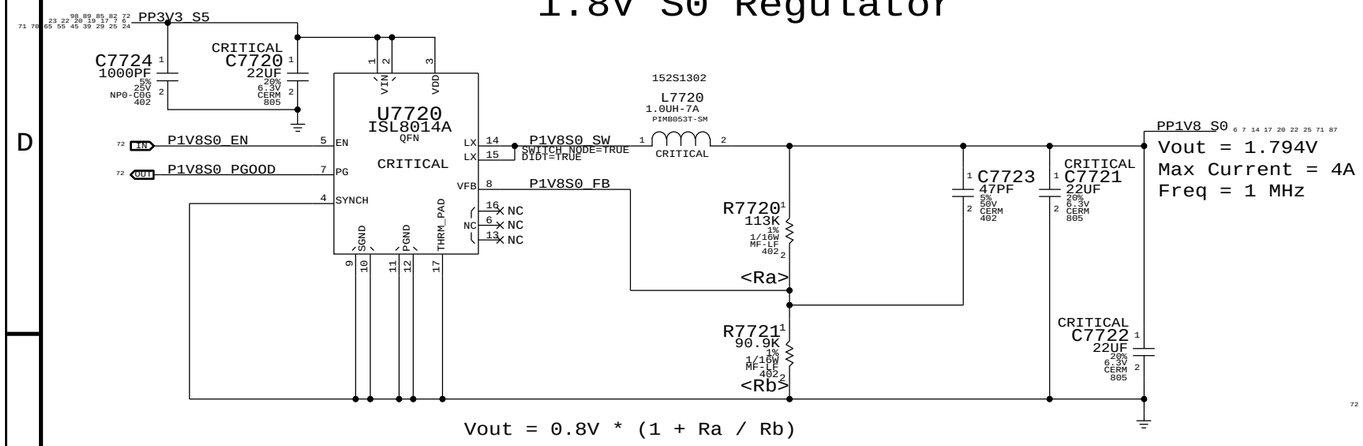
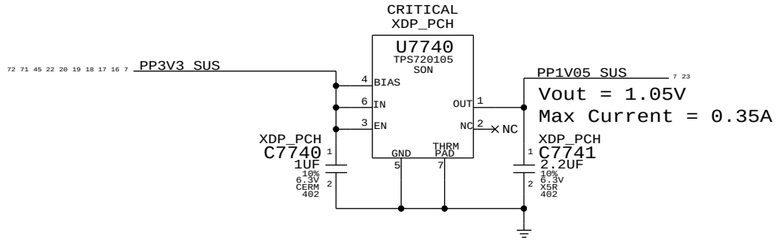
1.8V S0 Regulator



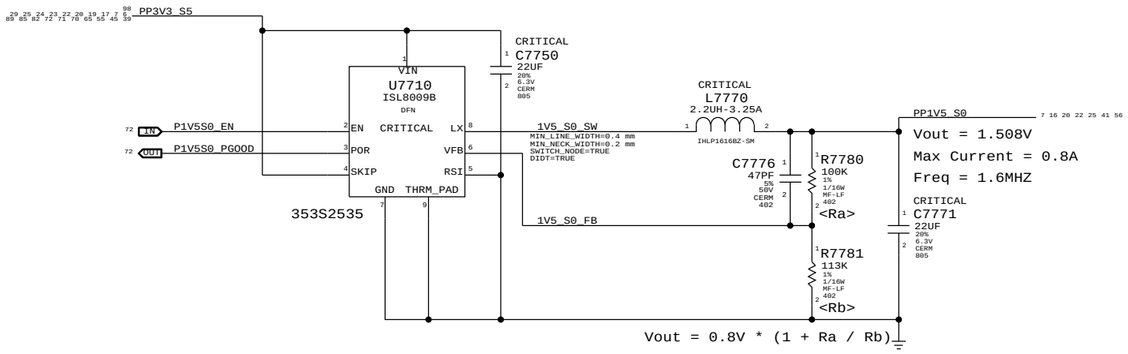
Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

Cougar Point-M requires JTAG pull-ups to be powered at 1.05V in Sus.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.

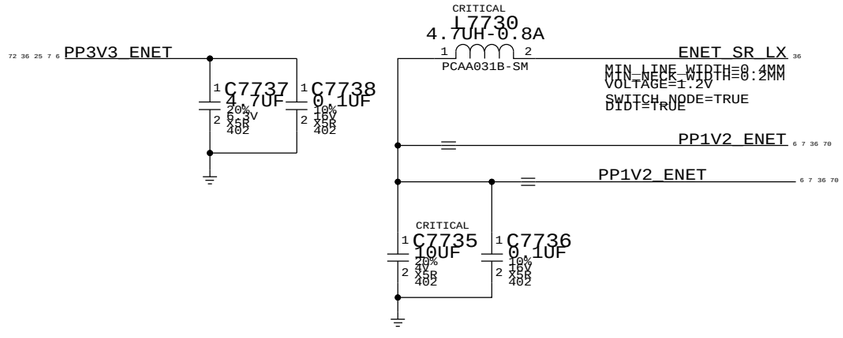


1.5V S0 Regulator

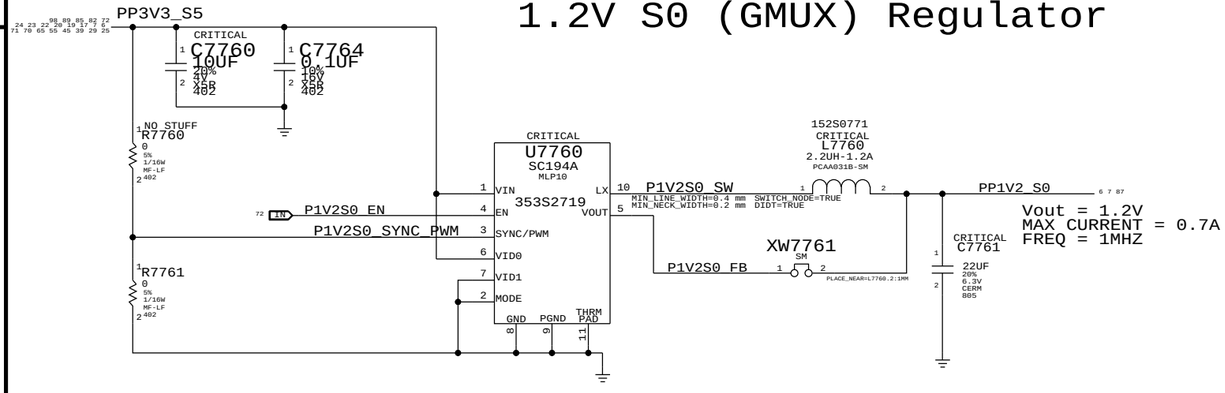


Vout = 0.8V * (1 + Ra / Rb)

CAESAR IV 1.2V INT.VR CMPTS



1.2V S0 (GMUX) Regulator



SYNC_MASTER=K91_ERIC	SYNC_DATE=11/01/2010
PAGE TITLE	Misc Power Supplies
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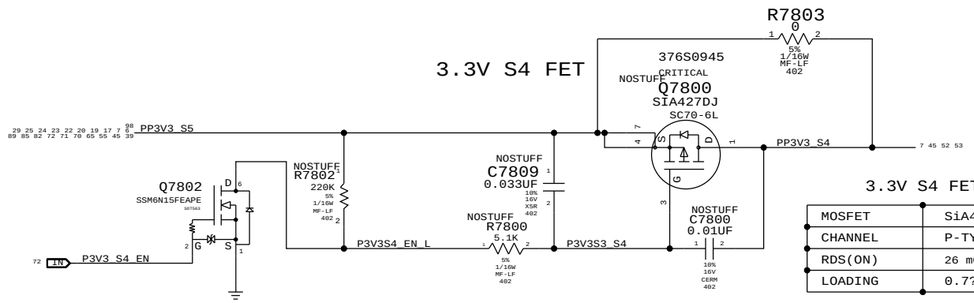
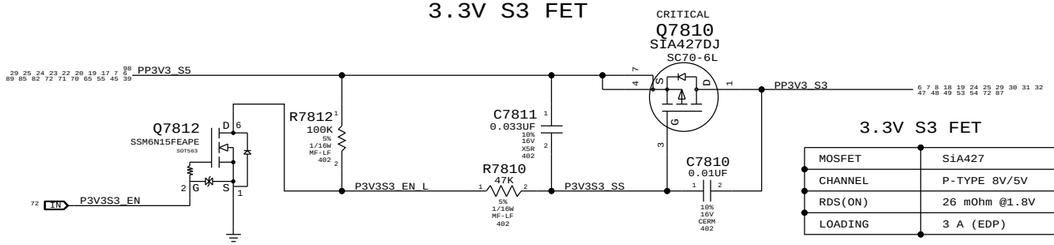
3.3V S4 FET



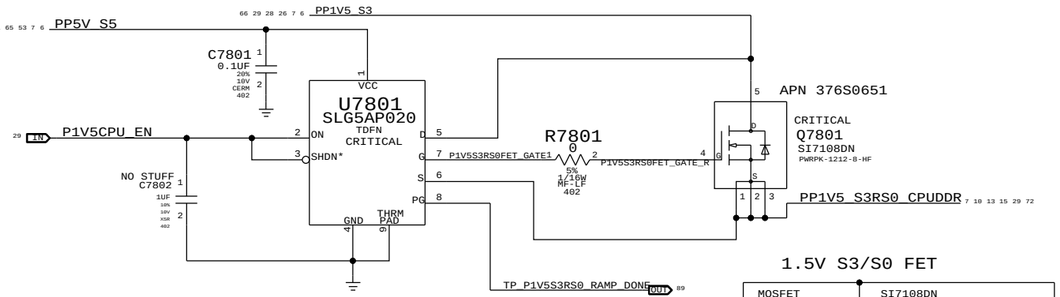
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET



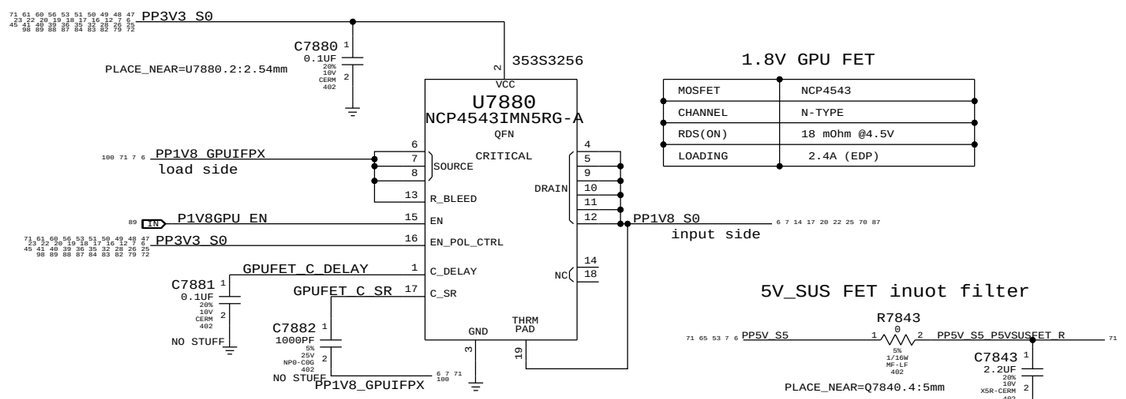
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET



1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

1.8V GPU FET

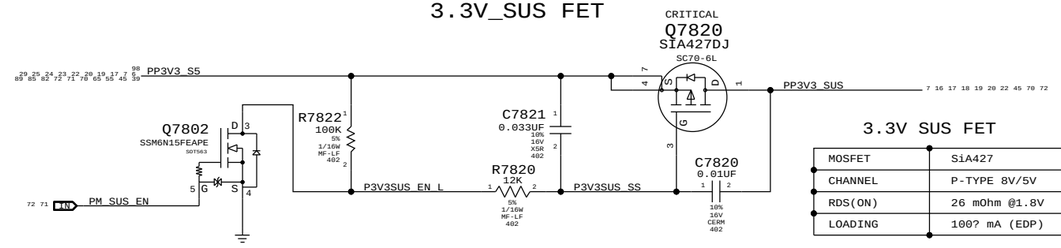


1.8V GPU FET	
MOSFET	NCP4543
CHANNEL	N-TYPE
RDS(ON)	18 mOhm @4.5V
LOADING	2.4A (EDP)

5V_SUS FET inuot filter

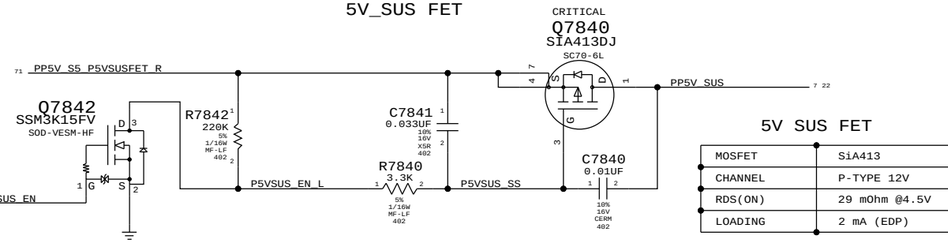
U7880 default Turn on delay EN--> on is 200~650us.

3.3V_SUS FET



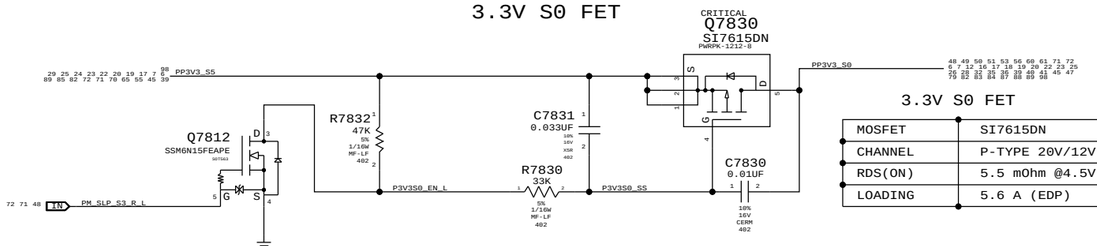
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



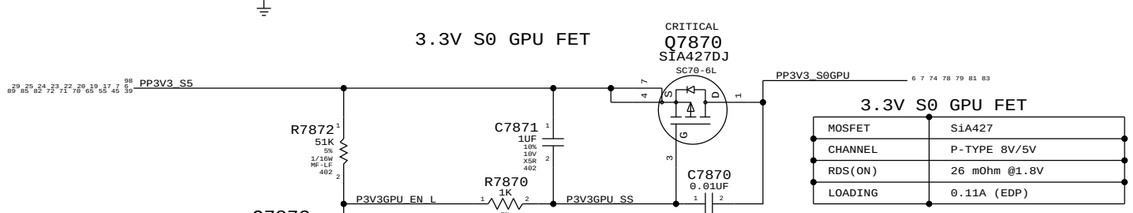
5V SUS FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

3.3V S0 FET



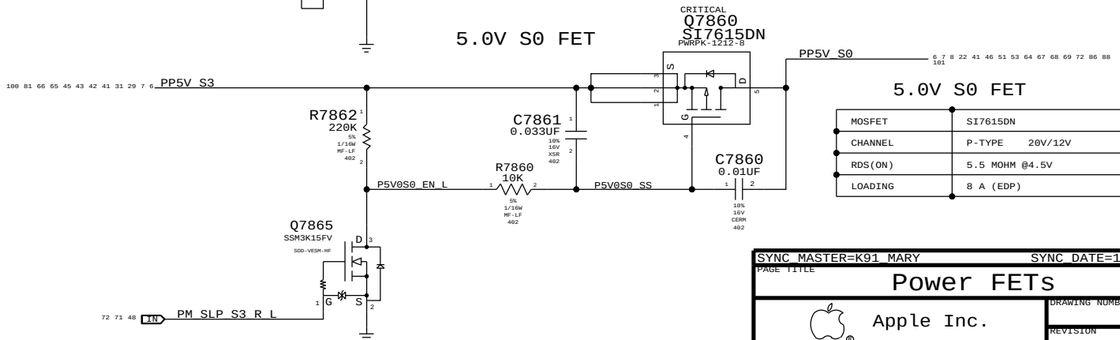
3.3V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

3.3V S0 GPU FET



3.3V S0 GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	8 A (EDP)

SYNC_MASTER=K91_MARY SYNC_DATE=10/14/2016

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Apple Inc.

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S5 Rail Enables & PGOOD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

SMC_PM_G2_EN
SMC_PM_G2_EN MAKE_BASE=TRUE
R7940 100 5% 1/16W MF-LF 402
PLACE_NEAR=U7201.21:7mm
C7942 0.0033UF 10% 50V CERM 402 NO STUFF
P3V3S5_EN MAKE_BASE=TRUE
P3V3S5_EN
PP3V42_G3H
PLACE_NEAR=U7201.20:7mm
R7941 100K 5% 1/16W MF-LF 402
S5_PWRGD
S5_PWRGD MAKE_BASE=TRUE
S5_PWRGD (old name RSMRST_PWRGD)-->SMC
SMC-->PM_DSW_PWRGD

3.3V/5.0V S4 ENABLE

NOSTUFF
R7916 0 5% 1/16W MF-LF 402
PLACE_NEAR=U1800.G18:5mm
PM_SLP_S5_L
P3V3_S4_EN MAKE_BASE=TRUE
P3V3_S4_EN
PM_SLP_S5_L:100K pull down on PCH page

3.3V,5V S3 ENABLE

PM_SLP_S4_L
PM_SLP_S4_L MAKE_BASE=TRUE
PM_SLP_S4_L:100K pull down in PCH page
R7911 5.1K 5% 1/16W MF-LF 402 PLACE_NEAR=U7300.16:6mm
R7912 0 5% 1/16W MF-LF 402 PLACE_NEAR=Q7812.2:6mm
R7913 3.3K 5% 1/16W MF-LF 402
PLACE_NEAR=U5701.4:6mm
TPAD_VBUS_EN
P3V3S3_EN MAKE_BASE=TRUE
P3V3S3_EN
DDRREG_EN MAKE_BASE=TRUE
DDRREG_EN
C7910 0.47UF 10% 6.3V CERM-X5R 402
C7912 0.47UF 10% 6.3V CERM-X5R 402 NO STUFF

3.3V/5.0V Sus ENABLE

PP3V3_S5
PLACE_NEAR=U7940.1:2.3mm
C7940 0.1uF 20% 10V CERM 402
U7940 74AUP1G3208 SOT891
SMC_BATLOW_L:100K pull up on SMC page
SMC_BATLOW_L
PM_SLP_SUS_L:100K pull down on PCH page
PM_SLP_SUS_L
PM_SUS_EN MAKE_BASE=TRUE
PM_SUS_EN
PM_SUS_EN
NO STUFF R7917 0 5% 1/16W MF-LF 402

S0 ENABLE

R7978 100 5% 1/16W MF-LF 402
PM_SLP_S3_L
PM_SLP_S3_L:100K pull down in PCH page
(PM_SLP_S3_R_L)
PM_SLP_S3_R_L MAKE_BASE=TRUE
PM_SLP_S3_R_L
PM_SLP_S3_R_L
PM_SLP_S3_R_L
R7987 33K 5% 1/16W MF-LF 402 PLACE_NEAR=U7100.15:6mm
R7981 20K 5% 1/16W MF-LF 402 PLACE_NEAR=U7600.3:6mm
R7985 20K 5% 1/16W MF-LF 402 PLACE_NEAR=U7760.4:6mm
R7988 10K 5% 1/16W MF-LF 402 PLACE_NEAR=U7720.5:6mm
R7986 5.1K 5% 1/16W MF-LF 402
P1V8S0_EN MAKE_BASE=TRUE
P1V8S0_EN
P1V5S0_EN MAKE_BASE=TRUE
P1V5S0_EN
P1V2S0_EN MAKE_BASE=TRUE
P1V2S0_EN
CPUVCCIOS0_EN MAKE_BASE=TRUE
CPUVCCIOS0_EN
PVCCSA_EN MAKE_BASE=TRUE
PVCCSA_EN
C7987 0.47UF 10% 6.3V CERM-X5R 402 PLACE_NEAR=U7100.15:6mm
C7981 0.47UF 10% 6.3V CERM-X5R 402 PLACE_NEAR=U7600.3:6mm
C7985 1UF 10% 6.3V CERM-X5R 402 PLACE_NEAR=U7760.4:6mm
C7988 0.47UF 10% 6.3V CERM-X5R 402 PLACE_NEAR=U7710.2:6mm
C7986 0.47UF 10% 6.3V CERM-X5R 402 PLACE_NEAR=U7720.5:6mm

CPUVCORE ENABLE

ALL_SYS_PWRGD
CPUIMVP_VR_ON
R7974 0 5% 1/16W MF-LF 402 PLACE_NEAR=U7400.7:5mm
R7976 0 5% 1/16W MF-LF 402 NO STUFF PLACE_NEAR=U7400.7:5mm
CPUVCCIOS0_PGOOD
PM_PECI_PWRGD
R7975 0 5% 1/16W MF-LF 402 PLACE_NEAR=U7400.7:5mm

CHGR VFRQ Generation

PP3V42_G3H
R7931 100K 5% 1/16W MF-LF 402
CHGR_VFRQ
Q7931 SSM3K15FV SOD-VESM-HF

VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

S0 Rail PGOOD (BJT Version)

PP3V3_S5
PP3V3_S0
R7951 15.0K 1% 1/16W MF-LF 402
R7956 150K 1% 1/16W MF-LF 402
S0PGD_C
ALL_SYS_PWRGD
R7953 1K 5% 1/16W MF-LF 402
VMON_3V3_DIV
VMON_Q2_BASE
R7952 7.15K 1% 1/16W MF-LF 402
R7954 1K 5% 1/16W MF-LF 402
NC
VMON_Q3_BASE
PP1V5_S3RS0_CPUDDR
PP1V5_S3RS0
Q7950 ASMCC0179 DFN2015H4-8 CRITICAL
R7955 1K 5% 1/16W MF-LF 402
PP1V05_S0
VMON_Q4_BASE
353S2809
S0PGD_BJT_GND_R
R7957 100 5% 1/16W MF-LF 402
Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

3.3V SUS Detect

PP3V3_S5
PLACE_NEAR=U7930.6:2.3mm
No stuff C7931, 12ms Min delay time
U7930 Sense input threhold is 3.07V
C7930 0.1uF 20% 16V CERM 402
R7933 100K 5% 1/16W MF-LF 402
PP3V3_SUS
CRITICAL
U7930 TPS3808G33DBVRG4 SOT23-6
PP3V3_SUS
PM_RSMRST_L
PM_RSMRST_L goes to U1800.C21
Sus_PGOOD_CT
C7931 0.001UF 10% 50V CERM 402 NO STUFF

ENET Enable Generation

3.3V ENET FET

PP3V3_S3
R7921 10K 5% 1/16W MF-LF 402
R7922 100K 5% 1/16W MF-LF 402
PM_SLP_S3_ENET
C7921 0.033UF 10% 16V CERM 402
P3V3ENET_SS
C7922 0.01UF 10% 16V CERM 402
PP3V3_ENET
Q7922 NTR4101P SOT-23-HF CRITICAL
Q7921 SSM3K15FV SOD-VESM-HF
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.
PM_SLP_S3_L
Q7925 2N7002DW-X-G SOT-363
PM_WLAN_EN_L
Q7925 2N7002DW-X-G SOT-363
AP_PWR_EN
WOL_EN
AC_EN_L
(AC_EN_L)
Q7920 2N7002DW-X-G SOT-363
NO STUFF R7929 0 5% 1/16W MF-LF 402
Q7920 2N7002DW-X-G SOT-363
SMC_ADAPTER_EN
(PM_SLP_S3_L)

S0 Rail PGOOD Circuitry (ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

PP5V_S0
PP1V5_S3RS0_CPUDDR
PP1V05_S0
S0PGOOD_ISL
R7960 6.04K 1%
R7970 10K 1%
R7972 6.04K 1%
R7961 15.0K 1%
R7971 10K 1%
R7973 15.0K 1%
PP5V_DIV_VMON
PP1V05_DIV_VMON
PP1V05_VID_VMON
C7960 0.1uF 20% 10V CERM 402
U7960 ISL88042IRTEZ TDFN (IPU) CRITICAL
V2MON
V3MON
V4MON
MR*
RST*
GND
THRM_PAD
353S2310
S0PGOOD_ISL
R7962 330 5%
ALL_SYS_PWRGD_R
ALL_SYS_PWRGD
PP3V3_S0
R7967 10K 5%
R7968 100 5%
P1V5S0_PGOOD
P1V5S0_PGOOD from U7710
P1V8S0_PGOOD
R7966 100 5%
R7965 100 5%
P5VS3_PGOOD
R7964 100 5%
CPUVCCIOS0_PGOOD
R7963 100 5%
PVCCSA_PGOOD
SMC_S4_WAKESRC_EN MAKE_BASE=TRUE
SMC_S4_WAKESRC_EN

SYNC_MASTER=K91_MARY SYNC_DATE=07/22/2010
PAGE TITLE
Power Control 1/ENABLE
Apple Inc.
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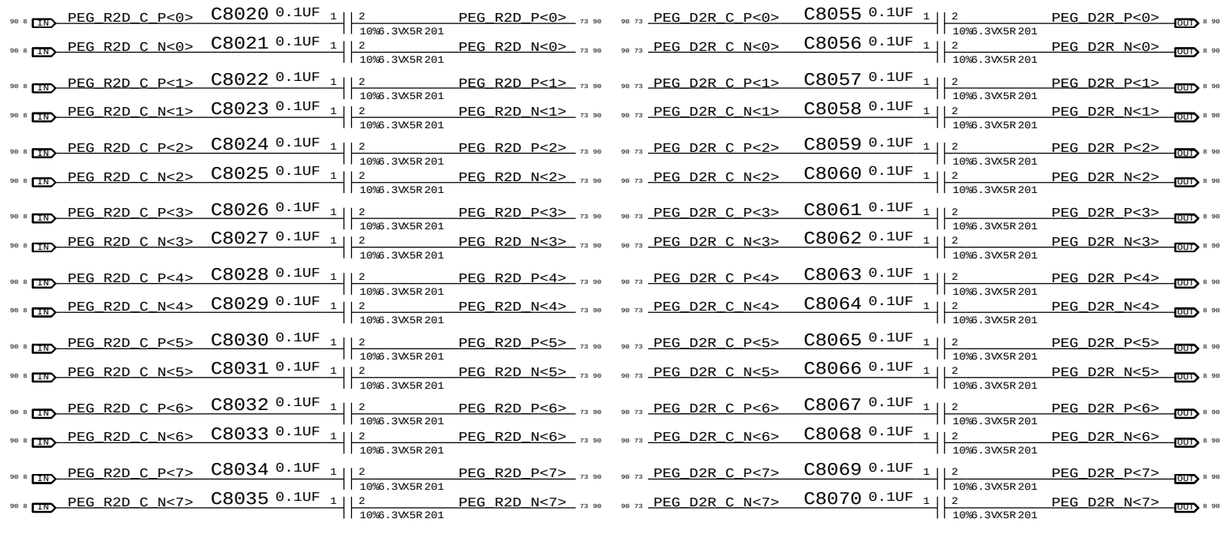
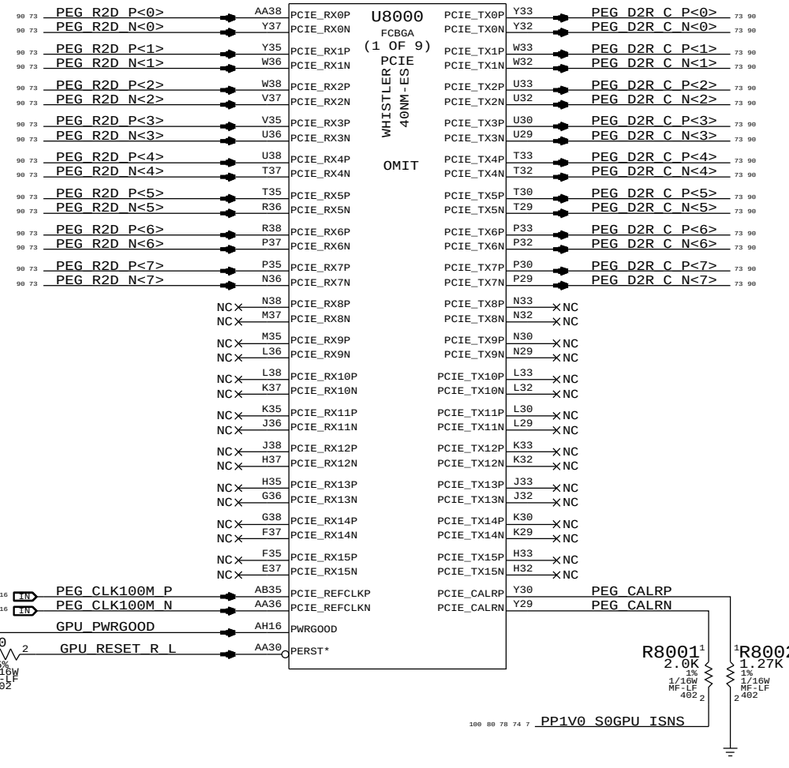
Page Notes

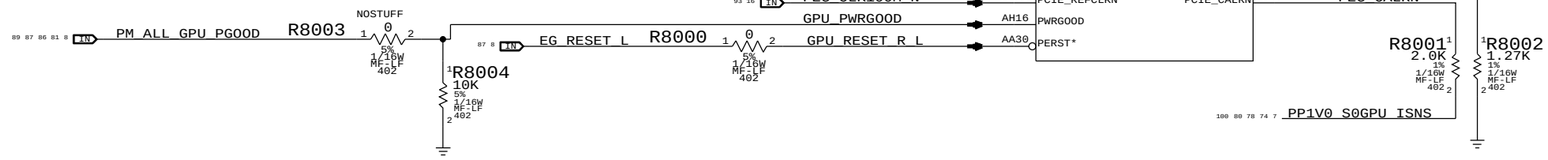
Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)







SYNC_MASTER=K92_SUMA SYNC_DATE=06/15/2010

PAGE TITLE: Whistler PCI-E

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

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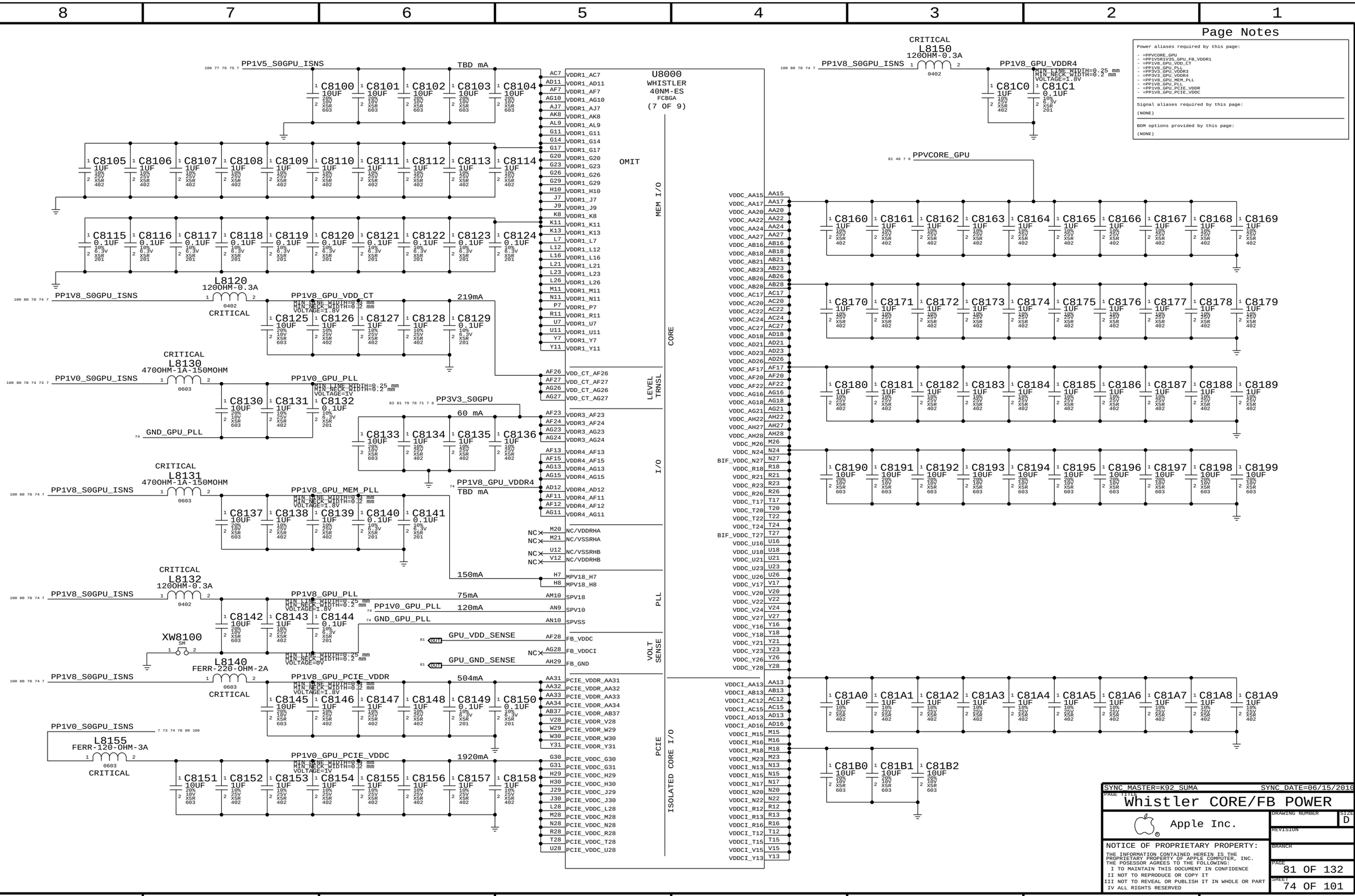
Page Notes
Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V5R1V35_GPU_FB_VDDR1
- =PP1V8_GPU_VDD_CT
- =PP1V0_GPU_PLL
- =PP3V3_GPU_VDDR3
- =PP3V3_GPU_VDDR4
- =PP1V8_GPU_MEM_PLL
- =PP1V8_GPU_PLL
- =PP1V8_GPU_PCIE_VDDR
- =PP1V8_GPU_PCIE_VDDC
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
U8000
WHISTLER
40NM-ES
FCBGA
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MEM I/O
CORE
LEVEL TRNSL
I/O
PLL
VOLT SENSE
PCIE
ISOLATED CORE I/O
PP1V5_S0GPU_ISNS
TBD mA
PP1V8_S0GPU_ISNS
PP1V8_GPU_VDD_CT
219mA
PP1V0_S0GPU_ISNS
PP1V0_GPU_PLL
PP3V3_S0GPU
60 mA
PP1V8_GPU_VDDR4
PP1V8_GPU_MEM_PLL
PP1V8_GPU_PLL
PP1V8_GPU_PCIE_VDDR
PP1V0_GPU_PCIE_VDDC
1920mA
PPVCORE_GPU
OMIT
150mA
75mA
120mA
GPU_VDD_SENSE
GPU_GND_SENSE
504mA
GND_GPU_PLL
CRITICAL
L8120
120OHM-0.3A
L8130
470OHM-1A-150MOHM
L8131
470OHM-1A-150MOHM
L8132
120OHM-0.3A
L8140
FERR-220-OHM-2A
L8150
120OHM-0.3A
L8155
FERR-120-OHM-3A
XW8100
SM
SYNC_MASTER=K92_SUMA
SYNC_DATE=06/15/2010
PAGE TITLE
Whistler CORE/FB POWER
Apple Inc.
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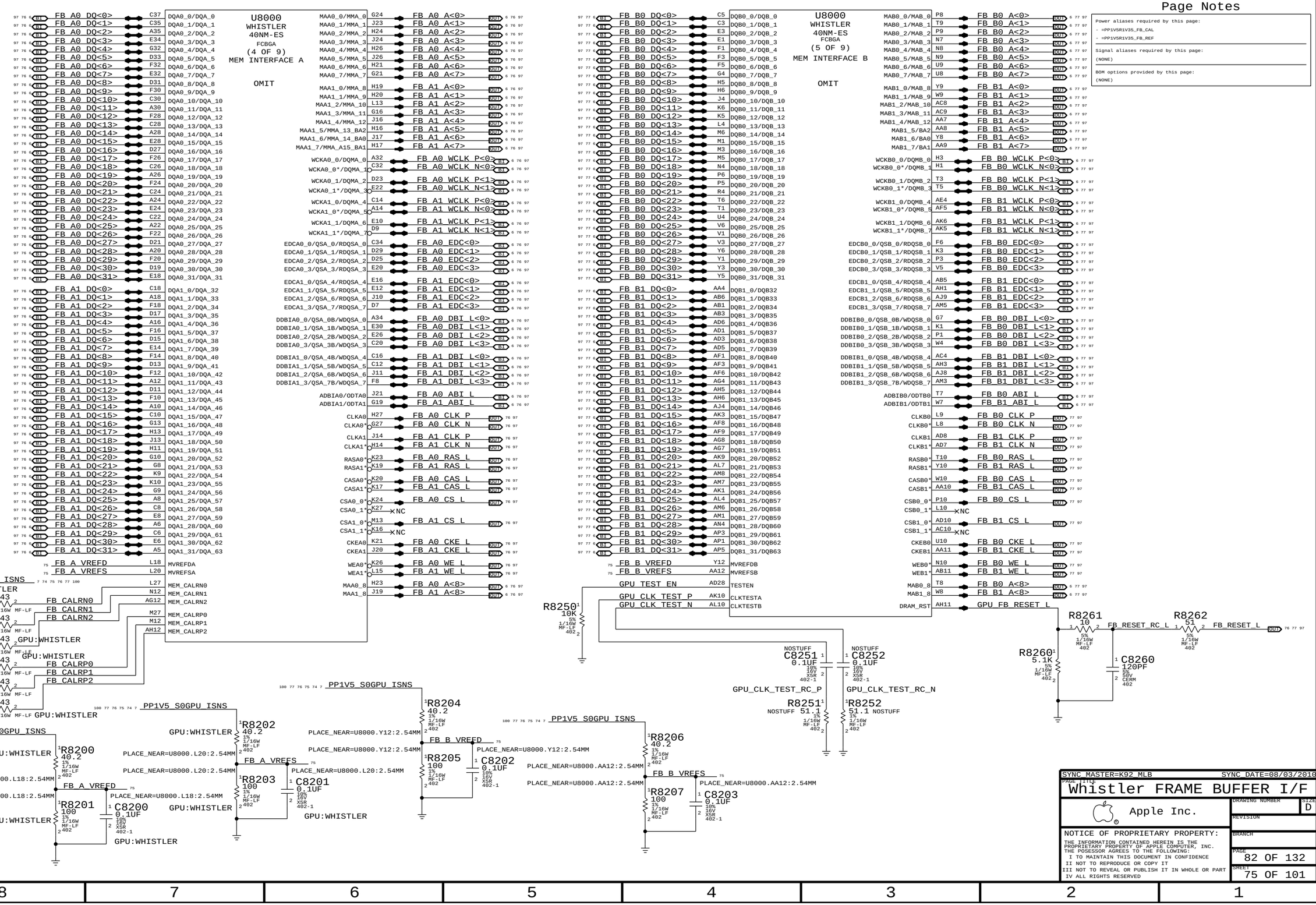
U8000
WHISTLER
40NM-ES
FCBGA
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MEM INTERFACE A
OMIT
U8000
WHISTLER
40NM-ES
FCBGA
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MEM INTERFACE B
OMIT
Page Notes
Power aliases required by this page:
- =PP1V5R1V35_FB_CAL
- =PP1V5R1V35_FB_REF
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
PP1V5_S0GPU_ISNS
GPU:WHISTLER
FB_A_VREFD
FB_A_VREFS
FB_B_VREFD
FB_B_VREFS
GPU_TEST_EN
GPU_CLK_TEST_P
GPU_CLK_TEST_N
GPU_CLK_TEST_RC_P
GPU_CLK_TEST_RC_N
FB_RESET_RC_L
FB_RESET_L
GPU_FB_RESET_L
NOSTUFF
PLACE_NEAR=U8000.L18:2.54MM
PLACE_NEAR=U8000.L20:2.54MM
PLACE_NEAR=U8000.Y12:2.54MM
PLACE_NEAR=U8000.AA12:2.54MM
SYNC_MASTER=K92_MLB
SYNC_DATE=08/03/2016
PAGE TITLE
Whistler FRAME BUFFER I/F
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Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
GPU:WHISTLER is the BOM option called out on all Rs and Cs on this page

GPU:WHISTLER is the BOM option called out on ALL Rs and Cs on this page!

U8400 — 32MX32-1.25GHZ-MFL

BGA
H5GQ1H24AFR-T2C

(1 OF 2)

OMIT

FB_A0_A<2>	H11	BA0/A2	
FB_A0_A<5>	K10	BA1/A5	
FB_A0_A<4>	K11	BA2/A4	
FB_A0_A<3>	H10	BA3/A3	
FB_A0_A<7>	K4	A8/A7	
FB_A0_A<1>	H5	A9/A1	
FB_A0_A<0>	H4	A10/A0	
FB_A0_A<6>	K5	A11/A6	
FB_A0_CKE_L	J3	CKE*	
FB_A0_CLK_P	J12	CK	
FB_A0_CLK_N	J11	CK*	
FB_A0_CS_L	G12	CS*	
FB_A0_WE_L	L12	WE*	
FB_A0_CAS_L	L3	CAS*	
FB_A0_RAS_L	G3	RAS*	
FB_A0_ZQ	J13	ZQ	
FB_A0_MF	J1	MF (MF=0)	
FB_A0_SEN	J10	SEN	
FB_RESET_L	J2	RESET*	
FB_A0_ABI_L	J4	ABI*	
FB_A0_EDC<0>	C2	EDC0	
FB_A0_EDC<1>	C13	EDC1	
FB_A0_EDC<3>	R13	EDC2	
FB_A0_EDC<2>	R2	EDC3	
FB_A0_WCLK_P<0>	D4	WCK01	
FB_A0_WCLK_N<0>	D5	WCK01*	
FB_A0_WCLK_P<1>	P4	WCK23	
FB_A0_WCLK_N<1>	P5	WCK23*	

PP1V5_S0GPU_ISNS

R8401 60.4 1% 1/16W MF-LF 402
R8402 60.4 1% 1/16W MF-LF 402

R8400 120 1% 1/20W MF 201
R8404 120 1% 1/20W MF 201
R8403 120 1% 1/20W MF 201

DBI0*	D2	FB_A0_DBI_L<0>
DBI1*	D13	FB_A0_DBI_L<1>
DBI2*	P13	FB_A0_DBI_L<3>
DBI3*	P2	FB_A0_DBI_L<2>
DQ0	A4	FB_A0_DQ<0>
DQ1	A2	FB_A0_DQ<1>
DQ2	B4	FB_A0_DQ<2>
DQ3	B2	FB_A0_DQ<3>
DQ4	E4	FB_A0_DQ<4>
DQ5	E2	FB_A0_DQ<5>
DQ6	F4	FB_A0_DQ<6>
DQ7	F2	FB_A0_DQ<7>
DQ8	A11	FB_A0_DQ<8>
DQ9	A13	FB_A0_DQ<9>
DQ10	B11	FB_A0_DQ<10>
DQ11	B13	FB_A0_DQ<11>
DQ12	E11	FB_A0_DQ<13>
DQ13	E13	FB_A0_DQ<12>
DQ14	F11	FB_A0_DQ<15>
DQ15	F13	FB_A0_DQ<31>
DQ16	U11	FB_A0_DQ<30>
DQ17	U13	FB_A0_DQ<29>
DQ18	T11	FB_A0_DQ<28>
DQ19	T13	FB_A0_DQ<26>
DQ20	N11	FB_A0_DQ<27>
DQ21	N13	FB_A0_DQ<24>
DQ22	M11	FB_A0_DQ<25>
DQ23	M13	FB_A0_DQ<20>
DQ24	U4	FB_A0_DQ<23>
DQ25	U2	FB_A0_DQ<21>
DQ26	T4	FB_A0_DQ<22>
DQ27	T2	FB_A0_DQ<17>
DQ28	N4	FB_A0_DQ<18>
DQ29	N2	FB_A0_DQ<16>
DQ30	M4	FB_A0_DQ<19>
DQ31	M2	
NC	A5, J5, U5	NC
		FB_A0_A<8>

PP1V5_S0GPU_ISNS

R8430 2.37K 1% 1/16W MF-LF 402
R8431 5.49K 1% 1/16W MF-LF 402
R8432 2.37K 1% 1/16W MF-LF 402
R8433 5.49K 1% 1/16W MF-LF 402
R8434 2.37K 1% 1/16W MF-LF 402
R8435 5.49K 1% 1/16W MF-LF 402

C8430 1UF 10% 6.3V CERM-X5R 402
C8431 1UF 10% 6.3V CERM-X5R 402
C8432 1UF 10% 6.3V CERM-X5R 402
C8433 1UF 10% 6.3V CERM-X5R 402
C8434 1UF 10% 6.3V CERM-X5R 402
C8435 1UF 10% 6.3V CERM-X5R 402

FB_A0_VREFC
FB_A0_VREFD1
FB_A0_VREFD2

U8400 — 32MX32-1.25GHZ-MFL

BGA
H5GQ1H24AFR-T2C

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OMIT

VDD	C5, C10, D11, G1, G4, G11, G14, L1, L4, L11, L14, P11, R5, R10	
VDDQ	B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14	
VSS	B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10	
VSSQ	A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14	
VREFC	J14	FB_A0_VREFC
VREFD	A10, U10	FB_A0_VREFD1, FB_A0_VREFD2

C8400 4.7UF 20% 6.3V X5R 402
C8401 4.7UF 20% 6.3V X5R 402
C8402 4.7UF 20% 6.3V X5R 402
C8403 4.7UF 20% 6.3V X5R 402
C8404 4.7UF 20% 6.3V X5R 402
C8405 4.7UF 20% 6.3V X5R 402
C8406 1UF 10% 6.3V CERM-X5R 402
C8407 1UF 10% 6.3V CERM-X5R 402
C8408 1UF 10% 6.3V CERM-X5R 402
C8409 1UF 10% 6.3V CERM-X5R 402
C8410 1UF 10% 6.3V CERM-X5R 402
C8411 1UF 10% 6.3V CERM-X5R 402
C8412 1UF 10% 6.3V CERM-X5R 402
C8413 1UF 10% 6.3V CERM-X5R 402
C8414 1UF 10% 6.3V CERM-X5R 402
C8415 1UF 10% 6.3V CERM-X5R 402
C8416 0.1UF 10% 6.3V X5R 201
C8417 0.1UF 10% 6.3V X5R 201
C8418 0.1UF 10% 6.3V X5R 201
C8419 0.1UF 10% 6.3V X5R 201
C8420 0.1UF 10% 6.3V X5R 201
C8421 0.1UF 10% 6.3V X5R 201
C8422 0.1UF 10% 6.3V X5R 201
C8423 0.1UF 10% 6.3V X5R 201
C8424 0.1UF 10% 6.3V X5R 201
C8425 0.1UF 10% 6.3V X5R 201

U8450 — 32MX32-1.25GHZ-MFL

BGA
H5GQ1H24AFR-T2C

(1 OF 2)

OMIT

FB_A1_A<2>	H11	BA0/A2	
FB_A1_A<5>	K10	BA1/A5	
FB_A1_A<4>	K11	BA2/A4	
FB_A1_A<3>	H10	BA3/A3	
FB_A1_A<7>	K4	A8/A7	
FB_A1_A<1>	H5	A9/A1	
FB_A1_A<0>	H4	A10/A0	
FB_A1_A<6>	K5	A11/A6	
FB_A1_CKE_L	J3	CKE*	
FB_A1_CLK_P	J12	CK	
FB_A1_CLK_N	J11	CK*	
FB_A1_CS_L	G12	CS*	
FB_A1_WE_L	L12	WE*	
FB_A1_CAS_L	L3	CAS*	
FB_A1_RAS_L	G3	RAS*	
FB_A1_ZQ	J13	ZQ	
FB_A1_MF	J1	MF (MF=0)	
FB_A1_SEN	J10	SEN	
FB_RESET_L	J2	RESET*	
FB_A1_ABI_L	J4	ABI*	
FB_A1_EDC<0>	C2	EDC0	
FB_A1_EDC<1>	C13	EDC1	
FB_A1_EDC<2>	R13	EDC2	
FB_A1_EDC<3>	R2	EDC3	
FB_A1_WCLK_P<0>	D4	WCK01	
FB_A1_WCLK_N<0>	D5	WCK01*	
FB_A1_WCLK_P<1>	P4	WCK23	
FB_A1_WCLK_N<1>	P5	WCK23*	

PP1V5_S0GPU_ISNS

R8451 60.4 1% 1/16W MF-LF 402
R8452 60.4 1% 1/16W MF-LF 402

R8450 120 1% 1/20W MF 201
R8454 120 1% 1/20W MF 201
R8453 120 1% 1/20W MF 201

DBI0*	D2	FB_A1_DBI_L<0>
DBI1*	D13	FB_A1_DBI_L<1>
DBI2*	P13	FB_A1_DBI_L<2>
DBI3*	P2	FB_A1_DBI_L<3>
DQ0	A4	FB_A1_DQ<1>
DQ1	A2	FB_A1_DQ<0>
DQ2	B4	FB_A1_DQ<3>
DQ3	B2	FB_A1_DQ<2>
DQ4	E4	FB_A1_DQ<4>
DQ5	E2	FB_A1_DQ<6>
DQ6	F4	FB_A1_DQ<5>
DQ7	F2	FB_A1_DQ<7>
DQ8	A11	FB_A1_DQ<9>
DQ9	A13	FB_A1_DQ<8>
DQ10	B11	FB_A1_DQ<11>
DQ11	B13	FB_A1_DQ<10>
DQ12	E11	FB_A1_DQ<12>
DQ13	E13	FB_A1_DQ<13>
DQ14	F11	FB_A1_DQ<14>
DQ15	F13	FB_A1_DQ<15>
DQ16	U11	FB_A1_DQ<21>
DQ17	U13	FB_A1_DQ<22>
DQ18	T11	FB_A1_DQ<23>
DQ19	T13	FB_A1_DQ<20>
DQ20	N11	FB_A1_DQ<18>
DQ21	N13	FB_A1_DQ<19>
DQ22	M11	FB_A1_DQ<17>
DQ23	M13	FB_A1_DQ<16>
DQ24	U4	FB_A1_DQ<31>
DQ25	U2	FB_A1_DQ<30>
DQ26	T4	FB_A1_DQ<28>
DQ27	T2	FB_A1_DQ<29>
DQ28	N4	FB_A1_DQ<25>
DQ29	N2	FB_A1_DQ<27>
DQ30	M4	FB_A1_DQ<24>
DQ31	M2	FB_A1_DQ<26>
NC	A5, J5, U5	NC
		FB_A1_A<8>

PP1V5_S0GPU_ISNS

R8480 2.37K 1% 1/16W MF-LF 402
R8481 5.49K 1% 1/16W MF-LF 402
R8482 2.37K 1% 1/16W MF-LF 402
R8483 5.49K 1% 1/16W MF-LF 402
R8484 2.37K 1% 1/16W MF-LF 402
R8485 5.49K 1% 1/16W MF-LF 402

C8480 1UF 10% 6.3V CERM-X5R 402
C8481 1UF 10% 6.3V CERM-X5R 402
C8482 1UF 10% 6.3V CERM-X5R 402
C8483 1UF 10% 6.3V CERM-X5R 402
C8484 1UF 10% 6.3V CERM-X5R 402
C8485 1UF 10% 6.3V CERM-X5R 402

FB_A1_VREFC
FB_A1_VREFD1
FB_A1_VREFD2

U8450 — 32MX32-1.25GHZ-MFL

BGA
H5GQ1H24AFR-T2C

(2 OF 2)

OMIT

VDD	C5, C10, D11, G1, G4, G11, G14, L1, L4, L11, L14, P11, R5, R10	
VDDQ	B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14	
VSS	B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10	
VSSQ	A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14	
VREFC	J14	FB_A1_VREFC
VREFD	A10, U10	FB_A1_VREFD1, FB_A1_VREFD2

C8450 4.7UF 20% 6.3V X5R 402
C8451 4.7UF 20% 6.3V X5R 402
C8452 4.7UF 20% 6.3V X5R 402
C8453 4.7UF 20% 6.3V X5R 402
C8454 4.7UF 20% 6.3V X5R 402
C8455 4.7UF 20% 6.3V X5R 402
C8456 1UF 10% 6.3V CERM-X5R 402
C8457 1UF 10% 6.3V CERM-X5R 402
C8458 1UF 10% 6.3V CERM-X5R 402
C8459 1UF 10% 6.3V CERM-X5R 402
C8460 1UF 10% 6.3V CERM-X5R 402
C8461 1UF 10% 6.3V CERM-X5R 402
C8462 1UF 10% 6.3V CERM-X5R 402
C8463 1UF 10% 6.3V CERM-X5R 402
C8464 1UF 10% 6.3V CERM-X5R 402
C8465 1UF 10% 6.3V CERM-X5R 402
C8466 0.1UF 10% 6.3V X5R 201
C8467 0.1UF 10% 6.3V X5R 201
C8468 0.1UF 10% 6.3V X5R 201
C8469 0.1UF 10% 6.3V X5R 201
C8470 0.1UF 10% 6.3V X5R 201
C8471 0.1UF 10% 6.3V X5R 201
C8472 0.1UF 10% 6.3V X5R 201
C8473 0.1UF 10% 6.3V X5R 201
C8474 0.1UF 10% 6.3V X5R 201
C8475 0.1UF 10% 6.3V X5R 201

SYNC_MASTER=K92_MLB
SYNC_DATE=08/19/2010

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Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT

U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT

PP1V5_S0GPU_ISNS

R8501 60.4 1% 1/16W MF-LF 402
R8502 60.4 1% 1/16W MF-LF 402
R8551 60.4 1% 1/16W MF-LF 402
R8552 60.4 1% 1/16W MF-LF 402

R8500 120 1% 1/20W MF 201
R8504 120 1% 1/20W MF 201
R8503 120 1% 1/20W MF 201
R8550 120 1% 1/20W MF 201
R8554 120 1% 1/20W MF 201
R8553 120 1% 1/20W MF 201

FB_B0_A<2>	H11	BA0/A2	
FB_B0_A<5>	K10	BA1/A5	
FB_B0_A<4>	K11	BA2/A4	
FB_B0_A<3>	H10	BA3/A3	
FB_B0_A<7>	K4	A8/A7	
FB_B0_A<1>	H5	A9/A1	
FB_B0_A<0>	H4	A10/A0	
FB_B0_A<6>	K5	A11/A6	
FB_B0_CKE_L	J3	CKE*	
FB_B0_CLK_P	J12	CK	
FB_B0_CLK_N	J11	CK*	
FB_B0_CS_L	G12	CS*	
FB_B0_WE_L	L12	WE*	
FB_B0_CAS_L	L3	CAS*	
FB_B0_RAS_L	G3	RAS*	
FB_B0_ZQ	J13	ZQ	
FB_B0_MF	J1	MF (MF=0)	
FB_B0_SEN	J10	SEN	
FB_RESET_L	J2	RESET*	
FB_B0_ABI_L	J4	ABI*	
FB_B0_EDC<0>	C2	EDC0	
FB_B0_EDC<1>	C13	EDC1	
FB_B0_EDC<3>	R13	EDC2	
FB_B0_EDC<2>	R2	EDC3	
FB_B0_WCLK_P<0>	D4	WCK01	
FB_B0_WCLK_N<0>	D5	WCK01*	
FB_B0_WCLK_P<1>	P4	WCK23	
FB_B0_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_B0_DBI_L<0>	
DBI1*	D13	FB_B0_DBI_L<1>	
DBI2*	P13	FB_B0_DBI_L<2>	
DBI3*	P2	FB_B0_DBI_L<3>	
DQ0	A4	FB_B0_DQ<0>	
DQ1	A2	FB_B0_DQ<1>	
DQ2	B4	FB_B0_DQ<2>	
DQ3	B2	FB_B0_DQ<3>	
DQ4	E4	FB_B0_DQ<4>	
DQ5	E2	FB_B0_DQ<5>	
DQ6	F4	FB_B0_DQ<6>	
DQ7	F2	FB_B0_DQ<7>	
DQ8	A11	FB_B0_DQ<8>	
DQ9	A13	FB_B0_DQ<9>	
DQ10	B11	FB_B0_DQ<10>	
DQ11	B13	FB_B0_DQ<11>	
DQ12	E11	FB_B0_DQ<12>	
DQ13	E13	FB_B0_DQ<13>	
DQ14	F11	FB_B0_DQ<14>	
DQ15	F13	FB_B0_DQ<15>	
DQ16	U11	FB_B0_DQ<31>	
DQ17	U13	FB_B0_DQ<30>	
DQ18	T11	FB_B0_DQ<29>	
DQ19	T13	FB_B0_DQ<28>	
DQ20	N11	FB_B0_DQ<25>	
DQ21	N13	FB_B0_DQ<26>	
DQ22	M11	FB_B0_DQ<27>	
DQ23	M13	FB_B0_DQ<24>	
DQ24	U4	FB_B0_DQ<23>	
DQ25	U2	FB_B0_DQ<22>	
DQ26	T4	FB_B0_DQ<19>	
DQ27	T2	FB_B0_DQ<21>	
DQ28	N4	FB_B0_DQ<20>	
DQ29	N2	FB_B0_DQ<18>	
DQ30	M4	FB_B0_DQ<17>	
DQ31	M2	FB_B0_DQ<16>	
NC	A5, J5, U5	NC	
		FB_B0_A<8>	

FB_B1_A<2>	H11	BA0/A2	
FB_B1_A<5>	K10	BA1/A5	
FB_B1_A<4>	K11	BA2/A4	
FB_B1_A<3>	H10	BA3/A3	
FB_B1_A<7>	K4	A8/A7	
FB_B1_A<1>	H5	A9/A1	
FB_B1_A<0>	H4	A10/A0	
FB_B1_A<6>	K5	A11/A6	
FB_B1_CKE_L	J3	CKE*	
FB_B1_CLK_P	J12	CK	
FB_B1_CLK_N	J11	CK*	
FB_B1_CS_L	G12	CS*	
FB_B1_WE_L	L12	WE*	
FB_B1_CAS_L	L3	CAS*	
FB_B1_RAS_L	G3	RAS*	
FB_B1_ZQ	J13	ZQ	
FB_B1_MF	J1	MF (MF=0)	
FB_B1_SEN	J10	SEN	
FB_RESET_L	J2	RESET*	
FB_B1_ABI_L	J4	ABI*	
FB_B1_EDC<0>	C2	EDC0	
FB_B1_EDC<1>	C13	EDC1	
FB_B1_EDC<2>	R13	EDC2	
FB_B1_EDC<3>	R2	EDC3	
FB_B1_WCLK_P<0>	D4	WCK01	
FB_B1_WCLK_N<0>	D5	WCK01*	
FB_B1_WCLK_P<1>	P4	WCK23	
FB_B1_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_B1_DBI_L<0>	
DBI1*	D13	FB_B1_DBI_L<1>	
DBI2*	P13	FB_B1_DBI_L<2>	
DBI3*	P2	FB_B1_DBI_L<3>	
DQ0	A4	FB_B1_DQ<0>	
DQ1	A2	FB_B1_DQ<3>	
DQ2	B4	FB_B1_DQ<1>	
DQ3	B2	FB_B1_DQ<2>	
DQ4	E4	FB_B1_DQ<6>	
DQ5	E2	FB_B1_DQ<5>	
DQ6	F4	FB_B1_DQ<7>	
DQ7	F2	FB_B1_DQ<4>	
DQ8	A11	FB_B1_DQ<8>	
DQ9	A13	FB_B1_DQ<9>	
DQ10	B11	FB_B1_DQ<10>	
DQ11	B13	FB_B1_DQ<11>	
DQ12	E11	FB_B1_DQ<12>	
DQ13	E13	FB_B1_DQ<13>	
DQ14	F11	FB_B1_DQ<14>	
DQ15	F13	FB_B1_DQ<15>	
DQ16	U11	FB_B1_DQ<23>	
DQ17	U13	FB_B1_DQ<22>	
DQ18	T11	FB_B1_DQ<21>	
DQ19	T13	FB_B1_DQ<20>	
DQ20	N11	FB_B1_DQ<19>	
DQ21	N13	FB_B1_DQ<18>	
DQ22	M11	FB_B1_DQ<16>	
DQ23	M13	FB_B1_DQ<17>	
DQ24	U4	FB_B1_DQ<31>	
DQ25	U2	FB_B1_DQ<26>	
DQ26	T4	FB_B1_DQ<30>	
DQ27	T2	FB_B1_DQ<29>	
DQ28	N4	FB_B1_DQ<27>	
DQ29	N2	FB_B1_DQ<28>	
DQ30	M4	FB_B1_DQ<24>	
DQ31	M2	FB_B1_DQ<25>	
NC	A5, J5, U5	NC	
		FB_B1_A<8>	

C8500 C8501 C8502 C8503 C8504 C8505 4.7UF 20% 6.3V X5R 402

C8506 C8507 C8508 C8509 C8510 C8511 C8512 C8513 1UF 10% 6.3V CERM-X5R 402

C8514 C8515 C8516 C8517 1UF 10% 6.3V CERM-X5R 402
C8516 C8517 0.1UF 10% 6.3V X5R 201

C8518 C8519 C8520 C8521 C8522 C8523 C8524 C8525 0.1UF 10% 6.3V X5R 201

VDD
VDDQ
VSS
VSSQ

FB_B0_VREFC J14 VREFC
FB_B0_VREFD1 A10
FB_B0_VREFD2 U10 VREFD

R8530 2.37K 1% 1/16W MF-LF 402
R8531 5.49K 1% 1/16W MF-LF 402
R8532 2.37K 1% 1/16W MF-LF 402
R8533 5.49K 1% 1/16W MF-LF 402
R8534 2.37K 1% 1/16W MF-LF 402
R8535 5.49K 1% 1/16W MF-LF 402

C8530 C8531 C8532 C8533 C8534 C8535 1UF 10% 6.3V CERM-X5R 402

FB_B0_VREFC
FB_B0_VREFD1
FB_B0_VREFD2

C8550 C8551 C8552 C8553 C8554 C8555 4.7UF 20% 6.3V X5R 402

C8556 C8557 C8558 C8559 C8560 C8561 C8562 C8563 1UF 10% 6.3V CERM-X5R 402

C8564 C8565 C8566 C8567 C8568 C8569 C8570 C8571 0.1UF 10% 6.3V X5R 201

C8572 C8573 C8574 C8575 0.1UF 10% 6.3V X5R 201

FB_B1_VREFC J14 VREFC
FB_B1_VREFD1 A10
FB_B1_VREFD2 U10 VREFD

R8580 2.37K 1% 1/16W MF-LF 402
R8581 5.49K 1% 1/16W MF-LF 402
R8582 2.37K 1% 1/16W MF-LF 402
R8583 5.49K 1% 1/16W MF-LF 402
R8584 2.37K 1% 1/16W MF-LF 402
R8585 5.49K 1% 1/16W MF-LF 402

C8580 C8581 C8582 C8583 C8584 C8585 1UF 10% 6.3V CERM-X5R 402

FB_B1_VREFC
FB_B1_VREFD1
FB_B1_VREFD2

SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2010

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VRAM BOM OPTION TABLE

	VRAM_DVP0 (STUFF R8613?)	VRAM_DVP1 (STUFF R8612?)	VRAM_DVP2 (STUFF R8611?)
K92 SAMSUNG 1G	NO	NO	YES
K92 HYNIX 1G	YES	NO	YES
K91F SAMSUNG 512M	NO	NO	NO
K91F HYNIX 512M	NO	YES	NO
K91F SAMSUNG 1G	YES	NO	NO
K91F HYNIX 1G	YES	YES	NO

NOTE: AMD STRAPS FOR IDENTIFYING VRAM VENDOR & SIZE FOR WHISTLER

K92 Samsung 1G - NOSTUFF R8613, NOSTUFF R8612, STUFF R8611
K92 Hynix 1G - STUFF R8613, NOSTUFF R8612, STUFF R8611

K91FSamsung 512M - NOSTUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 512M - NOSTUFF R8613, STUFF R8612, NOSTUFF R8611
K91FSamsung 1G - STUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 1G - STUFF R8613, STUFF R8612, NOSTUFF R8611

NO STRAP CHANGES ARE REQUIRED FOR SEYMOUR BASED SYSTEMS

PP1V8_S0GPU_ISNS — R8610 10K 5% 1/16W MF-LF 402 NOSTUFF; R8611 10K 5% 1/16W MF-LF 402 VRAM_DVP2; R8612 10K 5% 1/16W MF-LF 402 VRAM_DVP1; R8613 10K 5% 1/16W MF-LF 402 VRAM_DVP0

PP3V3_S0GPU — R8600 4.7K 5% 1/16W MF-LF 402; R8601 4.7K 5% 1/16W MF-LF 402

PP1V8_S0GPU_ISNS — R8602 499 1% 1/16W MF-LF 402; C8600 0.1UF 10% 16V X5R 402-1; R8603 249 1% 1/16W MF-LF 402

CRITICAL L8600 470OHM-1A-150MOHM 0603: PP1V8_S0GPU_ISNS (VOLTAGE=1.8V) — C8601 10UF 20% 10V X5R 603; C8602 1UF 10% 16V X5R 402; C8603 0.1UF 10% 16V X5R 402-1 (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V)

CRITICAL L8601 470OHM-1A-150MOHM 0603: PP1V0_S0GPU_ISNS — C8604 10UF 20% 10V X5R 603; C8605 1UF 10% 25V X5R 402; C8606 0.1UF 10% 16V X5R 402-1 (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1V)

XW8600 SM: GND_GPU_DPLL (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V)

CRITICAL L8602 120OHM-0.3A 0402: PP1V8_S0GPU_ISNS — C8607 10UF 20% 10V X5R 603; C8608 1UF 10% 25V X5R 402; C8609 0.1UF 10% 16V X5R 402-1 (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V)

XW8601 SM: GND_GPU_TSVSS (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V)

U8000 WHISTLER 40NM-ES FCBGA (2 OF 9)

TP_DVPCNTL_M<0>	AR8	DVPCNTL_MVP_0	
TP_DVPCNTL_M<1>	AU8	DVPCNTL_MVP_1	
TP_DVPCNTL<0>	AP8	DVPCNTL_0	
TP_DVPCNTL<1>	AW8	DVPCNTL_1	
TP_DVPCNTL<2>	AR3	DVPCNTL_2	
TP_DVPCLK	AR1	DVPCLK	
DVPDATA<0>	AU1	DVPDATA_0	
DVPDATA<1>	AU3	DVPDATA_1	
DVPDATA<2>	AW3	DVPDATA_2	
DVPDATA<3>	AP6	DVPDATA_3	
TP_DVPDATA<4>	AW5	DVPDATA_4	
TP_DVPDATA<5>	AU5	DVPDATA_5	
TP_DVPDATA<6>	AR6	DVPDATA_6	
TP_DVPDATA<7>	AW6	DVPDATA_7	
TP_DVPDATA<8>	AU6	DVPDATA_8	
TP_DVPDATA<9>	AT7	DVPDATA_9	
TP_DVPDATA<10>	AV7	DVPDATA_10	
TP_DVPDATA<11>	AN7	DVPDATA_11	
TP_DVPDATA<12>	AV9	DVPDATA_12	
TP_DVPDATA<13>	AT9	DVPDATA_13	
TP_DVPDATA<14>	AR10	DVPDATA_14	
TP_DVPDATA<15>	AW10	DVPDATA_15	
TP_DVPDATA<16>	AU10	DVPDATA_16	
TP_DVPDATA<17>	AP10	DVPDATA_17	
TP_DVPDATA<18>	AV11	DVPDATA_18	
TP_DVPDATA<19>	AT11	DVPDATA_19	
TP_DVPDATA<20>	AR12	DVPDATA_20	
TP_DVPDATA<21>	AW12	DVPDATA_21	
TP_DVPDATA<22>	AU12	DVPDATA_22	
TP_DVPDATA<23>	AP12	DVPDATA_23	
NC	AJ21	SWAPLOCKA	
NC	AK21	SWAPLOCKB	
GPU_I2C_SCL	AK26	SCL	I2C
GPU_I2C_SDA	AJ26	SDA	
GPU_PCIE_TX_PWR	AH20	GPIO_0	
GPU_GPIO_TX_DEEMP	AH18	GPIO_1	
GPU_PCIE_GEN2	AN16	GPIO_2	
GPU_SMB_DAT	AH23	GPIO_3_SMBDATA	
GPU_SMB_CLK	AJ23	GPIO_4_SMBCLK	
GPU_AC_BATT	AH17	GPIO_5_AC_BATT	
GPU_VCORE_VID0	AJ17	GPIO_6	
EG_BKLT_EN	AK17	GPIO_7_BLON	
GPU_ROM_SO	AJ13	GPIO_8_ROMSO	
GPU_ROM_SI	AH15	GPIO_9_ROMSI	
GPU_ROM_SCLK	AJ16	GPIO_10_ROMSCK	
GPU_CONFIG_0	AK16	GPIO_11	
GPU_CONFIG_1	AL16	GPIO_12	
GPU_CONFIG_2	AM16	GPIO_13	
DP_T29SNK0_HPD_GPU	AM14	GPIO_14_HPD2	
GPU_VCORE_VID1	AM13	GPIO_15_PWRCNTL_0	
GPU_VCORE_VID2	AK14	GPIO_16	
SMC_GFX_THROTTLE_R_L	AG30	GPIO_17_THERMAL_INT	
DP_T29SNK1_HPD_GPU	AN14	GPIO_18_HPD3	
SMC_GFX_OVERTEMP_R_L	AM17	GPIO_19_CTF	
GPU_VCORE_VID3	AL13	GPIO_20_PWRCNTL_1	
FBVDD_ALTVO	AJ14	GPIO_21_BB_EN	
GPU_ROM_CS_L	AK13	GPIO_22_ROMCS*	
PEX_CLKREQ_L_R	AN13	GPIO_23_CLKREQ*	
TP_GPU_JTAG_TRST_L	AM23	JTAG_TRST*	
TP_GPU_JTAG_TDI	AN23	JTAG_TDI	
TP_GPU_JTAG_TCK	AK23	JTAG_TCK	
TP_GPU_JTAG_TMS	AL24	JTAG_TMS	
TP_GPU_JTAG_TDO	AM24	JTAG_TDO	
NC_GPU_GENERICA	AJ19	GENERICA	
NC_GPU_GENERICB	AK19	GENERICB	
NC_GPU_GENERICC	AJ20	GENERICC	
DP_CA_DET_EG_R	AK20	GENERICD	
NC_GPU_GENERICE	AJ24	GENERICE_HPD4	
NC_GPU_GENERICF	AH26	GENERICF_HPD5	
NC_GPU_GENERICG	AH24	GENERICG_HPD6	
DP_EG_HPD	AK24	HPD1	
GPU_VREFG	AH13	VREFG	
PP1V8_GPU_DPLL 75mA (GND_GPU_DPLL)	AM32	DPLL_PVDD	PLL/CLK
	AN32	DPLL_PVSS	
PP1V0_GPU_DPLL 125mA	AN31	DPLL_VDDC	
NC	AV33	XTALIN	
NC	AU34	XTALOUT	
GPU_CLK27M	AW34	XO_IN	
GPU_CLK100M	AW35	XO_IN2	
GPU_TDIODE_P	AF29	DPLUS	THERMAL
GPU_TDIODE_N	AG29	DMINUS	
NC	AK32	TS_FDO	
NC	AL31	TSA/NC	
PP1V8_GPU_TSVDD 20mA (GND_GPU_TSVSS)	AJ32	TSVDD	DDC/AUX
	AJ33	TSVSS	

OMIT

TXCAP_DPA3P	AU24	DP_EXTA_ML_C_P<3>	OUT
TXCAM_DPA3N	AV23	DP_EXTA_ML_C_N<3>	OUT
TX0P_DPA2P	AT25	DP_EXTA_ML_C_P<2>	OUT
TX0M_DPA2N	AR24	DP_EXTA_ML_C_N<2>	OUT
TX1P_DPA1P	AU26	DP_EXTA_ML_C_P<1>	OUT
TX1M_DPA1N	AV25	DP_EXTA_ML_C_N<1>	OUT
TX2P_DPA0P	AT27	DP_EXTA_ML_C_P<0>	OUT
TX2M_DPA0N	AR26	DP_EXTA_ML_C_N<0>	OUT
TXCBP_DPB3P	AR30	DP_T29SNK0_ML_C_P<3>	OUT
TXCBM_DPB3N	AT29	DP_T29SNK0_ML_C_N<3>	OUT
TX3P_DPB2P	AV31	DP_T29SNK0_ML_C_P<2>	OUT
TX3M_DPB2N	AU30	DP_T29SNK0_ML_C_N<2>	OUT
TX4P_DPB1P	AR32	DP_T29SNK0_ML_C_P<1>	OUT
TX4M_DPB1N	AT31	DP_T29SNK0_ML_C_N<1>	OUT
TX5P_DPB0P	AT33	DP_T29SNK0_ML_C_P<0>	OUT
TX5M_DPB0N	AU32	DP_T29SNK0_ML_C_N<0>	OUT
TXCCP_DPC3P	AU14	DP_T29SNK1_ML_C_P<3>	OUT
TXCCM_DPC3N	AV13	DP_T29SNK1_ML_C_N<3>	OUT
TX0P_DPC2P	AT15	DP_T29SNK1_ML_C_P<2>	OUT
TX0M_DPC2N	AR14	DP_T29SNK1_ML_C_N<2>	OUT
TX1P_DPC1P	AU16	DP_T29SNK1_ML_C_P<1>	OUT
TX1M_DPC1N	AV15	DP_T29SNK1_ML_C_N<1>	OUT
TX2P_DPC0P	AT17	DP_T29SNK1_ML_C_P<0>	OUT
TX2M_DPC0N	AR16	DP_T29SNK1_ML_C_N<0>	OUT
TXCDP_DPD3P	AU20	NC	
TXCDM_DPD3N	AT19	NC	
TX3P_DPD2P	AT21	NC	
TX3M_DPD2N	AR20	NC	
TX4P_DPD1P	AU22	NC	
TX4M_DPD1N	AV21	NC	
TX5P_DPD0P	AT23	NC	
TX5M_DPD0N	AR22	NC	
R	AD39	NC	
R*	AD37	NC	
G	AE36	NC	
G*	AD35	NC	
B	AF37	NC	
B*	AE38	NC	
HSYNC	AC36	GPU_AUD_1	
VSYNC	AC38	GPU_AUD_0	
RSET	AB34	NC	
AVDD	AD34	PP1V8_S0GPU_ISNS	
AVSSQ	AE34		
VDD1DI	AC33		
VSS1DI	AC34		
R2/NC	AC30	NC	
R2*/NC	AC31	NC	
G2/NC	AD30	NC	
G2*/NC	AD31	NC	
B2/NC	AF30	NC	
B2*/NC	AF31	NC	
C/NC	AC32	NC	
Y/NC	AD32	NC	
COMP/NC	AF32	NC	
H2SYNC/GENLK_CLK	AD29	NC	
V2SYNC/GENLK_VSYNC	AC29	NC	
VDD2DI/NC	AG31	NC	
VSS2DI/NC	AG32	NC	
A2VDD/NC	AG33	NC	
A2VDDQ/NC	AD33	NC	
A2VSSQ/TSVSSQ	AF33	GND_GPU_TVSSQ (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V)	
R2SET/NC	AA29	NC	
DDC1CLK	AM26	DP_EG_DDC_CLK	OUT
DDC1DATA	AN26	DP_EG_DDC_DATA	BI
AUX1P	AM27	DP_EG_AUXCH_P	BI
AUX1N	AL27	DP_EG_AUXCH_N	BI
DDC2CLK	AM19	NC	
DDC2DATA	AL19	NC	
AUX2P	AN20	DP_T29SNK0_AUXCH_C_P	BI
AUX2N	AM20	DP_T29SNK0_AUXCH_C_N	BI
DDCCLK_AUX3P	AL30	DP_T29SNK1_AUXCH_C_P	BI
DDCDATA_AUX3N	AM30	DP_T29SNK1_AUXCH_C_N	BI
DDCCLK_AUX4P	AL29	NC	
DDCDATA_AUX4N	AM29	NC	
DDCCLK_AUX5P	AN21	LVDS_EG_DDC_CLK	OUT
DDCDATA_AUX5N	AM21	LVDS_EG_DDC_DATA	BI
DDC6CLK	AJ30	NC	
DDC6DATA	AJ31	NC	
DDCCLK_AUX7P	AK30	NC	
DDCDATA_AUX7N	AK29	NC	

XW8602 SM

PP3V3_S0GPU — Straps for audio on DP and HDMI

R8604 10K 5% 1/16W MF-LF 402; R8605 10K 5% 1/16W MF-LF 402

U8000 FCBGA (3 OF 9) WHISTLER 40NM-ES — LVDS_CNTL

VARY_BL	AK27	LVDS_EG_BLK_PWM	
DIGON	AJ27	EG_LCD_PWR_EN	OUT
TXCLK_UP_DPF3P	AK35	NC_LVDS_EG_B_CLK_P	
TXCLK_UN_DPF3N	AL36	NC_LVDS_EG_B_CLK_N	
TXOUT_U0P_DPF2P	AJ38	LVDS_EG_B_DATA_P<0>	OUT
TXOUT_U0N_DPF2N	AK37	LVDS_EG_B_DATA_N<0>	OUT
TXOUT_U1P_DPF1P	AH35	LVDS_EG_B_DATA_P<1>	OUT
TXOUT_U1N_DPF1N	AJ36	LVDS_EG_B_DATA_N<1>	OUT
TXOUT_U2P_DPF0P	AG38	LVDS_EG_B_DATA_P<2>	OUT
TXOUT_U2N_DPF0N	AH37	LVDS_EG_B_DATA_N<2>	OUT
TXOUT_U3P	AF35	NC_LVDS_EG_B_DATA_P<3>	
TXOUT_U3N	AG36	NC_LVDS_EG_B_DATA_N<3>	
TXCLK_LP_DPE3P	AP34	LVDS_EG_A_CLK_P	OUT
TXCLK_LN_DPE3N	AR34	LVDS_EG_A_CLK_N	OUT
TXOUT_L0P_DPE2P	AW37	LVDS_EG_A_DATA_P<0>	OUT
TXOUT_L0N_DPE2N	AU35	LVDS_EG_A_DATA_N<0>	OUT
TXOUT_L1P_DPE1P	AR37	LVDS_EG_A_DATA_P<1>	OUT
TXOUT_L1N_DPE1N	AU39	LVDS_EG_A_DATA_N<1>	OUT
TXOUT_L2P_DPE0P	AP35	LVDS_EG_A_DATA_P<2>	OUT
TXOUT_L2N_DPE0N	AR35	LVDS_EG_A_DATA_N<2>	OUT
TXOUT_L3P	AN36	NC_LVDS_EG_A_DATA_P<3>	
TXOUT_L3N	AP37	NC_LVDS_EG_A_DATA_N<3>	

OMIT

R8606 10K 5% 1/16W MF-LF 402

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_I2C
- =PP1V8_GPU_VREFG
- =PP1V8_GPU_DPLL
- =PP1V0_GPU_DPLL
- =PP1V0_GPU_TS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=K92_MLB SYNC_DATE=12/01/2010

PAGE TITLE: Whistler LVDS/DP/GPIO

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GPIOs

GPU_PCIE_TX_PWR	GP	GPU_PCIE_TX_PWR	MAKE_BASE=TRUE
GPU_GPIO_TX_DEEMP	GP	GPU_GPIO_TX_DEEMP	MAKE_BASE=TRUE
GPU_PCIE_GEN2	GP	GPU_PCIE_GEN2	MAKE_BASE=TRUE
GPU_SMB_DAT	GP	GPU_SMB_DAT	MAKE_BASE=TRUE
GPU_SMB_CLK	GP	GPU_SMB_CLK	MAKE_BASE=TRUE
GPU_AC_BATT	GP	GPU_AC_BATT	MAKE_BASE=TRUE
GPU_VCORE_VID0	GP	GPU_VCORE_VID0	MAKE_BASE=TRUE
EG_BKLT_EN	GP	EG_BKLT_EN	MAKE_BASE=TRUE
GPU_ROM_SO	GP	GPU_ROM_SO	MAKE_BASE=TRUE
GPU_ROM_SI	GP	GPU_ROM_SI	MAKE_BASE=TRUE
GPU_ROM_SCLK	GP	GPU_ROM_SCLK	MAKE_BASE=TRUE
GPU_CONFIG_0	GP	GPU_CONFIG_0	MAKE_BASE=TRUE
GPU_CONFIG_1	GP	GPU_CONFIG_1	MAKE_BASE=TRUE
GPU_CONFIG_2	GP	GPU_CONFIG_2	MAKE_BASE=TRUE
DP_T29SNK0_HPD_GPU	GP	DP_T29SNK0_HPD_GPU	MAKE_BASE=TRUE
GPU_VCORE_VID1	GP	GPU_VCORE_VID1	MAKE_BASE=TRUE

GPIOs

GPU_VCORE_VID2	GP	GPU_VCORE_VID2	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_R_L	GP	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE
DP_T29SNK1_HPD_GPU	GP	DP_T29SNK1_HPD_GPU	MAKE_BASE=TRUE
SMC_GFX_OVERTEMP_R_L	GP	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE
GPU_VCORE_VID3	GP	GPU_VCORE_VID3	MAKE_BASE=TRUE
FBVDD_ALTVO	GP	FBVDD_ALTVO	MAKE_BASE=TRUE
GPU_ROM_CS_L	GP	GPU_ROM_CS_L	MAKE_BASE=TRUE
PEX_CLKREQ_L_R	GP	PEX_CLKREQ_L_R	MAKE_BASE=TRUE
NC_GPU_GENERICA	GP	NC_GPU_GENERICA	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICB	GP	NC_GPU_GENERICB	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICC	GP	NC_GPU_GENERICC	MAKE_BASE=TRUE NO_TEST=TRUE
DP_CA_DET_EG_R	GP	DP_CA_DET_EG_R	MAKE_BASE=TRUE
NC_GPU_GENERICE	GP	NC_GPU_GENERICE	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICF	GP	NC_GPU_GENERICF	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICG	GP	NC_GPU_GENERICG	MAKE_BASE=TRUE NO_TEST=TRUE
DP_EG_HPD	GP	DP_EG_HPD	MAKE_BASE=TRUE

T29 HPD GPU isolation

PP3V3_S0 — C8741 0.1UF 20% 10V CERM 402

DP_T29SNK0_HPD → U8741 (74LVC2G08GT SOT833, CRITICAL) → DP_T29SNK0_HPD_GPU

PP3V3_GPU_VDD33_R — R8741 0 5% 1/16W MF-LF 402 — PP3V3_S0GPU

PP3V3_S0 → U8741 → DP_T29SNK1_HPD_GPU

DP_T29SNK1_HPD

Unused signals

TP_GPU_JTAG_TCK		TP_GPU_JTAG_TCK	MAKE_BASE=TRUE
TP_GPU_JTAG_TDI		TP_GPU_JTAG_TDI	MAKE_BASE=TRUE
TP_GPU_JTAG_TDO		TP_GPU_JTAG_TDO	MAKE_BASE=TRUE
TP_GPU_JTAG_TMS		TP_GPU_JTAG_TMS	MAKE_BASE=TRUE
TP_GPU_JTAG_TRST_L		TP_GPU_JTAG_TRST_L	MAKE_BASE=TRUE
NC_LVDS_EG_B_CLK_P		NC_LVDS_EG_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_B_CLK_N		NC_LVDS_EG_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_A_DATA_P<3>		NC_LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_A_DATA_N<3>		NC_LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_B_DATA_P<3>		NC_LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_B_DATA_N<3>		NC_LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE

Config Straps

PP3V3_S0GPU

R8700	NOSTUFF	GPU_PCIE_TX_PWR
R8701	NOSTUFF	GPU_GPIO_TX_DEEMP
R8702		GPU_PCIE_GEN2
R8703	NOSTUFF	GPU_SMB_DAT
R8704	NOSTUFF	GPU_SMB_CLK
R8705	NOSTUFF	GPU_AC_BATT
R8706	NOSTUFF	EG_BKLT_EN
R8707	NOSTUFF	GPU_ROM_SO
R8708	NOSTUFF	GPU_ROM_SI
R8709	NOSTUFF	GPU_ROM_SCLK
R8710		GPU_CONFIG_0
R8711	NOSTUFF	GPU_CONFIG_1
R8712	GPU_ROM:YES	GPU_CONFIG_2
R8713	NOSTUFF	FBVDD_ALTVO
R8714	NOSTUFF	PEX_CLKREQ_L_R

All: 10K 1% 1/16W MF-LF 402

GPU_ROM_SI / SCLK / CS_L / WP_L

PP3V3_S0GPU — C8721 0.1UF 20% 10V CERM 402 — GPU_ROM:YES

R8723	33 5% 1/16W MF-LF 402	GPU_ROM_SI
R8720	10K 5% 1/16W MF-LF 402	GPU_ROM_SI_R
R8721	0 5% 1/16W MF-LF 402	GPU_ROM_CS_L_R
R8724	33 5% 1/16W MF-LF 402	GPU_ROM_SCLK
R8725	33 5% 1/16W MF-LF 402	GPU_ROM_CS_L
R8722	NO STUFF 0 5% 1/16W MF-LF 402	GPU_ROM_WP_L

U8701 M25P10A UFDFPN8 CRITICAL OMIT_TABLE

VCC, S*, W*, HOLD*, VSS, THRM PAD

GPU_ROM_SO_R — R8726 33 5% 1/16W MF-LF 402 — GPU_ROM_SO (GPU_ROM:YES)

DP_EG_DDC / DP_IG_DDC

PP3V3_S0 / PP3V3_S0GPU

R8750	NO STUFF 2.2K 5% 1/16W MF-LF 402	DP_EG_DDC_CLK
R8751	NO STUFF 2.2K 5% 1/16W MF-LF 402	DP_EG_DDC_DATA
R8752	4.7K 5% 1/16W MF-LF 402	DP_IG_DDC_CLK
R8753	4.7K 5% 1/16W MF-LF 402	DP_IG_DDC_DATA

ISOLATION R's for GPU Int Temp Sense

GPU_SMB_DAT	R8780 NOSTUFF 0 5% 1/16W MF-LF 402	SMBUS_SMC_0_S0_SDA	
GPU_SMB_CLK	R8781 NOSTUFF 0 5% 1/16W MF-LF 402	SMBUS_SMC_0_S0_SCL	

PP3V3_S0GPU → PP3V3_GPU_OSC_27M / 100M

L8703 120OHM-0.3A 0402 — PP3V3_GPU_OSC_27M (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

L8702 120OHM-0.3A 0402 — PP3V3_GPU_OSC_100M (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

C8702 0.1UF 10% 16V X5R 402-1

C8703 0.1UF 10% 16V X5R 402-1

GPU Reference Clocks

U8700 SL16010DC DFN — VDD1, VDD2, SSCLK, REFCLK, SSEL0, SSEL1, VSS1, VSS2, THM PAD

GPU_OSC_27M_XTALIN, GPU_OSC_27M_XTALOUT

CRITICAL Y8700 SM-2.5X2.0MM 27MHZ-15PPM-18PF

C8700 30PF 5% 50V CERM 402

C8701 30PF 5% 50V CERM 402

R8730	0 5% 1/16W MF-LF 402	GPU_CLK100M_R → GPU_CLK100M (OUT)
R8731	0 5% 1/16W MF-LF 402	GPU_CLK27M_R → GPU_CLK27M (OUT)

SMC_GFX_OVERTEMP / THROTTLE

PP3V3_S0GPU

R8796	NO STUFF 2.2K 5% 1/16W MF-LF 402	SMC_GFX_OVERTEMP_R_L
R8797	2.2K 5% 1/16W MF-LF 402	SMC_GFX_THROTTLE_R_L

DP_CA_DET_EG_R	R8791 0 5% 1/16W MF-LF 402	DP_CA_DET_EG	IN
PEX_CLKREQ_L_R	R8795 0 5% 1/16W MF-LF 402	PEX_CLKREQ_L	OUT
SMC_GFX_OVERTEMP_R_L	R8798 0 5% 1/16W MF-LF 402	SMC_GFX_OVERTEMP_L	OUT
SMC_GFX_THROTTLE_R_L	R8799 0 5% 1/16W MF-LF 402	SMC_GFX_THROTTLE_L	IN

EG_LCD_PWR_EN (OUT), EG_BKLT_EN (OUT), FBVDD_ALTVO (OUT)

PP3V3_S0GPU

R8792	10K 5% 1/16W MF-LF 402	
R8793	10K 5% 1/16W MF-LF 402	
R8794	10K 5% 1/16W MF-LF 402	

SYNC_MASTER=K92_MLB SYNC_DATE=11/23/2010

PAGE TITLE: Whistler GPIOs & STRAPs

Apple Inc.

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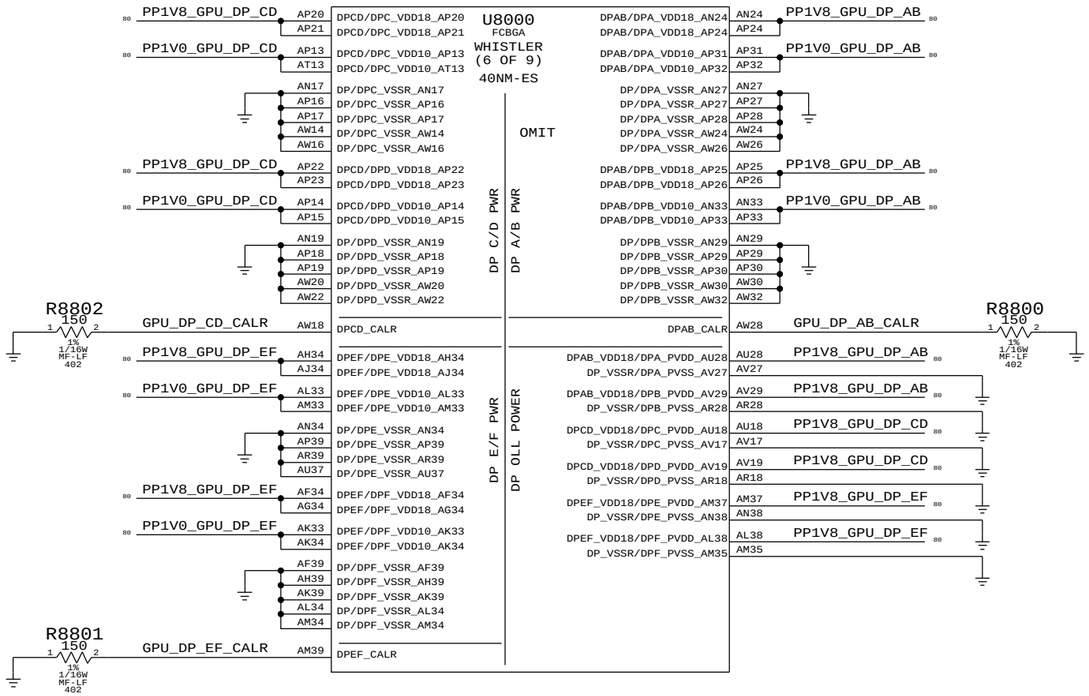

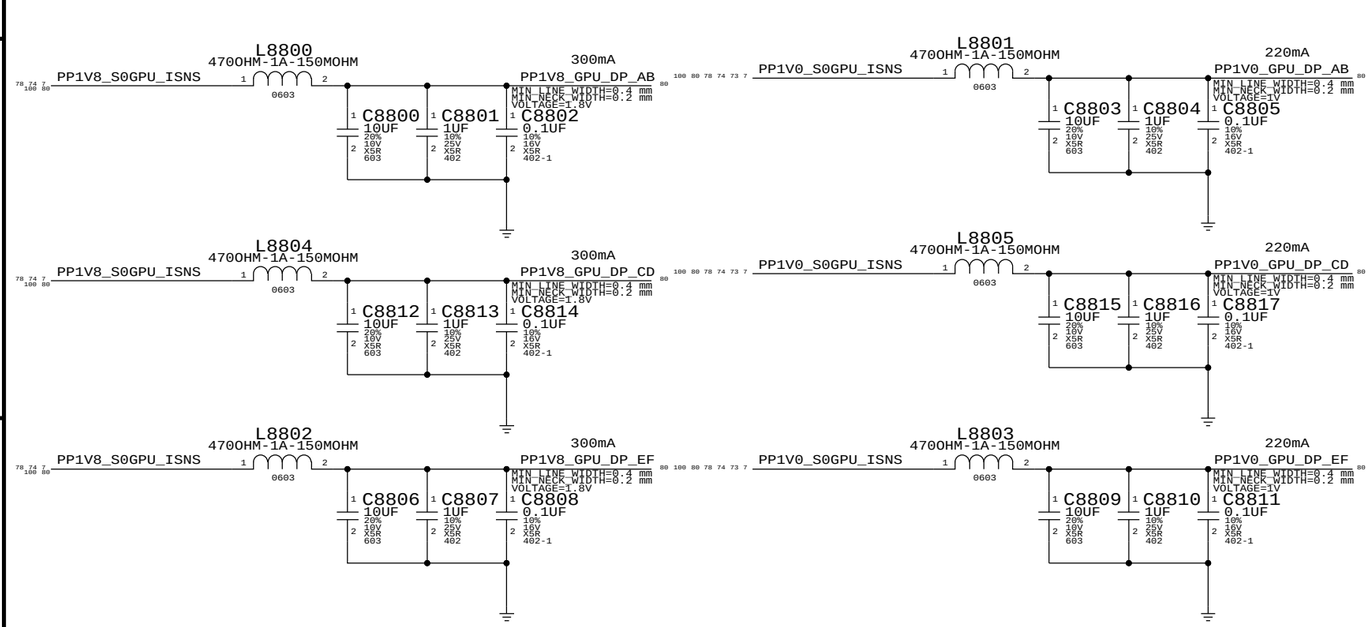

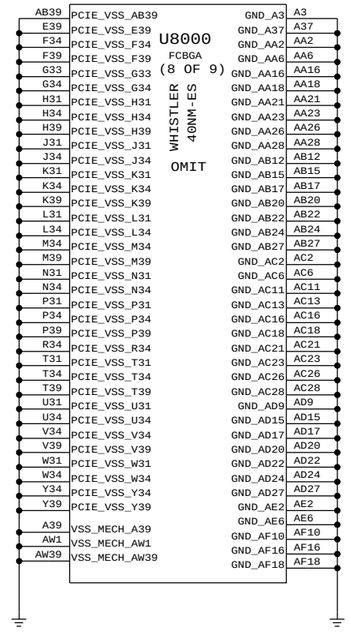

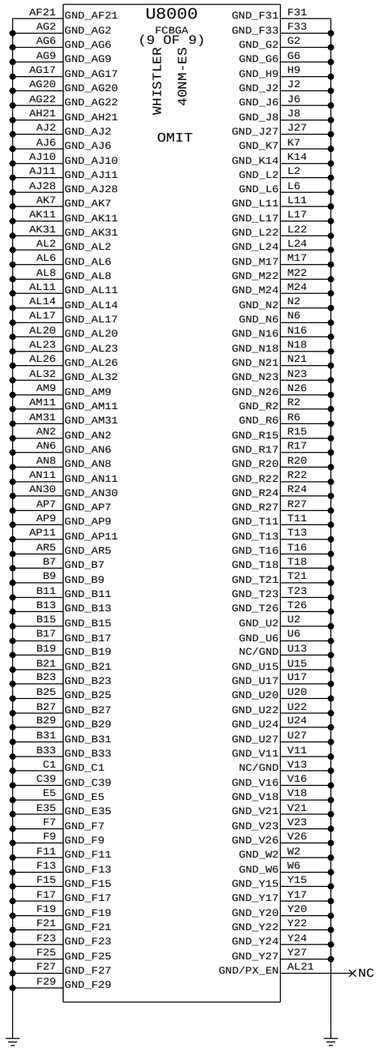

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_DP_AB
- =PP1V8_GPU_DP_CD
- =PP1V8_GPU_DP_EF
- =PP1V0_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V0_GPU_DP_EF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=K92_SUMA SYNC_DATE=06/15/2010

PAGE TITLE: Whistler DP PWR/GNDs

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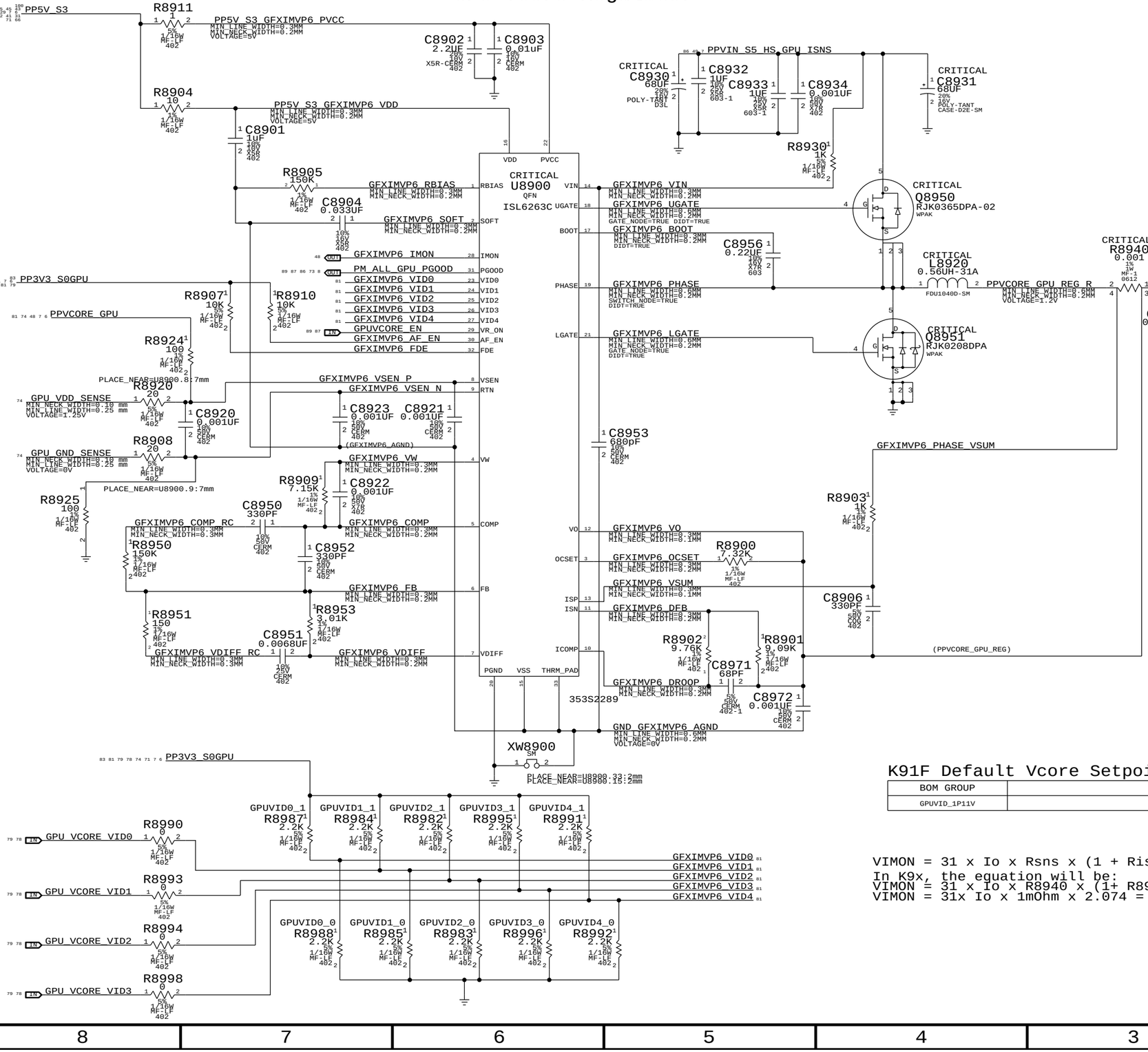
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

GPU VCore Setpoints not up-to-date!

K91F Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P11V	GPUVID4_0,GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_1

VIMON = 31 x Io x Rsns x (1 + Ris2/Ris1)
In K9x, the eguation will be:
VIMON = 31 x Io x R8940 x (1+ R8902/R8901)
VIMON = 31x Io x 1mOhm x 2.074 = Io x 64.29 mV/A

SYNC_MASTER=K91_ERIC SYNC_DATE=12/21/2010

PAGE TITLE
GPU (Whistler) CORE SUPPLY

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LCD (LVDS) INTERFACE

LCD_PWR_EN

R9094 10K 5% 1/16W MF-LF 402

CRITICAL U9000 FPF1009 MFET-2X2
ON, VIN_1, VIN_2, VOUT_1, VOUT_2, GND, THRM PAD

PP3V3_S5

C9009 0.1UF 10% 16V X5R 402-1

C9011 0.1UF 10% 16V X5R 402-1

C9012 10UF 20% 6.3V X5R 603

CRITICAL L9000 FERR-250-OHM SM

PP3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

C9001 0.1UF 10% 16V X5R 402-1

C9002 0.001UF 10% 50V X7R 402

PP3V3_S0

R9010 100K 5% 1/16W MF-LF 402

R9011 100K 5% 1/16W MF-LF 402

100K pull-ups are for
no-panel case (development).
Panel has 2K pull-ups

LVDS_DDC_CLK
LVDS_DDC_DATA

C9010 0.001UF 10% 50V X7R 402

CRITICAL L9010 90-OHM-100MA DLP11S

LVDS_CONN_A_CLK_N
LVDS_CONN_A_CLK_P

Place close to the connector

CRITICAL L9011 90-OHM-100MA DLP11S

LVDS_CONN_B_CLK_N
LVDS_CONN_B_CLK_P

Place close to the connector

CRITICAL J9000 20474-040E-11 F-RT-SM

PP3V3_SW_LCD
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

NC

LVDS_CONN_A_DATA_N<0>
LVDS_CONN_A_DATA_P<0>
LVDS_CONN_A_DATA_N<1>
LVDS_CONN_A_DATA_P<1>
LVDS_CONN_A_DATA_N<2>
LVDS_CONN_A_DATA_P<2>
LVDS_CONN_A_CLK_F_N
LVDS_CONN_A_CLK_F_P
LVDS_CONN_B_DATA_N<0>
LVDS_CONN_B_DATA_P<0>
LVDS_CONN_B_DATA_N<1>
LVDS_CONN_B_DATA_P<1>
LVDS_CONN_B_DATA_N<2>
LVDS_CONN_B_DATA_P<2>
LVDS_CONN_B_CLK_F_N
LVDS_CONN_B_CLK_F_P
LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1

NC

PPVOUT_S0_LCDBKLT

C9000 0.001UF 10% 50V CERM 402

518S0651

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE
LVDS Display Connector

Apple Inc.

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LVDS Transmitter Termination

All emulated LVDS outputs require this termination

PLACE_NEAR=U9600.A6:7mm
R9220 357 1% 1/20W MF 201
LVDS_A_CLK_P → LVDS_CONN_A_CLK_P

PLACE_NEAR=U9600.A7:7mm
R9222 357 1% 1/20W MF 201
LVDS_A_CLK_N → LVDS_CONN_A_CLK_N

R9225 357 1% 1/20W MF 201
LVDS_A_DATA_P<0> → LVDS_CONN_A_DATA_P<0>
PLACE_NEAR=U9600.A8:7mm

PLACE_NEAR=U9600.B9:7mm
R9227 357 1% 1/20W MF 201
LVDS_A_DATA_N<0> → LVDS_CONN_A_DATA_N<0>

R9230 357 1% 1/20W MF 201
LVDS_A_DATA_P<1> → LVDS_CONN_A_DATA_P<1>
PLACE_NEAR=U9600.A9:7mm

PLACE_NEAR=U9600.C10:7mm
R9232 357 1% 1/20W MF 201
LVDS_A_DATA_N<1> → LVDS_CONN_A_DATA_N<1>

R9235 357 1% 1/20W MF 201
LVDS_A_DATA_P<2> → LVDS_CONN_A_DATA_P<2>
PLACE_NEAR=U9600.B10:7mm

PLACE_NEAR=U9600.A10:7mm
R9237 357 1% 1/20W MF 201
LVDS_A_DATA_N<2> → LVDS_CONN_A_DATA_N<2>

R9240 357 1% 1/20W MF 201
LVDS_B_CLK_P → LVDS_CONN_B_CLK_P
PLACE_NEAR=U9600.C8:7mm

PLACE_NEAR=U9600.C9:7mm
R9242 357 1% 1/20W MF 201
LVDS_B_CLK_N → LVDS_CONN_B_CLK_N

R9245 357 1% 1/20W MF 201
LVDS_B_DATA_P<0> → LVDS_CONN_B_DATA_P<0>
PLACE_NEAR=U9600.A2:7mm

PLACE_NEAR=U9600.A3:7mm
R9247 357 1% 1/20W MF 201
LVDS_B_DATA_N<0> → LVDS_CONN_B_DATA_N<0>

R9250 357 1% 1/20W MF 201
LVDS_B_DATA_P<1> → LVDS_CONN_B_DATA_P<1>
PLACE_NEAR=U9600.A1:7mm

PLACE_NEAR=U9600.B3:7mm
R9252 357 1% 1/20W MF 201
LVDS_B_DATA_N<1> → LVDS_CONN_B_DATA_N<1>

R9255 357 1% 1/20W MF 201
LVDS_B_DATA_P<2> → LVDS_CONN_B_DATA_P<2>
PLACE_NEAR=U9600.C5:7mm

R9257 357 1% 1/20W MF 201
LVDS_B_DATA_N<2> → LVDS_CONN_B_DATA_N<2>
PLACE_NEAR=U9600.A5:7mm

DP AUX, DDC, & HPD muxing to IG/EG

PP3V3_S0
R9202 10K 5% 1/10W MF-LF 402
C9220 0.1UF 20% 16V CERM 402
C9230 0.1UF 20% 16V CERM 402

U9220 CBTL03062 BGA (CRITICAL)
VDD
GND

DP_IG_AUX_CH_P	17	DAUX1+
DP_IG_AUX_CH_N	16	DAUX1-
DP_EG_AUXCH_P	14	DAUX2+
DP_EG_AUXCH_N	13	DAUX2-
DP_IG_DDC_CLK	12	DDC_CLK1
DP_IG_DDC_DATA	11	DDC_DAT1
DP_EG_DDC_CLK	9	DDC_CLK2
DP_EG_DDC_DATA	8	DDC_DAT2
DP_IG_HPD	10	HPD_1
DP_EG_HPD	7	HPD_2
DP_MUX_SEL_EG	5	GPU_SEL
DP_MUX_EN	15	XSD*

AUX+	20	DP_EXTA_AUXCH_C_P
AUX-	1	DP_EXTA_AUXCH_C_N
DDC_CLK	2	DP_EXTA_DDC_CLK
DDC_DAT	3	DP_EXTA_DDC_DATA
HPDIN	4	(DP_EXTA_HPD)

R9204 100K 5% 1/10W MF-LF 402
R9205 100K 5% 1/10W MF-LF 402

T29/DP HOT PLUG IN

R9206 0 5% 1/10W MF-LF 402
DP_EXTA_HPD
PP3V3_S0
T29_DP_HPD:ALL_OR C9210 0.1UF 20% 16V CERM 402
CRITICAL
T29_DP_HPD:ALL_OR 74LVC2G32GT SOT833 U9210
DP_T29SNK0_HPD
DP_T29SNK1_HPD
T29_HOTPLUG_DET_OR
T29_DP_HPD:ALL_OR 74LVC2G32GT SOT833 U9210
(DP_EXTA_HPD)
DP_HOTPLUG_DET

T29_DP_HPD:MCU_GMUX Q9280 SSM3K15FV SOT-VESM-MF
PP3V3_S0
T29_DP_HPD:MCU_GMUX R9281 100K 5% 1/10W MF-LF 402
DP_A_EXT_HPD

LVDS DDC MUX

PP3V3_S0GPU
PP3V3_S0
R9270 20K 5% 1/10W MF-LF 402
R9271 20K 5% 1/10W MF-LF 402
C9270 0.1UF 10% 16V CERM 402
R9272 20K 5% 1/10W MF-LF 402
R9273 20K 5% 1/10W MF-LF 402

U9270 SN74LV4066A QFN1 (CRITICAL)
VCC
GND THRM

LVDS_DDC_SEL_EG	C1	A1 / B1
LVDS_DDC_SEL_IG	C2	A2 / B2
	C3	A3 / B3
	C4	A4 / B4

LVDS_EG_DDC_CLK
LVDS_IG_DDC_CLK
LVDS_DDC_CLK
LVDS_EG_DDC_DATA
LVDS_IG_DDC_DATA
LVDS_DDC_DATA

SYNC_MASTER=K92_MLB SYNC_DATE=11/21/2010

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T29 A High-Speed Signals

DP_EXTA_ML_C_P<0> C9300 0.1uF → DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1uF → DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1uF → DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1uF → DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1uF → DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1uF → DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1uF → DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1uF → DP_EXTA_ML_N<3>
DP_EXTA_AUXCH_C_P C9308 0.1uF → DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1uF → DP_EXTA_AUXCH_N

PP3V3_S0 → R9309 1M 5% MF-LF 1/16W 402 → DP_EXTA_AUXCH_P
R9308 1M 5% MF-LF 1/16W 402 → DP_EXTA_AUXCH_N

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

T29_D2R_N<0> → C9370 0.47uF → T29_D2R_C_N<0>
T29_D2R_P<0> → C9371 0.47uF → T29_D2R_C_P<0>

OVERSIZE_PAD=0.875 mm^2 (Both L's)
T29_R2D_C_N<0> → L9372 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_N<0> → C9372 0.47uF (C9372.2) GND_VOID=TRUE
T29_R2D_C_P<0> → L9373 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_P<0> → C9373 0.47uF (C9373.2) GND_VOID=TRUE
Inductor values TBD

T29_A_BIAS_R2D_P0 → R9372 1.5K 5% MF 1/20W 201 → T29_R2D_P<0>
T29_A_BIAS_R2D_N0 → R9373 1.5K 5% MF 1/20W 201 → T29_R2D_N<0>
GND_VOID=TRUE (C9370/C9371)

T29 signals are P/N-swapped after AC caps to improve layout.

T29_D2R_N<1> → C9380 0.47uF → T29_D2R_C_N<1>
T29_D2R_P<1> → C9381 0.47uF → T29_D2R_C_P<1>

OVERSIZE_PAD=0.875 mm^2 (Both L's)
T29_R2D_C_N<1> → L9382 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_N<1> → C9382 0.47uF (C9383.2) GND_VOID=TRUE
T29_R2D_C_P<1> → L9383 1.0NH+/-0.1NH 0201-1 → T29_R2D_C_F_P<1> → C9383 0.47uF (C9383.2) GND_VOID=TRUE

T29_A_BIAS_R2D_P1 → R9382 1.5K 5% MF 1/20W 201 → T29_R2D_P<1>
T29_A_BIAS_R2D_N1 → R9383 1.5K 5% MF 1/20W 201 → T29_R2D_N<1>
GND_VOID=TRUE (C9380/C9381)

T29 Path Biasing

T29_D2R_C_P<0> → T29_D2R_P<0>
T29_D2R_C_N<0> → T29_D2R_N<0>
T29_D2R_C_P<1> → T29_D2R_P<1>
T29_D2R_C_N<1> → T29_D2R_N<1>

D9364 BAR90-02LRH (D9364.2)
D9372 BAR90-02LRH
D9373 BAR90-02LRH
D9365 BAR90-02LRH
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY
T29: TX_0
T29DPA_ML_C_P<0> → T29DPA_ML_P<0>
T29DPA_ML_C_N<0> → T29DPA_ML_N<0>
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
R9374 1.5K, R9375 1.5K 5% MF 1/20W 201

D9360 BAR90-02LRH (D9360.2)
D9382 BAR90-02LRH
D9383 BAR90-02LRH
D9361 BAR90-02LRH
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)
T29: TX_1
T29DPA_ML_C_P<2> → T29DPA_ML_P<2>
T29DPA_ML_C_N<2> → T29DPA_ML_N<2>
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
R9384 1.5K, R9385 1.5K 5% MF 1/20W 201

DP A Super-Driver

PP3V3_S0 → C9310 2.2UF, C9311 0.1UF, C9312 0.1UF

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP_EXTA_ML_P<0>	1 IN_D0P	OUT_D0P 30	DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	2 IN_D0N	OUT_D0N 29	DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	4 IN_D1P	OUT_D1P 28	DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	5 IN_D1N	OUT_D1N 27	DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	7 IN_D2P	OUT_D2P 25	DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	8 IN_D2N	OUT_D2N 24	DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	9 IN_D3P	OUT_D3P 23	DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	10 IN_D3N	OUT_D3N 22	DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	14 IN_SCL	AC_AUXP 20	DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	13 IN_SDA	AC_AUXN 19	DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	16 IN_AUXP	OUT_AUXP_SCL	(DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	15 IN_AUXN	OUT_AUXN_SDA	(DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	3 IN_HPD	(IPD) OUT_HPD	(DP_SDRVA_HPD)
DPSDRVA_I2C_CTL_EN	26 I2C_CTL_EN (IPU)	CA_DET	32 DP_A_CA_DET
DPSDRVA_I2C_ADDR0	36 I2C_ADDR0 (IPD)	CEXT	11 DPSDRVA_CEXT
DPSDRVA_I2C_ADDR1	35 I2C_ADDR1 (IPD)		
I2C_DPSDRVA_SCL	38 SCL_CTL		
I2C_DPSDRVA_SDA	37 SDA_CTL		
DPSDRVA_REXT	12 REXT		
DP_AUXCH_ISOL	39 AUXDDC_OFF (IPD)		
DP_A_PWRDWN_R	34 PD (IPD)		

NO STUFF R9311 1K, R9310 1K, R9312 1K

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).
SDRV_PD R9318 0, R9319 4.99K 1%

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

R9354 30 5% 1/20W MF 201 → DP_SDRVA_ML_R_P<0>
R9353 270 5% 1/20W MF 201 → DP_SDRVA_ML_R_N<0>
R9355 30 → DP_SDRVA_ML_R_P<2>
R9350 30 → DP_SDRVA_ML_R_N<2>
R9351 30
R9352 270

DP_SDRVA_ML_R_P<0> → C9364 0.22uF → DP_SDRVA_ML_P<0>
DP_SDRVA_ML_R_N<0> → C9365 0.22uF → DP_SDRVA_ML_N<0>
DP_SDRVA_ML_R_P<2> → C9360 0.22uF → DP_SDRVA_ML_P<2>
DP_SDRVA_ML_R_N<2> → C9361 0.22uF → DP_SDRVA_ML_N<2>

DP Path Biasing

R9361 1.5K, R9360 1.5K, R9365 1.5K, R9364 1.5K 5% MF 1/20W 201
DP_A_BIAS0 VOLTAGE=3.3V → R9362 51 5% 1/20W MF 201 PLACE_NEAR=C9361.1:2mm
DP_A_BIAS2 VOLTAGE=3.3V → R9363 51 5% 1/20W MF 201 PLACE_NEAR=C9361.1:2mm

PP3V3_S0 → C9359 0.1UF → CRITICAL U9359 74LVC1G04DBDCK SC70
DP_A_PWRDWN → DP_A_BIAS

IC supports input high while Vcc = 0V.

DP/T29 A Low-Speed MUX

C9363 0.1uF → DP_SDRVA_ML_C_N<1>
C9362 0.1uF → DP_SDRVA_ML_C_P<2>
C9367 0.1uF → DP_SDRVA_ML_C_P<3>
C9366 0.1uF → DP_SDRVA_ML_C_N<3>
C9369 0.1uF → DP_SDRVA_AUXCH_C_P
C9368 0.1uF → DP_SDRVA_AUXCH_C_N

AUXCH Snoop Port, used by PS8301 during training.

C9319 2.2UF 20% 6.3V CERM 402-LF

PP3V3_SW_DPAPWR
Must be 3.3V DP A port power

C9390 0.1UF, C9391 0.1UF 20% 10V CERM 402

U9390 CBTL04DP081 HVQFN CRITICAL

DP_SDRVA_ML_N<3>	31 DIN1_0+	DOUT_0+ 1	T29DPA_ML_N<3>
DP_SDRVA_ML_P<3>	30 DIN1_0-	DOUT_0- 2	T29DPA_ML_P<3>
DP_SDRVA_ML_N<1>	27 DIN1_1+		T29: Unused
DP_SDRVA_ML_P<1>	26 DIN1_1-		
DP_SDRVA_AUXCH_P	19 AUX1+	DOUT_1+ 4	T29DPA_ML_N<1>
DP_SDRVA_AUXCH_N	18 AUX1-	DOUT_1- 5	T29DPA_ML_P<1>
DP_SDRVA_HPD	17 HPD_1		T29: LSX_A_R2P/P2R (P/N)
CKPLUS_WAIVE=NdifPr_badTerm			
T29_A_RSVD_N	25 DIN2_0+	AUX+ 6	DP_A_EXT_AUXCH_P
T29_A_RSVD_P	24 DIN2_0-	AUX- 7	DP_A_EXT_AUXCH_N
(T29_A_LSX_P2R)	23 DIN2_1+		T29: RX_1 Bias Sink
(T29_A_LSX_R2P)	22 DIN2_1-		
T29_D2R1_BIASP	15 AUX2+	HPD_IN 8	DP_A_EXT_HPD
T29_D2R1_BIASN	14 AUX2-		
NC	13 HPD_2		
DP_A_PWRDWN	10 GPU_SEL		
T29_A_BIAS	32 AUX_SEL		
NC	11 NC		

R9399 100K 5% 1/16W MF-LF 402
R9396 1K, R9397 1K 5% 1/16W MF-LF 402
R9398 100K 5% 1/16W MF-LF 402
OMIT_TABLE
LO=Port A
HI=Port B

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 11 for HPD.

SIGNAL_MODEL=T29DP_MUX

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100 ohm pull-downs would defeat DP Sink's detection of DP Source.

Port A MCU

PP3V3_SW_DPAPWR
Must be 3.3V DP A port power

C9330 0.1UF, C9331 0.1UF 20% 10V CERM 402

U9330 LPC1112A HVQFN25 CRITICAL OMIT_TABLE

DP_A_CA_DET	1 RESET#/PIO0_0	R/PIO1_0/AD1 16	T29DPA_CONFIG1_RC
	2 PIO0_1/CLKOUT	R/PIO1_1/AD2 17	T29DPA_CONFIG2_RC
T29_LSEO<0>	7 PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3 18	T29_A_HV_EN_R
I2C_T29_SCL	8 PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4 19	T29_A_UC_ADDR
I2C_T29_SDA	9 PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP 20	DP_A_EXT_HPD
T29DPA_HPD	10 PIO0_6/SCK	PIO1_6/RXD 23	T29_A_LSX_P2R
T29_A_BIAS	11 PIO0_7/CTS#	PIO1_7/TXD 24	T29_A_LSX_R2P
T29_LSOE<0>	12 PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0 6	T29_LSEO<1>
T29_LSOE<1>	13 PIO0_9/MOSI/CT16B0_MAT1		
	14 SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)		
T29_MCU_INT_L	15 R/PIO0_11/AD0 (OD)	XTALIN 4	
	VSS 3	THRM PAD 25	

R9338 10K → T29_A_HV_EN
R9334 10K
R9392 51, R9393 51 5% 1/16W MF-LF 402

P2R = Plug to Receptacle
R2P = Receptacle to Plug

I2C Addr: 0x26/0x27 (Wr/Rd)

R9339 1M 5% 1/16W MF-LF 402
R9335 1K, R9336 10K 5% 1/16W MF-LF 402

PCIE_WAKE_L → OMIT R9330 0 → SWCLK, SWDIO
T29_A_UC_ADDR

=T29_WAKE_L:
use PCIe WAKE#

R9330 provides pads for programming/debug of MCU, please make accessible.
If project has space for 10-pin programming header it should be used.

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

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3.3V/HV Power MUX

Port A 3.3V Power Switch

Port A HV Power Switch

PP3V3_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PP15V_T29
20V Max

R9416 470K 5% 1/10W MF-LF 402

C9410 0.1UF 10% 50V X7R 603-1

U9410 SN1010017 QFN
VIN VOUT EN* (IPU-Weak!) FLT* RTRY* ILIM CT IFLT GND THRM PAD

C9411 0.1UF 10% 50V X7R 603-1

PPHV_SW_DPAPWR

D9410 SM STPS2L30AF

DPAPWRSW_HVEN_L_R
TP_DPAPPWRSW_FLT_L
DPAPWRSW_ILIM
DPAPWRSW_IFLT

C9412 0.47UF 10% 16V CERM-X5R 402 <CT>
OMIT_TABLE

R9410 100K 5% 1/10W MF-LF 402 <RFLT>

R9411 210K 1% 1/10W MF-LF 402 <RLIM>

(*) U9410 tolerance unknown

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

IFLT = 200k / RFLT = 885mA
ILIM = 201k / RLIM = 935mA
TFLT = CCT * 38900
TSD = CCT * 100000

Q9415 SSM3K15FV SOD-VESM-HF

Bleeder Resistor
2.5V / 249 ohm = 10mA
R9419 249 1% 1/10W MF-LF 402 P = ~27mW

DPAPWR_BLDR_E
MIN_LINE_WIDTH=0.20 MM
MIN_NECK_WIDTH=0.20 MM

Q9419 DMB53D0UV SOT-563

DPAPWR_BLDR_B

Note: Bleeder active when DPAPWRSW_HV_DET is HIGH and T29_A_HV_EN is LOW.

T29_A_HV_EN

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL D9425 POWERDI-123 DFLS1100

CRITICAL Q9425 SI8409DB 8A

3.3V/HV MUXed

3.3V Always

Blocking FET, off when Source >3.4V or HV_EN high.

R9427 100K 1% 1/10W MF-LF 402

R9425 4.7K 5% 1/10W MF-LF 402

R9426 1K 5% 1/16W MF-LF 402

R9430 4.7K 5% 1/16W MF-LF 402

R9428 21.5K 1% 1/10W MF-LF 402

DPAPWRSW_VREF

CRITICAL U9426 ZXRE060A SOT353 IN OUT GND PGND FB

R9429 4.7K 5% 1/10W MF-LF 402

C9424 0.47UF 10% 16V CERM-X5R 402

DPAPWRSW_P3V3_ON_L
DPAPWRSW_HV_DET_R_L
DPAPWRSW_ON_L_C
DPAPWRSW_HV_DET_L

NO STUFF C9429 0.1UF 20% 10V CERM 402

R9424 22 5% 1/16W MF-LF 402

C9426 0.1UF 20% 10V CERM 402

Q9426 MMDT3946XG SOT363

DPAPWRSW_NPN_E

R9418 1K 5% 1/10W MF-LF 402 DPAPWRSW_HV_DET

ZXRE060A REF range: 0.595-0.605V (0.600V nominal)
Circuit threshold range: 3.363-3.439V (3.395V nominal)

CRITICAL U9480 TPS2051B SOT23 OUT IN OC* EN GND

DP_PWR must be S4 to support wake from T29 devices.

PP3V3_S5

T29_A_HV_EN
SMC_S4_WAKESRC_EN

C9486 10UF 20% 6.3V X5R 603
C9485 0.1UF 20% 10V CERM 402
C9481 0.1UF 20% 10V CERM 402
C9480 22UF 20% 6.3V X5R-CERM-1 603
C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM

T29_A_BIAS

CRITICAL U9435 ZXRE060A SOT353 IN OUT FB PGND GND

C9435 0.1UF 20% 10V CERM 402

C9436 1UF 10% 10V X5R 402

DPAPWRSW_P3V3_ON

Q9430 SSM6N37FEAPE SOT563

DPAPWRSW_ON_C
T29_A_HV_EN

R9437 82 5% 1/10W MF-LF 402

T29_2V9_ENABLE

R9435 100K 1% 1/10W MF-LF 402

DPAPWR_FB_DIV

R9436 24.9K 1% 1/10W MF-LF 402

R9433 220 5% 1/16W MF-LF 402

R9432 10K 5% 1/16W MF-LF 402

DisplayPort/T29 A Connector

L9400 FERR-120-OHM-3A 0603

PP3V3RHV_SW_DPAPWR_UF
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

C9400 0.01UF 10% 50V X7R 402

PP3V3RHV_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

Circuit threshold range: 2.877-2.941V (2.903V nominal)

C9490 0.1UF 10% 6.3V X5R 201

PLACE_NEAR=C9490.1:2mm

R9490 51 5% 1/20W MF 201

T29_A_BIAS_R
VOLTAGE=3.3V

T29_A_BIAS_D2R_P1
T29_A_BIAS_D2R_N1

R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201

T29_D2R_C_P<0>
T29_D2R_C_N<0>

R9494 1K 5% 1/20W MF 201
SIGNAL_MODEL=EMPTY

R9495 1K 5% 1/20W MF 201
SIGNAL_MODEL=EMPTY

T29 Dir DP Dir

R9403 12 5% 1/16W MF-LF 402
GND_DPACONN_8
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

R9404 12 5% 1/16W MF-LF 402
GND_DPACONN_14
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

T29DPA_ML_P<3>
T29DPA_ML_N<3>
T29: Unused

T29_D2R_C_P<1>
T29_D2R_C_N<1>

D9498 BAR90-02LRH TSLP-2-7
D9499 BAR90-02LRH TSLP-2-7

CRITICAL L9498 650NH-5%-0.430MA-0.052OHM 0603
CRITICAL L9499 650NH-5%-0.430MA-0.052OHM 0603
SIGNAL_MODEL=T29PIN
(Both L's)

T29DPA_D2R1_AUXCH_P
T29DPA_D2R1_AUXCH_N

DP_A_EXT_AUXCH_P
DP_A_EXT_AUXCH_N

R9402 12 5% 1/10W MF-LF 402
T29DPA_HPD_R

R9401 12 5% 1/16W MF-LF 402
DPCONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

C9498 30PF 5% 50V CERM 402
C9499 30PF 5% 50V CERM 402
C9402 0.01UF 10% 50V X7R 402
C9401 0.01UF 10% 50V X7R 402

T29DPA_HPD

T29DPA_CONFIG1_RC
T29DPA_CONFIG2_RC

R9452 1M 5% 1/10W MF-LF 402
R9451 1M 5% 1/10W MF-LF 402

C9494 330PF 10% 50V CERM 402
C9495 330PF 10% 50V CERM 402

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

R9441 100K 5% 1/16W MF-LF 402

For J9400 T29 SMT pads (3, 5, 7, 8, 19):
GND_VOID=TRUE

CRITICAL J9400 DSPLYPRT-M97-1 F-RT-THSM

BOT ROW TH PINS / TOP ROW SM PINS

2	HOT_PLUG_DETECT	GND	1
4	CONFIG1	ML_LANE0P	3
6	CONFIG2	ML_LANE0N	5
8	GND	GND	7
10	ML_LANE3P	ML_LANE1P	9
12	ML_LANE3N	ML_LANE1N	11
14	GND	GND	13
16	AUX_CHP	ML_LANE2P	15
18	AUX_CHN	ML_LANE2N	17
20	DP_PWR	RETURN	19

SHIELD PINS 22 21

GND_DPACONN_1
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

R9405 12 5% 1/20W MF 201

DP Dir T29 Dir

T29DPA_ML_P<0>
T29DPA_ML_N<0>
T29: TX_0

GND_DPACONN_7
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

R9406 12 5% 1/20W MF 201

T29: LSX_R2P/P2R (P/N)

GND_DPACONN_13
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

R9407 12 5% 1/20W MF 201

T29DPA_ML_P<2>
T29DPA_ML_N<2>
T29: TX_1

GND_DPACONN_19
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

L9408 FERR-120-OHM-3A 0603

R9408 12 5% 1/20W MF 201

GND_VOID=TRUE (Both C's)

C9470 0.47UF 20% 4V CERM-X5R-1 201
C9471 0.47UF 20% 4V CERM-X5R-1 201
C9472 0.47UF 20% 4V CERM-X5R-1 201
C9473 0.47UF 20% 4V CERM-X5R-1 201

R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0 OHM,5,1/16W,0402,SMD,LF	C9412		
132S0121	1	CAP,CER,0.1UF,10%,6.3V,XSR,0201,SMD	R9405		
132S0121	1	CAP,CER,0.1UF,10%,6.3V,XSR,0201,SMD	R9406		

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

PAGE TITLE: DisplayPort/T29 A Connector

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

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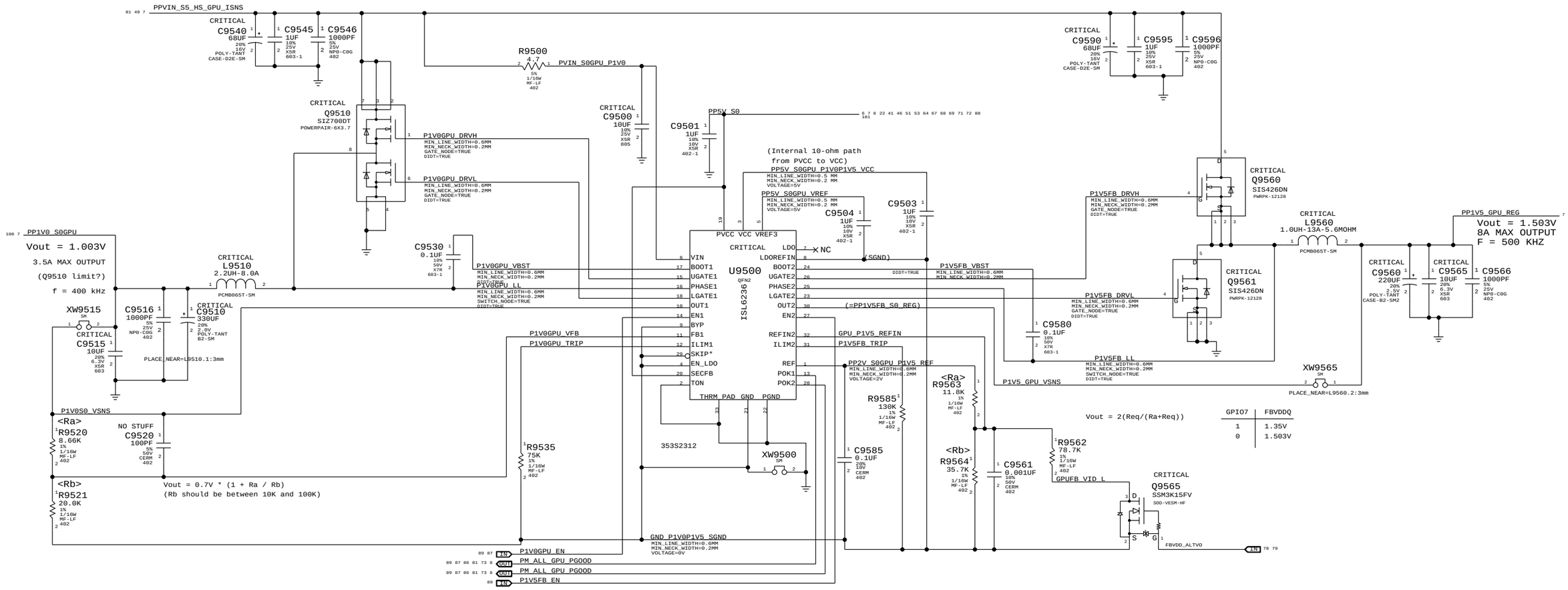

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: 1V0 GPU / 1V5 FB Power Supply

Apple Inc.

DRAWING NUMBER: SIZE D

REVISION:

BRANCH:

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GMUX CPLD

LVDS Receiver Termination

LVDS_IG_A_CLK_P	R9650	100	PLACE_NEAR=U9600.H3:5mm	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>	R9651	100	PLACE_NEAR=U9600.E1:5mm	LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>	R9652	100	PLACE_NEAR=U9600.E3:5mm	LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>	R9653	100	PLACE_NEAR=U9600.G1:5mm	LVDS_IG_A_DATA_N<2>
LVDS_IG_B_DATA_P<0>	R9654	100	PLACE_NEAR=U9600.G2:5mm	LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>	R9655	100	PLACE_NEAR=U9600.G3:5mm	LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>	R9656	100	PLACE_NEAR=U9600.B2:5mm	LVDS_IG_B_DATA_N<2>
LVDS_EG_A_CLK_P	R9660	100	PLACE_NEAR=U9600.J12:5mm	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>	R9661	100	PLACE_NEAR=U9600.D13:5mm	LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>	R9662	100	PLACE_NEAR=U9600.E14:5mm	LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>	R9663	100	PLACE_NEAR=U9600.F12:5mm	LVDS_EG_A_DATA_N<2>
LVDS_EG_B_DATA_P<0>	R9664	100	PLACE_NEAR=U9600.G14:5mm	LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>	R9665	100	PLACE_NEAR=U9600.G13:5mm	LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>	R9666	100	PLACE_NEAR=U9600.H12:5mm	LVDS_EG_B_DATA_N<2>

All: 1% 1/20W MF 201

Required Pullups

SIGNAL_MODEL=EMPTY

PP3V3_S0

EG_PWRSEQ_EN	R9684	1K	5% 1/20W MF 201
JTAG_GMUX_TDI	R9685	10K	5% 1/20W MF 201
JTAG_GMUX_TDO	R9686	10K	5% 1/20W MF 201
GMUX_DEBUG_RESET_L	R9680	1K	5% 1/20W MF 201

NO STUFF
R9679 10K 1% 1/10W MF-LF 402
SILK_PART=GMUX_RST

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K	5% 1/20W MF 201
LVDS_DDC_SEL_IG	R9682	10K	5% 1/20W MF 201
LVDS_DDC_SEL_EG	R9683	10K	5% 1/20W MF 201
EG_RESET_L	R9691	100K	5% 1/20W MF 201
LCD_BKLT_PWM	R9693	100K	5% 1/20W MF 201

NO STUFF
(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

R9600 0 5% 1/16W MF-LF 402 — PP3V3_S0
R9610 0 5% 1/16W MF-LF 402 — PP1V8_S0

PP3V3_S0_GMUX_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

C9610–C9629 0.1UF 20% 10V CERM 402

PP1V8_S0_GMUX_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=1.8V

C9611–C9617 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_ULC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

L9621 FERR-220-OHM 0402
C9631 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_LRC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

L9620 FERR-220-OHM 0402
C9630 0.1UF 20% 10V CERM 402

PP1V2_S0
C9600 4.7UF 20% 6.3V X5R-1 402
C9604–C9609 0.1UF 20% 10V CERM 402

PP3V3_S0
R9645 10K 1% 1/20W MF 201
R9640 10K 1% 1/20W MF 201
NO STUFF R9646 10K 1% 1/20W MF 201
NO STUFF R9641 10K 1% 1/20W MF 201

VCC: B11, C4, J3, J13, N11, P8
VCCAUX: C11, J2, J14, M8
VCCIO6: B5
VCCIO1: B7
VCCIO2: A12, C14, F13
VCCIO3: M12
VCCIO4: M9
VCCIO5: M3, N5
VCCIO6: M1
VCCIO7: C3, F2
VCCJ: K12
ULC_VCCPLL: A4
LRC_VCCPLL: P11

OMIT
CRITICAL
U9600
XP25-5
CSBGA

JTAG_ISP_TCK	K14	TCK
JTAG_GMUX_TDI	L13	TDI
JTAG_GMUX_TDO	K13	TDO
JTAG_GMUX_TMS	L12	TMS
GMUX_TOE	K2	TOE
GMUX_CFG0	K1	CFG0
LCD_BKLT_EN	P2	PB7A
LCD_BKLT_PWM	N2	PB7B
LVDS_DDC_SEL_EG	P4	PB14A
LVDS_DDC_SEL_IG	N4	PB14B
DP_MUX_EN	N3	PB15A (OD)
DP_MUX_SEL_EG	M4	PB15B
EG_RESET_L	P5	PB16A
P3V3GPU_EN	M5	PB16B
GPUVCORE_EN	P6	PB17A
P1V0GPU_EN	M6	PB17B
P1V5FB1V8GPU_R_EN	P7	PB18A
PEG_CLKREQ_L	M7	PB18B (OD)
DP_CA_DET_EG	N7	PB19A
LCD_PWR_EN	N8	PB19B
LPC_AD<0>	P9	PB20A
LPC_AD<1>	N9	PB20B
LPC_AD<2>	P10	PB26A
LPC_AD<3>	M10	PB26B
LPC_FRAME_L	P12	PB27A
LPCPLUS_RESET_L	P13	PB27B
LPC_CLK33M_GMUX	N12	PB28A
GMUX_INT	P14	PB28B
LVDS_IG_B_DATA_P<2>	B1	PL2A
LVDS_IG_B_DATA_N<2>	B2	PL2B
GMUX_PL6A	C2	PL6A
TP_GMUX_PL6B	D3	PL6B
LVDS_IG_A_DATA_P<0>	D1	PL7A
LVDS_IG_A_DATA_N<0>	E1	PL7B
LVDS_IG_A_DATA_P<1>	D2	PL8A
LVDS_IG_A_DATA_N<1>	E3	PL8B
LVDS_IG_A_DATA_P<2>	F1	PL9A
LVDS_IG_A_DATA_N<2>	G1	PL9B
LVDS_IG_B_DATA_P<0>	F3	PL10A
LVDS_IG_B_DATA_N<0>	G2	PL10B
LVDS_IG_B_DATA_P<1>	H2	PL11A
LVDS_IG_B_DATA_N<1>	G3	PL11B
LVDS_IG_A_CLK_P	H1	PL12A
LVDS_IG_A_CLK_N	H3	PL12B
TP_LVDS_MUX_SEL_EG	L1	PL14A
TP_GMUX_PL14B	L3	PL14B
GMUX_RESET_L	K3	PL15A
GMUX_VSYNC	L2	PL15B
PM_ALL_GPU_PGOOD	N1	PL25A
PEX_CLKREQ_L	P1	PL25B

BANK5: PB7A–PB28B
BANK4: PB20A–PB28B
BANK7: PL2A–PL12B
BANK6: PL14A–PL25B

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

GND: J1, B8, C6, C12, C13, C15, M14, N10, N6, P3, M2, C1, E2, B4, M11
GNDIO0–GNDIO7, ULC_GNDPLL, LRC_GNDPLL

PT7A	A2	LVDS_B_DATA_P<0>
PT7B	A3	LVDS_B_DATA_N<0>
PT8A	A1	LVDS_B_DATA_P<1>
PT8B	B3	LVDS_B_DATA_N<1>
PT9A	C5	LVDS_B_DATA_P<2>
PT9B	A5	LVDS_B_DATA_N<2>
PT14A	B6	EG_PWRSEQ_EN
PT14B	C7	GMUX_DEBUG_RESET_L
PT15A	A6	LVDS_A_CLK_P
PT15B	A7	LVDS_A_CLK_N
PT16A	C8	LVDS_B_CLK_P
PT16B	C9	LVDS_B_CLK_N
PT17A	A8	LVDS_A_DATA_P<0>
PT17B	B9	LVDS_A_DATA_N<0>
PT18A	A9	LVDS_A_DATA_P<1>
PT18B	C10	LVDS_A_DATA_N<1>
PT19A	B10	LVDS_A_DATA_P<2>
PT19B	A10	LVDS_A_DATA_N<2>
PT20A	A11	GND
PT20B	B12	GND
PT28A	B13	GND
PT28B	A13	GND

BANK1: PT7A–PT19B
BANK2: PR2A–PR12B
BANK3: PR14A–PR24B

PR2A	A14	DP_A_CA_DET
PR2B	B14	DP_HOTPLUG_DET
PR6A	D12	LVDS_EG_A_DATA_P<0>
PR6B	D13	LVDS_EG_A_DATA_N<0>
PR7A	D14	LVDS_EG_A_DATA_P<1>
PR7B	E14	LVDS_EG_A_DATA_N<1>
PR8A	E12	LVDS_EG_A_DATA_P<2>
PR8B	F12	LVDS_EG_A_DATA_N<2>
PR9A	F14	LVDS_EG_B_DATA_P<0>
PR9B	G14	LVDS_EG_B_DATA_N<0>
PR10A	G12	LVDS_EG_B_DATA_P<1>
PR10B	G13	LVDS_EG_B_DATA_N<1>
PR11A	H13	LVDS_EG_B_DATA_P<2>
PR11B	H12	LVDS_EG_B_DATA_N<2>
PR12A	H14	LVDS_EG_A_CLK_P
PR12B	J12	LVDS_EG_A_CLK_N
PR14A	L14	LVDS_IG_PANEL_PWR
PR14B	M13	EG_LCD_PWR_EN
PR24A	N14	LVDS_IG_BKL_ON
PR24B	N13	EG_BKLT_EN

CRITICAL
J9600 1909782 M-RT-SM — GMUX_JTAG_CONN

1	PP3V3_S0
2	JTAG_GMUX_TDO
3	JTAG_GMUX_TDI
4	JTAG_GMUX_TMS
5	
6	JTAG_ISP_TCK
8	

NO STUFF R9647 10K 1% 1/20W MF 201

PP3V3_S0 → R9670 10K 1% 1/20W MF 201 → GMUX_VSYNC

R9605 1K 5% 1/20W MF 201 — PP3V3_T29 → T29_JTAG_FET

Q9605 SSM6N15FEAPE SOT563 — JTAG_GMUX_TDI → JTAG_ISP_TDI
Q9605 SSM6N15FEAPE SOT563 — JTAG_GMUX_TDO → JTAG_ISP_TDO

PP3V3_S3 → R9676 100K 5% 1/20W MF 201 → GMUX_S3_PD_EN

Q9607 SSM6N15FEAPE SOT563 — GMUX_S3_PD_EN
Q9607 SSM6N15FEAPE SOT563 — ALL_SYS_PWRGD

R9678 4.7K 5% 1/20W MF 201
R9671 4.7K 5% 1/20W MF 201
R9672 4.7K 5% 1/20W MF 201
R9673 4.7K 5% 1/20W MF 201
R9674 4.7K 5% 1/20W MF 201
→ GMUX_S3_PD_GND

NO STUFF R9675 0 5% 1/10W MF-LF 402

SYNC_MASTER	K91_MARY
SYNC_DATE	08/03/2010
PAGE TITLE	Graphics MUX (GMUX)
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Apple Inc.

PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)

THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

PPBUS_G3H
F9700 3AMP-32V-467 603-HF BOTTOM
PPBUS_S0_LCDBKLT_FUSED
CRITICAL Q9706 FDC638APZ_SBMS001 SSOT6-HF
PPBUS_SW_LCDBKLT_PWR
R9788 301K 1% 1/16W MF-LF 402
C9782 0.1UF 10% 16V X5R 402
LCDBKLT_EN_DIV
R9789 147K 1% 1/16W MF-LF 402
LCDBKLT_EN_L
Q9707 SSM6N15FEAPE SOT563
LCD_BKLT_EN
LCDBKLT_DISABLE
Q9707 SSM6N15FEAPE SOT563
BKLT_PLT_RST_L
PP5V_S0
PPBUS_SW_BKL
CRITICAL C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
PLACE_NEAR=L9701.1:3mm
PLACE_NEAR=L9701.1:3mm
CRITICAL L9701 33UH-1.8A-110OHM 1217AS-2SM
PPBUS_SW_LCDBKLT_PWR_SW
CRITICAL D9701 SOD-123 RB160M-60G
PLACE_NEAR=L9701.2:3mm
PLACE_NEAR=U9701.A5:3mm
C9796 220PF 10% 50V X7R-CERM 402
CRITICAL C9797 10UF 10% 50V X5R 1210-1
CRITICAL C9799 10UF 10% 50V X5R 1210-1
PLACE_NEAR=D9701.2:5mm
PLACE_NEAR=D9701.2:3mm
PPVOUT_S0_LCDBKLT
PLACE_NEAR=U9701.D1:5mm
C9710 1UF 10% 25V X5R 603-1
C9714 0.01UF 10% 25V X7R-CERM 402
PLACE_NEAR=U9701.D1:3mm
XW9720 SM
PPVOUT_SW_LCDBKLT_FB
PLACE_NEAR=C9797.1:5mm
PP3V3_S0
PLACE_NEAR=U9701.C4:4mm
C9711 0.1UF 10% 16V X5R 402
BKL_VSYNC_R
MIN_NECK_WIDTH=0.075 mm
NO STUFF R9754 0 5% 1/16W MF-LF 402
R9755 10K 5% 1/16W MF-LF 402
NO STUFF C9741 1UF 10% 6.3V X5R 402
GMUX_VSYNC
NO STUFF C9740 10UF 20% 6.3V X5R 603
NO STUFF R9740 47.0K 1% 1/16W MF-LF 402
R9741 10K 1% 1/16W MF-LF 402
MIN_NECK_WIDTH=0.075 mm
R9753 0 5% 1/16W MF-LF 402
SMBUS_PCH_CLK
R9757 0 5% 1/16W MF-LF 402
SMBUS_PCH_DATA
Addr: 0x58(Wr)/0x59(Rd)
PPBUS_SW_LCDBKLT_PWR
R9731 301K 1% 1/16W MF-LF 402
R9715 100K 1% 1/16W MF-LF 402
PLACE_SIDE=BOTTOM
R9704 33 5% 1/16W MF-LF 402
LCD_BKLT_PWM
C9704 33PF 5% 50V C0GRM 402
U9701 25-BUMP-MICRO LP8550
VDDIO VLDO VIN
VSYNC SW_0 SW_1 FB FILTER ISET FSET SCLK SDA PWM EN FAULT GND_S GND_L GND_SW GND_SW
BKL_FLTR BKL_ISET BKL_FSET BKL_SCL BKL_SDA BKL_PWM BKL_EN TP_BKL_FAULT
OUT1 OUT2 OUT3 OUT4 OUT5 OUT6
BKL_ISEN1 BKL_ISEN2 BKL_ISEN3 BKL_ISEN4 BKL_ISEN5 BKL_ISEN6
CRITICAL
R9716 90.9K 1% 1/16W MF-LF 402
R9714 16.2K 1% 1/16W MF-LF 402
I_LED=22.7mA
Fpwm=9.62kHz
see spec for others
PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)
XW9710 SM
GND_BKL_SGND
I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

BKLT:PROD R9717 0 5% 1/16W MF-LF 402 LED_RETURN_1
BKLT:PROD R9718 0 5% 1/16W MF-LF 402 LED_RETURN_2
BKLT:PROD R9719 0 5% 1/16W MF-LF 402 LED_RETURN_3
BKLT:PROD R9720 0 5% 1/16W MF-LF 402 LED_RETURN_4
BKLT:PROD R9721 0 5% 1/16W MF-LF 402 LED_RETURN_5
BKLT:PROD R9722 0 5% 1/16W MF-LF 402 LED_RETURN_6

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K901_KIRA SYNC DATE=06/25/2010

LCD Backlight Driver

Apple Inc.

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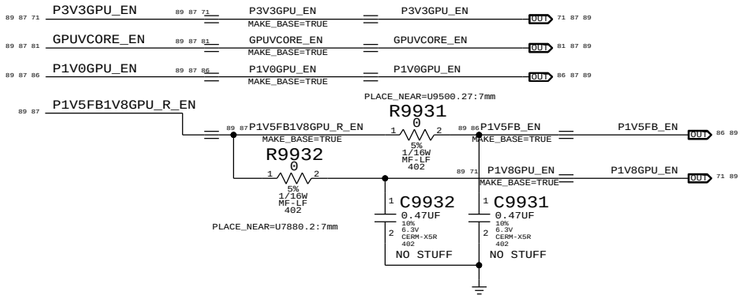
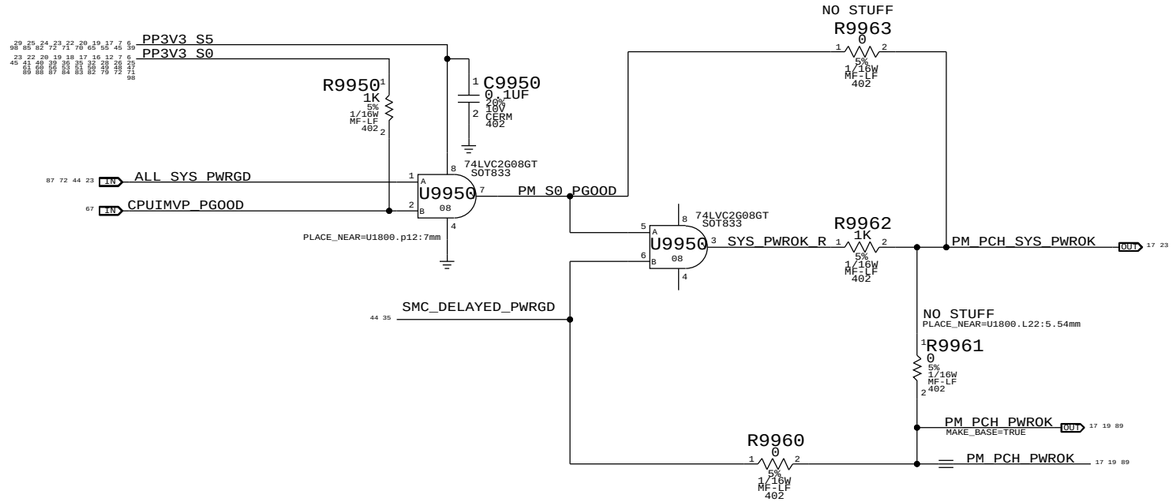
GPU Rail Sequencing

Whistler GPU requires rails to come up in the following order:

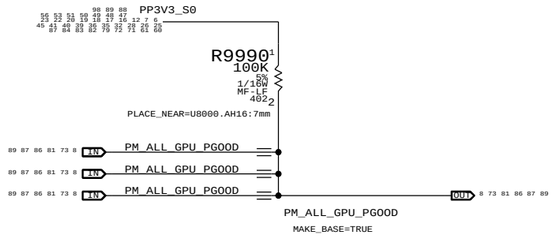
1) GPU_3.3V
2) GPUVcore
3) GPU_1.0V
4) GPU_1.8V;GDDR5 1.5/1.35V



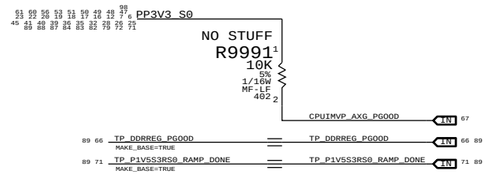
PCH S0 PWRGD



EXT GPU PWRGD Pullup



Unused PGOOD signal



SYNC_MASTER=K91_MARY SYNC_DATE=08/03/2010

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	6 9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	6 9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	6 9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	6 9 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
	CPU_50S	CPU_AGTL	FDI_INT	6 9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 44
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 29
XDP_CPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	23
XDP_BDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..16>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	10 17
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 45 67
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_55S	CPU_8MIL	CPU_PSI_L	
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	10 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 67
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	12
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	
	CPU_50S	CPU_AGTL	GFX_VR_EN	
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	
	PCIE_85D	PCIE	PEG_R2D_P<7..0>	73
	PCIE_85D	PCIE	PEG_R2D_N<7..0>	73
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<7..0>	8 73
	PCIE_85D	PCIE	PEG_R2D_C_N<7..0>	8 73
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<7..0>	8 73
	PCIE_85D	PCIE	PEG_D2R_N<7..0>	8 73
	PCIE_85D	PCIE	PEG_D2R_C_P<7..0>	73
	PCIE_85D	PCIE	PEG_D2R_C_N<7..0>	73
	CPU_50S	CPU_VID	CPU_VIDSOUT	12 67
	CPU_50S	CPU_VID	CPU_VIDSCLK	12 67
	CPU_50S	CPU_VID	CPU_VIDALERT_L	12 67

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 6 11 26
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0> 6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0> 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 6 11 26
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 6 11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 6 11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 6 11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 6 11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 6 11 26 27
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 6 11 27
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 6 11 27
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 6 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 6 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 6 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 6 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 6 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 6 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 6 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 6 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 6 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 6 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 6 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 6 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 6 11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 6 11 26 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 6 11 26 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 6 11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 6 11 27
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 6 11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0> 6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0> 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 6 11 28
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 6 11 27
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 6 11 27
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 6 11 27
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 6 11 27
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 6 11 27 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 6 11 27
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 6 11 27
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 6 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 6 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 6 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 6 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 6 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 6 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 6 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 6 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 6 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 6 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 6 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 6 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 6 11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 6 11 27 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 6 11 27 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 6 11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 6 11 27

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
LVDS	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	ISL3,ISL4,ISL9,ISL10	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P 8 17 83
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N 8 17 83
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P 18 87
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N 18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0> 18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0> 18 87
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3> 8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3> 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0> 18 87
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0> 18 87
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P 16 41
	SATA_90D	SATA	SATA_HDD_R2D_C_N 16 41
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_N 6 41
T21 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P 41
T21	SATA_90D	SATA	SATA_HDD_R2D_UF_N 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P 16 41
	SATA_90D	SATA	SATA_HDD_D2R_N 16 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_C_P 6 41
	SATA_90D	SATA	SATA_HDD_D2R_C_N 6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P 16 41
	SATA_90D	SATA	SATA_ODD_R2D_C_N 16 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P 6 41
	SATA_90D	SATA	SATA_ODD_R2D_N 6 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P 16 41
	SATA_90D	SATA	SATA_ODD_D2R_N 16 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_UF_P 6 41
	SATA_90D	SATA	SATA_ODD_D2R_UF_N 6 41
T21 PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP 16
T21 PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP 16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P 18 24
	USB_85D	USB	USB_HUB1_UP_N 18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P 18 24
	USB_85D	USB	USB_HUB2_UP_N 18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P 24 42
	USB_85D	USB	USB_EXTA_N 24 42
USB_EXTB	USB_85D	USB	USB_EXTB_P 24 42
	USB_85D	USB	USB_EXTB_N 24 42
USB_EXTC	USB_85D	USB	USB_EXTC_P 8 24
	USB_85D	USB	USB_EXTC_N 8 24
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 6 31
	USB_85D	USB	USB_CAMERA_CONN_N 6 31
USB_BT	USB_85D	USB	USB_BT_P 24 31
	USB_85D	USB	USB_BT_N 24 31
USB_TPAD	USB_85D	USB	USB_TPAD_P 24 52
	USB_85D	USB	USB_TPAD_N 24 52
USB_IR	USB_85D	USB	USB_IR_P 24 43
	USB_85D	USB	USB_IR_N 24 43
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS 18
T21 USB_T29A	USB_85D	USB	USB_T29A_P 8 24
T21	USB_85D	USB	USB_T29A_N 8 24

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
LPC_AD	LPC_50S	LPC	LPC AD<3..0>	6 16 44 46 87
LPC_FRAME_L	LPC_50S	LPC	LPC FRAME_L	6 16 44 46 87
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 25 46 87
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC R	18 25
	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC	25 44
	CLK_LPC_50S	CLK_LPC	LPC CLK33M LPCPLUS	6 25 46
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 23 26 28 30 41 47 61 88
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 23 26 28 30 41 47 61 88
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 47
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 47
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 47
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 47
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 56
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 56
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	16 56
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 56
	HDA_50S	HDA	AUD_SDI_R	56
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 56
	HDA_50S	HDA	HDA_SDOUT_R	16
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 46
	SPI_55S	SPI	SPI_CLK	46
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 46
	SPI_55S	SPI	SPI_MOSI	46
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 46
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 46
	SPI_55S	SPI	SPI_CS0_L	46
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	36
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 36
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 36
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 36
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	36
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	36
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 31
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 31
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 16 31
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 16 31
	PCIE_85D	PCIE	PCIE_FW_R2D_P	38
	PCIE_85D	PCIE	PCIE_FW_R2D_N	38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 38
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 38
	PCIE_85D	PCIE	PCIE_FW_D2R_N	16 38
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	38
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	38
T25	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
T24	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
T23	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 33
T22	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 33
T35	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
T37	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
T36	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
T34	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
T33	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
T26	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 25
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	16 73
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	16 73
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 31
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 38
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_P	8 16
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_N	8 16
T28	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 9 33
T27	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 9 33
T29	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	33
T30	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	33
T28	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	8 9 33
T27	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	8 9 33
T29	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	33
T30	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	33

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR	*	=3X_DIELECTRIC	?

SOURCE: Attila Farkas Email - 8/2/10

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
	ENET_50S	ENET_3X	ENET_RESET_L	32 36
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_DATA_R<7..0>	
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_CMD_R	32
CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK_R	32
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_DATA<7..0>	32 36
CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_CMD	32 36
CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK	32 36
CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK_R_L	32

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 38 40
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	38 40
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	6 38 40
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	6 38 40
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	38 40
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	38 40
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	38 40
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	38 40

Port 2 Not Used

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius’s T29 Routing Notes

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	6 84
T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	6 84
T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	6 84
T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	6 84
	T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	84
	T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	84
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0>	6 84 85
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0>	6 84 85
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1>	6 84 85
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1>	6 84 85
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	6 85
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	6 84
	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	6 84
	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	84
	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	84
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	6 84 95
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	6 84 95
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	84
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	84
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	84
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	84
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	84
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	84
	T29DP_80D	T29DP	T29DPA_ML_P<3..0>	6 84 85
	T29DP_80D	T29DP	T29DPA_ML_N<3..0>	6 84 85
	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	84 85
	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	84 85
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	84 85
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	84 85
T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>	
T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>	
	T29DP_80D	T29DP	T29_R2D_C_F_P<3..2>	
	T29DP_80D	T29DP	T29_R2D_C_F_N<3..2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	95
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	95
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
	T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	6 33 78
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	6 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	6 33 78
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	6 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	6 33 78
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	6 33
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	6 33 78
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	6 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	
	T29_I2C_55S	T29_I2C	I2C_T29_SCL	33 47 84
	T29_I2C_55S	T29_I2C	I2C_T29_SDA	33 47 84
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	33
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	33
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	33
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	33
	T29DP_80D	T29DP	T29_R2D_C_P<3..0>	6 8 33 84
	T29DP_80D	T29DP	T29_R2D_C_N<3..0>	6 8 33 84
	T29DP_100D	T29DP	T29_D2R_P<3..0>	6 8 33 84
	T29DP_100D	T29DP	T29_D2R_N<3..0>	6 8 33 84

Only used on hosts supporting T29 video-in

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL 6 31 44 47 53 54
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA 6 31 44 47 53 54
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL 44 47 50
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA 44 47 50
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL 6 31 44 47 50 79
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA 6 31 44 47 50 79
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL 6 44 47 62 63
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA 6 44 47 62 63
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL 44 47 100
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA 44 47 100

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 63
	1TO1_DIFFPAIR		CHGR_CSI_N 63
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 63
	1TO1_DIFFPAIR		CHGR_CSO_N 63

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: SMC Constraints

Apple Inc.

DRAWING NUMBER | SIZE: D

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	75 76
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	75 76
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	75 76
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_A<8..0>	6 75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_A<8..0>	6 75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_ABI_L	6 75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_ABI_L	6 75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_RAS_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_RAS_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CAS_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CAS_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_WE_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_WE_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CKE_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CKE_L	75 76
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CS_L	75 76
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CS_L	75 76
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	6 75 76
L295 FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	6 75 76
L293 FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	6 75 76
L292 FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	6 75 76
L290 FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	6 75 76
L297 FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	6 75 76
L298 FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	6 75 76
L299 FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	6 75 76
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	6 75 76
L295 FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	6 75 76
L300 FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	6 75 76
L302 FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	6 75 76
L302 FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	6 75 76
L303 FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	6 75 76
L304 FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	6 75 76
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	6 75 76
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>	6 75 76
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>	6 75 76
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>	6 75 76
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>	6 75 76
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>	6 75 76
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>	6 75 76
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>	6 75 76
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>	6 75 76
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	6 75 76
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	6 75 76
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	6 75 76
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	6 75 76
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	6 75 76
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	6 75 76
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	6 75 76
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	6 75 76
FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB_RESET_L	75 76 77

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	75 77
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	75 77
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	75 77
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_A<8..0>	6 75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_A<8..0>	6 75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_ABI_L	6 75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_ABI_L	6 75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_RAS_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_RAS_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CAS_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CAS_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_WE_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_WE_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CKE_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CKE_L	75 77
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CS_L	75 77
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CS_L	75 77
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	6 75 77
L305 FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	6 75 77
L306 FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	6 75 77
L307 FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	6 75 77
L310 FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	6 75 77
L308 FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	6 75 77
L309 FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	6 75 77
L311 FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	6 75 77
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	6 75 77
L314 FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	6 75 77
L312 FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	6 75 77
L314 FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	6 75 77
L314 FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	6 75 77
L314 FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	6 75 77
L314 FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	6 75 77
L314 FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	6 75 77
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	6 75 77
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	6 75 77
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	6 75 77
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	6 75 77
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	6 75 77
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	6 75 77
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	6 75 77
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	6 75 77
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	6 75 77
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	6 75 77
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	6 75 77
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	6 75 77
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	6 75 77
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	6 75 77
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	6 75 77
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	6 75 77

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P	83 87
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N	83 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>	83 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>	83 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P	83 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N	83 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>	83 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>	83 87
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P	6 82
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N	6 82
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P	6 82
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N	6 82
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P	82 83
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N	82 83
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P	82 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N	82 83
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>	6 82 83

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	78 79
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M	78 79
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P	78 87
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N	78 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>	78 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>	78 87
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>	78 79
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>	78 79
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>	78 87
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>	78 87
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>	78 79
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>	78 79
DP_MI	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	78 84
	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	78 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	83 84
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	83 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUXCH_P	8 78 83
	DP_85D	DISPLAYPORT	DP_EG_AUXCH_N	8 78 83

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GPU (Whistler) CONSTRAINTS

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K91 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	50
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	50
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	50
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	50 78
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	50 78
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	48 64
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	48 64
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_P	48
	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_N	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P	48
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	48 69
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	48 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_P	48
	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_N	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	48
	SENSE_1TO1_55S	SENSE	GPUISENS_P	48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	48 66
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	48 66
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	98
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	98
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	100
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	100
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	
	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	100
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P	100
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_P	
	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_R_P	100
	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_R_N	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_P	
	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_R_P	100
	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_R_N	100
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	49 68
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	49 68
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	49
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	49
	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	49
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	49
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 59
	AUDIODIFF	AUDIO	AUD_LO1_R_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 59
	AUDIODIFF	AUDIO	AUD_LO2_L_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 59
	AUDIODIFF	AUDIO	AUD_LO2_R_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	59
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	59
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_P	59
	AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_N	59

K91 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 31
	1TO1_DIFFPAIR		CHGR_CSI_R_P	63
	1TO1_DIFFPAIR		CHGR_CSI_R_N	63
	1TO1_DIFFPAIR		CHGR_CSO_R_P	49 63
	1TO1_DIFFPAIR		CHGR_CSO_R_N	49 63
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	42
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	6 42
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	6 42
	USB_85D	USB	CONN_USB2_BT_P	6
	USB_85D	USB	CONN_USB2_BT_N	6
	USB_85D	USB	USB_LT2_P	6 42
	USB_85D	USB	USB_LT2_N	6 42
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375L_P	59
	AUDIODIFF	AUDIO	SSM2375L_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375R_P	59
	AUDIODIFF	AUDIO	SSM2375R_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375S_P	59
	AUDIODIFF	AUDIO	SSM2375S_N	59
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	6 59 60
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	6 59 60
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	6 59 60
	USB_85D	USB	USB_TPAD_R_P	52
	USB_85D	USB	USB_TPAD_R_N	52
		SB_POWER	PP3V3_S5	45 55 65 70 71 72 82 85 89 6 7 17 19 20 22 23 24 25 29 39
		SB_POWER	PP3V3_S0	40 41 50 51 53 56 60 61 71 72 6 7 12 16 17 18 19 20 22 23 25 75 83 83 84 87 88 89 41 45 47 75 82
		SB_POWER	PP1V5_S3RS0	
		GND	GND	

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K91 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

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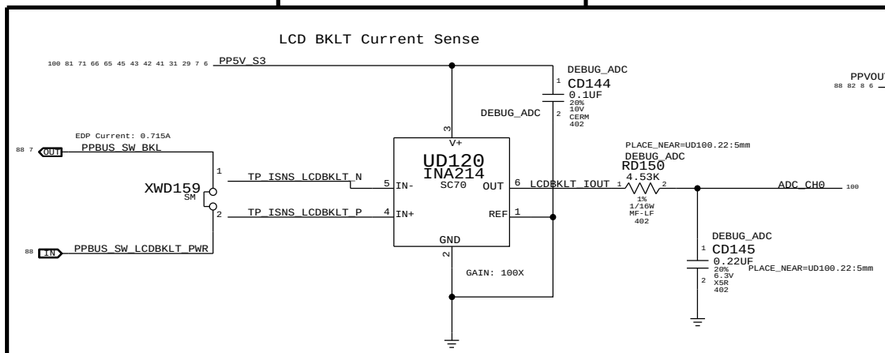

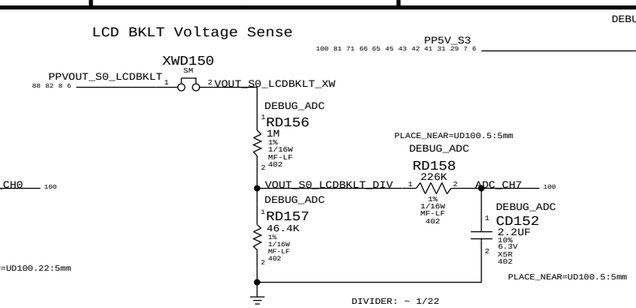

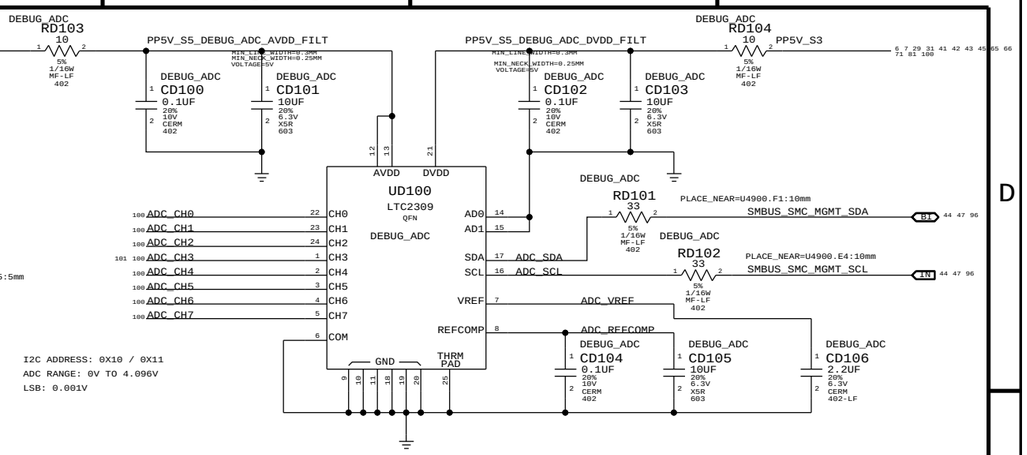

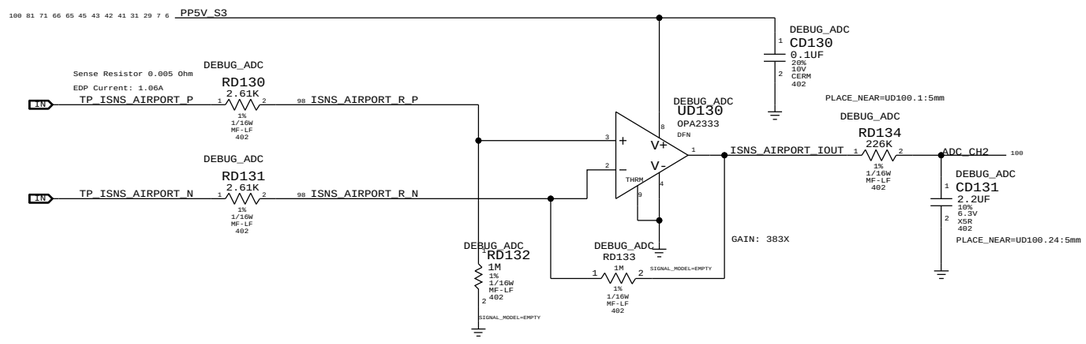

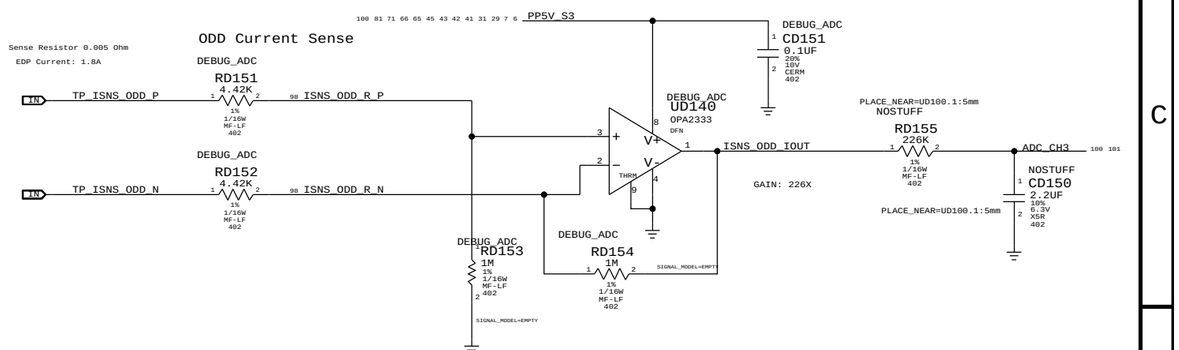

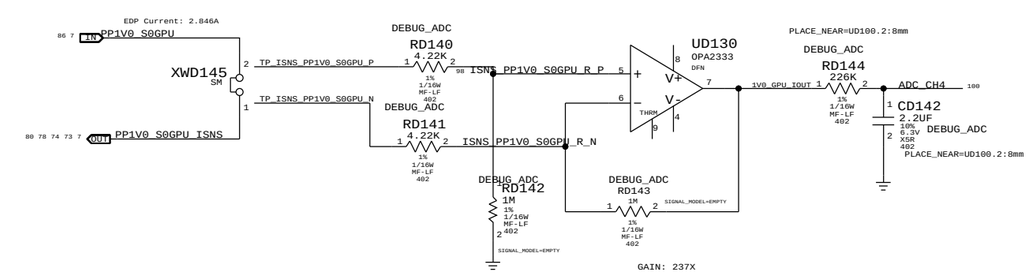

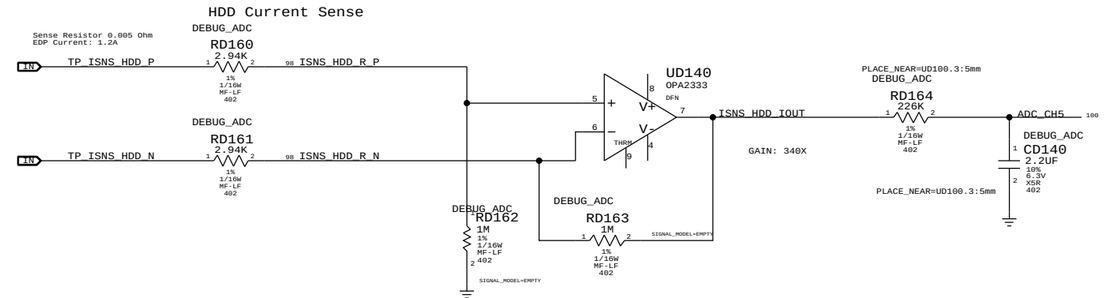

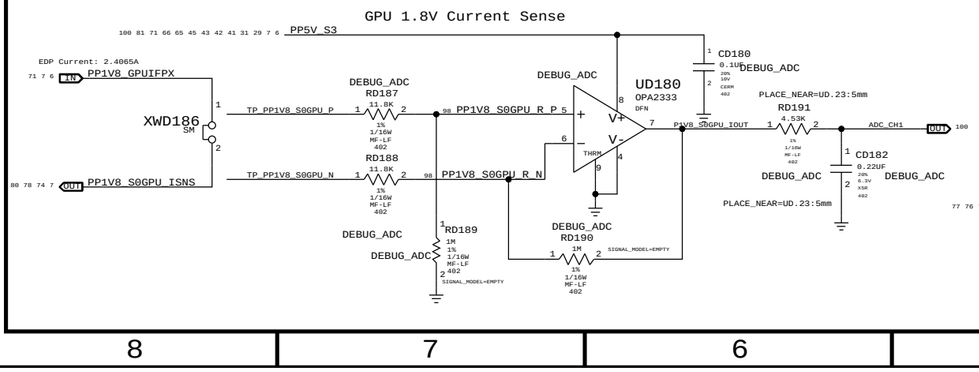

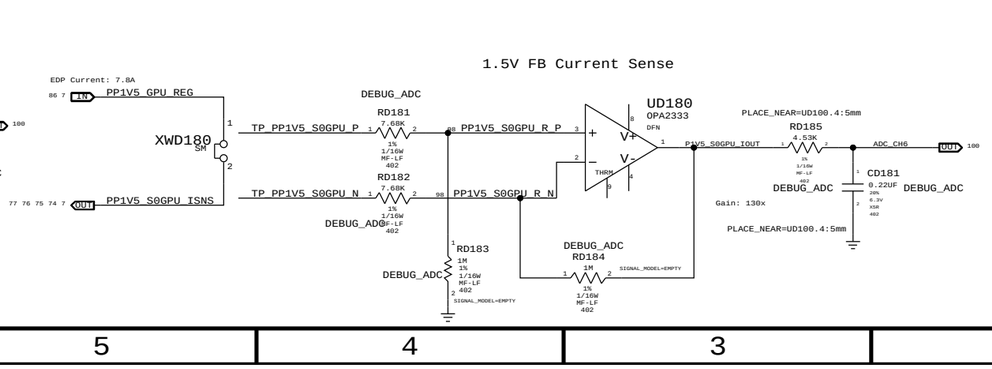

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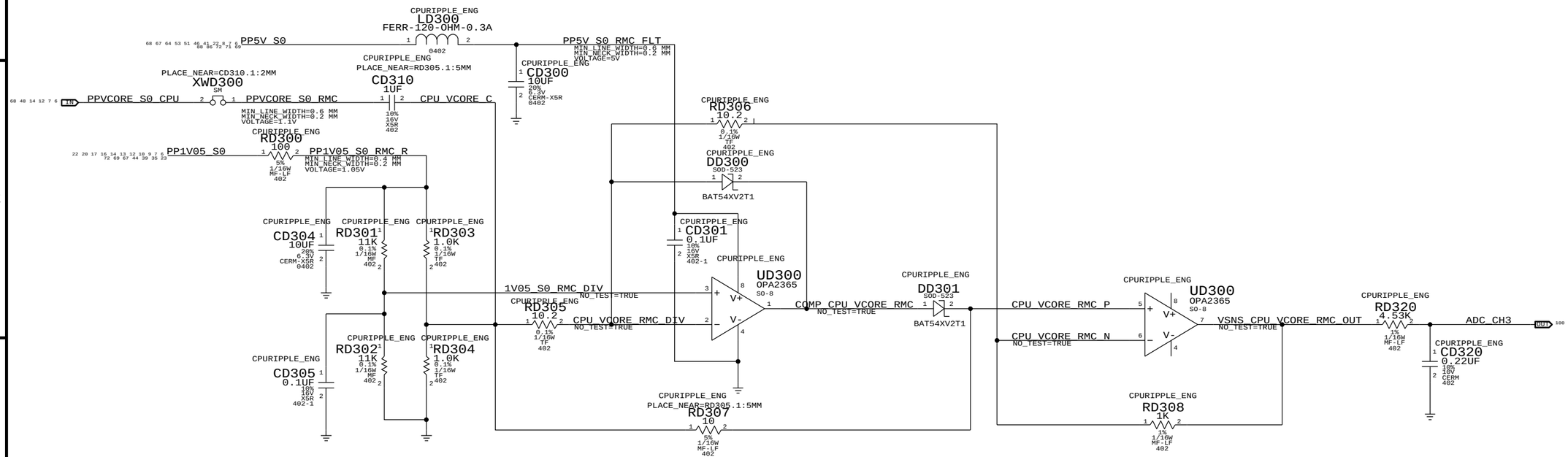

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