F9J SCHEMATIC Revision 2.0

SYSTEM PAGE REF.

POWER PAGE REF.

<Variant Name>

Title : PAGE REF.

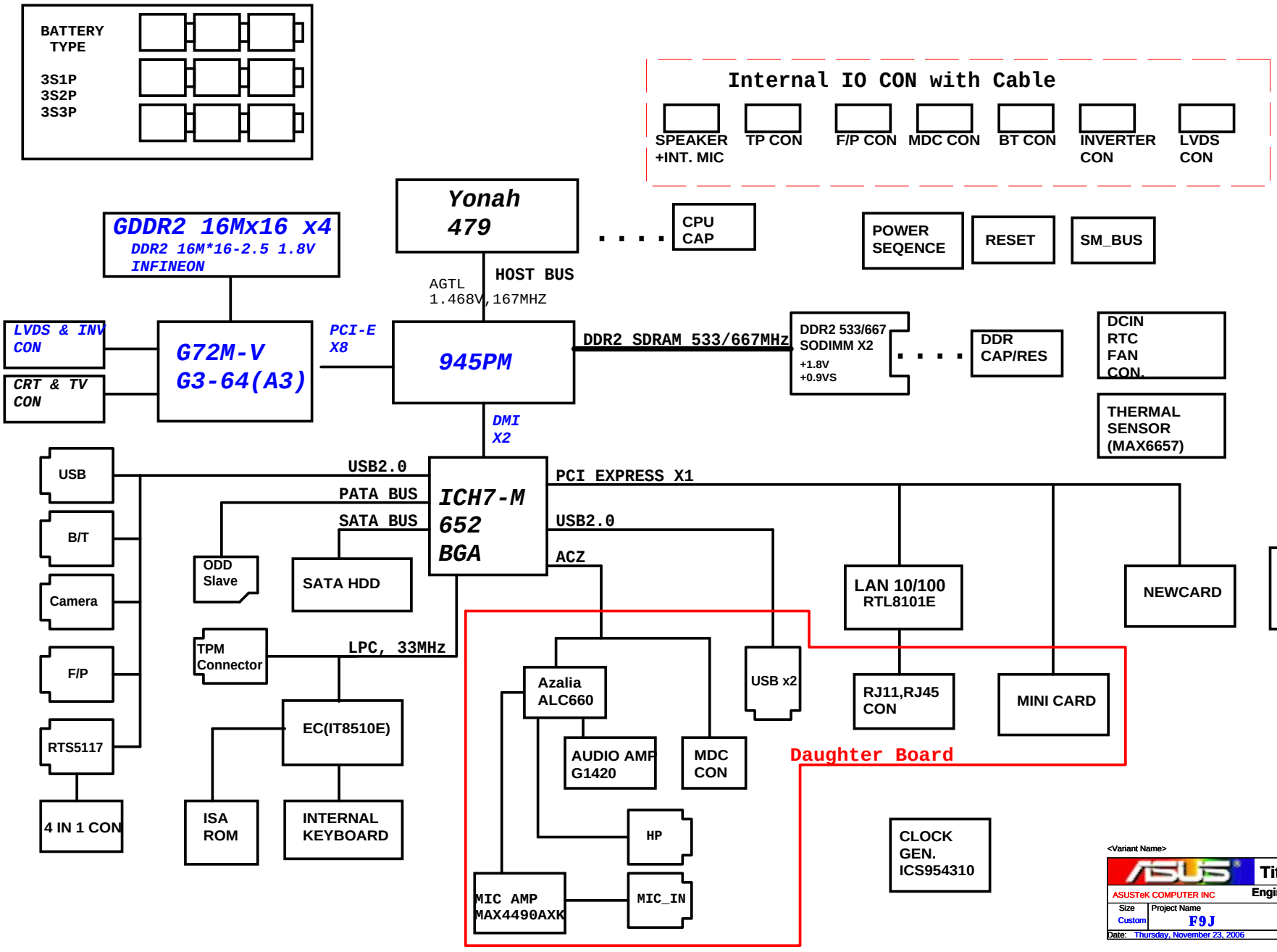
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: Thursday, November 23, 2006 Sheet 1 of 63

F9J BLOCK DIAGRAM



<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	N/A	I
47	CLKOUT/GPC0	N/A	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	N/A	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PCI_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	N/A	
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_SW#	I
88	ADC5/GPE1	BT_SW#	I
89	ADC6/GPE2	N/A	
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	N/A	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	N/A	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	N/A	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
81	ADC0	BAT_AD	I
82	ADC1	ADP_ERR#	I
83	ADC2	AC_AD	I
84	ADC3	N/A	
93	ADC8	KID0	
94	ADC9	KID1	
99	DAC0	N/A	
100	DAC1	N/A	
101	DAC2	INVTER_DA	O
102	DAC3	BATSEL_2P#	O

ICH7M_PCI EXPRESS

PCI-E Device	PAIR
RTL8101E	1
GOLAN	2
NEWCARD	3

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A4)
Thermal Sensor(MAX6657)--CPU	1001100x (98)
Thermal Sensor(G781-1)--VGA	1001101x (9A)

PCI Device	IDSEL#	REQ/GNT#	Interrupts

ICH7M_GPIO

Pin			Use As	Signal Name	Power
GPIO 00	i		GPI	PM_BMBUSY#	+3VS
GPIO 01	i		GPI	PCI_REQ#5	+3VS
GPIO [5:2]	i		GPI	PCI_INT[E:H]#	+3VS
GPIO 06	i		GPO	BT_LED_EN	+3VS
GPIO 07	i		GPI	RF_ON_SW#	+3VS
GPIO 08	i		GPI	EXTSMI#	+3VSUS
GPIO 09	i		GPI	N/A	+3VSUS
GPIO 10	i		GPI	N/A	+3VSUS
GPIO 11	i		Native	SMB_ALERT#	+3VSUS
GPIO 12	i		GPI	KBC_SCI#	+3VSUS
GPIO 13	i		GPI	N/A	+3VSUS
GPIO 14	i		GPI	N/A	+3VSUS
GPIO 15	i		GPO	802_LED_EN	+3VSUS
GPIO 16	O	0	GPO	PM_DPRSLPVR	+3VS
GPIO 17	O	1	GPO	PCI_GNT#5	+3VS
GPIO 18	O	1	GPO	STP_PCI#	+3VS
GPIO 19	i	1	GPI	N/A	+3VS
GPIO 20	O	1	GPO	STP_CPU#	+3VS
GPIO 21	i	1	GPO	N/A	+3VS
GPIO 22	i	1	Native	PCI_REQ#4	+3VS
GPIO 23	i	1	Native	N/A	+3VS
GPIO 24	O	0	GPO	MSK_PCIRST	+3VSUS
GPIO 25	O	1	GPO	N/A	+3VSUS
GPIO 26	O	0	GPO	BT_ON#	+3VSUS
GPIO 27	O	0	GPO	WLAN_ON#	+3VSUS
GPIO 28	O	0	GPO	N/A	+3VSUS
GPIO 29	i	0	Native	USB_OC#5	+3VSUS
GPIO 30	i	0	Native	USB_OC#6	+3VSUS
GPIO 31	i	0	Native	USB_OC#7	+3VSUS
GPIO 32	O	1	GPO	PM_CLKRUN#	+3VS
GPIO 33	O	1	GPO	N/A	+3VS
GPIO 34	O	0	GPO	N/A	+3VS
GPIO 35	O	0	GPO	N/A	+3VS
GPIO 36	i	0	GPO	N/A	+3VS
GPIO 37	i	0	GPI	PCB_ID0	+3VS
GPIO 38	i	0	GPI	PCB_ID1	+3VS
GPIO 39	i	0	GPI	PCB_ID2	+3VS
GPIO [40:47]			NA	NA	NA
GPIO 48			Native	PCI_GNT#4	+3VS
GPIO 49			Native	H_PWRGD	+VCORE

<Variant Name>

Title : Schematic data

ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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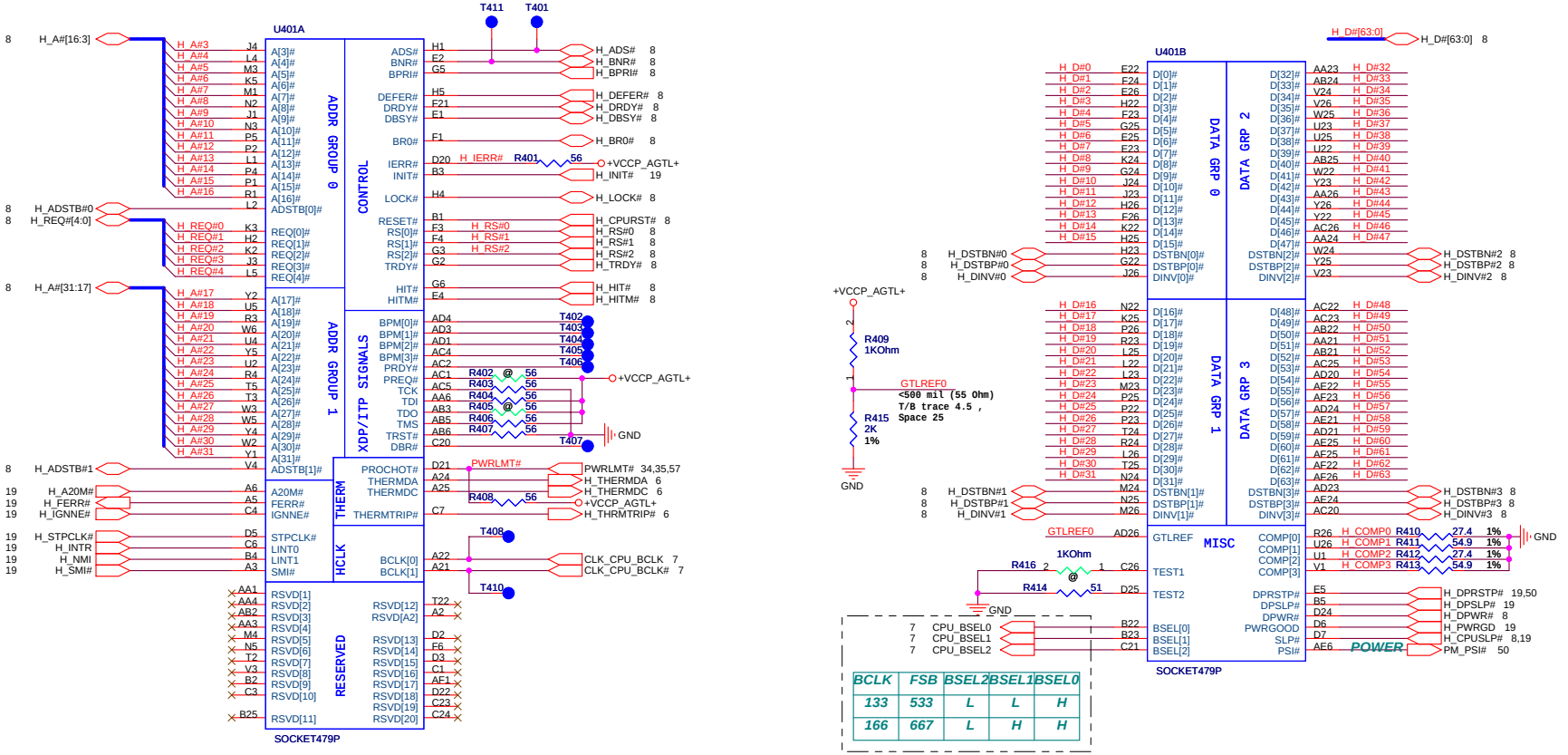

<Variant Name>

ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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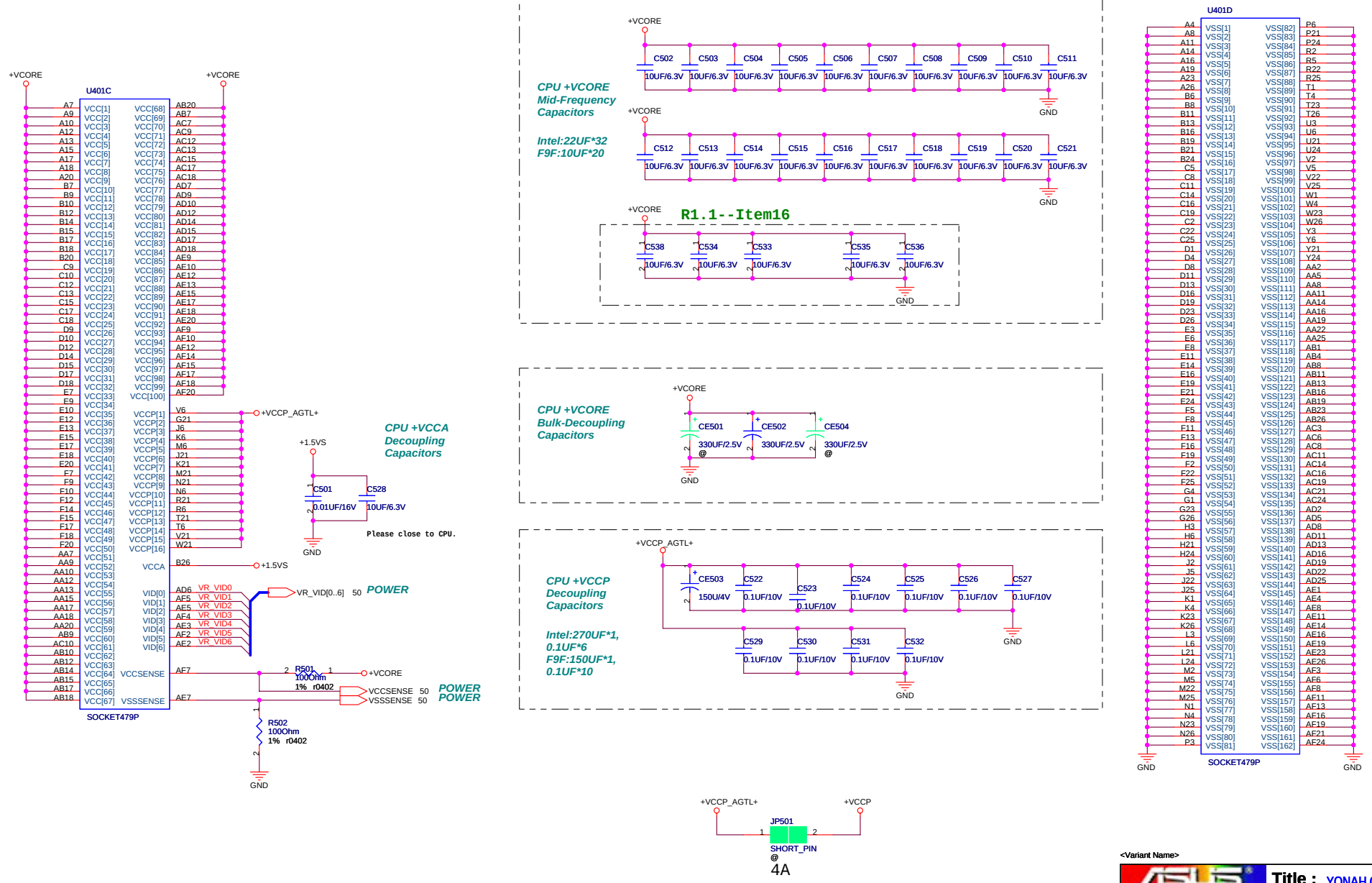

<Variant Name>

ASUSTeK COMPUTER INC	Title : YONAH CPU (2)	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
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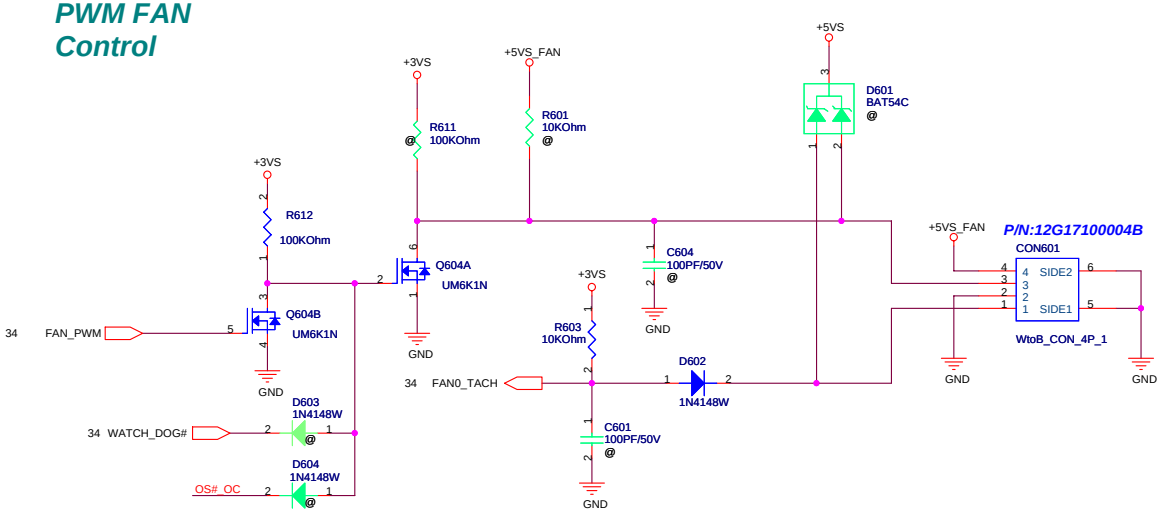
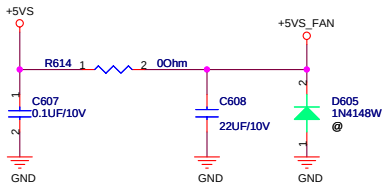
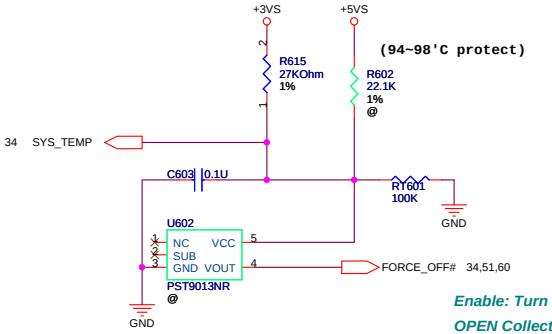
PWM FAN Control



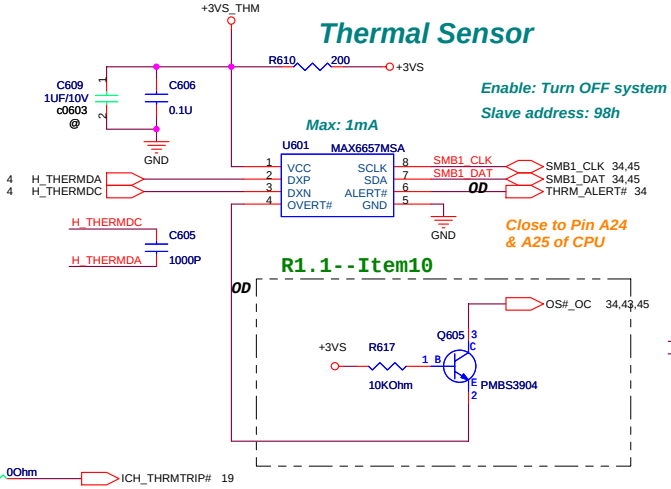


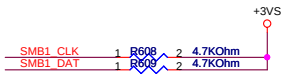
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

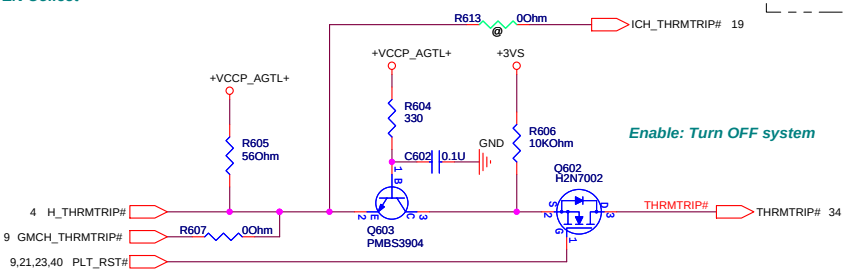


Enable: Turn OFF system
OPEN Collect

Thermal Sensor







Enable: Turn OFF system

<Variant Name>

ASUSTeK COMPUTER INC	Title : FAN_CTRL&Thermal	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
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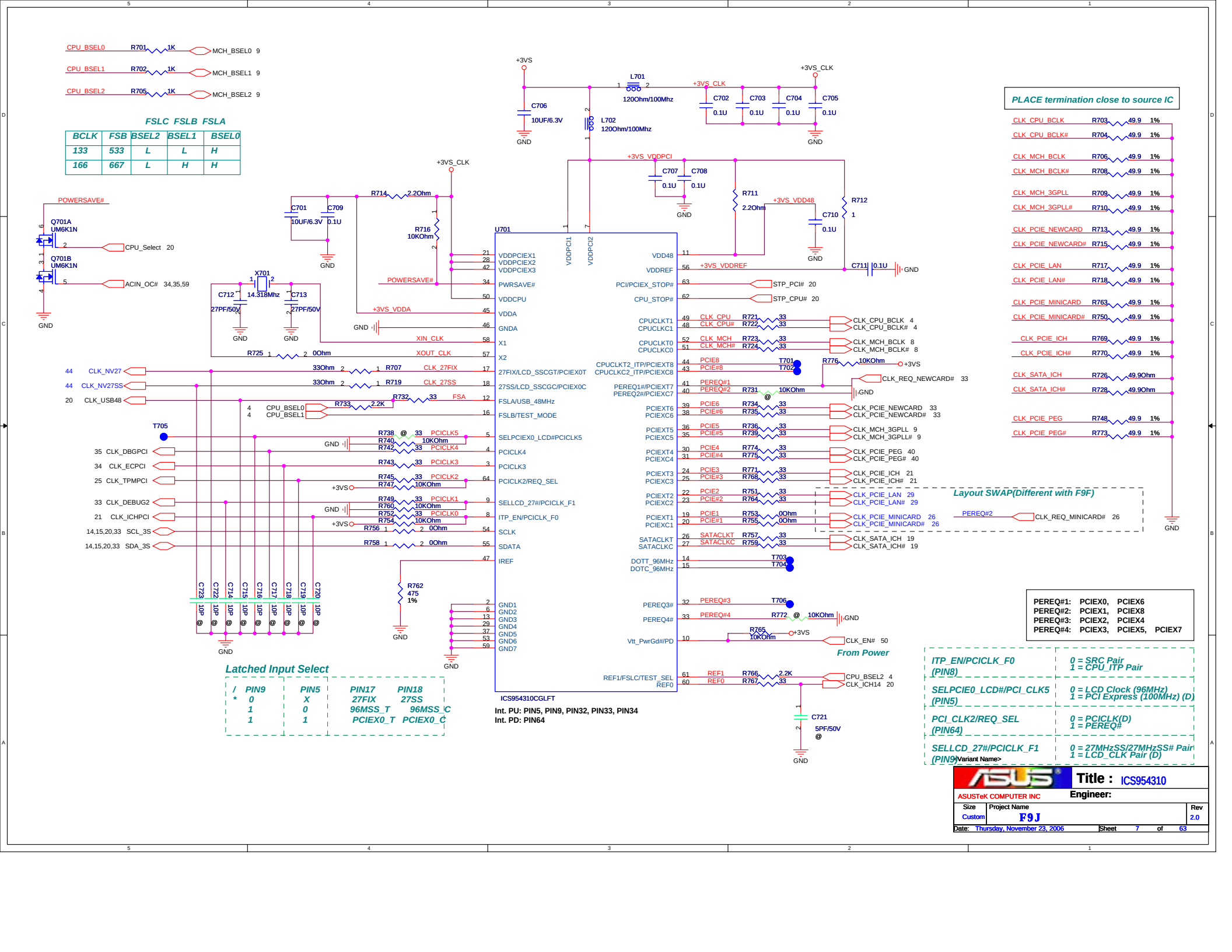
CPU_BSEL0 R701 1K MCH_BSEL0 9
CPU_BSEL1 R702 1K MCH_BSEL1 9
CPU_BSEL2 R705 1K MCH_BSEL2 9
FSLC FSLB FSLA
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
+3VS
+3VS_CLK
L701 120Ohm/100Mhz
L702 120Ohm/100Mhz
C706 10UF/6.3V
C702 C703 C704 C705 0.1U
C707 C708 0.1U
+3VS_VDDPCI
R711 2.2Ohm
+3VS_VDD48
R712 1
C710 0.1U
C711 0.1U
+3VS_VDDREF
PLACE termination close to source IC
CLK_CPU_BCLK R703 49.9 1%
CLK_CPU_BCLK# R704 49.9 1%
CLK_MCH_BCLK R706 49.9 1%
CLK_MCH_BCLK# R708 49.9 1%
CLK_MCH_3GPLL R709 49.9 1%
CLK_MCH_3GPLL# R710 49.9 1%
CLK_PCIE_NEWCARD R713 49.9 1%
CLK_PCIE_NEWCARD# R715 49.9 1%
CLK_PCIE_LAN R717 49.9 1%
CLK_PCIE_LAN# R718 49.9 1%
CLK_PCIE_MINICARD R763 49.9 1%
CLK_PCIE_MINICARD# R750 49.9 1%
CLK_PCIE_ICH R769 49.9 1%
CLK_PCIE_ICH# R770 49.9 1%
CLK_SATA_ICH R726 49.9Ohm
CLK_SATA_ICH# R728 49.9Ohm
CLK_PCIE_PEG R748 49.9 1%
CLK_PCIE_PEG# R773 49.9 1%
POWERSAVE#
Q701A UM6K1N
Q701B UM6K1N
CPU_Select 20
ACIN_OC# 34,35,59
C701 10UF/6.3V
C709 0.1U
R714 2.2Ohm
R716 10KOhm
X701 14.318Mhz
C712 27PF/50V
C713 27PF/50V
+3VS_VDDA
XIN_CLK
XOUT_CLK
R725 0Ohm
U701
VDDPCIEX1
VDDPCIEX2
VDDPCIEX3
PWRSAVE#
VDDCPU
VDDA
GNDA
X1
X2
27FIX/LCD_SSCGT/PCIEX0T
27SS/LCD_SSCGC/PCIEX0C
FSLA/USB_48MHz
FSLB/TEST_MODE
SELPCIEX0_LCD#PCICLK5
PCICLK4
PCICLK3
PCICLK2/REQ_SEL
SELLCD_27#/PCICLK_F1
ITP_EN/PCICLK_F0
SCLK
SDATA
IREF
GND1
GND2
GND3
GND4
GND5
GND6
GND7
VDD48
VDDREF
PCI/PCIEX_STOP#
CPU_STOP#
CPUCLKT1
CPUCLKC1
CPUCLKT0
CPUCLKC0
CPUCLKT2_ITP/PCIEXT8
CPUCLKC2_ITP/PCIEXC8
PEREQ1#/PCIEXT7
PEREQ2#/PCIEXC7
PCIEXT6
PCIEXC6
PCIEXT5
PCIEXC5
PCIEXT4
PCIEXC4
PCIEXT3
PCIEXC3
PCIEXT2
PCIEXC2
PCIEXT1
PCIEXC1
SATACLKT
SATACLKC
DOTT_96MHz
DOTC_96MHz
PEREQ3#
PEREQ4#
Vtt_PwrGd#/PD
REF1/FSLC/TEST_SEL
REF0
ICS954310CGLFT
Int. PU: PIN5, PIN9, PIN32, PIN33, PIN34
Int. PD: PIN64
STP_PCI# 20
STP_CPU# 20
CLK_CPU_BCLK 4
CLK_CPU_BCLK# 4
CLK_MCH_BCLK 8
CLK_MCH_BCLK# 8
CLK_REQ_NEWCARD# 33
CLK_PCIE_NEWCARD 33
CLK_PCIE_NEWCARD# 33
CLK_MCH_3GPLL 9
CLK_MCH_3GPLL# 9
CLK_PCIE_PEG 40
CLK_PCIE_PEG# 40
CLK_PCIE_ICH 21
CLK_PCIE_ICH# 21
CLK_PCIE_LAN 29
CLK_PCIE_LAN# 29
CLK_PCIE_MINICARD 26
CLK_PCIE_MINICARD# 26
CLK_SATA_ICH 19
CLK_SATA_ICH# 19
CLK_EN# 50
CPU_BSEL2 4
CLK_ICH14 20
Layout SWAP(Different with F9F)
PEREQ#2
CLK_REQ_MINICARD# 26
From Power
PEREQ#1: PCIEX0, PCIEX6
PEREQ#2: PCIEX1, PCIEX8
PEREQ#3: PCIEX2, PCIEX4
PEREQ#4: PCIEX3, PCIEX5, PCIEX7
Latched Input Select
/ PIN9 PIN5 PIN17 PIN18
* 0 X 27FIX 27SS
1 0 96MSS_T 96MSS_C
1 1 PCIEX0_T PCIEX0_C
ITP_EN/PCICLK_F0 (PIN8)
0 = SRC Pair
1 = CPU_ITP Pair
SELPCIE0_LCD#/PCI_CLK5 (PIN5)
0 = LCD Clock (96MHz)
1 = PCI Express (100MHz) (D)
PCI_CLK2/REQ_SEL (PIN64)
0 = PCICLK(D)
1 = PEREQ#
SELLCD_27#/PCICLK_F1 (PIN9)
0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair (D)
Variant Name>
ASUSTeK COMPUTER INC
Title : ICS954310
Engineer:
Size Custom
Project Name F9J
Rev 2.0
Date: Thursday, November 23, 2006
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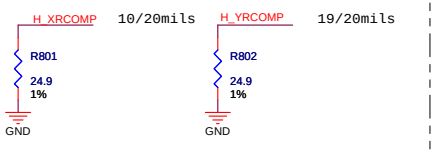
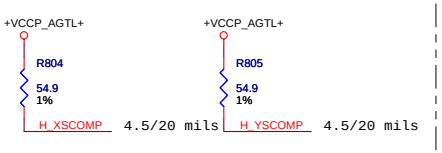
RCOMP

For Calibrating FSB I/O Buffer



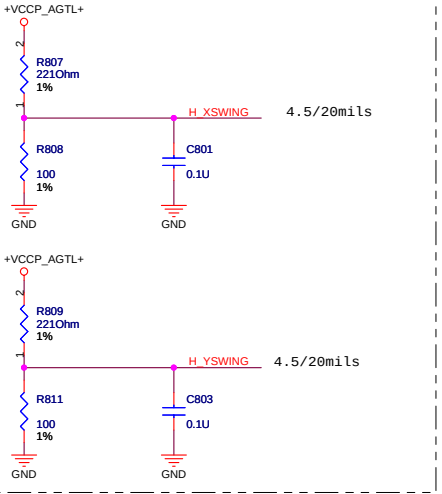
SCOMP

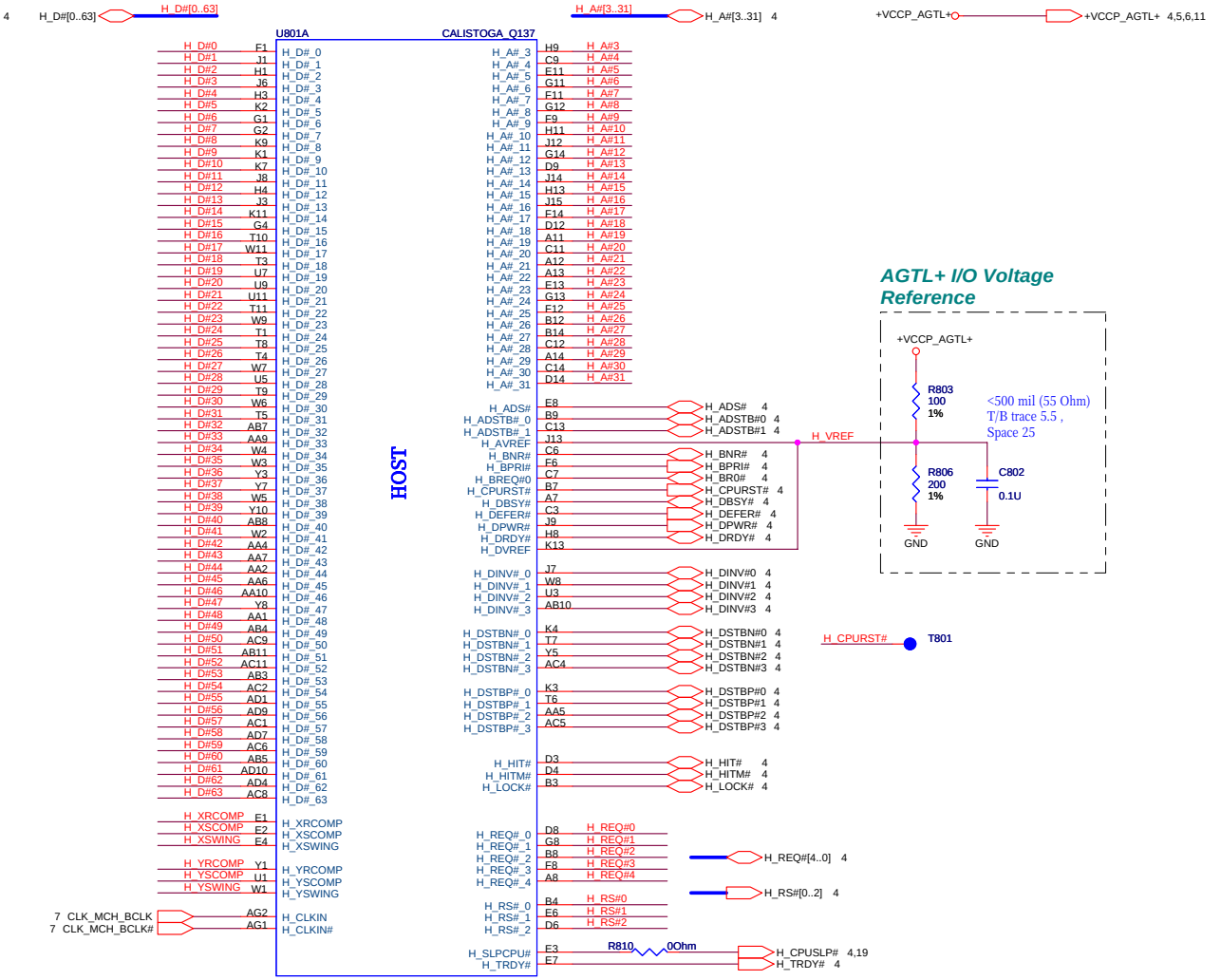
For Slew Rate Compensation on the FSB



Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP Circuit





AGTL+ I/O Voltage Reference

<variant_name>

ASUSTeK COMPUTER INC	Title : Calistoga--CPU	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
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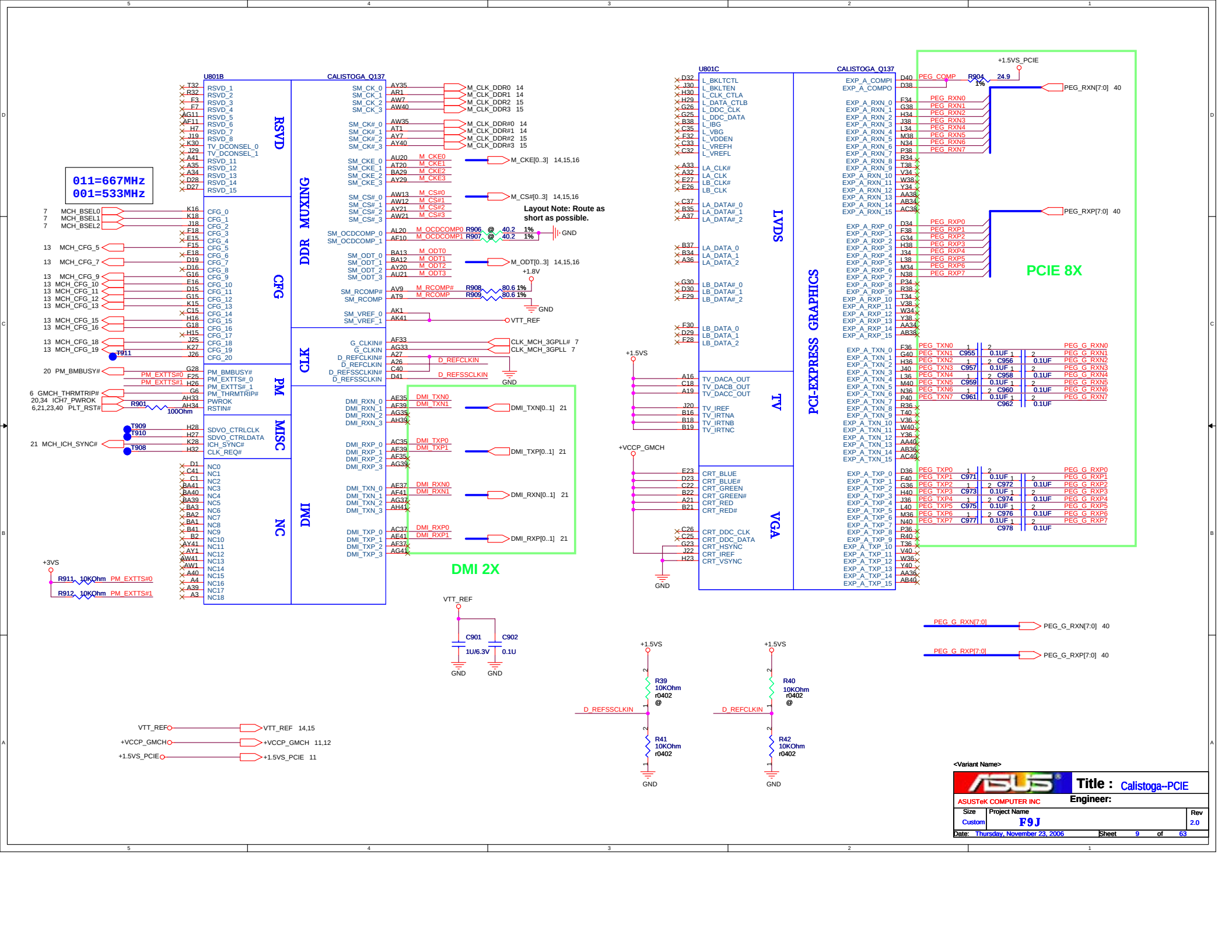
011=667MHz
001=533MHz
U801B
CALISTOGA_Q137
RSVD
CFG
PM
MISC
NC
DDR MUXING
CLK
DMI
U801C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
PCIE 8X
DMI 2X
Layout Note: Route as short as possible.
+1.5VS_PCIE
+1.8V
+1.5VS
+3VS
+VCCP_GMCH
VTT_REF
GND
PEG_RXN[7:0] 40
PEG_RXP[7:0] 40
PEG_G_RXN[7:0] 40
PEG_G_RXP[7:0] 40
D_REFSSCLKIN
D_REFCLKIN
R39 10KOhm r0402 @
R40 10KOhm r0402 @
R41 10KOhm r0402
R42 10KOhm r0402
C901 1U/6.3V
C902 0.1U
R901 100Ohm
R911 10KOhm PM_EXTTS#0
R912 10KOhm PM_EXTTS#1
R904 24.9 1%
VTT_REF 14,15
+VCCP_GMCH 11,12
+1.5VS_PCIE 11
<Variant Name>
Title : Calistoga--PCIE
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9J
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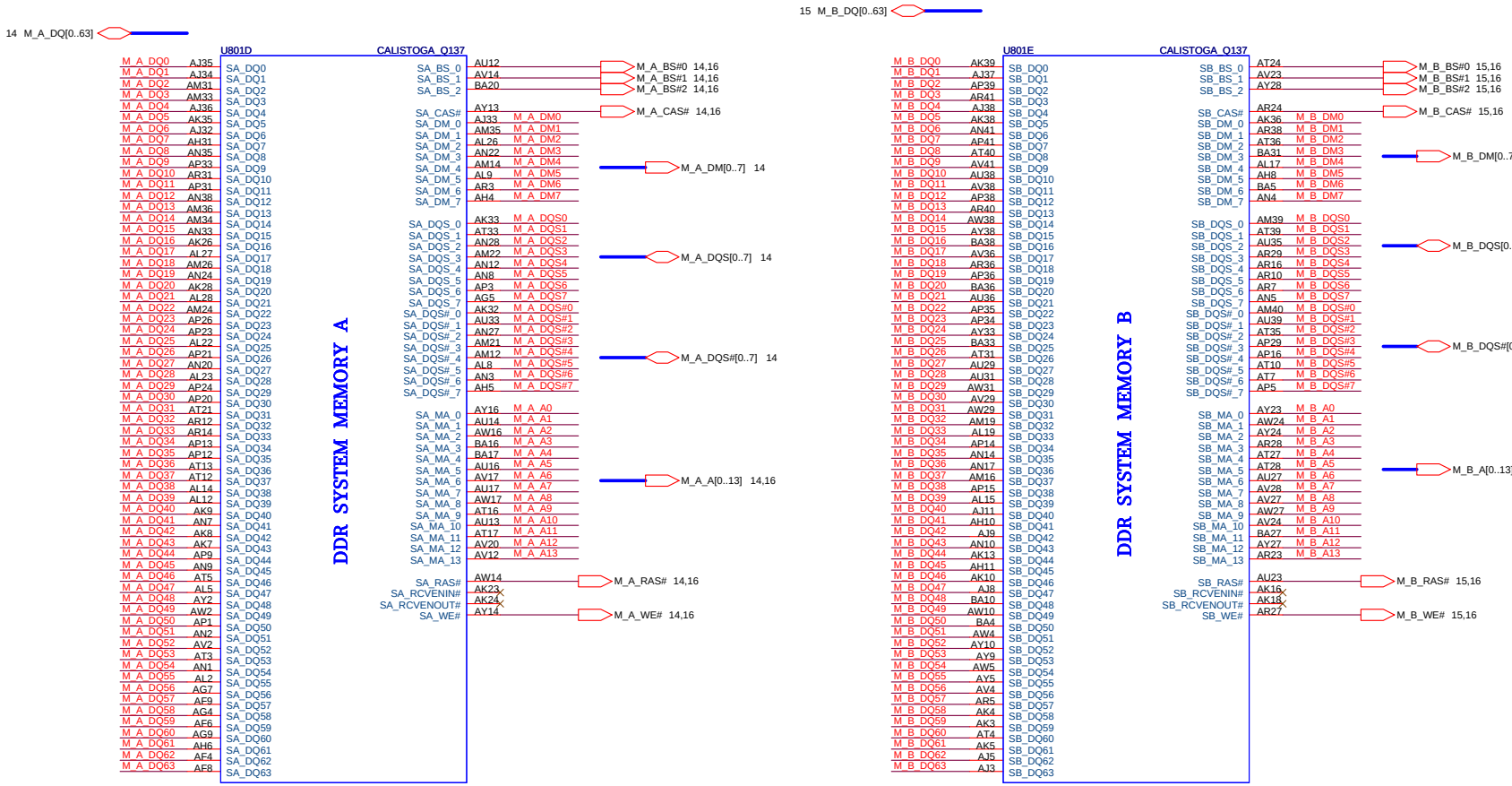
14 M_A_DQ[0..63]
U801D
CALISTOGA_Q137
DDR SYSTEM MEMORY A
SA_DQ0 SA_DQ1 SA_DQ2 SA_DQ3 SA_DQ4 SA_DQ5 SA_DQ6 SA_DQ7 SA_DQ8 SA_DQ9 SA_DQ10 SA_DQ11 SA_DQ12 SA_DQ13 SA_DQ14 SA_DQ15 SA_DQ16 SA_DQ17 SA_DQ18 SA_DQ19 SA_DQ20 SA_DQ21 SA_DQ22 SA_DQ23 SA_DQ24 SA_DQ25 SA_DQ26 SA_DQ27 SA_DQ28 SA_DQ29 SA_DQ30 SA_DQ31 SA_DQ32 SA_DQ33 SA_DQ34 SA_DQ35 SA_DQ36 SA_DQ37 SA_DQ38 SA_DQ39 SA_DQ40 SA_DQ41 SA_DQ42 SA_DQ43 SA_DQ44 SA_DQ45 SA_DQ46 SA_DQ47 SA_DQ48 SA_DQ49 SA_DQ50 SA_DQ51 SA_DQ52 SA_DQ53 SA_DQ54 SA_DQ55 SA_DQ56 SA_DQ57 SA_DQ58 SA_DQ59 SA_DQ60 SA_DQ61 SA_DQ62 SA_DQ63
M_A_DQ0 AJ35 M_A_DQ1 AJ34 M_A_DQ2 AM31 M_A_DQ3 AM33 M_A_DQ4 AJ36 M_A_DQ5 AK35 M_A_DQ6 AJ32 M_A_DQ7 AH31 M_A_DQ8 AN35 M_A_DQ9 AP33 M_A_DQ10 AR31 M_A_DQ11 AP31 M_A_DQ12 AN38 M_A_DQ13 AM36 M_A_DQ14 AM34 M_A_DQ15 AN33 M_A_DQ16 AK26 M_A_DQ17 AL27 M_A_DQ18 AM26 M_A_DQ19 AN24 M_A_DQ20 AK28 M_A_DQ21 AL28 M_A_DQ22 AM24 M_A_DQ23 AP26 M_A_DQ24 AP23 M_A_DQ25 AL22 M_A_DQ26 AP21 M_A_DQ27 AN20 M_A_DQ28 AL23 M_A_DQ29 AP24 M_A_DQ30 AP20 M_A_DQ31 AT21 M_A_DQ32 AR12 M_A_DQ33 AR14 M_A_DQ34 AP13 M_A_DQ35 AP12 M_A_DQ36 AT13 M_A_DQ37 AT12 M_A_DQ38 AL14 M_A_DQ39 AL12 M_A_DQ40 AK9 M_A_DQ41 AN7 M_A_DQ42 AK8 M_A_DQ43 AK7 M_A_DQ44 AP9 M_A_DQ45 AN9 M_A_DQ46 AT5 M_A_DQ47 AL5 M_A_DQ48 AY2 M_A_DQ49 AW2 M_A_DQ50 AP1 M_A_DQ51 AN2 M_A_DQ52 AV2 M_A_DQ53 AT3 M_A_DQ54 AN1 M_A_DQ55 AL2 M_A_DQ56 AG7 M_A_DQ57 AF9 M_A_DQ58 AG4 M_A_DQ59 AF6 M_A_DQ60 AG9 M_A_DQ61 AH6 M_A_DQ62 AF4 M_A_DQ63 AF8
SA_BS_0 SA_BS_1 SA_BS_2 SA_CAS# SA_DM_0 SA_DM_1 SA_DM_2 SA_DM_3 SA_DM_4 SA_DM_5 SA_DM_6 SA_DM_7 SA_DQS_0 SA_DQS_1 SA_DQS_2 SA_DQS_3 SA_DQS_4 SA_DQS_5 SA_DQS_6 SA_DQS_7 SA_DQS#_0 SA_DQS#_1 SA_DQS#_2 SA_DQS#_3 SA_DQS#_4 SA_DQS#_5 SA_DQS#_6 SA_DQS#_7 SA_MA_0 SA_MA_1 SA_MA_2 SA_MA_3 SA_MA_4 SA_MA_5 SA_MA_6 SA_MA_7 SA_MA_8 SA_MA_9 SA_MA_10 SA_MA_11 SA_MA_12 SA_MA_13 SA_RAS# SA_RCVENIN# SA_RCVENOUT# SA_WE#
AU12 AV14 BA20 AY13 AJ33 AM35 AL26 AN22 AM14 AL9 AR3 AH4 AK33 AT33 AN28 AM22 AN12 AN8 AP3 AG5 AK32 AU33 AN27 AM21 AM12 AL8 AN3 AH5 AY16 AU14 AW16 BA16 BA17 AU16 AV17 AU17 AW17 AT16 AU13 AT17 AV20 AV12 AW14 AK23 AK24 AY14
M_A_BS#0 14,16
M_A_BS#1 14,16
M_A_BS#2 14,16
M_A_CAS# 14,16
M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7
M_A_DM[0..7] 14
M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7
M_A_DQS[0..7] 14
M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7
M_A_DQS#[0..7] 14
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13
M_A_A[0..13] 14,16
M_A_RAS# 14,16
M_A_WE# 14,16
15 M_B_DQ[0..63]
U801E
CALISTOGA_Q137
DDR SYSTEM MEMORY B
SB_DQ0 SB_DQ1 SB_DQ2 SB_DQ3 SB_DQ4 SB_DQ5 SB_DQ6 SB_DQ7 SB_DQ8 SB_DQ9 SB_DQ10 SB_DQ11 SB_DQ12 SB_DQ13 SB_DQ14 SB_DQ15 SB_DQ16 SB_DQ17 SB_DQ18 SB_DQ19 SB_DQ20 SB_DQ21 SB_DQ22 SB_DQ23 SB_DQ24 SB_DQ25 SB_DQ26 SB_DQ27 SB_DQ28 SB_DQ29 SB_DQ30 SB_DQ31 SB_DQ32 SB_DQ33 SB_DQ34 SB_DQ35 SB_DQ36 SB_DQ37 SB_DQ38 SB_DQ39 SB_DQ40 SB_DQ41 SB_DQ42 SB_DQ43 SB_DQ44 SB_DQ45 SB_DQ46 SB_DQ47 SB_DQ48 SB_DQ49 SB_DQ50 SB_DQ51 SB_DQ52 SB_DQ53 SB_DQ54 SB_DQ55 SB_DQ56 SB_DQ57 SB_DQ58 SB_DQ59 SB_DQ60 SB_DQ61 SB_DQ62 SB_DQ63
M_B_DQ0 AK39 M_B_DQ1 AJ37 M_B_DQ2 AP39 M_B_DQ3 AR41 M_B_DQ4 AJ38 M_B_DQ5 AK38 M_B_DQ6 AN41 M_B_DQ7 AP41 M_B_DQ8 AT40 M_B_DQ9 AV41 M_B_DQ10 AU38 M_B_DQ11 AV38 M_B_DQ12 AP38 M_B_DQ13 AR40 M_B_DQ14 AW38 M_B_DQ15 AY38 M_B_DQ16 BA38 M_B_DQ17 AV36 M_B_DQ18 AR36 M_B_DQ19 AP36 M_B_DQ20 BA36 M_B_DQ21 AU36 M_B_DQ22 AP35 M_B_DQ23 AP34 M_B_DQ24 AY33 M_B_DQ25 BA33 M_B_DQ26 AT31 M_B_DQ27 AU29 M_B_DQ28 AU31 M_B_DQ29 AW31 M_B_DQ30 AV29 M_B_DQ31 AW29 M_B_DQ32 AM19 M_B_DQ33 AL19 M_B_DQ34 AP14 M_B_DQ35 AN14 M_B_DQ36 AN17 M_B_DQ37 AM16 M_B_DQ38 AP15 M_B_DQ39 AL15 M_B_DQ40 AJ11 M_B_DQ41 AH10 M_B_DQ42 AJ9 M_B_DQ43 AN10 M_B_DQ44 AK13 M_B_DQ45 AH11 M_B_DQ46 AK10 M_B_DQ47 AJ8 M_B_DQ48 BA10 M_B_DQ49 AW10 M_B_DQ50 BA4 M_B_DQ51 AW4 M_B_DQ52 AY10 M_B_DQ53 AY9 M_B_DQ54 AW5 M_B_DQ55 AY5 M_B_DQ56 AV4 M_B_DQ57 AR5 M_B_DQ58 AK4 M_B_DQ59 AK3 M_B_DQ60 AT4 M_B_DQ61 AK5 M_B_DQ62 AJ5 M_B_DQ63 AJ3
SB_BS_0 SB_BS_1 SB_BS_2 SB_CAS# SB_DM_0 SB_DM_1 SB_DM_2 SB_DM_3 SB_DM_4 SB_DM_5 SB_DM_6 SB_DM_7 SB_DQS_0 SB_DQS_1 SB_DQS_2 SB_DQS_3 SB_DQS_4 SB_DQS_5 SB_DQS_6 SB_DQS_7 SB_DQS#_0 SB_DQS#_1 SB_DQS#_2 SB_DQS#_3 SB_DQS#_4 SB_DQS#_5 SB_DQS#_6 SB_DQS#_7 SB_MA_0 SB_MA_1 SB_MA_2 SB_MA_3 SB_MA_4 SB_MA_5 SB_MA_6 SB_MA_7 SB_MA_8 SB_MA_9 SB_MA_10 SB_MA_11 SB_MA_12 SB_MA_13 SB_RAS# SB_RCVENIN# SB_RCVENOUT# SB_WE#
AT24 AV23 AY28 AR24 AK36 AR38 AT36 BA31 AL17 AH8 BA5 AN4 AM39 AT39 AU35 AR29 AR16 AR10 AR7 AN5 AM40 AU39 AT35 AP29 AP16 AT10 AT7 AP5 AY23 AW24 AY24 AR28 AT27 AT28 AU27 AV28 AV27 AW27 AV24 BA27 AY27 AR23 AU23 AK16 AK18 AR27
M_B_BS#0 15,16
M_B_BS#1 15,16
M_B_BS#2 15,16
M_B_CAS# 15,16
M_B_DM0 M_B_DM1 M_B_DM2 M_B_DM3 M_B_DM4 M_B_DM5 M_B_DM6 M_B_DM7
M_B_DM[0..7] 15
M_B_DQS0 M_B_DQS1 M_B_DQS2 M_B_DQS3 M_B_DQS4 M_B_DQS5 M_B_DQS6 M_B_DQS7
M_B_DQS[0..7] 15
M_B_DQS#0 M_B_DQS#1 M_B_DQS#2 M_B_DQS#3 M_B_DQS#4 M_B_DQS#5 M_B_DQS#6 M_B_DQS#7
M_B_DQS#[0..7] 15
M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13
M_B_A[0..13] 15,16
M_B_RAS# 15,16
M_B_WE# 15,16
<Variant Name>
Title : Calistoga--DDR2
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9J
Rev 2.0
Date: Thursday, November 23, 2006
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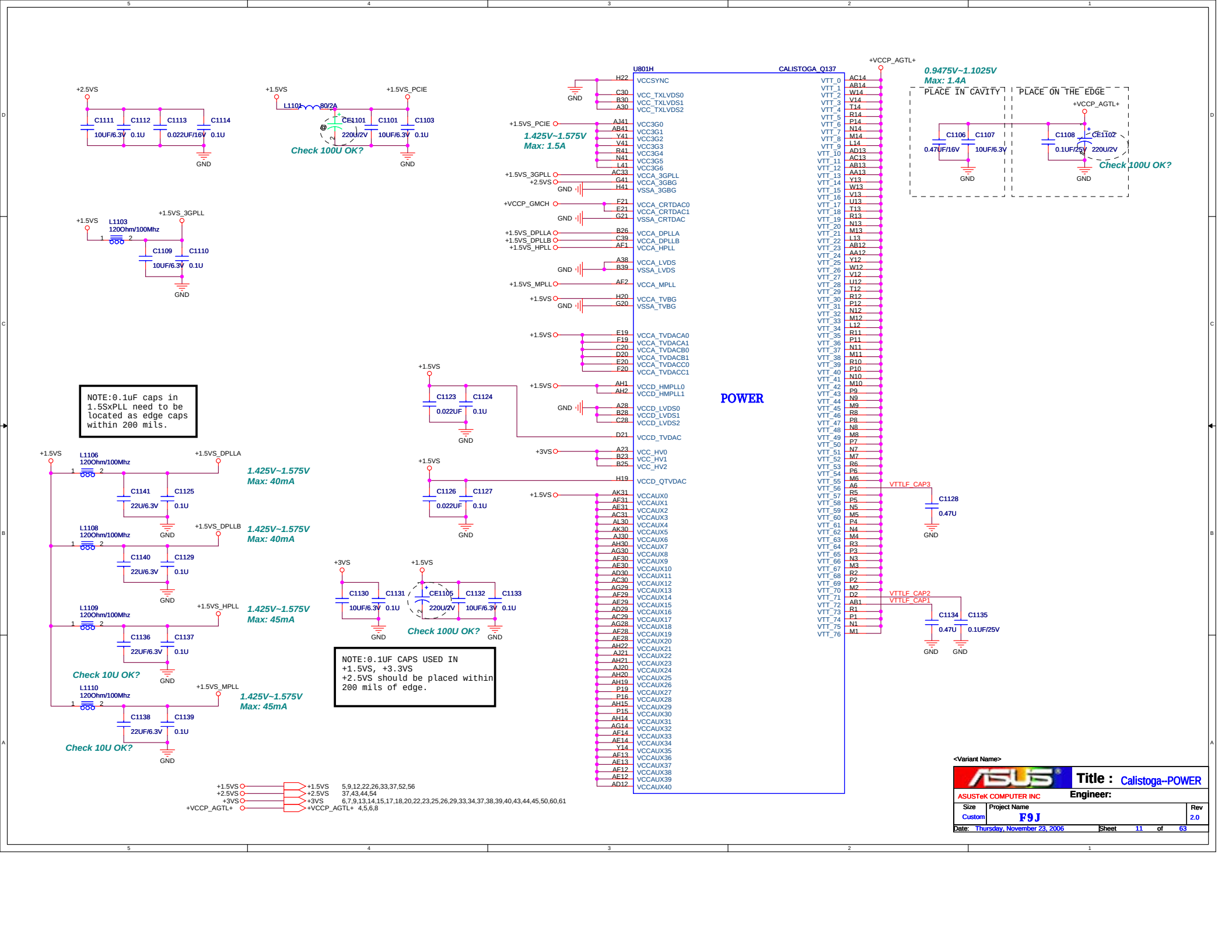
+2.5VS
C1111 10UF/6.3V
C1112 0.1U
C1113 0.022UF/16V
C1114 0.1U
GND
+1.5VS
L1101 80/2A
+1.5VS_PCIE
CE1101 220U/2V
C1101 10UF/6.3V
C1103 0.1U
Check 100U OK?
+1.5VS_3GPLL
L1103 120Ohm/100Mhz
C1109 10UF/6.3V
C1110 0.1U
NOTE:0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.
+1.5VS_DPLLA
L1106 120Ohm/100Mhz
C1141 22U/6.3V
C1125 0.1U
1.425V~1.575V
Max: 40mA
+1.5VS_DPLLB
L1108 120Ohm/100Mhz
C1140 22U/6.3V
C1129 0.1U
+1.5VS_HPLL
L1109 120Ohm/100Mhz
C1136 22U/6.3V
C1137 0.1U
Max: 45mA
Check 10U OK?
+1.5VS_MPLL
L1110 120Ohm/100Mhz
C1138 22U/6.3V
C1139 0.1U
C1123 0.022UF
C1124 0.1U
C1126 0.022UF
C1127 0.1U
+3VS
C1130 10UF/6.3V
C1131 0.1U
CE1105 220U/2V
C1132 10UF/6.3V
C1133 0.1U
NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.
U801H
CALISTOGA_Q137
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
POWER
+VCCP_AGTL+
0.9475V~1.1025V
Max: 1.4A
PLACE IN CAVITY
PLACE ON THE EDGE
C1106 0.47UF/16V
C1107 10UF/6.3V
C1108 0.1UF/25V
CE1102 220U/2V
Check 100U OK?
VTTLF_CAP3
C1128 0.47U
VTTLF_CAP2
VTTLF_CAP1
C1134 0.47U
C1135 0.1UF/25V
+1.5VS 5,9,12,22,26,33,37,52,56
+2.5VS 37,43,44,54
+3VS 6,7,9,13,14,15,17,18,20,22,23,25,26,29,33,34,37,38,39,40,43,44,45,50,60,61
+VCCP_AGTL+ 4,5,6,8
<Variant Name>
Title : Calistoga--POWER
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9J
Rev 2.0
Date: Thursday, November 23, 2006
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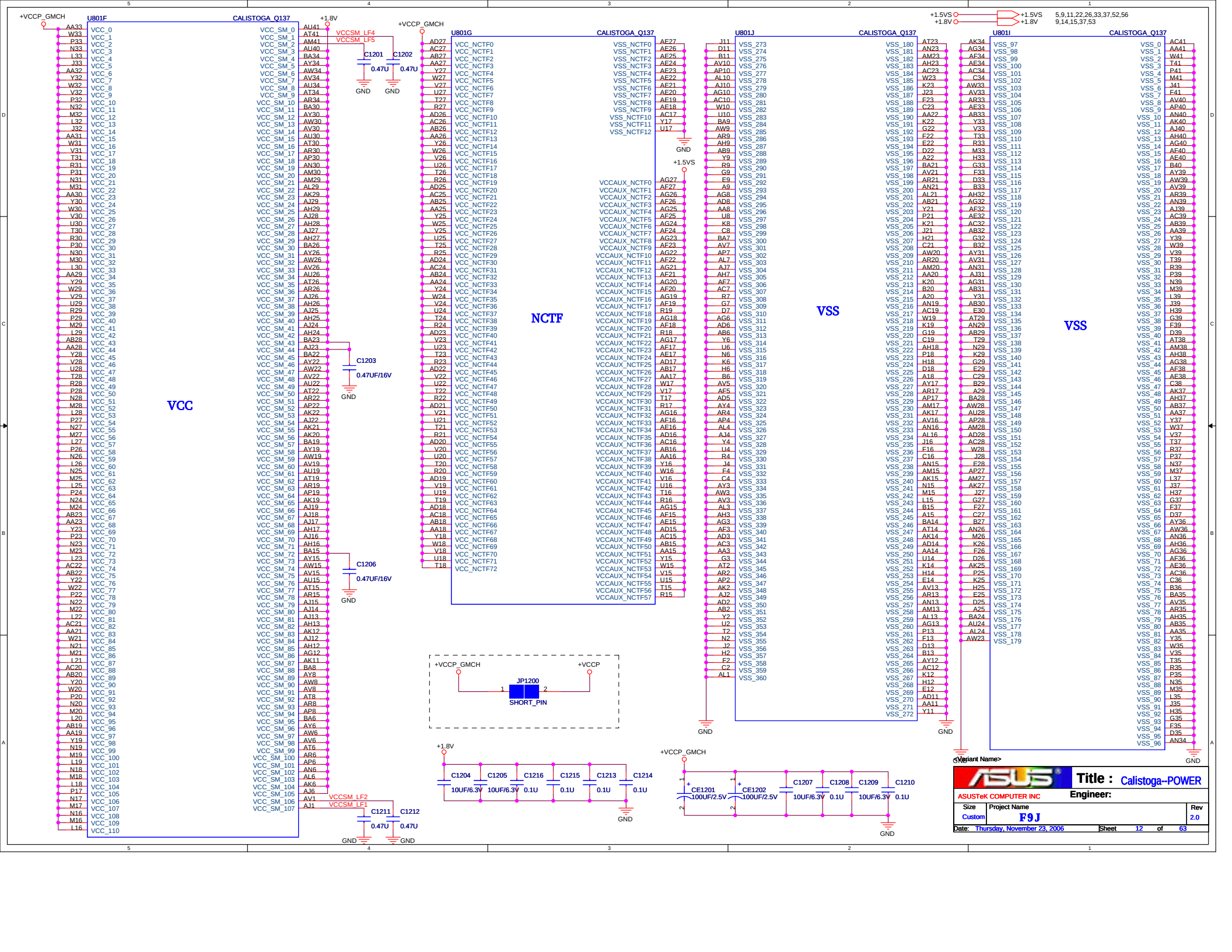
+VCCP_GMCH
U801F
CALISTOGA_Q137
VCC
+1.8V
VCCSM_LF4
VCCSM_LF5
C1201
C1202
0.47U
GND
U801G
NCTF
VSS_NCTF0
VSS_NCTF1
VSS_NCTF2
VSS_NCTF3
VSS_NCTF4
VSS_NCTF5
VSS_NCTF6
VSS_NCTF7
VSS_NCTF8
VSS_NCTF9
VSS_NCTF10
VSS_NCTF11
VSS_NCTF12
+1.5VS
VCCAUX_NCTF0
VCCAUX_NCTF1
VCCAUX_NCTF2
VCCAUX_NCTF3
VCCAUX_NCTF4
VCCAUX_NCTF5
VCCAUX_NCTF6
VCCAUX_NCTF7
VCCAUX_NCTF8
VCCAUX_NCTF9
VCCAUX_NCTF10
VCCAUX_NCTF11
VCCAUX_NCTF12
VCCAUX_NCTF13
VCCAUX_NCTF14
VCCAUX_NCTF15
VCCAUX_NCTF16
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VCCAUX_NCTF18
VCCAUX_NCTF19
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VCCAUX_NCTF21
VCCAUX_NCTF22
VCCAUX_NCTF23
VCCAUX_NCTF24
VCCAUX_NCTF25
VCCAUX_NCTF26
VCCAUX_NCTF27
VCCAUX_NCTF28
VCCAUX_NCTF29
VCCAUX_NCTF30
VCCAUX_NCTF31
VCCAUX_NCTF32
VCCAUX_NCTF33
VCCAUX_NCTF34
VCCAUX_NCTF35
VCCAUX_NCTF36
VCCAUX_NCTF37
VCCAUX_NCTF38
VCCAUX_NCTF39
VCCAUX_NCTF40
VCCAUX_NCTF41
VCCAUX_NCTF42
VCCAUX_NCTF43
VCCAUX_NCTF44
VCCAUX_NCTF45
VCCAUX_NCTF46
VCCAUX_NCTF47
VCCAUX_NCTF48
VCCAUX_NCTF49
VCCAUX_NCTF50
VCCAUX_NCTF51
VCCAUX_NCTF52
VCCAUX_NCTF53
VCCAUX_NCTF54
VCCAUX_NCTF55
VCCAUX_NCTF56
VCCAUX_NCTF57
U801J
VSS
+1.5VS
+1.8V
5,9,11,22,26,33,37,52,56
9,14,15,37,53
U801I
C1203
C1206
C1211
C1212
0.47UF/16V
VCCSM_LF2
VCCSM_LF1
JP1200
SHORT_PIN
+VCCP
C1204
C1205
C1216
C1215
C1213
C1214
10UF/6.3V
0.1U
CE1201
CE1202
100UF/2.5V
C1207
C1208
C1209
C1210
<Variant Name>
Title : Calistoga--POWER
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
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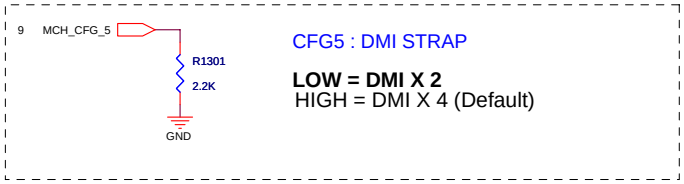
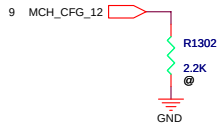
+3VS +3VS 6,7,9,11,14,15,17,18,20,22,23,25,26,29,33,34,37,38,39,40,43,44,45,50,60,61



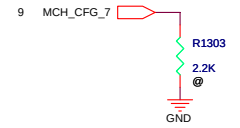
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



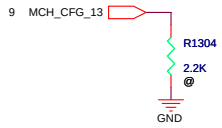
CFG[13:12] : GMCH TEST MODE SELECT

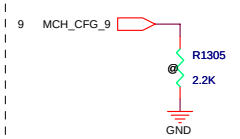
00 = Partial CLK gating disable
01 = XOR Mode Enable
10 = ALL Z Mode Enable
11 = NORMAL OPERATION (Default)



CFG7 : CPU STRAP

LOW = RESERVED
HIGH = Mobile Yonah CPU (Default)



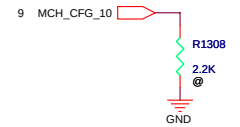


CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)

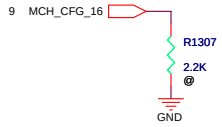
CFG15 : ICH RESET Disable

LOW = ICH RESET Disabled
HIGH = Normal Operation (Default)



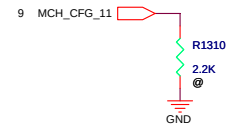
CFG10 : HOST PLL VCO SELECT

LOW = RESERVED
HIGH = MOBILITY (Default)



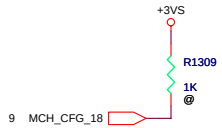
CFG16 : FSB Dynamic ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG11 : PSB 4x CLK ENABLE

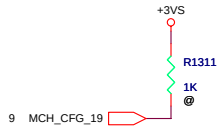
LOW = 4X ENABLED
HIGH = 8X ENABLED (Default)



CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
HIGH = 1.5V

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.



CFG19 : DMI LANE REVERSAL

LOW = NORMAL (Default)
HIGH = LANES REVERSED

<Variant Name>

Title : Calistoga--Strap

ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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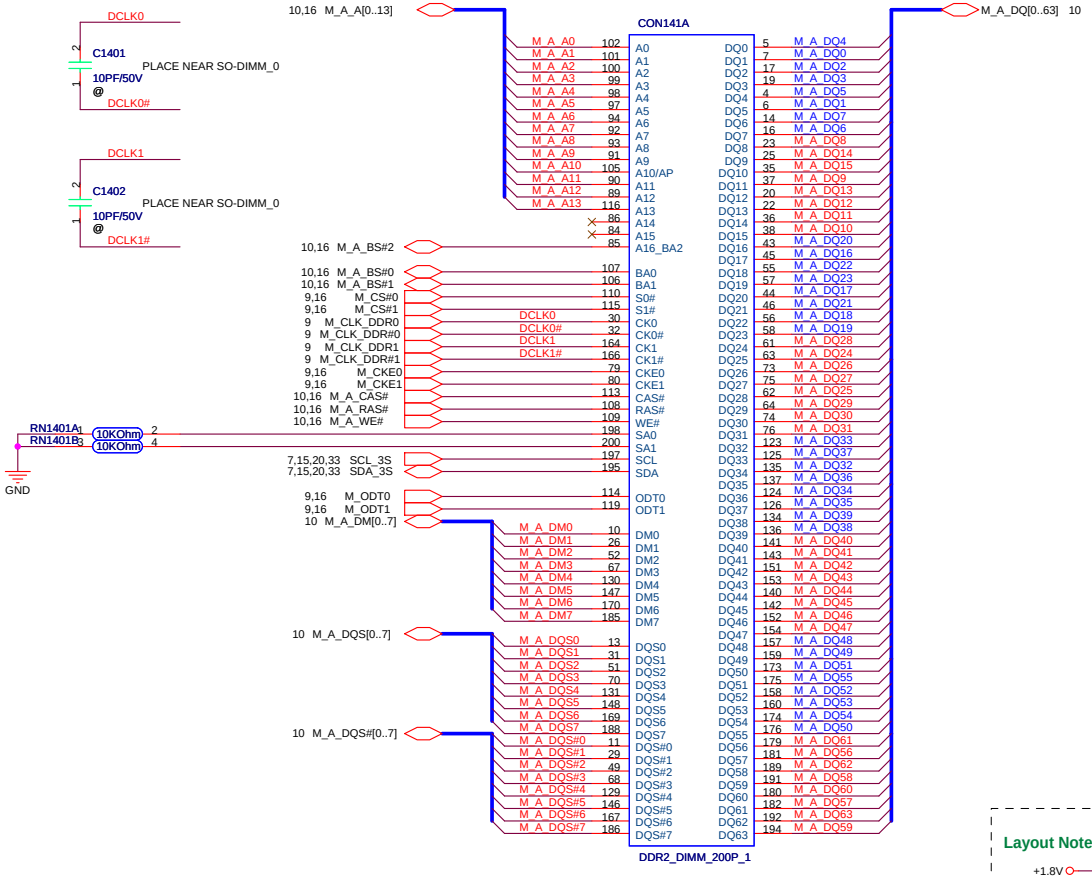
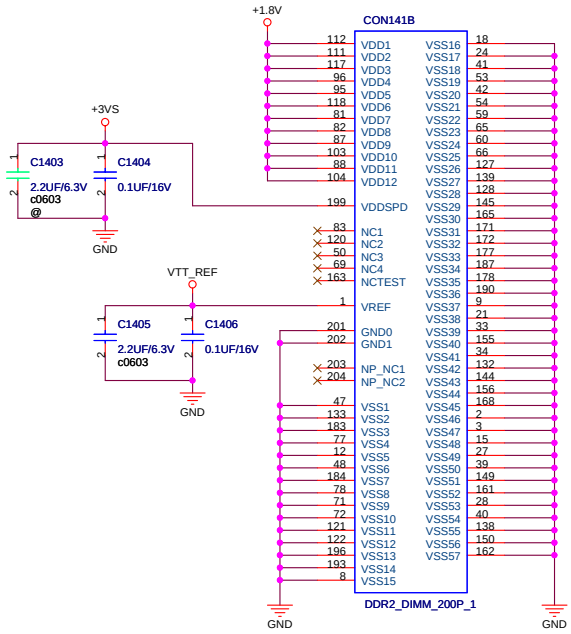
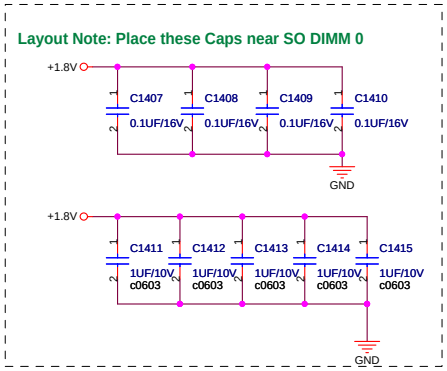
SMBus Slave Address:A0H



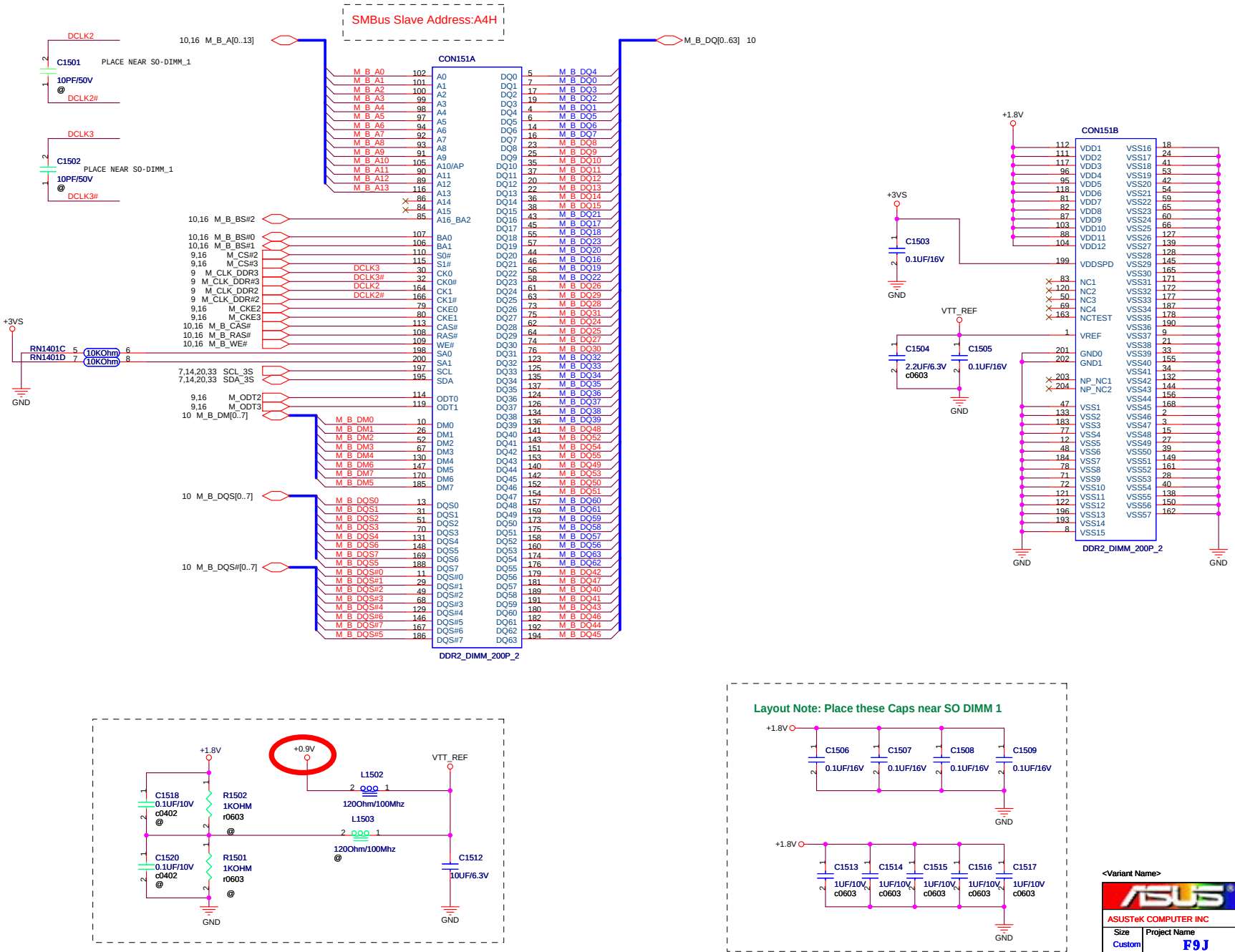
Hight: 4.0 mm

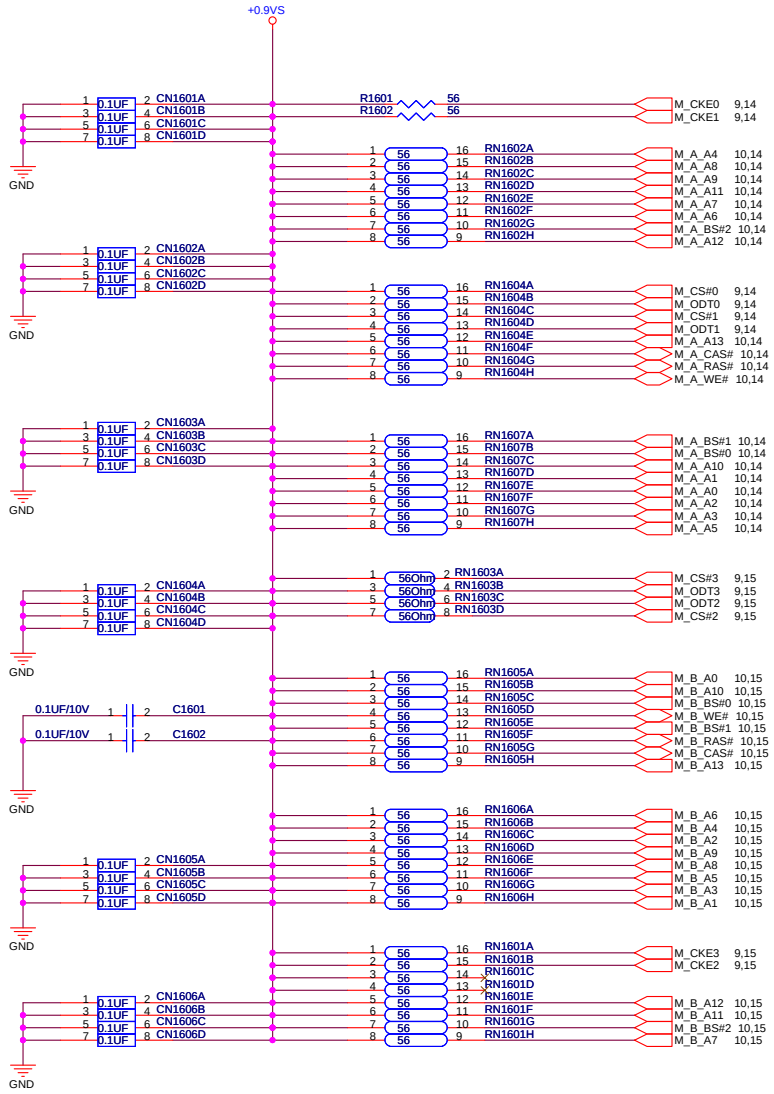




<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM_0	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Thursday, November 23, 2006	Sheet 14 of 63	


SMBus Slave Address:A4H
CON151A
DDR2_DIMM_200P_2
CON151B
DDR2_DIMM_200P_2
Layout Note: Place these Caps near SO DIMM 1
Title : DDR2 SO-DIMM_1
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
F9J
Rev
2.0
Date: Thursday, November 23, 2006
Sheet 15 of 63



Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR2 TERMINATION

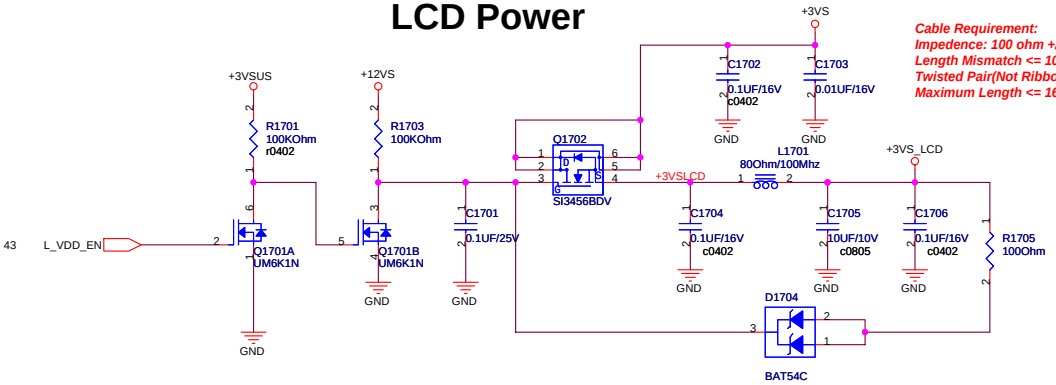
Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: Thursday, November 23, 2006 Sheet 16 of 63

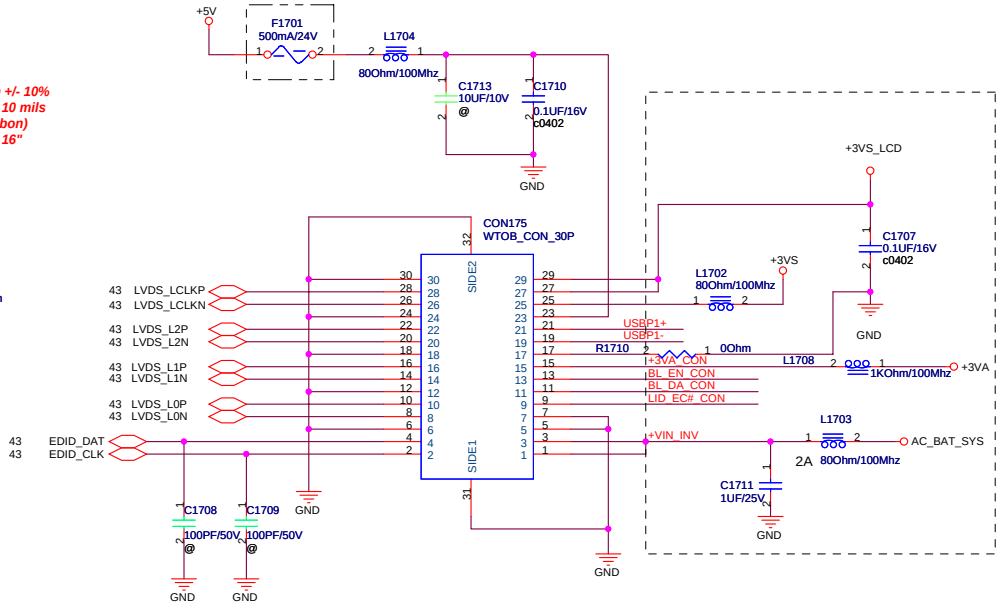
LCD Backlight Control

LCD Power



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

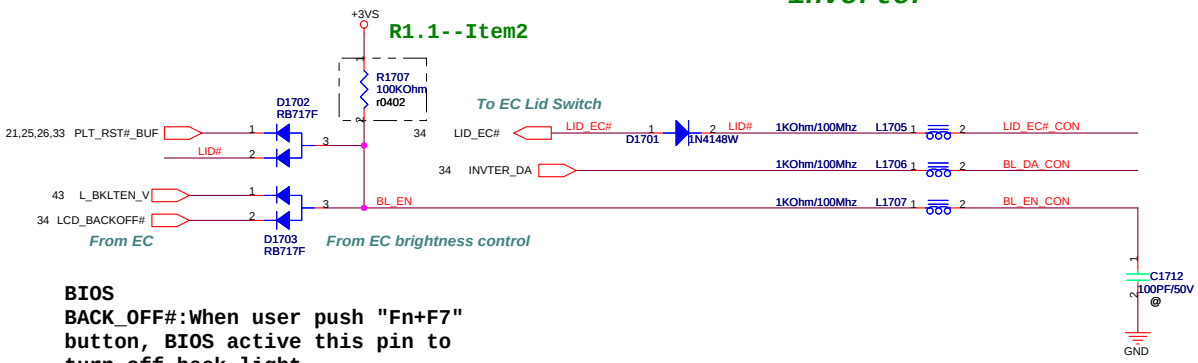
R2.0--Item12



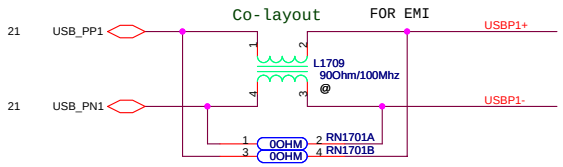
Use F3JA's inverter

CCD connecter

R1.1--Item2

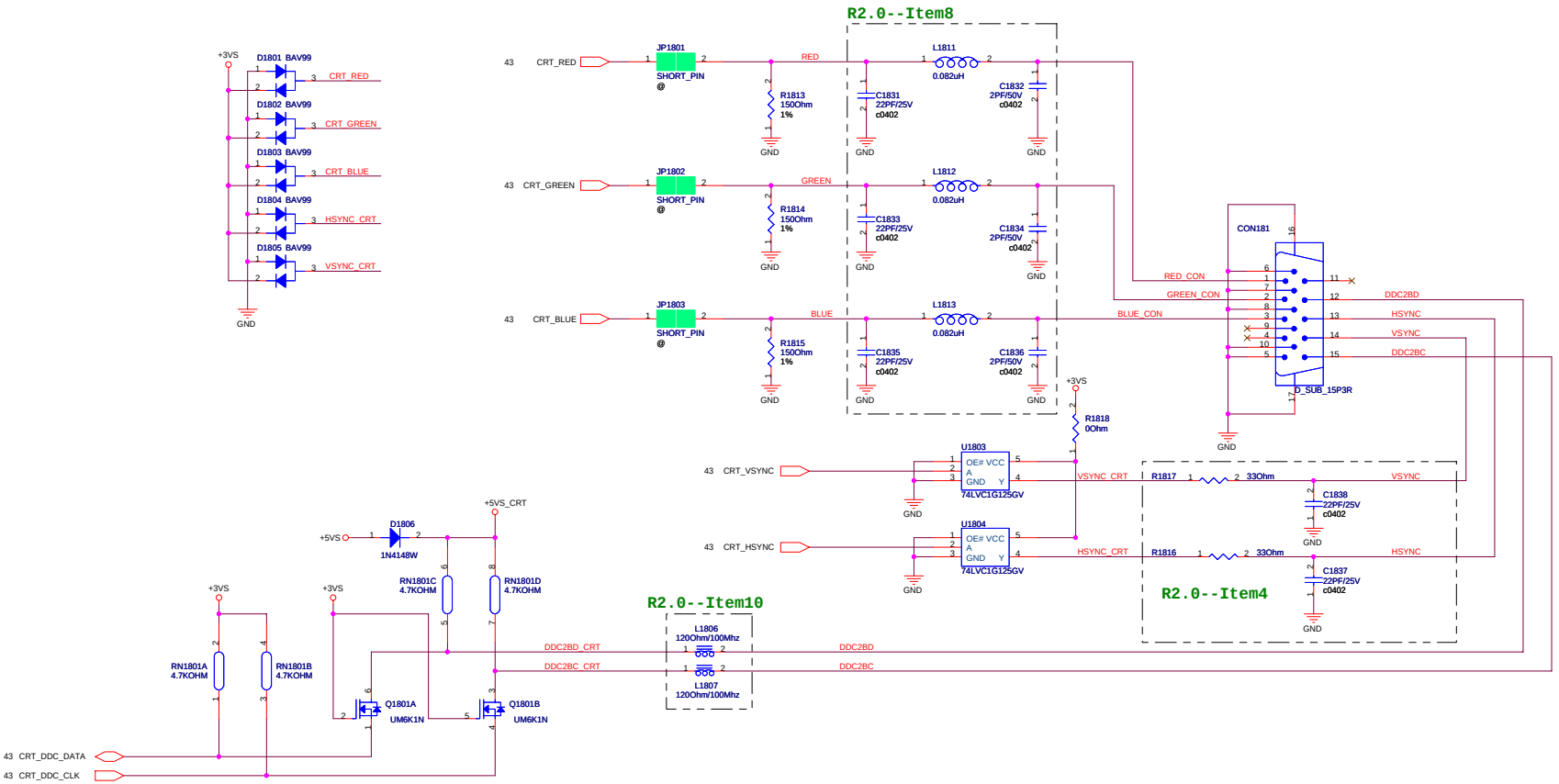


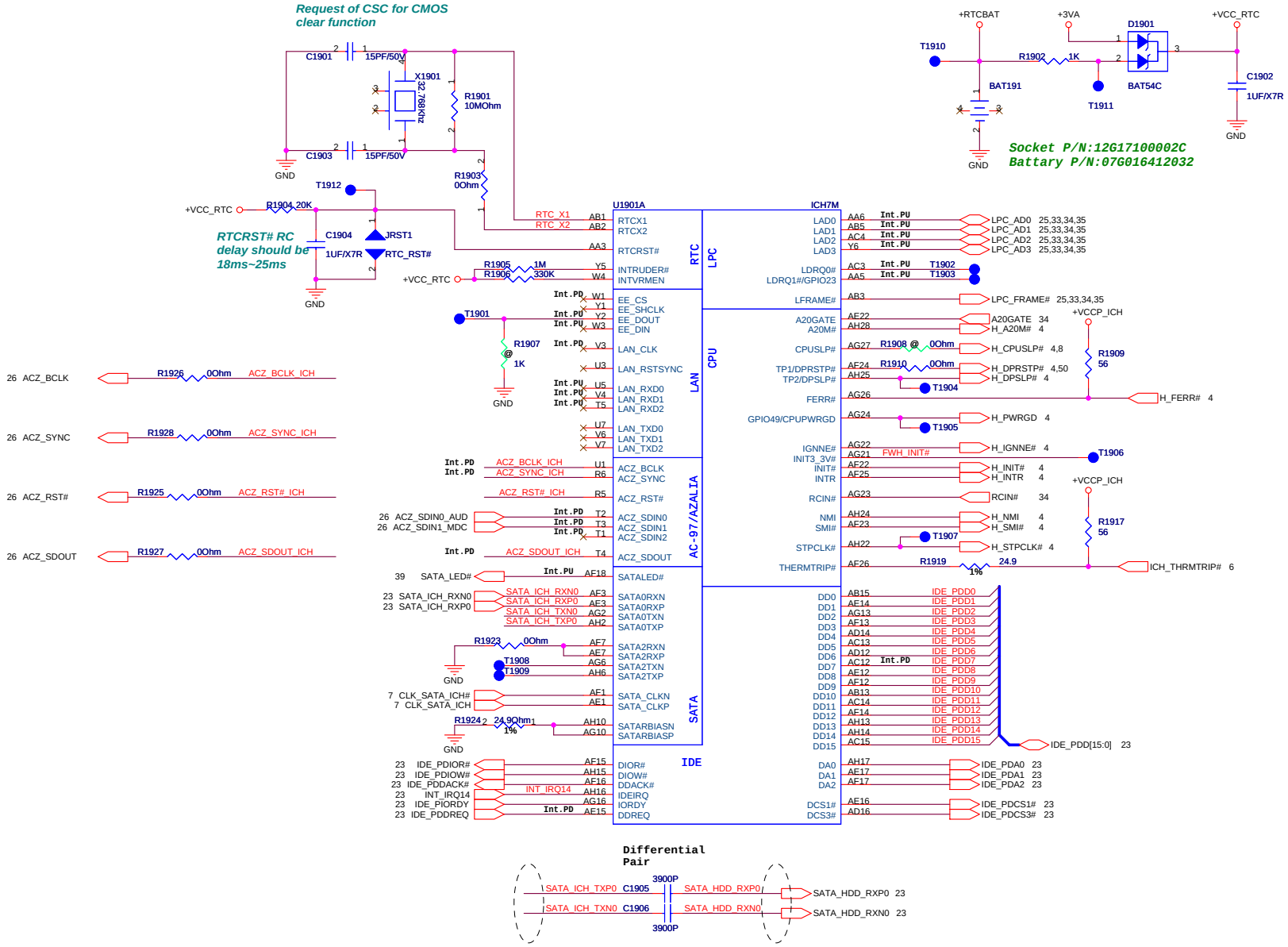
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Thursday, November 23, 2006	Sheet 17 of 63	


R2.0--Item8
D1801 BAV99
D1802 BAV99
D1803 BAV99
D1804 BAV99
D1805 BAV99
CRT_RED
CRT_GREEN
CRT_BLUE
HSYNC_CRT
VSYNC_CRT
JP1801
JP1802
JP1803
SHORT_PIN
R1813 150Ohm 1%
R1814 150Ohm 1%
R1815 150Ohm 1%
L1811 0.082uH
L1812 0.082uH
L1813 0.082uH
C1831 22PF/25V c0402
C1832 2PF/50V c0402
C1833 22PF/25V c0402
C1834 2PF/50V c0402
C1835 22PF/25V c0402
C1836 2PF/50V c0402
CON181
D_SUB_15P3R
R1818 0Ohm
U1803
U1804
74LVC1G125GV
R1817 33Ohm
R1816 33Ohm
C1838 22PF/25V c0402
C1837 22PF/25V c0402
R2.0--Item4
D1806 1N4148W
RN1801C 4.7KOHM
RN1801D 4.7KOHM
RN1801A 4.7KOHM
RN1801B 4.7KOHM
Q1801A UM6K1N
Q1801B UM6K1N
R2.0--Item10
L1806 120Ohm/100Mhz
L1807 120Ohm/100Mhz
CRT_DDC_DATA
CRT_DDC_CLK
DDC2BD_CRT
DDC2BC_CRT
DDC2BD
DDC2BC
RED_CON
GREEN_CON
BLUE_CON
VSYNC_CRT
HSYNC_CRT
R2.0--Item3
C4702 22PF/50V
C4703 22PF/50V
C4704 22PF/50V
L1815 1.8UH
L1814 1.8UH
L1816 1.8UH
R1821 150Ohm 1%
R1819 150Ohm 1%
R1820 150Ohm 1%
C1840 270PF/50V
C1842 270PF/50V
C1843 270PF/50V
C1839 330PF/50V
C1841 330PF/50V
C1844 330PF/50V
R1.1--Item1
TV
P/N:12G14101107K
CON182 MINI_DIN_7P
D1809 BAV99
D1808 BAV99
D1807 BAV99
TV_C
TV_Y
TV_CVBS
C_CON
Y_CON
CVBS_CON
<Variant Name>
Title : CRT & TV OUT
ASUSTeK COMPUTER INC
Engineer:
Size C
Project Name F9J
Rev 2.0
Date: Thursday, November 23, 2006
Sheet 18 of 63



<Variant Name>

ASUSTeK COMPUTER INC

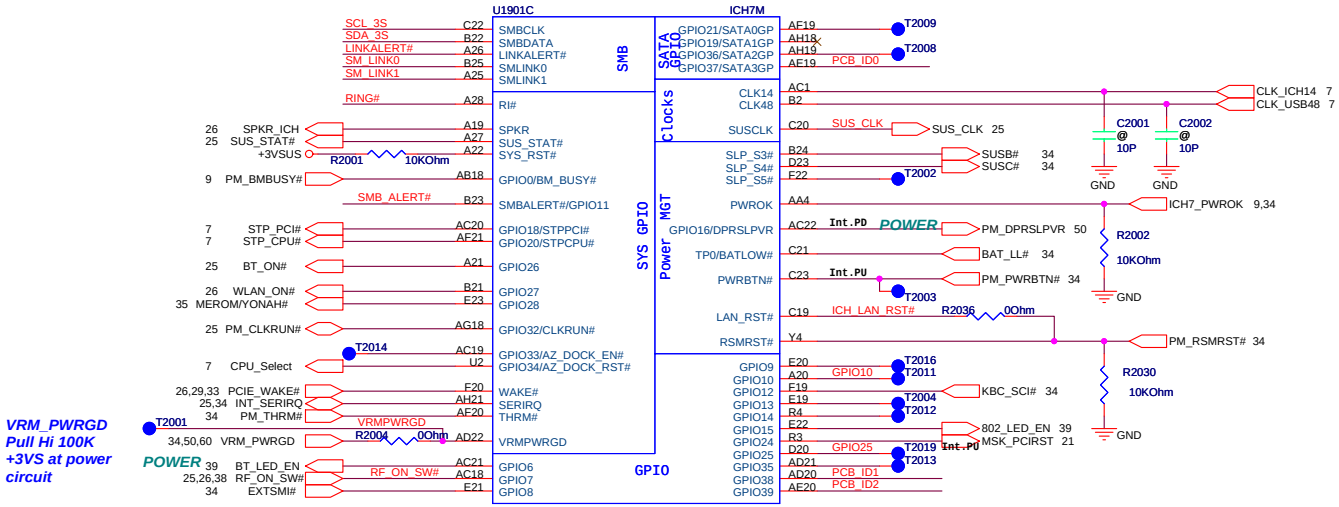
Title : ICH7M (1)

Engineer:

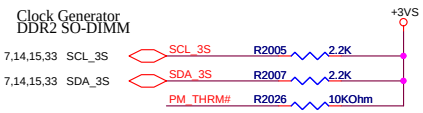
Size	Project Name	Rev
Custom	F9J	2.0

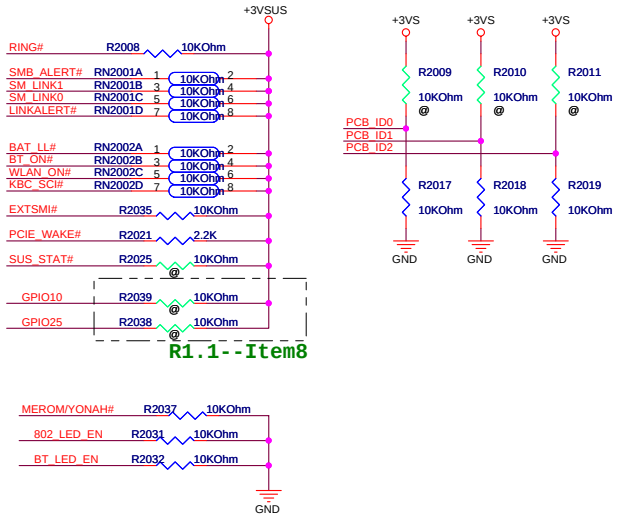
Date: Thursday, November 23, 2006 Sheet 19 of 63

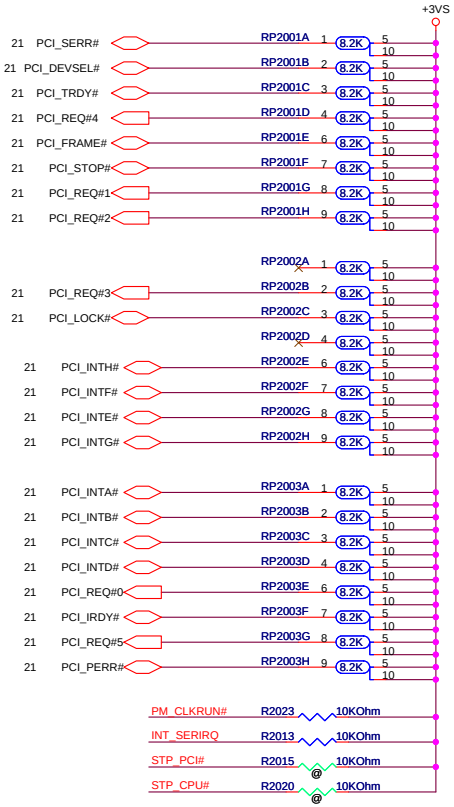
To new card check power plane



VRM_PWRGD
Pull Hi 100K
+3VS at power
circuit







<Variant Name>

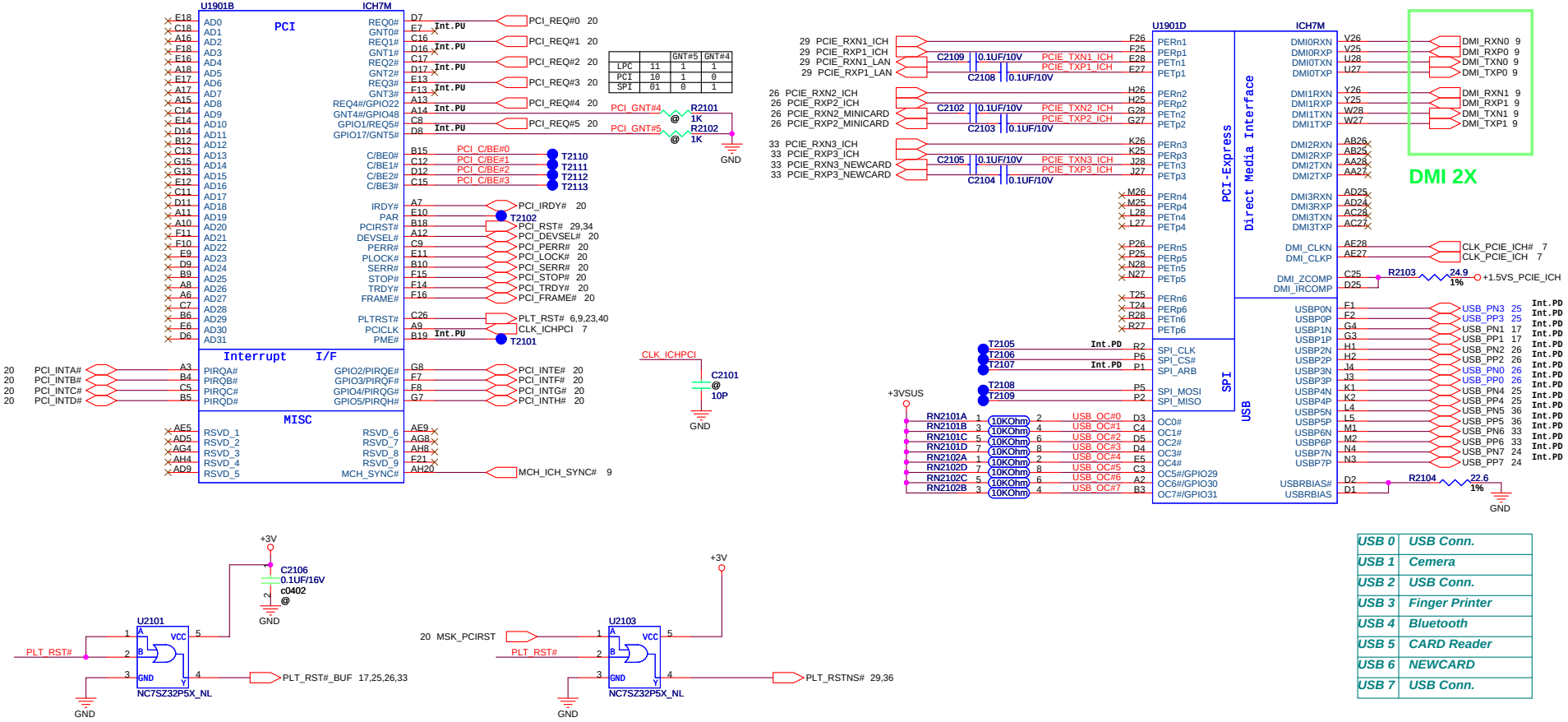
ASUSTeK COMPUTER INC

Title : ICH7M (2)

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: Thursday, November 23, 2006 Sheet 20 of 63



USB 0	USB Conn.
USB 1	Cemera
USB 2	USB Conn.
USB 3	Finger Printer
USB 4	Bluetooth
USB 5	CARD Reader
USB 6	NEWCARD
USB 7	USB Conn.

<Variant Name>

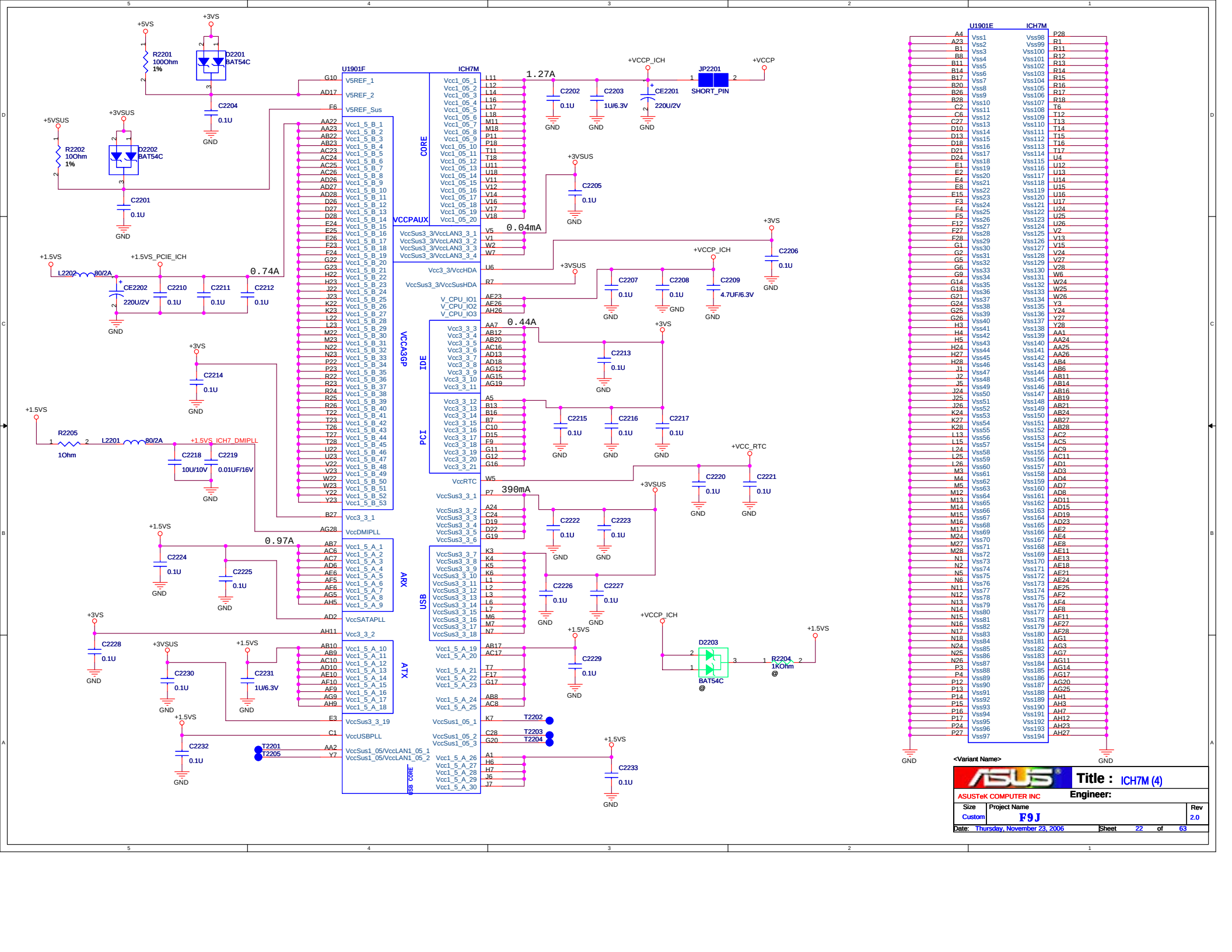
ASUSTeK COMPUTER INC

Title : ICH7M (3)

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: Thursday, November 23, 2006 Sheet 21 of 63



<Variant Name>

ASUSTeK COMPUTER INC

Title : ICH7M (4)

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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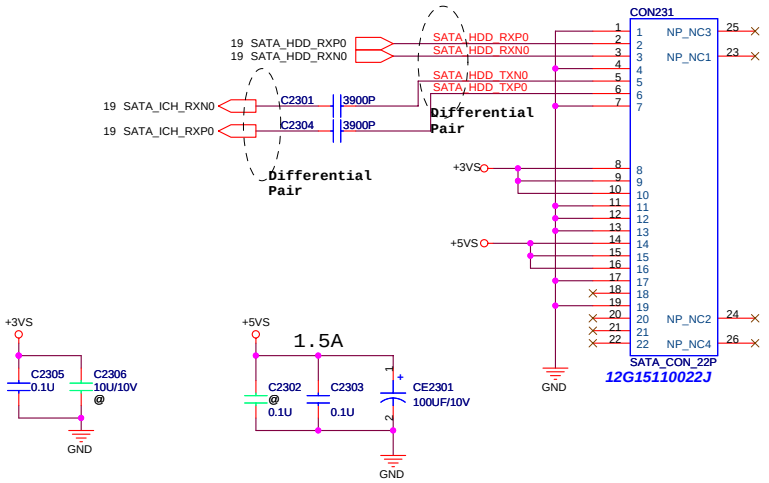
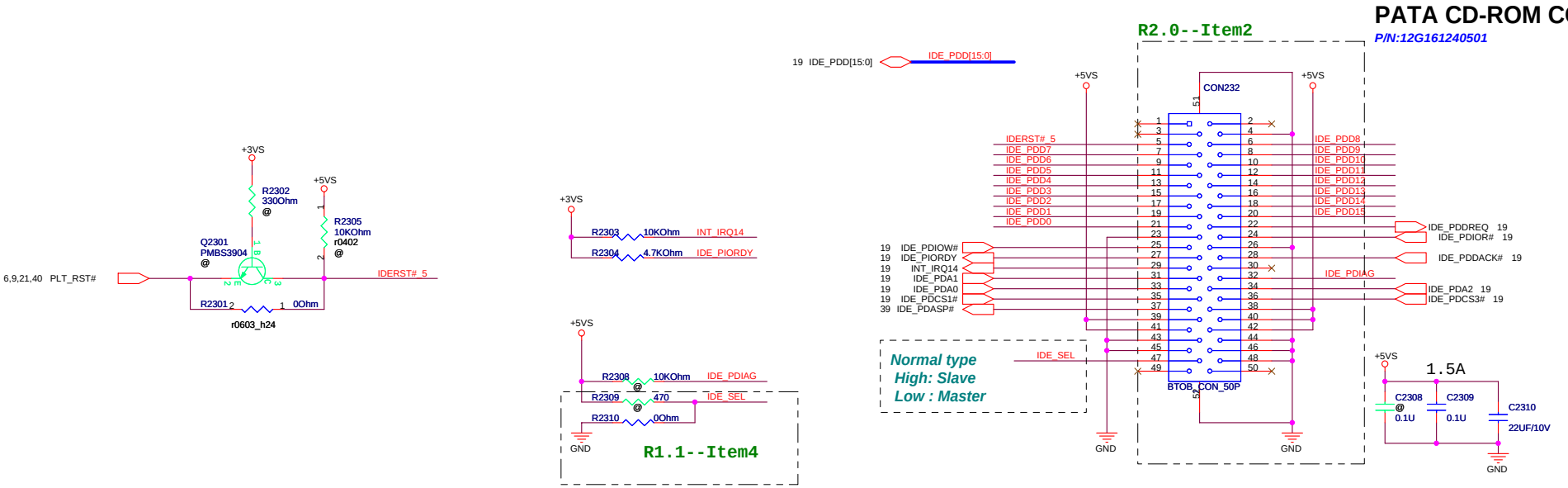
SATA HDD CON

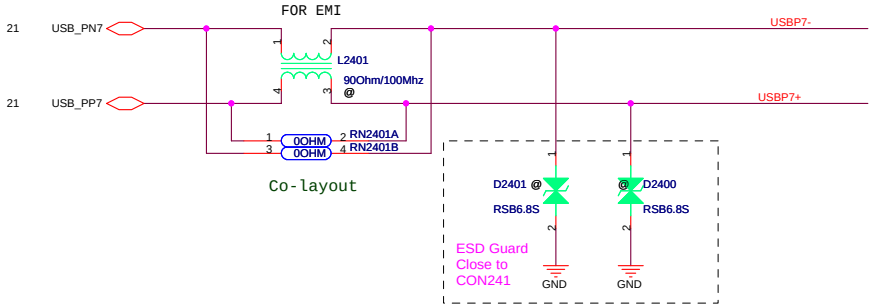


PATA CD-ROM CON

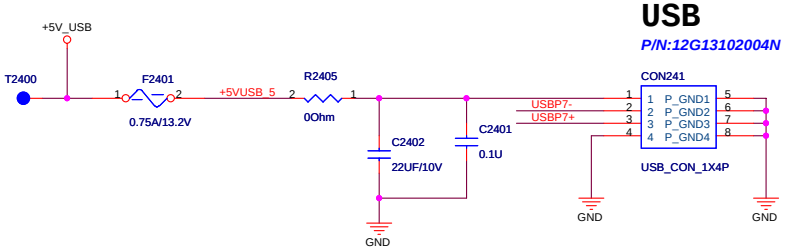


<Variant Name>

ASUSTeK COMPUTER INC	Title : HDD & CDROM	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Thursday, November 23, 2006	Sheet 23 of 63	

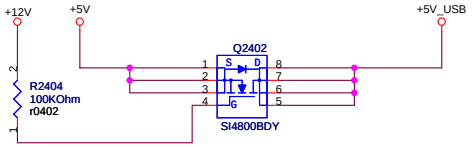


Change ESD package for layout placement.



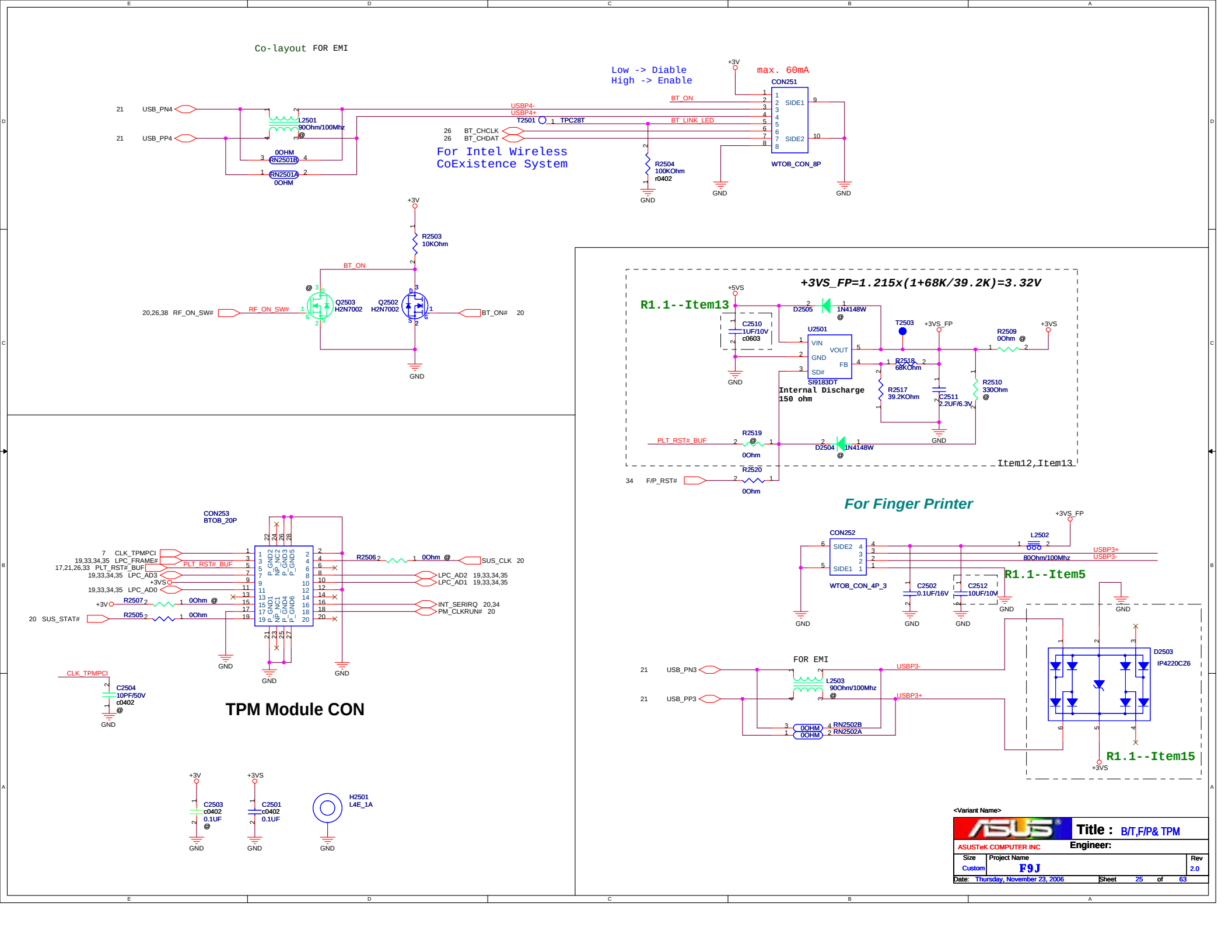
USB

P/N:12G13102004N



<Variant Name>

ASUSTeK COMPUTER INC	Title : USB PORTS	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Thursday, November 23, 2006	Sheet 24 of 63	


Co-layout FOR EMI
Low -> Diable
High -> Enable
max. 60mA
For Intel Wireless
CoExistence System
CON251
WTOB_CON_8P
T2501
TPC28T
L2501
90Ohm/100Mhz
RN2501A
RN2501B
0OHM
R2504
100KOhm
r0402
R2503
10KOhm
Q2503
H2N7002
Q2502
H2N7002
BT_ON
RF_ON_SW#
BT_ON#
+3VS_FP=1.215x(1+68K/39.2K)=3.32V
R1.1--Item13
U2501
SI9183DT
Internal Discharge
150 ohm
D2505
D2504
1N4148W
T2503
R2518
68KOhm
R2517
39.2KOhm
C2511
2.2UF/6.3V
R2510
330Ohm
R2509
0Ohm
C2510
1UF/10V
c0603
R2519
R2520
0Ohm
PLT_RST# BUF
F/P_RST#
Item12,Item13
For Finger Printer
CON252
WTOB_CON_4P_3
L2502
80Ohm/100Mhz
C2502
0.1UF/16V
C2512
10UF/10V
R1.1--Item5
FOR EMI
L2503
90Ohm/100Mhz
RN2502B
RN2502A
D2503
IP4220CZ6
R1.1--Item15
CON253
BTOB_20P
TPM Module CON
R2506
R2507
R2505
C2504
10PF/50V
c0402
C2503
c0402
0.1UF
C2501
c0402
0.1UF
H2501
L4E_1A
<Variant Name>
Title : B/T,F/P& TPM
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9J
Rev 2.0
Date: Thursday, November 23, 2006
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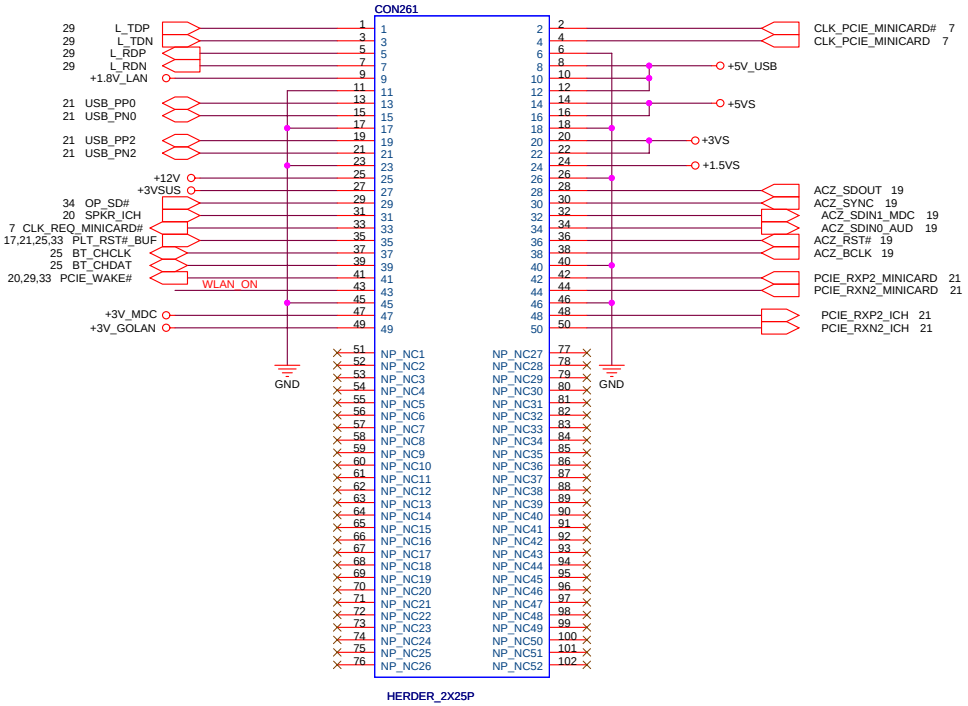
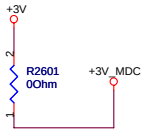
POWER CONSUMPTION:
+3VS: +3.003V~+3.597V
Max= 750 mA

+1.5VS:+1.425V~+1.575V
Max= 375 mA

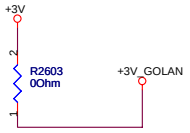
+3VAUX_GOLAN:+3.003V~+3.597V
Max= 250 mA

+3VAUX_MDC:+3.003V~+3.597V
Max= 300 mA



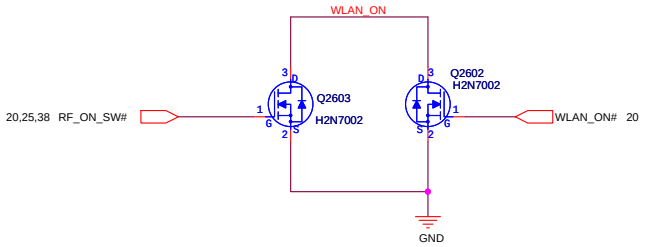


Reserved R to +3VSUS for
Wake on RING function!



Reserved R to +3VSUS for
Wake on WLAN function!

Intel SPEC(18780):Internal
Pull UP 110Kohm



<Variant Name>

ASUSTeK COMPUTER INC	Title : B TO B CONN(M)	
	Engineer:	
Size: Custom	Project Name	Rev: 2.0
Date: Thursday, November 23, 2006	Sheet 26 of 63	

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9F	2.0

Date: Thursday, November 23, 2006 Sheet 27 of 63

<Variant Name>

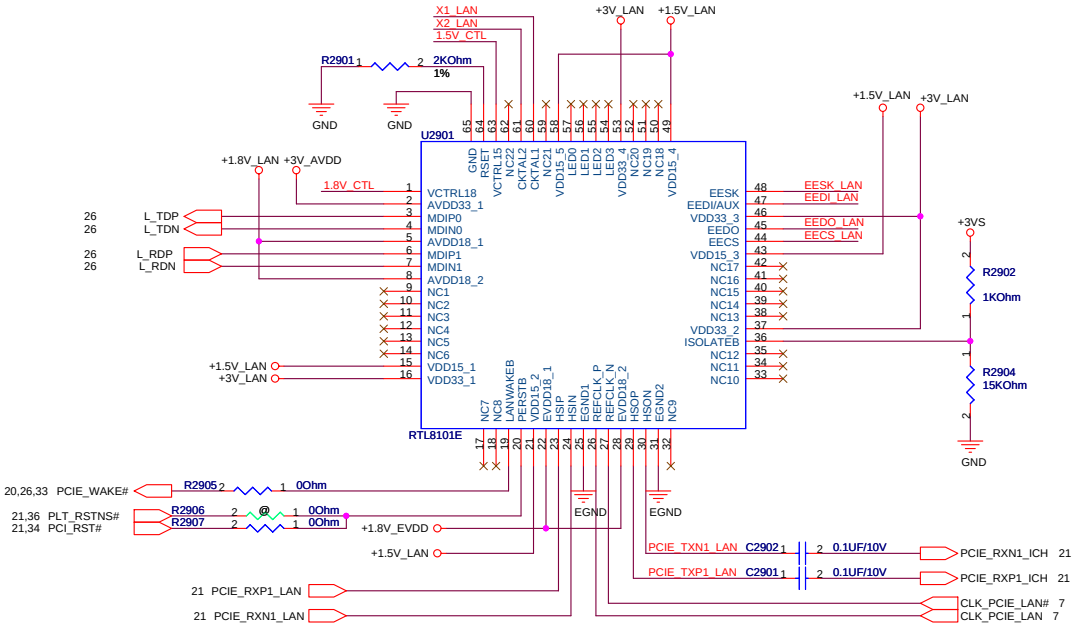
Title : EMPTY

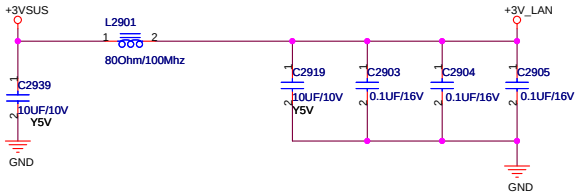
ASUSTeK COMPUTER INC

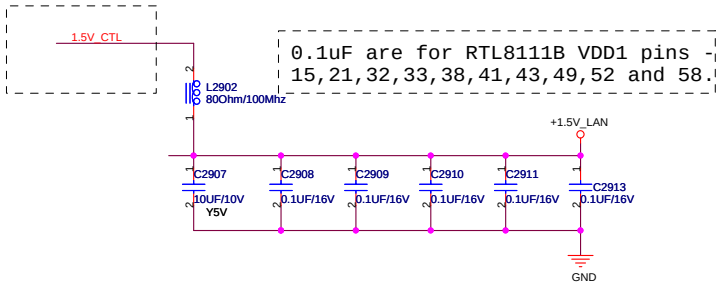
Engineer:

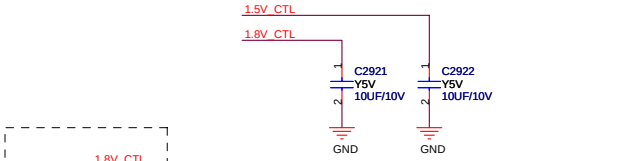
Size	Project Name	Rev
Custom	F9F	2.0

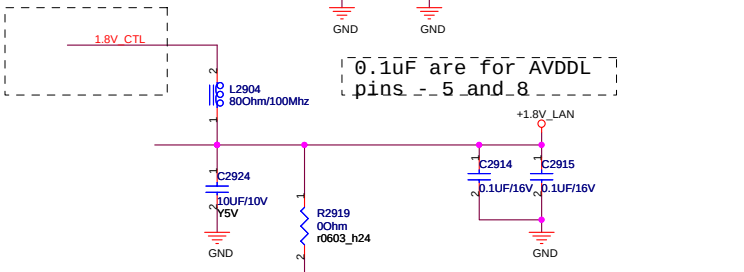
Date: Thursday, November 23, 2006 Sheet 28 of 63

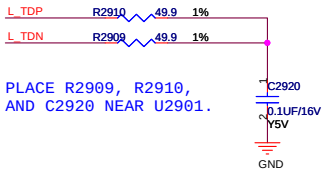

X1_LAN
X2_LAN
1.5V_CTL
+3V_LAN
+1.5V_LAN
R2901 2KOhm 1%
GND
U2901
RTL8101E
+1.8V_LAN
+3V_AVDD
1.8V_CTL
L_TDP
L_TDN
L_RDP
L_RDN
EESK_LAN
EEDI_LAN
EEDO_LAN
EECS_LAN
+3VS
R2902 1KOhm
R2904 15KOhm
20,26,33 PCIE_WAKE#
R2905 0Ohm
21,36 PLT_RSTNS#
21,34 PCI_RST#
R2906 0Ohm
R2907 0Ohm
+1.8V_EVDD
EGND
PCIE_TXN1_LAN C2902 0.1UF/10V
PCIE_TXP1_LAN C2901 0.1UF/10V
PCIE_RXN1_ICH 21
PCIE_RXP1_ICH 21
21 PCIE_RXP1_LAN
21 PCIE_RXN1_LAN
CLK_PCIE_LAN# 7
CLK_PCIE_LAN 7

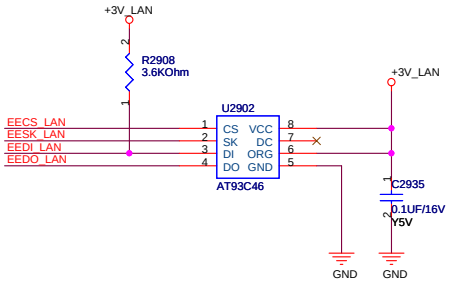

+3VSUS
L2901 80Ohm/100Mhz
C2939 10UF/10V Y5V
C2919 10UF/10V Y5V
C2903 0.1UF/16V
C2904 0.1UF/16V
C2905 0.1UF/16V
+3V_LAN
GND

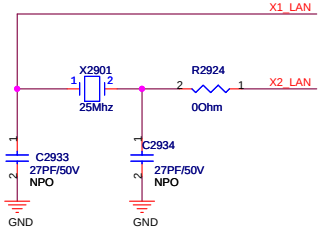

1.5V_CTL
L2902 80Ohm/100Mhz
0.1uF are for RTL8111B VDD1 pins - 15,21,32,33,38,41,43,49,52 and 58.
+1.5V_LAN
C2907 10UF/10V Y5V
C2908 0.1UF/16V
C2909 0.1UF/16V
C2910 0.1UF/16V
C2911 0.1UF/16V
C2913 0.1UF/16V
GND

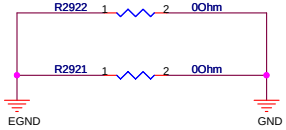

1.5V_CTL
1.8V_CTL
C2921 Y5V 10UF/10V
C2922 Y5V 10UF/10V
GND

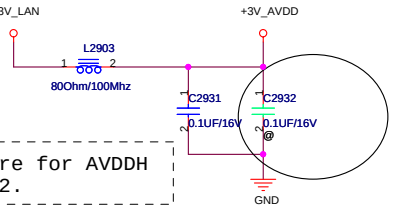

1.8V_CTL
L2904 80Ohm/100Mhz
0.1uF are for AVDDL pins - 5 and 8
+1.8V_LAN
C2924 10UF/10V Y5V
C2914 0.1UF/16V
C2915 0.1UF/16V
R2919 0Ohm r0603_h24
GND
Caps are for VDD1A pins
+1.8V_EVDD
C2938 4.7UF/6.3V X5R
C2927 0.1UF/16V
C2928 0.1UF/16V
C2929 100PF/50V NPO
C2930 100PF/50V NPO
EGND


L_TDP
L_TDN
R2910 49.9 1%
R2909 49.9 1%
PLACE R2909, R2910,
AND C2920 NEAR U2901.
C2920 0.1UF/16V Y5V
GND


+3V_LAN
R2908 3.6KOhm
U2902
AT93C46
EECS_LAN
EESK_LAN
EEDI_LAN
EEDO_LAN
CS VCC
SK DC
DI ORG
DO GND
C2935 0.1UF/16V Y5V
GND


X1_LAN
X2901 25Mhz
R2924 0Ohm
X2_LAN
C2933 27PF/50V NPO
C2934 27PF/50V NPO
GND


R2922 0Ohm
R2921 0Ohm
EGND
GND


+3V_LAN
+3V_AVDD
L2903 80Ohm/100Mhz
C2931 0.1UF/16V
C2932 0.1UF/16V
@
0.1uF are for AVDDH pins - 2.
GND

<Variant Name>
Title : LAN RTL8101E
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9J
Rev 2.0
Date: Thursday, November 23, 2006
Sheet 29 of 63

Title : EMPTY

ASUSTek COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: Thursday, November 23, 2006 Sheet 30 of 63

Title : EMPTY

ASUSTek COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: Thursday, November 23, 2006 Sheet 31 of 63

<Variant Name>

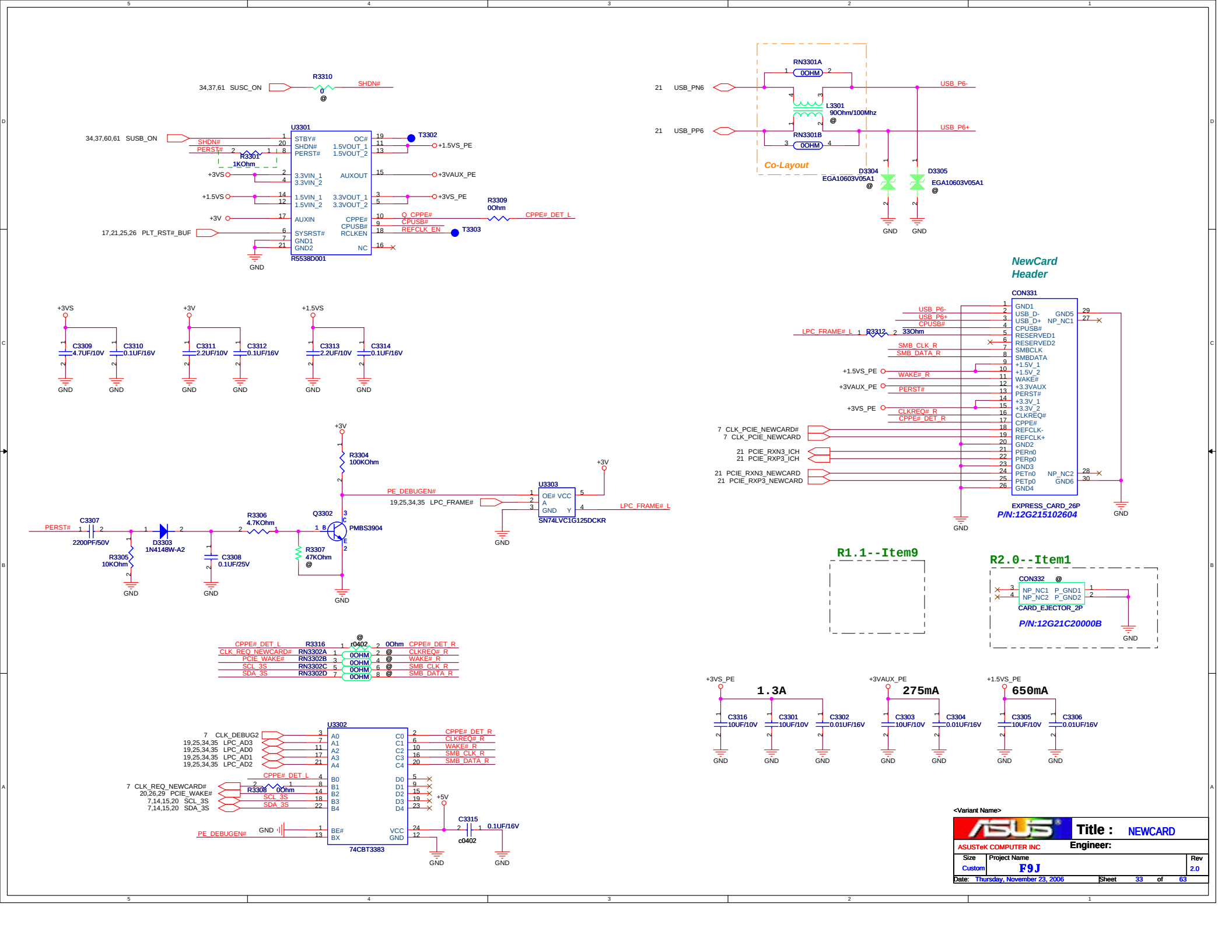
Title : EMPTY

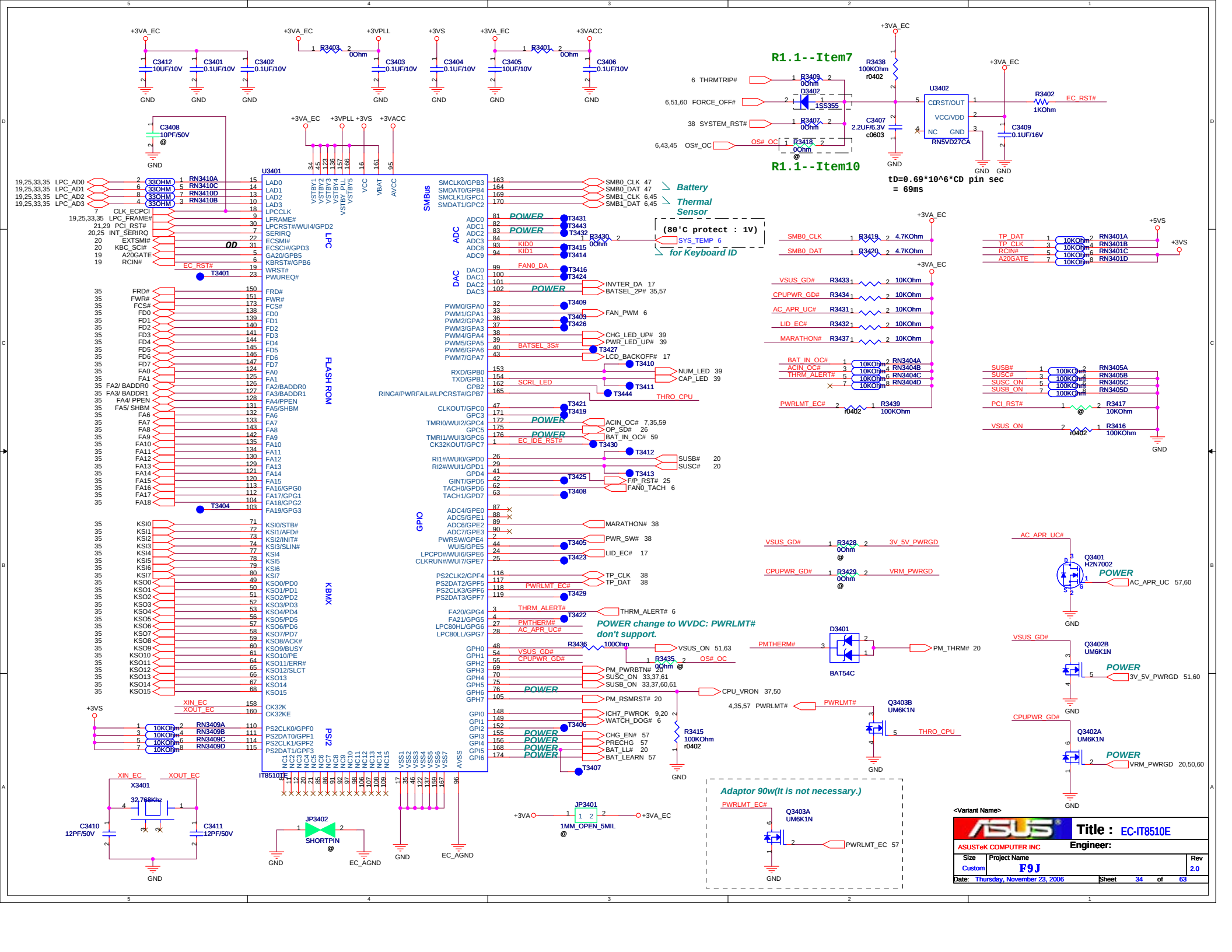
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: Thursday, November 23, 2006 Sheet 32 of 63


R3310
34,37,61 SUSC_ON
SHDN#
U3301
R5538D001
T3302
T3303
+1.5VS_PE
+3VAUX_PE
+3VS_PE
R3309
0Ohm
CPPE# DET L
17,21,25,26 PLT_RST#_BUF
RN3301A
RN3301B
L3301
90Ohm/100Mhz
21 USB_PN6
21 USB_PP6
USB_P6-
USB_P6+
Co-Layout
D3304
EGA10603V05A1
D3305
C3309 4.7UF/10V
C3310 0.1UF/16V
C3311 2.2UF/10V
C3312 0.1UF/16V
C3313 2.2UF/10V
C3314 0.1UF/16V
NewCard Header
CON331
EXPRESS_CARD_26P
P/N:12G215102604
LPC_FRAME# L
R3312 33Ohm
SMB_CLK_R
SMB_DATA_R
WAKE# R
PERST#
CLKREQ# R
CPPE# DET R
7 CLK_PCIE_NEWCARD#
7 CLK_PCIE_NEWCARD
21 PCIE_RXN3_ICH
21 PCIE_RXP3_ICH
21 PCIE_RXN3_NEWCARD
21 PCIE_RXP3_NEWCARD
R3304 100KOhm
PE_DEBUGEN#
19,25,34,35 LPC_FRAME#
U3303
SN74LVC1G125DCKR
LPC_FRAME# L
C3307 2200PF/50V
R3306 4.7KOhm
Q3302
PMBS3904
D3303 1N4148W-A2
R3305 10KOhm
C3308 0.1UF/25V
R3307 47KOhm
R1.1--Item9
R2.0--Item1
CON332
CARD_EJECTOR_2P
P/N:12G21C20000B
CPPE# DET L
R3316
CLK_REQ_NEWCARD#
PCIE_WAKE#
SCL_3S
SDA_3S
RN3302A
RN3302B
RN3302C
RN3302D
CLKREQ# R
WAKE# R
SMB_CLK_R
SMB_DATA_R
U3302
74CBT3383
7 CLK_DEBUG2
19,25,34,35 LPC_AD3
19,25,34,35 LPC_AD0
19,25,34,35 LPC_AD1
19,25,34,35 LPC_AD2
7 CLK_REQ_NEWCARD#
20,26,29 PCIE_WAKE#
7,14,15,20 SCL_3S
7,14,15,20 SDA_3S
PE_DEBUGEN#
C3315 0.1UF/16V
+3VS_PE 1.3A
+3VAUX_PE 275mA
+1.5VS_PE 650mA
C3316 10UF/10V
C3301 10UF/10V
C3302 0.01UF/16V
C3303 10UF/10V
C3304 0.01UF/16V
C3305 10UF/10V
C3306 0.01UF/16V
GND
Title : NEWCARD
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9J
Rev 2.0
Date: Thursday, November 23, 2006
Sheet 33 of 63


R1.1--Item7
R1.1--Item10
tD=0.69*10^6*CD pin sec
= 69ms
U3401
IT8510TE
Battery
Thermal
Sensor
(80'C protect : 1V)
for Keyboard ID
POWER change to WVDC: PWRLMT#
don't support.
Adaptor 90w(It is not necessary.)
LPC
FLASH ROM
KBMX
PS/2
SMBus
ADC
DAC
GPIO
OD
Title : EC-IT8510E
ASUSTeK COMPUTER INC
Engineer:
Project Name F9J
Size Custom
Rev 2.0
Date: Thursday, November 23, 2006
Sheet 34 of 63

EC Hardware Strapping

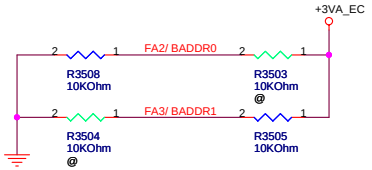
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

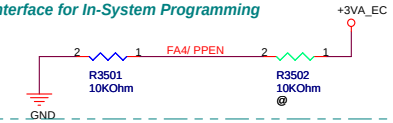


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

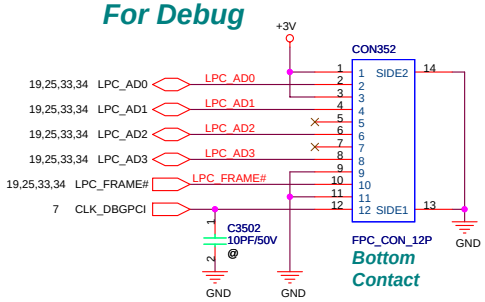


FA5/ SHBM

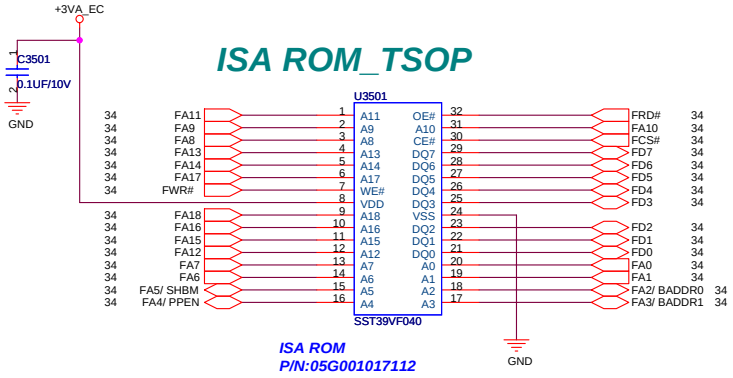
0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS

For Debug



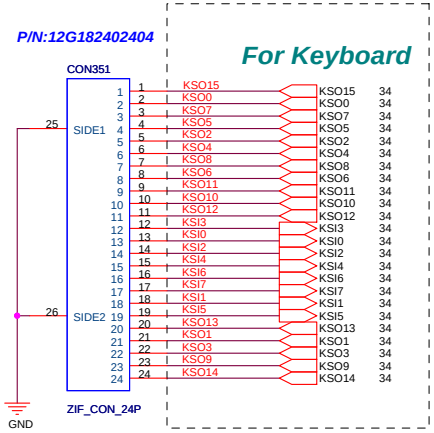
ISA ROM_TSOP

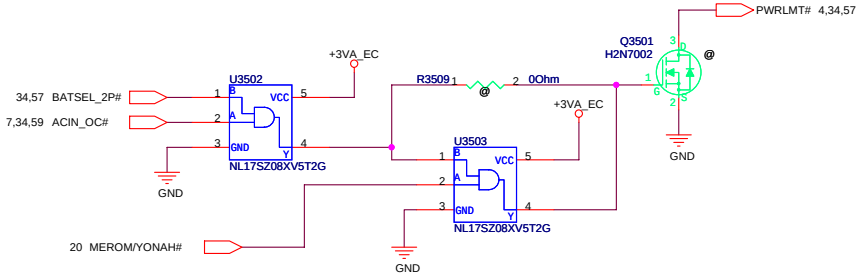


ISA ROM
P/N:05G001017112

P/N:12G182402404

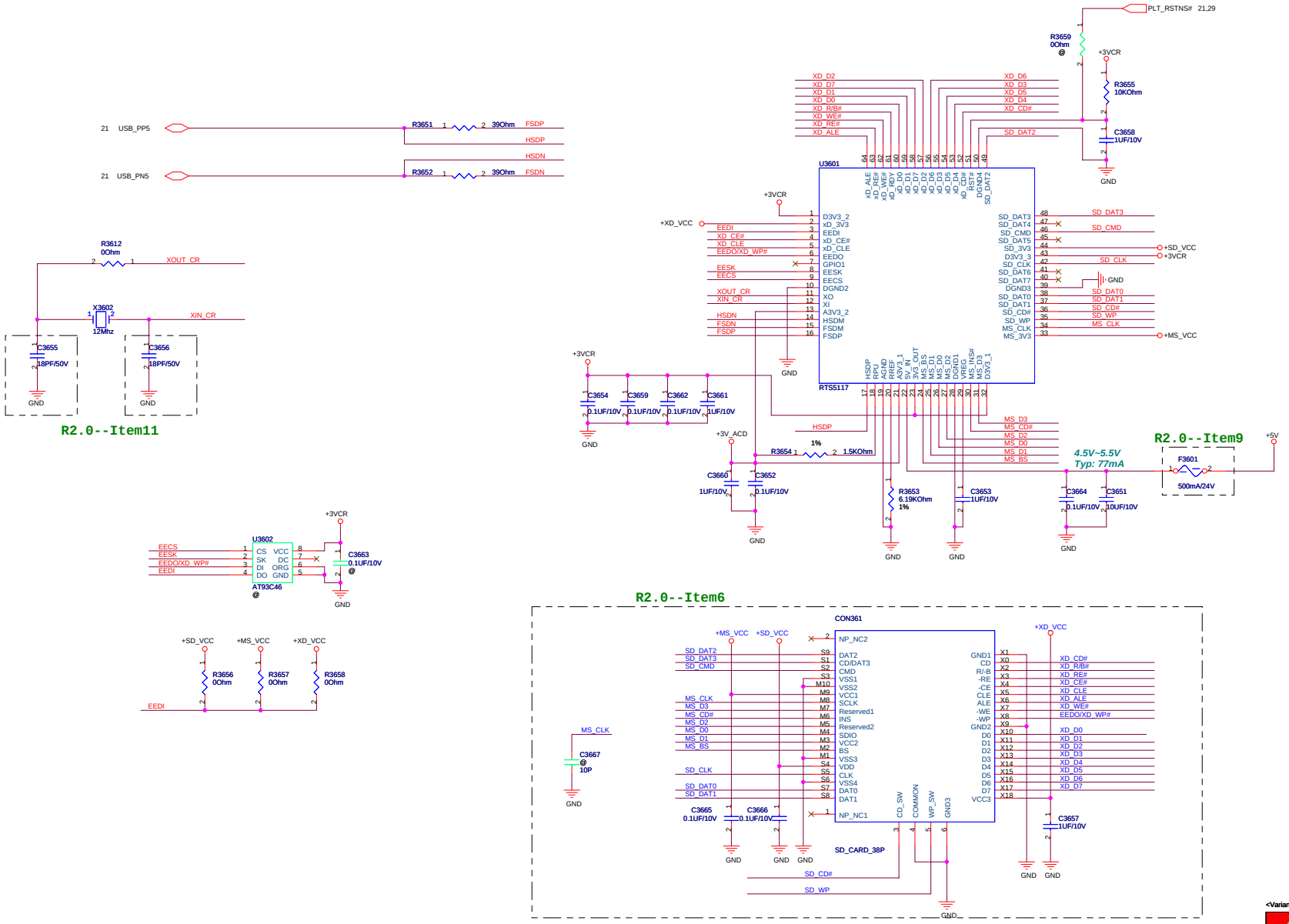
For Keyboard





<Variant Name>

ASUSTeK COMPUTER INC	Title : ISA_ROM&KB conn	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Thursday, November 23, 2006	Sheet 35 of 63	



<Variant Name>

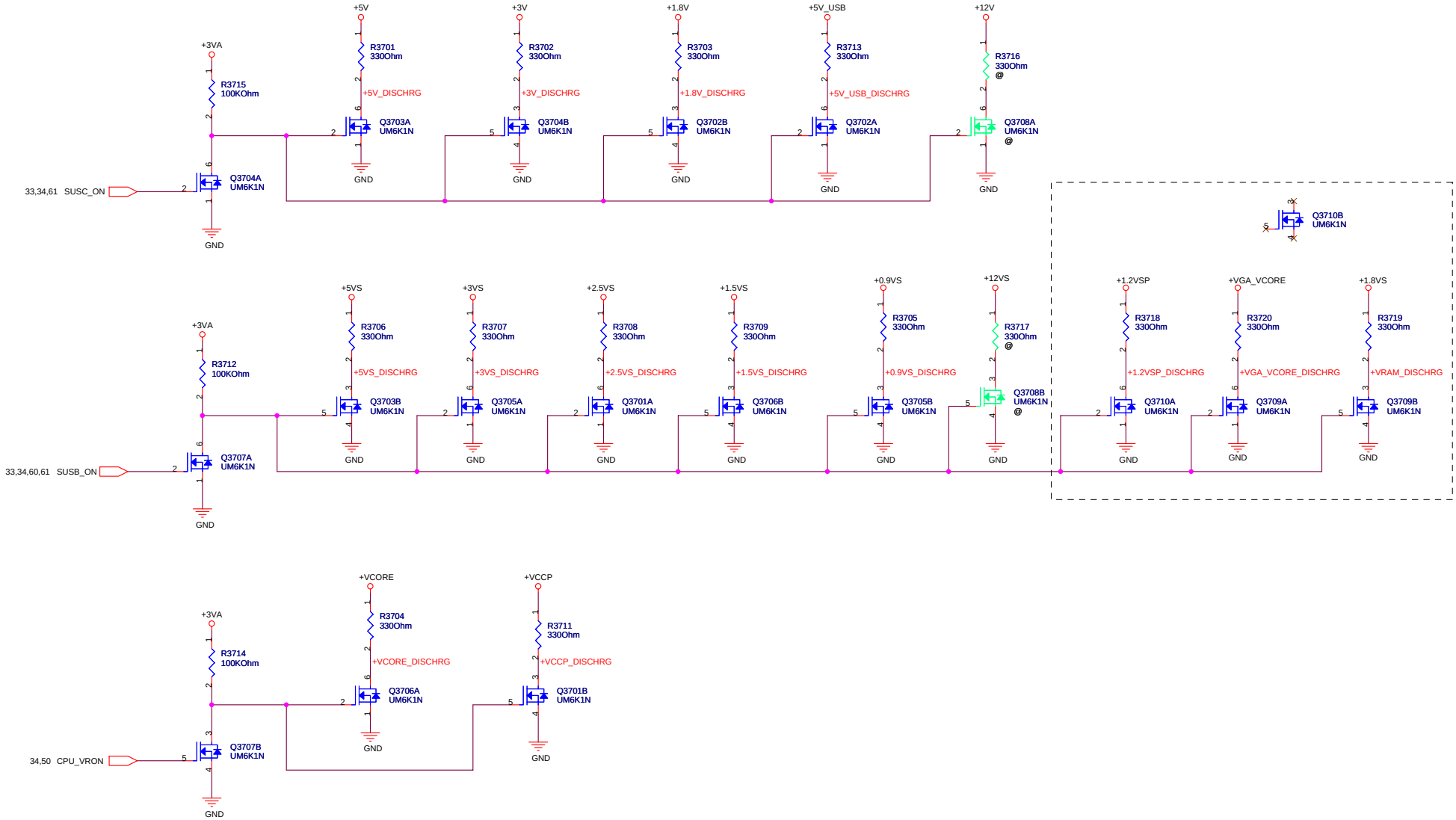
ASUSTeK COMPUTER INC

Title : RTS5117

Engineer:

Size	Project Name	Rev
C	F9J	2.0

Date: Thursday, November 23, 2006 Sheet 36 of 63



<Variant Name>

ASUSTeK COMPUTER INC

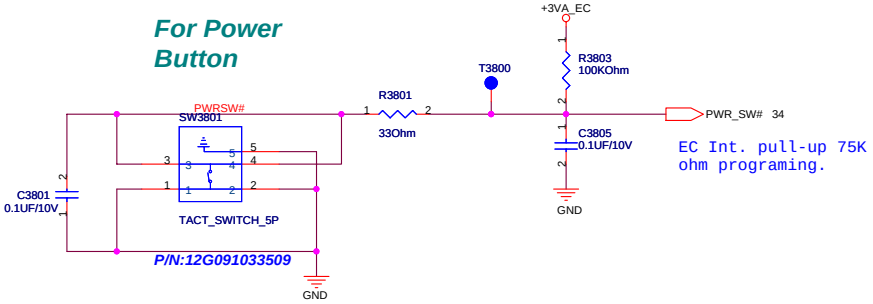
Title : DISCHARGE

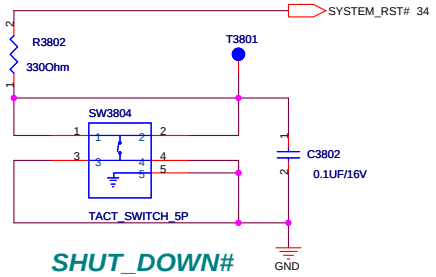
Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

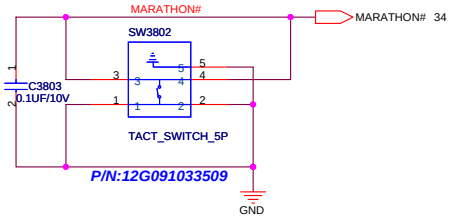
Date: Thursday, November 23, 2006 Sheet 37 of 63

For Power Button

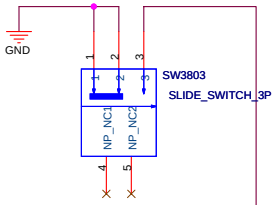




SHUT_DOWN#

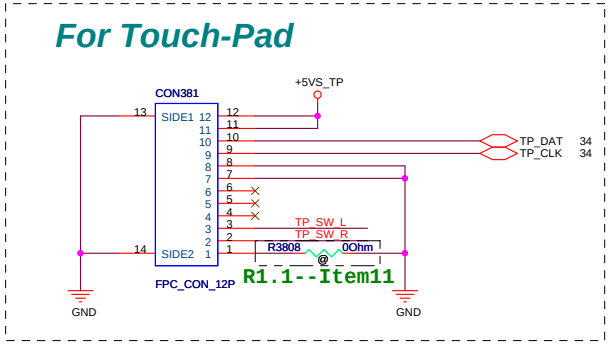


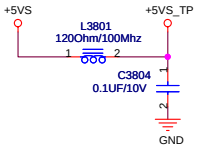
MARATHON#

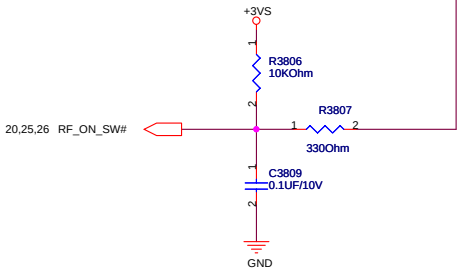


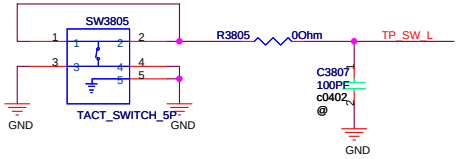
BT/WLAN SW

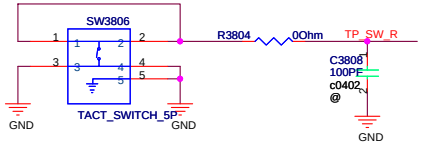
For Touch-Pad











<Variant Name>

ASUSTeK COMPUTER INC

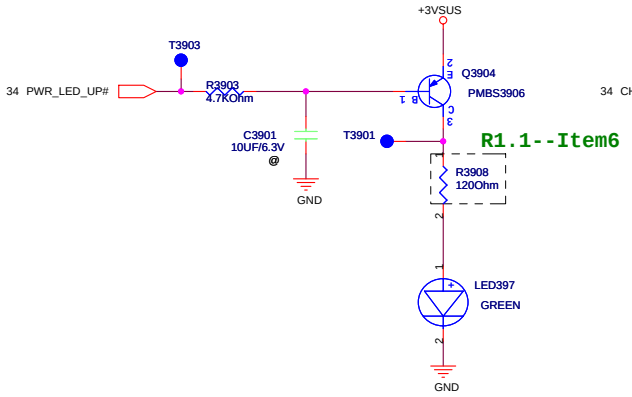
Title : KEY & LED

Engineer:

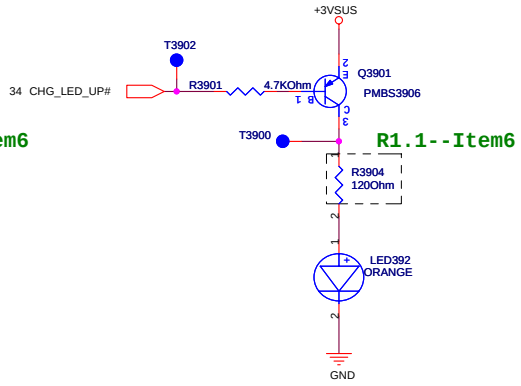
Size	Project Name	Rev
Custom	F9J	2.0

Date: Thursday, November 23, 2006 Sheet 38 of 63

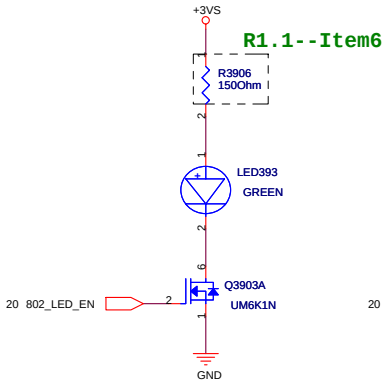
For PWR LED



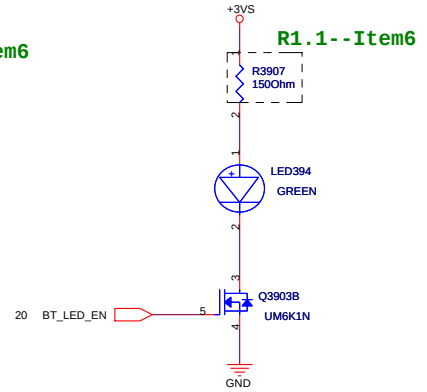
For BATTERY LED



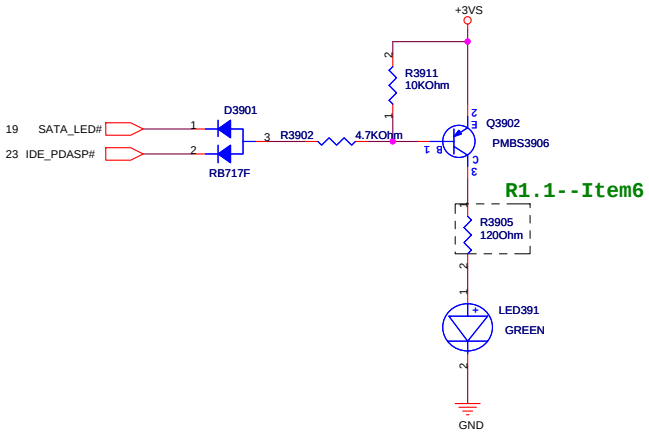
For WireLess LED



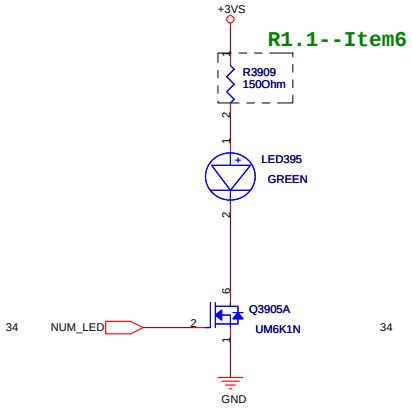
For BT LED



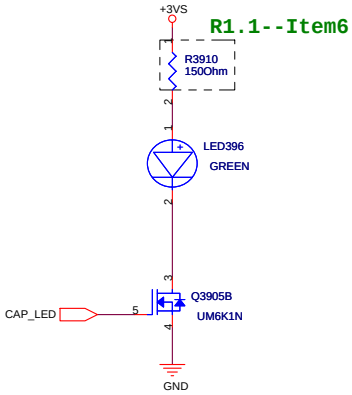
For SATA/IDE LED



For Num Lock

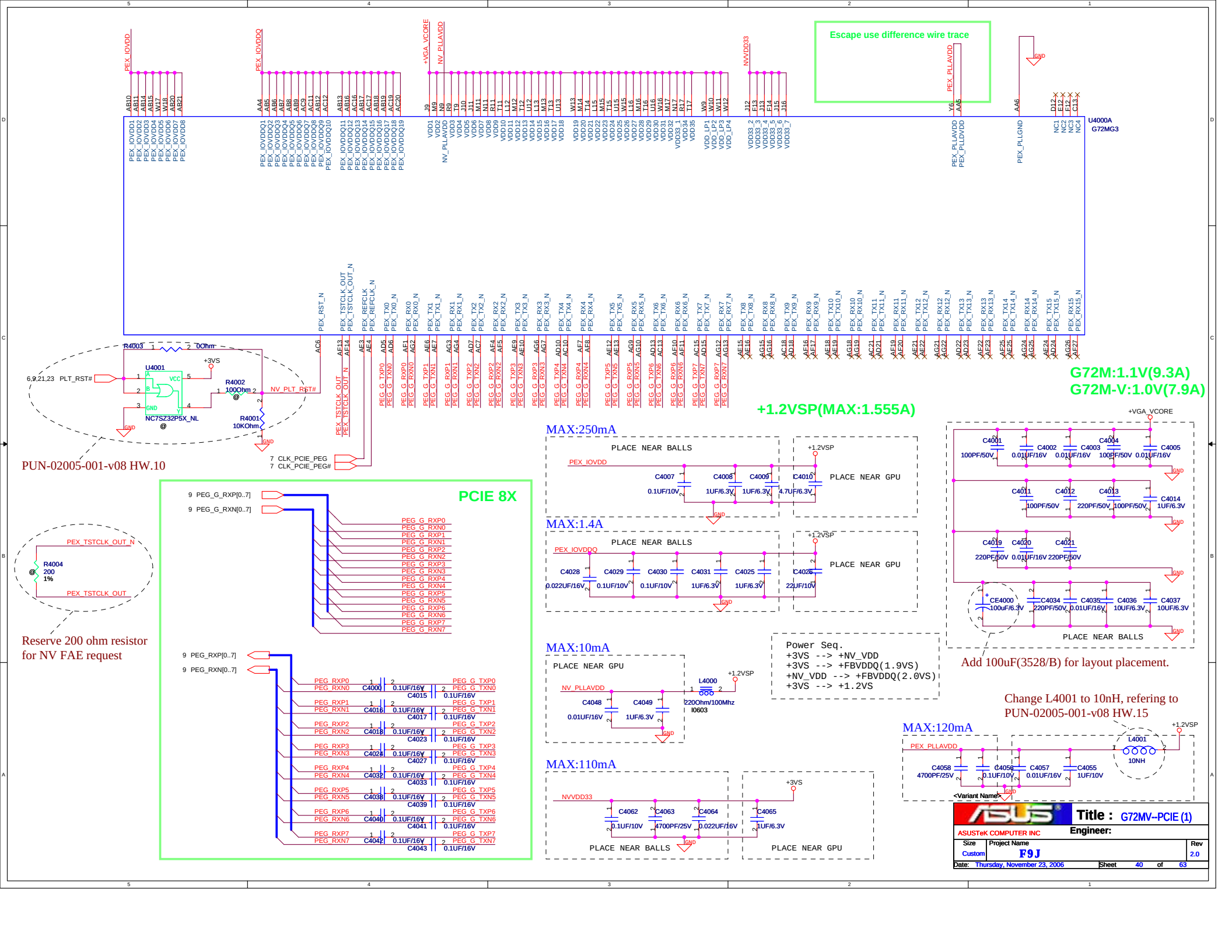


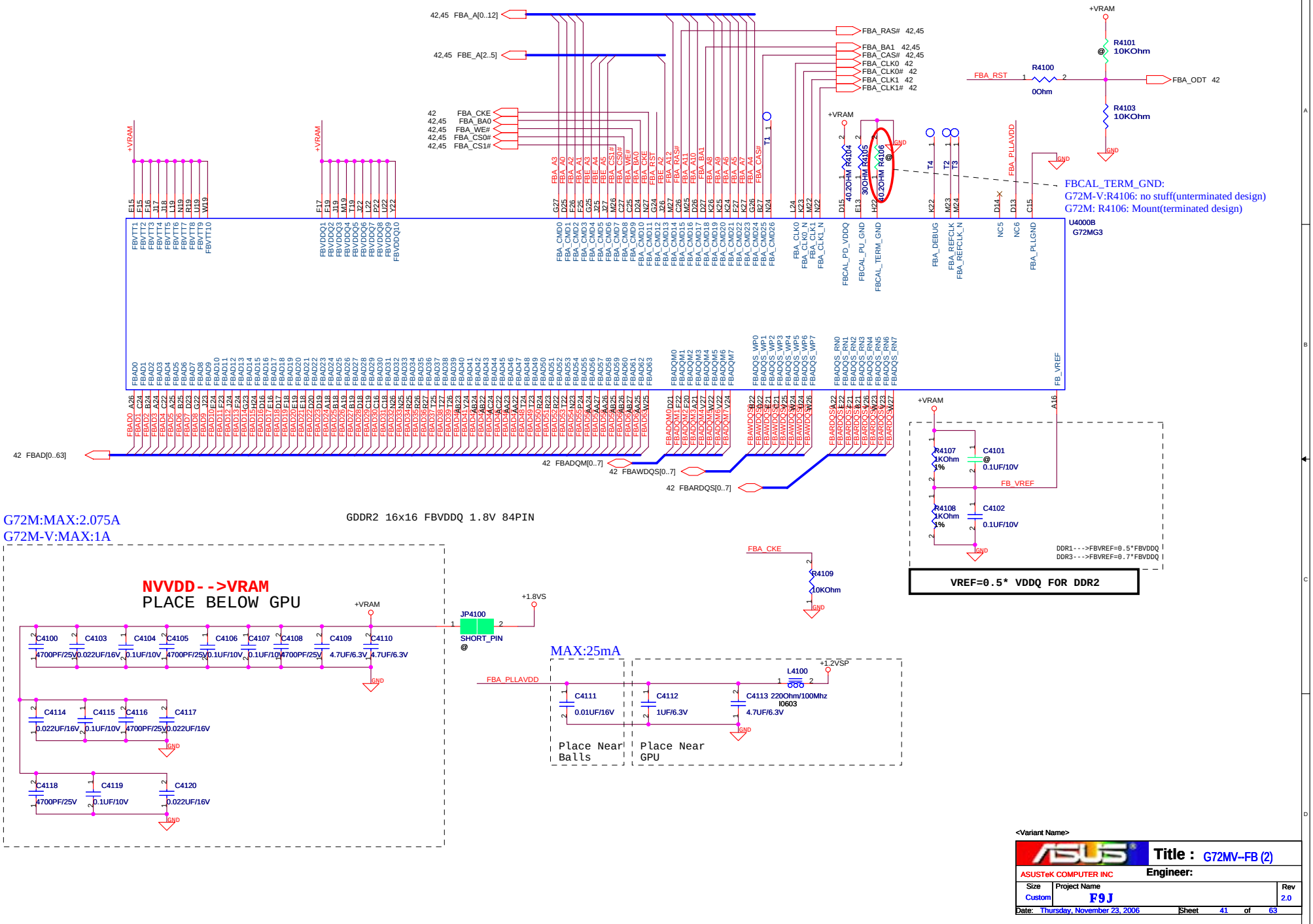
For Cap. Lock



<Variant Name>

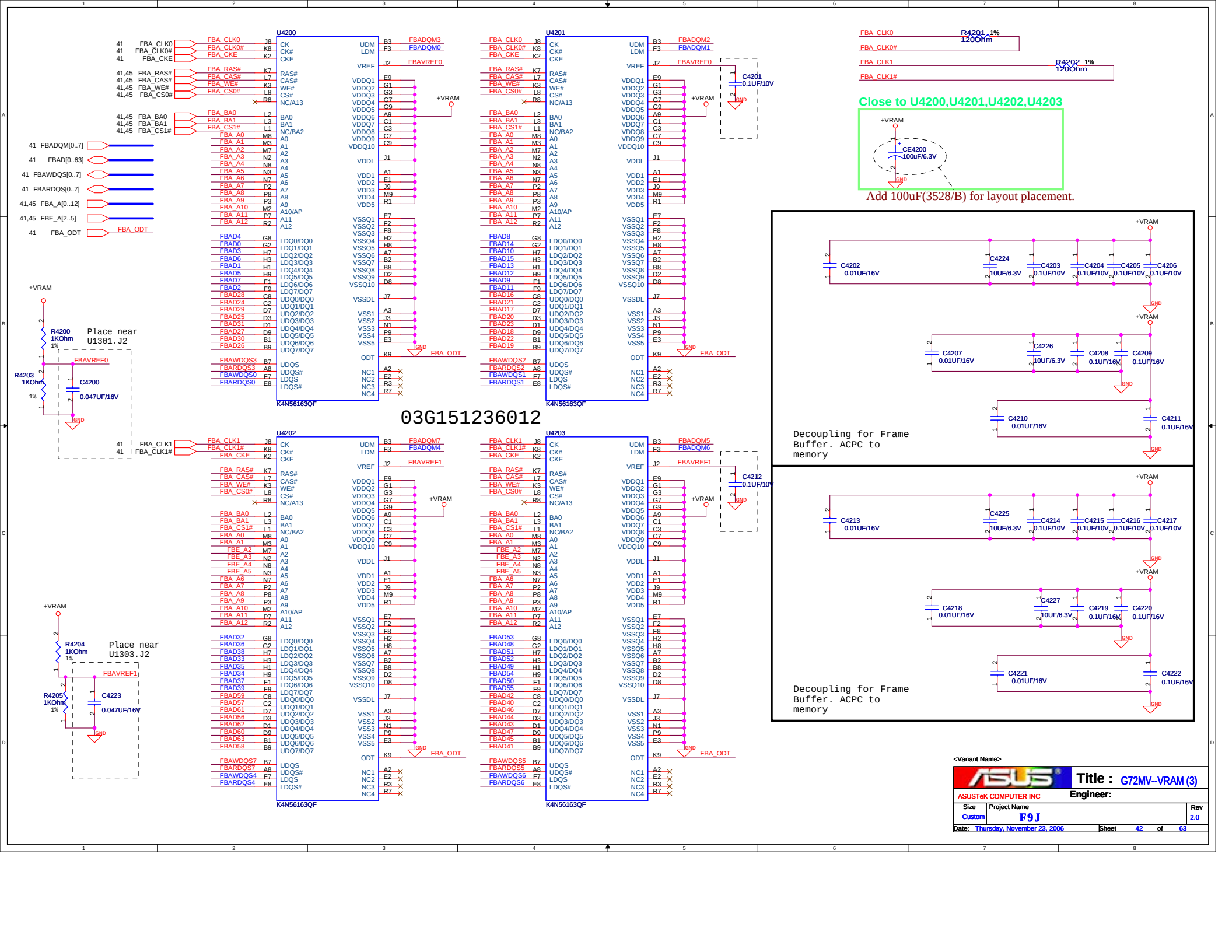
ASUSTeK COMPUTER INC	Title : LEDs	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Thursday, November 23, 2006	Sheet 39 of 63	


Escape use difference wire trace
U4000A
G72MG3
G72M:1.1V(9.3A)
G72M-V:1.0V(7.9A)
+1.2VSP(MAX:1.555A)
PUN-02005-001-v08 HW.10
PCIE 8X
Reserve 200 ohm resistor for NV FAE request
MAX:250mA
MAX:1.4A
MAX:10mA
MAX:110mA
MAX:120mA
PLACE NEAR BALLS
PLACE NEAR GPU
Power Seq.
+3VS --> +NV_VDD
+3VS --> +FBVDDQ(1.9VS)
+NV_VDD --> +FBVDDQ(2.0VS)
+3VS --> +1.2VS
Add 100uF(3528/B) for layout placement.
Change L4001 to 10nH, refering to PUN-02005-001-v08 HW.15
ASUSTeK COMPUTER INC
Title : G72MV--PCIE (1)
Engineer:
Project Name F9J
Rev 2.0
Thursday, November 23, 2006
Sheet 40 of 63



<Variant Name>

ASUSTeK COMPUTER INC	Title : G72MV-FB (2)	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Thursday, November 23, 2006	Sheet 41 of 63	



<Variant Name>

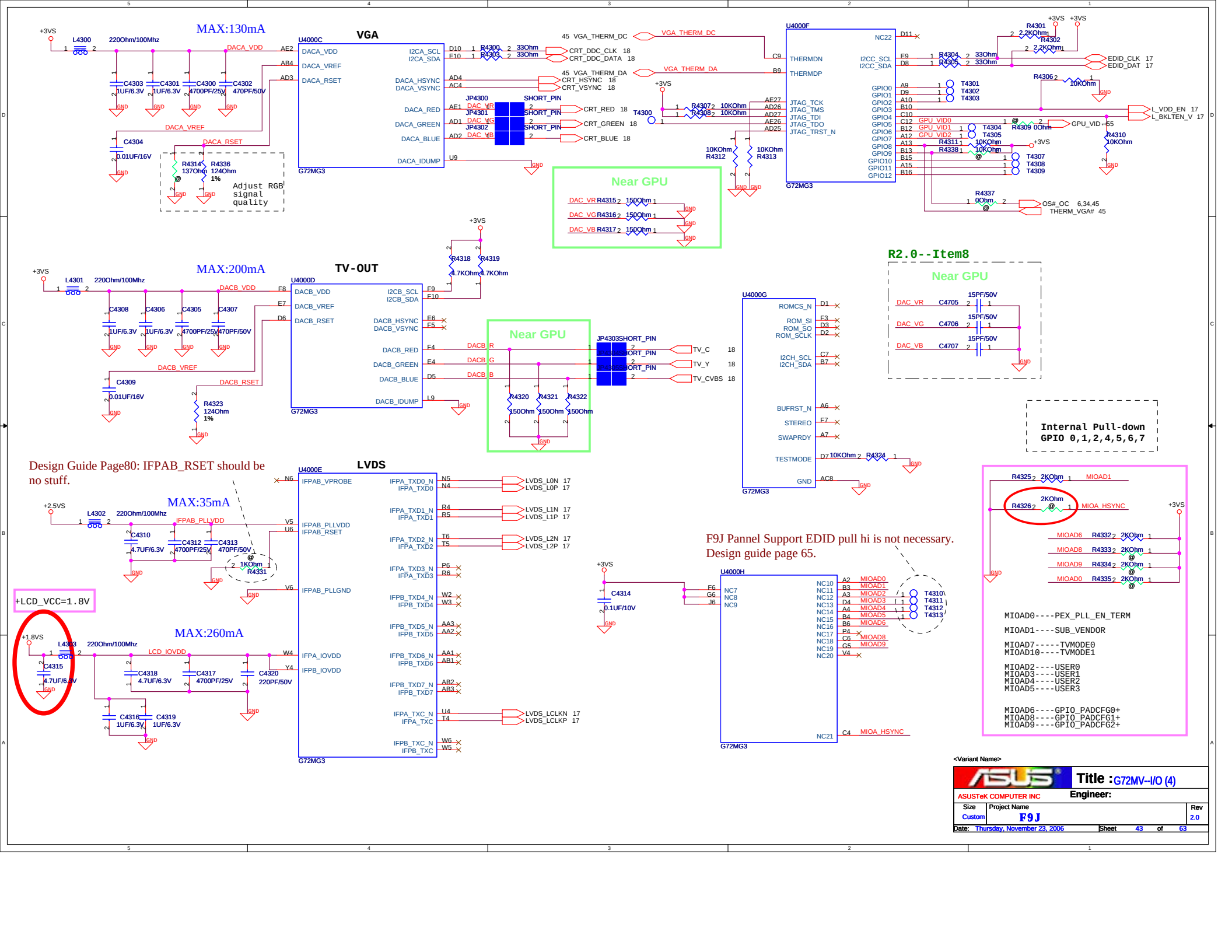
ASUSTeK COMPUTER INC

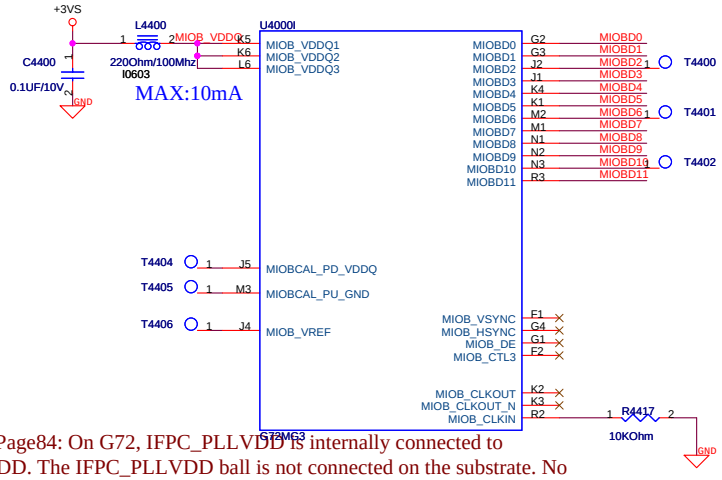
Title : G72MV-VRAM (3)

Engineer:

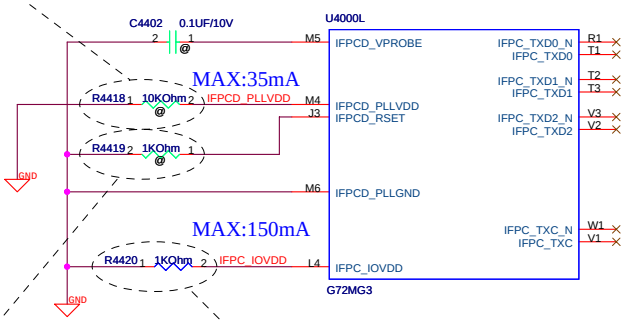
Size	Project Name	Rev
Custom	F9J	2.0

Date: Thursday, November 23, 2006 Sheet 42 of 63


VGA
MAX:130mA
U4000C
G72MG3
DACA_VDD
DACA_VREF
DACA_RSET
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_IDUMP
I2CA_SCL
I2CA_SDA
L4300
220Ohm/100Mhz
C4303 1UF/6.3V
C4301 1UF/6.3V
C4300 4700PF/25V
C4302 470PF/50V
C4304 0.01UF/16V
R4314 137Ohm 1%
R4336 124Ohm 1%
Adjust RGB signal quality
JP4300 SHORT_PIN
JP4301 SHORT_PIN
JP4302 SHORT_PIN
CRT_DDC_CLK 18
CRT_DDC_DATA 18
CRT_HSYNC 18
CRT_VSYNC 18
CRT_RED 18
CRT_GREEN 18
CRT_BLUE 18
VGA_THERM_DC
VGA_THERM_DA
45 VGA_THERM_DC
45 VGA_THERM_DA
T4300
R4307 10KOhm
R4308 10KOhm
U4000F
THERMDN
THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST_N
R4312 10KOhm
R4313 10KOhm
R4301 2.2KOhm
R4302 2.2KOhm
R4304 33Ohm
R4305 33Ohm
EDID_CLK 17
EDID_DAT 17
R4306 10KOhm
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
T4301
T4302
T4303
L_VDD_EN 17
L_BKLTEN_V 17
GPU_VID0
GPU_VID1
GPU_VID2
GPU_VID 55
T4304
T4305
R4309 0Ohm
R4310 10KOhm
R4311 10KOhm
R4338 10KOhm
T4307
T4308
T4309
R4337 0Ohm
OS#_OC 6,34,45
THERM_VGA# 45
Near GPU
DAC_VR R4315 150Ohm
DAC_VG R4316 150Ohm
DAC_VB R4317 150Ohm
TV-OUT
MAX:200mA
U4000D
DACB_VDD
DACB_VREF
DACB_RSET
DACB_HSYNC
DACB_VSYNC
DACB_RED
DACB_GREEN
DACB_BLUE
DACB_IDUMP
I2CB_SCL
I2CB_SDA
L4301
220Ohm/100Mhz
C4308 1UF/6.3V
C4306 1UF/6.3V
C4305 4700PF/25V
C4307 470PF/50V
C4309 0.01UF/16V
R4323 124Ohm 1%
R4318 4.7KOhm
R4319 4.7KOhm
JP4303SHORT_PIN
JP4304SHORT_PIN
JP4305SHORT_PIN
TV_C 18
TV_Y 18
TV_CVBS 18
R4320 150Ohm
R4321 150Ohm
R4322 150Ohm
U4000G
ROMCS_N
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST_N
STEREO
SWAPRDY
TESTMODE
GND
R4324 10KOhm
R2.0--Item8
Near GPU
DAC_VR C4705 15PF/50V
DAC_VG C4706 15PF/50V
DAC_VB C4707 15PF/50V
Internal Pull-down
GPIO 0,1,2,4,5,6,7
Design Guide Page80: IFPAB_RSET should be no stuff.
LVDS
MAX:35mA
U4000E
IFPAB_VPROBE
IFPAB_PLLVDD
IFPAB_RSET
IFPAB_PLLGND
IFPA_IOVDD
IFPB_IOVDD
IFPA_TXD0_N
IFPA_TXD0
IFPA_TXD1_N
IFPA_TXD1
IFPA_TXD2_N
IFPA_TXD2
IFPA_TXD3_N
IFPA_TXD3
IFPB_TXD4_N
IFPB_TXD4
IFPB_TXD5_N
IFPB_TXD5
IFPB_TXD6_N
IFPB_TXD6
IFPB_TXD7_N
IFPB_TXD7
IFPA_TXC_N
IFPA_TXC
IFPB_TXC_N
IFPB_TXC
LVDS_L0N 17
LVDS_L0P 17
LVDS_L1N 17
LVDS_L1P 17
LVDS_L2N 17
LVDS_L2P 17
LVDS_LCLKN 17
LVDS_LCLKP 17
L4302
220Ohm/100Mhz
C4310 4.7UF/6.3V
C4312 4700PF/25V
C4313 470PF/50V
R4331 1KOhm
+LCD_VCC=1.8V
MAX:260mA
L4303
220Ohm/100Mhz
C4315 4.7UF/6.3V
C4318 4.7UF/6.3V
C4317 4700PF/25V
C4320 220PF/50V
C4316 1UF/6.3V
C4319 1UF/6.3V
F9J Pannel Support EDID pull hi is not necessary.
Design guide page 65.
U4000H
NC7
NC8
NC9
NC10
NC11
NC12
NC13
NC14
NC15
NC16
NC17
NC18
NC19
NC20
NC21
MIOAD0
MIOAD1
MIOAD2
MIOAD3
MIOAD4
MIOAD5
MIOAD6
MIOAD8
MIOAD9
MIOA_HSYNC
C4314 0.1UF/10V
T4310
T4311
T4312
T4313
R4325 2KOhm
R4326 2KOhm
MIOA_HSYNC
R4332 2KOhm
R4333 2KOhm
R4334 2KOhm
R4335 2KOhm
MIOAD0----PEX_PLL_EN_TERM
MIOAD1----SUB_VENDOR
MIOAD7-----TVMODE0
MIOAD10----TVMODE1
MIOAD2----USER0
MIOAD3----USER1
MIOAD4----USER2
MIOAD5----USER3
MIOAD6----GPIO_PADCFG0+
MIOAD8----GPIO_PADCFG1+
MIOAD9----GPIO_PADCFG2+
<Variant Name>
Title : G72MV--I/O (4)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9J
Rev 2.0
Date: Thursday, November 23, 2006
Sheet 43 of 63

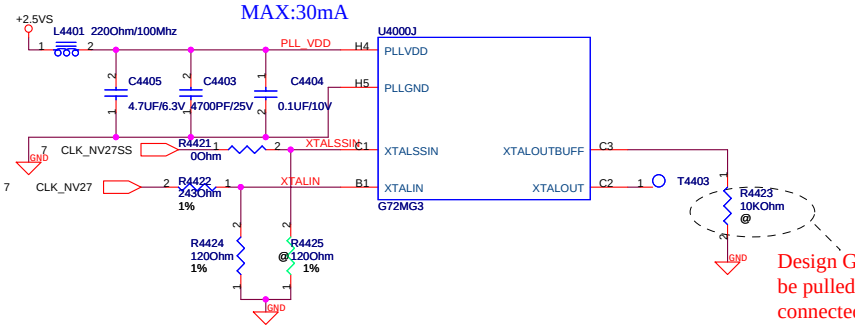


Design Guide Page84: On G72, IFPC_PLLVDD is internally connected to IFPAB_PLLVDD. The IFPC_PLLVDD ball is not connected on the substrate. No connection or filter is required.(V6,W7J:Mount 10Kohm)



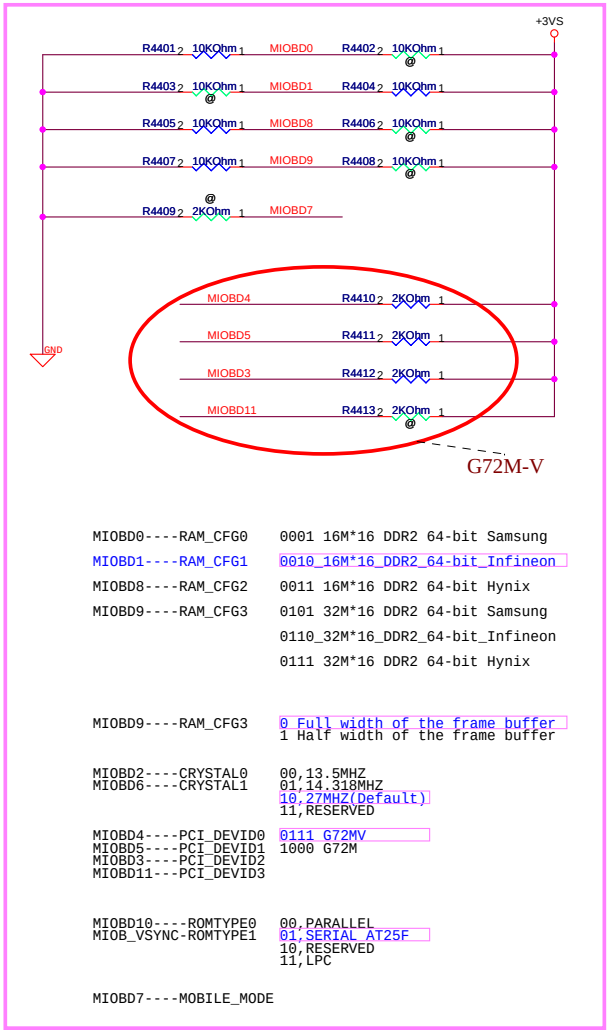
Design Guide Page80: IFPCD_RSET should be no stuff.(V6,W7J:no stuff)

Design Guide Page84: Suggest pull low 1K ohm(V6,W7J:10Kohm)

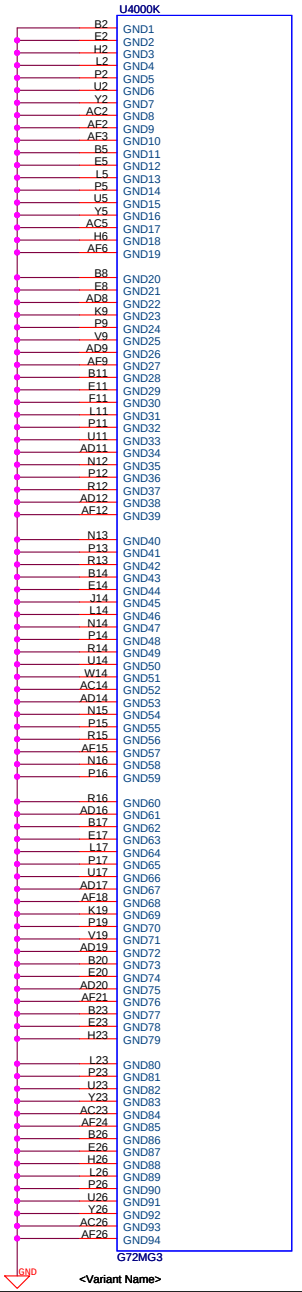


Design Guide Page63: The XTALOUTBUF signal should be pulled down using a 60 Ω resistor if it is not connected to an external device. (Check NV FAE)

STRAP




```
MIOBD0----RAM_CFG0    0001 16M*16 DDR2 64-bit Samsung
MIOBD1----RAM_CFG1    0010_16M*16_DDR2_64-bit_Infineon
MIOBD8----RAM_CFG2    0011 16M*16 DDR2 64-bit Hynix
MIOBD9----RAM_CFG3    0101 32M*16 DDR2 64-bit Samsung
                      0110_32M*16_DDR2_64-bit_Infineon
                      0111 32M*16 DDR2 64-bit Hynix


MIOBD9----RAM_CFG3    0 Full width of the frame buffer
                      1 Half width of the frame buffer


MIOBD2----CRYSTAL0    00,13.5MHZ
MIOBD6----CRYSTAL1    01,14.318MHZ
                      10,27MHZ(Default)
                      11,RESERVED

MIOBD4----PCI_DEVID0  0111 G72MV
MIOBD5----PCI_DEVID1  1000 G72M
MIOBD3----PCI_DEVID2
MIOBD11---PCI_DEVID3


MIOBD10----ROMTYPE0   00,PARALLEL
MIOB_VSYNC-ROMTYPE1   01,SERIAL_AT25F
                      10,RESERVED
                      11,LPC

MIOBD7----MOBILE_MODE
```



<Variant Name>

ASUSTeK COMPUTER INC

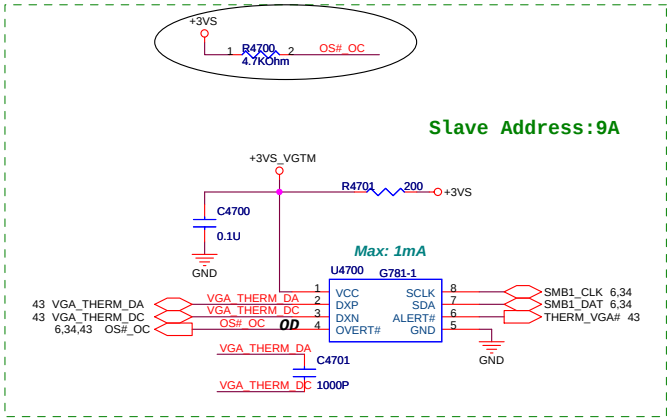
Title : G72MV--TMDS (5)

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

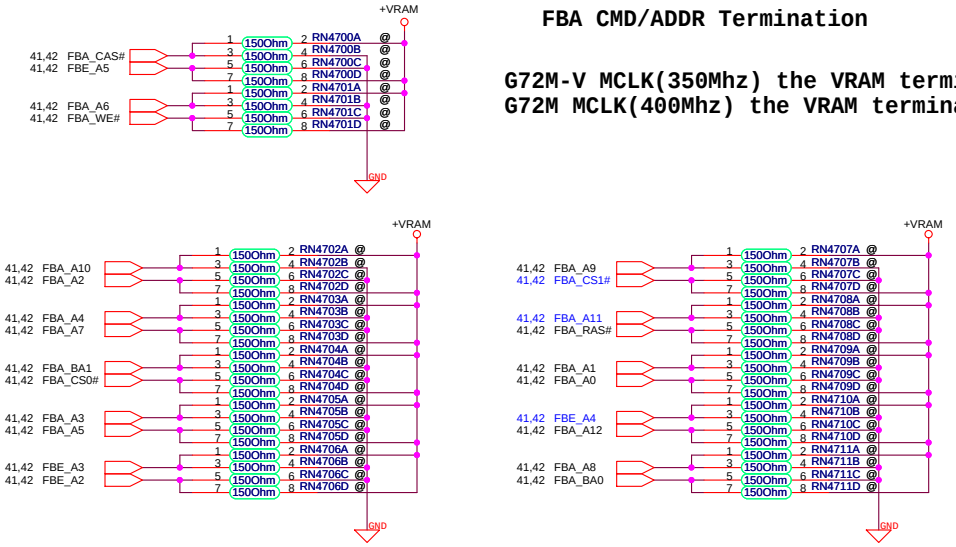
Date: Thursday, November 23, 2006 Sheet 44 of 63

OS#_OC connector to EC U3402(pin5) DNI R4700



FBA CMD/ADDR Termination

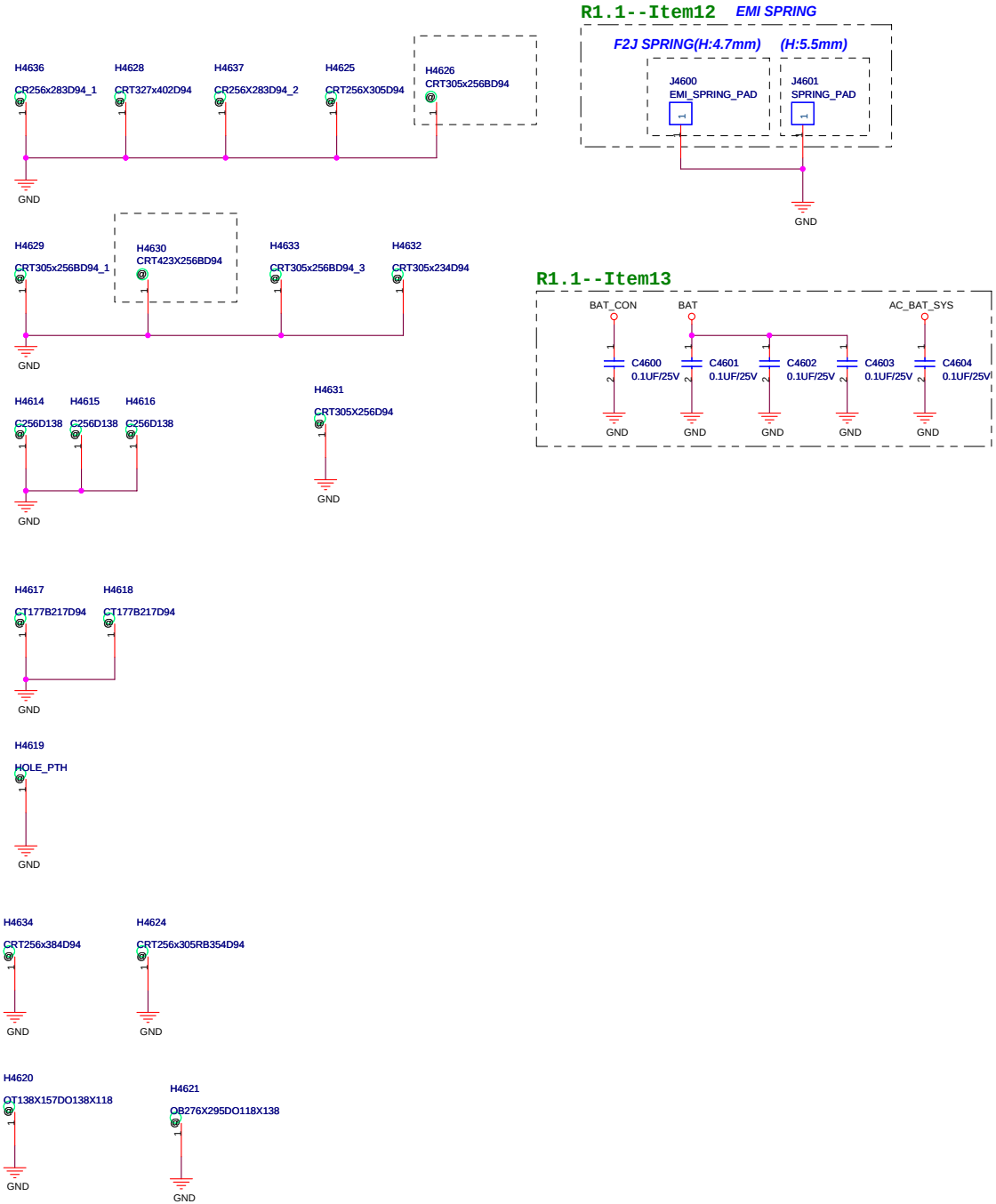
G72M-V MCLK(350Mhz) the VRAM termination is not necessary.
G72M MCLK(400Mhz) the VRAM termination is necessary.



CMD/ADDR termination resistors 150ohm. Design Guide Page47

<Variant Name>

ASUSTeK COMPUTER INC	Title G72MV--VRAM_TERM	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Thursday, November 23, 2006	Sheet 45 of 63	



<Variant Name>

ASUSTeK COMPUTER INC

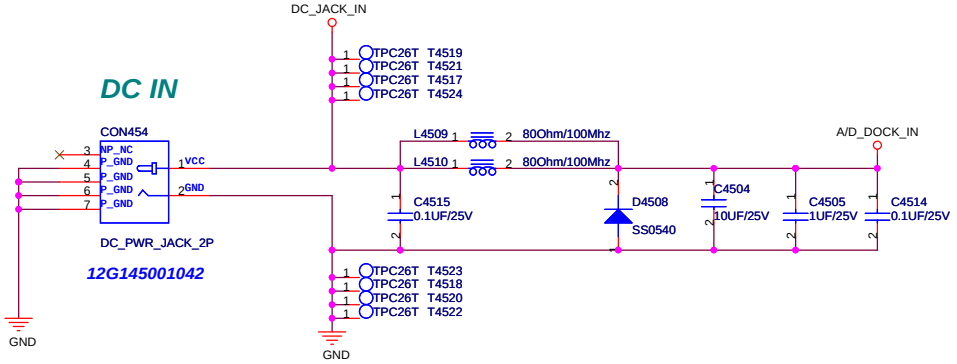
Title : HDD & CDROM

Engineer:

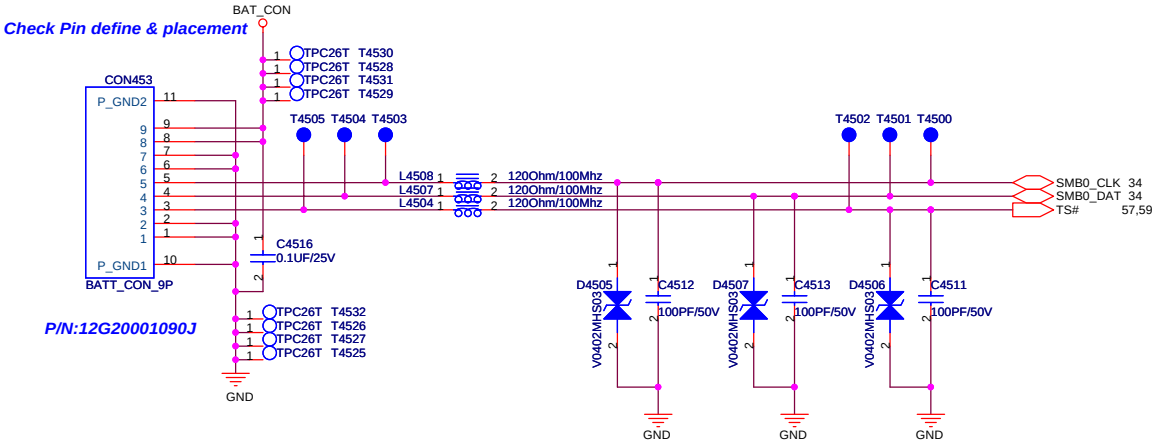
Size	Project Name	Rev
Custom	F9J	2.0

Date: Thursday, November 23, 2006 Sheet 46 of 63

DC IN



BAT IN



<Variant Name>

ASUSTeK COMPUTER INC

Title : G72M-Terminator

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: Thursday, November 23, 2006 Sheet 47 of 63

F9J SR_0928(R1.0---->R1.1)

(1)Change the s-vedio CON(CON182) to 12G14101107K for SMT issue.---page18.

(2)R1707 change from 10Kohm to 100Kohm to solve the LCD flash during warm boot.---Page17

(3)CON361(4 in 1) change to 12G340003800 to solve the factory yield rate issue.---Page36

(4)Add R2309 and R2310 for IDE select---Page 23

(5)Add C2512(10UF/10V) for FP power---Page 25

(6)Change R3904,R3905 and R3908 to 120 ohm, change R3906,R3907,R3909 and R2910 to 150 ohm to control LED current is about 10mA.---Page 39

(7)Del R3418, R3408,R617 and Q605,and add D3402 and D3403 for the OS#_OC function.---Page6; Page 34

(8)Reserved R2038 10K for GPIO10 pull high and R2039 10K for GPIO25 pull high.---Page 20

(9)Add NPTH H3301 & H3302 for New Card EJECTOR CON for ME request.---Page33

(10)Modify OS#_OC schematic: add R617 ; Q605 & reserved R3418.---Page6; Page34.

(11)Reserved R3808 0 ohm to support ALPS TP.---Page38

(12)Add J4600;J4601 EMI SPRING for EMI request.---Page46

(13)Change C2510 from 0.1u to 1uF for FP power.---Page25

(14)Reserved Change Cap C4600-C4604(0.1uF) for ESD issue of Buttom floating part ---Page46

(15)Mount voltage protector on D2503 for ESD issue of Finger printer.---Page25

(16)Mount 10uF capacitor on C534,C538,C533,C535,C536.---Page5

(17)Mount 600 ohm Bead on L1814,L1815,L1816 and 100P capacitor on C1839 ~C1844 for EMI issue of S-terminal.---Page18
(ER double check signal quality).

F9J ER_1102(R1.1---->R2.0)

(1) Update new CARD_EJECTOR_2P(CON332) footprint(add 2 npth hole) & remove 2 npth hole(H3301;H3302).---Page33

(2) Change the ODD CON(CON232) from 12G16121050P to 12G161240501 for ME request.(Board lock hole:1.8mm; 3.0H)---Page23

(3) Change the TV filter circuit. (Follow G72M design guide); this circuit can pass TV signal quality & EMI testing.---Page18

(4) Change R1816 & R1817 from 0ohm to 33ohm; mount cap 22pf on C1837 & C1838 for VSYNC/HSYNC.---Page18

(5) R753 & R755 change from 33ohm to 0ohm for CLK_PCIE_MINICARD#/CLK_PCIE_MINICARD signal quality.---Page7

(6)CON361 change from 12G340003800 to 12G340003810 to improve the yield rate.---Page36

(7)Add test point for factory request:
T1910(+RTCBAT);D1901 PIN2(T1911);+5V_USB(T2400);BAT_LL#(T3407);PWRSW#(R3801_2)(T3800);CHG_LED_UP(Q3901_3)(T3900);PWR_LED_UP(Q3904_3)(T3901).

(8)For CRT signal quality & EMI issue change the filter components:
a.L1811-L1813 change to 0.082uH
b.C1831;C1833;C1835 change from 15pF to 22pF.
c.C1832;C1834:C1836 change from 22pF to 2pF.
d.Add C4705;C4706;C4707 15pF.

(9)Change the card reader fuse(F3601) from 0.2A/30V to 0.5A/24V.(250mA_flash card + 77mA _ core logic)

(10)R1806,R1807 change to L1806;L1807(120 ohm bead) to improve the noise from CRT port for EMI request.

(11)C3658/C3655 change from 15pF to 18pF for card reader crystal adjustment.

(12)CCD polyswitch(F1701) change to 07G014050102(RAYCHEM 500mA).

<Variant Name>

ASUSTeK COMPUTER INC	Title : History(1)	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Thursday, November 23, 2006	Sheet 48 of 63	

<Variant Name>

Title : History(2)

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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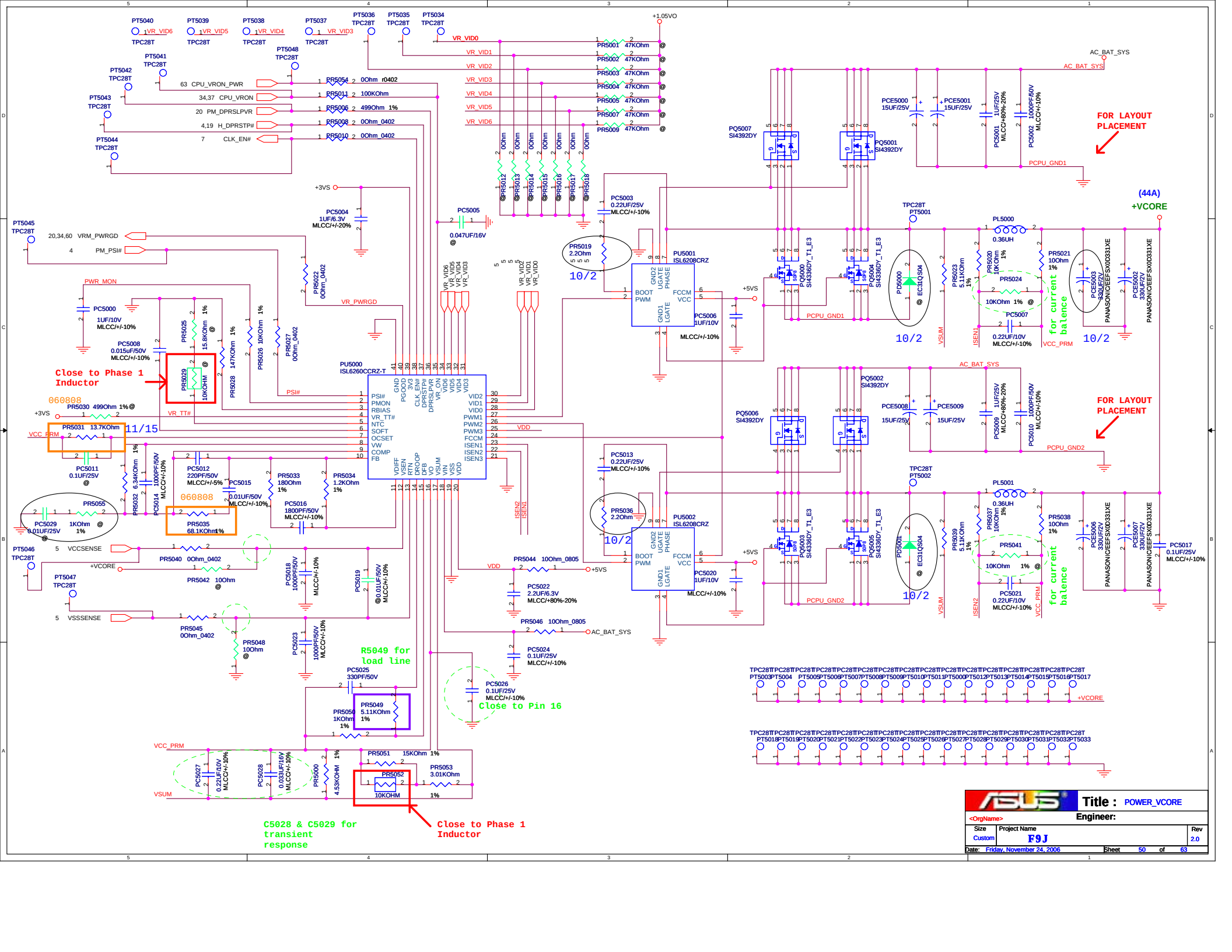
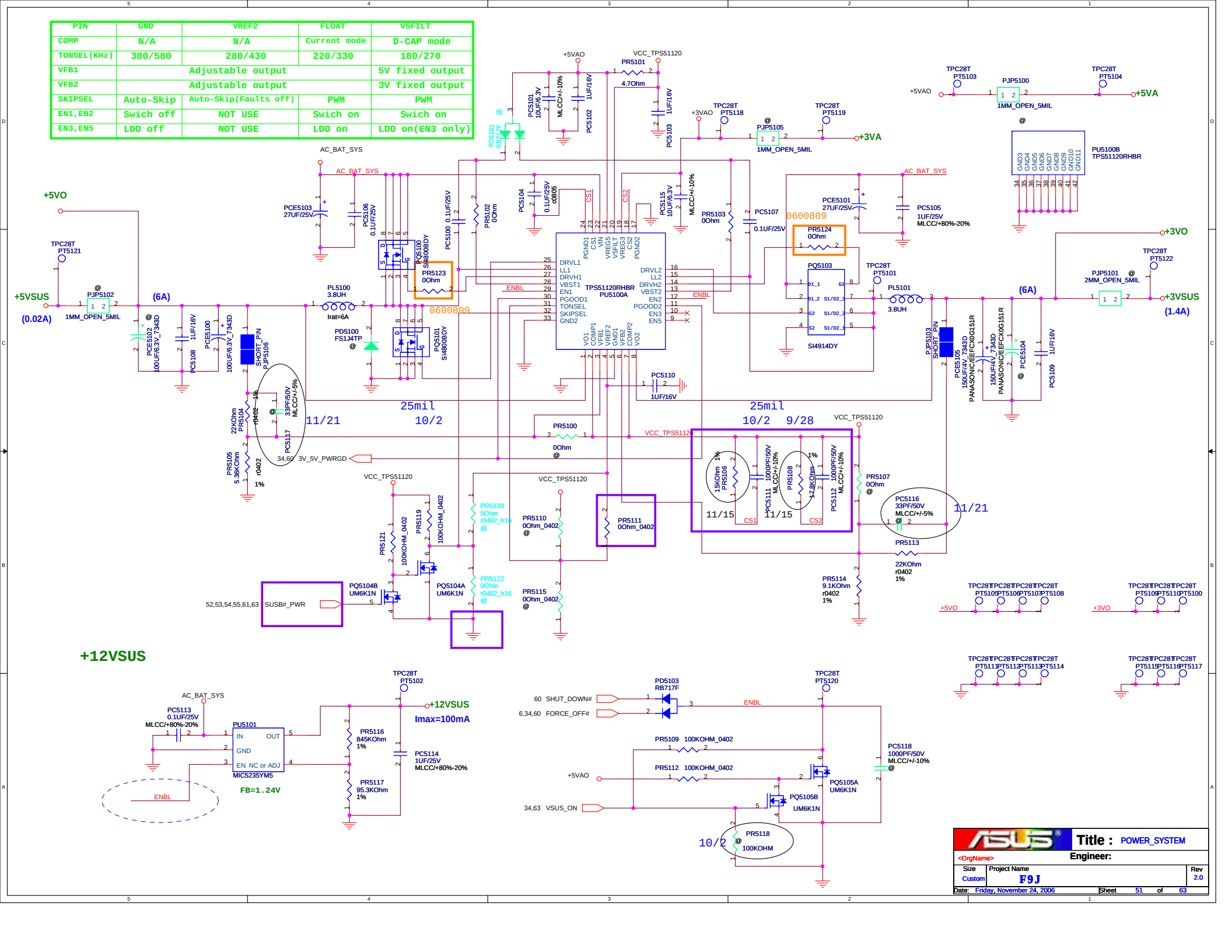
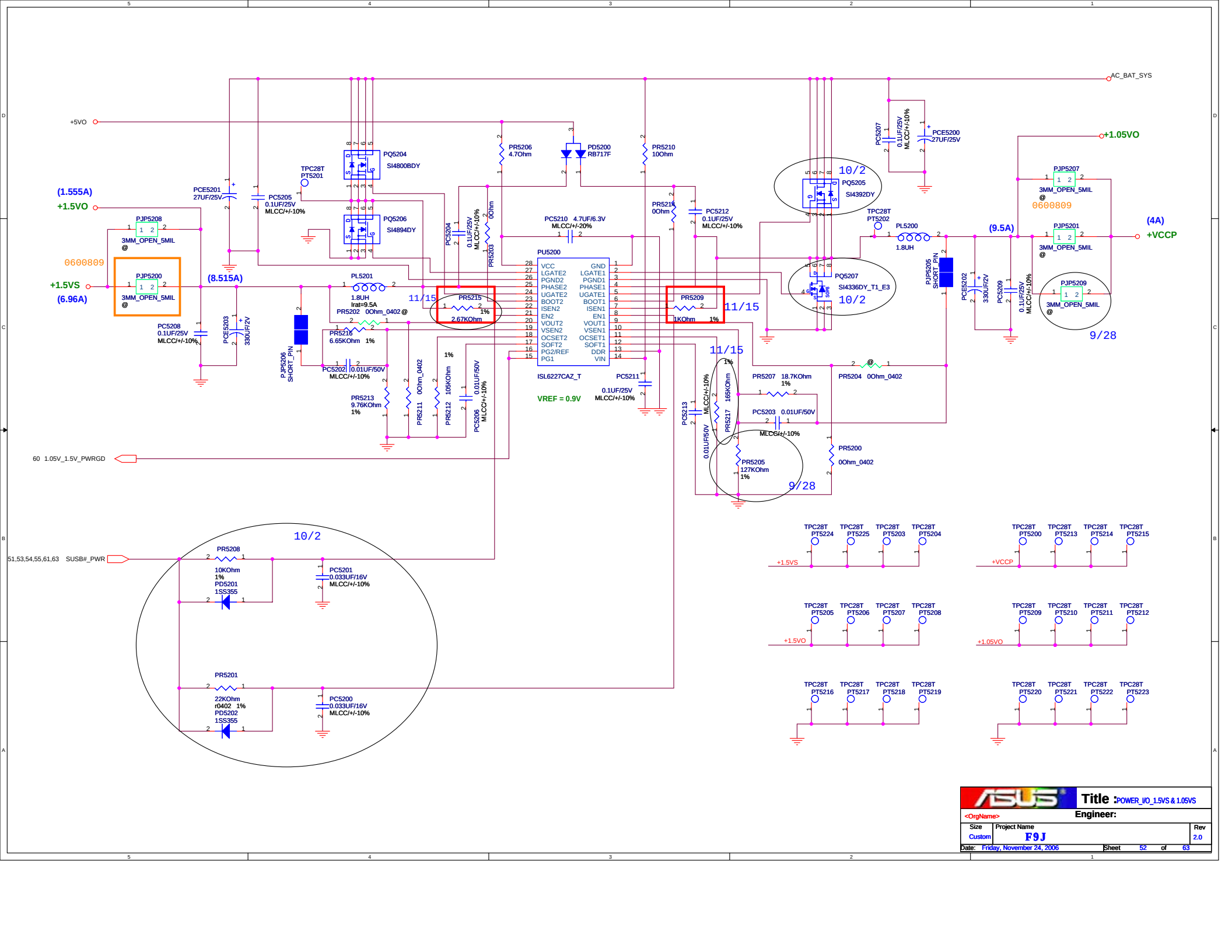

PU5000 ISL6260CCRZ-T
PU5001 ISL6208CRZ
PU5002 ISL6208CRZ
PQ5007 SI4392DY
PQ5001 SI4392DY
PQ5002 SI4392DY
PQ5006 SI4392DY
PQ5000 SI4336DY_T1_E3
PQ5004 SI4336DY_T1_E3
PQ5003 SI4336DY_T1_E3
PQ5005 SI4336DY_T1_E3
PD5000 @ EC31QS04
PD5001 @ EC31QS04
+1.05VO
+3VS
+5VS
+VCORE
AC_BAT_SYS
PCPU_GND1
PCPU_GND2
VCC_PRM
VSUM
VDD
PWR_MON
VRM_PWRGD
PM_PSI#
VR_TT#
CPU_VRON_PWR
CPU_VRON
DPRSLPVR
H_DPRSTP#
CLK_EN#
VCCSENSE
VSSSENSE
FOR LAYOUT PLACEMENT
for current balence
10/2
11/15
(44A)
+VCORE
Close to Phase 1 Inductor
Close to Pin 16
R5049 for load line
C5028 & C5029 for transient response
Close to Phase 1 Inductor
Title : POWER_VCORE
Engineer:
Project Name F9J
Rev 2.0
Date: Friday, November 24, 2006
Sheet 50 of 63

PIN	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current mode	D-CAP mode
TONSEL(KHz)	380/580	280/430	220/330	180/270
VFB1	Adjustable output			5V fixed output
VFB2	Adjustable output			3V fixed output
SKIPSEL	Auto-Skip	Auto-Skip(Faults off)	PWM	PWM
EN1,EN2	Swich off	NOT USE	Swich on	Swich on
EN3,EN5	LDO off	NOT USE	LDO on	LDO on(EN3 only)

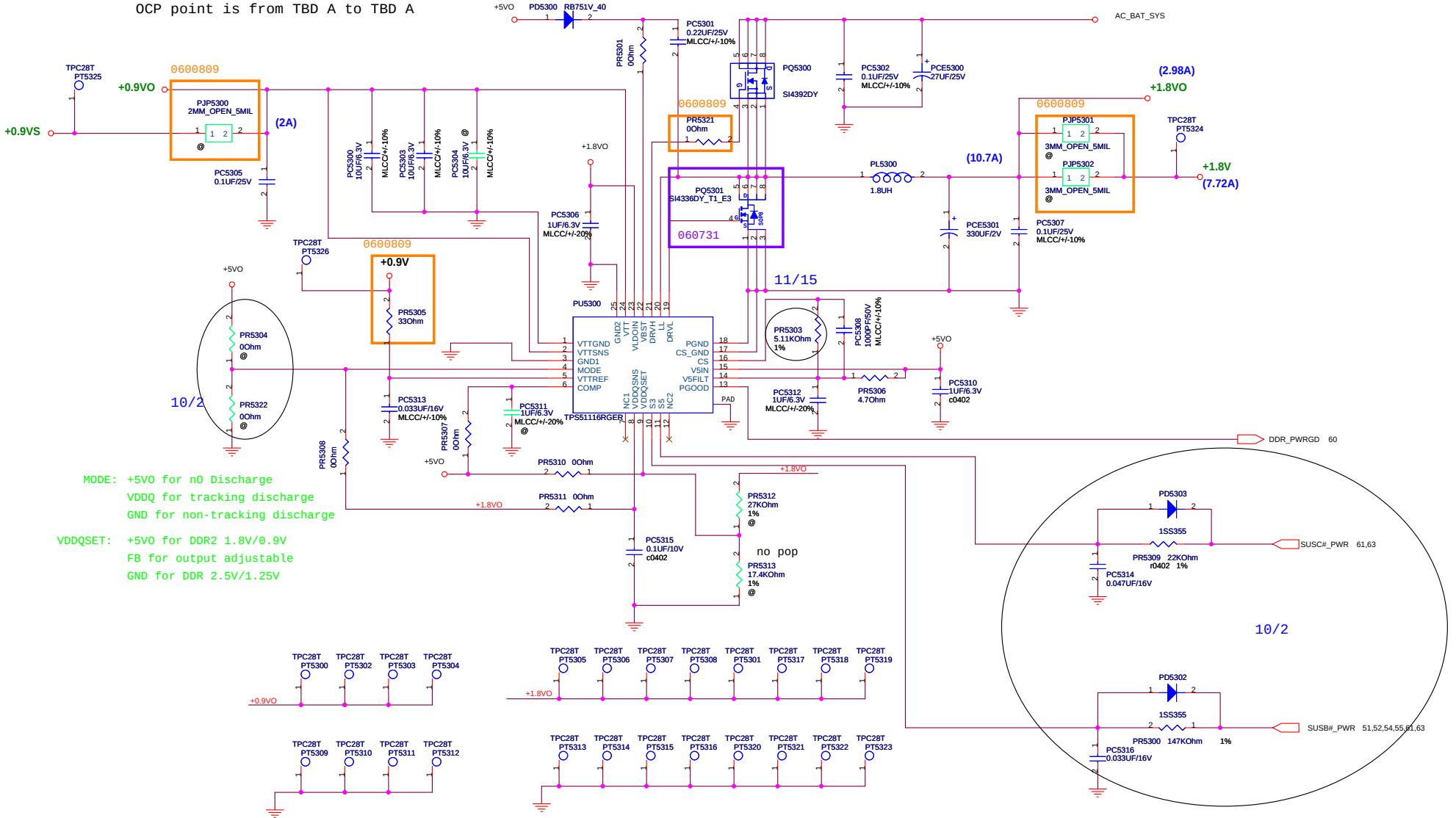




ASUS	Title : POWER_I/O_1.5VS & 1.05VS	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Friday, November 24, 2006	Sheet 52 of 63	

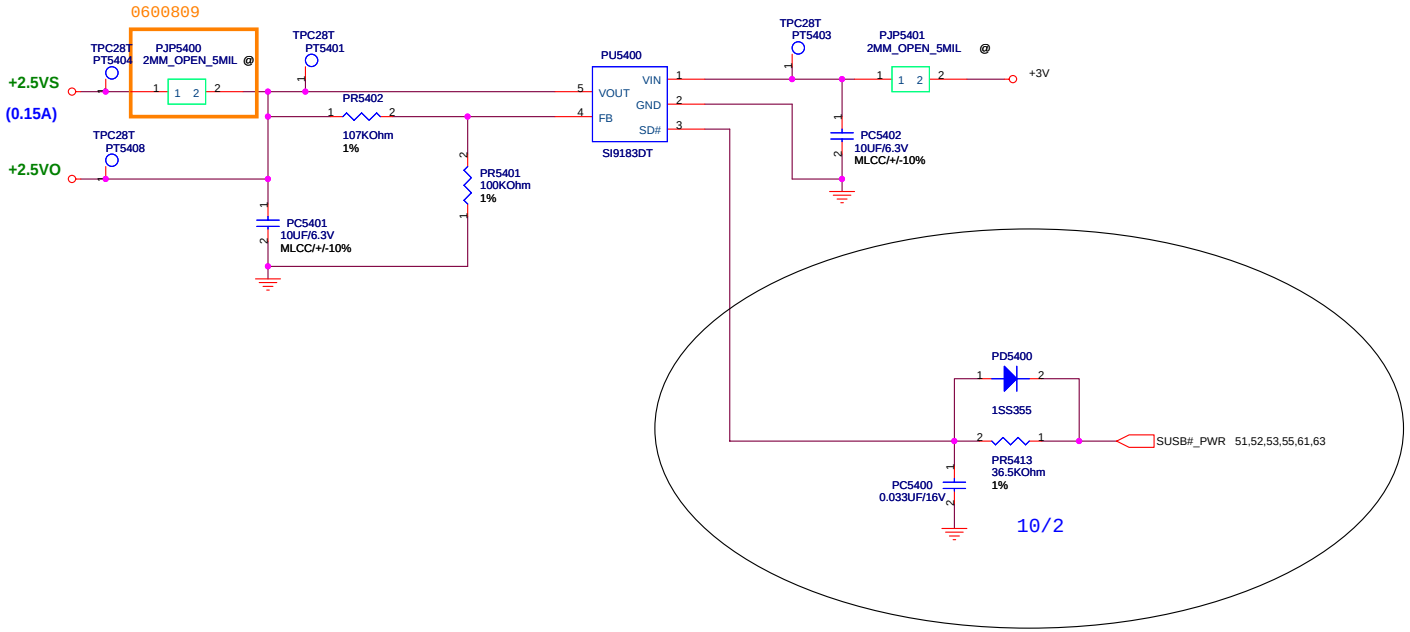
.9 Volt +/-5%.9 Volt +/-5%
Design Current:1.05A
Maximum current:1.5A
OCP point is from TBD A to TBD A

1.8Volt +/-5%
Design Current:7.3A
Maximum current:10.5A
OCP point is from TBD A to TBD A

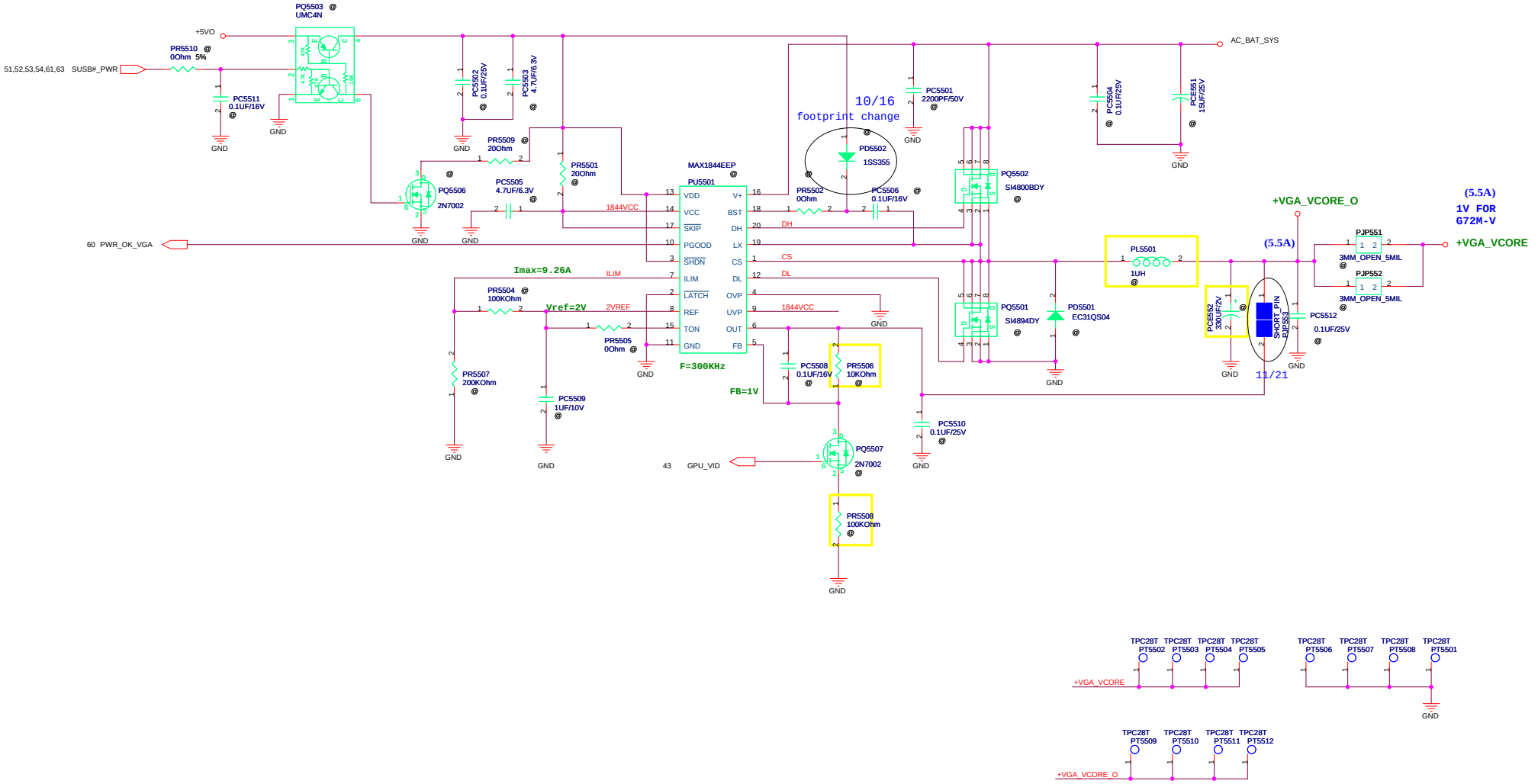


Title : POWER_I/O_DDR & VTT			
<OrgName>	Engineer:		
Size: Custom	Project Name: F9J		Rev: 2.0
Date: Friday, November 24, 2006	Sheet 53 of 63		

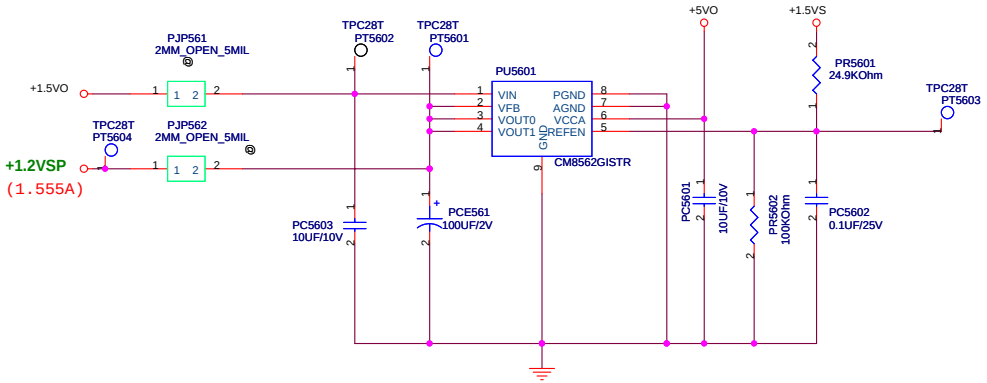
+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Friday, November 24, 2006	Sheet 54 of 63	

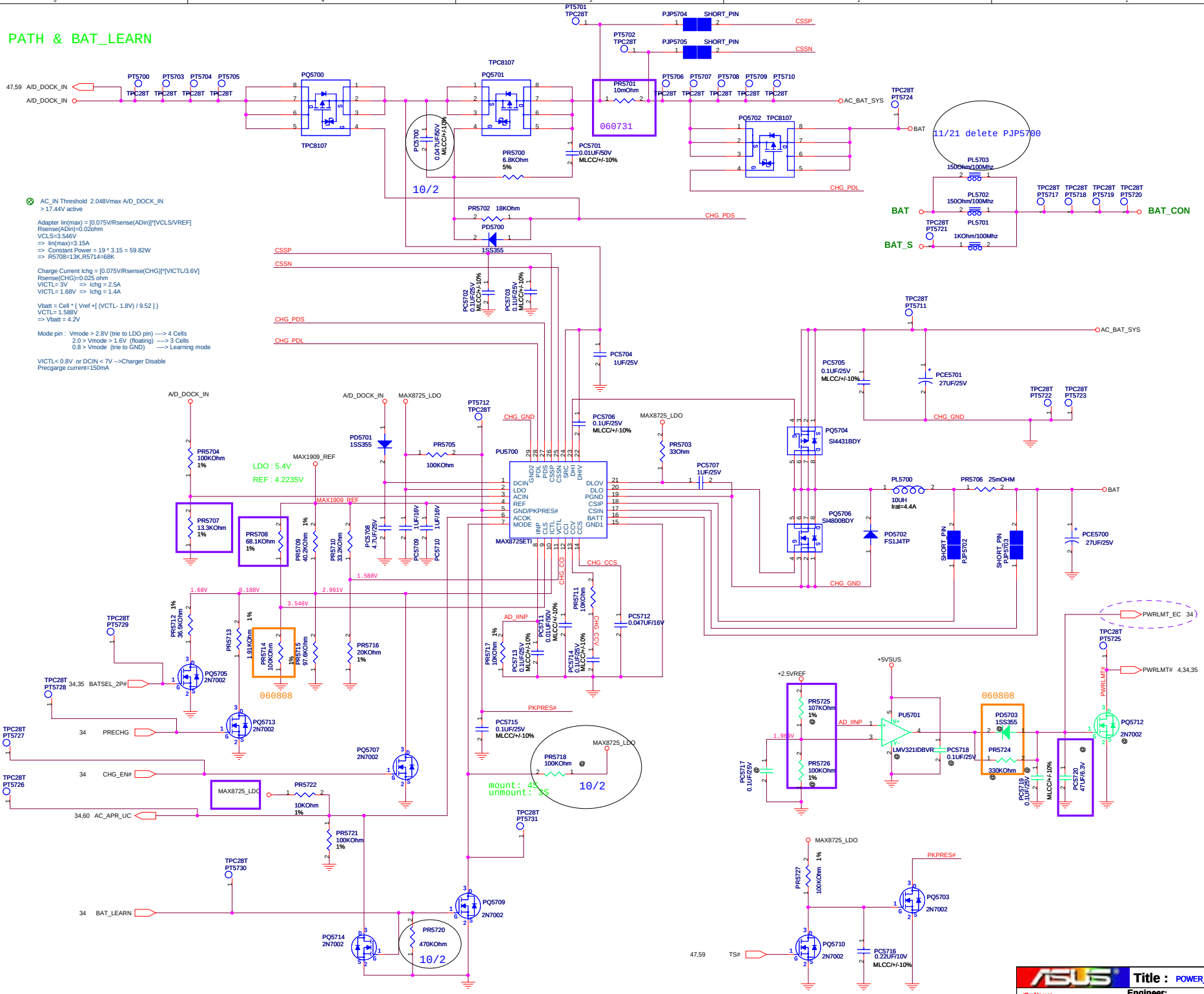


ASUS	Title : POWER_VGA_VCORE	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Friday, November 24, 2006	Sheet 55 of 63	



ASUS	Title : +1.2VSP	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Friday, November 24, 2006	Sheet 56 of 63	

POWER PATH & BAT_LEARN



ASUS	Title : POWER_CHARGER		
<OrgName>	Engineer:		
Size: Custom	Project Name: F9J		Rev: 2.0
Date: Friday, November 24, 2006	Sheet 57 of 63		

Title : POWER_PIC

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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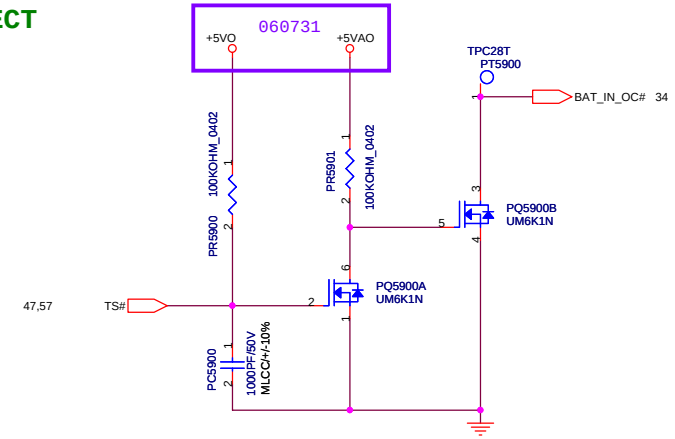
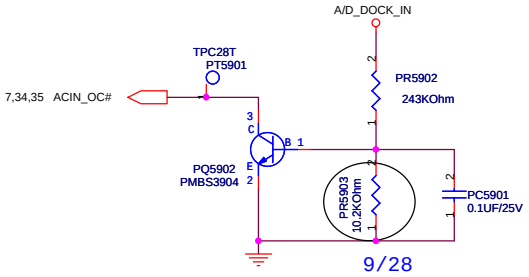
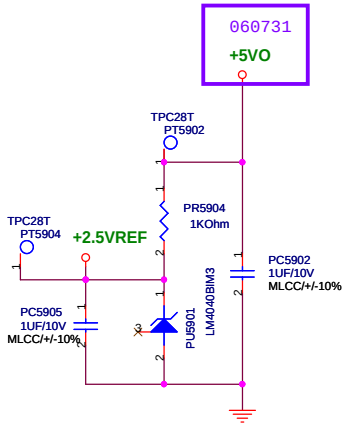
BATTERY IN DETECT



ADAPTER IN DETECT

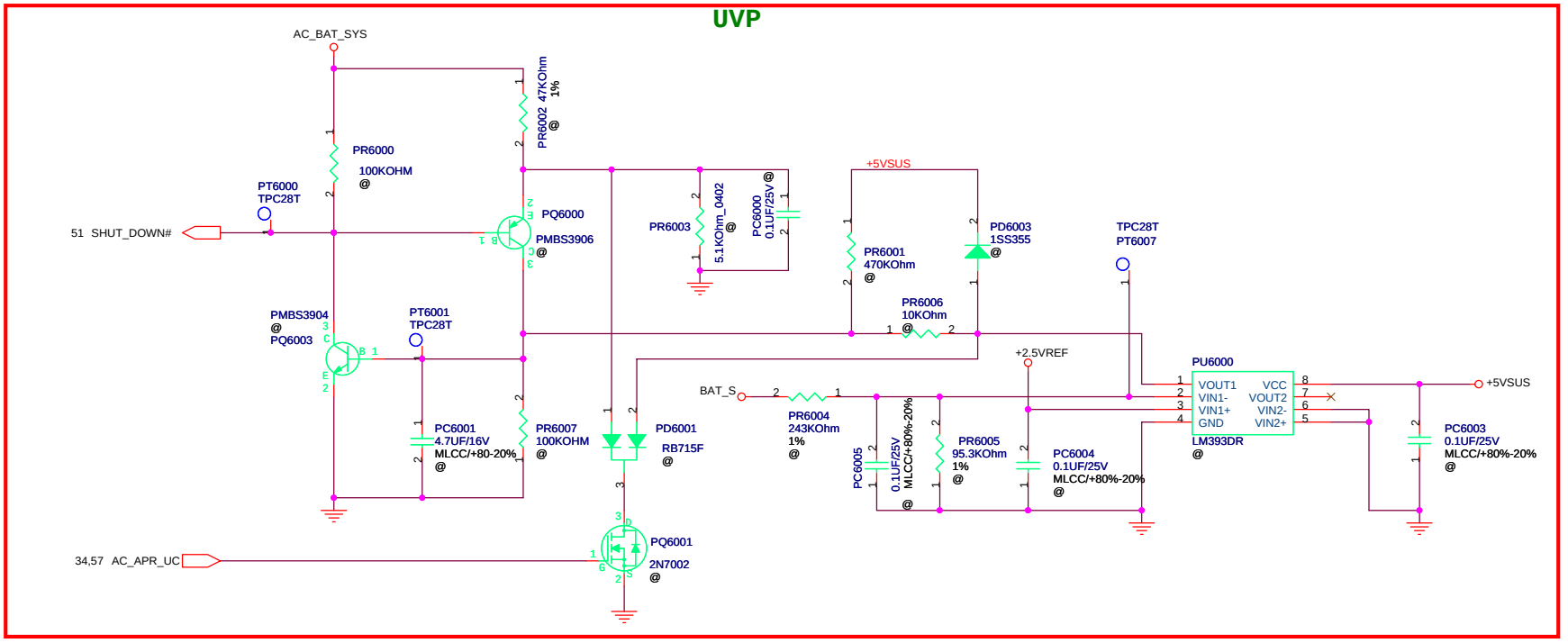


+5VLCM, +5VCHG & +2.5VREF

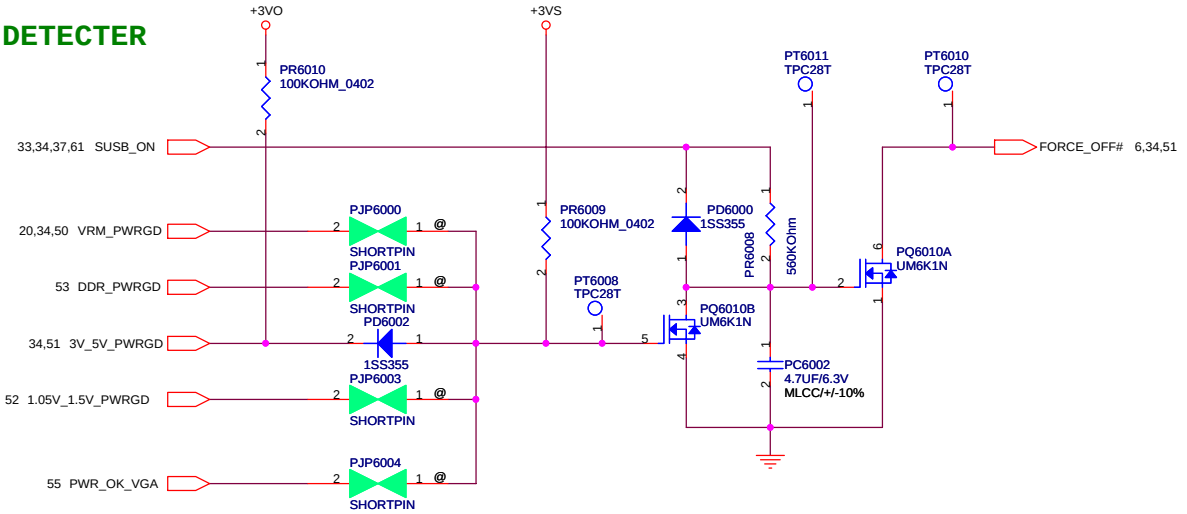


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Friday, November 24, 2006	Sheet 59 of 63	

UVP



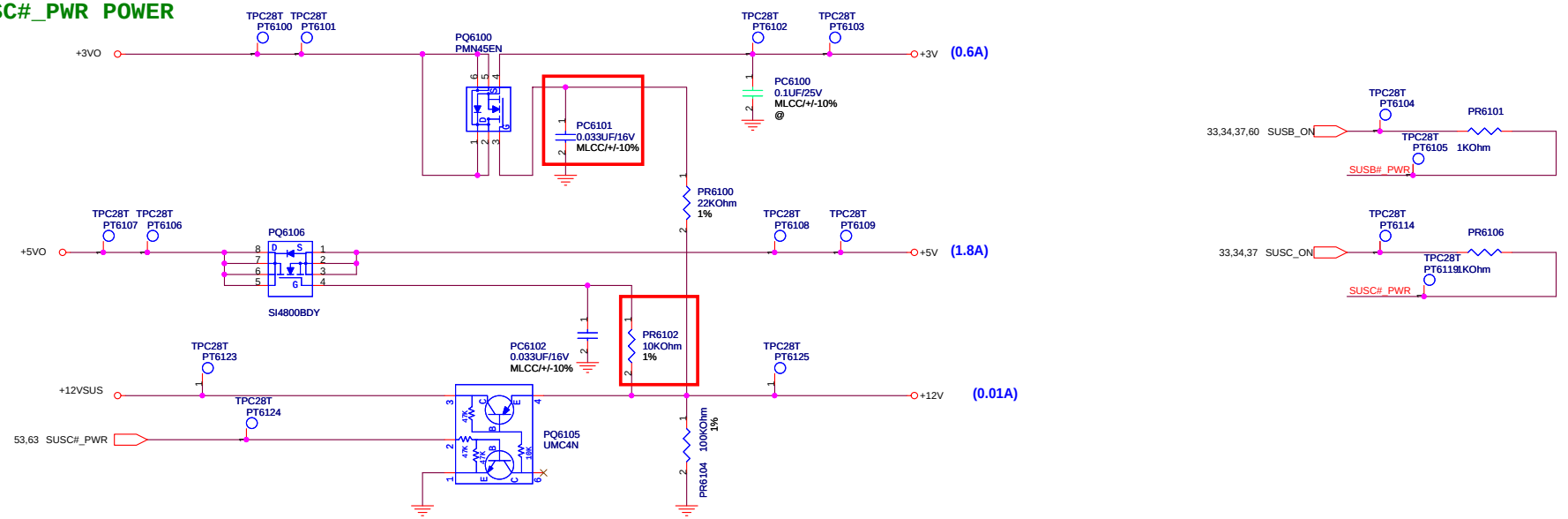
POWER GOOD DETECTER



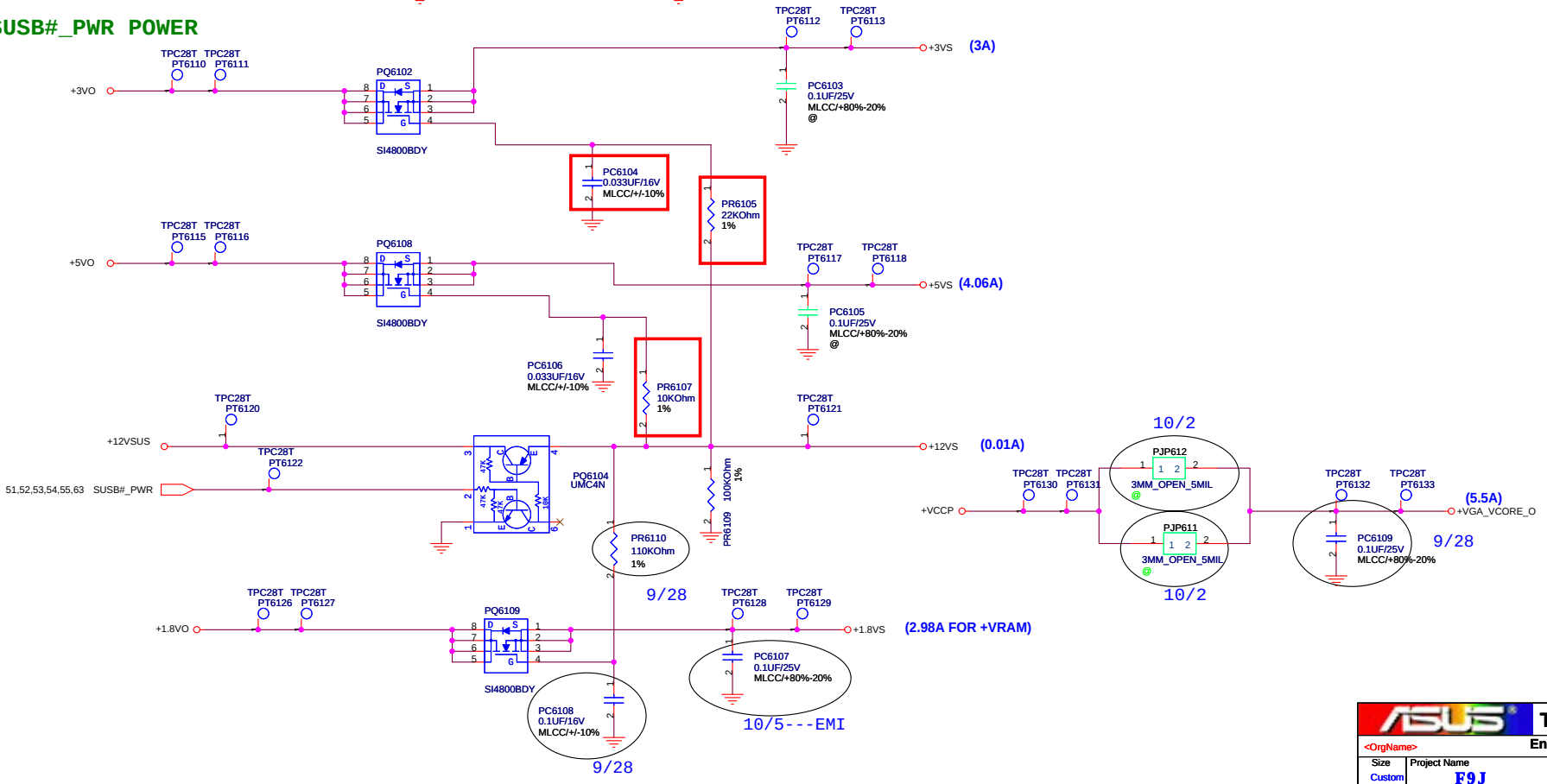
TPC28T	PT6003	VRM_PWRGD
TPC28T	PT6004	DDR_PWRGD
TPC28T	PT6005	3V_5V_PWRGD
TPC28T	PT6006	1.05V_1.5V_PWRGD
TPC28T	PT6009	PWR_OK_VGA

ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Friday, November 24, 2006	Sheet 60 of 63	

SUSC#_PWR POWER

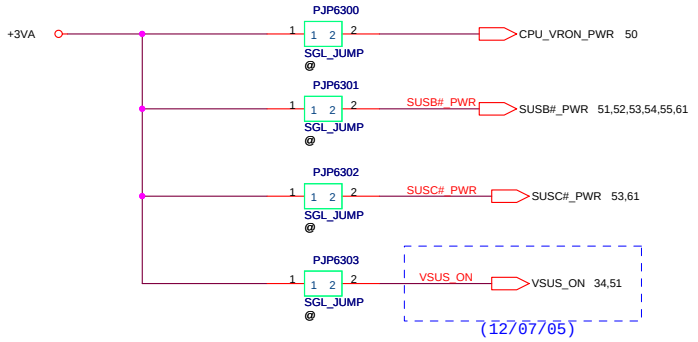


SUSB#_PWR POWER

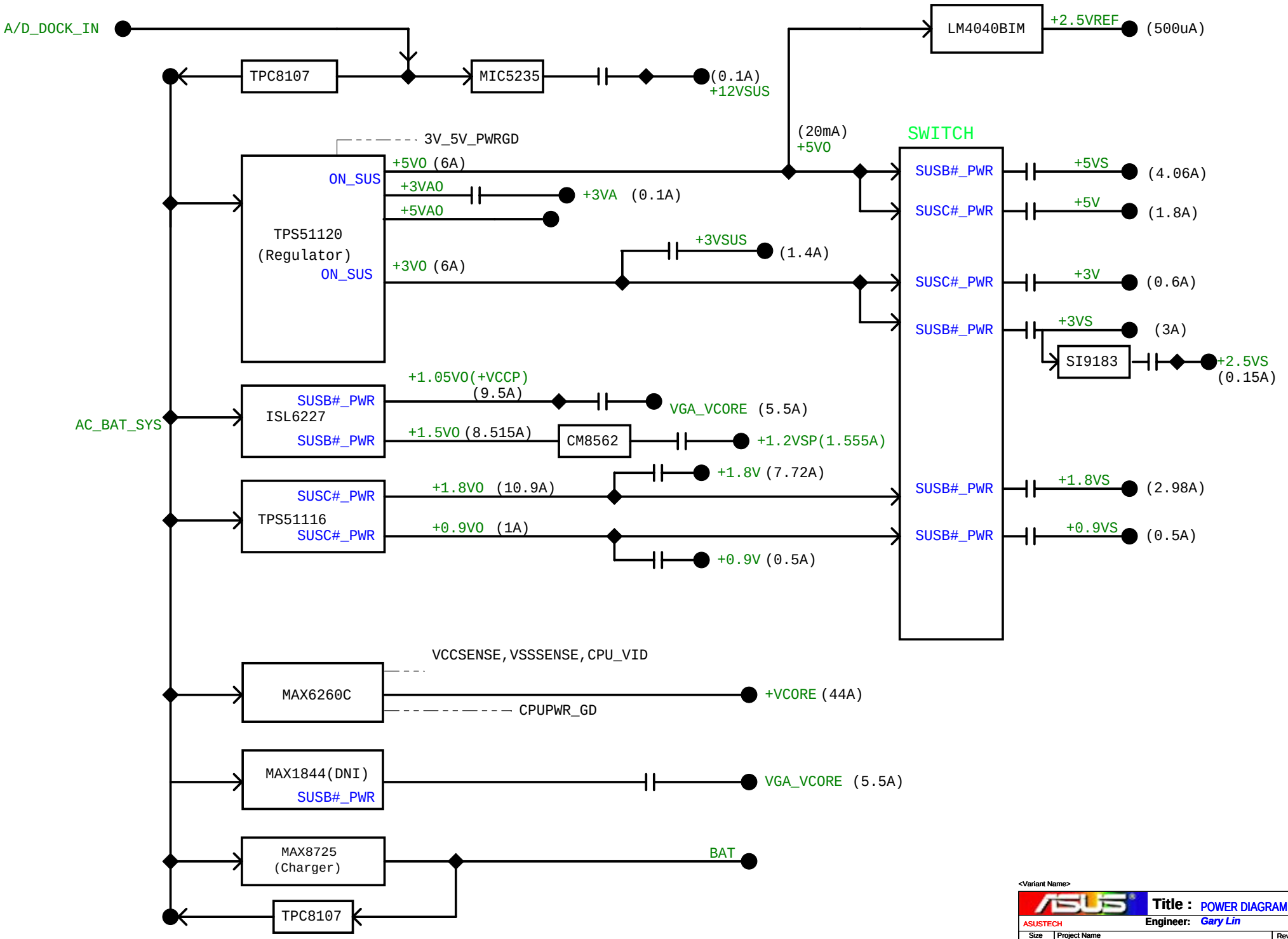


ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Friday, November 24, 2006	Sheet 61 of 63	

FOR POWER TEST



ASUS	Title : POWER_SIGNAL	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: Friday, November 24, 2006	Sheet 63 of 63	



<Variant Name>

ASUSTECH

Title : POWER DIAGRAM

Engineer: Gary Lin

Size	Project Name	Rev
Custom	F9J	2.0

Date: Friday, November 24, 2006 Sheet 74 of 74