F9S SCHEMATIC Revision 1.3

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SYSTEM PAGE REF.

POWER PAGE REF.

<Variant Name>

ASUSTeK COMPUTER INC

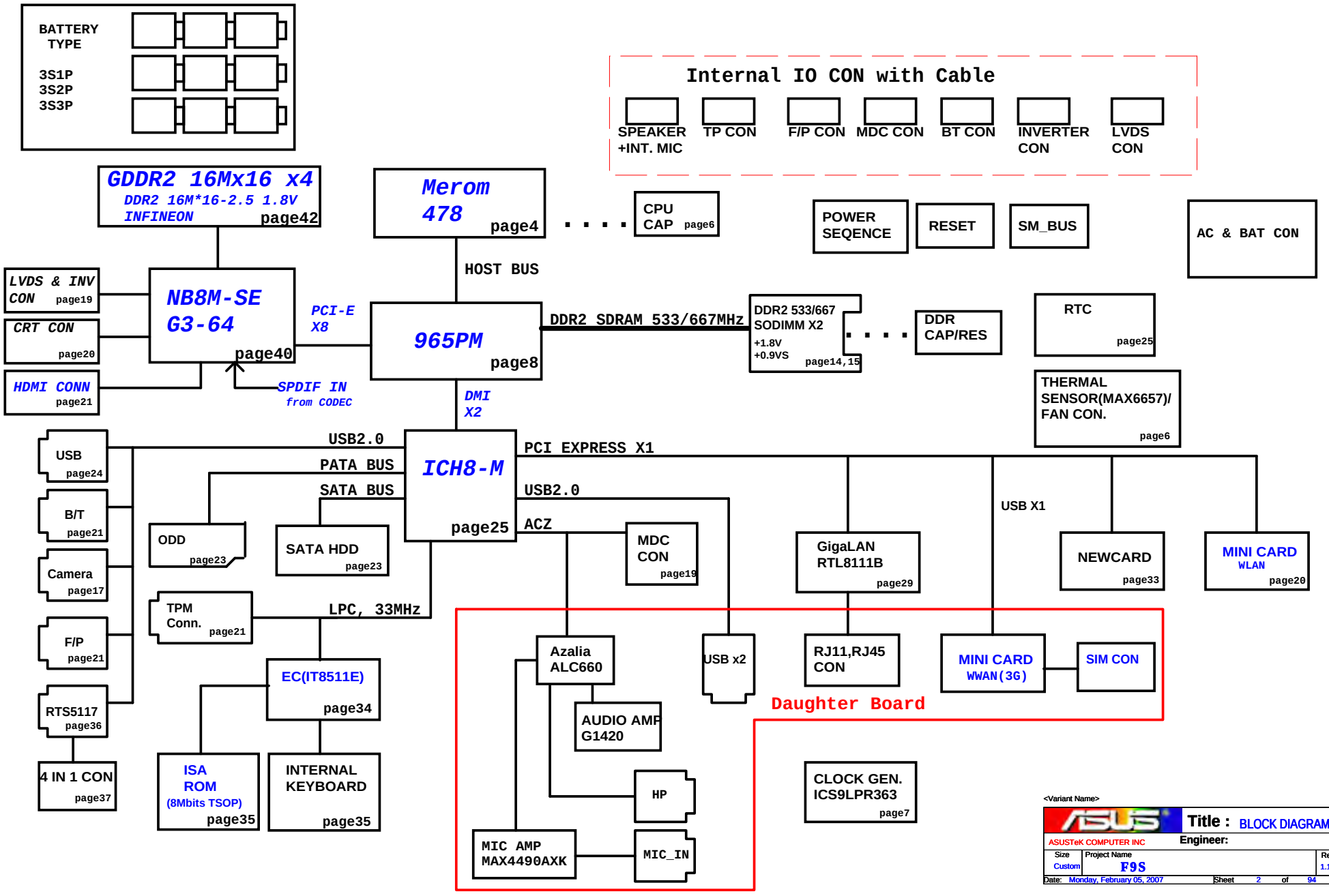
Title : PAGE REF.

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Thursday, February 15, 2007 Sheet 1 of 94

F9S BLOCK DIAGRAM



<Variant Name>

Title : BLOCK DIAGRAM

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Monday, February 05, 2007 Sheet 2 of 94

EC-IT8511 GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	LCD_BL_PWM	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	BAT1_CNT1#	I
37	PWM3/GPA3	BAT2_CNT1#	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	O
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	N/A	
169	SMCLK1/GPC1	SMB1_CLK	O
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	PWRLIMIT#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	RF_ON_SW#	O
42	GINT/GPD5	PM_SLP_M#	O
62	TACH0/GPD6	FAN0_TACH	
63	TACH1/GPD7	COLOREN#	I
87	ADC4/GPE0	BLUETOOTH#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	BAT2_IN_OC#	I
24	LPCPD#/WUI6/GPE6	WLAN_SW#	I
25	CLKRUN#/WUI7/GPE7	ME_ALERT#	
110	PS2CLK0/GPF0	NC/PS2CLK0	O
111	PS2DAT0/GPF1	NC/PS2DAT0	I/0
114	PS2CLK1/GPF2	DVD/CD_ON#	I
115	PS2DAT1/GPF3	TV_ON#	I
116	PS2CLK2/GPF4	TP_CLK	O
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	SLOT_ON# ??	I
119	PS2DAT3/GPF7	INSTANT_ON#	I
113	FA16/GPG0	FA16_SWAP	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	FA19 BAT2_IN_OC#	O
3	FA20/GPG4	LID_EC#	I
4	FA21/GPG5	BAT2_IN_OC#	I
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD	I
55	GPH2	CPUPWR_GD	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC0#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH8_PWROK	O
149	GPI1	ALL_SYS_PWRGD	I
152	GPI2	BAT1_CNT2#	O
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	EC_CLK_EN	O
174	GPI6	BAT_LEARN	O

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(MAX6657)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

ICH8M_GPIO

Pin.	Default	RST#	Use As	Signal Name	Power	Mux
GPIO 00	i		GPI	PM_BMBUSY#	+3VS	BM_BUSY#
GPIO 01	i	0	GPI	BT_DET#	+3VS	TACH1
GPIO [5:2]	i	H-Z	GPI	PCI_INT[H:E]#	+3VS	PIRQ[H:E]#
GPIO 06	i	0	GPO	BIOS_REC_?_(TP)	+3VS	TACH2
GPIO 07	i	0	GPO	802_LED_EN	+3VS	TACH3
GPIO 08	i		GPI	EXTSMI#	+3VSUS	N/A
GPIO 09	i	H-Z	GPO	LAN_WOL_EN_?_(TP)	+3VSUS	WOL_EN
GPIO 10	i	H-Z	GPO	RST#_NEWCARD	+3VSUS	ALERT#
GPIO 11	Nat.	H-Z	Native	SMB_ALERT#	+3VSUS	SMBALERT#
GPIO 12	i		GPI	KBC_SCI#	+3VSUS	GLAN_DOCK#
GPIO 13	Nat.		GPI	N/A	+3VSUS	ENERGY_DETECT
GPIO 14	i	H-Z	GPI	N/A	+3VSUS	NETDETECT
GPIO 15	Nat.	1	Native	STP_PCI#	+3VSUS	STP_PCI# , No-GPIO, in Mobile
GPIO 16	Nat.	0	Native	PM_DPRSLPVR	+3VS	DPRSLPVR
GPIO 17	i	1	GPO	WLAN_ON#	+3VS	TACH0
GPIO 18	O	freq 1K	GPO	N/A	+3VS	N/A
GPIO 19	i		GPO	CPU_SELECT	+3VS	SATA1GP
GPIO 20	O	1	GPO	BT_LED_EN	+3VS	N/A
GPIO 21	i		GPI	CPPE#_DET	+3VS	SATA0GP
GPIO 22	i		GPI	N/A	+3VS	SCLOCK
GPIO 23	Nat.		Native	N/A	+3VS	LDRQ1#
GPIO 24	O	H-Z	GPO	MSK_PCIRST	+3VSUS	CLGPIO0(MEM_LED), Not Cleared by CF9h RST event.
GPIO 25	Nat.	1	Native	STP_CPU#	+3VS	STP_CPU# , No-GPIO, in Mobile
GPIO 26	Nat.		GPO	CPPE_EN	+3VSUS	S4_STATE#
GPIO 27	O	0	GPO	BT_ON#	+3VSUS	QRT_STATE0
GPIO 28	O	0	GPO	CB_SD#_?_(TP)	+3VSUS	QRT_STATE1
GPIO 29	Nat.		Native	USB_OC#5	+3VSUS	OC5#
GPIO 30	Nat.		Native	USB_OC#6	+3VSUS	OC6#
GPIO 31	Nat.		Native	USB_OC#7	+3VSUS	OC7#
GPIO 32	O	0	Native	PM_CLKRUN#	+3VS	CLKRUN# , No-GPIO, in Mobile
GPIO 33	O	1	GPO	N/A	+3VS	HDA_DOCK_EN#
GPIO 34	O	0	GPO	N/A	+3VS	HDA_DOCK_RST#
GPIO 35	O	0	GPO	SATACLKREQ#_?_(TP)	+3VS	SATACLKREQ#
GPIO 36	i		GPO	EMAIL_LED#_?_(TP)	+3VS	SATA2GP
GPIO 37	i	0	GPI	PCB_ID0	+3VS	SATA3GP
GPIO 38	i		GPI	PCB_ID1	+3VS	SLOAD

Pin	Default	RST#	Use As	Signal Name	Power	Mux
GPIO 39	i		GPI	PCB_ID2	+3VS	SDATAOUT0
GPIO [40:43]	Nat.		Native	USB_OC[4:1]#	+3VSUS	OC[4:1]#
GPIO [47:44]	n/a		N/A	N/A	N/A	No implement
GPIO 48	i	1	Native		+3VS	SDATAOUT1
GPIO 49	Nat.		Native	H_PWRGD	+VCORE	CPUPWRGD
GPIO 50	Nat.		Native	PCI_REQ1#	+5VS	REQ1#
GPIO 51	Nat.	1	Native	PCI_GNT1#	+3VS	GNT1#
GPIO 52	Nat.		Native	PCI_REQ2#	+5VS	REQ2#
GPIO 53	Nat.	1	Native	PCI_GNT2#	+3VS	GNT2#
GPIO 54	Nat.		Native	PCI_REQ3#	+5VS	REQ3#
GPIO 55	Nat.	1	Native	PCI_GNT3#	+3VS	GNT3#

<Variant Name>

ASUSTeK COMPUTER INC

Title : Schematic Info.

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

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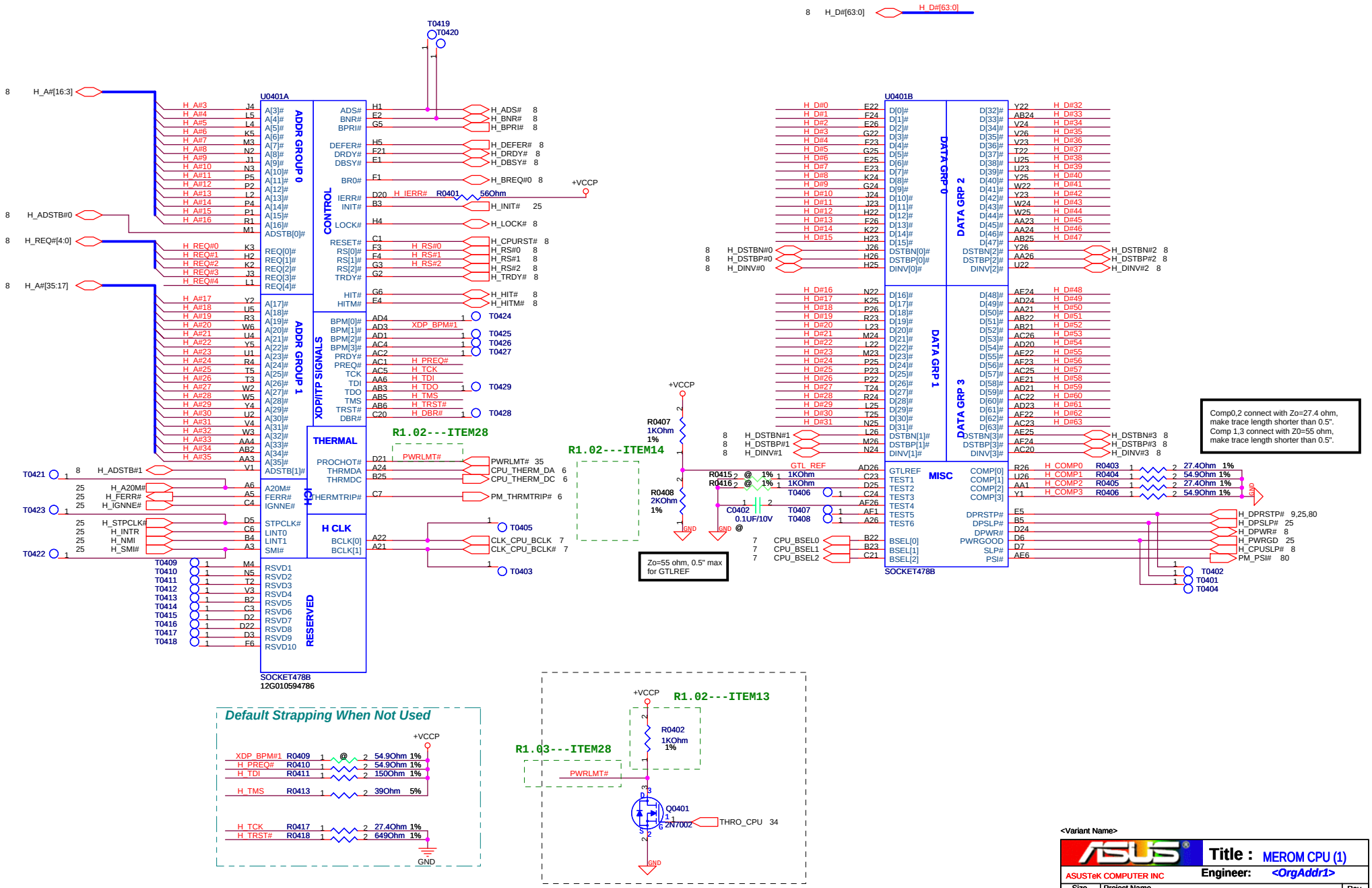

<Variant Name>

ASUSTeK COMPUTER INC

Title : MEROM CPU (1)

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

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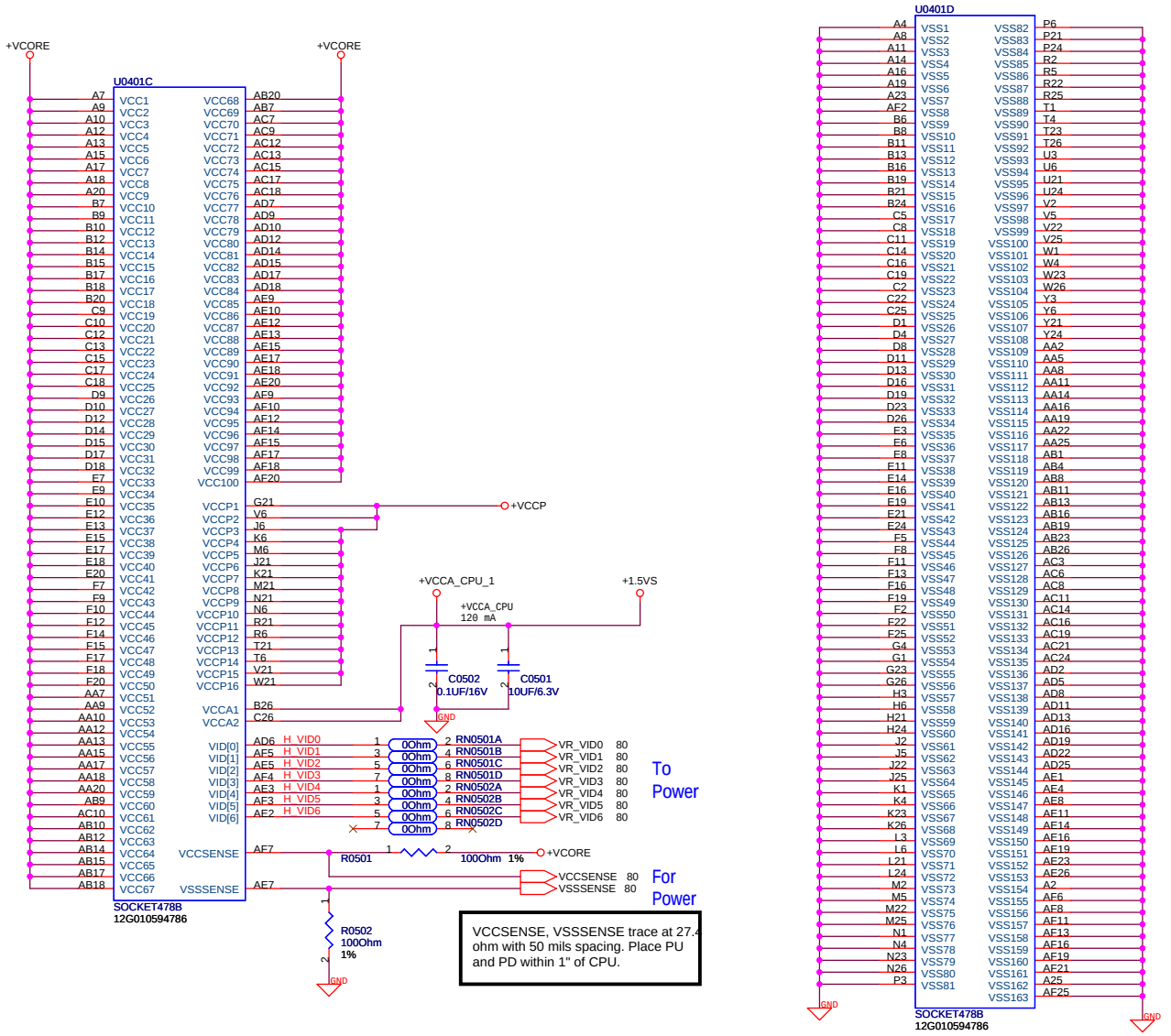

<Variant Name>

ASUSTeK COMPUTER INC

Title : MEROM CPU (2)

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

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+VCCP 4,5,7,8,9,11,12,28,37,85
+VCORE 5,37,80
+3VS 7,9,12,13,14,15,17,18,19,20,21,22,23,25,27,28,29,33,34,37,39,40,43,44,45,80,91,92
+5VA 81

Place on L1/L8, upper/lower side of inside socket. according intel layout suggestion.

44A for Merom

+VCORE

C0614 10UF/6.3V, C0632 10UF/6.3V, C0621 10UF/6.3V, C0603 10UF/6.3V, C0625 10UF/6.3V, C0609 10UF/6.3V, C0631 10UF/6.3V, C0604 10UF/6.3V, C0622 10UF/6.3V, C0629 10UF/6.3V

C0627 10UF/6.3V, C0620 10UF/6.3V, C0626 10UF/6.3V, C0607 10UF/6.3V, C0624 10UF/6.3V, C0605 10UF/6.3V, C0623 10UF/6.3V, C0601 10UF/6.3V, C0615 10UF/6.3V, C0602 10UF/6.3V

C0616 10UF/6.3V, C0639 10UF/6.3V, C0619 10UF/6.3V, C0610 10UF/6.3V, C0613 10UF/6.3V, C0608 10UF/6.3V, C0612 10UF/6.3V, C0617 10UF/6.3V, C0628 10UF/6.3V, C0630 10UF/6.3V

C0611 10UF/6.3V, C0633 10UF/6.3V

GND

+VCCP Decoupling Capacitor (Place near CPU)

+VCCP

CE0601 150UF/4V, C0618 0.1UF/16V X7R, C0606 0.1UF/16V X7R, C0636 0.1UF/16V X7R, C0635 0.1UF/16V X7R, C0638 0.1UF/16V X7R, C0637 0.1UF/16V X7R

GND

Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

Optimize it !_0907

Sub-SYS=CPU CAP

R0651 0Ohm ICH_THRMTRIP# 25

+VCCP, +3VS

R0652 330, C0650 0.1U, GND, R0654 10KOhm

Enable: Turn OFF system
To EC(Internal Pull Hi)

4 PM_THRMTRIP#
9 GMCH_THRMTRIP# R0655 0Ohm
9,23,26,40 PLT_RST#

Q0650 PMBS3904

Q0651 H2N7002

THRMTRIP# 34

To EC

Thermal Sensor

+3VS

SMB1_CLK 1 R0658 2 4.7KOhm
SMB1_DAT 1 R0657 2 4.7KOhm
THRM_ALERT#_CPU 1 R0650 2 10KOhm

+3VS_THM

R0656 200 +3VS

C0652 0.1U

Max: 1mA

U0650 MAX6657MSA

1	VCC	SCLK	8
2	DXP	SDA	7
3	DXN	ALERT#	6
4	OVERT#	GND	5

SMB1_CLK SMB1_DAT THRM_ALERT#_CPU

SMB1_CLK 34,40,45
SMB1_DAT 34,44,45

T0601

4 CPU_THERM_DA
4 CPU_THERM_DC

CPU_THERM_DA C0651 1000P CPU_THERM_DC

OS#_OC OS#_OC 34,43,45

Close to Pin A24 & A25 of CPU

Enable: Turn OFF system
Slave address: 98h

Max6657: 0.26(USD)
ADT7401ARMZ: 0.28(USD)

PWM FAN Control

+3VS

R0659 4.7KOhm

+5VS

CE0602 47UF/6.3V, D0601 1N4148W

P/N:12G17000004B

34 FAN0_TACH R0661 1.2KOhm

34 FAN_PWM R0671 @ 150Ohm FAN_PWM_CON FANSP

CON601

4	SIDE2		6
3			
2			
1	SIDE1		5

WtoB_CON_4P_1

C0653 100PF/50V, C0654 100PF/50V @

GND

R1.02---ITEM12

H/W Thermal Protect

+5VA

(94~98'C protect)

R0670 22.1K 1%

RT0671 100K

C0670 0.1U

U0670 PST9013NR

1	NC	VCC	5
2	SUB		
3	GND	VOUT	4

R0662 4.7KOhm @

FORCE_OFF# 34,81,92

Enable: Turn OFF system
OPEN Collector

+3VS

R0673 10KOhm

FAN_PWM

U0671 NC7SZ32M5X_NL

C0655 0.1UF/16V c0402

FAN_PWM_CON

34,43,45 OS#_OC R0672 0Ohm

Q0631 H2N7002

<Variant Name>

ASUSTeK COMPUTER INC

Title : CPU CAP, Thermal,FAN_CTRL

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

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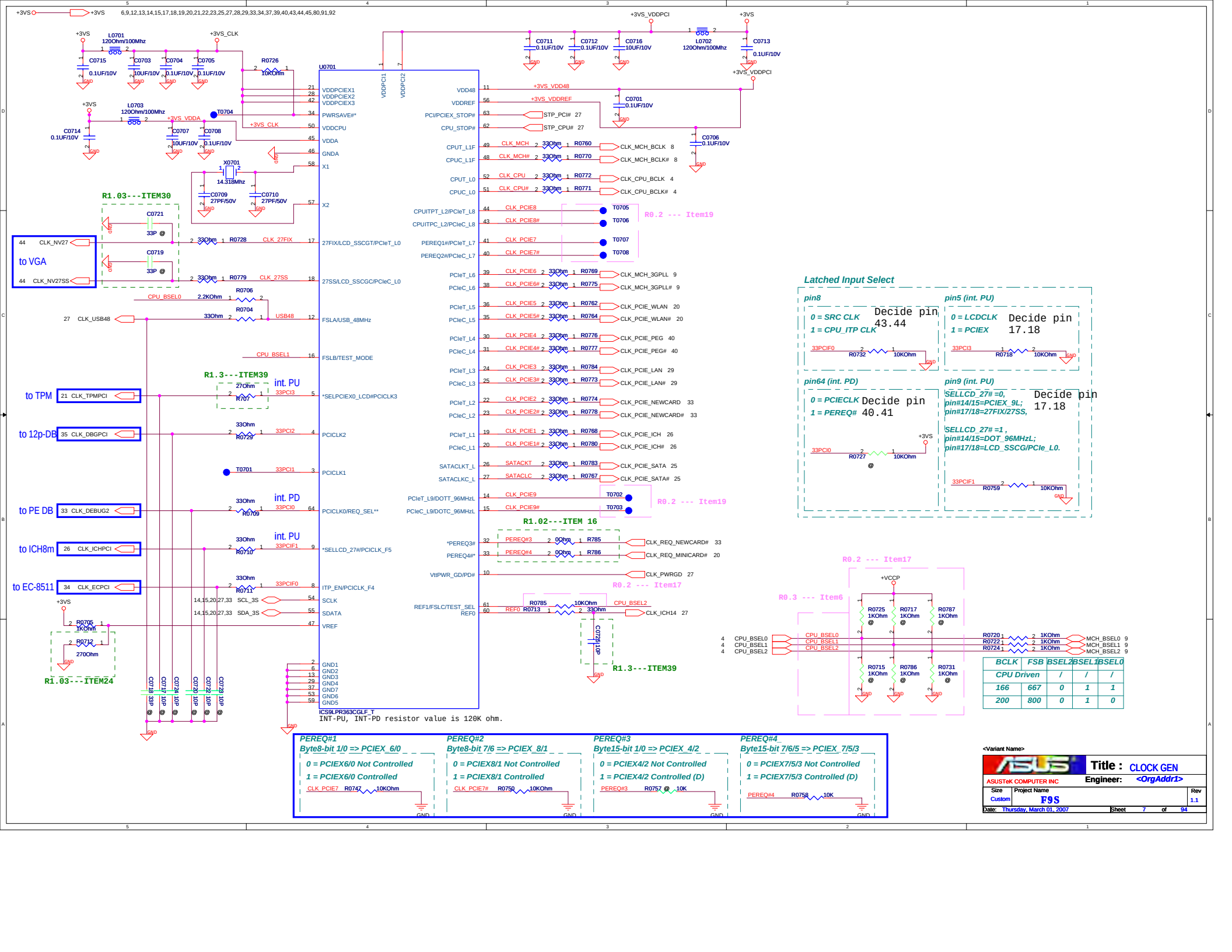
U0701
ICS9LPR363CGLF_T
INT-PU, INT-PD resistor value is 120K ohm.
R1.03---ITEM30
R1.3---ITEM39
R1.02---ITEM 16
R1.03---ITEM24
R0.2 --- Item19
R0.2 --- Item17
R0.3 --- Item6
to VGA
to TPM
to 12p-DB
to PE DB
to ICH8m
to EC-8511
int. PU
int. PD
Latched Input Select
pin8
0 = SRC CLK
1 = CPU_ITP CLK
Decide pin 43.44
pin5 (int. PU)
0 = LCDCLK
1 = PCIEX
Decide pin 17.18
pin64 (int. PD)
0 = PCIECLK
1 = PEREQ#
Decide pin 40.41
pin9 (int. PU)
SELLCD_27# =0, pin#14/15=PCIEX_9L; pin#17/18=27FIX/27SS,
SELLCD_27# =1 , pin#14/15=DOT_96MHzL; pin#17/18=LCD_SSCG/PCIe_L0.
Decide pin 17.18
PEREQ#1
Byte8-bit 1/0 => PCIEX_6/0
0 = PCIEX6/0 Not Controlled
1 = PCIEX6/0 Controlled
PEREQ#2
Byte8-bit 7/6 => PCIEX_8/1
0 = PCIEX8/1 Not Controlled
1 = PCIEX8/1 Controlled
PEREQ#3
Byte15-bit 1/0 => PCIEX_4/2
0 = PCIEX4/2 Not Controlled
1 = PCIEX4/2 Controlled (D)
PEREQ#4
Byte15-bit 7/6/5 => PCIEX_7/5/3
0 = PCIEX7/5/3 Not Controlled
1 = PCIEX7/5/3 Controlled (D)
BCLK | FSB | BSEL2 | BSEL1 | BSEL0
CPU Driven | | / | / | /
166 | 667 | 0 | 1 | 1
200 | 800 | 0 | 1 | 0
<Variant Name>
Title : CLOCK GEN
ASUSTeK COMPUTER INC
Engineer: <OrgAddr1>
Size: Custom
Project Name: F9S
Rev: 1.1
Date: Thursday, March 01, 2007
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RCOMP

For Calibrating the FSB I/O Buffer

R0801 24.9Ohm 1% — H_RCOMP — GND

SCOMP

For Slew Rate Compenssation on the FSB

+VCCP

R0802 54.9Ohm 1% — H_SCOMP

R0803 54.9Ohm 1% — H_SCOMP#

Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits

+VCCP — R0804 221Ohm — H_SWING — R0805 100Ohm 1% — GND; C0802 0.1UF/16V — GND

4 H_D#[63:0] — H_D#[63:0]

4 H_A#[35:3] — H_A#[35:3]

U0801A

HOST

H_D#0	E2	H_D#_0	
H_D#1	G2	H_D#_1	
H_D#2	G7	H_D#_2	
H_D#3	M6	H_D#_3	
H_D#4	H7	H_D#_4	
H_D#5	H3	H_D#_5	
H_D#6	G4	H_D#_6	
H_D#7	F3	H_D#_7	
H_D#8	N8	H_D#_8	
H_D#9	H2	H_D#_9	
H_D#10	M10	H_D#_10	
H_D#11	N12	H_D#_11	
H_D#12	N9	H_D#_12	
H_D#13	H5	H_D#_13	
H_D#14	P13	H_D#_14	
H_D#15	K9	H_D#_15	
H_D#16	M2	H_D#_16	
H_D#17	W10	H_D#_17	
H_D#18	Y8	H_D#_18	
H_D#19	V4	H_D#_19	
H_D#20	M3	H_D#_20	
H_D#21	J1	H_D#_21	
H_D#22	N5	H_D#_22	
H_D#23	N3	H_D#_23	
H_D#24	W6	H_D#_24	
H_D#25	W9	H_D#_25	
H_D#26	N2	H_D#_26	
H_D#27	Y7	H_D#_27	
H_D#28	Y9	H_D#_28	
H_D#29	P4	H_D#_29	
H_D#30	W3	H_D#_30	
H_D#31	N1	H_D#_31	
H_D#32	AD12	H_D#_32	
H_D#33	AE3	H_D#_33	
H_D#34	AD9	H_D#_34	
H_D#35	AC9	H_D#_35	
H_D#36	AC7	H_D#_36	
H_D#37	AC14	H_D#_37	
H_D#38	AD11	H_D#_38	
H_D#39	AC11	H_D#_39	
H_D#40	AB2	H_D#_40	
H_D#41	AD7	H_D#_41	
H_D#42	AB1	H_D#_42	
H_D#43	Y3	H_D#_43	
H_D#44	AC6	H_D#_44	
H_D#45	AE2	H_D#_45	
H_D#46	AC5	H_D#_46	
H_D#47	AG3	H_D#_47	
H_D#48	AJ9	H_D#_48	
H_D#49	AH8	H_D#_49	
H_D#50	AJ14	H_D#_50	
H_D#51	AE9	H_D#_51	
H_D#52	AE11	H_D#_52	
H_D#53	AH12	H_D#_53	
H_D#54	AJ5	H_D#_54	
H_D#55	AH5	H_D#_55	
H_D#56	AJ6	H_D#_56	
H_D#57	AE7	H_D#_57	
H_D#58	AJ7	H_D#_58	
H_D#59	AJ2	H_D#_59	
H_D#60	AE5	H_D#_60	
H_D#61	AJ3	H_D#_61	
H_D#62	AH2	H_D#_62	
H_D#63	AH13	H_D#_63	
H_SWING	B3	H_SWING	
H_RCOMP	C2	H_RCOMP	
H_SCOMP	W1	H_SCOMP	
H_SCOMP#	W2	H_SCOMP#	
H_CPURST#	B6	H_CPURST#	
H_CPUSLP#	E5	H_CPUSLP#	
H_AVREF	B9	H_AVREF	
H_DVREF	A9	H_DVREF	

H_A#_3	J13	H_A#3	
H_A#_4	B11	H_A#4	
H_A#_5	C11	H_A#5	
H_A#_6	M11	H_A#6	
H_A#_7	C15	H_A#7	
H_A#_8	F16	H_A#8	
H_A#_9	L13	H_A#9	
H_A#_10	G17	H_A#10	
H_A#_11	C14	H_A#11	
H_A#_12	K16	H_A#12	
H_A#_13	B13	H_A#13	
H_A#_14	L16	H_A#14	
H_A#_15	J17	H_A#15	
H_A#_16	B14	H_A#16	
H_A#_17	K19	H_A#17	
H_A#_18	P15	H_A#18	
H_A#_19	R17	H_A#19	
H_A#_20	B16	H_A#20	
H_A#_21	H20	H_A#21	
H_A#_22	L19	H_A#22	
H_A#_23	D17	H_A#23	
H_A#_24	M17	H_A#24	
H_A#_25	N16	H_A#25	
H_A#_26	J19	H_A#26	
H_A#_27	B18	H_A#27	
H_A#_28	E19	H_A#28	
H_A#_29	B17	H_A#29	
H_A#_30	B15	H_A#30	
H_A#_31	E17	H_A#31	
H_A#_32	C18	H_A#32	
H_A#_33	A19	H_A#33	
H_A#_34	B19	H_A#34	
H_A#_35	N19	H_A#35	
H_ADS#	G12	H_ADS#	4 H_ADS#
H_ADSTB#_0	H17	H_ADSTB#0	4 H_ADSTB#0
H_ADSTB#_1	G20	H_ADSTB#1	4 H_ADSTB#1
H_BNR#	C8	H_BNR#	4 H_BNR#
H_BPRI#	E8	H_BPRI#	4 H_BPRI#
H_BREQ#	F12	H_BREQ#0	4 H_BREQ#0
H_DEFER#	D6	H_DEFER#	4 H_DEFER#
H_DBSY#	C10	H_DBSY#	4 H_DBSY#
HPLL_CLK	AM5		CLK_MCH_BCLK 7
HPLL_CLK#	AM7		CLK_MCH_BCLK# 7
H_DPWR#	H8	H_DPWR#	4 H_DPWR#
H_DRDY#	K7	H_DRDY#	4 H_DRDY#
H_HIT#	E4	H_HIT#	4 H_HIT#
H_HITM#	C6	H_HITM#	4 H_HITM#
H_LOCK#	G10	H_LOCK#	4 H_LOCK#
H_TRDY#	B7	H_TRDY#	4 H_TRDY#
H_DINV#_0	K5		4 H_DINV#0
H_DINV#_1	L2		4 H_DINV#1
H_DINV#_2	AD13		4 H_DINV#2
H_DINV#_3	AE13		4 H_DINV#3
H_DSTBN#_0	M7		4 H_DSTBN#0
H_DSTBN#_1	K3		4 H_DSTBN#1
H_DSTBN#_2	AD2		4 H_DSTBN#2
H_DSTBN#_3	AH11		4 H_DSTBN#3
H_DSTBP#_0	L7		4 H_DSTBP#0
H_DSTBP#_1	K2		4 H_DSTBP#1
H_DSTBP#_2	AC2		4 H_DSTBP#2
H_DSTBP#_3	AJ10		4 H_DSTBP#3
H_REQ#_0	M14	H_REQ#0	
H_REQ#_1	E13	H_REQ#1	
H_REQ#_2	A11	H_REQ#2	
H_REQ#_3	H13	H_REQ#3	
H_REQ#_4	B12	H_REQ#4	
H_RS#_0	E12	H_RS#0	4 H_RS#0
H_RS#_1	D7	H_RS#1	4 H_RS#1
H_RS#_2	D8	H_RS#2	4 H_RS#2

4 H_REQ#[4:0] — H_REQ#[4:0]

T0801 — 4 H_CPURST# — 4 H_CPUSLP# — R0807 0Ohm

+VCCP — R0809 1KOhm 1% — H_VREF — R0806 0Ohm — C0801 0.1UF/10V — GND; R0808 2KOhm 1% — GND

<Variant Name>

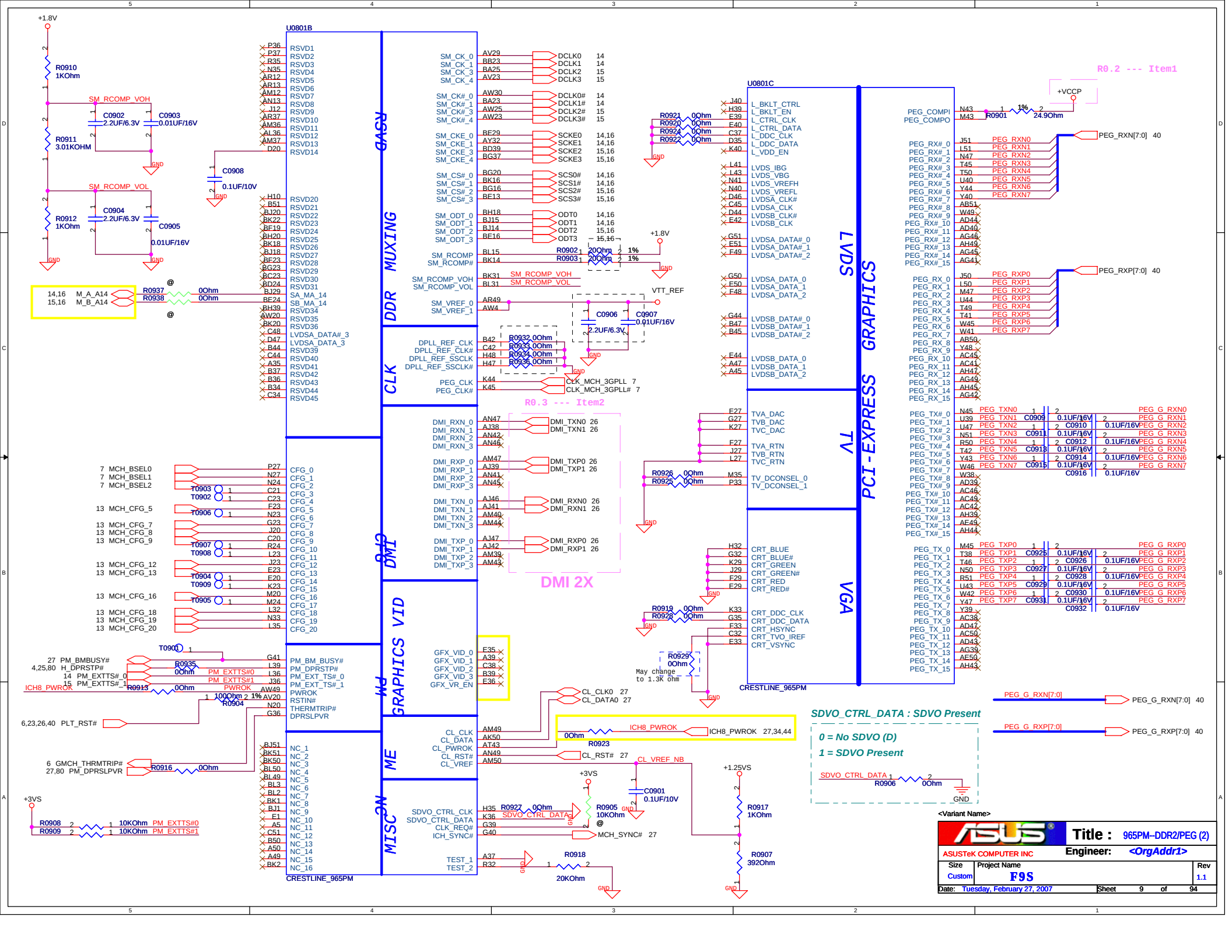
ASUSTeK COMPUTER INC

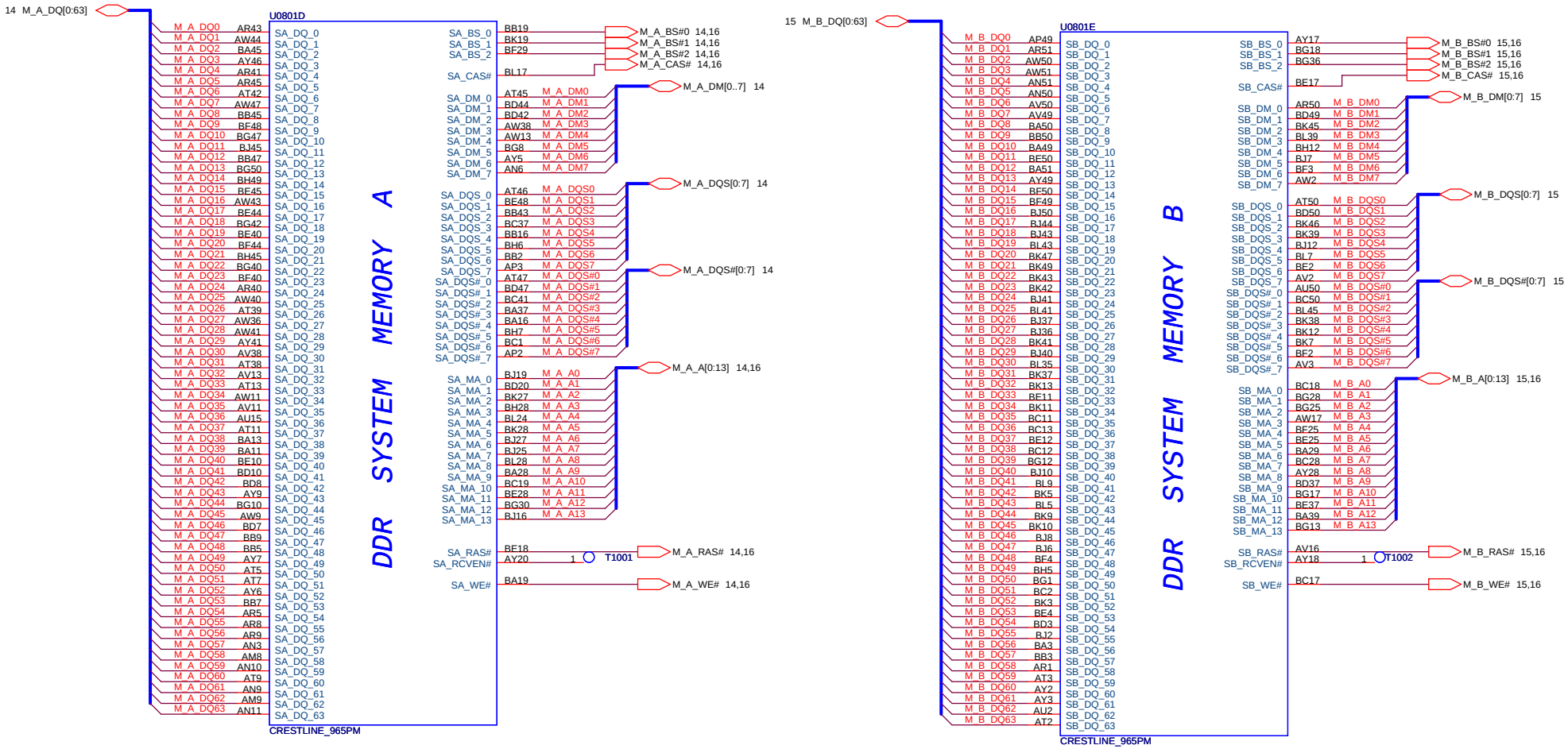
Title : 965PM -- CPU (1)

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 8 of 94


U0801B
U0801C
CRESTLINE_965PM
R0.2 --- Item1
R0.3 --- Item2
DMI 2X
SDVO_CTRL_DATA : SDVO Present
0 = No SDVO (D)
1 = SDVO Present
Title : 965PM--DDR2/PEG (2)
ASUSTeK COMPUTER INC
Engineer: <OrgAddr1>
Project Name F9S
Date: Tuesday, February 27, 2007
Sheet 9 of 94



<Variant Name>

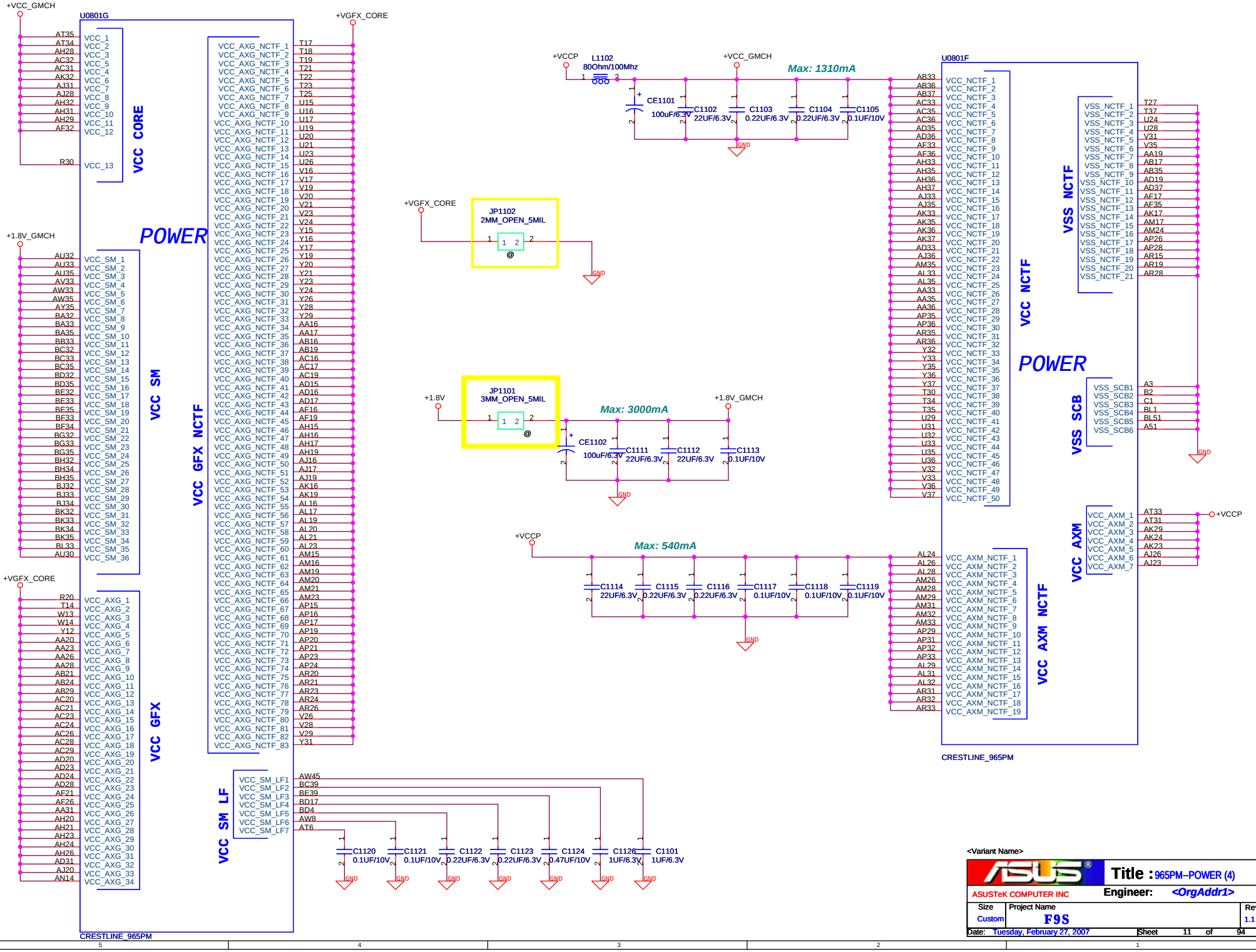
ASUSTeK COMPUTER INC

Title : 965PM--DDR2 bus (3)

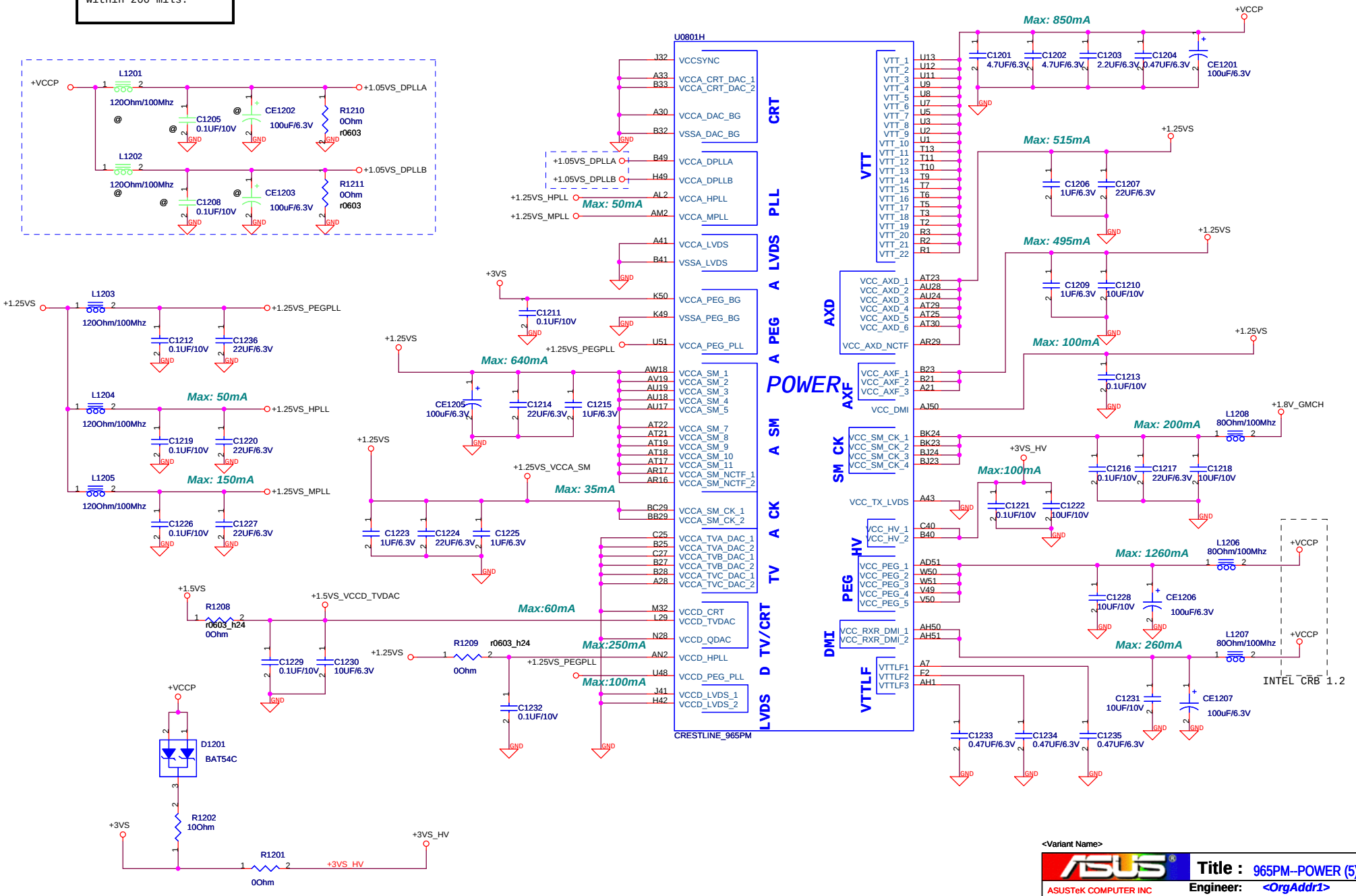
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 10 of 94


+VCC_GMCH
U0801G
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
+VGFX_CORE
+1.8V_GMCH
POWER
CRESTLINE_965PM
L1102
80Ohm/100Mhz
+VCCP
Max: 1310mA
CE1101
100uF/6.3V
C1102
22UF/6.3V
C1103
0.22UF/6.3V
C1104
0.22UF/6.3V
C1105
0.1UF/10V
GND
JP1102
2MM_OPEN_5MIL
JP1101
3MM_OPEN_5MIL
+1.8V
Max: 3000mA
CE1102
100uF/6.3V
C1111
22UF/6.3V
C1112
22UF/6.3V
C1113
0.1UF/10V
Max: 540mA
C1114
22UF/6.3V
C1115
0.22UF/6.3V
C1116
0.22UF/6.3V
C1117
0.1UF/10V
C1118
0.1UF/10V
C1119
0.1UF/10V
C1120
0.1UF/10V
C1121
0.1UF/10V
C1122
0.22UF/6.3V
C1123
0.22UF/6.3V
C1124
0.47UF/10V
C1126
1UF/6.3V
C1101
1UF/6.3V
U0801F
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
+VCCP
<Variant Name>
Title : 965PM--POWER (4)
ASUSTeK COMPUTER INC
Engineer: <OrgAddr1>
Size: Custom
Project Name: F9S
Rev: 1.1
Date: Tuesday, February 27, 2007
Sheet 11 of 94

NOTE:0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.



<Variant Name>

ASUSTeK COMPUTER INC

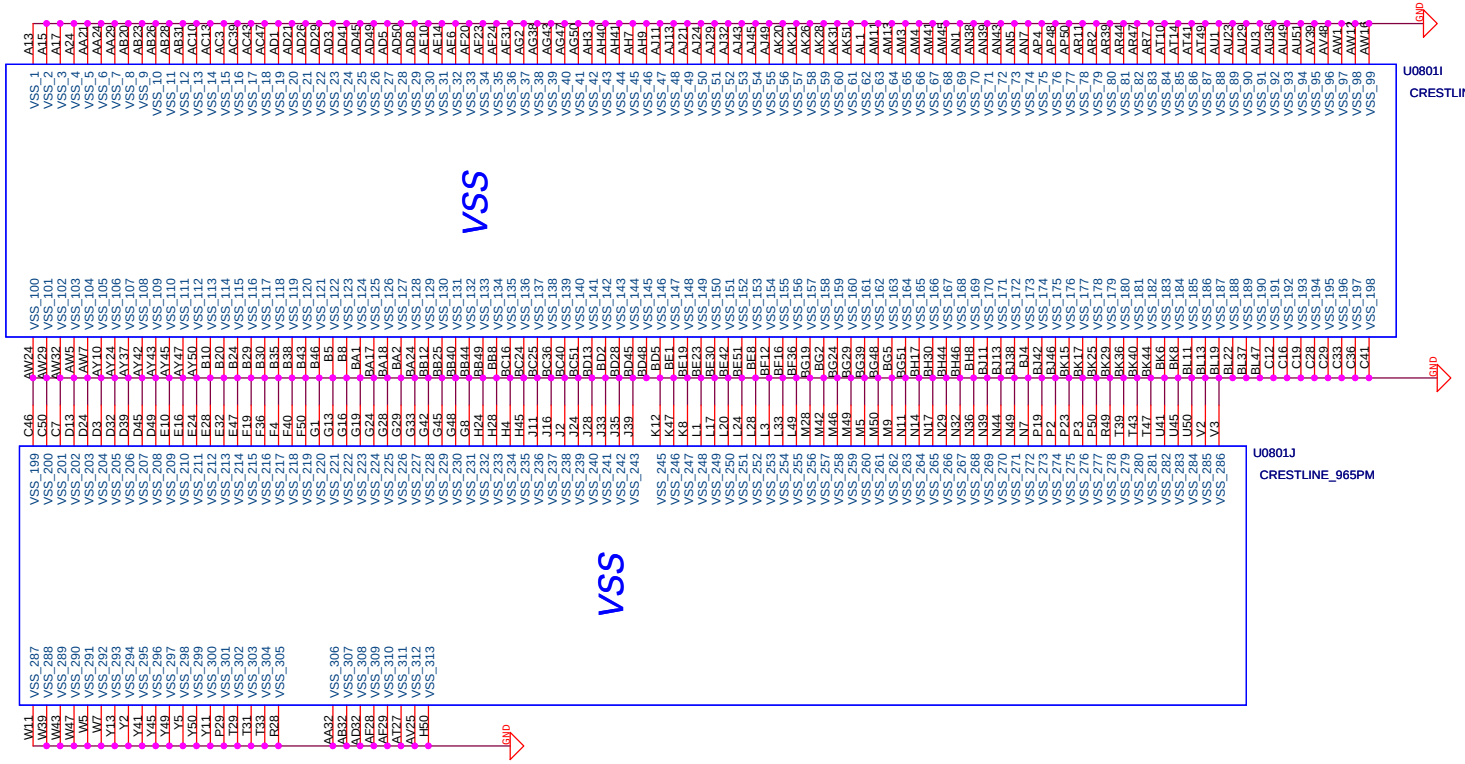
Title : 965PM--POWER (5)

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Monday, February 05, 2007 Sheet 12 of 94

HIGH = LANES REVERSED



9 MCH_CFG_5
R0.2 --- Item2
R1301
4.02KOHM

CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

9 MCH_CFG_7
R1304
4.02KOHM
@

CFG7 : CPU STRAP
HIGH = Mobile CPU (Default)
LOW = Reserved

9 MCH_CFG_8
R1306
4.02KOHM
@

CFG8 : Low Power PCI-E
0 = Normal mode
1 = Low Power Mode (Default)

9 MCH_CFG_9
R1302
4.02KOHM
@

CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = Normal Operation (Default)

9 MCH_CFG_16
R1305
4.02KOHM
@

CFG16 : Dynamic ODT STRAP
Low = Dynamic ODT Disabled
HIGH = Dyanamic ODT Enabled (default)

+3VS
R1310
4.02KOHM
@
9 MCH_CFG_18

CFG18 : VCC Select
LOW = 1.05V (default)
HIGH = 1.5V

+3VS
R1303
4.02KOHM
@
9 MCH_CFG_19

CFG19 : DMI LANE REVERSAL
LOW = NORMAL (default)
HIGH = LANES REVERSED

+3VS
R1307
4.02KOHM
@
9 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

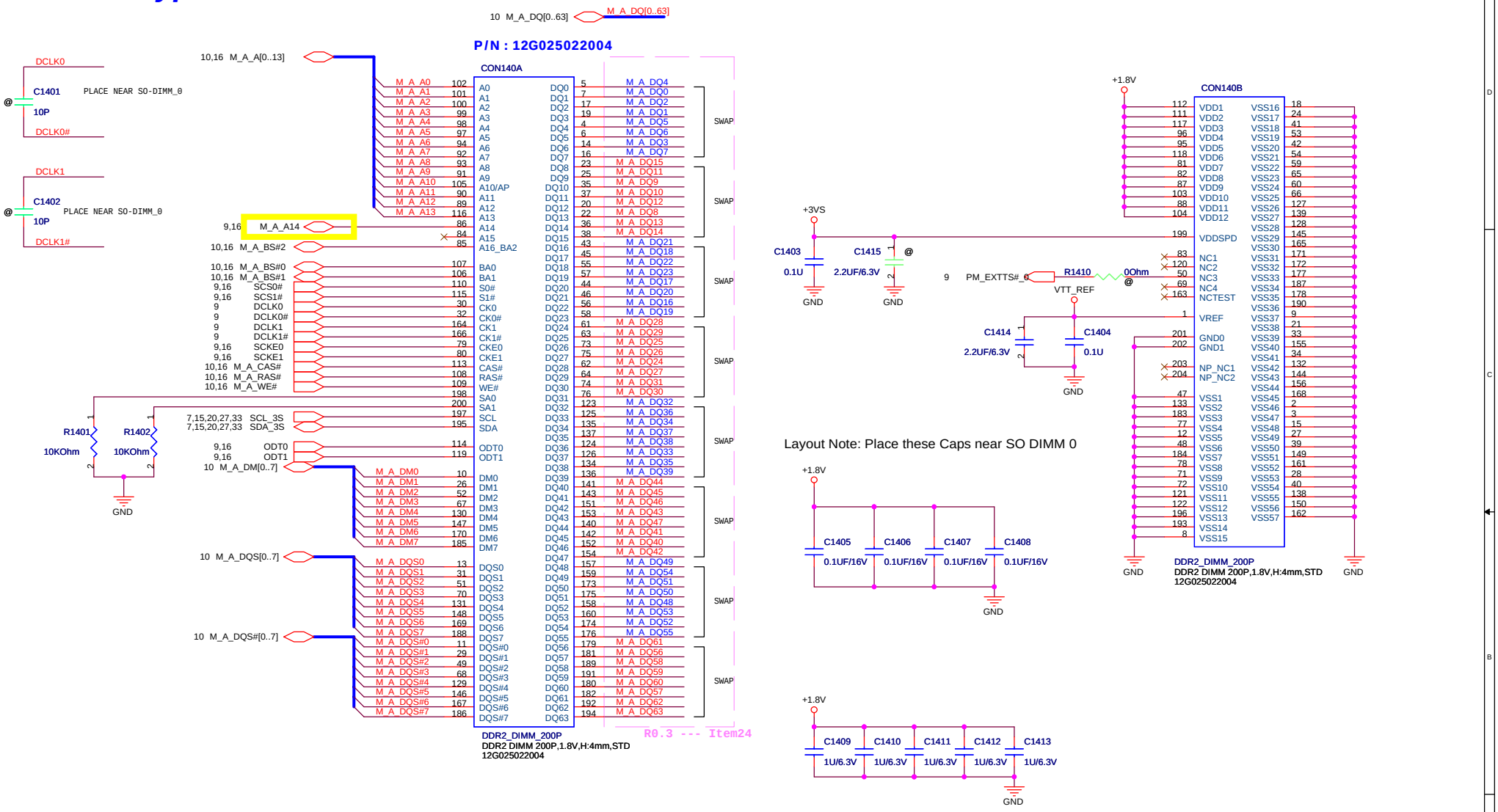
9 MCH_CFG_13
R1308
4.02KOHM
@

9 MCH_CFG_12
R1309
4.02KOHM
@

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)

ASUSTeK COMPUTER INC	Title : GND/Strapping (6)	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 13 of 94	

Standard Type



<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR SO-DIMM 0

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 14 of 94

Standard Type

10 M_B_DQ[0..63] — M_B_DQ[0..63]

P/N : 12G025C22004

CON150A

10,16 M_B_A[0..13]

DCLK2 — C1501 PLACE NEAR SO-DIMM_1 — @ 10P — DCLK2#

DCLK3 — C1502 PLACE NEAR SO-DIMM_1 — @ 10P — DCLK3#

+3VS — R1501 10KOhm — R1502 10KOhm — GND

M_B_A0	102	A0	DQ0	5	M_B_DQ4
M_B_A1	101	A1	DQ1	7	M_B_DQ1
M_B_A2	100	A2	DQ2	17	M_B_DQ3
M_B_A3	99	A3	DQ3	19	M_B_DQ2
M_B_A4	98	A4	DQ4	4	M_B_DQ5
M_B_A5	97	A5	DQ5	6	M_B_DQ0
M_B_A6	94	A6	DQ6	14	M_B_DQ6
M_B_A7	92	A7	DQ7	16	M_B_DQ7
M_B_A8	93	A8	DQ8	23	M_B_DQ9
M_B_A9	91	A9	DQ9	25	M_B_DQ8
M_B_A10	105	A10/AP	DQ10	35	M_B_DQ12
M_B_A11	90	A11	DQ11	37	M_B_DQ11
M_B_A12	89	A12	DQ12	20	M_B_DQ10
M_B_A13	116	A13	DQ13	22	M_B_DQ13
9,16 M_B_A14	86	A14	DQ14	36	M_B_DQ15
	84	A15	DQ15	38	M_B_DQ14
10,16 M_B_BS#2	85	A16_BA2	DQ16	43	M_B_DQ21
			DQ17	45	M_B_DQ16
	107		DQ18	55	M_B_DQ18
10,16 M_B_BS#0	106	BA0	DQ19	57	M_B_DQ22
10,16 M_B_BS#1	110	BA1	DQ20	44	M_B_DQ20
9,16 SCS2#	115	S0#	DQ21	46	M_B_DQ17
9,16 SCS3#	30	S1#	DQ22	56	M_B_DQ23
9 DCLK2	32	CK0	DQ23	58	M_B_DQ19
9 DCLK2#	164	CK0#	DQ24	61	M_B_DQ25
9 DCLK3	166	CK1	DQ25	63	M_B_DQ28
9 DCLK3#	79	CK1#	DQ26	73	M_B_DQ26
9,16 SCKE2	80	CKE0	DQ27	75	M_B_DQ31
9,16 SCKE3	113	CKE1	DQ28	62	M_B_DQ29
10,16 M_B_CAS#	108	CAS#	DQ29	64	M_B_DQ24
10,16 M_B_RAS#	109	RAS#	DQ30	74	M_B_DQ27
10,16 M_B_WE#	198	WE#	DQ31	76	M_B_DQ30
	200	SA0	DQ32	123	M_B_DQ36
7,14,20,27,33 SCL_3S	197	SA1	DQ33	125	M_B_DQ37
7,14,20,27,33 SDA_3S	195	SCL	DQ34	135	M_B_DQ38
		SDA	DQ35	137	M_B_DQ35
9,16 ODT2	114	ODT0	DQ36	124	M_B_DQ32
9,16 ODT3	119	ODT1	DQ37	126	M_B_DQ34
10 M_B_DM[0..7]			DQ38	134	M_B_DQ39
M_B_DM0	10	DM0	DQ39	136	M_B_DQ33
M_B_DM1	26	DM1	DQ40	141	M_B_DQ44
M_B_DM2	52	DM2	DQ41	143	M_B_DQ41
M_B_DM3	67	DM3	DQ42	151	M_B_DQ43
M_B_DM4	130	DM4	DQ43	153	M_B_DQ42
M_B_DM5	147	DM5	DQ44	140	M_B_DQ40
M_B_DM6	170	DM6	DQ45	142	M_B_DQ45
M_B_DM7	185	DM7	DQ46	152	M_B_DQ46
			DQ47	154	M_B_DQ47
10 M_B_DQS[0..7]			DQ48	157	M_B_DQ50
M_B_DQS0	13	DQS0	DQ49	159	M_B_DQ55
M_B_DQS1	31	DQS1	DQ50	173	M_B_DQ54
M_B_DQS2	51	DQS2	DQ51	175	M_B_DQ53
M_B_DQS3	70	DQS3	DQ52	158	M_B_DQ52
M_B_DQS4	131	DQS4	DQ53	160	M_B_DQ49
M_B_DQS5	148	DQS5	DQ54	174	M_B_DQ51
M_B_DQS6	169	DQS6	DQ55	176	M_B_DQ48
M_B_DQS7	188	DQS7	DQS#0	179	M_B_DQ60
10 M_B_DQS#[0..7]			DQS#1	181	M_B_DQ61
M_B_DQS#0	11	DQS#0	DQS#2	189	M_B_DQ58
M_B_DQS#1	29	DQS#1	DQS#3	191	M_B_DQ63
M_B_DQS#2	49	DQS#2	DQS#4	180	M_B_DQ56
M_B_DQS#3	68	DQS#3	DQS#5	182	M_B_DQ57
M_B_DQS#4	129	DQS#4	DQS#6	192	M_B_DQ62
M_B_DQS#5	146	DQS#5	DQS#7	194	M_B_DQ59
M_B_DQS#6	167	DQS#6			
M_B_DQS#7	186	DQS#7			

SWAP

DDR2_DIMM_200P

DDR2 DIMM 200P,1.8V,H:9.2mm,ST

12G025C22004

R0.3 --- Item24

+1.8V — +1.8V — 9,11,14,16,37,83

+3VS — +3VS — 6,7,9,12,13,14,17,18,19,20,21,22,23,25,27,28,29,33,34,37,39,40,43,44,45,80,91,92

VTT_REF — VTT_REF — 9,14,16

CON150B

112	VDD1	VSS16	18
111	VDD2	VSS17	24
117	VDD3	VSS18	41
96	VDD4	VSS19	53
95	VDD5	VSS20	42
118	VDD6	VSS21	54
81	VDD7	VSS22	59
82	VDD8	VSS23	65
87	VDD9	VSS24	60
103	VDD10	VSS25	66
88	VDD11	VSS26	127
104	VDD12	VSS27	139
		VSS28	128
199	VDDSPD	VSS29	145
		VSS30	165
83	NC1	VSS31	171
120	NC2	VSS32	172
50	NC3	VSS33	177
69	NC4	VSS34	187
163	NCTEST	VSS35	178
		VSS36	190
1	VREF	VSS37	9
		VSS38	21
201	GND0	VSS39	33
202	GND1	VSS40	155
		VSS41	34
203	NP_NC1	VSS42	132
204	NP_NC2	VSS43	144
		VSS44	156
47	VSS1	VSS45	168
133	VSS2	VSS46	2
183	VSS3	VSS47	3
77	VSS4	VSS48	15
12	VSS5	VSS49	27
48	VSS6	VSS50	39
184	VSS7	VSS51	149
78	VSS8	VSS52	161
71	VSS9	VSS53	28
72	VSS10	VSS54	40
121	VSS11	VSS55	138
122	VSS12	VSS56	150
196	VSS13	VSS57	162
193	VSS14		
8	VSS15		

DDR2_DIMM_200P

DDR2 DIMM 200P,1.8V,H:9.2mm,ST

12G025C22004

+3VS — C1503 0.1U — C1506 @ 2.2UF/6.3V — GND

9 PM_EXTTS#_1 — R1510 0Ohm @ — VTT_REF

C1504 2.2UF/6.3V — C1505 0.1U — GND

R0.3 --- Item1

Layout Note: Place these Caps near SO DIMM 1

+1.8V — C1517 0.1UF/16V — C1518 0.1UF/16V — C1515 0.1UF/16V — C1516 0.1UF/16V — GND

+1.8V — C1510 1U/6.3V — C1511 1U/6.3V — C1512 1U/6.3V — C1513 1U/6.3V — C1514 1U/6.3V — GND

<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR SO-DIMM_1

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

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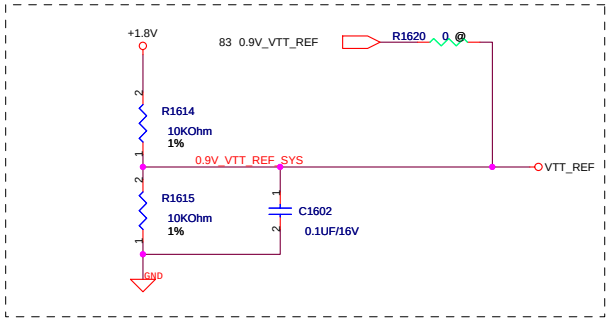
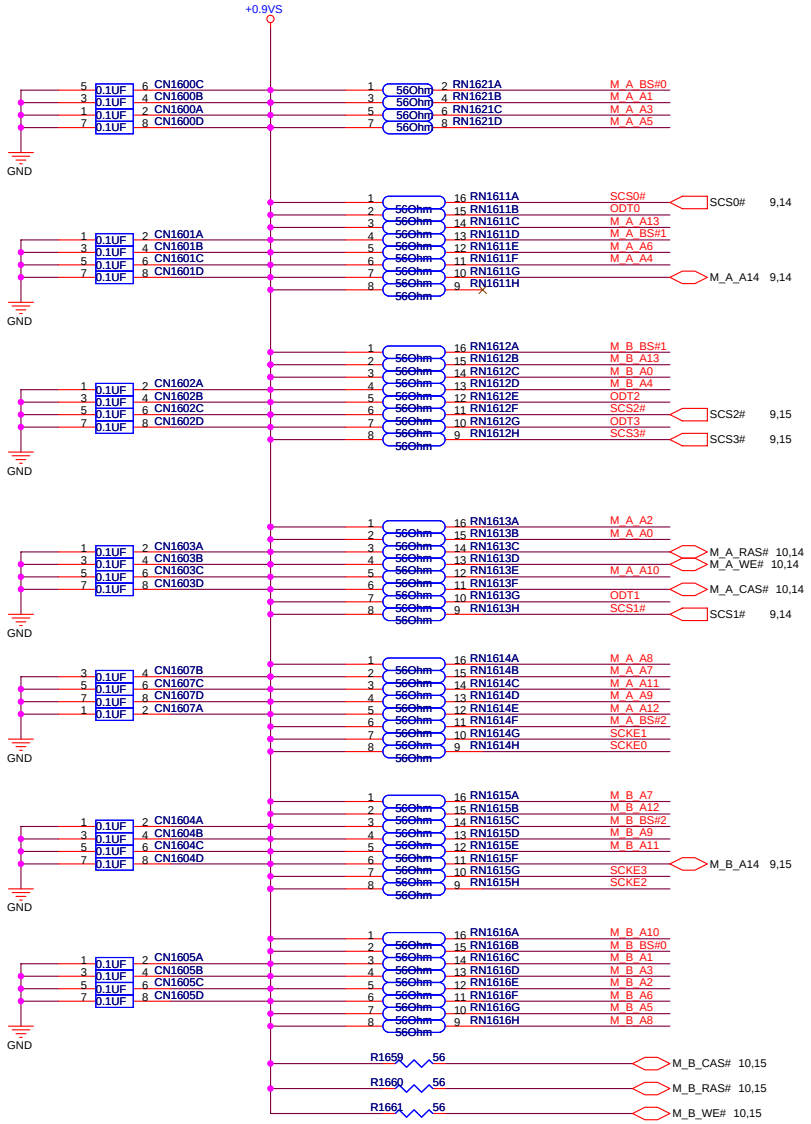


SWAPPED

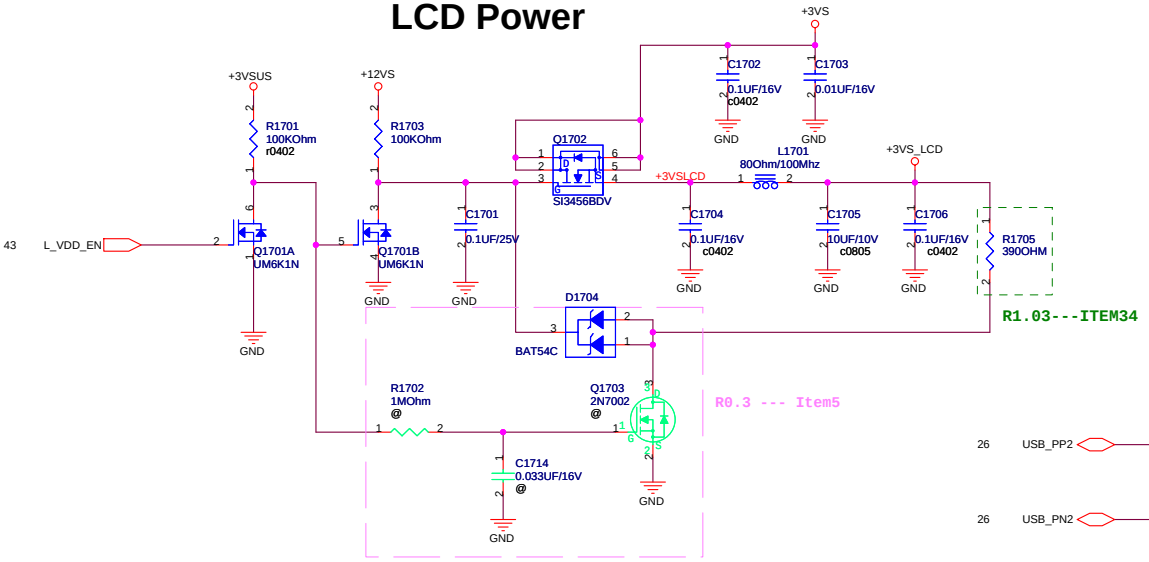


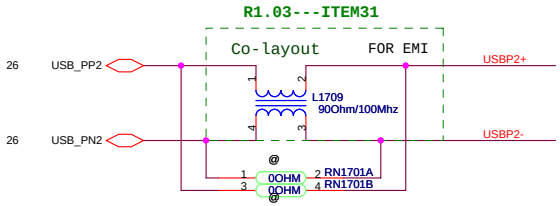
Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR2 ADDR TERM	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 16 of 94	

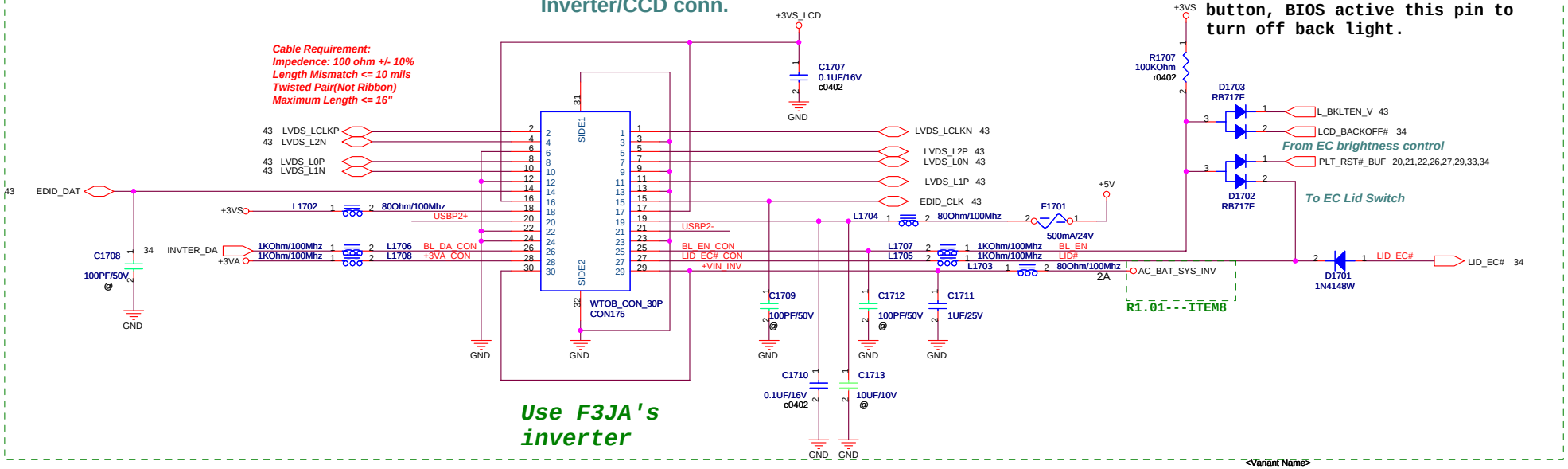
LCD Power





R1.2---ITEM36

Inverter/CCD conn.

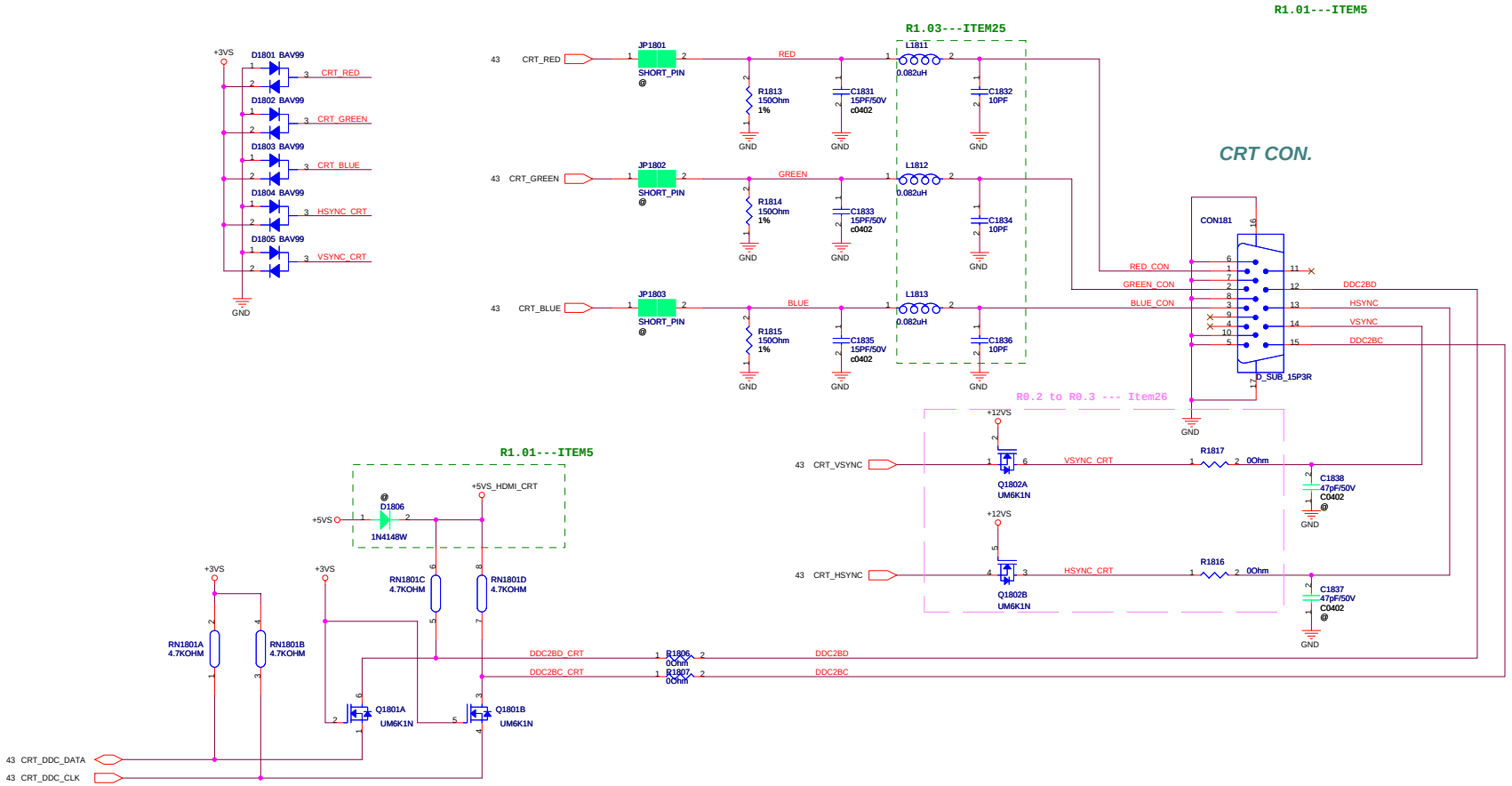


Use F3JA's inverter

BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

<Variant Name>

Title : LVDS & INVERTER	
ASUSTeK COMPUTER INC	Engineer:
Size: Custom	Project Name: F9S
Rev: 1.1	
Date: Tuesday, February 27, 2007	Sheet 17 of 94



<Variant Name>

ASUSTeK COMPUTER INC

Title : CRT

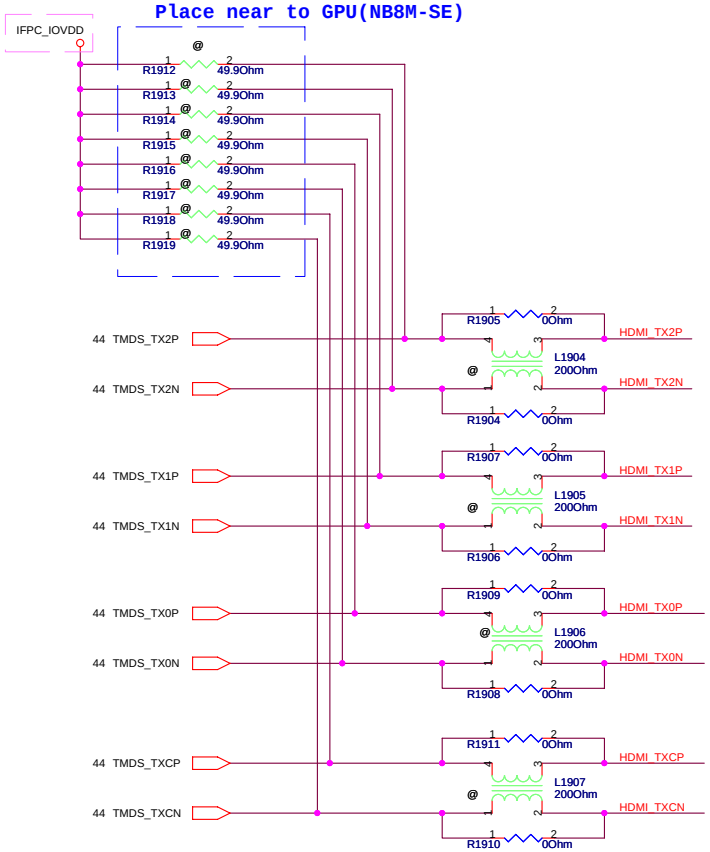
Engineer:

Size	Project Name	Rev
C	F9S	1.1

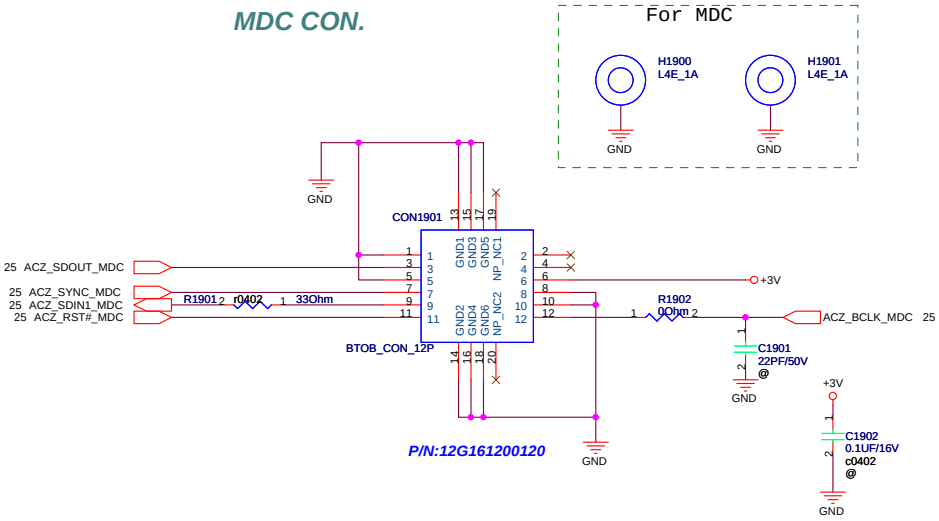
Date: Tuesday, February 27, 2007 Sheet 18 of 94

R0.2 --- Item5

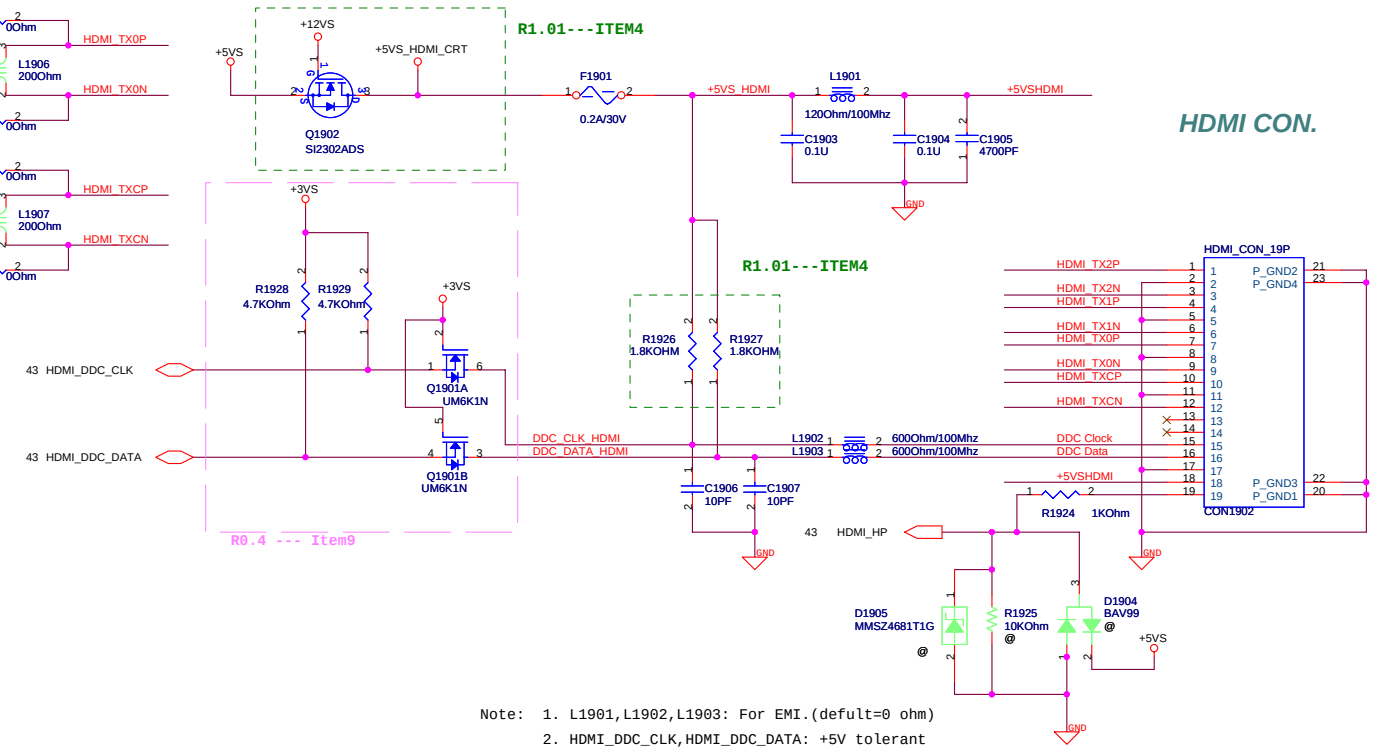
Place near to GPU(NB8M-SE)



MDC CON.



HDMI CON.



Note: 1. L1901,L1902,L1903: For EMI.(defult=0 ohm)

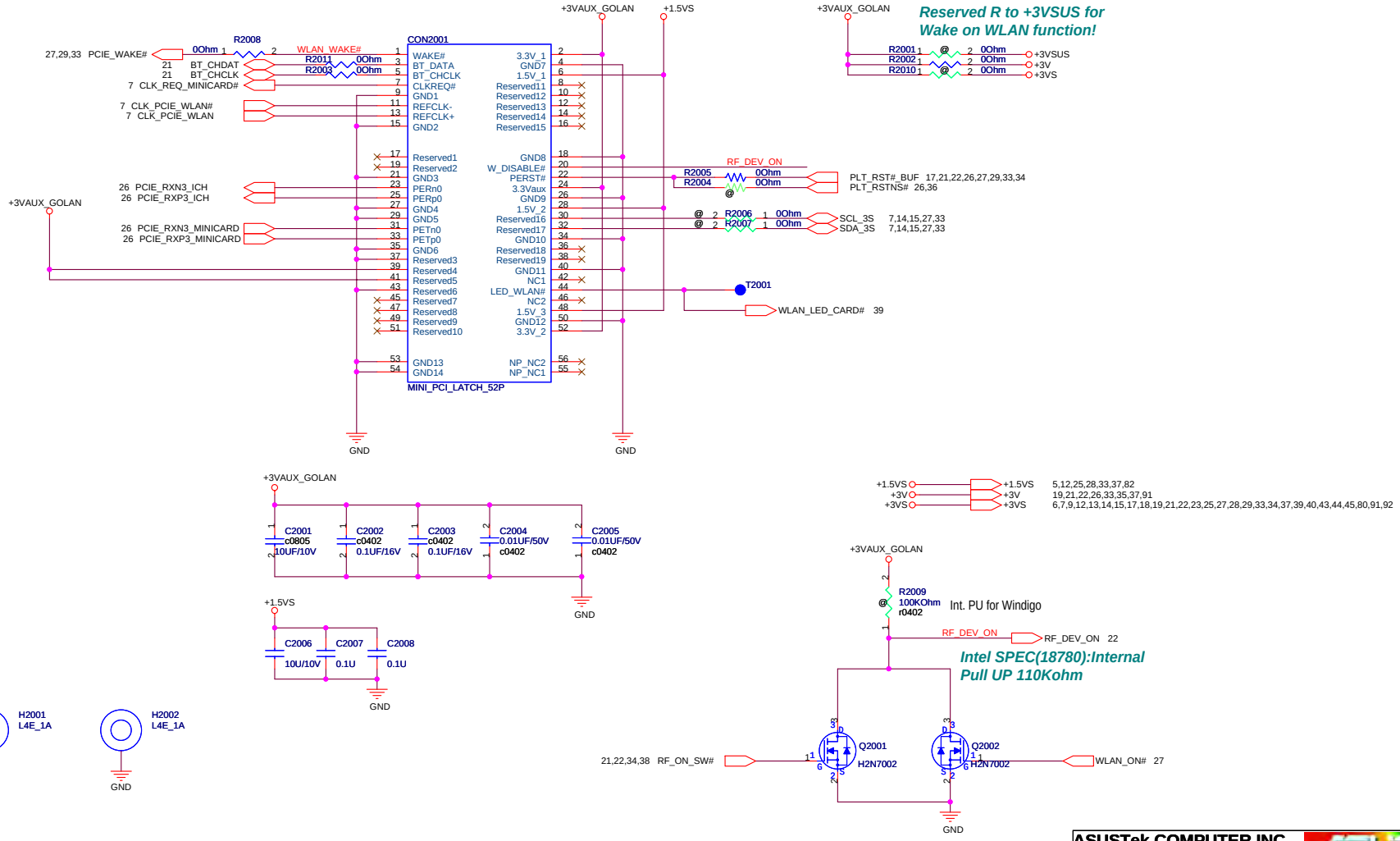
2. HDMI_DDC_CLK,HDMI_DDC_DATA: +5V tolerant

ASUSTek COMPUTER INC.		
<OrgAddr1> Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: MDC,HDMI CON		
Size: Custom	Document Number: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 19 of 94	

+3VAUX_GOLAN:+3.003V~+3.597V
Max= 1100 mA
+1.5VS:+1.425V~+1.575V
Max= 375 mA

P/N : 12G030100525_2006/1024

WLAN



ASUSTek COMPUTER INC.	
<OrgAddr1> Li-Te Rd.,Peitou, Taipei,Taiwan, ROC	
Title: **MINI CARD--(1)**	
Size: Custom	Document Number: **F9S**
Rev: 1.1	
Date: Tuesday, February 27, 2007	Sheet 20 of 94

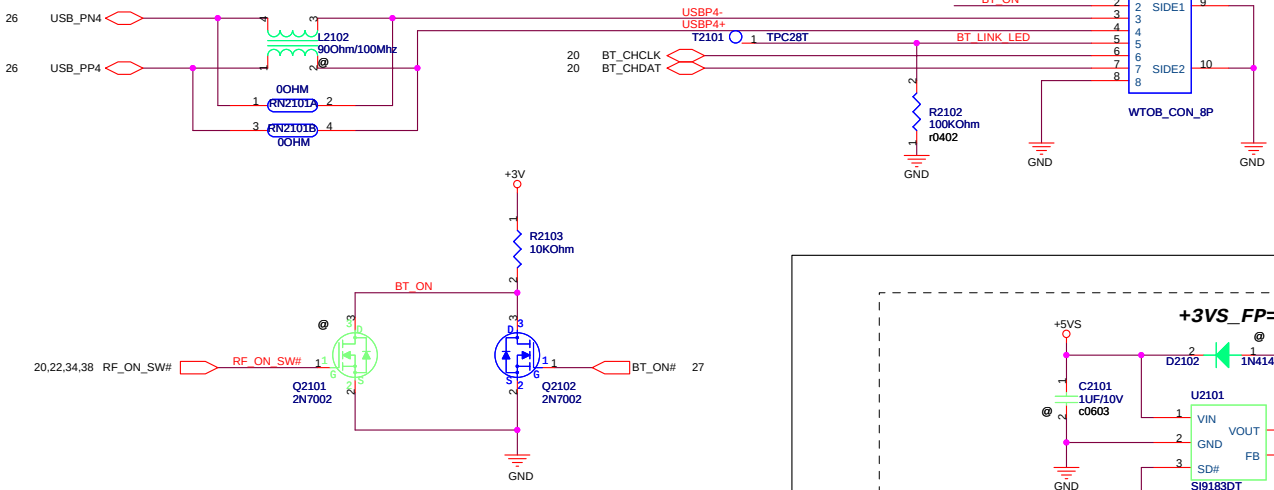
R1.02---ITEM10

Bluetooth Conn.

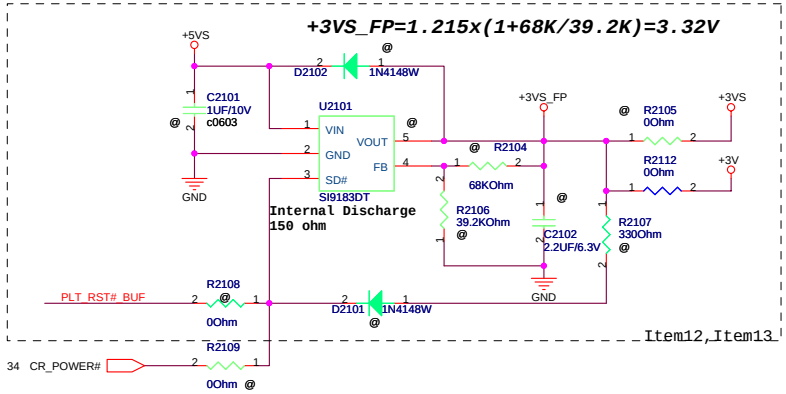
max. 60mA

Low -> Diable
High -> Enable

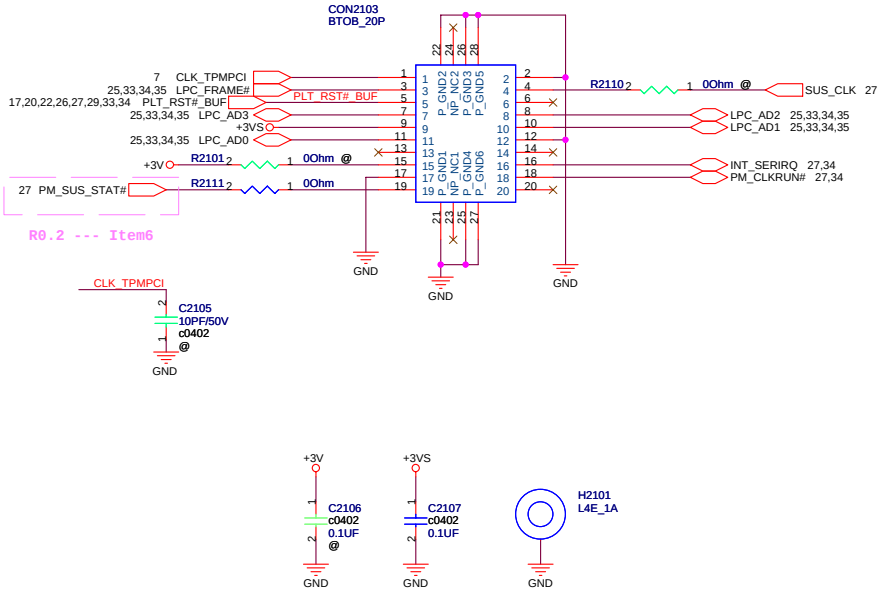
Co-layout FOR EMI



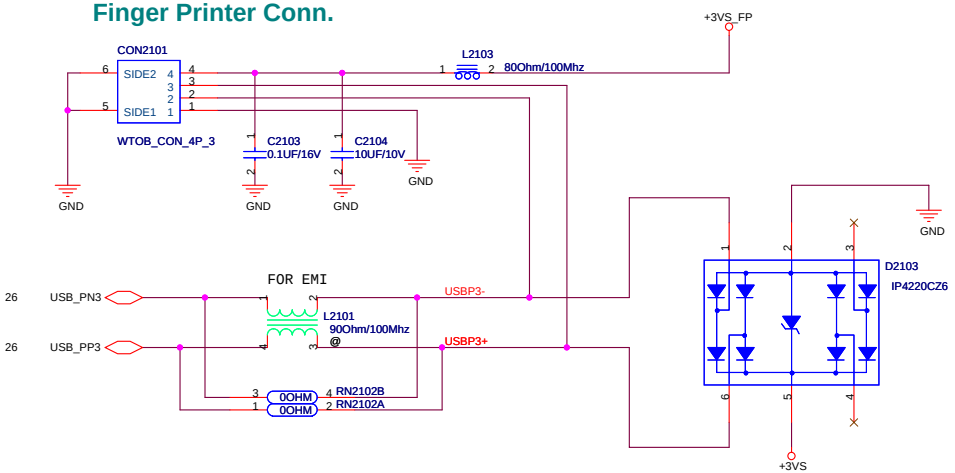
+3VS_FP=1.215x(1+68K/39.2K)=3.32V



TPM Module Conn.

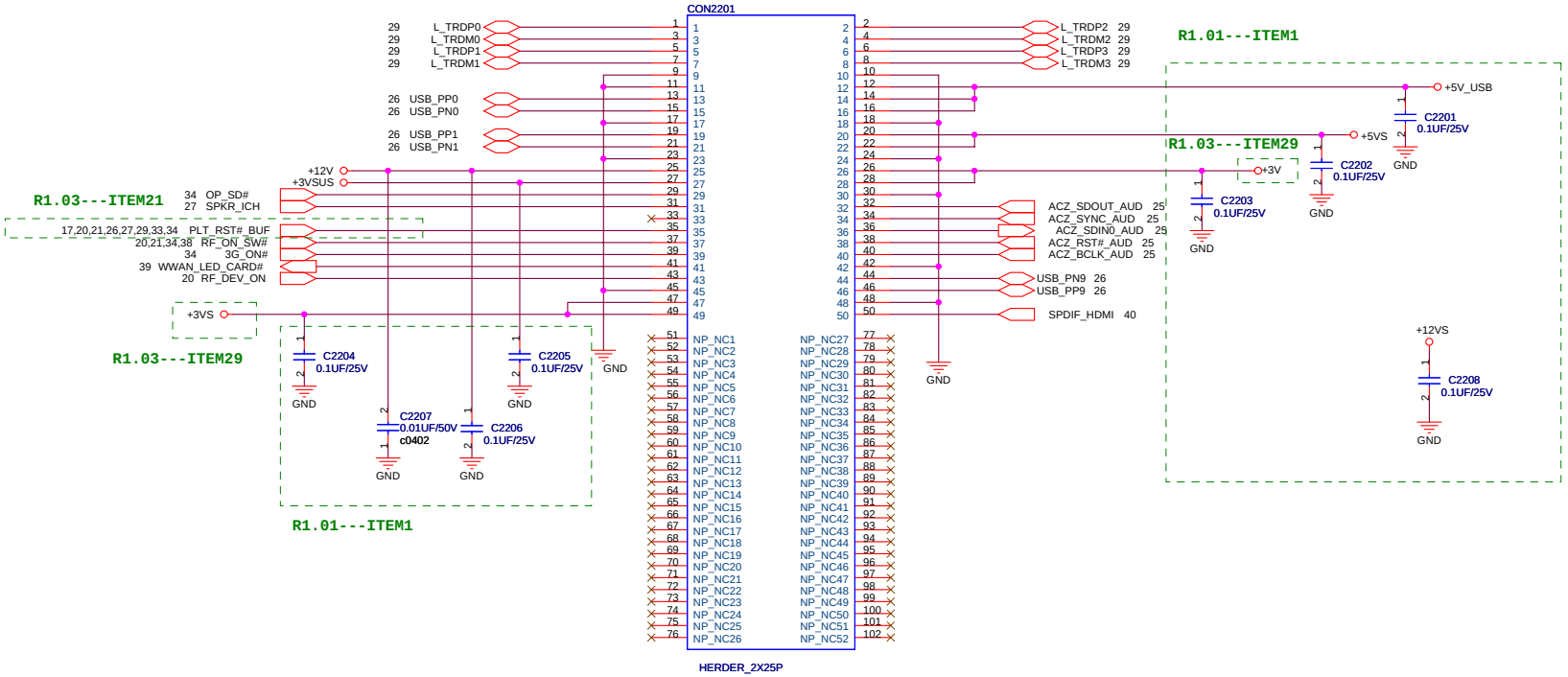


Finger Printer Conn.



<Variant Name>

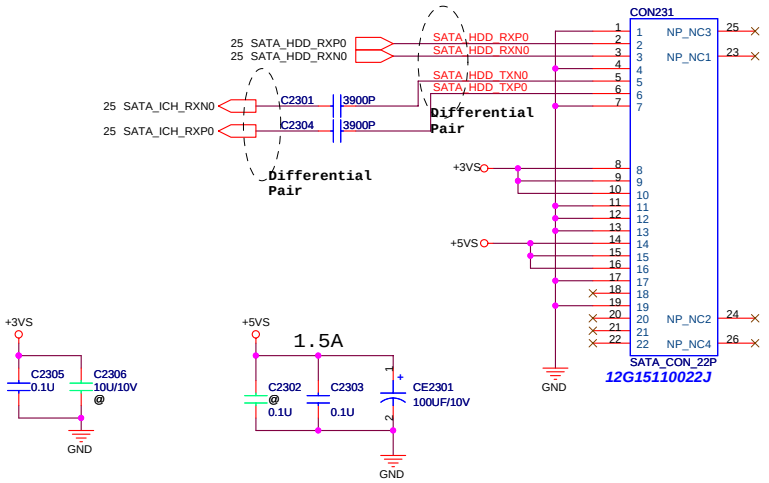
ASUSTeK COMPUTER INC	Title : B/T,F/P& TPM	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 21 of 94	



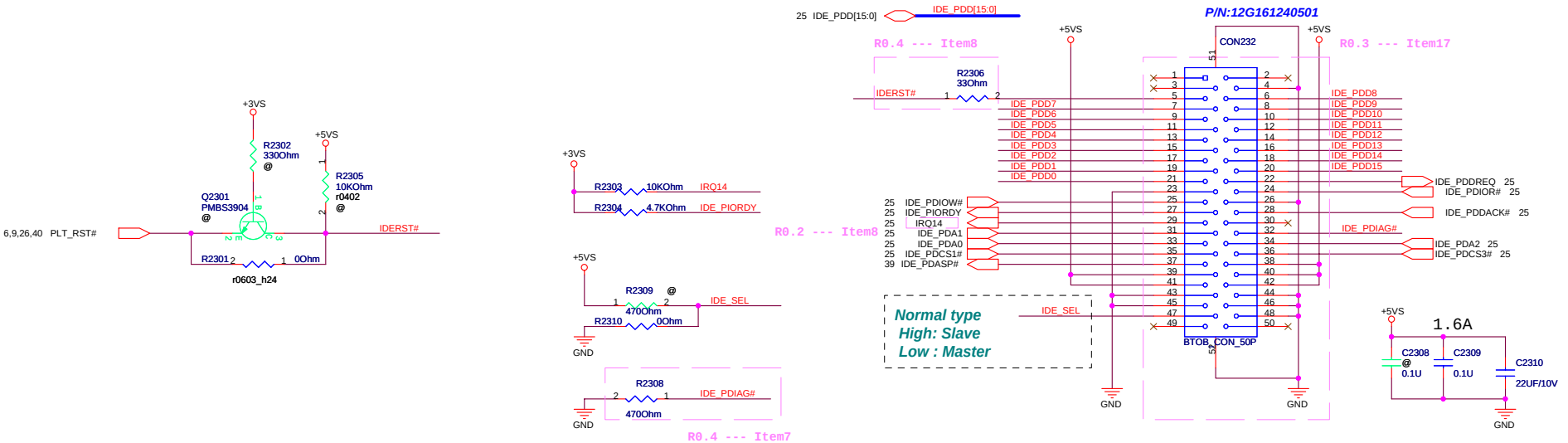
<Variant Name>

ASUSTeK COMPUTER INC	Title : B TO B CONN(M)	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 22 of 94	

SATA HDD CON



PATA CD-ROM CON



<Variant Name>

ASUSTeK COMPUTER INC	Title : HDD & CDROM	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 23 of 94	

R1.02---ITEM11

R1.03---ITEM27

+3VSUS +5VSUS

@ R2409 0Ohm

R2410 0Ohm

+USB_SUS

C2403 0.1UF/10V c0402

GND

U2401 SN74CB3Q3306APWR soic_8p_26_122x251 06G004195011

26 USB_PN7 — 1A — 1B — USB_N7

26 USB_PP7 — 2A — 2B — USB_P7

OE1# VCC OE2# GND

R1.03---ITEM27

+USB_SUS

R2408 100KOhm

USB_D-_OE#

Q2406 2N7002

27,34 PM_SUSC#

GND

FOR EMI

L2401 90Ohm/100Mhz @

USBP7-

USBP7+

0OHM RN2401A

0OHM RN2401B

Co-layout

R1.01---ITEM9

D2401 @ EGA10603V05A1

@ D2400 EGA10603V05A1

ESD Guard Close to CON241

GND GND

Change ESD package for layout placement.

USB

P/N:12G13102004N

+5V_USB_S

F2401 1.5A/6V

+5VUSB_5

R2405 0Ohm

C2402 22UF/10V

C2401 0.1U

USBP7-

USBP7+

CON241 USB_CON_1X4P

P_GND1 P_GND2 P_GND3 P_GND4

GND

R1.02---ITEM11

+12VSUS

R2407 100KOhm

R2406 100KOhm

USB_GV

Q2404A UM6K1N

Q2404B UM6K1N

34 USB_PWRSEL

Q2405A UM6K1N

Q2405B UM6K1N

PM_SUSC#

USB_PWRINT 34

R1.03---ITEM26

+5VSUS +5VSUS_USB

Q2403 FDW2501NZ 07G005161020

DRAIN_1 SOURCE_1 SOURCE_2 GATE_1 DRAIN_2 SOURCE_3 SOURCE_4 GATE_2

+5V_USB_S +5VSUS_USB

USB_GSUS

C2404 0.1UF/25V

USB_PWRSEL
Select Enable (H)/ Disable (L)
USB Port Charging Function on S4/ S5

USB_PWRINT
Select Enable (H)/ Disable (L)
USB Port Power Interrupt

USB_PWRSEL	PM_SUSC#	USB_GV	USB_GSUS
H	X	L	H
L	H	L	H
L	L	H	L

+12V +5V +5V_USB

R2404 100KOhm r0402

Q2402 SI4800BDY

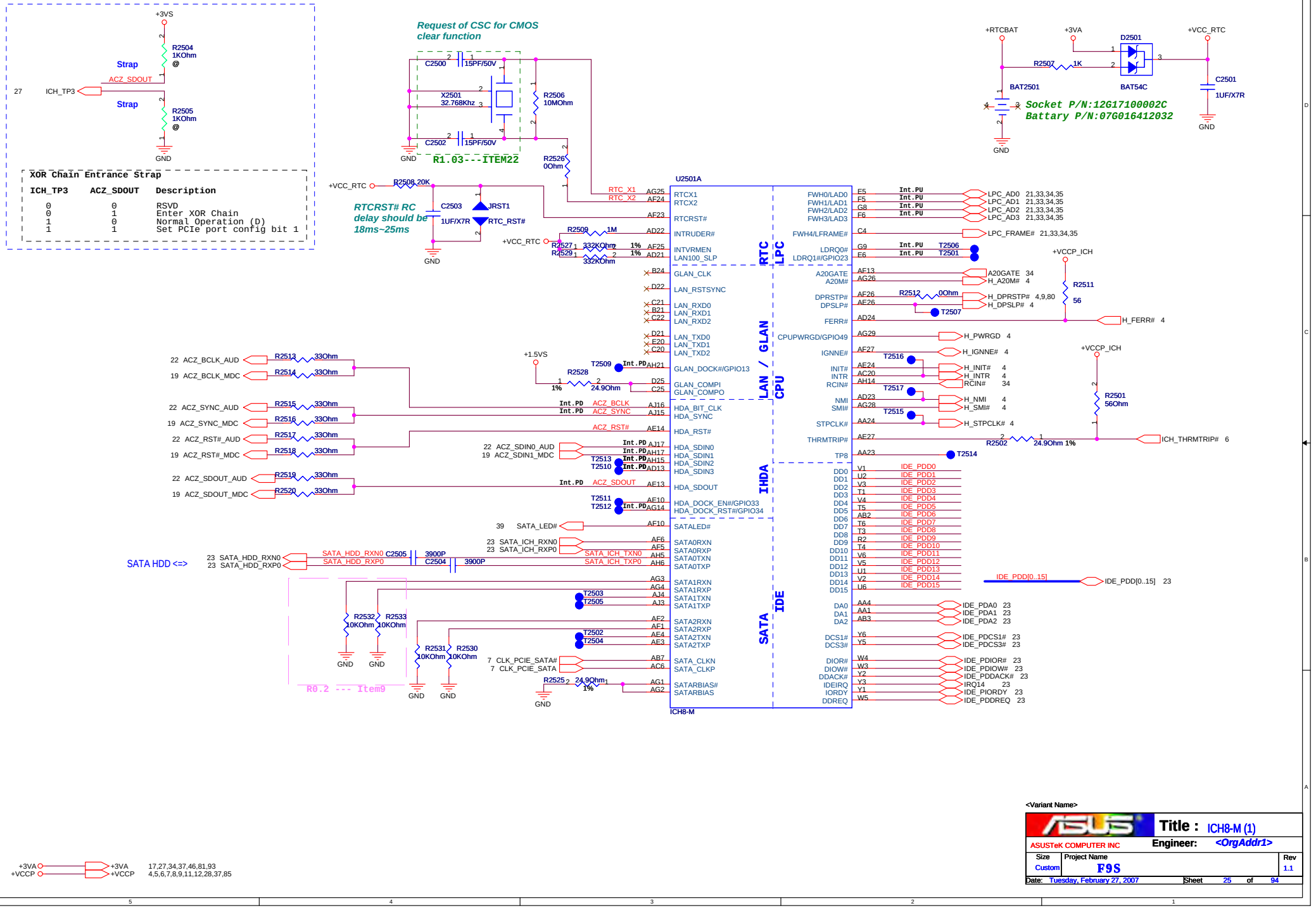
<Variant Name>

Title : USB PORTS

ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Friday, March 02, 2007 Sheet 24 of 94



<Variant Name>

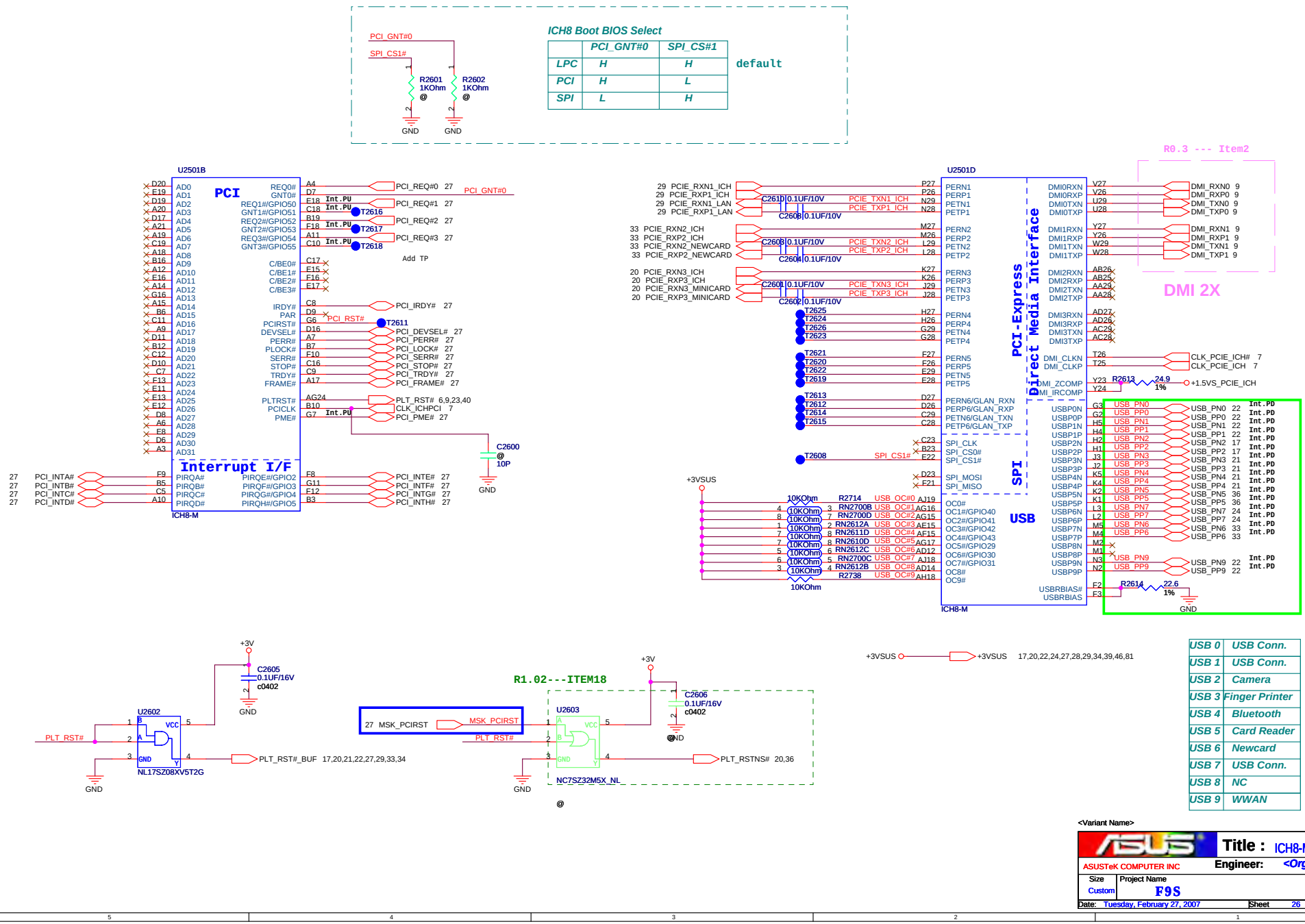
ASUSTeK COMPUTER INC

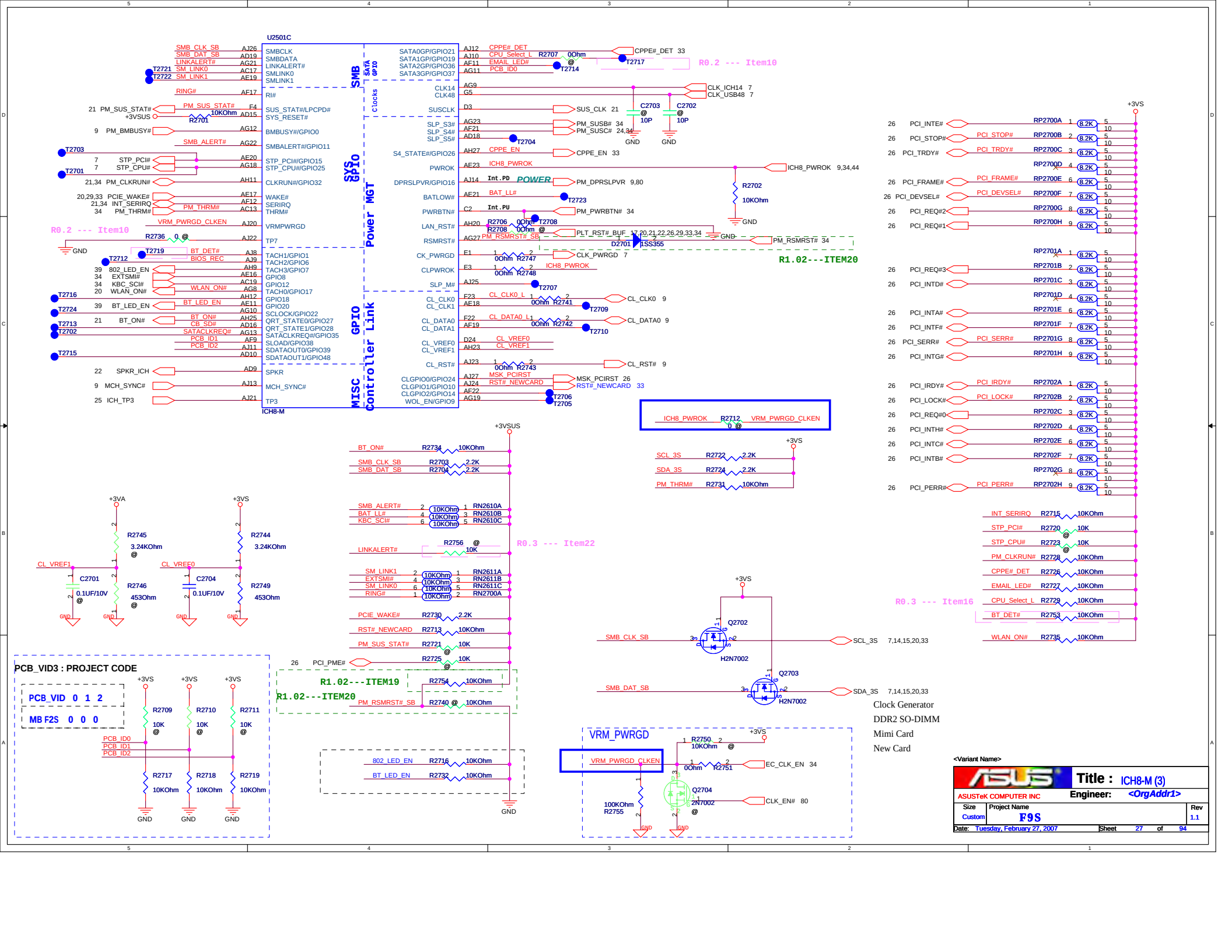
Title : ICH8-M (1)

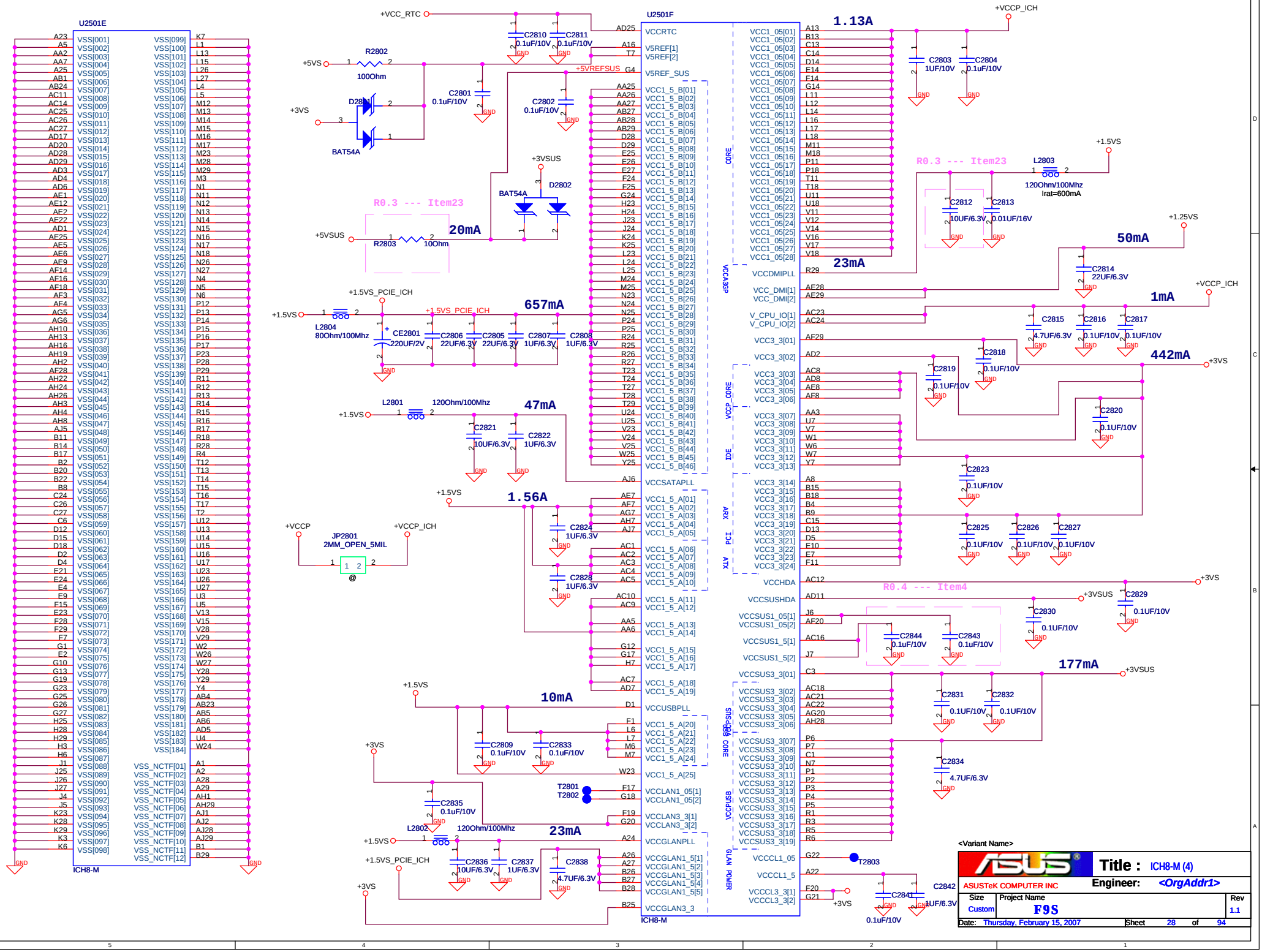
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 25 of 94


ICH8 Boot BIOS Select
PCI_GNT#0
SPI_CS1#
R2601 1KOhm @
R2602 1KOhm @
GND
GND
default
U2501B
PCI
Interrupt I/F
ICH8-M
PCI_REQ#0 27
PCI_GNT#0
PCI_REQ#1 27
PCI_REQ#2 27
PCI_REQ#3 27
Add TP
PCI_IRDY# 27
PCI_RST#
PCI_DEVSEL# 27
PCI_PERR# 27
PCI_LOCK# 27
PCI_SERR# 27
PCI_STOP# 27
PCI_TRDY# 27
PCI_FRAME# 27
PLT_RST# 6,9,23,40
CLK_ICHPCI 7
PCI_PME# 27
C2600 @ 10P
PCI_INTA# 27
PCI_INTB# 27
PCI_INTC# 27
PCI_INTD# 27
PCI_INTE# 27
PCI_INTF# 27
PCI_INTG# 27
PCI_INTH# 27
U2501D
PCI-Express
Direct Media Interface
SPI
USB
ICH8-M
DMI 2X
R0.3 --- Item2
DMI_RXN0 9
DMI_RXP0 9
DMI_TXN0 9
DMI_TXP0 9
DMI_RXN1 9
DMI_RXP1 9
DMI_TXN1 9
DMI_TXP1 9
CLK_PCIE_ICH# 7
CLK_PCIE_ICH 7
+1.5VS_PCIE_ICH
R2613 24.9 1%
R2614 22.6 1%
+3VSUS
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
R2714 10KOhm
RN2700B USB_OC#1
RN2700D USB_OC#2
RN2612A USB_OC#3
RN2611D USB_OC#4
RN2610D USB_OC#5
RN2612C USB_OC#6
RN2700C USB_OC#7
RN2612B USB_OC#8
R2738 10KOhm USB_OC#9
USB_PN0 22 Int.PD
USB_PP0 22 Int.PD
USB_PN1 22 Int.PD
USB_PP1 22 Int.PD
USB_PN2 17 Int.PD
USB_PP2 17 Int.PD
USB_PN3 21 Int.PD
USB_PP3 21 Int.PD
USB_PN4 21 Int.PD
USB_PP4 21 Int.PD
USB_PN5 36 Int.PD
USB_PP5 36 Int.PD
USB_PN7 24 Int.PD
USB_PP7 24 Int.PD
USB_PN6 33 Int.PD
USB_PP6 33 Int.PD
USB_PN9 22 Int.PD
USB_PP9 22 Int.PD
GND
+3V
C2605 0.1UF/16V c0402
U2602
NL17SZ08XV5T2G
PLT_RST#
PLT_RST#_BUF 17,20,21,22,27,29,33,34
R1.02---ITEM18
27 MSK_PCIRST
MSK_PCIRST
U2603
NC7SZ32M5X_NL
C2606 0.1UF/16V c0402
@
PLT_RSTNS# 20,36
+3VSUS +3VSUS 17,20,22,24,27,28,29,34,39,46,81
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 Camera
USB 3 Finger Printer
USB 4 Bluetooth
USB 5 Card Reader
USB 6 Newcard
USB 7 USB Conn.
USB 8 NC
USB 9 WWAN
<Variant Name>
Title : ICH8-M (2)
ASUSTeK COMPUTER INC
Engineer: <OrgAddr1>
Size Custom
Project Name F9S
Rev 1.1
Date: Tuesday, February 27, 2007
Sheet 26 of 94


U2501C
ICH8-M
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
R0.2 --- Item10
R0.3 --- Item22
R0.3 --- Item16
R1.02---ITEM20
R1.02---ITEM19
POWER
PCB_VID3 : PROJECT CODE
PCB_VID 0 1 2
MB F2S 0 0 0
VRM_PWRGD
Clock Generator
DDR2 SO-DIMM
Mimi Card
New Card
<Variant Name>
Title : ICH8-M (3)
ASUSTeK COMPUTER INC
Engineer: <OrgAddr1>
Size Custom
Project Name F9S
Rev 1.1
Date: Tuesday, February 27, 2007
Sheet 27 of 94


U2501E
ICH8-M
U2501F
ICH8-M
R2802
100Ohm
D2801
BAT54A
D2802
BAT54A
R0.3 --- Item23
20mA
R2803
10Ohm
L2804
80Ohm/100Mhz
CE2801
220UF/2V
657mA
L2801
120Ohm/100Mhz
47mA
1.56A
JP2801
2MM_OPEN_5MIL
10mA
L2802
120Ohm/100Mhz
23mA
1.13A
L2803
120Ohm/100Mhz
Irat=600mA
R0.3 --- Item23
50mA
23mA
1mA
442mA
177mA
R0.4 --- Item4
<Variant Name>
Title : ICH8-M (4)
ASUSTeK COMPUTER INC
Engineer: <OrgAddr1>
Size Custom
Project Name F9S
Rev 1.1
Date: Thursday, February 15, 2007
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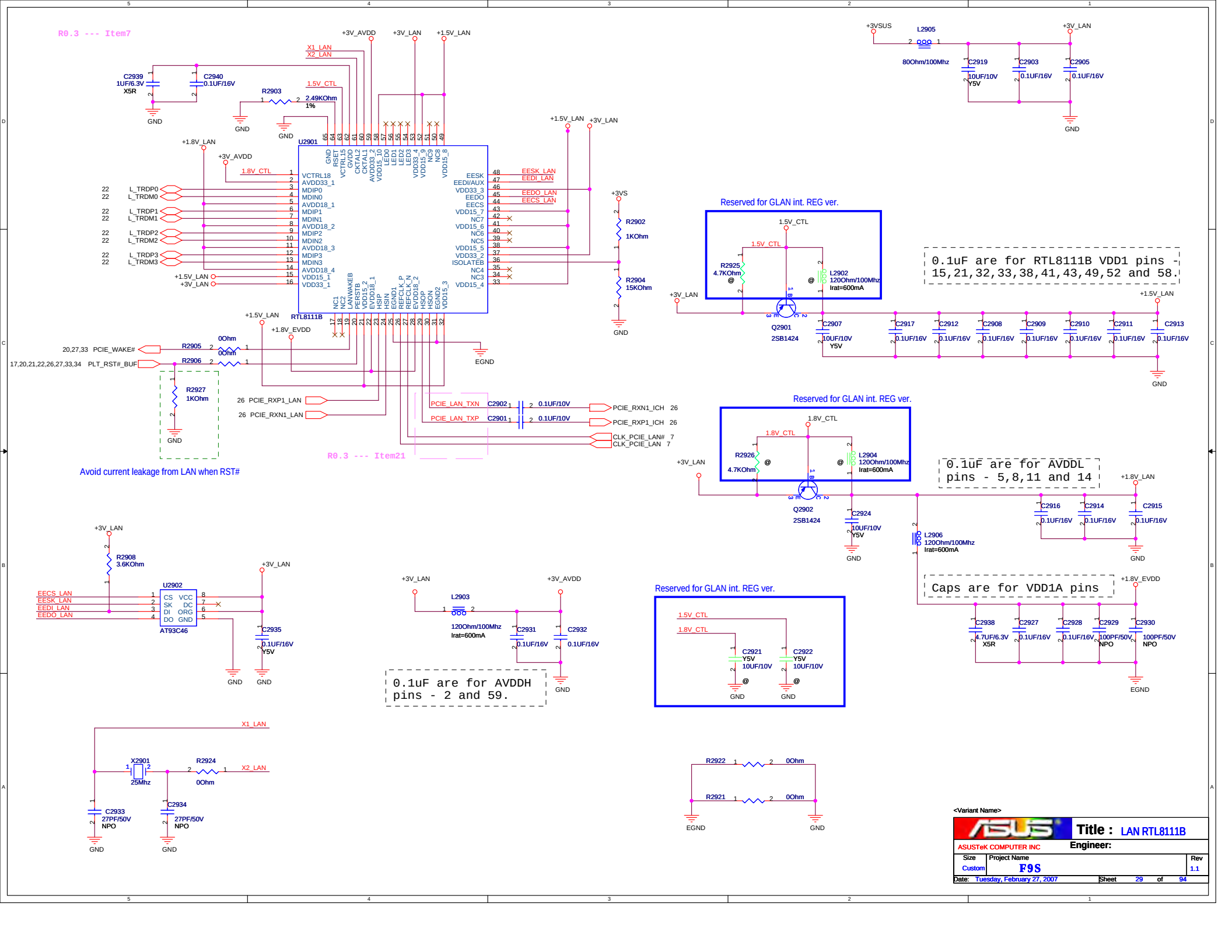

R0.3 --- Item7
U2901
RTL8111B
+3V_AVDD
+3V_LAN
+1.5V_LAN
+1.8V_LAN
+1.8V_EVDD
+3VS
+3VSUS
1.5V_CTL
1.8V_CTL
X1_LAN
X2_LAN
L_TRDP0
L_TRDM0
L_TRDP1
L_TRDM1
L_TRDP2
L_TRDM2
L_TRDP3
L_TRDM3
EESK_LAN
EEDI_LAN
EEDO_LAN
EECS_LAN
PCIE_WAKE#
PLT_RST#_BUF
PCIE_RXP1_LAN
PCIE_RXN1_LAN
PCIE_LAN_TXN
PCIE_LAN_TXP
PCIE_RXN1_ICH
PCIE_RXP1_ICH
CLK_PCIE_LAN#
CLK_PCIE_LAN
EGND
GND
Avoid current leakage from LAN when RST#
R0.3 --- Item21
Reserved for GLAN int. REG ver.
0.1uF are for RTL8111B VDD1 pins - 15,21,32,33,38,41,43,49,52 and 58.
0.1uF are for AVDDL pins - 5,8,11 and 14
0.1uF are for AVDDH pins - 2 and 59.
Caps are for VDD1A pins
AT93C46
Q2901
Q2902
2SB1424
L2902
L2903
L2904
L2905
L2906
120Ohm/100Mhz
Irat=600mA
80Ohm/100Mhz
25Mhz
<Variant Name>
Title : LAN RTL8111B
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9S
Rev 1.1
Date: Tuesday, February 27, 2007
Sheet 29 of 94

Title :

Engineer:

ASUSTek COMPUTER INC

Size	Project Name	Rev
Custom	F9S	1.1

Date: Thursday, February 08, 2007 Sheet 30 of 94

Title : EMPTY

ASUSTek COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Monday, February 05, 2007 Sheet 31 of 94

<Variant Name>

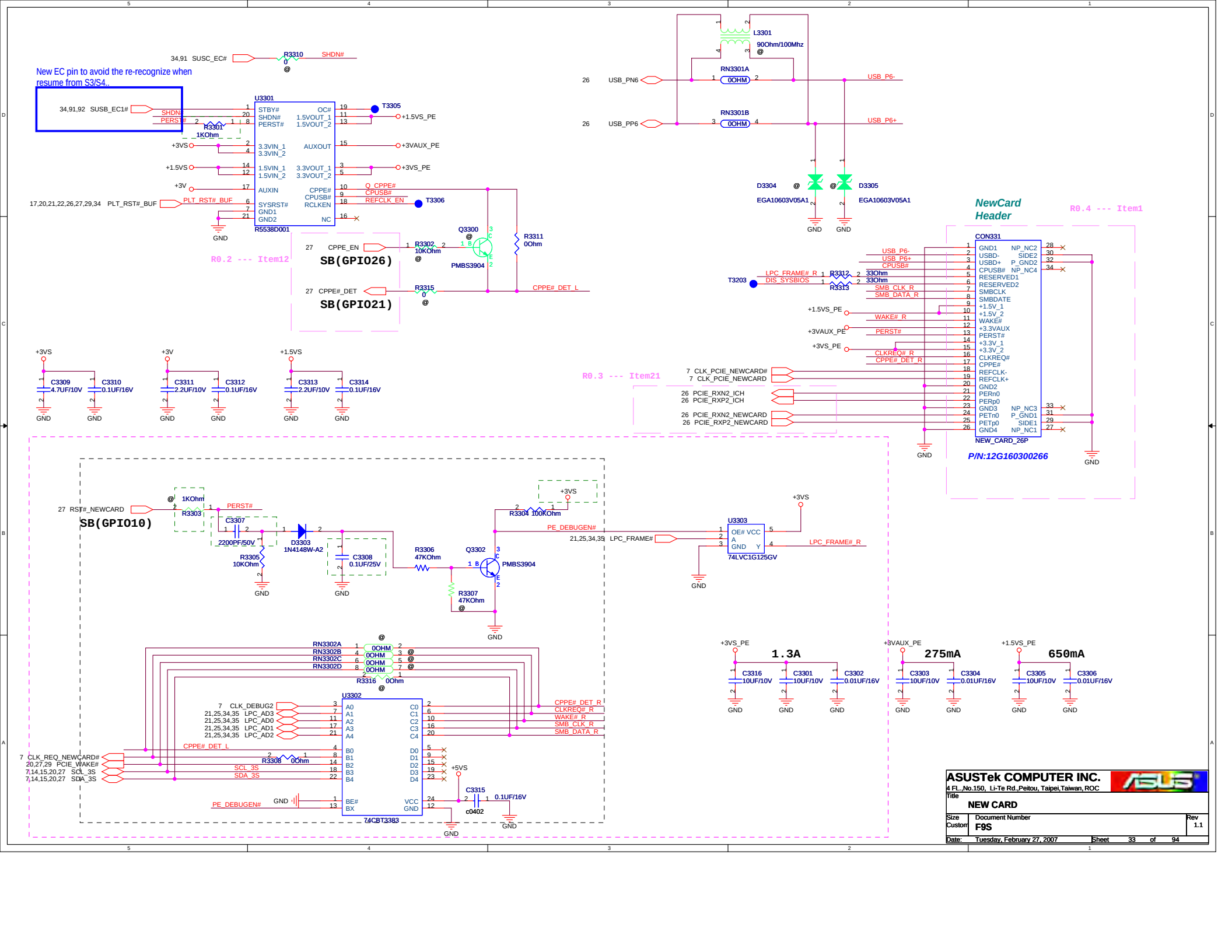
Title : EMPTY

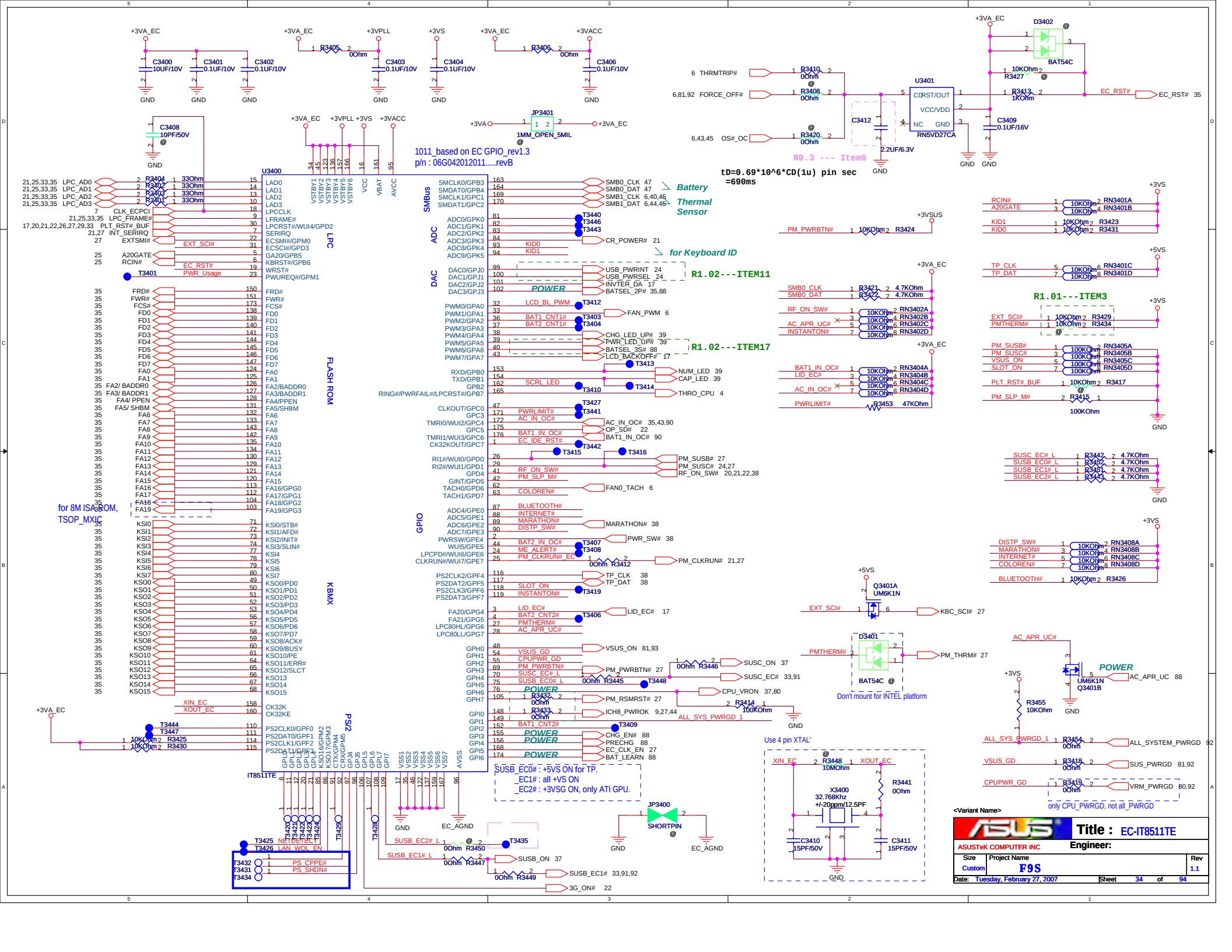
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Monday, February 05, 2007 Sheet 32 of 94


New EC pin to avoid the re-recognize when resume from S3/S4..
34,91 SUSC_EC#
R3310
SHDN#
34,91,92 SUSB_EC1#
U3301
R5538D001
R3301
1KOhm
+3VS
+1.5VS
+3V
17,20,21,22,26,27,29,34 PLT_RST#_BUF
PLT_RST#_BUF
GND
T3305
T3306
+1.5VS_PE
+3VAUX_PE
+3VS_PE
Q_CPPE#
CPUSB#
REFCLK_EN
R0.2 --- Item12
27 CPPE_EN
SB(GPIO26)
Q3300
PMBS3904
R3302
10KOhm
R3311
0Ohm
27 CPPE#_DET
SB(GPIO21)
R3315
CPPE#_DET_L
L3301
90Ohm/100Mhz
RN3301A
RN3301B
0OHM
26 USB_PN6
26 USB_PP6
USB_P6-
USB_P6+
D3304
D3305
EGA10603V05A1
NewCard Header
R0.4 --- Item1
CON331
NEW_CARD_26P
P/N:12G160300266
T3203
LPC_FRAME# R
DIS_SYSBIOS
R3312
R3313
33Ohm
SMB_CLK_R
SMB_DATA_R
WAKE# R
PERST#
CLKREQ# R
CPPE#_DET_R
R0.3 --- Item21
7 CLK_PCIE_NEWCARD#
7 CLK_PCIE_NEWCARD
26 PCIE_RXN2_ICH
26 PCIE_RXP2_ICH
26 PCIE_RXN2_NEWCARD
26 PCIE_RXP2_NEWCARD
C3309 4.7UF/10V
C3310 0.1UF/16V
C3311 2.2UF/10V
C3312 0.1UF/16V
C3313 2.2UF/10V
C3314 0.1UF/16V
27 RST#_NEWCARD
SB(GPIO10)
C3307
2200PF/50V
D3303
1N4148W-A2
R3305
10KOhm
C3308
0.1UF/25V
R3306
47KOhm
R3307
R3304 100KOhm
PE_DEBUGEN#
21,25,34,35 LPC_FRAME#
U3303
74LVC1G125GV
RN3302A
RN3302B
RN3302C
RN3302D
R3316
U3302
74CBT3383
7 CLK_DEBUG2
21,25,34,35 LPC_AD3
21,25,34,35 LPC_AD0
21,25,34,35 LPC_AD1
21,25,34,35 LPC_AD2
CPPE#_DET_L
7 CLK_REQ_NEWCARD#
20,27,29 PCIE_WAKE#
7,14,15,20,27 SCL_3S
7,14,15,20,27 SDA_3S
R3308
SCL_3S
SDA_3S
PE_DEBUGEN#
+5VS
C3315
c0402
0.1UF/16V
+3VS_PE
1.3A
C3316 10UF/10V
C3301 10UF/10V
C3302 0.01UF/16V
+3VAUX_PE
275mA
C3303 10UF/10V
C3304 0.01UF/16V
+1.5VS_PE
650mA
C3305 10UF/10V
C3306 0.01UF/16V
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC
Title
NEW CARD
Size Custom
Document Number F9S
Rev 1.1
Date: Tuesday, February 27, 2007
Sheet 33 of 94


U3400
IT8511TE
1011_based on EC GPIO_rev1.3
p/n : 06G042012011.....revB
LPC
FLASH ROM
KBMX
PS2
SMBus
ADC
DAC
GPIO
Battery
Thermal Sensor
for Keyboard ID
R1.02---ITEM11
R1.02---ITEM17
R1.01---ITEM3
POWER
for 8M ISA ROM, TSOP_MXIC
SUSB_EC0# : +5VS ON for TP.
_EC1# : all +VS ON
_EC2# : +3VSG ON, only ATI GPU.
tD=0.69*10^6*CD(1u) pin sec
=690ms
R0.3 --- Item6
U3401
RN5VD27CA
D3402
BAT54C
Q3401A
UM6K1N
D3401
BAT54C @
Don't mount for INTEL platform
Use 4 pin XTAL'
X3400
32.768Khz
+/-20ppm/12.5PF
JP3401
1MM_OPEN_5MIL
JP3400
SHORTPIN
Title : EC-IT8511TE
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9S
Rev 1.1
Date: Tuesday, February 27, 2007
Sheet 34 of 94

EC Hardware Strapping

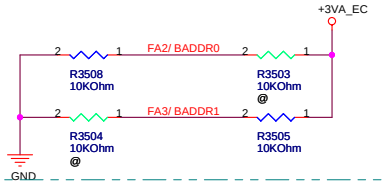
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

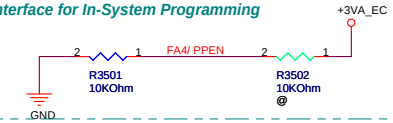


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



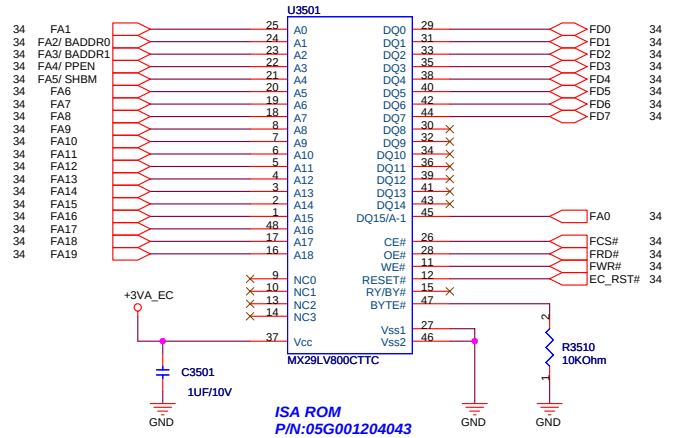
FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS

ISA ROM_TSOP

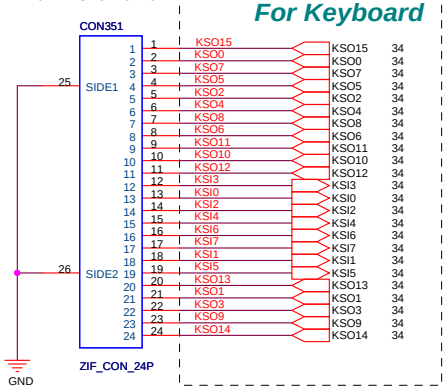
8M TSOP _ MXIC



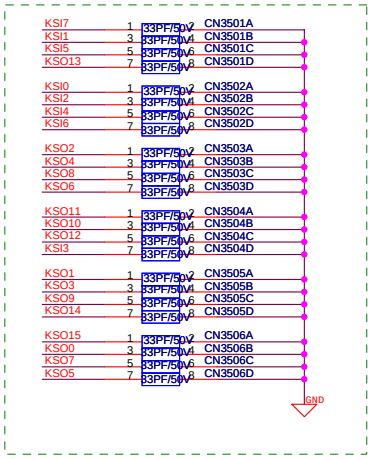
ISA ROM
P/N:05G001204043

For Keyboard

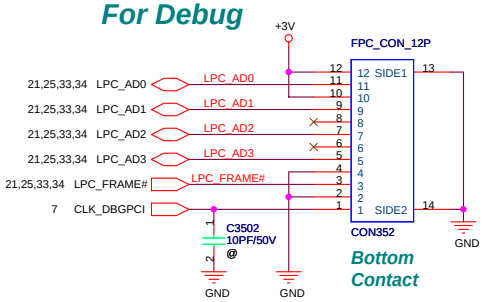
P/N:12G182402404



R1.3---ITEM38



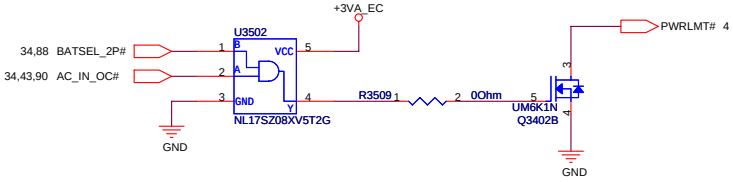
For Debug



Bottom Contact

R1.03---ITEM28

PWRLMT Circuit: For Battery 1P



<Variant Name>

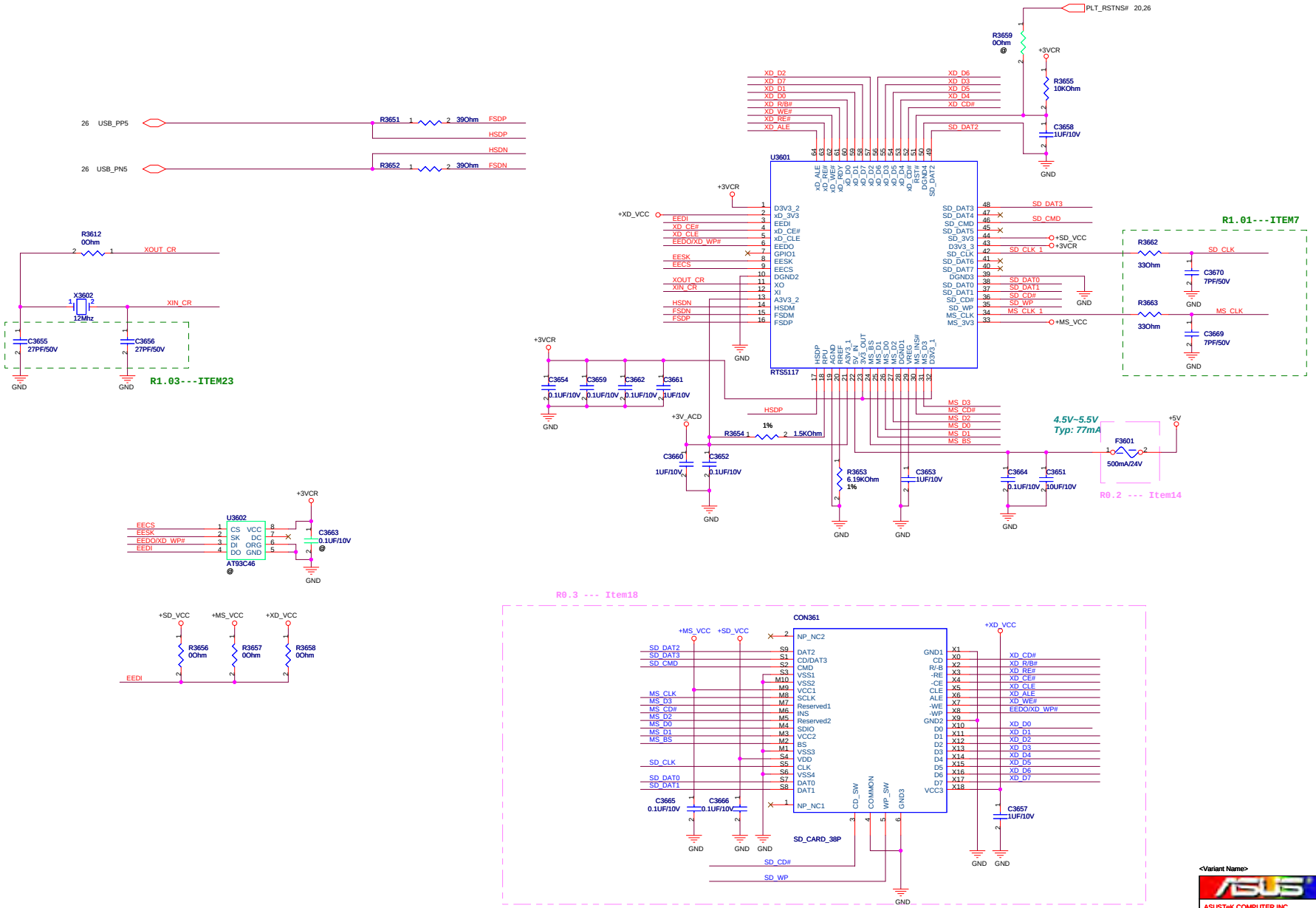
ASUSTeK COMPUTER INC

Title : ISA_ROM&KB conn

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 35 of 94



<Variant Name>

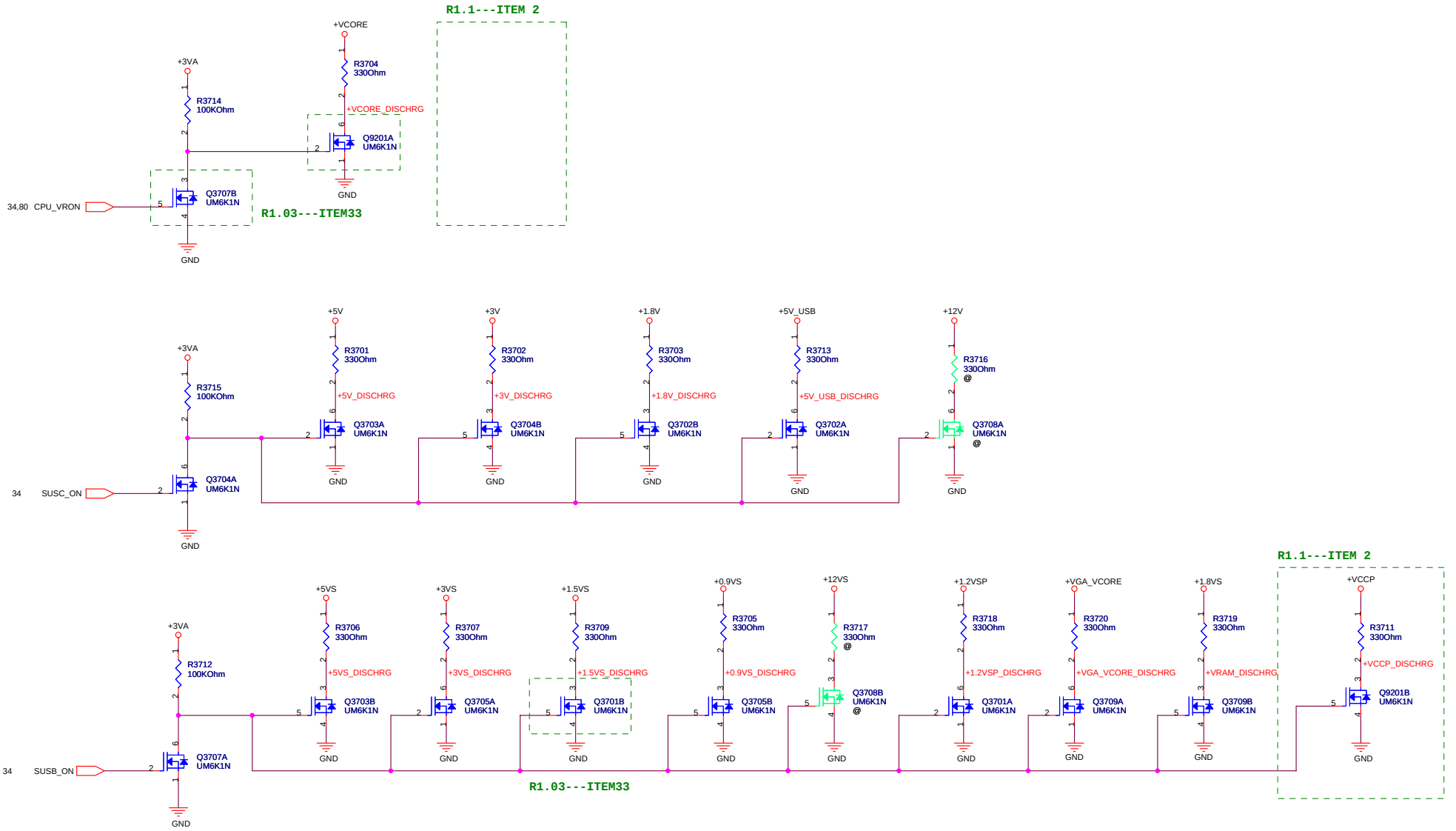
ASUSTeK COMPUTER INC

Title : RTS5117

Engineer:

Size	Project Name	Rev
C	F9S	1.1

Date: Tuesday, March 06, 2007 Sheet 36 of 94



<Variant Name>

Title : DISCHARGE

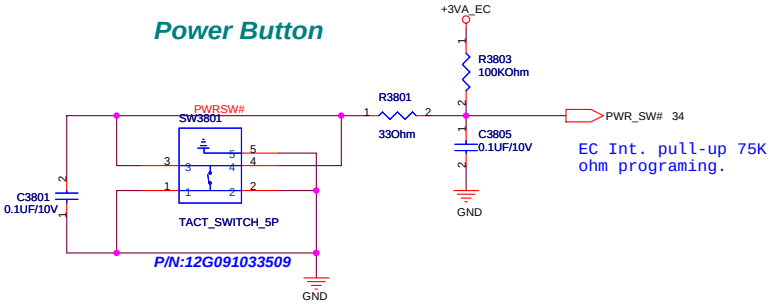
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

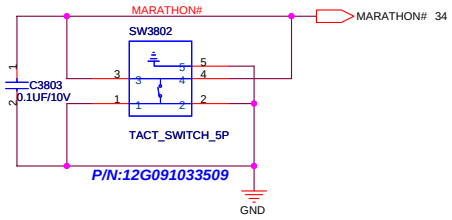
Date: Tuesday, February 27, 2007 Sheet 37 of 94

Power Button

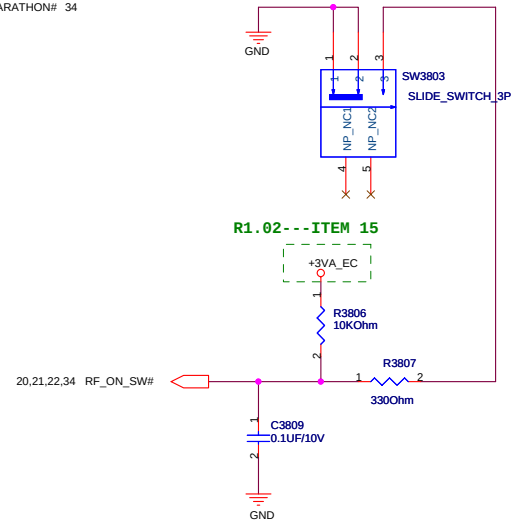


EC Int. pull-up 75K ohm programing.

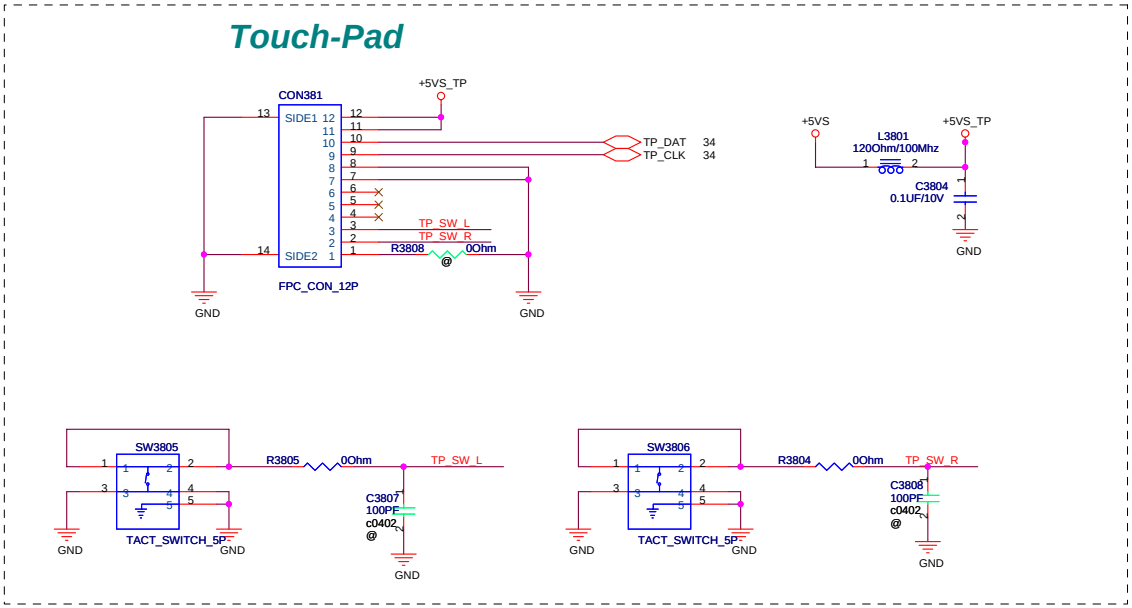
MARATHON#



BT/WLAN SW



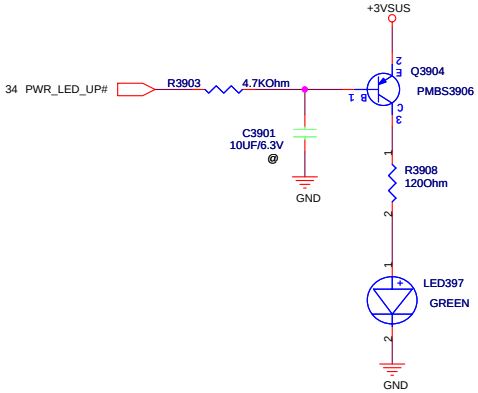
Touch-Pad



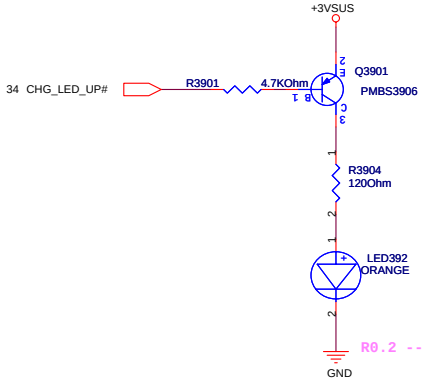
<Variant Name>

ASUSTeK COMPUTER INC	Title : KEY & LED	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 38 of 94	

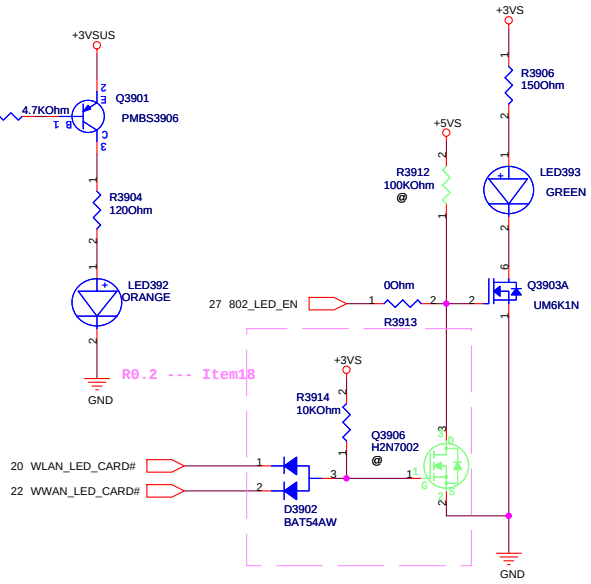
PWR LED



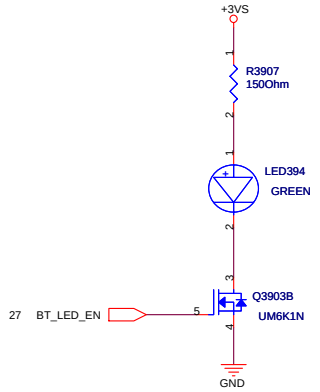
BATTERY LED



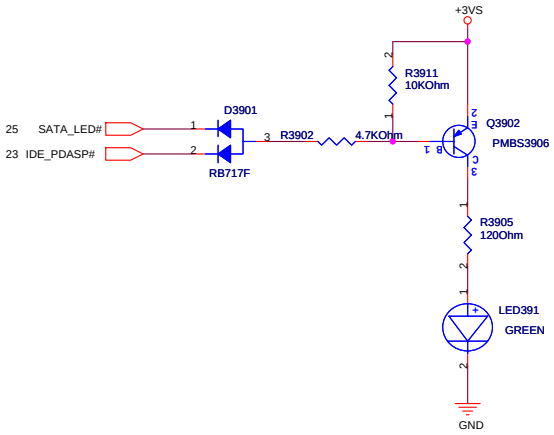
WireLess LED



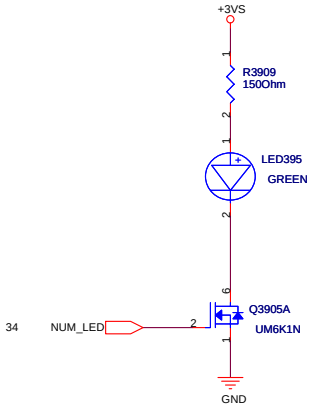
BT LED



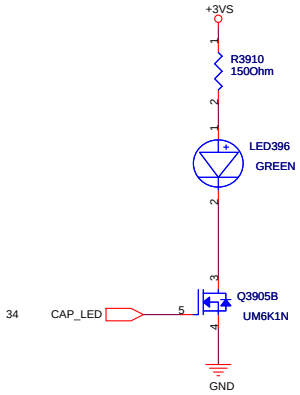
SATA/IDE LED



Num Lock

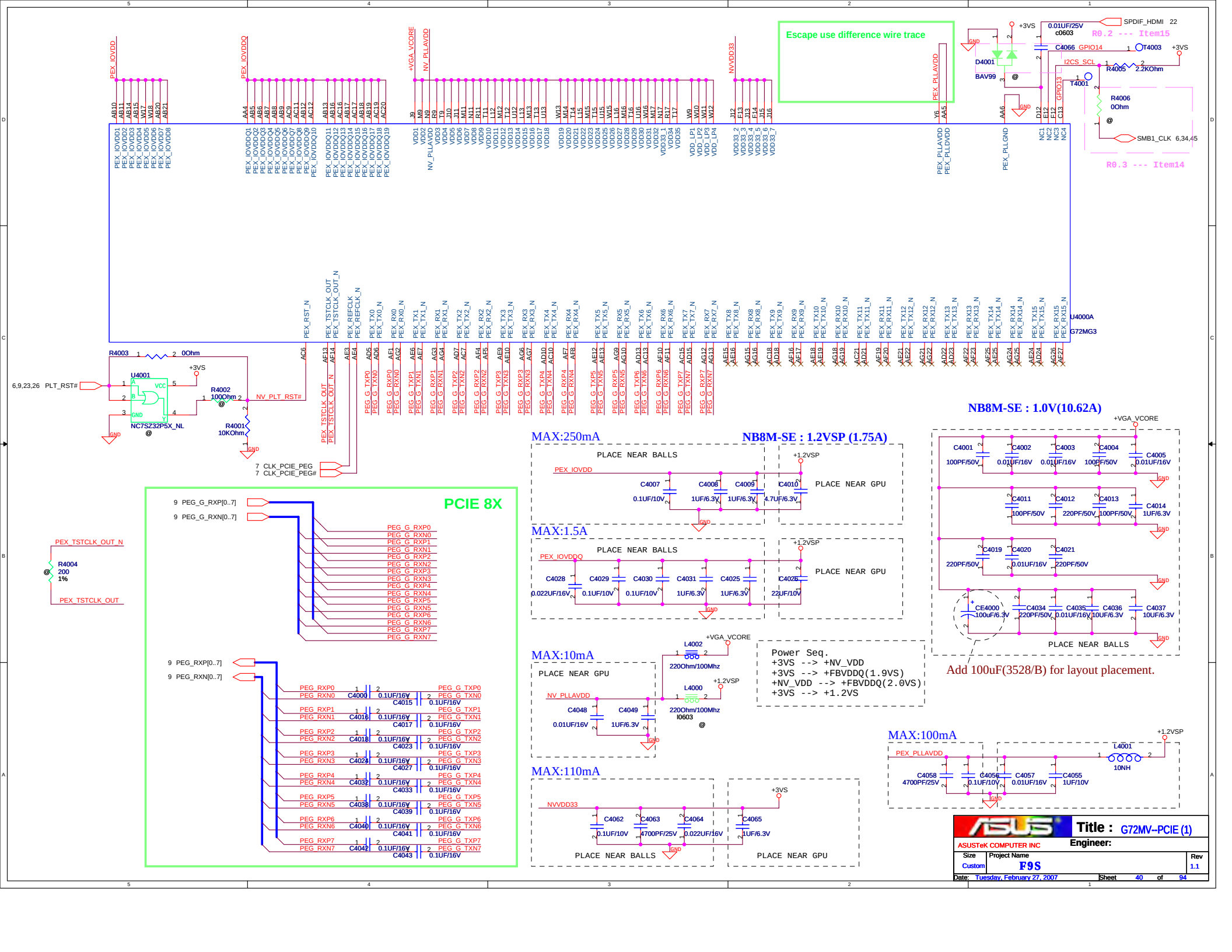


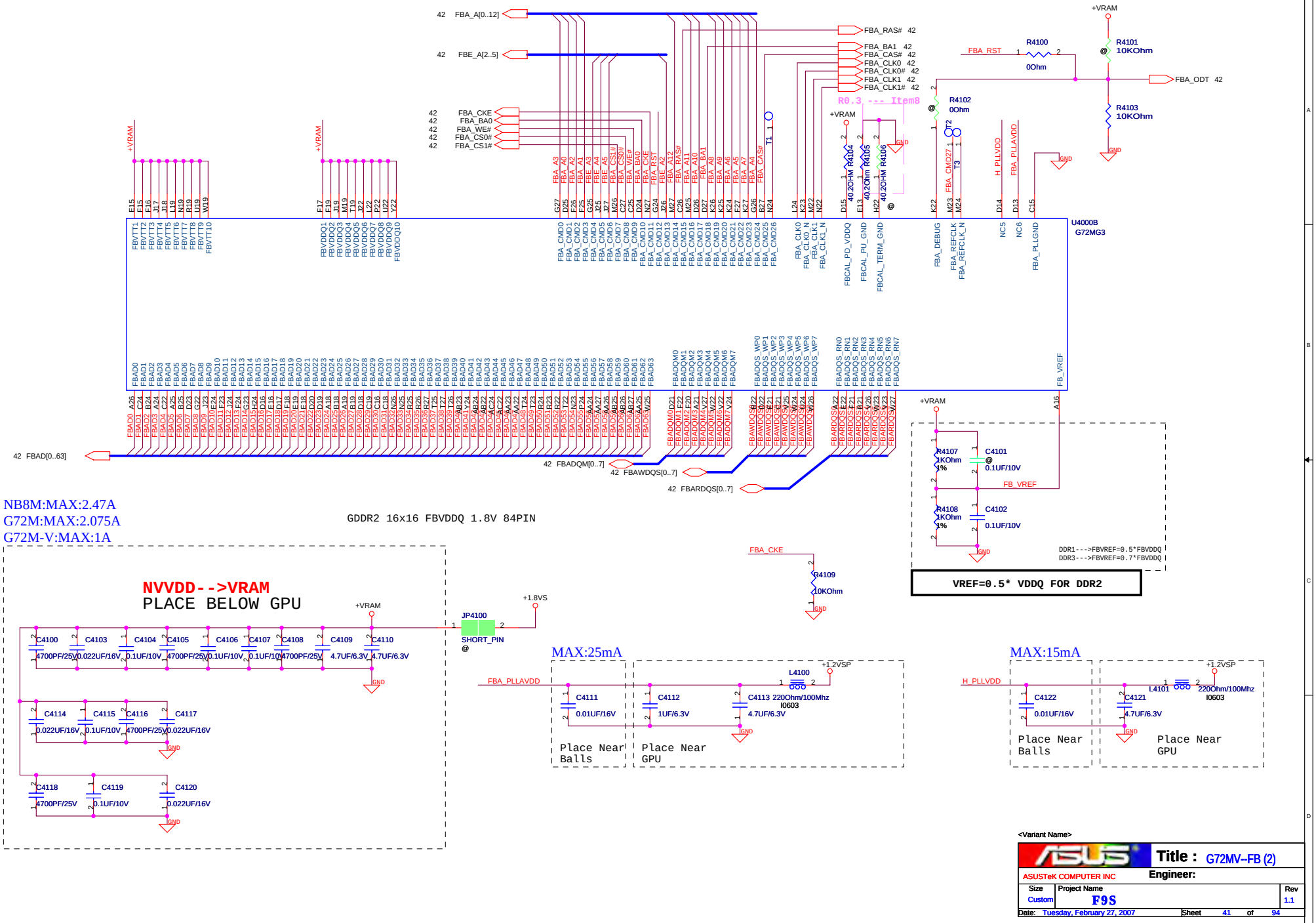
Cap. Lock



<Variant Name>

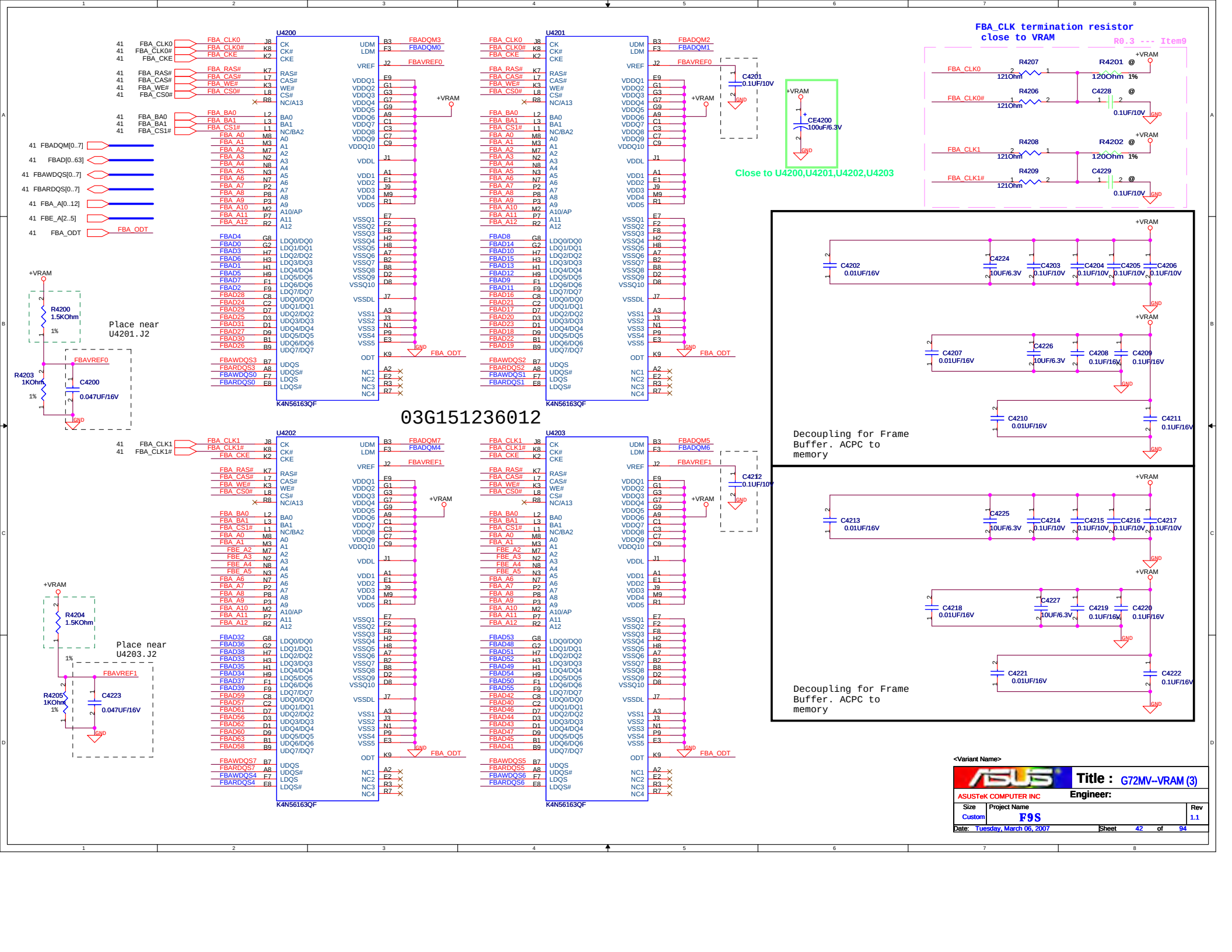
ASUSTeK COMPUTER INC	Title : LEDs	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 39 of 94	

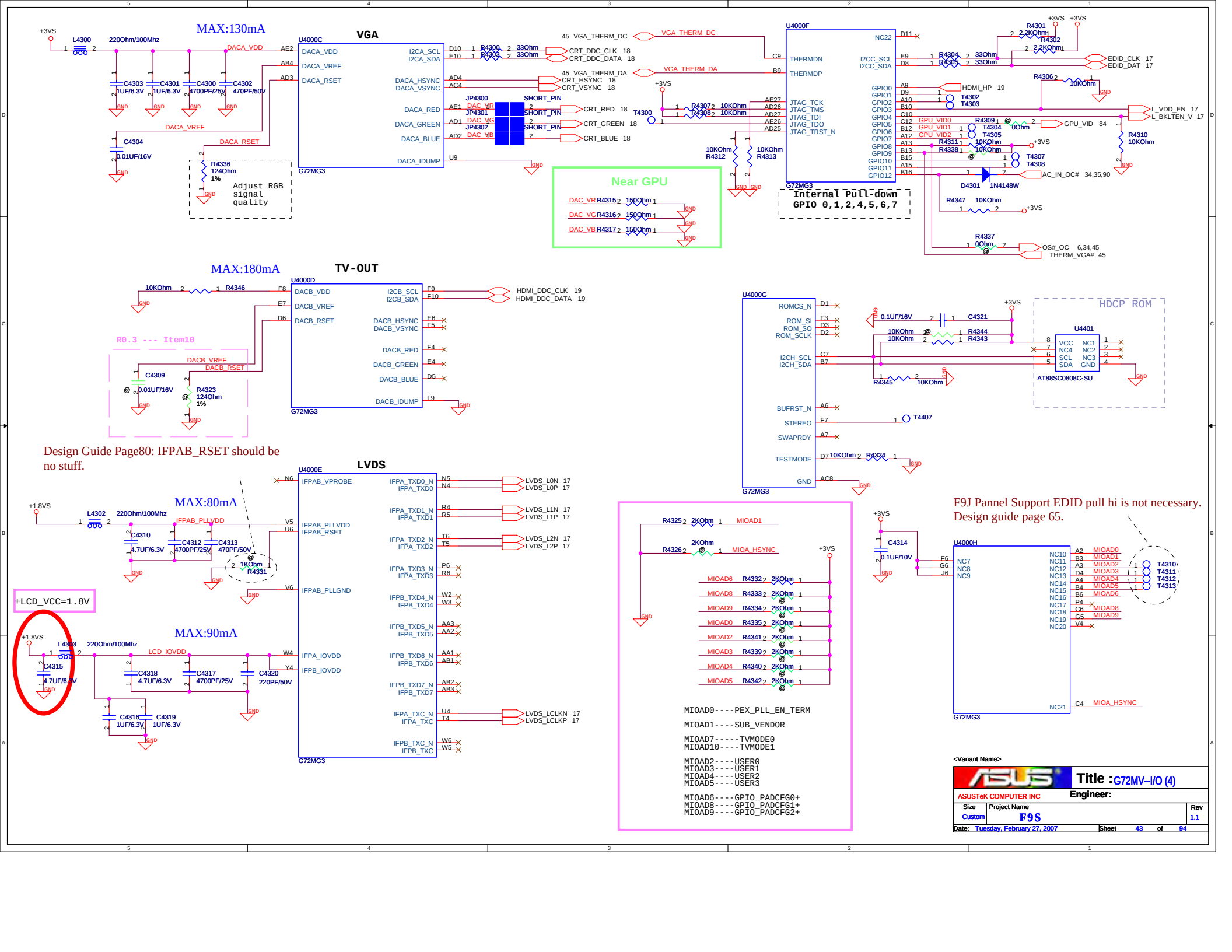

Escape use difference wire trace
U4000A
G72MG3
PCIE 8X
NB8M-SE : 1.0V(10.62A)
NB8M-SE : 1.2VSP (1.75A)
MAX:250mA
MAX:1.5A
MAX:10mA
MAX:110mA
MAX:100mA
Power Seq.
+3VS --> +NV_VDD
+3VS --> +FBVDDQ(1.9VS)
+NV_VDD --> +FBVDDQ(2.0VS)
+3VS --> +1.2VS
Add 100uF(3528/B) for layout placement.
Title : G72MV--PCIE (1)
ASUSTeK COMPUTER INC
Engineer:
Project Name F9S
Rev 1.1
Date: Tuesday, February 27, 2007
Sheet 40 of 94

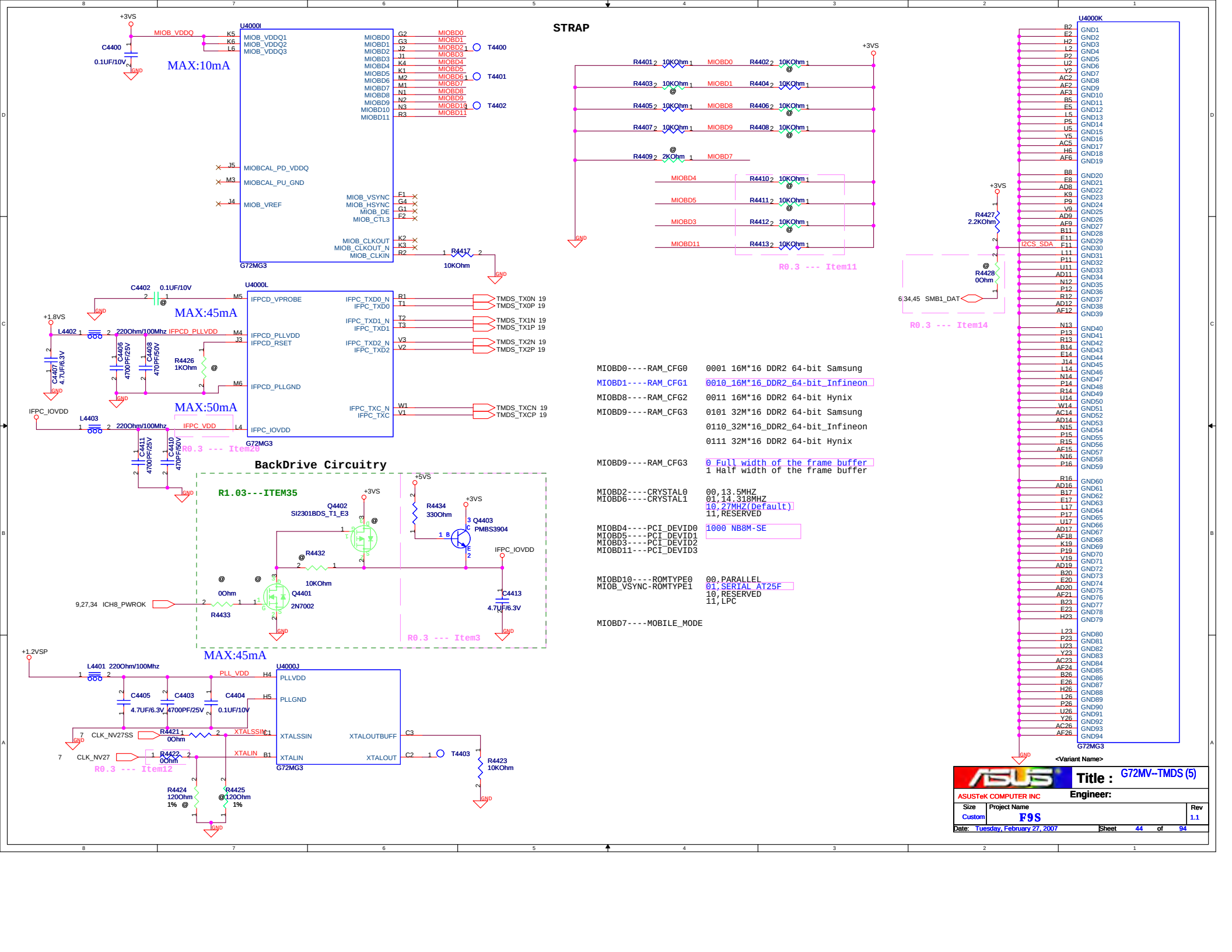


<Variant Name>

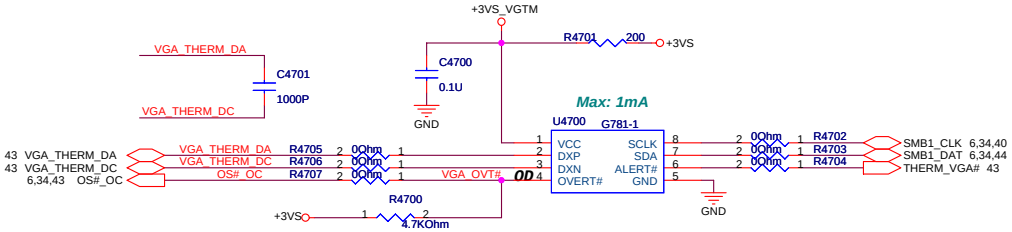
ASUSTeK COMPUTER INC	Title : G72MV-FB (2)	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 41 of 94	


FBA_CLK termination resistor close to VRAM
R0.3 --- Item9
Close to U4200,U4201,U4202,U4203
03G151236012
U4200
U4201
U4202
U4203
K4N56163QF
Place near U4201.J2
Place near U4203.J2
Decoupling for Frame Buffer. ACPC to memory
Decoupling for Frame Buffer. ACPC to memory
<Variant Name>
Title : G72MV--VRAM (3)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9S
Rev 1.1
Date: Tuesday, March 06, 2007
Sheet 42 of 94


MAX:130mA
VGA
U4000C
G72MG3
Adjust RGB signal quality
Near GPU
U4000F
Internal Pull-down GPIO 0,1,2,4,5,6,7
MAX:180mA
TV-OUT
U4000D
HDCP ROM
U4000G
U4401
AT88SC0808C-SU
Design Guide Page80: IFPAB_RSET should be no stuff.
LVDS
U4000E
MAX:80mA
MAX:90mA
+LCD_VCC=1.8V
F9J Pannel Support EDID pull hi is not necessary. Design guide page 65.
U4000H
MIOAD0----PEX_PLL_EN_TERM
MIOAD1----SUB_VENDOR
MIOAD7-----TVMODE0
MIOAD10----TVMODE1
MIOAD2----USER0
MIOAD3----USER1
MIOAD4----USER2
MIOAD5----USER3
MIOAD6----GPIO_PADCFG0+
MIOAD8----GPIO_PADCFG1+
MIOAD9----GPIO_PADCFG2+
<Variant Name>
Title : G72MV--I/O (4)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9S
Rev 1.1
Date: Tuesday, February 27, 2007
Sheet 43 of 94


STRAP
U4000I
G72MG3
MIOB_VDDQ
MIOB_VDDQ1
MIOB_VDDQ2
MIOB_VDDQ3
C4400
0.1UF/10V
MAX:10mA
MIOBD0
MIOBD1
MIOBD2
MIOBD3
MIOBD4
MIOBD5
MIOBD6
MIOBD7
MIOBD8
MIOBD9
MIOBD10
MIOBD11
T4400
T4401
T4402
MIOBCAL_PD_VDDQ
MIOBCAL_PU_GND
MIOB_VREF
MIOB_VSYNC
MIOB_HSYNC
MIOB_DE
MIOB_CTL3
MIOB_CLKOUT
MIOB_CLKOUT_N
MIOB_CLKIN
R4417
10KOhm
U4000L
C4402
0.1UF/10V
MAX:45mA
IFPCD_VPROBE
IFPCD_PLLVDD
IFPCD_RSET
IFPCD_PLLGND
IFPC_TXD0_N
IFPC_TXD0
IFPC_TXD1_N
IFPC_TXD1
IFPC_TXD2_N
IFPC_TXD2
IFPC_TXC_N
IFPC_TXC
IFPC_IOVDD
TMDS_TX0N 19
TMDS_TX0P 19
TMDS_TX1N 19
TMDS_TX1P 19
TMDS_TX2N 19
TMDS_TX2P 19
TMDS_TXCN 19
TMDS_TXCP 19
+1.8VS
L4402
220Ohm/100Mhz
IFPCD_PLLVDD
C4406
4700PF/25V
C4408
470PF/50V
C4407
4.7UF/6.3V
R4426
1KOhm
MAX:50mA
IFPC_VDD
L4403
C4411
4700PF/25V
C4410
470PF/50V
R0.3 --- Item20
BackDrive Circuitry
R1.03---ITEM35
Q4402
SI2301BDS_T1_E3
R4434
330Ohm
Q4403
PMBS3904
R4432
10KOhm
Q4401
2N7002
0Ohm
R4433
9,27,34 ICH8_PWROK
C4413
4.7UF/6.3V
R0.3 --- Item3
MAX:45mA
+1.2VSP
L4401
220Ohm/100Mhz
U4000J
PLL_VDD
PLLVDD
PLLGND
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
C4405
4.7UF/6.3V
C4403
4700PF/25V
C4404
0.1UF/10V
CLK_NV27SS
CLK_NV27
R4421
0Ohm
R4422
0Ohm
R0.3 --- Item12
T4403
R4423
10KOhm
R4424
120Ohm
1%
R4425
120Ohm
1%
R4401
R4402
R4403
R4404
R4405
R4406
R4407
R4408
R4409
10KOhm
2KOhm
MIOBD4
MIOBD5
MIOBD3
MIOBD11
R4410
R4411
R4412
R4413
R0.3 --- Item11
R4427
2.2KOhm
R4428
0Ohm
I2CS_SDA
6,34,45 SMB1_DAT
R0.3 --- Item14
U4000K
G72MG3
<Variant Name>
MIOBD0----RAM_CFG0 0001 16M*16 DDR2 64-bit Samsung
MIOBD1----RAM_CFG1 0010_16M*16_DDR2_64-bit_Infineon
MIOBD8----RAM_CFG2 0011 16M*16 DDR2 64-bit Hynix
MIOBD9----RAM_CFG3 0101 32M*16 DDR2 64-bit Samsung
0110_32M*16_DDR2_64-bit_Infineon
0111 32M*16 DDR2 64-bit Hynix
MIOBD9----RAM_CFG3 0 Full width of the frame buffer
1 Half width of the frame buffer
MIOBD2----CRYSTAL0 00,13.5MHZ
MIOBD6----CRYSTAL1 01,14.318MHZ
10,27MHZ(Default)
11,RESERVED
MIOBD4----PCI_DEVID0 1000 NB8M-SE
MIOBD5----PCI_DEVID1
MIOBD3----PCI_DEVID2
MIOBD11---PCI_DEVID3
MIOBD10----ROMTYPE0 00,PARALLEL
MIOB_VSYNC-ROMTYPE1 01,SERIAL_AT25F
10,RESERVED
11,LPC
MIOBD7----MOBILE_MODE
Title : G72MV--TMDS (5)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9S
Rev 1.1
Date: Tuesday, February 27, 2007
Sheet 44 of 94

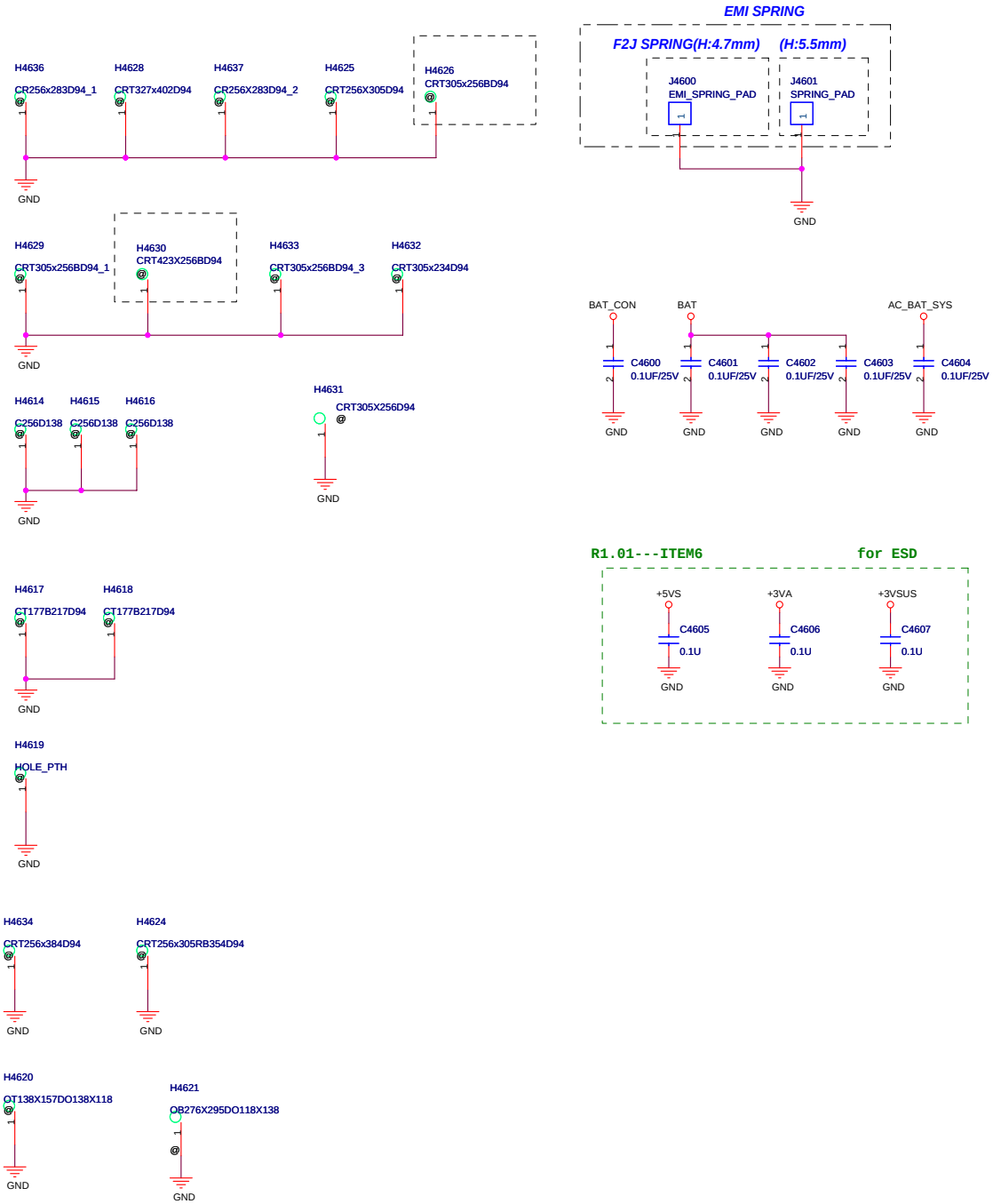
Slave Address:9A



For frame buffer address/command lines those external pull up resistor can be removed for easy layout from Nvidia FAE

<Variant Name>

ASUSTeK COMPUTER INC	Title G72MV--VRAM_TERM	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 45 of 94	



<Variant Name>

ASUSTeK COMPUTER INC

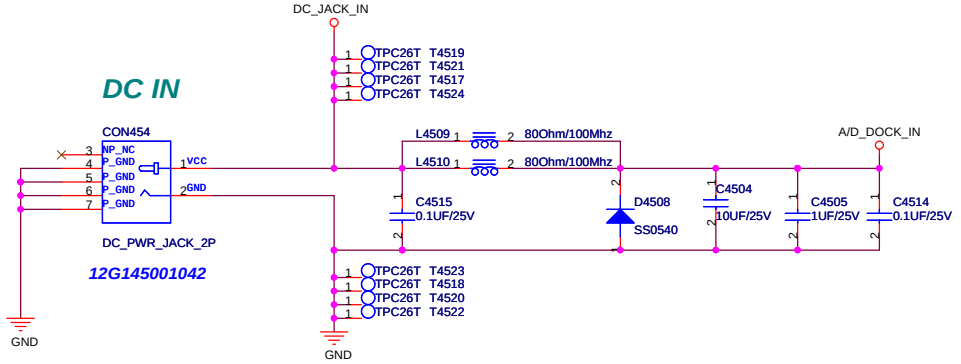
Title : SREW HOLE

Engineer:

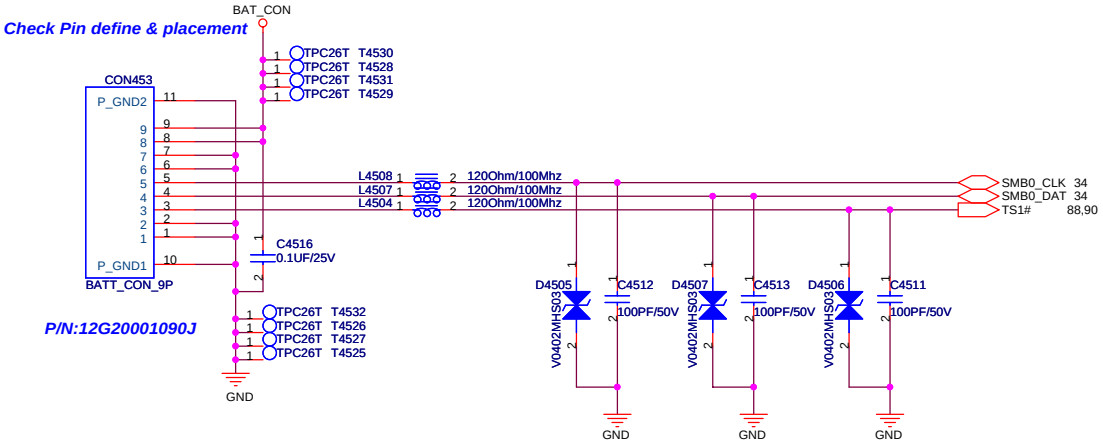
Size	Project Name	Rev
Custom	F9S	1.1

Date: Monday, February 05, 2007 Sheet 46 of 94

DC IN



BAT IN



<Variant Name>

ASUSTeK COMPUTER INC	Title : G72M-Terminator	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 47 of 94	

F9S SR_1128(R0.1---->R0.2)

(1)Delete R0930,R0931 to follow Intel spec.---page9
(2)Mount R1301 for DMI x2 ---page13
(3)Modify netname USBP1 to USBP2 ---page17
(4)Modify U1803,U1804 to N/A and R1817,R1818 connect to CRT_VSYNC,CRT_HSYNC ---page18
(5)change TMDS pull high from +3VS to IFPC_IOVDD ---page19
(6)Modify netname SUS_STAT# to PM_SUS_STAT# ---page21
(7)Add signal for 1G LAN, ---page22
Delete R2201,R2202,Q2201,Q2202 and Modify netname ----- page22
(8)Modify netname to IRQ14 ---page23
(9)Delete E-SATA signal and add R2532,R2533 ---page25
(10)Add test point T2717,T2719 ---page27
(11)change 10/100 LAN to 10/100/1000 LAN(RTL811B) ---page29
(12)Modify debug circuit ---page33
(13)Modify single netname ---page34
(14)Modify F3601 to 0.5A ---page36
(15)Add C4066 ,D4001 for SPDIF_HDMI ---page40
(16)Add R4434 to N/A ---page44
(17)Add R0785,R0786,R0787 to follow Intel for CPU_BSEL ---page7
(18)Add D3902,R3914,Q3906,R3912 for WLAN,WWAN LED(reserve) ---page39
(19)Delete R0765,R0766,R0781,R0782,R0761,R0763 ---page7
(20)Change CON2201 pin9 from +1.8V_LAN to GND---page22

F9S SR_1130(R0.2---->R0.3)

(1)Delete CN1500 and add C1515~C1518---page15
(2)DMI change to 2X---page9,26
(3)Modify backdrive circuitry ---page44
(4)Modify F1701 from 0.2A to 0.5A ---page17
(5)Add R1702,C1714,Q1703 to reserve it for LCD power---page17
(6)Delete R0719,R0721,R0723---page7
(7)Modify L2902,L2903,L2904 size and add L2905,L2906 ---page29
(8)R4105 change to 40ohm instead of 30ohm,and R4106 to N/A ---page41
(9)Reserve FBA_CLKx clock terminator for NB8M-SE memory tuning---page42
(10)Due to without TV function,C4309 and R4323 to N/A---page43
(11)PCI_DEVICEID please set to "1000" for NB8M-SE--page44
(12)For NB8M-SE ext. 27Mhz can connect directly without level shift, R4422 use 0 ohm is ok--page44
(13)For frame buffer address/command lines those external pull up resistor can be removed for easy layout.-page45
(14)I2CS_SCL and I2C_SDA to EC to access NB8M-SE internal thermal sensor---page40,44
(15)Delete power limit circuit due to EC change to IT8511TE--page35
(16)BT_DET# connect 3Vs to avoid the leakage-----Page27
(17)Change the ODD CON(CON232) from 12G16121050P to 12G161240501 for ME request. (Board lock hole:1.8mm; 3.0H)---Page23
(18)CON361 change from 12G340003800 to 12G340003810 to improve the yield rate.--Page36
(19)Add R1210,R1211 connect to GND for intel recommendation Rev1.5----page12
(20)To modify duplicated netname from IFPC_IOVDD to IFPC_VDD ---page44
(21)To modify duplicated netname of PCIE signal ---page29,33
(22)Change RN2700 to 0402 size and no mount R2756 for Intel recommendation---page27
(23)Change C2812,R2803 size from 0805 to 0603 for layout request.---page28
(24)DDR SWAP for layout request---page14,15
(25)Delete R3708,Q3710 due to +2.5VS power no use---page37
(26)Add Q1802 to avoid current leakage from CRT device---page18

F9S SR_1130(R0.3---->R0.4 same as R1.0)

(1)Change Newcard header H=3.2 and card ejector for F9S/E---page33
(2)C3658/C3655 change from 15pF to 18pF for card reader crystal adjustment.---page36
(3)No Mount R3806,to avoid +3VA_EC leakage to +3Vs--page38
(4)Add C2843,C2844 connect to GND for intel recommendation--page28
(5)Change C06XX from 10U to 22U for intel recommendation---page06
(6)Change C3412 from 1U to 2.2U and delay EC_RST#---page34
(7)R2308 reserve high change to pull low for intel recommendation. ---page23
(8)Add R2306 33ohm for checklist ---page24
(9)Add Q1901,R1928,R1929 to avoid leakage for HDMI DDC clk, and Data---page19
(10)Add R3660,R3661,C3667,C3668(SD and MS CLK) for EMI request ---page36

F9S ER_0122(R1.0---->R1.01)

(1)Add C2201 ~ C2208 for EMI request ---page22
(2)Change +VCCP discharge by SUSB_ON for the correspondence with power enable ----page37
(3)Change RES. 4R8P RN3403 to single RES R3429, R3434 for uncertain PMTHERM# leakag ---page34
(4)Delete D1901 and add Q1902 and R1926,R1927 change to 1.8K ohm for HDMI spec. ---page19
(5)+5VS_CRT change to +5VS_HDMI_CRT and D1806 to DNI ---page18
(6)Add C4605,C4606,C4607 0.1uf cap. for ESD ---page46
(7)R3660,R3661 mount 33 0hm and C3667,C3668 mount 10p for EMI issue---page36
(8)Power change to AC_BAT_SYS_INV for layout improve---page17
(9)Change D2401 ,D2400 part from RSB6.8S to EGA10603V05A1---page24

F9S ER_0125(R1.01---->R1.02)

(10)Add C2108 0.1uf cap. for ESD---page21
(11)Add USB Port Charging Function on S4/ S5---page24
(12))Add OS#_OC to FAN---page6
(13)Change R0402 from 68 ohm to 1k ohm 1% because it can fixes the PROCHOT# failure when driven by thermal sensor on the CRB.----page4
(14)Delete C0401 for intel recommend.---page4
(15)Change WLAN SW pull up to +3VA_EC for leakage prevention.--page38
(16)Del D0701,D0702 and add R785,R786 because there is no leakage at S3/S4 or card insertion.---page7
(17)Power add BATSEL_3S# connect to EC.---page34
(18)DNI useless U2603 and C2606.---page26
(19)Reserve a RES R2754 to pull up PM_RSMRST# to +3VSUS.---page27
(20)Change net name PM_RSMRST# to PM_RSMRST#_SB to pull up +3VSUS & add D2701 for leakage prevention.---page27

F9S ER_0126(R1.02---->R1.03 same as R1.1)

(21)Add PLT_RST#_BUF for Sierra card moderm reset signal MDL_RESET#.---page22
(22)Change C2500,C2502 from 22pF to 15pF to meet XTAL requirement---page25
(23)C3656/C3655 change from 18pF to 27pF to meet XTAL requirement---page36
(24)Change R0712 from 220 ohm to 270 ohm for clock signal quality improvement.--page07
(25)Change L1811,L1812,L1813 from BEAD 120ohm to 82nH and C1832,C1834,C1836 from 22p to 10p for CRT signal quality---page18
(26)Change Q2405,Q2407 2N7002 to UM6K1N ---page24
(27)Add R2409,R2410 to reserve +5VSUS for SN74CBTD3306 5V power. ---page24
(28)PWRLMT Circuit: For Battery 1P ---page35
(29)SWAP +3V and +3VS power for 3G requirement ---page22
(30)Add C0719,C0721 for 3G requirement ---page07
(31)Mount L1709 common mode choke for 3G requirement---page17
(32)Add C1715,C1716 for 3G requirement---page17
(33)To combine UM6K1N for cost down :delete Q3706,Q9202,Q9203---page37
(34)R1705 from 100 ohm change to 390 ohm for LCD power off sequence---page17
(35)Mount Q4403 and remove Q4402,Q4401,R4432,R4433 for cost down---page44

F9S ER_0207(R1.1---->R1.2)

(36)LVDS conn. pin modification for LVDS coxal cable---page17

F9S ER_0215(R1.2---->R1.3)

(37)Power team modify +1.5VS power rating to 3.5A ---page82
(38)Add CN3501~CN3506 for 3G requirement---page35
(39)Change CLK_TPMPCI R0707 from 33 ohm to 27 ohm and mount C0725(10p) to meet edge rate spec---page36

ASUSTeK COMPUTER INC	Title : History(1)	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Thursday, March 01, 2007	Sheet 48 of 94	

F9S ER_0122(R1.0---->R1.01 same as R1.1)---------POWER

change list:

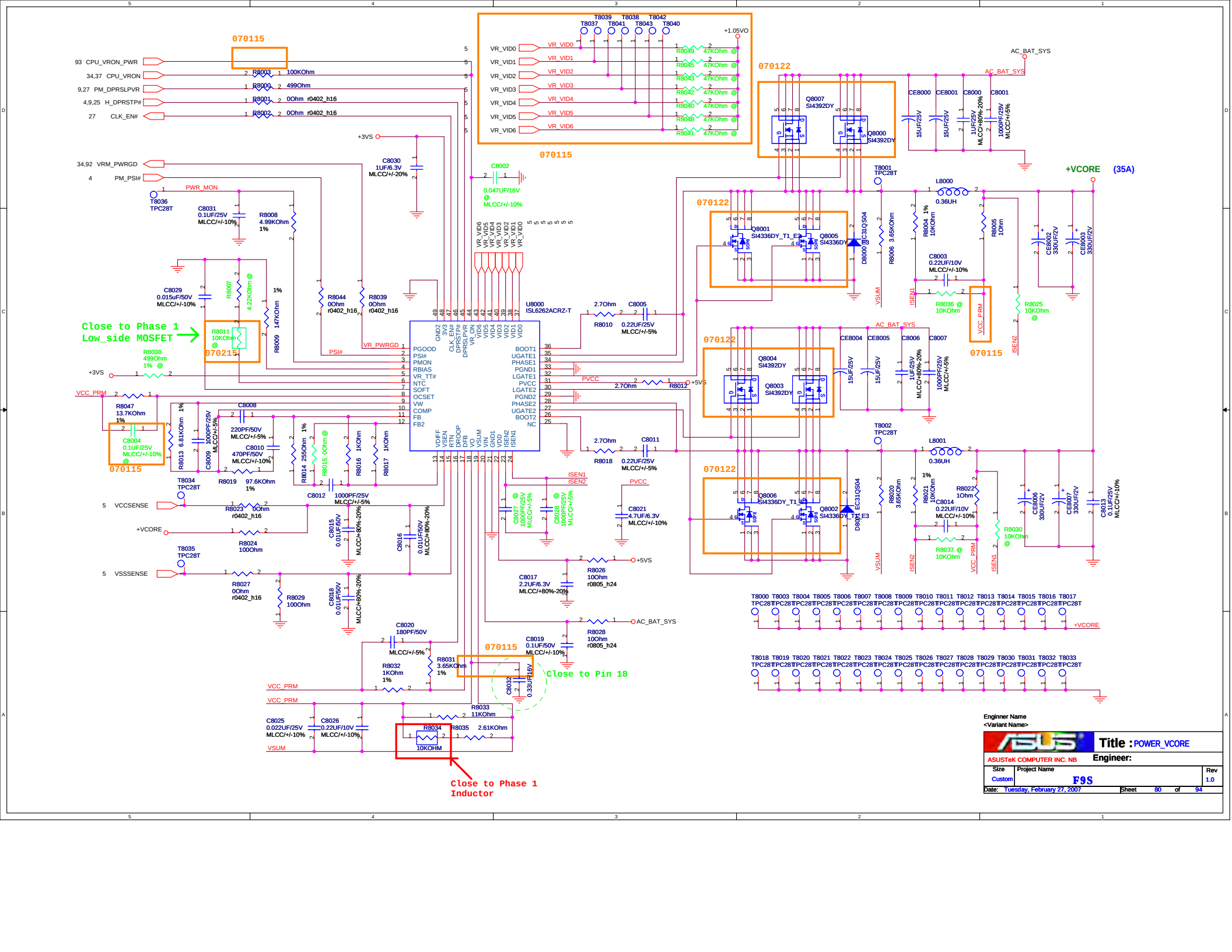
1. Delete R8046.
2. Change C8004(DNI) to U8000 pin8.
3. Change C8032 to U8000 pin18.
4. Add test point T8037~T8042.
5. For power sequency, change R8400 from 0 to 20K ohm.
6. For OCP adjust, change R8407 from 200K to 30K ohm.
7. For output voltage adjust, change R8406 from 20K to 4.22K, change R8409 from 100K to 20K ohm.
8. To Increase the saturation crrent of L8400, change L8400 from 09G02X103022 to 09G02X103U00.
9. DNI Q8404 and R8408.
10. Delete Q8505 and Q8501.
11. Change L8500 from 0.56uH to 1uH.
12. For OCP adjust, change R8508 from 100K to 51K.
13. For PWM oscillation issue, change output capacitor to 150uF/2V(ESR=18m ohm) *2.
14. For power sequency, change R8504 from 0 to 120K, change C8504 from DNI to 0.1uF, change C8515 from 0.033uF to 0.1uF.
15. Add JP8805 for layout improve.
16. Add 3S/4S selector circuit(DNI).
17. Add U9001 colay to U9000.
18. For power sequency, change R9108 and R9107 to 47K, change R9109 and R9110 to 22K, Delete R9106 and R9112.
19. Change Schematic_Part at Q8000,Q8001,Q8002,Q8003,Q8004 Q8005,Q8006,Q8007,Q8300,Q8301,Q8401,Q8403.
20. Change L8101 from 3.3uH/CYNTEC to 3.8uH/SUMIDA.
21. Change R8120 from 21K to 20K for OCP adjust.
22. For spec. change.Chagne Q8004 from SI4392 to SI4800, Change Q8006 from SI4336to SI4800, Change R8524 from 30K to 174K, Change L8500 from 1uH/18A to 1.8uH/9A. DNI CE8506, CE8504.

F9S ER_0215(R1.1 --> R1.3)-----------------POWER

23. Power team modify +1.5VS power rating to 3.5A ---page82

<Variant Name>

ASUSTeK COMPUTER INC	Title : History(2)	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Thursday, February 15, 2007	Sheet 49 of 94	


070115
93 CPU_VRON_PWR
34,37 CPU_VRON
9,27 PM_DPRSLPVR
4,9,25 H_DPRSTP#
27 CLK_EN#
R8003 100KOhm
R8000 499Ohm
R8001 0Ohm r0402_h16
R8002 0Ohm r0402_h16
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
T8037 T8039 T8038 T8042 T8043 T8040
+1.05VO
R8049 47KOhm
R8045 47KOhm
R8043 47KOhm
R8042 47KOhm
R8040 47KOhm
R8048 47KOhm
R8041 47KOhm
070115
AC_BAT_SYS
070122
Q8007 SI4392DY
Q8000 SI4392DY
CE8000 15UF/25V
CE8001 15UF/25V
C8000 1UF/25V MLCC/+80%-20%
C8001 1000PF/25V MLCC/+/-5%
+VCORE (35A)
34,92 VRM_PWRGD
4 PM_PSI#
PWR_MON
T8036 TPC28T
C8030 1UF/6.3V MLCC/+/-20%
C8002 0.047UF/16V @ MLCC/+/-10%
C8031 0.1UF/25V MLCC/+/-10%
R8008 4.99KOhm 1%
T8001 TPC28T
L8000 0.36UH
Q8001 SI4336DY_T1_E3
Q8005 SI4336DY
D8000 EC31QS04
R8006 3.65KOhm
R8004 10KOhm
R8005 1Ohm
C8003 0.22UF/10V MLCC/+/-10%
CE8002 330UF/2V
CE8003 330UF/2V
R8036 @ 10KOhm
R8025 10KOhm @
VCC_PRM
VSUM
ISEN1
ISEN2
Close to Phase 1 Low_side MOSFET
R8011 10KOhm @
070215
R8007 4.22KOhm @ 1%
R8009 147KOhm
R8044 0Ohm r0402_h16
R8039 0Ohm r0402_h16
C8029 0.015uF/50V MLCC/+/-10%
R8038 499Ohm 1% @
+3VS
VR_PWRGD
PSI#
U8000 ISL6262ACRZ-T
PGOOD
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
GND1
VSD2
ISEN1
2.7Ohm R8010
C8005 0.22UF/25V MLCC/+/-5%
PVCC
2.7Ohm R8012
+5VS
AC_BAT_SYS
070122
Q8004 SI4392DY
Q8003 SI4392DY
CE8004 15UF/25V
CE8005 15UF/25V
C8006 1UF/25V MLCC/+80%-20%
C8007 1000PF/25V MLCC/+/-5%
070115
VCC_PRM
R8047 13.7KOhm 1%
C8004 0.1UF/25V MLCC/+/-10% @
070115
R8013 6.81KOhm 1%
C8009 1000PF/25V MLCC/+/-5%
C8008 220PF/50V MLCC/+/-5%
C8010 470PF/50V MLCC/+/-10%
R8019 97.6KOhm 1%
R8014 255Ohm 1%
R8015 0Ohm @
R8016 1KOhm
R8017 1KOhm
T8002 TPC28T
L8001 0.36UH
Q8006 SI4336DY_T1_E3
Q8002 SI4336DY_T1_E3
D8001 EC31QS04
R8020 3.65KOhm
R8021 10KOhm 1%
C8014 0.22UF/10V MLCC/+/-10%
R8022 1Ohm
R8037 @ 10KOhm
R8030 10KOhm @
CE8006 330UF/2V
CE8007 330UF/2V
C8013 0.1UF/25V MLCC/+/-10%
T8034 TPC28T
5 VCCSENSE
R8023 0Ohm r0402_h16
C8012 1000PF/25V MLCC/+/-5%
C8027 @ 1000PF/25V MLCC/+/-5%
C8028 @ 1000PF/25V MLCC/+/-5%
C8021 4.7UF/6.3V MLCC/+/-10%
+VCORE
R8024 100Ohm
C8015 0.01UF/50V MLCC/+80%-20%
C8016 0.01UF/50V MLCC/+80%-20%
T8035 TPC28T
5 VSSSENSE
R8027 0Ohm r0402_h16
R8029 100Ohm
C8018 0.01UF/50V MLCC/+80%-20%
C8017 2.2UF/6.3V MLCC/+80%-20%
R8026 10Ohm r0805_h24
R8028 10Ohm r0805_h24
C8020 180PF/50V MLCC/+/-5%
R8031 3.65KOhm 1%
R8032 1KOhm 1%
C8019 0.1UF/50V MLCC/+/-10%
070115
Close to Pin 18
C8032 0.33UF/16V
VCC_PRM
VCC_PRM
R8033 11KOhm
C8025 0.022UF/25V MLCC/+/-10%
C8026 0.22UF/10V MLCC/+/-10%
R8034 10KOHM
R8035 2.61KOhm
VSUM
Close to Phase 1 Inductor
T8000 T8003 T8004 T8005 T8006 T8007 T8008 T8009 T8010 T8011 T8012 T8013 T8014 T8015 T8016 T8017
TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T
+VCORE
T8018 T8019 T8020 T8021 T8022 T8023 T8024 T8025 T8026 T8027 T8028 T8029 T8030 T8031 T8032 T8033
TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T TPC28T
Enginner Name
<Variant Name>
Title : POWER_VCORE
ASUSTeK COMPUTER INC. NB
Engineer:
Size Custom
Project Name F9S
Rev 1.0
Date: Tuesday, February 27, 2007
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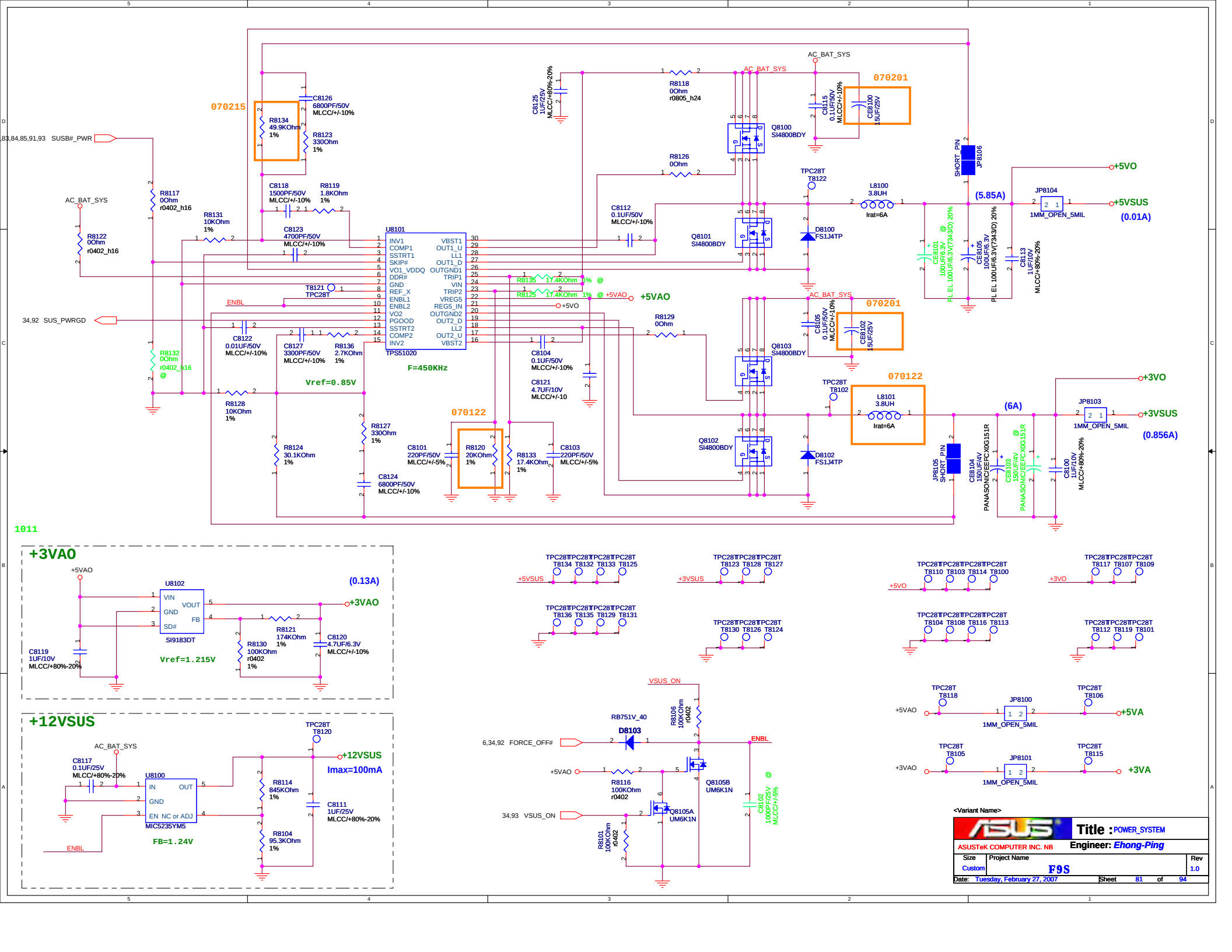
070215
C8126 6800PF/50V MLCC/+/-10%
R8134 49.9KOhm 1%
R8123 330Ohm 1%
C8118 1500PF/50V MLCC/+/-10%
R8119 1.8KOhm 1%
C8123 4700PF/50V MLCC/+/-10%
R8131 10KOhm 1%
R8117 0Ohm r0402_h16
R8122 0Ohm r0402_h16
AC_BAT_SYS
83,84,85,91,93 SUSB#_PWR
34,92 SUS_PWRGD
ENBL
T8121 TPC28T
R8132 0Ohm r0402_h16 @
C8122 0.01UF/50V MLCC/+/-10%
C8127 3300PF/50V MLCC/+/-10%
R8136 2.7KOhm 1%
Vref=0.85V
R8128 10KOhm 1%
R8124 30.1KOhm 1%
R8127 330Ohm 1%
C8124 6800PF/50V MLCC/+/-10%
U8101
INV1 COMP1 SSTRT1 SKIP# VO1_VDDQ DDR# GND REF_X ENBL1 ENBL2 VO2 PGOOD SSTRT2 COMP2 INV2
VBST1 OUT1_U LL1 OUT1_D OUTGND1 TRIP1 VIN TRIP2 VREG5 REG5_IN OUTGND2 OUT2_D LL2 OUT2_U VBST2
TPS51020
F=450KHz
C8125 1UF/25V MLCC/+80%-20%
R8118 0Ohm r0805_h24
AC_BAT_SYS
070201
CE8100 15UF/25V
C8115 0.1UF/50V MLCC/+/-10%
Q8100 SI4800BDY
R8126 0Ohm
C8112 0.1UF/50V MLCC/+/-10%
Q8101 SI4800BDY
TPC28T T8122
D8100 FS1J4TP
L8100 3.8UH Irat=6A
SHORT_PIN JP8105
(5.85A)
JP8104 1MM_OPEN_5MIL
+5VO
+5VSUS
(0.01A)
CE8101 100UF/6.3V @ PL EL 100UF/6.3V(7343/D) 20%
CE8105 100UF/6.3V PL EL 100UF/6.3V(7343/D) 20%
C8113 1UF/10V MLCC/+80%-20%
R8135 17.4KOhm 1% @
R8125 17.4KOhm 1% @ +5VAO
+5VAO
+5VO
R8129 0Ohm
C8104 0.1UF/50V MLCC/+/-10%
C8121 4.7UF/10V MLCC/+/-10
070122
R8120 20KOhm 1%
R8133 17.4KOhm 1%
C8101 220PF/50V MLCC/+/-5%
C8103 220PF/50V MLCC/+/-5%
Q8102 SI4800BDY
D8102 FS1J4TP
L8101 3.8UH Irat=6A
(6A)
JP8103 1MM_OPEN_5MIL
+3VO
+3VSUS
(0.856A)
JP8105 SHORT_PIN
CE8104 150UF/4V PANASONIC/EEFCX0G151R
CE8103 150UF/4V @ PANASONIC/EEFCX0G151R
C8100 1UF/10V MLCC/+80%-20%
1011
+3VA0
+5VAO
U8102
VIN GND SD# VOUT FB
SI9183DT
(0.13A)
+3VA0
C8119 1UF/10V MLCC/+80%-20%
Vref=1.215V
R8130 100KOhm r0402 1%
R8121 174KOhm 1%
C8120 4.7UF/6.3V MLCC/+/-10%
+12VSUS
TPC28T T8120
AC_BAT_SYS
C8117 0.1UF/25V MLCC/+80%-20%
U8100
IN GND EN NC or ADJ OUT
MIC5235YM5
FB=1.24V
ENBL
R8114 845KOhm 1%
R8104 95.3KOhm 1%
C8111 1UF/25V MLCC/+80%-20%
Imax=100mA
TPC28T T8134 T8132 T8133 T8125
+5VSUS
TPC28T T8136 T8135 T8129 T8131
TPC28T T8123 T8128 T8127
+3VSUS
TPC28T T8130 T8126 T8124
TPC28T T8110 T8103 T8114 T8100
+5VO
TPC28T T8104 T8108 T8116 T8113
TPC28T T8117 T8107 T8109
+3VO
TPC28T T8112 T8119 T8101
VSUS_ON
RB751V_40
D8103
R8106 100KOhm r0402
6,34,92 FORCE_OFF#
ENBL
+5VAO
R8116 100KOhm r0402
Q8105B UM6K1N
Q8105A UM6K1N
34,93 VSUS_ON
R8101 100KOhm r0402
C8102 1000PF/25V MLCC/+/-5% @
TPC28T T8118
JP8100 1MM_OPEN_5MIL
TPC28T T8106
+5VA
TPC28T T8105
JP8101 1MM_OPEN_5MIL
TPC28T T8115
+3VA
<Variant Name>
Title : POWER_SYSTEM
ASUSTeK COMPUTER INC. NB
Engineer: Ehong-Ping
Size Custom
Project Name F9S
Rev 1.0
Date: Tuesday, February 27, 2007
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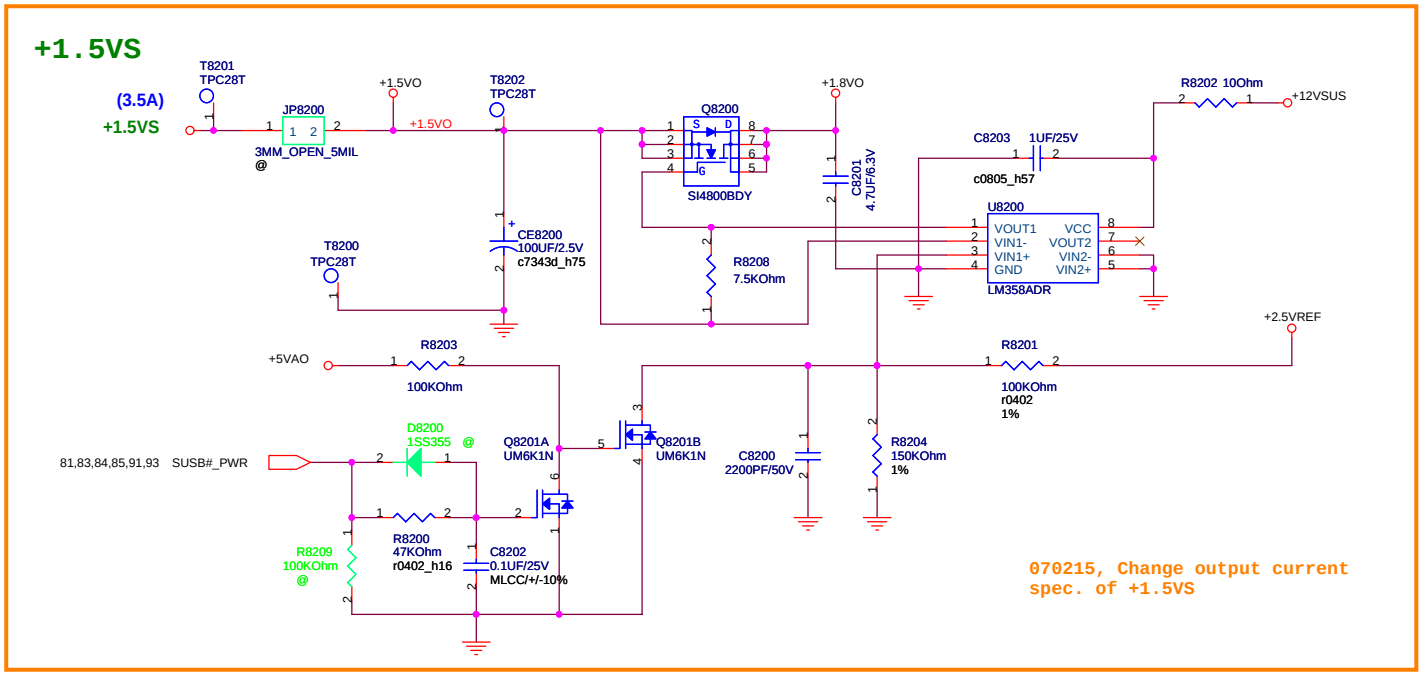

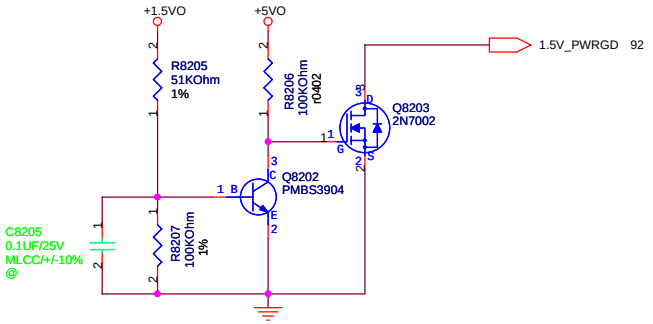

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_1.5VS & 1.05VS

Engineer: Ehong-Ping

Size	Project Name	Rev
B	F9S	1.0

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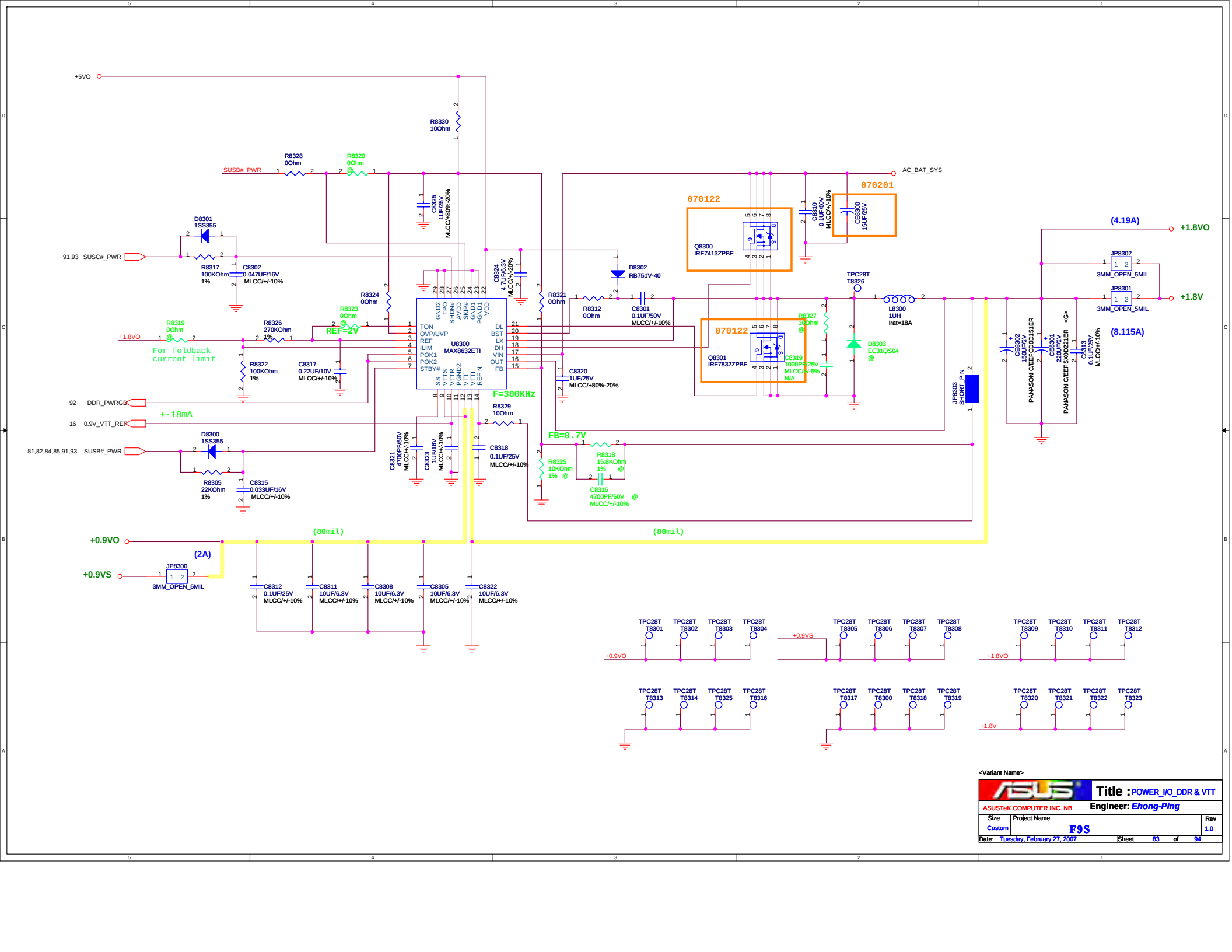
+5VO
R8330 10Ohm
R8328 0Ohm
R8320 0Ohm
SUSB#_PWR
C8325 1UF/25V MLCC/+80%-20%
AC_BAT_SYS
070201
070122
Q8300 IRF7413ZPBF
C8310 0.1UF/50V MLCC/+/-10%
CE8300 15UF/25V
(4.19A)
+1.8VO
JP8302 3MM_OPEN_5MIL
JP8301 3MM_OPEN_5MIL
+1.8V
(8.115A)
D8301 1SS355
91,93 SUSC#_PWR
R8317 100KOhm 1%
C8302 0.047UF/16V MLCC/+/-10%
C8324 4.7UF/6.3V MLCC/+/-20%
R8324 0Ohm
R8323 0Ohm
REF=2V
R8321 0Ohm
D8302 RB751V-40
R8312 0Ohm
C8301 0.1UF/50V MLCC/+/-10%
TPC28T T8326
L8300 1UH Irat=18A
R8327 10Ohm @
D8303 EC31QS04 @
Q8301 IRF7832ZPBF
C8319 1000PF/25V MLCC/+/-5% N/A
070122
R8319 0Ohm @
+1.8VO
For foldback current limit
R8326 270KOhm 1%
R8322 100KOhm 1%
C8317 0.22UF/10V MLCC/+/-10%
U8300 MAX8632ETI
TON
OVP/UVP
REF
ILIM
POK1
POK2
STBY#
SS
VTTS
VTTR
PGND2
VTTI
REFIN
DL
BST
LX
DH
VIN
OUT
FB
GND2
TPO
SHDN#
AVDD
SKIP#
GND1
PGND1
VDD
C8320 1UF/25V MLCC/+80%-20%
JP8303 SHORT PIN
CE8302 150UF/2V PANASONIC/EEFCD0D151ER
CE8301 220UF/2V PANASONIC/EEFSX0D221ER <G>
C8313 0.1UF/25V MLCC/+/-10%
92 DDR_PWRGD
+-18mA
16 0.9V_VTT_REF
F=300KHz
R8329 10Ohm
FB=0.7V
D8300 1SS355
81,82,84,85,91,93 SUSB#_PWR
C8321 4700PF/50V MLCC/+/-10%
C8323 1UF/16V MLCC/+/-10%
C8318 0.1UF/25V MLCC/+/-10%
R8325 10KOhm 1% @
R8318 15.8KOhm 1% @
C8316 4700PF/50V @ MLCC/+/-10%
R8305 22KOhm 1%
C8315 0.033UF/16V MLCC/+/-10%
(80mil)
(80mil)
+0.9VO
(2A)
+0.9VS
JP8300 3MM_OPEN_5MIL
C8312 0.1UF/25V MLCC/+/-10%
C8311 10UF/6.3V MLCC/+/-10%
C8308 10UF/6.3V MLCC/+/-10%
C8305 10UF/6.3V MLCC/+/-10%
C8322 10UF/6.3V MLCC/+/-10%
TPC28T T8301
TPC28T T8302
TPC28T T8303
TPC28T T8304
TPC28T T8305
TPC28T T8306
TPC28T T8307
TPC28T T8308
TPC28T T8309
TPC28T T8310
TPC28T T8311
TPC28T T8312
TPC28T T8313
TPC28T T8314
TPC28T T8325
TPC28T T8316
TPC28T T8317
TPC28T T8300
TPC28T T8318
TPC28T T8319
TPC28T T8320
TPC28T T8321
TPC28T T8322
TPC28T T8323
<Variant Name>
Title : POWER_I/O_DDR & VTT
ASUSTeK COMPUTER INC. NB
Engineer: Ehong-Ping
Size Custom
Project Name F9S
Rev 1.0
Date: Tuesday, February 27, 2007
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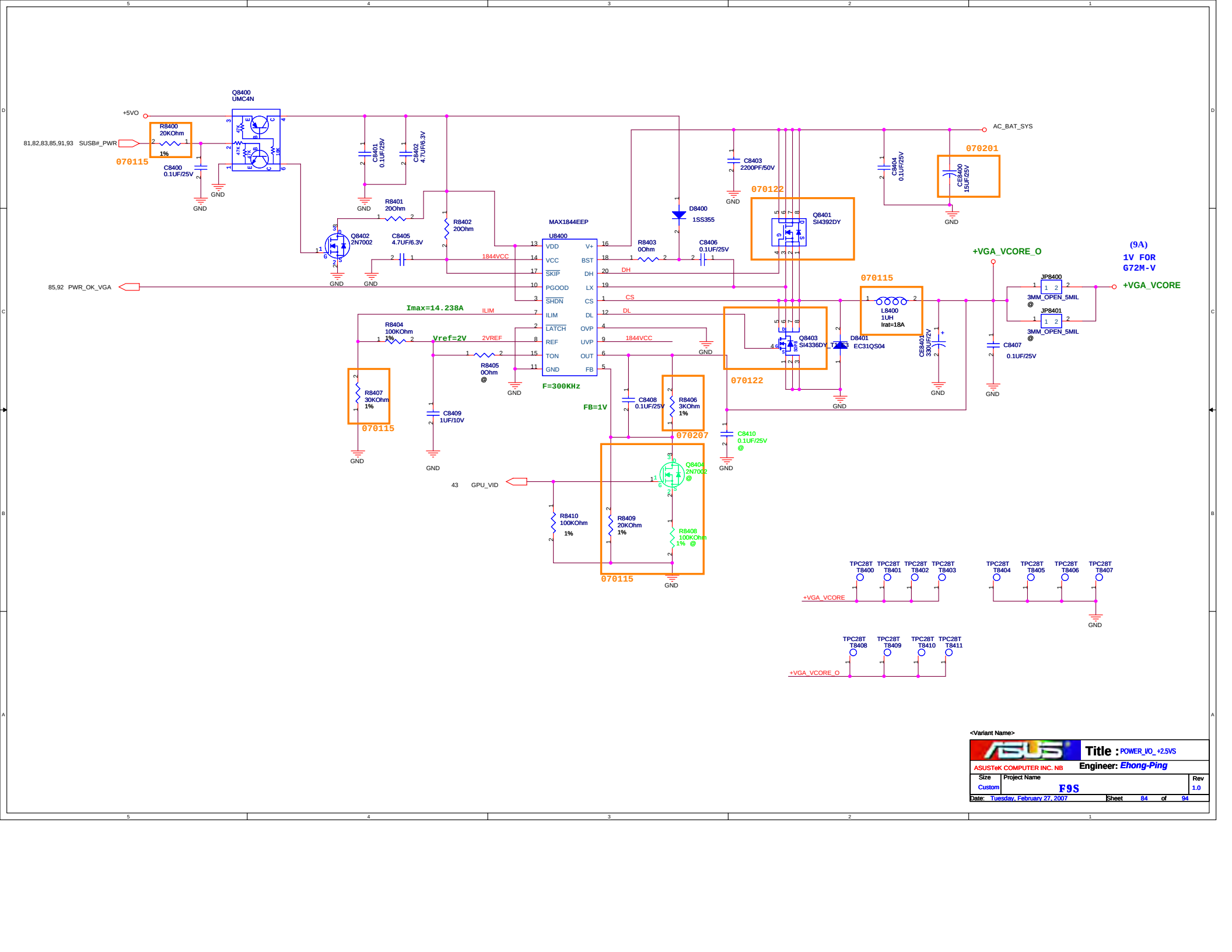
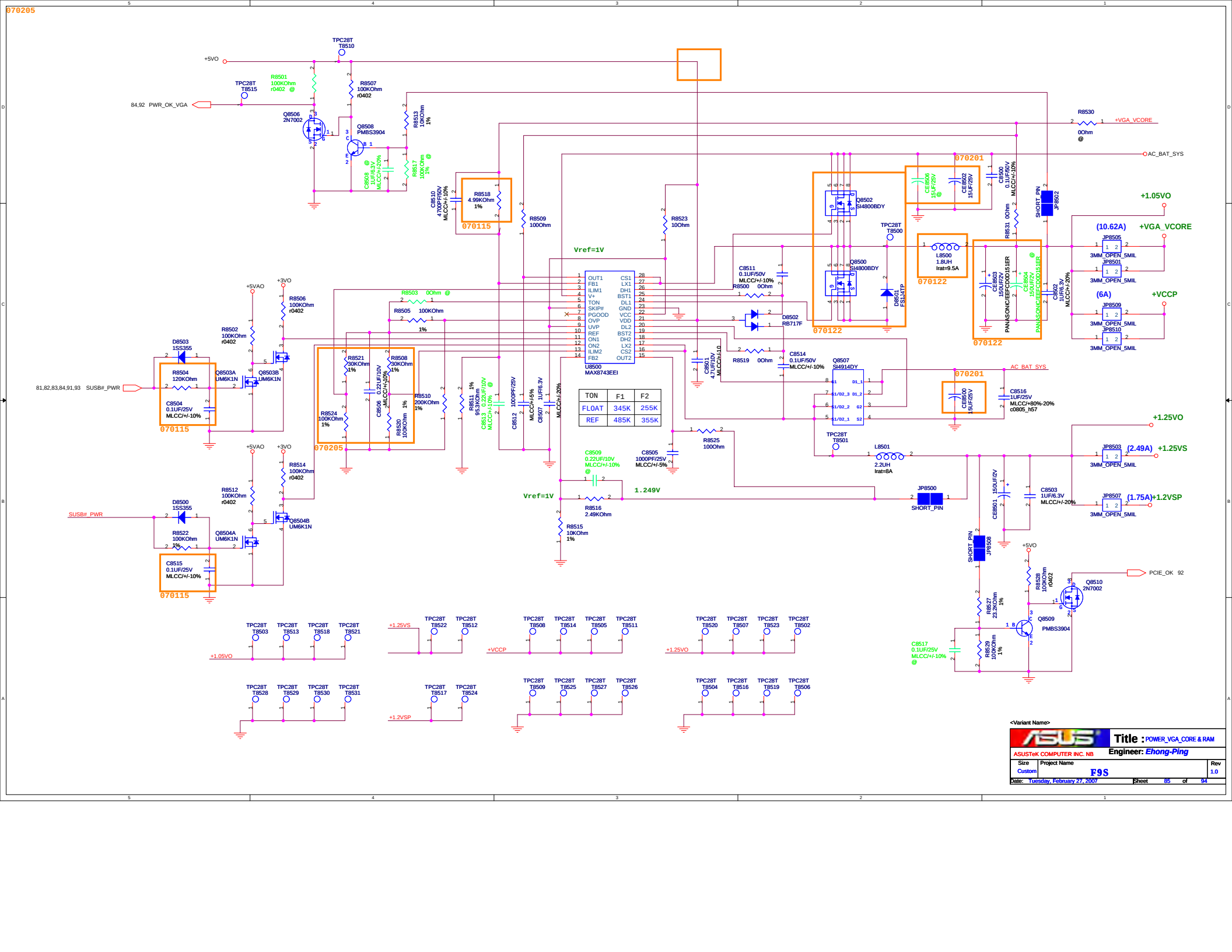


<Variant Name>

Title :	POWER_I/O_ +2.5VS
ASUSTeK COMPUTER INC. NB	Engineer: Ehong-Ping
Size: Custom	Project Name: F9S
Rev: 1.0	
Date: Tuesday, February 27, 2007	Sheet 84 of 94


070205
U8500
MAX8743EEI
Vref=1V
1.249V
TON F1 F2
FLOAT 345K 255K
REF 485K 355K
+5VO
+3VO
+5VAO
+1.05VO
+1.25VS
+1.25VO
+VCCP
+1.2VSP
+VGA_VCORE
+1.25VO
+VCCP
AC_BAT_SYS
PWR_OK_VGA
SUSB#_PWR
PCIE_OK
Title : POWER_VGA_CORE & RAM
Engineer: Ehong-Ping
ASUSTeK COMPUTER INC. NB
Project Name F9S
Size Custom
Rev 1.0
Date: Tuesday, February 27, 2007
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<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
B	F9S	1.0

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<Variant Name>

Title : POWER_SHUTDOWN#

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

Date: Thursday, February 15, 2007 Sheet 87 of 94

POWER PATH & BAT_LEARN

90 WATT

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.010ohm
VCLS=2.5341V
=> Iin(max)=4.5A
=> Constant Power = 19 * 4.5 = 85.5W
=> R5710=20K,R5715=30K

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A

Vbatt = Cell * [Vref +[(VCTL- 1.8V) / 9.52]]
VCTL= 1.588V
=> Vbatt = 4.2V

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

Precgarge current=150mA

LDO : 5.4V
REF : 4.2235V

90W->10m Ohm
65W->20m Ohm

90W->30K Ohm
65W->137K Ohm

070115

AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put JP8805 close to Q8800

4S: Mount R8808 only
3S: Unmount all components
3S/4S: Unmount R8808, and mount others

Title :	POWER_CHARGER
ASUSTeK COMPUTER INC. NB	Engineer: Ehong-Ping
Size: Custom	Project Name: F9S
Rev: 1.0	
Date: Tuesday, February 27, 2007	Sheet 88 of 94

<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

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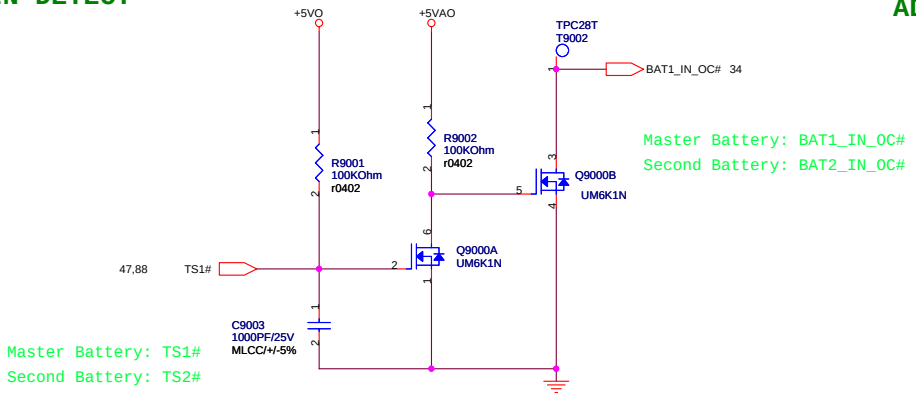
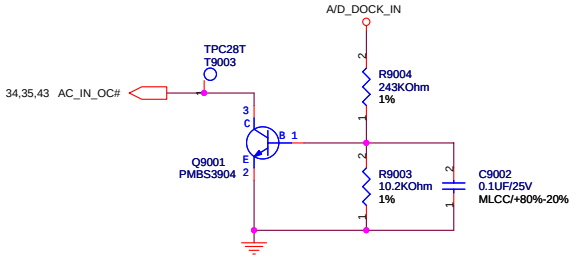
BATTERY IN DETECT



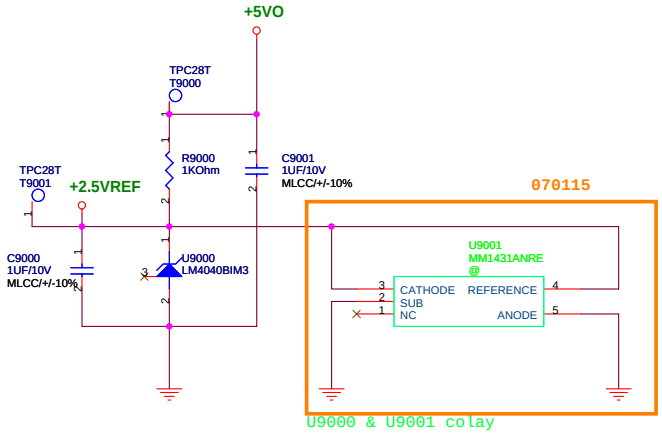
Master Battery: BAT1_IN_OC#
Second Battery: BAT2_IN_OC#

Master Battery: TS1#
Second Battery: TS2#

ADAPTER IN DETECT



+2.5VREF



U9000 & U9001 colay

<Variant Name>

Title : POWER_DETECT

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

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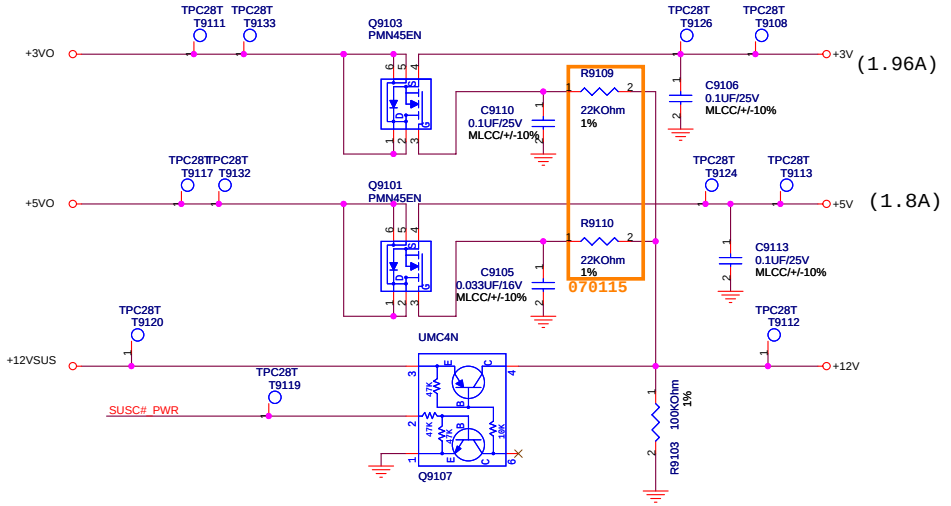
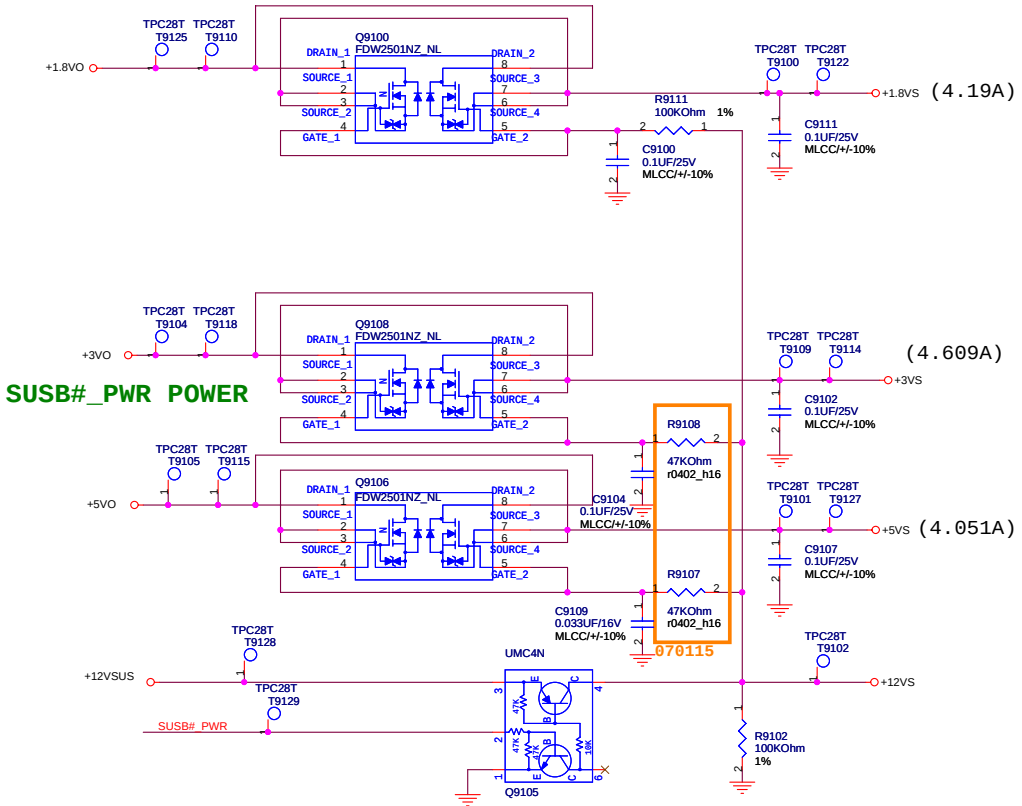
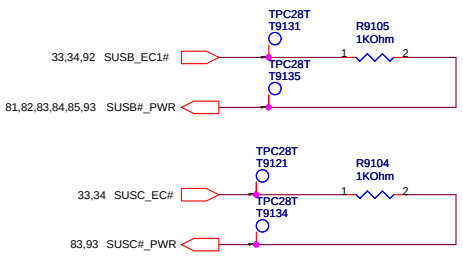
SUSC#_PWR POWER

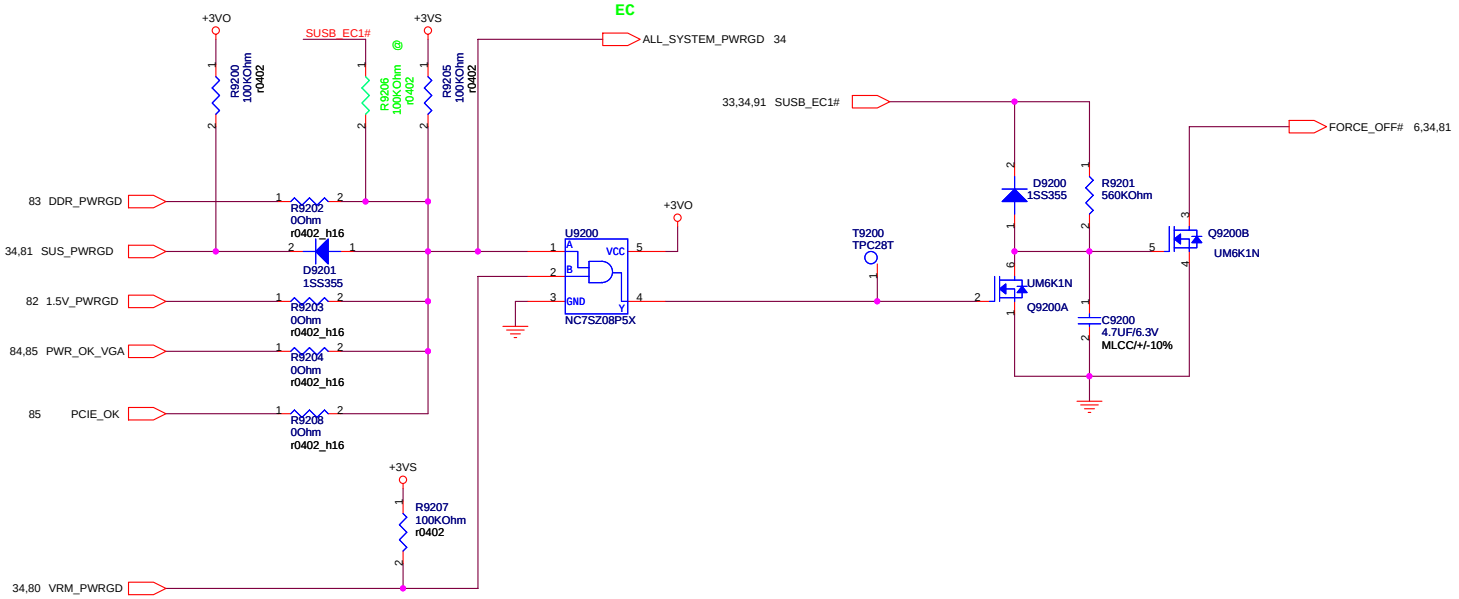






ASUSTeK COMPUTER INC. NB	Title : POWER_LOAD SWITCH	
	Engineer: Ehong-Ping	
Size: Custom	Project Name: F9S	Rev: 1.0
Date: Tuesday, February 27, 2007	Sheet 91 of 94	

POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_PROTECT	
	Engineer: Ehong-Ping	
Size: Custom	Project Name: F9S	Rev: 1.0
Date: Tuesday, February 27, 2007	Sheet 92 of 94	

AC_BAT_SYS — AC_BAT_SYS 46,80,81,83,84,85,88

BAT — BAT 46,88

BAT_CON — BAT_CON 46,47,88

+2.5VREF — +2.5VREF 82,90

+3VA — +3VA 17,25,27,34,37,46,81

+5VAO — +5VAO 81,82,85,90

+5VO — +5VO 81,82,83,84,85,90,91

+5VSUS — +5VSUS 24,28,81

+5V — +5V 17,24,36,37,91

+5VS — +5VS 6,18,19,21,22,23,28,33,34,37,38,39,44,46,80,91

+3VO — +3VO 81,85,91,92

+3VSUS — +3VSUS 17,20,22,24,26,27,28,29,34,39,46,81

+3V — +3V 19,20,21,22,26,33,35,37,91

+3VS — +3VS 6,7,9,12,13,14,15,17,18,19,20,21,22,23,25,27,28,29,33,34,37,39,40,43,44,45,80,91,92

+12VSUS — +12VSUS 24,81,82,91

+12V — +12V 22,24,37,91

+12VS — +12VS 17,18,19,22,37,91

+1.8VO — +1.8VO 82,83,91

+1.8V — +1.8V 9,11,14,15,16,37,83

+0.9VS — +0.9VS 16,37,83

+0.9VO — +0.9VO 83

+1.05VO — +1.05VO 80,85

+VCCP — +VCCP 4,5,6,7,8,9,11,12,28,37,85

+1.5VO — +1.5VO 82

+1.5VS — +1.5VS 5,12,20,25,28,33,37,82

+VCORE — +VCORE 5,6,37,80

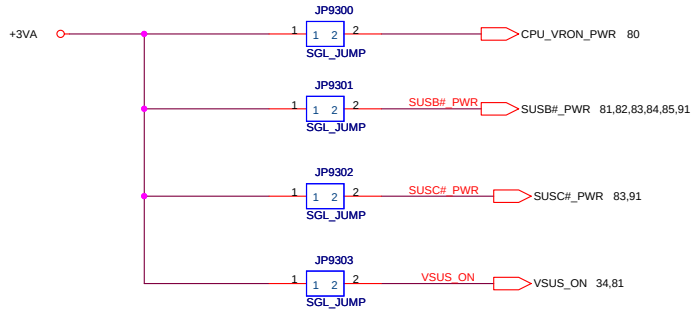
+VGA_VCORE — +VGA_VCORE 37,40,84,85

+1.8VS — +1.8VS 37,41,43,44,91

+1.2VSP — +1.2VSP 37,40,41,44,85

+1.25VS — +1.25VS 9,12,28,85

FOR POWER TEST



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_SIGNAL

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

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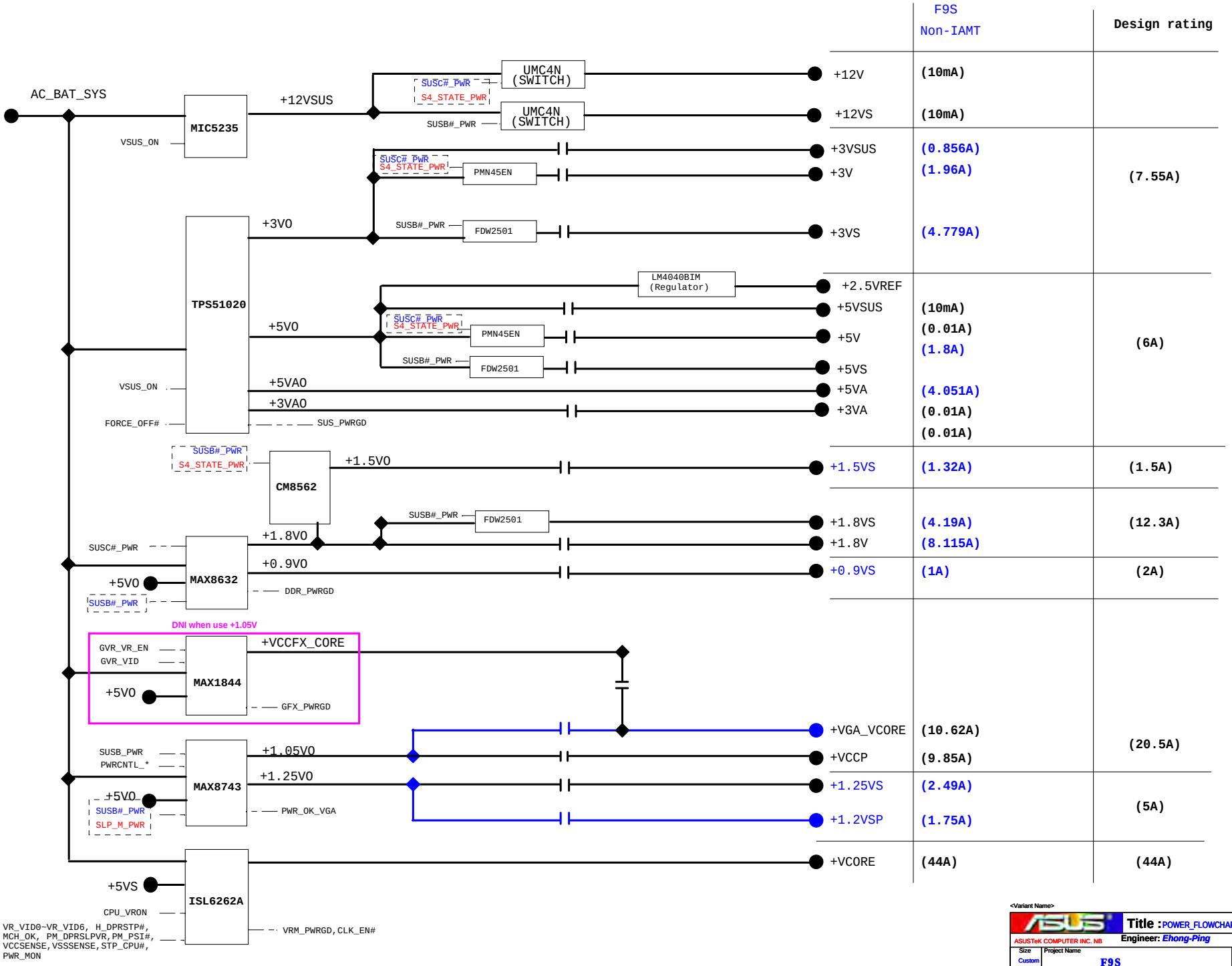

	F9S Non-IAMT	Design rating
+12V	(10mA)	
+12VS	(10mA)	
+3VSUS	(0.856A)	(7.55A)
+3V	(1.96A)	
+3VS	(4.779A)	
+2.5VREF		
+5VSUS	(10mA)	
+5V	(0.01A)	(6A)
+5VS	(1.8A)	
+5VA	(4.051A)	
+3VA	(0.01A)	
	(0.01A)	
+1.5VS	(1.32A)	(1.5A)
+1.8VS	(4.19A)	(12.3A)
+1.8V	(8.115A)	
+0.9VS	(1A)	(2A)
+VGA_VCORE	(10.62A)	(20.5A)
+VCCP	(9.85A)	
+1.25VS	(2.49A)	(5A)
+1.2VSP	(1.75A)	
+VCORE	(44A)	(44A)

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_FLOWCHART

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

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