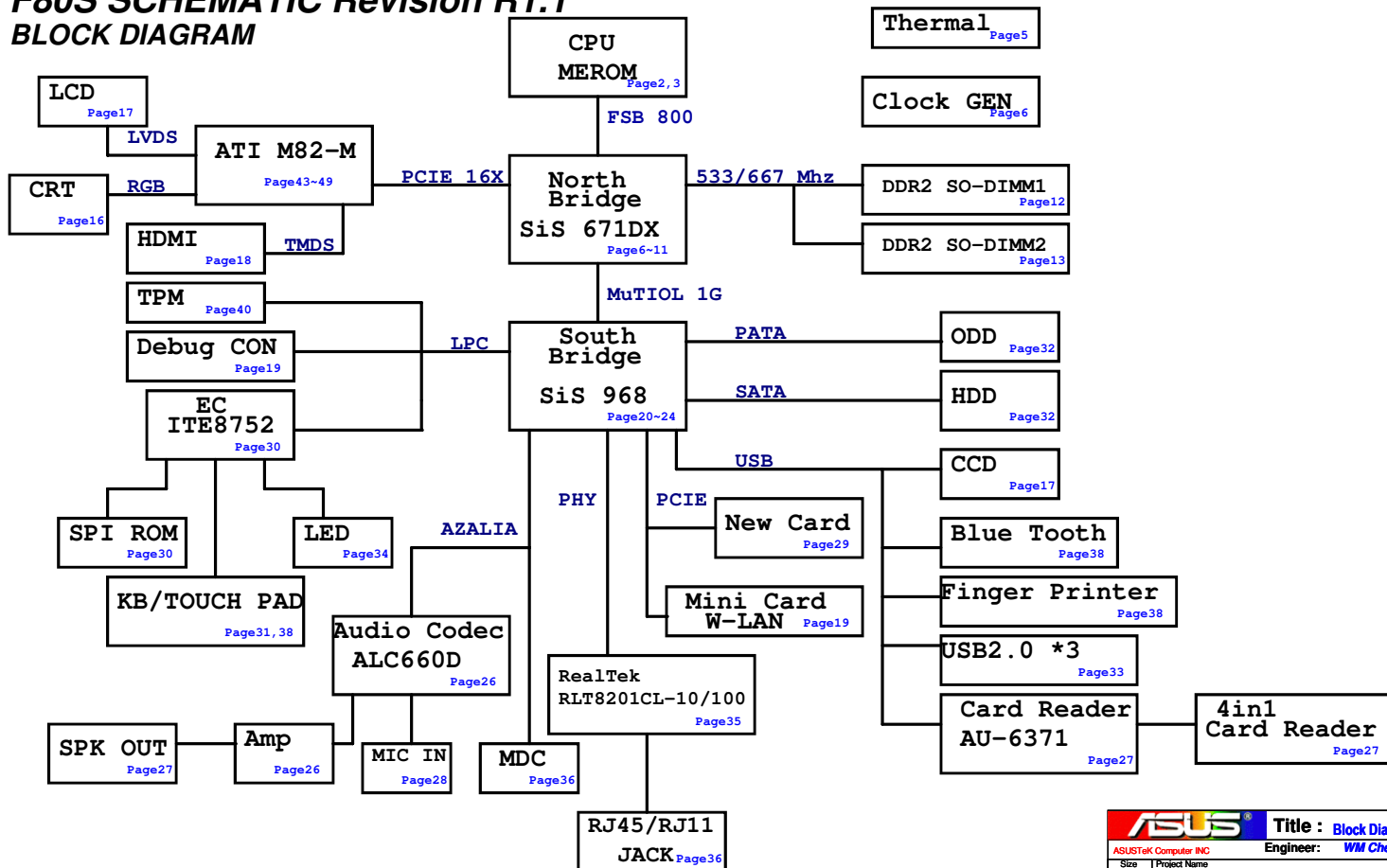
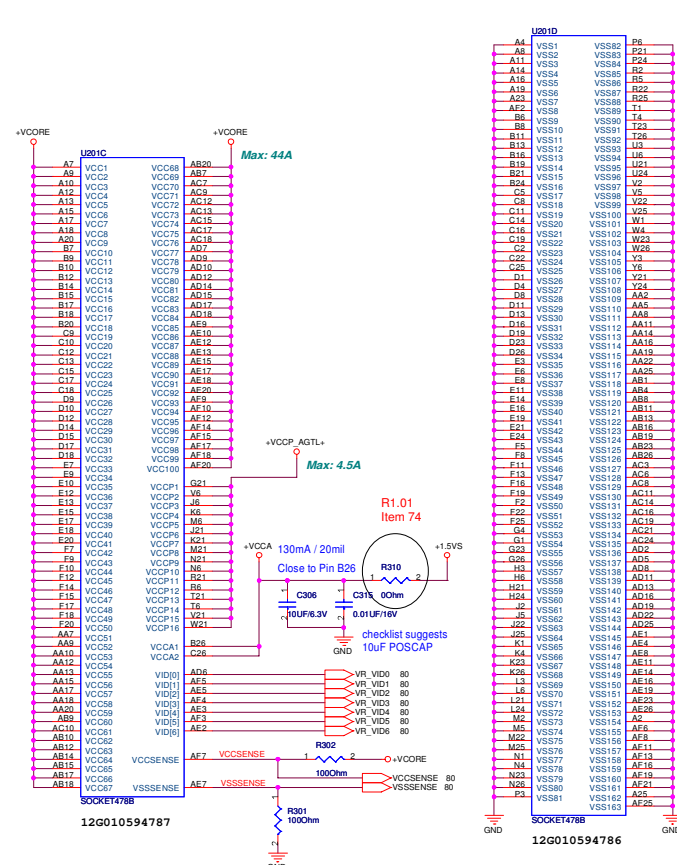


F80S SCHEMATIC Revision R1.1

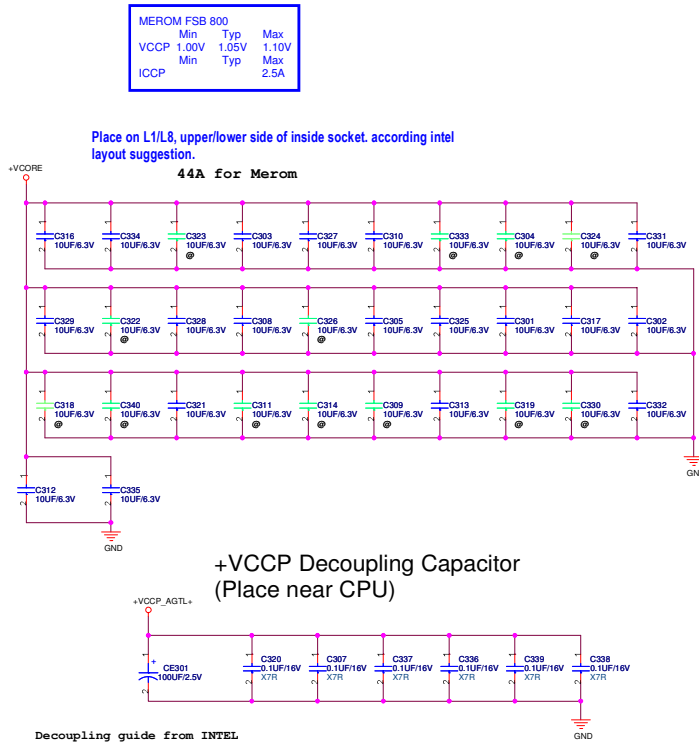
BLOCK DIAGRAM



ASUS		Title : Block Diagram	
ASUSTek Computer INC		Engineer: WM Chen	
Size	Project Name		Rev
B	F80S		1.1
Date: Friday, February 15, 2008		Sheet	1 of 34

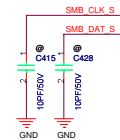


Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.



Decoupling guide from INTEL

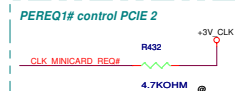
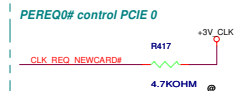
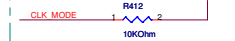
VCCORE	22uF/10V	* 32pcs
VCCP	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
VCCP	150uF	* 1pcs for CPU



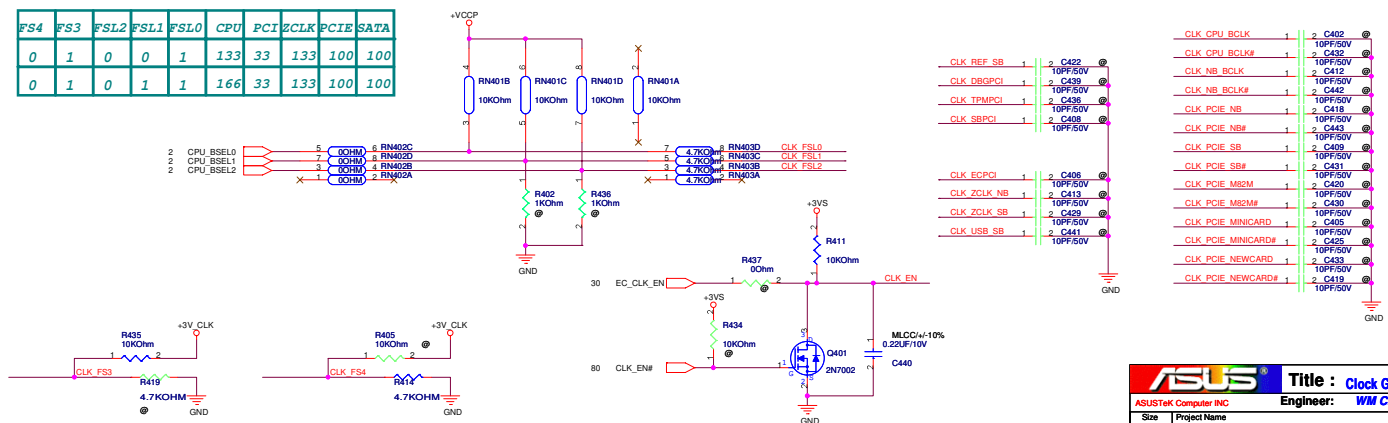
CLK_MODE

0 = Desktop Mode

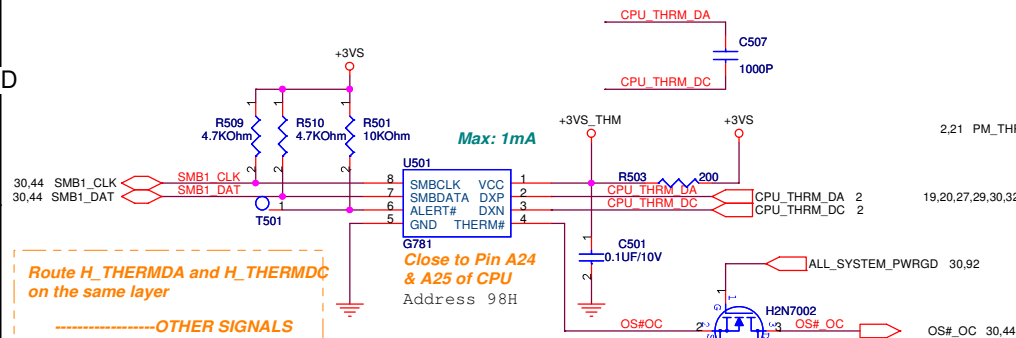
1 = Mobile Mode



FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100



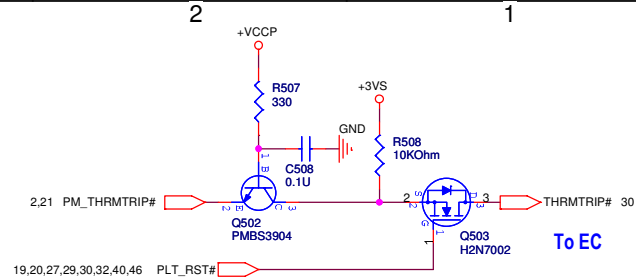
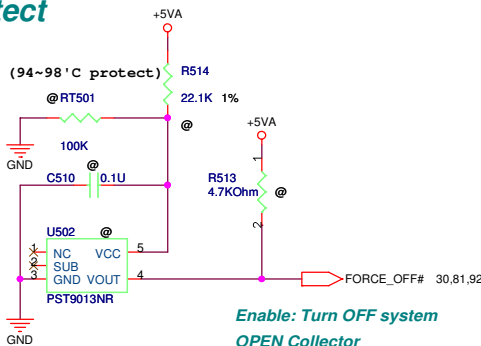
CPU Thermal Sensor



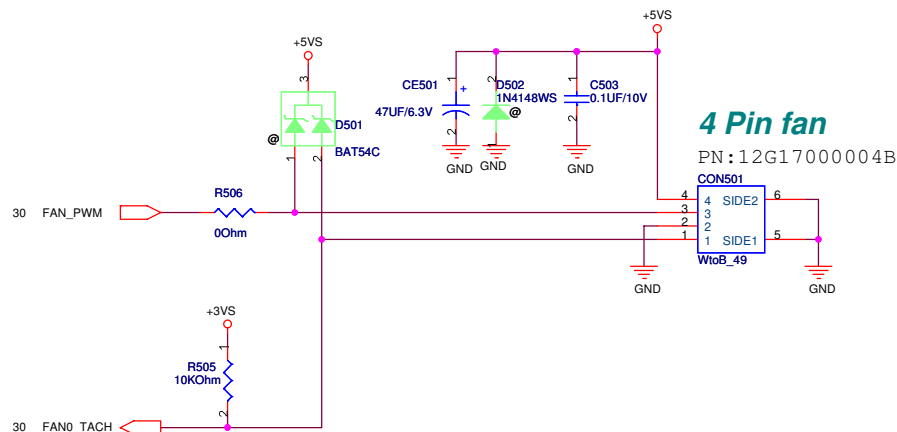
Route H_THERMDA and H_THERMDC
on the same layer

-----OTHER SIGNALS
20 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
20 mils
-----OTHER SIGNALS
Avoid FSB,Power

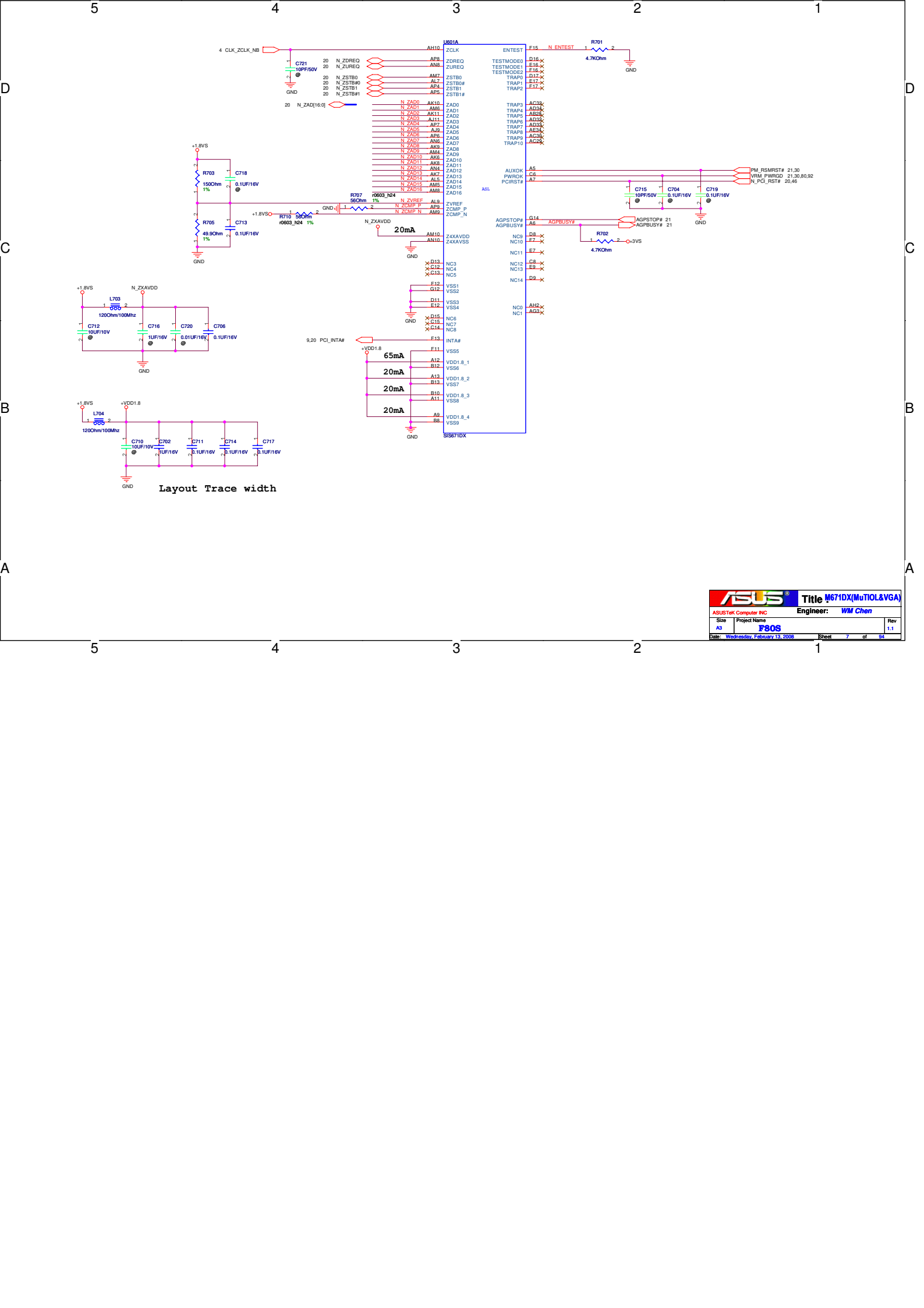
H/W Thermal Protect



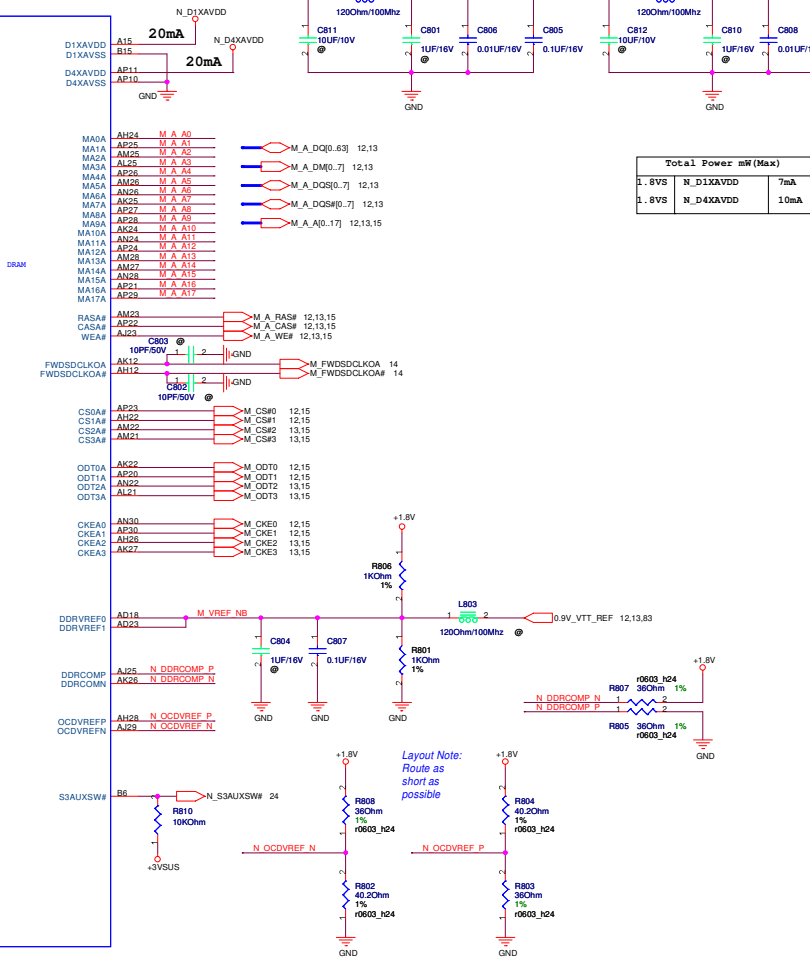
DC FAN Control

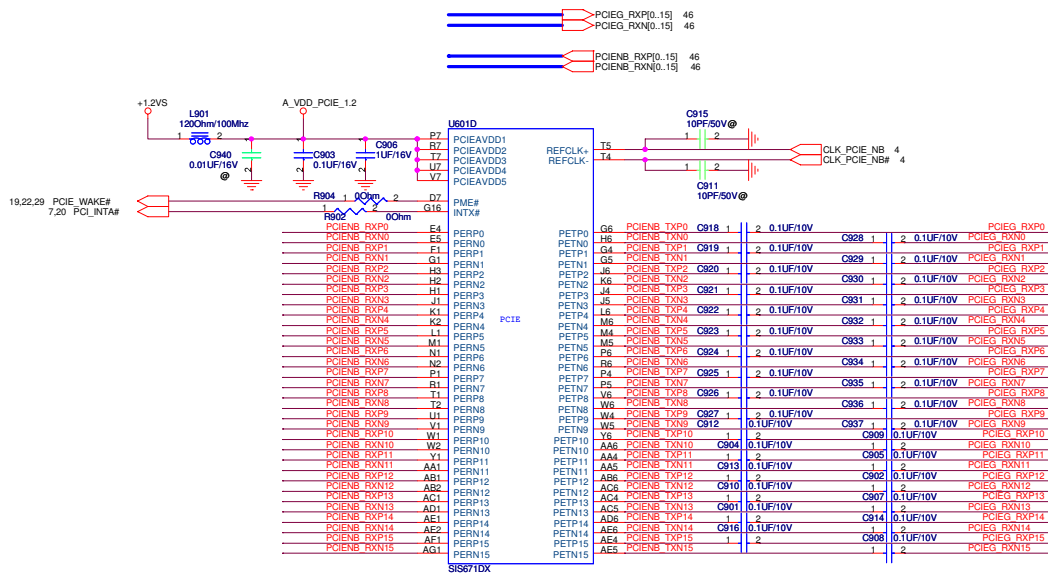


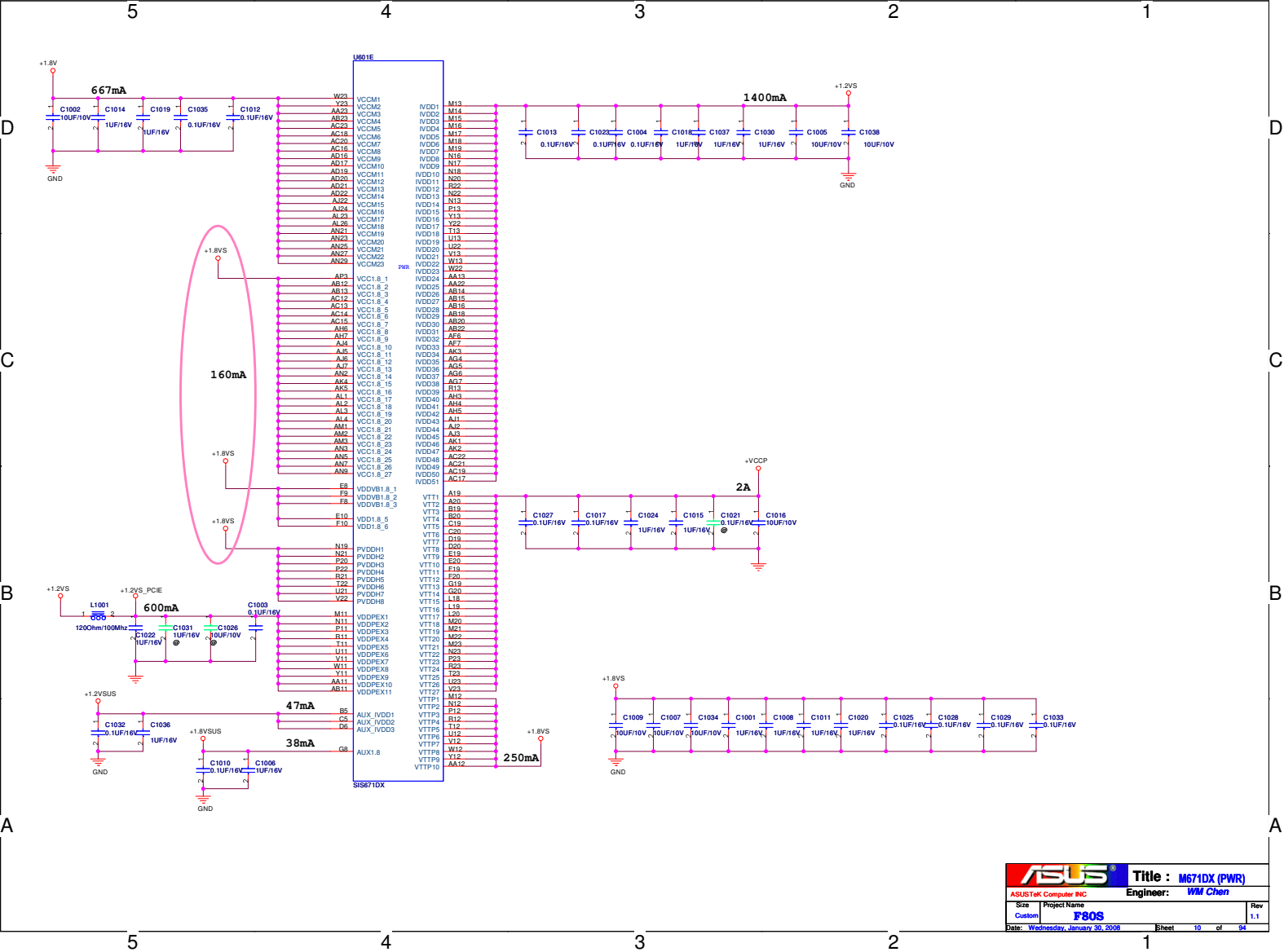
ASUS		Title : Thermal Sensor	
ASUSTeK Computer INC		Engineer: WM Chen	
Size A4	Project Name F80S		Rev 1.1
Date: Wednesday, February 13, 2008		Sheet 5 of 94	

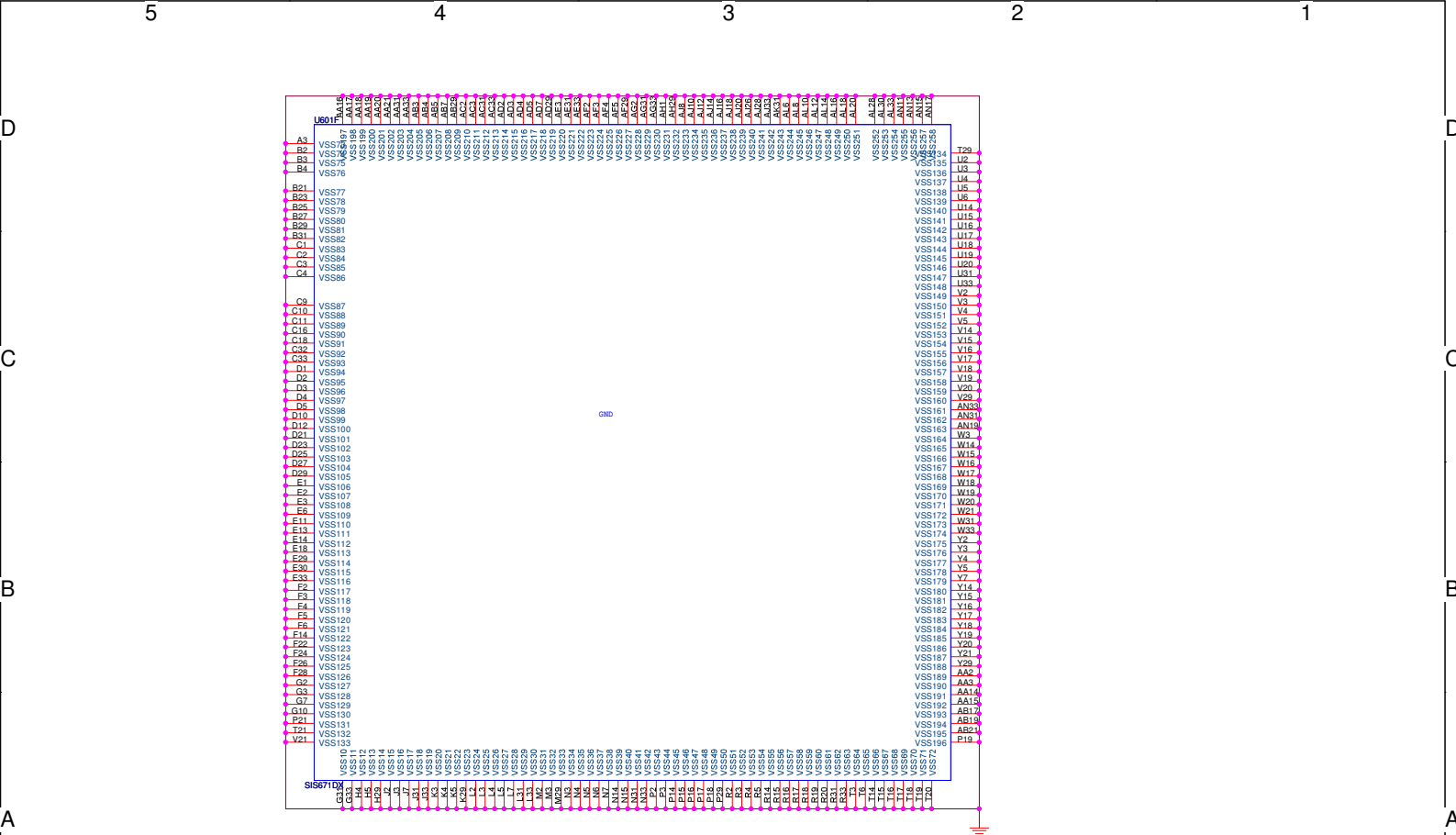


M_A_DQ00	AD34	MD0A
M_A_DQ01	AD30	MD1A
M_A_DQ02	AG34	MD2A
M_A_DQ03	AE32	MD3A
M_A_DQ04	AE32	MD4A
M_A_DQ05	AE34	MD5A
M_A_DQ06	AE31	MD6A
M_A_DQ07	AE31	MD7A
M_A_DQ08	AD28	MD8A
M_A_DQ09	AE32	MD9A
M_A_DQ10	AE31	MD10A
M_A_DQ11	AE30	MD11A
M_A_DQ12	AE30	MD12A
M_A_DQ13	AG34	MD13A
M_A_DQ14	AJ32	MD14A
M_A_DQ15	AJ31	MD15A
M_A_DQ16	AH34	MD16A
M_A_DQ17	AH32	MD17A
M_A_DQ18	AK32	MD18A
M_A_DQ19	AK30	MD19A
M_A_DQ20	AK32	MD20A
M_A_DQ21	AK34	MD21A
M_A_DQ22	AK34	MD22A
M_A_DQ23	AL31	MD23A
M_A_DQ24	AJ30	MD24A
M_A_DQ25	AK32	MD25A
M_A_DQ26	AK34	MD26A
M_A_DQ27	AK30	MD27A
M_A_DQ28	AK32	MD28A
M_A_DQ29	AK32	MD29A
M_A_DQ30	AK30	MD30A
M_A_DQ31	AK28	MD31A
M_A_DQ32	AK30	MD32A
M_A_DQ33	AK30	MD33A
M_A_DQ34	AK32	MD34A
M_A_DQ35	AK31	MD35A
M_A_DQ36	AK20	MD36A
M_A_DQ37	AK20	MD37A
M_A_DQ38	AK20	MD38A
M_A_DQ39	AK20	MD39A
M_A_DQ40	AK18	MD40A
M_A_DQ41	AJ17	MD41A
M_A_DQ42	AK17	MD42A
M_A_DQ43	AK18	MD43A
M_A_DQ44	AK18	MD44A
M_A_DQ45	AK18	MD45A
M_A_DQ46	AK18	MD46A
M_A_DQ47	AK17	MD47A
M_A_DQ48	AK18	MD48A
M_A_DQ49	AK18	MD49A
M_A_DQ50	AK18	MD50A
M_A_DQ51	AK18	MD51A
M_A_DQ52	AK18	MD52A
M_A_DQ53	AK18	MD53A
M_A_DQ54	AK18	MD54A
M_A_DQ55	AK18	MD55A
M_A_DQ56	AK18	MD56A
M_A_DQ57	AK18	MD57A
M_A_DQ58	AK18	MD58A
M_A_DQ59	AK18	MD59A
M_A_DQ60	AK18	MD60A
M_A_DQ61	AK18	MD61A
M_A_DQ62	AK18	MD62A
M_A_DQ63	AK18	MD63A
M_A_DQ64	AK18	MD64A
M_A_DQ65	AK18	MD65A
M_A_DQ66	AK18	MD66A
M_A_DQ67	AK18	MD67A
M_A_DQ68	AK18	MD68A
M_A_DQ69	AK18	MD69A
M_A_DQ70	AK18	MD70A
M_A_DQ71	AK18	MD71A
M_A_DQ72	AK18	MD72A
M_A_DQ73	AK18	MD73A
M_A_DQ74	AK18	MD74A
M_A_DQ75	AK18	MD75A
M_A_DQ76	AK18	MD76A
M_A_DQ77	AK18	MD77A
M_A_DQ78	AK18	MD78A
M_A_DQ79	AK18	MD79A
M_A_DQ80	AK18	MD80A
M_A_DQ81	AK18	MD81A
M_A_DQ82	AK18	MD82A
M_A_DQ83	AK18	MD83A
M_A_DQ84	AK18	MD84A
M_A_DQ85	AK18	MD85A
M_A_DQ86	AK18	MD86A
M_A_DQ87	AK18	MD87A
M_A_DQ88	AK18	MD88A
M_A_DQ89	AK18	MD89A
M_A_DQ90	AK18	MD90A
M_A_DQ91	AK18	MD91A
M_A_DQ92	AK18	MD92A
M_A_DQ93	AK18	MD93A
M_A_DQ94	AK18	MD94A
M_A_DQ95	AK18	MD95A
M_A_DQ96	AK18	MD96A
M_A_DQ97	AK18	MD97A
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M_A_DQ100	AK18	MD100A



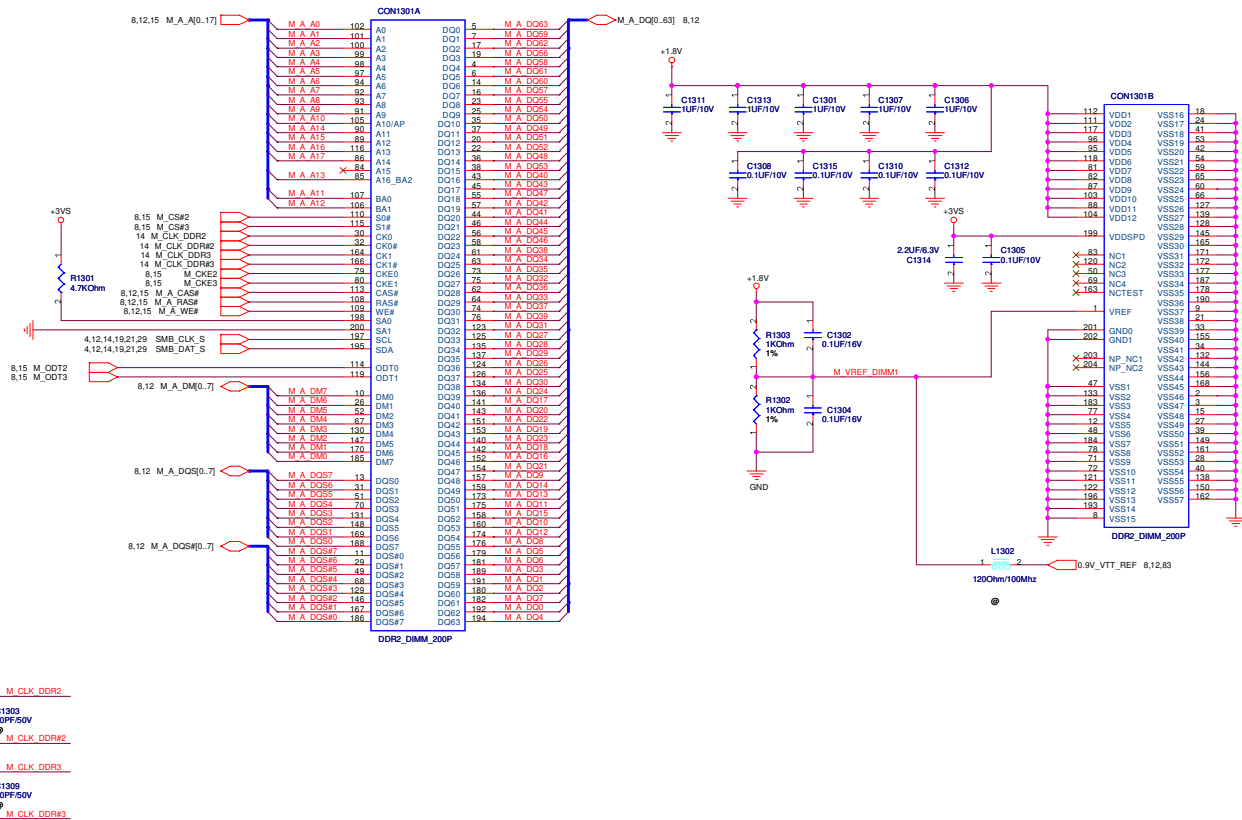


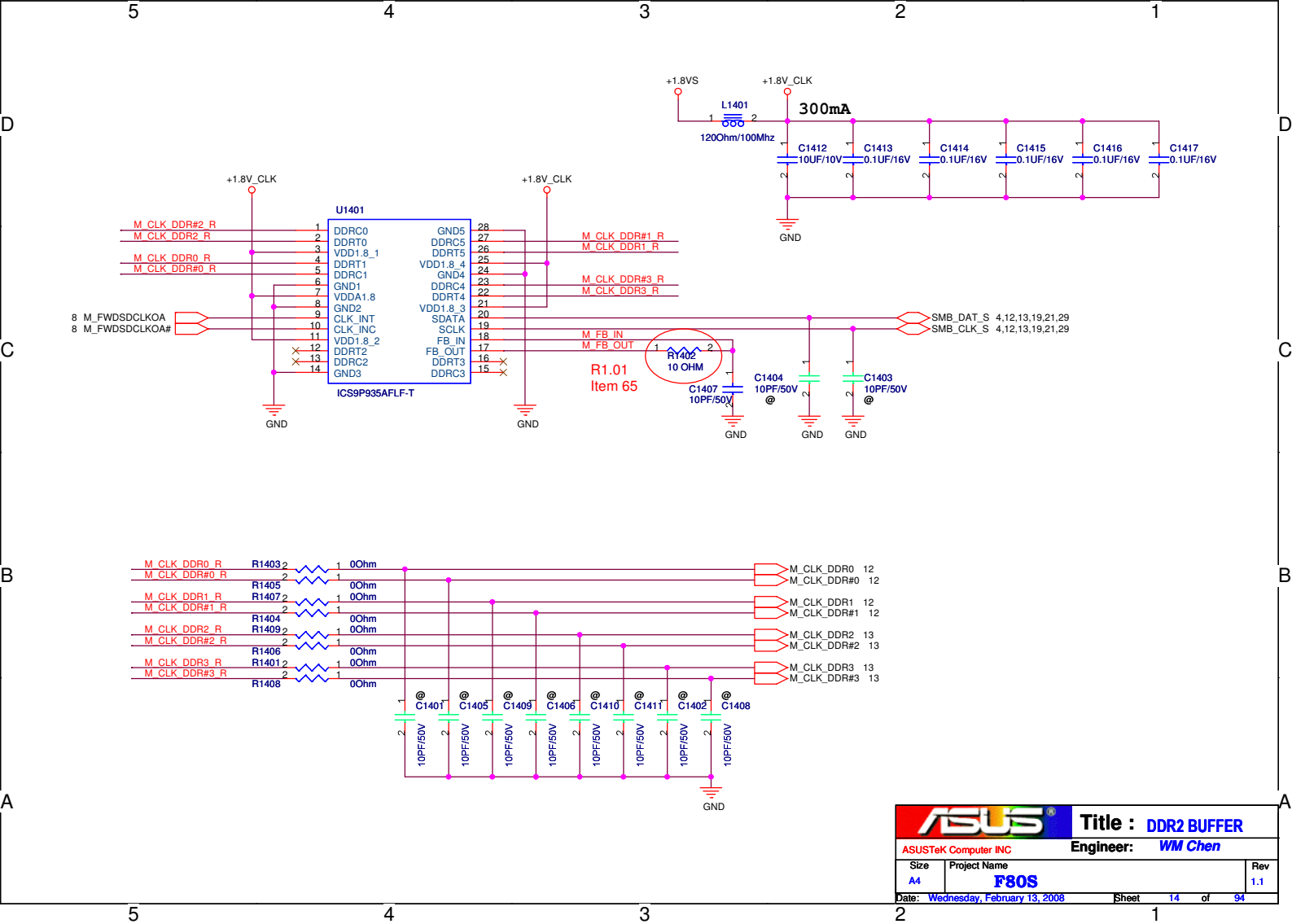




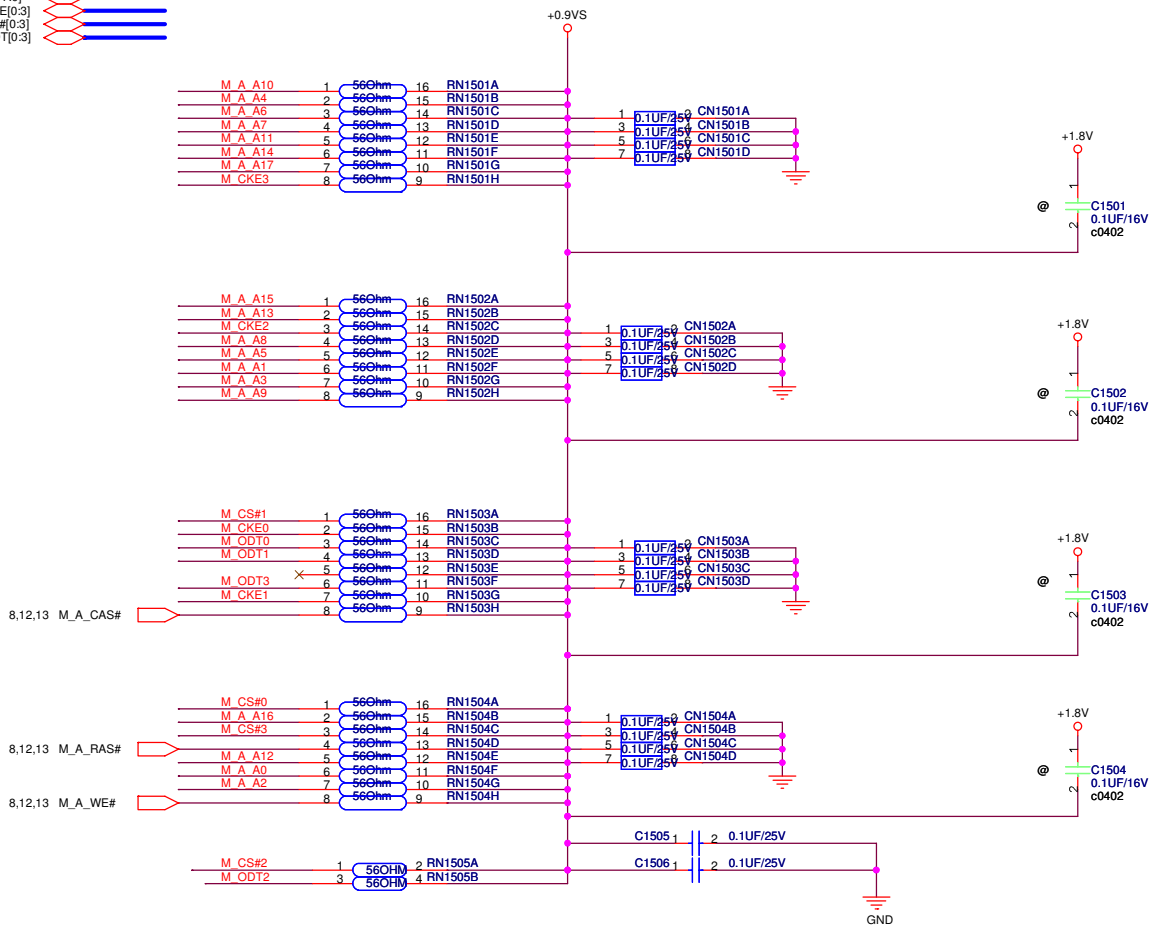
R0.4
Item 30

P/N : 12G025C22002 H:9.2mm





8,12,13 M_A_A[17:0]
8,12,13 M_CKE[0:3]
8,12,13 M_CS#[0:3]
8,12,13 M_ODT[0:3]

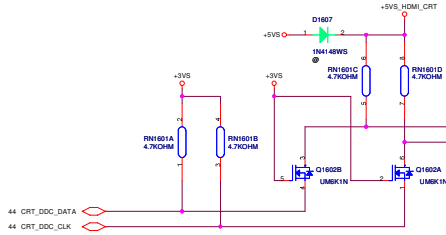
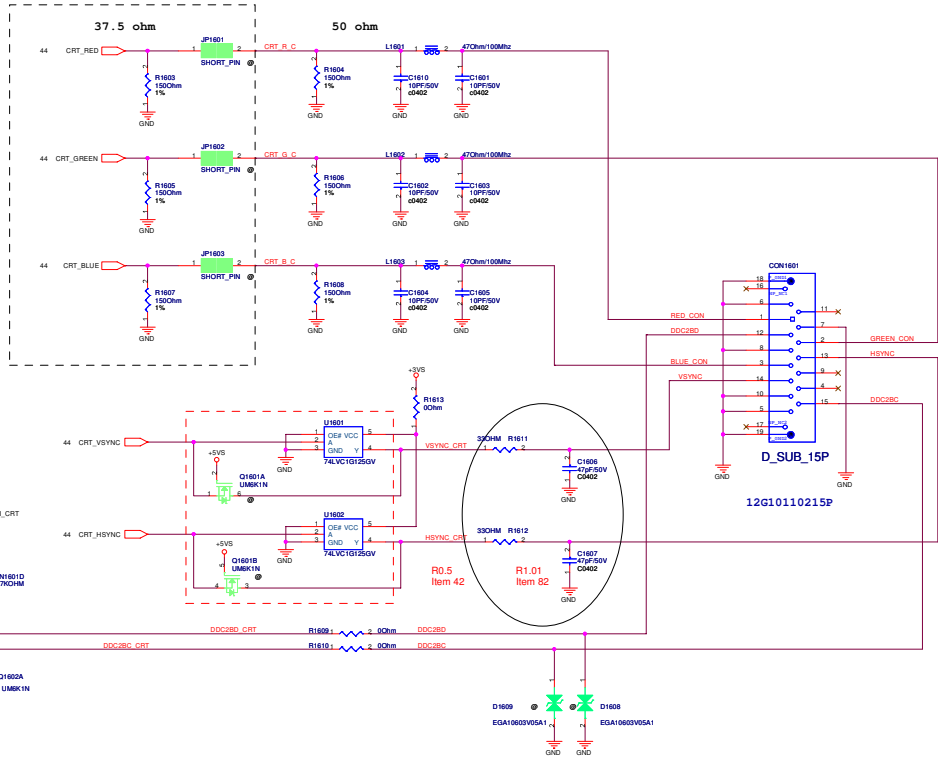
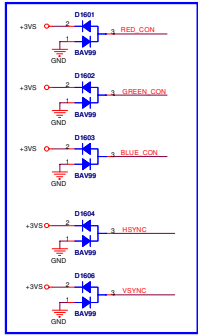


Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

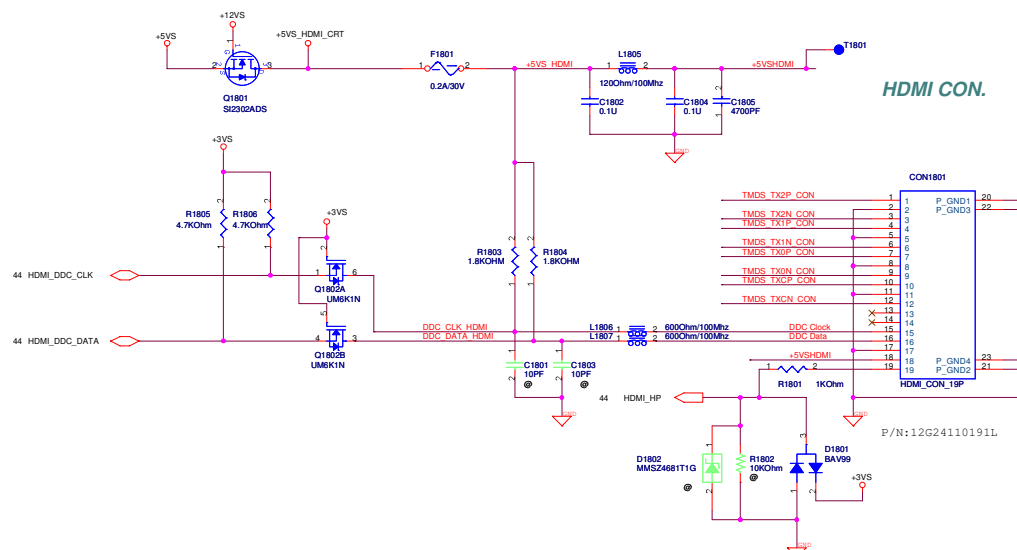
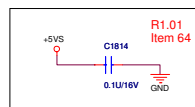
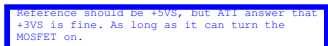
ASUS		Title : DDR2 TERMINATION	
ASUSTeK Computer INC		Engineer: WM Chen	
Size A4	Project Name F80S		Rev 1.1
Date: Wednesday, February 13, 2008		Sheet 15 of 94	

Layout note: Near U4401

PLACE ESD Diodes near connector

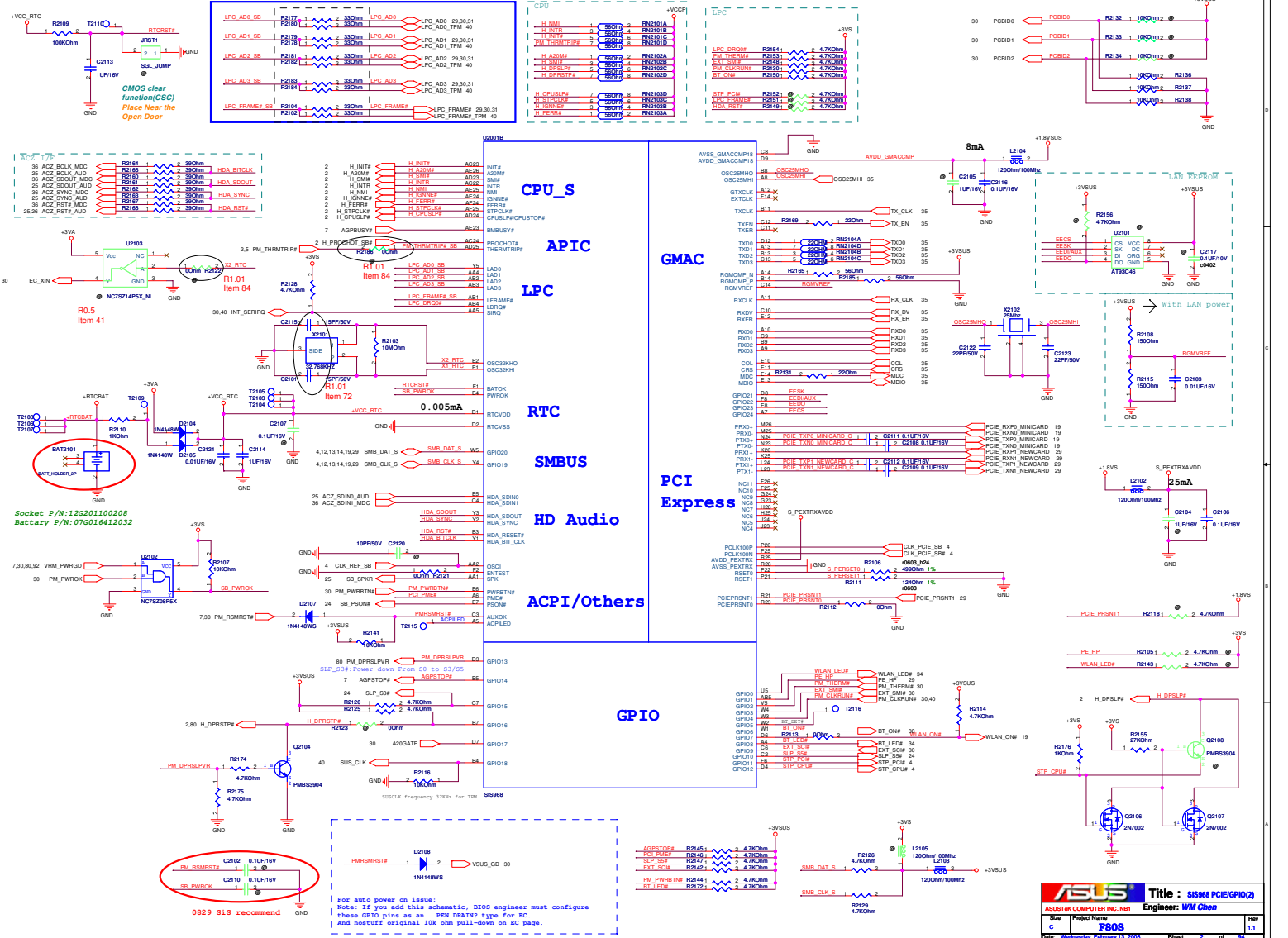


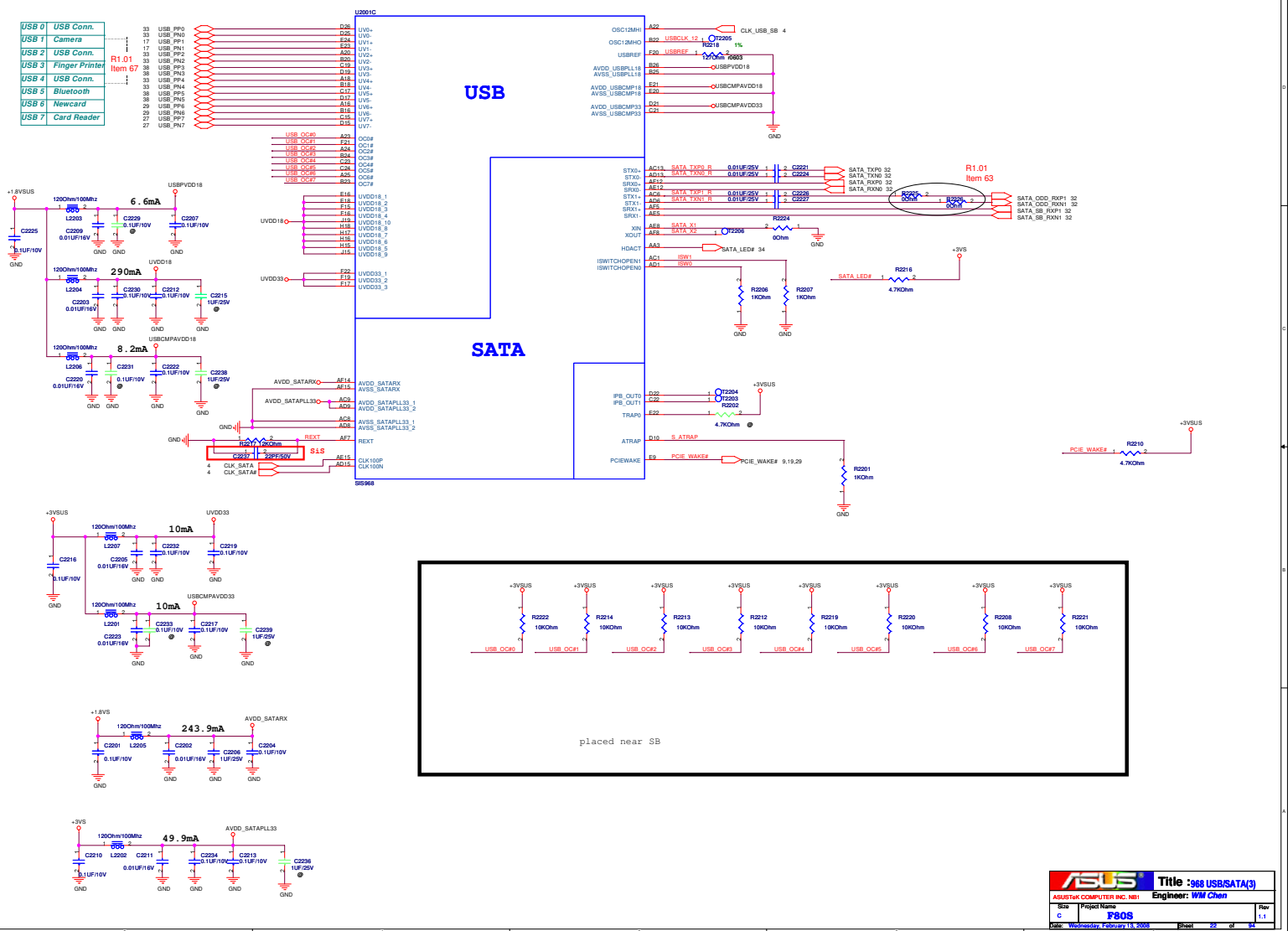
near the HDMI connector

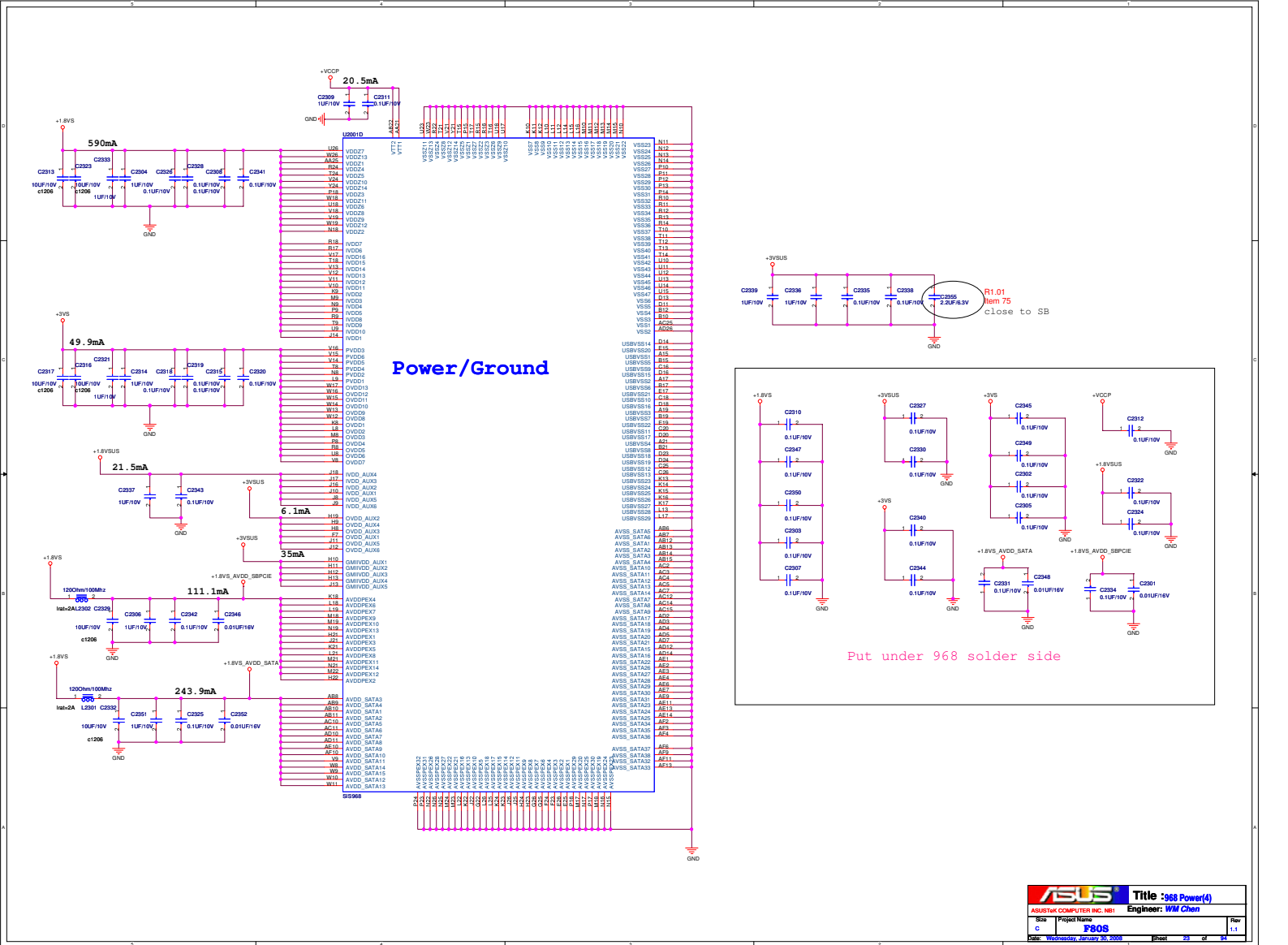


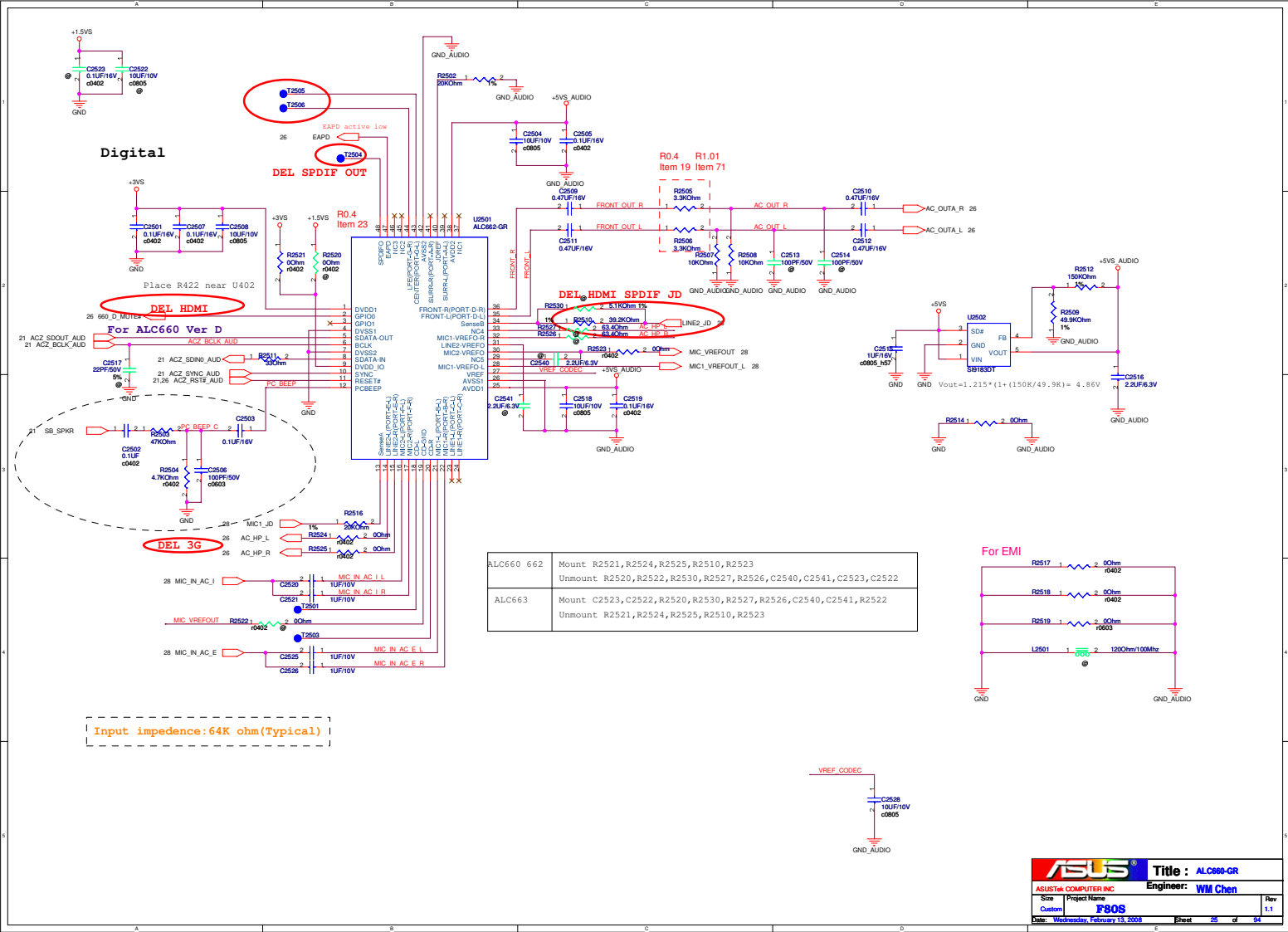
Note: 1. L1805,L1806,L1807: For EMI.(default=0 ohm)
2. DDC_CLK_HDMI,DDC_DATA_HDMI: +5V tolerant

		Title : TV & HDMI
ASUSTeK COMPUTER INC		Engineer: WM Chen
Size Custom	Project Name F80S	Rev 1.1
Date: Wednesday, February 13, 2008		Sheet: 18 of 94

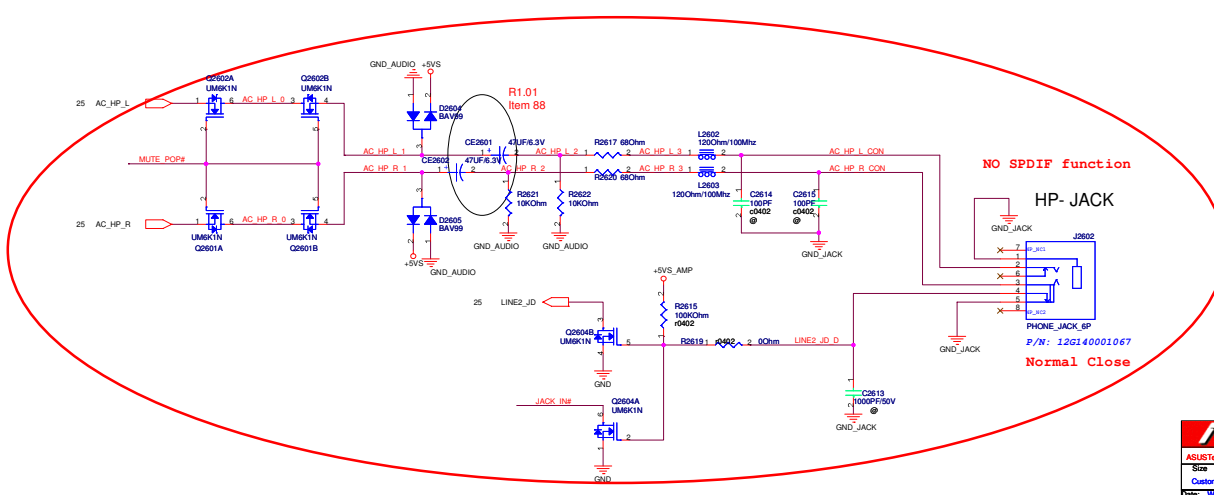
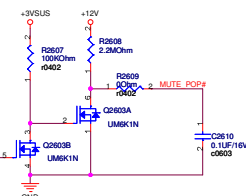
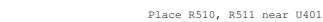
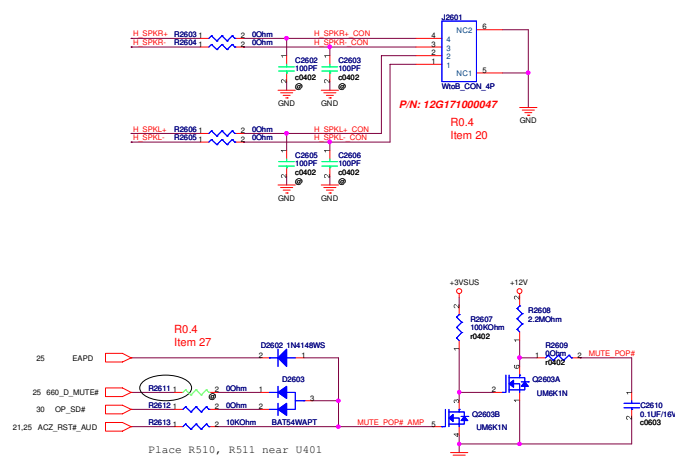
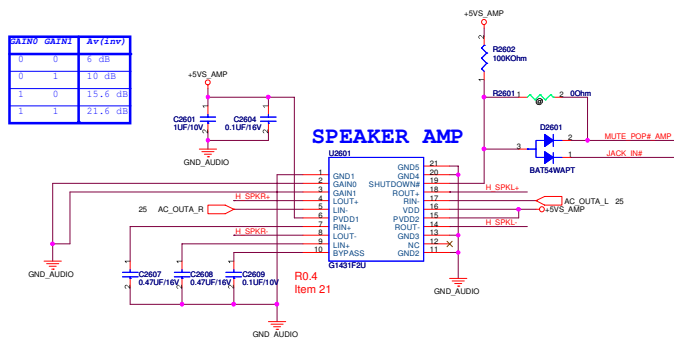


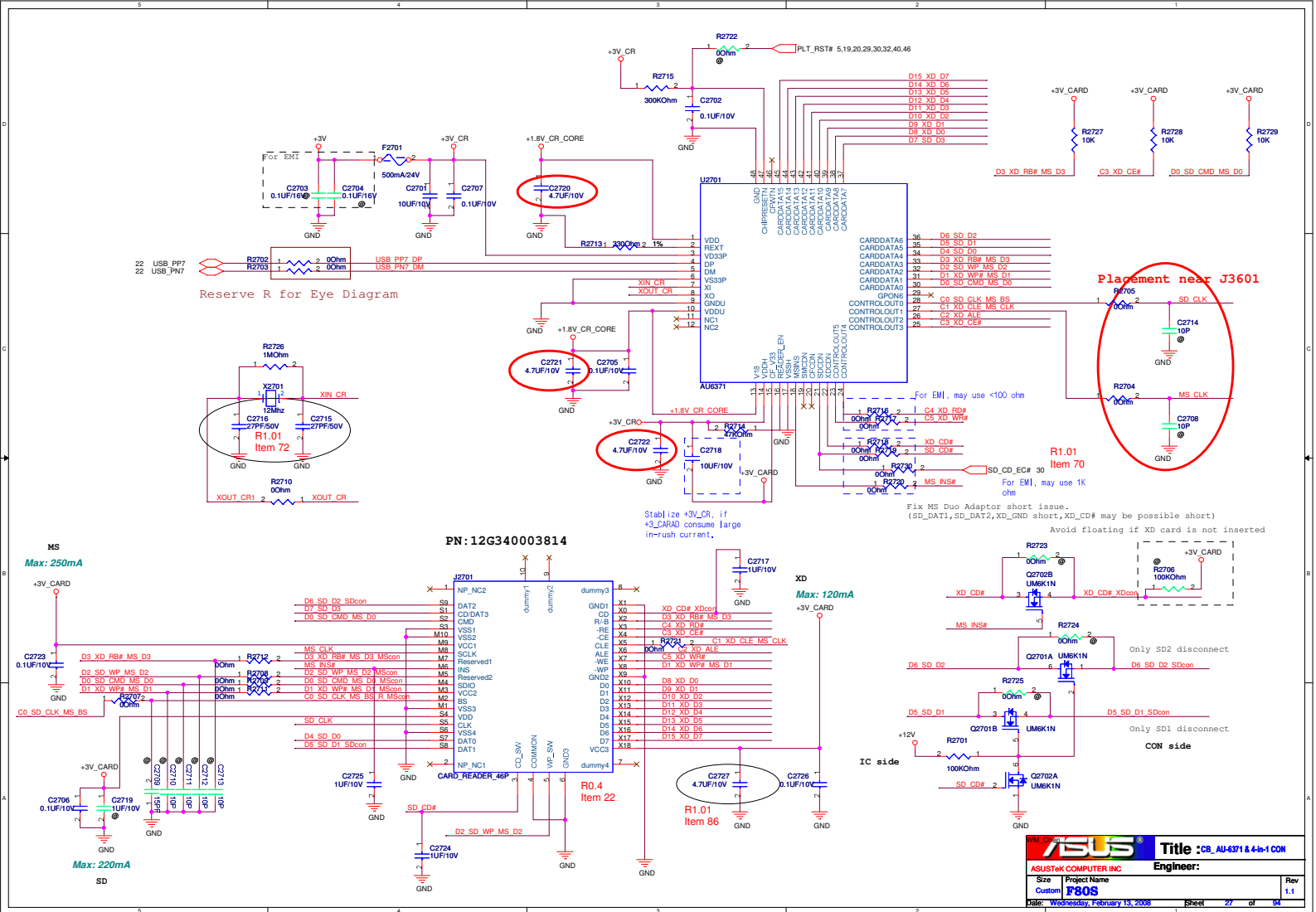




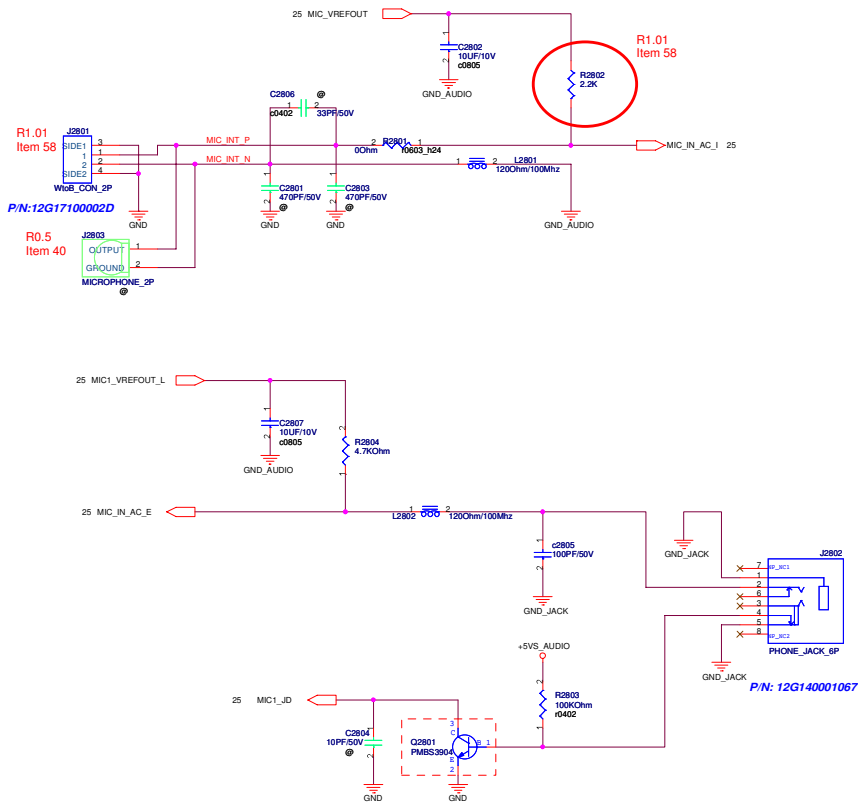


GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB





Internal MIC Pre-Amplifier

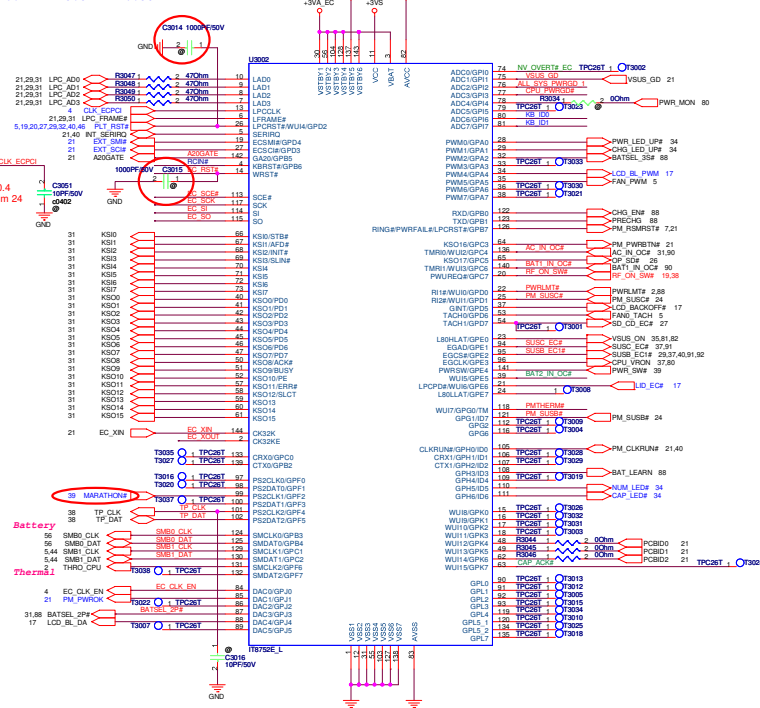


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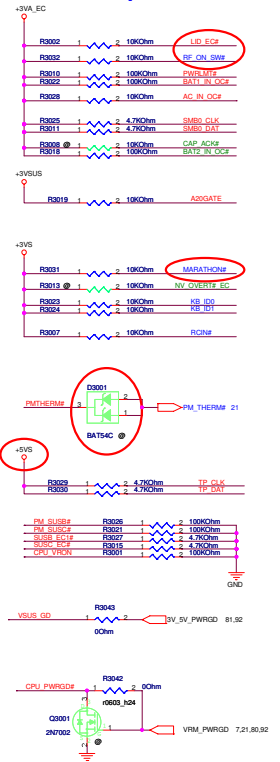
ASUS		Title : MICROPHONE	
ASUSTEK COMPUTER INC		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008		Sheet	28 of 54

IT8752 Core Chip

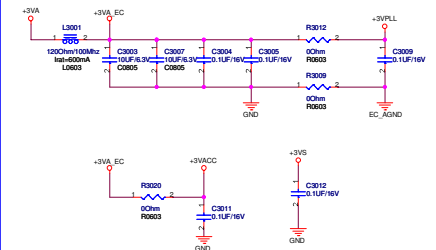
Standby (Sleep) Power Consumption:
0.1mA * 3.3V = 0.33mW



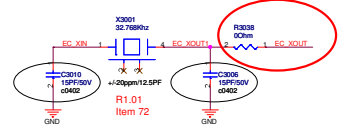
EC Pull-Up/Down



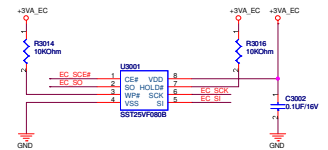
EC Power



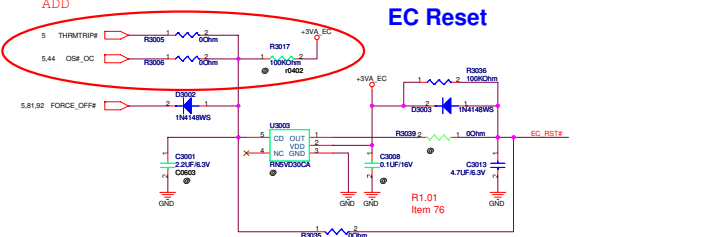
EC XTAL



SPI ROM



EC Reset



Pinout diagram for the N25G162002402 memory module. The diagram shows a 26-pin connector with pins labeled SIDE1 (1-13) and SIDE2 (14-26). Pin 1 is connected to CS0, pin 2 to CS1, pin 3 to CS2, pin 4 to CS3, pin 5 to CS4, pin 6 to CS5, pin 7 to CS6, pin 8 to CS7, pin 9 to CS8, pin 10 to CS9, pin 11 to CS10, pin 12 to CS11, pin 13 to CS12, pin 14 to CS13, pin 15 to CS14, pin 16 to CS15, pin 17 to CS16, pin 18 to CS17, pin 19 to CS18, pin 20 to CS19, pin 21 to CS20, pin 22 to CS21, pin 23 to CS22, pin 24 to CS23, pin 25 to CS24, and pin 26 to CS25. A GND symbol is shown at the top right, and a 5V symbol is shown at the bottom right.

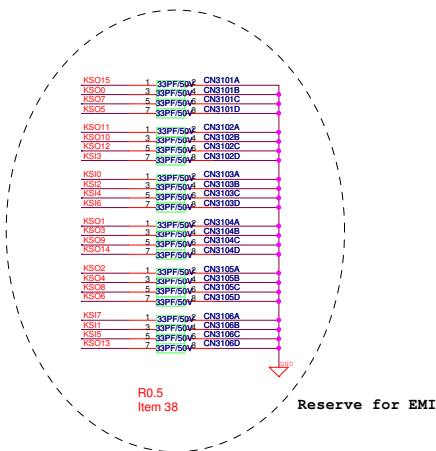


Diagram showing the connection for the bottom contact of the PFC_CDN_12P connector. The connector pins are labeled 12, 13, and 14. Pin 12 is connected to LPC_AD0. Pin 13 is connected to LPC_AD1. Pin 14 is connected to LPC_AD2. The connector is labeled PFC_CDN_12P and CON3102. The bottom contact is labeled Bottom Contact. The connector is connected to a 3V3 supply and a 100nF capacitor to ground.

30.88 BATSEL 2PW
30.90 AC_IN_OC#

U3101
74LVC16B06W

1 INB VCC
2 INA
3 GND OUTTY
4

5

3.3V EL
R0.4
Item 14
C3105 0.1UF16V
GND

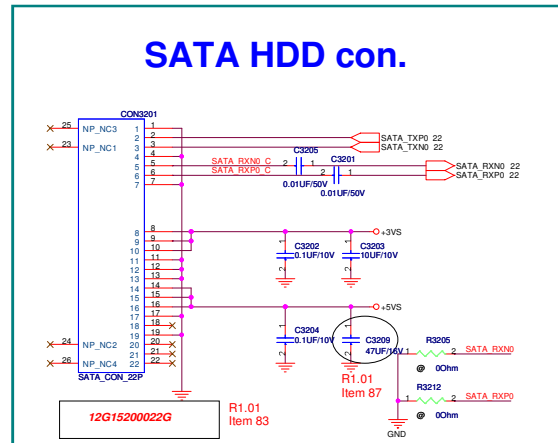
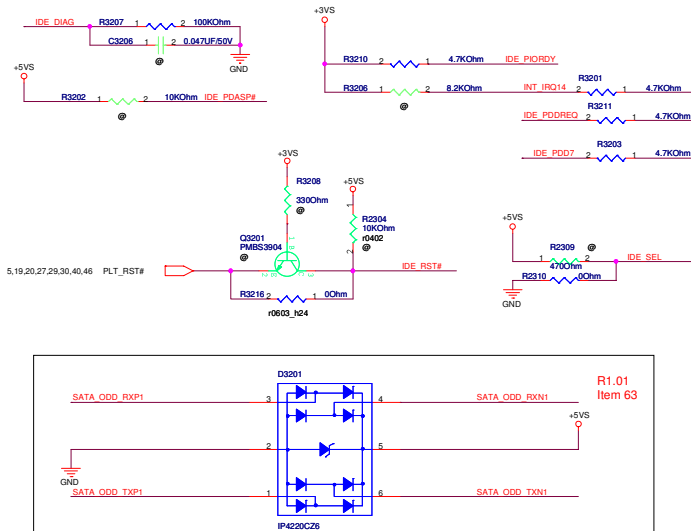
U4MKTN
C3101B

H_PROCHOT_S# 2

GND

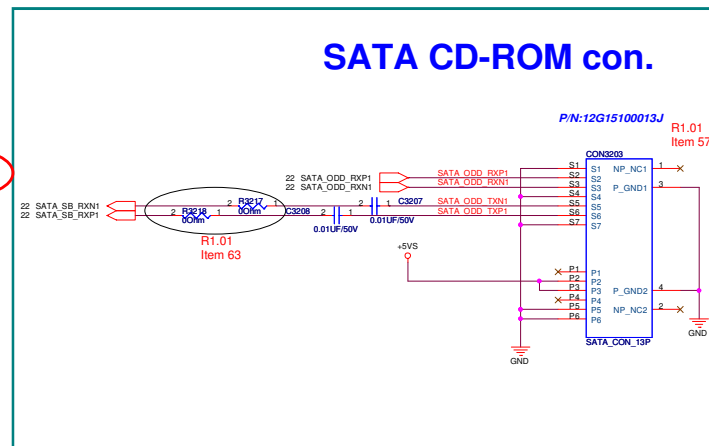
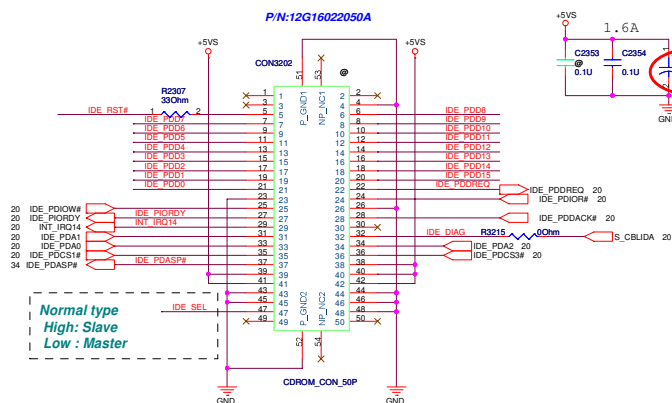
~Variant Name~

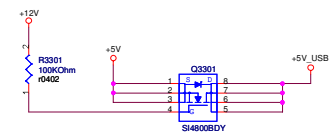
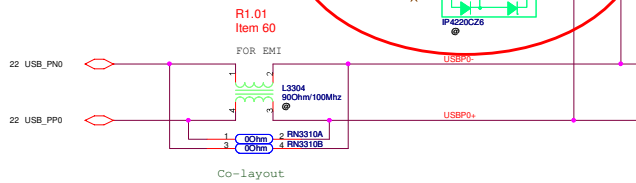
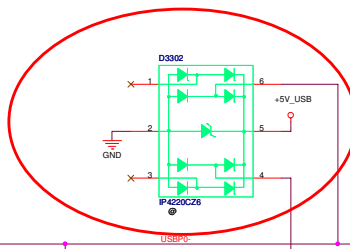
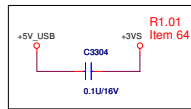
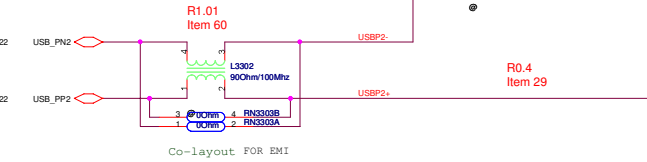
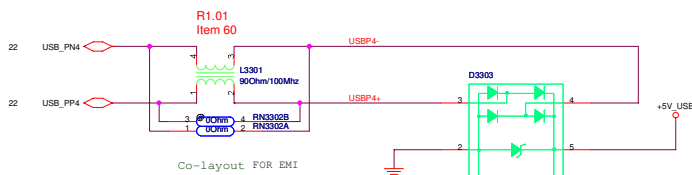
		Title : KB conn	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Size Custom	Project Name F80S		Rev 1.1
Date: Wednesday, February 13, 2008		Sheet 31	of 94



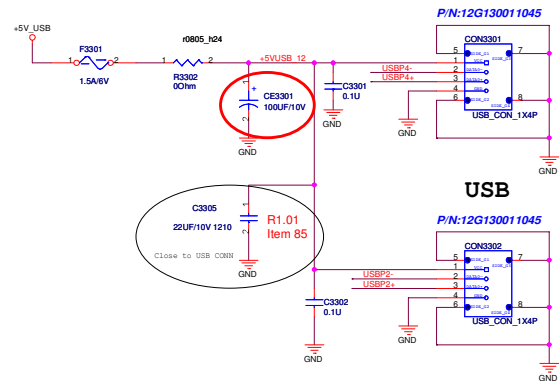
CD-ROM

PATA CD-ROM CON



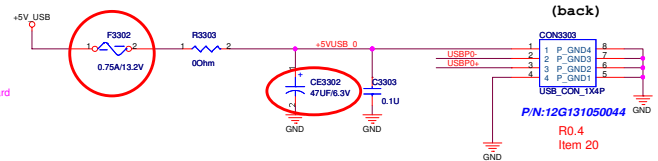


USB



USB

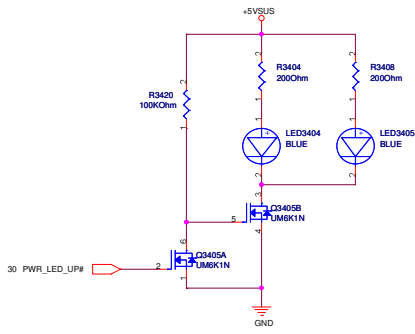
USB (back)



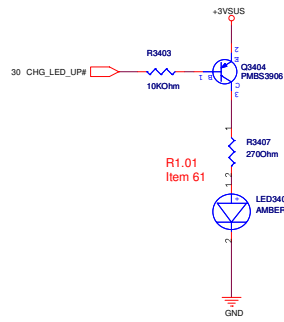
<Variant Name>

		Title : USB PORTS	
ASUSTeK COMPUTER INC		Engineer: WM Chen	
Size	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008		Sheet	33 of 34

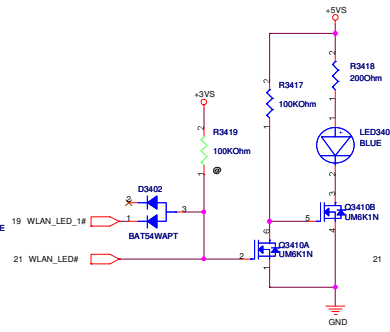
PWR LED



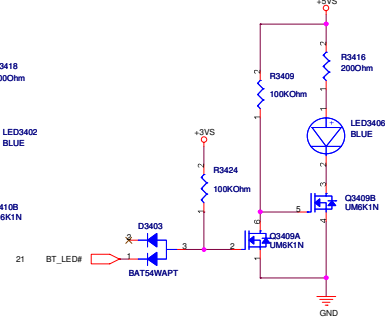
For BATTERY LED



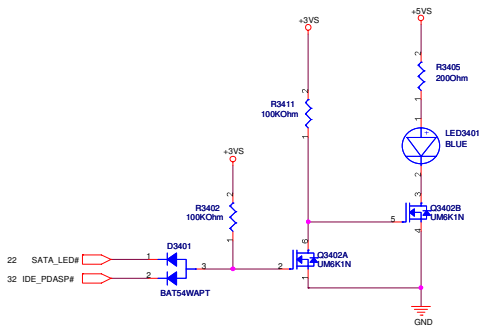
WireLess LED



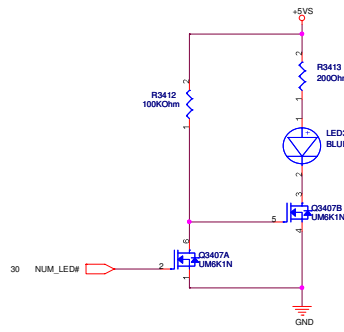
BT LED



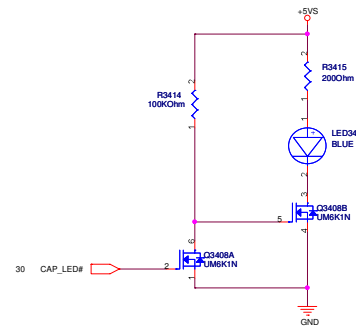
SATA/IDE LED



Num Lock



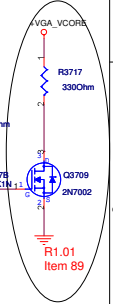
Cap. Lock



<Variant Name>

ASUS		Title : LED	
ASUSTeK COMPUTER INC		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008		Sheet 34 of 34	

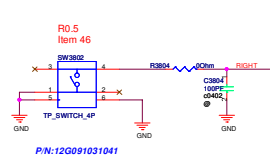
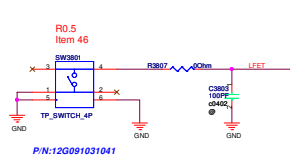
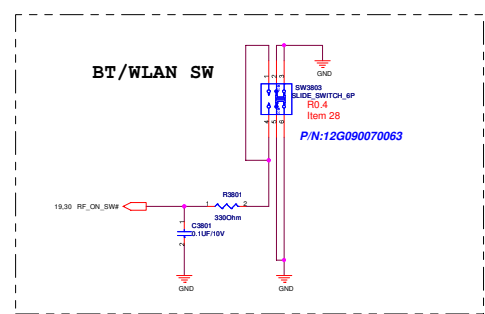
System Power Sequence
+VCCRSTC -> RTCRST# -> V5REFSUS -> 3.3/1.5VSUS<
RSMRST# -> SUSC# -> SUSB# -> VCCLAN -> LANPWROK
-> V5REF -> PWROK -> GMCH -> VCCP -> VCORE
SUSSTAT# -> PCIRST#
CPU : +VCORE, +VCCP, +1.05VS
NB : +1.05VS, +1.2VS, +2.5V, +VCCP
SB : +1.2VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
DDR : +1.8V, +0.9VS



<Variant Name>

ASUS		Title : DISCHARGE CKT	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Size	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008		Sheet	37 of 54

The schematic diagram illustrates the electrical connections for two components, R0.4 Item 15 and R0.5 Item 44. Both components are powered by a +5V5_TP supply and connected to a common ground. The R0.4 Item 15 component includes a U3002 oscillator, a C3002 capacitor, and a U3001 component. The R0.5 Item 44 component includes a C3812 capacitor, a C3813 capacitor, a U3801 component, and a U3810 oscillator. The diagram also shows connections to a PFC_CON12P pin and a R0.4 Item 28 component.

[illegible]

Finger Printer Conn.

R0.4
Item 28

C0K3800
FPC CON. 4P
PN:12G182400604

C8067
C0A 1.0uF 16V

C8065
C0A 1.0uF 16V

L3803
BOC 0.1uF 100MHz

L3801
BOC 0.1uF 100MHz

R1.1
Item 60

L3804
BOC 0.1uF 100MHz

FOR EX1

USBP3

USBP3+

D0801
F4205CZ26

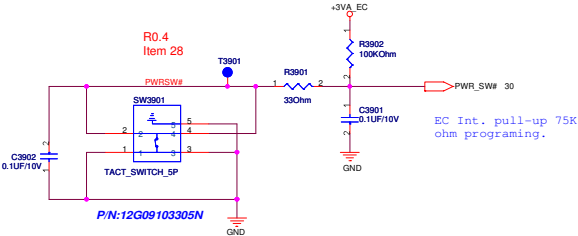
C8065
C0A 1.0uF 16V

From +3v to +3V EX R1.1 modify

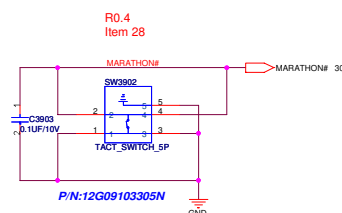
+3V

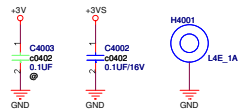
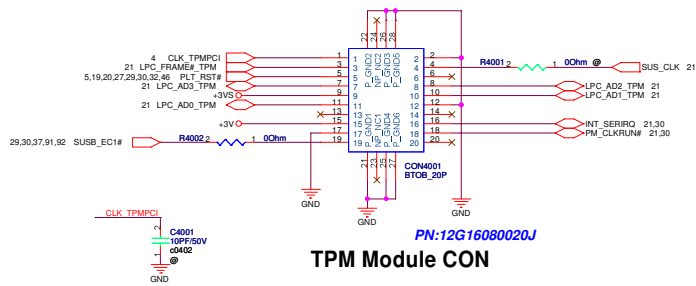
GND

Power Button

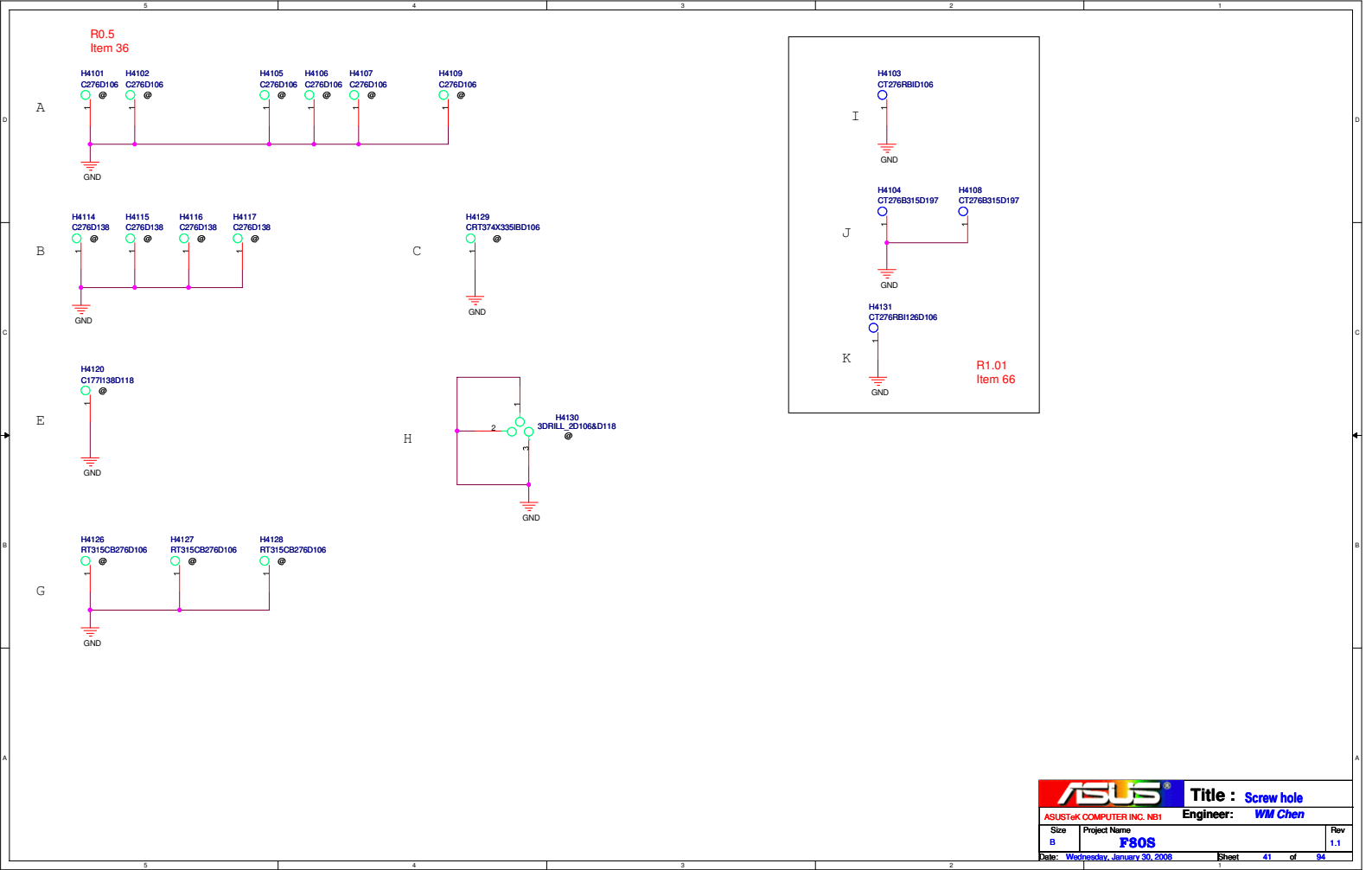


MARATHON#



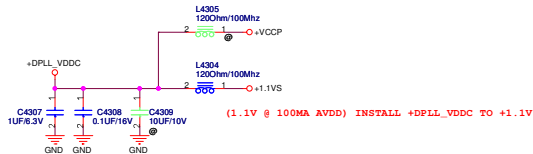
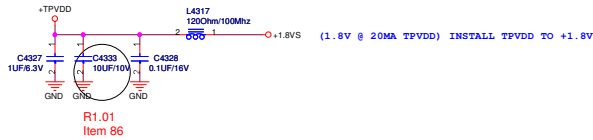
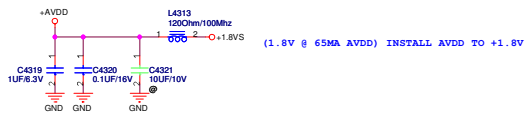
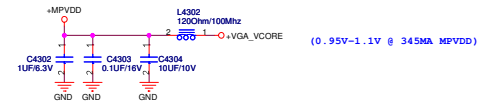
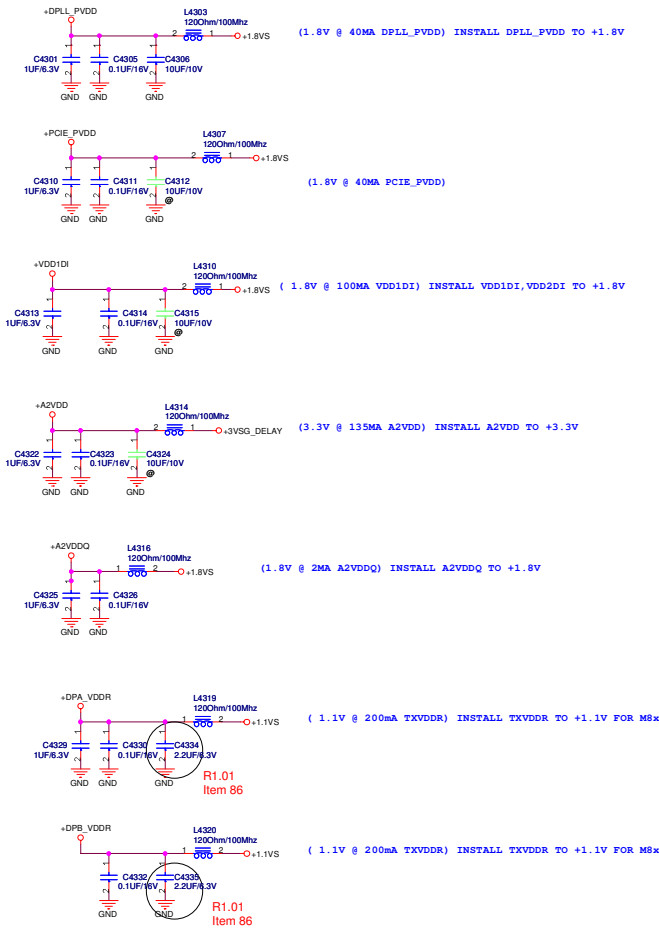


<Variant Name>			
ASUS		Title : TPM	
ASUSTeK COMPUTER INC. NE1		Engineer: WM Chen	
Size	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008		Sheet	40 of 54



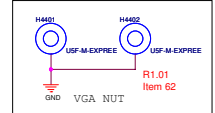
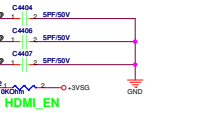
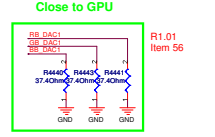
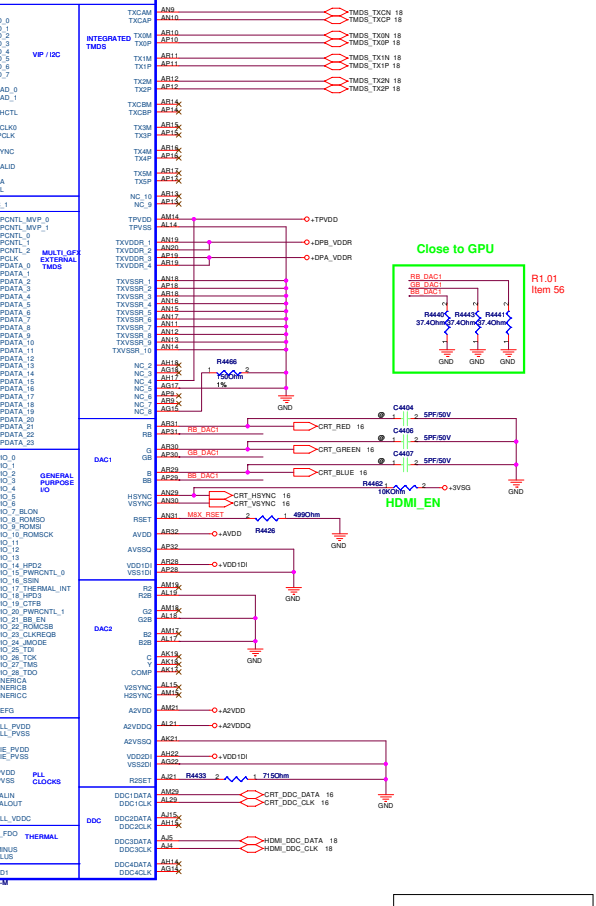
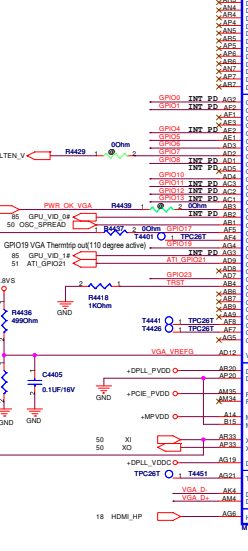
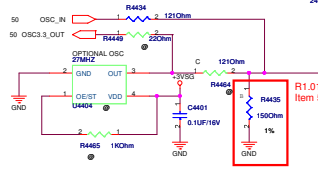
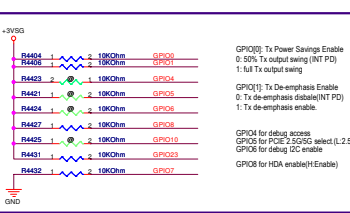
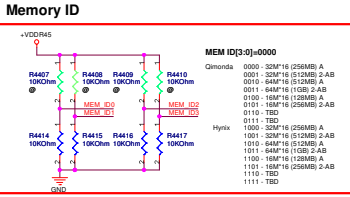
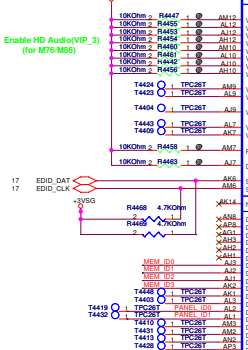
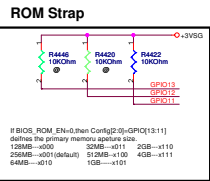
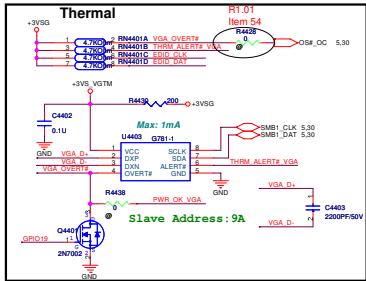
M8x Power

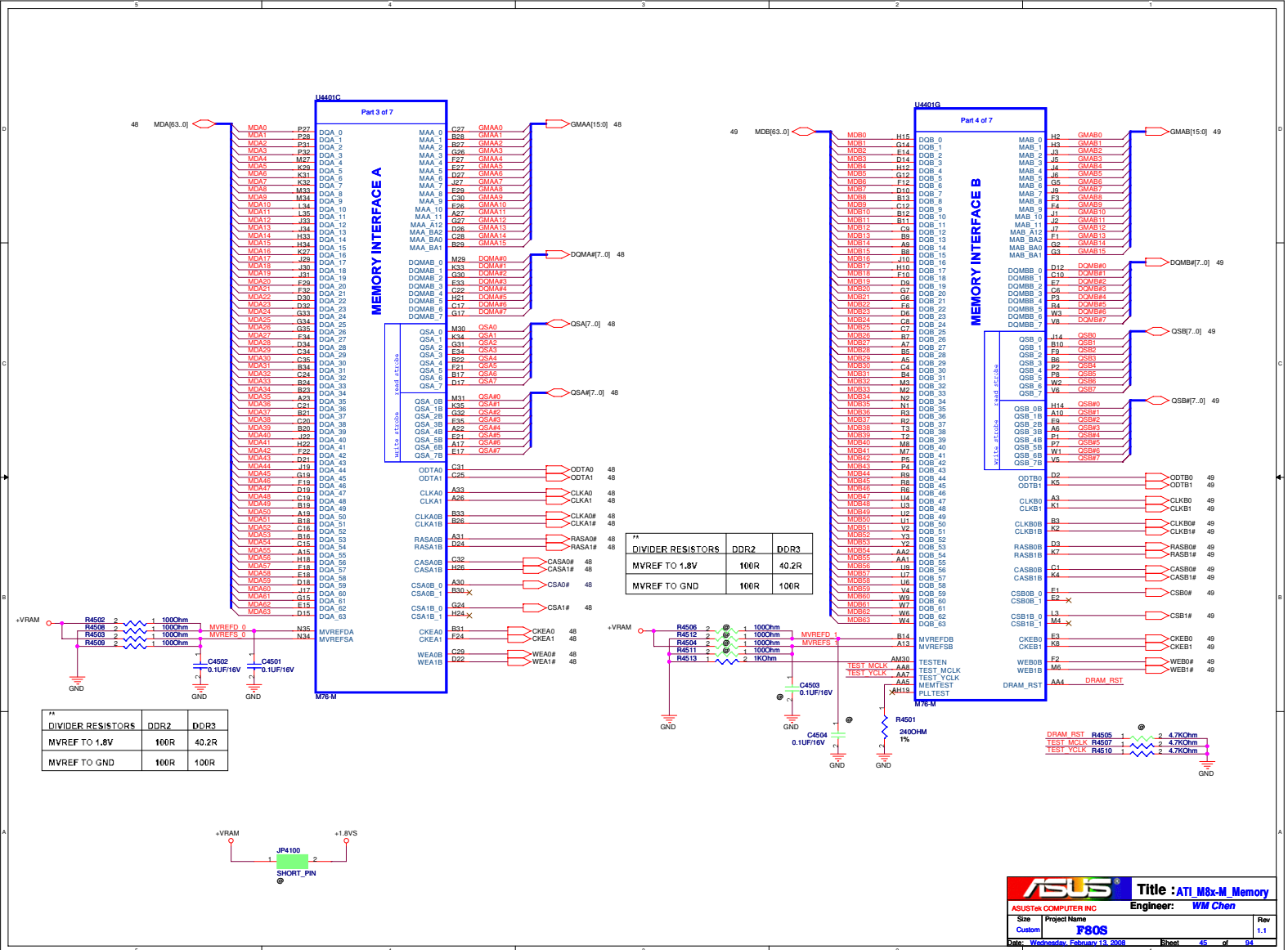
PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

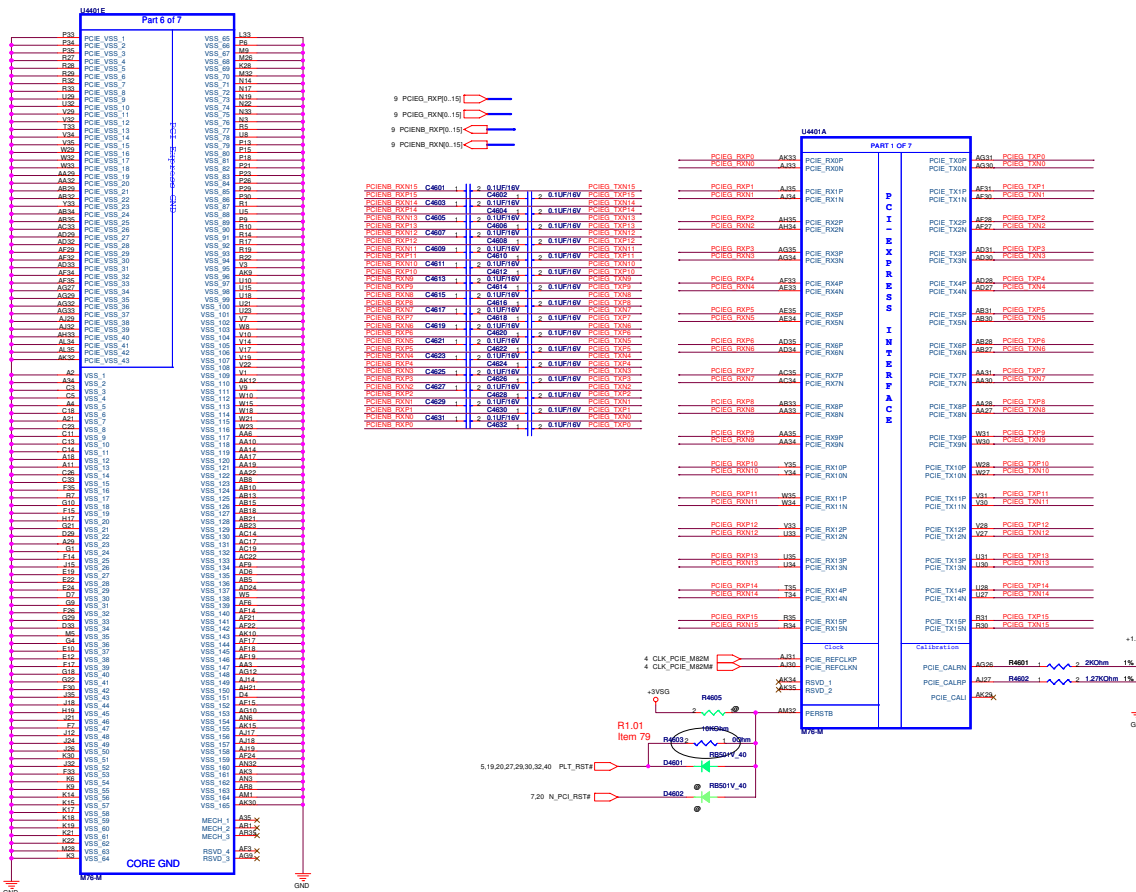


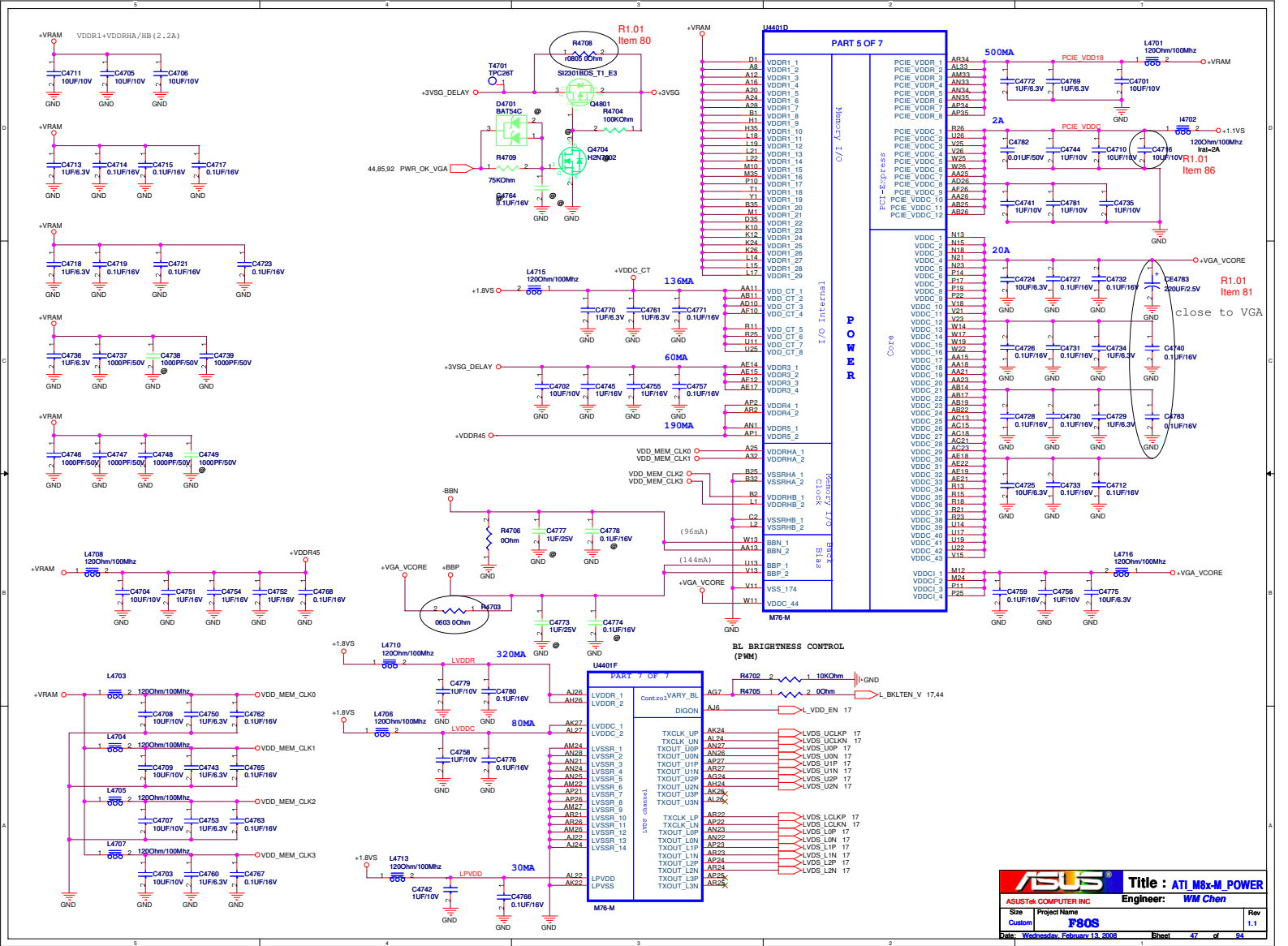
<Variant Name>

ASUS		Title : VGA M8x-M POWER	
ASUSTeK COMPUTER INC		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, January 30, 2019		Sheet	43 of 54

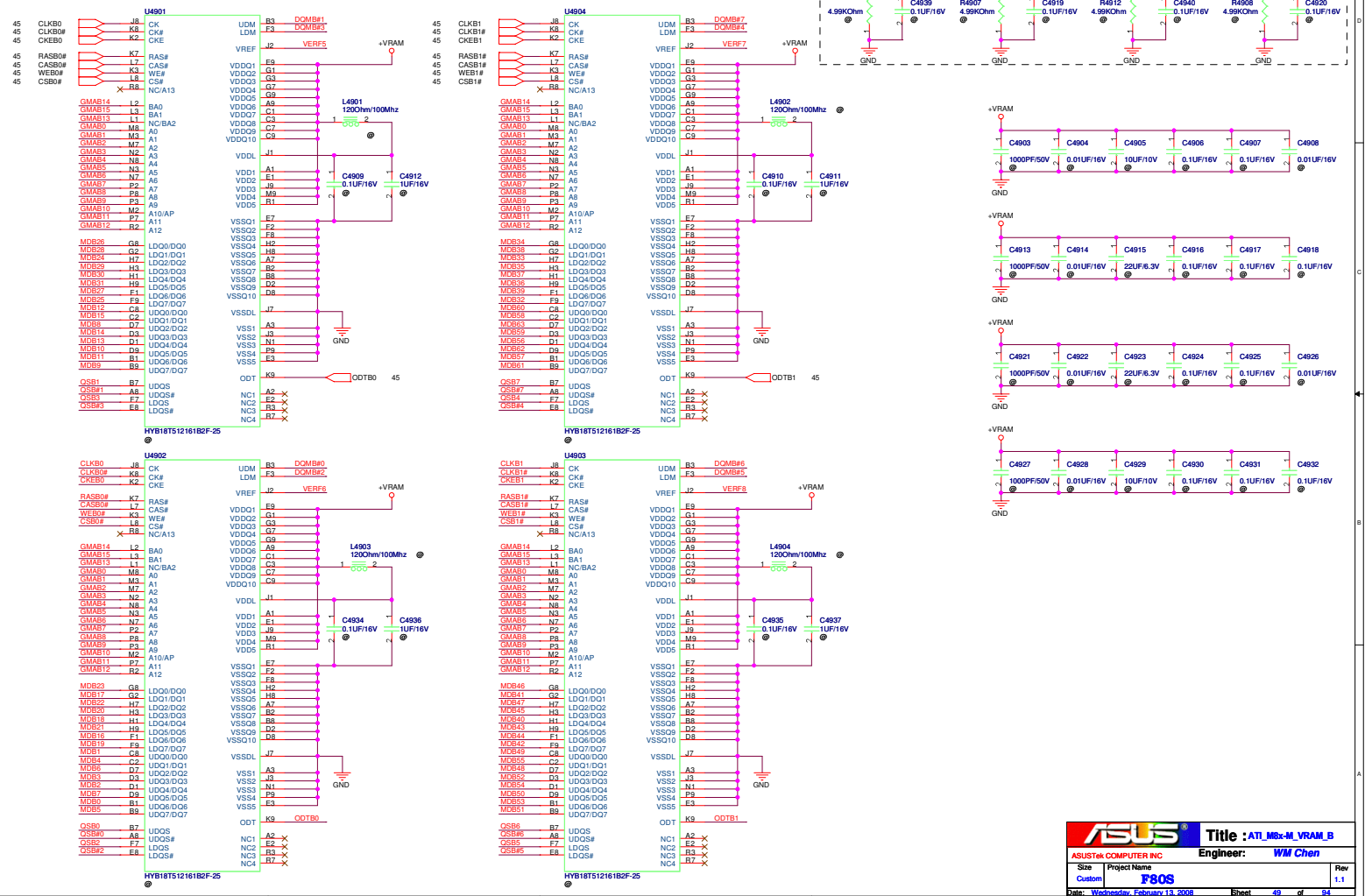


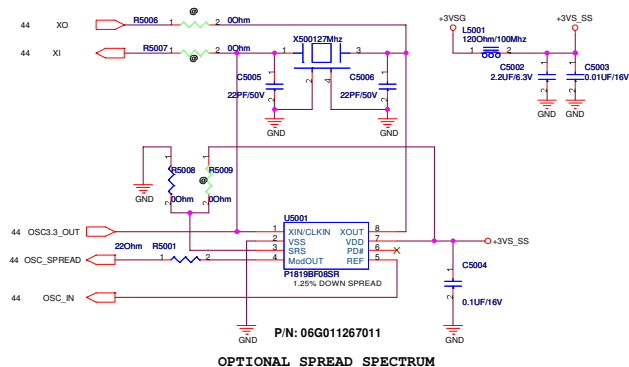






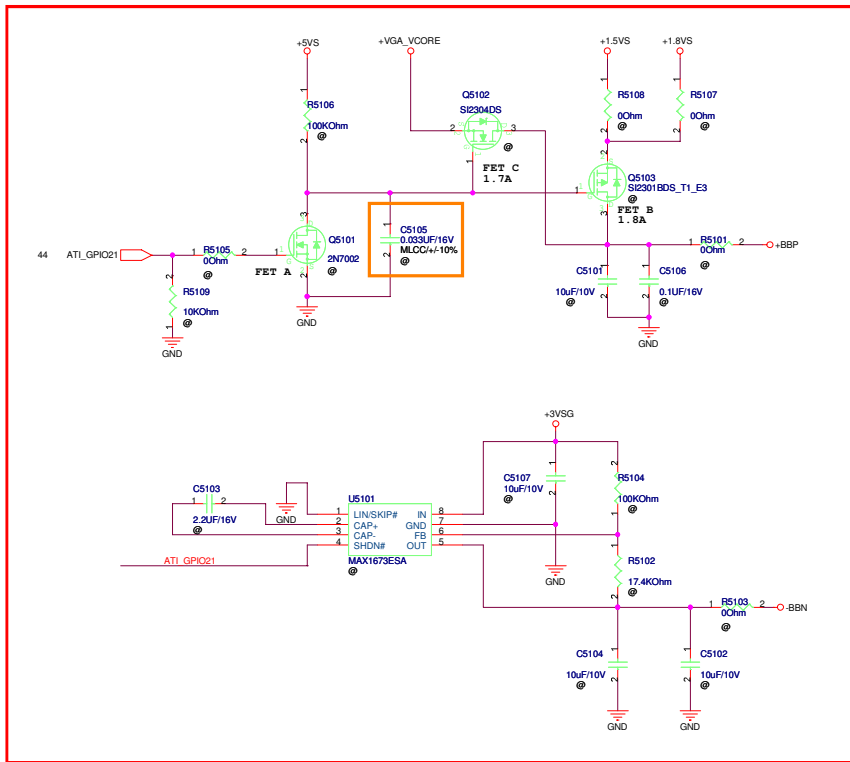
DO NOT INSTALL CHANNEL B
WITH M82M





COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED

R0.4
Item 30



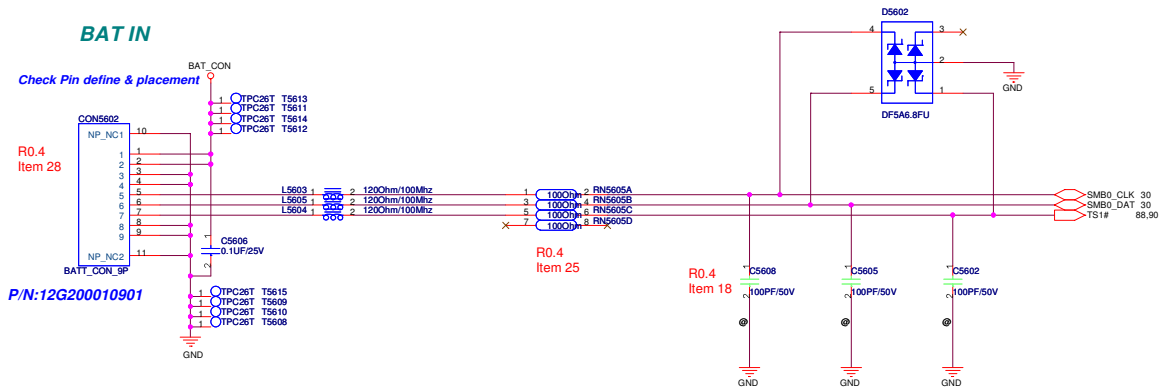
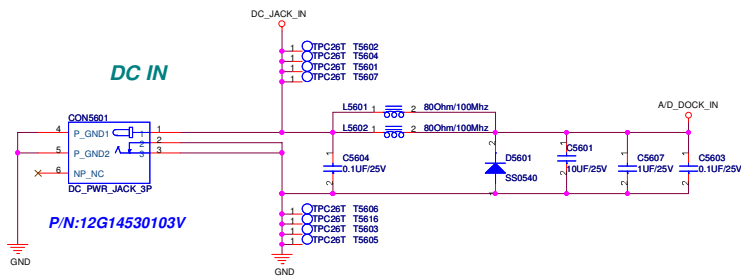
BB_ENA = 0V FOR BACK BIASING DISABLED
MAX1673 SHUTDOWN
-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND
N FET A = OFF, P FET B = OFF, N FET C = ON
+BBP = +VGA_CORE

BB_ENA = +3.3V FOR BACK BIASING ENABLED
MAX1673 ENABLED
-BBN = -.5V
N FET A = ON, P FET B = ON, N FET C = OFF
+BBP = +1.5V

GPIO_21_BB_EN	+BBP
0	1.1V
1	1.5V

GPIO_21_BB_EN	-BBN
0	GND
1	-0.5V

ASUS		Title : BACK BIAS	
ASUSTek COMPUTER INC. NBI		Engineer: WM Chen	
Size B	Project Name F80S	Rev 1.1	
Date: Wednesday, February 13, 2008		Sheet 51	of 94



R0.4
Item 31

		Title : Empty	
ASUSTeK COMPUTER INC. NB1		Engineer: WM Chen	
Size	Project Name		Rev
A	F80S		1.1
Date: Wednesday, January 30, 2008		Sheet	57 of 94



Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: *WM Chen*

Size

A

Project Name	
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F80S

Rev

1.1

Date: Wednesday, January 30, 2008

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R0.4 revision history:

1. Delete R511,R515,D503,C503,C509,Q505,R506 from 100K change to 0ohm for better signal quality .
2. Change D3302,D3303,D2107 from 1SS355 to 1N4148WS-L for cost down.
3. Change D3401,D3402,D2601,D2603 to BAT54WAPT for cost down and common part.
4. Change D2106 to BAT54C for cost down.
5. Change U1701 to AH180-WG-7 for cost down.
6. Delete RN301,RN302 for not use on board CPU cost down.
7. Add R3047-R3050 for newcard debug card.
8. Change CAP_ACK# from pin24 to pin63 for EC(page30) pin assignment R0.06.
9. Add R3028 for net:AC_IN_OC# pull hi.
10. Change C3002 from 1uF to 0.1uF for cost down.
11. Change Q4203 from 2N7002 to PMBS3904 for cost down and MIC jack.
12. Unmount R1727 for pull hi in p34.Change L1716 to R1710 for U1701 on MB.
13. Change USB connector J2401~ J2403.
14. Unmount C3102 for cost down.
15. Reserve R3810 for prevent power short cause large current.
16. Change R3404,R3403,R3412,R3414 from 4.7K to 10K for power saving.
17. Change L3601,L3605 to R3622,R3623 for EMI fine tune cost down.
18. Unmount C5608,C5605,C5602 for EMI fine tune cost down.
19. Change R2505,R2506 from 680ohm to 2.7Kohm for 1W speaker.
20. Change CON3303,J2601 part number for ME request.
21. Change U2601 from TI to GMT,C2609 to 0.1uF for cost down.
22. Change card reader connector J2701 part number for connector in bottom side.
23. Change U2501 from 660 to 662 for the logo request codec need 2-ADC after 2008/6.
24. Reserve C3051 for fine tune CLK_ECPCI.
25. Add RN5605 for protect EC to prevent voltage damage.
26. Change CON3802 pin assignment for use W7 BT cable.
27. Unmount R2611 for ALC662 not need.
28. Change SW3901,SW3902,SW3801,SW3802,SW3803,J2801,CON5602,BAT2101,CON3801,CON3803 part number for ME request.
29. Delete D3301 for cost down.
30. Add VGA Back Bias on page51 for power play function
31. +1.2VSUS from page57 change to page82 for power circuit
32. Delete H_PWRGD_EC (Q202,R233) because it's not necessary.

R0.5 revision history:

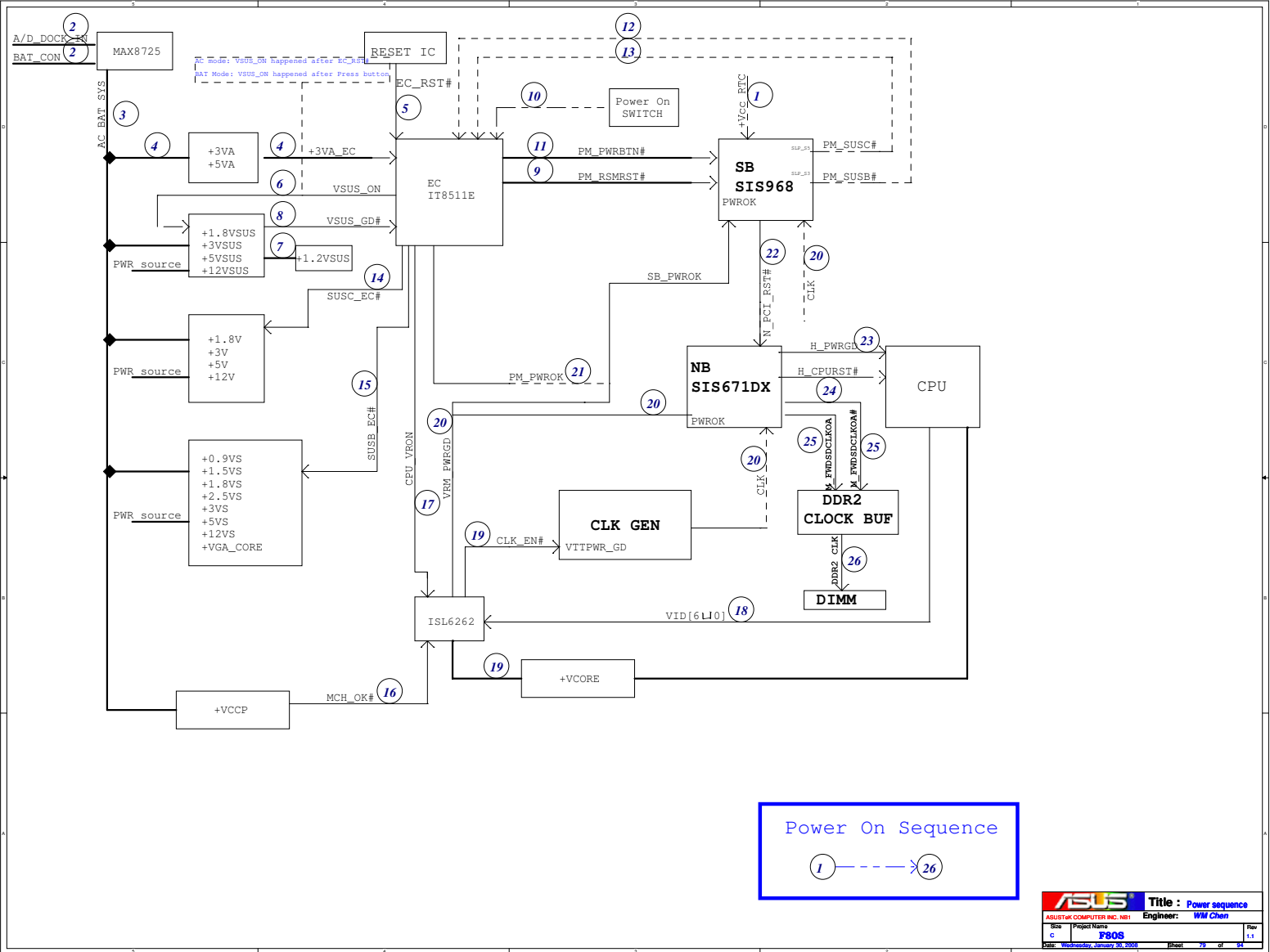
33. Reserve CON1901 pin24 to +3VAUX for Azurewave's Wireless-Lan Card.
34. Modify p25,p26 for colay ALC662 and ALC663 for sales recomment.
35. Change KB connector CON3101 part number for ME request.
36. Change Screw hole for ME request.
37. Change CON3602 part number for ME request.
38. Cap. Array CN3101-CN3106 from 0805 change to 1206 size.
39. Add H4401,H4402 VGA NUT
40. Reserve internal mic J2803 for experiment.
41. Reserve U3502,U2103 circuit for experiment.
42. Add U1601,U1602 for NB output 3.3V level cost down.
43. Change page34 LED schematic for use Blue LED.
44. Reserve C3812,C3813 for EMI request TP_GND.
45. Modify Page 22,32 for sales require SATA ODD.
46. Change SW3801,SW3802 part number for ME request.
47. Change U3001 part number for cost down.
48. Reserve R208,C202 for H_CPURST#.
49. Add U3801 for EMI request.
50. Add RN1801-RN1804 for EMI request.
51. Delete VRAM termination
52. Add Q4405,R4411,C4466 for +3VSG
53. Change Hall-sensor U1701 part number for ME request.

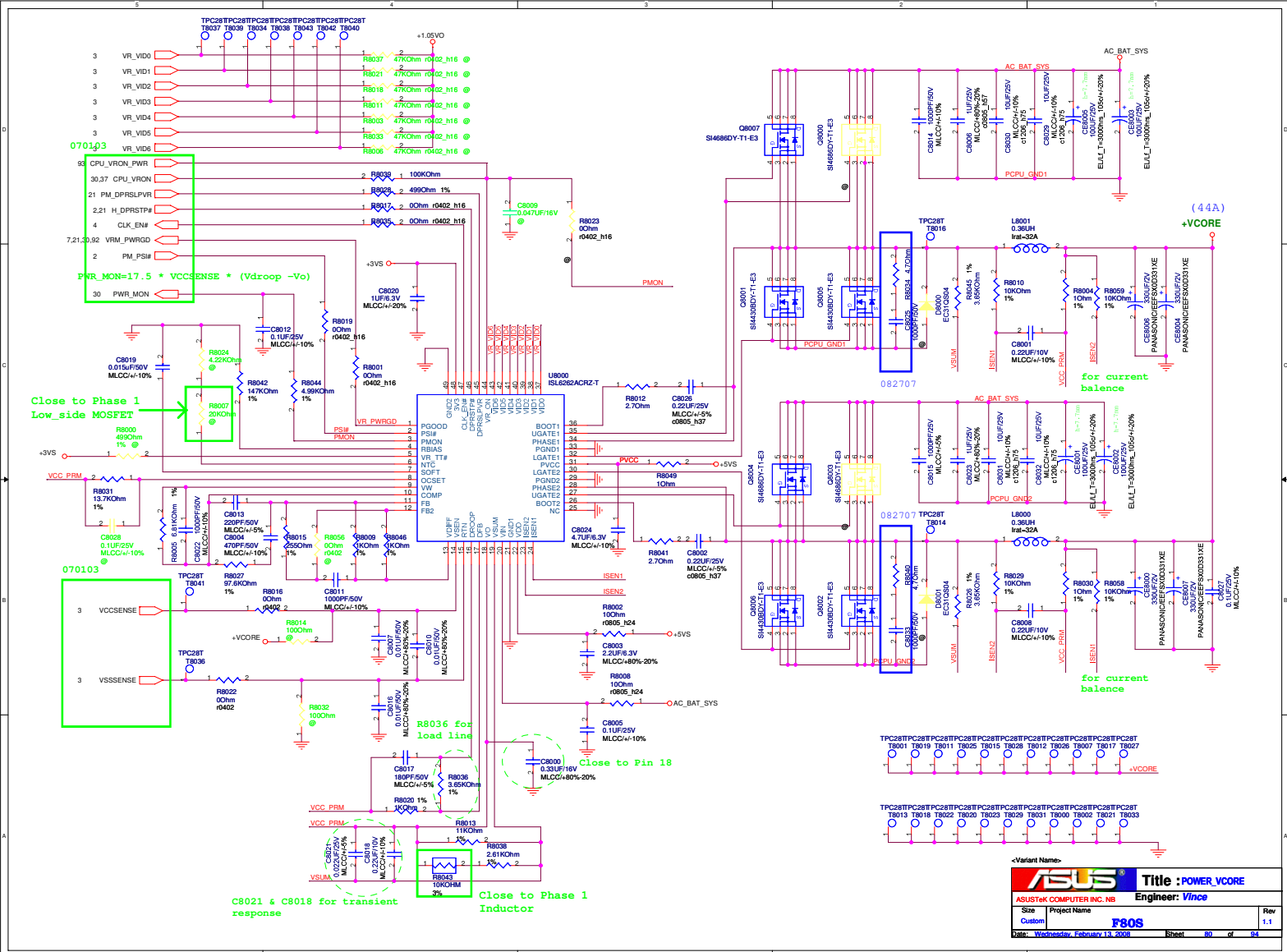
R1.01 revision history:

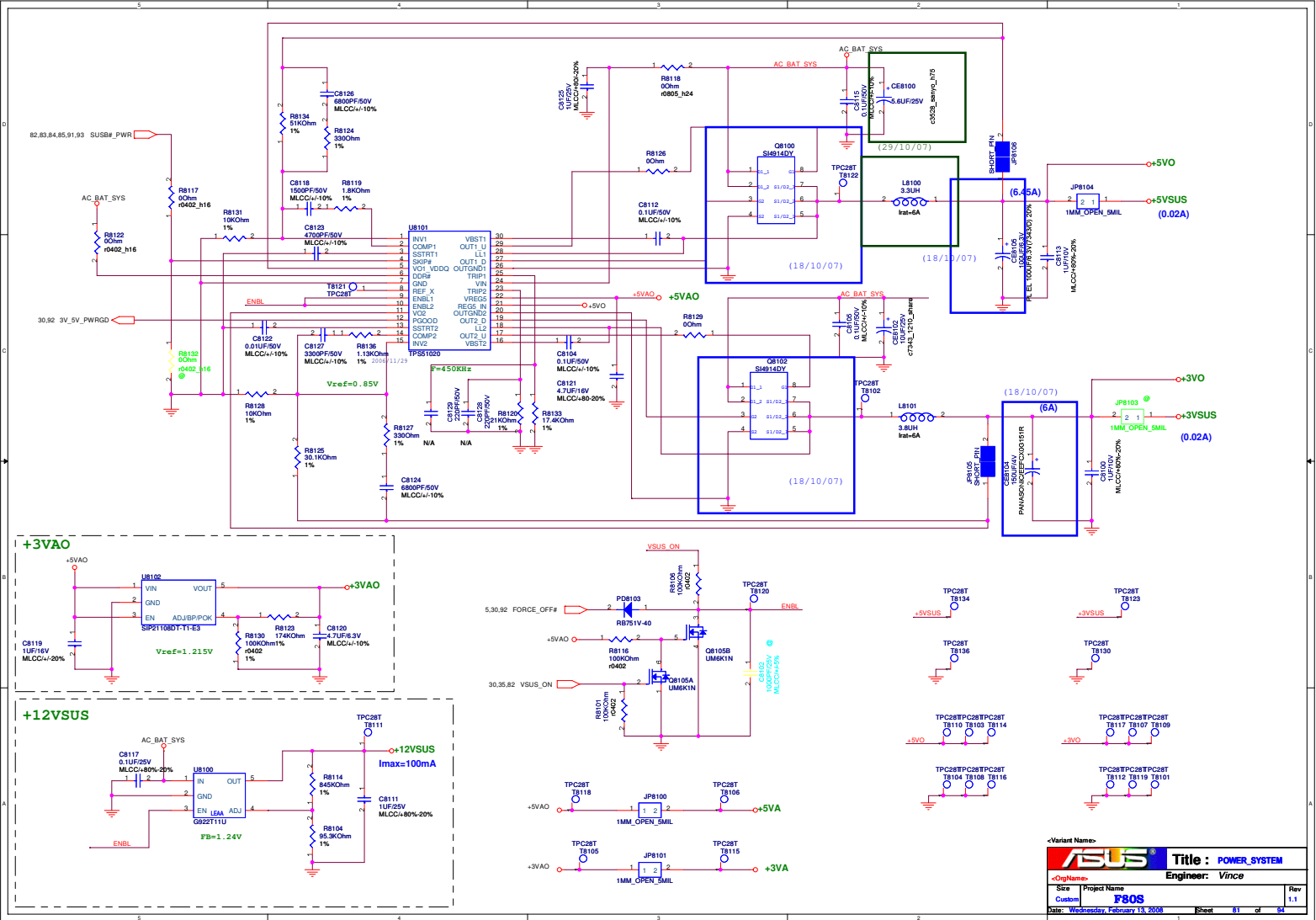
54. Unmount R4428 for leakage current issue.
55. Change R4435 from 71.5 to 150 for SIS request.
56. Mount R4440,R4441,R4443 37.4 ohm for VGA issue.
57. Change SATA ODD Connector CON3203 part number for ME request.
58. Change J2801 connector for Wire-MIC,change R2802 from 4.7K to 2.2K after test internal mic performance.
59. ADD D3603,C3609 for LAN ESD solution.
60. Change L1709,L3801,L3804,L3301,L3302,L3304,L2901 part number for colay footprint.
61. Change R3407,LED3403 value for meet factory LED spec.
62. Change VGA NUT H4401,H4402 to 13G021036001 for Thermal request.
63. Add D3201 IP4220CZ6 and R2225, R2226, R3217, R3218 0 ohm for EMI request.
64. Add C1218, C1707, C1814, C3304 0.1uF for EMI request.
65. Change R1402 from 22 to 10 for DDR Feedback quality.
66. Change Screw hole H4103, H4104, H4108 and Add H4131 for ME request.
67. Change USB external ports for controller.
68. Change CON3602 RJ11+45 part number for ME request.
69. Change R1705 from 100ohm to 330ohm for meet panel spec.
70. Add R2730 for factory recovery AU6371 driver CD.
71. Change R2505,R2506 from 2.7K to 3.3K for HDD-Speaker resonance issue.
72. Change C410,C417,C2101,C2115,C2715,C2716,C3006,C3010 value for TXC report suggest.
73. Del R1816,R1817 for SMT colay request.
74. Add R310 for +VCCA_CPU voltage ripple.
75. Add C2355 2.2uf for SB issue.
76. Unmount R3017,C3001,U3003,C3008,mount R3036,D3003,C3013,R3035,Add R3039 for cost down.
77. Add C3514 for Lan issue.
78. Mount R4459 and unmount Q4405, R4411,C4466 for cost down.
79. Add R4603 and unmount D4601 for cost down.
80. Mount R4708 and unmount Q4801,Q4704,R4709,R4704 for cost down.
81. ADD CE4783 220UF,C4740,C4783 0.1uF for VGA issue.
82. Mount R1611,R1612 from 0 ohm to 33 ohm and mount C1606,C1607 for meet spec.
83. Change CON3201 part number for ME request.
84. Add R2122,R2186 for SB issue.
85. Add C3305 22UF for meet spec.
86. Add C1905,C2727,C4333,C4334,C4335,C4716,Del C4331 for meet spec.
87. Del CE3202 100UF and Add C3209 47UF for ME request.
88. Change CE2601,CE2602 from 27uF to 47uF for better Low frequency response.
89. Add D4401,R3717,Q3709 for meet VGA spec.

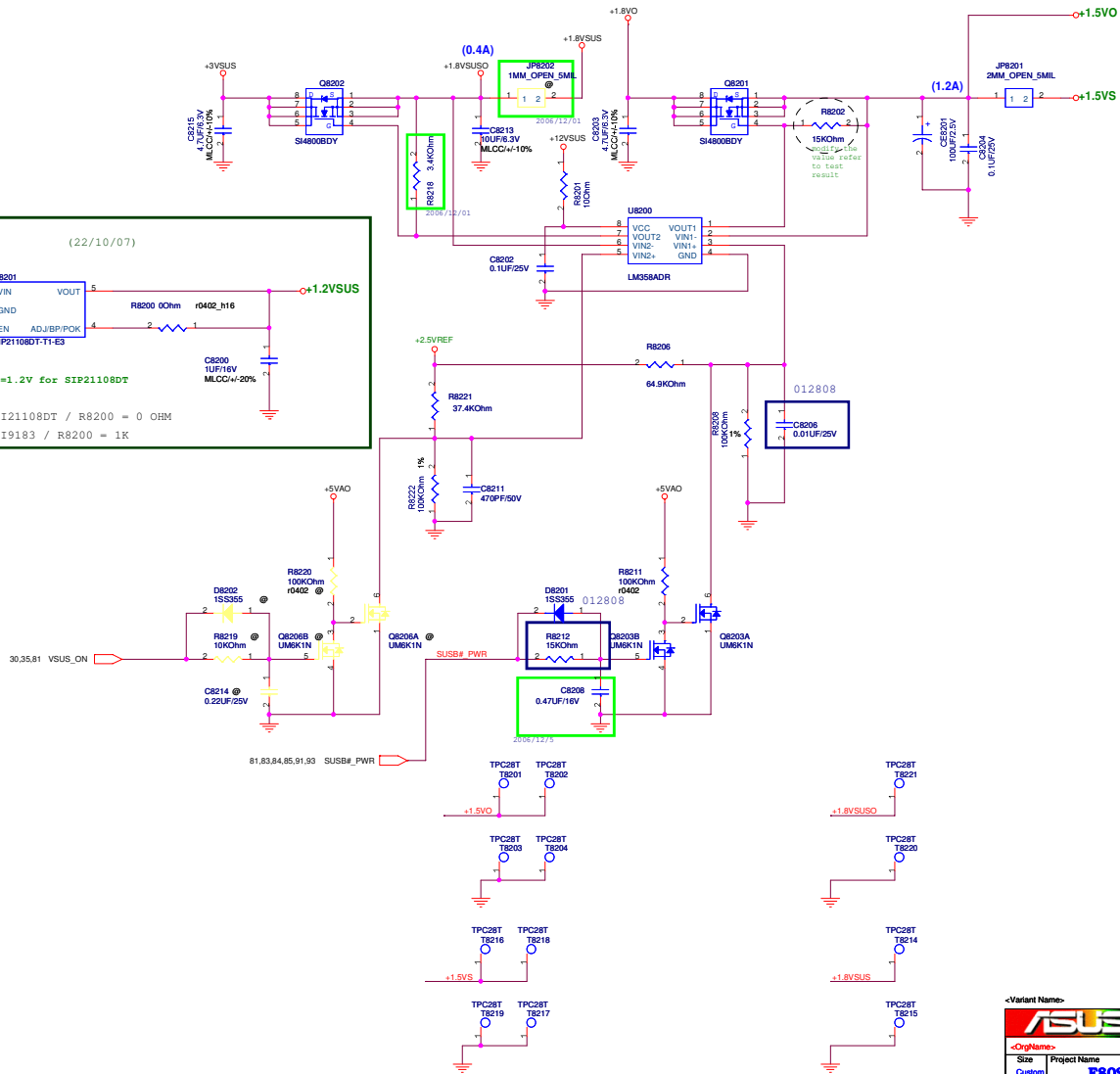
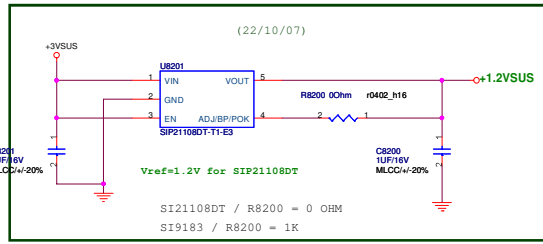
			Title :	
ASUSTek COMPUTER INC. NE1			Engineer:	WM Chen
Size	Project Name			Rev
Custom	F80S			1.1
Date: Wednesday, January 31, 2008			Sheet	58 of 84

		Title : BLANK	
ASUSTek COMPUTER INC. N01		Engineer: WM Chen	
Size Custom	Project Name F80S		Rev 1.1
Date: Wednesday, January 30, 2008		Sheet	60 of 94

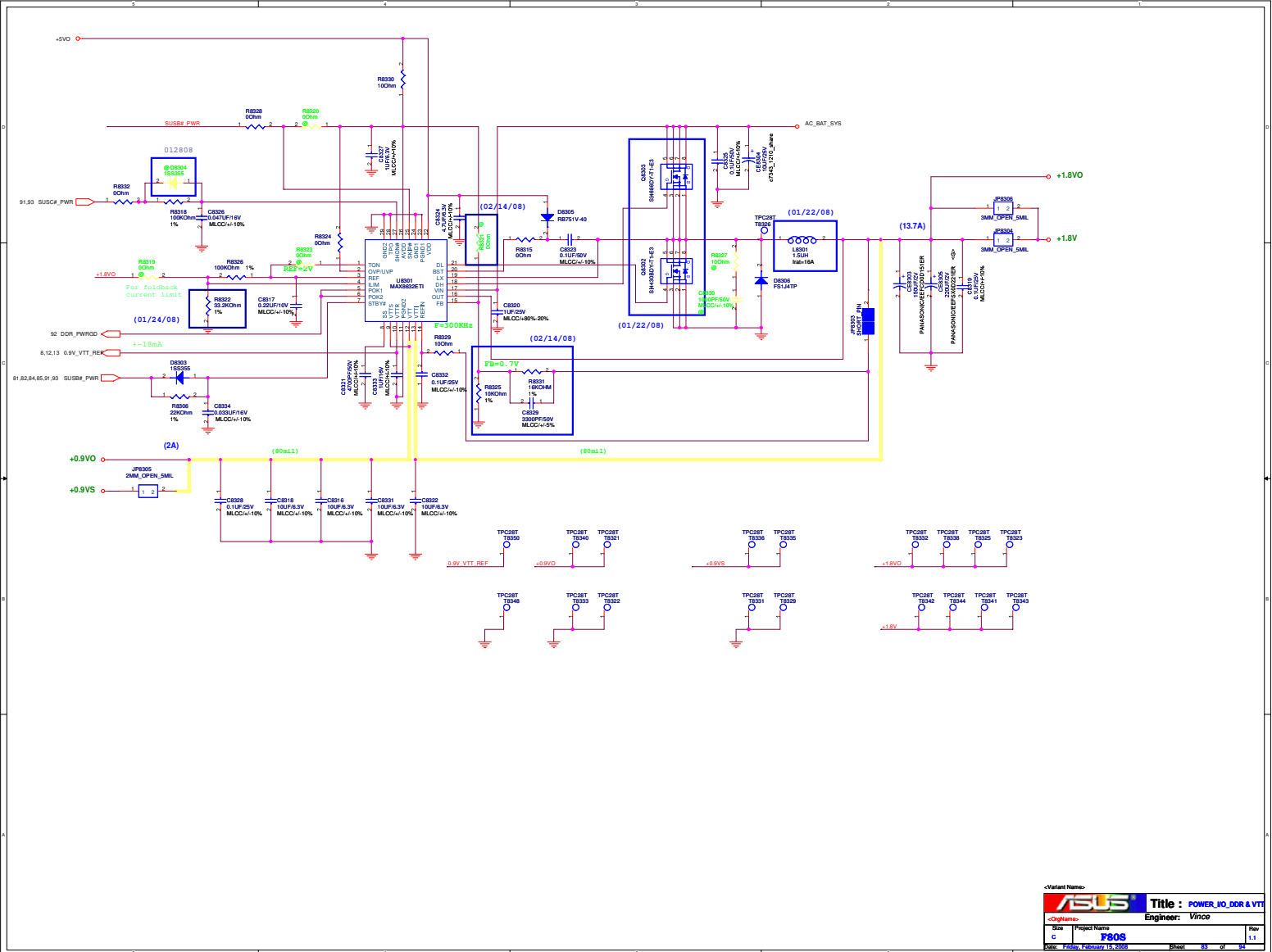


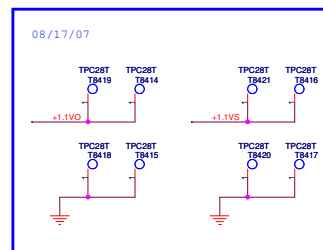
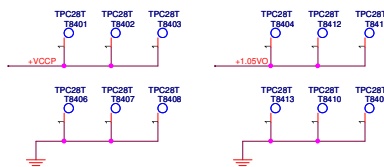
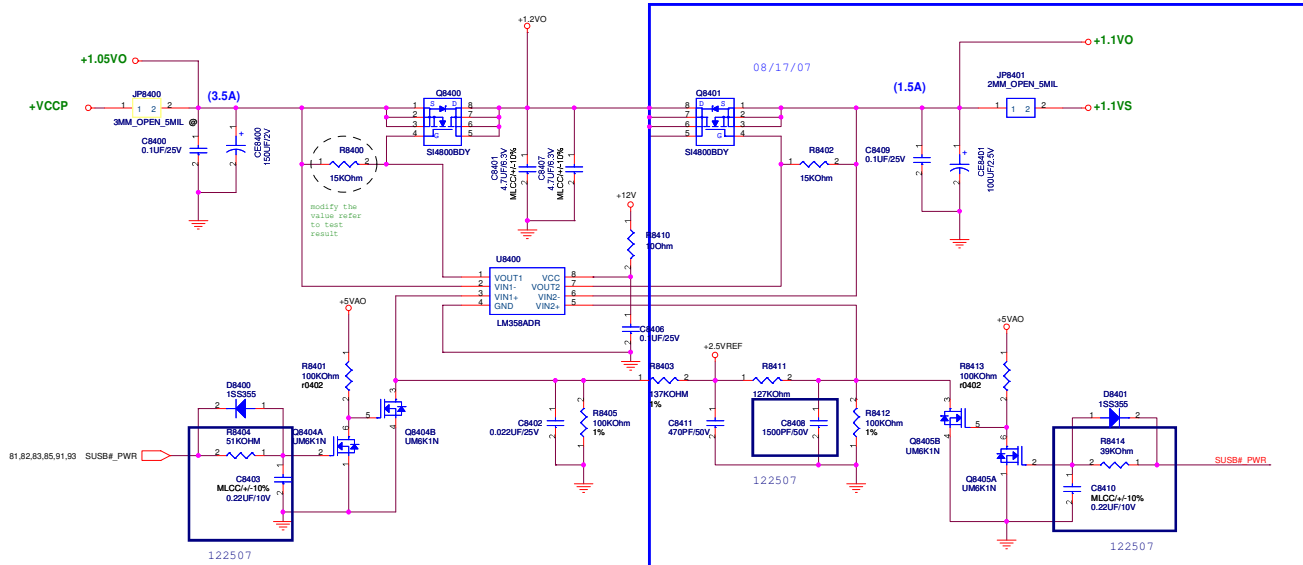






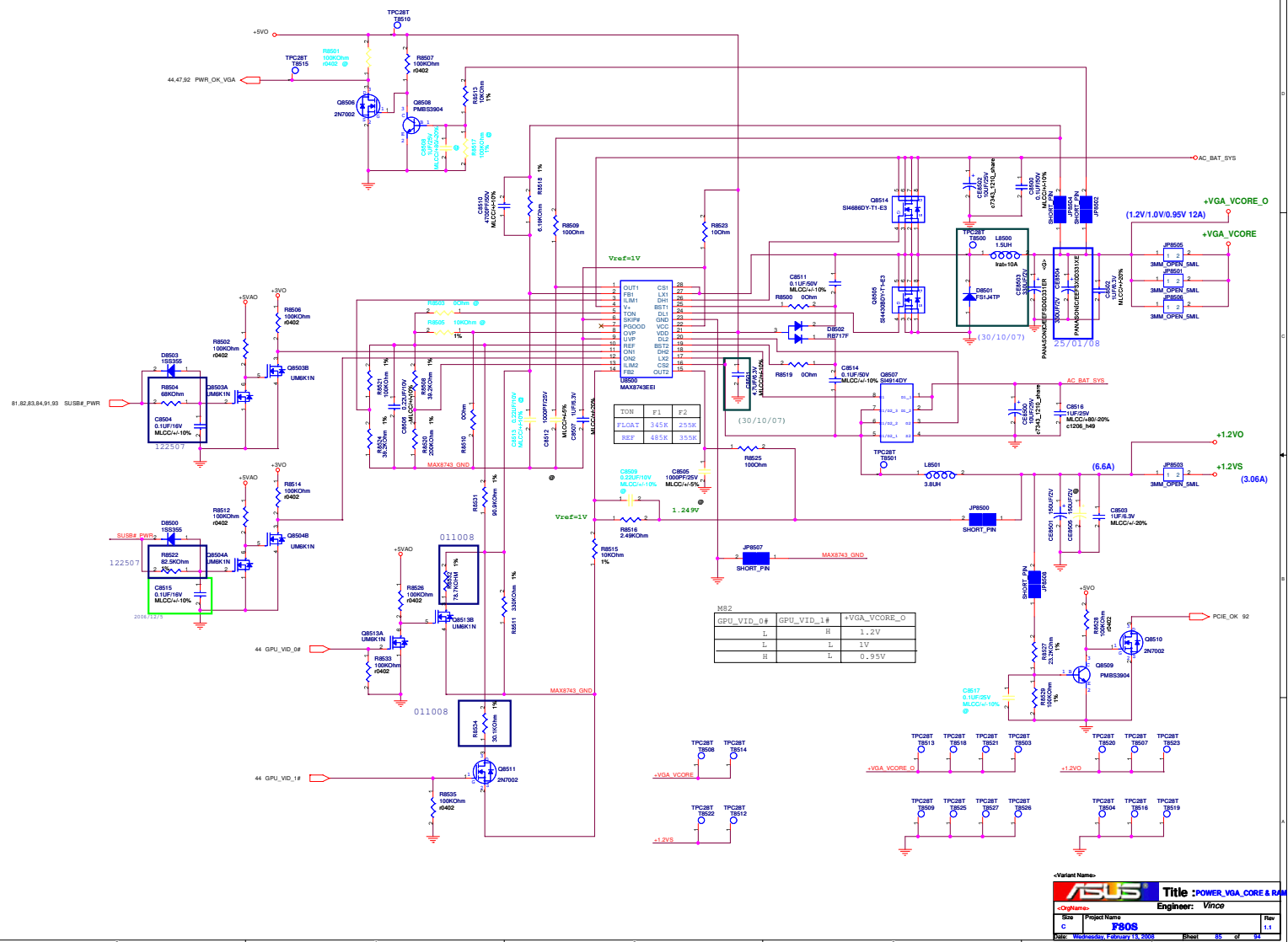
<Variant Name>	
	Title : POWER_IO_1.8VSUS & 1.5VS
Engineer: Vince	
Size Custom	Project Name F80S
Rev 1.1	
Date: Wednesday, February 13, 2008	Sheet 82 of 94





<Variant Name>

ASUS		Title : POWER_IQ_VCCP & 1.1VS	
<OrigName>		Engineer: Vince	
Size	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008		Sheet	84 of 84



D

C

3

A

<Variant Name>



Title : N/A

Engineer: *Vince*

<OrgName>	
Size	P

Size
B

Date:

Project Name	BC
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F80S
Wednesday, January 30, 2013

Rev

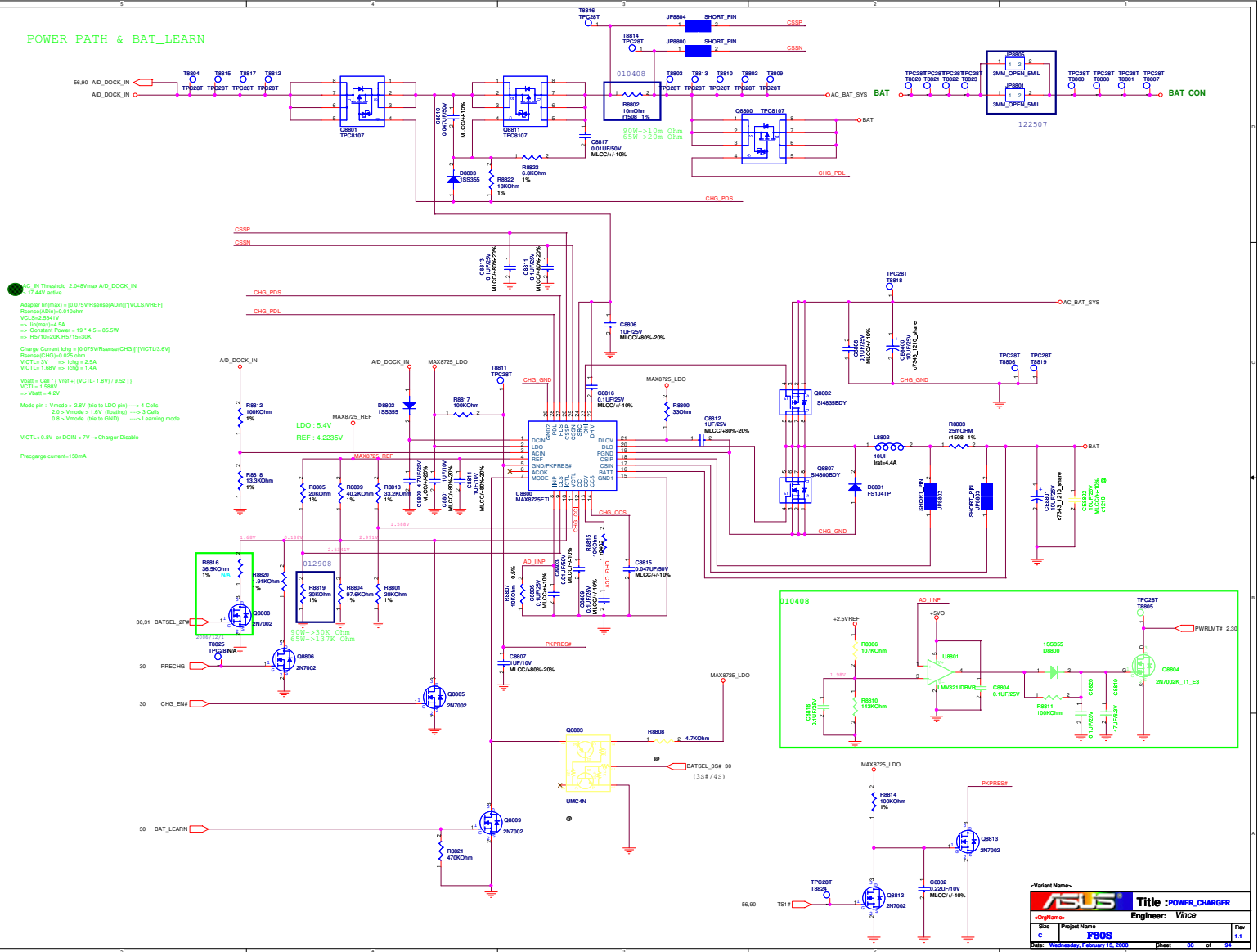
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Date: Wednesday, January 30, 2008

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S	A	S	2	1
D				D
C				C
B				B
A				A
<Variant Name>  Title : N/A <OrigName> Engineer: Vince Size Project Name Rev Custom F80S 1.1 Date: Wednesday, January 30, 2008 Sheet 87 of 84				
S	A	S	2	1

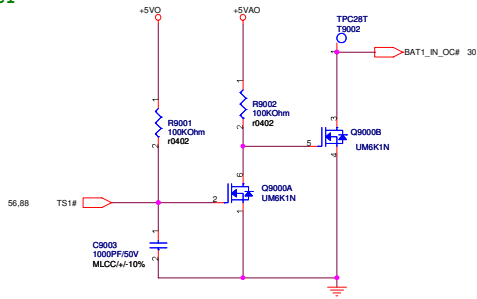
POWER PATH & BAT_LEARN



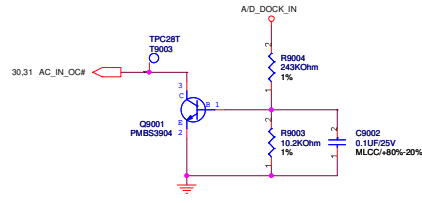
<Variant Name>

		Title : <i>NA</i>	
<OrgName>		Engineer: <i>Vince</i>	
Size <i>Custom</i>	Project Name F80S	Rev 1.1	
Date: <i>Wednesday, January 30, 2008</i>		Sheet <i>69</i> of <i>94</i>	

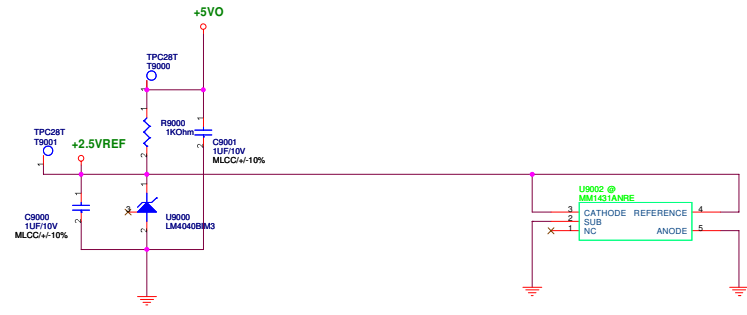
BATTERY IN DETECT



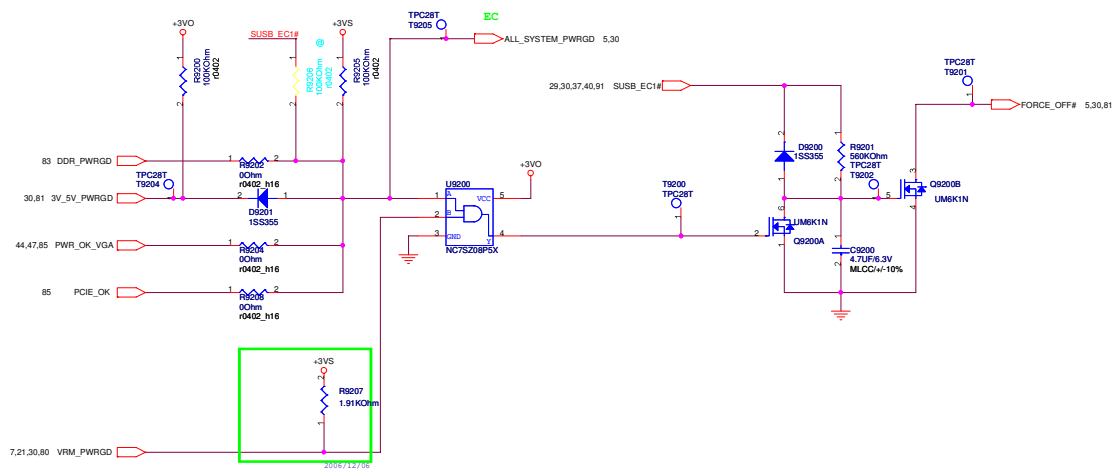
ADAPTER IN DETECT



+2.5VREF

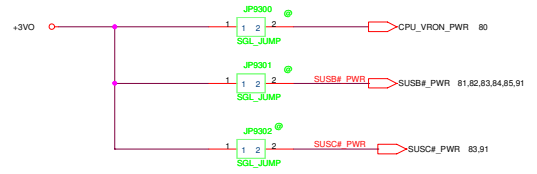


POWER GOOD DETECTOR



AC_BAT_SYS	AC_BAT_SYS	17,80,81,83,85,88
+3VA	+3VA	17,21,30,37,81
+5VA	+5VA	5,81
+5VO	+5VO	81,83,85,88,90,91
+3VO	+3VO	81,85,91,92
+3VSUS	+3VSUS	8,17,19,20,21,22,23,24,26,30,34,35,36,81,82
+5VSUS	+5VSUS	34,81
+3V	+3V	19,27,29,31,36,37,38,40,91
+3VS	+3VS	2,4,5,7,12,13,16,17,18,19,20,21,22,23,25,29,30,32,33,34,37,40,44,80,91,92
+12VSUS	+12VSUS	81,82,91
+12V	+12V	26,27,30,37,84,91
+12VS	+12VS	17,18,37,44,91
+5V	+5V	17,33,37,91
+5VS	+5VS	5,12,16,18,25,26,29,30,32,34,37,38,51,80,91
+1.8VO	+1.8VO	82,83,91
+1.8VSUS	+1.8VSUS	10,21,22,23,82
+1.8V	+1.8V	8,10,12,13,15,37,83
+1.8VS	+1.8VS	6,7,8,10,12,14,20,21,22,23,37,43,44,45,47,51,91
+1.5VS	+1.5VS	3,19,25,29,37,51,82
+VCCP	+VCCP	2,4,5,6,10,21,23,37,43,84
+0.9VS	+0.9VS	15,37,83
BAT	BAT	88
+2.5VREF	+2.5VREF	82,84,88,90
+VOCORE	+VOCORE	3,37,80
+VGA_VCORE	+VGA_VCORE	37,43,47,51,85
+1.2VO	+1.2VO	84,85
+1.2VS	+1.2VS	9,10,37,85
BAT_CON	BAT_CON	56,88

FOR POWER TEST



~Variant Name~		 Title : POWER_SIGNAL	
~OrigName~		Engineer: Vince	
Size	Project Name		Rev
Custom	F80S		1.1
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