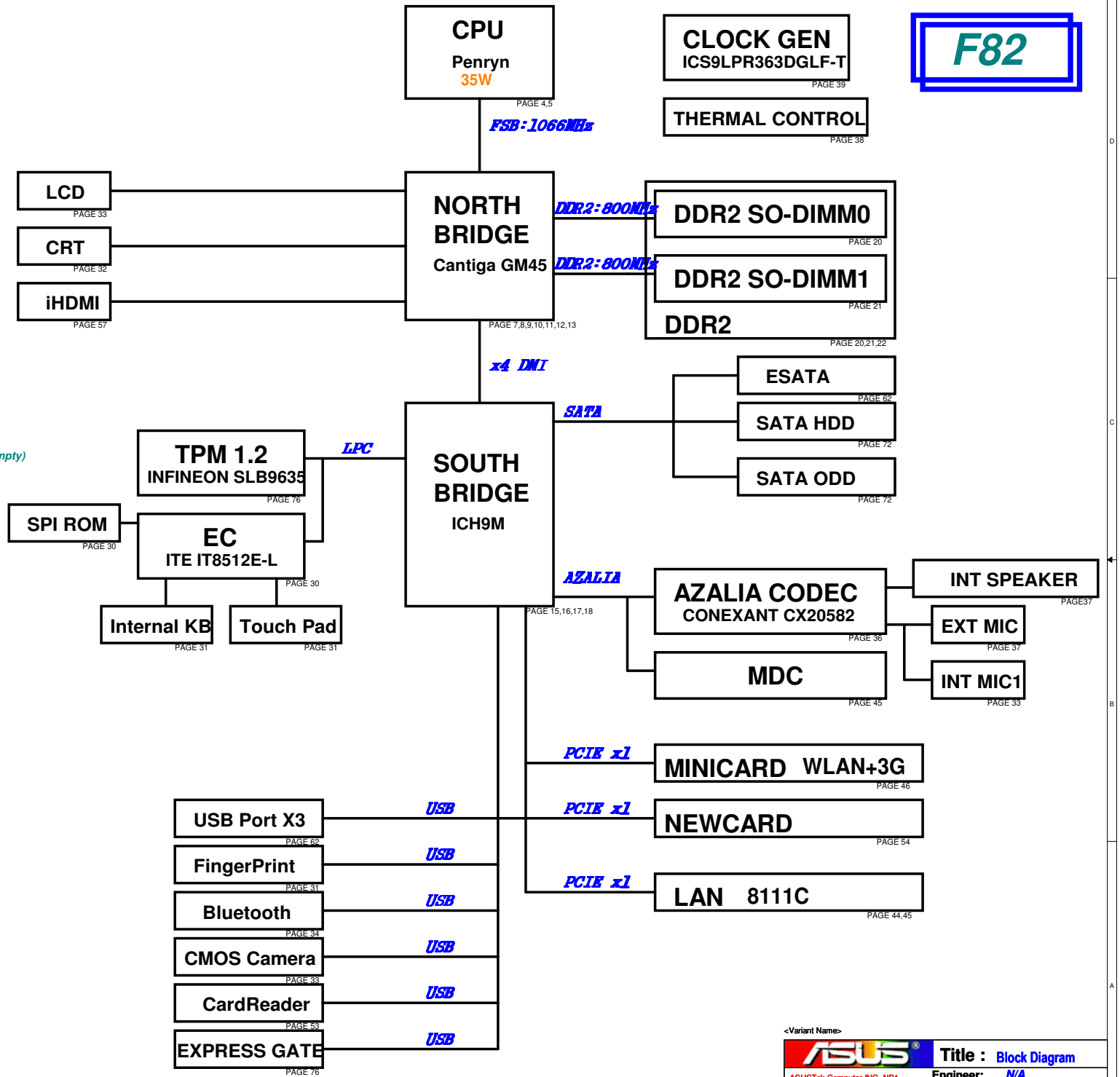


<Variant Name>

ASUSTek Computer INC. NB1

Title : Block Diagram

Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 1 of 93

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PMSYNC#(programmed as GPO)	+3VS
GPIO 01	GPI	EXT PU	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]# EXT PU	+5VS
GPIO 06	GPI	– EXT PU	+3VS
GPIO 07	GPI	– EXT PU	+3VS
GPIO 08	GPI	EXT_SMI# EXT PU	+3VSUS
GPIO 09	Native	WOL_EN	+3VSUS
GPIO 10	GPI	RTLAN_DSM# EXT PU	+3VSUS
GPIO 11	Native	EXT_SCI#(Programmed as GPI)	+3VSUS
GPIO 12	GPO	–	+3VSUS
GPIO 13	GPI		+3VSUS
GPIO 14	GPI	AC_PRESENT EXT PD	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLPVR INT PD*	+3VS
GPIO 17	GPI	WLAN_LED(Programmed as GPO)	+3VS
GPIO 18	GPO	–	+3VS
GPIO 19	GPI	– EXT PU	+3VS
GPIO 20	GPO	– INT PD*	+3VS
GPIO 21	GPI	– EXT PU	+3VS
GPIO 22	GPI	BT_DET# EXT PU	+3VS
GPIO 23	Native	ICH_LDRQ1# INT PU	+3VS
GPIO 24	GPO		+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO		+3VSUS
GPIO 29	Native	NEWCARD_OC#	+3VSUS
GPIO 30	Native	USB_OC#6	+3VSUS
GPIO 31	Native	USB_OC#7	+3VSUS
GPIO 32	GPO	PM_CLKRUN#	+3VS
GPIO 33	GPO	– INT PU*	+3VS
GPIO 34	GPO	–	+3VS
GPIO 35	GPO	–	+3VS
GPIO 36	GPI	– EXT PU	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC01#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	USB_OC8#	+3VSUS
GPIO 45	Native	USB_OC9#	+3VSUS
GPIO 46	Native	WLAN_ON	+3VSUS
GPIO 47	Native	USB_OC11#	+3VSUS
GPIO 48	GPI	EXT PU	+3VS
GPIO 49	GPO	HDCP_EPROM_PROTECT#	+3VS INT PU*
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU*	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU*	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU*	+3VS
GPIO 56	GPI	– EXT PU	+3VSUS
GPIO 57	GPI	– EXT PU	+3VSUS
GPIO 58	GPI	INT PU*	+3VSUS
GPIO 59	Native	USB_OC01#	+3VSUS
GPIO 60	Native	RTLAN_DSM_EN	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED_UP#	
GPA1	GPO	CHG_LED_UP#	
GPA2	GPO	–	
GPA3	–	–	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN0_PWM	
GPA6	GPO	VCORE_CNT1	
GPA7	GPO	VCORE_CNT2	
GPB0	GPO		
GPB1	GPO		
GPB2	GPI		
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI		
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPI	RFON_SW#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_SUSC#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI		
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT		
GPE6	GPI	LID_SW#	
GPE7	GPO		
GPF0	GPI		
GPF1	GPI		
GPF2	GPI	MARATHON#	
GPF3	ALT		
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	LAN_DISABLE	
GPG0	GPO	PM_THERM#	
GPG1	ALT	PM_SUSB#	
GPG2	GPO		
–	–	–	
–	–	–	

EC GPIO	Use As	Signal Name	Power
–	–	–	
GPG6	GPO		
–	–	–	
GPH0	OD	PM_CLKRUN#	
GPH1	GPO	3G_ON#	
GPH2	GPO	3G_LED	
GPH3	GPO		
GPH4	GPO	–	
GPH5	GPO	NUM_LED	
GPH6	GPO	CAP_LED	
–	–	–	
GPI0	GPI	–	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI		
GPI5	GPI		
GPI6	GPI		
GPI7	GPI		
GPJ0	GPO	HDCP_EPROM_PROTECT#	
GPJ1	GPO	PM_PWROK	
GPJ2	GPO	VSET_EC	
GPJ3	GPO	ISET_EC	
GPJ4	GPO		
GPJ5	GPO		

PCIE Device	Bus	PCIE Device	Bus
		3G/TV	PE(T/R)(p/n)4
WLAN	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3	GLAN	PE(T/R)(p/n)6

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
CPU Thermal Sensor(MAX6657)	1001100x (98)

GPIO33 Internal Pull High, Go Low= Flash Descriptor Security will be overriden

INT PU*: PU or PD in special time

<Variant Name>

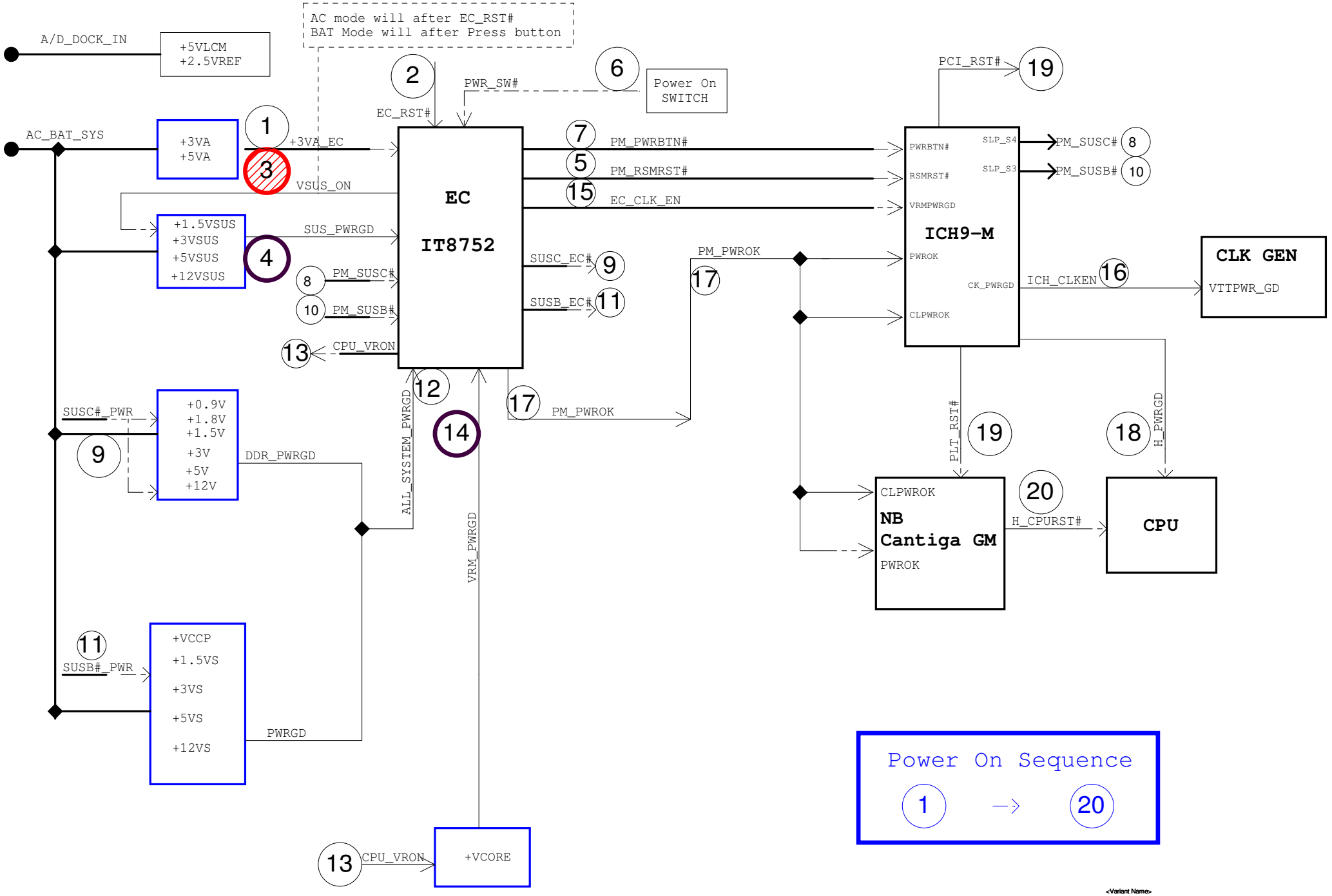
ASUSTek Computer INC. NB1

Title : System Setting

Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 2 of 93



<Variant Name>

ASUSTeK COMPUTER INC

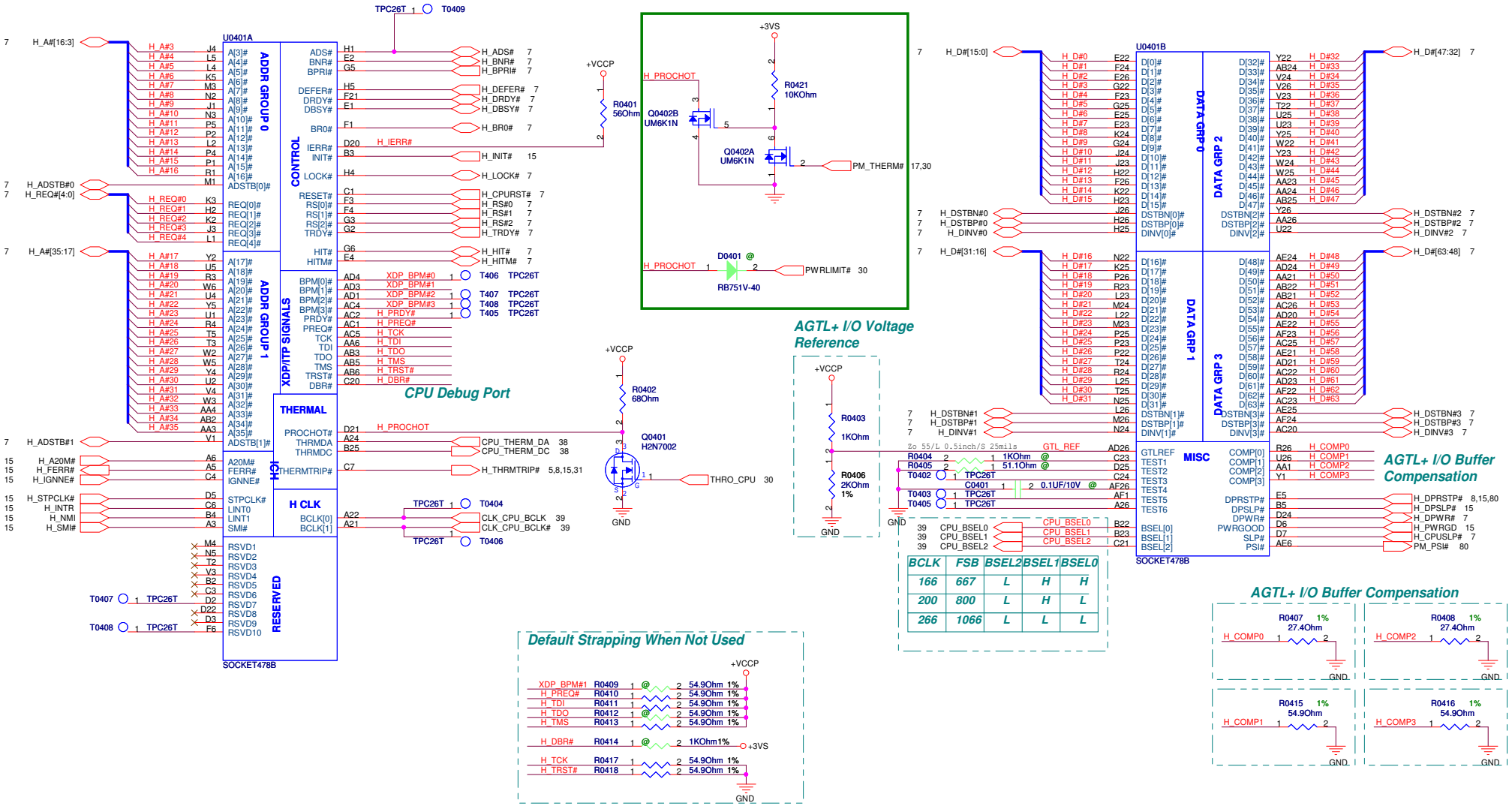
Title : Sequence

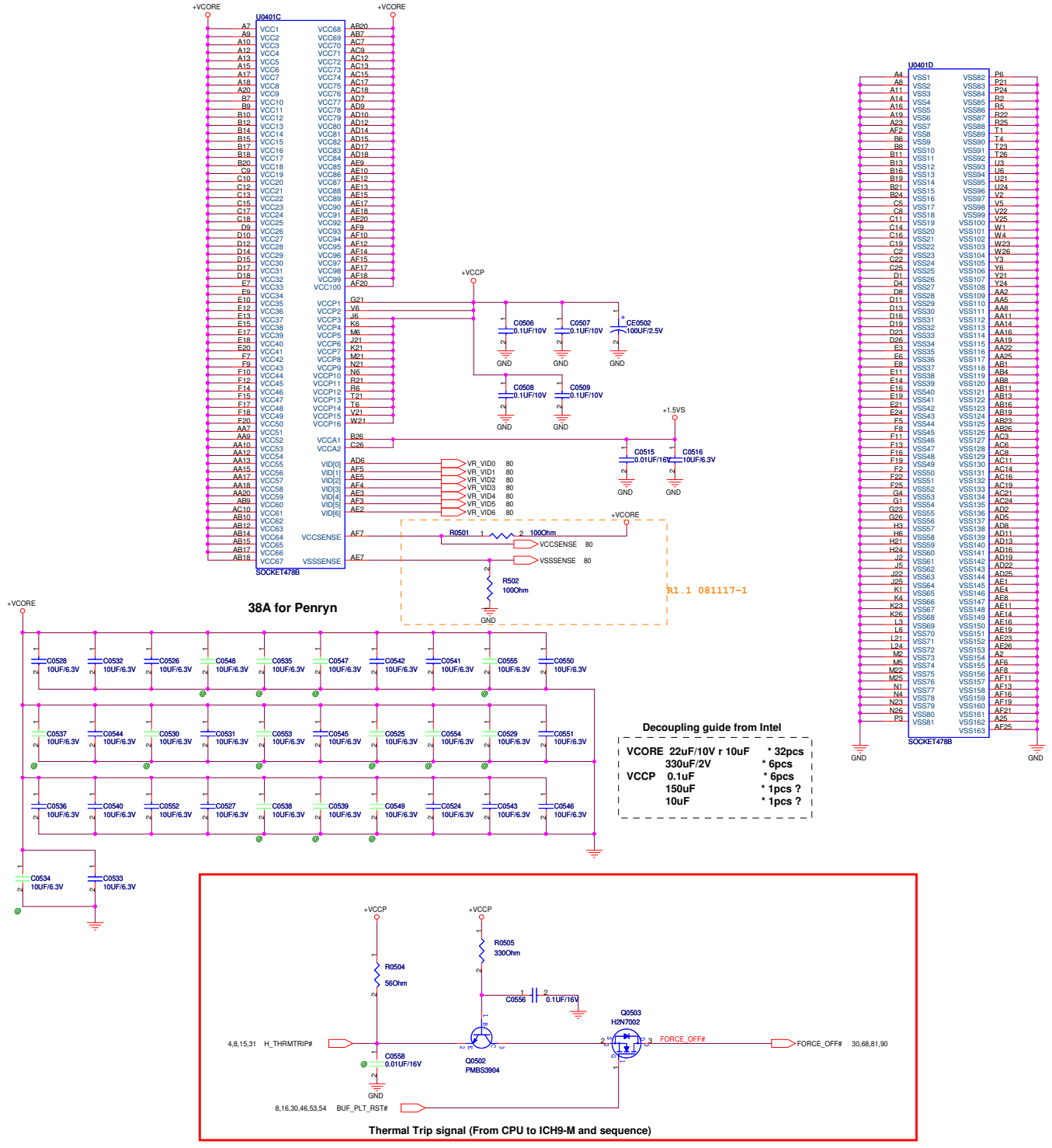
Engineer: N/A

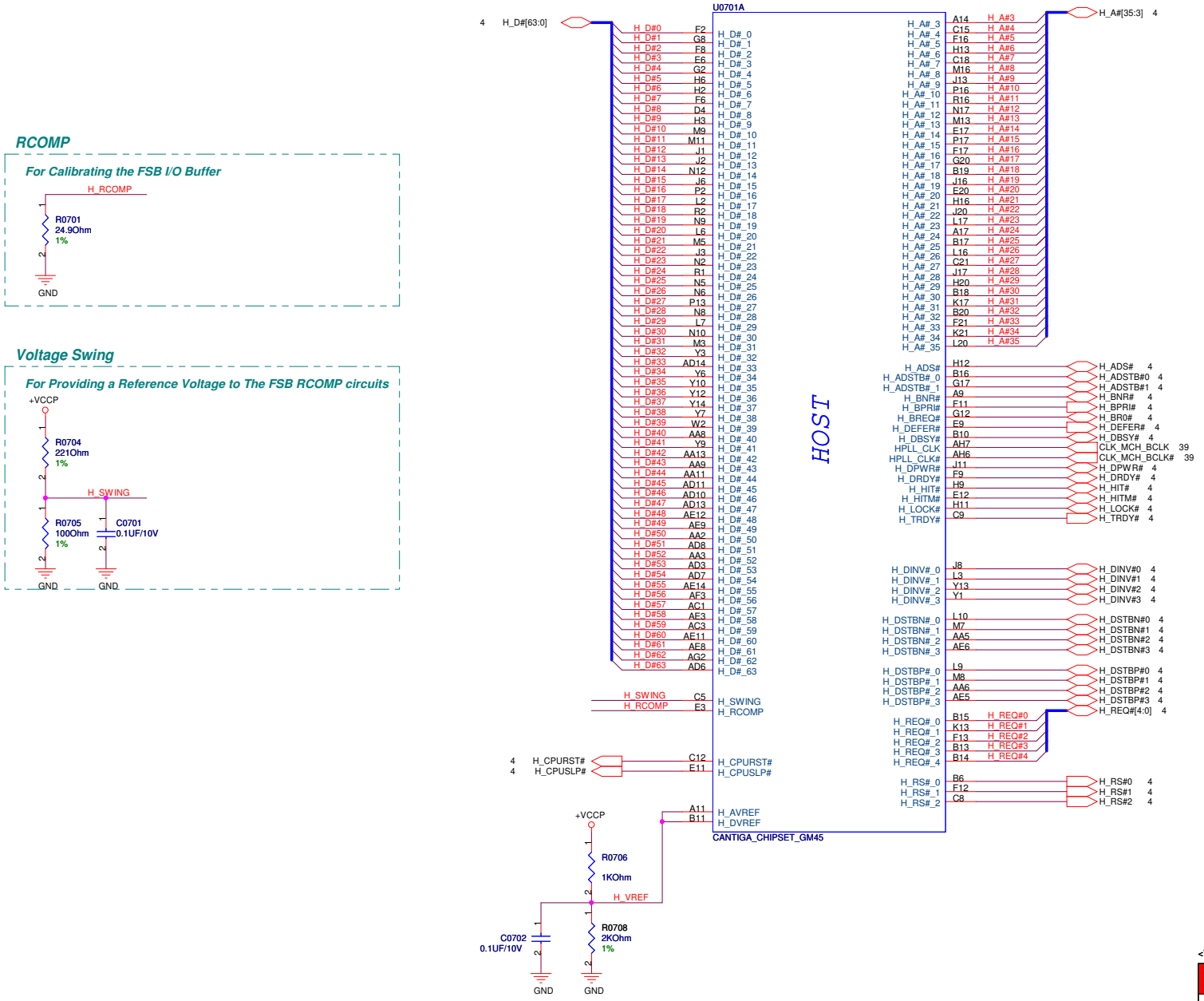
Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 3 of 93

add test point




U0401C
SOCKET478B
U0401D
SOCKET478B
38A for Penryn
R1.1 081117-1
Decoupling guide from Intel
VCORE 22uF/10V r 10uF * 32pcs
330uF/2V * 6pcs
VCCP 0.1uF * 6pcs
150uF * 1pcs ?
10uF * 1pcs ?
Thermal Trip signal (From CPU to ICH9-M and sequence)
Q0503
H2N7002
Q0502
PMBS3904
FORCE_OFF#
H_THRMTRIP#
BUF_PLT_RST#
Title : CPU_Penryn(PWR)
Engineer: N/A
ASUSTeK COMPUTER INC. NB1
Size C
Project Name F82
Rev 1.2
Date: Tuesday, December 30, 2008
Sheet 5 of 93



<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : NB-Cantiga(HOST)

Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 7 of 93

GMCH Strapping

CFG5 : DMI Strap
- 0 = DMI x2
- 1 = DMI x4 (D)

MCH_CFG_5 — R0896 @ — 2.21KOhm 1% — GND

CFG6: iTMP
- 0 = Enabled
- 1 = Disabled (D)

MCH_CFG_6 — R0862 @ — 2.21KOhm 1% — GND

CFG7: ME TLS
- 0 = ME TLS with no confidentiality
- 1 = ME TLS with confidentiality (D)

MCH_CFG_7 — R0861 @ — 2.21KOhm 1% — GND

CFG9 : PCIE Graphic Lane
- 0 = Reverse Lane
- 1 = Normal Operation (D)

MCH_CFG_9 — R0809 @ — 2.21KOhm 1% — GND

CFG10 : PCIE Loopback enable
CFG[13:12] : GMCH Test Mode

CFG10 : PCIE Loopback enable
- 0 = Enabled
- 1 = Disabled (D)

CFG[13:12] : GMCH Test Mode
- 00 = Reserved
- 10 = XOR Mode Enable
- 01 = All Z Mode Enable
- 11 = Normal Operation (D)

MCH_CFG_10 — R0871 @ — 2.21KOhm
MCH_CFG_12 — R0872 @ — 2.21KOhm
MCH_CFG_13 — R0873 @ — 2.21KOhm
— GND

CFG16 : FSB Dynamic ODT
- 0 = Dynamic ODT Disable
- 1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R0811 @ — 2.21KOhm 1% — GND

CFG19 : DMI Lane Reversal
- 0 = Normal Operation (D)
- 1 = Lanes Reversed

MCH_CFG_19 — R0802 @ — +3VS — 4.02KOHM 1%

CFG20 : Concurrent SDVO / PCIe
- 0 = Only one is operational (D)
- 1 = operate simultaneous

MCH_CFG_20 — R0808 @ — +3VS — 4.02KOHM 1%

SDVO_CTRL_DATA : SDVO/iHDMI/DP Interface Present
- 0 = SDVO/iHDMI/DP Disabled (D)
- 1 = SDVO/iHDMI/DP Enabled

HDMI_SCL — R0849 — +3VS — 4.02KOHM 1%

DDPC_CTRL_DATA : SDVO/iHDMI/DP Device Present
- 0 = No SDVO/iHDMI/DP (D)
- 1 = SDVO/iHDMI/DP Present

DDPC_CTRL_DATA — R0850 @ — +3VS — 4.02KOHM 1%

Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

DDPC_CTRL_DATA & SDVO_CTRL_DATA straps should both be high to enable Display Port.

BCLK	FSB	BSEL2	BSEL1	BSEL0
266	1066	L	L	L
166	667	L	H	H
200	800	L	H	L

39 MCH_BSEL0 — T25 CFG_0
39 MCH_BSEL1 — R25 CFG_1
39 MCH_BSEL2 — P25 CFG_2
P20 CFG_3
P24 CFG_4
MCH_CFG_5 — C25 CFG_5
MCH_CFG_6 — N24 CFG_6
MCH_CFG_7 — M24 CFG_7
E21 CFG_8
MCH_CFG_9 — C23 CFG_9
MCH_CFG_10 — C24 CFG_10
N21 CFG_11
MCH_CFG_12 — P21 CFG_12
MCH_CFG_13 — T21 CFG_13
P20 CFG_14
M20 CFG_15
MCH_CFG_16 — L21 CFG_16
H21 CFG_17
P29 CFG_18
MCH_CFG_19 — R28 CFG_19
MCH_CFG_20 — T28 CFG_20

R1.1 081114-1

21 PM_EXTTS#_1 — PM_EXTTS# 1

T0801 TPC26T

17 PM_SYNC# — R29 PM_SYNC#
4,15,80 H_DPRSTP# — B7 PM_DPRSTP#
+3VS — R0815 2 10KOhm 1 PM_EXTTS# 0 — N33 PM_EXT_TS#_0
R0816 2 10KOhm r0402 PM_EXTTS# 1 — P32 PM_EXT_TS#_1
17,30 PM_PWROK — PM_PWROK — AT40 PWROK
5,16,30,46,53,54 BUF_PLT_RST# — R0817 1 2 100Ohm RST_IN_MCH# — AT11 RSTIN#
4,5,15,31 H_THRMTRIP# — T20 THERMTRIP#
17,80 PM_DPRSLPVR — R32 DPRSLPVR

+1.8V — R0899 20Ohm — SM_RCOMP# — SM_RCOMP — R0898 20Ohm — GND

+VCCP — R0812 1KOhm — MCH_CLVREF — R0818 499Ohm 1% — C0801 0.1UF/10V — GND GND

+1.8V — R0821 1KOhm — SM_RCOMP_VOH — R0823 3.01KOHM 1% — C0802 1UF/10V — C0803 0.01UF/16V — GND GND
SM_RCOMP_VOL — R0827 1KOhm — C0805 1UF/10V — C0806 0.01UF/16V — GND GND GND

C0807 0.1UF/10V — GND — R0830 0Ohm @ — GND

U0701B

M36 RSVD1
N36 RSVD2
R33 RSVD3
T33 RSVD4
AH9 RSVD5
AH10 RSVD6
AH12 RSVD7
AH13 RSVD8
K12 RSVD9
AL34 RSVD10
AK34 RSVD11
AN35 RSVD12
AM35 RSVD13
T24 RSVD14
B31 RSVD15
AJ6 RSVD16
M1 RSVD17
AY21 RSVD20
A47 RSVD21
BG23 RSVD22
BF23 RSVD23
BH18 RSVD24
BF18 RSVD25

RSVD

SA_CK_0 AP24 — M_CLK_DDR0 20
SA_CK_1 AT21 — M_CLK_DDR1 20
SB_CK_0 AV24 — M_CLK_DDR2 21
SB_CK_1 AU20 — M_CLK_DDR3 21
SA_CK#_0 AR24 — M_CLK_DDR#0 20
SA_CK#_1 AR21 — M_CLK_DDR#1 20
SB_CK#_0 AU24 — M_CLK_DDR#2 21
SB_CK#_1 AV20 — M_CLK_DDR#3 21
SA_CKE_0 BC28 — M_CKE0 20,22
SA_CKE_1 AY28 — M_CKE1 20,22
SB_CKE_0 AY36 — M_CKE2 21,22
SB_CKE_1 BB36 — M_CKE3 21,22
SA_CS#_0 BA17 — M_CS#0 20,22
SA_CS#_1 AY16 — M_CS#1 20,22
SB_CS#_0 AV16 — M_CS#2 21,22
SB_CS#_1 AR13 — M_CS#3 21,22
SA_ODT_0 BD17 — M_ODT0 20,22
SA_ODT_1 AY17 — M_ODT1 20,22
SB_ODT_0 BF15 — M_ODT2 21,22
SB_ODT_1 AY13 — M_ODT3 21,22

DDR CONTROL/COMPENSATION

SM_RCOMP BG22 — SM_RCOMP — R0803 1 1% 2 80.6Ohm
SM_RCOMP# BH21 — SM_RCOMP# — R0804 1 1% 2 80.6Ohm — GND
SM_RCOMP_VOH BF28 — SM_RCOMP_VOH
SM_RCOMP_VOL BH28 — SM_RCOMP_VOL
SM_VREF AV42 — M_VREF_GMCH — M_VREF_MCH 20,21,22
SM_PWROK AD36
SM_REXT BF17 — R0897 1 499Ohm 2 — GND
SM_DRAMRST# BC361 — TPC26T T0802

+1.8V

DPLL_REF_CLK B38 — CLK_MCH_REF 39
DPLL_REF_CLK# A38 — CLK_MCH_REF# 39
DPLL_REF_SSCLK F41 — CLK_MCH_SSCLK 39
DPLL_REF_SSCLK# F41 — CLK_MCH_SSCLK# 39
PEG_CLK F43 — CLK_MCH_3GPLL 39
PEG_CLK# E43 — CLK_MCH_3GPLL# 39

CLK

DMI_RXN_0 AE41 — DMI_TXN0
DMI_RXN_1 AE37 — DMI_TXN1
DMI_RXN_2 AE47 — DMI_TXN2
DMI_RXN_3 AH39 — DMI_TXN3 — DMI_TXN[0:3] 16
DMI_RXP_0 AE40 — DMI_TXP0
DMI_RXP_1 AE38 — DMI_TXP1
DMI_RXP_2 AE48 — DMI_TXP2
DMI_RXP_3 AH40 — DMI_TXP3 — DMI_TXP[0:3] 16
DMI_TXN_0 AE35 — DMI_RXN0
DMI_TXN_1 AE43 — DMI_RXN1
DMI_TXN_2 AE46 — DMI_RXN2
DMI_TXN_3 AH42 — DMI_RXN3 — DMI_RXN[0:3] 16
DMI_TXP_0 AD35 — DMI_RXP0
DMI_TXP_1 AE44 — DMI_RXP1
DMI_TXP_2 AF46 — DMI_RXP2
DMI_TXP_3 AH43 — DMI_RXP3 — DMI_RXP[0:3] 16

DMI

GFX_VID_0 B33 — T0803 TPC26T
GFX_VID_1 B32 — T0804 TPC26T
GFX_VID_2 G33 — T0805 TPC26T
GFX_VID_3 F33 — T0806 TPC26T
GFX_VID_4 E33 — T0807 TPC26T
GFX_VR_EN C34 — T0808 TPC26T

GRAPHICS VID

CL_CLK AH37 — CL_CLK0 17
CL_DATA AH36 — CL_DATA0 17
CL_PWROK AN36 — PM_PWROK
CL_RST# AJ35 — CL_RST#0 17
CL_VREF AH34 — MCH_CLVREF

ME

DDPC_CTRLCLK N28 — T0811 TPC26T INT PD
DDPC_CTRLDATA M28 — DDPC_CTRL_DATA
SDVO_CTRLCLK G36 — HDMI_SCL — HDMI_SCL 57
SDVO_CTRLDATA E36 — HDMI_SDA — HDMI_SDA 57
CLKREQ# K36 — CLK_MCH_OE#
ICH_SYNC# H36 — MCH_ICH_SYNC# 17
TSATN# B12 — R0829 2 — +VCCP — 56Ohm

+3VS — R0813 10KOhm

MISC

HDA_BCLK B28 — ACZ_BCLK_NB_R 56
HDA_RST# B30 — ACZ_RST#_NB_R 56
HDA_SDI B29 — JHDMI 2 — ACZ_SDIN2_R 56
HDA_SDO C29 — R0874 33Ohm — ACZ_SDOUT_NB_R 56
HDA_SYNC A28 — ACZ_SYNC_NB_R 56

HDA

For HDMI

BG48 NC_1
BF48 NC_2
BD48 NC_3
BC48 NC_4
BH47 NC_5
BG47 NC_6
BF47 NC_7
BH46 NC_8
BF46 NC_9
BG45 NC_10
BH44 NC_11
BH43 NC_12
BH6 NC_13
BH5 NC_14
BG4 NC_15
BH3 NC_16
BF3 NC_17
BH2 NC_18
BG2 NC_19
BE2 NC_20
BG1 NC_21
BF1 NC_22
BD1 NC_23
BC1 NC_24
F1 NC_25

NC

CANTIGA_CHIPSET_GM45

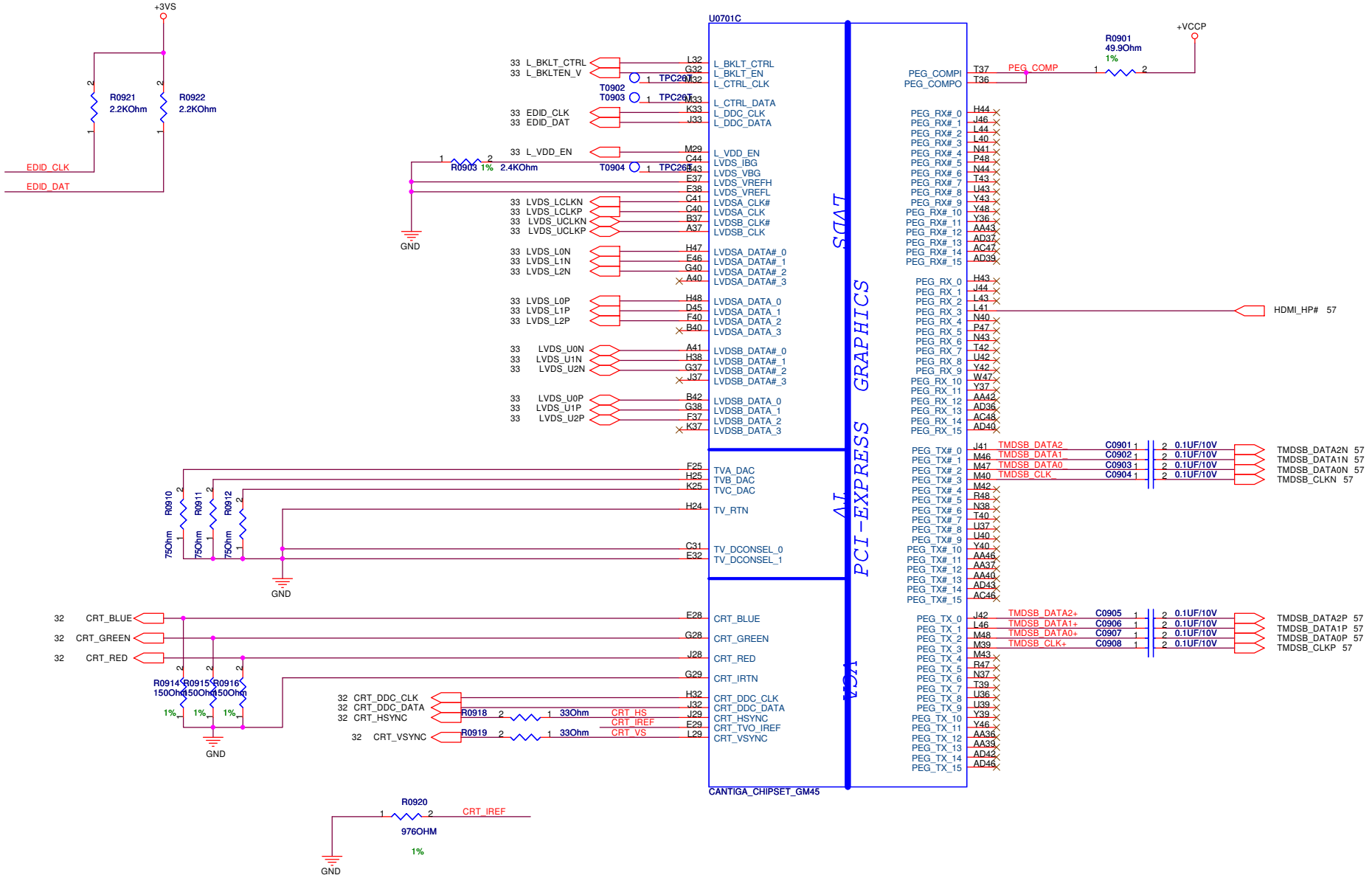
<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : NB-Cantiga(DMI & CFG)
Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 8 of 93



<Variant Name>

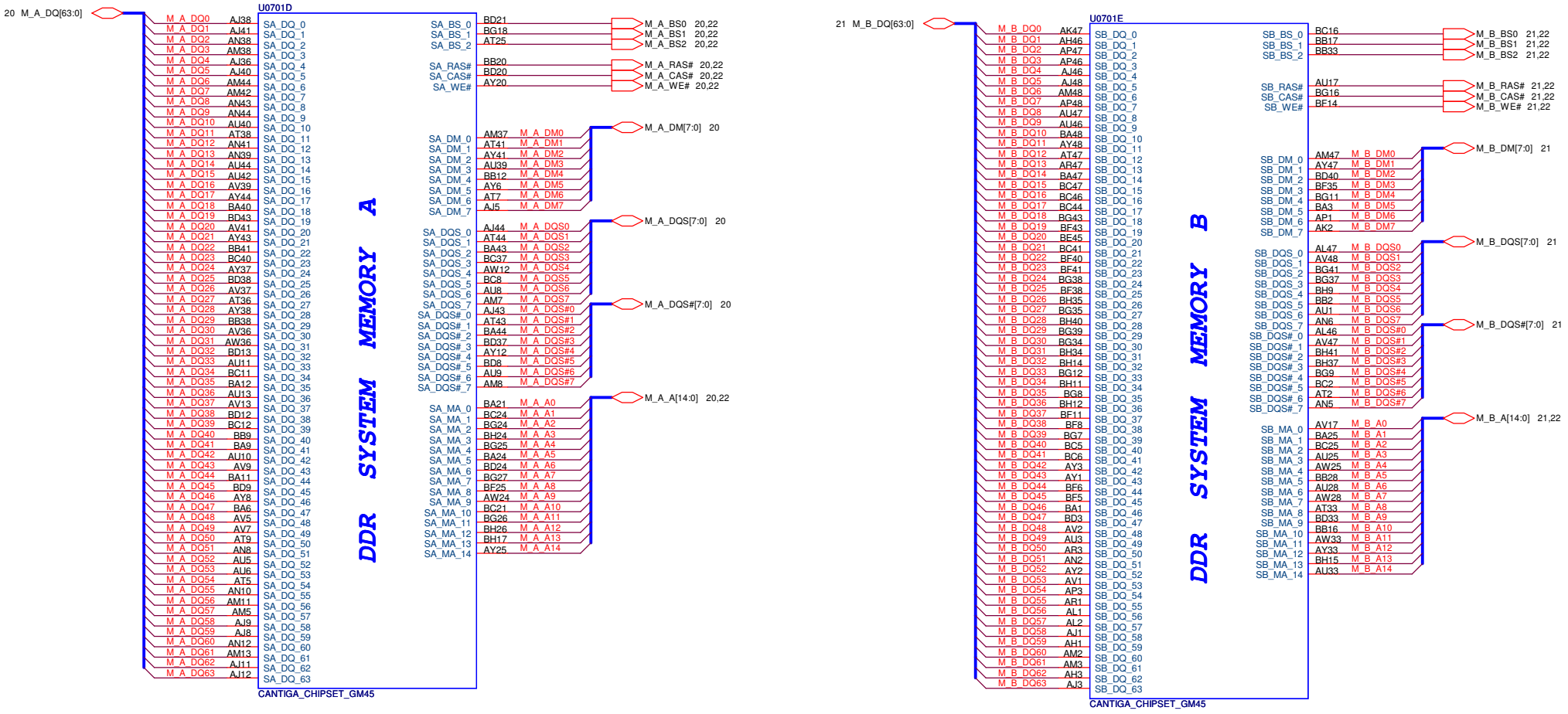
ASUSTeK COMPUTER INC. NB1

Title : NB_Cantiga(GRAPHIC)

Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 9 of 93



<Variant Name>

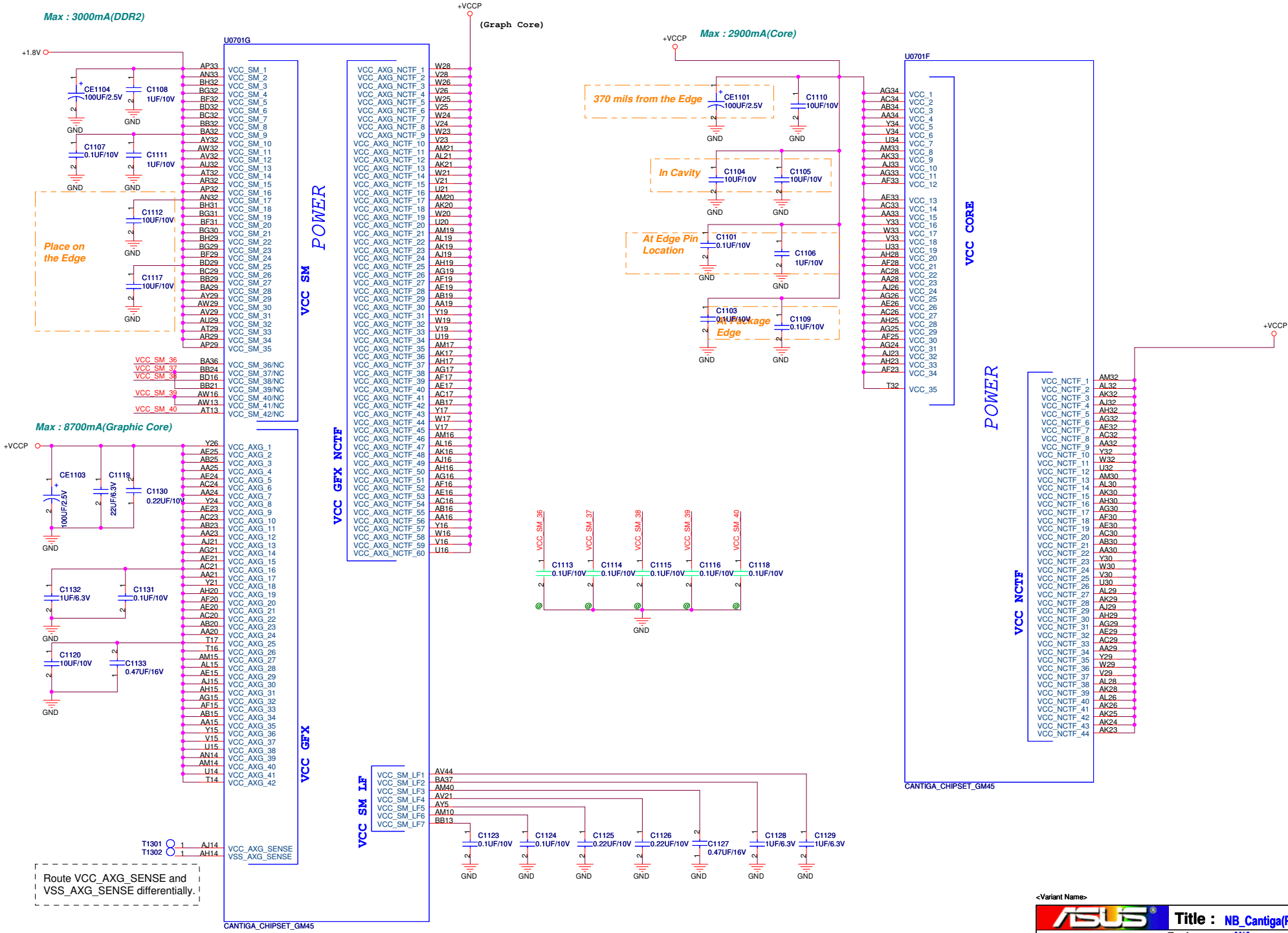
ASUSTeK COMPUTER INC. NB1

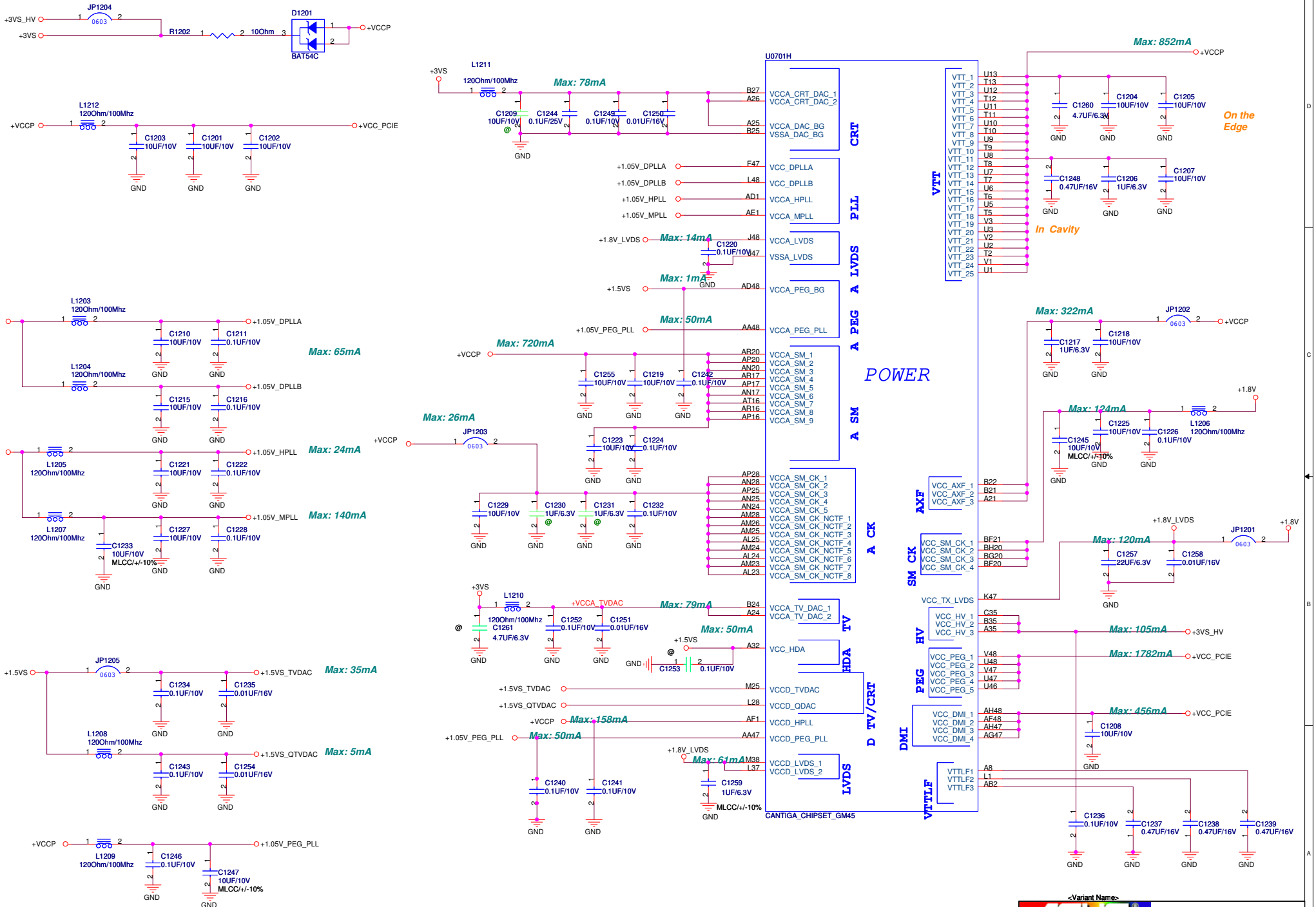
Title : NB-Cantiga(DDR2)

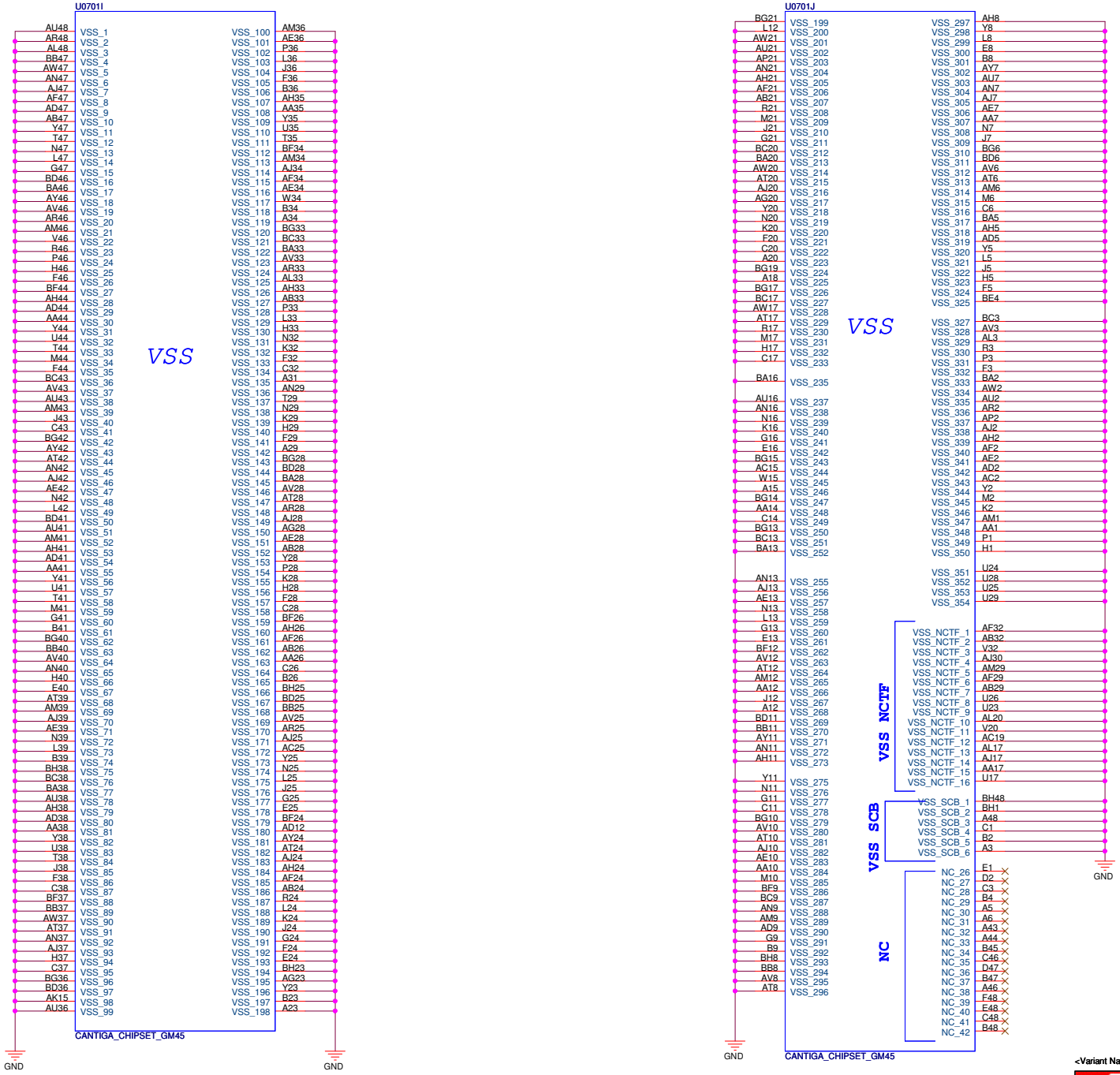
Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 10 of 93

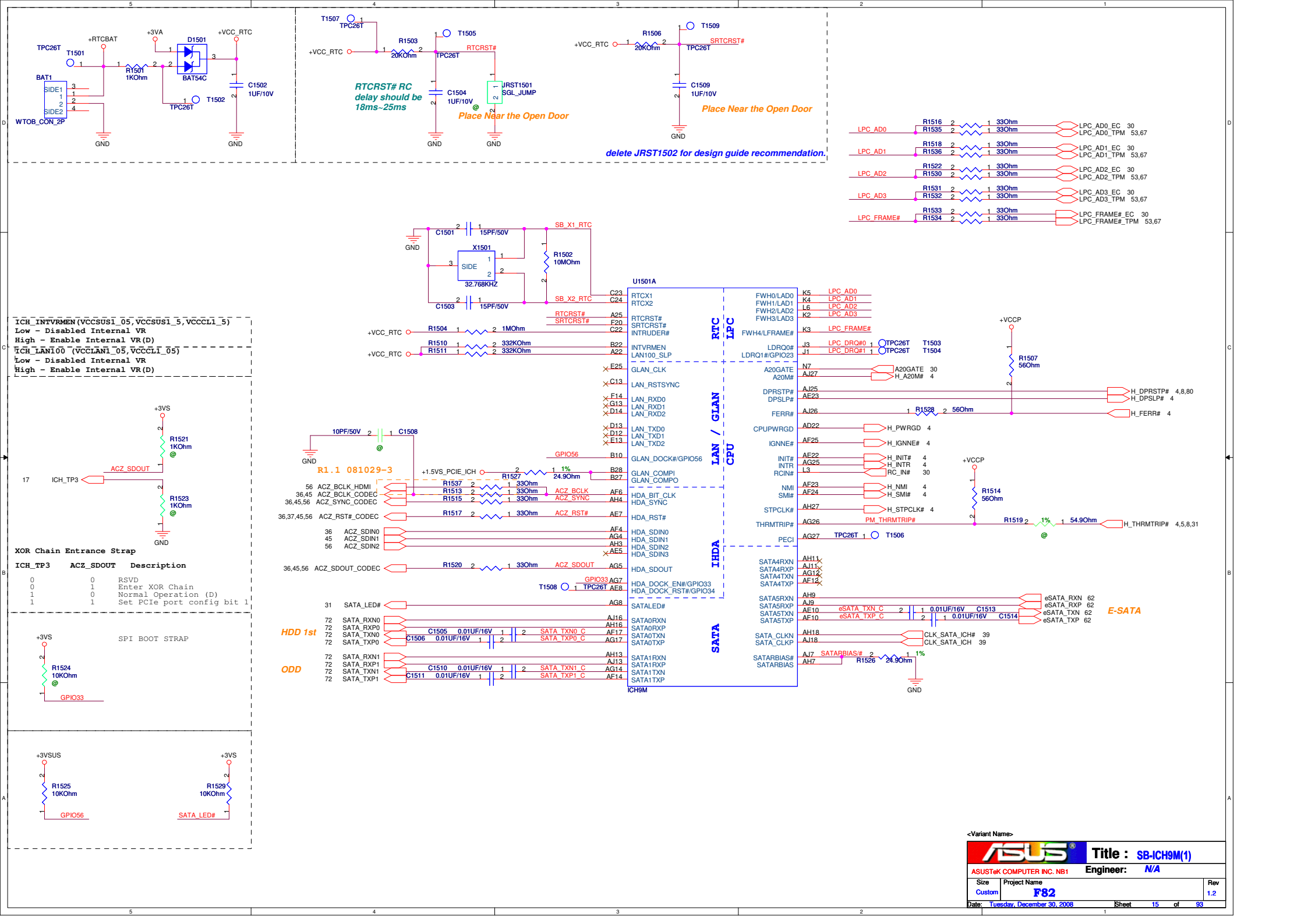

Max : 3000mA(DDR2)
Max : 8700mA(Graphic Core)
Max : 2900mA(Core)
(Graph Core)
U0701G
U0701F
+1.8V
+VCCP
GND
Place on the Edge
370 mils from the Edge
In Cavity
At Edge Pin Location
At Package Edge
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC CORE
VCC NCTF
POWER
CANTIGA_CHIPSET_GM45
Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially.
<Variant Name>
Title : NB_Cantiga(PWR)
ASUSTeK COMPUTER INC. NB1
Engineer: N/A
Size: Custom
Project Name: F82
Rev: 1.2
Date: Tuesday, December 30, 2008
Sheet 11 of 93

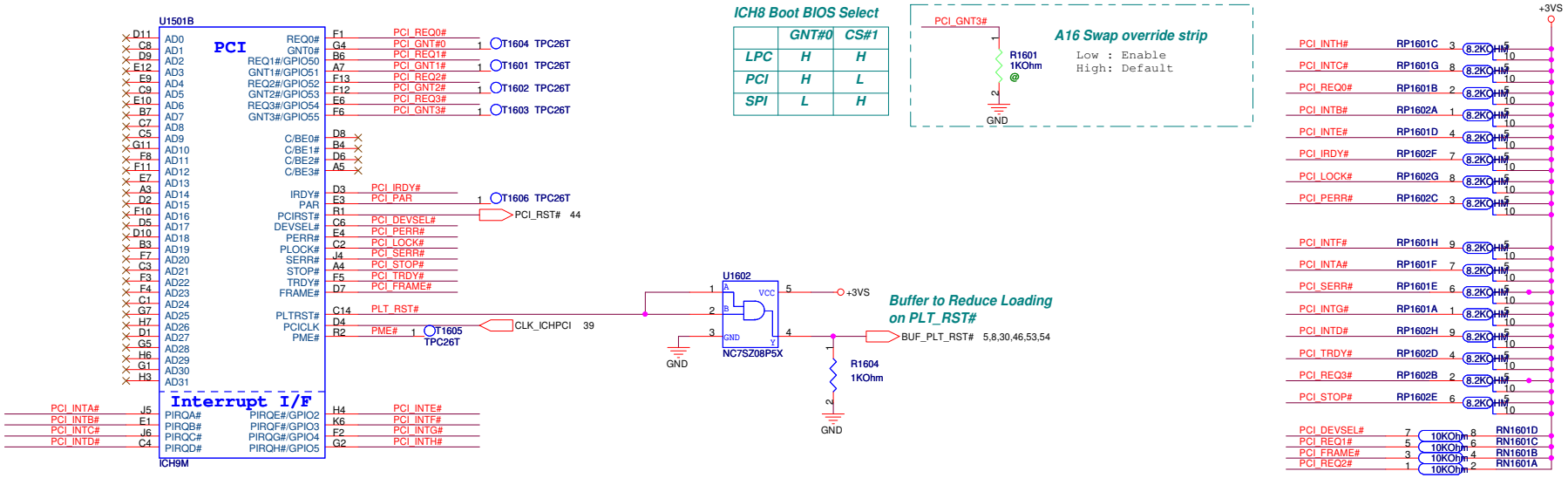

JP1204
+3VS_HV
+3VS
R1202
10Ohm
D1201
BAT54C
+VCCP
L1212
120Ohm/100Mhz
+VCCP
+VCC_PCIE
C1203 10UF/10V
C1201 10UF/10V
C1202 10UF/10V
GND
L1203
120Ohm/100Mhz
+1.05V_DPLLA
C1210 10UF/10V
C1211 0.1UF/10V
Max: 65mA
L1204
120Ohm/100Mhz
+1.05V_DPLLB
C1215 10UF/10V
C1216 0.1UF/10V
L1205
120Ohm/100Mhz
+1.05V_HPLL
C1221 10UF/10V
C1222 0.1UF/10V
Max: 24mA
L1207
120Ohm/100Mhz
+1.05V_MPLL
C1233 10UF/10V MLCC/+/-10%
C1227 10UF/10V
C1228 0.1UF/10V
Max: 140mA
JP1205
+1.5VS
+1.5VS_TVDAC
C1234 0.1UF/10V
C1235 0.01UF/16V
Max: 35mA
L1208
120Ohm/100Mhz
+1.5VS_QTVDAC
C1243 0.1UF/10V
C1254 0.01UF/16V
Max: 5mA
L1209
120Ohm/100Mhz
+1.05V_PEG_PLL
C1246 0.1UF/10V
C1247 10UF/10V MLCC/+/-10%
L1211
120Ohm/100Mhz
+3VS
Max: 78mA
C1209 10UF/10V
C1244 0.1UF/25V
C1249 0.1UF/10V
C1250 0.01UF/16V
U0701H
CANTIGA_CHIPSET_GM45
B27 VCCA_CRT_DAC_1
A26 VCCA_CRT_DAC_2
A25 VCCA_DAC_BG
B25 VSSA_DAC_BG
CRT
+1.05V_DPLLA F47 VCC_DPLLA
+1.05V_DPLLB L48 VCC_DPLLB
+1.05V_HPLL AD1 VCCA_HPLL
+1.05V_MPLL AE1 VCCA_MPLL
PLL
+1.8V_LVDS
Max: 14mA
C1220 0.1UF/10V
J48 VCCA_LVDS
J47 VSSA_LVDS
A LVDS
+1.5VS
Max: 1mA
AD48 VCCA_PEG_BG
A PEG
+1.05V_PEG_PLL
Max: 50mA
AA48 VCCA_PEG_PLL
+VCCP
Max: 720mA
C1255 10UF/10V
C1219 10UF/10V
C1242 0.1UF/10V
AR20 VCCA_SM_1
AP20 VCCA_SM_2
AN20 VCCA_SM_3
AR17 VCCA_SM_4
AP17 VCCA_SM_5
AN17 VCCA_SM_6
AT16 VCCA_SM_7
AR16 VCCA_SM_8
AP16 VCCA_SM_9
A SM
Max: 26mA
JP1203
+VCCP
C1223 10UF/10V
C1224 0.1UF/10V
AP28 VCCA_SM_CK_1
AN28 VCCA_SM_CK_2
AP25 VCCA_SM_CK_3
AN25 VCCA_SM_CK_4
AN24 VCCA_SM_CK_5
AM28 VCCA_SM_CK_NCTF_1
AM26 VCCA_SM_CK_NCTF_2
AM25 VCCA_SM_CK_NCTF_3
AL25 VCCA_SM_CK_NCTF_4
AM24 VCCA_SM_CK_NCTF_5
AL24 VCCA_SM_CK_NCTF_6
AM23 VCCA_SM_CK_NCTF_7
AL23 VCCA_SM_CK_NCTF_8
A CK
C1229 10UF/10V
C1230 1UF/6.3V
C1231 1UF/6.3V
C1232 0.1UF/10V
+3VS
L1210
120Ohm/100Mhz
C1261 4.7UF/6.3V
+VCCA_TVDAC
C1252 0.1UF/10V
C1251 0.01UF/16V
Max: 79mA
B24 VCCA_TV_DAC_1
A24 VCCA_TV_DAC_2
TV
Max: 50mA
+1.5VS
C1253 0.1UF/10V
A32 VCC_HDA
HDA
+1.5VS_TVDAC M25 VCCD_TVDAC
+1.5VS_QTVDAC L28 VCCD_QDAC
+VCCP
Max: 158mA
AF1 VCCD_HPLL
+1.05V_PEG_PLL
Max: 50mA
AA47 VCCD_PEG_PLL
D TV/CRT
+1.8V_LVDS
Max: 61mA
M38 VCCD_LVDS_1
L37 VCCD_LVDS_2
C1259 1UF/6.3V MLCC/+/-10%
C1240 0.1UF/10V
C1241 0.1UF/10V
LVDS
POWER
VTT
VTT_1 VTT_2 VTT_3 VTT_4 VTT_5 VTT_6 VTT_7 VTT_8 VTT_9 VTT_10 VTT_11 VTT_12 VTT_13 VTT_14 VTT_15 VTT_16 VTT_17 VTT_18 VTT_19 VTT_20 VTT_21 VTT_22 VTT_23 VTT_24 VTT_25
Max: 852mA
+VCCP
U13 T13 U12 T12 U11 T11 U10 T10 U9 T9 U8 T8 U7 T7 U6 T6 U5 T5 V3 U3 V2 U2 T2 V1 U1
C1260 4.7UF/6.3V
C1204 10UF/10V
C1205 10UF/10V
On the Edge
C1248 0.47UF/16V
C1206 1UF/6.3V
C1207 10UF/10V
In Cavity
AXF
VCC_AXF_1 VCC_AXF_2 VCC_AXF_3
B22 B21 A21
Max: 322mA
JP1202
+VCCP
C1217 1UF/6.3V
C1218 10UF/10V
SM_CK
VCC_SM_CK_1 VCC_SM_CK_2 VCC_SM_CK_3 VCC_SM_CK_4
BF21 BH20 BG20 BF20
+1.8V
Max: 124mA
C1245 10UF/10V MLCC/+/-10%
C1225 10UF/10V
C1226 0.1UF/10V
L1206
120Ohm/100Mhz
VCC_TX_LVDS
K47
+1.8V_LVDS
JP1201
+1.8V
Max: 120mA
C1257 22UF/6.3V
C1258 0.01UF/16V
HV
VCC_HV_1 VCC_HV_2 VCC_HV_3
C35 B35 A35
Max: 105mA
+3VS_HV
PEG
VCC_PEG_1 VCC_PEG_2 VCC_PEG_3 VCC_PEG_4 VCC_PEG_5
V48 U48 V47 U47 U46
Max: 1782mA
+VCC_PCIE
DMI
VCC_DMI_1 VCC_DMI_2 VCC_DMI_3 VCC_DMI_4
AH48 AF48 AH47 AG47
Max: 456mA
+VCC_PCIE
C1208 10UF/10V
VTTLF
VTTLF1 VTTLF2 VTTLF3
A8 L1 AB2
C1236 0.1UF/10V
C1237 0.47UF/16V
C1238 0.47UF/16V
C1239 0.47UF/16V
GND
<Variant Name>
Title : NB-Cantiga(PWR2)
ASUSTeK COMPUTER INC. NB1
Engineer: N/A
Size Custom
Project Name F82
Rev 1.2
Date: Tuesday, December 30, 2008
Sheet 12 of 93

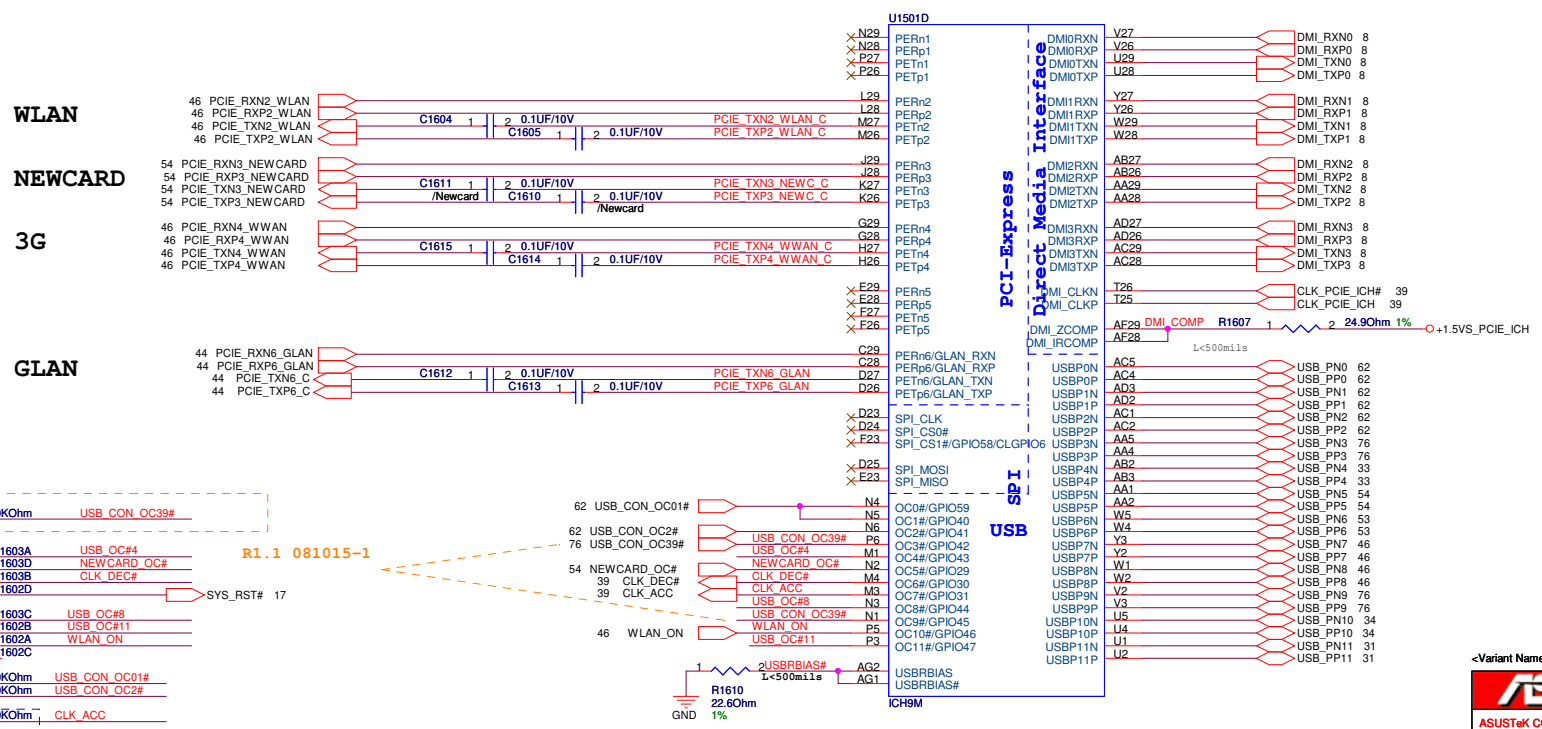


<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : NB_Cantiga(GND)	
	Engineer: N/A	
Size: Custom	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 13 of 93	


TPC26T T1501 +RTCBAT +3VA D1501 +VCC_RTC
R1501 1KOhm BAT54C C1502 1UF/10V
BAT1 SIDE1 SIDE2 WTOB_CON_2P T1502 TPC26T GND GND GND
T1507 TPC26T +VCC_RTC R1503 20KOhm T1505 RTCRST# TPC26T
C1504 1UF/10V JRST1501 SGL_JUMP
RTCRST# RC delay should be 18ms~25ms
Place Near the Open Door
R1506 20KOhm +VCC_RTC T1509 SRTCRST# TPC26T C1509 1UF/10V GND
Place Near the Open Door
delete JRST1502 for design guide recommendation.
LPC_AD0 R1516 R1535 33Ohm LPC_AD0_EC 30 LPC_AD0_TPM 53,67
LPC_AD1 R1518 R1536 33Ohm LPC_AD1_EC 30 LPC_AD1_TPM 53,67
LPC_AD2 R1522 R1530 33Ohm LPC_AD2_EC 30 LPC_AD2_TPM 53,67
LPC_AD3 R1531 R1532 33Ohm LPC_AD3_EC 30 LPC_AD3_TPM 53,67
LPC_FRAME# R1533 R1534 33Ohm LPC_FRAME#_EC 30 LPC_FRAME#_TPM 53,67
C1501 15PF/50V X1501 32.768KHZ C1503 15PF/50V SB_X1_RTC SB_X2_RTC R1502 10MOhm
U1501A
RTCX1 RTCX2 RTCRST# SRTCRST# INTRUDER# INTVRMEN LAN100_SLP
GLAN_CLK LAN_RSTSYNC LAN_RXD0 LAN_RXD1 LAN_RXD2 LAN_TXD0 LAN_TXD1 LAN_TXD2
GLAN_DOCK#/GPIO56 GLAN_COMPI GLAN_COMPO
HDA_BIT_CLK HDA_SYNC HDA_RST# HDA_SDIN0 HDA_SDIN1 HDA_SDIN2 HDA_SDIN3 HDA_SDOUT HDA_DOCK_EN#/GPIO33 HDA_DOCK_RST#/GPIO34
SATALED# SATA0RXN SATA0RXP SATA0TXN SATA0TXP SATA1RXN SATA1RXP SATA1TXN SATA1TXP
RTC LPC GLAN LAN / CPU IHDA SATA
FWH0/LAD0 FWH1/LAD1 FWH2/LAD2 FWH3/LAD3 FWH4/LFRAME# LDRQ0# LDRQ1#/GPIO23
A20GATE A20M# DPRSTP# DPSLP# FERR# CPUPWRGD IGNNE# INIT# INTR RCIN# NMI SMI# STPCLK# THRMTRIP# PECI
SATA4RXN SATA4RXP SATA4TXN SATA4TXP SATA5RXN SATA5RXP SATA5TXN SATA5TXP SATA_CLKN SATA_CLKP SATARBIAS# SATARBIAS
ICH9M
+VCCP R1507 56Ohm R1528 56Ohm R1514 56Ohm R1519 54.9Ohm
H_DPRSTP# H_DPSLP# H_FERR# H_PWRGD H_IGNNE# H_INIT# H_INTR H_NMI# H_SMI# H_STPCLK# PM_THRMTRIP# H_THRMTRIP#
R1527 24.9Ohm R1526 24.9Ohm
HDD 1st
ODD
E-SATA
eSATA_RXN eSATA_RXP eSATA_TXN eSATA_TXP
CLK_SATA_ICH# CLK_SATA_ICH
ICH_INTVRMEN(VCCSUS1_05,VCCSUS1_5,VCCCL1_5)
Low - Disabled Internal VR
High - Enable Internal VR(D)
ICH_LAN100 (VCCLAN1_05,VCCCL1_05)
Low - Disabled Internal VR
High - Enable Internal VR(D)
R1.1 081029-3
+3VS R1521 1KOhm ACZ_SDOUT ICH_TP3 R1523 1KOhm GND
XOR Chain Entrance Strap
ICH_TP3 ACZ_SDOUT Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal Operation (D)
1 1 Set PCIe port config bit 1
SPI BOOT STRAP
R1524 10KOhm GPIO33
+3VSUS R1525 10KOhm GPIO56
+3VS R1529 10KOhm SATA_LED#
<Variant Name>
Title : SB-ICH9M(1)
ASUSTeK COMPUTER INC. NB1
Engineer: N/A
Size Custom
Project Name F82
Rev 1.2
Date: Tuesday, December 30, 2008
Sheet 15 of 93





USB 0	USB Conn.(M/B)
USB 1	USB Conn.(M/B)
USB 2	USB Conn.(M/B)
USB 3	Reserve for 17"
USB 4	CMOS Camera(D/B)
USB 5	New CARD
USB 6	Card Reader
USB 7	WLAN
USB 8	3G
USB 9	EXPRESS GATE
USB 10	Bluetooth(M/B)
USB 11	FingerPrint

<Variant Name>

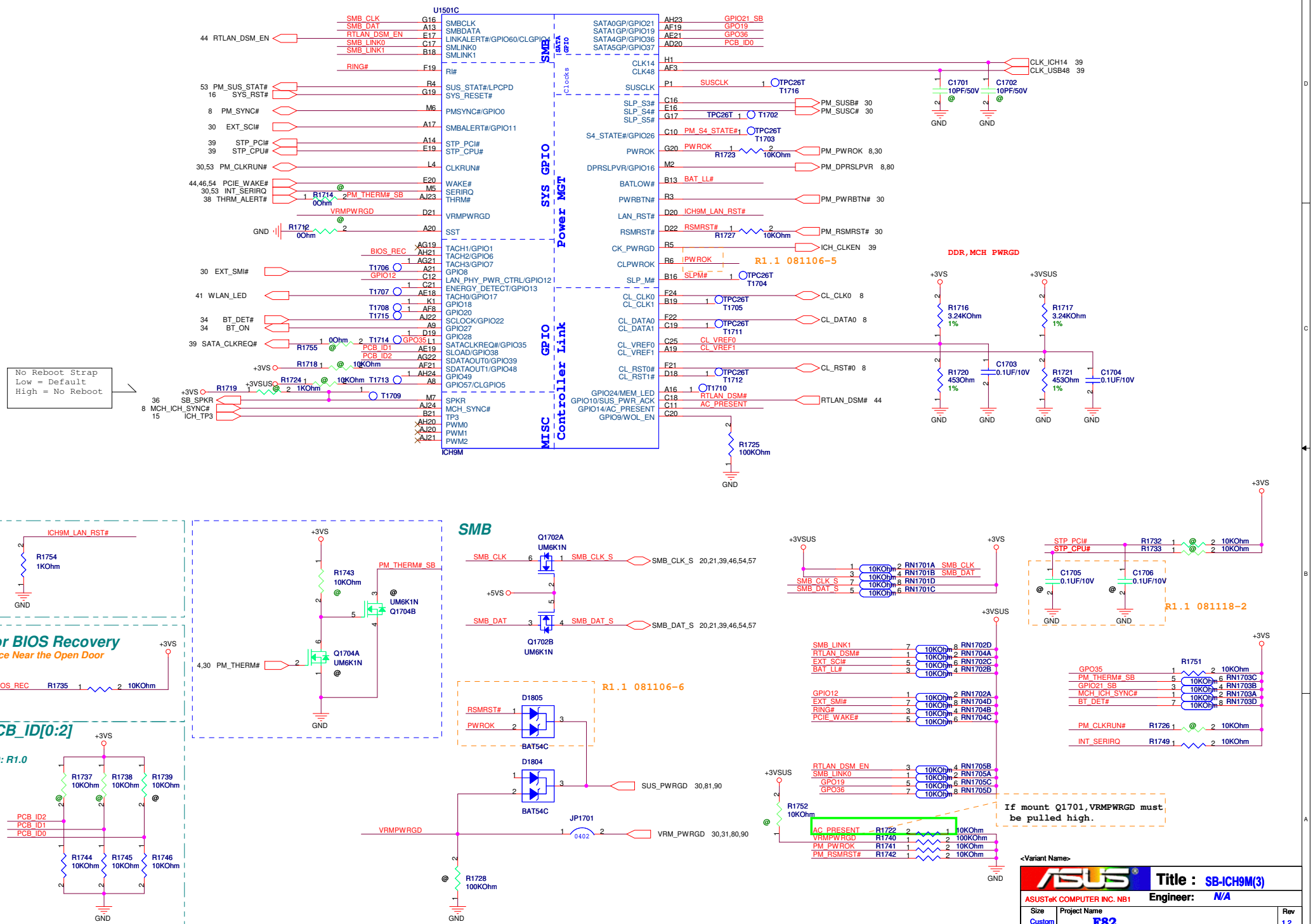
ASUSTeK COMPUTER INC. NB1

Title : SB-ICH9M(2)

Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 16 of 93


U1501C
SMB_CLK G16
SMB_DAT A13
RTLAN_DSM_EN E17
SMB_LINK0 C17
SMB_LINK1 B18
RING# F19
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA0GP/GPIO21 AH23 GPIO21_SB
SATA1GP/GPIO19 AF19 GPO19
SATA4GP/GPIO36 AE21 GPO36
SATA5GP/GPIO37 AD20 PCB_ID0
CLK14 H1
CLK48 AF3
SUSCLK P1
SLP_S3# C16
SLP_S4# E16
SLP_S5# G17
S4_STATE#/GPIO26 C10
PWROK G20
DPRSLPVR/GPIO16 M2
BATLOW# B13
PWRBTN# R3
LAN_RST# D20
RSMRST# D22
CK_PWRGD R5
CLPWROK R6
SLP_M# B16
CL_CLK0 F24
CL_CLK1 B19
CL_DATA0 F22
CL_DATA1 C19
CL_VREF0 C25
CL_VREF1 A19
CL_RST0# F21
CL_RST1# D18
GPIO24/MEM_LED A16
GPIO10/SUS_PWR_ACK C18
GPIO14/AC_PRESENT C11
GPIO9/WOL_EN C20
ICH9M
44 RTLAN_DSM_EN
53 PM_SUS_STAT#
16 SYS_RST#
8 PM_SYNC#
30 EXT_SCI#
39 STP_PCI#
39 STP_CPU#
30,53 PM_CLKRUN#
44,46,54 PCIE_WAKE#
30,53 INT_SERIRQ
38 THRM_ALERT#
R1714 0Ohm
PM_THERM# SB
VRMPWRGD
R1712 0Ohm
GND
BIOS_REC
30 EXT_SMI#
GPIO12
41 WLAN_LED
34 BT_DET#
34 BT_ON
39 SATA_CLKREQ#
R1755 0Ohm
GPO35
PCB_ID1
PCB_ID2
+3VS
R1718 10KOhm
R1724 1KOhm
+3VSUS
R1719
T1709
36 SB_SPKR
8 MCH_ICH_SYNC#
15 ICH_TP3
SUSCLK
PM_SUSB# 30
PM_SUSC# 30
PM_S4_STATE#
PWROK
R1723 10KOhm
PM_PWROK 8,30
PM_DPRSLPVR 8,80
BAT_LL#
PM_PWRBTN# 30
ICH9M_LAN_RST#
RSMRST#
R1727 10KOhm
PM_RSMRST# 30
ICH_CLKEN 39
R1.1 081106-5
SLPM#
CL_CLK0 8
CL_DATA0 8
CL_VREF0
CL_VREF1
CL_RST#0 8
RTLAN_DSM# 44
AC_PRESENT
R1725 100KOhm
CLK_ICH14 39
CLK_USB48 39
C1701 10PF/50V
C1702 10PF/50V
TPC26T T1716
TPC26T T1702
TPC26T T1703
TPC26T T1704
TPC26T T1705
TPC26T T1711
TPC26T T1712
T1710
DDR,MCH PWRGD
+3VS
+3VSUS
R1716 3.24KOhm 1%
R1717 3.24KOhm 1%
R1720 453Ohm 1%
R1721 453Ohm 1%
C1703 0.1UF/10V
C1704 0.1UF/10V
No Reboot Strap
Low = Default
High = No Reboot
ICH9M_LAN_RST#
R1754 1KOhm
For BIOS Recovery
Place Near the Open Door
BIOS_REC R1735 10KOhm
PCB_ID[0:2]
000: R1.0
R1737 10KOhm
R1738 10KOhm
R1739 10KOhm
R1744 10KOhm
R1745 10KOhm
R1746 10KOhm
PCB_ID2
PCB_ID1
PCB_ID0
R1743 10KOhm
PM_THERM# SB
UM6K1N Q1704B
Q1704A UM6K1N
4,30 PM_THERM#
SMB
Q1702A UM6K1N
SMB_CLK
SMB_CLK_S
SMB_CLK_S 20,21,39,46,54,57
+5VS
SMB_DAT
SMB_DAT_S
SMB_DAT_S 20,21,39,46,54,57
Q1702B UM6K1N
R1.1 081106-6
D1805
RSMRST#
PWROK
BAT54C
D1804
SUS_PWRGD 30,81,90
JP1701
0402
VRMPWRGD
VRM_PWRGD 30,31,80,90
R1728 100KOhm
RN1701A SMB_CLK
RN1701B SMB_DAT
RN1701D
RN1701C
SMB_CLK_S
SMB_DAT_S
RN1702D
RN1704A
RN1702C
RN1702B
SMB_LINK1
RTLAN_DSM#
EXT_SCI#
BAT_LL#
RN1702A
RN1704D
RN1704B
RN1704C
GPIO12
EXT_SMI#
RING#
PCIE_WAKE#
RN1705B
RN1705A
RN1705C
RN1705D
SMB_LINK0
GPO19
GPO36
R1752 10KOhm
AC_PRESENT R1722 10KOhm
VRMPWRGD R1740 100KOhm
PM_PWROK R1741 10KOhm
PM_RSMRST# R1742 10KOhm
If mount Q1701,VRMPWRGD must be pulled high.
STP_PCI# R1732 10KOhm
STP_CPU# R1733 10KOhm
C1705 0.1UF/10V
C1706 0.1UF/10V
R1.1 081118-2
R1751
GPO35
PM_THERM# SB
GPIO21_SB
MCH_ICH_SYNC#
BT_DET#
RN1703C
RN1703B
RN1703A
RN1703D
PM_CLKRUN# R1726 10KOhm
INT_SERIRQ R1749 10KOhm
GND
<Variant Name>
Title : SB-ICH9M(3)
ASUSTeK COMPUTER INC. NB1
Engineer: N/A
Size Custom
Project Name F82
Rev 1.2
Date: Tuesday, December 30, 2008
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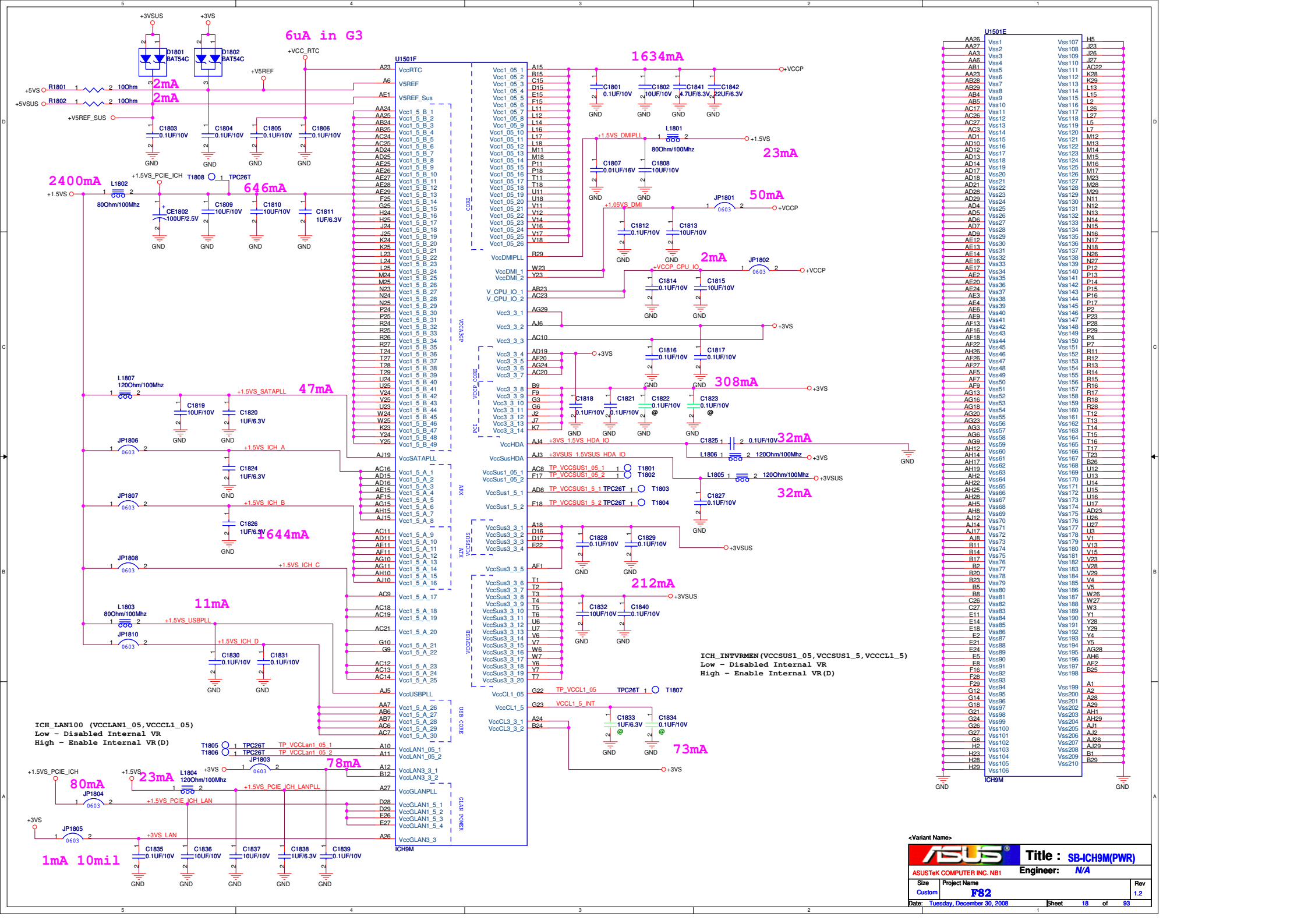
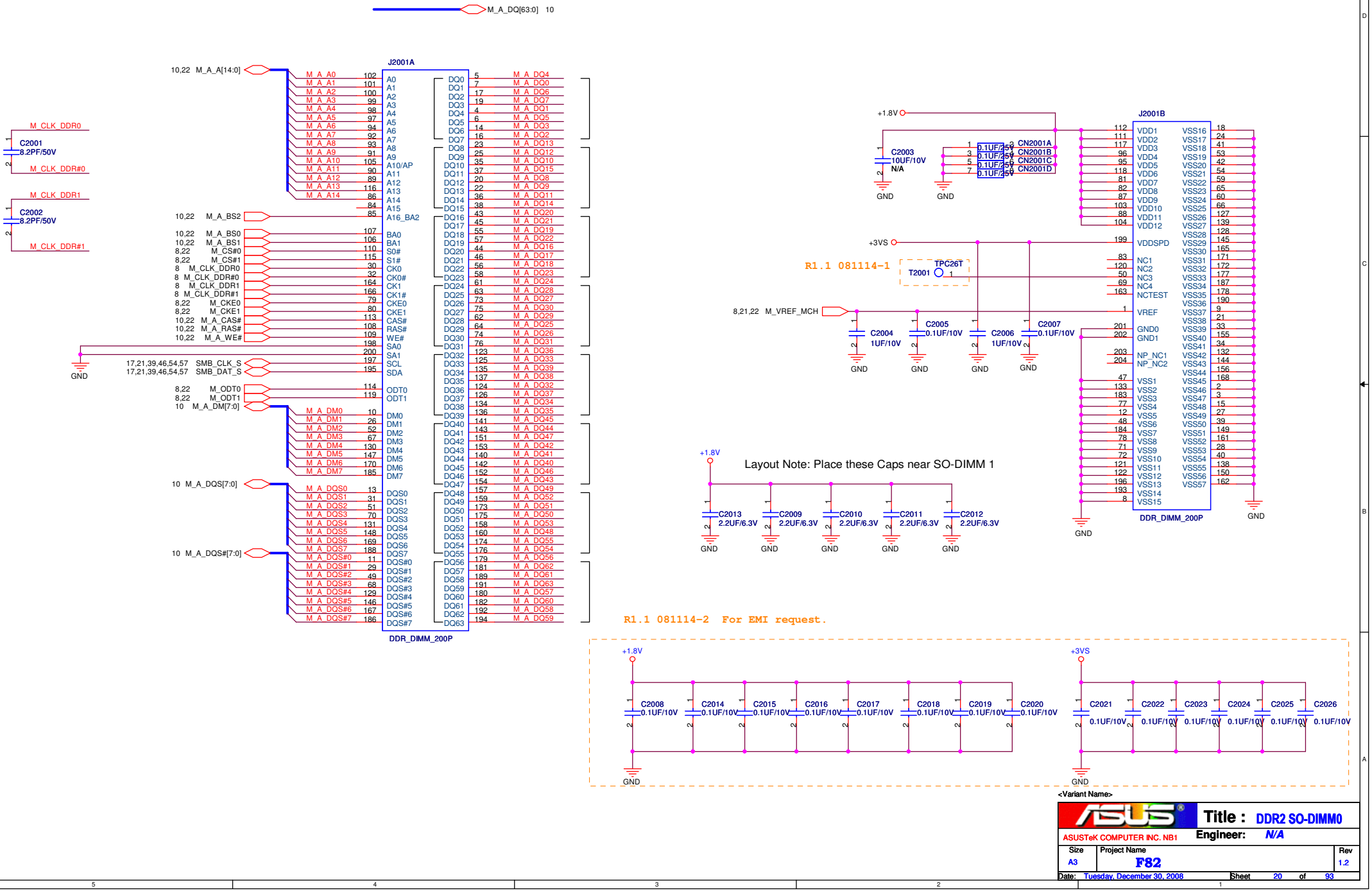

6uA in G3
2mA
2mA
2400mA
646mA
47mA
1644mA
11mA
1634mA
23mA
50mA
2mA
308mA
32mA
32mA
212mA
73mA
78mA
23mA
80mA
1mA 10mil
ICH_LAN100 (VCCLAN1_05,VCCCL1_05)
Low - Disabled Internal VR
High - Enable Internal VR(D)
ICH_INTVRMEN(VCCSUS1_05,VCCSUS1_5,VCCCL1_5)
Low - Disabled Internal VR
High - Enable Internal VR(D)
U1501F
ICH9M
U1501E
ICH9M
Title : SB-ICH9M(PWR)
ASUSTeK COMPUTER INC. NB1
Engineer: N/A
Project Name F82
Rev 1.2
Date: Tuesday, December 30, 2008
Sheet 18 of 93

DDR2 200P H=4.0mm (Reverse Type)



<Variant Name>

ASUSTeK COMPUTER INC. NB1

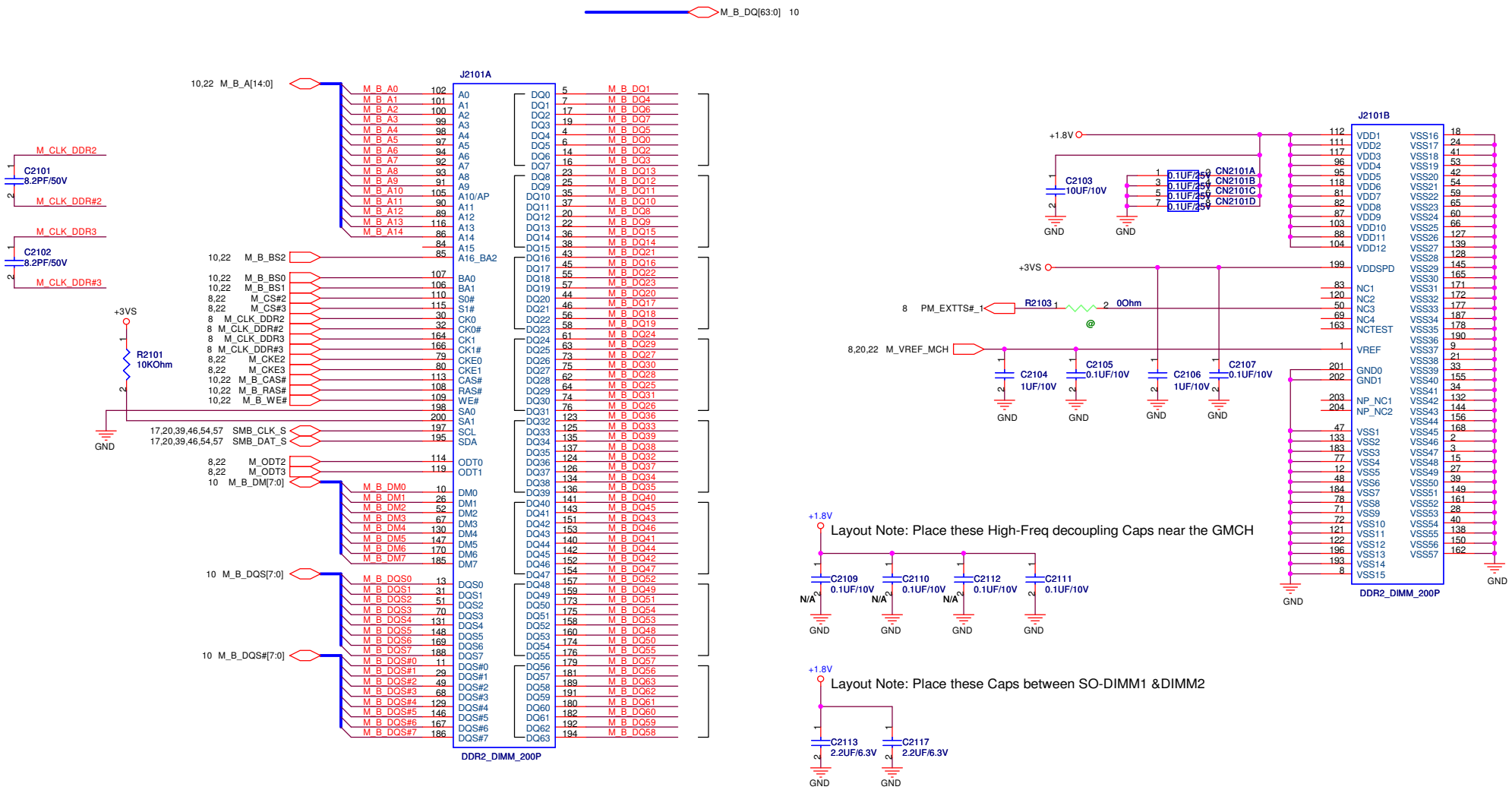
Title : DDR2 SO-DIMM0

Engineer: N/A

Size	Project Name	Rev
A3	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 20 of 93

DDR2 200P H=9.2mm (Reverse Type)



<Variant Name>

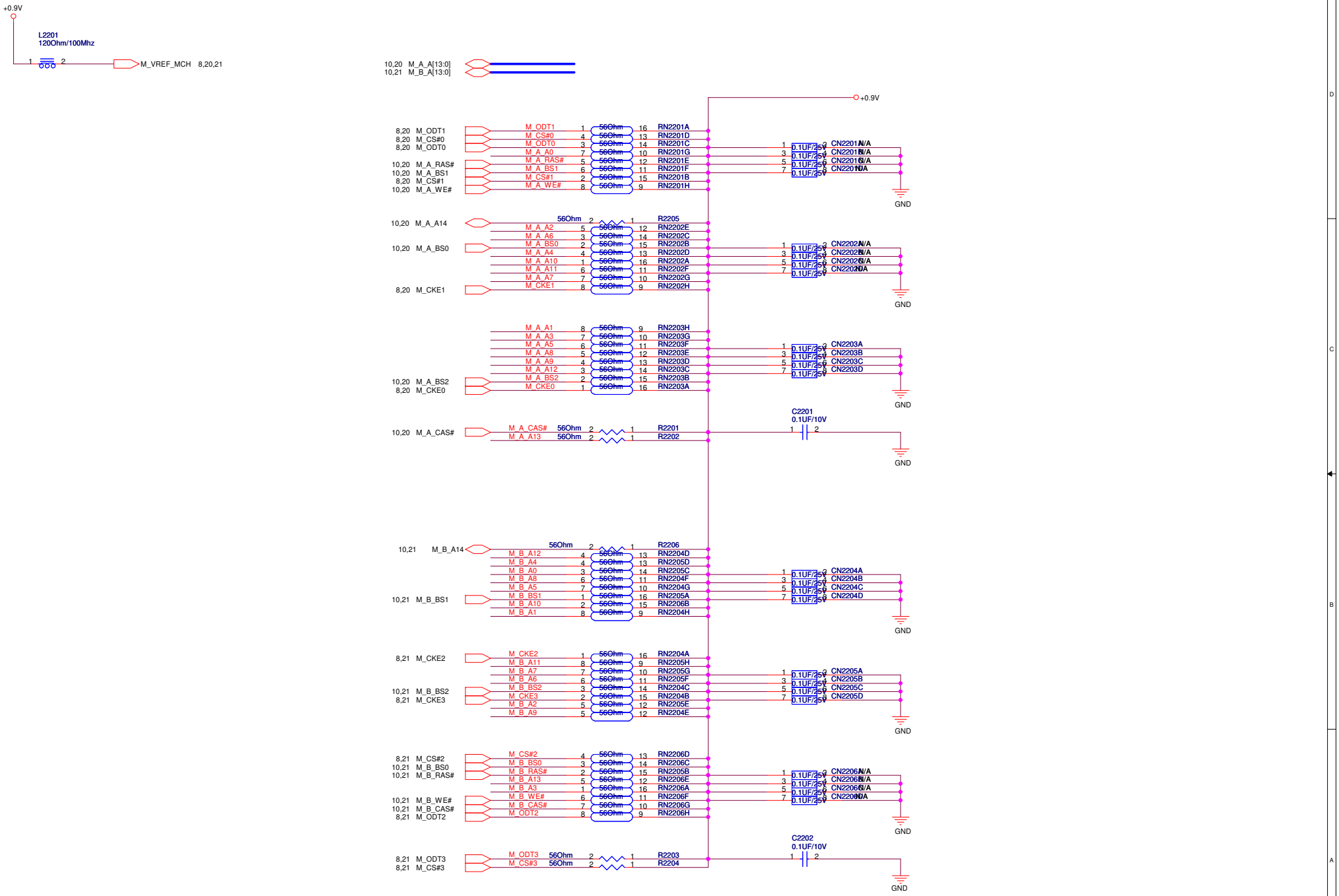
ASUSTeK COMPUTER INC. NB1

Title : DDR2 SO-DIMM1

Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 21 of 93



<Variant Name>

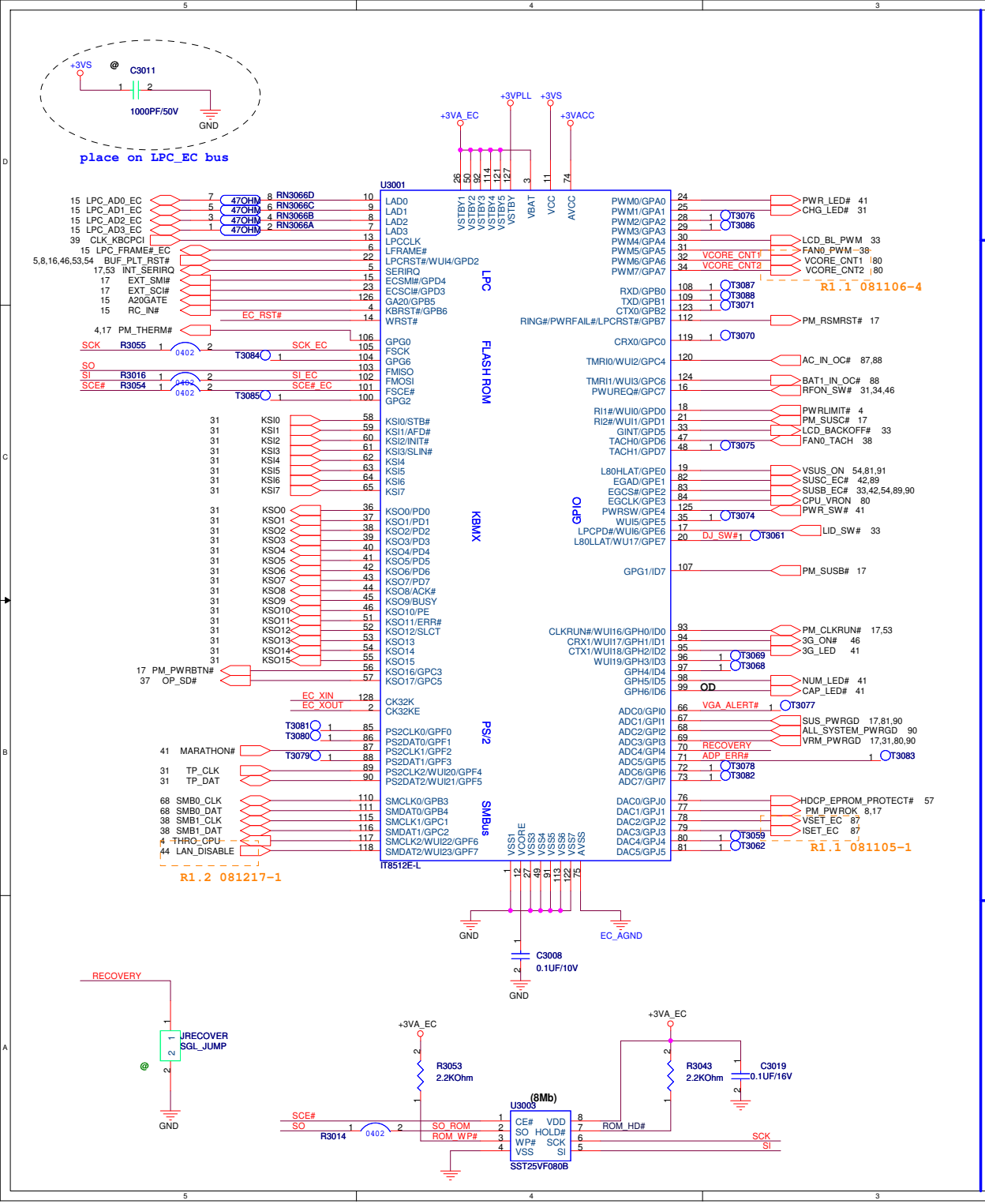
ASUSTeK COMPUTER INC. NB1

Title : DDR2 TERMINATION

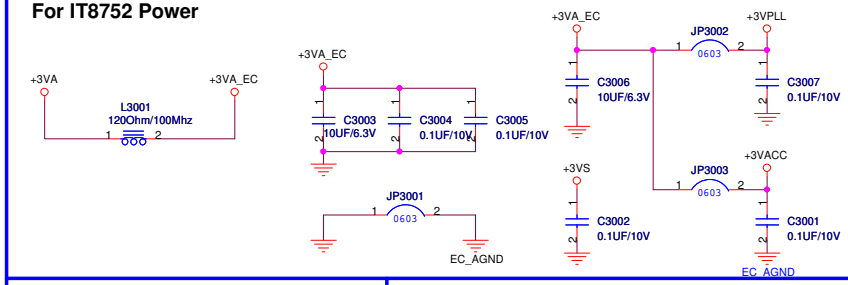
Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

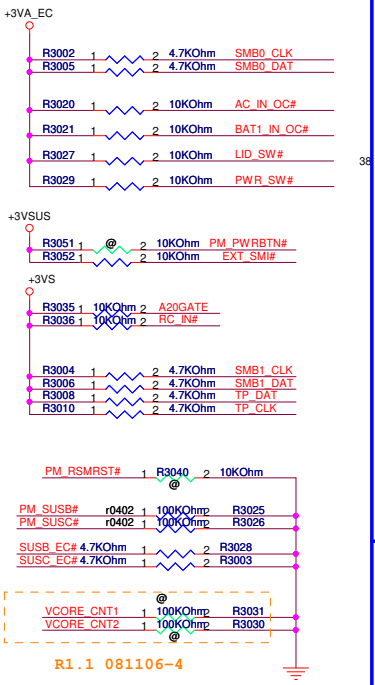
Date: Tuesday, December 30, 2008 Sheet 22 of 93



For IT8752 Power

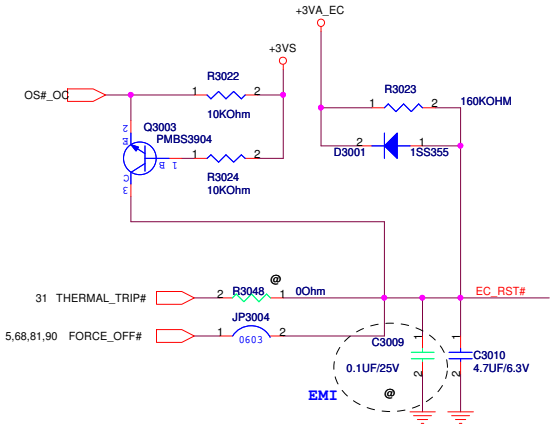


For PU / PD



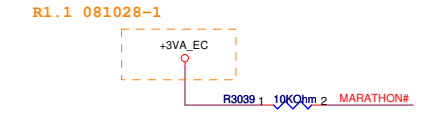
Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.

For EC Reset



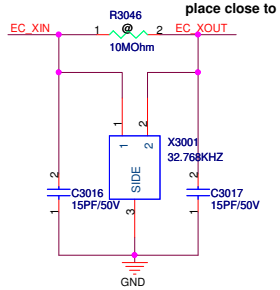
For Instant Key

Note: Close to EC



For X'tal

Note:
Cload=12.5PF
place close to EC



For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

Note: It can be programmable by EC fireware.

PP Enable

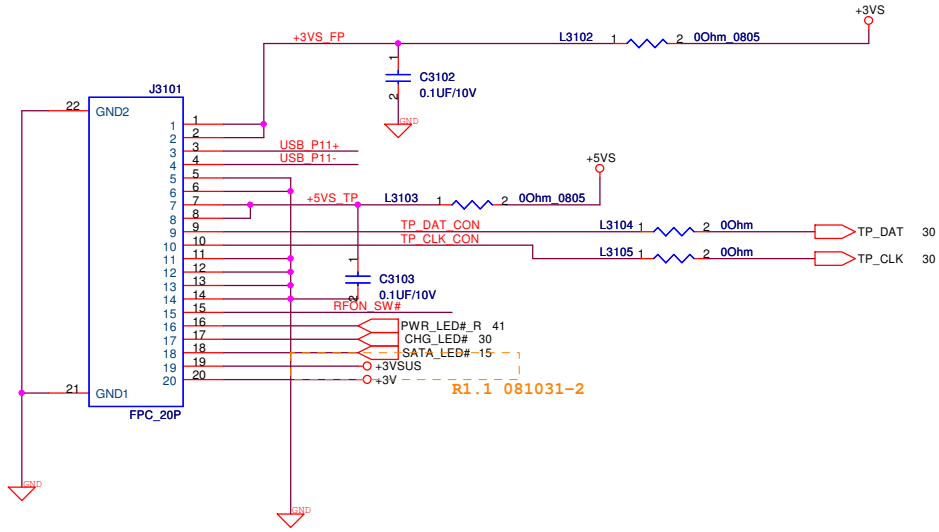
Note: Default Int. Pull-Low

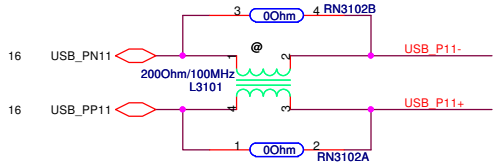
For iAMT pin name

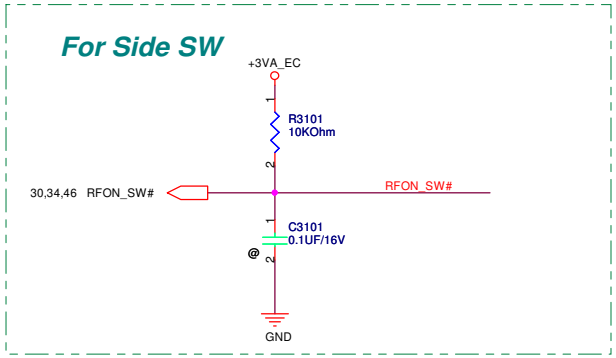
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

ASUSTeK COMPUTER INC. NB1	Title : EC_IT8512E-L (1/2)	
	Engineer: Wendell Lo	
Size: Custom	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 30 of 93	

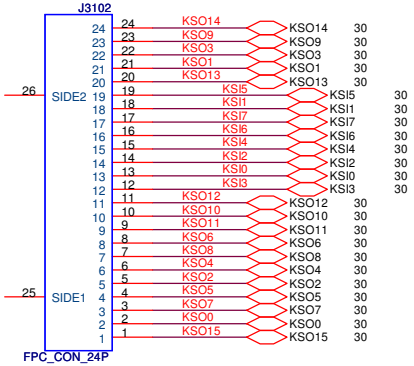
TouchPad & FingerPrint

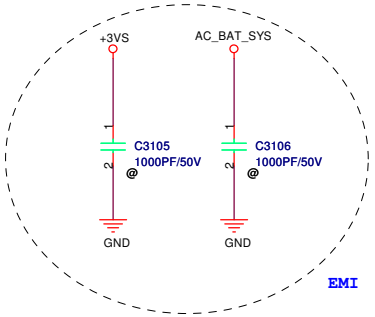






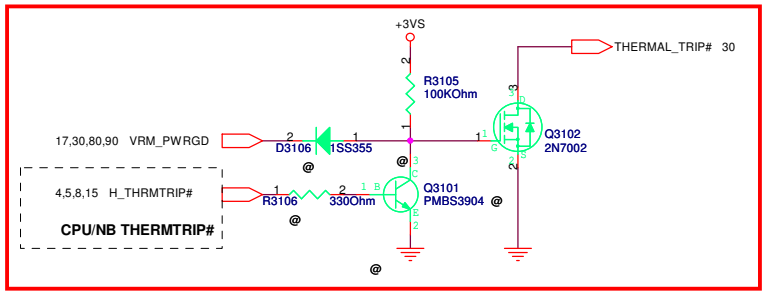
Keyboard Connector



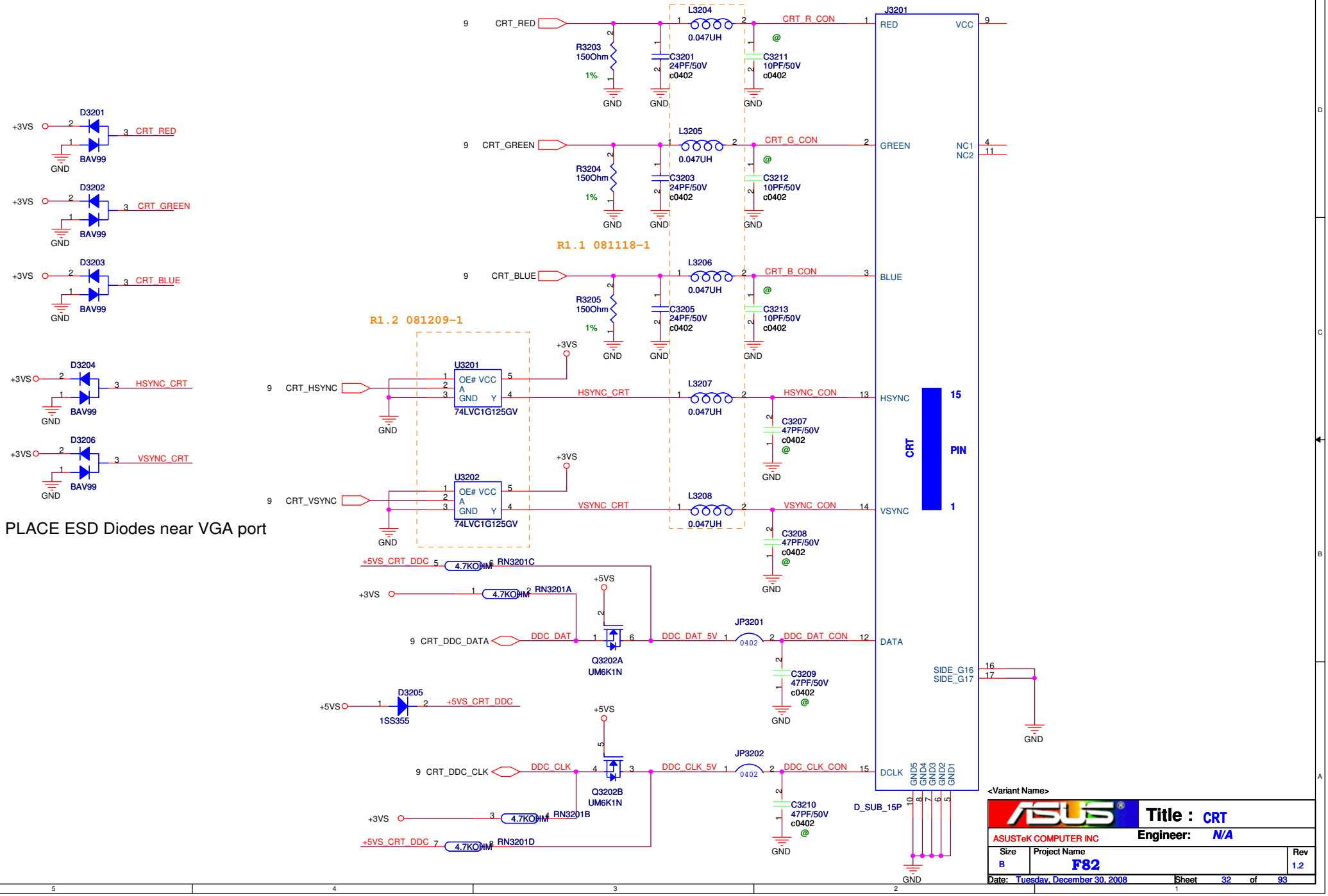


For Thermal Control Method

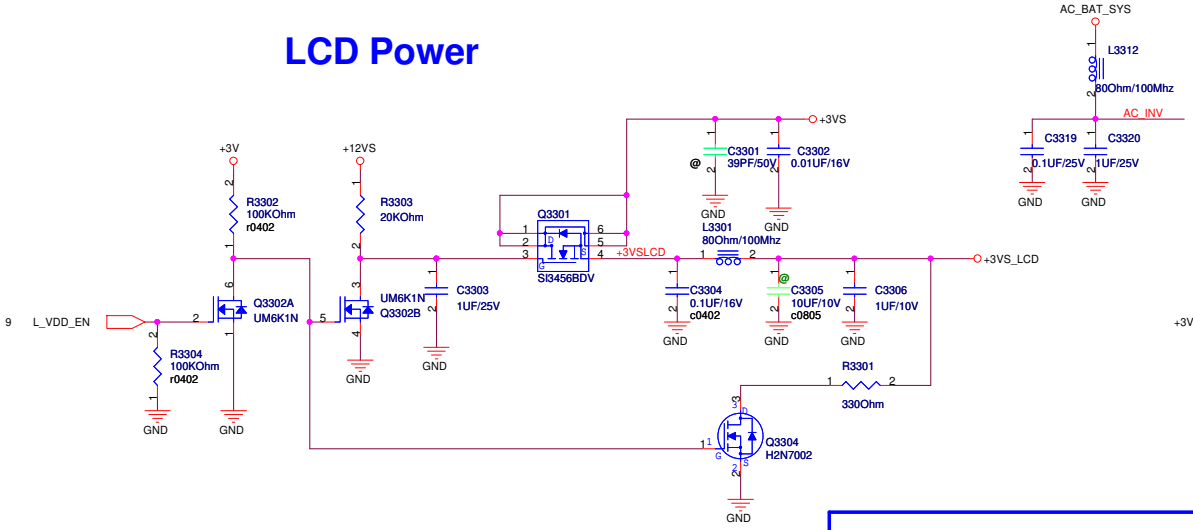
Remove redundant components



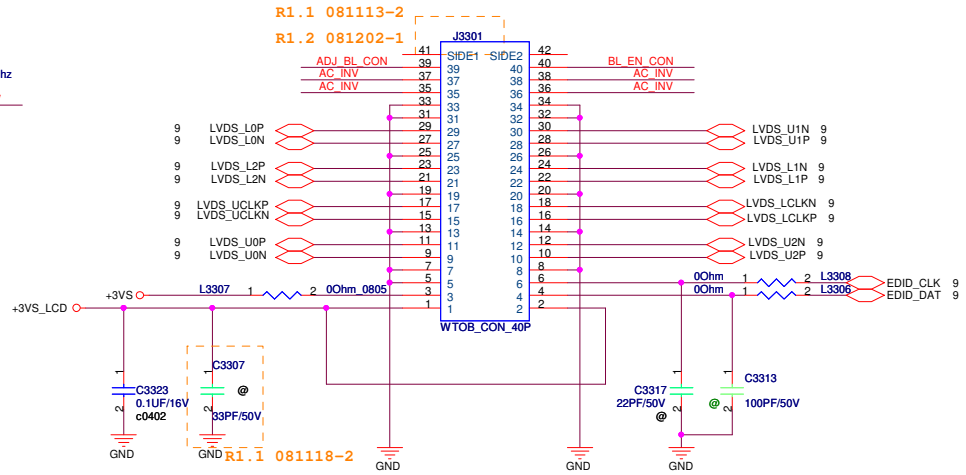
ASUSTeK COMPUTER INC. NB1	Title : EC_IT8752(2/2)		
	Engineer: N/A		
Size: Custom	Project Name: F82		Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 31 of 93		

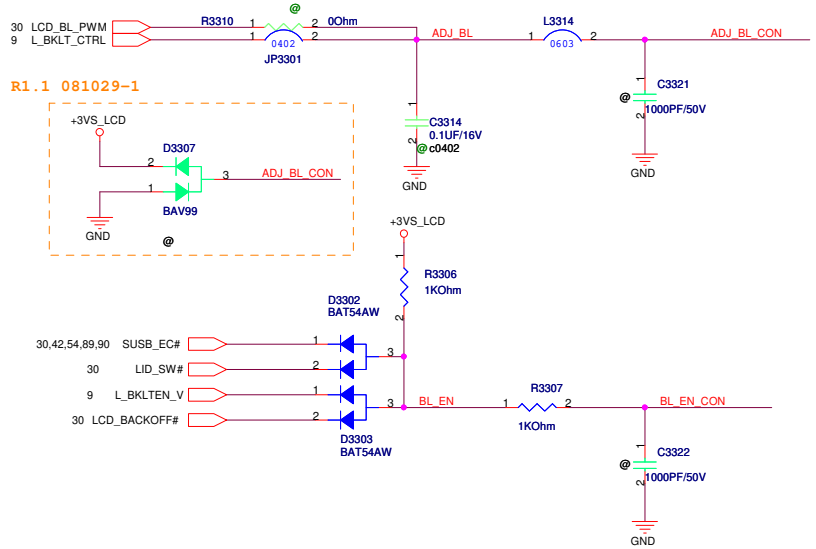

D3201
D3202
D3203
D3204
D3206
BAV99
+3VS
GND
CRT_RED
CRT_GREEN
CRT_BLUE
HSYNC_CRT
VSYNC_CRT
PLACE ESD Diodes near VGA port
R1.1 081118-1
R1.2 081209-1
L3204
L3205
L3206
0.047UH
R3203
R3204
R3205
150Ohm
1%
C3201
C3203
C3205
24PF/50V
c0402
C3211
C3212
C3213
10PF/50V
@
CRT_R_CON
CRT_G_CON
CRT_B_CON
J3201
RED
GREEN
BLUE
VCC
NC1
NC2
U3201
U3202
OE# VCC
A
GND Y
74LVC1G125GV
L3207
L3208
HSYNC_CON
VSYNC_CON
C3207
C3208
47PF/50V
HSYNC
VSYNC
CRT
PIN
15
1
+5VS_CRT_DDC
RN3201C
RN3201A
4.7KOHM
CRT_DDC_DATA
DDC_DAT
DDC_DAT_5V
DDC_DAT_CON
JP3201
0402
Q3202A
UM6K1N
C3209
DATA
D3205
1SS355
CRT_DDC_CLK
DDC_CLK
DDC_CLK_5V
DDC_CLK_CON
JP3202
Q3202B
RN3201B
RN3201D
C3210
DCLK
D_SUB_15P
GND5
GND4
GND3
GND2
GND1
SIDE_G16
SIDE_G17
<Variant Name>
Title : CRT
ASUSTeK COMPUTER INC
Engineer: N/A
Size B
Project Name F82
Rev 1.2
Date: Tuesday, December 30, 2008
Sheet 32 of 93

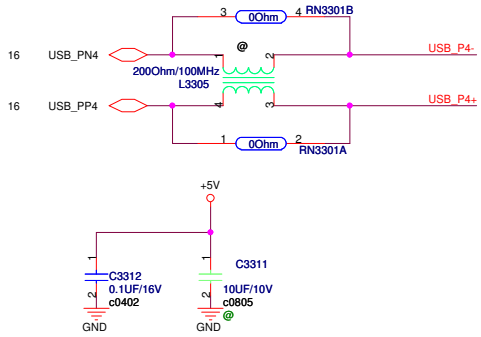
LCD Power



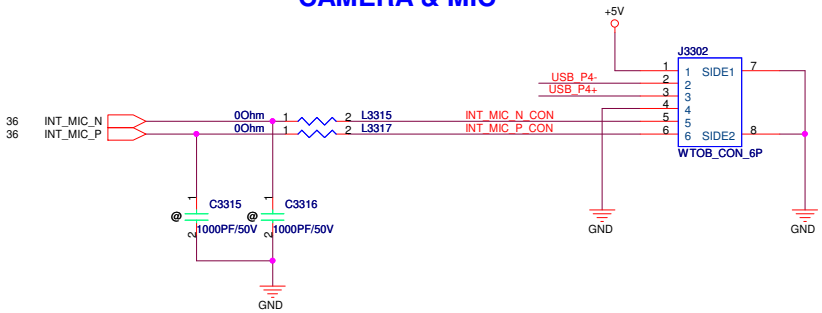
LED PANEL LVDS Interface



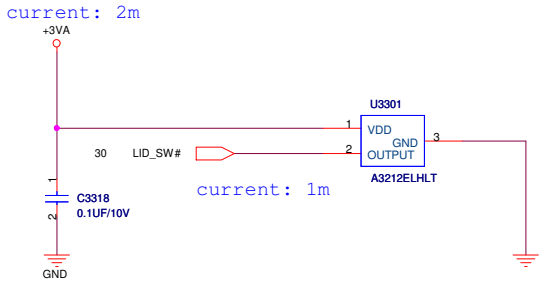




CAMERA & MIC



Hall effect switch



<Variant Name>

ASUSTeK COMPUTER INC

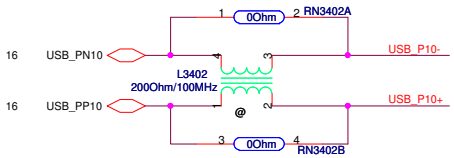
Title : LVDS & INVERTER

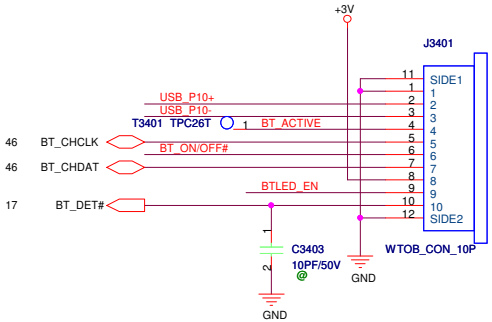
Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

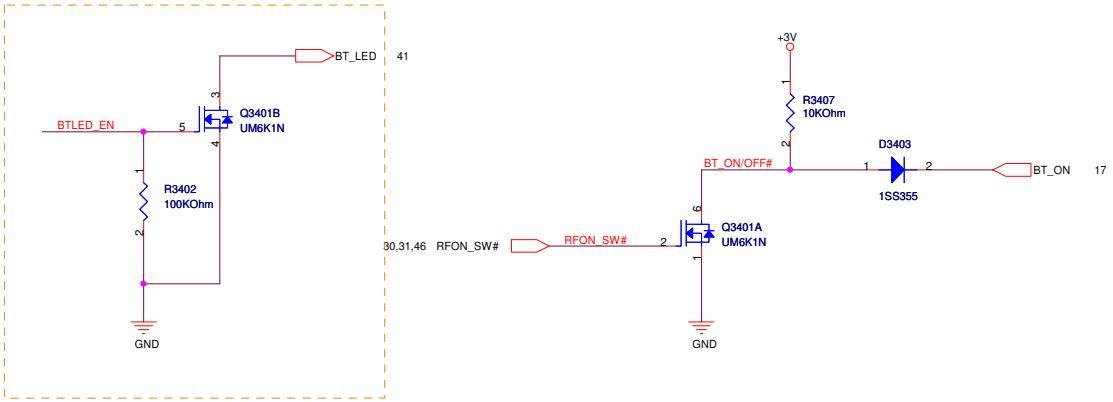
Date: Tuesday, December 30, 2008 Sheet 33 of 93

For Bluetooth





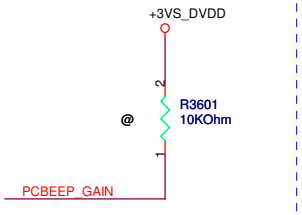
R1.1 081031-4



<Variant Name>

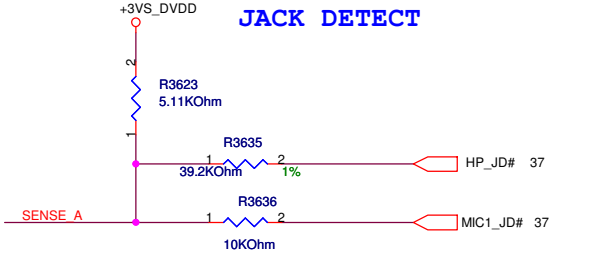
ASUSTeK COMPUTER INC	Title : BT	
	Engineer: N/A	
Size: Custom	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 34 of 93	

PC BEEP GAIN CONTROL



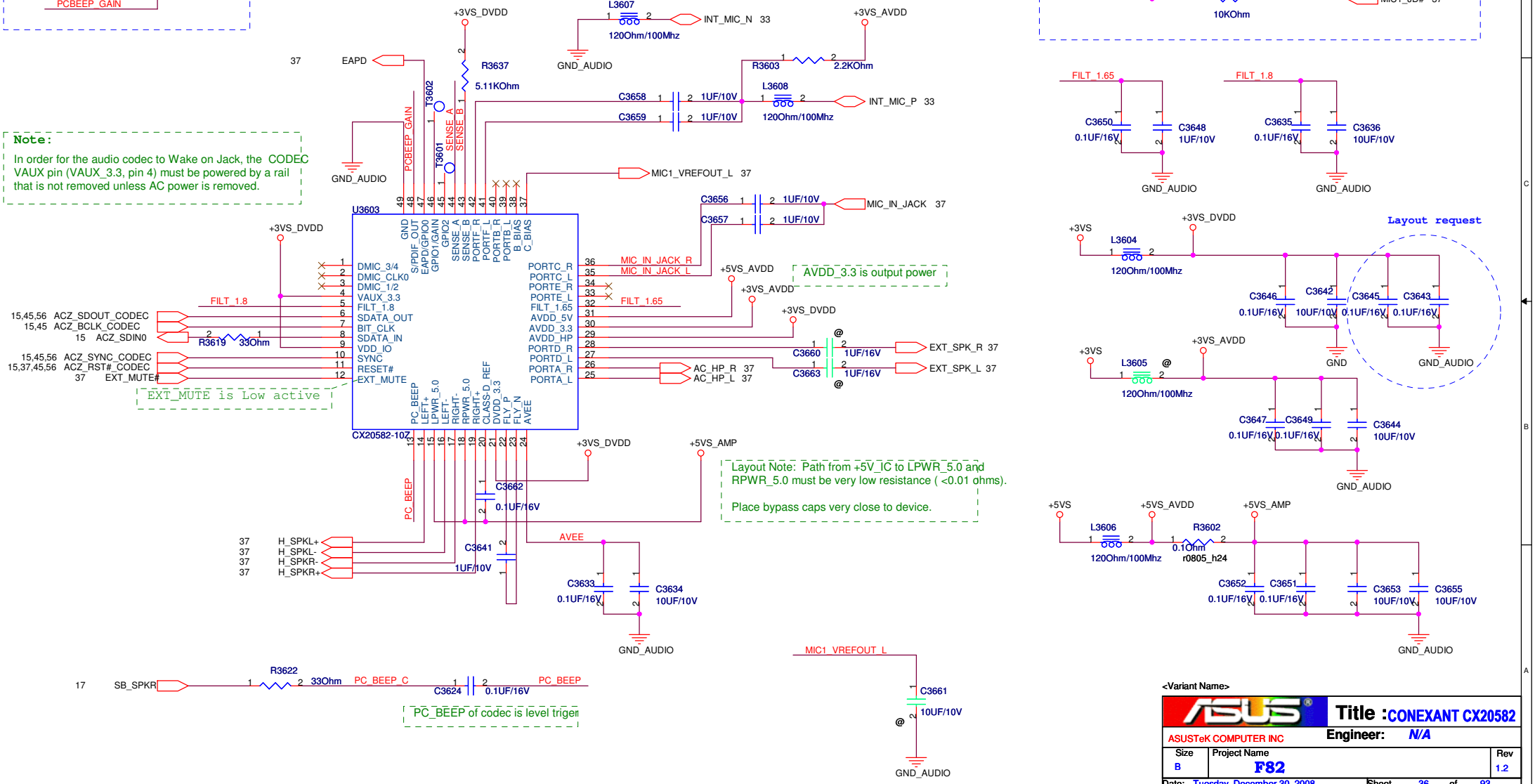
GAIN	R3601 Pull-up
-46 dB	Omit
-18 dB	Populate

JACK DETECT



Note:

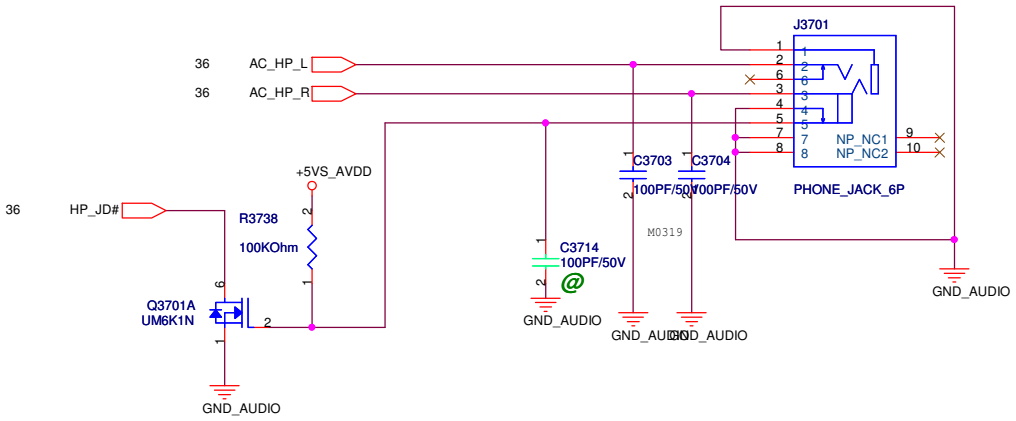
In order for the audio codec to Wake on Jack, the CODEC VAUX pin (VAUX_3.3, pin 4) must be powered by a rail that is not removed unless AC power is removed.



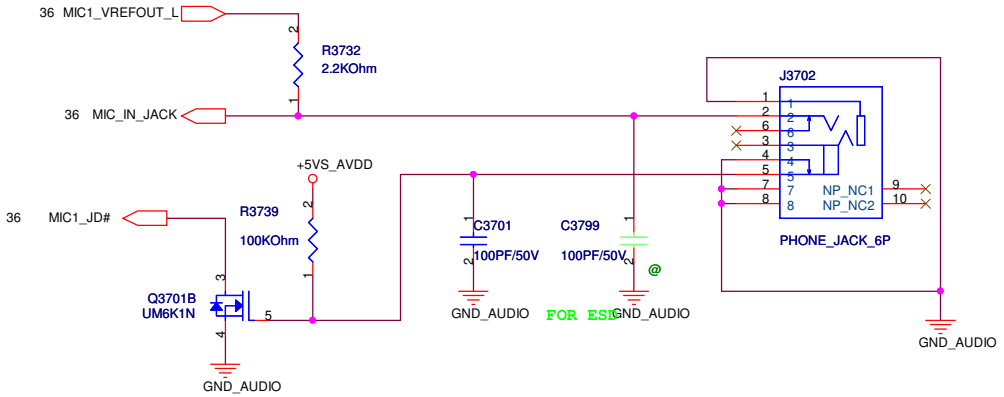
<Variant Name>

ASUSTeK COMPUTER INC	Title : CONEXANT CX20582	
	Engineer: N/A	
Size: B	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 36 of 93	

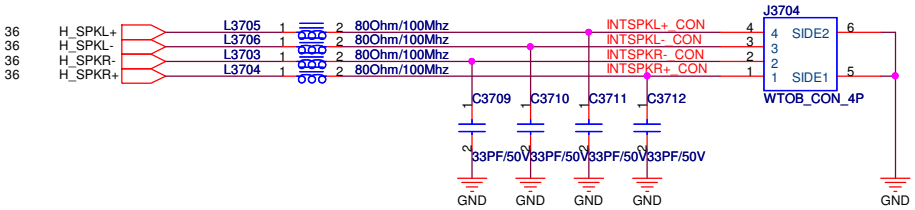
HP CONN



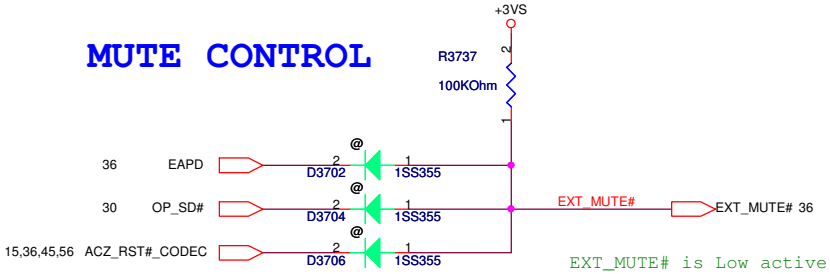
External MIC CONN



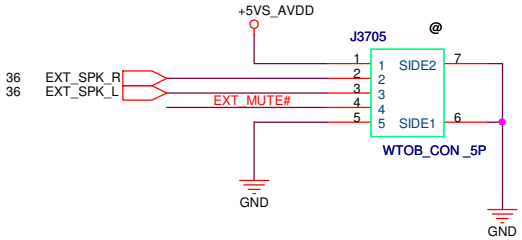
SPEAKER CONNECTOR(2W)

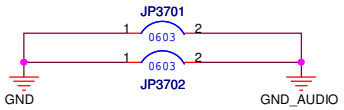


MUTE CONTROL



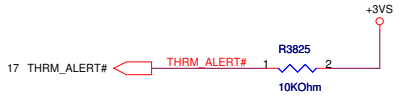
EXTENSION SPEAKER CONNECTOR

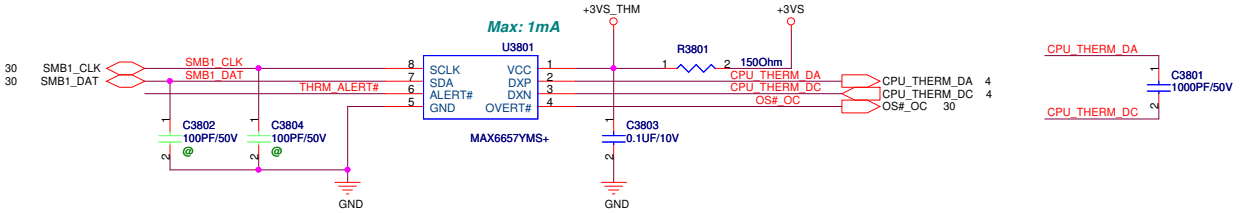




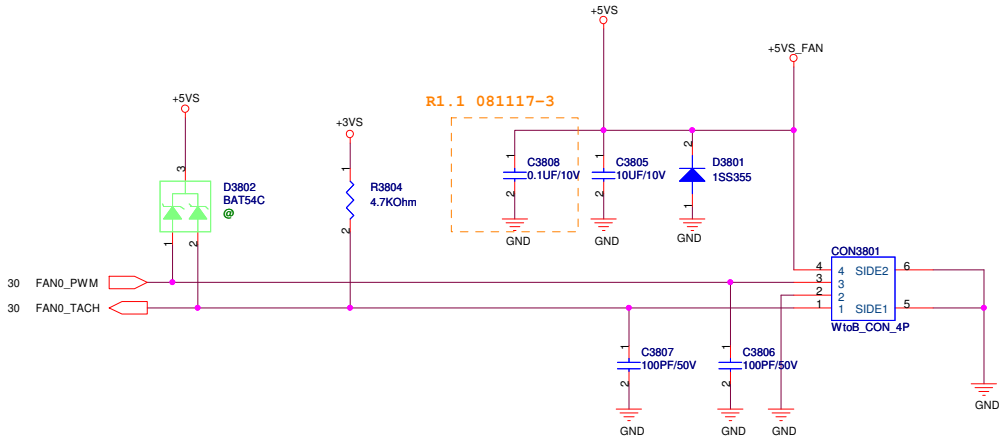
ASUSTeK COMPUTER INC. NB1	Title : AUDIO HP/MIC	
	Engineer: N/A	
Size: B	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 37 of 93	

Thermal Sensor



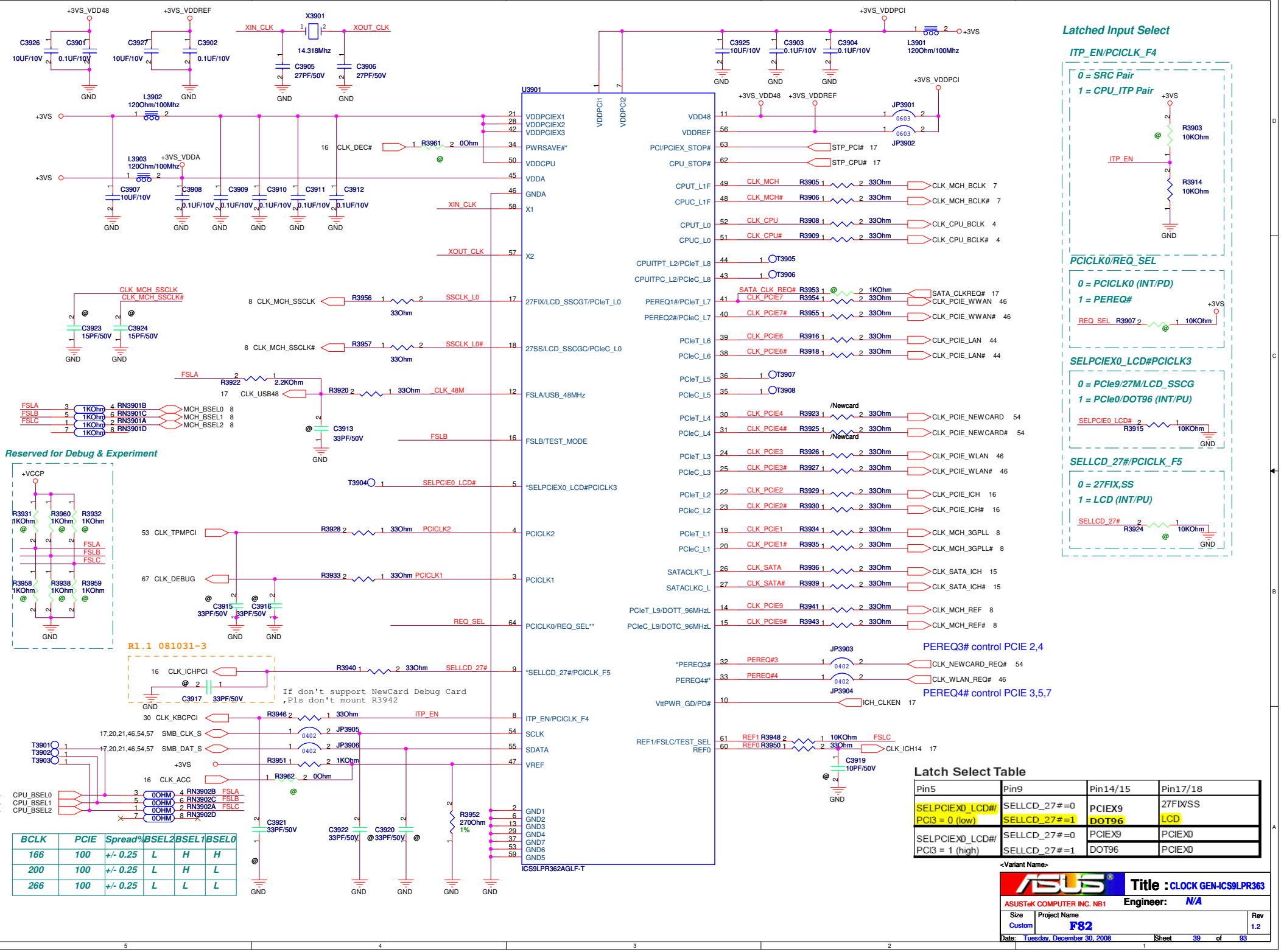


add 2nd source :06G023096010

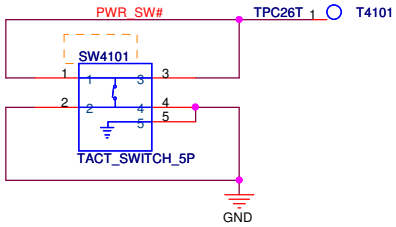


<Variant Name>

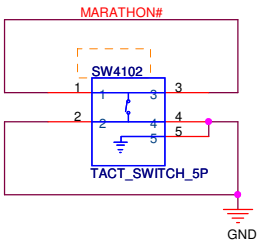
ASUSTeK COMPUTER INC. NB1	Title : THER SENSOR & FAN	
	Engineer: N/A	
Size: Custom	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 38 of 93	

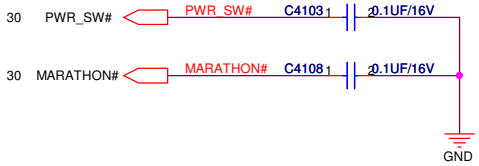

U3901
ICS9LPR362AGLF-T
X3901
14.318Mhz
XIN_CLK
XOUT_CLK
+3VS_VDD48
+3VS_VDDREF
+3VS_VDDPCI
+3VS_VDDA
+3VS
GND
L3902 120Ohm/100Mhz
L3903 120Ohm/100Mhz
L3901 120Ohm/100Mhz
C3926 10UF/10V
C3901 0.1UF/10V
C3927 10UF/10V
C3902 0.1UF/10V
C3905 27PF/50V
C3906 27PF/50V
C3925 10UF/10V
C3903 0.1UF/10V
C3904 0.1UF/10V
C3907 10UF/10V
C3908 0.1UF/10V
C3909 0.1UF/10V
C3910 0.1UF/10V
C3911 0.1UF/10V
C3912 0.1UF/10V
VDDPCIEX1
VDDPCIEX2
VDDPCIEX3
PWRSAVE#*
VDDCPU
VDDA
GNDA
X1
X2
27FIX/LCD_SSCGT/PCIeT_L0
27SS/LCD_SSCGC/PCIeC_L0
FSLA/USB_48MHz
FSLB/TEST_MODE
*SELPCIEX0_LCD#PCICLK3
PCICLK2
PCICLK1
PCICLK0/REQ_SEL**
*SELLCD_27#/PCICLK_F5
ITP_EN/PCICLK_F4
SCLK
SDATA
VREF
GND1
GND2
GND3
GND4
GND7
GND6
GND5
VDDPCI1
VDDPCI2
VDD48
VDDREF
PCI/PCIEX_STOP#
CPU_STOP#
CPUT_L1F
CPUC_L1F
CPUT_L0
CPUC_L0
CPUITPT_L2/PCIeT_L8
CPUITPC_L2/PCIeC_L8
PEREQ1#/PCIeT_L7
PEREQ2#/PCIeC_L7
PCIeT_L6
PCIeC_L6
PCIeT_L5
PCIeC_L5
PCIeT_L4
PCIeC_L4
PCIeT_L3
PCIeC_L3
PCIeT_L2
PCIeC_L2
PCIeT_L1
PCIeC_L1
SATACLKT_L
SATACLKC_L
PCIeT_L9/DOTT_96MHzL
PCIeC_L9/DOTC_96MHzL
*PEREQ3#
PEREQ4#*
VttPWR_GD/PD#
REF1/FSLC/TEST_SEL
REF0
JP3901
JP3902
JP3903
JP3904
JP3905
JP3906
T3901
T3902
T3903
T3904
T3905
T3906
T3907
T3908
R3903 10KOhm
R3914 10KOhm
R3907 10KOhm
R3915 10KOhm
R3924 10KOhm
R3961 0Ohm
R3962 0Ohm
R3956 33Ohm
R3957 33Ohm
R3922 2.2KOhm
R3920 33Ohm
R3928 33Ohm
R3933 33Ohm
R3940 33Ohm
R3946 33Ohm
R3951 1KOhm
R3952 270Ohm 1%
R3948 10KOhm
R3950 33Ohm
C3913 33PF/50V
C3915 33PF/50V
C3916 33PF/50V
C3917 33PF/50V
C3919 10PF/50V
C3921 33PF/50V
C3922 33PF/50V
C3920 33PF/50V
C3923 15PF/50V
C3924 15PF/50V
RN3901B 1KOhm
RN3901C 1KOhm
RN3901A 1KOhm
RN3901D 1KOhm
RN3902B 0OHM
RN3902C 0OHM
RN3902A 0OHM
RN3902D 0OHM
MCH_BSEL0
MCH_BSEL1
MCH_BSEL2
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
R3931 1KOhm
R3960 1KOhm
R3932 1KOhm
R3958 1KOhm
R3938 1KOhm
R3959 1KOhm
+VCCP
Reserved for Debug & Experiment
R1.1 081031-3
If don't support NewCard Debug Card ,Pls don't mount R3942
CLK_MCH_SSCLK
CLK_MCH_SSCLK#
CLK_USB48
CLK_48M
CLK_TPMPCI
CLK_DEBUG
CLK_ICHPCI
CLK_KBCPCI
SMB_CLK_S
SMB_DAT_S
CLK_ACC
CLK_DEC#
ITP_EN
SELPCIE0_LCD#
SELLCD_27#
REQ_SEL
FSLA
FSLB
FSLC
CLK_MCH
CLK_MCH#
CLK_CPU
CLK_CPU#
CLK_PCIE7
CLK_PCIE6
CLK_PCIE6#
CLK_PCIE4
CLK_PCIE4#
CLK_PCIE3
CLK_PCIE3#
CLK_PCIE2
CLK_PCIE2#
CLK_PCIE1
CLK_PCIE1#
CLK_SATA
CLK_SATA#
CLK_PCIE9
CLK_PCIE9#
PEREQ3#
PEREQ4#
REF1
REF0
STP_PCI#
STP_CPU#
SATA_CLK_REQ#
/Newcard
/Newcard
ICH_CLKEN
CLK_ICH14
Latched Input Select
ITP_EN/PCICLK_F4
0 = SRC Pair
1 = CPU_ITP Pair
PCICLK0/REQ_SEL
0 = PCICLK0 (INT/PD)
1 = PEREQ#
SELPCIEX0_LCD#/PCICLK3
0 = PCIe9/27M/LCD_SSCG
1 = PCIe0/DOT96 (INT/PU)
SELLCD_27#/PCICLK_F5
0 = 27FIX,SS
1 = LCD (INT/PU)
PEREQ3# control PCIE 2,4
PEREQ4# control PCIE 3,5,7
Latch Select Table
Pin5
Pin9
Pin14/15
Pin17/18
SELPCIEX0_LCD#/ PCI3 = 0 (low)
SELLCD_27#=0
SELLCD_27#=1
PCIEX9
DOT96
27FIX/SS
LCD
SELPCIEX0_LCD#/ PCI3 = 1 (high)
SELLCD_27#=0
SELLCD_27#=1
PCIEX9
DOT96
PCIEX0
PCIEX0
BCLK
PCIE
Spread%
BSEL2
BSEL1
BSEL0
166
100
+/- 0.25
L
H
H
200
100
+/- 0.25
L
H
L
266
100
+/- 0.25
L
L
L
<Variant Name>
Title : CLOCK GEN-ICS9LPR363
ASUSTeK COMPUTER INC. NB1
Engineer: N/A
Size Custom
Project Name F82
Rev 1.2
Date: Tuesday, December 30, 2008
Sheet 39 of 93

SWITCH BUTTON



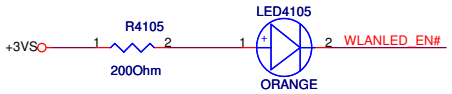
R1.1 081106-1



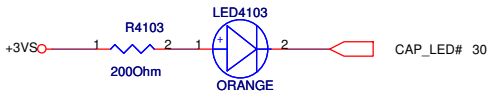


LED

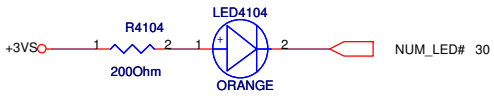
For WireLess LED



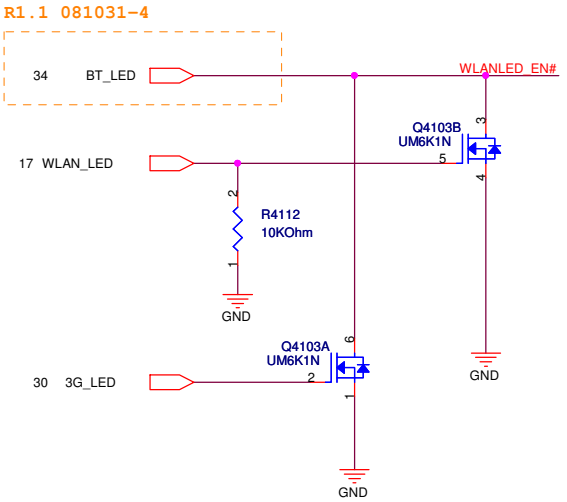
for Cap. Lock



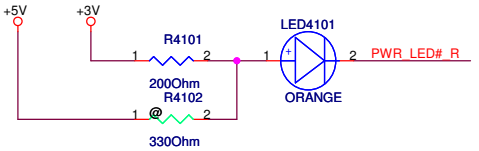
for Num Lock

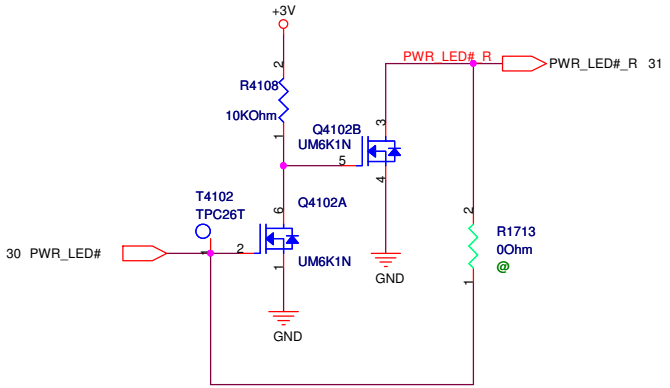


R1.1 081031-4



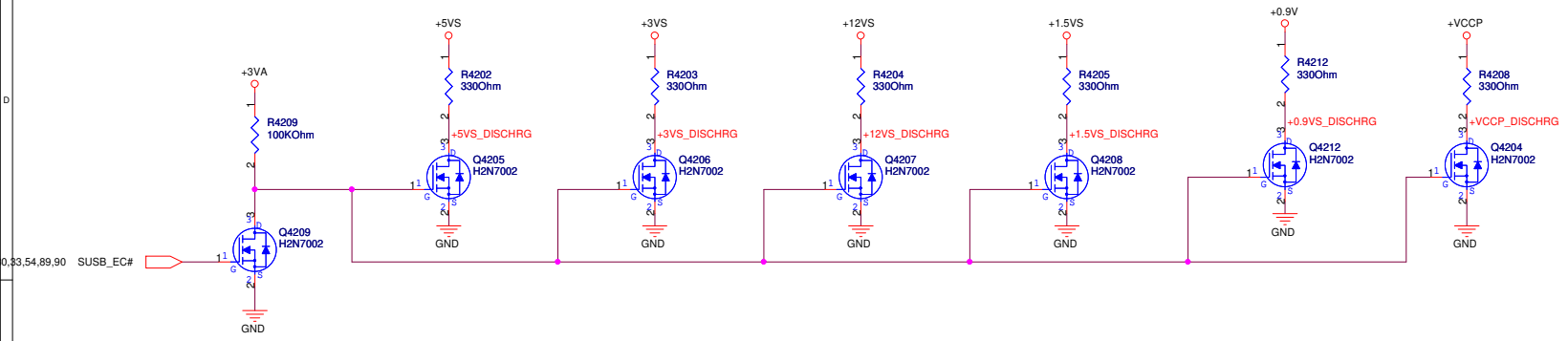
For POWER LED

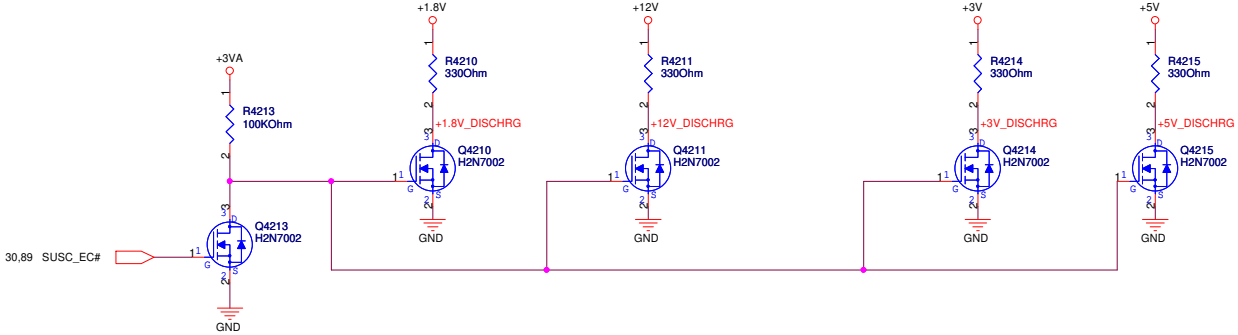




<Variant Name>

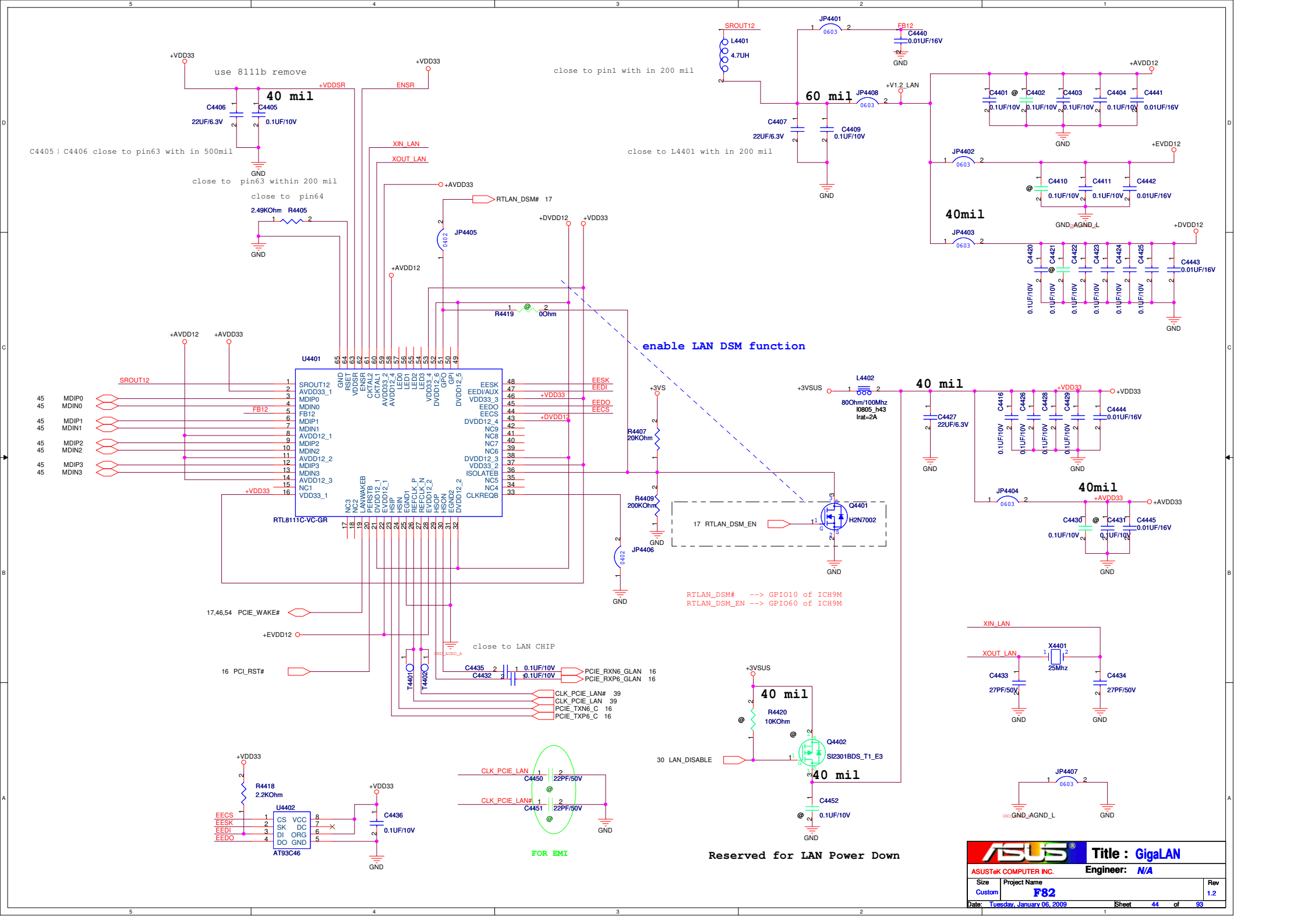
ASUSTeK COMPUTER INC	Title : Switch Button & LED	
	Engineer: N/A	
Size: B	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 41 of 93	





<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE	
	Engineer: N/A	
Size: Custom	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 42 of 93	


use 8111b remove
40 mil
C4406
22UF/6.3V
C4405
0.1UF/10V
C4405) C4406 close to pin63 with in 500mil
close to pin63 within 200 mil
close to pin64
close to pin1 with in 200 mil
close to L4401 with in 200 mil
60 mil
40mil
2.49KOhm R4405
R4419 0Ohm
enable LAN DSM function
RTL8111C-VC-GR
U4401
R4407 20KOhm
R4409 200KOhm
Q4401 H2N7002
RTLAN_DSM# --> GPIO10 of ICH9M
RTLAN_DSM_EN --> GPIO60 of ICH9M
close to LAN CHIP
R4420 10KOhm
Q4402 SI2301BDS_T1_E3
R4418 2.2KOhm
U4402 AT93C46
FOR EMI
Reserved for LAN Power Down
80Ohm/100Mhz
I0805_h43
Irat=2A
X4401 25Mhz
C4433 27PF/50V
C4434 27PF/50V
C4450 22PF/50V
C4451 22PF/50V
C4452 0.1UF/10V
C4435 0.1UF/10V
C4432 0.1UF/10V
C4436 0.1UF/10V
Title : GigaLAN
ASUSTeK COMPUTER INC.
Engineer: N/A
Project Name F82
Size Custom
Rev 1.2
Date: Tuesday, January 06, 2009
Sheet 44 of 93

MDC NUT

H4503 /MDC L5-1A GND

H4504 /MDC L5-1A GND

MDC CONN.

R1.1 081106-2

J4501 /MDC

15,36,56 ACZ_SDOUT_CODEC
15,36,56 ACZ_SYNC_CODEC
15 ACZ_SDIN1
15,36,37,56 ACZ_RST#_CODEC

R4502 2 /MDC 1 33Ohm

GND1 GND2 GND3 GND4 GND5 GND6 NP_NC1 NP_NC2

+3V

ACZ_BCLK_CODEC 15,36

BTOB_CON_12P

C4512 10PF/50V @

/MDC C4502 22PF/50V

/MDC C4501 39PF/50V

LAN CONN.

U4501

44	MDIP0	TCT1 1	TD1+ 2	24 MCT1	L_CMT0
44	MDIN0		TD1- 3	23 MX1+	L_TRLP0
		TCT2 4		22 MX1-	L_TRLM0
44	MDIP1		TD2+ 5	21 MCT2	L_CMT1
44	MDIN1		TD2- 6	20 MX2+	L_TRLP1
		TCT3 7		19 MX2-	L_TRLM1
44	MDIP2		TD3+ 8	18 MCT3	L_CMT2
44	MDIN2		TD3- 9	17 MX3+	L_TRLP2
		TCT4 10		16 MX3-	L_TRLM2
44	MDIP3		TD4+ 11	15 MCT4	L_CMT3
44	MDIN3		TD4- 12	14 MX4+	L_TRLP3
				13 MX4-	L_TRLM3

1GB

C4516 C4520 33PF/50V @ 0.01UF/16V
C4514 C4521 33PF/50V @ 0.01UF/16V
C4513 C4522 33PF/50V @ 0.01UF/16V
C4515 C4523 0.01UF/16V @

MDIP0 +VDD33 MDIP1 D4501 IP4220CZ6 MDIN0 MDIN1 GND

MDIP2 +VDD33 MDIP3 D4502 IP4220CZ6 MDIN2 MDIN3 GND

RN4501A 75Ohm L_CMT0 LAN_GND
RN4501B 75Ohm L_CMT1
RN4501C 75Ohm L_CMT2
RN4501D 75Ohm L_CMT3

C4503 1000PF/2KV GND

J4502 MODULAR_JACK_8P

L_TRLP0 L_TRLM0 L_TRLP1 L_TRLP2 L_TRLM2 L_TRLM1 L_TRLP3 L_TRLM3

P_GND1 NP_NC1 NP_NC2 P_GND2

GND_LAN

JP4501 0603
JP4502 0603

GND_LAN GND

EMI

<Variant Name>

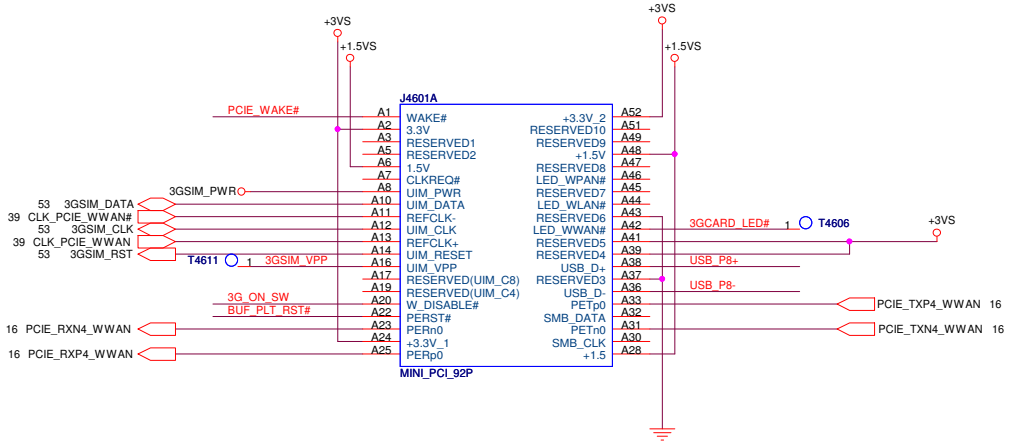
ASUSTeK COMPUTER INC. NB1

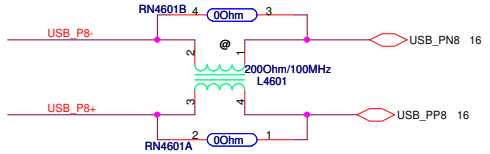
Title : MDC & RJ45+11

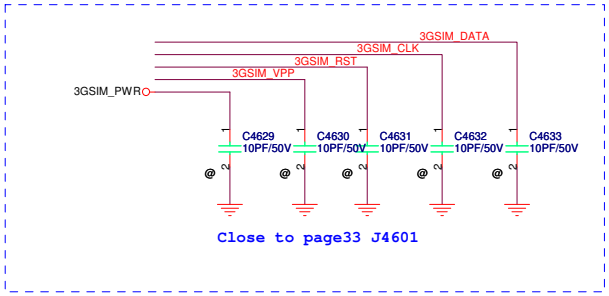
Engineer: N/A

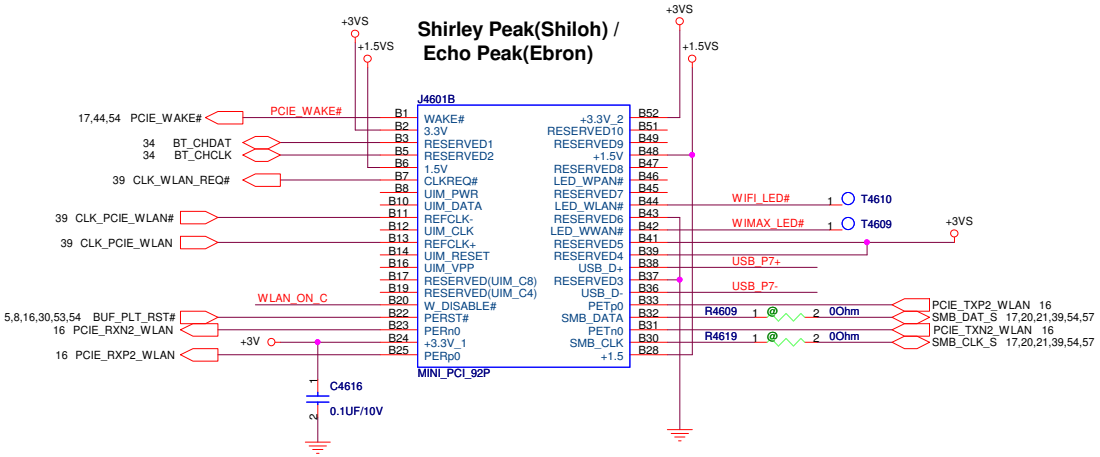
Size	Project Name	Rev
Custom	F82	1.2

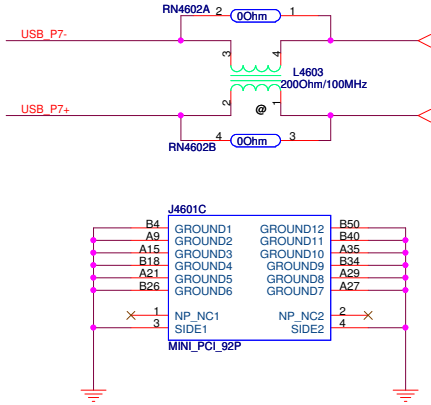
Date: Tuesday, December 30, 2008 Sheet 45 of 93

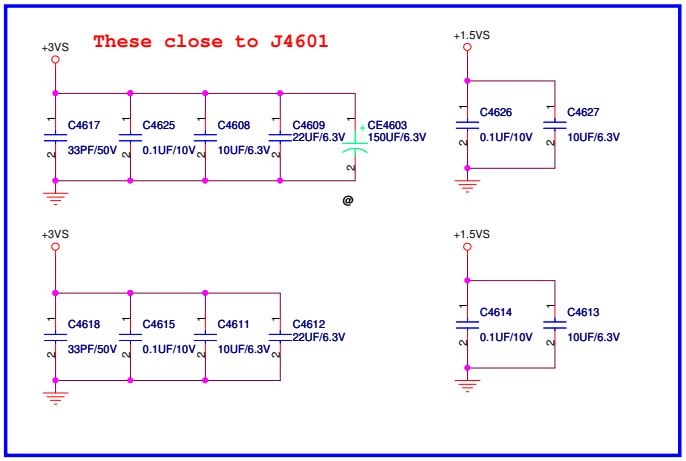


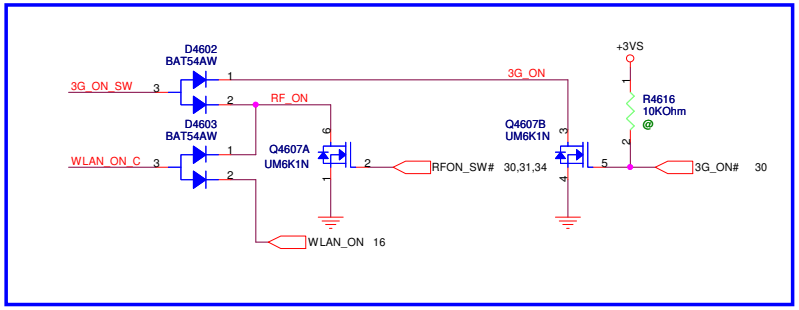


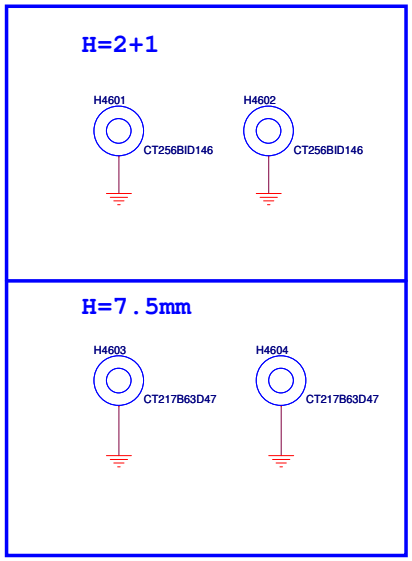












<variant_name>

ASUSTeK COMPUTER INC. NB1

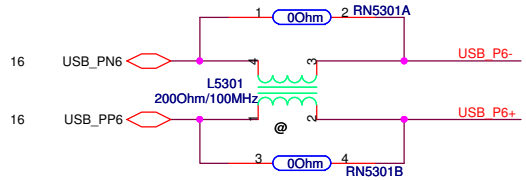
Title : Mini card_WLAN+3G

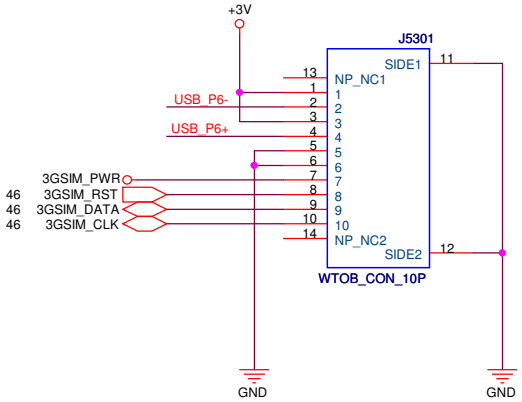
Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 46 of 93

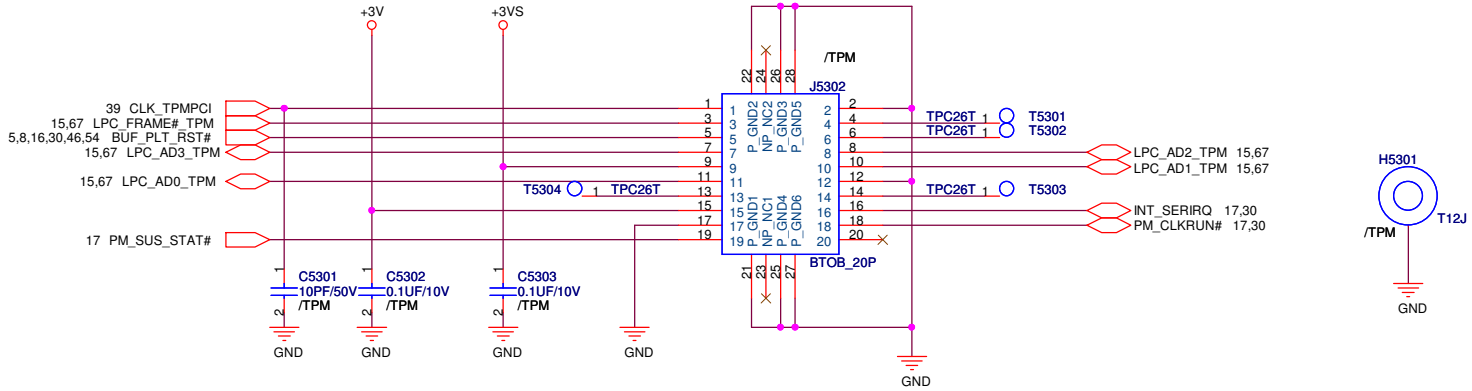
R1.1 081103-1





R1.1 081103-1

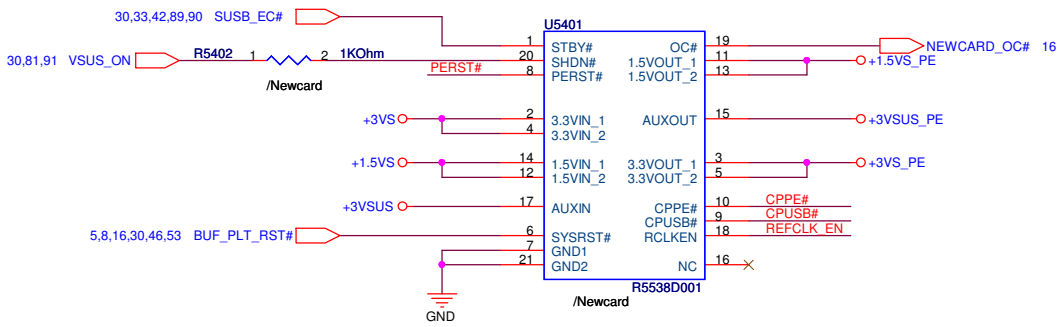
TPM Module CON

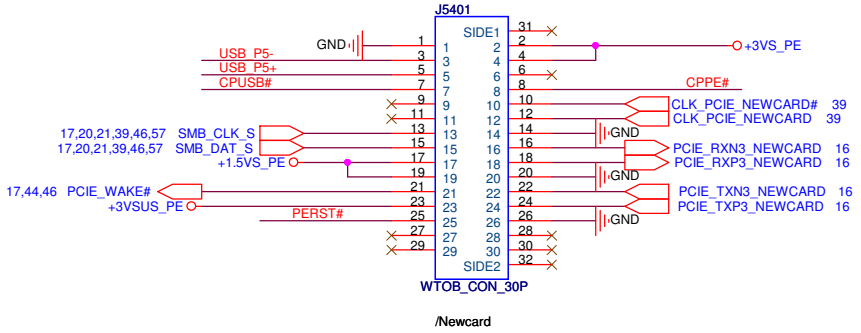


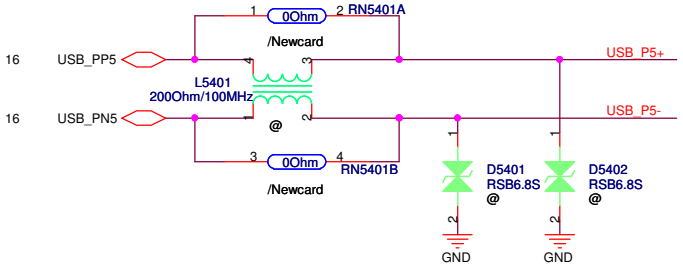
<Variant Name>

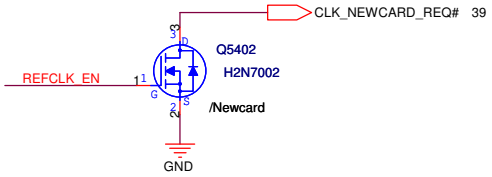
ASUSTeK COMPUTER INC	Title: CardReader & SIM&TPM	
	Engineer: N/A	
Size: B	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 53 of 93	

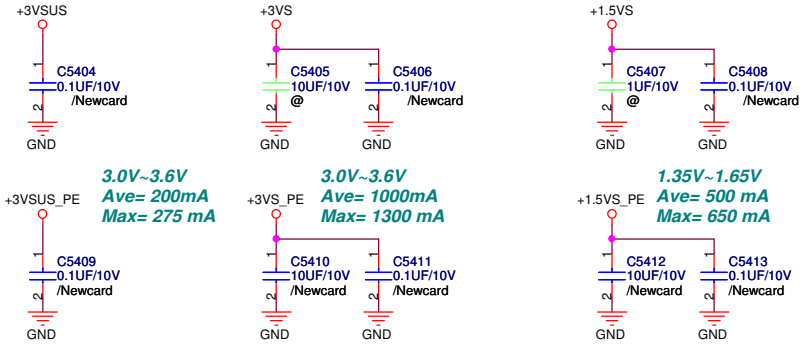
NewCard Connector





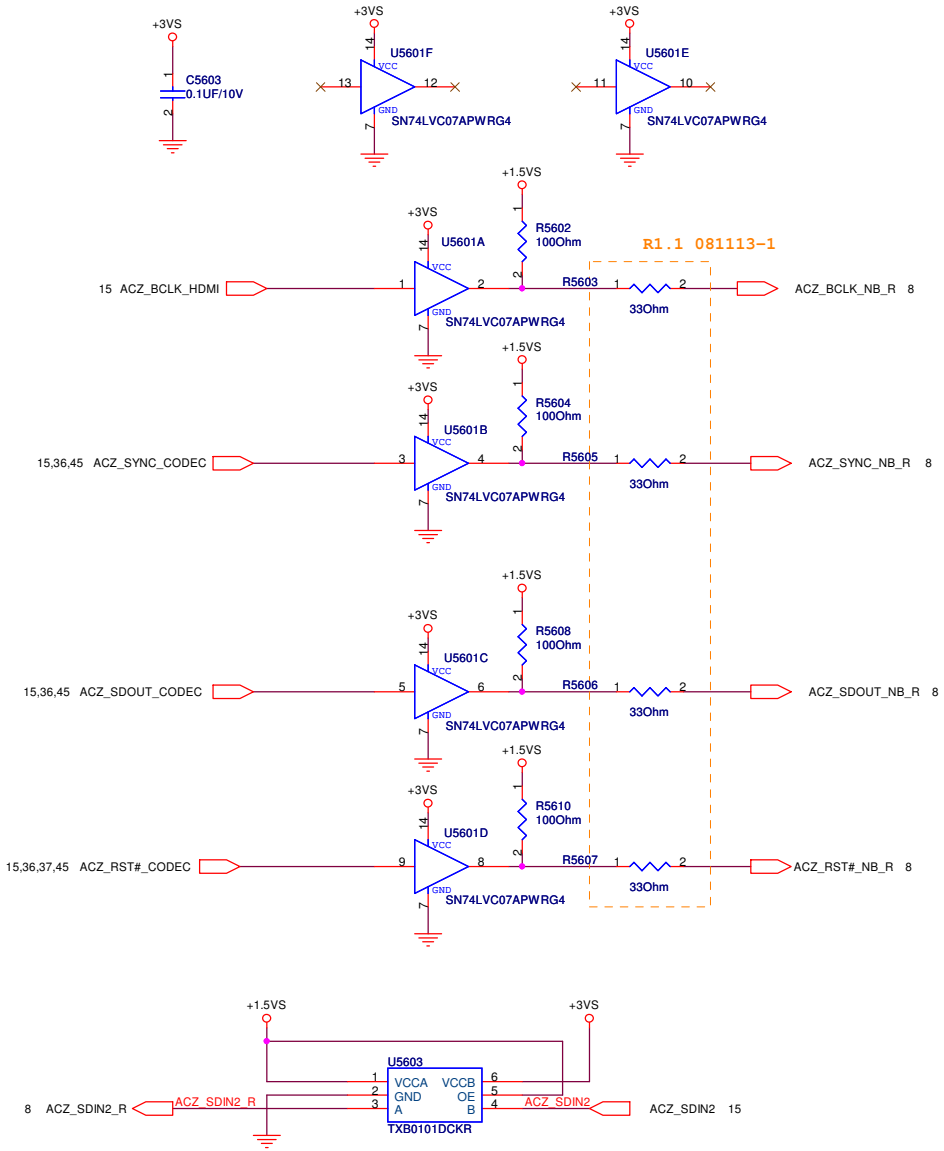






<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : NEWCARD	
	Engineer: N/A	
Size: B	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 54 of 93	



<Variant Name>

ASUSTeK COMPUTER INC. NB1

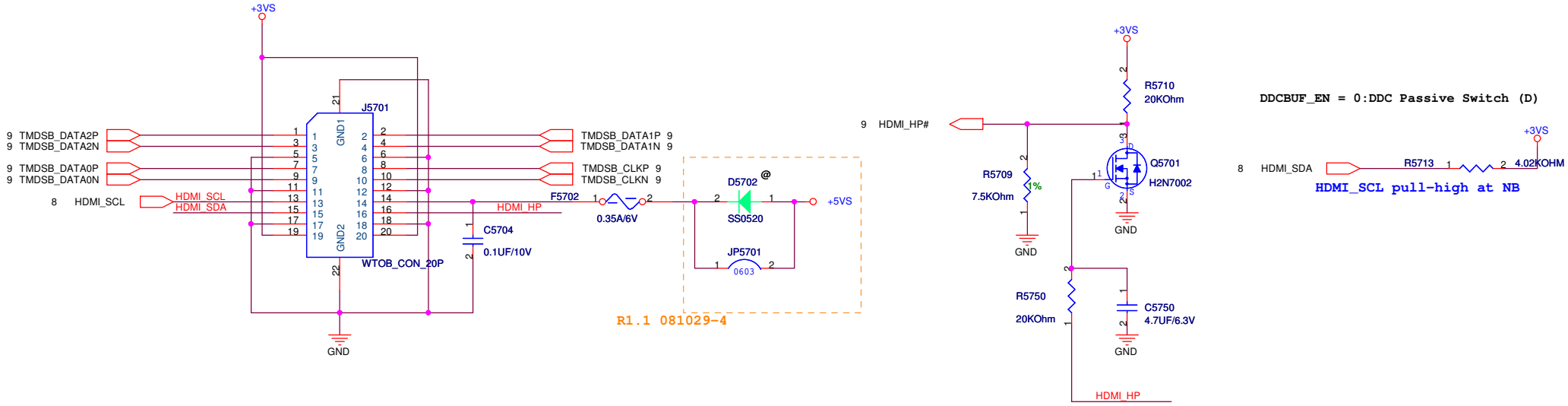
Title : HDA level shifter

Engineer: N/A

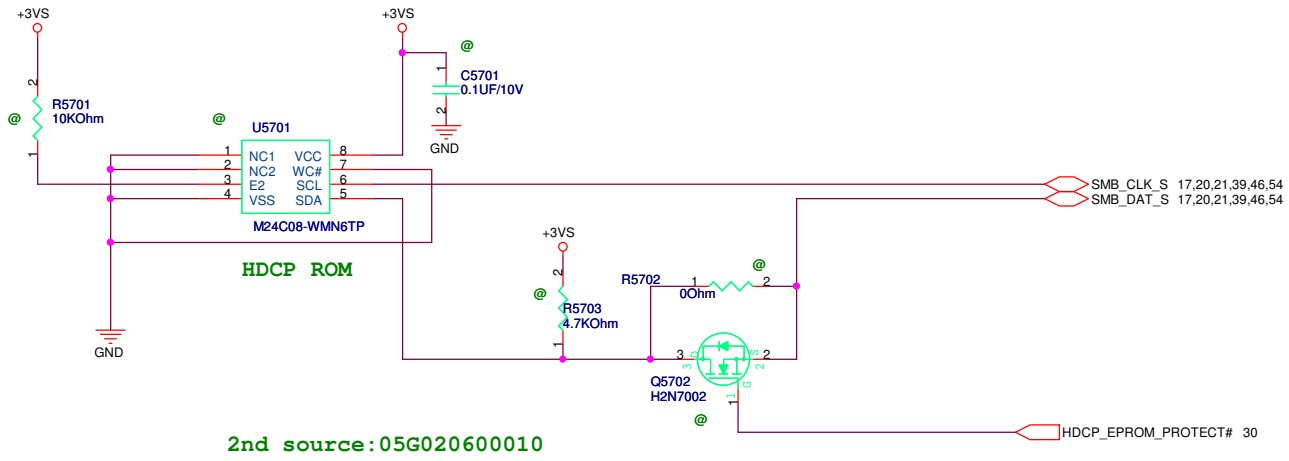
Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 56 of 93

HDMI WtoB Connector



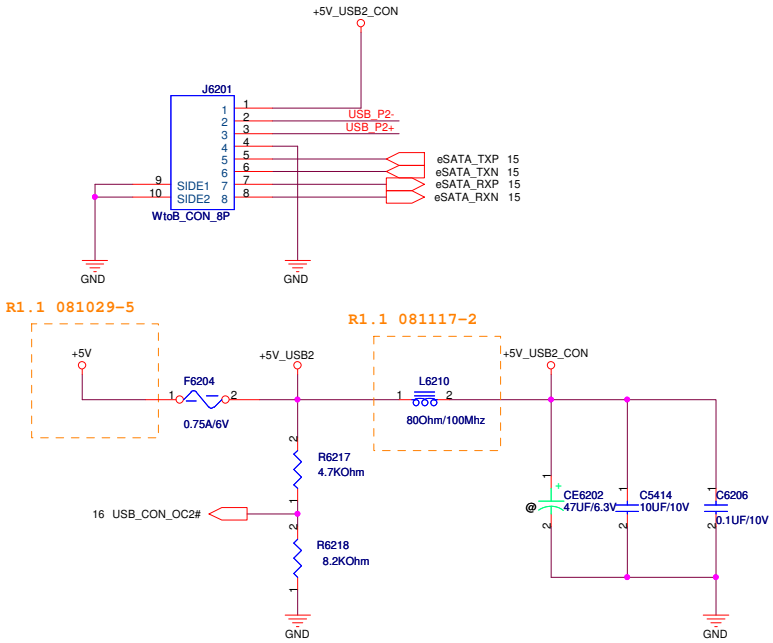
HDCP ROM

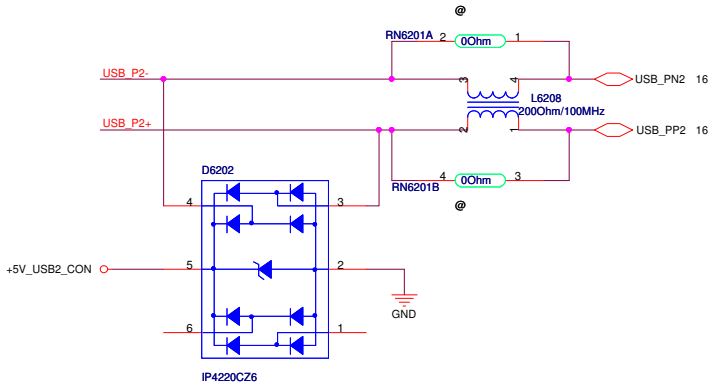


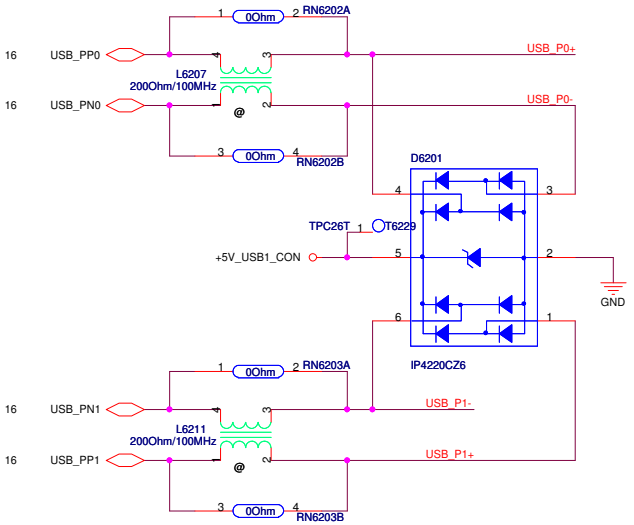
<Variant Name>

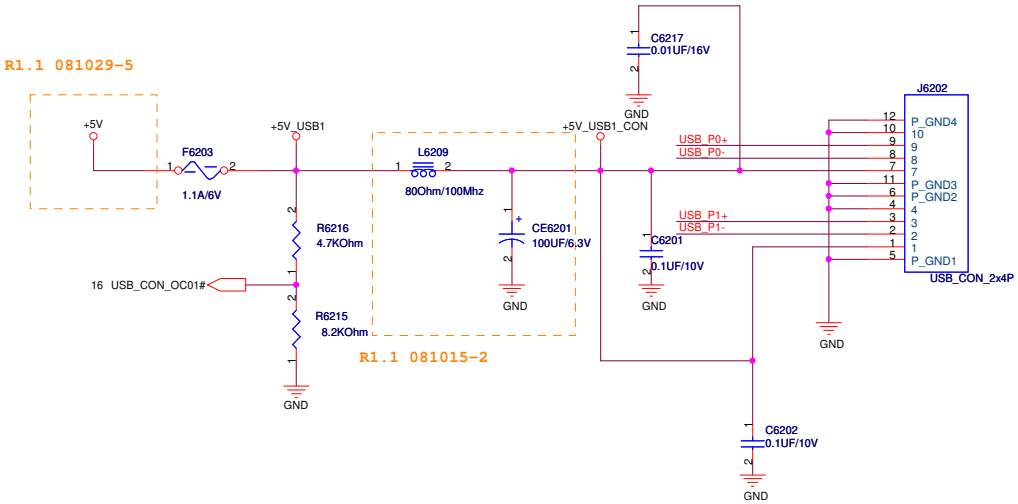
ASUSTeK COMPUTER INC. NB1	Title : iHDMI	
	Engineer: N/A	
Size: B	Project Name	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 57 of 95	

USB IO Board





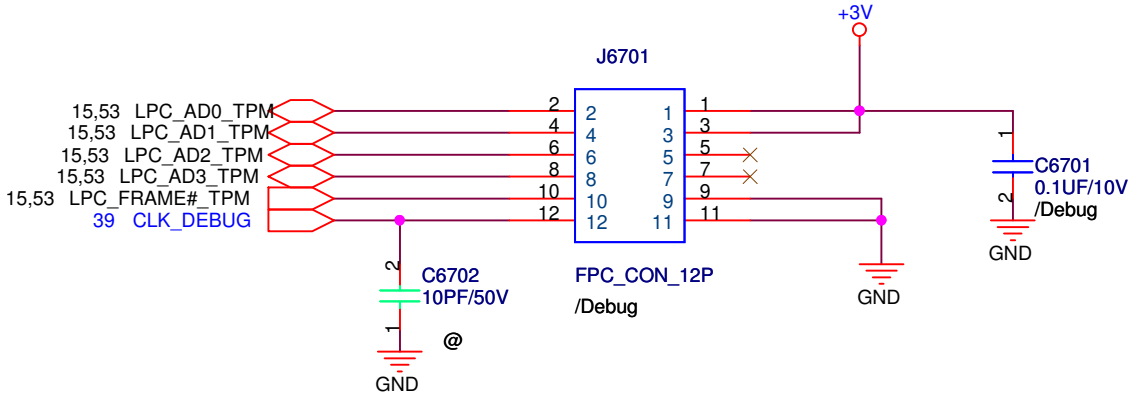




<Variant Name>

ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: N/A	
Size: Custom	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 62 of 93	

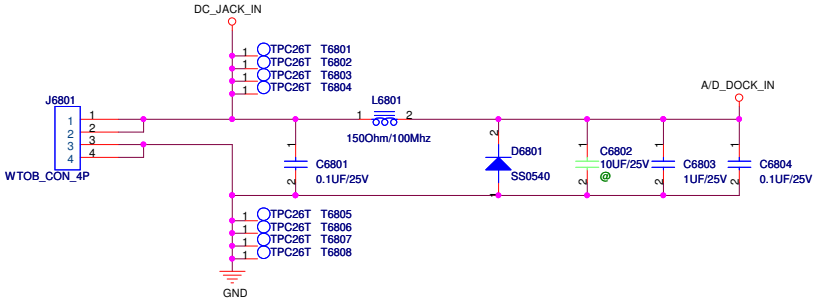
LPC DEBUG PORT



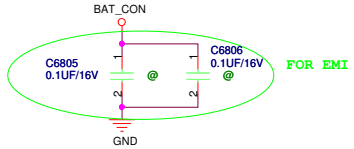
<Variant Name>

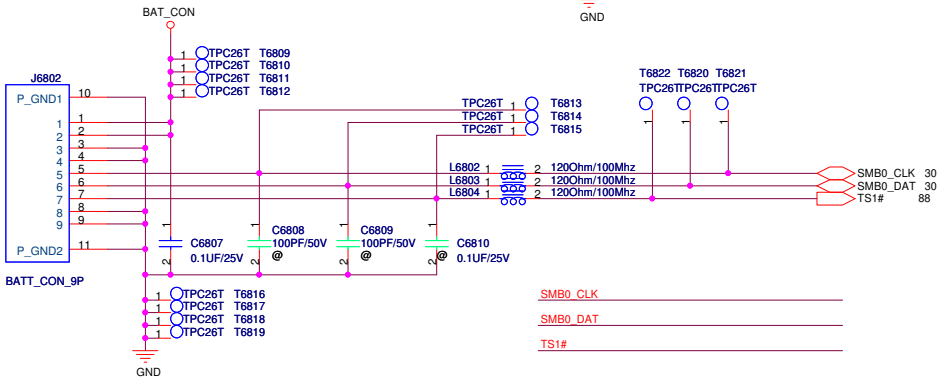
ASUSTeK COMPUTER INC	Title : DEBUG CONN	
	Engineer: N/A	
Size: A	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 67 of 93	

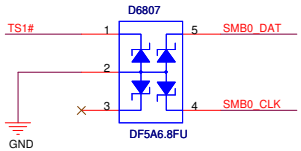
DC IN



BAT IN

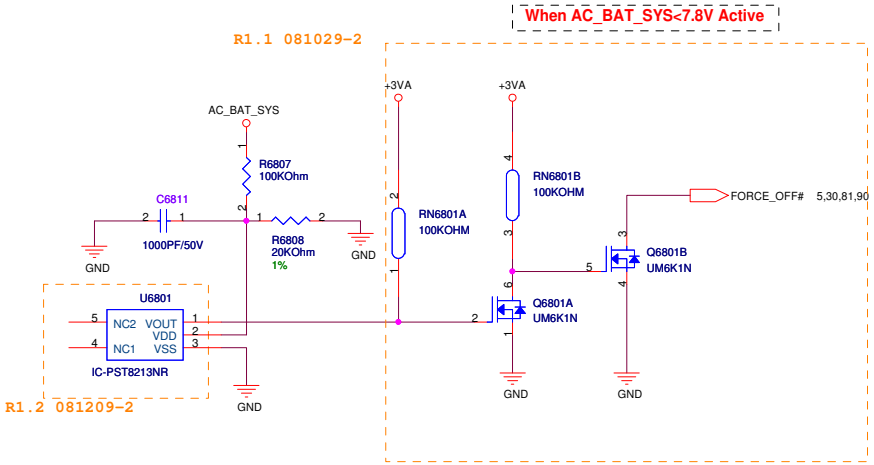






Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

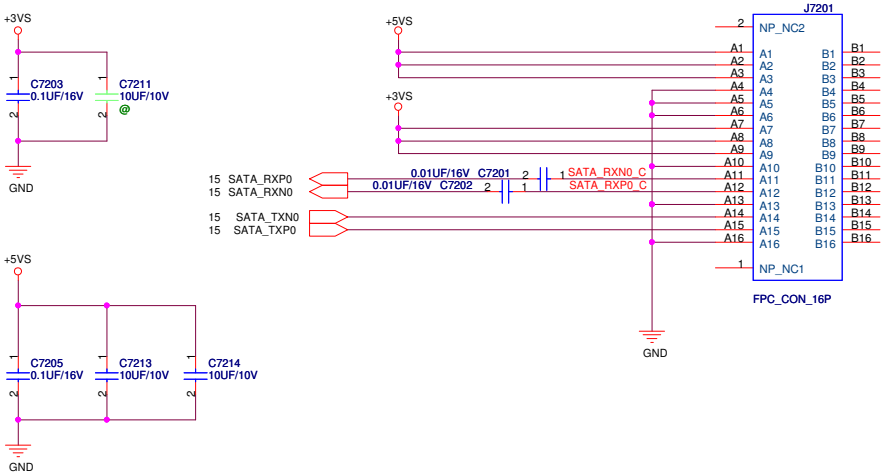
Without Battery & Pull out Adapter



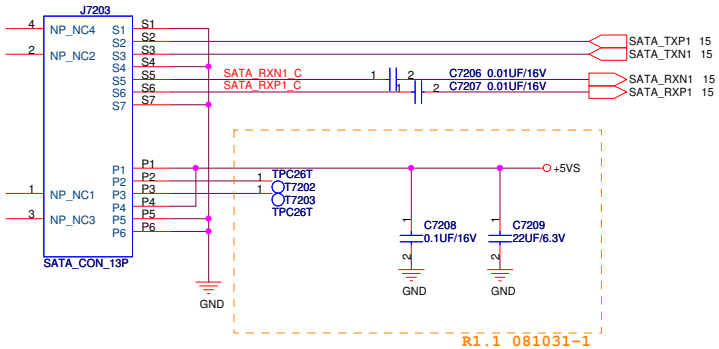
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN	
	Engineer: N/A	
Size: Custom	Project Name: F82	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 68 of 93	

SATA HDD-1



ODD



<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : SATA-HDD & ODD

Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 72 of 93

Hole-A

H7401
C71D71N

Hole-B

H7402
HOLE_NPTH

H7403
HOLE_NPTH

H7404
HOLE_NPTH

Hole-C

H7405
O83X71DO83X71N

Hole-D

H7409
CT276CB197ID138

H7410
CT276CB197ID138

H7411
CT276CB197ID138

H7412
CT276CB197ID138

GND

Hole-E

H7414
CT256B315D91N

H7406
CT256B315D91N

H7407
CT256B315D91N

H7408
CT256B315D91N

GND

H7416
CT256B315D91N

GND_AUDIO

Hole-F

H7417
CT256B220D91N

H7420
CT256B220D91N

GND

H7418
CRT266X256D91N

GND

H7419
RT335X305D91N

GND

H7421
CT256B220D91N

H7422
CT256B220D91N

H7413
CT256B220D91N

H7415
CT256B220D91N

GND

Spring

S7401
EMI_SPRING_PAD

S7402
EMI_SPRING_PAD

GND

GND

<Variant Name>

Title : Hole

ASUSTeK COMPUTER INC

Engineer: Leon Guo

Size	Project Name	Rev
B	F82	1.2

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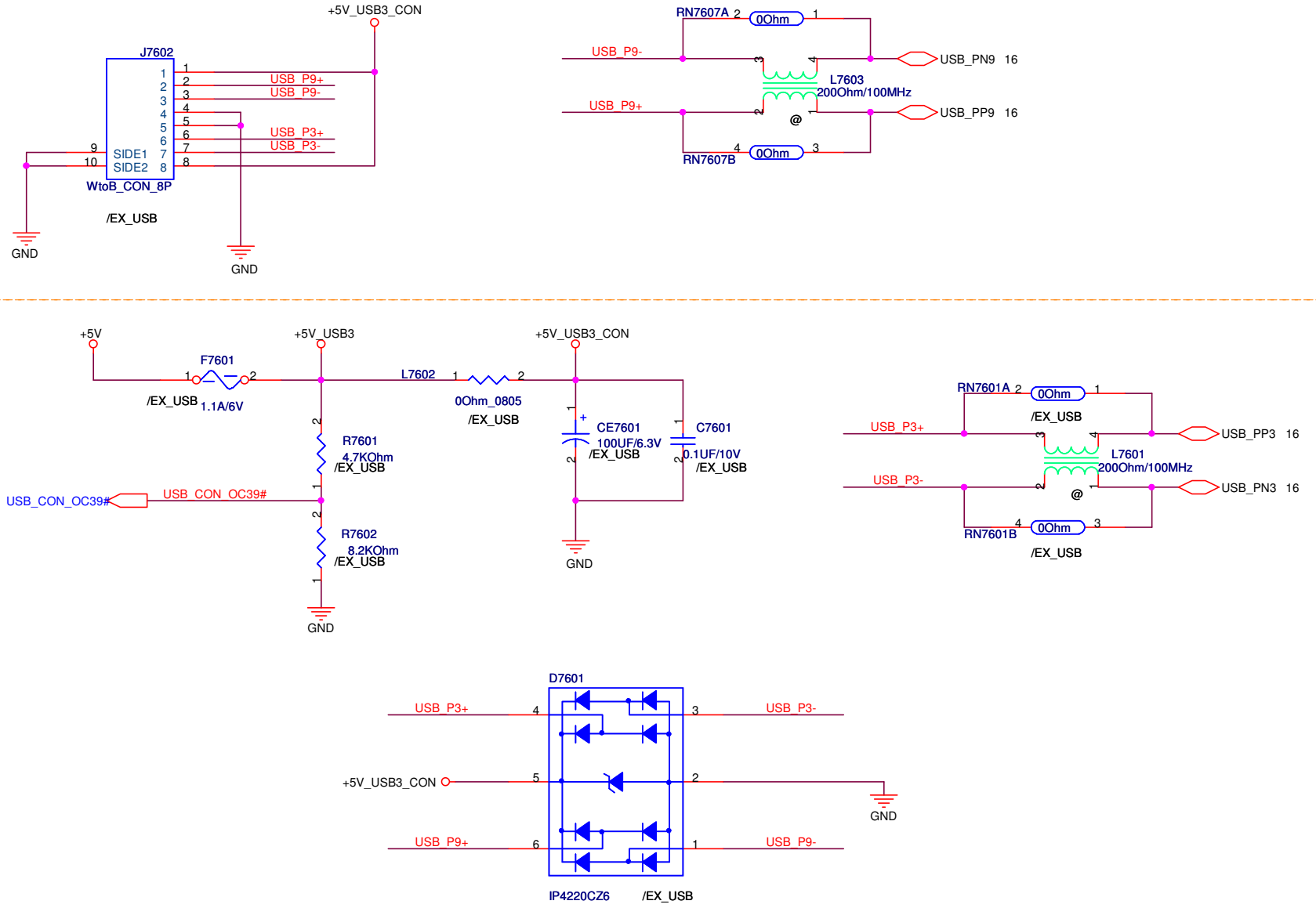
EXPRESS GATE CONN R1.1 081015-1



<Variant Name>

ASUSTeK COMPUTER INC

Title : EX_USB*2

Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 76 of 93

R1.1 081015-1 Reserve USB port on ExpressGate connector page16/76
R1.1 081015-2 Move CE6201 after bead(L6209) page62
R1.1 081021-1 Change pin2 from +3VS to +3V page53
R1.1 081028-1 Change +3VS to +3VA_EC page30
R1.1 081029-1 Reserve ESD diode for ADJ_BL_CON page33
R1.1 081029-2 Add Q6801 to improve discharge speed of FORCE_OFF# page68
R1.1 081029-3 Add R1537 to separate ACZ_BCLK page15
R1.1 081029-4 Add 0 ohm(R5704) page57
R1.1 081029-5 Del USB power switch page62
R1.1 081031-1 Swap ODD power(pin number is disorder) page72
R1.1 081031-2 Change +5VSUS to +3VSUS(Charge LED) page31
R1.1 081031-3 Change CLK_ICHPCI from pin64 to pin9.(Can't stop by STP_PCI#) page39
R1.1 081031-4 Add BT_LED to RF LED page34/41
R1.1 081105-1 Del CHG_EN#,PRECHG,BATSEL_2P# / Add ISET_EC,VSET_EC page30
R1.1 081106-1 Change Switch for ME request page41
R1.1 081106-2 Change MDC/Nut height to 5mm for ME request page45
R1.1 081106-4 Reserve for dynamic change Vcore page30
R1.1 081106-5 Change link after R1723 page17
R1.1 081106-6 Reserve for power sequence page17
R1.1 081111-1 Del reserve common chork page62
R1.1 081113-1 Add Damping R page56
R1.1 081113-2 Cost down, change LVDS connector to 30pin page33
R1.1 081114-1 Del PM_EXTTS#_0 connected to DDR slot page08/15
R1.1 081114-2 For EMI request page20
R1.1 081117-1 Add R0501 & R0502 for ATS page5
R1.1 081117-2 Add L6201 for EMI request page62
R1.1 081117-3 Add C3808 for EMI request page38
R1.1 081118-1 Change 83nH to 47nH page32
R1.1 081118-2 Reserve Cap for EMI request page17/33
R1.2 081202-1 Change to 40 pin connecotor and add 2nd LVDS page09/33
R1.2 081209-1 Add Buffer on HSYNC/VSYNC page32
R1.2 081209-2 Change Reset IC to new version page68
R1.2 081217-1 Change LAN_DISABLE from pin35 to pin118 of EC page30

<Variant Name>

ASUSTeK COMPUTER INC

Title : SPRING_PAD

Engineer: N/A

Size	Project Name	Rev
Custom	F82	1.2

Date: Tuesday, December 30, 2008 Sheet 77 of 93

IMON=Gm(IMON) * [(Vcsp1-Vcsn1) + (Vcsp2-Vcsn2)]

RIMON = 0.9V / [IMAX * Rsense(MIN) * Gm(IMON_MIN)]

Gm(IMON) = 2.4mS , Gm(IMON_MIN) = 2.36mS

Close to Phase 1 Low_side MOSFET

RIMON

RFB

Tsw = 16.3pF * (RTON +6.5K)

RFB = Rdroop / [(DCR*0.8) * Gm]

Gm = 600uS , R8022 for load lin

CNT1	CNT2	VID (1.05V)
1	0	VID+100mV
0	1	VID-100mV
0	0	VID

Voffset = [(R1/R2) * Vid] + [(R1/R2) * Vp]

R1 = R8020 , R2 = R8047 or R8048 , Vp = 3.3V or GND

New loadline = {Rfb + [(R1/R2) * Rfb] + R1} * Gm * (DCR*0.8)

Close to Phase 2 Inductor

Close to Phase 1 Inductor

DCR = 1.1m OHM

(10/14/08)

(09/30/08)

(44A)

+VCORE

<Variant Name>

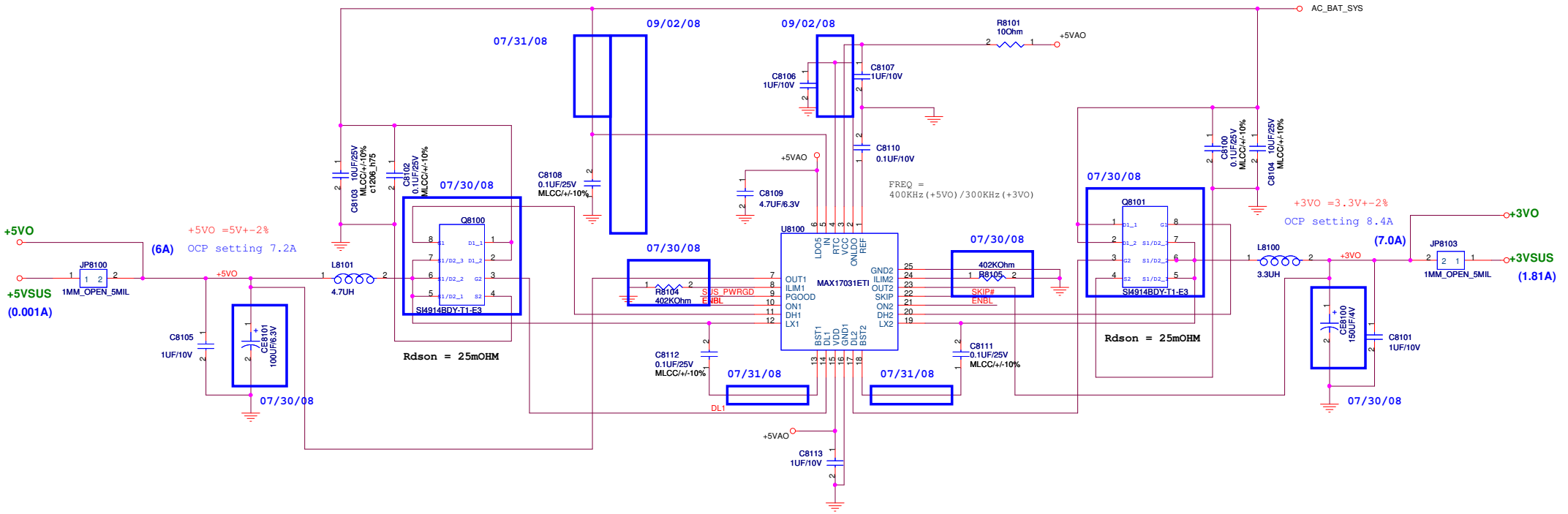
Title : POWER_VCORE

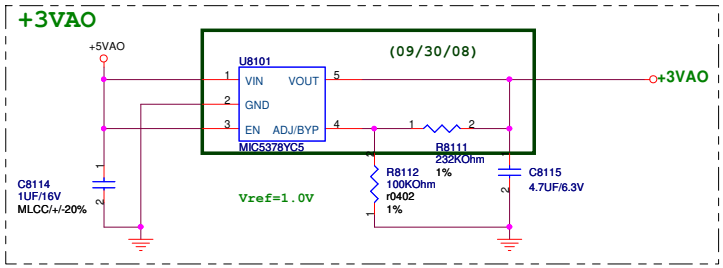
ASUSTeK COMPUTER INC. NB

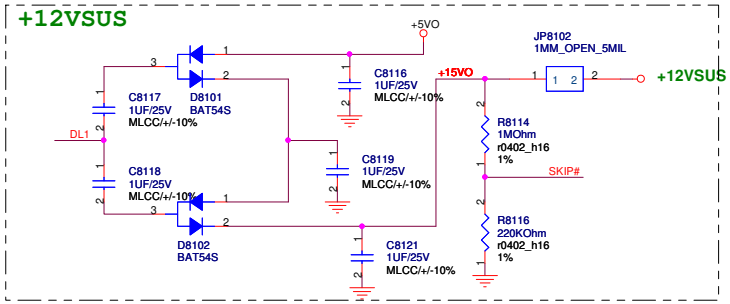
Engineer: Adams

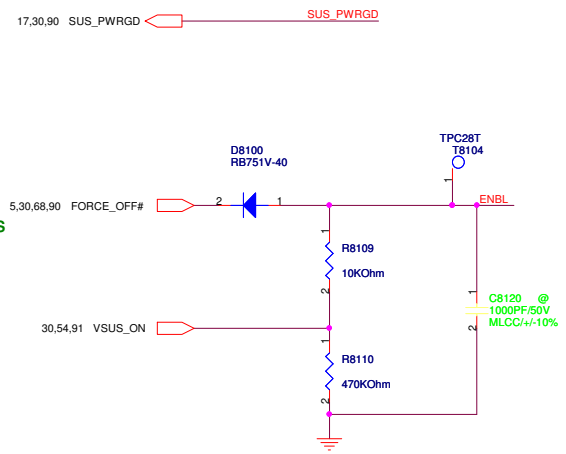
Size: Custom | Project Name | Rev: 1.2

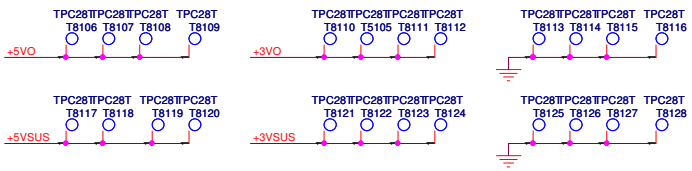
Date: Tuesday, December 30, 2008 | Sheet 80 of 93











<variant_name>

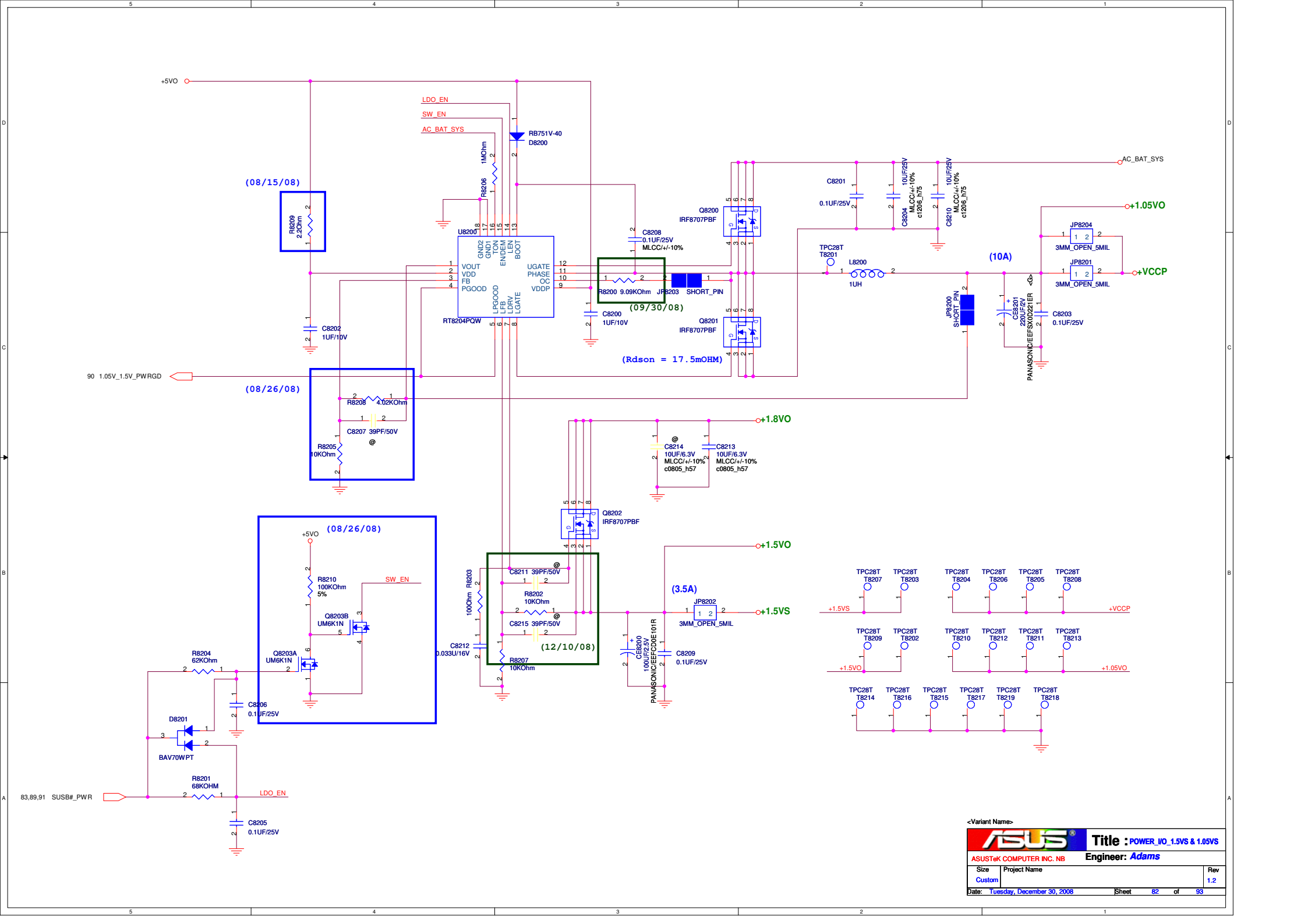
ASUSTeK COMPUTER INC. NB

Title : POWER_SYSTEM

Engineer: Adams

Size	Project Name	Rev
Custom		1.2

Date: Tuesday, December 30, 2008 Sheet 81 of 93


+5VO
LDO_EN
SW_EN
AC_BAT_SYS
RB751V-40
D8200
1MOhm
R8206
(08/15/08)
R8209
2.2Ohm
U8200
RT8204PQW
VOUT
VDD
FB
PGOOD
GND2
GND1
TON
ENDEM
LEN
BOOT
UGATE
PHASE
OC
VDDP
LPGOOD
LFB
LDRV
LGATE
C8202
1UF/10V
C8208
0.1UF/25V
MLCC/+/-10%
R8200 9.09KOhm
JP8203
SHORT_PIN
(09/30/08)
C8200
1UF/10V
Q8200
IRF8707PBF
Q8201
IRF8707PBF
(Rdson = 17.5mOHM)
C8201
0.1UF/25V
C8204
10UF/25V
MLCC/+/-10%
c1206_h75
C8210
10UF/25V
MLCC/+/-10%
c1206_h75
AC_BAT_SYS
+1.05VO
TPC28T
T8201
L8200
1UH
(10A)
JP8204
3MM_OPEN_5MIL
JP8201
3MM_OPEN_5MIL
+VCCP
JP8200
SHORT_PIN
CB8201
220UF/2V
PANASONIC/EEFSX0D221ER
C8203
0.1UF/25V
90 1.05V_1.5V_PWRGD
(08/26/08)
R8208
4.02KOhm
C8207 39PF/50V
@
R8205
10KOhm
+1.8VO
@
C8214
10UF/6.3V
MLCC/+/-10%
c0805_h57
C8213
10UF/6.3V
MLCC/+/-10%
c0805_h57
Q8202
IRF8707PBF
+1.5VO
(08/26/08)
+5VO
R8210
100KOhm
5%
SW_EN
Q8203B
UM6K1N
R8204
62KOhm
Q8203A
UM6K1N
C8206
0.1UF/25V
D8201
BAV70WPT
R8201
68KOHM
83,89,91 SUSB#_PWR
LDO_EN
C8205
0.1UF/25V
100Ohm R8203
C8211 39PF/50V
@
R8202
10KOhm
C8215 39PF/50V
@
(12/10/08)
C8212
0.033U/16V
R8207
10KOhm
(3.5A)
JP8202
3MM_OPEN_5MIL
+1.5VS
CE8200
100UF/2.5V
PANASONIC/EEFCD0E101R
C8209
0.1UF/25V
TPC28T T8207
TPC28T T8203
TPC28T T8204
TPC28T T8206
TPC28T T8205
TPC28T T8208
TPC28T T8209
TPC28T T8202
TPC28T T8210
TPC28T T8212
TPC28T T8211
TPC28T T8213
TPC28T T8214
TPC28T T8216
TPC28T T8215
TPC28T T8217
TPC28T T8219
TPC28T T8218
<Variant Name>
Title : POWER_I/O_1.5VS & 1.05VS
ASUSTeK COMPUTER INC. NB
Engineer: Adams
Size Custom
Project Name
Rev 1.2
Date: Tuesday, December 30, 2008
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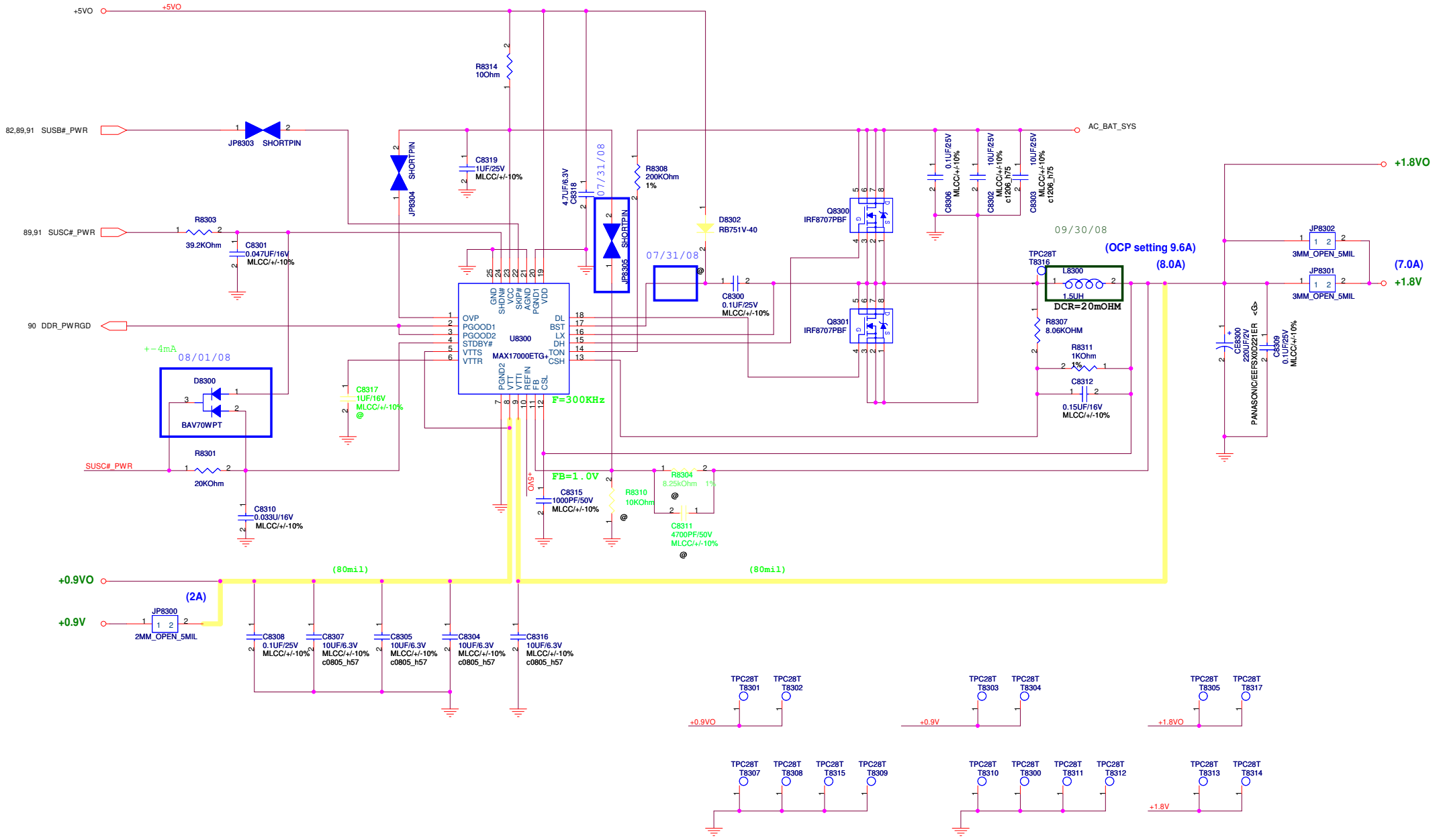

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_DDR_VTT

Engineer: Adams

Size	Project Name	Rev
Custom		1.2

Date: Tuesday, December 30, 2008 Sheet 83 of 93

<Variant Name>

Title : POWER_I/O

ASUSTeK COMPUTER INC. NB

Engineer: Adams

Size	Project Name	Rev
Custom		1.2

Date: Tuesday, December 30, 2008 Sheet 84 of 93

<Variant Name>

Title : POWER_VGA_CORE&1.1VS

ASUSTeK COMPUTER INC. NB

Engineer: Adams

Size	Project Name	Rev
C		1.2

Date: Tuesday, December 30, 2008 Sheet 85 of 93

<Variant Name>

Title : POWER_MCH_CORE

ASUSTeK COMPUTER INC. NB

Engineer: Adams

Size	Project Name	Rev
C		1.2

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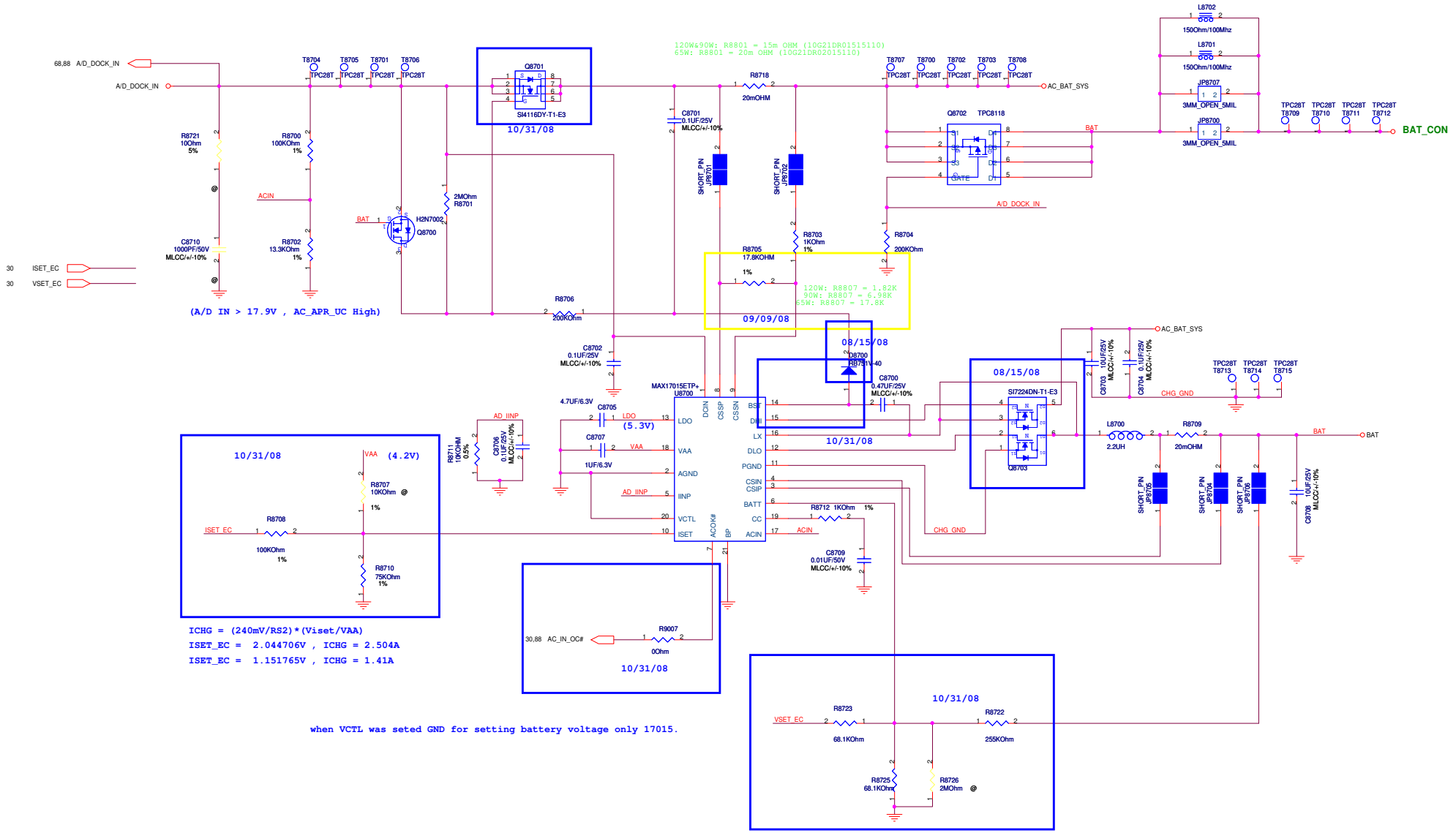
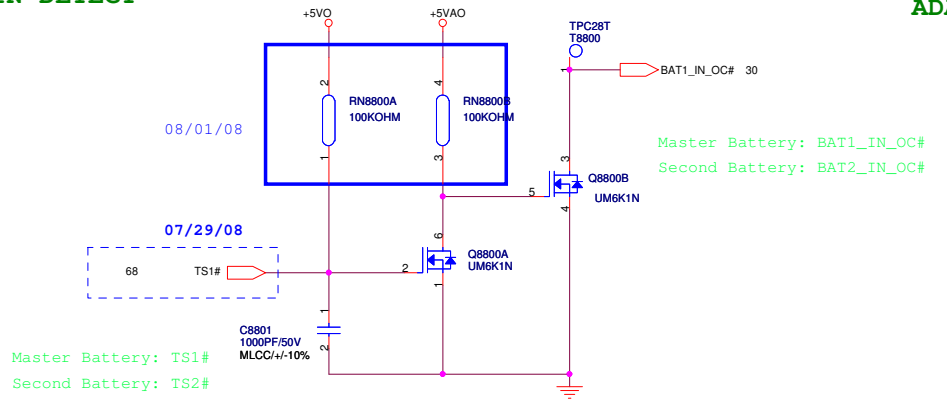


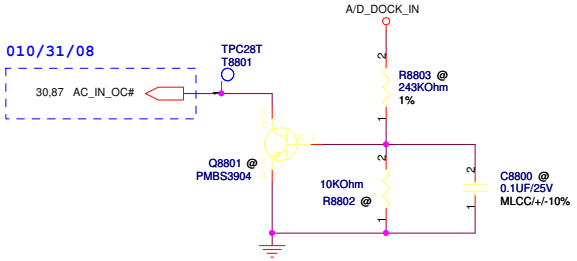
<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_CHARGER	
	Engineer: Adams	
Size: C	Project Name	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 87 of 93	

BATTERY IN DETECT



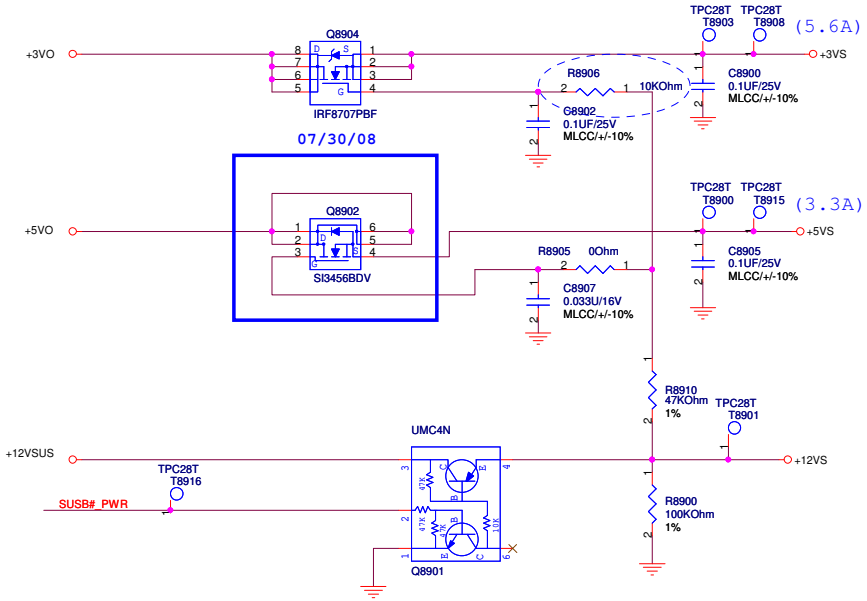
ADAPTER IN DETECT



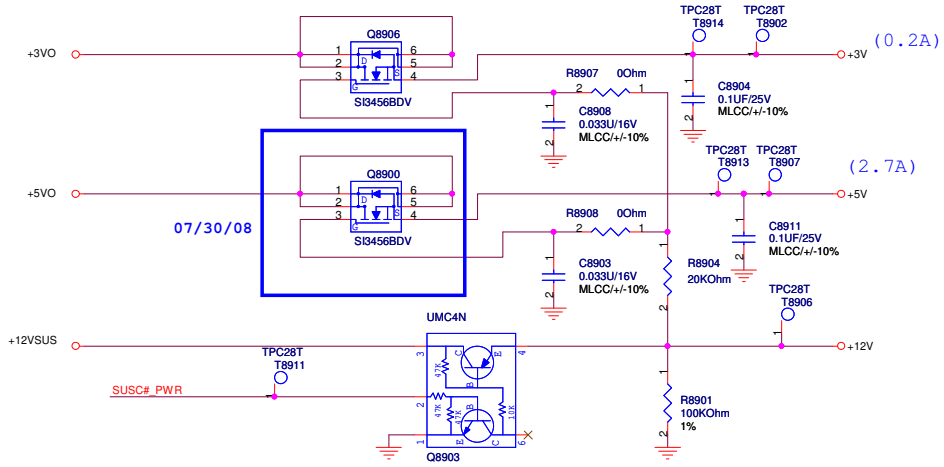
<Variant Name>

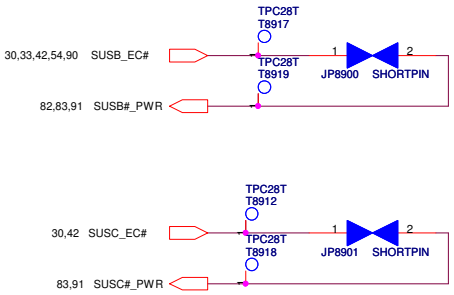
ASUSTeK COMPUTER INC. NB	Title : POWER_DETECT	
	Engineer: Adams	
Size: Custom	Project Name	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 88 of 93	

SUSB#_PWR POWER



SUSC#_PWR POWER





<Variant Name>

Title : POWER_LOADSWITCH

ASUSTeK COMPUTER INC. NB

Engineer: Adams

Size	Project Name	Rev
Custom		1.2

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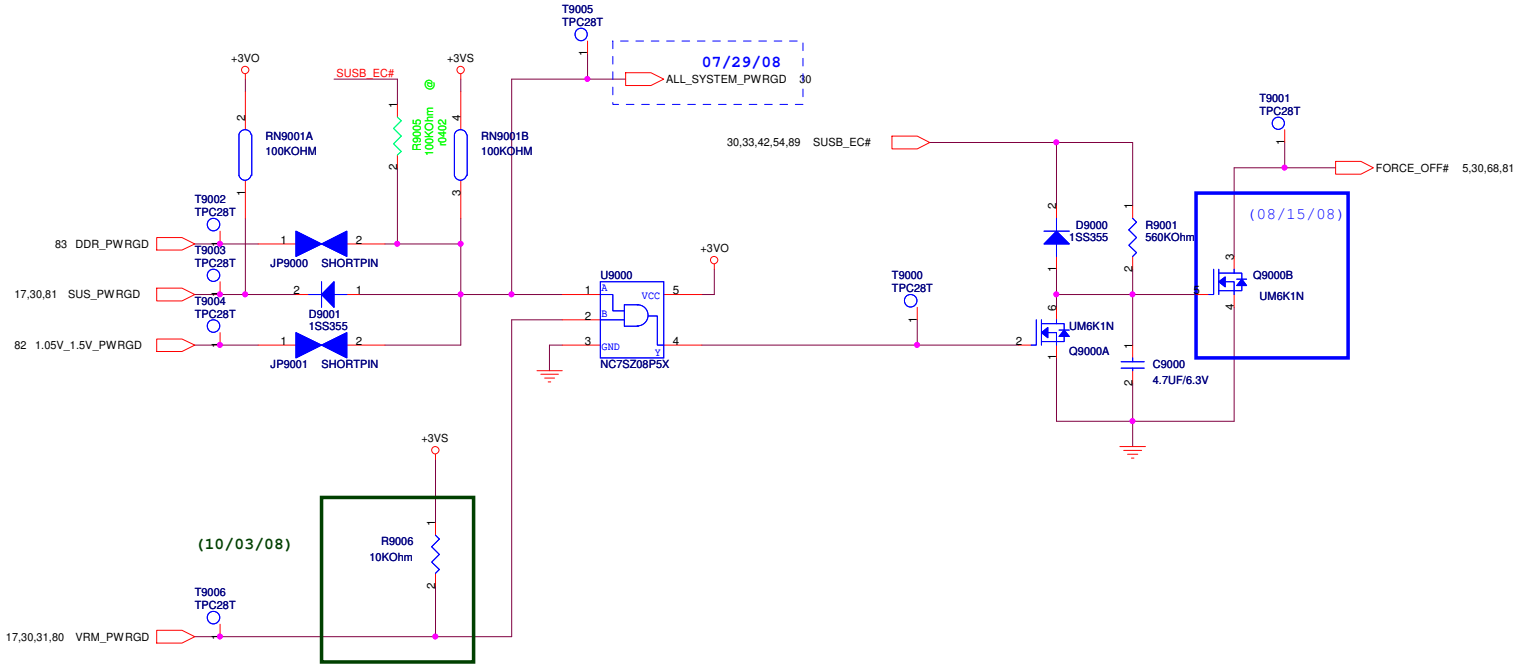
POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_PROTECT	
	Engineer: Adams	
Size: Custom	Project Name	Rev: 1.2
Date: Tuesday, December 30, 2008	Sheet 90 of 93	

AC_BAT_SYS → AC_BAT_SYS 31,33,68,80,81,82,83,87

BAT → BAT 87

BAT_CON → BAT_CON 68,87

+3VAO → +3VAO 81

+3VA → +3VA 15,30,33,42,68,81

+5VAO → +5VAO 81,88

+5VO → +5VO 81,82,83,88,89

+3VO → +3VO 81,89,90

+1.8VO → +1.8VO 82,83

+0.9VO → +0.9VO 83

+1.05VO → +1.05VO 82

+1.5VO → +1.5VO 82

+5VSUS → +5VSUS 18,81

+5VSUS → +5VSUS 18,81

+3VSUS → +3VSUS 15,16,17,18,30,31,44,54,81

+12VSUS → +12VSUS 81,89

+5V → +5V 33,41,42,62,76,89

+3V → +3V 31,33,34,41,42,45,46,53,67,89

+12V → +12V 42,89

+1.8V → +1.8V 8,11,12,20,21,42,83

+0.9V → +0.9V 22,42,83

+3VS → +3VS 4,8,9,12,15,16,17,18,20,21,30,31,32,33,36,37,38,39,41,42,44,46,53,54,56,57,72,80,89,90

+5VS → +5VS 17,18,31,32,36,38,42,57,72,80,89

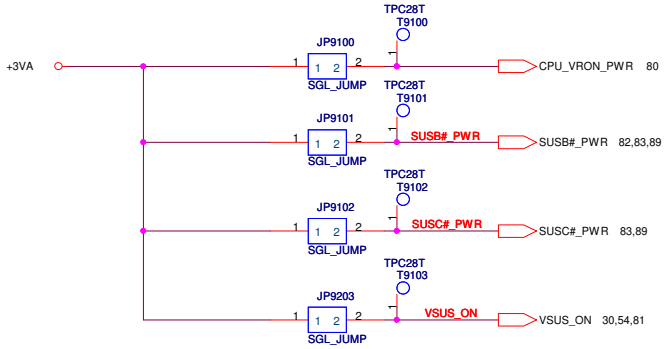
+12VS → +12VS 33,42,89

+1.5VS → +1.5VS 5,12,18,42,46,54,56,82

+VCCP → +VCCP 4,5,7,8,9,11,12,15,18,39,42,82

+VCORE → +VCORE 5,80

FOR POWER TEST



<Variant Name>

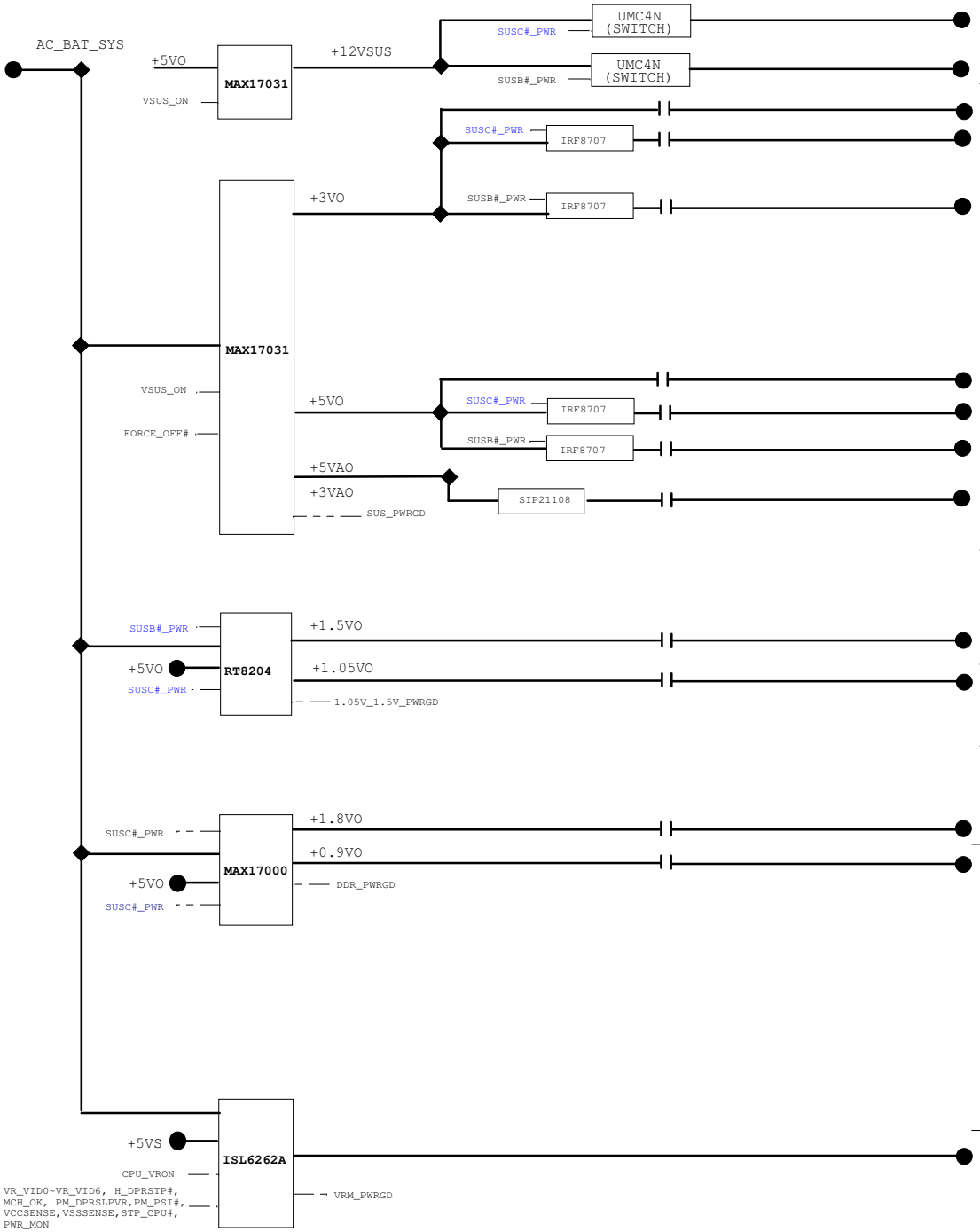
ASUSTeK COMPUTER INC. NB

Title : POWER_SINGAL

Engineer: Adams

Size	Project Name	Rev
Custom		1.2

Date: Tuesday, December 30, 2008 Sheet 91 of 93



	Spec rating	Design rating
+12V	(10mA)	
+12VS	(10mA)	
+3VSUS	(1.04A)	
+3V	(0.3A)	
+3VS	(5.6A)	OCP Setting 7.2A
+5VSUS	(0.03A)	
+5V	(2.7A)	
+5VS	(3.3A)	OCP Setting 7.2A
+3VA	(0.02A)	
+1.5VS	(3.5A)	OCP Setting 5A
+VCCP	(10A)	OCP Setting 12A
+1.8V	(8A)	OCP Setting 9.6A
+0.9V	(1A)	(2A)
+VCORE	(44A)	

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_FLOWCHART

Engineer: Adams

Size	Project Name	Rev
Custom		1.2

Date: Tuesday, December 30, 2008 Sheet 92 of 93

(08/15/08)

1. Q8706B rename to Q8704B .
2. Q9002 rename to Q8703 .
3. Q8203 rename to R8209 .
4. U8000 change from ISL6262A to ISL6266A .
5. Change R8015 from 255 OHM to 100 OHM.
6. Change C8004 from 470p to 270p.
7. Change C8011 from 1000p to 2200p.
8. Change C8013 from 220p to 100p.
9. Q9001B rename to Q9000B .
10. Change D8700 from 1SS355 to RB751
11. Unmount R8708 (Battery pack have pre-charge function)

(08/19/08)

12. Delete 1.5VSUS circuit .
13. Q8802A rename to Q8800A .
14. Add L8000,L8001 FB short pin .

(08/26/08)

15. Fix RT8204(U8200) to PWM mode .
16. Unmount R8715 .
17. Change R8208 to 4.02K ,R8205 to 10K .

(08/29/08)

18. Change U8200 PCB footprint .

(09/01/08) 243 pcs

19. Change Vcore solution to MAX17033 .

(09/02/08) 241 pcs

20. Delete R8102,R8103, connect U8100 pin 2 to pin 4 .
21. Add R8720 10HM .

(09/09/08) 242 pcs

22. Add D8701 , unmount .

R1.1 -- (09/30/08)

23. Change L8300 to 1.5uH
24. Change R8200 to 9.09K
25. Change CE8000,8004,8006,8007 to 220uF/2V/9mOHM
26. Change U8101 to MIC5378
27. Change R8111 to 232K

28. 3V_5V_PWRGD rename to SUS_PWRGD
29. Change R9001 to 4P2R , add R9006 .

(10/14/08)

30. Change Q8000,8003,8004,8007 to SI7716ADN

(10/21/08)

31. Del D8701 .
32. Modify circuit : Charge Vset & Iset control from EC .
33. Change Q8707 to SI4116 .

(12/10/08)

34. Add C8215 for LDO transient .

PEGATRON Title : POWER_HISTORY

ASUSTeK COMPUTER INC. NB Engineer: Wit_Yang

Size	Project Name	Rev
C	F82	1.2

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