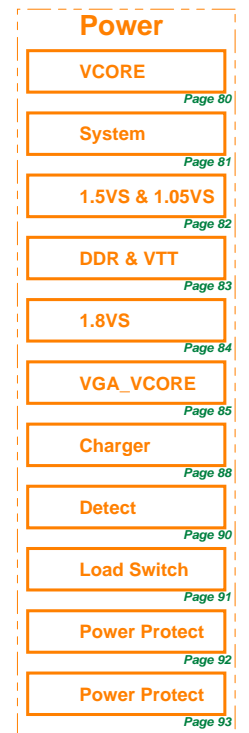
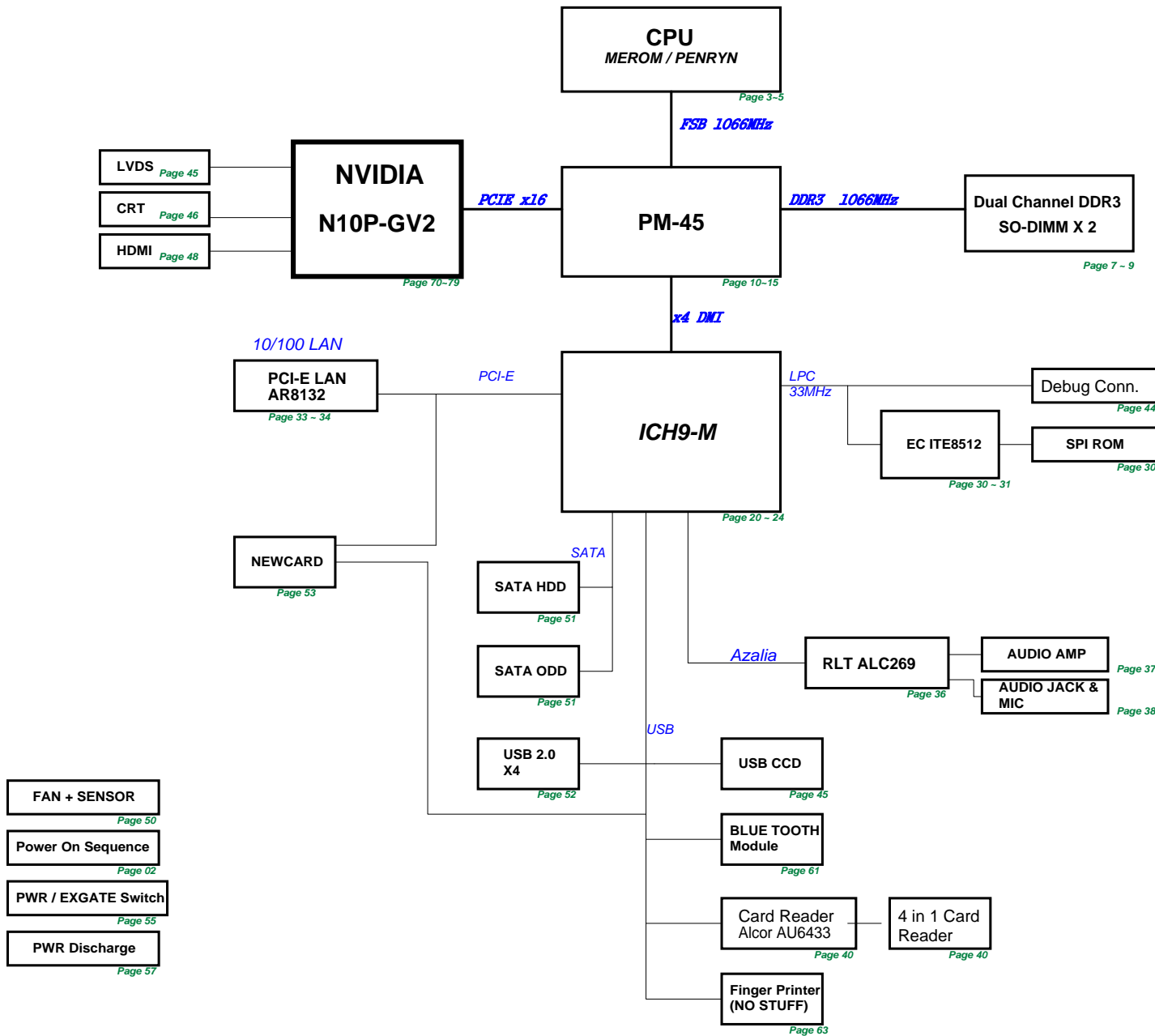
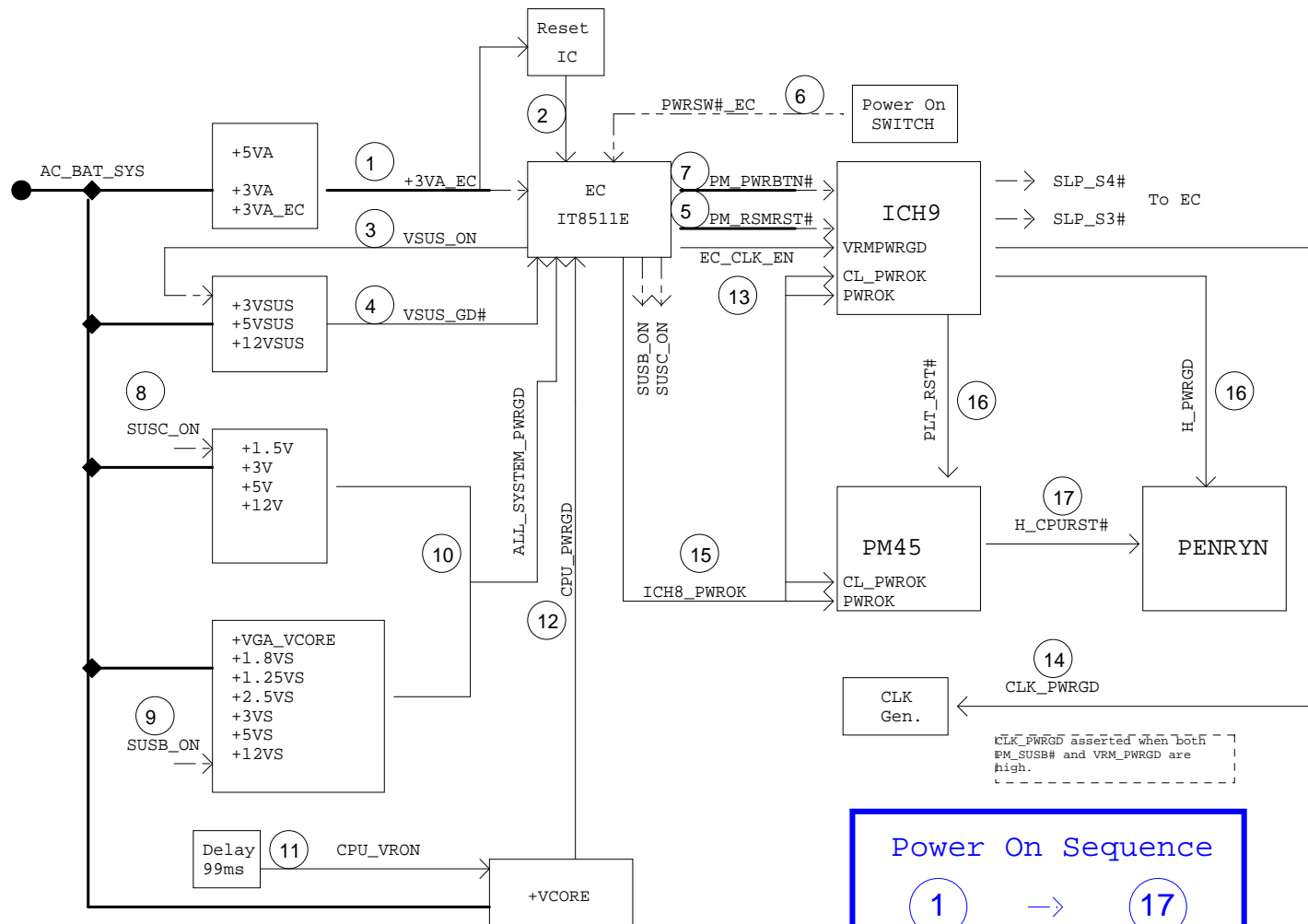


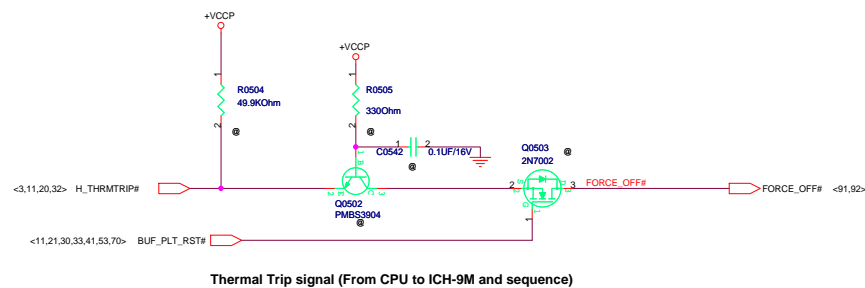
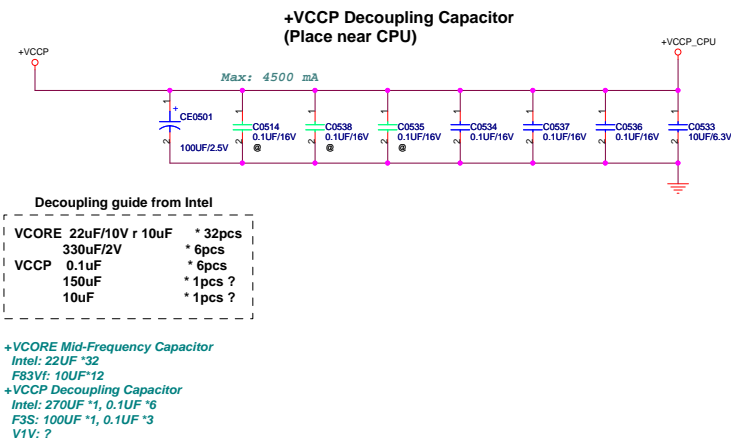
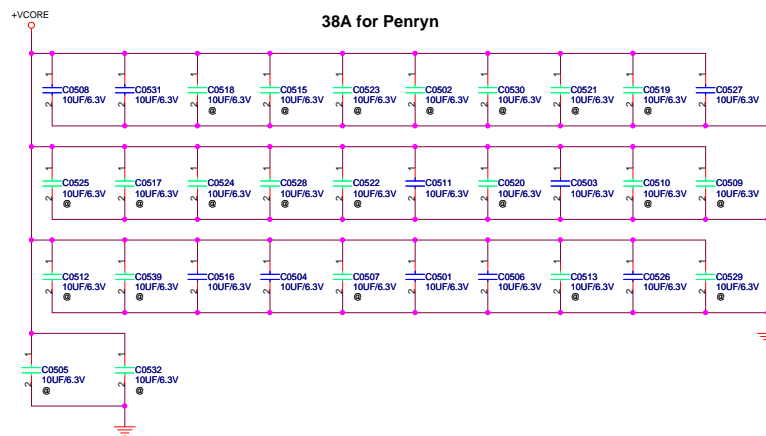
F83Vf MonteVina BLOCK DIAGRAM

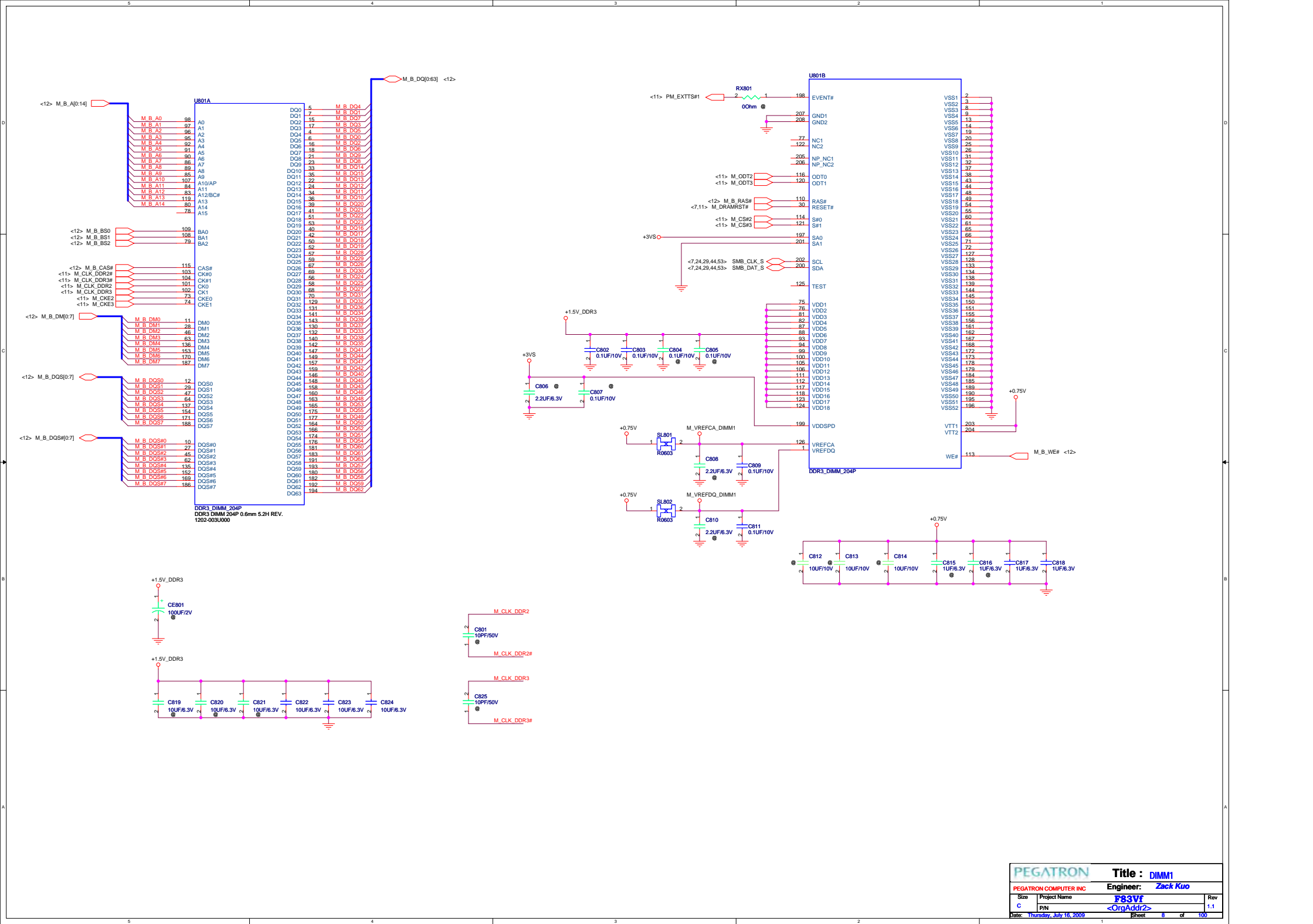


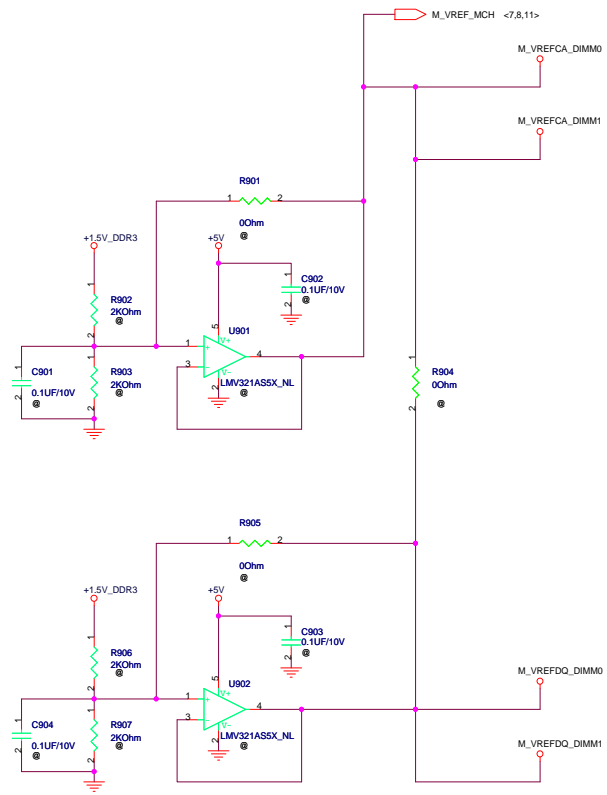


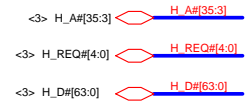
Power On Sequence

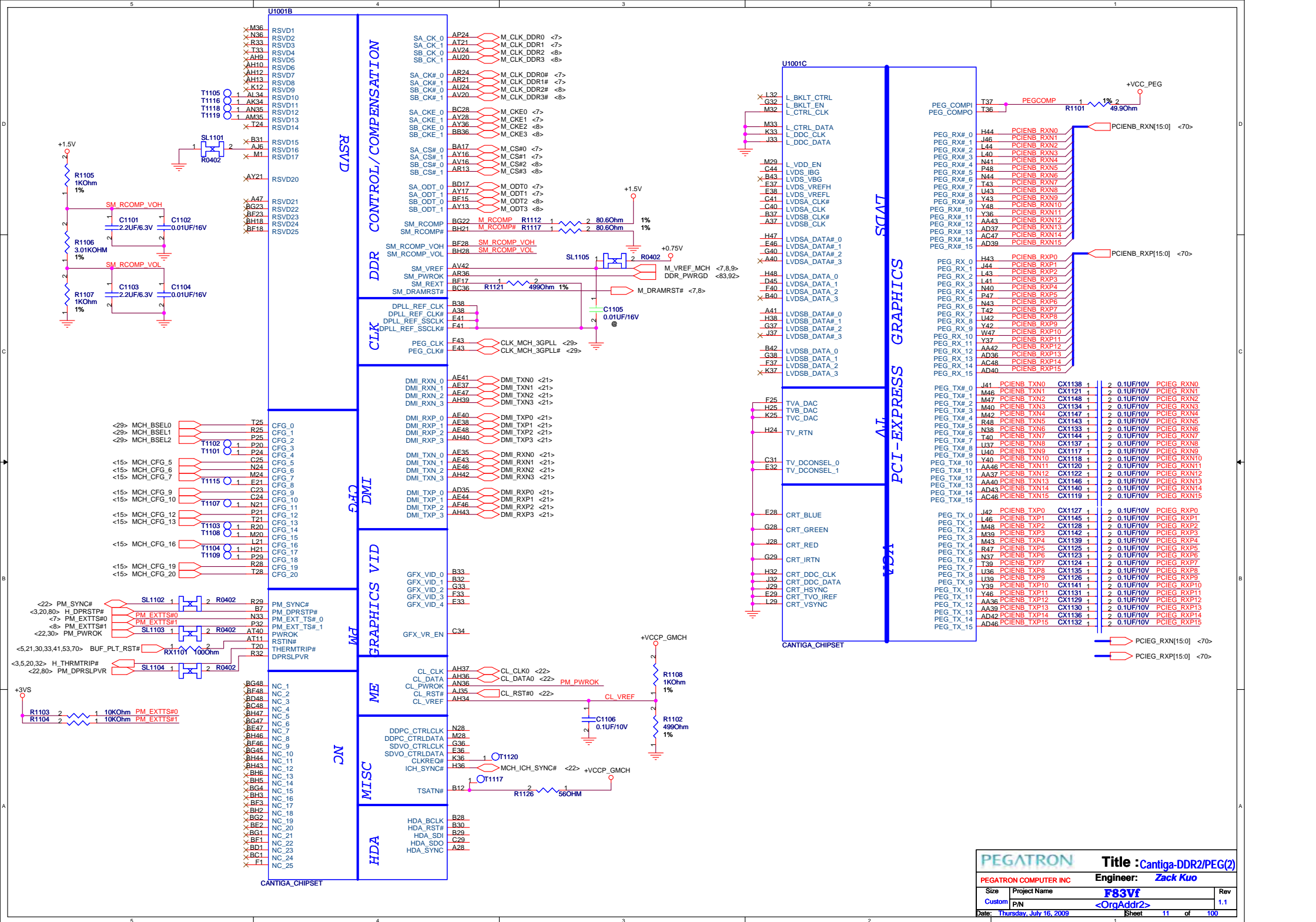
1 → 17

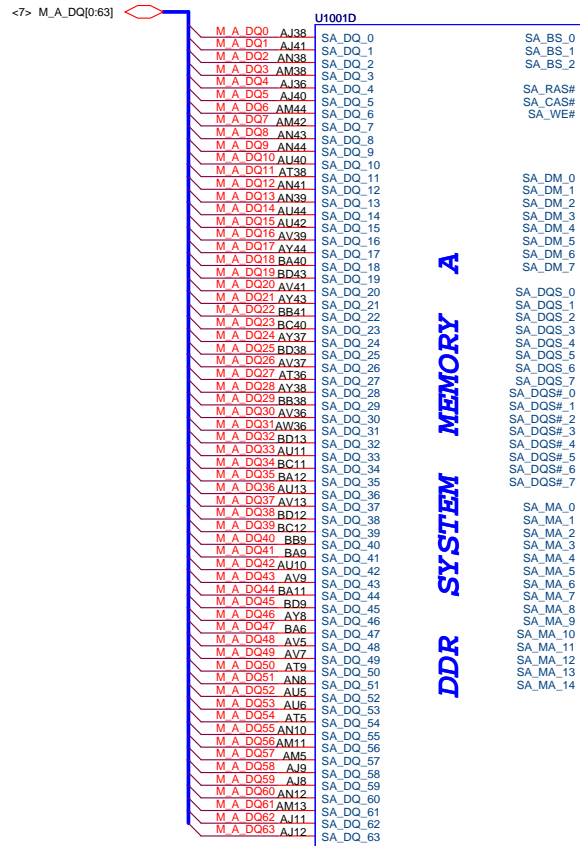






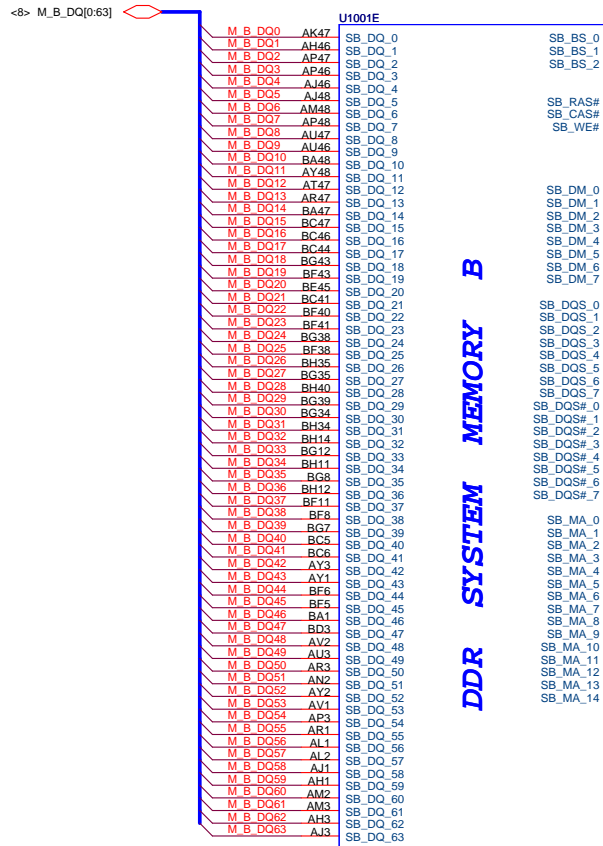






DDR SYSTEM MEMORY A

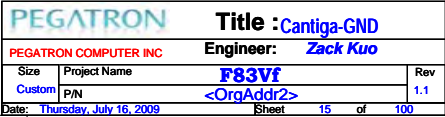
CANTIGA_CHIPSET

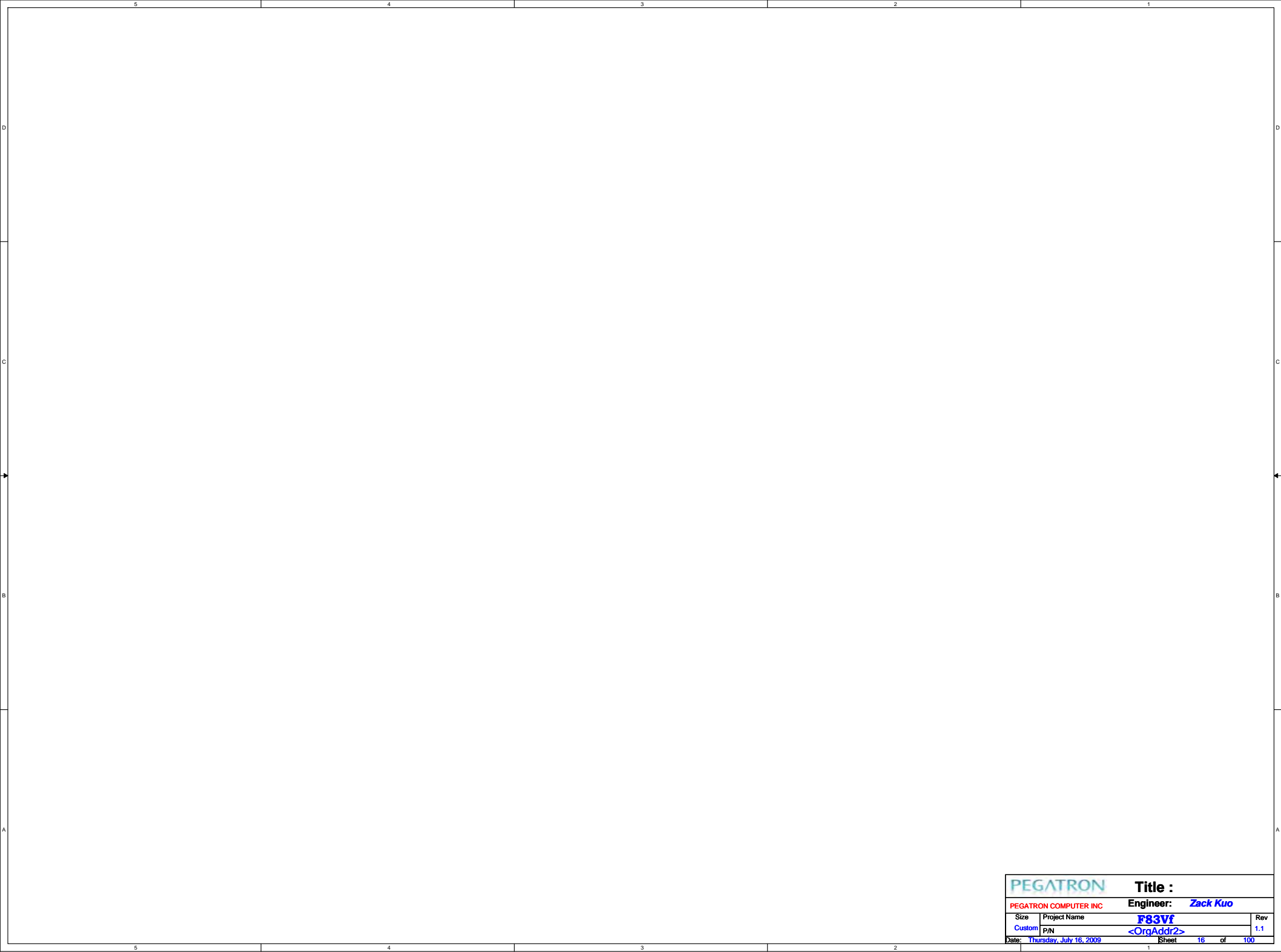


DDR SYSTEM MEMORY B

CANTIGA_CHIPSET







PEGATRON		Title :	
PEGATRON COMPUTER INC		Engineer: Zack Kuo	
Size	Project Name	F83Vf	Rev
Custom	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009		Sheet	16 of 100

PEGATRON

Title :

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	P/N	1.1
Date: Thursday, July 16, 2009		Sheet 17 of 100

PEGATRON


Title :

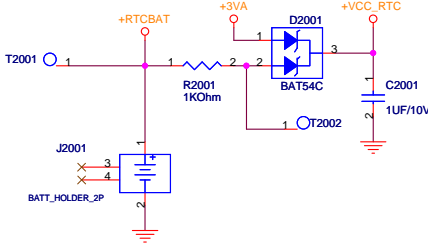
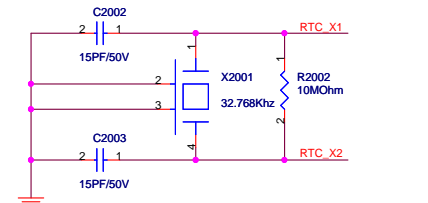
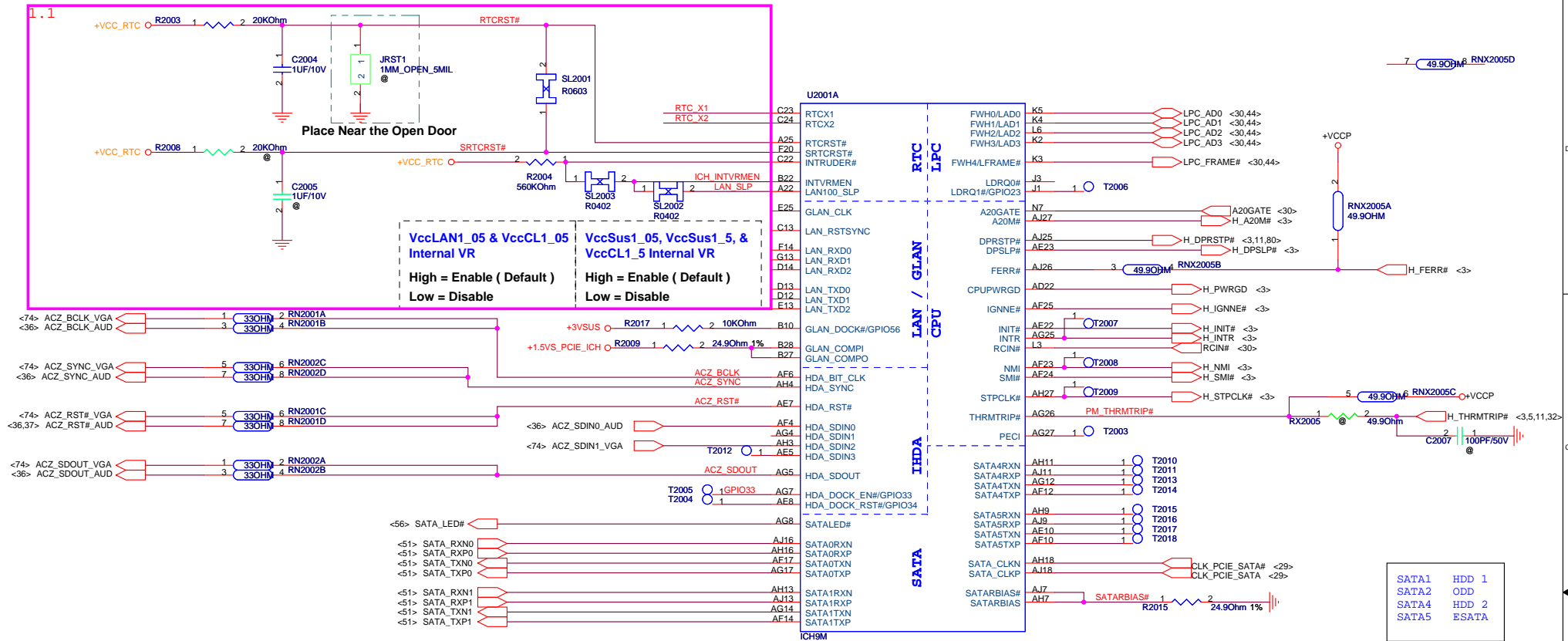
PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	P/N	1.1
Date: Thursday, July 16, 2009		Sheet 18 of 100

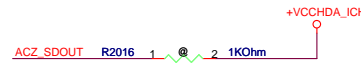
	5	4	3	2	1
D					
C					
B					
A					

		Title :	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009		Sheet 19 of 100	

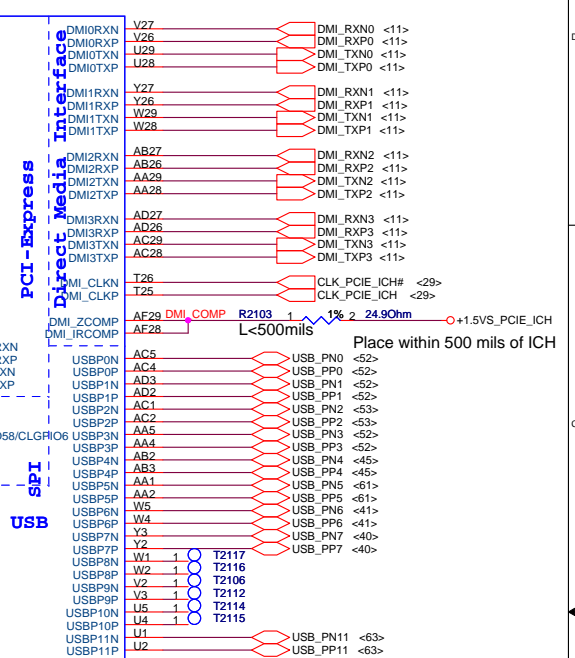
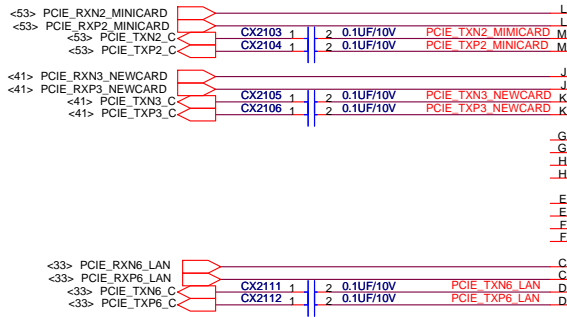
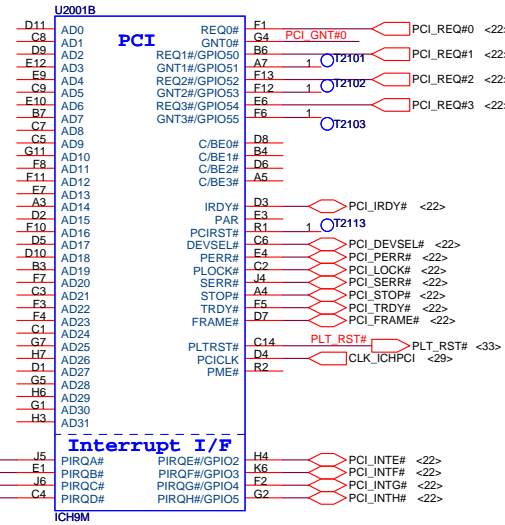


[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap

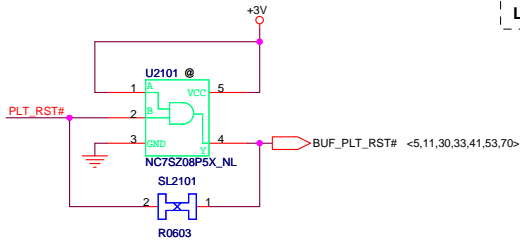
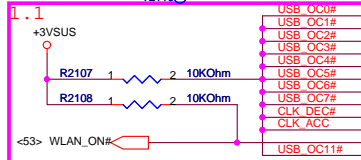
00 = Reserved
 01 = Enter XOR Chain
 10 = Normal Operation (Default)
 11 = Set PCIe Port Config Bit 1



PCIE1 NC
PCIE2 MiniCard
PCIE3 NewCard
PCIE4 NC
PCIE5 NC
PCIE6 LAN



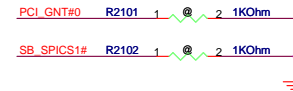
SPI MOSI
ITPM Enable
High = Enable
Low = Disable(Default)



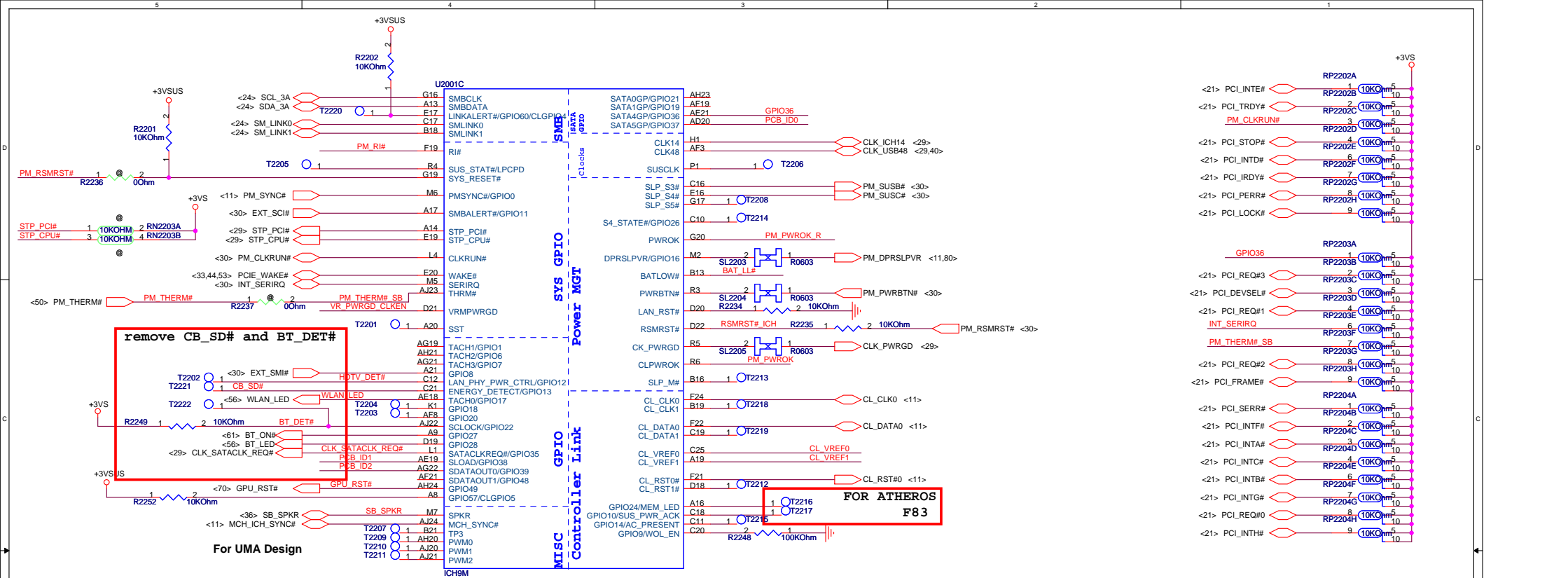
ICH9 Boot BIOS select

	GNT#0	CS#1
LPC	11	1
PCI	10	1
SPI	01	0

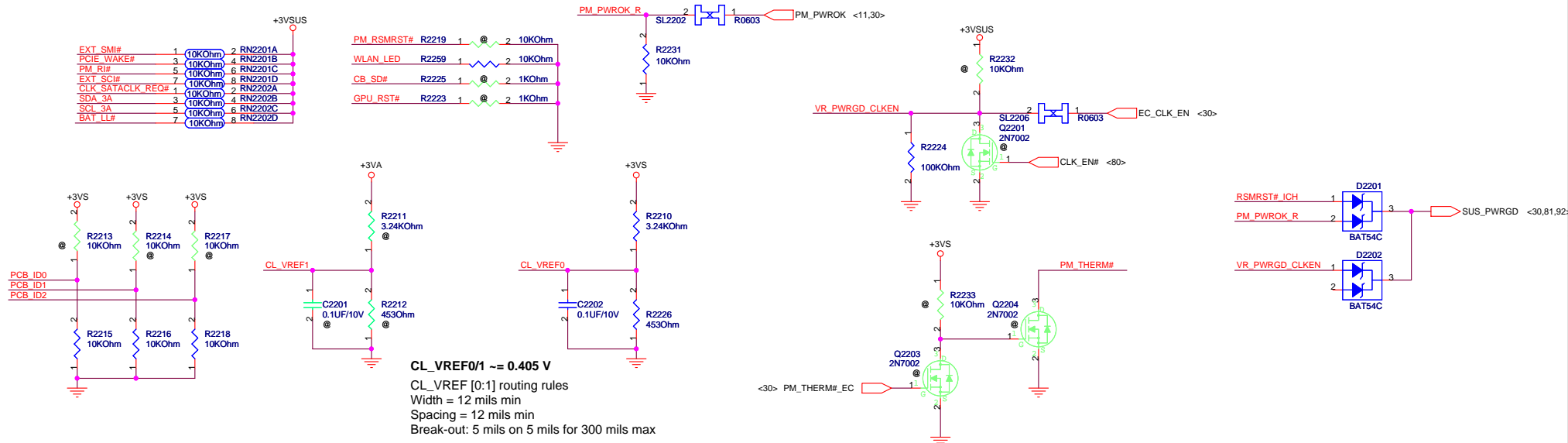
(default)



USB0 External Port 1
USB1 External Port 2
USB2 WLAN
USB3 External Port 3
USB4 CMOS Camera
USB5 BT
USB6 NEWCARD
USB7 CardReader
USB8 FREE
USB9 FREE
USB10 FREE
USB11 FingerPrinter



Mount/unmount as same R2236



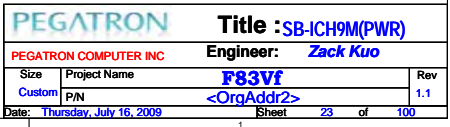
CL_VREF0/1 ~ 0.405 V

CL_VREF [0:1] routing rules

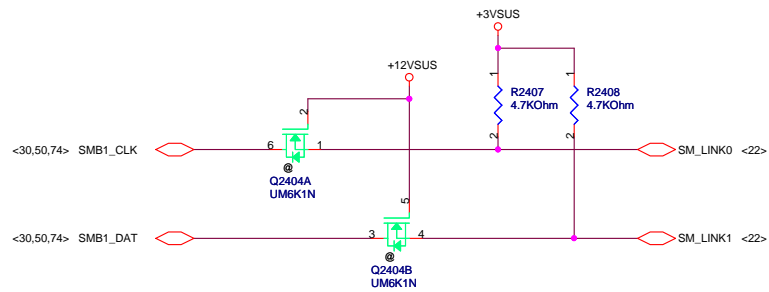
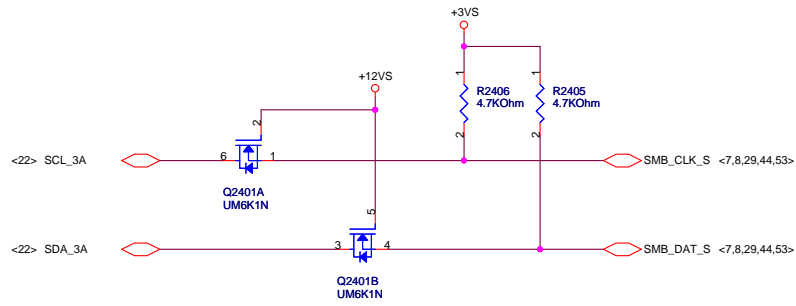
Width = 12 mils min

Spacing = 12 mils min

Break-out: 5 mils on 5 mils for 300 mils max



ICH9-M



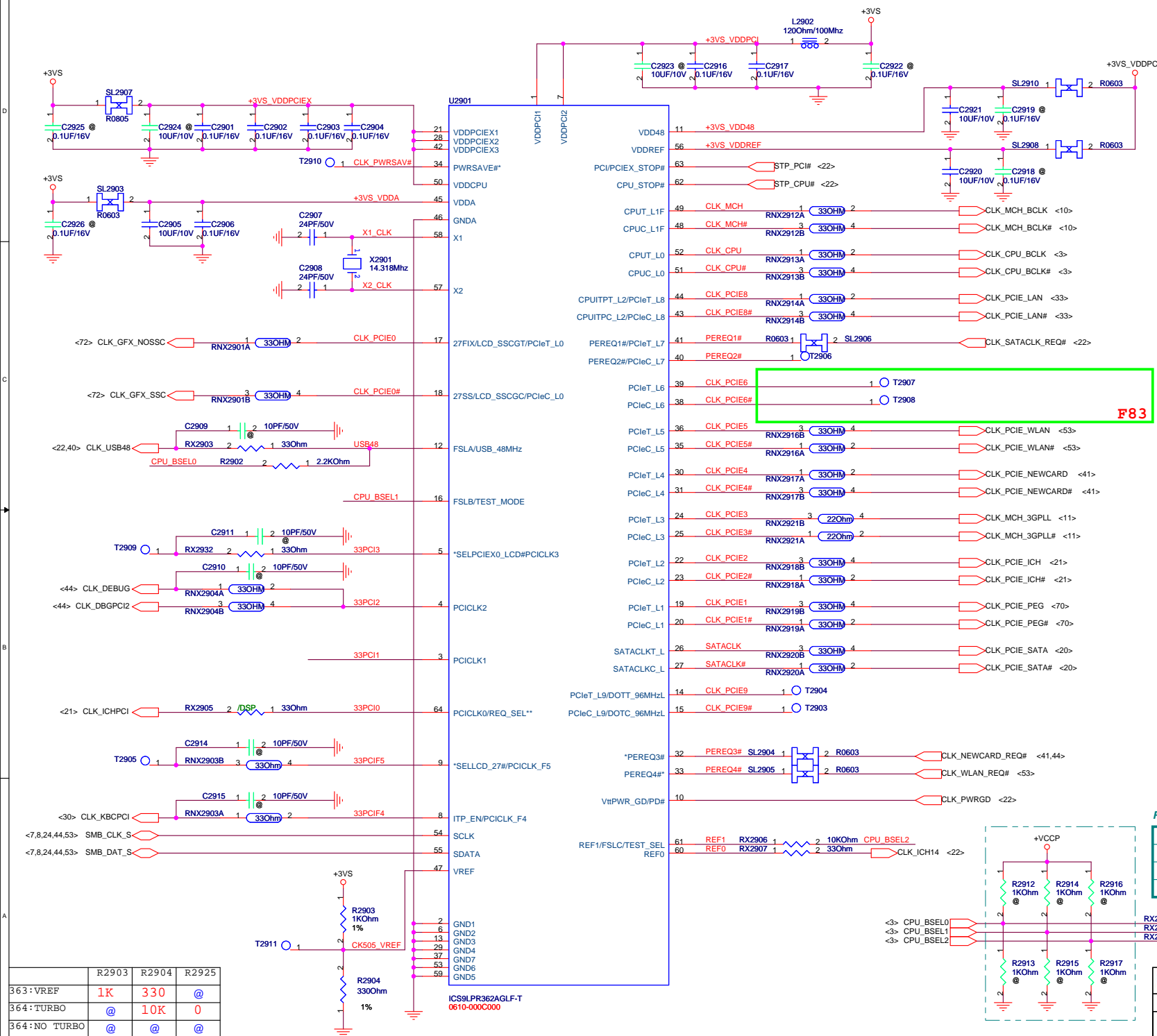
PEGATRON

Title :SB ****

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	P/N	1.1
Date: Thursday, July 16, 2009		Sheet 28 of 100



Latched Input Select

- 0 : Pin 17/18 = LCD_SSCG
- 1 : Pin 17/18 = PCIe_L0

- | 0 : Pin 43/44 = SRC CLK
- | 1 : Pin 43/44 = CPU_ITP CLK

```
0 : Pin 14/15 = PCIe_L9
    Pin 17/18 = 27FIX/27SS
1 : Pin 14/15 = DOT_96MHz
    Pin 17/18 = LCD_SSCG/PCIe_L0
```

0 : Pin 40/41 = PCIe_L7
1 : Pin 40/41 = PEREQ#

PEREQ1#:

PEREQ2#:

PEREQ3# : PCIEX2/4
PEREQ4# : PCIEX3/5/7

For 364 Over-clocking

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0

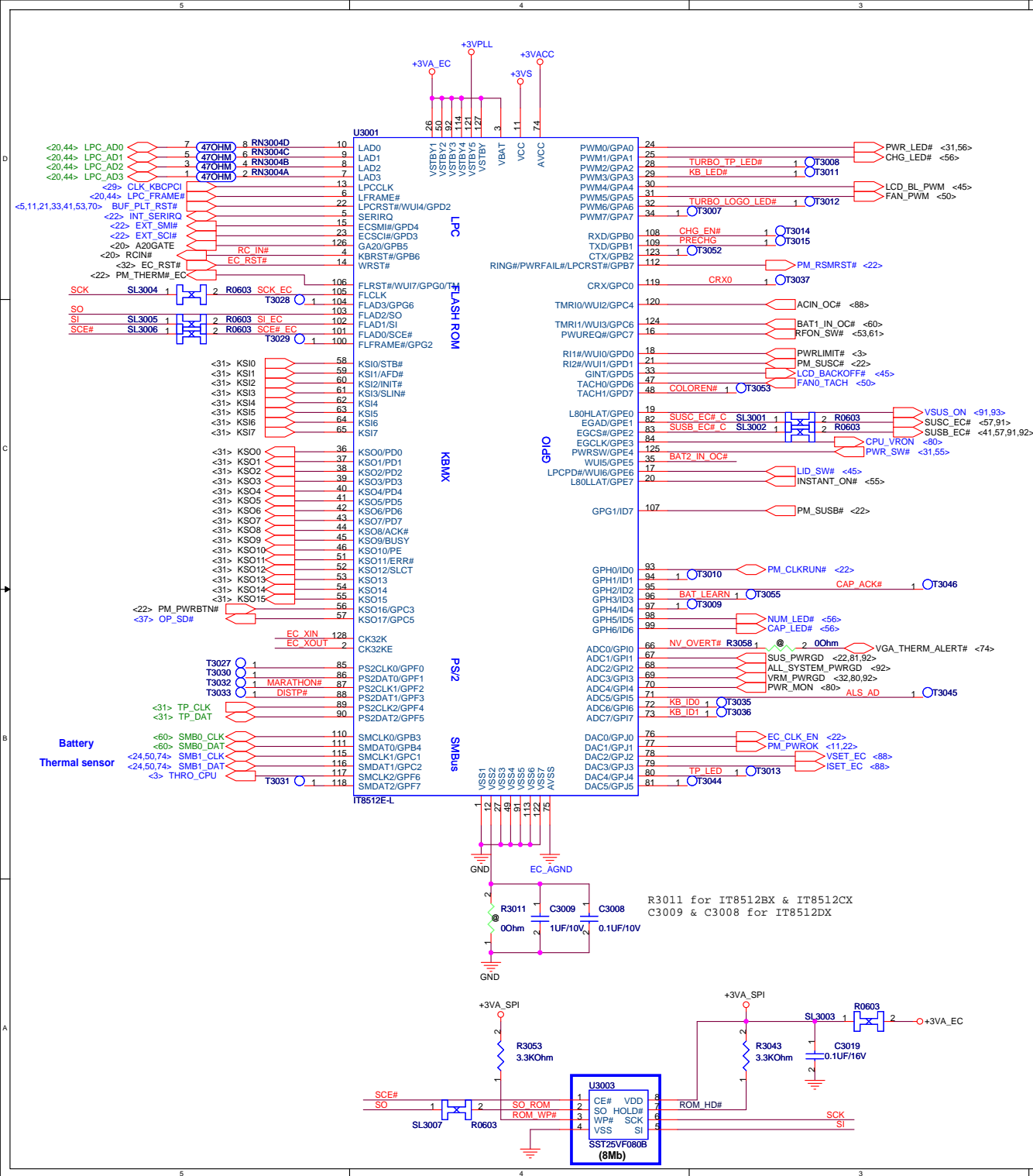
Reserved for R1.0 Debug

PEGATRON Title : CLK_ICS9LPR363

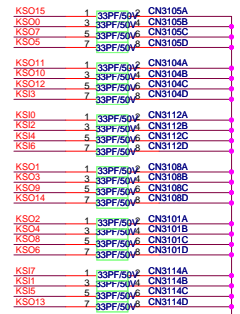
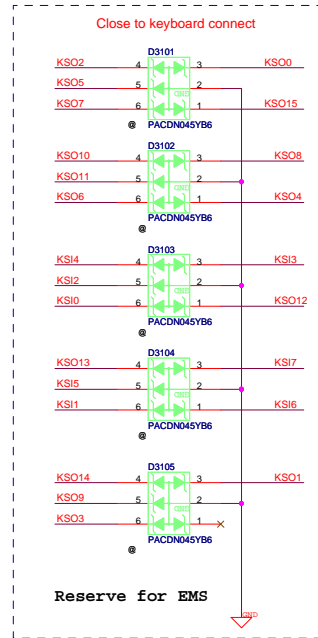
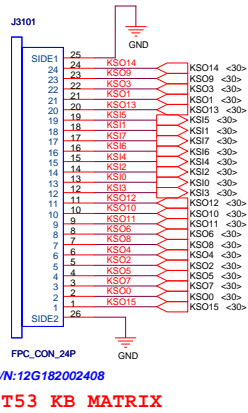
PEGATRON COMPUTER INC Engineer: **Zack Kuo**

Size	Project Name	F83Vf
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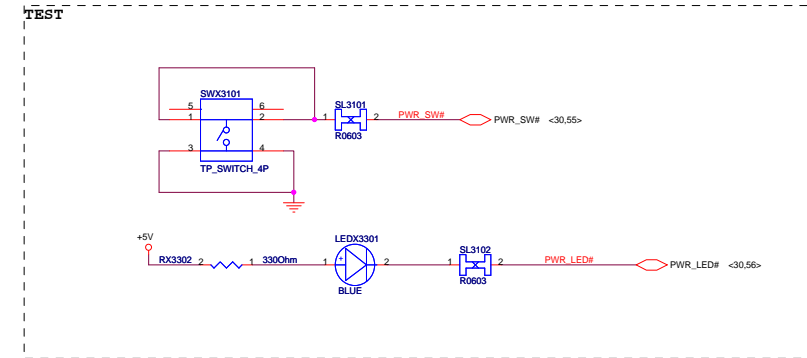
Custom	P/N	<OrgAddr2>
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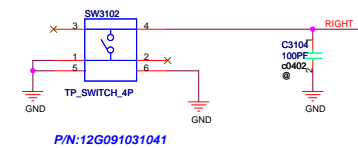
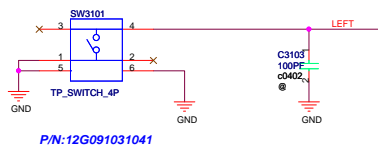
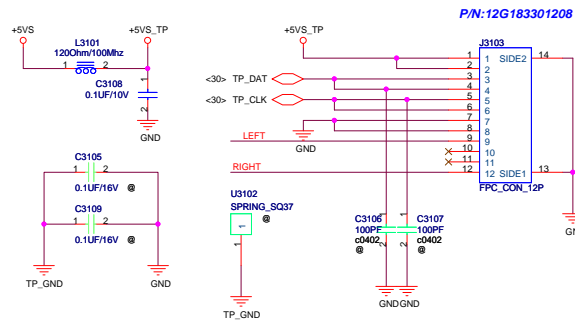
For Keyboard

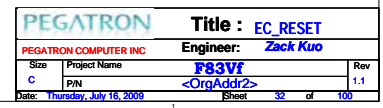


Reserve for EMI

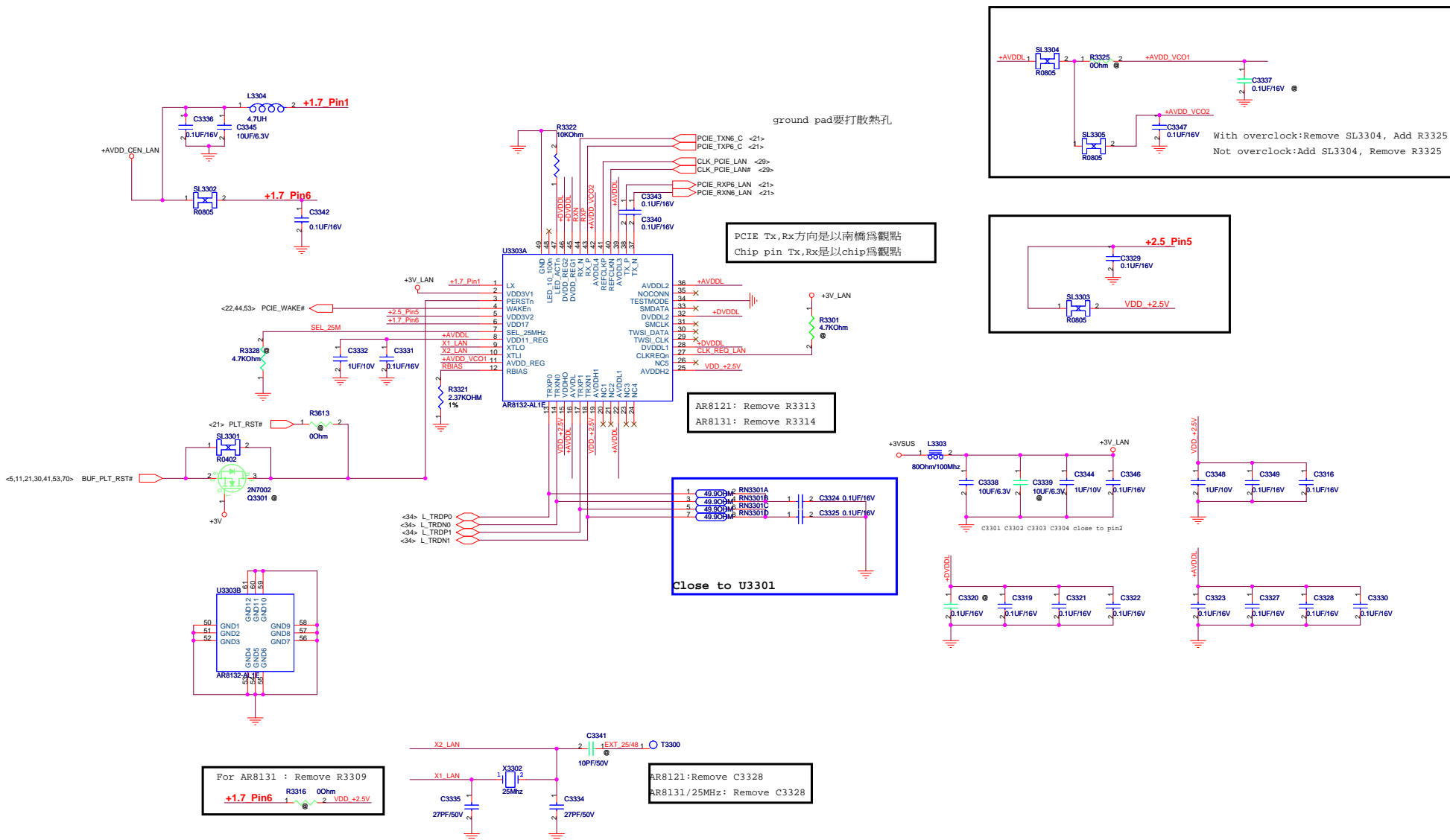


Touch-Pad

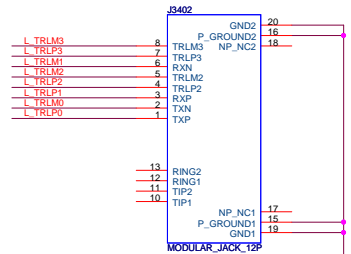
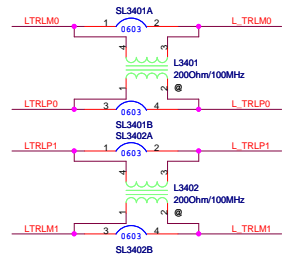
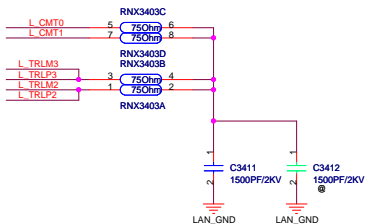
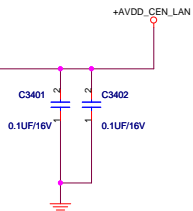
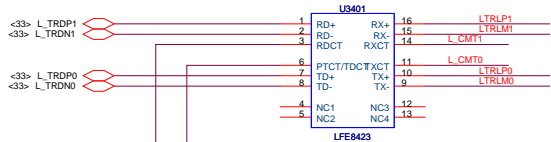
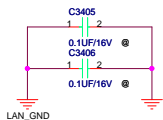
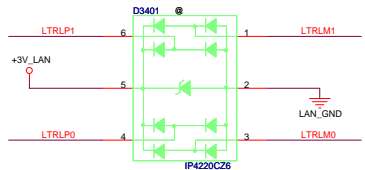


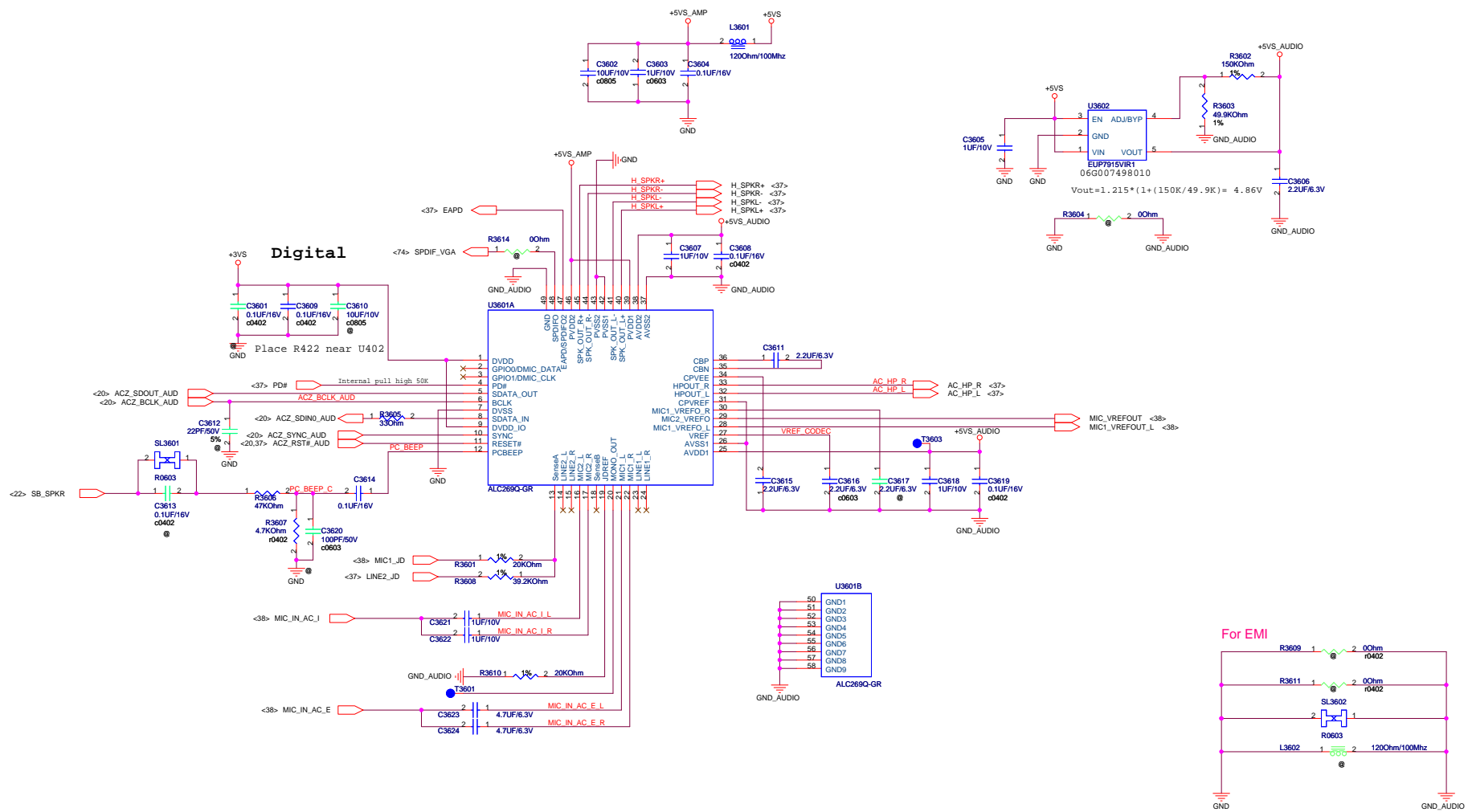


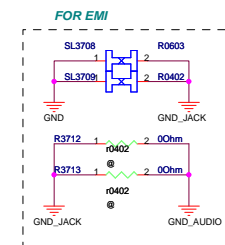
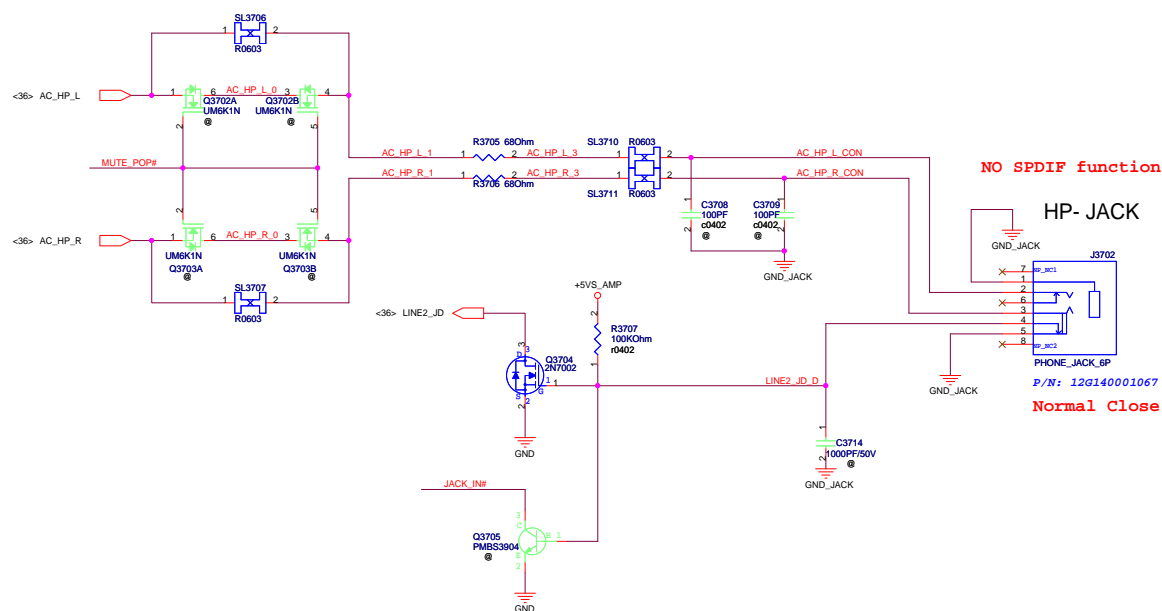
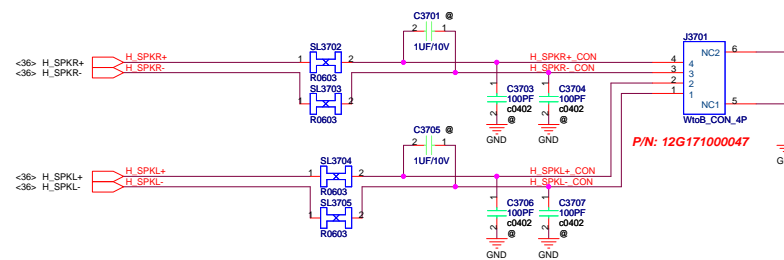
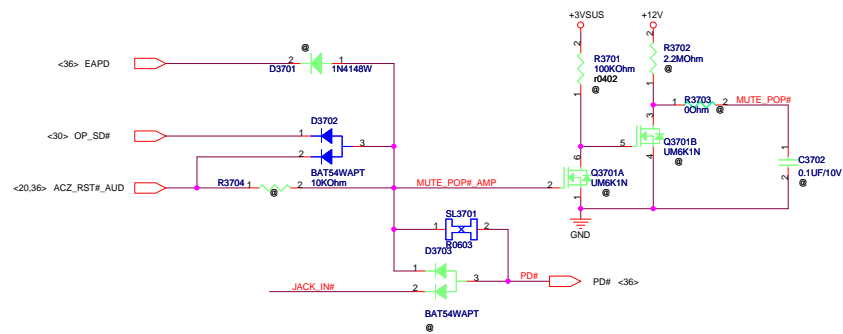
+3VS <3,7,8,11,14,15,22,23,24,29,30,32,36,40,41,44,45,46,48,50,51,53,56,57,70,72,74,80,91,92>
+3VSUS <20,21,22,23,24,30,37,45,53,56,91,92>
GND <3,4,5,7,8,9,10,11,13,14,15,20,21,22,23,29,30,31,32,34,36,37,38,40,41,44,45,46,48,50,51,52,53,55,56,57,60,61,63,68,70,72,73,74,75,76,77,80,81,82,83,84,85,88,91,92>
LAN_GND <34>
LAN_GND

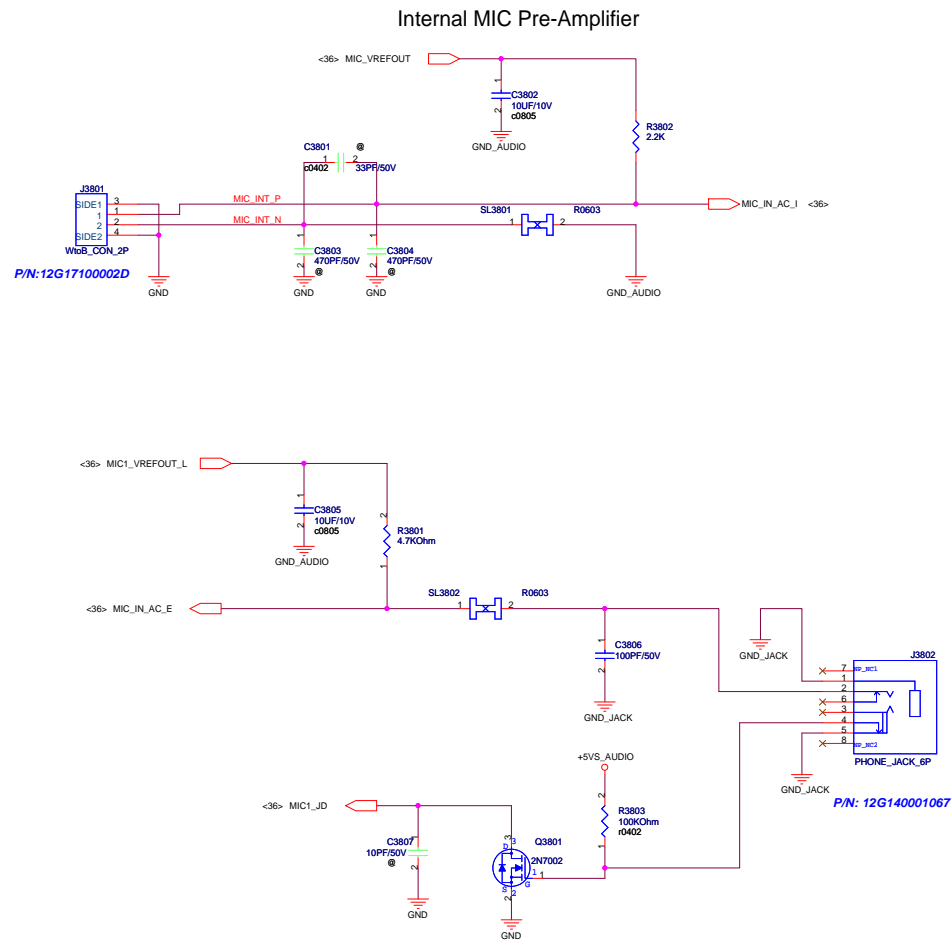


LAN / MODEM PORT



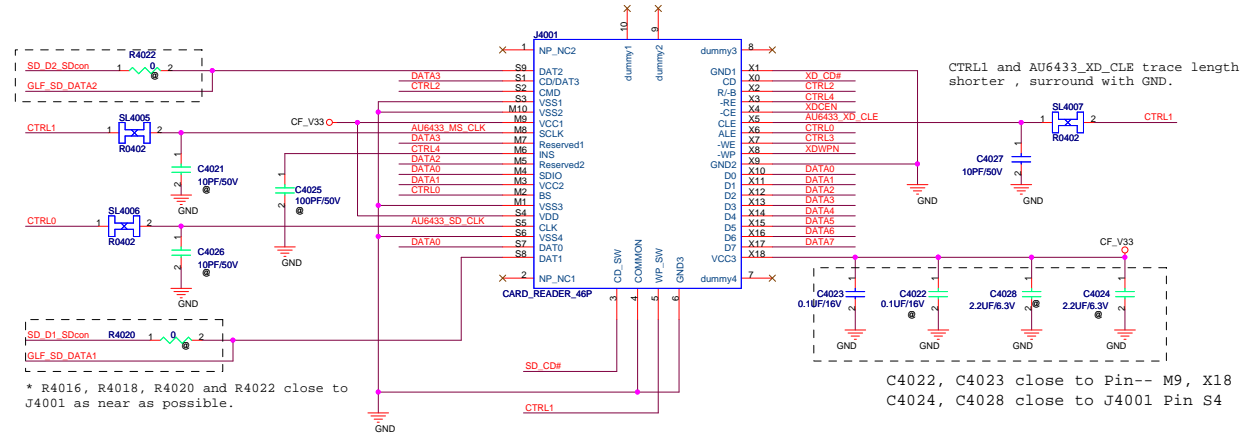
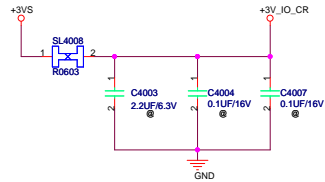




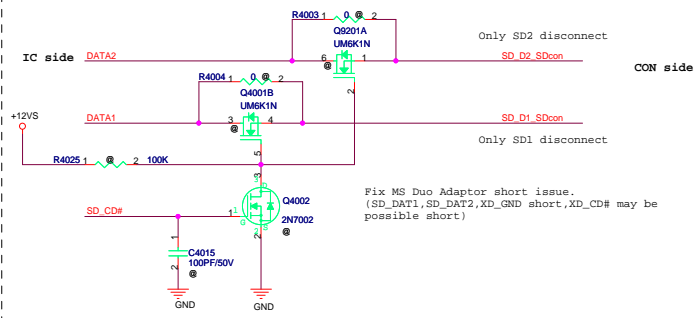


0304 for card reader chip via

CARD READER CONNECTOR

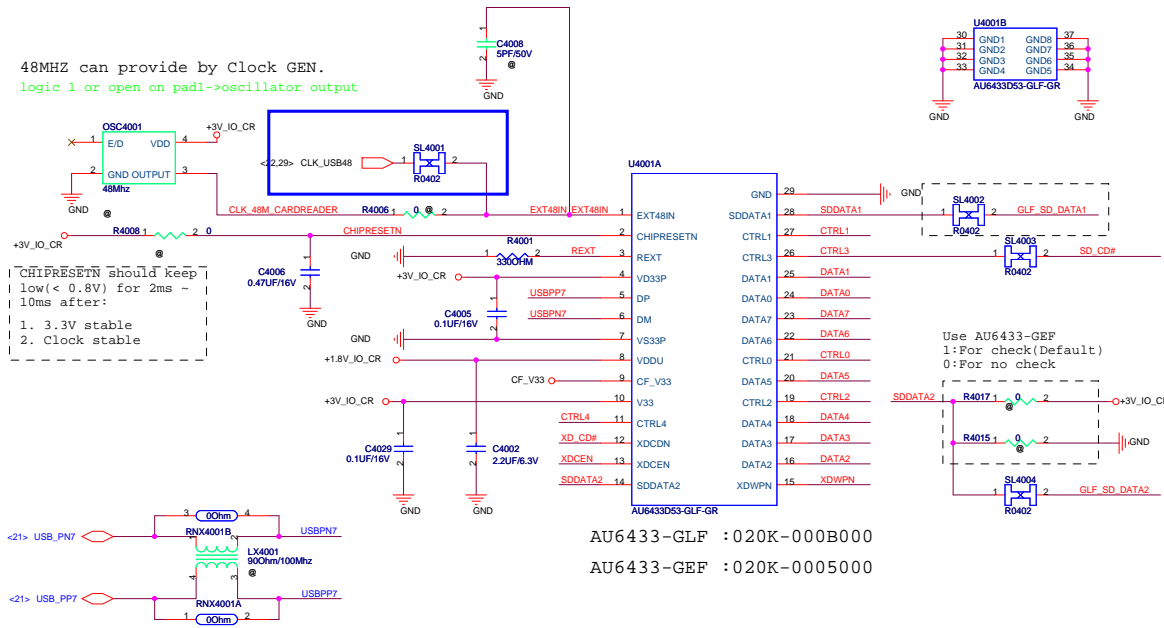


For AU6433-GEF



0304 for card reader chip via

48MHZ can provide by Clock GEN.
logic 1 or open on pad1->oscillator output



CTRL0->SDCLK/XDALE/MSBS
CTRL1->SDWP/XDCLE/MSCLK
CTRL2->SDCMD/XDRBN
CTRL3->SDCDN/XDWRN
CTRL4->XDRDN/MSINS

XDCDN->XDCDN
XDCEN->XDCEN
SDDATA2->SDDATA2/xD CIS check is disable
XDWPEN->XDWPEN

ADDDATA1->SDDATA1

DATA0->SDDATA0/XDDATA0/MSDATA0
DATA1->XDDATA1/MSDATA1
DATA2->XDDATA2/MSDATA2
DATA3->SDDATA3/XDDATA3/MSDATA3
DATA4->SDDATA4/XDDATA4/MSDATA4
DATA5->SDDATA5/XDDATA5/MSDATA5
DATA6->SDDATA6/XDDATA6/MSDATA6
DATA7->SDDATA7/XDDATA7/MSDATA7

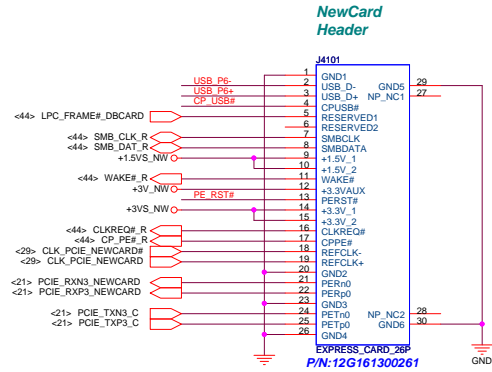
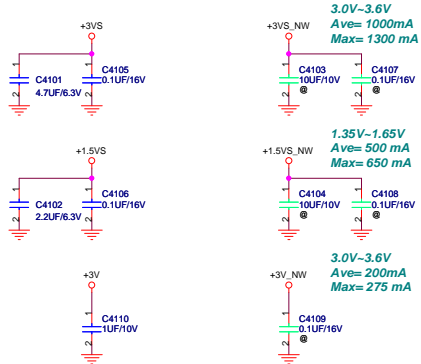
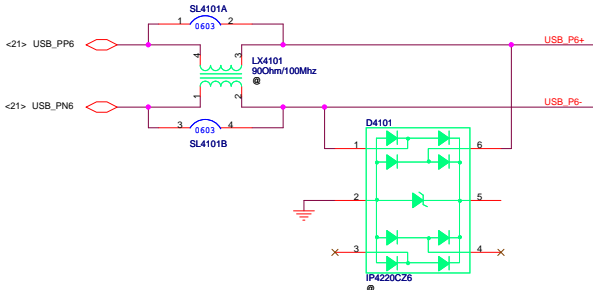
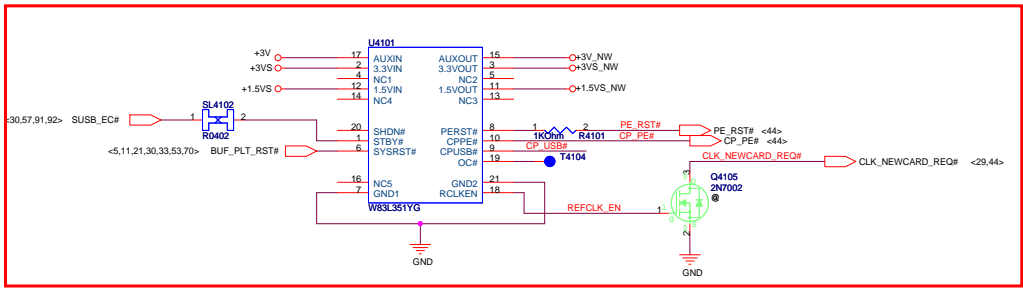
AU6433 GEF /GLF colay.

Option 1:AU6433-GEF
If use GEF package need:

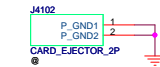
unmount-> R4016,R4018
mount->R4017,R4020,R4022,R4025,Q4001,Q4002.

Option 2:AU6433-GLF
If use GLF package need:

unmount->
R4017,R4020,R4022,R4025,Q4001,Q4002.
mount->R4016,R4018



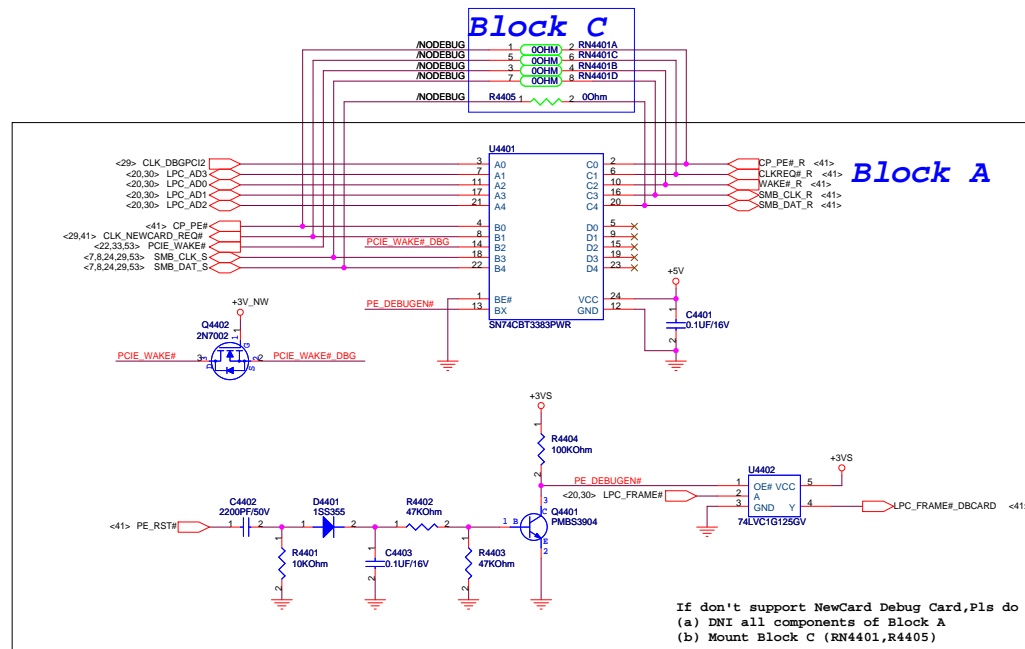
NewCard Ejecter



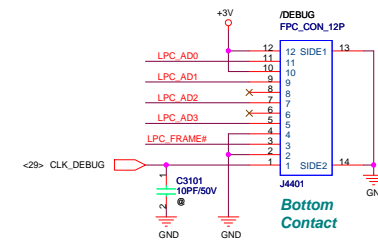
	5	4	3	2	1
D					
C					
B					
A					

PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: Zack Kuo	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009		Sheet 42 of 100	

For NewCard Debug Card

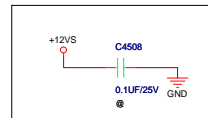
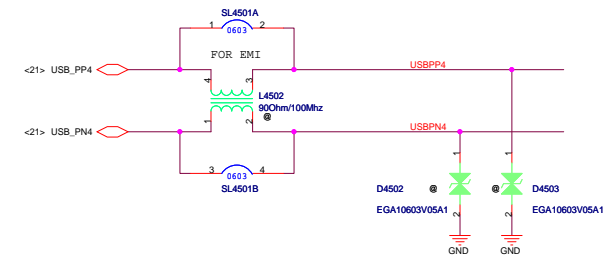


LPC Debug Port

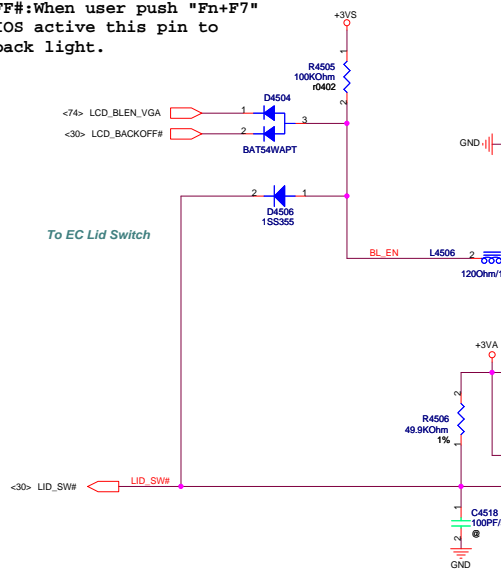


LCD Power

The diagram illustrates a power supply circuit for an LCD. It features a +12V input and a +3V3VUS input. The circuit includes several transistors (Q4501, Q4502, Q4503) and capacitors (C4501 through C4507) for regulation and filtering. A 120Ohm/100mHz inductor (L4501) is used for the +3V3V_LCD output. The output is connected to a 74V3 LCD_PPN_VGA signal.



BIOS
LCD_BACKOFF#:When user push "Fn+F7"
button, BIOS active this pin to
turn off back light.



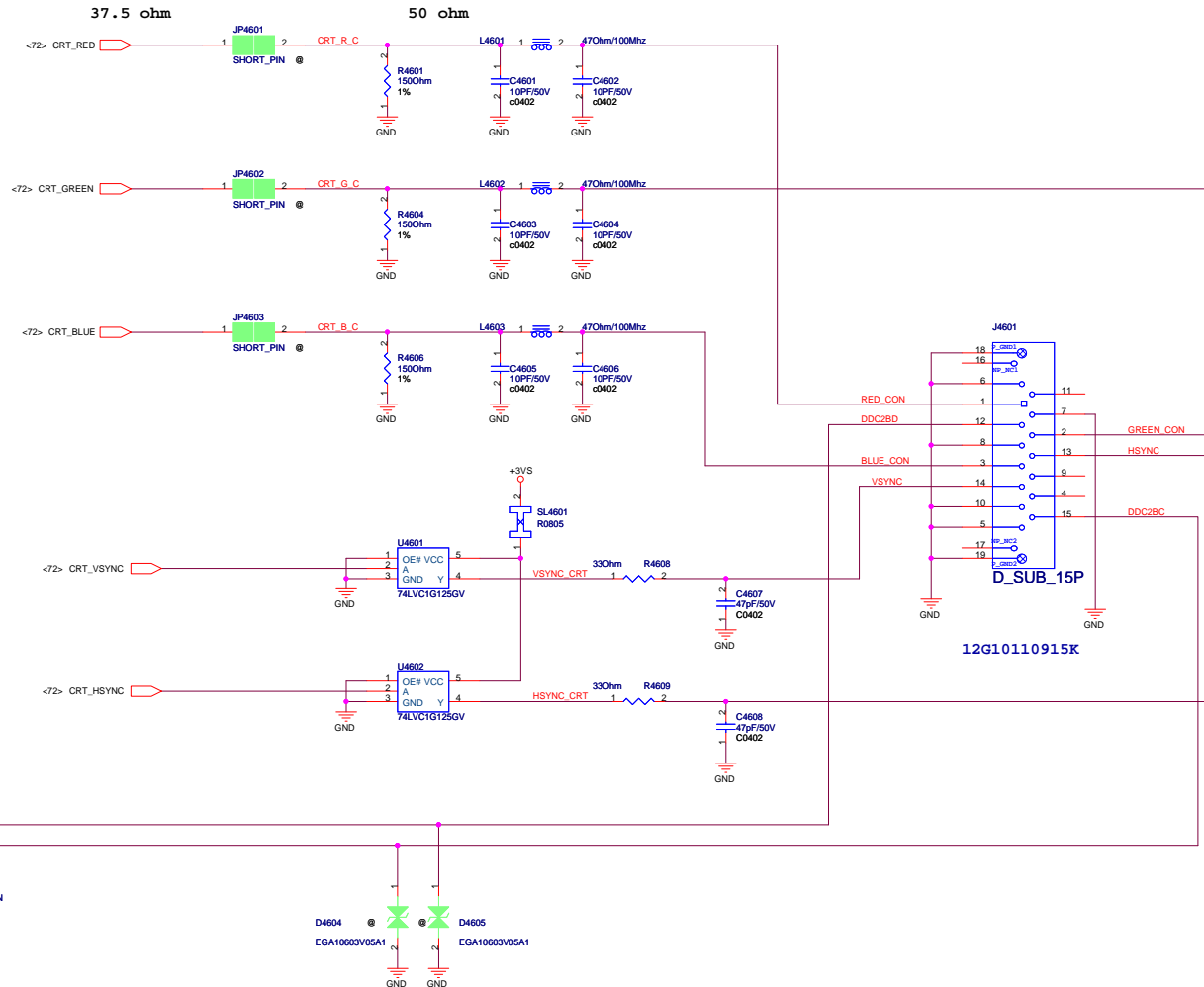
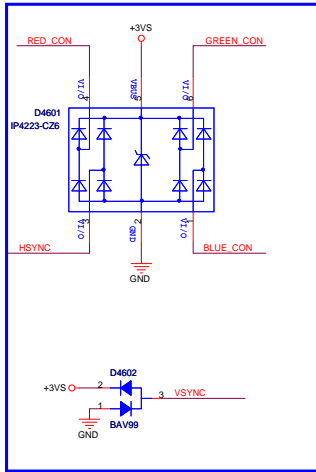
The schematic diagram illustrates the J4501 module's internal connections and external interfaces. Key components and connections include:

- Capacitors:** C4513 (100PF/50V), C4517 (1UF/25V), C4515 (0.1UF/16V), C4516 (10UF/16V), C4509 (0.1UF/16V), and C4511 (100PF/50V).
- Resistors:** L4508 (120Ohm/100mhz), L4509 (120Ohm/100mhz), L4507 (120Ohm/100mhz), and L4502 (R6063).
- Connectors and Pins:** J4501 (SIDE2) with pins 1-42, J4502 (SIDE1) with pins 1-42, and various other connectors like USBP4, AC_BAT_SYS, and LCD_BL_PWM.
- Power and Grounding:** +VIN_INV, +VIN, +3VS, +5V, and GND connections are shown throughout the circuit.
- Signal Lines:** LVDS_L0N, LVDS_L1P, LVDS_L2N, LVDS_L0P, LVDS_L1N, LVDS_L2P, LVDS_L0CKN, LVDS_L0CKP, LVDS_U0N, LVDS_U1P, LVDS_U2N, LVDS_U0P, LVDS_U1N, LVDS_U2P, LVDS_U0CKN, LVDS_U0CKP, EDID_CLK, EDID_DAT, BL_PWM_CON, and WT0B_CON_40P.
- Other Components:** SL4502 (R6063) and L4503 (120Ohm/100mhz) are also present.

Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

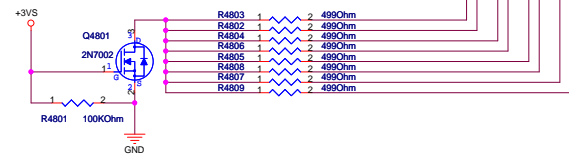
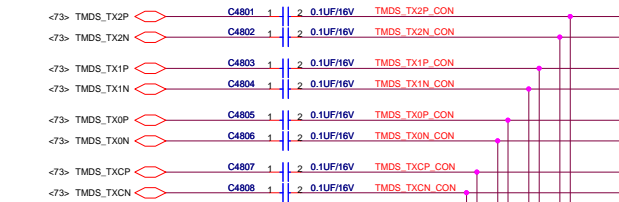
PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: Zack Kuo	
Size C	Project Name F83Vf	Rev 1.1	
Date: Thursday, July 16, 2009	P/N <OrgAdd>	Sheet 45	of 100

PLACE ESD Diodes near connector

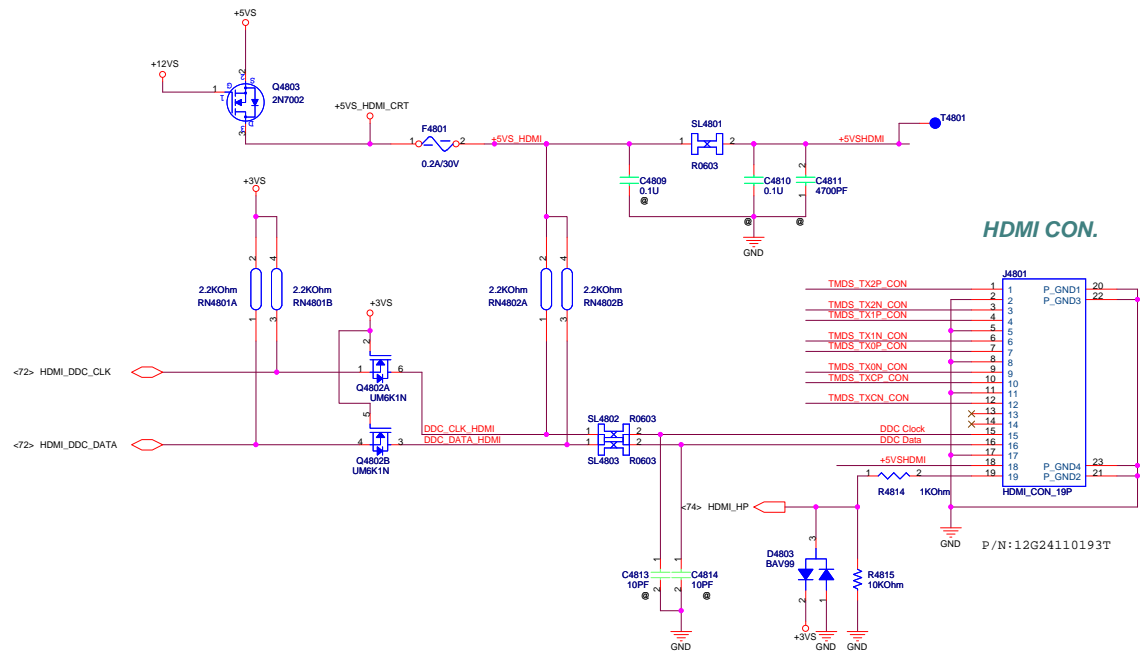


HDMI

near the HDMI connector

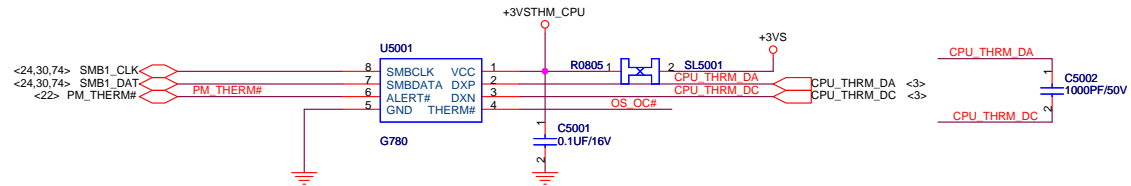


Reference should be +5VS, but All answer that +3VS is fine. As long as it can turn the MOSFET on.

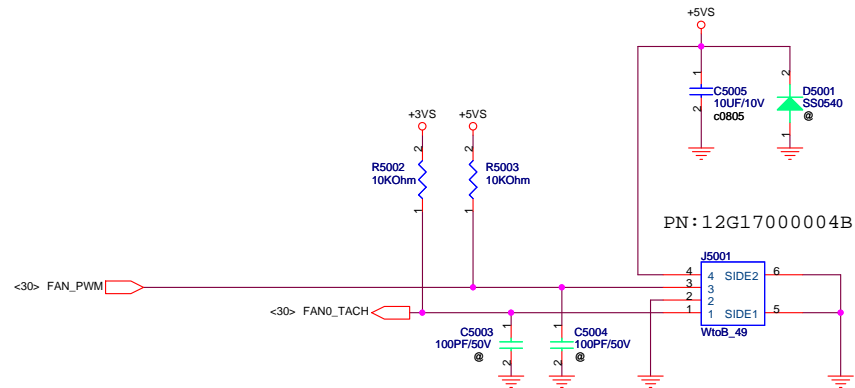


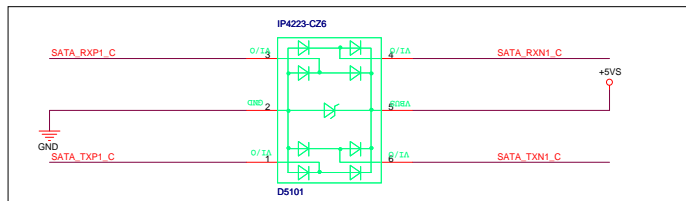
Note: 1. L1805,L1806,L1807: For EMI.(default=0 ohm)
 2. DDC_CLK_HDMI,DDC_DATA_HDMI: +5V tolerant

CPU Thermal Sensor

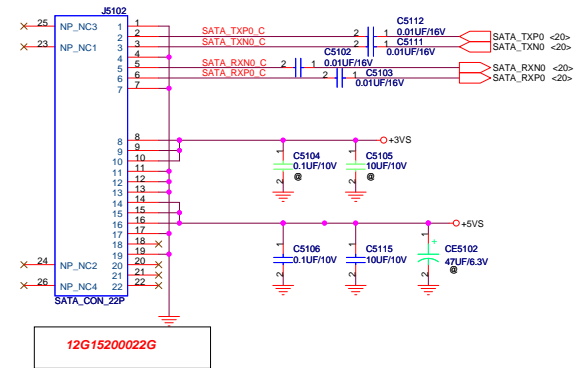


PWM Fan

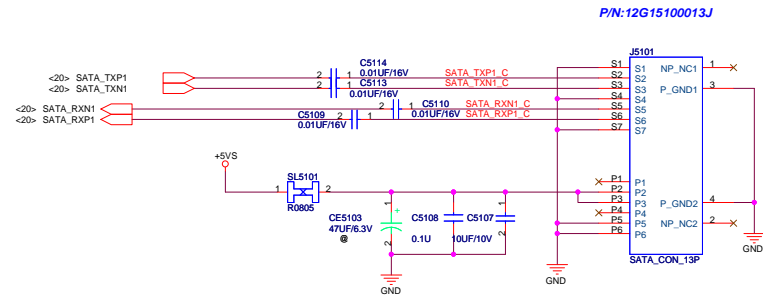


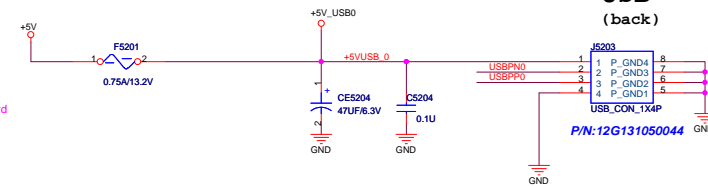
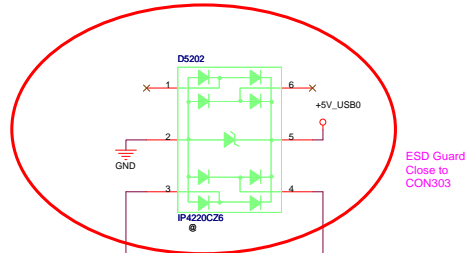
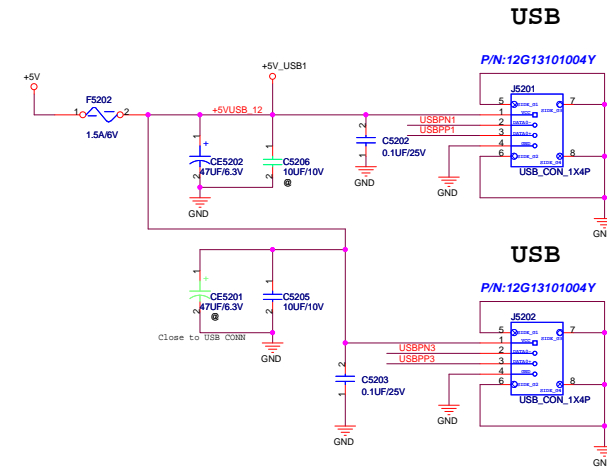
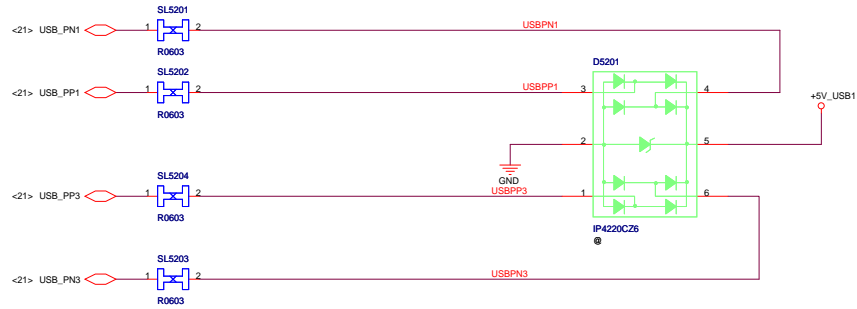


SATA HDD con.



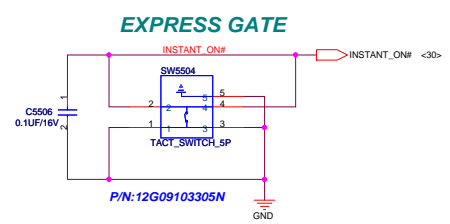
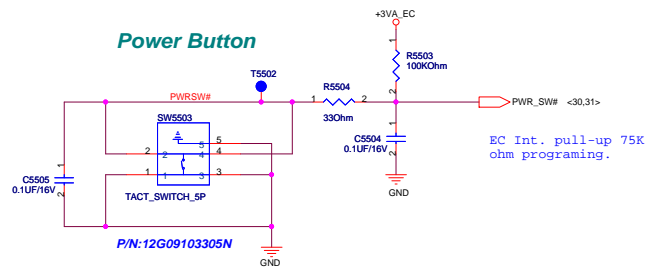
SATA CD-ROM con.





	5	4	3	2	1
D					
C					
B					
A					

PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: Zack Kuo	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	54 of 100

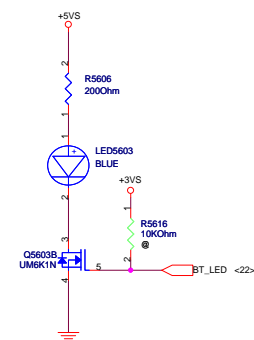
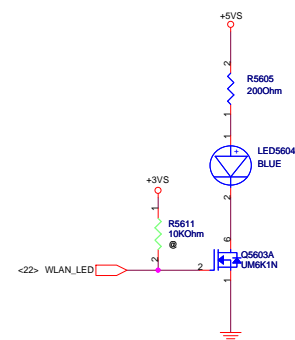
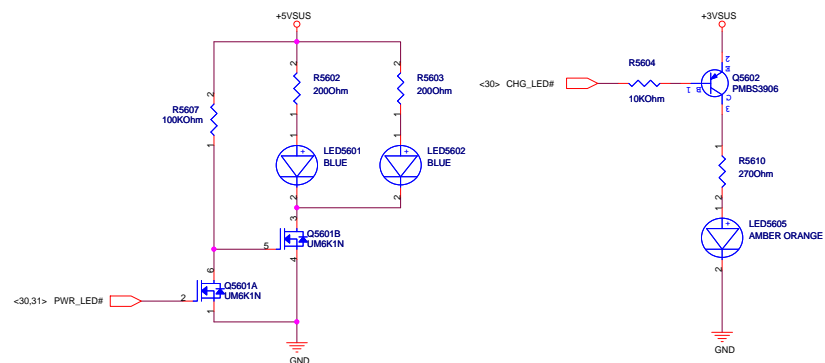


PWR LED

For BATTERY LED

WireLess LED

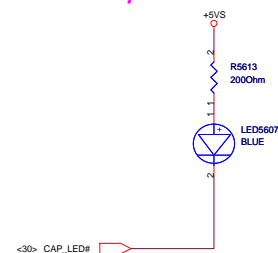
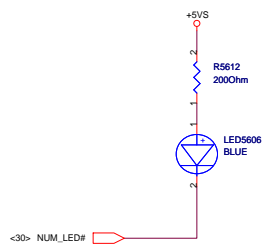
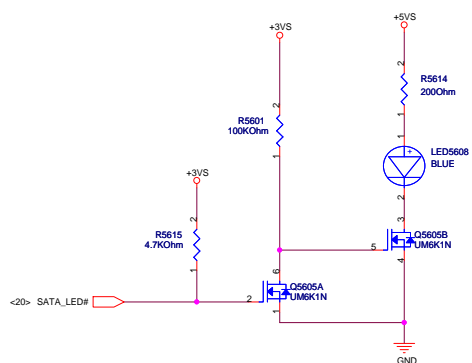
BT LED

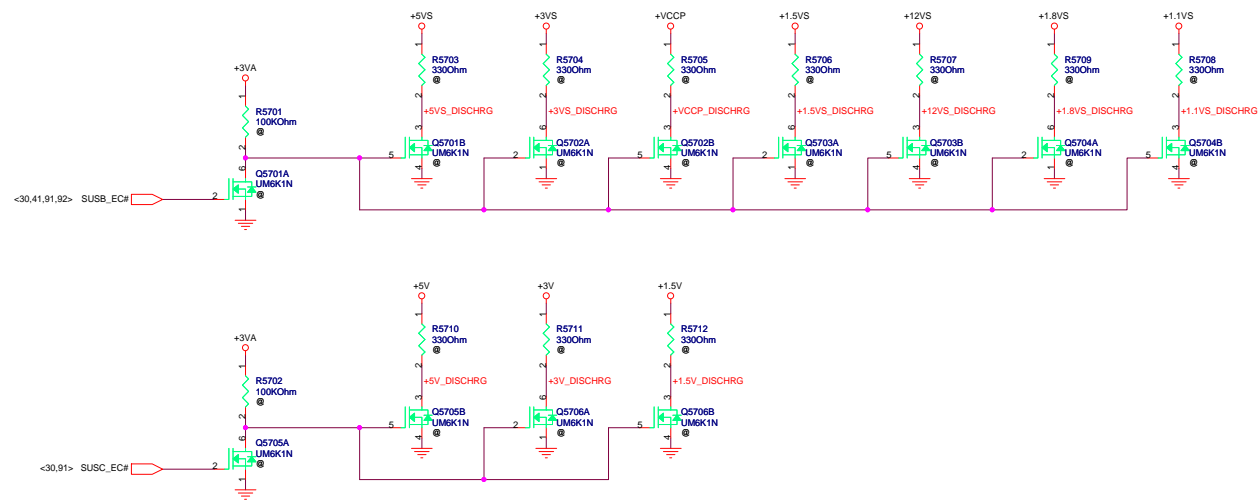


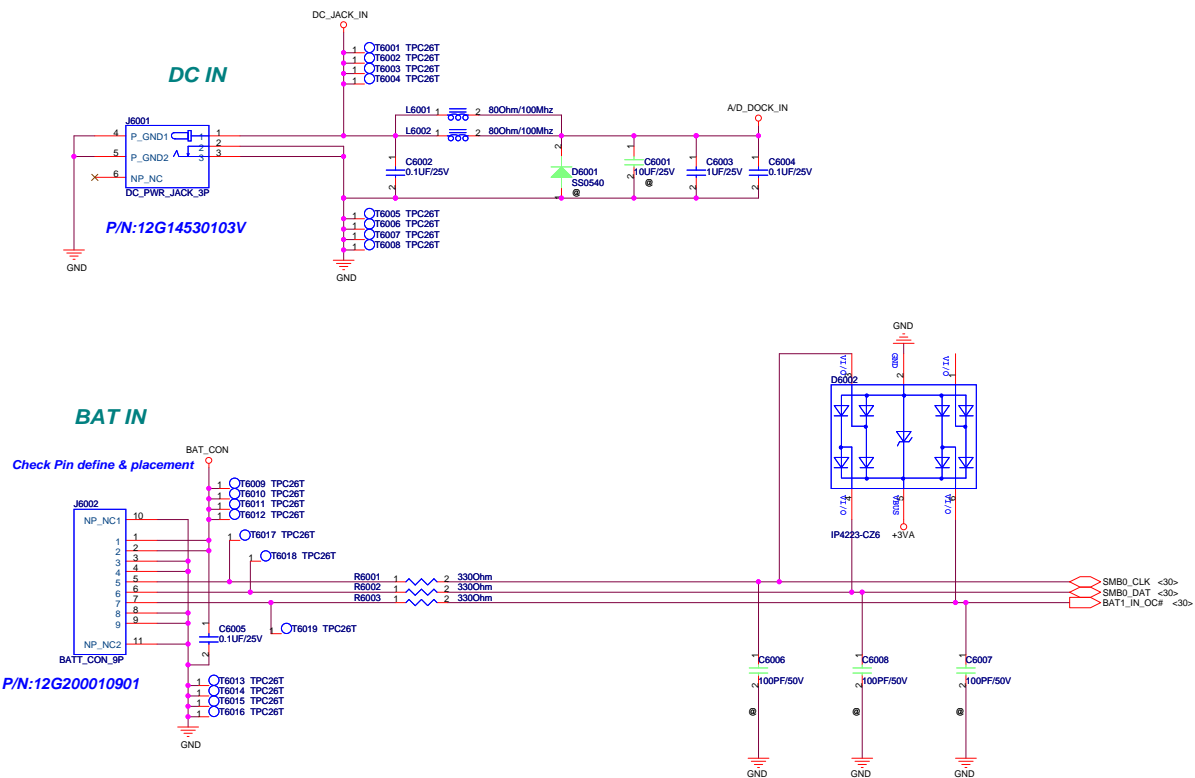
SATA LED

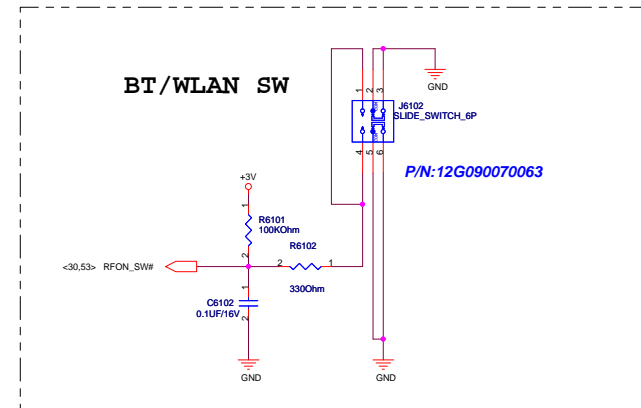
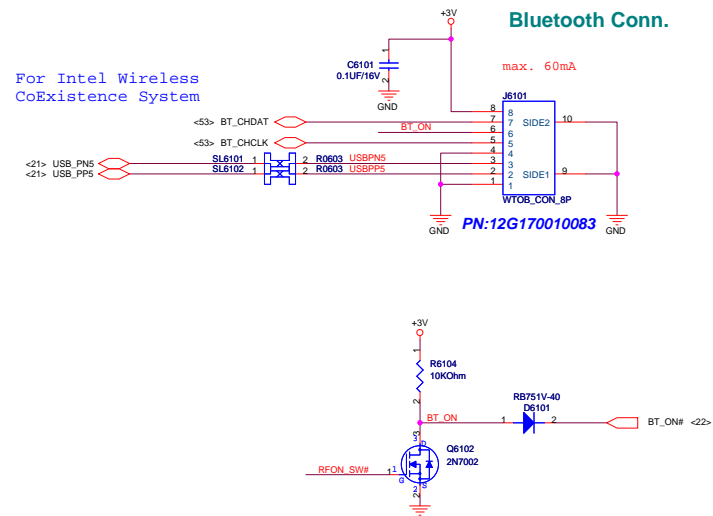
Num Lock

Cap. Lock



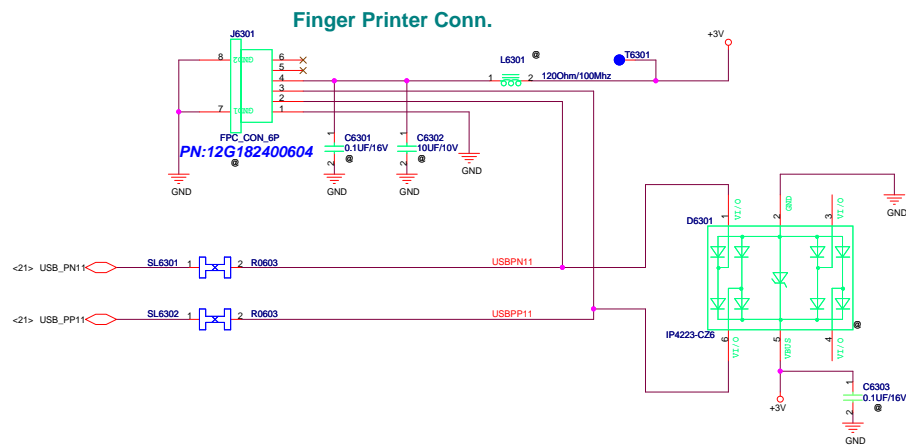


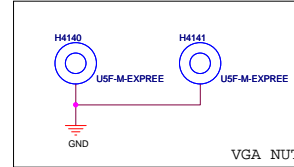
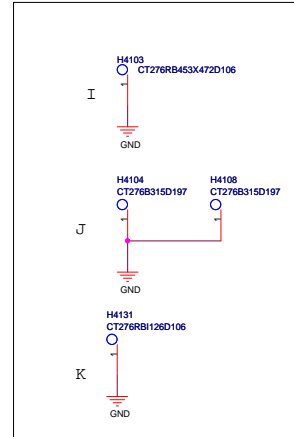
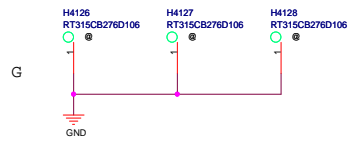
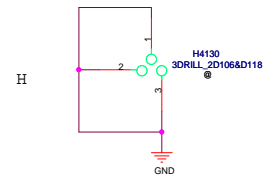
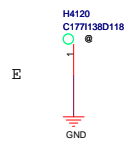
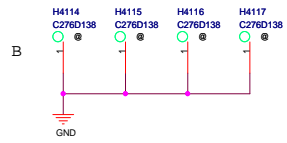
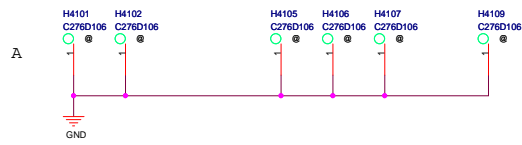




	5	4	3	2	1
D					
C					
B					
A					

PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: Zack Kuo	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009		Sheet 62 of 100	





R1.1

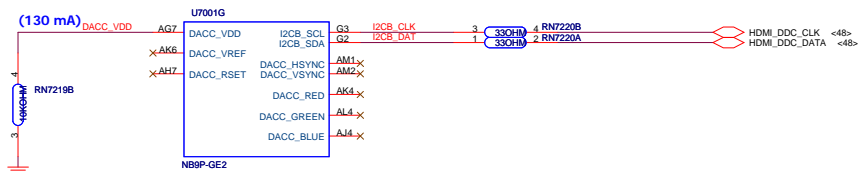
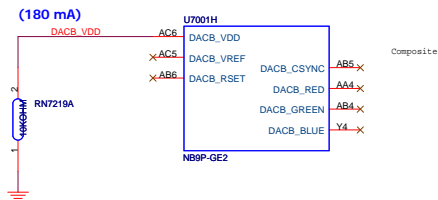
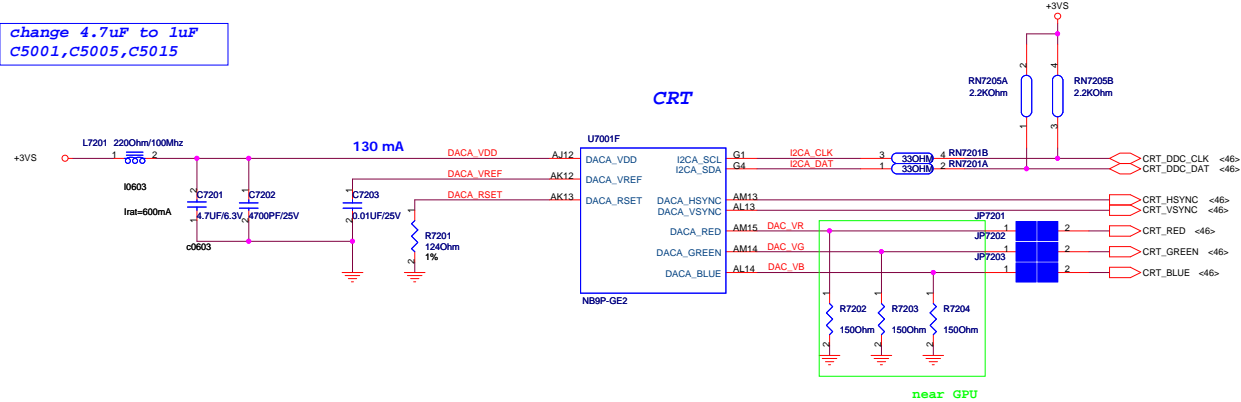
2009/06/30

- 1. Set DDR3 VREF to 0.75V LDO output.
- 2. Change Card Reader to AU6433D53-GLF.
- 3. Change LAN to Atheros AR6132.
- 4. Change Transformer to 10/100 TAIMAG HA003
- 5. Change ClockGen to ICS9LPR363.
- 6. Remove ClockGen 3362 circuits.
- 7. Unstuff Finger Printer Connector.
- 8.

	5	4	3	2	1
D					
C					
B					
A					

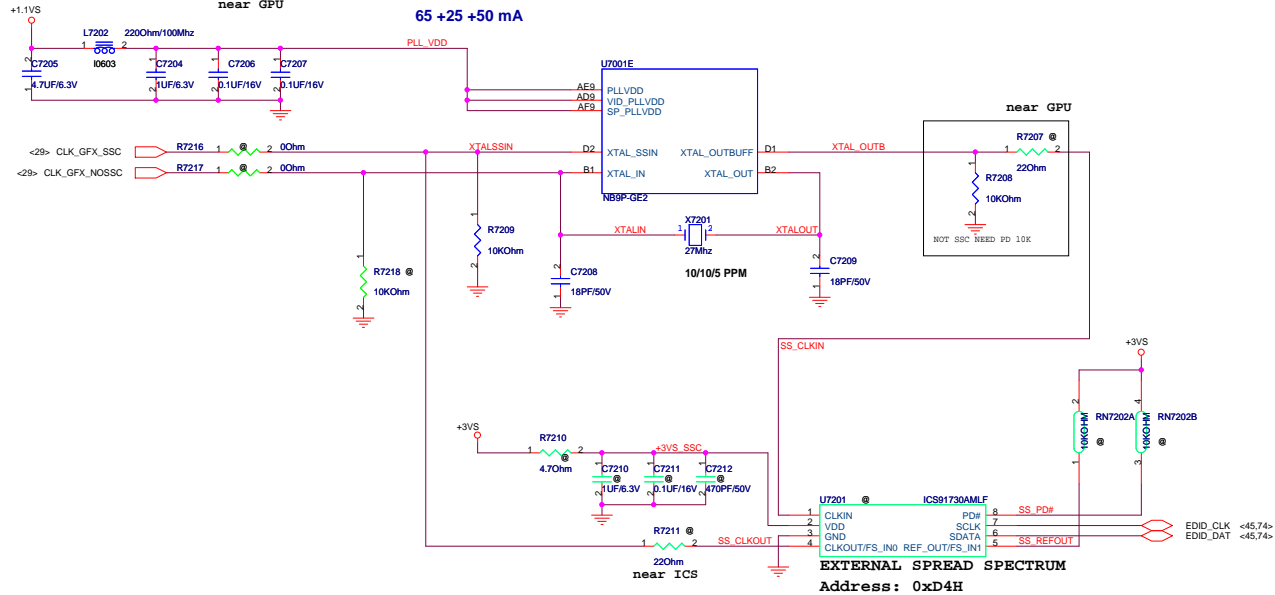
PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <OrgAddr1>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009		Sheet 71 of 100	

change 4.7uF to 1uF
C5001,C5005,C5015

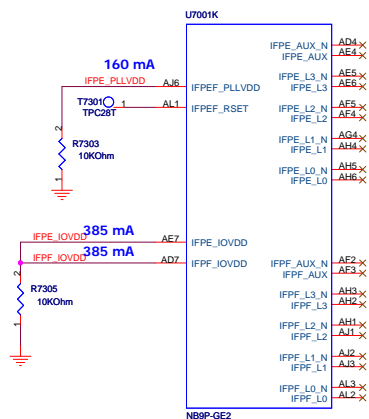
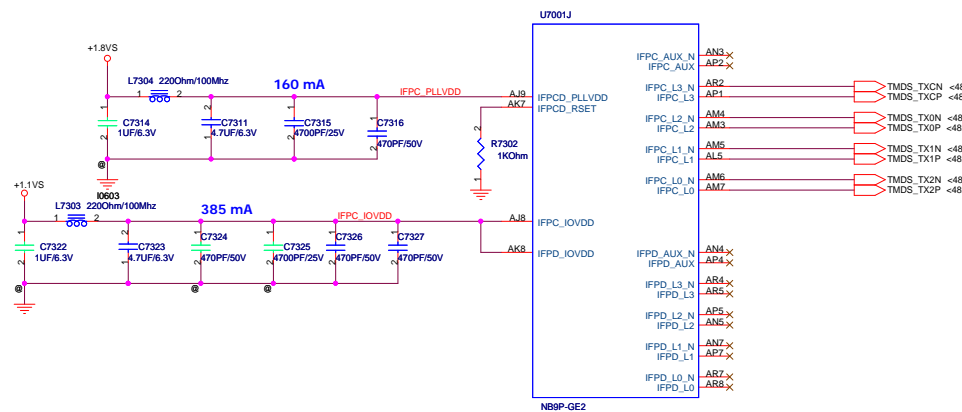
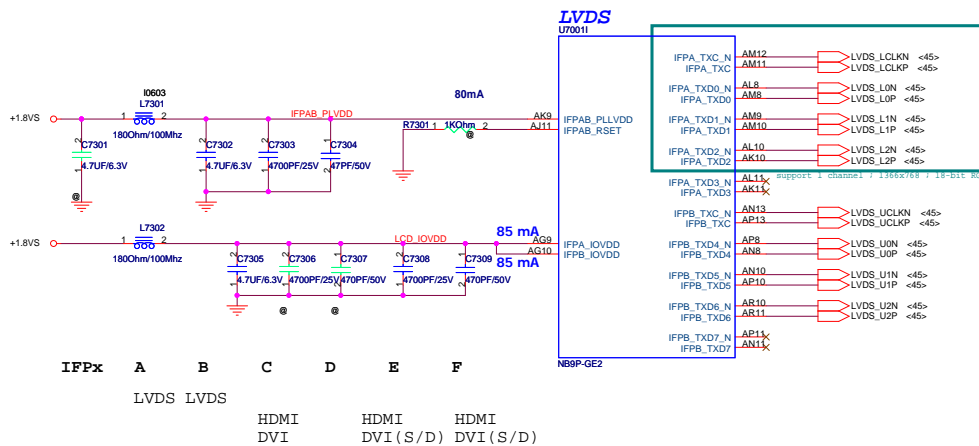


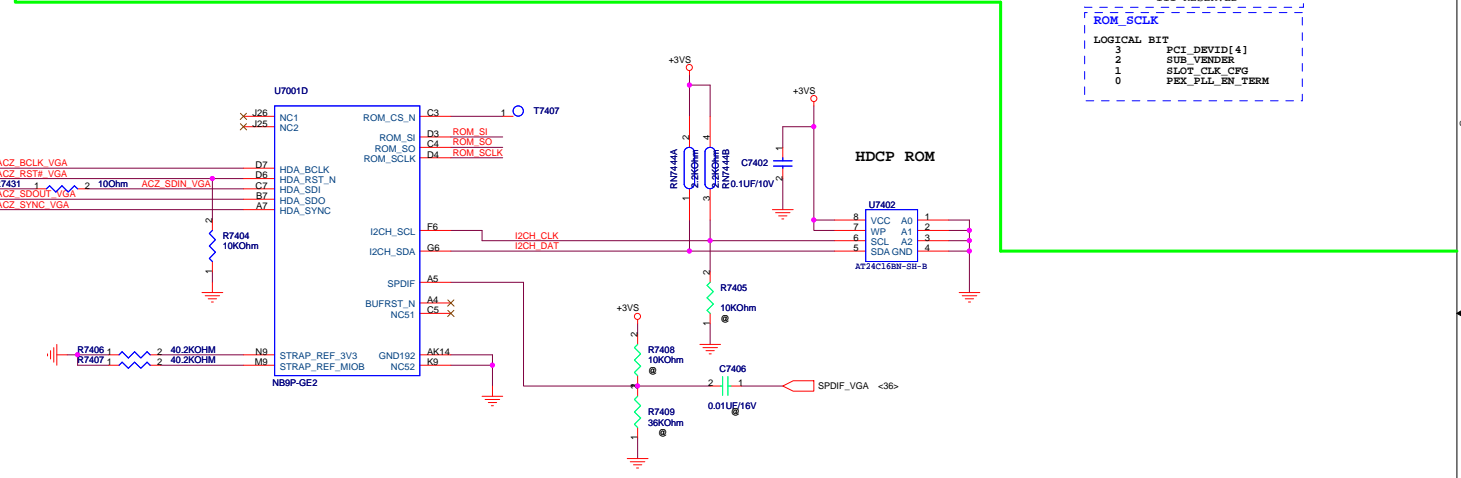
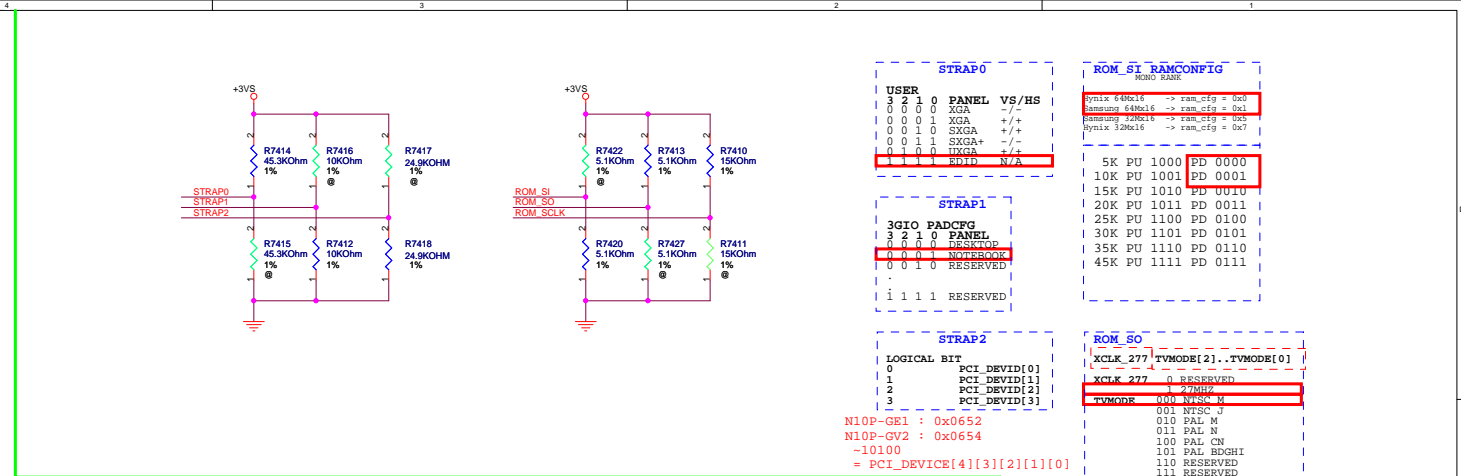
XTAL_IN , XTAL_OUT
3.3V tolerance

correspondent BGA balls must be
12mils and 16 mil wide

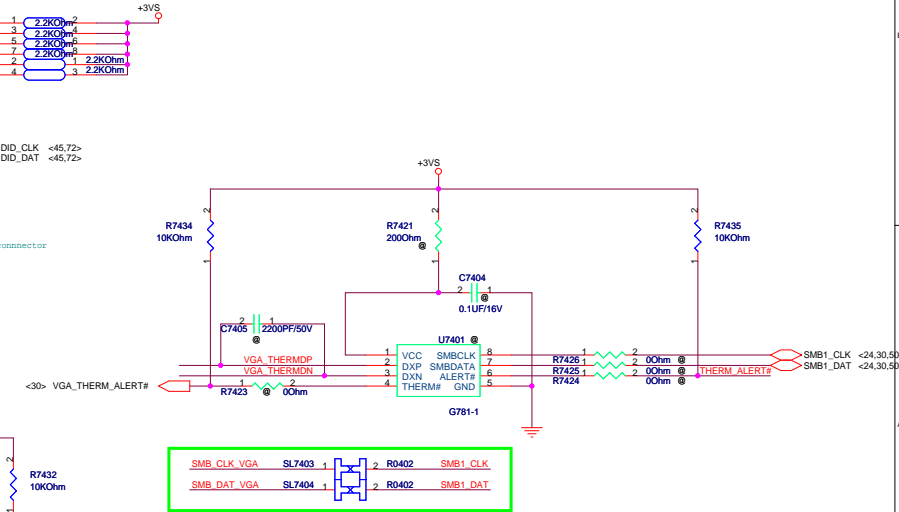


EXTERNAL SPREAD SPECTRUM
Address: 0xD4H

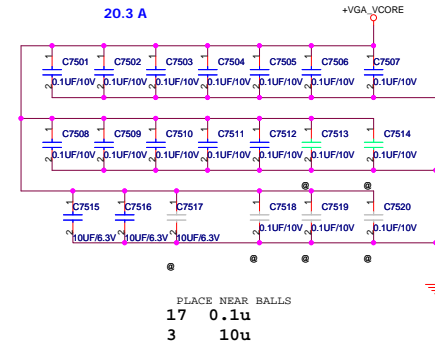
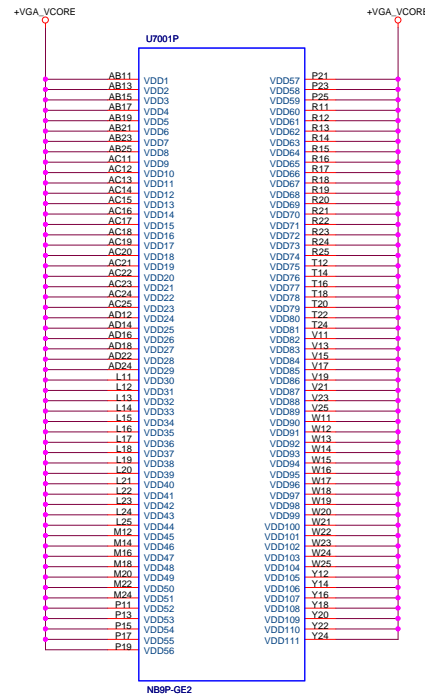
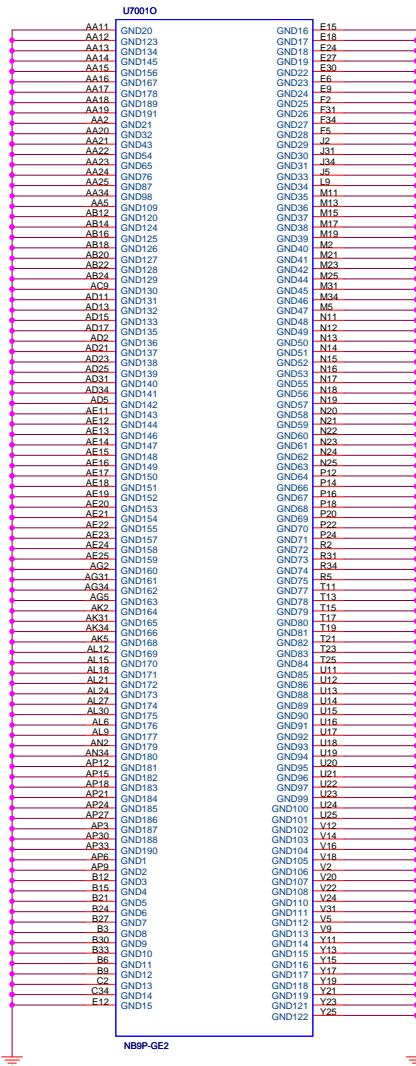


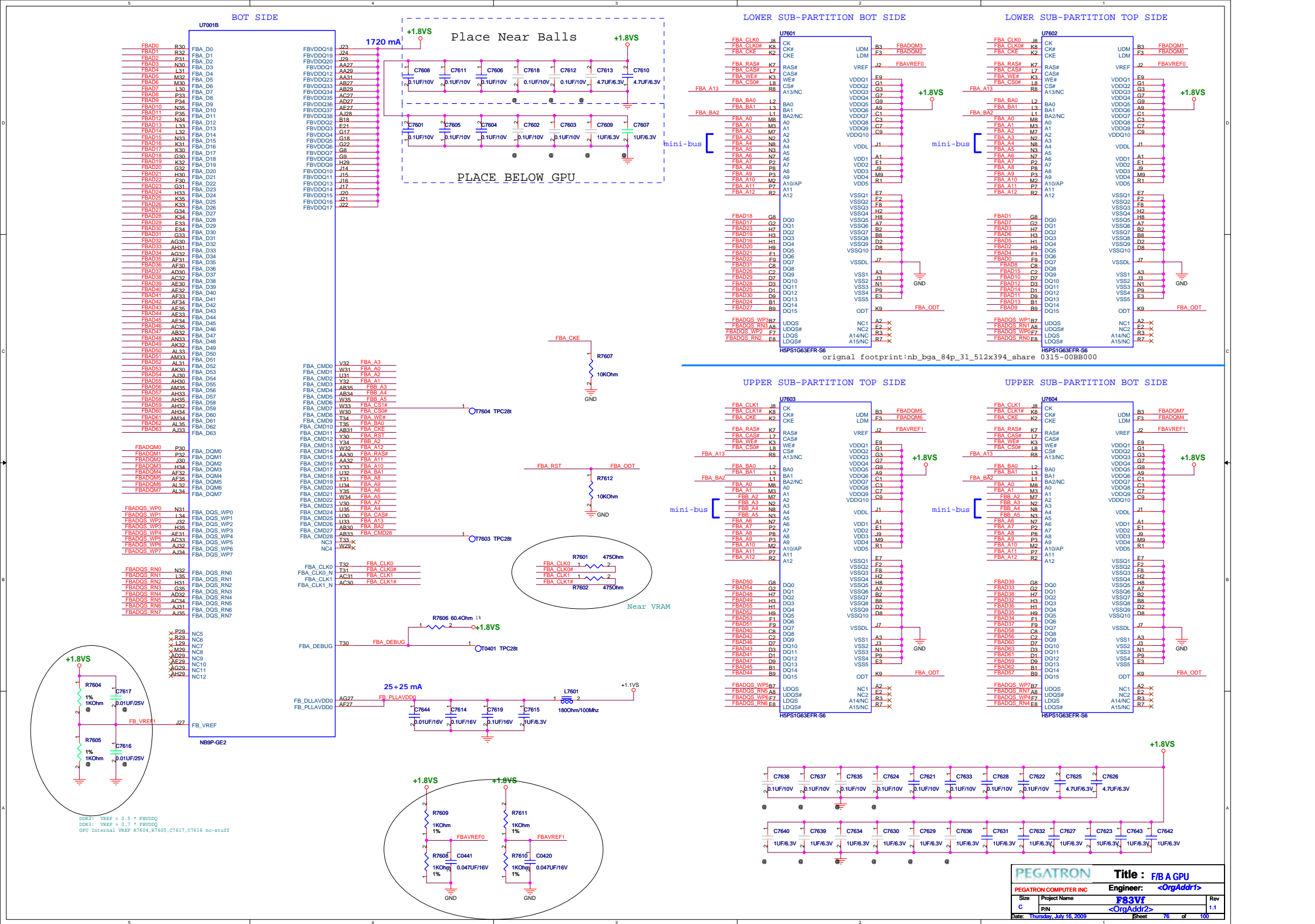


GPU_VID0	VID0	+VGA_VCORE
Low	0	0.9V
High	1	1.10V



PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <OrgAddr1>	
Size C	Project Name F83Vf	Rev 1.1	
Date: Thursday, July 16, 2009	P/N <OrgAddr2>	Sheet 74	of 100

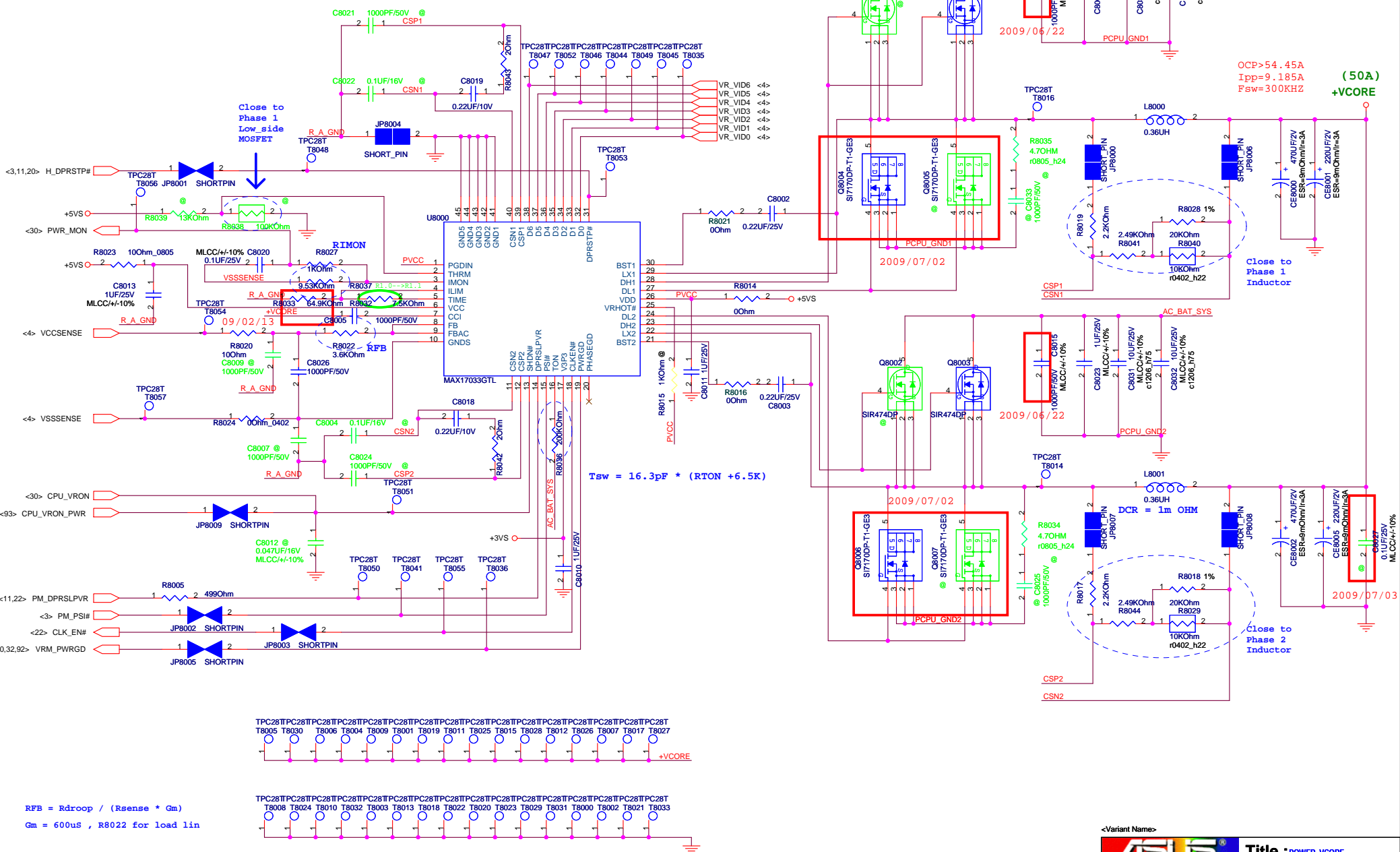





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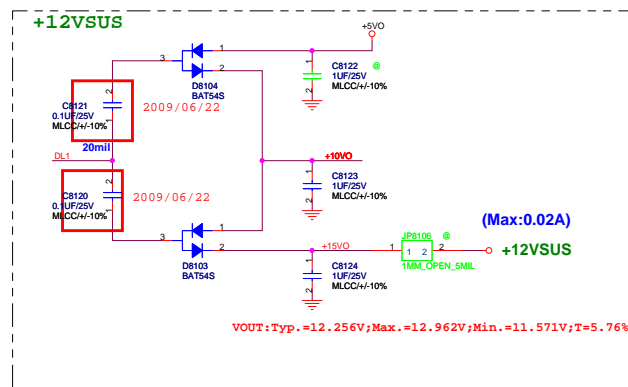
IMON=Gm(IMON) * [ (Vcsp1-Vcsn1) + (Vcsp2-Vcsn2) ]
RIMON = 0.9V / [ IMAX * Rsense(MIN) * Gm(IMON_MIN)]
Gm(IMON) = 2.4mS , Gm(IMON_MIN) = 2.36mS

```


$$R_{FB} = R_{droop} / (R_{sense} * G_m)$$

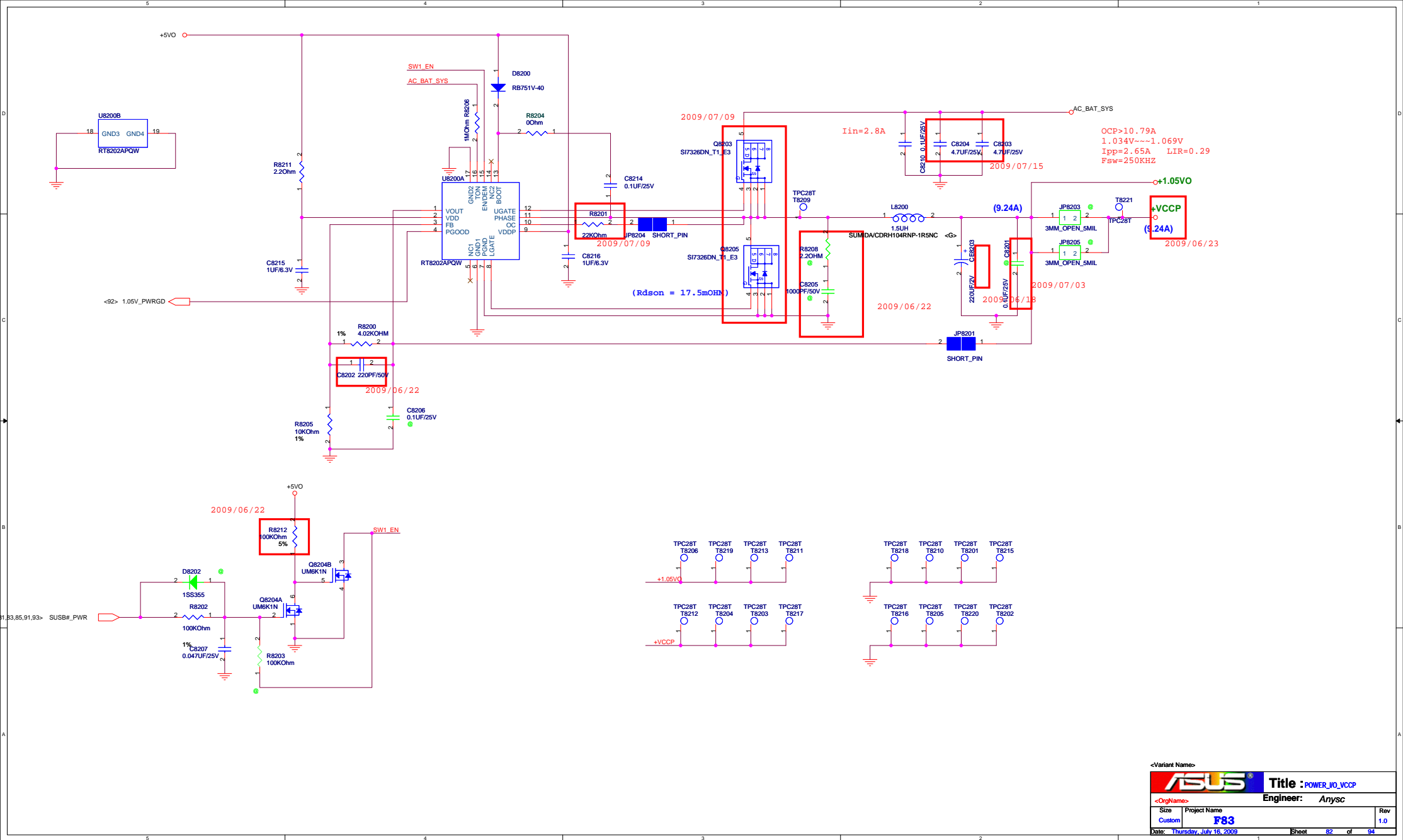
$$G_m = 600\mu S, R_{8022} \text{ for load lin}$$

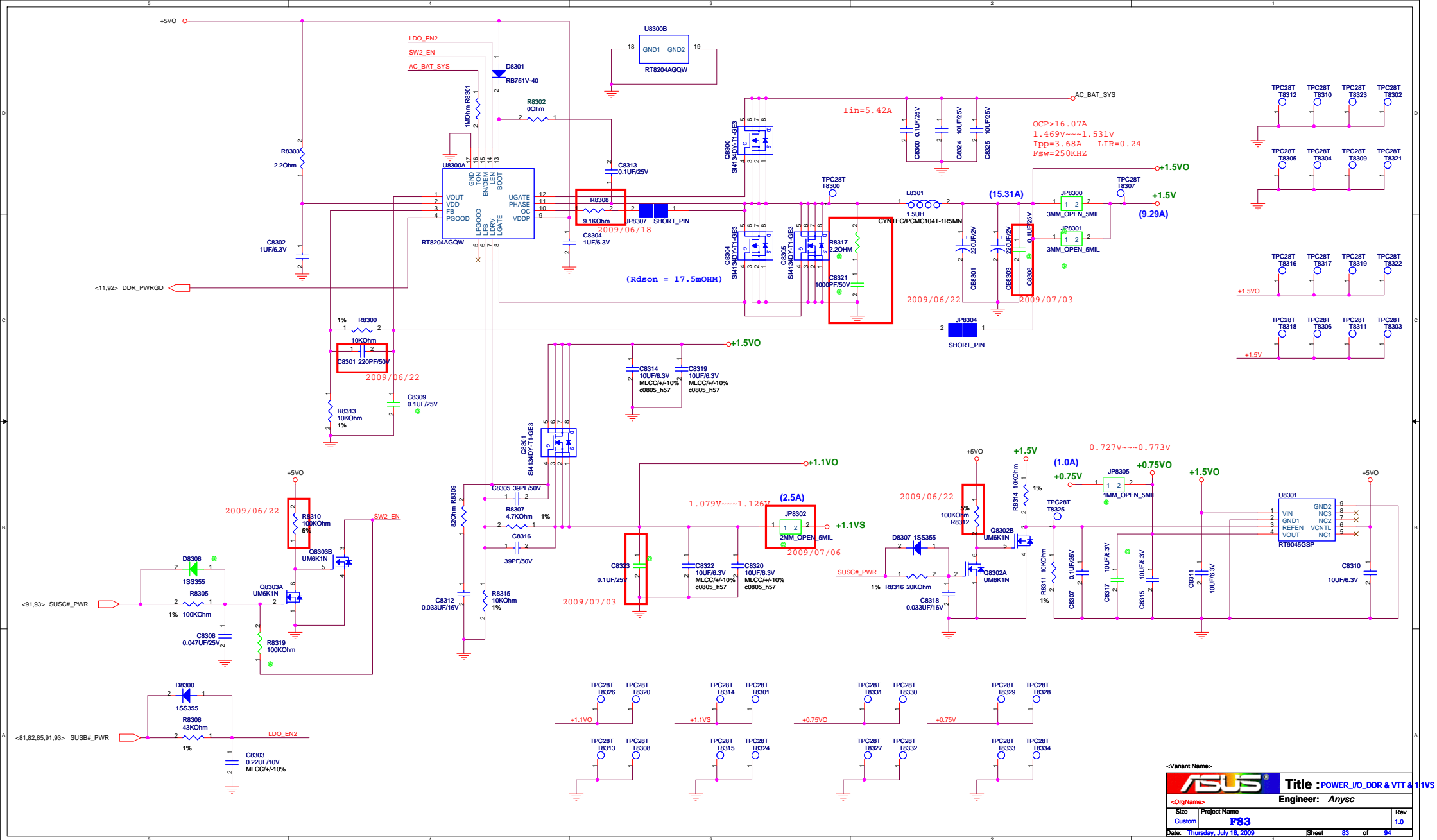
VENLDO:
Rising Edge:Max:2V;Typ:1.6V;Min:1.2V
Falling Edge:Max:1.06V;Typ:1V;Min:0.94V



<Variant Name:








5	4	3	2	1
D				
C				
B				
A				
5	4	3	2	1

<Variant Name>

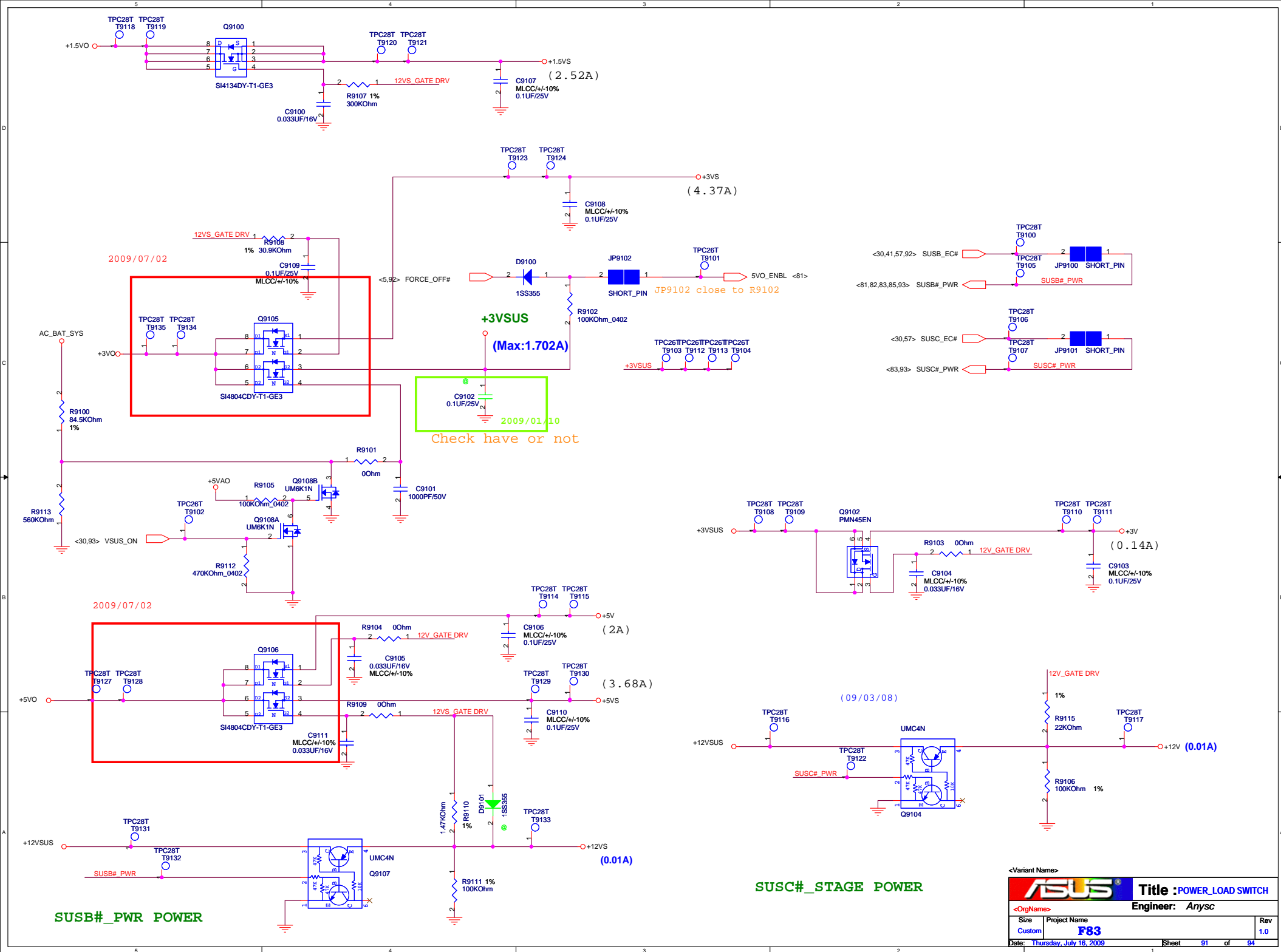
		Title : <i>N/A</i>	
<OrgName>		Engineer: <i>Anyisc</i>	
Size	Project Name		Rev
Custom	F83		1.0
Date: <i>Thursday, July 16, 2009</i>		Sheet	86 of 94

5					4					3					2					1				
D																								
C																								
B																								
A																								
<div><div><Variant Name></div><div><div><div>ASUS®</div><div>Title :<i>N/A</i></div></div><div><div><OrgName></div><div>Engineer: <i>Anysc</i></div></div><div><div><div>Size</div><div>Project Name</div><div>Rev</div></div><div><div>Custom</div><div>F83</div><div>1.0</div></div></div><div><div>Date: <i>Thursday, July 16, 2009</i></div><div>Sheet <i>89</i> of <i>94</i></div></div></div></div>																								
5					4					3					2					1				

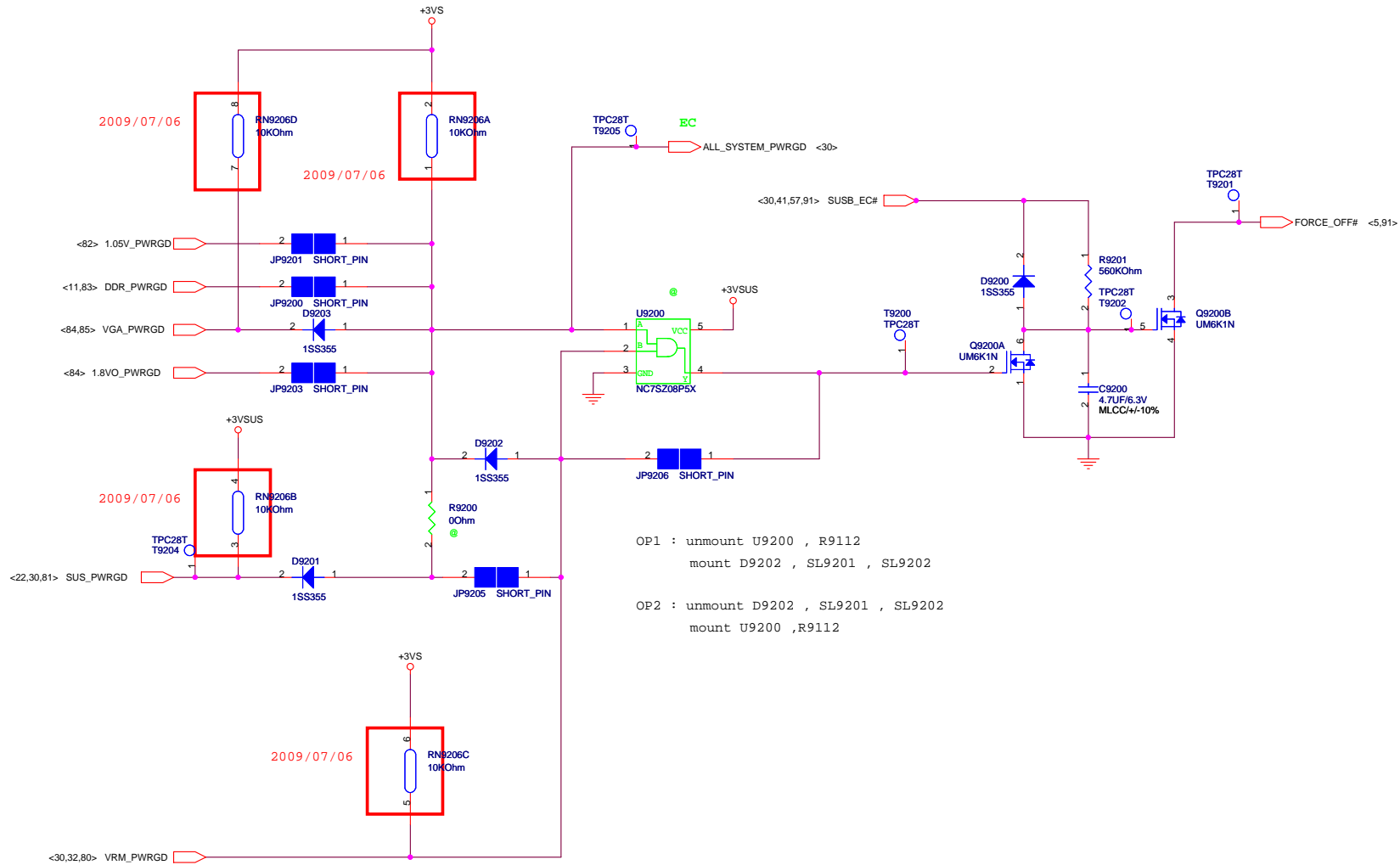
BATTERY IN DETECT

2009/07/08
delete batt detect





POWER GOOD DETECTOR



<Variant Name>

ASUS		Title : POWER_PROTECT	
<OrigName>		Engineer: Anyisc	
Size	Project Name	Rev	
Custom	F83	1.0	
Date: Thursday, July 16, 2009		Sheet	92 of 94

FOR POWER TEST

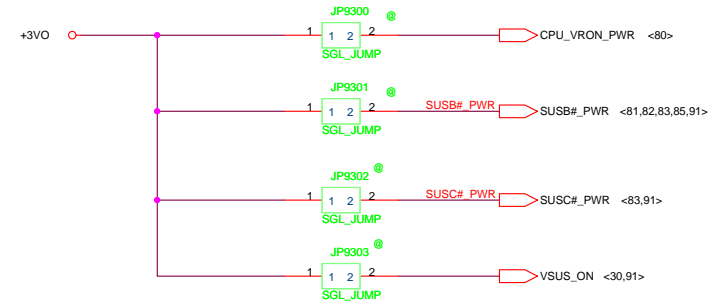
+3VA ○ → +3VA <20,22,30,45,57,60,81>
+3VSUS ○ → +3VSUS <20,21,22,23,24,30,33,37,45,53,56,91,92>
+5VSUS ○ → +5VSUS <23,56,81>
+12VSUS ○ → +12VSUS <24,81,91>

+5VO ○ → +5VO <81,82,83,84,85,91>
+3VO ○ → +3VO <81,91>
+1.05VO ○ → +1.05VO <82>
+1.5VO ○ → +1.5VO <83,91>
+0.75VO ○ → +0.75VO <83>
+1.8VO ○ → +1.8VO <84>
+1.1VO ○ → +1.1VO <83>
+VGA_VCORE_O ○ → +VGA_VCORE_O <85>

+3V ○ → +3V <21,33,41,44,53,57,61,63,91>
+5V ○ → +5V <9,31,44,45,52,57,91>
+12V ○ → +12V <37,91>
+1.5V ○ → +1.5V <7,8,9,11,13,14,57,83>

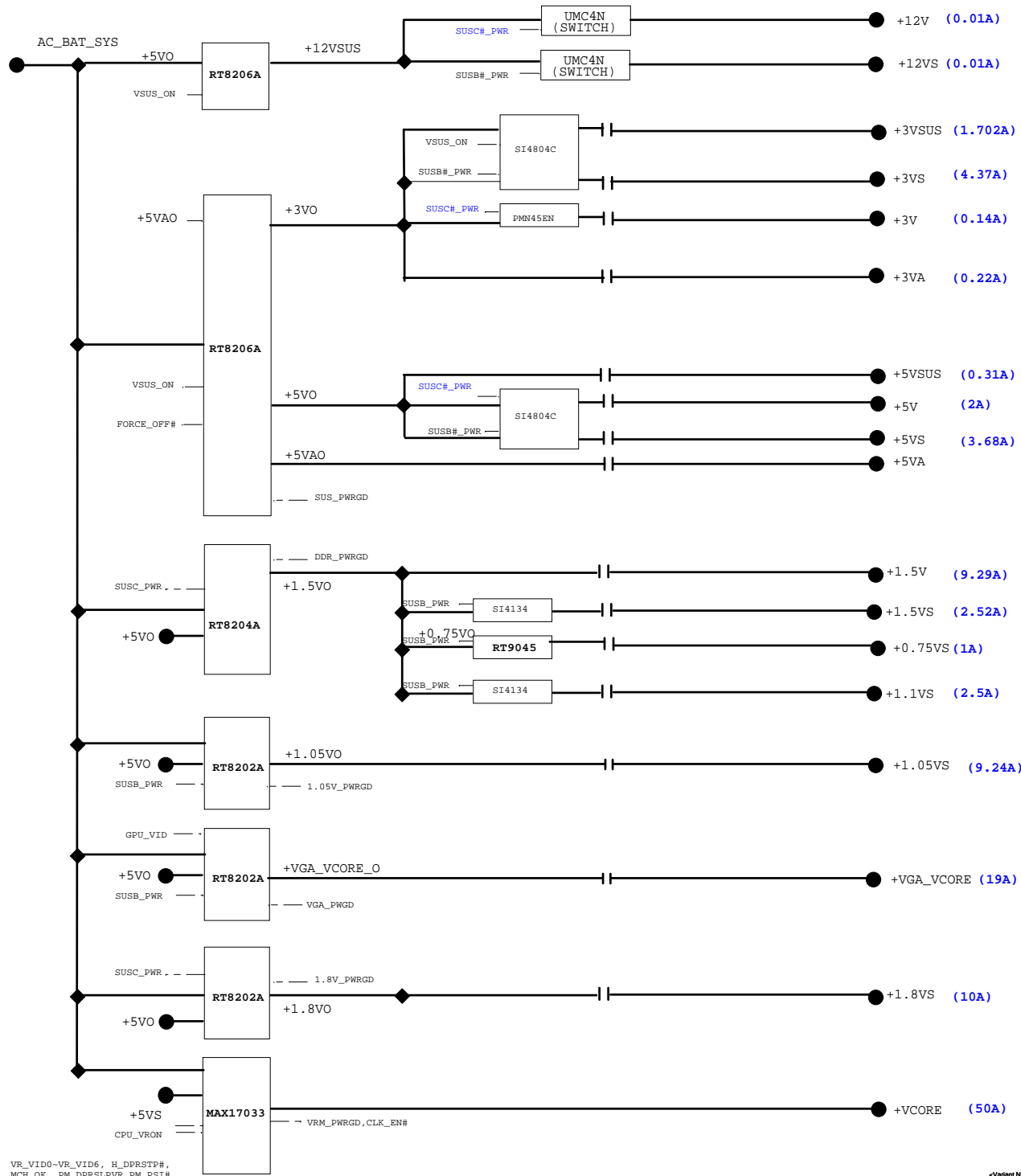
+3VS ○ → +3VS <3,7,8,11,14,15,22,23,24,29,30,32,36,40,41,44,45,46,48,50,51,53,56,57,70,72,74,80,91,92>
+12VS ○ → +12VS <24,40,45,48,57,91>
+5VS ○ → +5VS <23,31,36,46,48,50,51,56,57,80,91>
+1.8VS ○ → +1.8VS <57,73,76,77,84>
+1.5VS ○ → +1.5VS <4,14,23,41,53,57,91>
+VCCP ○ → +VCCP <3,4,5,10,11,13,14,20,23,29,57,82>
+0.75V ○ → +0.75V <7,8,11,83>
+1.1VS ○ → +1.1VS <57,70,72,73,76,77,83>
+VGA_VCORE ○ → +VGA_VCORE <75,85>
+VCORE ○ → +VCORE <4,5,80>

AC_BAT_SYS ○ → AC_BAT_SYS <45,80,81,82,83,84,85,88,91>
BAT ○ → BAT <88>
BAT_CON ○ → BAT_CON <60,88>



<Variant Name>

ASUS		Title : POWER_SIGNAL	
<OrgName>		Engineer: Anysc	
Size Custom	Project Name F83	Rev 1.0	
Date: Thursday, July 16, 2009		Sheet 93 of 94	



VR_VID0-VR_VID6, H_DPRSTP#,
MCH_OK, PM_DPRS1PVR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: Colin Chang	
Size	Project Name	Vx5	Rev
C	P/N	<OrgAddr2>	1.0
Date: Thursday, July 16, 2009		Sheet 99 of 100	