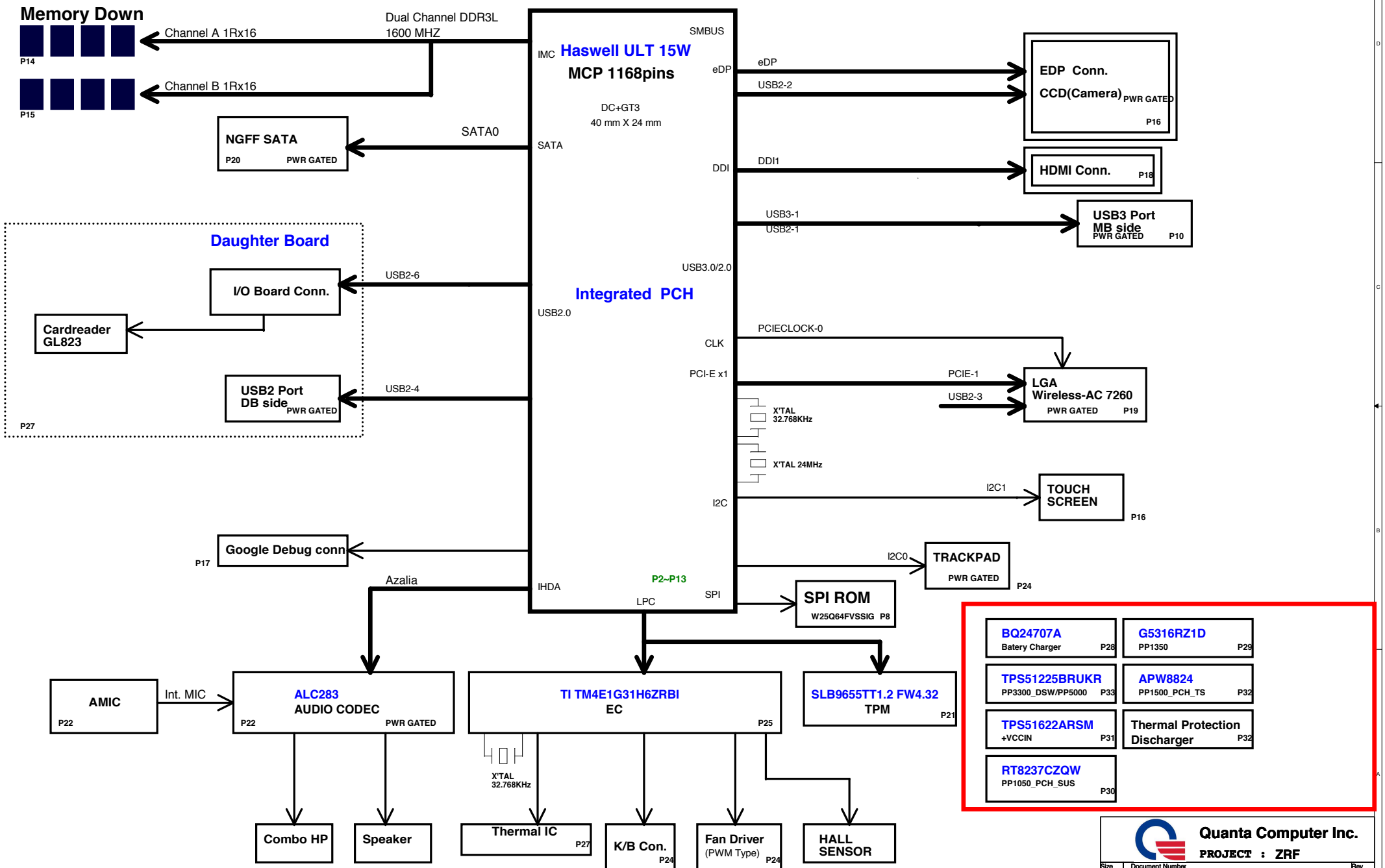
Melvita (ZRF) SHB ULT SYSTEM BLOCK DIAGRAM

01



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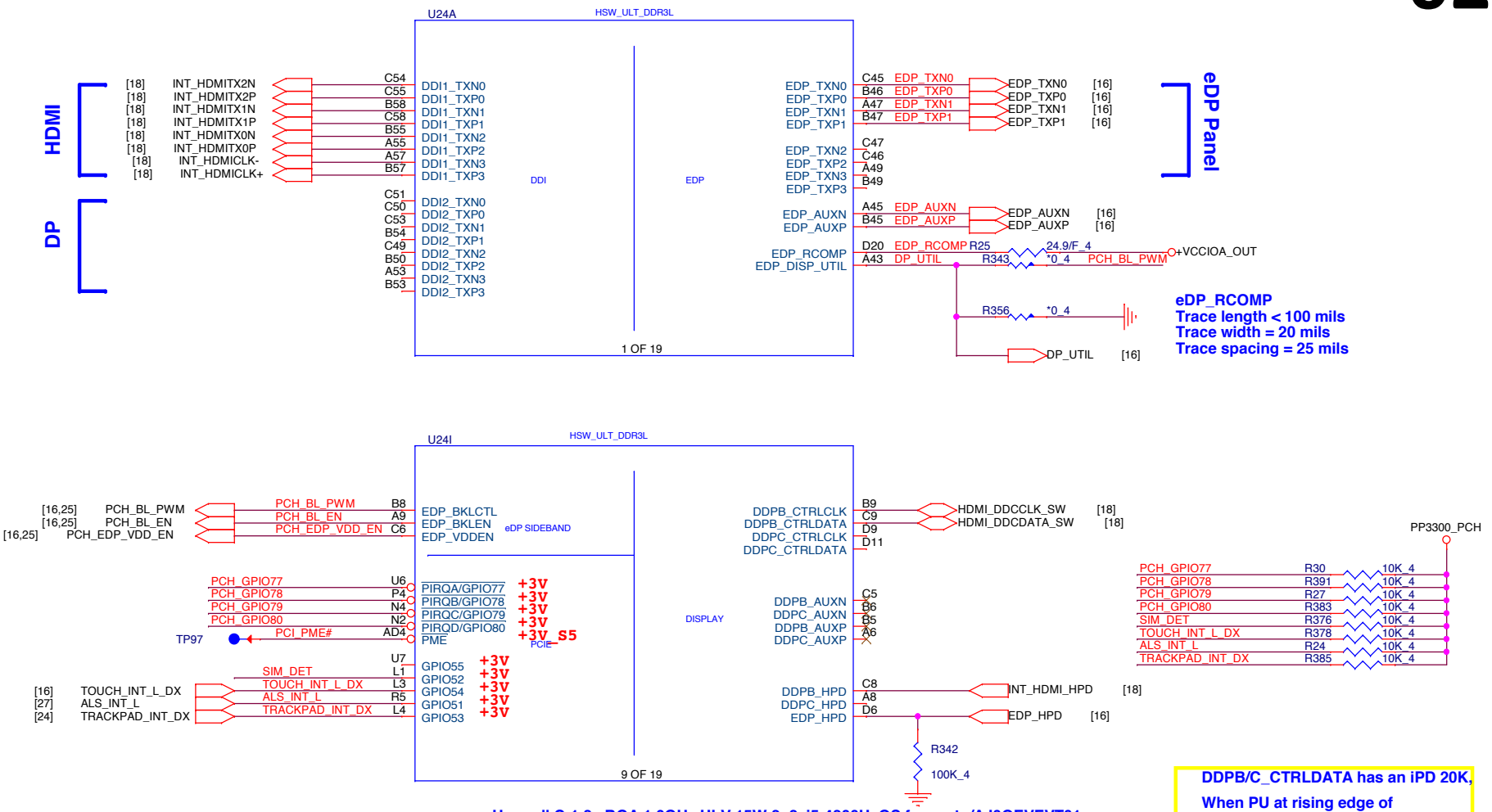
Haswell ULT (DISPLAY,eDP)

02



Haswell C-1 2c BGA 1.6GHz ULV 15W 2+2 i5-4200U QS for proto/AJ0QEVEVT01

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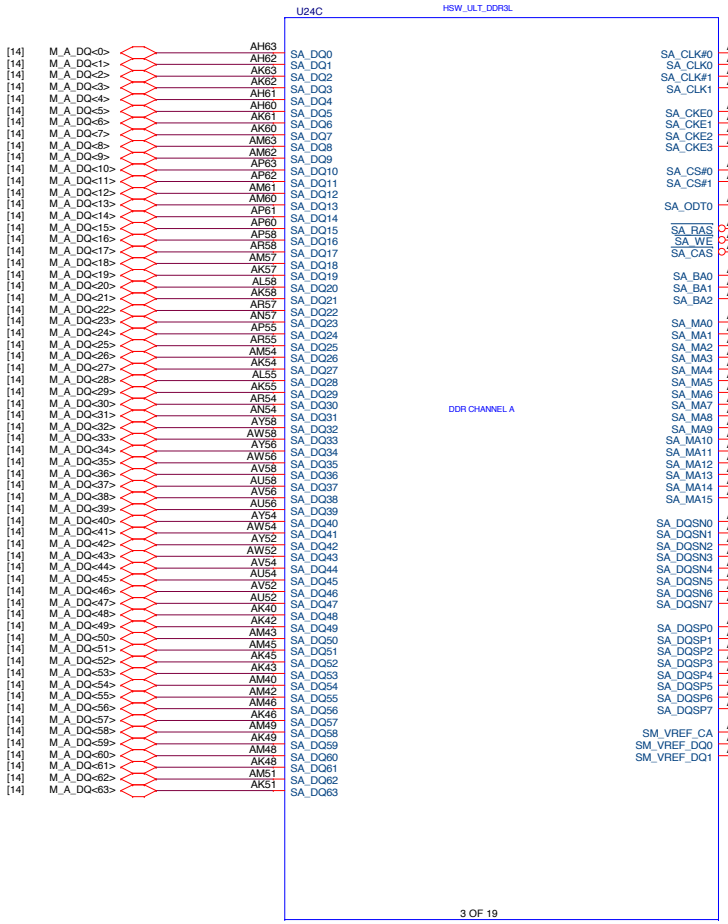
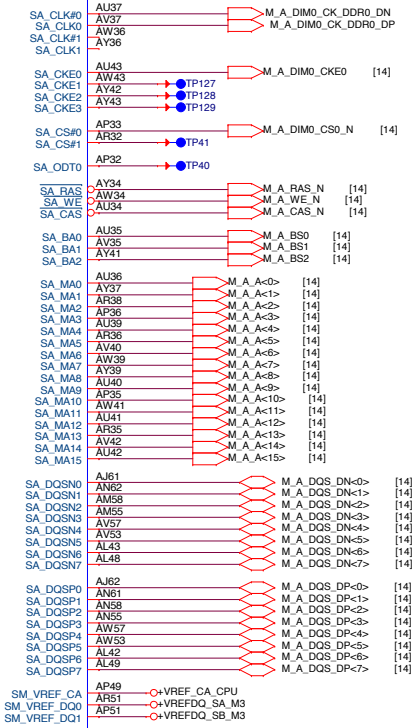
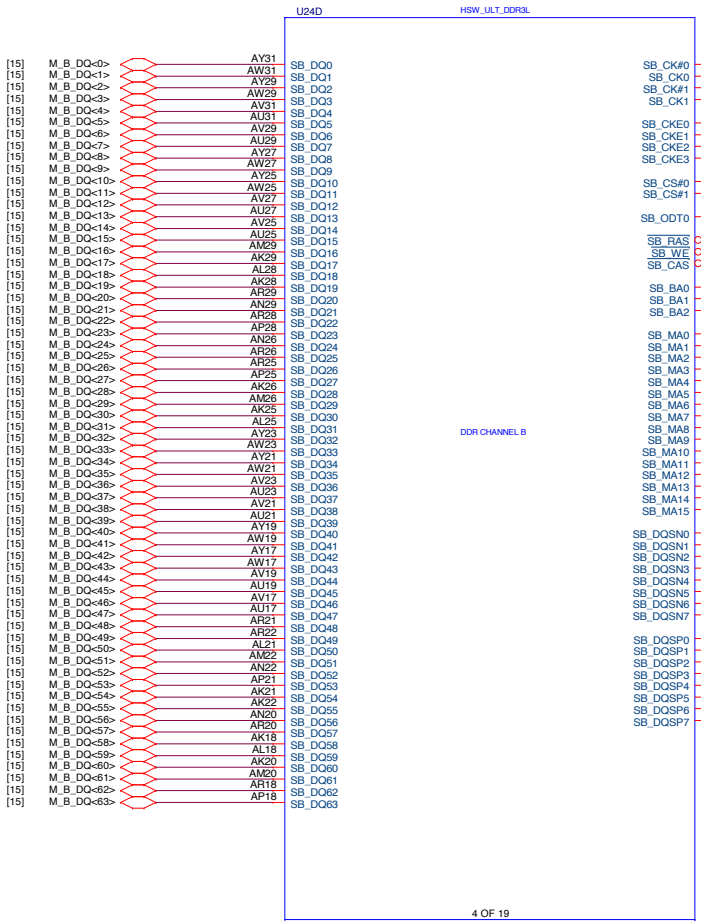
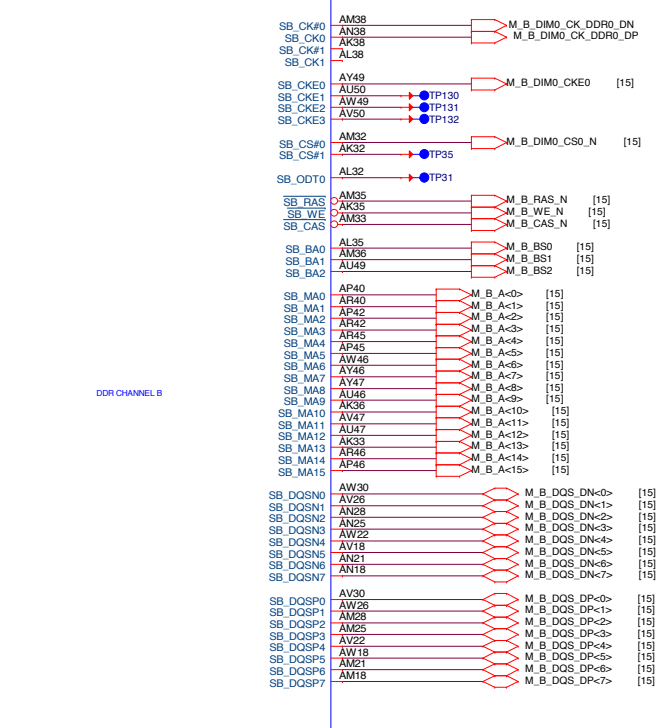
Haswell ULT (DDR3L)





Haswell Processor (DDR3L)





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	Haswell 2/5 (DDR3 I/F)	A
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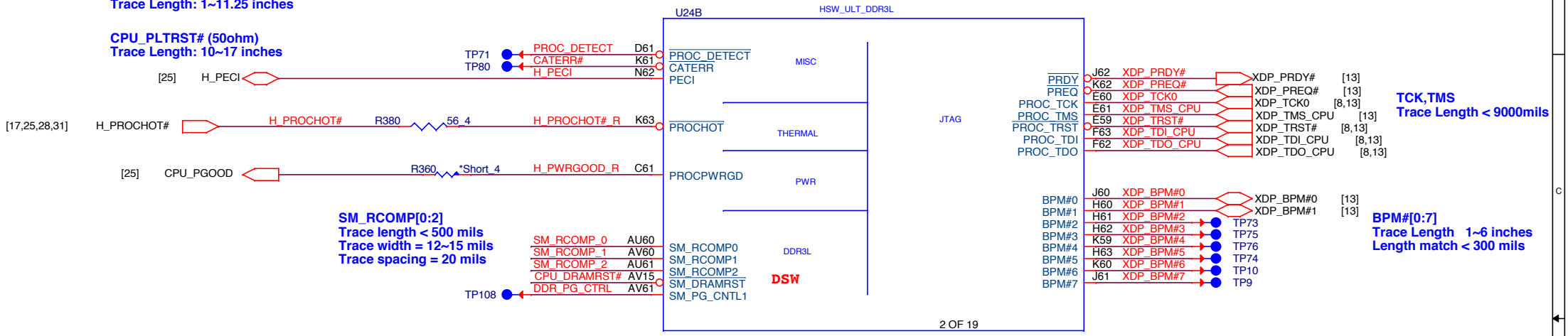
04

Haswell ULT (SIDEBAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

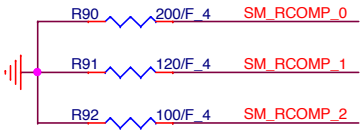


TCK,TMS
Trace Length < 9000mils

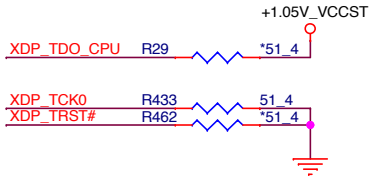
SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

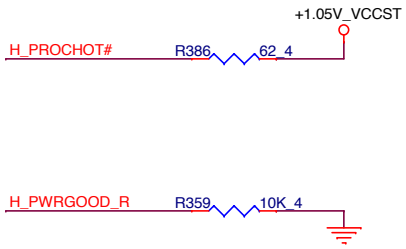
DRAM COMP



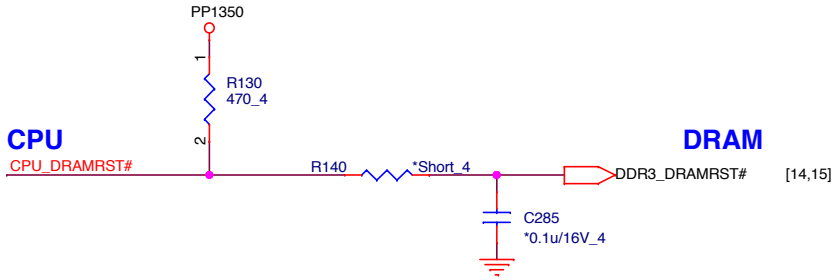
XDP PU/PD



PU/PD of CPU



DRAMRST



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	Haswell 3/5 (SideBand)	A
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Haswell ULT (POWER)

05

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

SVID

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to CPU

Place PU resistor close to CPU

VCCST PWRGD

20141205 EOD parts, change PN.

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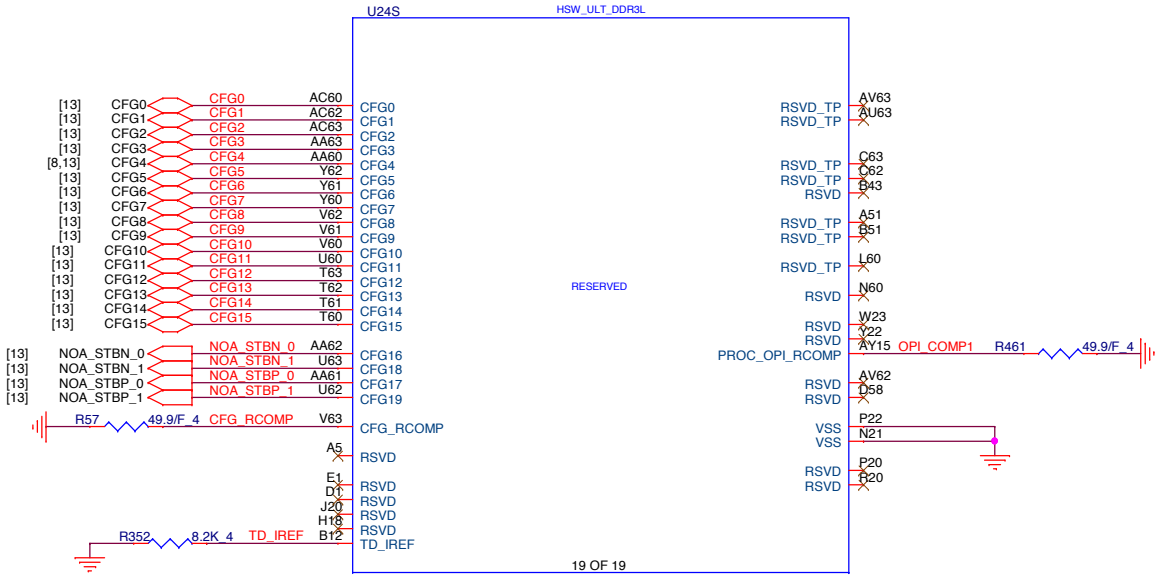
Haswell ULT (CFG,RSVD)

06



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R417 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R423 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R409 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R403 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R394 *1K_4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R56 *1K_4

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	Haswell 5/5 (CFG/GND)	A

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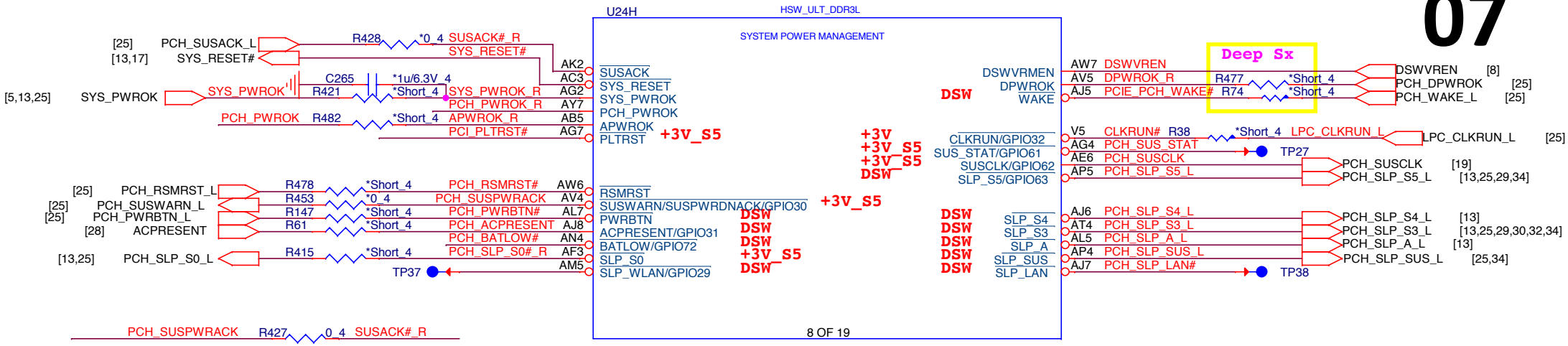
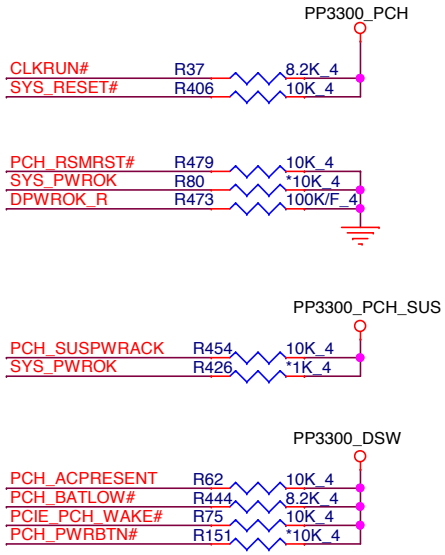
Haswell ULT PCH (PM)

07

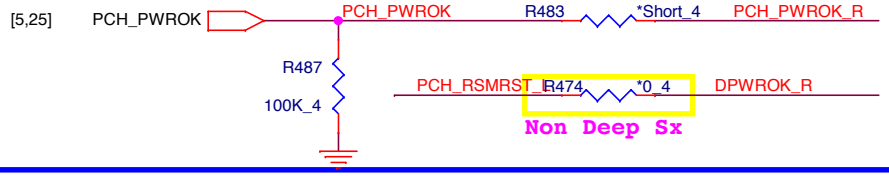


4/22 modify, default skip EC control

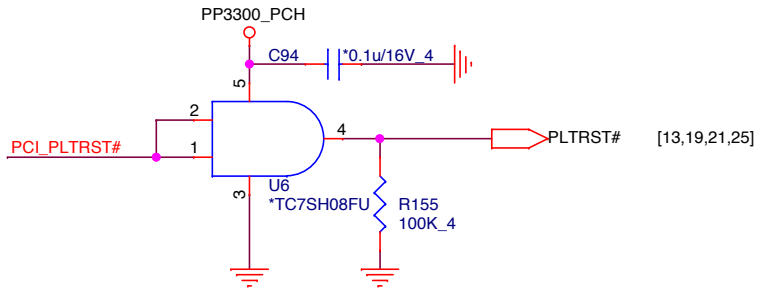
PCH PM PU/PD



PCH PWROK



PLTRST# Buffer



4/22 modify, default is bypass PLTRST#

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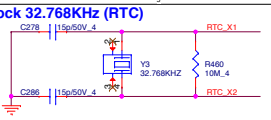
Haswell ULT PCH (RTC/HDA/SATA/SPI)

Haswell ULT PCH(LPC,SPI,SMBUS,C-LINK,THERMAL)

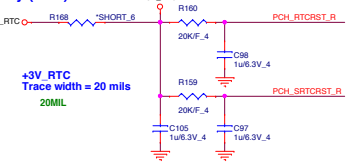
08

RTC Clock 32.768KHz (RTC)

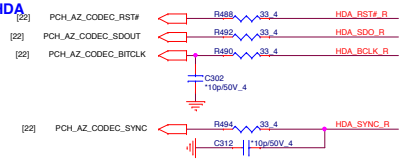


RTC Circuitry (RTC)

+3V_RTC
Trace width = 30 mils



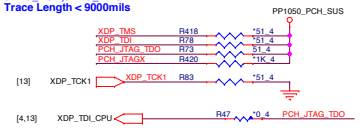
HDA



PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

MP remove(Intel)

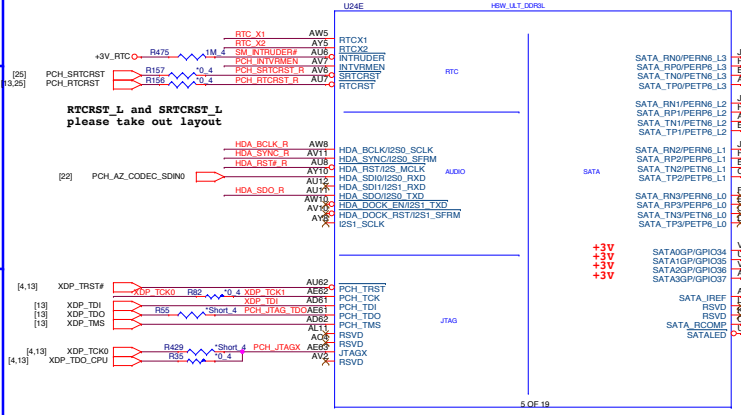


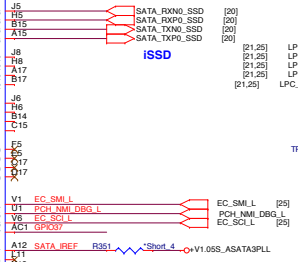
ULT Strapping Table

Note: R493 need stuff on MP.

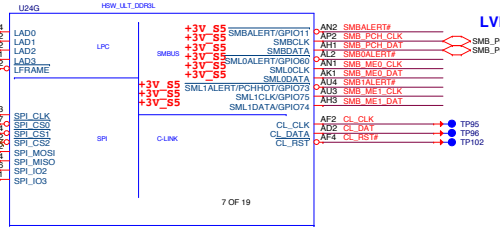
Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (iPD 20K) 1 =Disable No-Reboot mode	PP3300_PCH R400 *1K_4 SPKR — SPKR [10,22]
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (iPD 20K) 1 =can't program ME	HDA_SDO_R R493 *0_4 PCH_HDA_SDO [25]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	+3V_RTC R484 330K_4 PCH_INTVRMEN R485 *330K_4
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	[10] GPIO66 — PP3300_PCH R330 *1K_4 GPIO66 R340 *1K_4
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (iPD 20K) 1 =LPC	[10] GPIO86 — PP3300_PCH R1 *1K_4 GPIO86 R7 *1K_4
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	[10] GPIO15 — PP3300_PCH_SUS R50 *8.2K_4 GPIO15 R58 *1K_4 x86 stuff
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 =disable	[6,13] CFG4 — CFG4 R64 1K_4
DSWVREN	Deep Sx well on die VR enable		1=Should be always pull-up	[7] DSWVREN — +3V_RTC R476 330K_4 DSWVREN R472 *330K_4

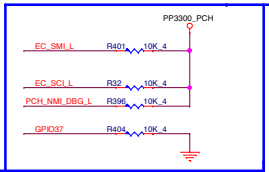
Haswell ULT PCH (RTC/HDA/SATA/SPI)



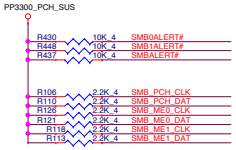


LVDS Bridge



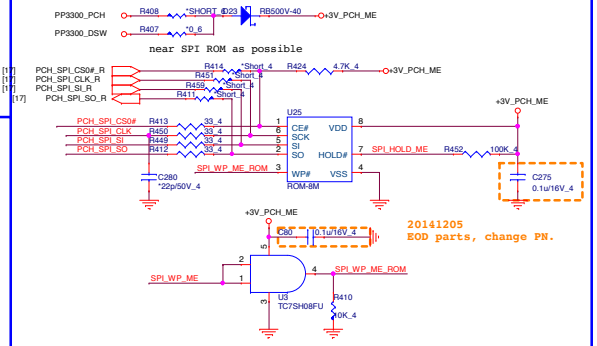


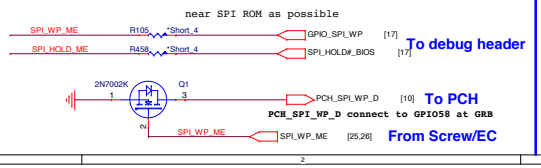
SMBus



PCH dual I/O SPI ROM

W25Q64FVSSIG(SOIC) / AKE3EFPON06------>8MB





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	PCH 2/6 (RTC/HDA/SATA/SPI)	A
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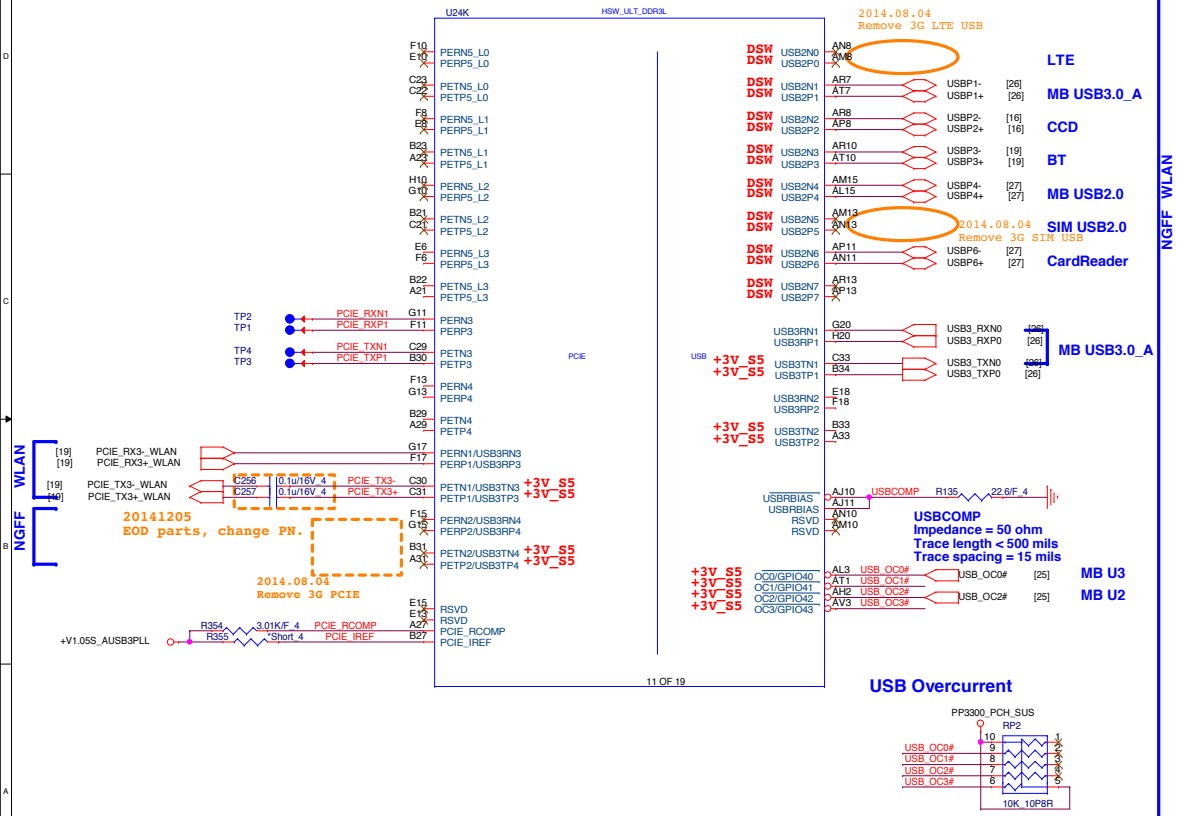
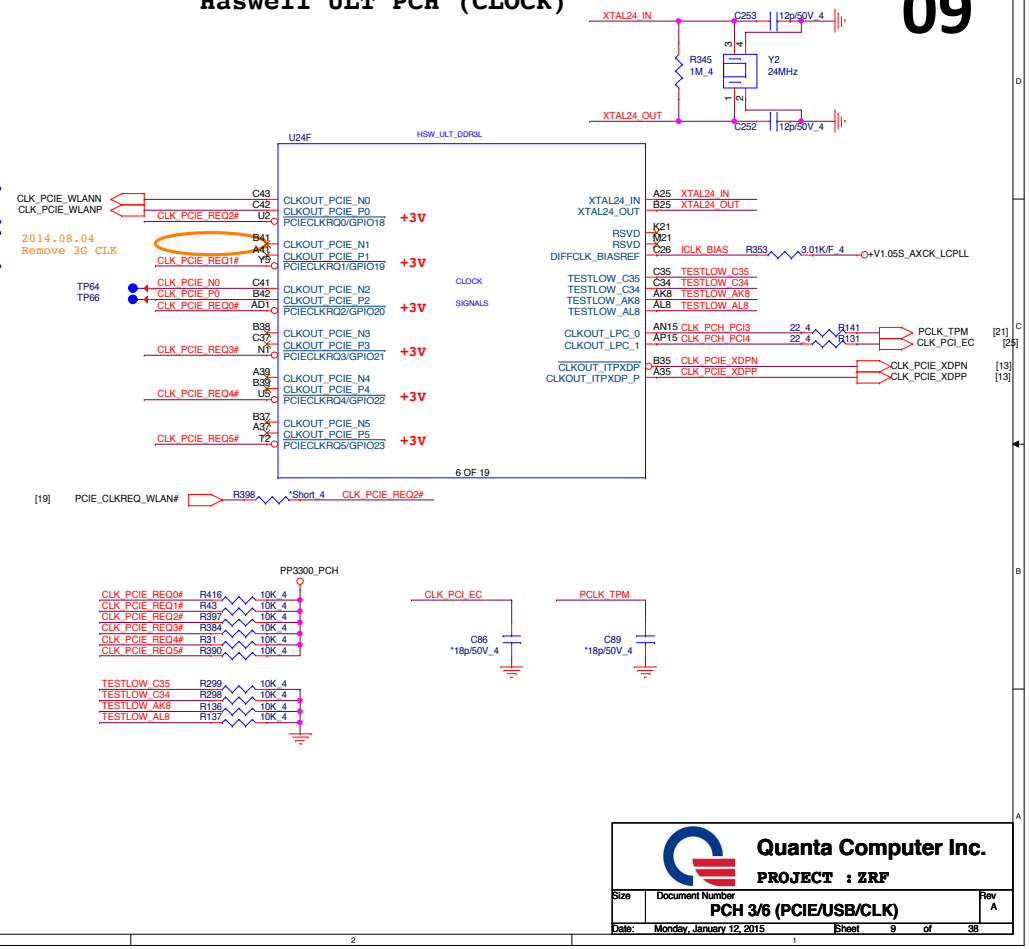
Haswell ULT PCH (PCIE,USB3.0,USB2.0)



Haswell ULT PCH (CLOCK)

09



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Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

U24J — HSW_ULT_DDR3L — 10 OF 19

PCH_GPIO76 P1 BMBUSY/GPIO76 +3V
LTE_WAKE_L_Q AU2 GPIO8 +3V_S5
[24] TRACKPAD_INT_L TRACKPAD_INT_L AM7 LAN_PHY_PWR_CTRL/GPIO12 DSW
[8] GPIO15 AD6 GPIO15 +3V_S5
PCH_SSD_12_EN Y1 GPIO16 +3V
PCH_SSD_18_EN T3 GPIO17 +3V
TP19 GPIO24 AD5 GPIO24 +3V_S5
WK_GPIO27 AN5 GPIO27 DSW
TP20 GPIO28 AD7 GPIO28 +3V_S5
ODD_PRSNT# AN3 GPIO26 +3V_S5

LTE_DISABLE_L need PU to +3V_LTE

TP28 GPIO56 AG6 GPIO56 +3V_S5
PP3300_CCD_EN AP1 GPIO57 +3V_S5
[8] PCH_SPI_WP_D PCH_SPI_WP_D AL4 GPIO58 +3V_S5
20140807 Remove 3G, GPIO pull high. LTE_DISABLE_L AT5 GPIO59 +3V_S5
PP3300_SSD_EN AK4 GPIO44 +3V_S5
RAM_ID2 AB6 GPIO47 +3V_S5
TPM_LP_EN_L U4 GPIO48 +3V
PP3300_SSD_IO_EN Y3 GPIO49 +3V
GPIO50 P3 GPIO50 +3V
[11] MODPHY_EN MODPHY_EN Y2 HSIOPC/GPIO71 +3V
RAM_ID0 AT3 GPIO13 +3V_S5
[24] EC_IN_RW R88 *Short_4 GPIO14 AH4 GPIO14 +3V_S5
[16] TOUCH_INT_L TOUCH_INT_L AM4 GPIO25 DSW
[22] PP5000_CODEC_EN AG5 GPIO45 +3V_S5
[19] WLAN_DISABLE_L AG3 GPIO46 +3V_S5
RAM_ID1 AM3 GPIO9 +3V_S5
WLAN_WAKE_L_Q AM2 GPIO10 +3V_S5
[20] DEVSLP0 DEVSLP0 P2 DEVSLP0/GPIO33 +3V +3V
GPIO70 C4 SDIO_POWER_EN/GPIO70
GPIO38 L2 DEVSLP1/GPIO38 +3V
GPIO39 N5 DEVSLP2/GPIO39 +3V
[8,22] SPKR SPKR V2 SPKR/GPIO81 +3V

CPU/MISC: THRMTRIP, RCIN/GPIO82, SERIRQ, PCH_OPI_RCOMP, RSVD, RSVD

D60 THRMTRIP# — V4 EC_RCIN_L — T4 IRQ_SERIRQ — AW15 OPI_COMP2 R463 49.9/F_4 — AF20 — AB21

EC_RCIN_L [25]
IRQ_SERIRQ [21,25]

GPIO: GSPI0_CS/GPIO83, GSPI0_CLK/GPIO84, GSPI0_MISO/GPIO85, GSPI0_MOSI/GPIO86, GSPI1_CS/GPIO87, GSPI1_CLK/GPIO88, GSPI1_MISO/GPIO89, GSPI1_MOSI/GPIO90, UART0_RXD/GPIO91, UART0_TXD/GPIO92, UART0_RTS/GPIO93, UART0_CTS/GPIO94, UART1_RXD/GPIO0, UART1_TXD/GPIO1, UART1_RST/GPIO2, UART1_CTS/GPIO3, I2C0_SDA/GPIO4, I2C0_SCL/GPIO5, I2C1_SDA/GPIO6, I2C1_SCL/GPIO7, SDIO_CLK/GPIO64, SDIO_CMD/GPIO65, SDIO_D0/GPIO66, SDIO_D1/GPIO67, SDIO_D2/GPIO68, SDIO_D3/GPIO69

R6 GPIO83
L6 GPIO84
N6 GPIO85
L8 GPIO86 — GPIO86 [8] **strapping**
R7 GPIO87
L5 GPIO88
N7 GPIO89
K2 GPIO90
J1 GPIO91
K3 GPIO92
J2 GPIO93
G1 GPIO94
K4 GPIO0
G2 GPIO1
J3 GPIO2
J4 GPIO3
F2 I2C0_SDA_GPIO4 — I2C0_SDA_GPIO4 [24]
F3 I2C0_SCL_GPIO5 — I2C0_SCL_GPIO5 [24] **TRACKPAD**
G4 I2C1_SDA_GPIO6 — I2C1_SDA_GPIO6 [16,27]
F1 I2C1_SCL_GPIO7 — I2C1_SCL_GPIO7 [16,27] **TOUCHSCREEN / ALS**
E3 GPIO64
F4 GPIO65
D3 GPIO66 — GPIO66 [8] **strapping**
E4 GPIO67
C3 GPIO68
E2 GPIO69

PCH GPIO PU/PD

PP3300_PCH

useless GPIO:
EC_RCIN_L R44 10K_4
IRQ_SERIRQ R36 10K_4
PCH_SSD_12_EN R399 *10K_4
PCH_SSD_18_EN R33 *10K_4
DEVSLP0 R382 10K_4
PCH_GPIO76 R393 10K_4
ODD_PRSNT# R440 10K_4
TPM_LP_EN_L R402 10K_4
PP3300_SSD_IO_EN R405 *10K_4
GPIO50 R392 10K_4
GPIO70 R348 10K_4
GPIO38 R375 10K_4
GPIO39 R6 10K_4

GSP:
GPIO83 R28 *10K_4
GPIO84 R8 *10K_4
GPIO85 R5 *10K_4
GPIO87 R20 *10K_4
GPIO88 R2 *10K_4
GPIO89 R4 *10K_4
GPIO90 R377 *10K_4
GPIO91 R364 *10K_4

UART:
GPIO92 R369 *10K_4
GPIO93 R365 *10K_4
GPIO94 R363 *10K_4
GPIO0 R3 *10K_4
GPIO1 R362 *10K_4
GPIO2 R366 *10K_4
GPIO3 R370 *10K_4

SDIO:
GPIO64 R329 *10K_4
GPIO65 R349 *10K_4
GPIO67 R335 *10K_4
GPIO68 R341 *10K_4
GPIO69 R339 *10K_4

I2C:
I2C0_SDA_GPIO4 R333 4.7K_4
I2C0_SCL_GPIO5 R334 4.7K_4
I2C1_SDA_GPIO6 R331 4.7K_4
I2C1_SCL_GPIO7 R332 4.7K_4

PP3300_PCH_SUS
R146 10K_4 LTE_WAKE_L_Q
R145 10K_4 WLAN_WAKE_L_Q

PP3300_PCH PP3300_PCH_SUS
G Path **I Path**
R97 0_4 — R101 *0_4
R89 10K_4 PCH_SPI_WP_D
R81 10K_4 GPIO14

PP3300_DSW PP3300_PCH_SUS
I Path **G Path**
R150 *0_4 — R144 0_4
R143 10K_4 TRACKPAD_INT_L
R139 10K_4 TOUCH_INT_L

RAM ID

PP3300_PCH_SUS
R39 10K_4 RAM_ID2 — R45 *10K_4
R434 10K_4 RAM_ID1 — R435 *10K_4
R446 10K_4 RAM_ID0 — R447 *10K_4

Vender	RAM_ID			Q PN	Mfr. PN	Freq.
	ID2	ID1	ID0			
Micron(4G)	0	0	0	AKD5JGSTL10	MT41K256M16HA-125:E	1600MHz
Hynix(4G)	0	0	1	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz
Hynix(4G)	0	1	0	AKD5PGSTW13	H5TC4G63AFR-PBA(25nm)	1600MHz
Micron(2G)	1	0	0	AKD5JGSTL10	MT41K256M16HA-125:E	1600MHz
Hynix(2G)	1	0	1	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz
Hynix(2G)	1	1	0	AKD5PGSTW13	H5TC4G63AFR-PBA(25nm)	1600MHz

CPU thermal trip

+1.05V_VCCST
IMVP_PWRGD_3V 2 — Q11 FDV301N
+1.05V_VCCST
R313 1K_4
R314 1K_4
THRMTRIP# — Q12 MMBT3904-7-F — SYS_SHDN# [25,32,33]

[19,25,34] PP3300_WLAN_EN
WLAN_WAKE_L_Q 3 — Q23 2N7002K — 1 WLAN_WAKE_L [19]

2014.8.07 Remove NGFF 3G SCH
two channel MOS change to single channel

[5,31] VCORE_PGOOD
U23 74AUP1G07GW: 1 NC, 2 A, 3 GND, 5 VCC, 4 Y
+1.05V_VCCST
C249 0.1u/16V_4
PP3300_PCH
R344 10K_4
IMVP_PWRGD_3V [25]

20141205 EOD parts, change PN.

PP3300_DSW
WK_GPIO27 — R96 10K_4 — R79 *10K_4

GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

PP3300_PCH_SUS
GPIO28 R49 10K_4
PP3300_CCD_EN R16 *10K_4
PP3300_SSD_EN R575 *10K_4
LTE_DISABLE_L R629 10K_4

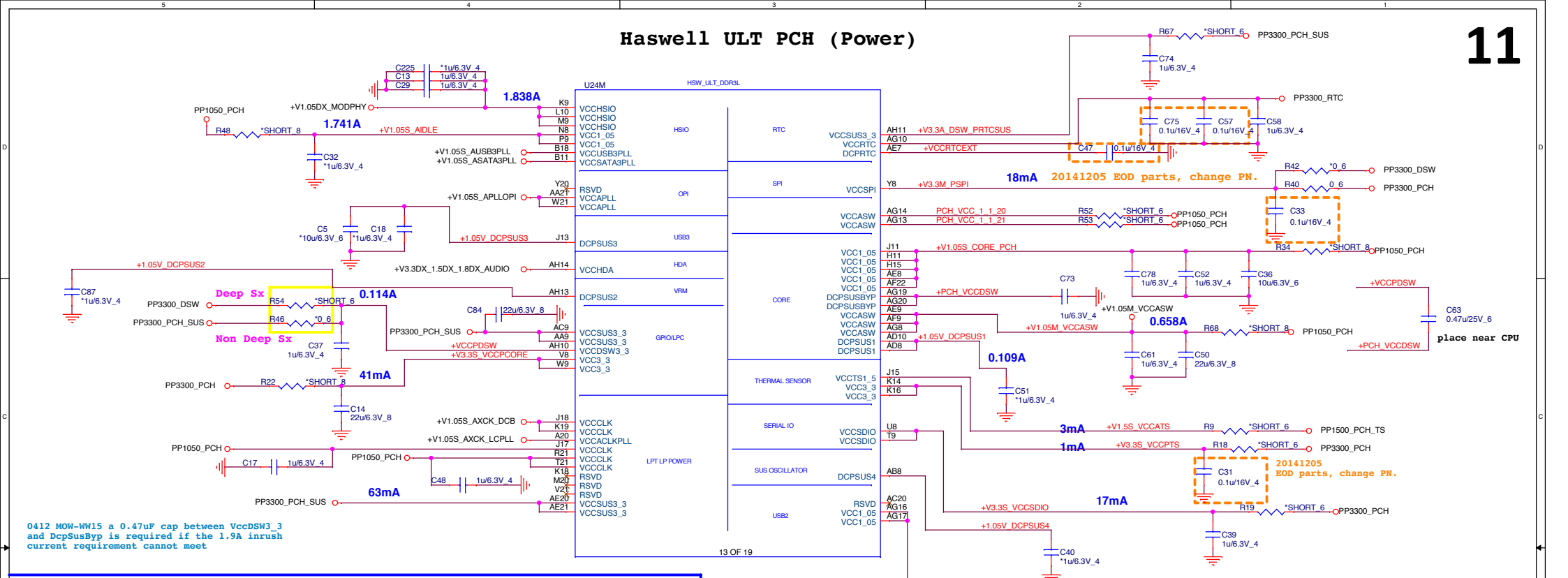
PP3300_CCD_EN R15 100K_4
PP3300_SSD_EN R570 100K_4

Quanta Computer Inc.
PROJECT : ZRF

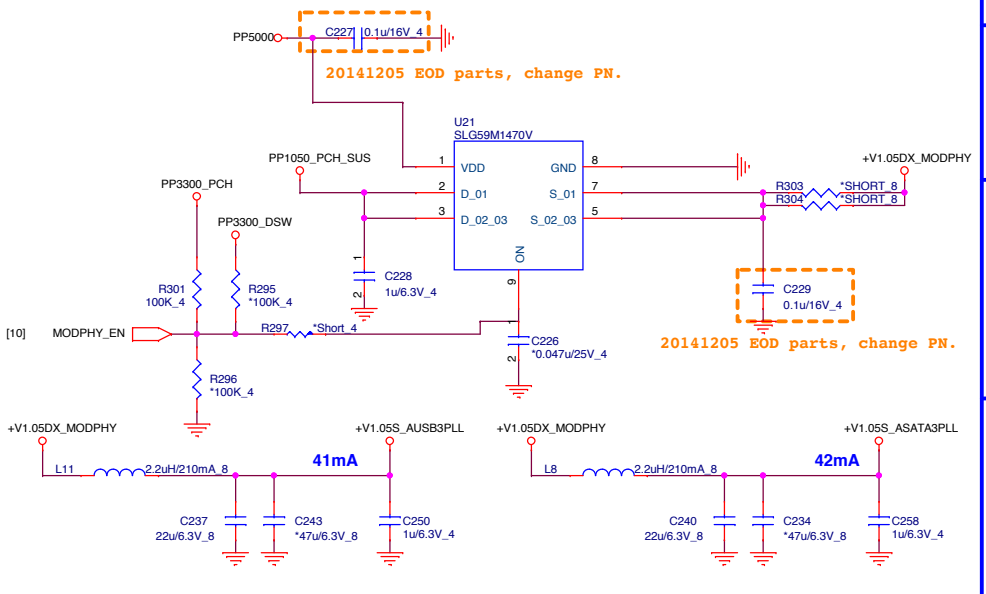
Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	A

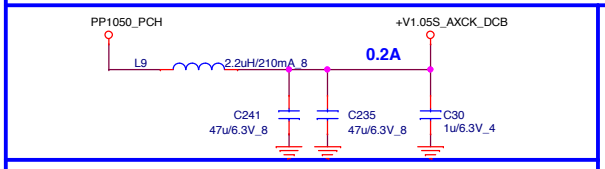
Date: Monday, January 12, 2015 Sheet 10 of 38

Haswell ULT PCH (Power)

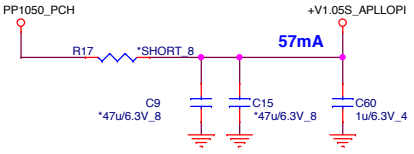


PCH VCCHSIO Power

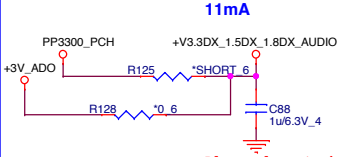


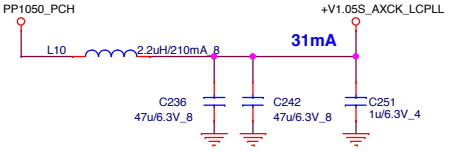


VCCAPLL power



PCH HDA Power





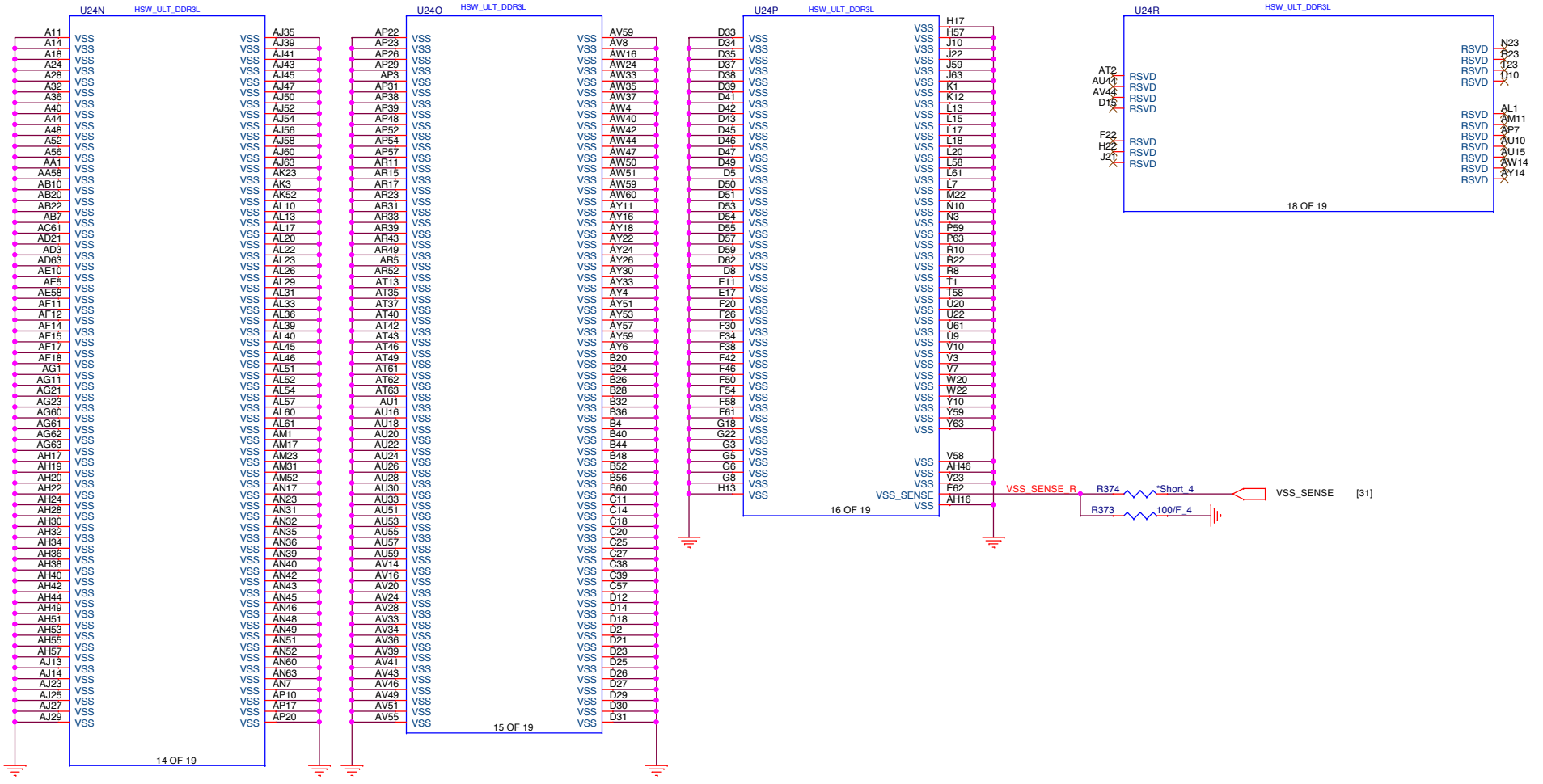
Quanta Computer Inc.

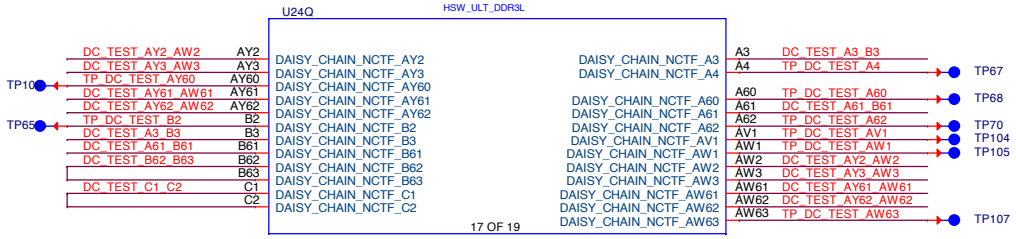
PROJECT : ZRF

Size	Document Number	Rev
	PCH 5/6 (POWER)	A

Date: Monday, January 12, 2015 Sheet 11 of 38

Haswell ULT (GND)



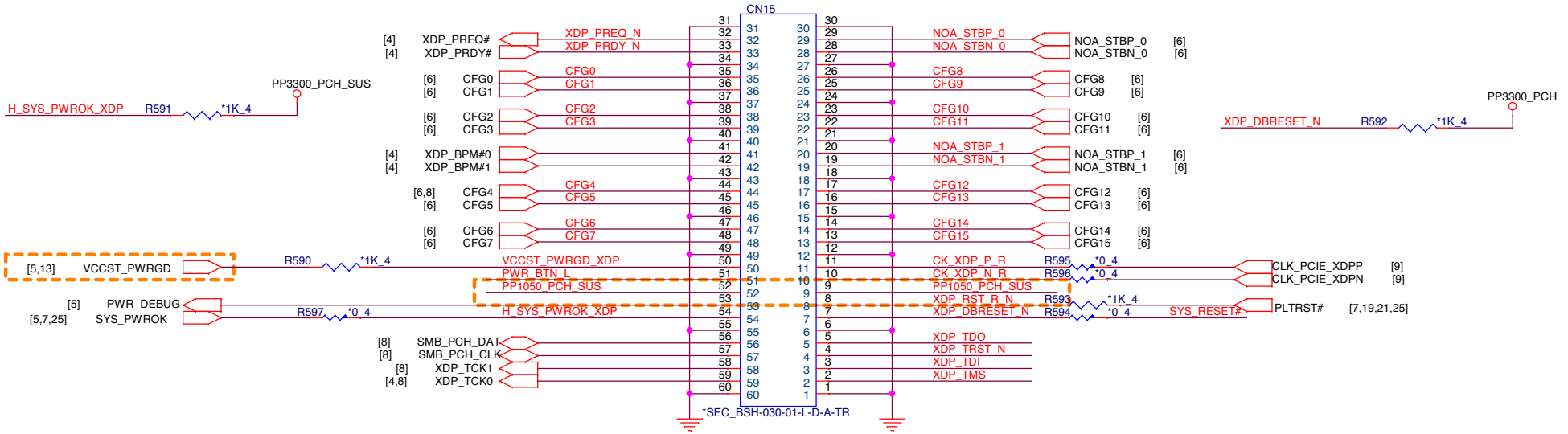


Quanta Computer Inc.

PROJECT : ZRF

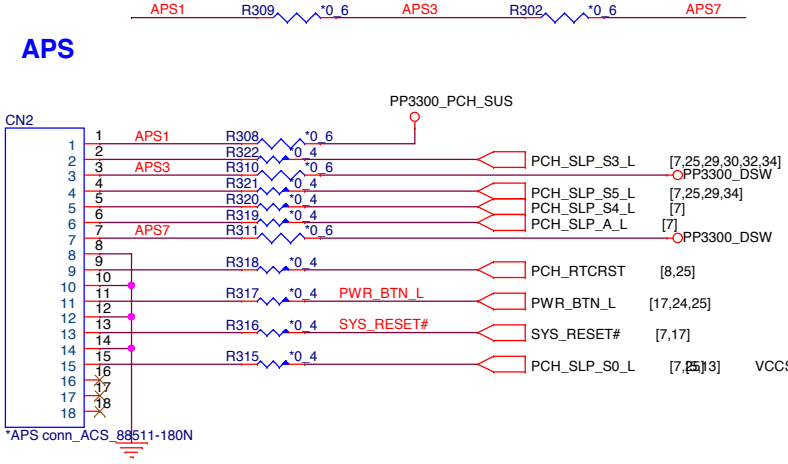
Size	Document Number	Rev
	PCH 6/6 (GND)	A

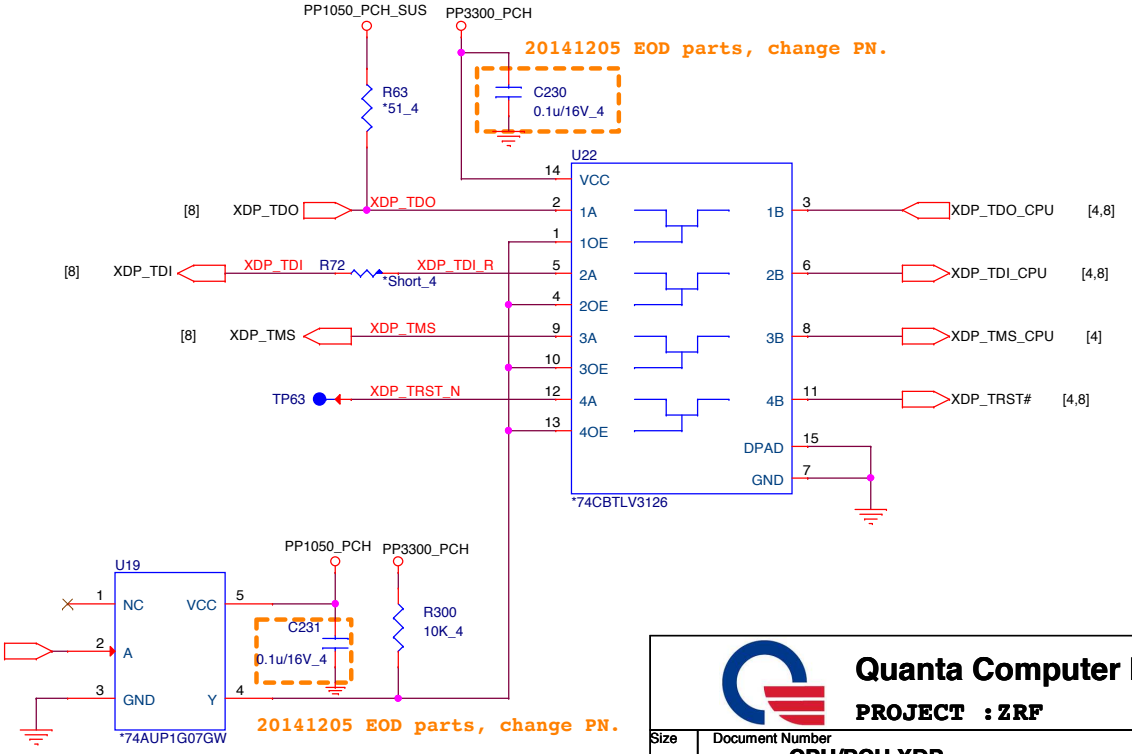
Date: Monday, January 12, 2015 Sheet 12 of 38



20141021 Intel require modify ITP CN15 P9/P51 add PP1050_PCH_SUS, P50 PP1050_PGOOD change to VCCST_PWRGD.

APS





Quanta Computer Inc.

PROJECT : ZRF

Size	Document Number	Rev
	CPU/PCH XDP	A
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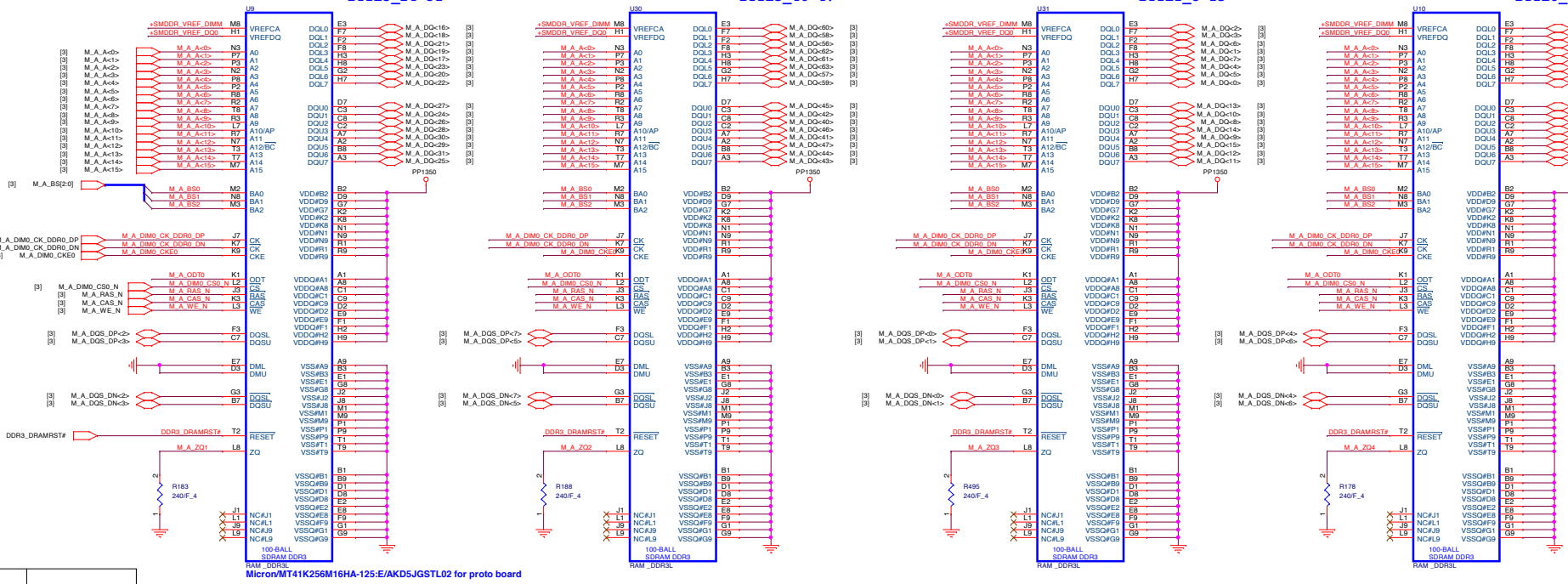
<DDR>

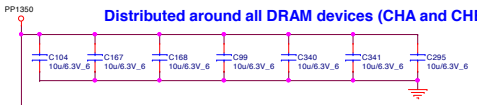
BYTE2_16-23
BYTE3_24-31
BYTE7_56-63
BYTE5_40-47
BYTE0_0-7
BYTE1_8-15
BYTE4_32-39
BYTE6_48-55



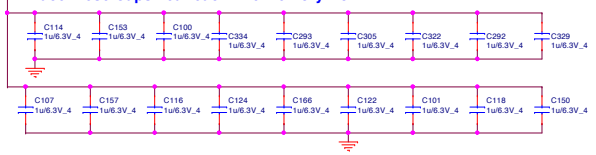
Micron/MT41K256M16HA-125:E/AKD5JGSTL02 for proto board

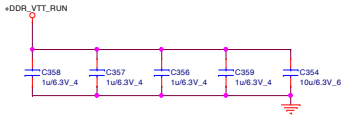
Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

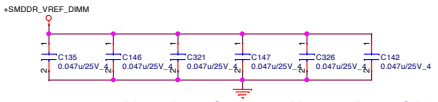
Distributed around all DRAM devices (CHA and CHB)



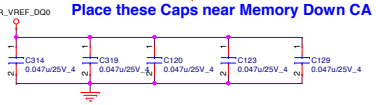
Place these Caps near each X16 Memory Down



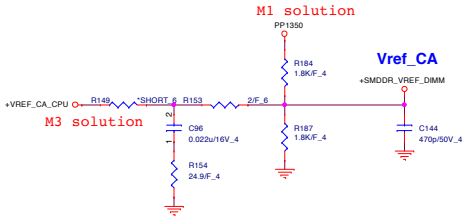


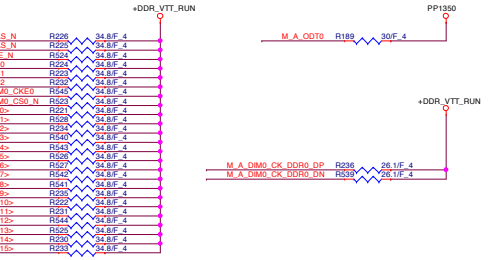


Place these Caps near Memory Down CA & DQ pin

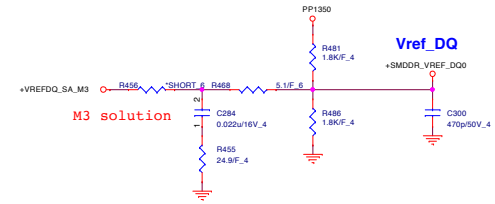


M1 solution





M1 solution



S_CLIP1 *SUL-12A2M
S_CLIP3 *SUL-12A2M
S_CLIP2 *SUL-12A2M
S_CLIP4 *SUL-12A2M

Quanta Computer Inc.
PROJECT : ZRF

Size	Document Number	Rev
	DDR3L MEMORY DOWNx16 A	A

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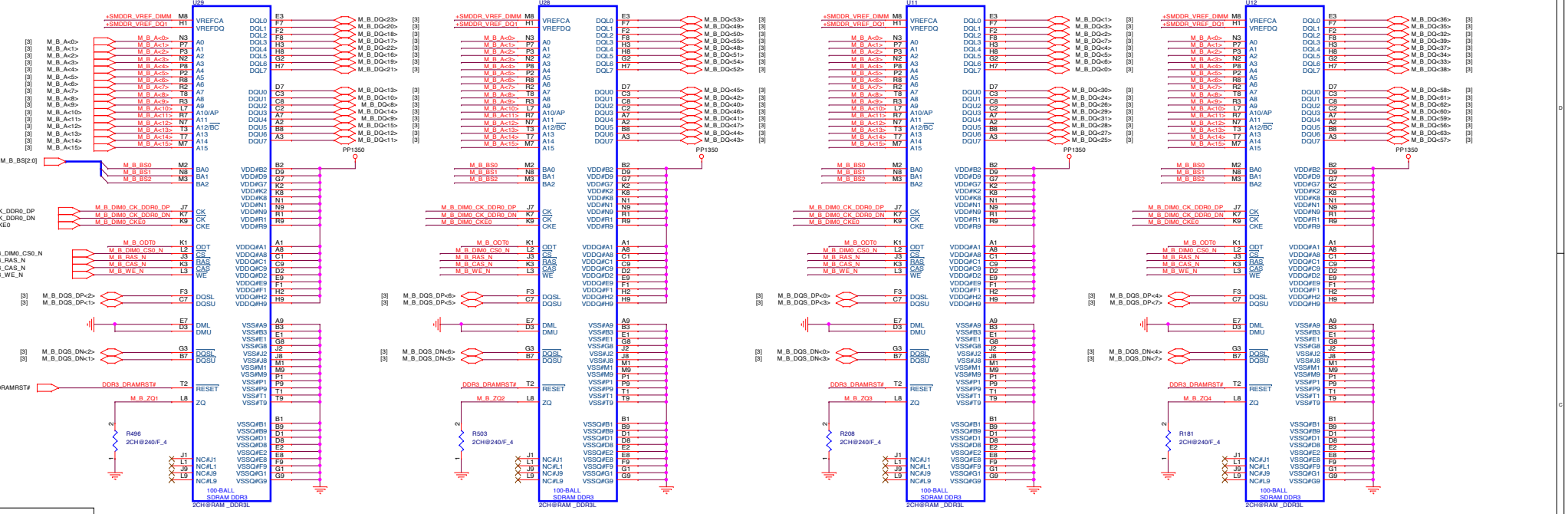
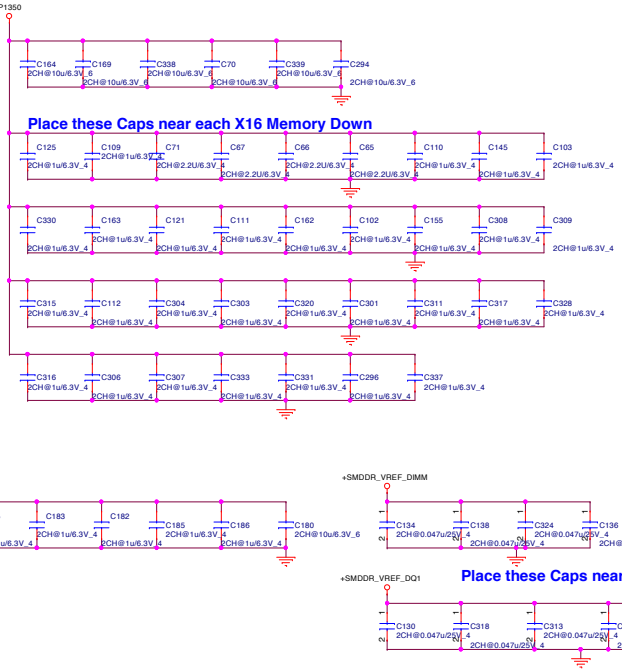
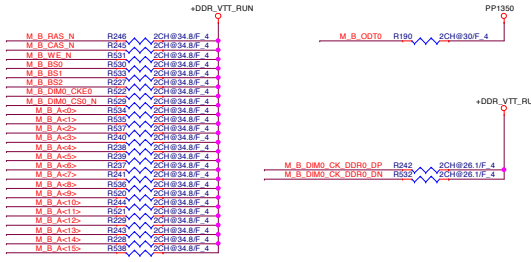
BYTE1_8-15
BYTE2_16-23
BYTE5_40-47
BYTE6_48-55
BYTE0_0-7
BYTE3_24-31
BYTE4_32-39
BYTE7_56-63

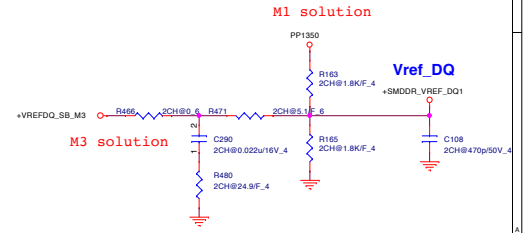


Micron/MT41K256M16HA-125:E/AKD5JGSTL02 for proto board

Vendor	P/N	
Hynix	AKD5JGETW04	DDR3L 1600Mhz 4Gb
Elpida	AKD5JGST407	DDR3L 1600Mhz 4Gb
Micron	AKD5JGSTL10	DDR3L 1600Mhz 4Gb







Quanta Computer Inc.
PROJECT : ZRF

Size	Document Number	Rev
	DDR3L MEMORY DOWNx16 B	A

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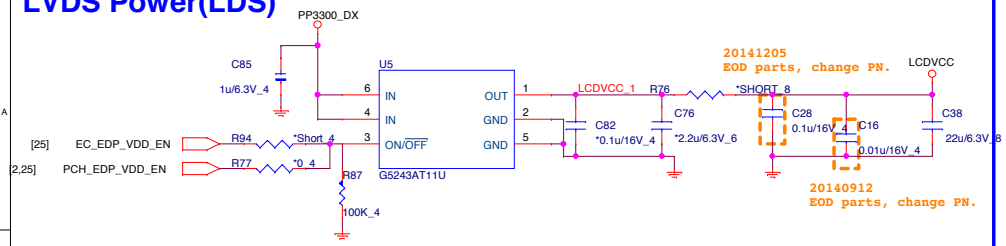
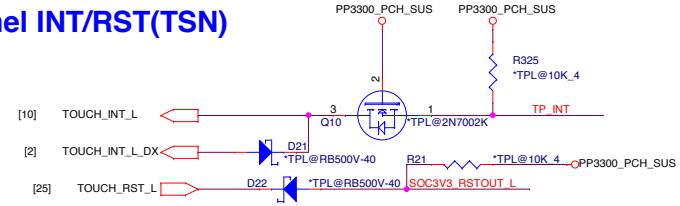
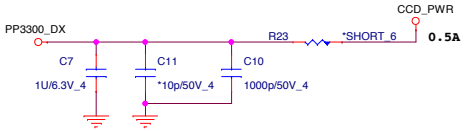
LVDS Power(LDS)



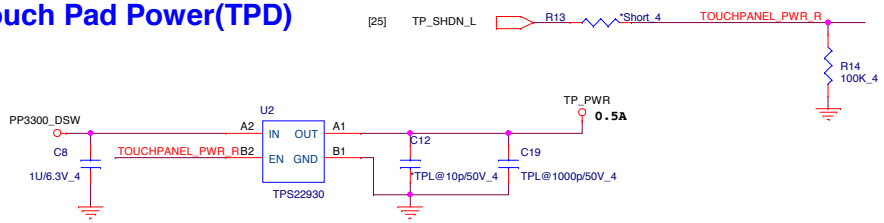
Touch Panel INT/RST(TSN)



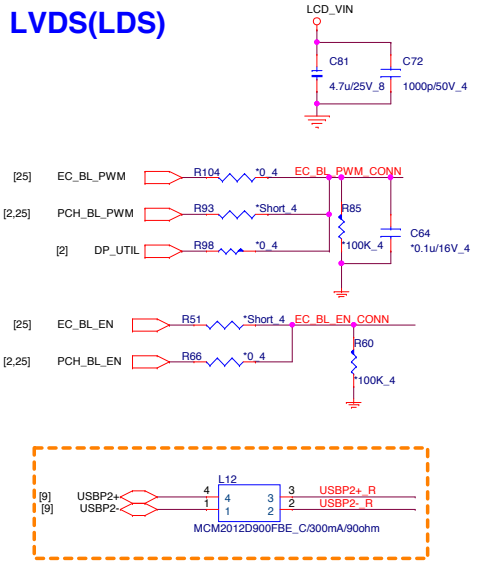
CCD power(CCD)



Touch Pad Power(TPD)

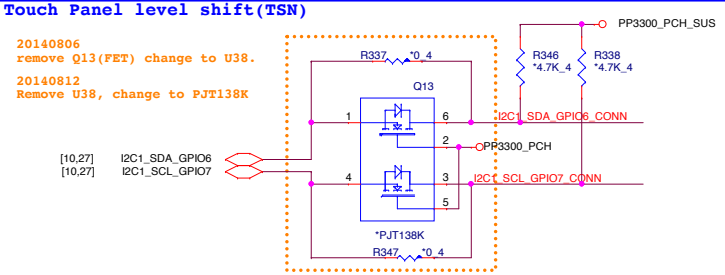


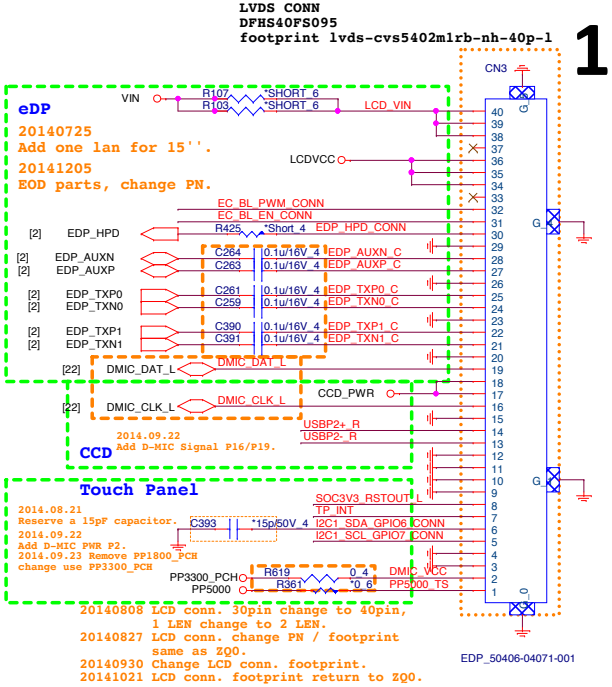
LVDS(LDS)



CCD(CCD)

Touch Panel level shift(TSN)





Quanta Computer Inc.

PROJECT : ZRF

Size	Document Number	Rev
	LVDS/CCD/DMIC/TS	A
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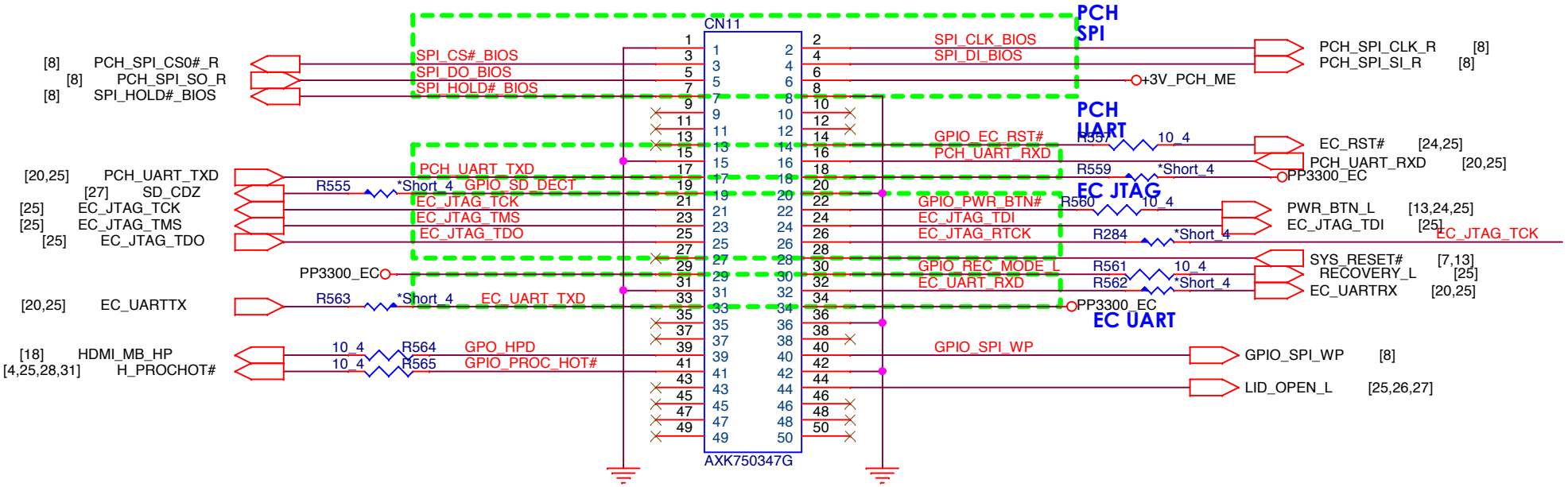
Debug Port(DBG)

PIN7 OD
PIN14 OD
PIN19 OD
PIN22 OD
PIN28 OD
PIN30 OD
PIN37 OD
PIN38 OD
PIN39 OD
PIN41 OD
PIN43 OD
PIN44 OD
PIN45 OD
PIN46 OD
PIN47 OD
PIN48 OD
PIN49 OD
PIN50 OD



Quanta Computer Inc.		
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Size	Document Number: Google Debug	Rev: A
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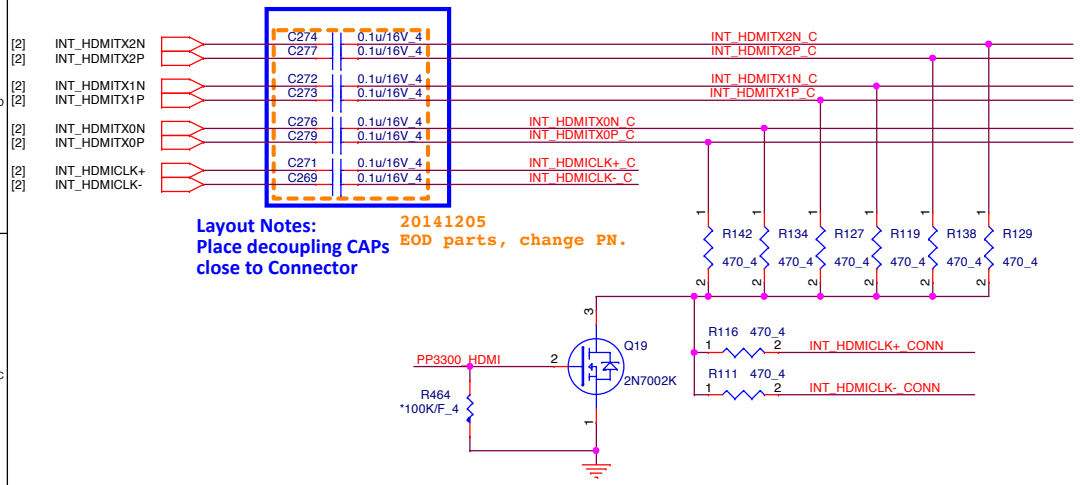
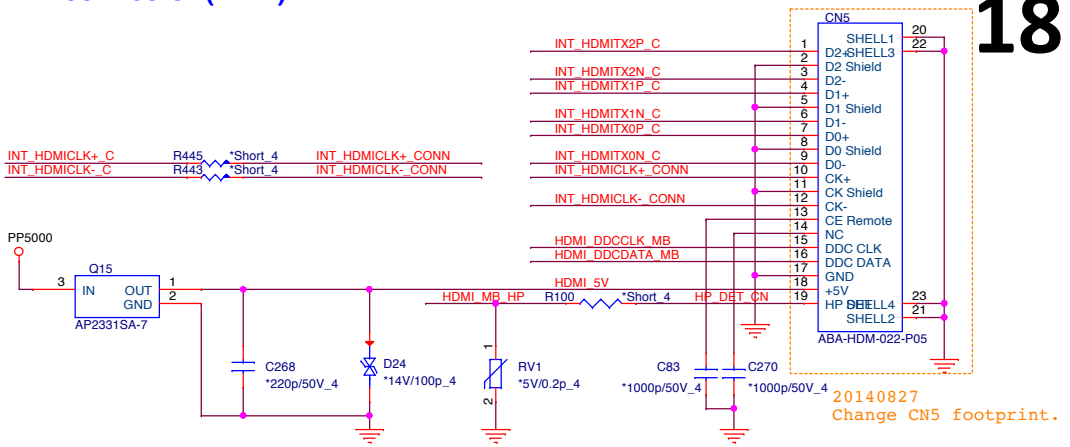
HDMI Cost Reduced level shift (HDM)



Layout Notes:
Place decoupling CAPs close to Connector

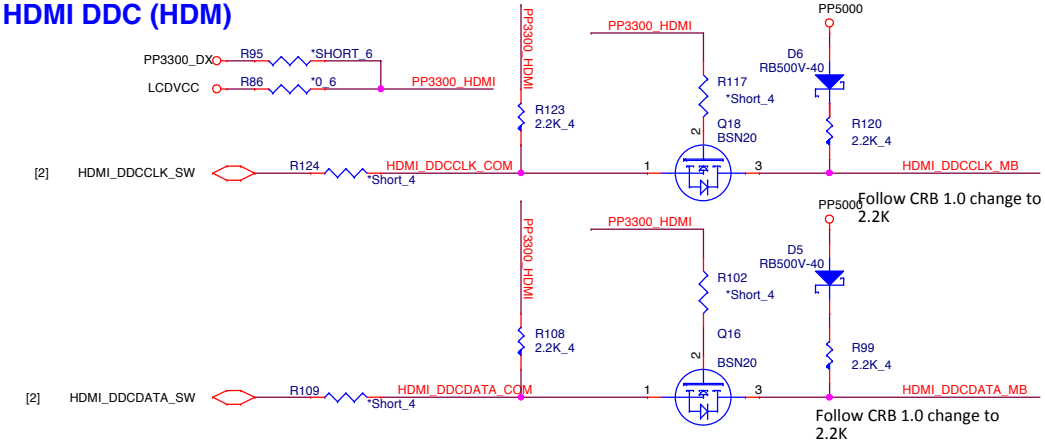
20141205
EOD parts, change PN.

HDMI connector (HDM)

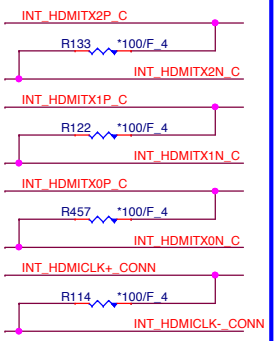


20140827
Change CN5 footprint.

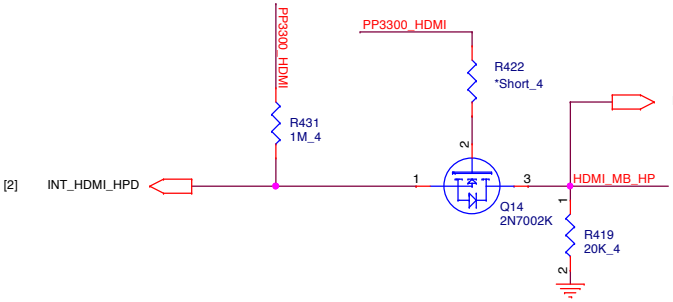
HDMI DDC (HDM)



EMI (HDM)



HDMI-detect (HDM)



Quanta Computer Inc.

PROJECT : ZRF

Size	Document Number	Rev
	HDMI	A
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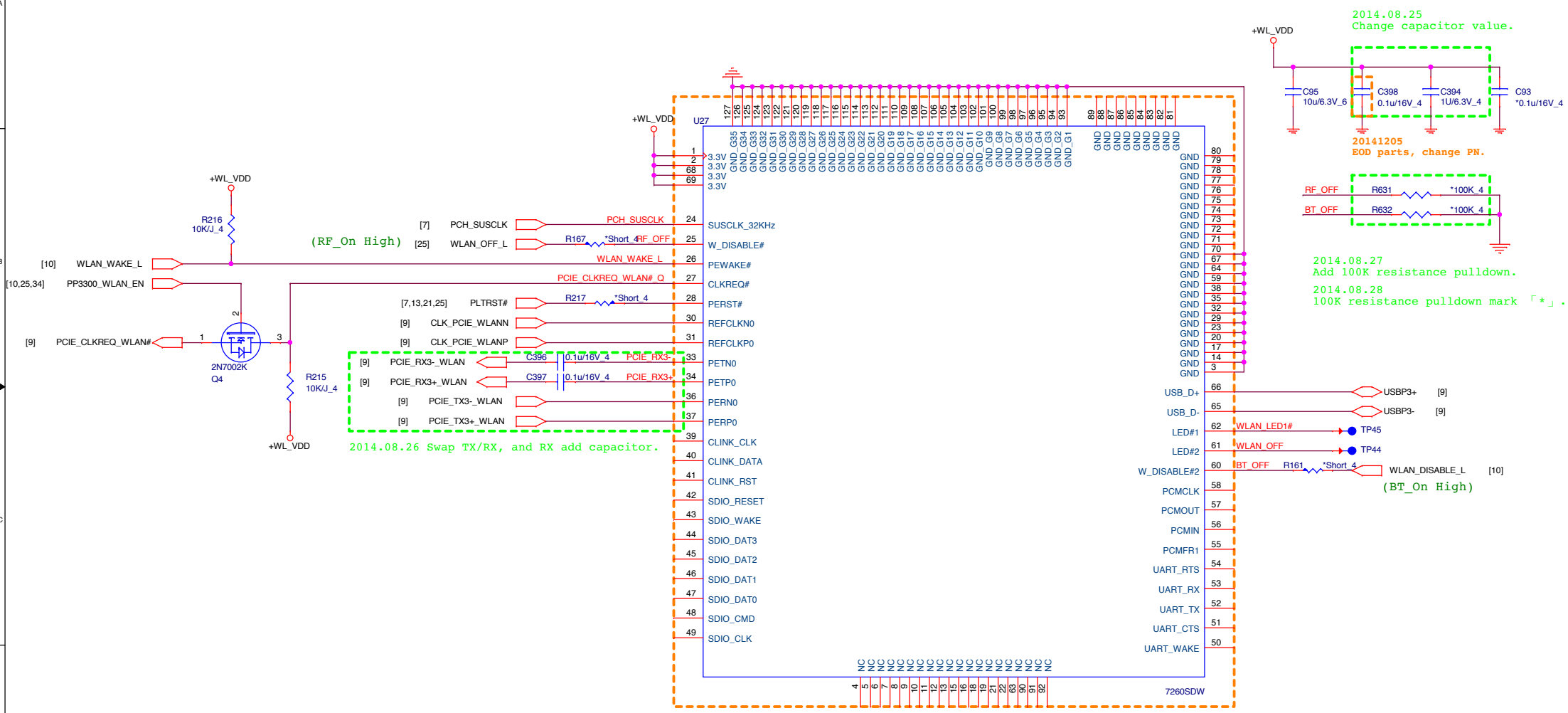

20140820 On board IC change to same as ZS8 connector
20140822 Return to another wifi onboard module 7260SDW
20140826 Change wifi onboard module 7260SDW footprint
20140909 Change wifi onboard module 7260SDW footprint
20141014 Change wifi onboard module 7260SDW PN.

Quanta Computer Inc.
PROJECT : ZRF

Size	Document Number	Rev
	WIFI / BT	A

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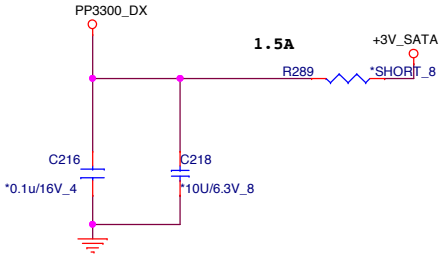
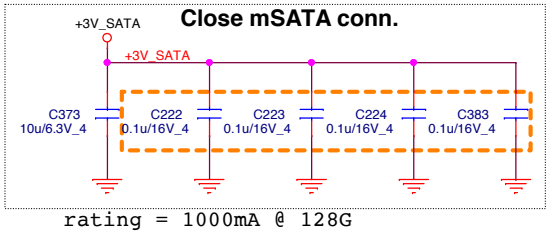
NGFF SSD connector.

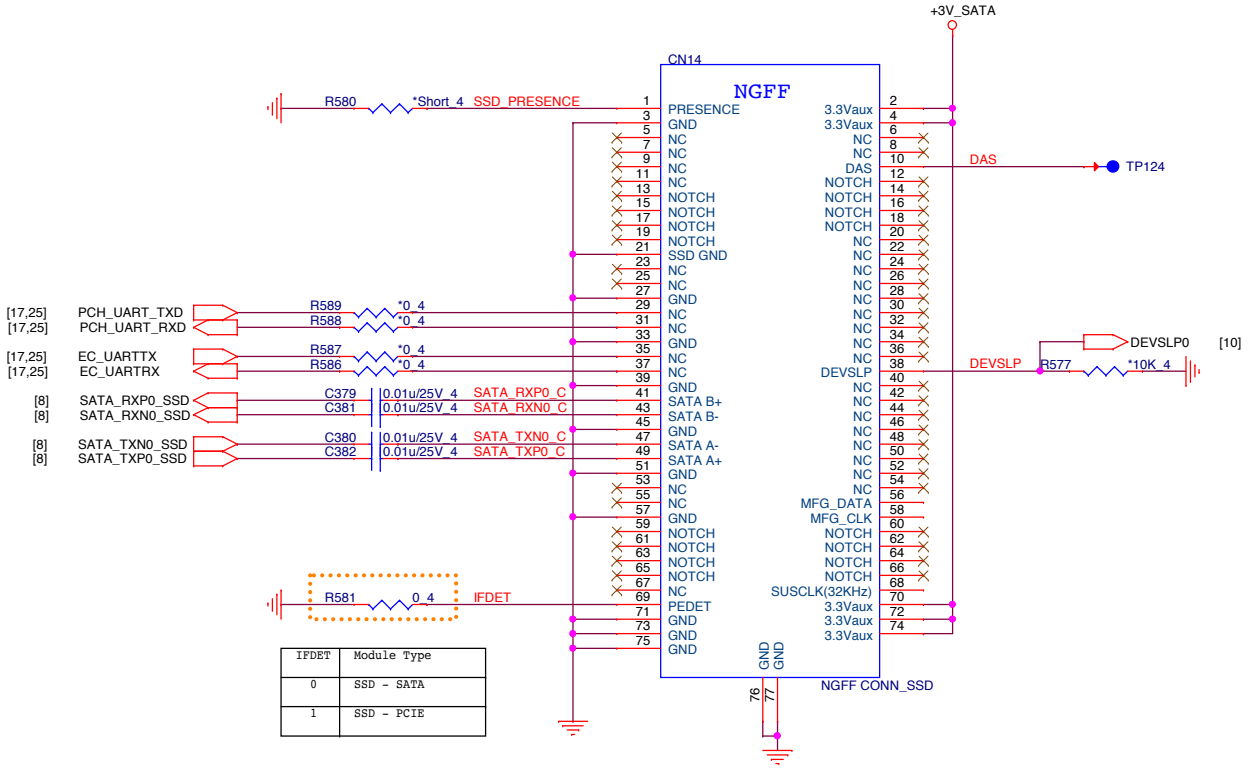
San Disk SSD Card.





20141205 EOD parts, change PN.

rating = 1000mA @ 128G



IFDET	Module Type
0	SSD - SATA
1	SSD - PCIE

Quanta Computer Inc.

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Size	Document Number	Rev
	NGFF SSD	A
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TPM (TPM)

20141201 Change TPM power.

4 x100nF (place close to device VDD/GND pins)

PP3300_PCH

R470
2.2_6

TPM_VDD

20141205 EOD parts, change PN.

C297 0.1u/16V_4
C287 0.1u/16V_4
C298 0.1u/16V_4
C288 0.1u/16V_4

TPM_VDD

R467
*20K_4

U7

TPM_GPIO

R465 0_4 TPM_PP

TPM_VDD R469 *4.7K_4

0411 FAE : install R80 value is 4K7,
and PIN7 wo an internal PD

6	GPIO	
2	NC2	
7	PP	
13	NC13	
14	NC14	
8	NC8	
12	NC12	
3	NC3	
1	NC1	
4	GND[1]	
11	GND[2]	
18	GND[3]	
25	GND[4]	

TPM SLB9655

SLB9655

10	VDD[4]	
5	VDD[3]	
24	VDD[2]	
19	VDD[1]	
21	LCLK	PCLK_TPM [9]
22	LFRAME#	LPC_LFRAME# [8,25]
17	LAD3	LPC_LAD3 [8,25]
20	LAD2	LPC_LAD2 [8,25]
23	LAD1	LPC_LAD1 [8,25]
26	LAD0	LPC_LAD0 [8,25]
28	NC28	
16	LRESET#[1]	
9	LRESET#[2]	TPM_RST_R R148 *Short_4 PLTRST# [7,13,19,25]
27	SERIRQ	SERIRQ_R R491 *Short_4 IRQ_SERIRQ [10,25]
15	NC15	

near pin 21 as possible

C291 *10p/50V_4

0411 FAE : a 0ohm between pin9 to LRESET signals

Quanta Computer Inc.

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Size	Document Number	Rev
	TPM SLB9655 / LED	A
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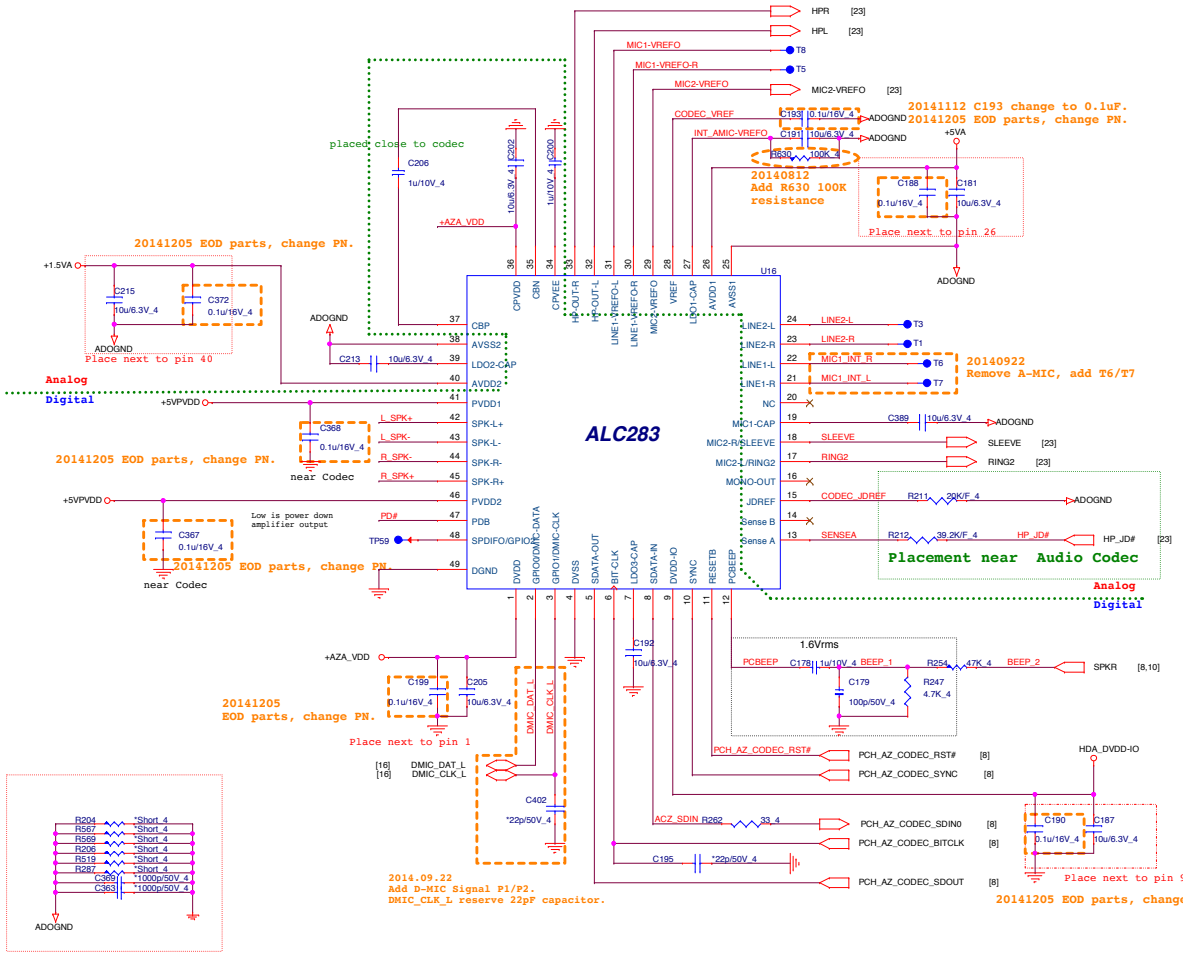
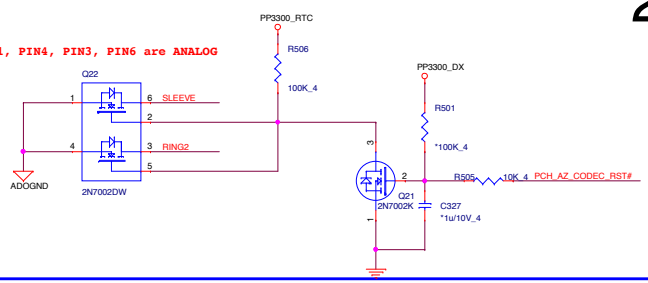
Codec(ADO)

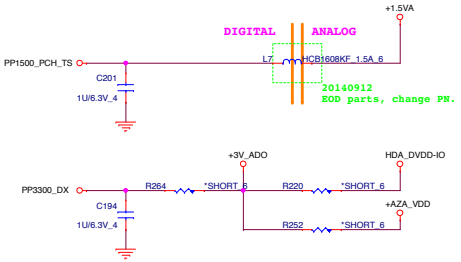


Grounding circuit(ADO)

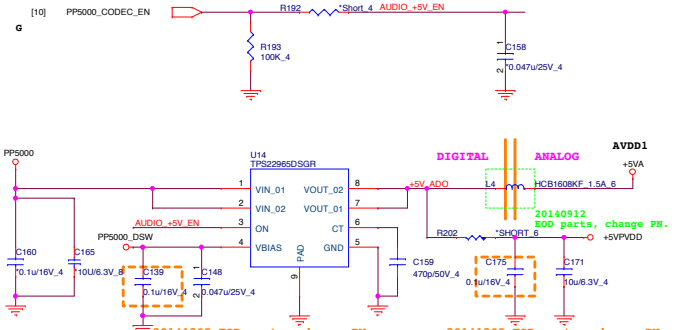


D-Mic

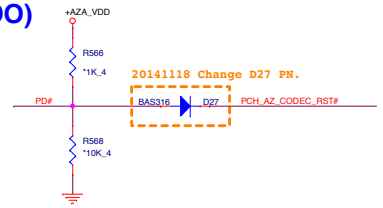
Codec PWR 3V/1.5V(ADO)



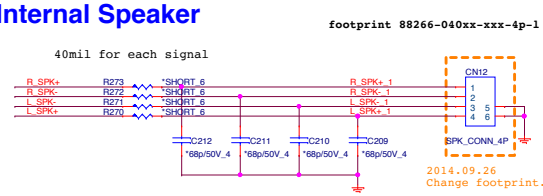
Codec PWR 5V(ADO)



Mute(ADO)



Internal Speaker



Quanta Computer Inc.	
PROJECT : ZRF	
Size	Document Number: ALC283/HP/SPK — Rev: A
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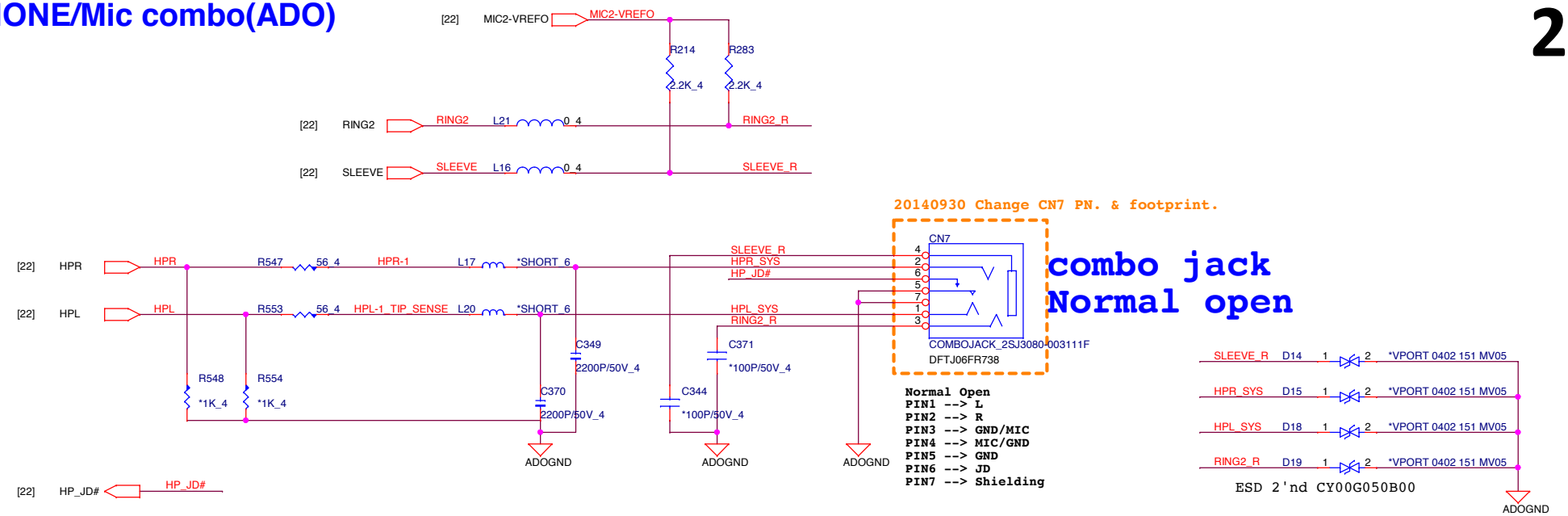
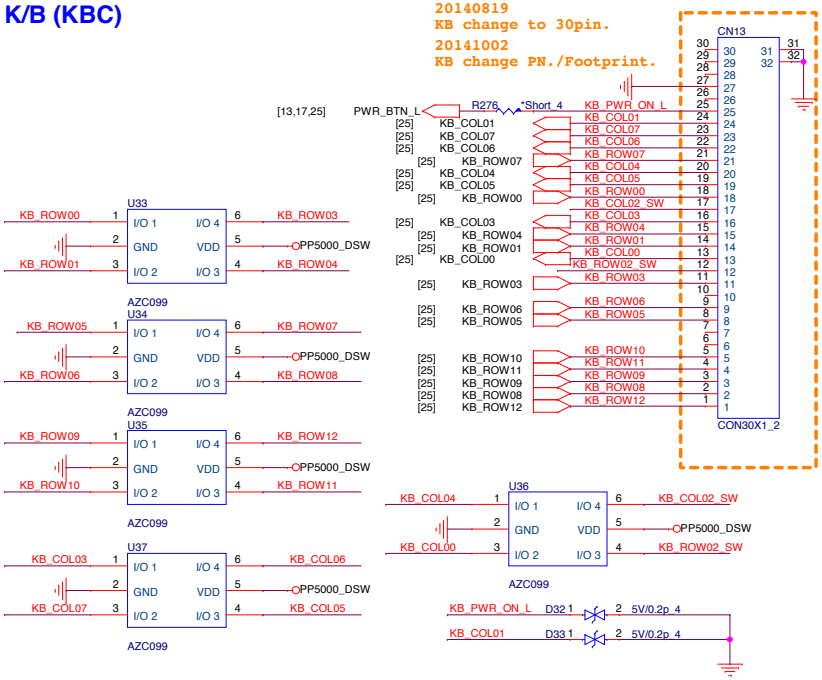
HEADPHONE/Mic combo(ADO)



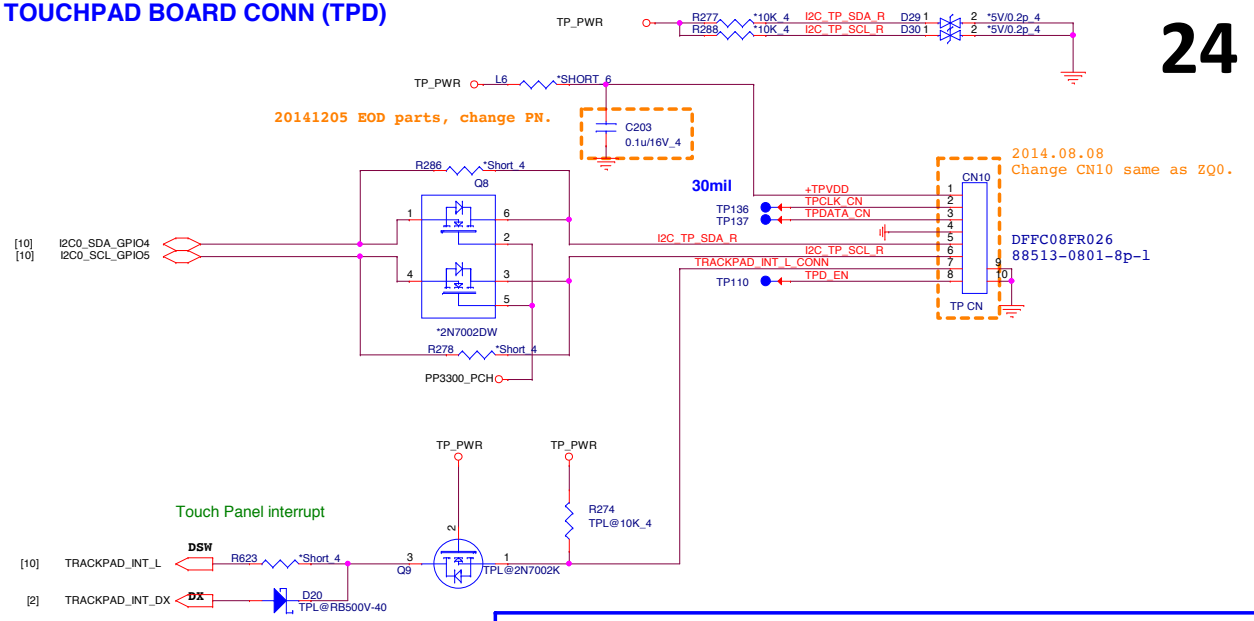
Quanta Computer Inc.			
PROJECT : ZRF			
Size	Document Number		Rev
	Audio Headset SW		A
Date: Monday, January 12, 2015	Sheet 23 of 38		

K/B (KBC)

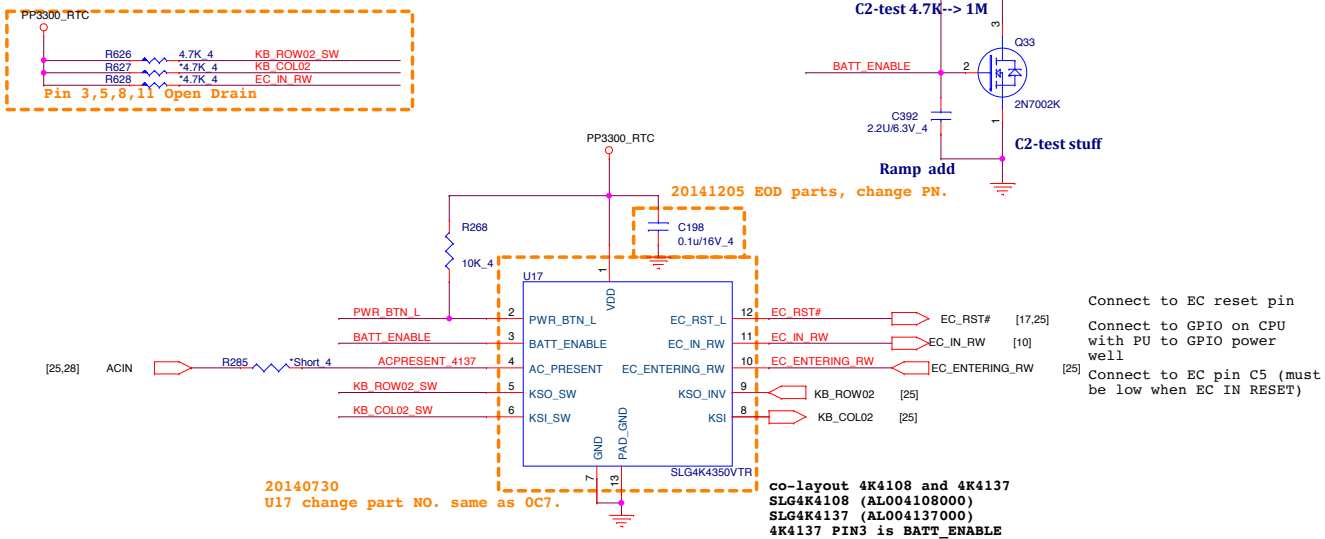
20140819
KB change to 30pin.
20141002
KB change PN./Footprint.



TOUCHPAD BOARD CONN (TPD)



HOLELESS RESET 2-CHIP(KBC)

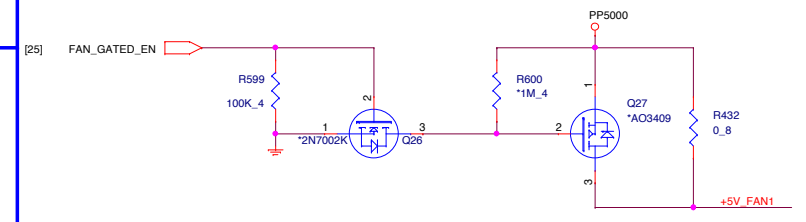


Connect to EC reset pin

Connect to GPIO on CPU with PU to GPIO power well

Connect to EC pin C5 (must be low when EC IN RESET)

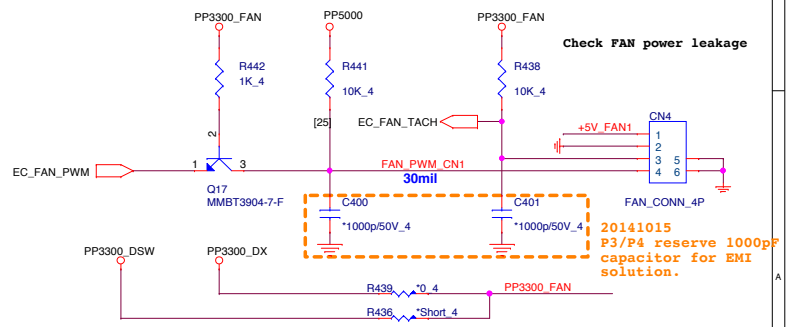
co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT



CPU FAN1 (THM)

Check pin define 0321

footprint 88266-040xx-xxx-4p-1



Quanta Computer Inc.			
PROJECT : ZRF			
Size	Document Number		Rev
	KB/TP/FAN/HW Reset		A
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EC(KBC)

20141205 EOD parts, change PN.

20140930 Change U15 PN.
20141201 Change U15 new PN.
20150109 Change U15 PN. for MP.

20141205 EOD parts, change PN.

20140912 EOD parts, change PN.

20141205 EOD parts, 20140912 change PN. EOD parts, change PN.

20141205 EOD parts change PN

20141205 EOD parts, change PN.

20141009 BAT_ID pin add R633 pull high.

20141205 EOD parts, change PN.

20141009 Add BAT_ID pin to identify 45watt BATT. conn.

4/23 modify, remove DSW_GATED power

20141205 EOD parts, change PN.

20141205 EOD parts, change PN.

20140912 EOD parts, change PN.

20141120 Change EC_BRD_ID, ID2 change to High, ID3 change to Low, because EC change code.

20141118 Change D28 PN.

SM BUS/I2C PU(KBC)

BATT and CHARGER / LCD BL — PP3300_EC
EC_SMB0_CLK R185 4.7K_4
EC_SMB0_DATA R186 4.7K_4

Light BAR — PP3300_DX
EC_SMB1_CLK R209 4.7K_4
EC_SMB1_DATA R213 4.7K_4

THERMAL SENSOR — PP3300_DX
EC_SMB2_CLK R498 4.7K_4
EC_SMB2_DATA R499 4.7K_4

EC HIB WAKE SOURCES

SM BUS ARRANGEMENT TABLE

SM Bus 0	BATT and CHARGER
SM Bus 1	NA
SM Bus 2	THERMAL SENSOR

For test only

J1 2 1 PWR_BTN_L
*SHORT_ PAD1

Quanta Computer Inc.
PROJECT : ZRF

Size	Document Number	Rev
	KBC TI TM4E1G31H6ZRBI	A
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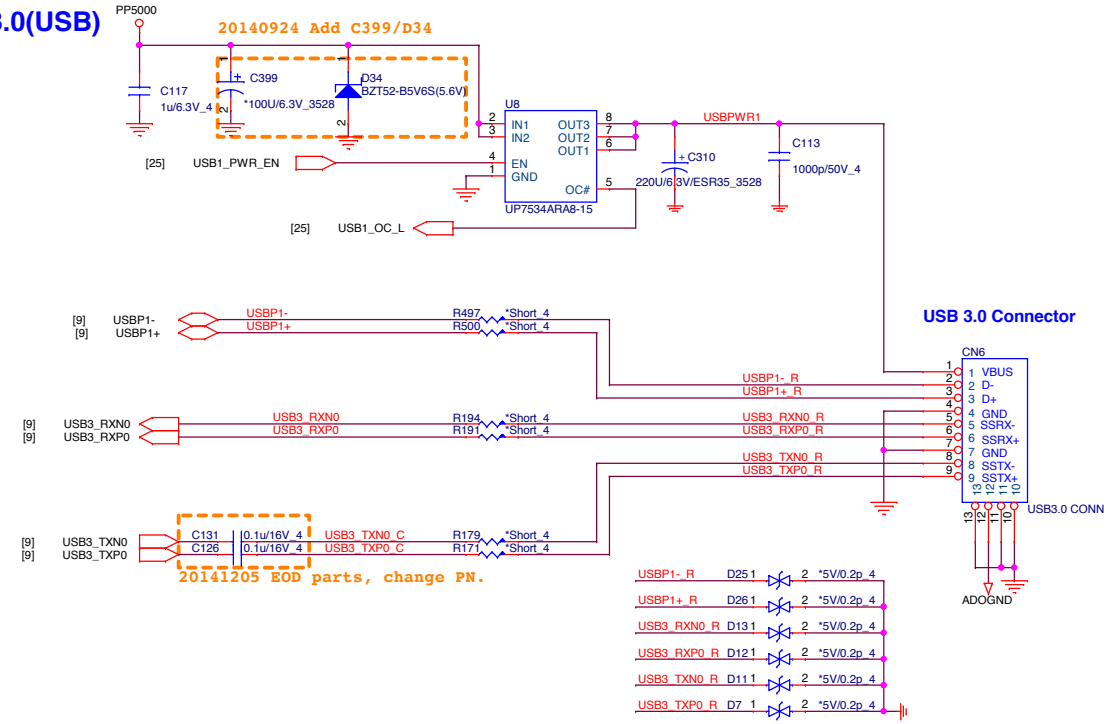
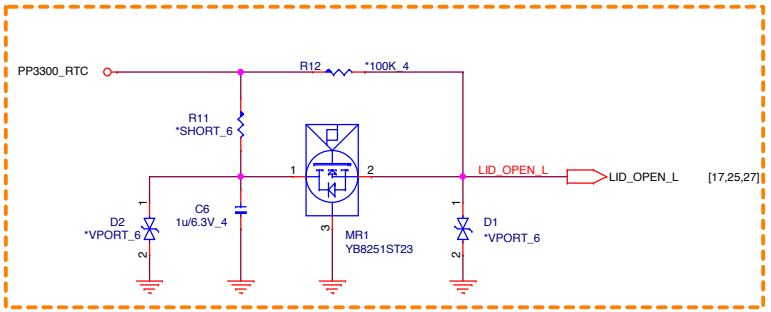
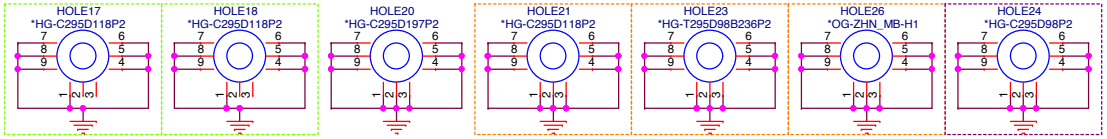
USB3.0(USB)



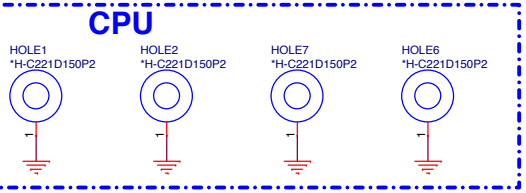
Lid Switch (HSR)

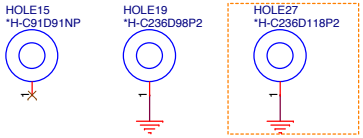


HOLE(OTH)



CPU





20140828
1. Add HOLE27
2. Change HOLE17/HOLE18/HOLE21/HOLE22 /HOLE23/HOLE26 footprint
3. Remove HOLE9/HOLE16

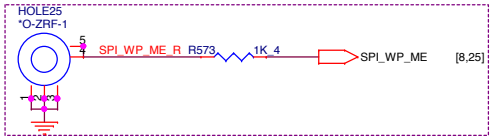
20140829
1. Change HOLE27 footprint
2. HOLE17/HOLE18/HOLE22 remove Pin1/Pin2/Pin3

20140901
1. Remove HOLE22

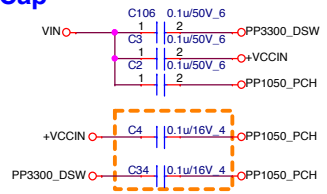
20140923
1. Remove battery enable, change to HOLE24

20140926
1. HOLE24 change footprint.
2. HOLE25 Add more 2pin & change footprint.
3. Remove HOLE3/4/5/8/10/11/12/13/14.

ROM WP#



EMI Cap



20141205 EOD parts, change PN.

Quanta Computer Inc.
PROJECT : ZRF

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	USB3/Hole	A
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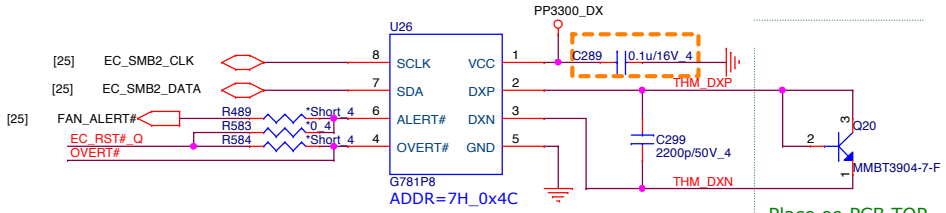
Thermal Sensor(THM)

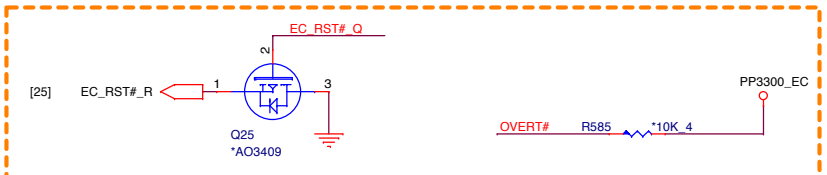
20141205 EOD parts, change PN.



ADDR=7H_0x4C

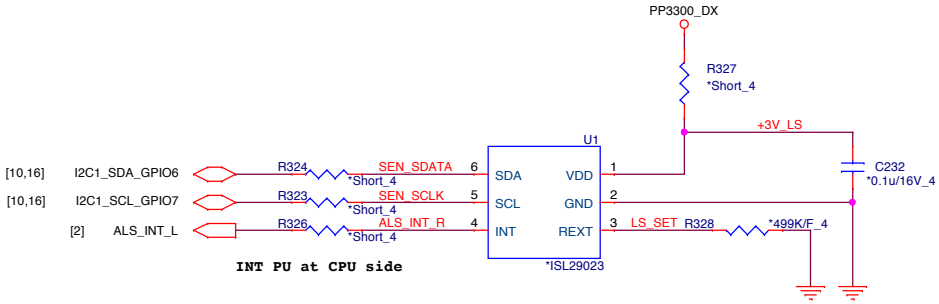
Place oo PCB BOT
Local Temp.

Place oo PCB TOP
Remote Temp.



20140925 Q25/R585 mark 「*」 un-stuff.
OVERT# power PP3300_DX change to PP3300_EC.

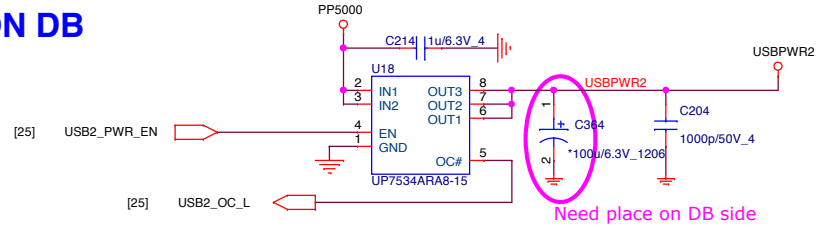
Light sensor & TP (ALS)



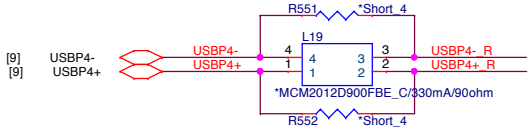
INT PU at CPU side

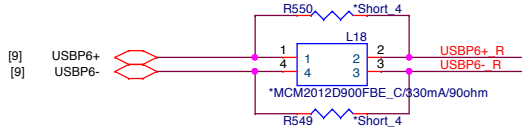
ADDR: 1000100

FUNCTION DB



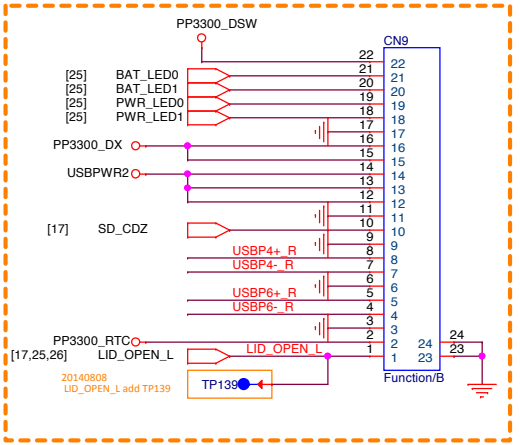
Need place on DB side





HSR	+3VPCU
	LID_OPEN_L
	GND
LED	+3VPCU
	LED x 4
	GND
USB	+3V x 2
	GND x 2
	USBP0+
	USBP0-
CR	CR_DET
	+3V x 2
	USBP6+
	USBP6-
	GND x 2
LID	PP3300_RTC
	LID_OPEN_L

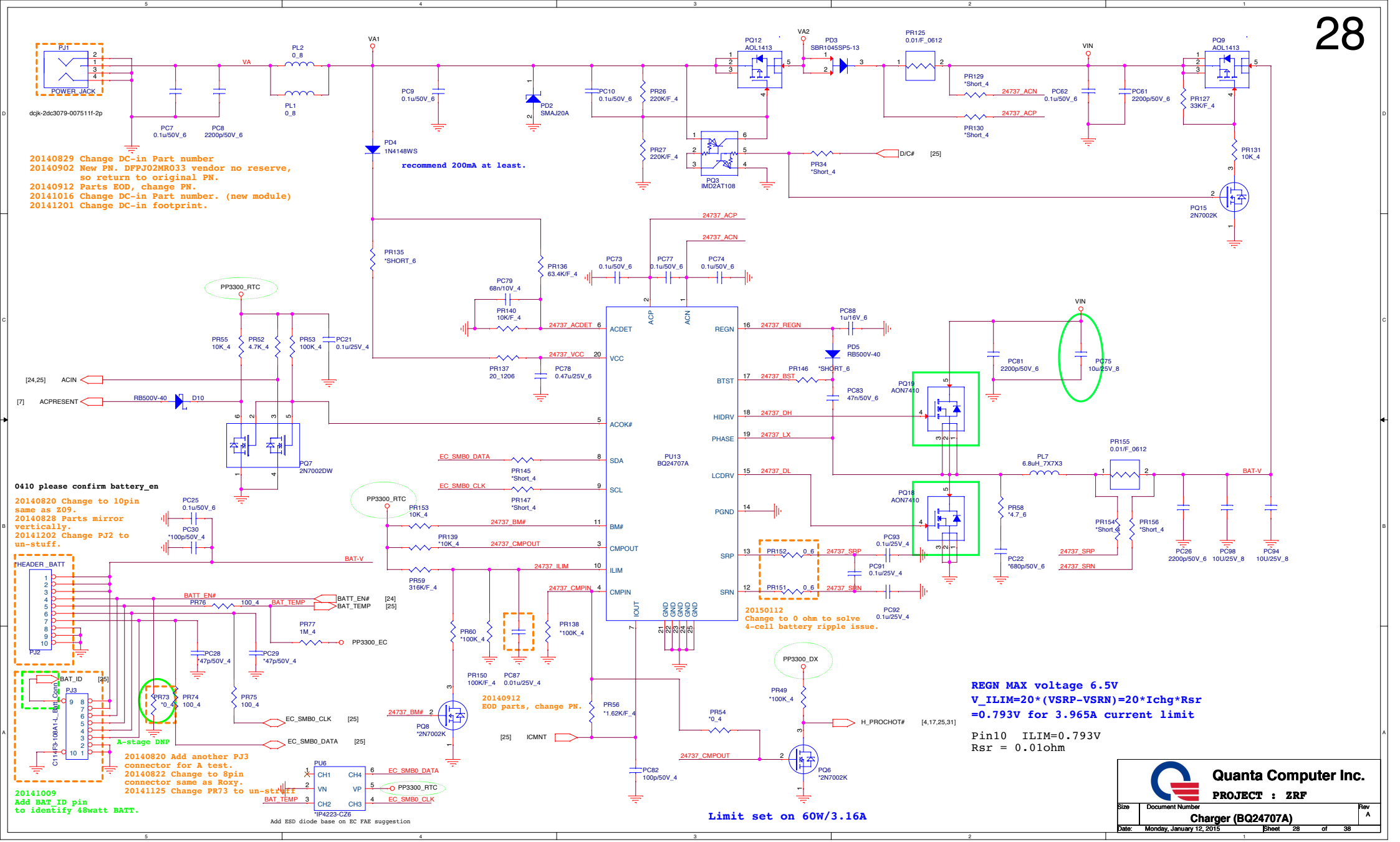
footprint 50501-0220n-v01-22p-l
DFFC22FR019



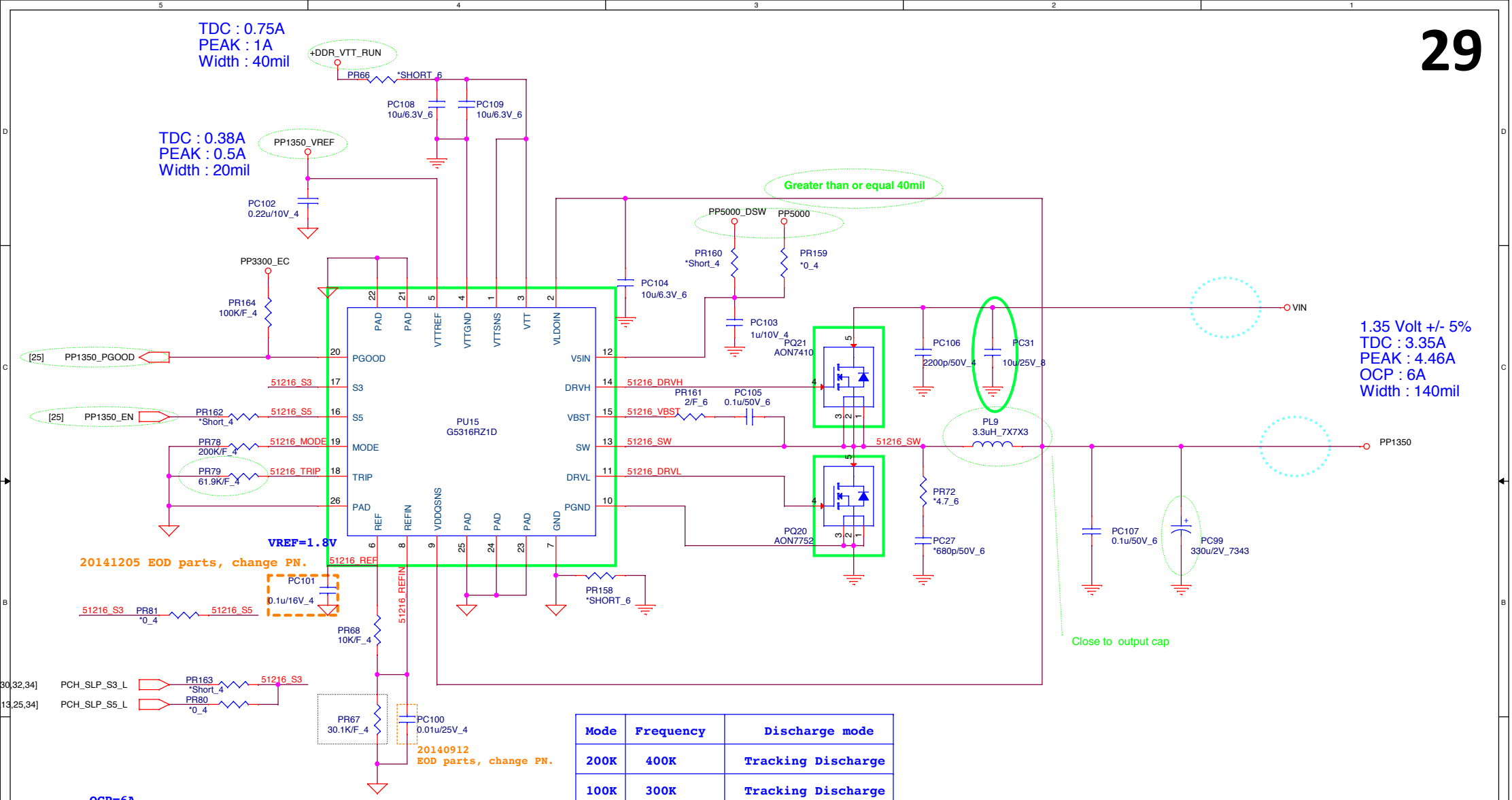
20140728 Modify to 22pin.
20140819 Change footprint

Quanta Computer Inc.
PROJECT : ZRF

Size	Document Number	Rev
	DB/ALS/Thermal sensor	A
Date: Monday, January 12, 2015	Sheet 27 of 38	



Quanta Computer Inc.			
PROJECT : ZRF			
Size	Document Number		Rev
	Charger (BQ24707A)		A
Date: Monday, January 12, 2015	Sheet 28	of 38	



Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=6A
L ripple current
=(19-1.35)*1.35/(3.3u*400k*19)
=0.95A
Vtrip=[6-(0.95/2)]*14mohm
=0.07735V
Rlimit=0.07335/10uA*8=61.88Kohm

Quanta Computer Inc.
PROJECT : ZRF

Size	Document Number	Rev
	DDR 1.35V (G5316)	A

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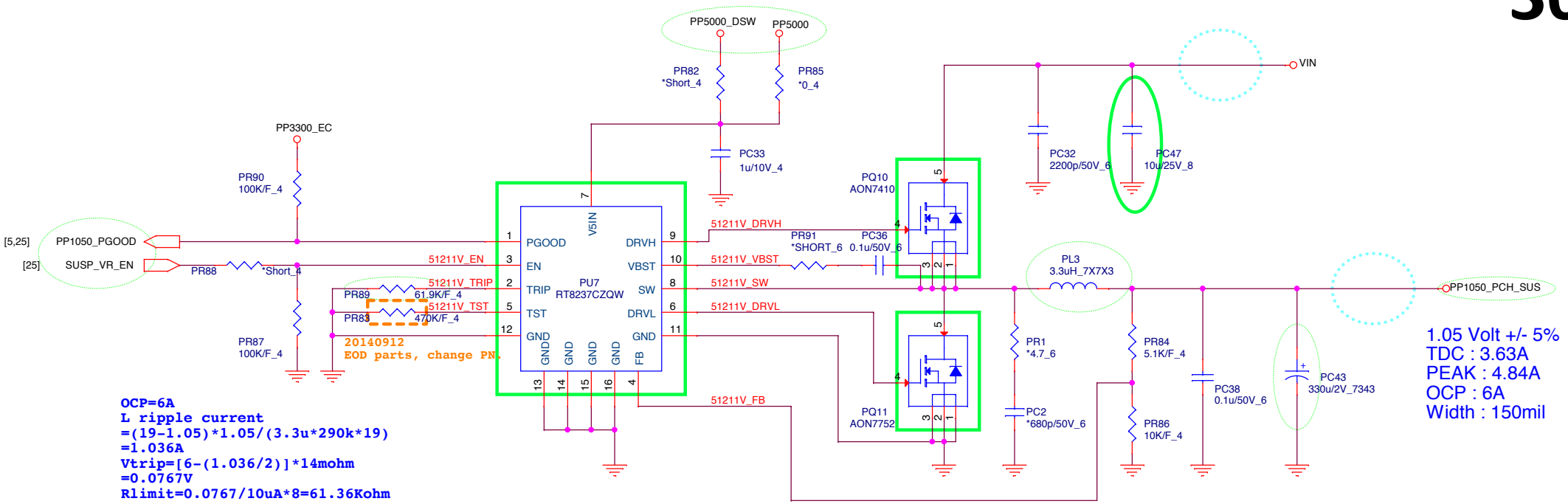
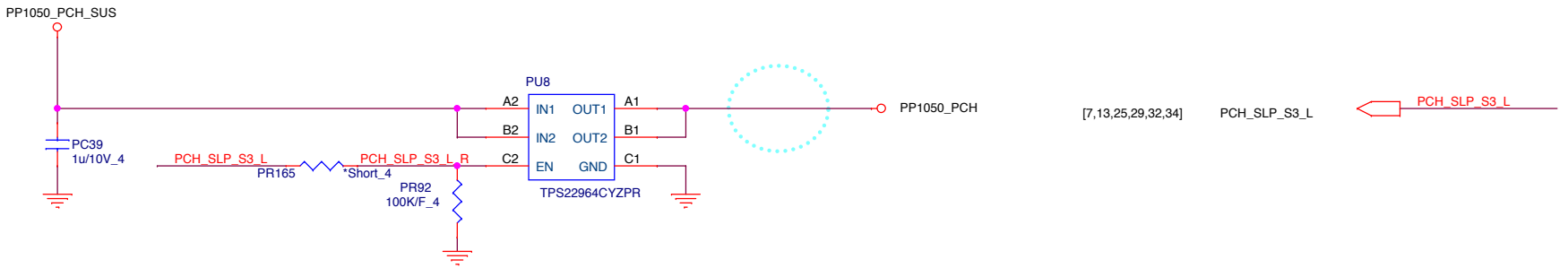


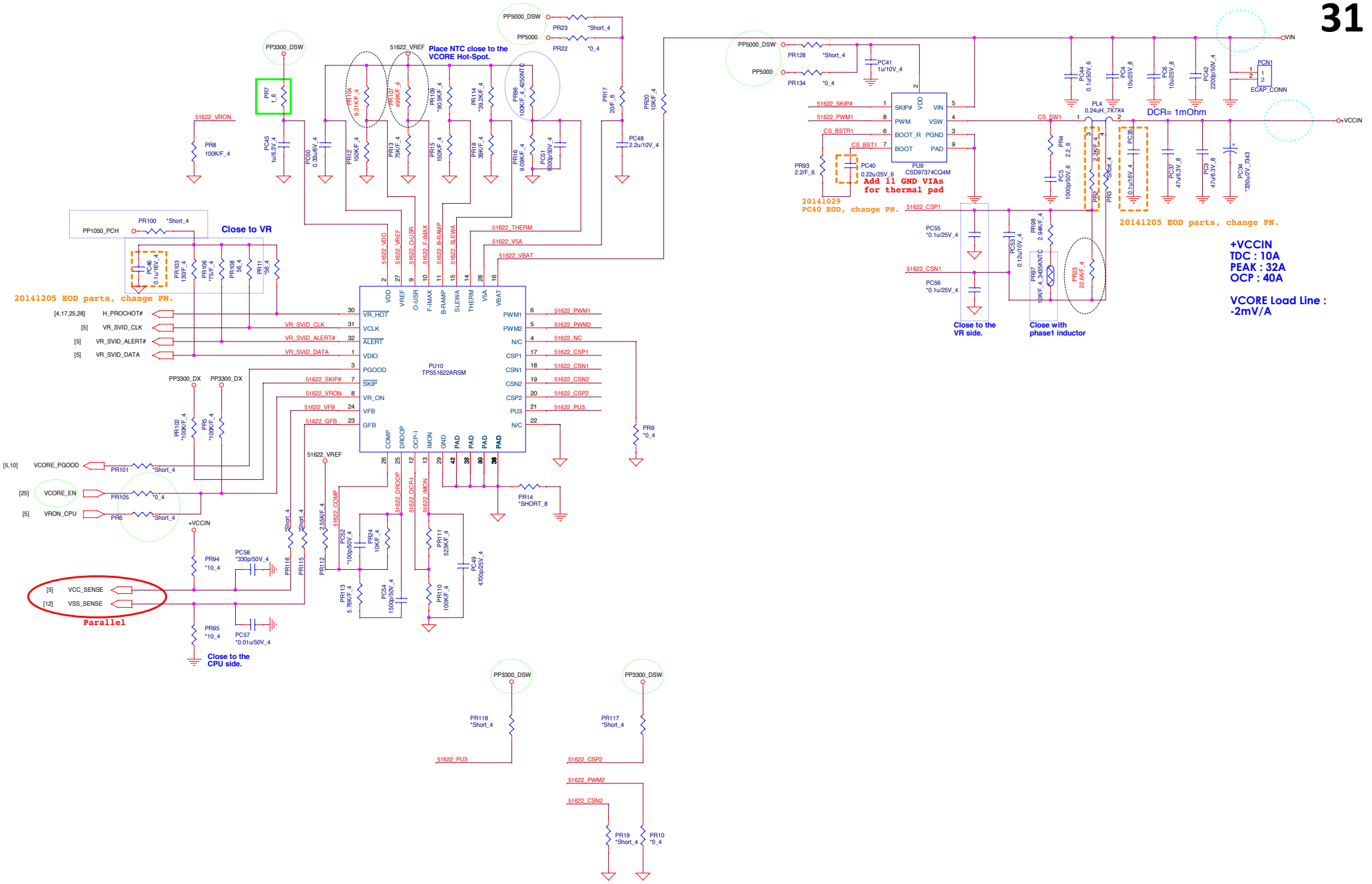
place at PQ37 area



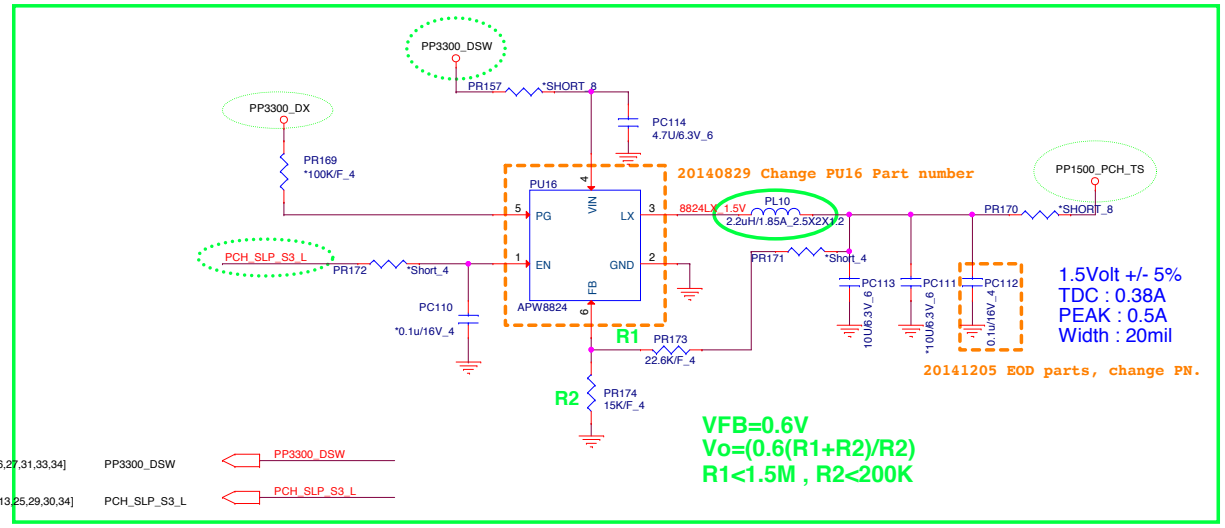
Quanta Computer Inc.

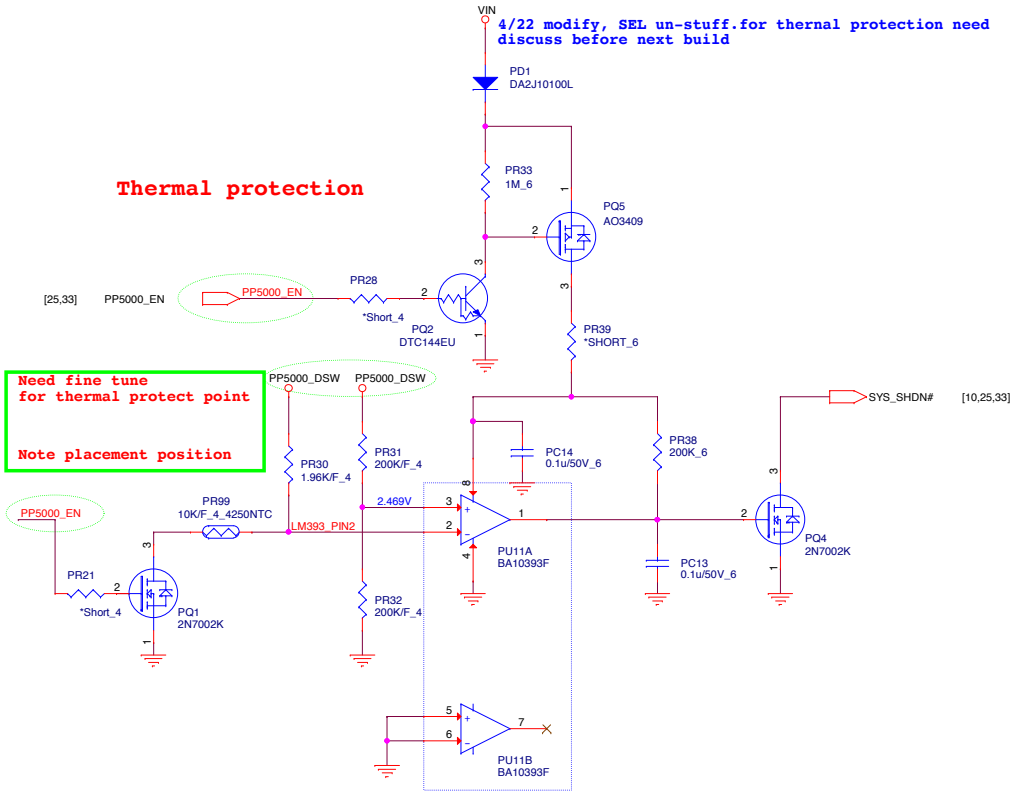
PROJECT : ZRF

Size	Document Number	Rev
	+1.05V (RT8237)	A
Date: Monday, January 12, 2015	Sheet 30 of 38	



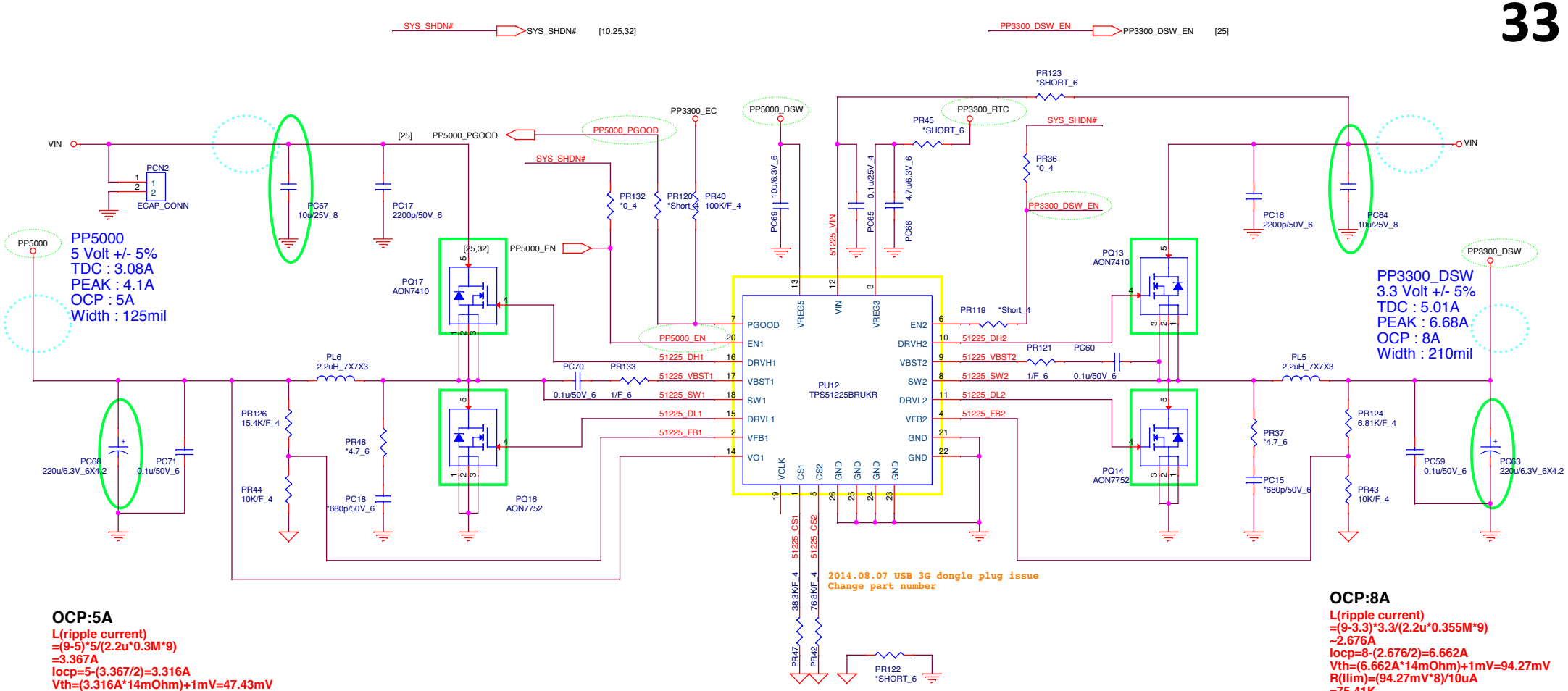
Quanta Computer Inc.		
PROJECT : ZRF		
Size	Document Number: +VCCIN(TPS51622)	Rev: A
Date: Monday, January 12, 2015	Sheet 31 of 38	



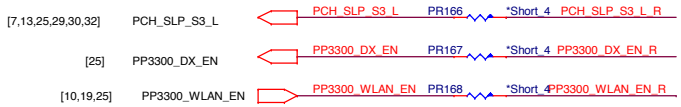


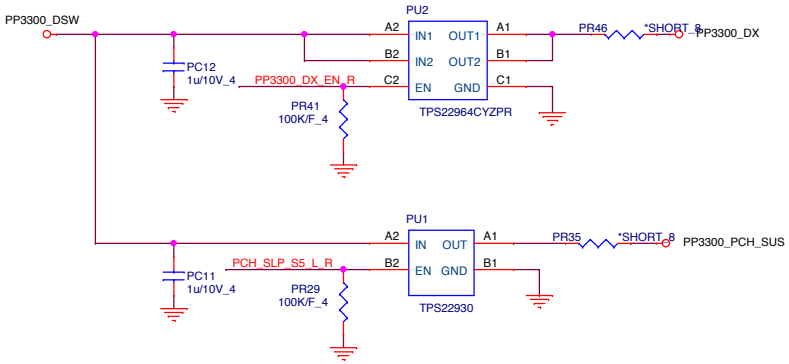
For EC control thermal protection (output 3.3V)

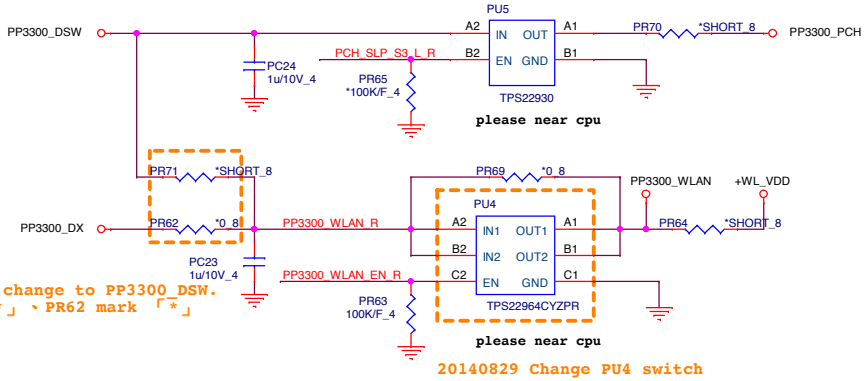
Quanta Computer Inc.			
PROJECT : ZRF			
Size	Document Number		Rev
	+1.5V/Thermal protect		A
Date: Monday, January 12, 2015	Sheet 32 of 38		



Quanta Computer Inc.		
PROJECT : ZRF		
Size	Document Number: SYSTEM 5V/3V (TPS51225)	Rev: A
Date: Monday, January 12, 2015	Sheet 33 of 38	

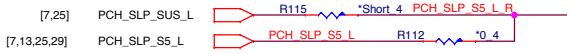






20140902 Power change to PP3300_DSW.
PR71 cancel 「*」、PR62 mark 「*」

20140829 Change PU4 switch



Quanta Computer Inc.
PROJECT : ZRF

Size	Document Number	Rev
	Load Switch	A

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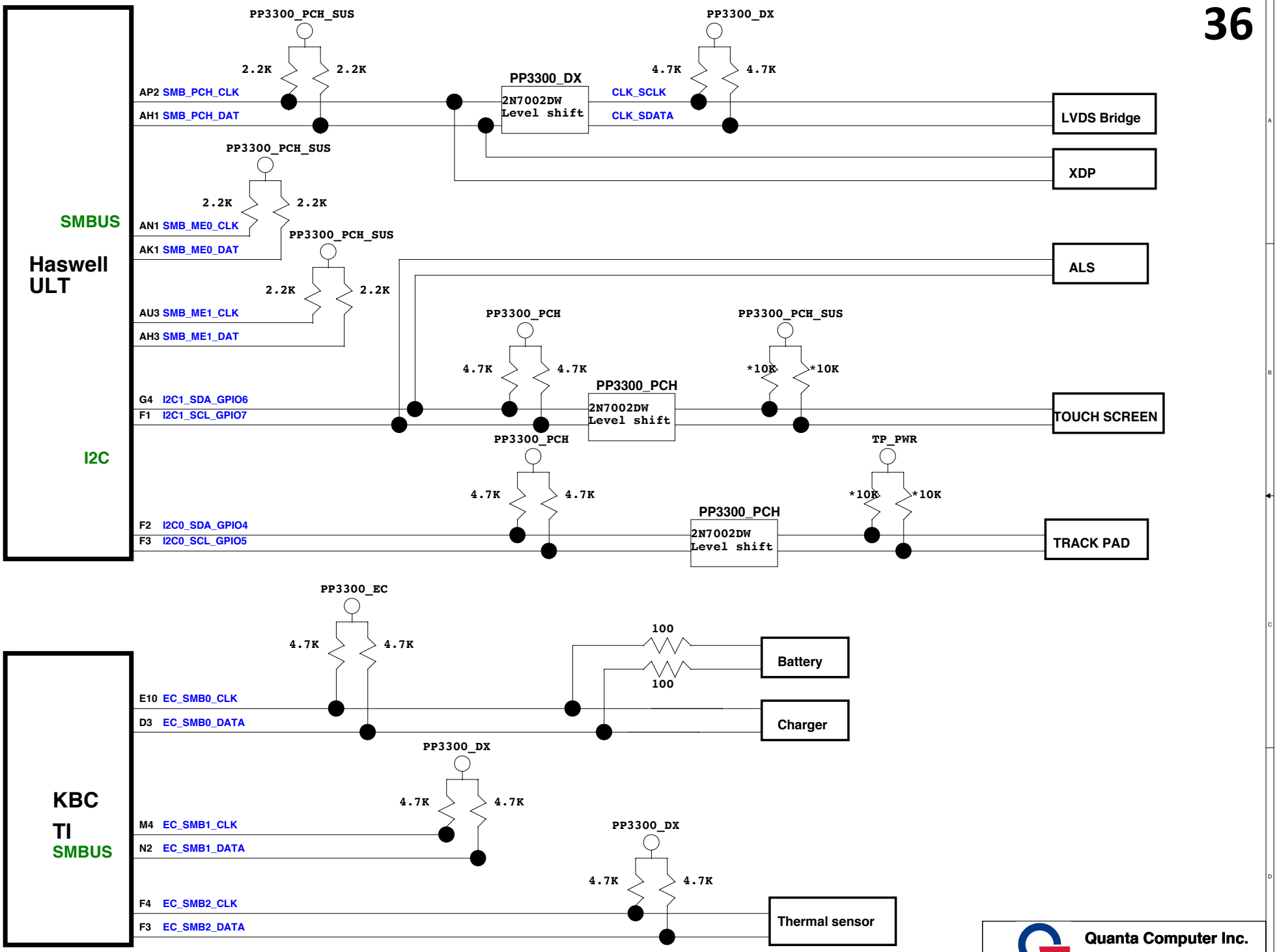
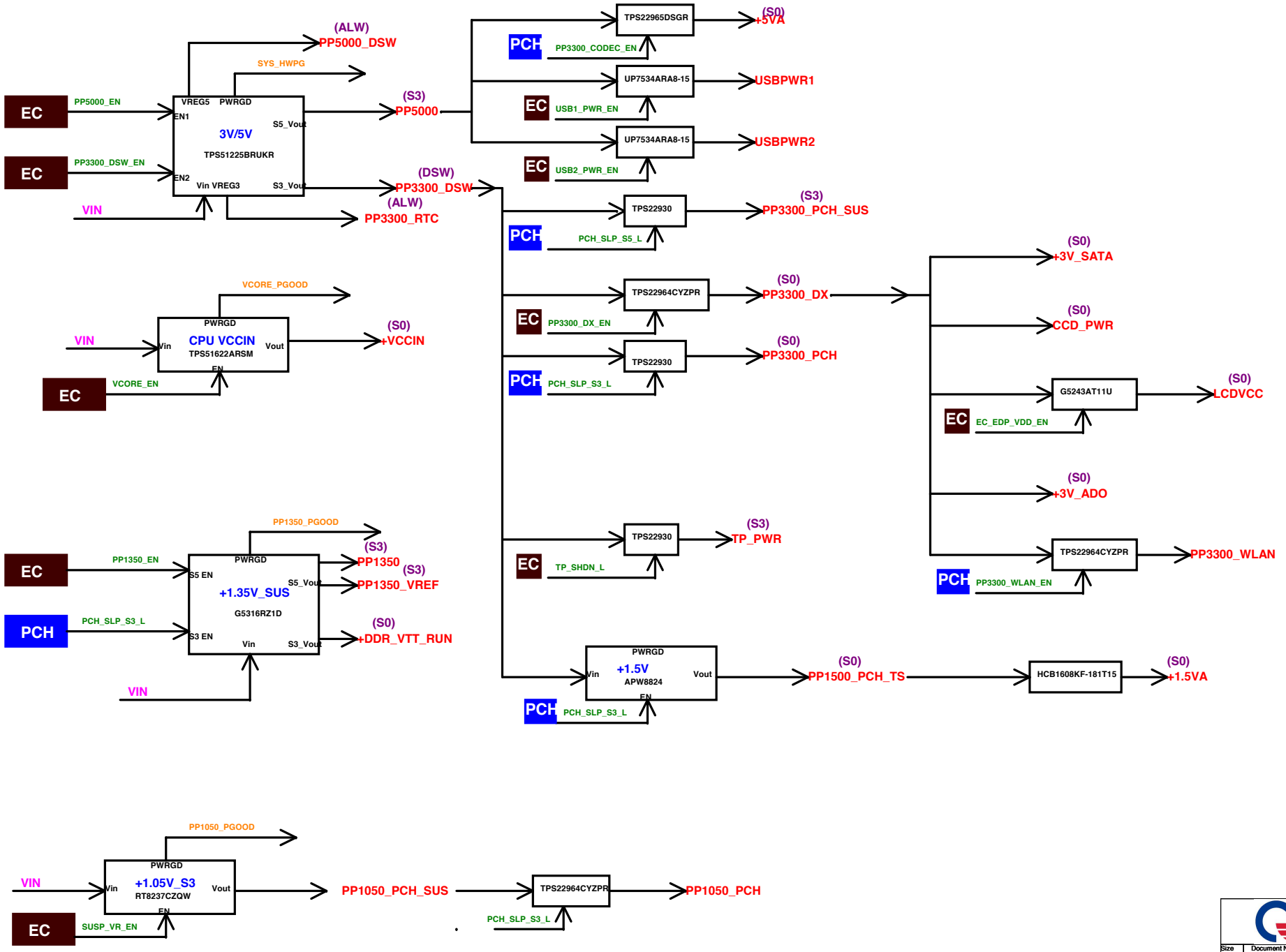
Battery Mode



Quanta Computer Inc.
PROJECT : ZRF

Size	Document Number	Rev
	SMBUS_I2C	A
Date: Monday, January 12, 2015	Sheet 36 of 38	



Quanta Computer Inc.

PROJECT : ZRF

Size	Document Number	Rev
	ULT PWR CONTROL	A
Date: Monday, January 12, 2015	Sheet 37 of 38	

Model	Version	CHANGE LIST
ZRF	1A-1	2014/07/28 Hall sensor change to LED board. (MR1) 2014/07/28 Page24: Change touchpad conn. as Hugo. (CN10) (change to larger pitch) 2014/07/28 Page25: Cardreader conn. 20 pin change to 22 pin. (CN9) 2014/07/28 Page24: Add Q44 on Track Pad INT# for leakage issue
	1A-2	2014/07/30 Page24: U17 change part NO. same as 0C7.
	1A-3	2014/08/04 Page16: LCD conn. 30pin change to 40pin, 1 LEN change to 2 LEN. (CN3)
	1A-4	2014/08/06 Page16: touchpanel level shift remove Q13 change to U38.
	1A-5	2014/08/07 Page24: Remove 3G/SIM, Q23 MOS 1 channel change to 2 channel, remove USBP9+ - USBP5+ pin, remove NGFF PCIE pin, remove NGFF CLK pin, GPIO59 pull high. 2014/08/07 Page33: System 5V/3V change part NO. (PU12)
	1A-6	2014/08/08 Page16: Touch panel INT/RST(TPS) mark 「*」 2014/08/08 Page24: Change CN10 same as ZQ0. 2014/08/08 Page27: LID_OPEN_L pin add TP139
	1A-7	2014/08/11 Page10: LTE_DISABLE_L (GPIO39) pull high to PP3300_PCH_SUS 2014/08/11 Page27: Remove light semor.
	1A-8	2014/08/12 Page16: touchpanel level shift remove U38 change to PJT138K. 2014/08/12 Page22: Codec pin27 add 100K resistance
	1A-9	2014/08/19 Page24: KB change to 30pin. 2014/08/19 Page27: CR cable connector change footprint
	1A-10	2014/08/20 Page19: Wifi on board IC change to same as ZS8 connector. 2014/08/20 Page28: PJ2 battery connector change to 10pin same as Z09. 2014/08/20 Page28: Add another PJ3 battery connector for A test.
	1A-11	2014/08/21 Page16: LCD conn. I2C1_SDA_GPIO6_CONN pin reserve a 15pF capacitor.
	1A-12	2014/08/22 Page19: Wifi return to another onboard module 7260SDW 2014/08/22 Page28: PJ3 battery connector change to 8pin same as Rexy.
	1A-13	2014/08/25 Page19: Change power capacitor value.
	1A-14	2014/08/26 Page28: Change power output MOS/capacitor. (PQ18 + PQ19 + PC75) 2014/08/26 Page29: Change power output MOS/capacitor. (PQ20 + PQ21 + PC31) 2014/08/26 Page30: Change power output MOS/capacitor. (PQ10 + PQ11 + PC47) 2014/08/26 Page32: Change 1.5V solution IC. 2014/08/26 Page33: Change power output MOS/capacitor. (PQ13 + PQ14 + PQ16 + PQ17 + PC63 + PC64 + PC67 + PC68) 2014/08/26 Page19: Wifi PCIE TX/RX swap, and RX add capacitor. 2014/08/26 Page19: Change wifi onboard module 7260SDW footprint.
	1A-15	2014/08/27 Page19: Pin W_DISABLE# / W_DISABLE#2 add 100K resistance pulldown. 2014/08/27 Page16: LCD conn. change PN / footprint same as ZQ0. 2014/08/27 Page18: Change HDMI conn. CN5 footprint.
	1A-16	2014/08/28 Page28: BATT conn. P12 mirror vertically. 2014/08/28 Page26: 1. Add HOLE27. 2.Change HOLE17/HOLE18/HOLE21/HOLE22/HOLE23/HOLE26 footprint. 3. Remove HOLE9/HOLE16. 2014/08/28 Page19: Wifi 100K resistance R631/R632 mark 「*」
	1A-17	2014/08/29 Page34: Change LDO PU4 switch 2014/08/29 Page28: Change PJ1 DC-IN part number. 2014/08/29 Page32: Change 1.5V PU16 part number.
	1A-18	2014/09/2 Page28: DC-in return to original PN.
	1A-19	2014/09/9 Page19: Change wifi onboard module 7260SDW footprint.
	1A-20	2014/09/12 Page16: C16 EOD, change PN. 2014/09/12 Page20: C379/C380/C381/C382 EOD, change PN. 2014/09/12 Page22: L45,7 EOD, change PN. 2014/09/12 Page25: C208/C352/C360/L15 EOD, change PN. 2014/09/12 Page28: PC87/PJ1 EOD, change PN. 2014/09/12 Page29: PC100 EOD, change PN. 2014/09/12 Page30: PR83 EOD, change PN.
	1B-1	2014/09/22 Page22: A-MIC change to D-MIC same as Hugo(ZHQ).
	1B-2	2014/09/23 Page26: Add Lid Switch (HSI) 2014/09/23 Page22: D-MIC PWR remove PP1800_PCH, change use PP3300_PCH.
	1B-3	2014/09/24 Page26: USB3.0 U8 P1/P2 add C399/D34.
	1B-4	2014/09/25 Page27: Thermal MOSFET Q25/Resistance R585 mark 「*」 un-stuff. OVERT# power PP3300_DX change to PP3300_EC.
	1B-5	2014/09/26 Page22: Change CN12 footprint.
	1B-6	2014/09/30 Page23: Change CN7 Audio_Jack PN. & footprint. 2014/09/30 Page16: Change CN3 LCD conn. footprint. 2014/09/30 Page25: Change U5 EC PN.
	1B-7	2014/10/02 Page24: KB change PN./Footprint.
	1C-1	2014/10/09 Page25: EC N12 pin add BAT_ID to identify 48watt BATT. conn. & add R633 pull high. 2014/10/09 Page28: BATT. conn. add BAT_ID to identify 48watt BATT.
	1C-2	2014/10/14 Page19: Change wifi onboard module 7260SDW PN.
	1C-3	2014/10/15 Page24: Fan connector Pin3/Pin4 reserve 1000pF capacitor for EMI solution.
	1C-4	2014/10/16 Page28: Change DC-in PN. (new module)
	1C-5	2014/10/20 Page34: LDO PU4 power change to PP3300_DSW, PR71 cancel 「*」 + PR62 mark 「*」
	1C-6	2014/10/21 Page16: LCD conn. footprint return to ZQ0. 2014/10/21 Page13: Intel require modify ITP CN15 P9/P51 add PP1050_PCH_SUS, P50 PP1050_PGOOD change to VCCST_PWRGD.
	1D-1	2014/10/29 Page31: PC40 EOD, change PN.
	1D-2	2014/11/12 Page22: C193 change to 0.1uF. 2014/11/12 Page all: 0 ohm resistance change to short pad.
	1D-3	2014/11/18 Page22/Page25: change D27/D28 PN.
	1D-4	2014/11/20 Page25 Change EC_BRD_ID, ID2 change to High, ID3 change to Low, because EC change code.
	1D-5	2014/11/25 Page28 Change PR73 to un-stuff.
	1D-6	2014/12/01 Page21 Change TPM power. 2014/12/01 Page22 DMIC_CLK_L reserve 22pF capacitor. 2014/12/01 Page25 Change EC new PN. 2014/12/01 Page27 Stuff L12, remove R371/R372. 2014/12/01 Page28 Change DC-in footprint.
	1D-6	2014/12/02 Page28 Change PJ2 to un-stuff.
	1D-7	2014/12/05 CH4102K1B03 EOD parts, change PN. CH4103K1B08. 2014/12/05 CH4102K.B93 EOD parts, change PN. CH4103K1B08. 2014/12/05 CS22212FB11 EOD parts, change PN. CS22202FB08. 2014/12/05 「R549/R550/R598/R600/140/R307/R313/R360/R381/R388/R147/R415/R421/R477/R478/R492/R493/R61/R74/R351/R429/R55/R355/R399/R374/R100/R109/R124/R192/R278/R285/R286/R198/R205/R259/R260/R502/R512/R558/R489/R584/R148/R491/R152/R133/R425/R51/R93/R94/R102/R117/R422/PR3/R284/R555/R559/R562/R563/R546/PR129/PR130/PR145/PR147/PR154/PR156/PR34/PR73/PR171/PR172/PR117/PR118/R204/R206/R287/R519/R567/R568/PR160/PR162/PR163/PR165/PR82/PR88/PR100/PR101/PR115/PR116/PR126/PR19/PR23/PR86/PR21/PR28/PR119/PR120/R369/R38/R105/R411/R414/R451/R459/R489/R88/R297/R72/R371/R372/R443/R445/R461/R167/R217/R276/R436/R171/R179/R191/R194/R497/R598/R551/R552/R0/PR166/PR167/PR168/R115/L17/L20/R456/R168/R125/R18/R19/R52/R53/R54/R67/R9/R95/R11/PR146/R408/R103/R107/R23/R202/R220/R252/R264/PR158/PR86/PR91/PR39/PR122/R270/R271/R272/R273/R14-49/L6/PR135/PR123/PR45/R34/R59/R17/R22/R303/R304/R468/R84/R76/R289/PR14/PR170/PR175/PR35/PR46/PR64/PR70/PR71」 0 ohm change to shortpad.
	1D-8	2015/01/09 Page25 Change U15 EC IC PN. for MP.
	1D-9	2015/01/12 Page28 Change resistance PR151/PR152 to 0 ohm to solve 4-cell battery ripple issue.

DOC NO.	PROJECT MODEL :	Chrome	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

Quanta Computer Inc.
PROJECT : ZRF
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