GA-970A-D3

Revision : 3.02

GIGABYTE™

Title	COVER SHEET
Size	Custom
Document Number	GA-970A-D3
Rev	3.02
Date:	Monday, October 08, 2012
Sheet	1 of 36

Model Name:GA-970A-D3

Component value change history

Version: 3.02

P-Code: U98094-0

Date	Change Item		Reason
2012.07.17	9M970AD3-00-30A	PCB Ver 3.0	
2012.08.09	9M970AD3-00-30B	PCB Ver 3.01	
2012.10.02	9M970AD3-00-30C	PCB Ver 3.02	

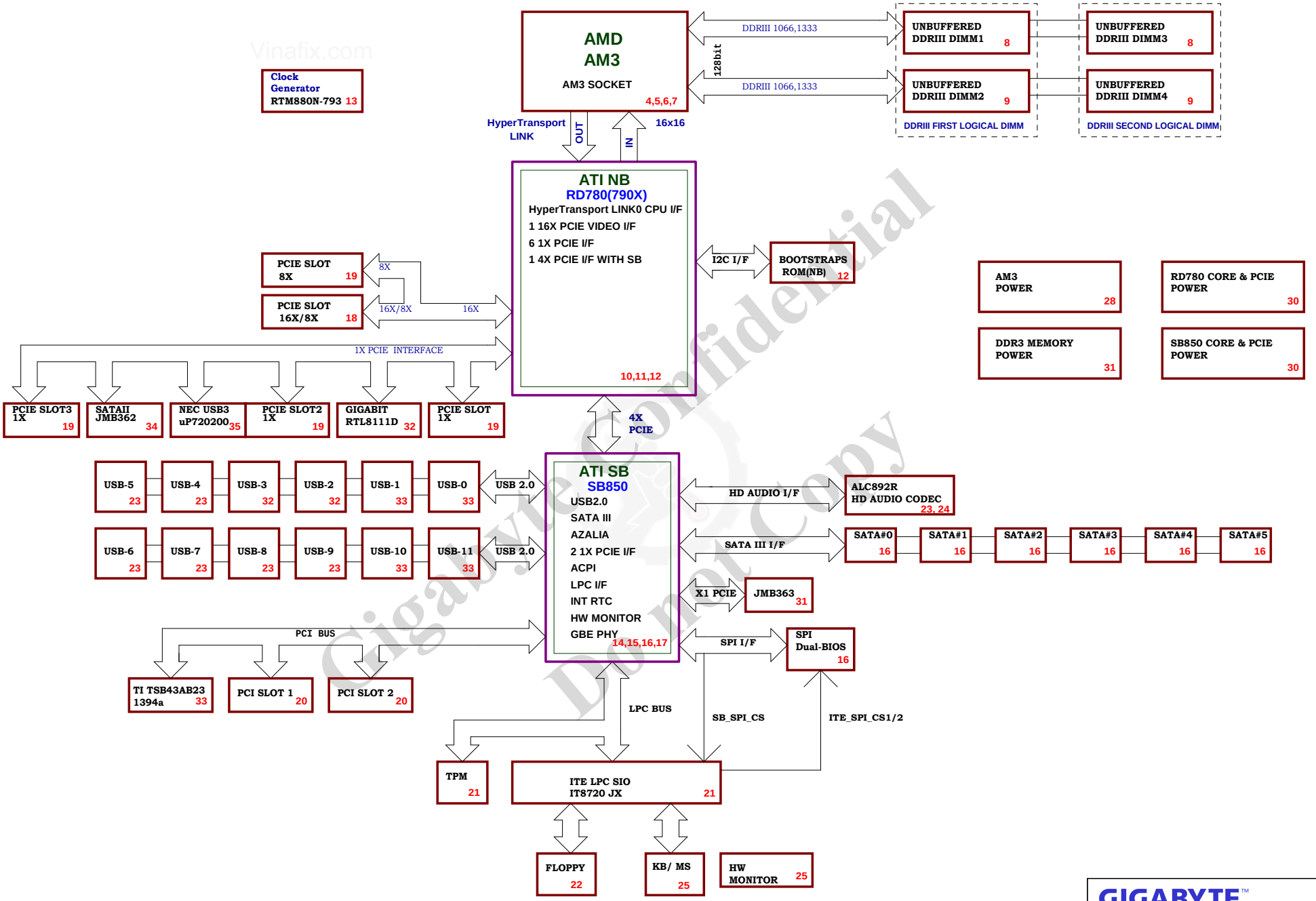
Circuit or PCB layout change for next version

Date	Change Item	Reason
2012.07.17	MODIFY TO 970A-D3 REV1.3	
2012.07.17	1.I/O 8720 change 8728 2.新增erp 0.5w control線路 3.5VDUAL改由PWROK控制 4.Etron usb3.0 pin88.89 接GND(新製程IC)	
2012.08.09	ADD EPR POWER ISSUE	
	EPR GP53 ISSUE	
2012.10.02	調整POWER +-5%不開ISSUE 移除 " EASY ENERGY SAVER"	9M970AD3-00-30C

2012.10.02

GIGABYTE™

Title	BOM & PCB HISTORY	
Size: Custom	Document Number: GA-970A-D3	Rev: 3.02
Date: Monday, October 08, 2012	Sheet 2 of 36	



GIGABYTE™

Title: BLOCK DIAGRAM

Size	Document Number	Rev
Custom	GA-970A-D3	3.02

Date: Thursday, October 04, 2012 Sheet 3 of 36

L0_CADIN_L[0..15] — L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15] — L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15] — L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15] — L0_CADOUT_H[0..15] 10

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

10 L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 10
10 L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 10
10 L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 10
10 L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 10
10 L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 10
10 L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 10
10 L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 10
10 L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 10
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AE5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AE4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AE1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/942AM3b/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

COUPON1 — COUPON1 1 2 COUPON/X — VCC
COUPON2 — COUPON2 1 2 COUPON/X

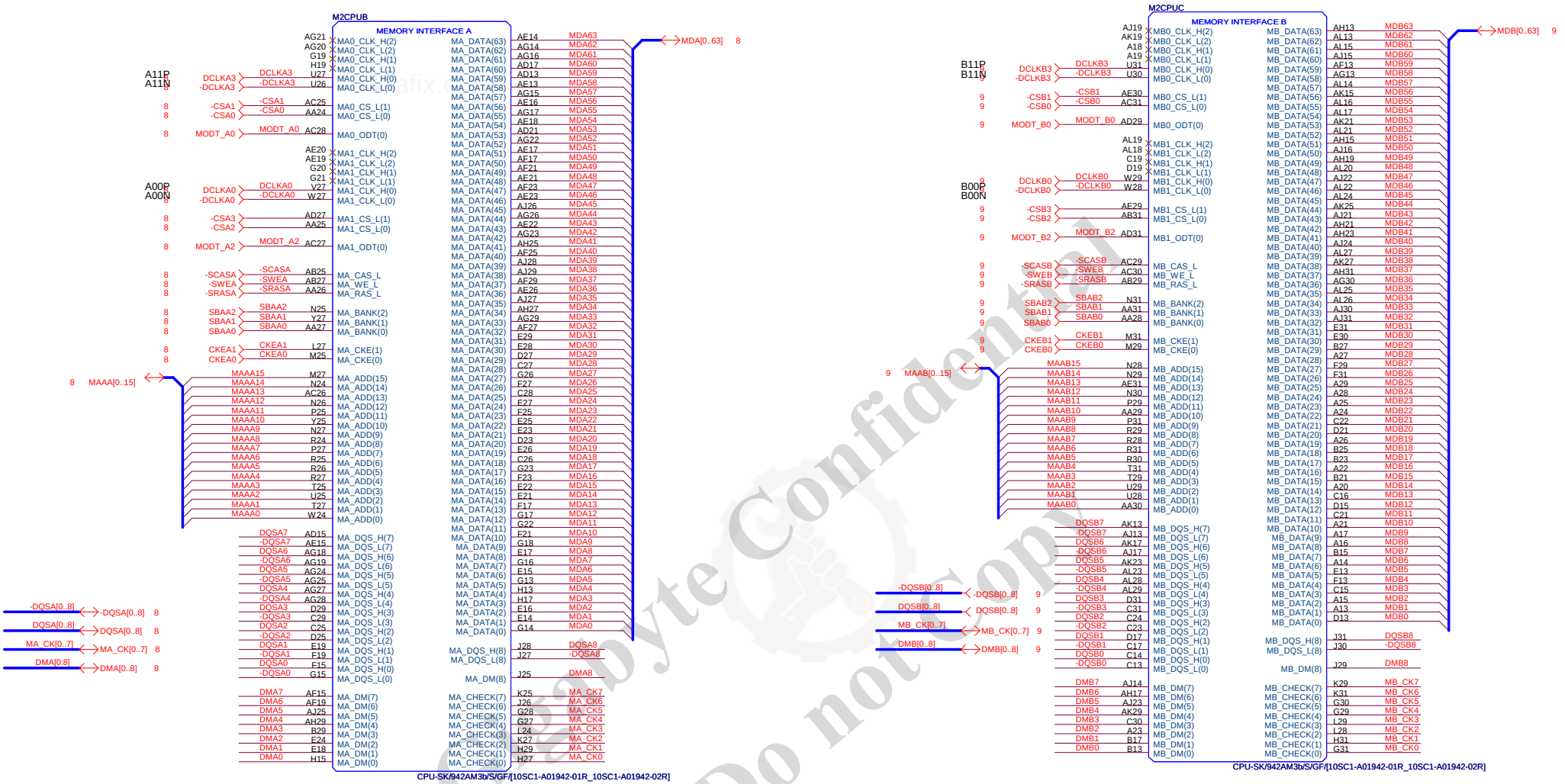
M2CPU
AM3RM/SC/BL/MB/[12KRC-04K812-31R_12KRC-04K812-32R]

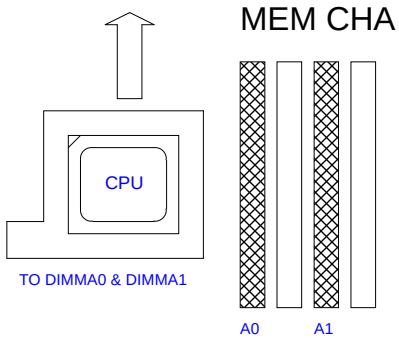
GIGABYTE™

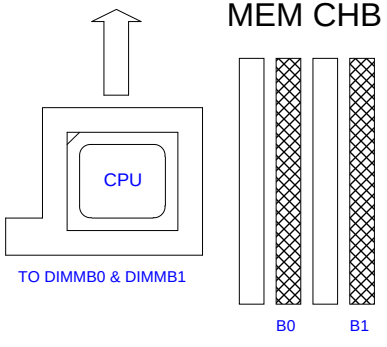
Title: CPU HYPER TRANSPORT

Size	Document Number	Rev
Custom	GA-970A-D3	3.02

Date: Thursday, October 04, 2012 Sheet 4 of 36

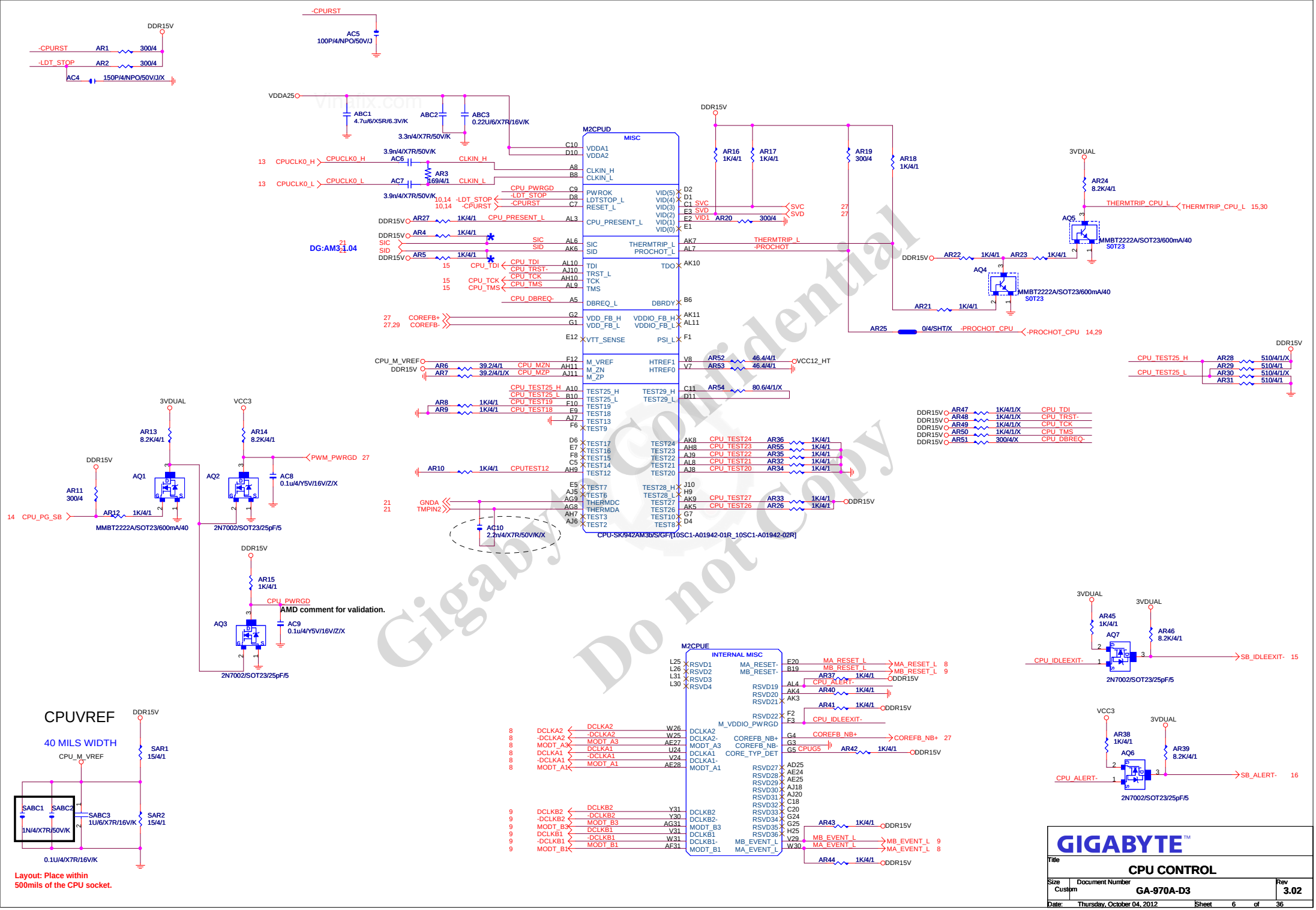






GIGABYTE™

Title	CPU DDRIII MEMORY	
Size: Custom	Document Number: GA-970A-D3	Rev: 3.02
Date: Thursday, October 04, 2012	Sheet 5 of 36	


-CPURST
AC5
100P/4/NPO/50V/J
DDR15V
-CPURST
AR1
300/4
-LDT_STOP
AR2
300/4
AC4
150P/4/NPO/50V/J/X
VDDA25
ABC1
4.7u/6/X5R/6.3V/K
ABC2
3.3n/4/X7R/50V/K
ABC3
0.22U/6/X7R/16V/K
M2CPUD
MISC
VDDA1
VDDA2
CLKIN_H
CLKIN_L
PWROK
LDTSTOP_L
RESET_L
CPU_PRESENT_L
VID(5)
VID(4)
VID(3)
VID(2)
VID(1)
VID(0)
SIC
SID
THERMTRIP_L
PROCHOT_L
TDI
TRST_L
TCK
TMS
TDO
DBREQ_L
DBRDY
VDD_FB_H
VDD_FB_L
VDDIO_FB_H
VDDIO_FB_L
VTT_SENSE
PSI_L
M_VREF
M_ZN
M_ZP
HTREF1
HTREF0
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST17
TEST16
TEST15
TEST14
TEST12
TEST7
TEST6
THERMDC
THERMDA
TEST3
TEST2
TEST29_H
TEST29_L
TEST24
TEST23
TEST22
TEST21
TEST20
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
CPU-SKt/942AM3b/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]
DG:AM3.1.04
CPUCLK0_H
CPUCLK0_L
CLKIN_H
CLKIN_L
CPU_PWRGD
-LDT_STOP
-CPURST
CPU_PRESENT_L
SIC
SID
CPU_TDI
CPU_TRST-
CPU_TCK
CPU_TMS
CPU_DBREQ-
COREFB+
COREFB-
CPU_M_VREF
CPU_TEST25_H
CPU_TEST25_L
CPU_TEST19
CPU_TEST18
CPUTEST12
GNDA
TMPIN2
AC10
2.2n/4/X7R/50V/K/X
AR3
169/4/1
AR4
AR5
AR27
AR6
39.2/4/1
AR7
39.2/4/1/X
AR8
AR9
AR10
CPU_MZN
CPU_MZP
CPU_PRESENT_L
AR16
1K/4/1
AR17
1K/4/1
AR18
1K/4/1
AR19
300/4
AR20
300/4
SVC
SVD
VID1
THERMTRIP_L
-PROCHOT
AR21
AR22
AR23
AR24
8.2K/4/1
AR25
0/4/SHT/X
-PROCHOT_CPU
THERMTRIP_CPU_L
AQ4
AQ5
MMBT2222A/SOT23/600mA/40
S0T23
AR52
46.4/4/1
AR53
46.4/4/1
VCC12_HT
AR54
80.6/4/1/X
AR47
AR48
AR49
AR50
AR51
CPU_TDI
CPU_TRST-
CPU_TCK
CPU_TMS
CPU_DBREQ-
AR28
AR29
AR30
AR31
510/4/1/X
510/4/1
3VDUAL
VCC3
AR13
8.2K/4/1
AR14
8.2K/4/1
AR11
300/4
AR12
AQ1
AQ2
AC8
0.1u/4/Y5V/16V/Z/X
PWM_PWRGD
CPU_PG_SB
MMBT2222A/SOT23/600mA/40
2N7002/SOT23/25pF/5
AR15
1K/4/1
CPU_PWRGD
AQ3
AC9
0.1u/4/Y5V/16V/Z/X
AMD comment for validation.
M2CPUE
INTERNAL MISC
RSVD1
RSVD2
RSVD3
RSVD4
MA_RESET-
MB_RESET-
RSVD19
RSVD20
RSVD21
RSVD22
M_VDDIO_PWRGD
DCLKA2
DCLKA2-
MODT_A3
DCLKA1
DCLKA1-
MODT_A1
COREFB_NB+
COREFB_NB-
CORE_TYP_DET
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
DCLKB2
DCLKB2-
MODT_B3
DCLKB1
DCLKB1-
MODT_B1
MB_EVENT_L
MA_EVENT_L
MA_RESET_L
MB_RESET_L
CPU_ALERT-
CPU_IDLEEXIT-
CPUG5
AR37
AR40
AR41
AR42
AR43
AR44
MB_EVENT_L
MA_EVENT_L
AR45
1K/4/1
AR46
8.2K/4/1
AQ7
CPU_IDLEEXIT-
SB_IDLEEXIT-
2N7002/SOT23/25pF/5
AR38
1K/4/1
AR39
8.2K/4/1
AQ6
CPU_ALERT-
SB_ALERT-
CPUVREF
40 MILS WIDTH
CPU_M_VREF
SAR1
15/4/1
SAR2
15/4/1
SABC1
SABC2
1N/4/X7R/50V/K
SABC3
1U/6/X7R/16V/K
0.1U/4/X7R/16V/K
Layout: Place within
500mils of the CPU socket.
GIGABYTE
Title
CPU CONTROL
Size
Custom
Document Number
GA-970A-D3
Rev
3.02
Date:
Thursday, October 04, 2012
Sheet
6
of
36
Gigabyt Confidential
Do not Copy

VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

M2CPUE
VDD1

AE9 Missing pins on package and socket used for mechanical keying. =>AM3

M2CPUG
VDD2

H22 Missing pins on package and socket used for mechanical keying. =>AM3

M2CPUH
VDD3

AM3 Only

M2CPUI
VDDIO

BUTTOM SIDE

BUTTOM SIDE

AMD Validation

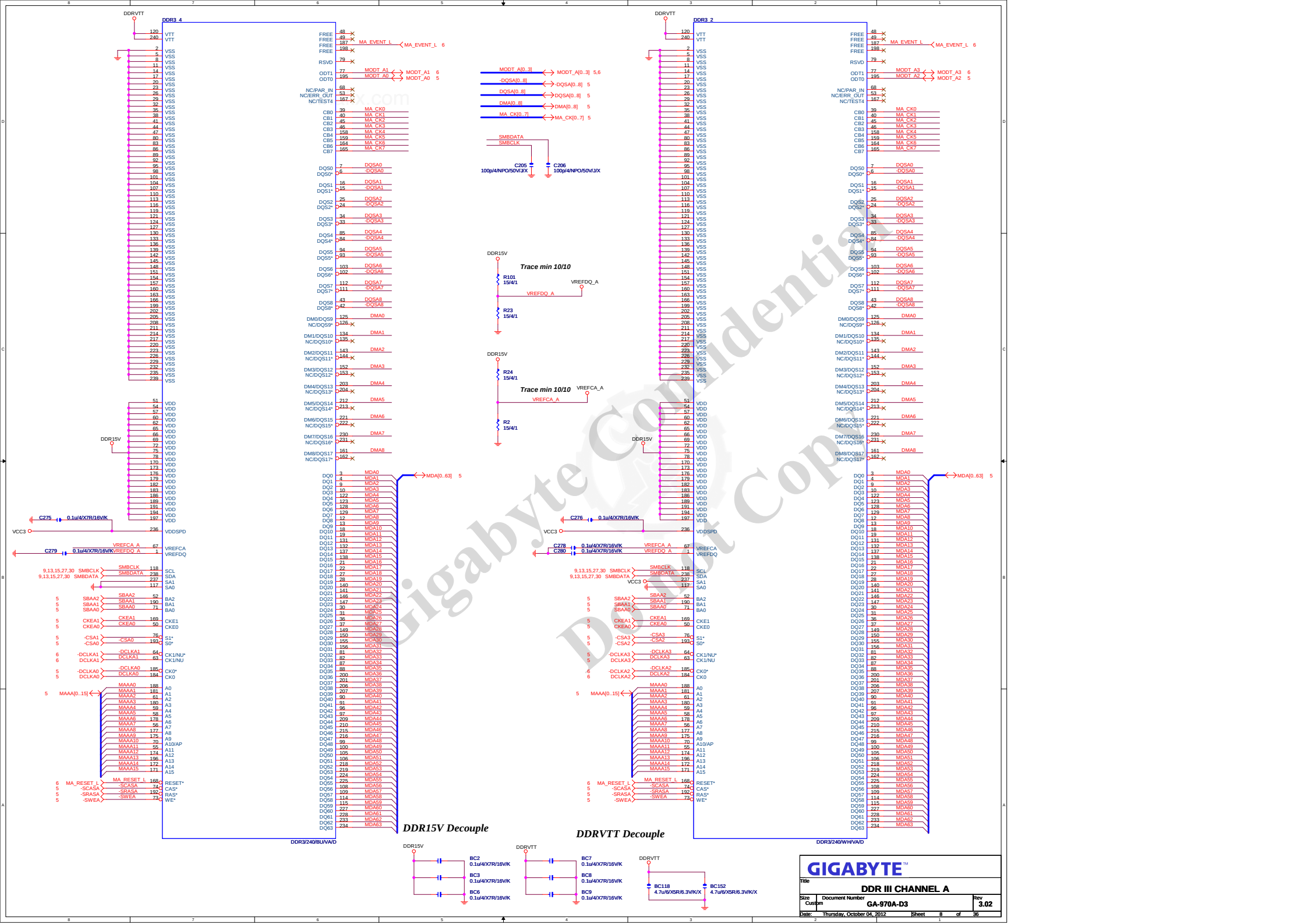
BUTTOM SIDE

AMD Validation

AMD Validation

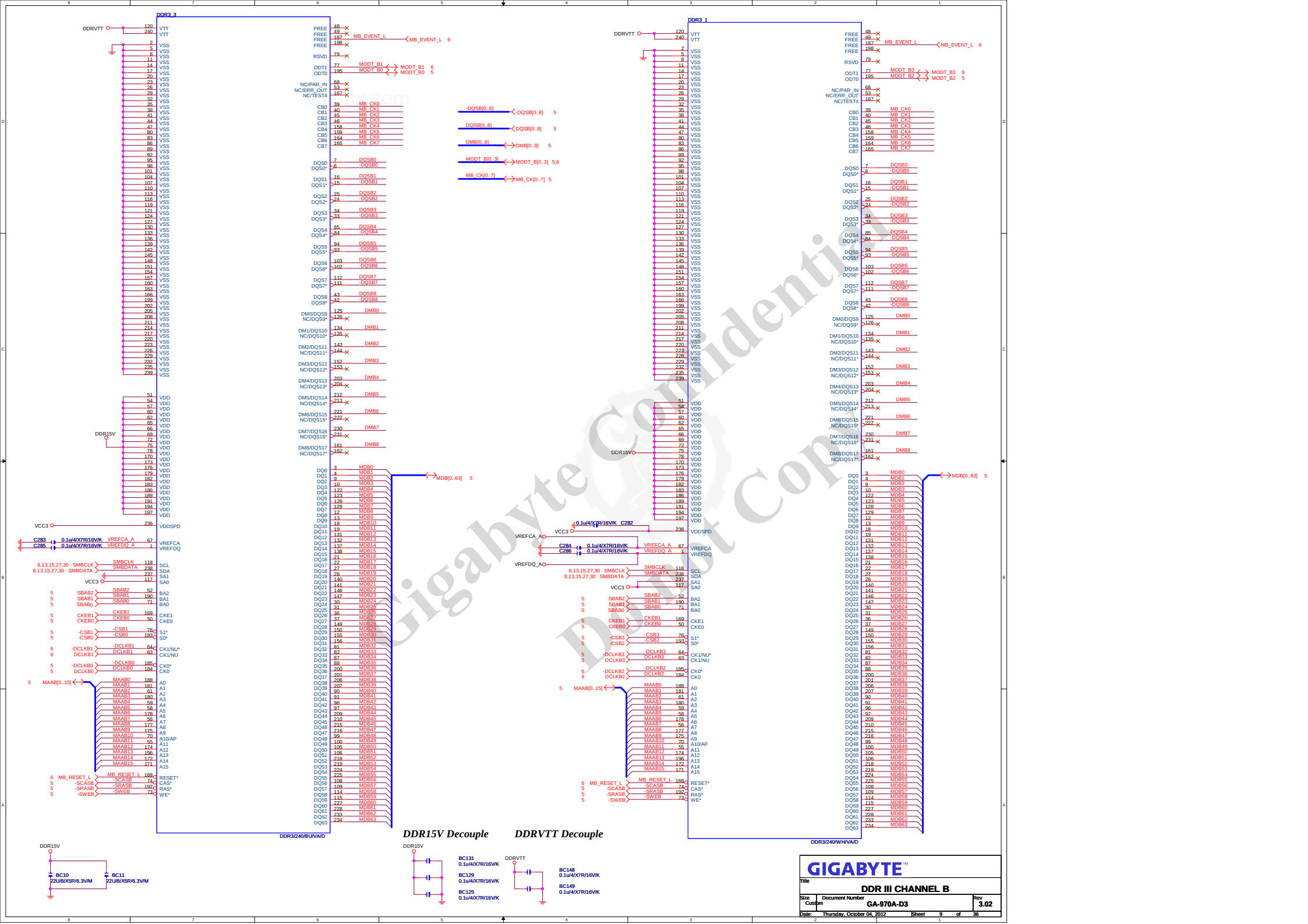
1021 EMI

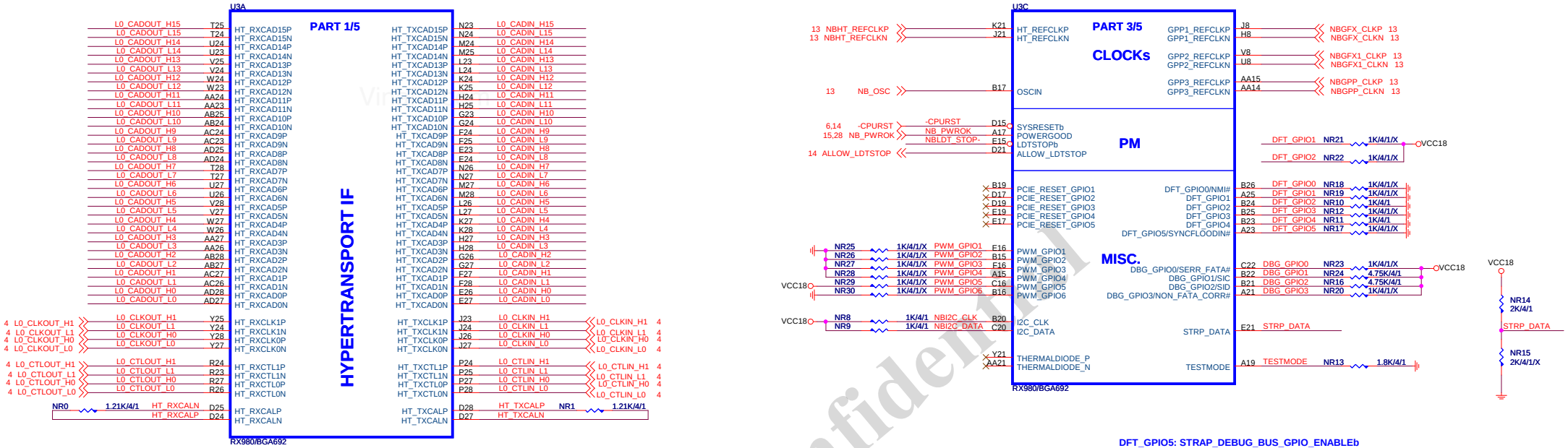
Title	CPU POWER & GND	
Size: Custom	Document Number: GA-970A-D3	Rev: 3.02
Date: Thursday, October 04, 2012	Sheet 7 of 36	

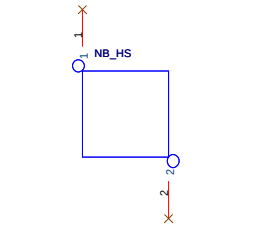


GIGABYTE™

Title	DDR III CHANNEL A	
Size: Custom	Document Number: GA-970A-D3	Rev: 3.02
Date: Thursday, October 04, 2012	Sheet 8 of 36	







DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

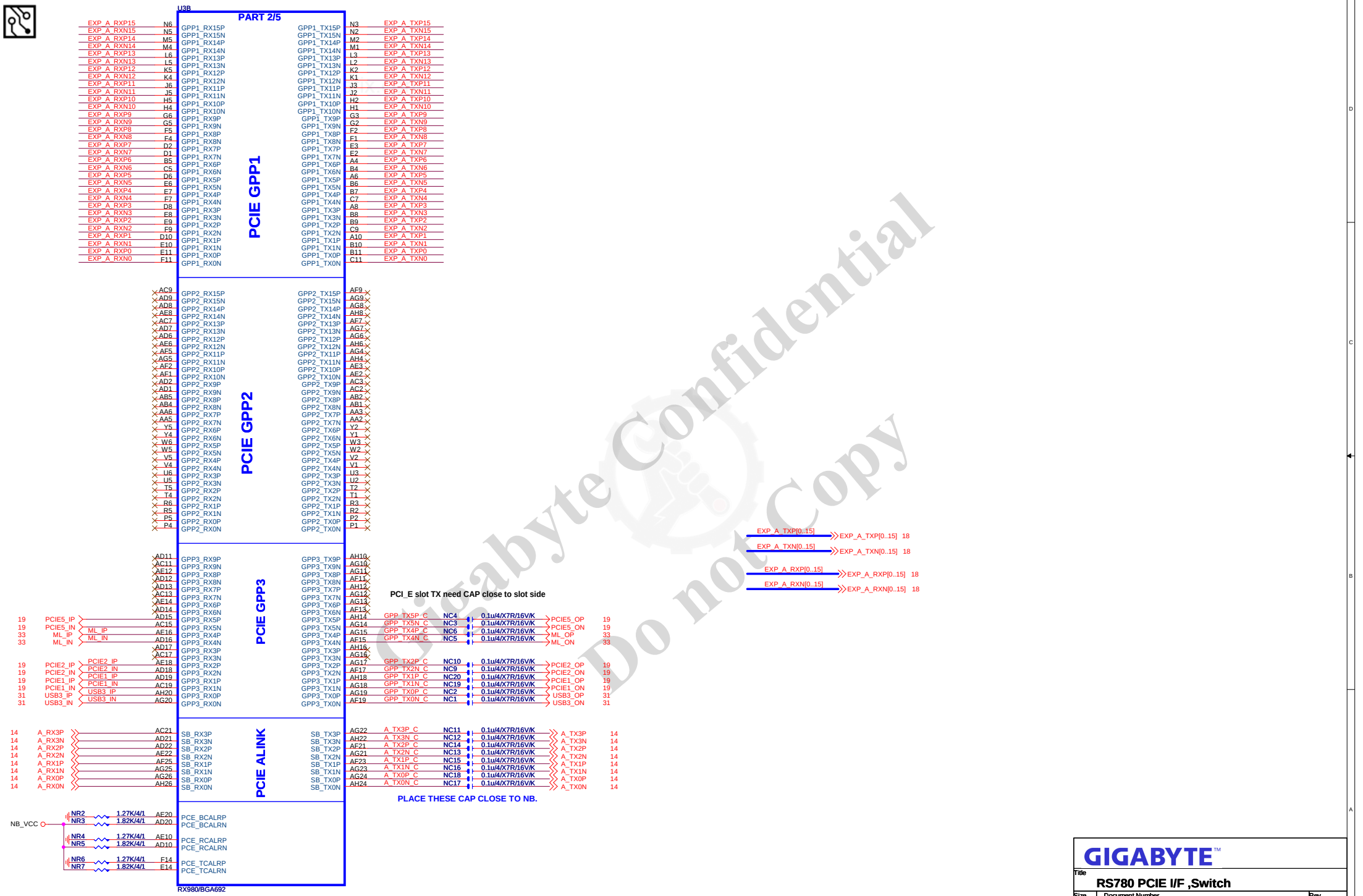
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

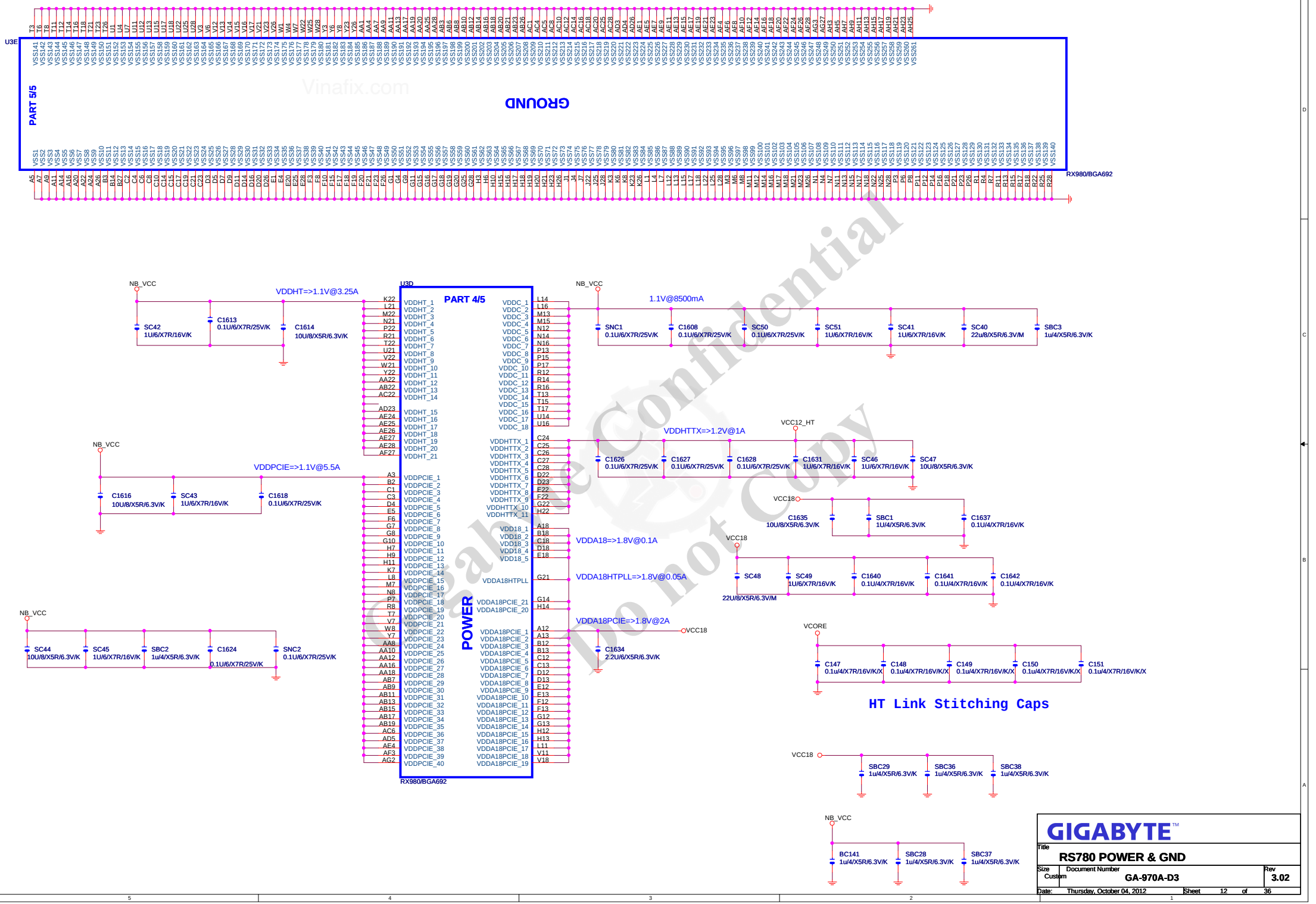
DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

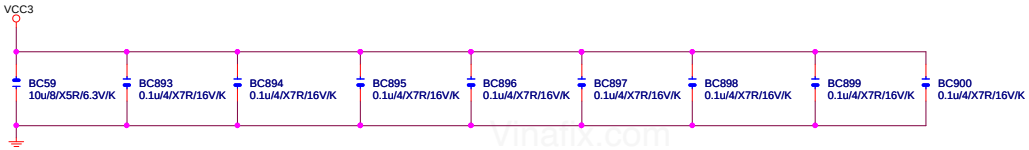
Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

GIGABYTE™

Title	RS780 HT-LINK I/F	
Size: Custom	Document Number: GA-970A-D3	Rev: 3.02
Date: Thursday, October 04, 2012	Sheet 10 of 36	


U3B
PART 2/5
PCIE GPP1
PCIE GPP2
PCIE GPP3
PCIE ALINK
RX980/BGA692
PCI_E slot TX need CAP close to slot side
PLACE THESE CAP CLOSE TO NB.
NB_VCC
Gigabyte Confidential
Do not Copy
GIGABYTE
Title
RS780 PCIE I/F ,Switch
Size
Custom
Document Number
GA-970A-D3
Rev
3.02
Date: Thursday, October 04, 2012
Sheet 11 of 36





1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

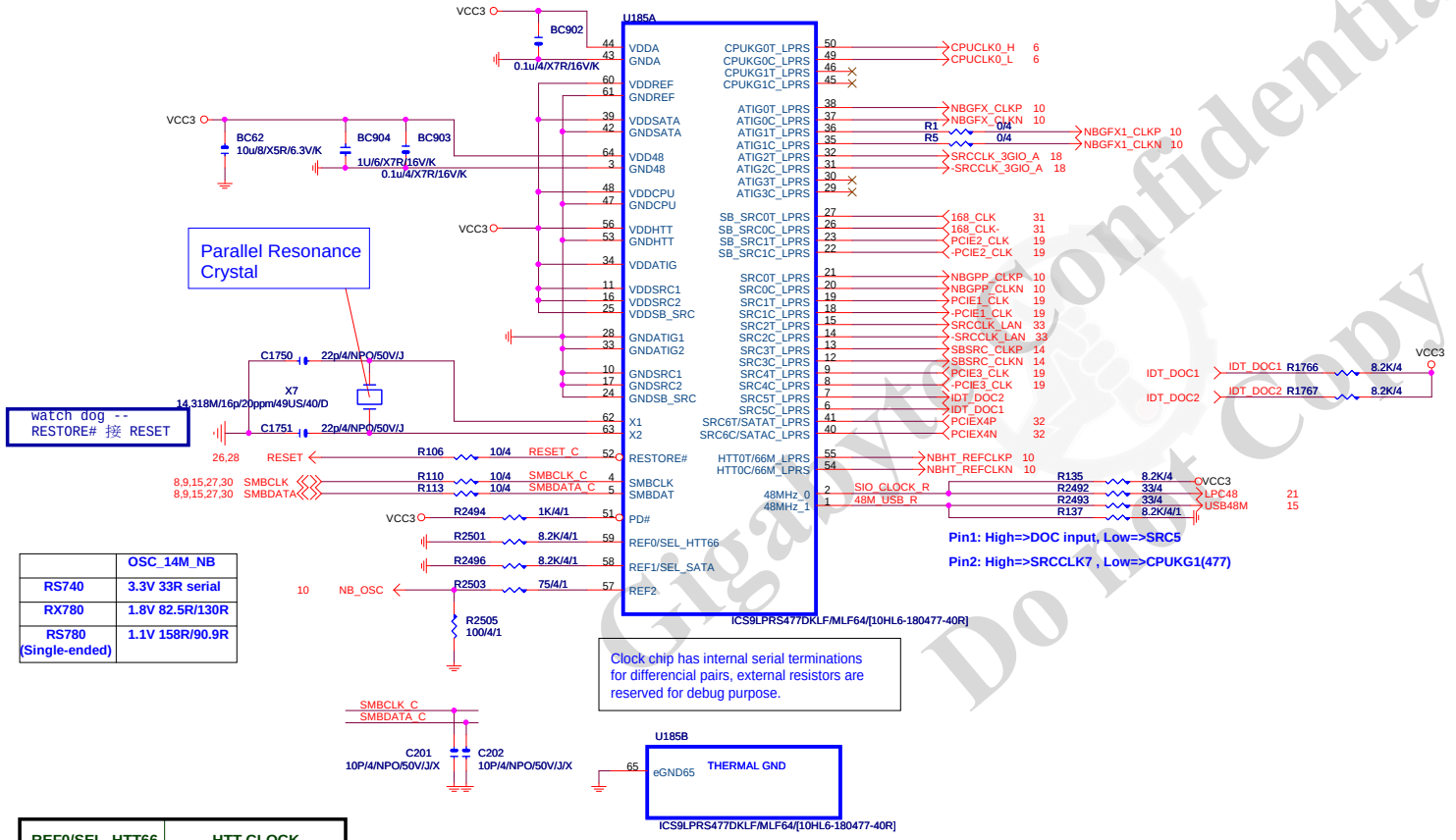
3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



Pin1: High=>DOC input, Low=>SRC5

Pin2: High=>SRCCLK7 , Low=>CPUKG1(477)

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

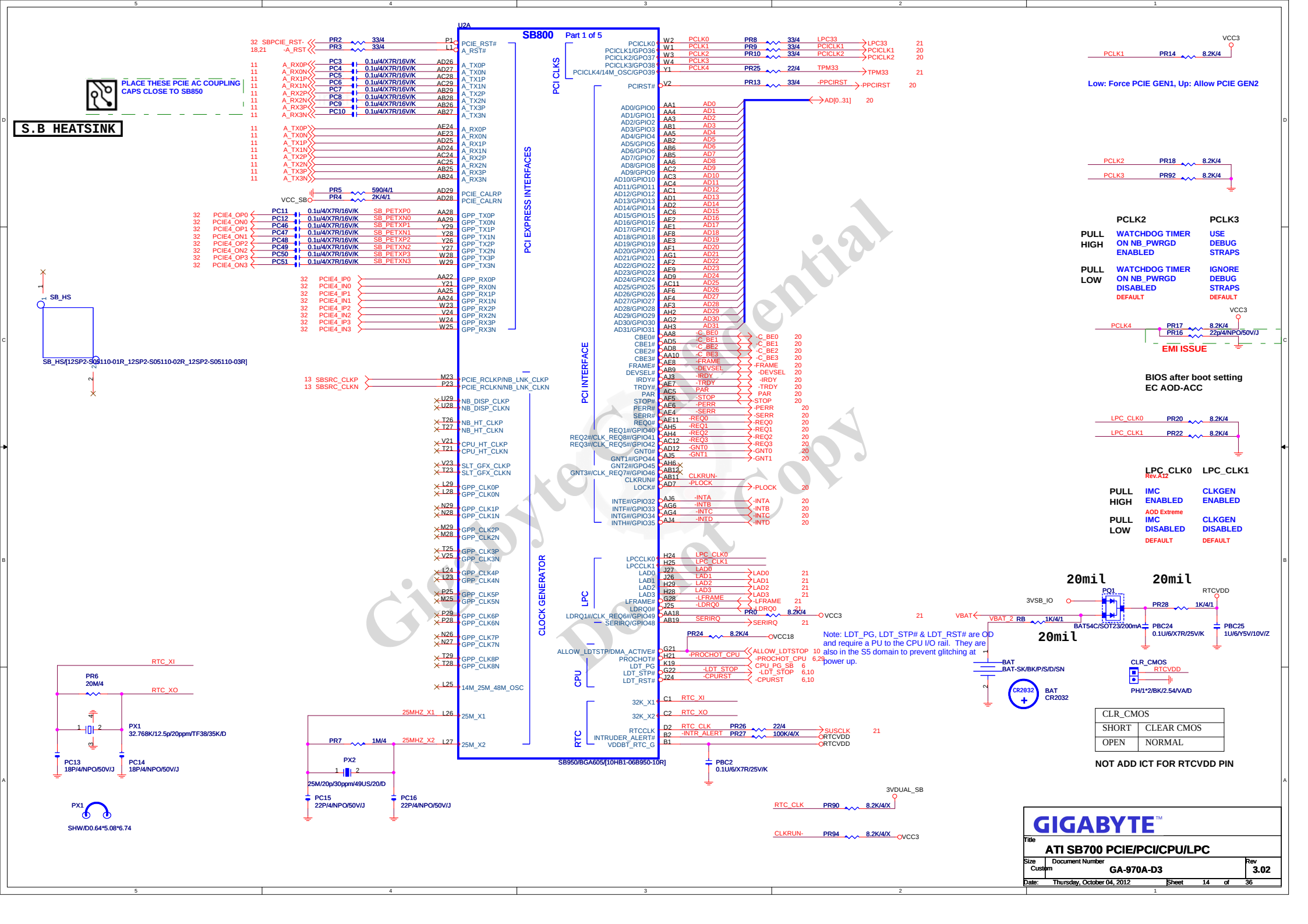
REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

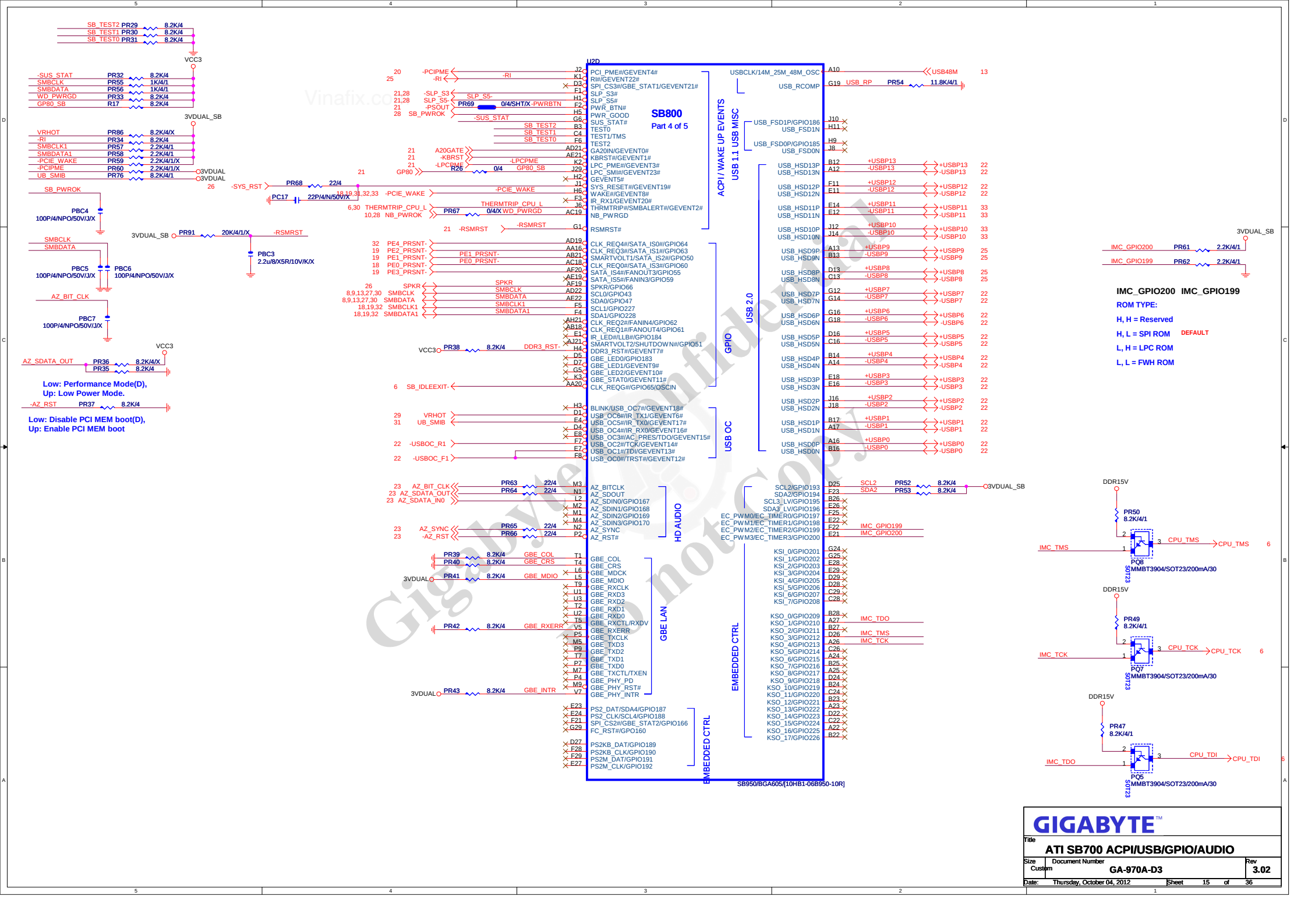
GIGABYTE™

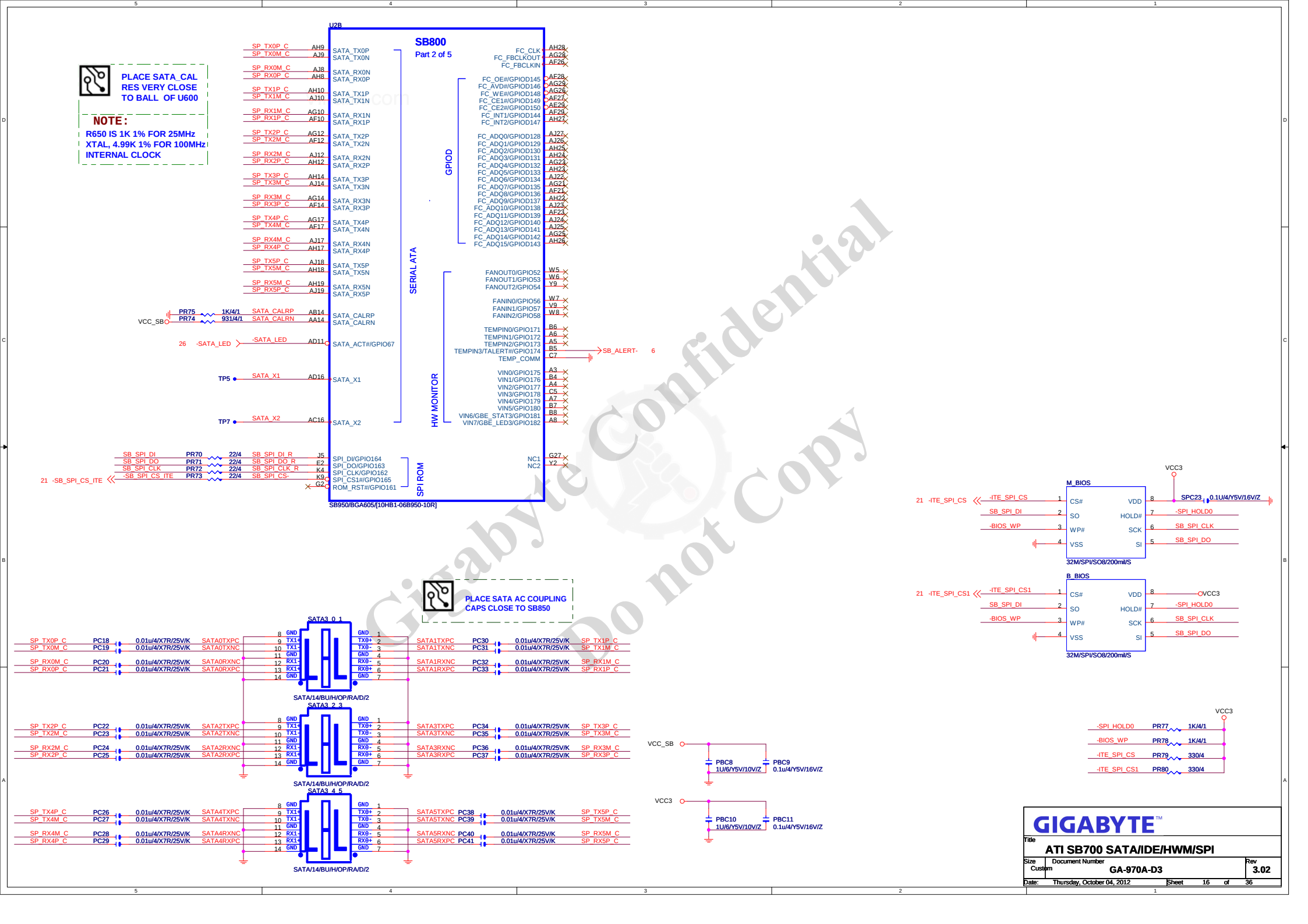
Title: RTM880N-793

Size: Custom | Document Number: GA-970A-D3 | Rev: 3.02

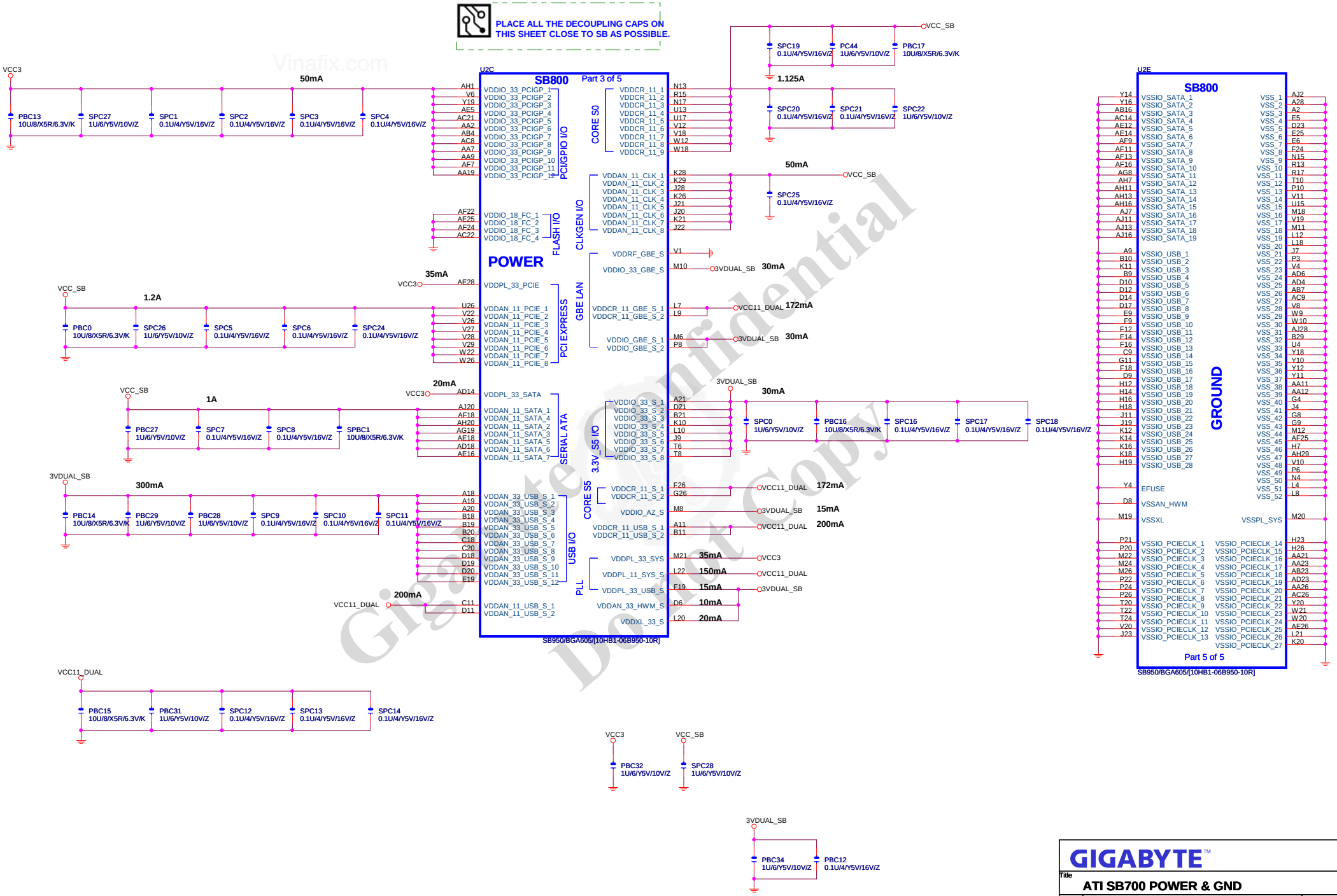
Date: Thursday, October 04, 2012 | Sheet 13 of 36

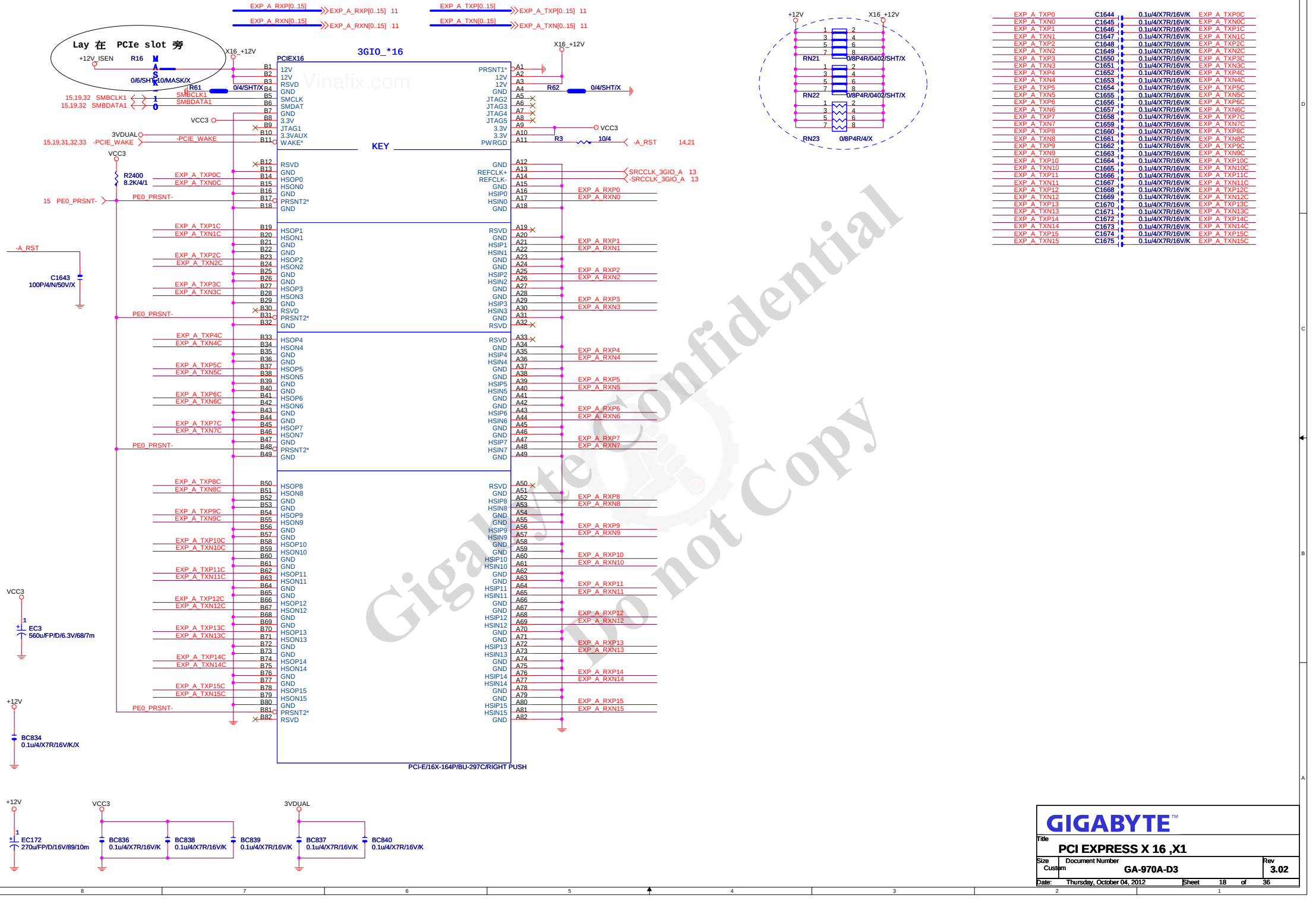

S.B HEATSINK
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850
SB800 Part 1 of 5
PCI EXPRESS INTERFACES
PCI INTERFACE
PCI CLKS
CLOCK GENERATOR
LPC
CPU
RTC
SB950/BGA605/[10HB1-06B950-10R]
SB_HS
SB_HS/[12SP2-S05110-01R_12SP2-S05110-02R_12SP2-S05110-03R]
PX1
32.768K/12.5p/20ppm/TF38/35K/D
PC13 18P/4/NPO/50V/J
PC14 18P/4/NPO/50V/J
PR6 20M/4
RTC_XI
RTC_XO
PX2
25M/20p/30ppm/49US/20/D
PC15 22P/4/NPO/50V/J
PC16 22P/4/NPO/50V/J
PR7 1M/4
SHW/D0.64*5.08*6.74
PCLK1 PR14 8.2K/4
Low: Force PCIE GEN1, Up: Allow PCIE GEN2
PCLK2 PR18 8.2K/4
PCLK3 PR92 8.2K/4
PCLK2 PCLK3
PULL HIGH WATCHDOG TIMER ON NB_PWRGD ENABLED USE DEBUG STRAPS
PULL LOW WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT IGNORE DEBUG STRAPS DEFAULT
PCLK4 PR17 8.2K/4 PR16 22p/4/NPO/50V/J
EMI ISSUE
BIOS after boot setting
EC AOD-ACC
LPC_CLK0 PR20 8.2K/4
LPC_CLK1 PR22 8.2K/4
LPC_CLK0 Rev.A12 LPC_CLK1
PULL HIGH IMC ENABLED CLKGEN ENABLED
AOD Extreme
PULL LOW IMC DISABLED CLKGEN DISABLED
DEFAULT DEFAULT
20mil 20mil
PQ1 BAT54C/SOT23/200mA
PR28 1K/4/1
PBC24 0.1U/6/X7R/25V/K
PBC25 1U/6/Y5V/10V/Z
20mil
BAT BAT-SK/BK/P/S/D/SN
CR2032 BAT CR2032
CLR_CMOS PH/1*2/BK/2.54/VA/D
CLR_CMOS
SHORT CLEAR CMOS
OPEN NORMAL
NOT ADD ICT FOR RTCVDD PIN
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.
PR24 8.2K/4
PR25 22/4
PR26 22/4
PR27 100K/4/X
PR90 8.2K/4/X
PR94 8.2K/4/X
PBC2 0.1U/6/X7R/25V/K
GIGABYTE
Title ATI SB700 PCIE/PCI/CPU/LPC
Size Custom Document Number GA-970A-D3 Rev 3.02
Date: Thursday, October 04, 2012 Sheet 14 of 36
Gigabyte Confidential
Dept Copy

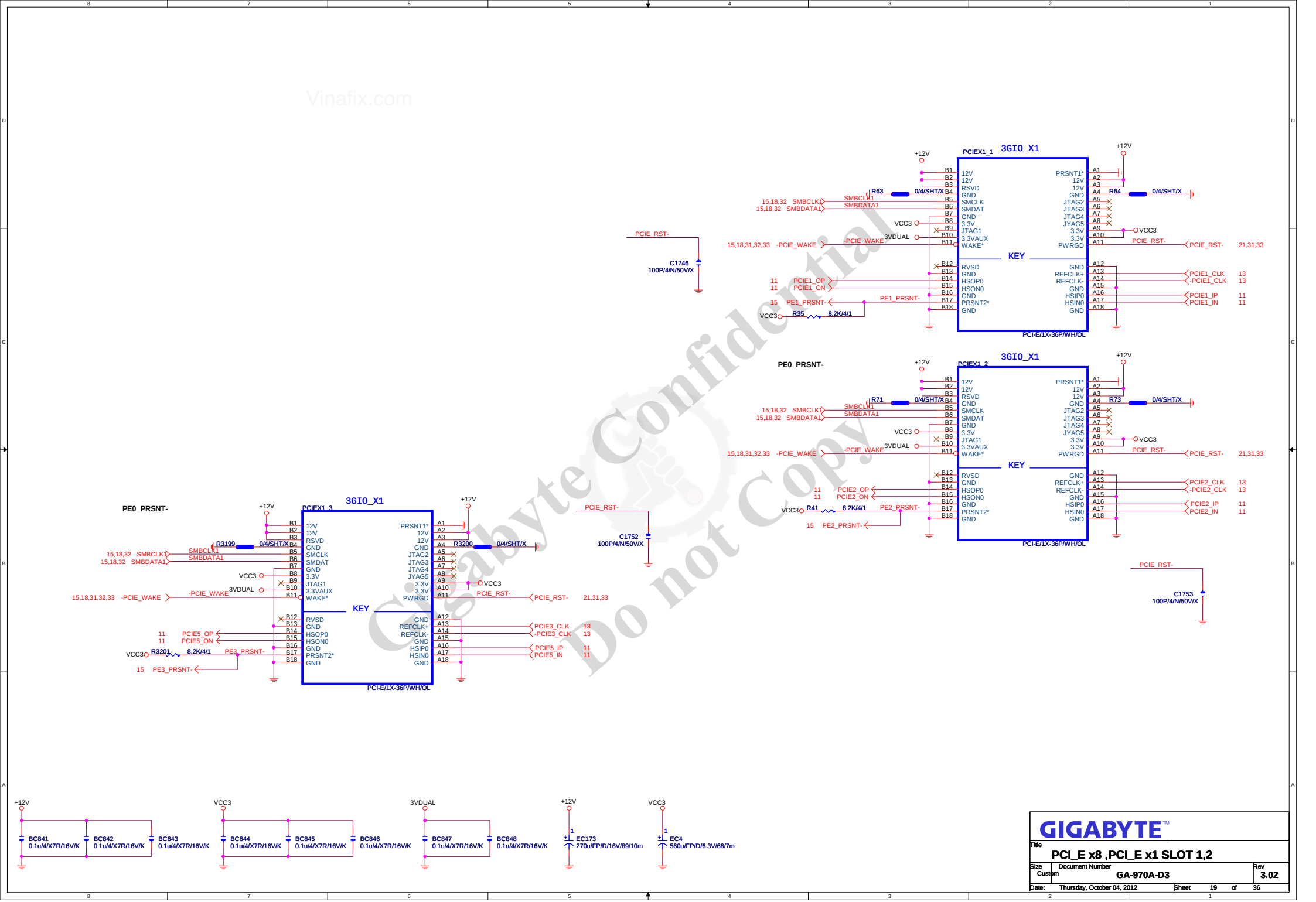

SB800
Part 4 of 5
SB950/BGA605/[10HB1-06B950-10R]
ACPI / WAKE UP EVENTS
USB 1.1 USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
EMBEDDED CTRL
Low: Performance Mode(D), Up: Low Power Mode.
Low: Disable PCI MEM boot(D), Up: Enable PCI MEM boot
IMC_GPIO200 IMC_GPIO199
ROM TYPE:
H, H = Reserved
H, L = SPI ROM DEFAULT
L, H = LPC ROM
L, L = FWH ROM
GIGABYTE
ATI SB700 ACPI/USB/GPIO/AUDIO
GA-970A-D3
3.02
Thursday, October 04, 2012
Sheet 15 of 36



Title	ATI SB700 SATA/IDE/HWM/SPI
Size	Custom
Document Number	GA-970A-D3
Rev	3.02
Date:	Thursday, October 04, 2012
Sheet	16 of 36


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
SB800
Part 3 of 5
POWER
GROUND
Part 5 of 5
SB950/BGA605/[10HB1-06B950-10R]
CORE S0
PCI/GPIO I/O
FLASH I/O
CLKGEN I/O
GBE LAN
PCI EXPRESS
SERIAL ATA
3.3V_S5 I/O
CORE S5
USB I/O
PLL
50mA
1.125A
1.2A
35mA
20mA
1A
300mA
200mA
30mA
172mA
15mA
150mA
10mA
Gigabyte Confidential
Don't Copy
GIGABYTE
ATI SB700 POWER & GND
GA-970A-D3
3.02
Thursday, October 04, 2012
17 of 36

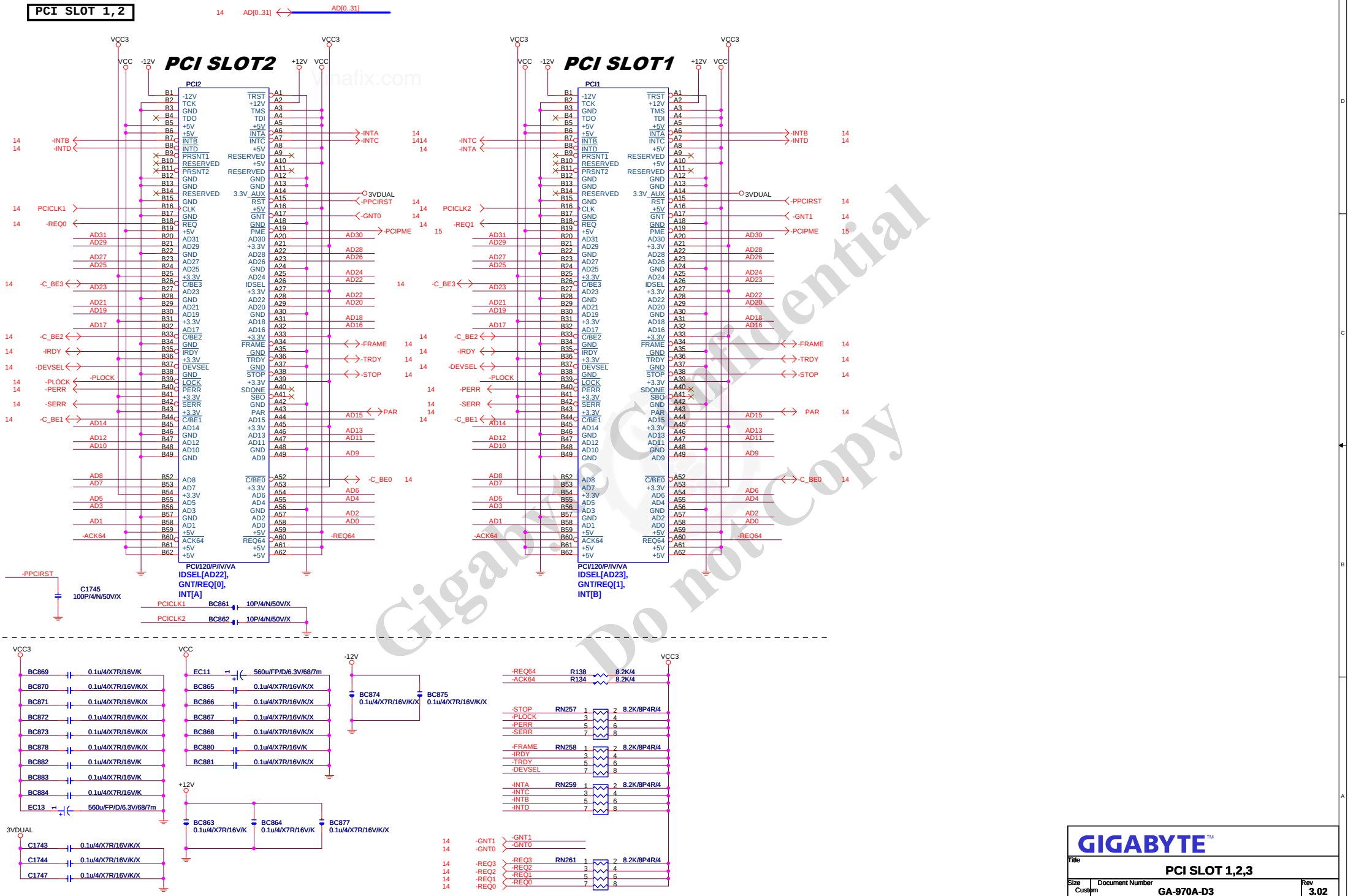

Lay 在 PCIe slot 旁
PCIEX16
3GIO_*16
KEY
PCI-E/16X-164P/BU-297C/RIGHT PUSH
Gigabyte Confidential
Do not Copy
GIGABYTE
PCI EXPRESS X 16 ,X1
GA-970A-D3
3.02
Thursday, October 04, 2012



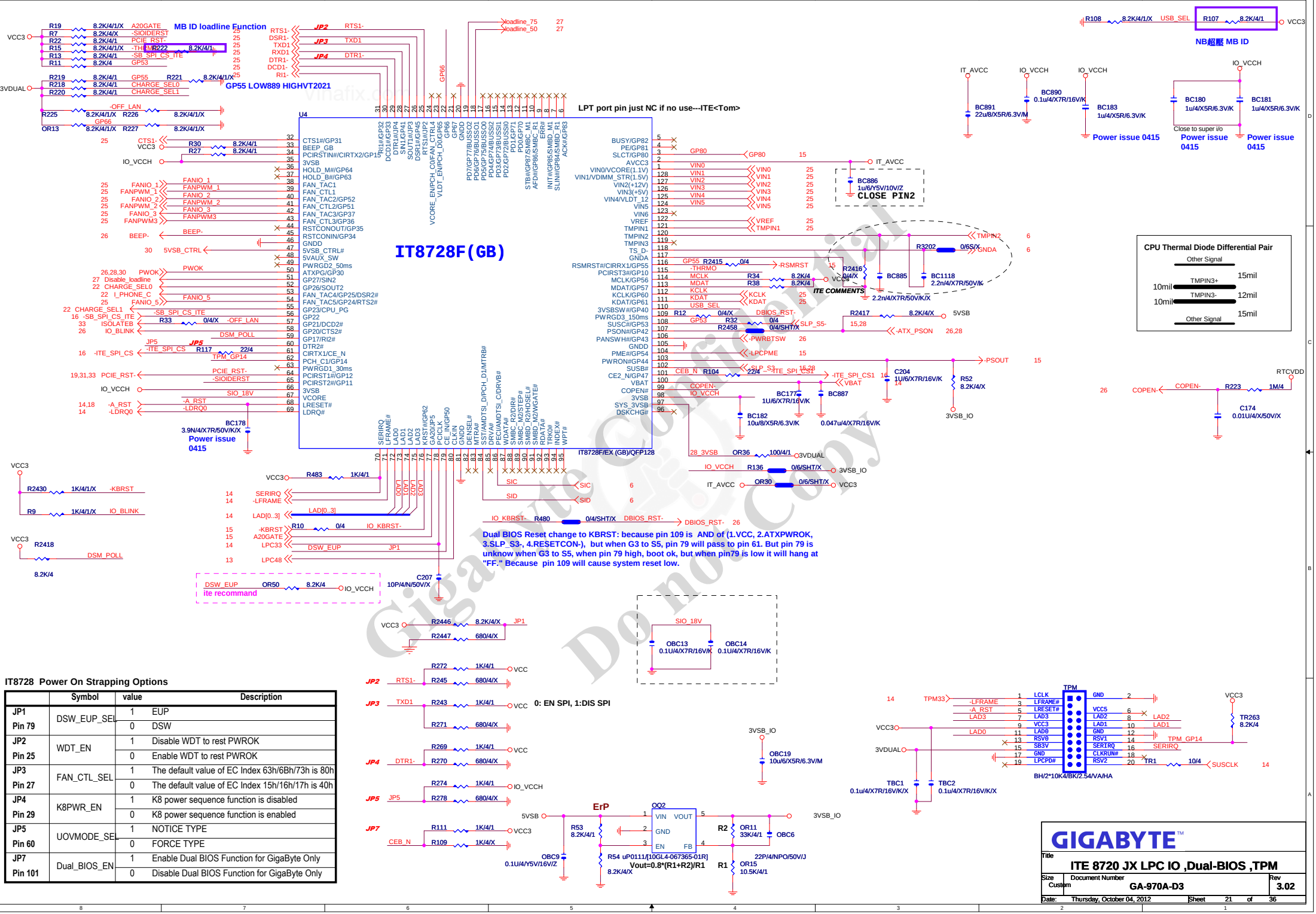
GIGABYTE™

Title	PCI_E x8 ,PCI_E x1 SLOT 1,2	
Size: Custom	Document Number: GA-970A-D3	Rev: 3.02
Date: Thursday, October 04, 2012	Sheet 19 of 36	

PCI SLOT 1,2

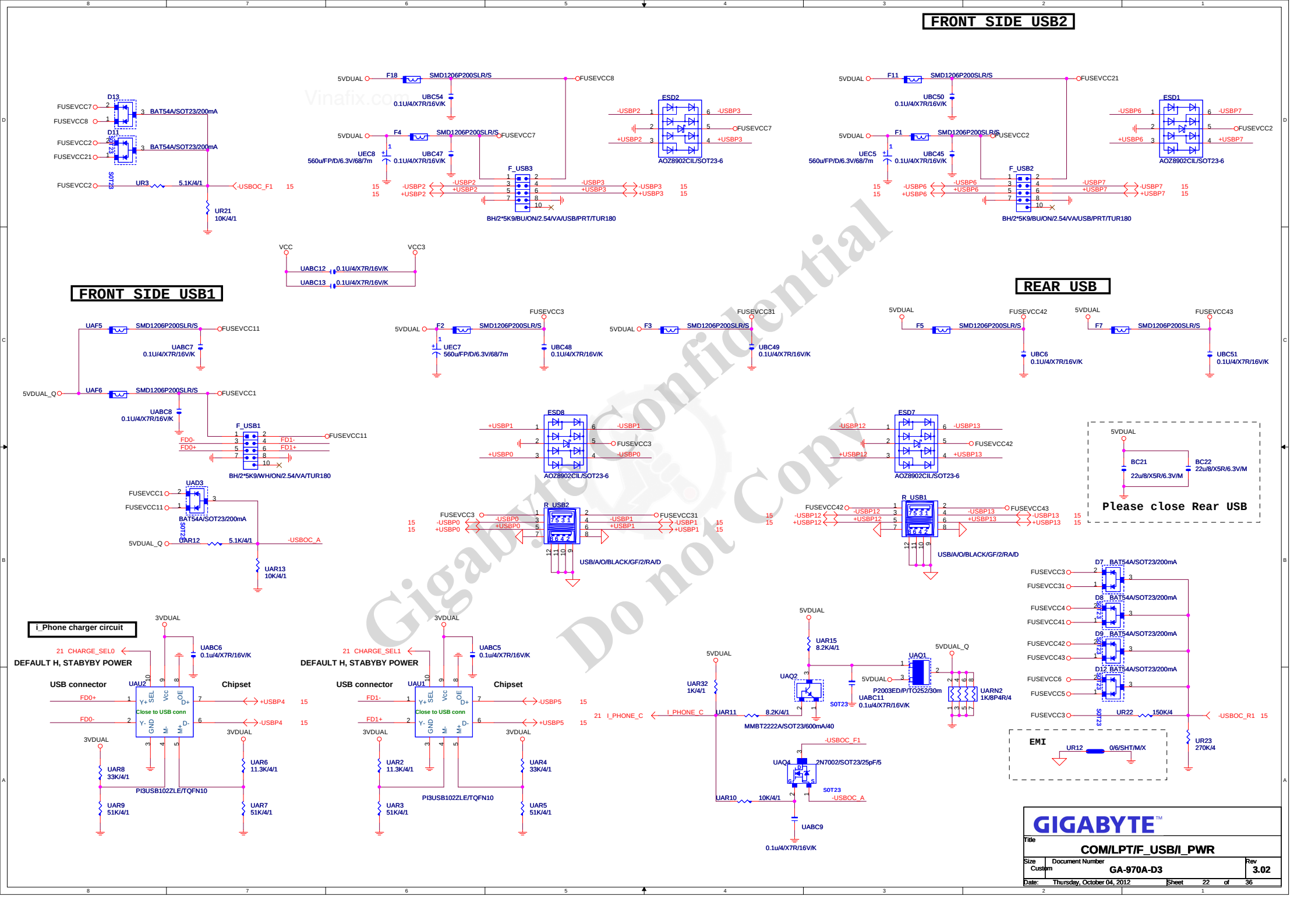


GIGABYTE			
Title	PCI SLOT 1,2,3		
Size: Custom	Document Number: GA-970A-D3	Rev: 3.02	
Date: Thursday, October 04, 2012	Sheet 20 of 36		



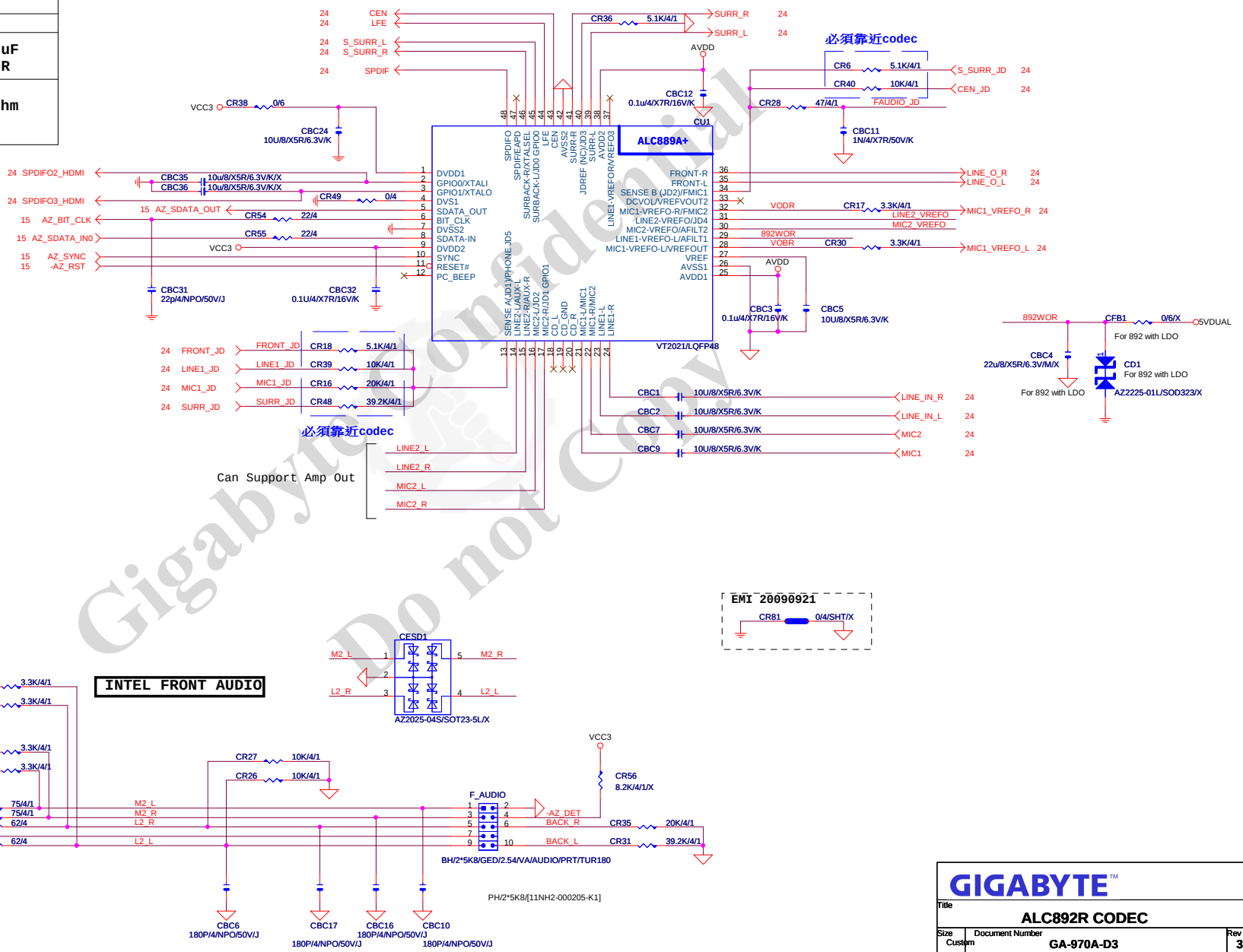
IT8728 Power On Strapping Options

	Symbol	value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin 79		0	DSW
JP2	WDT_EN	1	Disable WDT to rest PWROK
Pin 25		0	Enable WDT to rest PWROK
JP3	FAN_CTL_SEL	1	The default value of EC Index 63h/6Bh/73h is 80h
Pin 27		0	The default value of EC Index 15h/16h/17h is 40h
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 29		0	K8 power sequence function is enabled
JP5	UOVMODE_SEL	1	NOTICE TYPE
Pin 60		0	FORCE TYPE
JP7	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
Pin 101		0	Disable Dual BIOS Function for GigaByte Only

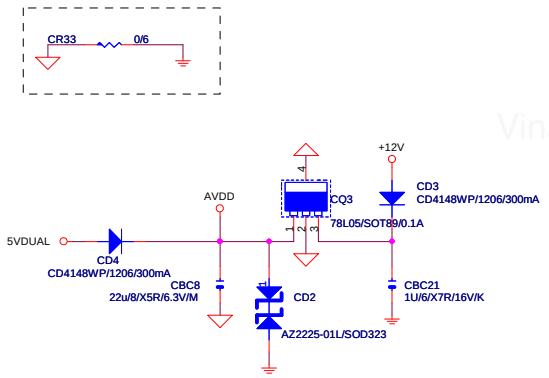

FRONT SIDE USB2
FRONT SIDE USB1
REAR USB
i_Phone charger circuit
DEFAULT H, STABYBY POWER
USB connector
Chipset
Close to USB conn
PI3USB102ZLE/TQFN10
BH/2*5K9/BU/ON/2.54/VA/USB/PRT/TUR180
BH/2*5K9/WH/ON/2.54/VA/TUR180
AOZ8902CIL/SOT23-6
USB/A/O/BLACK/GF/2/RA/D
P2003ED/P/TO252/30m
MMBT2222A/SOT23/600mA/40
2N7002/SOT23/25pF/5
Please close Rear USB
EMI
GIGABYTE
COM/LPT/F_USB/I_PWR
GA-970A-D3
3.02
Thursday, October 04, 2012
Sheet 22 of 36
Gigabyte Confidential
Do not Copy

AZALIA CODEC *ALC892/ALC889/ Colay*

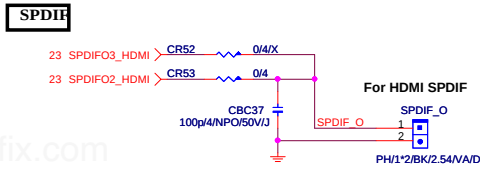
	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm

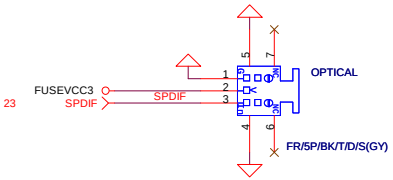


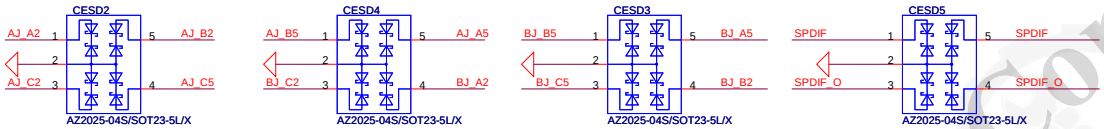
Title	ALC892R CODEC
Size	Custom
Document Number	GA-970A-D3
Rev	3.02
Date:	Thursday, October 04, 2012
Sheet	23 of 36

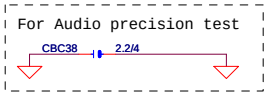


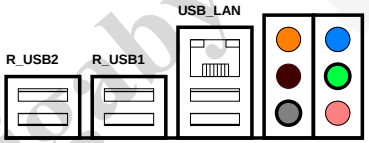
For ESD PROTECT DIODE

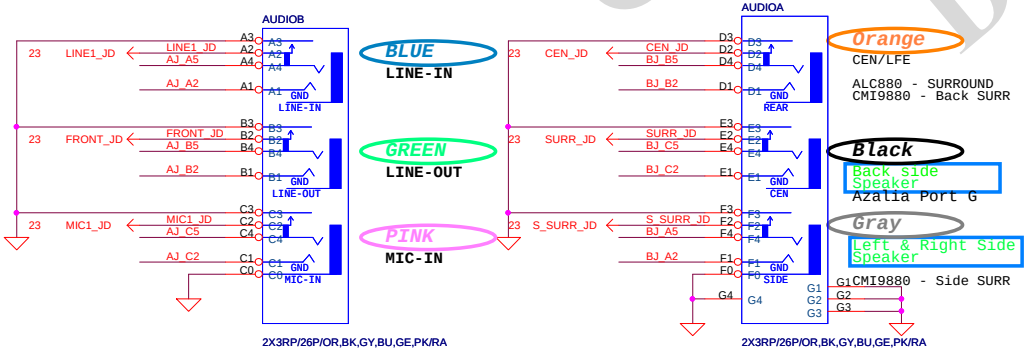








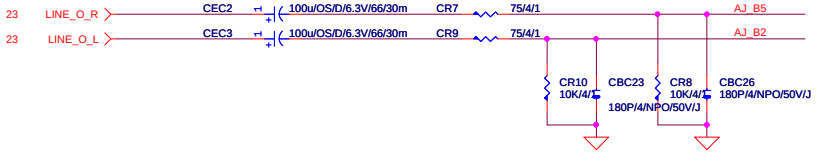




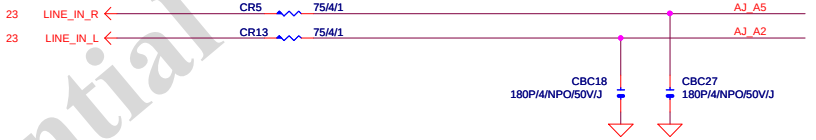
A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ+15F/[11NR6-403004-11]

A3RJ/13P/OBG/[11NR6-403006-71]
3RJ+15F/[11NR6-403004-31]

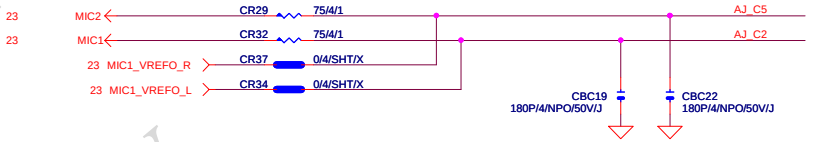
LINE OUT FRONT OUT



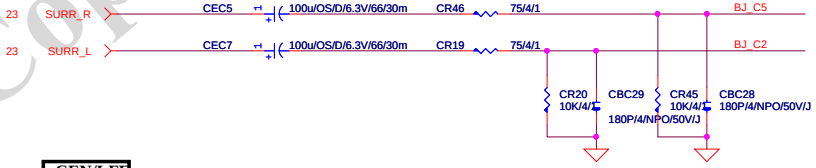
LINE-IN



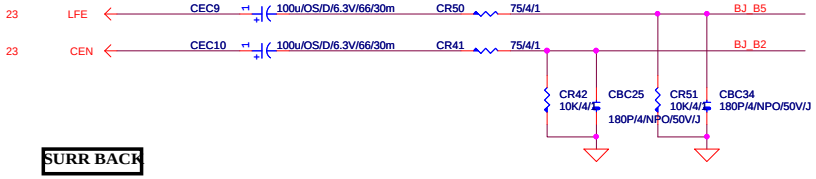
MIC



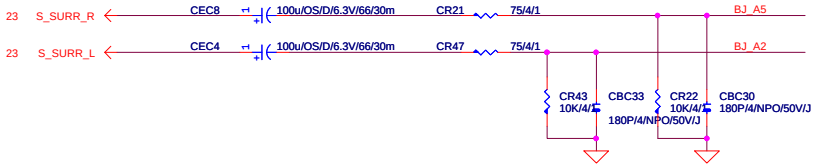
SURROUND



CEN/LFE



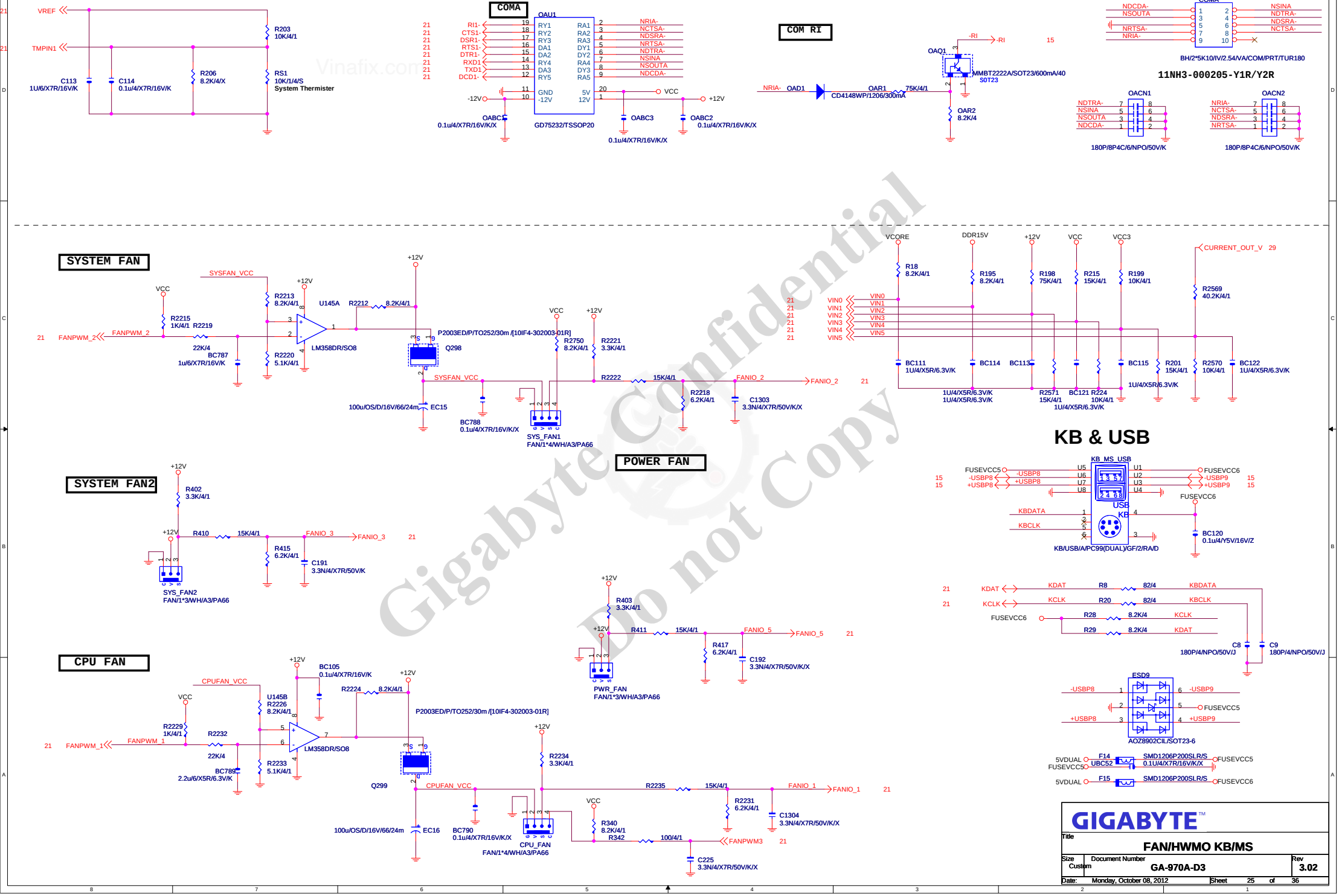
SURR BACK

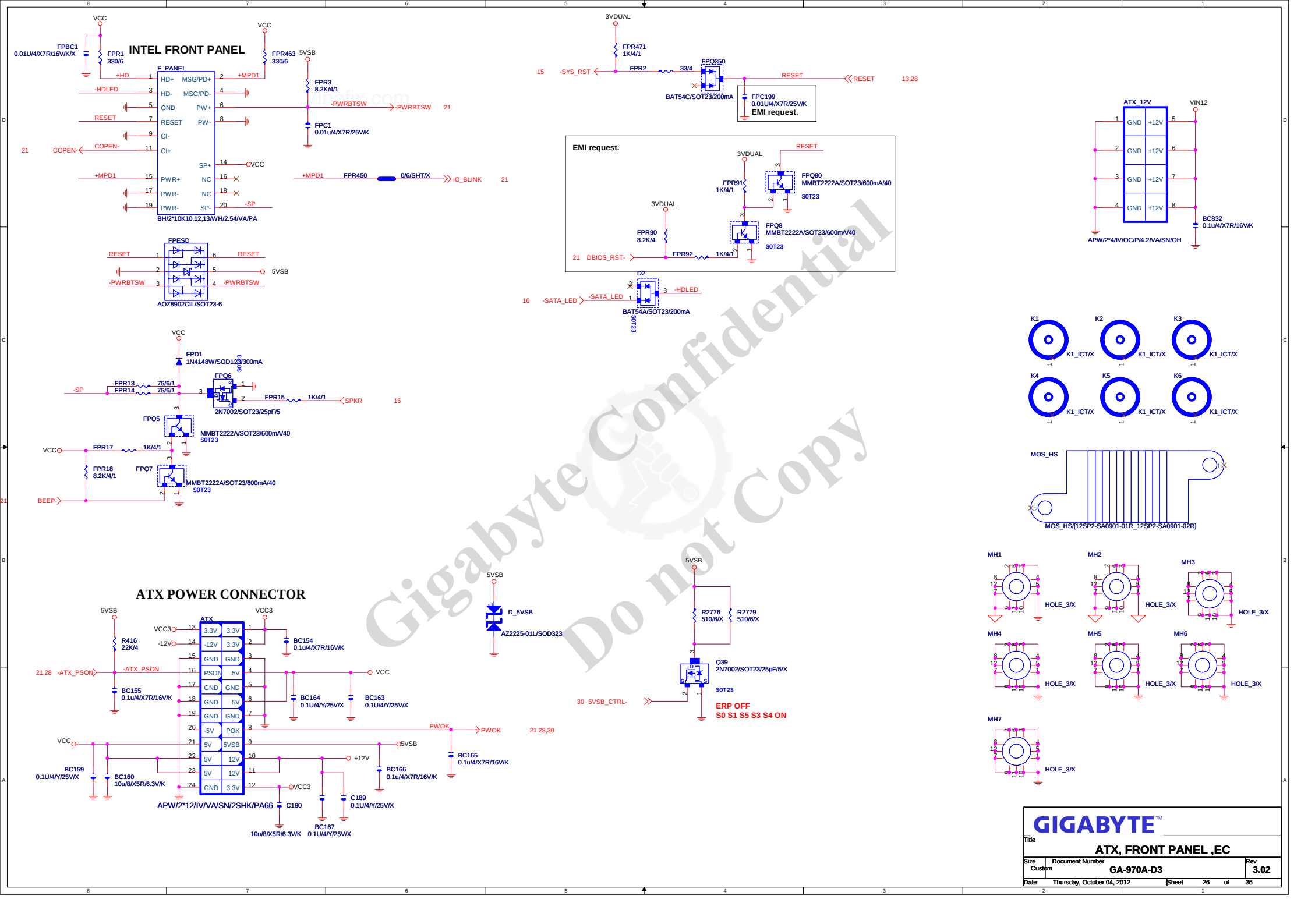


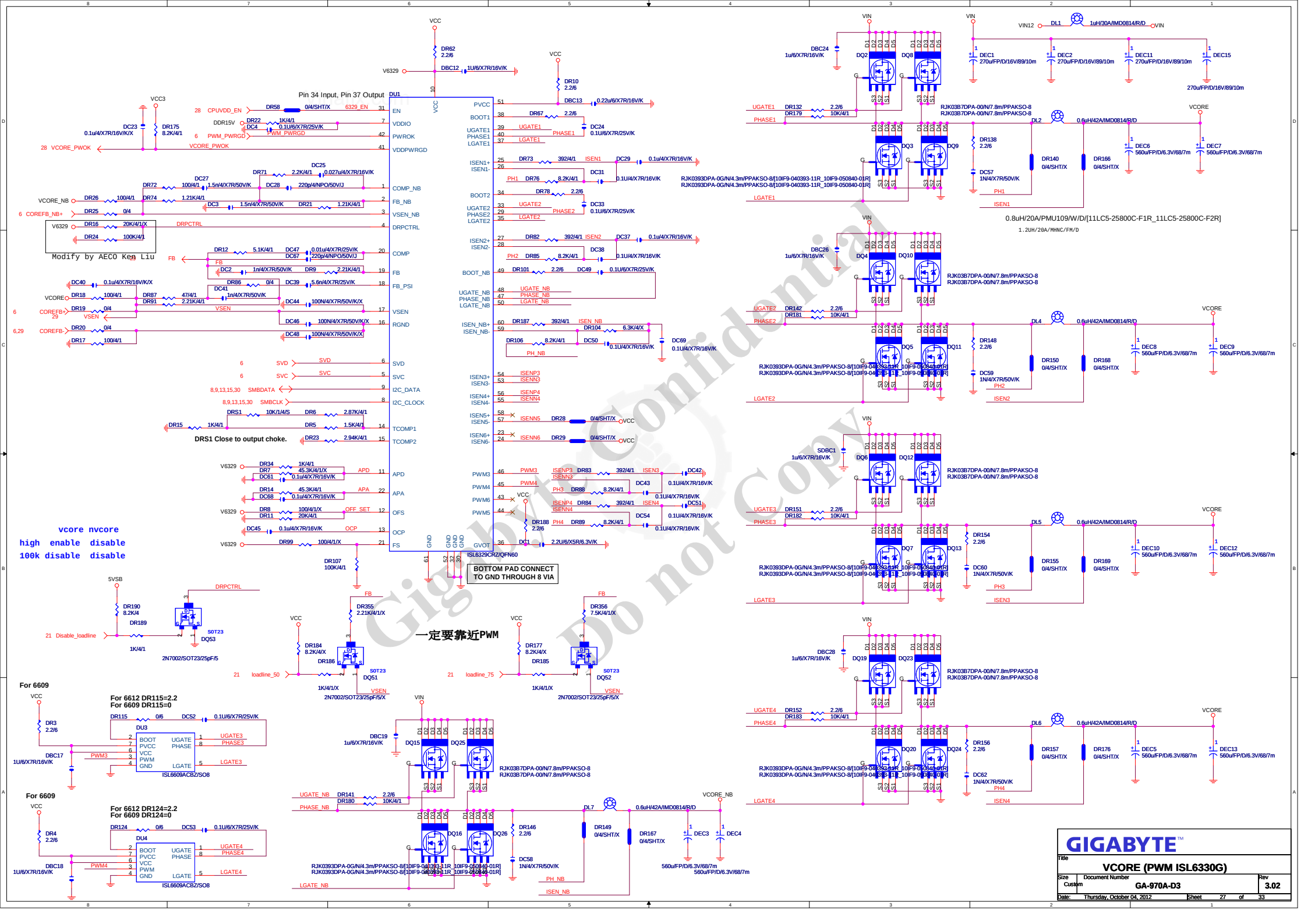
GIGABYTE™

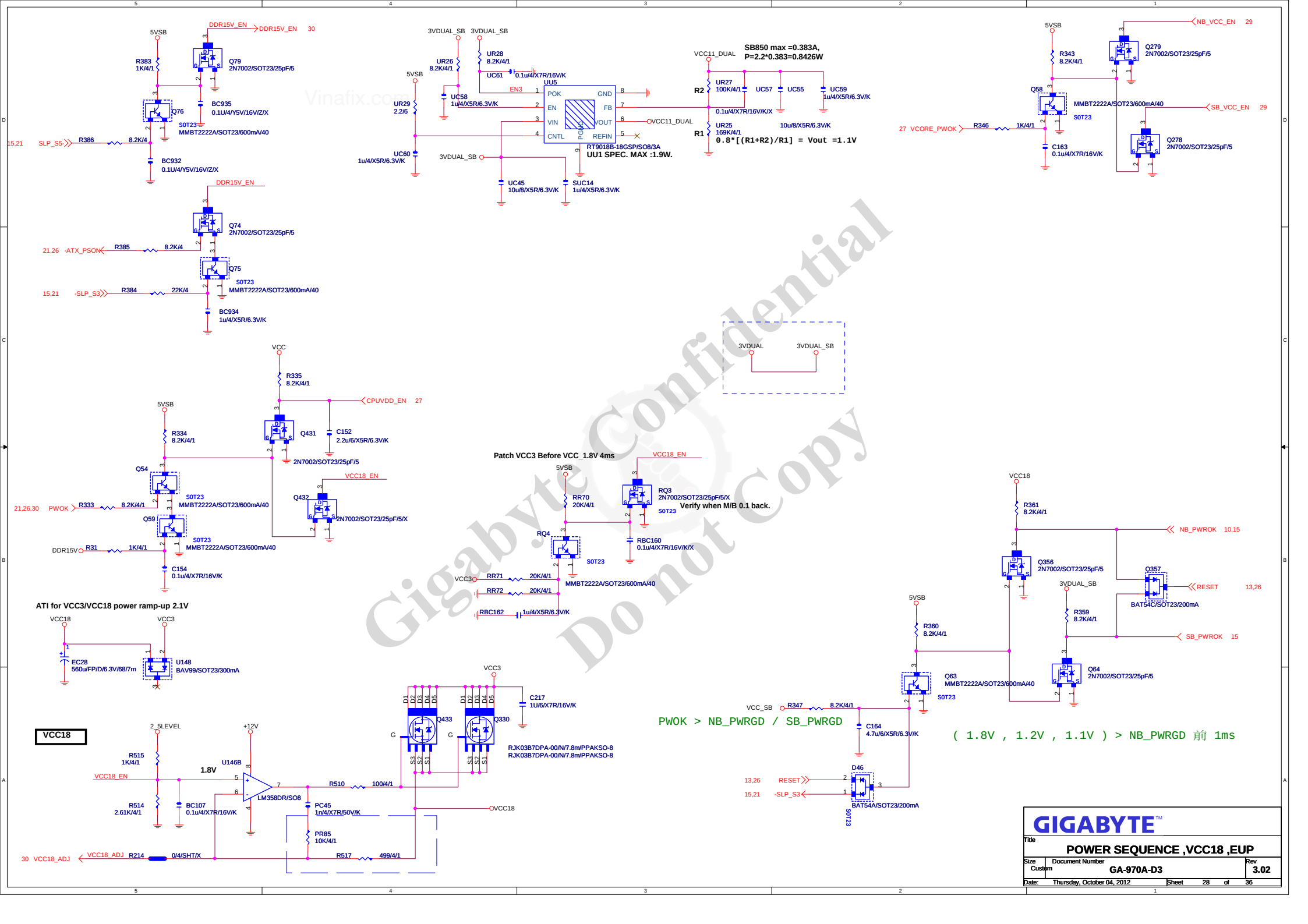
Title: AUDIO JACK		
Size: Custom	Document Number: GA-970A-D3	Rev: 3.02
Date: Thursday, October 04, 2012	Sheet 24 of 36	

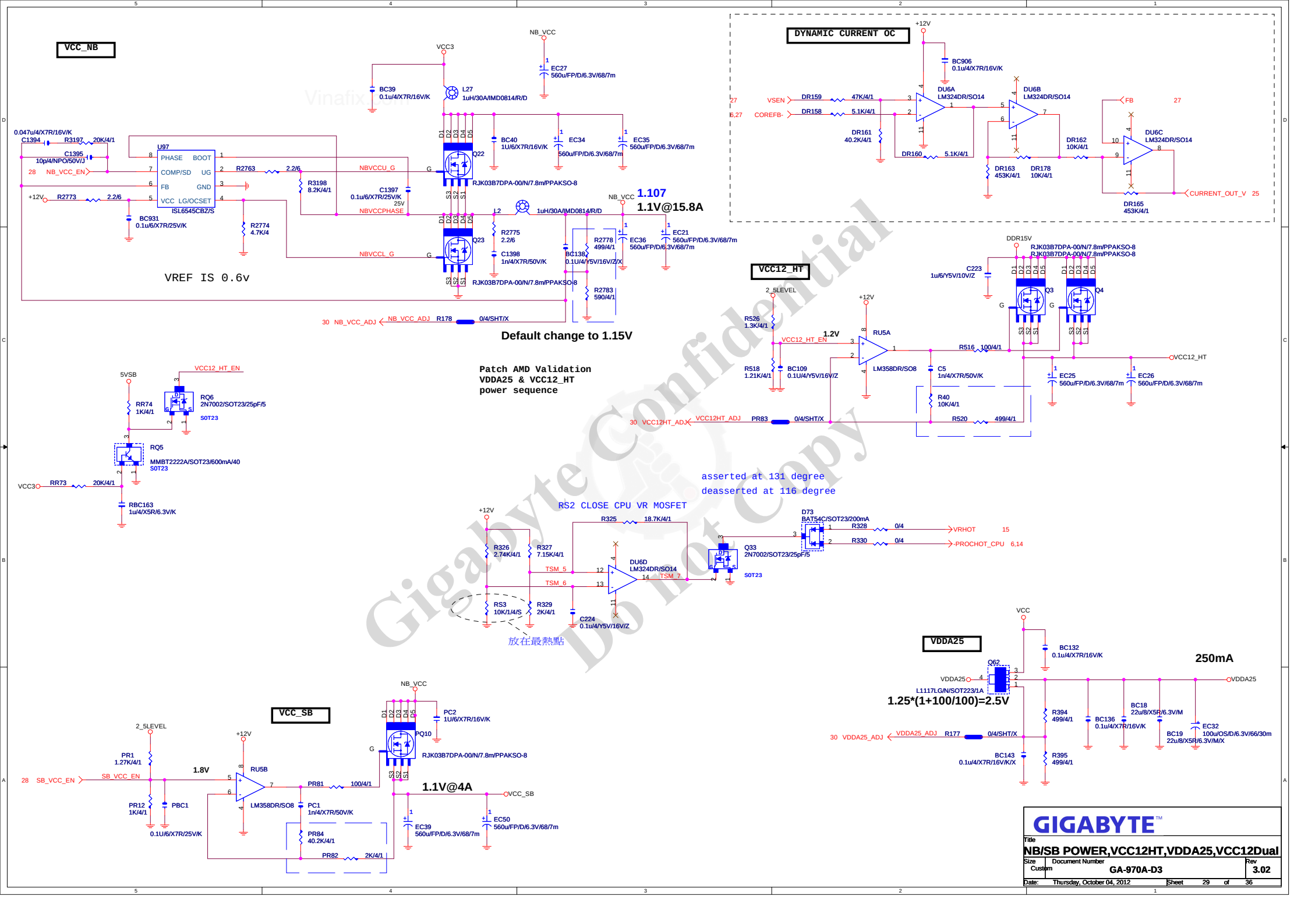
Hardware Monitor circuits

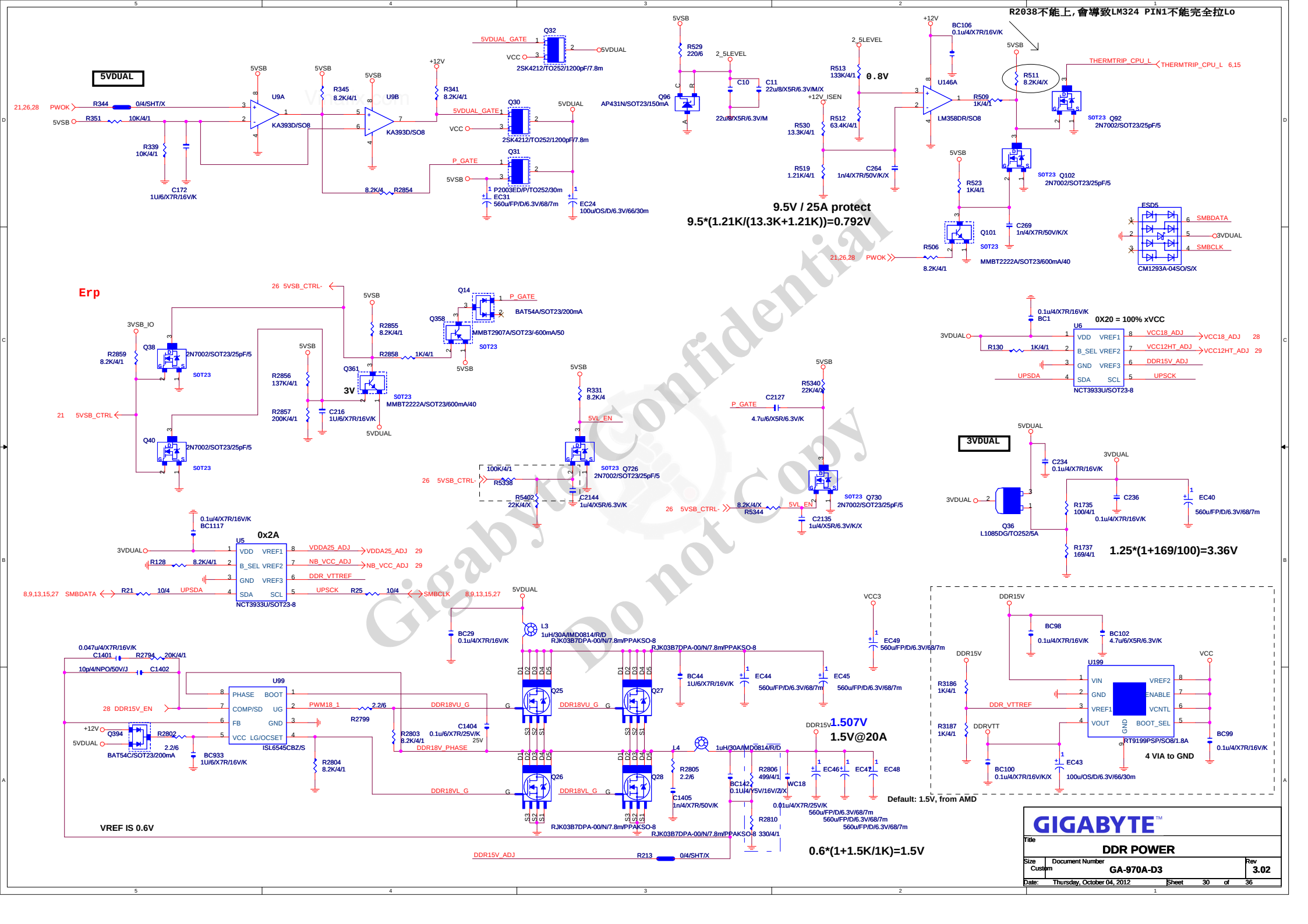


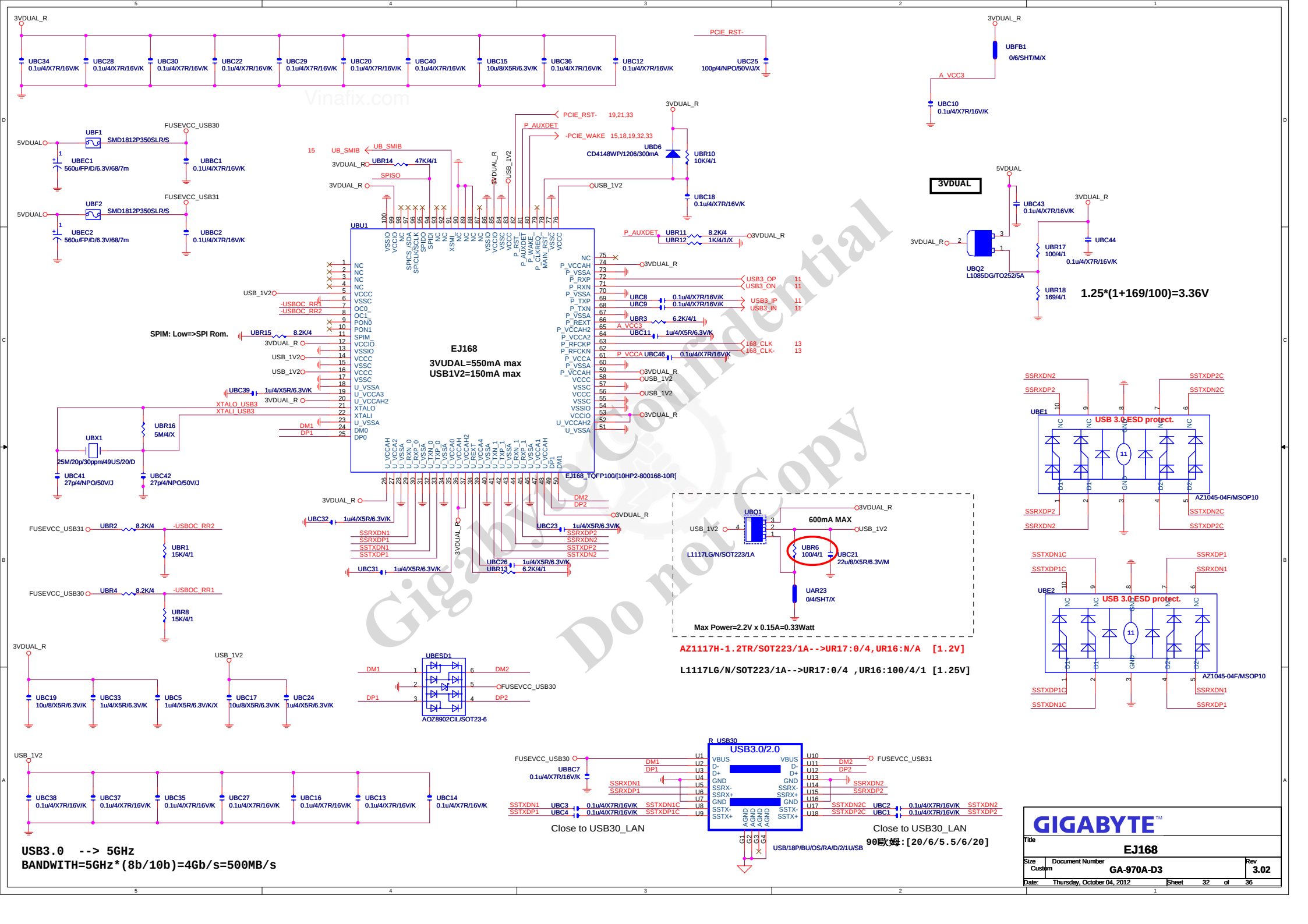


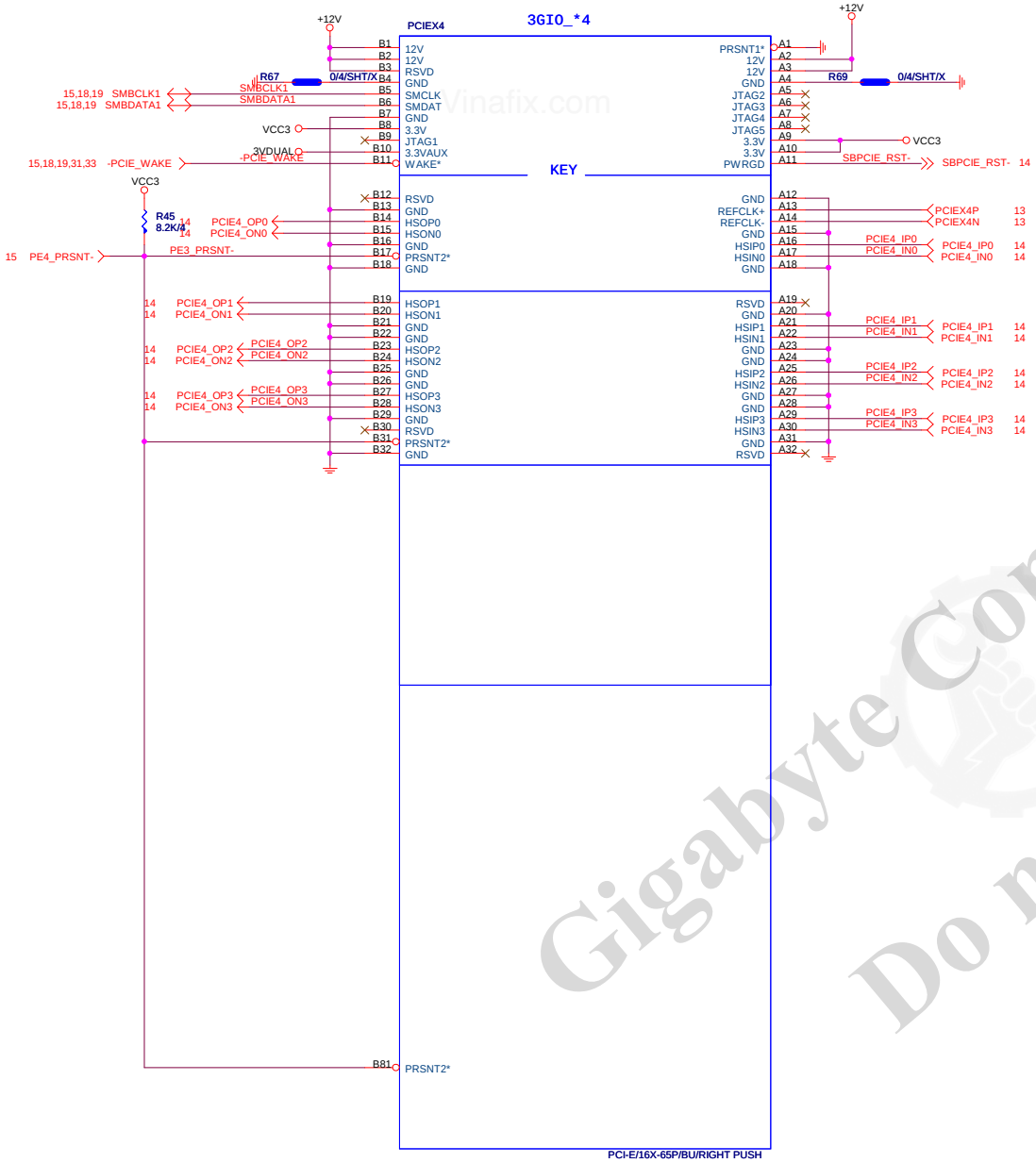



5VSB
DDR15V_EN
DDR15V_EN 30
R383 1K/4/1
Q79 2N7002/SOT23/25pF/5
BC935 0.1U/4/Y5V/16V/Z/X
Q76
S0T23
MMBT2222A/SOT23/600mA/40
15,21 SLP_S5
R386 8.2K/4
BC932 0.1U/4/Y5V/16V/Z/X
3VDUAL_SB
UR26 8.2K/4/1
UR28 8.2K/4/1
UC61 0.1u/4/X7R/16V/K
UU5
POK
EN
VIN
CNTL
GND
FB
VOUT
REFIN
PGND
EN3
UR29 2.2/6
UC58 1u/4/X5R/6.3V/K
UC60 1u/4/X5R/6.3V/K
UC45 10u/8/X5R/6.3V/K
SUC14 1u/4/X5R/6.3V/K
RT9018B-18GSP/SO8/3A
UU1 SPEC. MAX :1.9W.
VCC11_DUAL
R2
R1
UR27 100K/4/1
UR25 169K/4/1
UC57
UC55
UC59 1u/4/X5R/6.3V/K
10u/8/X5R/6.3V/K
0.1u/4/X7R/16V/K/X
SB850 max =0.383A,
P=2.2*0.383=0.8426W
0.8*[(R1+R2)/R1] = Vout =1.1V
NB_VCC_EN 29
R343 8.2K/4/1
Q279 2N7002/SOT23/25pF/5
Q58
MMBT2222A/SOT23/600mA/40
SB_VCC_EN 29
Q278 2N7002/SOT23/25pF/5
27 VCORE_PWOK
R346 1K/4/1
C163 0.1u/4/X7R/16V/K
DDR15V_EN
Q74 2N7002/SOT23/25pF/5
21,26 -ATX_PSON
R385 8.2K/4
Q75
15,21 -SLP_S3
R384 22K/4
BC934 1u/4/X5R/6.3V/K
3VDUAL
3VDUAL_SB
VCC
R335 8.2K/4/1
CPUVDD_EN 27
Q431 2N7002/SOT23/25pF/5
C152 2.2u/6/X5R/6.3V/K
R334 8.2K/4/1
Q54
21,26,30 PWOK
R333 8.2K/4/1
Q59
DDR15V
R31 1K/4/1
C154 0.1u/4/X7R/16V/K
VCC18_EN
Q432 2N7002/SOT23/25pF/5/X
Patch VCC3 Before VCC_1.8V 4ms
RR70 20K/4/1
RQ3 2N7002/SOT23/25pF/5/X
Verify when M/B 0.1 back.
RQ4
RBC160 0.1u/4/X7R/16V/K/X
VCC3
RR71 20K/4/1
RR72 20K/4/1
RBC162 1u/4/X5R/6.3V/K
MMBT2222A/SOT23/600mA/40
ATI for VCC3/VCC18 power ramp-up 2.1V
EC28 560u/FP/D/6.3V/68/7m
U148 BAV99/SOT23/300mA
VCC18
2_5LEVEL
+12V
R515 1K/4/1
U146B
1.8V
LM358DR/SO8
R514 2.61K/4/1
BC107 0.1u/4/X7R/16V/K
R510 100/4/1
PC45 1n/4/X7R/50V/K
PR85 10K/4/1
R517 499/4/1
30 VCC18_ADJ
R214 0/4/SHT/X
Q433
Q330
RJK03B7DPA-00/N/7.8m/PPAKSO-8
RJK03B7DPA-00/N/7.8m/PPAKSO-8
C217 1U/6/X7R/16V/K
R361 8.2K/4/1
NB_PWROK 10,15
Q356 2N7002/SOT23/25pF/5
Q357
BAT54C/SOT23/200mA
RESET 13,26
R359 8.2K/4/1
SB_PWROK 15
Q64 2N7002/SOT23/25pF/5
R360 8.2K/4/1
Q63 MMBT2222A/SOT23/600mA/40
VCC_SB
R347 8.2K/4/1
C164 4.7u/6/X5R/6.3V/K
PWOK > NB_PWRGD / SB_PWRGD
(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms
D46
13,26 RESET
15,21 -SLP_S3
BAT54A/SOT23/200mA
Gigabyte Confidential
Do not Copy
GIGABYTE
Title
POWER SEQUENCE ,VCC18 ,EUP
Size Custom
Document Number GA-970A-D3
Rev 3.02
Date: Thursday, October 04, 2012
Sheet 28 of 36


VCC_NB
VCC3
NB_VCC
BC39 0.1u/4/X7R/16V/K
L27 1uH/30A/IMD0814/R/D
EC27 560u/FP/D/6.3V/68/7m
0.047u/4/X7R/16V/K
C1394
R3197 20K/4/1
C1395 10p/4/NPO/50V/J
28 NB_VCC_EN
+12V
R2773 2.2/6
BC931 0.1u/6/X7R/25V/K
U97
PHASE BOOT
COMP/SD UG
FB GND
VCC LG/OCSET
ISL6545CBZ/S
R2763 2.2/6
R3198 8.2K/4/1
R2774 4.7K/4
NBVCCU_G
NBVCCPHASE
NBVCCL_G
C1397 0.1u/6/X7R/25V/K 25V
Q22
Q23
RJK03B7DPA-00/N/7.8m/PPAKSO-8
BC40 1U/6/X7R/16V/K
EC34 560u/FP/D/6.3V/68/7m
EC35 560u/FP/D/6.3V/68/7m
L2 1uH/30A/IMD0814/R/D
R2775 2.2/6
C1398 1n/4/X7R/50V/K
BC138 0.1U/4/Y5V/16V/Z/X
R2778 499/4/1
R2783 590/4/1
EC36 560u/FP/D/6.3V/68/7m
EC21 560u/FP/D/6.3V/68/7m
1.107
1.1V@15.8A
VREF IS 0.6v
30 NB_VCC_ADJ
NB_VCC_ADJ
R178
0/4/SHT/X
Default change to 1.15V
DYNAMIC CURRENT OC
+12V
BC906 0.1u/4/X7R/16V/K
DU6A LM324DR/SO14
DU6B LM324DR/SO14
DU6C LM324DR/SO14
27 VSEN
6,27 COREFB-
DR159 47K/4/1
DR158 5.1K/4/1
DR161 40.2K/4/1
DR160 5.1K/4/1
DR162 10K/4/1
DR163 453K/4/1
DR178 10K/4/1
FB 27
CURRENT_OUT_V 25
DR165 453K/4/1
Patch AMD Validation
VDDA25 & VCC12_HT
power sequence
VCC12_HT
DDR15V
2_5LEVEL
+12V
RJK03B7DPA-00/N/7.8m/PPAKSO-8
RJK03B7DPA-00/N/7.8m/PPAKSO-8
C223 1u/6/Y5V/10V/Z
Q3
Q4
R526 1.3K/4/1
VCC12_HT_EN
1.2V
RU5A
LM358DR/SO8
R518 1.21K/4/1
BC109 0.1U/4/Y5V/16V/Z
R516 100/4/1
C5 1n/4/X7R/50V/K
R40 10K/4/1
R520 499/4/1
EC25 560u/FP/D/6.3V/68/7m
EC26 560u/FP/D/6.3V/68/7m
VCC12_HT
30 VCC12HT_ADJ
VCC12HT_ADJ
PR83
0/4/SHT/X
5VSB
VCC12_HT_EN
RR74 1K/4/1
RQ6 2N7002/SOT23/25pF/5
SOT23
RQ5
MMBT2222A/SOT23/600mA/40
S0T23
VCC3
RR73 20K/4/1
RBC163 1u/4/X5R/6.3V/K
asserted at 131 degree
deasserted at 116 degree
RS2 CLOSE CPU VR MOSFET
+12V
R325 18.7K/4/1
R326 2.74K/4/1
R327 7.15K/4/1
TSM_5
TSM_6
TSM_7
DU6D LM324DR/SO14
RS3 10K/1/4/S
R329 2K/4/1
C224 0.1u/4/Y5V/16V/Z
放在最熱點
D73 BAT54C/SOT23/200mA
Q33 2N7002/SOT23/25pF/5
R328 0/4
R330 0/4
VRHOT 15
PROCHOT_CPU 6,14
VCC_SB
NB_VCC
2_5LEVEL
+12V
PR1 1.27K/4/1
PR12 1K/4/1
PBC1
0.1U/6/X7R/25V/K
1.8V
RU5B
LM358DR/SO8
PC1 1n/4/X7R/50V/K
PR84 40.2K/4/1
PR82 2K/4/1
PR81 100/4/1
PC2 1U/6/X7R/16V/K
PQ10
RJK03B7DPA-00/N/7.8m/PPAKSO-8
28 SB_VCC_EN
SB_VCC_EN
1.1V@4A
VCC_SB
EC39 560u/FP/D/6.3V/68/7m
EC50 560u/FP/D/6.3V/68/7m
VDDA25
VCC
Q62
L1117LG/N/SOT223/1A
1.25*(1+100/100)=2.5V
BC132 0.1u/4/X7R/16V/K
250mA
VDDA25
30 VDDA25_ADJ
VDDA25_ADJ
R177
0/4/SHT/X
R394 499/4/1
R395 499/4/1
BC136 0.1u/4/X7R/16V/K
BC18 22u/8/X5R/6.3V/M
BC19 22u/8/X5R/6.3V/M/X
EC32 100u/OS/D/6.3V/66/30m
BC143 0.1u/4/X7R/16V/K/X
Gigabyte Confidential
Do not Copy
GIGABYTE
Title
NB/SB POWER,VCC12HT,VDDA25,VCC12Dual
Size Custom
Document Number GA-970A-D3
Rev 3.02
Date: Thursday, October 04, 2012
Sheet 29 of 36


R2038不能上,會導致LM324 PIN1不能完全拉Lo
5VDUAL
9.5V / 25A protect
9.5*(1.21K/(13.3K+1.21K))=0.792V
Erp
0x2A
0X20 = 100% xVCC
3VDUAL
1.25*(1+169/100)=3.36V
1.507V
1.5V@20A
VREF IS 0.6V
Default: 1.5V, from AMD
0.6*(1+1.5K/1K)=1.5V
4 VIA to GND
GIGABYTE
DDR POWER
GA-970A-D3
3.02
Thursday, October 04, 2012
Gigabyte Confidential
Do not Copy


3VDUAL_R
UBC34 0.1u/4/X7R/16V/K
UBC28 0.1u/4/X7R/16V/K
UBC30 0.1u/4/X7R/16V/K
UBC22 0.1u/4/X7R/16V/K
UBC29 0.1u/4/X7R/16V/K
UBC20 0.1u/4/X7R/16V/K
UBC40 0.1u/4/X7R/16V/K
UBC15 10u/8/X5R/6.3V/K
UBC36 0.1u/4/X7R/16V/K
UBC12 0.1u/4/X7R/16V/K
PCIE_RST-
UBC25 100p/4/NPO/50V/J/X
3VDUAL_R
UBFB1 0/6/SHT/M/X
A_VCC3
UBC10 0.1u/4/X7R/16V/K
5VDUAL
UBF1 SMD1812P350SLR/S
FUSEVCC_USB30
UBEC1 560u/FP/D/6.3V/68/7m
UBBC1 0.1U/4/X7R/16V/K
UBF2 SMD1812P350SLR/S
FUSEVCC_USB31
UBEC2 560u/FP/D/6.3V/68/7m
UBBC2 0.1U/4/X7R/16V/K
15
UB_SMIB
UBR14 47K/4/1
SPISO
PCIE_RST- 19,21,33
P_AUXDET
-PCIE_WAKE 15,18,19,32,33
UBD6 CD4148WP/1206/300mA
UBR10 10K/4/1
UBC18 0.1u/4/X7R/16V/K
USB_1V2
UBU1
EJ168
3VUDAL=550mA max
USB1V2=150mA max
EJ168_TQFP100/[10HP2-800168-10R]
SPIM: Low=>SPI Rom.
UBR15 8.2K/4
-USBOC_RR1
-USBOC_RR2
UBC39 1u/4/X5R/6.3V/K
XTALO_USB3
XTALI_USB3
UBR16 5M/4/X
UBX1 25M/20p/30ppm/49US/20/D
UBC41 27p/4/NPO/50V/J
UBC42 27p/4/NPO/50V/J
DM1
DP1
UBC32 1u/4/X5R/6.3V/K
UBC23 1u/4/X5R/6.3V/K
UBC31 1u/4/X5R/6.3V/K
UBC26 1u/4/X5R/6.3V/K
UBR13 6.2K/4/1
SSRXDN1
SSRXDP1
SSTXDN1
SSTXDP1
SSRXDN2
SSRXDP2
SSTXDN2
SSTXDP2
DM2
DP2
P_AUXDET
UBR11 8.2K/4
UBR12 1K/4/1/X
USB3_OP
USB3_ON
USB3_IP
USB3_IN
UBC8 0.1u/4/X7R/16V/K
UBC9 0.1u/4/X7R/16V/K
UBR3 6.2K/4/1
UBC11 1u/4/X5R/6.3V/K
168_CLK
168_CLK-
UBC46 0.1u/4/X7R/16V/K
FUSEVCC_USB31
UBR2 8.2K/4
UBR1 15K/4/1
FUSEVCC_USB30
UBR4 8.2K/4
UBR8 15K/4/1
UBESD1
AOZ8902CIL/SOT23-6
3VDUAL
UBC43 0.1u/4/X7R/16V/K
UBC44 0.1u/4/X7R/16V/K
UBR17 100/4/1
UBR18 169/4/1
UBQ2 L1085DG/TO252/5A
1.25*(1+169/100)=3.36V
UBQ1 L1117LG/N/SOT223/1A
600mA MAX
UBR6 100/4/1
UBC21 22u/8/X5R/6.3V/M
UAR23 0/4/SHT/X
Max Power=2.2V x 0.15A=0.33Watt
AZ1117H-1.2TR/SOT223/1A-->UR17:0/4,UR16:N/A [1.2V]
L1117LG/N/SOT223/1A-->UR17:0/4 ,UR16:100/4/1 [1.25V]
UBE1
USB 3.0 ESD protect.
AZ1045-04F/MSOP10
UBE2
USB 3.0 ESD protect.
AZ1045-04F/MSOP10
UBC19 10u/8/X5R/6.3V/K
UBC33 1u/4/X5R/6.3V/K
UBC5 1u/4/X5R/6.3V/K/X
UBC17 10u/8/X5R/6.3V/K
UBC24 1u/4/X5R/6.3V/K
UBC38 0.1u/4/X7R/16V/K
UBC37 0.1u/4/X7R/16V/K
UBC35 0.1u/4/X7R/16V/K
UBC27 0.1u/4/X7R/16V/K
UBC16 0.1u/4/X7R/16V/K
UBC13 0.1u/4/X7R/16V/K
UBC14 0.1u/4/X7R/16V/K
USB3.0 --> 5GHz
BANDWITH=5GHz*(8b/10b)=4Gb/s=500MB/s
R_USB30
USB3.0/2.0
UBBC7 0.1u/4/X7R/16V/K
UBC3 0.1u/4/X7R/16V/K
UBC4 0.1u/4/X7R/16V/K
SSTXDN1C
SSTXDP1C
SSTXDN2C
SSTXDP2C
UBC2 0.1u/4/X7R/16V/K
UBC1 0.1u/4/X7R/16V/K
Close to USB30_LAN
Close to USB30_LAN
90歐姆:[20/6/5.5/6/20]
USB/18P/BU/OS/RA/D/2/1U/SB
GIGABYTE
Title EJ168
Size Custom
Document Number GA-970A-D3
Rev 3.02
Date: Thursday, October 04, 2012
Sheet 32 of 36
Gigabyte Confidential
Do not Copy



GIGABYTE™

Title: JMB362		
Size: Custom	Document Number: GA-970A-D3	Rev: 3.02
Date: Thursday, October 04, 2012	Sheet 33 of 36	

PCIE-1G LAN

要用1% 的電阻,trace不能太長,建議在200 mil以內

LA_VDD33

LAR10 1K/4/1

LAR12 2.49K/4/1

RSET, VDD10, XTALI_P, XTALO_P, VDD10, LED_ACT_TXRX, OGPIO, LED_LINK100

LAU1

GND

AVDD33, AVDD33, RSET, AVDD10, CKXTAL2, CKXTAL1, AVDD33, DVDD10(NC), LEDO, DVDD10, DATAO, GPO/SMBALERT, LED1/EESK

MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 AVDD10(NC) MDIP2(NC) MDIN2(NC) AVDD10(NC) MDIP3(NC) MDIN3(NC) AVDD33(NC)

P_MDI0+ P_MDI0- VDD10 P_MDI1+ P_MDI1- VDD10 P_MDI2+ P_MDI2- VDD10 P_MDI3+ P_MDI3- 3VDUAL_R

REGOUT VDDREG VDDREG ENSWREG EEDI LED3/EEDO EECS DVDD10 LANWAKEB DVDD33 ISOLATEB PERSTB

DVDD10, SMBCLK(NC), SMBDATA(NC), CLKREQB, HSIP, HSIN, REFCLK_P, REFCLK_N, EVDD10, HSOP, HSON, GND

RTL8111F-VL-CG/QFN48

0.2版要修改

Data trace(MDI0~3)的+/-線長需等長,誤差在5mils以內,Pair跟Pair之間線長,最長跟最短data trace請勿超過800 mil

XTALI_P, XTALO_P

LAX1 25M/20p/30ppm/49US/20/D

LAC5 27p/4/NPO/50V/J

LAC6 27p/4/NPO/50V/J

Pin34/35(VDDREG) 接到3VDUAL的trace 建議寬度大於 40mil

REGOUT, VDDREG_IN

LAR9 1/6

LA_VDD33

ENSWREG LAR8 0/6/SHT/M/X

LAR7 8.2K/4

LED_LINK1000

LAR6 8.2K/4

VDD10

-PCIE_WAKE

LA_VDD33

ISOLATEB

PCIE_RST-

LABC12 LABC13 4.7u/6/X5R/6.3V/K

0.1u/4/X7R/16V/K

VCC3

LAR4 1K/4/1

LAR5 15K/4/1

ISOLATEB 21

-PCIE_WAKE 15,18,19,31,32

PCIE_RST- 19,21,31

PCIE_RST- LABC4 100p/4/NPO/50V/J/X

LAR2 8.2K/4

LAR1 8.2K/4

3VDUAL_R

ML_OP, ML_ON, SRCCLK_LAN, -SRCCLK_LAN

ML_IP LC3 0.1u/4/X7R/16V/K

ML_IN LC4 0.1u/4/X7R/16V/K

CLOSE LAN CHIP 離IC近越好200mil以內

3VDUAL_R

LAEC1 560u/FP/D/6.3V/68/7m

LABC6 LABC16 LABC15 LABC5 LABC18 LABC14 0.1u/4/X7R/16V/K

(CLOSE LU1)

VDD10

DVDD10

LABC11 LABC10 LABC9 LABC3 LABC19 LABC17 LABC8 0.1u/4/X7R/16V/K

USB_LAN CONNECTOR

P35-152-19W9

U4 U3 U2 U1 U8 U7 U6 U5 L1 L3 L5 L7 L9 L2 L4 L6 L8 L10 D1 D2 D3 D4

YELLOW ORANGE (+,-) GREEN (-,+)

VDD10

LAL1 4.7uH/0.8A/3225/S REGOUT

LABC20 4.7u/6/X5R/6.3V/K LABC21 0.1u/4/X7R/16V/K LABC1 0.1u/4/X7R/16V/K LABC2 1u/4/X5R/6.3V/K

建議使用X5R電容

USB_LAN

RTL8101E:LR38/LC5/LR43/LC6-->O

RTL8111C:LC6-->O

RTL8102E:LC5/LC6-->O

FOR EMI

LABC22 0.01u/4/X7R/25V/K

USB_LAN

P_MDI0+ P_MDI0- P_MDI1+ P_MDI1- P_MDI2+ P_MDI2- P_MDI3+ P_MDI3- L1 L2 L3 L4 L5 L6 L7 L8 L9 L10

LABC25 0.01u/4/X7R/25V/K

UP

DOWN

USB+LAN/1G/GO,Y/OS/RA/D/1

D1 LED_ACT_TXRX

D2 LED_D2 LAR13 150/4/1

D3 LED_LINK100

D4 LED_LINK1000

3VDUAL_R

LAFB2 0/6/SHT/M/X

LABC24 0.1u/4/Y5V/16V/Z/X

U1 U2 -USBP10 U3 +USBP10 U4 U5 FUSEVCC41 U6 -USBP11 U7 +USBP11 U8

FUSEVCC4 -USBP10 15 +USBP10 15

FUSEVCC41 USBP11 15 +USBP11 15

5VDUAL UBF3 SMD1206P200SLR/S

UEC6 560u/FP/D/6.3V/68/7m

FUSEVCC4

LABC7 0.1U/4/X7R/16V/K

5VDUAL UBF4 SMD1206P200SLR/S

FUSEVCC41

LABC23 0.1U/4/X7R/16V/K

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)

1G :USB+LAN/1G/GO,Y/OS/RA/D/1

100M:USB+LAN/100/GO,Y/OS/RA/D/1

EMI LR1 0/6/SHT/M/X

UBESD3

+USBP10 1 -USBP11 6

2 5 FUSEVCC4

-USBP10 3 4 +USBP11

AOZ8902CIL/SOT23-6

GIGABYTE™

Title: REALTK RTL8111C

Size: Custom | Document Number: GA-970A-D3 | Rev: 3.02

Date: Thursday, October 04, 2012 | Sheet 34 of 36