Fircrest 13" Schematics Document

Whiskey Lake -U 42

2019-04-11

REV:X02

DY : None Installed
WWAN:For WWAN installed
Sensor:For Sensor Installed
Debug:For Debug Port installed
GD:For google installed
TPM:For windows installed

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A4	Document Number: Fircrest 13"	Rev: X01
Date: Thursday, April 18, 2019	Sheet 1 of 106	

Project code : 4PD0H8010001
PCB P/N : 18780
Revision : SE

Fircrest Bay 13" Block Diagram

eDP 13" Panel 55 — EDP 1.4
Touch Panel 55 — I2C

NON_TBT_CONFIG

HDMI Level Shift PS8407A 57 — TMDS / DDI1
Retiming Switch PS8802QFN52GTR 71 — DDI/USB3.1 / DDI2 / USB3.1 [1] GEN2

HDMI 1.4b 57 — TMDS
Type C Connector 73 — TBT3 / USB3.1 / DP 1.2

ALPINE RIDGE JHL6340 71
DDI1
DDI2
PCIE[5] PCIE GEN2
PCIE[6] PCIE GEN2
PCIE[7] PCIE GEN2
PCIE[8] PCIE GEN2

Flash ROM WINBOND W25Q80DVSSIG 71 — SPI

TBT_CONFIG
USB2.0 / I2C
CC control pin

Type C PD TI TPS65982DD 72
From EC — I2C
USB2.0 [1]

Flash ROM WINBOND W25Q80DVSSIG 72 — SPI

M.2 2230 Hybrid Key E
WLAN+BT
802.11ac / BT 5.0
support CNVi / Discrete mode 61
USB2.0 [10]
PCIE[10] PCIE GEN2
CNVI

Micro SIM 62

M.2 3042 KEY B
WWAN/LTE/SSD 62
USB2.0 [7]
SATA[1] SATA GEN3/ PCIE [12] PCIE Gen2
USB3.1 [4] GEN1

De-pop on Fircrest
Connector RJ45 32 — LOM Intel WGI219LM-vPRO 97 / WGI219V-Non-vPRO
PCIE [9] PCIE GEN1

Connector SD 4.0 33 — Card Reader Realtek RTS5242 33
PCIE [11] PCIE GEN3

M.2 2280 KEY M
SSD 63
PCIE[13] PCIE GEN3
PCIE[14] PCIE GEN3
PCIE[15] PCIE GEN3
PCIE[16] PCIE GEN3
SATA[2] SATA GEN3

Intel CPU

WHISKEY LAKE-U 42

WHL U PCH-LP

16 PCIe* Lanes
3 SATA Lanes
6 USB3.1 Gen1/Gen2 Lanes
5 GbE Lanes
2 Remapped PCIe* storage

3,4,5,6,7,8,9,10,11,15
16,17,18,19,20,21,22,23

DDR4 Channel A — DDR4 2400 SODIMM A 12
DDR4 Channel B — DDR4 2400 SODIMM B 13
NON-INTERLEAVE MODE

USB2.0 [3] — USB PowerShare PERICOM PI5USB2546ZHEX 36 — USB2.0 [3] — USB3.1 / PowerShare USB Port : 2 35
USB3.1 [3] GEN1

USB2.0 [2] — USB3.1 USB Port : 1 35
USB3.1 [2] GEN1

USB2.0 [6] — Internal Digital MIC Camera 55
Universal Jack

HDA — Audio Codec RealTek ALC3254 27 — (2W, 4ohm /channel) 2CH Speaker

SPI — Flash ROM WSON MXIC MX25L25645GZ2I-08G (32MB) 25 — SPI — Google Servo 88
SPI

I2C / UART — H1 Secure Microcontroller 88 — UART — Google Servo 88

eSPI — EC SMSC MEC 5106 24
KB/TP Conn 65
Thermal & Fan 26
eSPI debug port 68

GPIO — Hall sensor SEIKO S-5712ACDL1-M3T1U 67
GPIO — LED BD SEIKO S-5712ACDL1-M3T1U 64

USB2.0 [9][RESV] — Finger Printer 92 — USB2.0

USH BD
From EC
SMBUS
USB2.0 [8]
CV3 Lynx Controller Broadcom BCM58202 66
FLASH ROM WSON 6*5 Winbond WQ64JVZPIQ(8MB) CV3
RFID/NFC RFID Antenna
SmartCard IC NXP TDA8034HN
Connector Smart Card

Accelerometer ST LNG2DMTR 70
E-compass ST LIS2MDLTR
Accelerometer + Gyro ST LSM6DS3USTR
P-sensor SEMTECH SX9310
I2C — Sensor BD

Charger ISL9538HRTZ-GP-U 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC SY8288BRAC/SY8288CRAC 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 3D3V_S5 5V_AUX_S5 5V_S5

CPU DC/DC FDMF3035-GP 47

INPUTS	OUTPUTS
DCBATOUT	1V_VCCGT

CPU DC/DC ISL95808HRZ-T-1-GP 50

INPUTS	OUTPUTS
DCBATOUT	1V_VCCSA

SYSTEM DC/DC SY8288RAC 51

INPUTS	OUTPUTS
DCBATOUT	1D2V_S3

SYSTEM DC/DC AOZ2260QI-10-GP 52

INPUTS	OUTPUTS
DCBATOUT	1D05V_S5

SYSTEM DC/DC RT6542AGQW-GP 54

INPUTS	OUTPUTS
DCBATOUT	1D05V_VCCPRIM_CORE

Load Switches

INPUTS	OUTPUTS
3D3V_S5	3D3V_S5_PCH 3D3V_LAN 3D3V_S5_WWAN 3D3V_S5_WLAN 2D5V_S3 1D8V_S5 VCDVDD_FUSE 3D3V_S0
3D3V_S0	+3V_AVDD 3D3V_CAMERA_S0 3D3V_S0_SATA
5V_S5	5V_S0 1D05V_VCCIO
5V_S0	+5V_PVDD 5V_TSP_S0 5V_HDMI
1D8V_S5	1D8V_S0
1D2V_S3	0D6V_S0 1D2V_VCCPLL_OC
1D05V_S5	1D05V_VCCST 1D05V_VCCSTG

PCB LAYER(FR4-10 Layer)

L1:Top	L6:Signal
L2:GND	L7:GND/PWR
L3:Signal	L8:Signal
L4:GND	L9:GND
L5:Signal	L10:Bottom

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A2 | Document Number: Fircrest 13" | Rev: X01
Date: Thursday, April 18, 2019 | Sheet 2 of 106

Main Func = CPU

[24] PECI_CPU
[24,43,44,46] PROCHOT#_CPU
[24] THERMTRIP#_CPU
[99] BPM_N0
[99] BPM_N1
[99] CPU_JTAG_TCK
[99] CPU_JTAG_TDI
[99] CPU_JTAG_TDO
[99] CPU_JTAG_TMS
[99] CPU_JTAG_TRST#
[99] CPU_JTAG_PRDY#
[99] CPU_JTAG_PREQ#
[99] PCH_JTAG_TCK
[17] H_CPUPWRGD
[55] TOUCH_SCREEN_PD#_R
[24,65] TOUCHPAD_INTR#
[55] TOUCH_SCREEN_DET#

TP309 Do Not Stuff
R301 DY Do Not Stuff
CATERR# PECI_CPU PROCHOT#_CPU_R THERMTRIP#_CPU
TP310 Do Not Stuff
TP311 Do Not Stuff
BPM_N0 BPM_N1 BPM_N2 BPM_N3

CPU1D 4 OF 20
CATERR# PECI PROCHOT# THRMTRIP#
BPM#0 BPM#1 BPM#2 BPM#3
PROC_TCK PROC_TDI PROC_TDO PROC_TMS PROC_TRST#
PCH_TCK PCH_TDI PCH_TDO PCH_TMS PCH_TRST# PCH_JTAGX
GPP_E3/CPU_GP0 GPP_E7/CPU_GP1 GPP_B3/CPU_GP2 GPP_B4/CPU_GP3
PROC_PREQ# PROC_PRDY#
PROC_POPIRCOMP PCH_OPIRCOMP
Do Not Stuff

CPU_JTAG_TCK CPU_JTAG_TDI CPU_JTAG_TDO CPU_JTAG_TMS CPU_JTAG_TRST# PCH_JTAG_TCK CPU_JTAG_PREQ# CPU_JTAG_PRDY#
MEM_INTERLEAVED TOUCH_SCREEN_PD# TOUCHPAD_INTR# TOUCH_SCREEN_DET#
49D9R2F-GP R305 CPU_POPIRCOMP
49D9R2F-GP R304 PCH_POPIRCOMP

1D05V_VCCSTG
R311 0R1J-GP
R320 DY Do Not Stuff
R323 100R2F-L1-GP-U
RN302 DEBUG SRN51J-GP
R319 51R2J-2-GP
RN304 DY Do Not Stuff

R302 100R2F-L1-GP-U
TOUCH_SCREEN_PD#_R TOUCH_SCREEN_PD#
PQ4305 DY
TOUCH_SCREEN_PD#_Q
R303 DY Do Not Stuff
3D3V_S0
Do Not Stuff

#544669 CRB Rev0.52
1D05V_VCCST
R310 1KR2J-1-GP
THERMTRIP#_CPU
H_CPUPWRGD
ED301 DY Do Not Stuff
Do Not Stuff

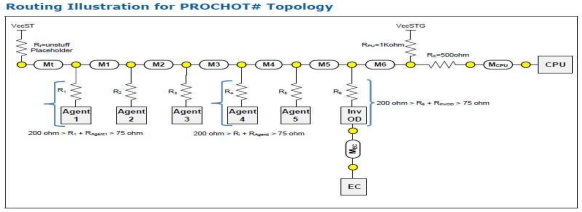
3D3V_S0
1D8V_S0
R308 10KR2F-2-GP TOUCHPAD_INTR#
R309 DY Do Not Stuff TOUCH_SCREEN_PD#
R313 DY Do Not Stuff On_LCD_SIDE

3D3V_SUS
DY R314 Do Not Stuff
MEM_INTERLEAVED
R315 10KR2F-2-GP

1D05V_VCCSTG
R306 1KR2J-1-GP
Rb
R307 499R2F-2-GP
Ra
PROCHOT#_CPU PROCHOT#_CPU_R

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

DIMM_TYPE	
LOW	HIGH
NON_INTERLEAVED	INTERLEAVED

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)
Size: A4
Document Number: Fircrest 13"
Rev: X01
Date: Thursday, April 18, 2019
Sheet 3 of 106

Main Func = CPU

Edp

[55] eDP_TX_CPU_N0
[55] eDP_TX_CPU_P0
[55] eDP_TX_CPU_N1
[55] eDP_TX_CPU_P1

[55] eDP_AUX_CPU_N
[55] eDP_AUX_CPU_P

[55] EDP_HPD

[55] eDP_BLEN_CPU
[55] eDP_BLCTRL_CPU
[55] eDP_VDDEN_CPU

DP to HDMI

[57] HDMI_DDI_TX_N2
[57] HDMI_DDI_TX_P2
[57] HDMI_DDI_TX_N1
[57] HDMI_DDI_TX_P1
[57] HDMI_DDI_TX_N0
[57] HDMI_DDI_TX_P0
[57] HDMI_DDI_TX_N3
[57] HDMI_DDI_TX_P3

[57] HDMI_DET_CPU

[57] HDMI_SCL_CPU
[57] HDMI_SDA_CPU

DP to AR

[71] DP2_DDI_TX_N0
[71] DP2_DDI_TX_P0
[71] DP2_DDI_TX_N1
[71] DP2_DDI_TX_P1
[71] DP2_DDI_TX_N2
[71] DP2_DDI_TX_P2
[71] DP2_DDI_TX_N3
[71] DP2_DDI_TX_P3

[71] DP2_AUX_CPU_P
[71] DP2_AUX_CPU_N

[71,72] DP2_HPD_CPU

[88] PCH_WP
[24] eDP_BLEN_CPU_R

DP to HDMI

HDMI_DDI_TX_N2 AL5
HDMI_DDI_TX_P2 AL6
HDMI_DDI_TX_N1 AJ5
HDMI_DDI_TX_P1 AJ6
HDMI_DDI_TX_N0 AF6
HDMI_DDI_TX_P0 AF5
HDMI_DDI_TX_N3 AE5
HDMI_DDI_TX_P3 AE6

DP to MUX

DP2_DDI_TX_N0 AC4
DP2_DDI_TX_P0 AC3
DP2_DDI_TX_N1 AC1
DP2_DDI_TX_P1 AC2
DP2_DDI_TX_N2 AE4
DP2_DDI_TX_P2 AE3
DP2_DDI_TX_N3 AE1
DP2_DDI_TX_P3 AE2

CPU1A 1 OF 20

DDI1_TXN0
DDI1_TXP0
DDI1_TXN1
DDI1_TXP1
DDI1_TXN2
DDI1_TXP2
DDI1_TXN3
DDI1_TXP3

DDI2_TXN0
DDI2_TXP0
DDI2_TXN1
DDI2_TXP1
DDI2_TXN2
DDI2_TXP2
DDI2_TXN3
DDI2_TXP3

EDP_TXN0 AG4 eDP_TX_CPU_N0
EDP_TXP0 AG3 eDP_TX_CPU_P0
EDP_TXN1 AG2 eDP_TX_CPU_N1
EDP_TXP1 AG1 eDP_TX_CPU_P1
EDP_TXN2 AJ4
EDP_TXP2 AJ3
EDP_TXN3 AJ2
EDP_TXP3 AJ1

EDP_AUX_N AH4 eDP_AUX_CPU_N
EDP_AUX_P AH3 eDP_AUX_CPU_P

DISP_UTILS AM7

DDI1_AUX_N AC7
DDI1_AUX_P AC6
DDI2_AUX_N AD4 DP2_AUX_CPU_N
DDI2_AUX_P AD3 DP2_AUX_CPU_P
DDI3_AUX_N AG7
DDI3_AUX_P AG6

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6 HDMI_DET_CPU_R
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6 DP2_HPD_CPU_R
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7 PCH_WP
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6 FFS_INT2
GPP_E17/EDP_HPD/DISP_MISC4 CM7 EDP_HPD

EDP_BKLTEN CK11 eDP_BLEN_CPU_R
EDP_VDDEN CG11 eDP_VDDEN_CPU
EDP_BKLTCTL CH11 eDP_BLCTRL_CPU

For TYPEC

TP401 Do Not Stuff

R402 1 Do Not Stuff eDP_BLEN_CPU

575412

eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length
eDP_RCOMP	5 mils	25 mils	24.9 or 100 Ω ±1%	600 mils
Note: Must maintain low DC resistance routing (<0.1Ω)				

0D95V_VCCIO

R401 24D9R2F-L-GP

eDP_RCOMP_CPU AM6

DISP_RCOMP

PH/PL on TBT Page

HDMI_SCL_CPU CC8
HDMI_SDA_CPU CC9
GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
GPP_E19/DPPB_CTRLDATA

CPU_DP2_CTRL_CLK CH4
CPU_DP2_CTRL_DATA CH3
GPP_E20/DPPC_CTRLCLK
GPP_E21/DPPC_CTRLDATA

CP4
CN4
GPP_E22/DPPD_CTRLCLK
GPP_E23/DPPD_CTRLDATA

CR26
CP26
GPP_H16/DDPF_CTRLCLK
GPP_H17/DDPF_CTRLDATA

Do Not Stuff

3D3V_S0 R411 Do Not Stuff
DX
CPU_DP2_CTRL_CLK
CPU_DP2_CTRL_DATA
R412 2K2R2F-GP

3D3V_S5_PCH

R405 10KR2J-3-GP
R406 10KR2J-3-GP
Q401
HDMI_DET_CPU_R
HDMI_DET_CPU
HDMI_DET_CPU_P
R403 100KR2J-1-GP
2N7002KDW-1-GP
75.27002.F7C

R407 10KR2J-3-GP
R408 10KR2J-3-GP
Q402
DP2_HPD_CPU_R
DP2_HPD_CPU
CPU_DP2_HPD_P
R410 100KR2J-1-GP
2N7002KDW-1-GP
75.27002.F7C

ALL

	Canon Lake U PCH-LP	CPU (iTBT, DP1.4, USB3.1 g2) eDP DDI A	DDI 1	DDI 2		
North Bay 13 Bandon	13 UU (non-TBT)	LCD	HDMI 1.4	Type-C Port 1		
	13 UU (TBT)	LCD	TBT (Alpine Ridge Port 0)	TBT (Alpine Ridge Port 1)	HDMI on AR side-port	

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

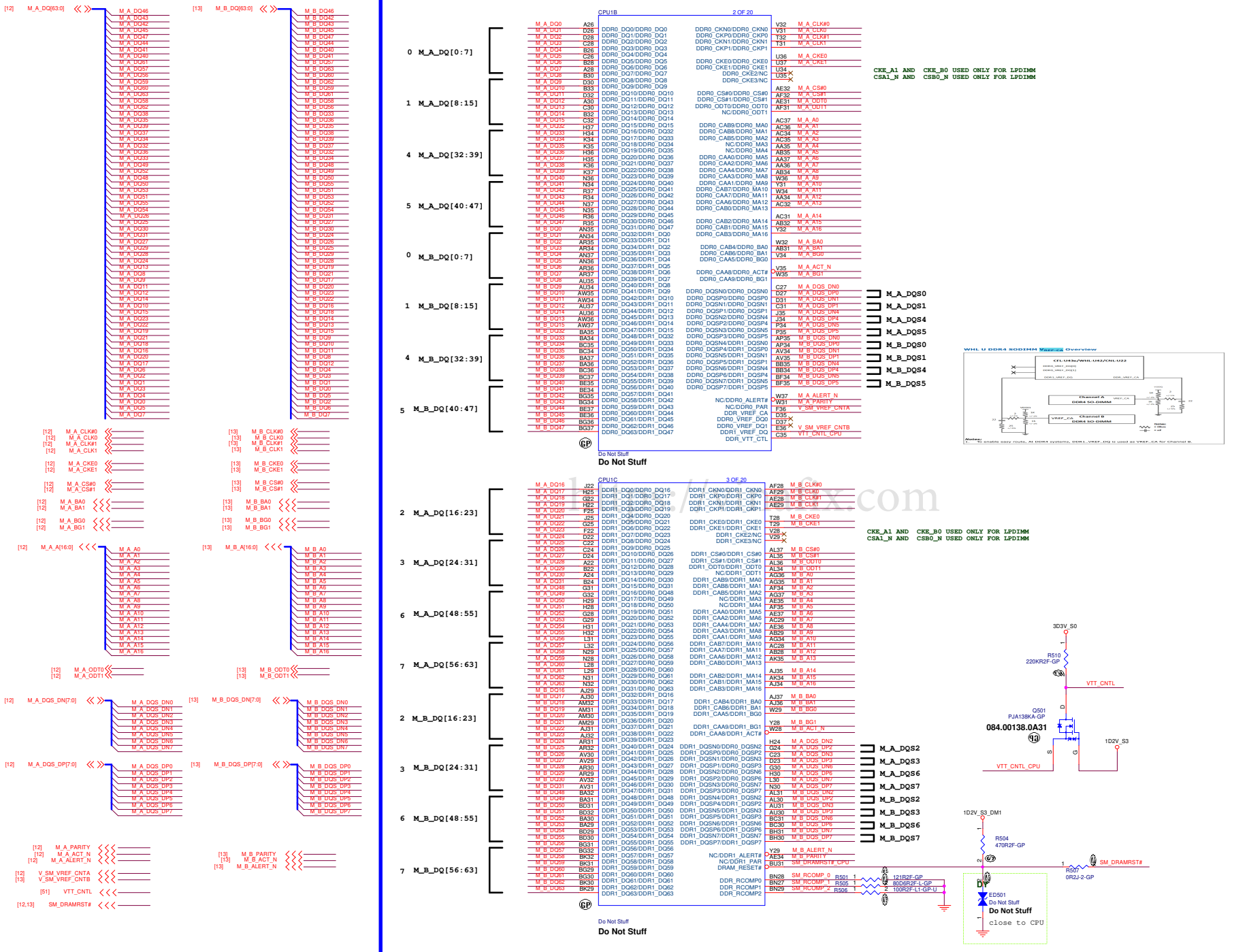
Title: CPU_(JTAG/CPU SIDE BAND)

Size: A4 | Document Number: Fircrest 13" | Rev: X00

Date: Thursday, April 18, 2019 | Sheet 4 of 106

Main Func = CPU

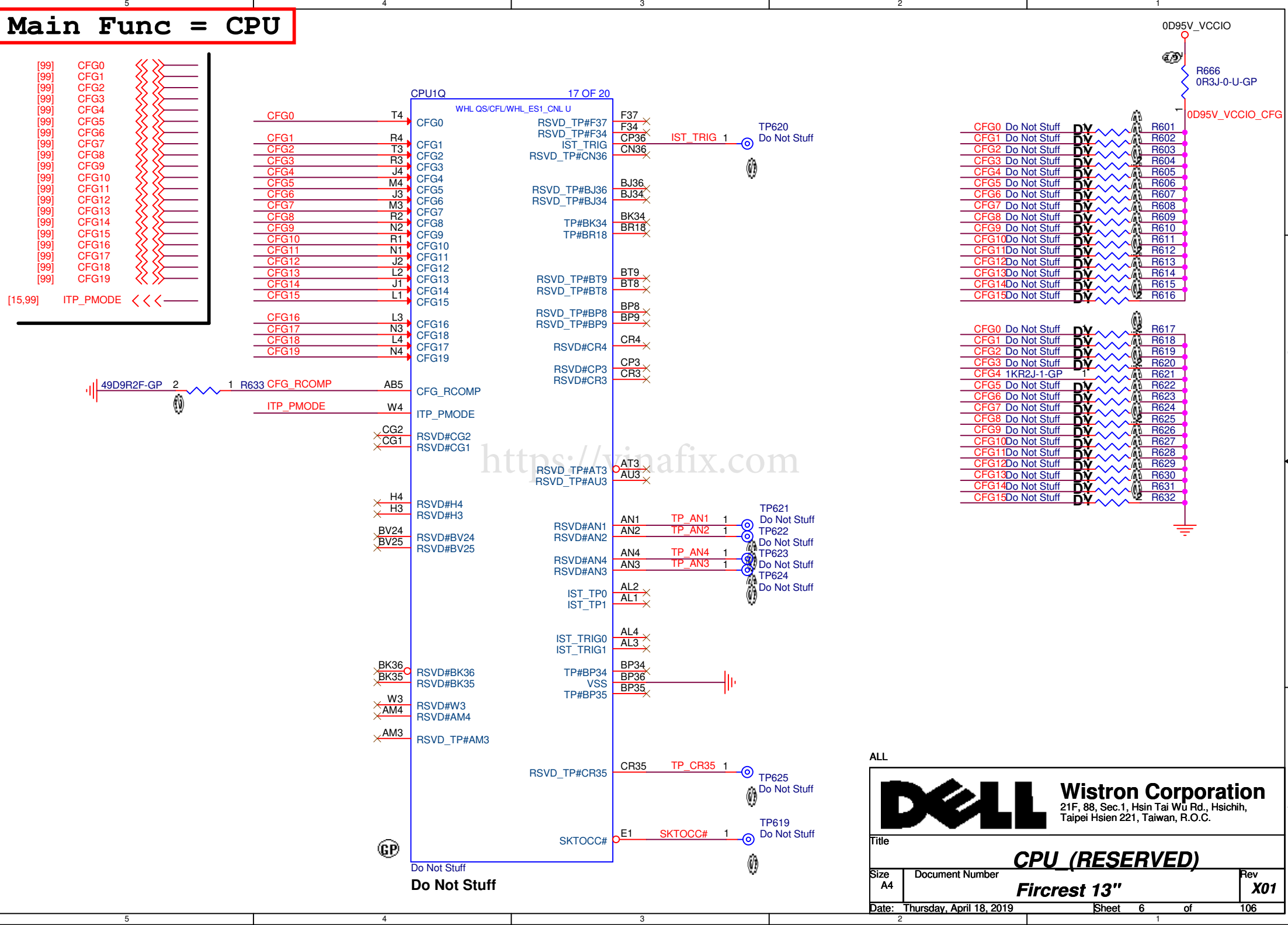
DDR4 ball type: NON- Interleaved Type



teknisi indonesia

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (DDR)
Size	A2
Document Number	Fircrest 13"
Rev	X01
Date:	Thursday, April 18, 2019
Sheet	5 of 106

Main Func = CPU



Do Not Stuff

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_(RESERVED)**

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 6 of 106

Main Func = CPU

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

[46] VCCCORE_SENSE
[46] VSSCORE_SENSE
[46] SVID_DATA_CPU
[46] SVID_CLK_CPU
[46] SVID_ALERT#_CPU

SVID DATA

1D05V_VCCST
#575962
CLOSE TO VR
R726
100R2F-L1-GP-U
SVID_DATA_CPU_R
R702
0R2J-2-GP
SVID_DATA_CPU

SVID CLOCK

1D05V_VCCST
#575962
CLOSE TO VR
DY
R723
Do Not Stuff
SVID_CLK_CPU_R
R703
0R2J-2-GP
SVID_CLK_CPU

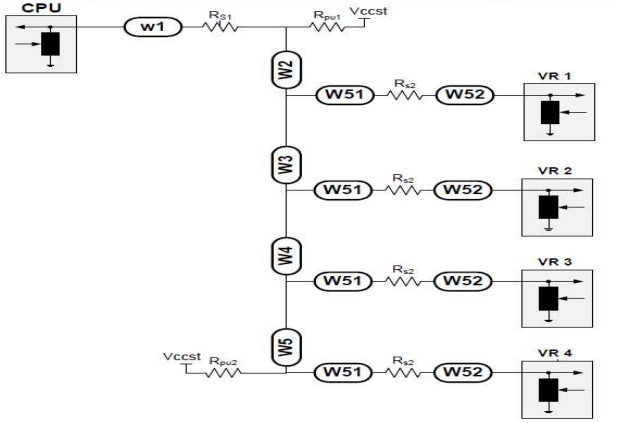
SVID ALERT

1D05V_VCCST
#575962
CLOSE TO VR
R727
56R2J-4-GP
SVID_ALERT#_CPU_R
R728
220R2J-L2-GP
SVID_ALERT#_CPU

Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{BT} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

Figure 10-7. Routing Illustration for SVID Topology



1V_CPU_CORE
CPU1L
12 OF 20
1V_CPU_CORE

AN9	VCCCORE	VCCCORE	AW24
AN10	VCCCORE	VCCCORE	AW25
AN24	VCCCORE	VCCCORE	AW26
AN26	VCCCORE	VCCCORE	AW27
AN27	VCCCORE	VCCCORE	AY24
AP2	VCCCORE	VCCCORE	AY26
AP9	VCCCORE	VCCCORE	BA5
AP24	VCCCORE	VCCCORE	BA7
AP26	VCCCORE	VCCCORE	BA8
AR5	VCCCORE	VCCCORE	BA25
AR6	VCCCORE	VCCCORE	BA27
AR7	VCCCORE	VCCCORE	BB2
AR8	VCCCORE	VCCCORE	BB26
AR10	VCCCORE	VCCCORE	BC5
AR25	VCCCORE	VCCCORE	BC6
AR27	VCCCORE	VCCCORE	BC7
AT9	VCCCORE	VCCCORE	BC9
AT24	VCCCORE	VCCCORE	BC10
AT26	VCCCORE	VCCCORE	BC26
AU5	VCCCORE	VCCCORE	BC27
AU6	VCCCORE	VCCCORE	BD5
AU7	VCCCORE	VCCCORE	BD8
AU8	VCCCORE	VCCCORE	BD10
AU9	VCCCORE	VCCCORE	BD25
AU24	VCCCORE	VCCCORE	BD27
AU25	VCCCORE	VCCCORE	BE9
AU26	VCCCORE	VCCCORE	BE24
AU27	VCCCORE	VCCCORE	BE25
AV2	VCCCORE	VCCCORE	BE26
AV5	VCCCORE	VCCCORE	BE27
AV7	VCCCORE	VCCCORE	BF2
AV10	VCCCORE	VCCCORE	BF9
AV27	VCCCORE	VCCCORE	BF24
AW5	VCCCORE	VCCCORE	BF26
AW6	VCCCORE	VCCCORE	BG27
AW7	VCCCORE	VCCCORE	
AW8	VCCCORE		
AW9	VCCCORE	VCC_SENSE	AN6 VCCCORE_SENSE
AW10	VCCCORE	VSS_SENSE	AN5 VSSCORE_SENSE
	VCCCORE		
BB9		VIDALERT#	AA3 SVID_ALERT#_CPU_R
BC24	RSVD#BB9	VIDSCK	AA1 SVID_CLK_CPU_R
AY9	RSVD#BC24		
BB24	RSVD#AY9	VIDSOUT	AA2 SVID_DATA_CPU_R
	RSVD#BB24	RSVD#Y3	Y3
		VCCSTG	BG3

Do Not Stuff
Do Not Stuff

1D05V_VCCSTG

1V_CPU_CORE
R719
100R2F-L1-GP-U
VCCCORE_SENSE
VSSCORE_SENSE
R720
100R2F-L1-GP-U

Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(VCC_CORE)**

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 7 of 106

Main Func = CPU

[46] VCCGT_SENSE
[46] VSSGT_SENSE

[46] VSSSA_SENSE
[46] VCCSA_SENSE

[54] VCCIO_SENSE
[54] VSSIO_SENSE

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE

1V_VCCGT
R807 100R2F-L1-GP-U
VCCGT_SENSE
VSSGT_SENSE
R808 100R2F-L1-GP-U

1V_VCCSA
R810 100R2F-L1-GP-U
VCCSA_SENSE
VSSSA_SENSE
R809 100R2F-L1-GP-U

1V_VCCGT
CPU1M 13 OF 20
WHL QS/CFL/WHL_ES1_CNL U
VCCGT: A5, A6, A8, A11, A12, A14, A15, A17, A18, A20, B3, B4, B6, B8, B11, B14, B17, B20, C2, C3, C6, C7, C8, C11, C12, C14, C15, C17, C18, C20, D4, D7, D11, D12, D14, D15, D17, D18, D20, E4, F5, F6, F7, F8, F11, F14, F17, F20, G11, G12, G14, G15, G17, G18, G20, H5, H6, H7, H8, H11
VCCGT: H12, H14, H15, H17, H18, H20, J7, J8, J11, J14, J17, J20, K2, K11, L7, L8, L10, M9, N7, N8, N9, N10, P2, P8, R9, T8, T9, T10, U8, U10, V9, W8, W9
1V_CPU_CORE
VCCCORE: AA9, AB2, AB8, AB9, AB10, AC8, AD9, AE8, AE9, AE10, AF2, AF8, AF10, AG8, AG9, AH9, AJ8, AJ10, AK2, AK9, AL8, AL9, AL10, AM8, V2, Y8, Y10
VCCGT_SENSE: E3
VSSGT_SENSE: D2
Do Not Stuff
Do Not Stuff

1V_VCCGT
1D2V_S3
C804 DY Do Not Stuff

+VCCIO(ICCMAX.=2.73A
0D95V_VCCIO
CPU1N 14 OF 20
VDDQ: AD36, AH32, AH36, AM36, AN32, AW32, AY36, BE32, BH36, R32, Y36
VCCIO_OUT: AK24, AK26, AL24, AL25, AL26, AL27, AM25, AM27, BH24, BH25, BH26, BH27, BJ24, BJ26, BP16, BP18
RSVD#BC28: BC28

1D05V_VCCST
C801 SC1U10V2KX-1DLGP2
VCCST: BP11, BP2
0.04 A

1D05V_VCCSTG
C802 SC1U10V2KX-1DLGP2
VCCSTG: BG1, BG2

1D2V_VCC_PLL_OC
C803 SC1U10V2KX-1DLGP2
VCCPLL_OC: BL27, BM26

1D05V_VCCST
BR11, BT11
0.12 A
VCCPLL
C807 SC22U6D3V3MX-1-DL-GP
C805 SCD1U16V2KX-3DLGP
C806 SC1U10V2KX-1DLGP

1V_VCCSA
VCCSA: BG8, BG10, BH9, BJ8, BJ9, BJ10, BK8, BK25, BK27, BL8, BL9, BL10, BL24, BL26, BM24, BN25
VCCIO_SENSE: BP28
VSSIO_SENSE: BP29
VSSSA_SENSE: BE7
VCCSA_SENSE: BG7
Do Not Stuff
Do Not Stuff

Vcc_{PLL_OC}	1x 1uF 0402		Do not merge Vcc_{PLL}, Vcc_{PLL_OC} and Vcc_{ST} to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
Vcc_{PLL}	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
Vcc_{ST}	1x 1uF 0402		
Vcc_{STG}	1x 1uF 0402		

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(DISPLAY)
Size: A4
Document Number: Fircrest 13"
Rev: X01
Date: Thursday, April 18, 2019
Sheet 8 of 106

(Blanking)

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A4	*Fircrest 13"*	*X01*

Date: Thursday, April 18, 2019 Sheet 9 of 106

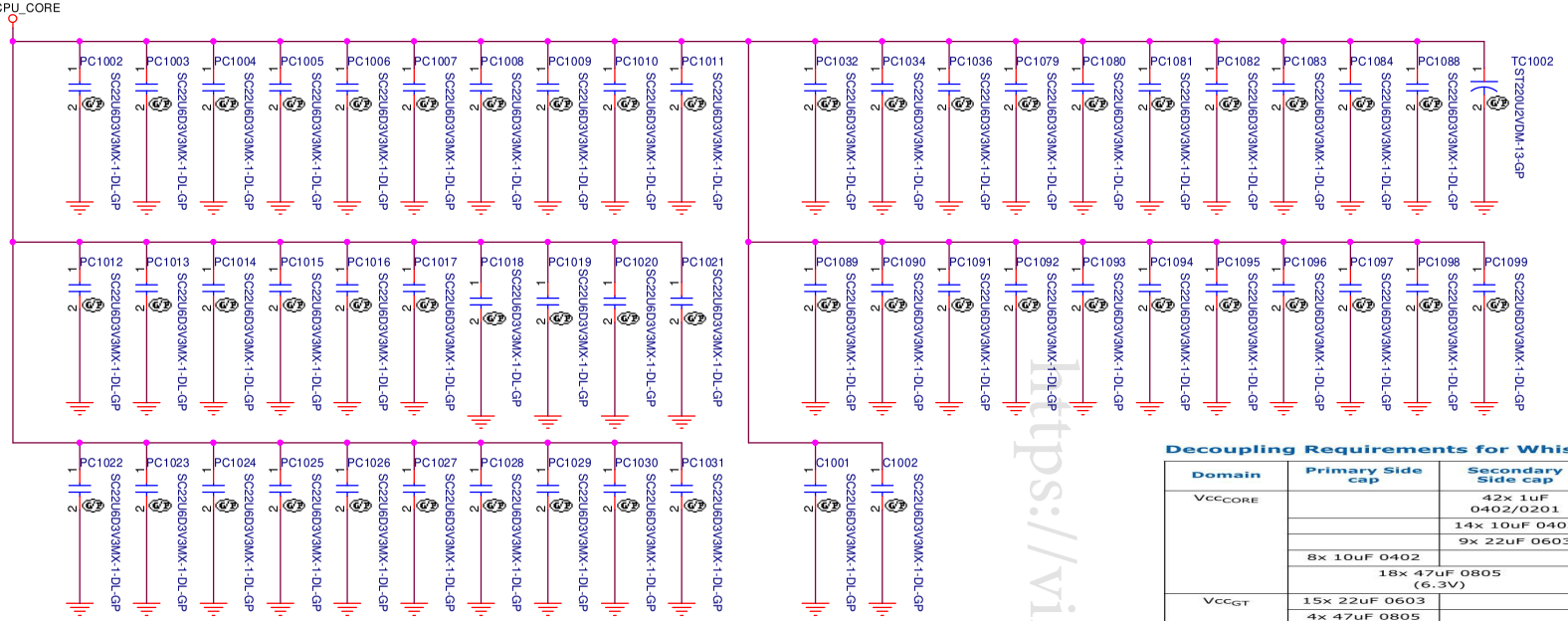
Main Func = CPU

Follow RO13 CAP account and vaule .

1V_CPU_CORE

22U*52/220U*1

1V_CPU_CORE



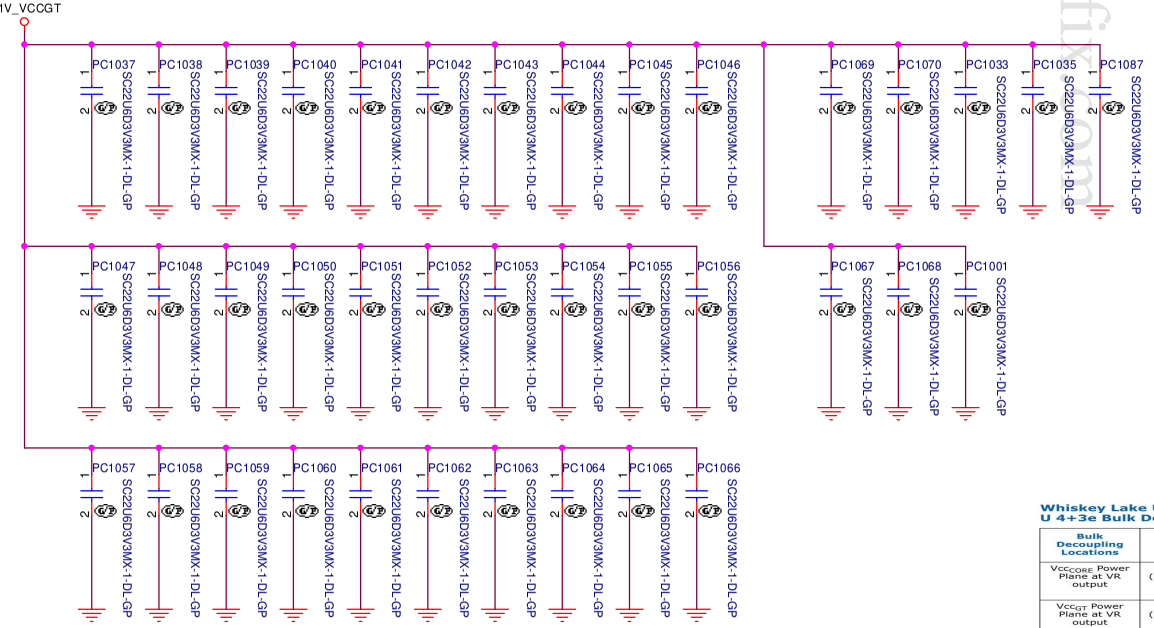
Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
$V_{CC_{CORE}}$		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.
$V_{CC_{GT}}$	15x 22uF 0603		Place as close to the package as possible
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	

1V_VCCGT

22U x 38

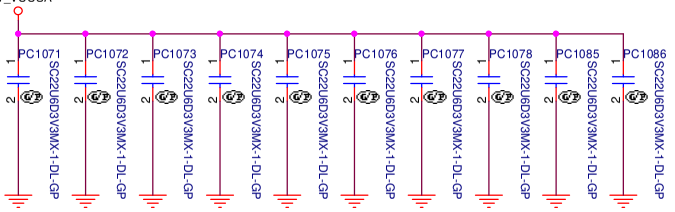
1V_VCCGT



1V_VCCSA

22U x 10

1V_VCCSA



Domain	Primary Side cap	Secondary Side cap	Placement guideline
$V_{CC_{SA}}$		*4x 0402*	*Placeholder only.*
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		*Placeholder Only*

Whiskey Lake U 4+2/Whiskey Lake U 4+2f/Cannon Lake U 2+2/ Coffee Lake U 4+3e Bulk Decoupling Example

Bulk Decoupling Locations	Example WHL U42	Example WHL U42f	Example CNL U22	Example CFL U43e	Notes
$V_{CC_{CORE}}$ Power Plane at VR output	4x 220uF (@4.5mO ESR)	3x 220uF (@4.5mO ESR)	TBD	3x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
$V_{CC_{GT}}$ Power Plane at VR output	4x 220uF (@4.5mO ESR)	2x 220uF (@4.5mO ESR)	TBD	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

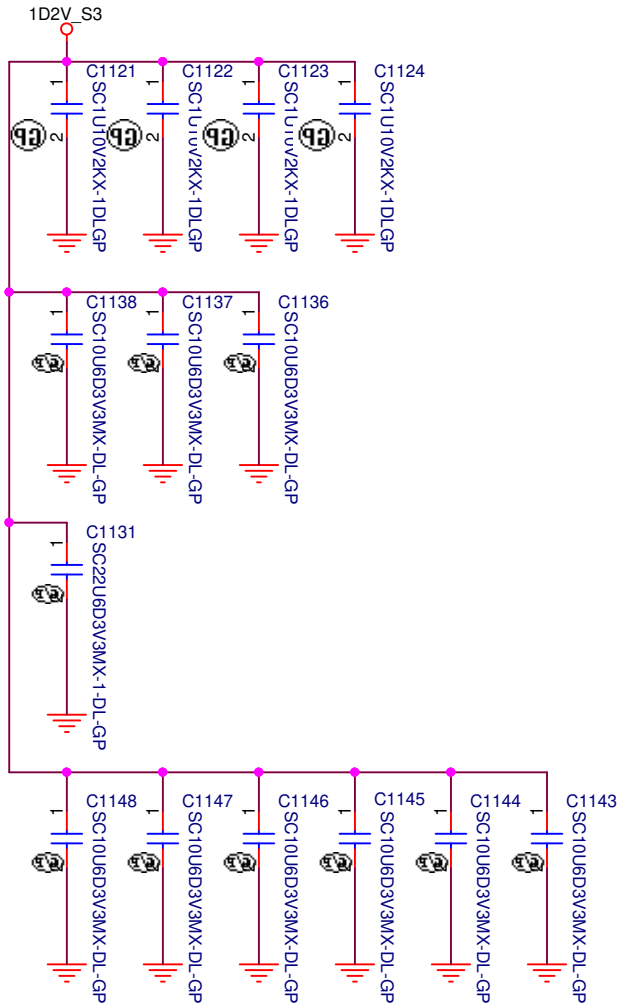
Title: CPU (Power CAP1)

Size	Document Number	Rev
A3	Fircrest 13"	X01

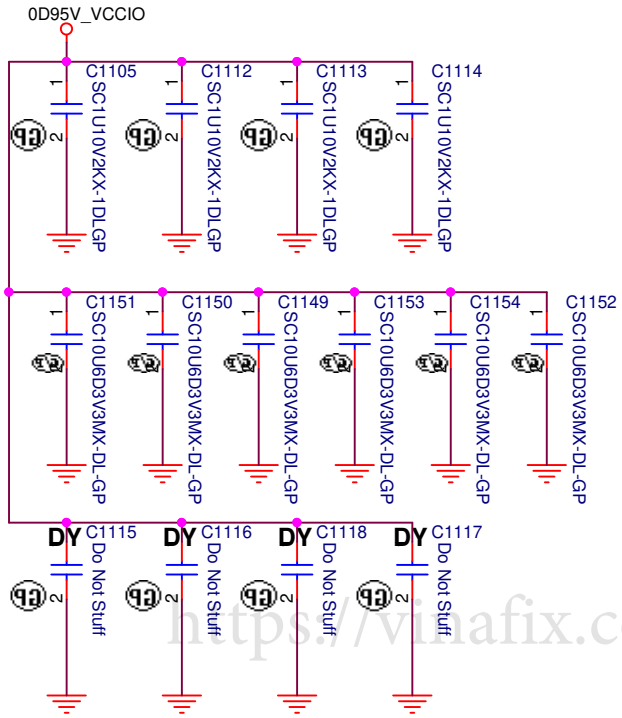
Date: Thursday, April 18, 2019 Sheet 10 of 106

Main Func = CPU

VDDQ



VCCIO



V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
Vcc_{IO}	4x 1uF 0201		Place as close to the package as possible
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		*Placeholder Only*

ALL

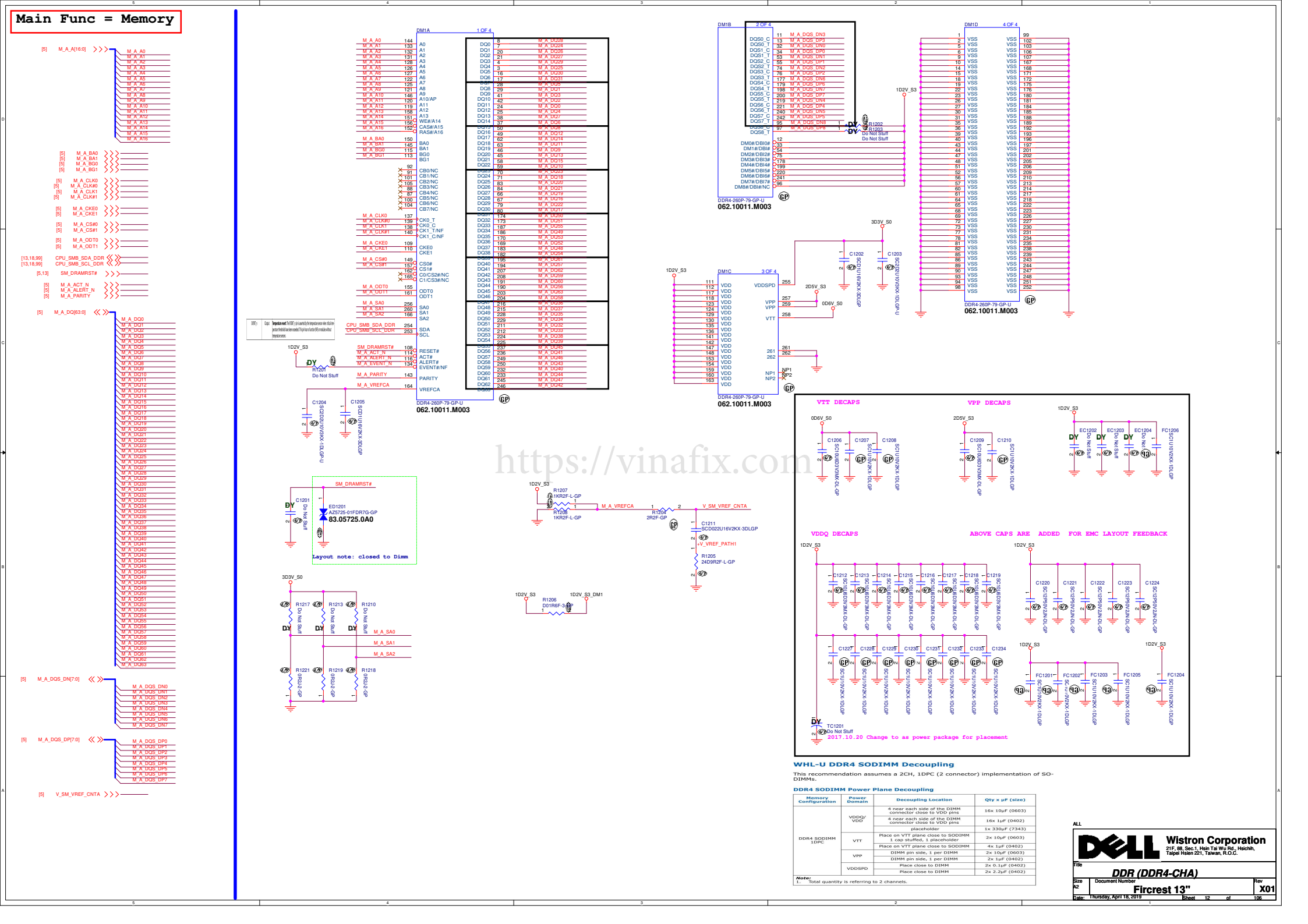
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_(Power CAP2)***

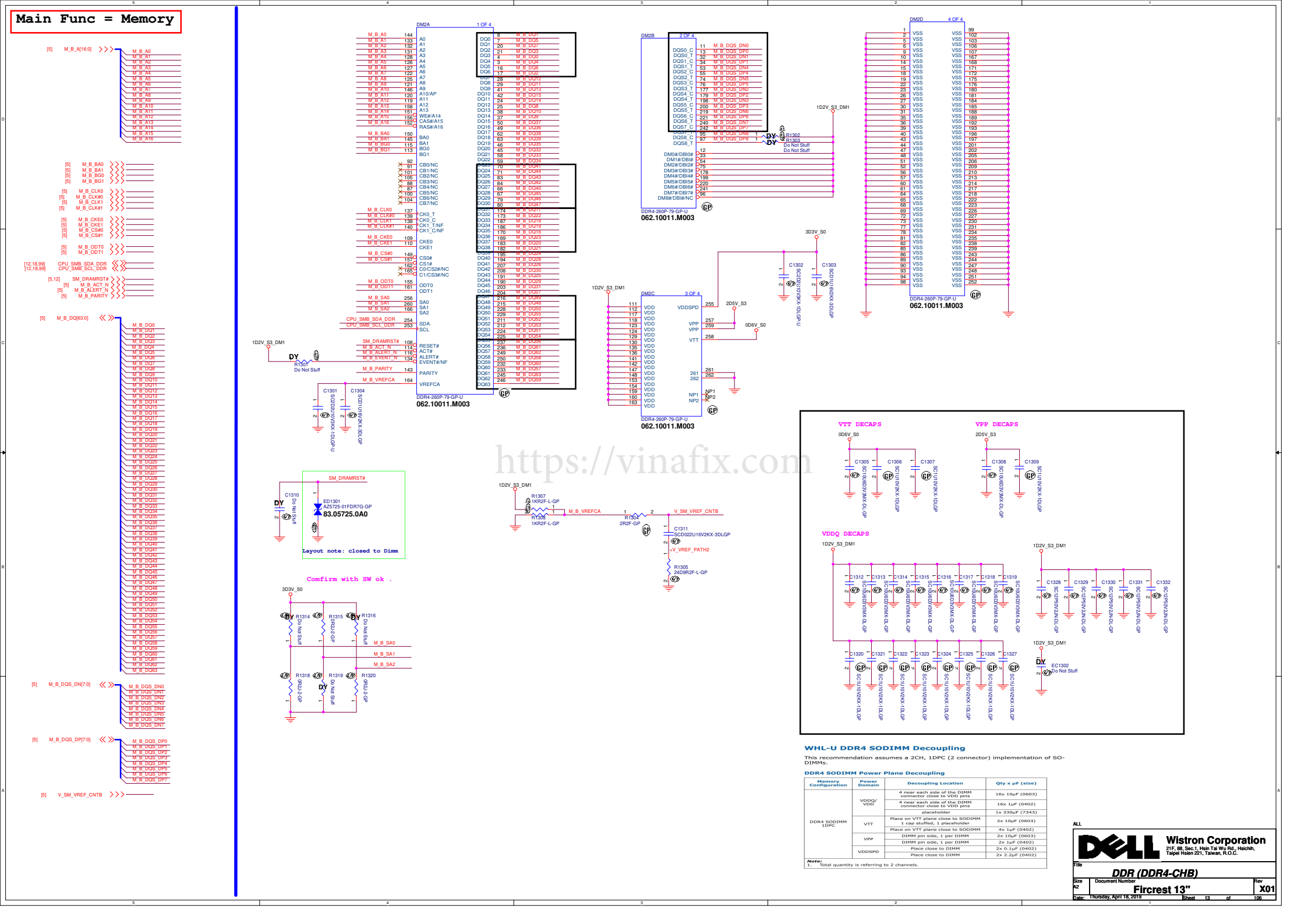
Size	Document Number	Rev
A4	***Fircrest 13"***	***X01***

Date: Thursday, April 18, 2019 Sheet 11 of 106

Main Func = Memory



Main Func = Memory



WHL-U DDR4 SODIMM Decoupling

This recommendation assumes a 2CH, 1DPC (2 connector) implementation of SO-DIMMs.

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 SODIMM 1DPC	VDDQ/ VDD	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)
		placeholder	1x 330µF (7343)
	VTT	Place on VTT plane close to SODIMM 1 cap stuffed, 1 placeholder	2x 10µF (0603)
		Place on VTT plane close to SODIMM	4x 1µF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10µF (0603)
		DIMM pin side, 1 per DIMM	2x 1µF (0402)
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)
		Place close to DIMM	2x 2.2µF (0402)

Note:
1. Total quantity is referring to 2 channels.

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHB)

Size: A2 | Document Number: Fircrest 13" | Rev: X01

Date: Thursday, April 18, 2019 | Sheet 13 of 106

(Blanking)

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

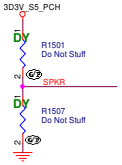
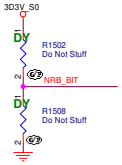
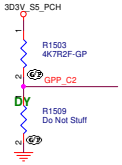
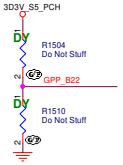
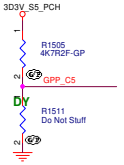
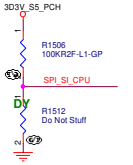
Title: *(Reserved)_SODIMM _SODIMM4*

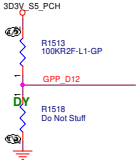
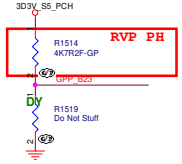
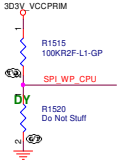
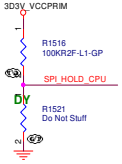
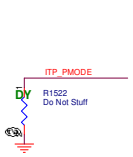
Size	Document Number	Rev
A4	*Fircrest 13"*	*X01*

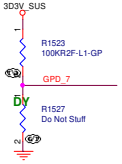
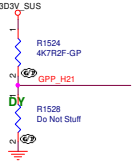
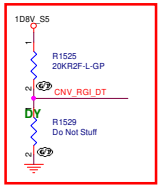
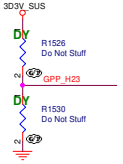
Date: Thursday, April 18, 2019 Sheet 14 of 106

Main Func = PCH

[19,27]	SPKR	<<<
[20]	NRB_BIT	<<<
[18,68,99]	SPI_SI_CPU	<<<
[18,68,99]	SPI_WP_CPU	<<<
[18,68]	SPI_HOLD_CPU	<<<
[18]	GPP_C2	<<<
[6,99]	CFG3	>>>
[6,99]	CFG4	>>>
[15,21]	GPD_7	<<<
[20]	GPP_D12	>>>
[18]	GPP_B23	>>>
[15,21]	GPD_7	>>>
[21]	GPP_H21	>>>
[21]	GPP_H23	>>>
[6,99]	ITP_PMODE	>>>
[19]	HDA_SDO	>>>
[18]	GPP_C5	>>>
[20]	GPP_B22	>>>
[20,61]	CNV_RGI_DT	>>>

Description	Top Swap Override	No Reboot	TLS Confi-dentiality	BOOT BIOS STRAP (BBS)	ESPI OR LPC	BOOT HALT
GPIO	GPP_B14 / SPKR / TIME_SYNC1 / GSPI0_CS#	GPP_B18	GPP_C2	GPP_B22	GPP_C5	SPI0_MOSI
						
LOW	Disable (Default)	Disable (Default)	Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)	SPI SELECTED. (DEFAULT)	LPC SELECTED	
HIGH	Enable	Enable	Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.	LPC SELECTED FOR SYSTEM FLASH	HIGH: ESPI IS SELECTED FOR EC	This strap should sample HIGH.
	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.	20 K± 30% internal pull-up.

Description	JTAG ODT DISABLE	EXI BOOT STALL BYPASS	CONSENT STRAP	A0 PERSONALITY STRAP	Flash Descriptor Security Override	DFXTESTMODE
GPIO	GPP_D12	GPP_B23	SPI0_IO2	SPI0_IO3	HDA_SDO/I2S0_TXD	ITP_PMODE
						
LOW	JTAGE ODT DISABLED	ENABLED (BSSB 2+2)	ENABLED	ENABLED	Enable security measures, and security is not overridden	DFXTESTMODE DISABLE (DEFAULT)
HIGH	JTAG ODT ENABLED	DIABLED (BSSB 4 WIRE)	DISABLED	DISABLED	Disable security measures, and security is overridden	DFXTESTMODE ENABLE
	20 K± 30% internal pull-up	20 K± 30% internal pull-up	20 K± 30% internal pull-up	20 K± 30% internal pull-up	20 K± 30% internal pull-down.	20 K± 30% internal pull-up

Description	RING OSCILLATOR BYPASS	XTAL FREQUENCY SELECT	M.2 CNVi Mode Select	MAF/SAF STRAP
GPIO	GPD7	GPP_H21	GPP_F6 /CNV_RGI_DT	GPP_H23
				
LOW	XTAL INPUT IS SINGLE ENDED	38.4/19.2MHZ (DEFAULT)	Integrated CNVi enabled	MAF ENABLE
HIGH	XTAL INPUT IS ATTACHED	24MHZ	Integrated CNVi disabled	SAF ENABLE

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(CS-2/EMMC)

Size	Document Number	Rev
A2	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 15 of 106

Main Func = PCH

USB3.1 PORT3
[35] USB3_USB31_RX_N
[35] USB3_USB31_RX_P
[35] USB3_USB31_TX_N
[35] USB3_USB31_TX_P

USB3.1 PORT4
[35] USB4_USB31_RX_N
[35] USB4_USB31_RX_P
[35] USB4_USB31_TX_N
[35] USB4_USB31_TX_P

WWAN
[62] WWAN_USB31_RX_N
[62] WWAN_USB31_RX_P
[62] WWAN_USB31_TX_N
[62] WWAN_USB31_TX_P

LAN
[57] LAN_PCIE_RX_N
[57] LAN_PCIE_RX_P
[57] LAN_PCIE_TX_N
[57] LAN_PCIE_TX_P

CARD
[33] CARD_PCIE_RX_N
[33] CARD_PCIE_RX_P
[33] CARD_PCIE_TX_N
[33] CARD_PCIE_TX_P

WLAN
[61] WLAN_PCIE_RX_N
[61] WLAN_PCIE_RX_P
[61] WLAN_PCIE_TX_N
[61] WLAN_PCIE_TX_P

WWAN
[62] WWAN_SATA_RX_N
[62] WWAN_SATA_RX_P
[62] WWAN_SATA_TX_N
[62] WWAN_SATA_TX_P

SSD
[63] SSD_PCIE_RX_N1
[63] SSD_PCIE_RX_P1
[63] SSD_PCIE_TX_N1
[63] SSD_PCIE_TX_P1
[63] SSD_PCIE_RX_N2
[63] SSD_PCIE_RX_P2
[63] SSD_PCIE_TX_N2
[63] SSD_PCIE_TX_P2
[63] SSD_PCIE_RX_N3
[63] SSD_PCIE_RX_P3
[63] SSD_PCIE_TX_N3
[63] SSD_PCIE_TX_P3
[63] SSD_SATA_RX_N
[63] SSD_SATA_RX_P
[63] SSD_SATA_TX_N
[63] SSD_SATA_TX_P

Type C port 1
[72] USB1_USB20_N
[72] USB1_USB20_P

FP
[92] FP_USB20_N
[92] FP_USB20_P

USB charger
[36] Charger_USB20_N
[36] Charger_USB20_P

USB2.0 port1
[35] USB3_USB20_N
[35] USB3_USB20_P

CAMERA
[56] CCD_USB20_N
[56] CCD_USB20_P

WWAN
[62] WWAN_USB20_N
[62] WWAN_USB20_P

USH
[66] USH_USB20_N
[66] USH_USB20_P

BT
[61] BT_USB20_N
[61] BT_USB20_P

[35] USB_OC1#
[36] USB_OC0#

#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

CPU1H — 8 OF 20

PCIE5_RXN/USB31_5_RXN
PCIE5_RXP/USB31_5_RXP
PCIE5_TXN/USB31_5_TXN
PCIE5_TXP/USB31_5_TXP
PCIE6_RXN/USB31_6_RXN
PCIE6_RXP/USB31_6_RXP
PCIE6_TXN/USB31_6_TXN
PCIE6_TXP/USB31_6_TXP
PCIE7_RXN
PCIE7_RXP
PCIE7_TXN
PCIE7_TXP
PCIE8_RXN
PCIE8_RXP
PCIE8_TXN
PCIE8_TXP
PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP
PCIE10_RXN
PCIE10_RXP
PCIE10_TXN
PCIE10_TXP
PCIE11_RXN/SATA0_RXN
PCIE11_RXP/SATA0_RXP
PCIE11_TXN/SATA0_TXN
PCIE11_TXP/SATA0_TXP
PCIE12_RXN/SATA1A_RXN
PCIE12_RXP/SATA1A_RXP
PCIE12_TXN/SATA1A_TXN
PCIE12_TXP/SATA1A_TXP
PCIE13_RXN
PCIE13_RXP
PCIE13_TXN
PCIE13_TXP
PCIE14_RXN
PCIE14_RXP
PCIE14_TXN
PCIE14_TXP
PCIE15_RXN/SATA1B_RXN
PCIE15_RXP/SATA1B_RXP
PCIE15_TXN/SATA1B_TXN
PCIE15_TXP/SATA1B_TXP
PCIE16_RXN/SATA2_RXN
PCIE16_RXP/SATA2_RXP
PCIE16_TXN/SATA2_TXN
PCIE16_TXP/SATA2_TXP
PCIE_RCOMPN
PCIE_RCOMPP
PCIE_RCOMP_N
PCIE_RCOMP_P
GPP_H12/M2_SKT2_CFG0
GPP_H13/M2_SKT2_CFG1
GPP_H14/M2_SKT2_CFG2
GPP_H15/M2_SKT2_CFG3
Do Not Stuff

PCIE1_RXN/USB31_1_RXN
PCIE1_RXP/USB31_1_RXP
PCIE1_TXN/USB31_1_TXN
PCIE1_TXP/USB31_1_TXP
PCIE2_RXN/USB31_2_RXN/SSIC_1_RXN
PCIE2_RXP/USB31_2_RXP/SSIC_1_RXP
PCIE2_TXN/USB31_2_TXN/SSIC_1_TXN
PCIE2_TXP/USB31_2_TXP/SSIC_1_TXP
PCIE3_RXN/USB31_3_RXN
PCIE3_RXP/USB31_3_RXP
PCIE3_TXN/USB31_3_TXN
PCIE3_TXP/USB31_3_TXP
PCIE4_RXN/USB31_4_RXN
PCIE4_RXP/USB31_4_RXP
PCIE4_TXN/USB31_4_TXN
PCIE4_TXP/USB31_4_TXP
USB2N_1 / USB2P_1
USB2N_2 / USB2P_2
USB2N_3 / USB2P_3
USB2N_4 / USB2P_4
USB2N_5 / USB2P_5
USB2N_6 / USB2P_6
USB2N_7 / USB2P_7
USB2N_8 / USB2P_8
USB2N_9 / USB2P_9
USB2N_10 / USB2P_10
USB2_COMP
USB_ID
USB_VBUSSENSE
GPP_E9/USB2_OC0#/GP_BSSB_CLK
GPP_E10/USB2_OC1#/GP_BSSB_DI
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#
GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2
GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2
GPP_E8/SATALED#/SPI1_CS1#
RSVD#AR3

USB3.1 PORT3	LAN	USB3.1 port1
	WLAN	USB3.1 port3
	CARDREADER	USB3.1 port4
	WWAN	WWAN
	SSD	Type C port 1
		USB3.1 port 3
		USB3.1 port 4
		CAMERA
		WWAN
		USH
		FP
		BT

USB_OC3#, USB_OC2#, USB_OC1#, USB_OC0# — RN1601 SRN10KJ-6-GP — 3D3V_S5_PCH
HDD_DET# — R1605 Do Not Stuff / DV — 3D3V_SUS
m2280_PCIE_SATA# / m3042_PCIE#_SATA — RN1602 SRN10KJ-5-GP — 3D3V_S0
R1607 113R2F-GP, R1608 0R2J-2-GP / DV, R1609 Do Not Stuff
TP1602 Do Not Stuff
R1601 Do Not Stuff, R1602, R1603 Do Not Stuff, R1604 100R2F-L1-GP-U, 100KR2J-GP
PCH_PLTRST#_A, SSD_SCP_PWR_EN_PCH, BT_RADIO_DIS#_PCH

Do Not Stuff

Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

	PCIe Controller 1				PCIe Controller 2				PCIe Controller 3				PCIe Controller 4				
	SATA Port 1 can be mapped to HSIO 12 or 15																
	PCIe Gen3 (6 CLKS)																
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
Canon Lake U PCH-LP	USB3.1 / 3.0 -1	USB3.1 / 3.0 -2	USB3.1 / 3.0 -3	USB3.1 / 3.0 -4	USB3.1 / 3.0 -5	USB3.1 / 3.0 -6	GbE	GbE	GbE	PCIe-10	SATA-0	SATA-1	GbE	GbE	SATA-1*	SATA-2	CNVi
	PCIe-1	PCIe-2	PCIe-3	PCIe-4	PCIe-5	PCIe-6	PCIe-7	PCIe-8	PCIe-9		PCIe-11	PCIe-12	PCIe-13	PCIe-14	PCIe-15	PCIe-16	
	X2 X2				X2 X2				X2 X2				X2 X2				
	X4				X4				X4				X4				
	No Remapping				No Remapping				Intel RST for PCIe Storage Device				Intel RST for PCIe Storage Device				
North Bay 13 Bandon	13 UU (non-TBT)	Type-C Port 1 (gen2)	Type-A Port 1 (gen1)	Type-A Port 2 (gen1)	M.2 3042 (LTE)				LOM	M.2 2230 (WLAN)	SD Reader	M.2 3042 (LTE)	M.2 2280 (PCIe x 4 or SATA SSD)				M.2 2230 (WLAN)
	13 UU (TBT)		Type-A Port 1 (gen1)	Type-A Port 2 (gen1)	M.2 3042 (LTE)	TBT Controller x4			LOM	M.2 2230 (WLAN)	SD Reader	M.2 3042 (LTE)	M.2 2280 (PCIe x 4 or SATA SSD)				M.2 2230 (WLAN)

		USB2.0 (10 ports)									
	Canon Lake U PCH-LP	USB2-1	USB2-2	USB2-3	USB2-4	USB2-5	USB2-6	USB2-7	USB2-8	USB2-9	USB2-10
North Bay 13 Bandon	13 UU (non-TBT)	Type-C Port 1	Type-A Port 1	Type-A Port 2			UF Camera	M.2 3042 (WWAN)	CV2	FPR in PB	M.2 2230 (BT)
	13 UU (TBT)	Type-C Port 1	Type-A Port 1	Type-A Port 2			UF Camera	M.2 3042 (WWAN)	CV2	FPR in PB	M.2 2230 (BT)

[63] m2280_PCIE_SATA#
[24] m3042_PCIE#_SATA
[62] M3042_DEVSLP
[16,63] M2280_DEVSLP
[16,63] M2280_DEVSLP

[88] RECOVERY#
[61] BT_RADIO_DIS#_PCH
[63] SSD_SCP_PWR_EN_PCH
[63] PCH_PLTRST#_A

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(PCIE/SATA/USB)
Size: Custom | Document Number: Fircrest 13" | Rev: X01
Date: Friday, April 19, 2019 | Sheet 18 of 106

Main Func = PCH

[24,40,52,53,54] SIO_SLP_SUS#
[68] SIO_SLP_S5#
[40,51,68] SIO_SLP_S4#
[24,40,51,68] SIO_SLP_S3#
[68] SIO_SLP_A#
[40,54,68,91] SIO_SLP_S0#
[40] SIO_SLP_WLAN#
[40] SIO_SLP_LAN#
[68,99] SYS_RESET#
[24] DSW_PWROK_R
[46] PCH_PWROK
[24] SYS_PWROK_R
[24,99] SIO_PWRBTN#
[24] AC_PRESENT
[24,97] LAN_WAKE#
[24,62] PCH_PCIE_WAKE#
[97] PM_LANPHY_ENABLE
[18,24] RTCRST_ON
[24,64,99] RSMRST#_KBC
[24] ALL_SYS_PWRGD
[33,61,62,91,97] PCH_PLTRST#_RIGHT
[63,99] PCH_PLTRST#_LEFT
[21,24,40,54,91] CPU_C10_GATE#
[3] H_CPUPWRGD
[40] 3.3V_CAM_EN#
[44] AC_DIS_ACP

CPU1K
11 OF 20
GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGOOD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SPL_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#
INPUT3VSEL
Do Not Stuff

PCH_PLTRST# BJ35
SYS_RESET# CN10
PCH_RSMRST#_R BR36
H_CPUPWRGD AR2
VCCST_PWRGD_R BJ2
SYS_PWROK_CPU CR10
PCH_PWROK_R BP31
DSW_PWROK BP30
ME_SUS_PWR_ACK BV34
SUSACK# BY32
PCH_PCIE_WAKE# BU30
LAN_WAKE# BU32
PM_LANPHY_ENABLE BU34
BJ37 SIO_SLP_S0#
BU36 SIO_SLP_S3#
BU27 SIO_SLP_S4#
BT29 SIO_SLP_S5#
BU29 SIO_SLP_SUS#
BT31 SIO_SLP_LAN#
BT30 SIO_SLP_WLAN#
BU37 SIO_SLP_A#
BU28 SIO_PWRBTN#
BU35 AC_PRESENT
BV36 PCH_BATLOW#
BR35 RTC_INTRUDER#
CC37 3.3V_CAM_EN#
CC36 VRALERT#
BT27 INPUT3VSEL

RSMRST#_KBC 0R2J-2-GP 1 R1744 PCH_PLTRST#
SYS_PWROK_R 0R2J-2-GP 1 R1742 SYS_PWROK_CPU
PCH_PWROK 0R2J-2-GP 1 R1743 PCH_PWROK_R
TP1701 Do Not Stuff
TP1702 Do Not Stuff
Reserve Can be remove on EVT .

RSMRST#_KBC NON_DS R1745 0R2J-2-GP
DSW_PWROK_R DS R1738 0R2J-2-GP DSW_PWROK
DS R1739 100KR2F-L1-GP
From EC Control

3D3V_SUS
AC_PRESENT R1723 100KR2F-L1-GP
SIO_SLP_S0# R1733 100KR2F-L1-GP
SYS_RESET# R1726 10KR2F-2-GP
VRALERT# R1735 10KR2F-2-GP
DY SIO_PWRBTN# R1728 Do Not Stuff
LAN LAN_WAKE# R1724 10KR2F-2-GP
PCH_PCIE_WAKE# R1727 1KR2J-1-GP
3.3V_CAM_EN# R1736 100KR2F-L1-GP

SIO_SLP_S3# DX R1737 Do Not Stuff
SIO_SLP_S4# DX R1746 Do Not Stuff
SIO_SLP_SUS# DX R1747 Do Not Stuff
SIO_SLP_LAN# DX R1748 Do Not Stuff
SIO_SLP_WLAN# DX R1749 Do Not Stuff
SIO_SLP_A# DX R1750 Do Not Stuff

3V SELECT STRAP
LOW → 3.3V +/-5%
HIGH → 3.0V +/-5%

SPI Voltage Configu-ration

RSMRST#_KBC
PCH_RSMRST#_R
PCH_PWROK
DSW_PWROK_R
SYS_RESET#
PCH_PLTRST#
DY EC1705 Do Not Stuff
R1713 10KR2F-2-GP
R1709 100KR2F-L1-GP
DY EC1701 Do Not Stuff
DY EC1702 Do Not Stuff
DY EC1703 Do Not Stuff
ED1702 AZ5725-01FDR7G-GP
83.05725.0A0

3D3V_RTC_PCH
R1731 330KR2J-L1-GP
RTC_INTRUDER#

3D3V_SUS
DY R1729 Do Not Stuff
INPUT3VSEL
R1730 4K7R2F-GP

3D3V_SUS
R1725 10KR2F-2-GP
PCH_BATLOW#
DY R1732 Do Not Stuff

CheckList 10K ,Reserve PL for RTC rst test

PCH_PWROK:
pull-up resistance should be in range 1/10th of pull down resistance

3D3V_SUS
C1704 SCD1U16V2KX-3DLGP
1D05V_VCCST
R1740 1KR2J-1-GP
U1702
NC#1 VCC
A
GND Y
ALL_SYS_PWRGD
VCCST_PWRGD
R1741 62R2F-GP
VCCST_PWRGD_R
74LVC1G07GW-GP
73.01G07.0HG
Volatge Level 1V

PCH_PLTRST#
U1701
A VCC
B
GND Y
U74LVC1G08G-AL5-R-GP-U
73.01G08.EHG
2ND = 73.7SZ08.DAH
3D3V_SUS
C1701 SCD1U16V2KX-3DLGP
PCH_PLTRST#_Q
R1708 100KR2F-L1-GP
R1701 0R2J-2-GP PCH_PLTRST#_RIGHT
R1706 0R2J-2-GP PCH_PLTRST#_LEFT

Intel requst set as PDG .

SSD TBT	EC LAN CARDREADER WLAN WWAN TPM ESPI CONN1 ESPI CONN2

D1702
RB751VM-40TE-17-GP
83.R2004.J8F
AC_DIS_ACP
AC_PRESENT
RSMRST#_KBC
3D3V_AUX_S5
R1734 100KR2F-L1-GP
Q1702
2N7002KDW-1-GP
75.27002.F7C

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)
Size: Custom
Document Number: Fircrest 13"
Rev: X01
Date: Thursday, April 18, 2019
Sheet 17 of 106

Main Func = PCH

SPI ROM
[68] SPI_CLK_CPU
[15,68,99] SPI_SI_CPU
[68] SPI_SO_CPU
[15,68,99] SPI_WP_CPU
[15,68] SPI_HOLD_CPU
[68] SPI_CS_CPU_N0
[68] SPI_CS_CPU_N1
[91] SPI_CS_CPU_N2

WLAN
[61] WLAN_CLK_CPU_P
[61] WLAN_CLK_CPU_N
[61] WLAN_CLKREQ_CPU_N

WWAN
[62] WWAN_CLK_CPU_P
[62] WWAN_CLK_CPU_N
[62] WWAN_CLKREQ_CPU_N

LAN
[97] LAN_CLK_CPU_N
[97] LAN_CLK_CPU_P
[97] LAN_CLKREQ_CPU_N

CARD
[33] CARD_CLK_CPU_N
[33] CARD_CLK_CPU_P
[33] CARD_CLKREQ_CPU_N

SSD
[63] SSD_CLK_CPU_N
[63] SSD_CLK_CPU_P
[63] SSD_CLKREQ_CPU_N

ESPI
[24,68] ESPI_IO0
[24,68] ESPI_IO1
[24,68] ESPI_IO2
[24,68] ESPI_IO3
[24,68] ESPI_CS#
[24,68] ESPI_RESET#
[24,68] ESPI_CLK

OTHER
[12,13,99] CPU_SMB_SCL_DDR
[12,13,99] CPU_SMB_SDA_DDR
[15] GPP_C2
[97] SML0_SMBCLK
[97] SML0_SMBDATA
[24] SML1_SMBCLK
[24] SML1_SMBDAT
[15] GPP_C5
[61,63] SUSCLK

[62] WWAN_GPIO_PERST#
[62] WWAN_BB_RST#
[99] XDP_CLK_CPU_N
[99] XDP_CLK_CPU_P
TBT_CLK_CPU_N
TBT_CLK_CPU_P
TBT_CLKREQ_CPU_N
[61] PULSAR_38P4M_REFCLK
[61] CL_CLK
[61] CL_RST#
[61] CL_DATA
[68] RTC_RST#
[15] GPP_B23
[24] ESPI_ALERT#
[24] RTCRST_ON
[33] MEDIACARD_IRQ#
[20,25] RTC_DET#

CPU1E — 5 OF 20
SPI_CLK_CPU CH37 — SPI0_CLK
SPI_SO_CPU CF37 — SPI0_MISO
SPI_SI_CPU CF36 — SPI0_MOSI
SPI_WP_CPU CF34 — SPI0_IO2
SPI_HOLD_CPU CG34 — SPI0_IO3
SPI_CS_CPU_N0 CG36 — SPI0_CS0#
SPI_CS_CPU_N1 CG35 — SPI0_CS1#
SPI_CS_CPU_N2 CH34 — SPI0_CS2#
ISH_LAN# CF20 — GPP_D1/SPI1_CLK/BK1/SBK1
RTC_DET#_2 CG22 — GPP_D2/SPI1_MISO_IO1/BK2/SBK2
WWAN_BB_RST# CF22 — GPP_D3/SPI1_MOSI_IO0/BK3/SBK3
WWAN_GPIO_PERST# CG25 — GPP_D21/SPI1_IO2
MEDIACARD_IRQ# CH23 — GPP_D22/SPI1_IO3
CG20 — GPP_D0/SPI1_CS0#/BK0/SBK0
CL_CLK CH7 — CL_CLK
CL_DATA CH8 — CL_DATA
CL_RST# CH9 — CL_RST#
ESPI_ALERT# BV29 — GPP_A0/RCIN#/TIME_SYNC1
BV28 — GPP_A6/SERIRQ
CK14 MEM_SMBCLK — GPP_C0/SMBCLK
CH15 MEM_SMBDATA — GPP_C1/SMBDATA
CJ15 GPP_C2 — GPP_C2/SMBALERT#
CK14 SML0_SMBCLK — GPP_C3/SML0CLK
CF15 SML0_SMBDATA — GPP_C4/SML0DATA
CG15 GPP_C5 — GPP_C5/SML0ALERT#
CN15 SML1_SMBCLK — GPP_C6/SML1CLK
CM15 SML1_SMBDAT — GPP_C7/SML1DATA
CC34 GPP_B23 — GPP_B23/SML1ALERT#/PCHHOT#
CA29 ESPI_CPU_IO0_R — GPP_A1/LAD0/ESPI_IO0
BY29 ESPI_CPU_IO1_R — GPP_A2/LAD1/ESPI_IO1
BY27 ESPI_CPU_IO2_R — GPP_A3/LAD2/ESPI_IO2
BV27 ESPI_CPU_IO3_R — GPP_A4/LAD3/ESPI_IO3
CA28 ESPI_CS# — GPP_A5/LFRAME#/ESPI_CS#
CA27 ESPI_RESET# — GPP_A14/SUS_STAT#/ESPI_RESET#
BV32 ESPI_CPU_CLK_R — GPP_A9/CLKOUT_LPC0/ESPI_CLK
BV30 — GPP_A10/CLKOUT_LPC1
BY30 CLKRUN# — GPP_A8/CLKRUN#
Do Not Stuff
Do Not Stuff

teknisi indonesia

3D3V_S0
RN1803 SRN2K2J-1-GP
MEM_SMBDATA — Q1803 2N7002KDW-1-GP — CPU_SMB_SDA_DDR
75.27002.F7C
MEM_SMBCLK — CPU_SMB_SCL_DDR

ESPI_CPU_CLK_R — R1834 33R2F-3-GP — ESPI_CLK
ESPI_CPU_IO0_R — R1835 15R2F-2-GP — ESPI_IO0
ESPI_CPU_IO1_R — R1836 15R2F-2-GP — ESPI_IO1
ESPI_CPU_IO2_R — R1838 15R2F-2-GP — ESPI_IO2
ESPI_CPU_IO3_R — R1850 15R2F-2-GP — ESPI_IO3
Intel requst set as PDG .

ESPI Interface Checklist

Pin Name	System Pull-up/ Pull-down	Schematics Notes
ESPI_CLK ESPI_IO[3:0]		15 Ω series resistor, placed near the driver for Data 33Ω series resistor for Clock placed near the Driver. Note that ESPI_CLK# and ESPI_RESET# do not require series resistors.

RF Reserve
ESPI_CLK — DY — FC1802 Do Not Stuff

R1821 10KR2J-3-GP — 1D8V_VCCPRIM — ESPI_ALERT#
SERIRQ PH:
PDG: 8.2k
CRB: 10k

3D3V_LAN
SML0_SMBCLK R1802 DY Do Not Stuff
SML0_SMBDATA R1812 DY Do Not Stuff

3D3V_S5_PCH
SML0_SMBCLK R1807 499R2F-2-GP
SML0_SMBDATA R1808 499R2F-2-GP
SML1_SMBCLK — RN1804 SRN1KJ-7-GP
SML1_SMBDAT
MEM_SMBCLK — RN1806 SRN1KJ-7-GP
MEM_SMBDATA

3D3V_S0
CLKRUN# R1810 DY Do Not Stuff
SPI_CLK_CPU R1809 100KR2F-L-GP
ESPI_RESET# R1813 DY Do Not Stuff
ESPI_CS# R1814 DY Do Not Stuff

3D3V_S5_PCH
BAYDON R1818 100KR2F-L-GP — ISH_LAN#
NORTHBAY R1819 100KR2F-L-GP

3D3V_RTC_PCH
RN1802 SRN20KJ-1-GP
C1801 SC1U10V2KX-1DLGP
SRTC_RST#
RTC_RST#
G1802 Do Not Stuff
C1802 SC1U10V2KX-1DLGP

RTC_DET# — R1843 0R2J-2-GP — RTC_DET#_2

CPU1J — 10 OF 20
R1842 0R2J-2-GP — LAN_CLK_CPU_N AW2 — LAN_CLKREQ_CPU_N
LAN_CLK_CPU_P AY3
CLKREQ_PCIE#0 CF32
CLKOUT_PCIE_N0 — LAN
CLKOUT_PCIE_P0
GPP_B5/SRCCLKREQ0#
R1845 0R2J-2-GP — CARD_CLK_CPU_N BC1 — CARD_CLKREQ_CPU_N
CARD_CLK_CPU_P BC2
CLKREQ_PCIE#1 CE32
CLKOUT_PCIE_N1 — CARDREADER
CLKOUT_PCIE_P1
GPP_B6/SRCCLKREQ1#
R1847 0R2J-2-GP — WLAN_CLK_CPU_N BD3 — WLAN_CLKREQ_CPU_N
WLAN_CLK_CPU_P BC3
CLKREQ_PCIE#2 CF30
CLKOUT_PCIE_N2 — WLAN
CLKOUT_PCIE_P2
GPP_B7/SRCCLKREQ2#
R1848 0R2J-2-GP — WWAN_CLK_CPU_N BH3 — WWAN_CLKREQ_CPU_N
WWAN_CLK_CPU_P BH4
CLKREQ_PCIE#3 CE31
CLKOUT_PCIE_N3 — WWAN
CLKOUT_PCIE_P3
GPP_B8/SRCCLKREQ3#
R1849 0R2J-2-GP — SSD_CLK_CPU_N BA1 — SSD_CLKREQ_CPU_N
SSD_CLK_CPU_P BA2
CLKREQ_PCIE#4 CE30
CLKOUT_PCIE_N4 — SSD
CLKOUT_PCIE_P4
GPP_B9/SRCCLKREQ4#
R1851 0R2J-2-GP — TBT_CLK_CPU_N BE1 — TBT_CLKREQ_CPU_N
TBT_CLK_CPU_P BE2
CLKREQ_PCIE#5 CF31
CLKOUT_PCIE_N5 — TBT
CLKOUT_PCIE_P5
GPP_B10/SRCCLKREQ5#
Do Not Stuff
Do Not Stuff

CLKOUT_ITPXDP_N AU1 — XDP_CLK_CPU_N
CLKOUT_ITPXDP_P AU2 — XDP_CLK_CPU_P
GPD8/SUSCLK BT32 — SUSCLK
XTAL_IN CK3 — XTL_24M_X1_CPU
XTAL_OUT CK2 — XTL_24M_X2_CPU
XCLK_BIASREF CJ1 — PULSAR_38P4M_REFCLK_CPU — R1823 60D4R2F-GP
CLKIN_XTAL CM3
RTCX1 BN31 — XTL_32K_X1_CPU
RTCX2 BN32 — XTL_32K_X2_CPU
SRTCRST# BR37 — SRTC_RST#
RTCRST# BR34 — RTC_RST#

XTL_32K_X2_CPU
XTL_32K_X1_CPU — R1815 10MR2J-L-GP
X1802 XTAL-32D768KHZ-98-GP 082.30003.0301
C1804 SC12P50V2JN-DL-GP
C1803 SC12P50V2JN-DL-GP

PULSAR_38P4M_REFCLK_CPU — R1853 0R2J-2-GP — PULSAR_38P4M_REFCLK
R1825 10KR2J-3-GP

RTCRST_ON — R1844 0R2J-2-GP — RTCRST_ON_Q — Q1802 2N7002K-2-GP 84.2N702.J31 — RTC_RST#_R — R1852 75R2F-2-GP — RTC_RST#
R1846 100KR2F-L-GP
ARD 0.85

3D3V_S0
RN1805 SRN10KJ-6-GP
CARD_CLKREQ_CPU_N
WWAN_CLKREQ_CPU_N
WLAN_CLKREQ_CPU_N
LAN_CLKREQ_CPU_N
R1822 10KR2F-2-GP — SSD_CLKREQ_CPU_N
R1824 10KR2F-2-GP — TBT_CLKREQ_CPU_N
DY R1817 Do Not Stuff — SUSCLK

XTL_24M_X1_CPU — R1839 33R2F-3-GP — XTL_24M_X1_R — C1807 SC15P50V2JN-DL-GP
R1841 200KR2F-L-GP — X1801 XTAL-24MHZ-189-GP 082.30006.0571
XTL_24M_X2_CPU — R1840 33R2F-3-GP — XTL_24M_X2_R — C1808 SC15P50V2JN-DL-GP

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPC/SPI/SMBUS/CL/CLK)
Size: A3 | Document Number: Fircrest 13" | Rev: X01
Date: Thursday, April 18, 2019 | Sheet 18 of 106

Main Func = PCH

[27] HDA_SDI0
[27] HDA_SDOUT_CODEC
[27] HDA_SYNC_CODEC
[27] HDA_BITCLK_CODEC
[15] HDA_SDO

[66] CONTACTLESS_DET#
[56] CAM_MIC_CBL_DET#
[29] SPK_DET#
[33] HOST_SD_WP#
[27] AUD_PWR_EN
[88] H1_PCH_INT#_BUFF_D
[68] ME_FWP_PCH
[15,27] SPKR
[61] CLKREQ_CNV
[61] CNV_RF_RESET#
[65] KB_DET#
[62] WWAN_GPIO_WAKE#
TBT_CIO_PLUG_EVENT#
[56] DMIC_SDA_CODEC_CPU
[56] DMIC_SCL_CODEC_CPU
[62] ANT_CONFIG

[61] CNV_EN
[27] HDA_RST#

HDA_SYNC_CODEC 1 R1915 33R2F-3-GP 2 HDA_SYNC BN34
HDA_BITCLK_CODEC 1 R1914 33R2F-3-GP 2 HDA_BCLK BN37
HDA_SDOUT_CODEC 1 R1916 33R2F-3-GP 2 HDA_SDO BN36
HDA_SDI0 BN35
BL36
HDA_RST# BL35
WWAN_GPIO_WAKE# CK23
BL37
BL34
CNV_RF_RESET# CJ32
CH32
CLKREQ_CNV_R CH29
CNV_EN CH30
GPP_D19 CP24
GPP_D20 CN24
KB_DET# CK25
H1_PCH_INT#_BUFF_D CJ25
SPKR CF35

CPU1G 7 OF 20

HDA_SYNC/I2S0_SFRM
HDA_BCLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD/SNDW1_DATA
HDA_RST#/I2S1_SCLK/SNDW1_CLK
GPP_D23/I2S_MCLK
I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA
GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO
GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_D20/DMIC_DATA0/SNDW4_DATA
GPP_D17/DMIC_CLK1/SNDW3_CLK
GPP_D18/DMIC_DATA1/SNDW3_DATA
GPP_B14/SPKR

GPP_G0/SD_CMD
GPP_G1/SD_DATA0
GPP_G2/SD_DATA1
GPP_G3/SD_DATA2
GPP_G4/SD_DATA3
GPP_G5/SD_CD#
GPP_G6/SD_CLK
GPP_G7/SD_WP
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
GPP_A16/SD_1P8_SEL
SD_1P8_RCOMP
SD_3P3_RCOMP

CH36 CAM_MIC_CBL_DET#
CL35 ANT_CONFIG
CL36 TBT_CIO_PLUG_EVENT#
CM35
CN35 CONTACTLESS_DET#
CH35 HOST_SD_WP#
CK36 AUD_PWR_EN
CK34 SPK_DET#
BW36
BY31
CK33 SD3_RCOMP
CM34
R1916 200R2F-L-GP 1 2

Do Not Stuff
Do Not Stuff

3D3V_S0
R1908 1 100KR2F-L-GP 2 AUD_PWR_EN
R1909 1 10KR2F-2-GP 2 HOST_SD_WP#
R1911 1 10KR2F-2-GP 2 CONTACTLESS_DET#

3D3V_SUS
R1903 1 100KR2F-L-GP 2 KB_DET#

3D3V_S0
R1910 1 100KR2F-L-GP 2 CAM_MIC_CBL_DET#

GPIO0.5 change to 1.8V

HDA_BCLK
DY EC1901 Do Not Stuff

3D3V_S5_PCH
R1913 1 10KR2F-2-GP 2 TBT_CIO_PLUG_EVENT#
VCC3P3_SX
R1917 1 DY Do Not Stuff 2

R1905 Do Not Stuff
DMIC_SDA_CODEC_CPU DY 2 GPP_D20
R1906 Do Not Stuff
DMIC_SCL_CODEC_CPU DY 2 GPP_D19

Reserve for Dmic connect to PCH

R1912 33R2F-3-GP
CLKREQ_CNV_R 1 2 CLKREQ_CNV

R1901 1 WIN 2 0R1J-GP
D1901
ME_FWP_PCH A K ME_FWP_PCH_D 1
GD RB751S40T1G-GP
R1904 2 HDA_SDO
2K2R2J-2-GP

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(AUDIO/SDIO/SDXC)
Size: A4 | Document Number: Fircrest 13" | Rev: X01
Date: Thursday, April 18, 2019 | Sheet 19 of 106

Main Func = PCH

[68] CPU_UART2_TXD
[68] CPU_UART2_RXD
[55] CPU_I2C_SDA_TS
[55] CPU_I2C_SCL_TS
[65] CPU_I2C_SDA_TP
[65] CPU_I2C_SCL_TP
[69,70] CPU_I2C_SDA_SENSOR
[69,70] CPU_I2C_SCL_SENSOR
[62] CPU_I2C_SDA_GNSS
[62] CPU_I2C_SCL_GNSS
[69] GSEN_INT1
[70] LNG2DMTR_INT1
[24] NB_MODE#
[24] LID_CL#_NB_R
[24] LID_CL#_TAB_R
[15,20] NRB_BIT
[91] TPM_PIRQ#
[40] PCH_3.3V_TS_EN
[15] GPP_B22
[55] TS_INT#
[24] SIO_EXT_WAKE#
[55] LCD_CBL_DET#
[61] CNV_BRI_RSP
[15,61] CNV_RGI_DT
[61] CNV_BRI_DT
[61] CNV_RGI_RSP
[15,20] NRB_BIT
[15] GPP_D12
[56] IR_CAM_DET#
[62] WWAN_FULL_PWR_EN_R
[54] PRIM_CORE_OPT_DIS
[18,25] RTC_DET#
[88] I2C4_SDA_H1
[88] I2C4_SCL_H1
[20,68] H1_BOOT_UART_RX_R
[20,68] H1_BOOT_UART_TX_R

CPU1F — 6 OF 20

PRIM_CORE_OPT_DIS CC27 — GPP_B15/GSPI0_CS0#
CC32 — GPP_A7/PIRQA#/GSPI0_CS1#
ONE_DIMM# CE28 — GPP_B16/GSPI0_CLK
RTC_DET#_1 CE27 — GPP_B17/GSPI0_MISO
NRB_BIT CE29 — GPP_B18/GSPI0_MOSI
TP2003 Do Not Stuff — HDD_FALL_INT CA31 — GPP_B19/GSPI1_CS0#
CA32 — GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#
TPM_PIRQ# CC29 — GPP_B20/GSPI1_CLK
PCH_3.3V_TS_EN CC30 — GPP_B21/GSPI1_MISO
GPP_B22 CA30 — GPP_B22/GSPI1_MOSI
CNV_BRI_PRX_DTX CK20 — GPP_F5/CNV_BRI_RSP
CNV_RGI_PTX_DRX CG19 — GPP_F6/CNV_RGI_DT
CNV_BRI_PTX_DRX CJ20 — GPP_F4/CNV_BRI_DT
CNV_RGI_PRX_DTX CH19 — GPP_F7/CNV_RGI_RSP
CPU_UART2_RXD CR12 — GPP_C20/UART2_RXD
CPU_UART2_TXD CP12 — GPP_C21/UART2_TXD
CN12 — GPP_C22/UART2_RTS#
TS_INT# CM12 — GPP_C23/UART2_CTS#
TS — TS_I2C_SDA CM11 — GPP_C16/I2C0_SDA
TS_I2C_SCL CN11 — GPP_C17/I2C0_SCL
TP — I2C1_SDA_TP CK12 — GPP_C18/I2C1_SDA
I2C1_SCK_TP CJ12 — GPP_C19/I2C1_SCL
ALS — CF27 — GPP_H4/I2C2_SDA
CF29 — GPP_H5/I2C2_SCL
ANT — CH27 — GPP_H6/I2C3_SDA
CH28 — GPP_H7/I2C3_SCL
H1 — I2C4_SDA_H1 CJ30 — GPP_H8/I2C4_SDA
I2C4_SCL_H1 CJ31 — GPP_H9/I2C4_SCL
Do Not Stuff

GPP_D9/ISH_SPI_CS#/GSPI2_CS0# — CN22 IR_CAM_DET#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK — CR22
GPP_D11/ISH_SPI_MISO/GSPI2_MISO — CM22 TBT_DET#
GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI — CP22 GPP_D12
GPP_D5/ISH_I2C0_SDA — CK22 ISH_I2C0_SDA
GPP_D6/ISH_I2C0_SCL — CH20 ISH_I2C0_SCL
SENSOR
GPP_D7/ISH_I2C1_SDA — CH22
GPP_D8/ISH_I2C1_SCL — CJ22
ALS
GPP_H10/I2C5_SDA/ISH_I2C2_SDA — CJ27 ISH_I2C2_SDA
GPP_H11/I2C5_SCL/ISH_I2C2_SCL — CJ29 ISH_I2C2_SCL
WWAN
GPP_D13/ISH_UART0_RXD — CM24 ISH_CPU_UART0_RX — R2018 1 DY — Do Not Stuff H1_BOOT_UART_RX_R
GPP_D14/ISH_UART0_TXD — CN23 ISH_CPU_UART0_TX — R2027 1 DY — Do Not Stuff H1_BOOT_UART_TX_R
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1# — CM23 WWAN_FULL_PWR_EN — R2051 1 — 0R2J-2-GP — WWAN_FULL_PWR_EN_R
GPP_D16/ISH_UART0_CTS#/SML0BALERT# — CR24
GPP_C12/UART1_RXD/ISH_UART1_RXD — CG12 SIO_EXT_WAKE#
GPP_C13/UART1_TXD/ISH_UART1_TXD — CH12 GPP_C13 — 1 TP2007 Do Not Stuff
GPP_C14/UART1_RTS#/ISH_UART1_RTS# — CF12 LCD_CBL_DET#
GPP_C15/UART1_CTS#/ISH_UART1_CTS# — CG14 PCH_HDD_EN — 1 TP2006 Do Not Stuff
GPP_A18/ISH_GP0 — BW35 ISH_ACC1_INT# — R2047 1 — 0R2J-2-GP — GSEN_INT1
GPP_A19/ISH_GP1 — BW34 ISH_ACC2_INT# — R2042 1 — 0R2J-2-GP — LNG2DMTR_INT1
ACC_SENSOR_BD
GPP_A20/ISH_GP2 — CA37
GPP_A21/ISH_GP3 — CA36
ACC_MB
GPP_A22/ISH_GP4 — CA35 ISH_NB_MODE
GPP_A23/ISH_GP5 — CA34 ISH_LID_CL#_NB — R2057 1 — 0R2J-2-GP — LID_CL#_NB_R
GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF# — BW37 ISH_LID_CL#_TAB — R2058 1 — 0R2J-2-GP — LID_CL#_TAB_R

Do Not Stuff

3D3V_SUS
R2001 1 — 10KR2F-2-GP — SIO_EXT_WAKE#
R2003 1 — 49K9R2F-L-GP — CPU_UART2_RXD
R2005 1 — 49K9R2F-L-GP — CPU_UART2_TXD
DEBUG

3D3V_S0
R2016 1 — 100KR2F-L1-GP — IR_CAM_DET#
R2021 1 — 100KR2F-L1-GP — LID_CL#_NB_R
R2020 1 — 10KR2F-2-GP — LID_CL#_TAB_R
R2002 1 — 100KR2F-L1-GP — PCH_3.3V_TS_EN
R2007 1 — 100KR2F-L1-GP — LCD_CBL_DET#
R2004 DY — Do Not Stuff — CPU_UART2_RXD
R2006 DY — Do Not Stuff — CPU_UART2_TXD
RN2004 — 1 GSEN_INT1, 2 7, 3 6, 4 5, 8 LNG2DMTR_INT1
SRN10KJ-6-GP

CNV_BRI_PRX_DTX R2028 1 — 22R2J-2-GP — CNV_BRI_RSP
CNV_RGI_PTX_DRX R2029 1 — 33R2F-3-GP — CNV_RGI_DT
CNV_BRI_PTX_DRX R2030 1 — 33R2F-3-GP — CNV_BRI_DT
CNV_RGI_PRX_DTX R2035 1 — 22R2J-2-GP — CNV_RGI_RSP

RTC_DET# — R2026 Do Not Stuff DY — 2 RTC_DET#_1

3D3V_SUS
BANDON
R2010 10KR2F-2-GP
NB_MODE# — Q2002 2N7002KDW-1-GP 75.27002.F7C — NB_MODE_Q
ISH_NB_MODE — R2017 100KR2F-L1-GP
R2038 Do Not Stuff DY — ISH_NB_MODE — NB_MODE#

3D3V_SUS
BANDON
R2019 100KR2F-L1-GP
NB_MODE#
NORTHBAY
R2009 10KR2F-2-GP

Check final GPIO group , if connect to 3.3V group can reserve Q2002 .

3D3V_S0
RN2002 SRN2K2J-1-GP
R2014 0R2J-2-GP — TS_I2C_SDA — CPU_I2C_SDA_TS
R2015 0R2J-2-GP — TS_I2C_SCL — CPU_I2C_SCL_TS
R2025 0R2J-2-GP — I2C1_SDA_TP — CPU_I2C_SDA_TP
R2024 0R2J-2-GP — I2C1_SCK_TP — CPU_I2C_SCL_TP

1D8V_S5
RN2006 Do Not Stuff DY
R2022 Do Not Stuff DY — ISH_I2C2_SDA — CPU_I2C_SDA_GNSS
R2023 Do Not Stuff DY — ISH_I2C2_SCL — CPU_I2C_SCL_GNSS
R2032 0R2J-2-GP — CPU_I2C_SDA_SENSOR — ISH_I2C0_SDA
R2031 0R2J-2-GP — CPU_I2C_SCL_SENSOR — ISH_I2C0_SCL

3D3V_S0
DY
R2013 Do Not Stuff
ONE_DIMM#
R2011 10KR2F-2-GP

DIMM Dectect	
HIGH	1 DIMM
LOW	2 DIMM

3D3V_SUS
NON_TBT
R2008 10KR2F-2-GP
TBT_DET#
TBT
R2012 10KR2F-2-GP

TBT_DET# Dectect	
HIGH	NON TBT
LOW	TBT

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPSS/ISH)
Size: A3 | Document Number: Fircrest 13" | Rev: X01
Date: Thursday, April 18, 2019 | Sheet 20 of 106

Main Func = PCH

[61] CNV_WR_DN0
[61] CNV_WR_DP0
[61] CNV_WR_DN1
[61] CNV_WR_DP1
[61] CNV_WR_CLKN
[61] CNV_WR_CLKP
[61] CNV_WT_DN0
[61] CNV_WT_DP0
[61] CNV_WT_DN1
[61] CNV_WT_DP1
[61] CNV_WT_CLKN
[61] CNV_WT_CLKP
[61,62] CNV_COEX3
[62,68] SBIOS_TX
[24,40,54,91] CPU_C10_GATE#
TBT_FORCE_PWR
PCH_TBT_PERST#
[61,62] CNV_MFUART2_TXD
[61,62] CNV_MFUART2_RXD
[15] GPP_H21
[15] GPP_H23
[15] GPD_7
TBT_RTD3_WAKE#
RTD3_CIO_PWR_EN

CPU1I

CNV_WR_DN0 CR30 → CNV_WR_D0N
CNV_WR_DP0 CP30 → CNV_WR_D0P
CNV_WR_DN1 CM30 → CNV_WR_D1N
CNV_WR_DP1 CN30 → CNV_WR_D1P
CNV_WT_DN0 CN32 → CNV_WT_D0N
CNV_WT_DP0 CM32 → CNV_WT_D0P
CNV_WT_DN1 CP33 → CNV_WT_D1N
CNV_WT_DP1 CN33 → CNV_WT_D1P
CNV_WR_CLKN CN31 → CNV_WR_CLKN
CNV_WR_CLKP CP31 → CNV_WR_CLKP
CNV_WT_CLKN CP34 → CNV_WT_CLKN
CNV_WT_CLKP CN34 → CNV_WT_CLKP
R2102 150R2F-1-GP
CNV_WT_RCOMP CP32 → CNV_WT_RCOMP#CP32
CR32 → CNV_WT_RCOMP#CR32
CNV_COEX3 CP20 → GPP_F0/CNV_PA_BLANKING
CK19 → GPP_F1
CG17 → GPP_F2
PCH_TBT_PERST# CR14 → GPP_C8/UART0_RXD
SBIOS_TX CP14 → GPP_C9/UART0_TXD
TYPEC_CON_SEL1 CN14 → GPP_C10/UART0_RTS#
TYPEC_CON_SEL2 CM14 → GPP_C11/UART0_CTS#
CNV_COEX1 CJ17 → GPP_F8/CNV_MFUART2_RXD
CNV_COEX2 CH17 → GPP_F9/CNV_MFUART2_TXD
CF17 → GPP_F23/A4WP_PRESENT

WLAN (CNVI)

9 OF 20

CN27 CPU_C10_GATE# ← GPP_H18/CPU_C10_GATE#
CM27 ← GPP_H19/TIMESYNC0
CF25 GPP_H21 ← GPP_H21
CN26 RTD3_CIO_PWR_EN ← GPP_H22
CM26 GPP_H23 ← GPP_H23
CK17 ← GPP_F10
R2110 0R2J-2-GP
BV35 GPD_7 ← GPD7
CN20 ← GPP_F3
TBT_RTD3_WAKE#
CG25 TBT_FORCE_PWR ← GPP_D4/IMGCLKOUT0/BK4/SBK4
CH25 ← GPP_H20/IMGCLKOUT1
CR20 ← GPP_F12/EMMC_DATA0
CM20 ← GPP_F13/EMMC_DATA1
CN19 ← GPP_F14/EMMC_DATA2
CM19 ← GPP_F15/EMMC_DATA3
CN18 ← GPP_F16/EMMC_DATA4
CR18 ← GPP_F17/EMMC_DATA5
CP18 ← GPP_F18/EMMC_DATA6
CM18 ← GPP_F19/EMMC_DATA7
CM16 ← GPP_F20/EMMC_RCLK
CP16 ← GPP_F21/EMMC_CLK
CR16 ← GPP_F11/EMMC_CMD
CN16 ← GPP_F22/EMMC_RESET#
CK15 EMMC_RCOMP ← EMMC_RCOMP
R2104 200R2F-L-GP

Do Not Stuff

3D3V_S5_PCH
R2111 Do Not Stuff
3D3V_S0
CPU_C10_GATE#
R2103 Do Not Stuff

Do Not Stuff

R2108 Do Not Stuff CNV_COEX2 → CNV_MFUART2_TXD
R2109 Do Not Stuff CNV_COEX1 → CNV_MFUART2_RXD

3D3V_S0
R2105 Do Not Stuff
TYPEC_CON_SEL1
R2106 10KR2F-2-GP

3D3V_S0
R2101 Do Not Stuff
TYPEC_CON_SEL2
R2107 10KR2F-2-GP

Vendor	JAE	FOXCON	TBD	TBD
TYPEC_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPEC_CON_SEL2	LOW	HIGH	LOW	HIGH

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER1)
Size: A4
Document Number: Fircrest 13"
Rev: X01
Date: Thursday, April 18, 2019
Sheet 21 of 106

Main Func = PCH

[54] PRIMCORE_G0
[54] PRIMCORE_G1

CPU1P — 16 OF 20

1D05V_VCCPRIM	BP20	VCCPRIM_1P05	
	BW16	VCCPRIM_1P05	
	BW18	VCCPRIM_1P05	
	BW19	VCCPRIM_1P05	
	BY16	VCCPRIM_1P05	
	CA14	VCCPRIM_1P05	
1D8V_VCCPRIM	CC15	VCCPRIM_1P8	
	CD15	VCCPRIM_1P8	
	CD16	VCCPRIM_1P8	
	CP17	VCCPRIM_1P8	
3D3V_VCCPRIM	CB22	VCCPRIM_3P3	
	CB23	VCCPRIM_3P3	
	CC22	VCCPRIM_3P3	
	CC23	VCCPRIM_3P3	
	CD22	VCCPRIM_3P3	
	CD23	VCCPRIM_3P3	
	CP29	VCCPRIM_3P3	
1D05V_VCCPRIM_CORE	BU15	VCCPRIM_CORE	
	BU22	VCCPRIM_CORE	
	BV15	VCCPRIM_CORE	
	BV16	VCCPRIM_CORE	
	BV18	VCCPRIM_CORE	
	BV19	VCCPRIM_CORE	
	BV20	VCCPRIM_CORE	
	BV22	VCCPRIM_CORE	
	BW20	VCCPRIM_CORE	
	BW22	VCCPRIM_CORE	
	CA12	VCCPRIM_CORE	
	CA16	VCCPRIM_CORE	
	CA18	VCCPRIM_CORE	
	CA19	VCCPRIM_CORE	
	CA20	VCCPRIM_CORE	
	CB12	VCCPRIM_CORE	
	CB14	VCCPRIM_CORE	
	CB15	VCCPRIM_CORE	
1D05V_VCCDSW	BT24	VCCDSW_1P05	
1D05V_VCCPRIM	BU14	VCCAPLL_1P05	
1D05V_VCCMPHYGTAON	BV12	VCCPRIM_MPHY_1P05	
	BW12	VCCPRIM_MPHY_1P05	
	BW14	VCCPRIM_MPHY_1P05	
	BV12	VCCPRIM_MPHY_1P05	
	BV14	VCCPRIM_MPHY_1P05	
1D05V_VCCAMPHYPLL	BV2	VCCAMPHYPLL_1P05	
1D05V_VCCPRIM	BR15	VCCAPLL_1P05	
1D05V_VCCPRIM	CC12	VCCDUSB_1P05	
3D3V_SUS	BR24	VCCDSW_3P3	
3D3V_VCCPRIM	BT20	VCCHDA	
3D3V_VCCPRIM	BV23	VCCSPI	
1D05V_VCCPRIM	BT18	VCCPRIM_1P05	
	BT19	VCCPRIM_1P05	
	BU18	VCCPRIM_1P05	
	BU19	VCCPRIM_1P05	
1D05V_VCCPRIM	BT22	VCCPRIM_1P05	
	BP22	VCCPRIM_1P05	
1D05V_VCCMPHYGTAON	BV14	VCCPRIM_MPHY_1P05	

VCCPRIM_3P3	CB16	3D3V_VCCPRIM	
VCCRTC	BR23	3D3V_RTC_PCH	
VCCPRIM_1P05	BY20	1D05V_VCCPRIM	
DCPRTC	BP24	VCCRTCEXT	
VCCPRIM_1P05	BR20	1D05V_VCCPRIM	
VCCAPLL_1P05	BT12	1D05V_VCCPRIM	
VCCA_BCLK_1P05	BP14	1D05V_VCCPRIM	
VCCAPLL_1P05	BR14	1D05V_VCCPRIM	
VCCA_SRC_1P05	BU12	1D05V_VCCPRIM	
VCCA_XTAL_1P05	CP5	1D05V_VCCA_XTAL	
VCCDPHY_1P24	BY24	1D24V_VCCDPHY	
VCCDPHY_1P24	CA24		
VCCDPHY_1P24	BY23		
VCCDPHY_1P24	CA23		
VCCDPHY_1P24	CP25	1D24V_VCCDPHY_EC	
VCCDSW_3P3	BT23	3D3V_SUS	
VCCA_19P2_1P05	BR12	1D05V_VCCPRIM	
VCCPRIM_1P8	CC18	1D8V_VCCPRIM	
VCCPRIM_1P8	CC19		
VCCPRIM_1P8	CD18		
VCCPRIM_1P8	CD19		
VCCPRIM_1P8	CP23		
VCCPRIM_3P3	BW23	3D3V_VCCPRIM	
VCCPRIM_3P3	BP23	3D3V_VCCPRIM	
GPP_B0/CORE_VID0	CB36	PRIMCORE_G0	
GPP_B1/CORE_VID1	CB35	PRIMCORE_G1	

Do Not Stuff

Do Not Stuff

CPU1O — 15 OF 20 — WHL QS/CFL U/WHL ES1_CNL U22

K12	RSVD#K12	RSVD#AA24	AA24
K14	RSVD#K14	RSVD#AA26	AA26
K15	RSVD#K15	RSVD#AB25	AB25
K17	RSVD#K17	RSVD#AC24	AC24
K18	RSVD#K18	RSVD#AC25	AC25
K20	RSVD#K20	RSVD#AC26	AC26
L25	RSVD#L25	RSVD#AD24	AD24
M24	RSVD#M24	RSVD#AD26	AD26
M26	RSVD#M26	RSVD#V25	V25
P24	RSVD#P24	RSVD#T25	T25
P26	RSVD#P26	RSVD#A35	A35
R24	RSVD#R24	RSVD#D34	D34
R25	RSVD#R25	RSVD#N5	N5
R26	RSVD#R26		
V24	RSVD#V24		
W25	RSVD#W25		
Y24	RSVD#Y24		
Y25	RSVD#Y25		
G2	RSVD#G2		
G1	RSVD#G1		
C34	RSVD#C34		
G3	RSVD#G3		
G4	RSVD#G4		
A34	RSVD#A34		
B35	RSVD#B35		
AJ27	RSVD#AJ27		
AH26	RSVD#AH26		
L5	RSVD#L5		

Do Not Stuff

Do Not Stuff

2mA

1D05V_VCCPRIM — R2201 D01R3F-L-GP — 1D05V_VCCA_XTAL

1D05V_VCCA_XTAL — C2201 SC1U10V2KX-1DLGP — C2202 SC22U6D3V3MX-1-DL-GP

Layout Note:
R2202 near CP5

702mA

1D8V_S5 — R2202 D01R3F-L-GP — 1D8V_VCCPRIM

1D8V_VCCPRIM — C2203 SC1U10V2KX-1DLGP — C2204 DY Do Not Stuff — R2203 DY Do Not Stuff

823mA

3D3V_S5_PCH — R2204 D01R3F-L-GP — 3D3V_VCCPRIM

3D3V_VCCPRIM — C2205 DY Do Not Stuff — R2205 DY Do Not Stuff — C2206 DY Do Not Stuff — C2207 DY Do Not Stuff

152mA

1D05V_S5 — R2206 D01R3F-L-GP — 1D05V_VCCAMPHYPLL

2063mA

1D05V_VCCMPHYGTAON — R2208 D01R3F-L-GP

1625mA

1D05V_VCCPRIM — R2209 D01R3F-L-GP

1D05V_VCCAMPHYPLL — C2208 SC1U10V2KX-1DLGP — C2209 DY Do Not Stuff

Layout Note:
22uF:
C2209 near BV2

1D05V_VCCMPHYGTAON — C2210 SC22U6D3V3MX-1-DL-GP

1D05V_VCCPRIM — C2211 SC1U10V2KX-1DLGP — R2207 DY Do Not Stuff

1D05V_VCCPRIM_CORE — C2213 DY Do Not Stuff

1D05V_VCCDSW — C2214 SC1U10V2KX-1DLGP

3D3V_SUS — C2215 DY Do Not Stuff

3D3V_RTC_PCH — C2216 SC1U10V2KX-1DLGP — C2212 SCD1U16V2KX-3DLGP

VCCRTCEXT — C2217 DY Do Not Stuff

1D24V_VCCDPHY_EC — C2218 SC4D7U6D3V2KX-GP-U

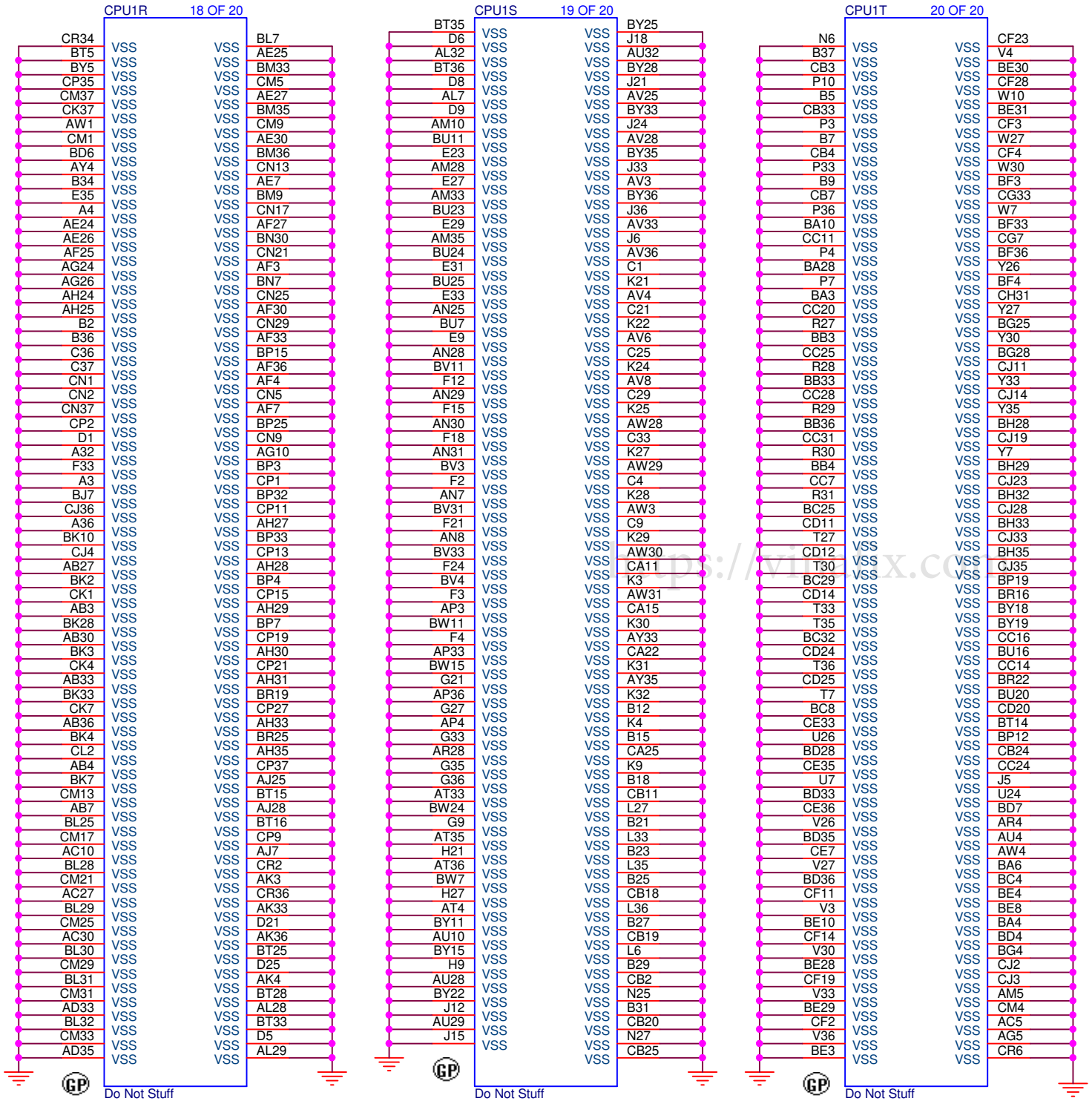
ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

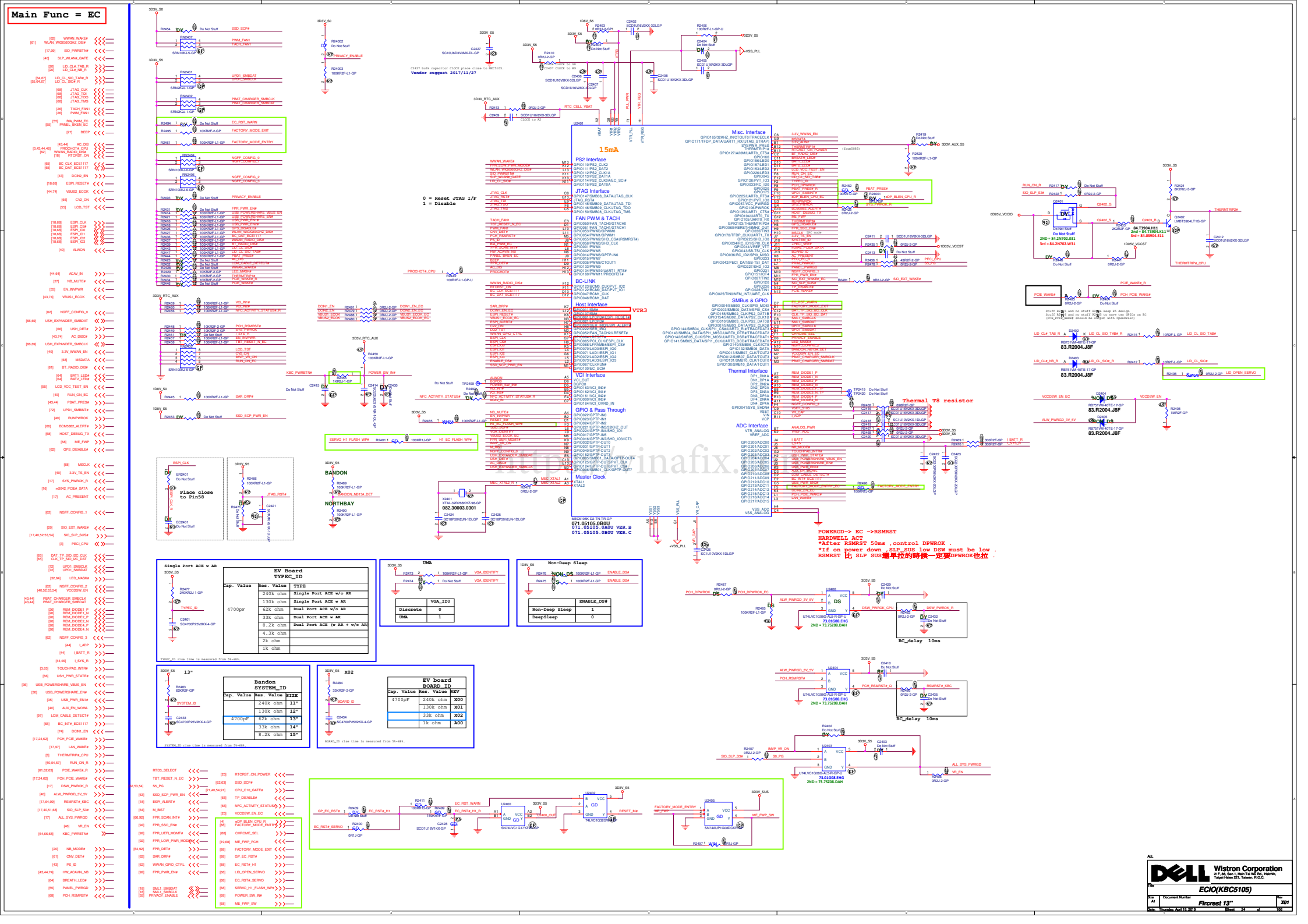
Title: CPU_(RSVD)

Size: A3 | Document Number: Fircrest 13" | Rev: X01

Date: Thursday, April 18, 2019 | Sheet 22 of 106


CPU1R 18 OF 20
CR34 BT5 BY5 CP35 CM37 CK37 AW1 CM1 BD6 AY4 B34 E35 A4 AE24 AE26 AF25 AG24 AG26 AH24 AH25 B2 B36 C36 C37 CN1 CN2 CN37 CP2 D1 A32 F33 A3 BJ7 CJ36 A36 BK10 CJ4 AB27 BK2 CK1 AB3 BK28 AB30 BK3 CK4 AB33 BK33 CK7 AB36 BK4 CL2 AB4 BK7 CM13 AB7 BL25 CM17 AC10 BL28 CM21 AC27 BL29 CM25 AC30 BL30 CM29 BL31 CM31 AD33 BL32 CM33 AD35
VSS
BL7 AE25 BM33 CM5 AE27 BM35 CM9 AE30 BM36 CN13 AE7 BM9 CN17 AF27 BN30 CN21 AF3 BN7 CN25 AF30 CN29 AF33 BP15 AF36 AF4 CN5 AF7 BP25 CN9 AG10 BP3 CP1 BP32 CP11 AH27 BP33 CP13 AH28 BP4 CP15 AH29 BP7 CP19 AH30 CP21 AH31 BR19 CP27 AH33 BR25 AH35 CP37 AJ25 BT15 AJ28 BT16 CP9 AJ7 CR2 AK3 CR36 AK33 D21 AK36 BT25 D25 AK4 BT28 AL28 BT33 D5 AL29
Do Not Stuff
Do Not Stuff
CPU1S 19 OF 20
BT35 D6 AL32 BT36 D8 AL7 D9 AM10 BU11 E23 AM28 E27 AM33 BU23 E29 AM35 BU24 E31 BU25 E33 AN25 BU7 E9 AN28 BV11 F12 AN29 F15 AN30 F18 AN31 BV3 F2 AN7 BV31 F21 AN8 BV33 F24 BV4 F3 AP3 BW11 F4 AP33 BW15 G21 AP36 G27 AP4 G33 AR28 G35 G36 AT33 BW24 G9 AT35 H21 AT36 BW7 H27 AT4 BY11 AU10 BY15 H9 AU28 BY22 J12 AU29 J15
VSS
BY25 J18 AU32 BY28 J21 AV25 BY33 J24 AV28 BY35 J33 AV3 BY36 J36 AV33 J6 AV36 C1 K21 AV4 C21 K22 AV6 C25 K24 AV8 C29 K25 AW28 C33 K27 AW29 C4 K28 AW3 C9 K29 AW30 CA11 K3 AW31 CA15 K30 AY33 CA22 K31 AY35 K32 B12 K4 B15 CA25 K9 B18 CB11 L27 B21 L33 B23 L35 B25 CB18 L36 B27 CB19 L6 B29 CB2 N25 B31 CB20 N27 CB25
Do Not Stuff
Do Not Stuff
CPU1T 20 OF 20
N6 B37 CB3 P10 B5 CB33 P3 B7 CB4 P33 B9 CB7 P36 BA10 CC11 P4 BA28 P7 BA3 CC20 R27 BB3 CC25 R28 BB33 CC28 R29 BB36 CC31 R30 BB4 CC7 R31 BC25 CD11 T27 CD12 T30 BC29 CD14 T33 T35 BC32 CD24 T36 CD25 T7 BC8 CE33 U26 BD28 CE35 U7 BD33 CE36 V26 BD35 CE7 V27 BD36 CF11 V3 BE10 CF14 V30 BE28 CF19 V33 BE29 CF2 V36 BE3
VSS
CF23 V4 BE30 CF28 W10 BE31 CF3 W27 CF4 W30 BF3 CG33 W7 BF33 CG7 BF36 Y26 BF4 CH31 Y27 BG25 Y30 BG28 CJ11 Y33 CJ14 Y35 BH28 CJ19 Y7 BH29 CJ23 BH32 CJ28 BH33 CJ33 BH35 CJ35 BP19 BR16 BY18 BY19 CC16 BU16 CC14 BR22 BU20 CD20 BT14 BP12 CB24 CC24 J5 U24 BD7 AR4 AU4 AW4 BA6 BC4 BE4 BE8 BA4 BD4 BG4 CJ2 CJ3 AM5 CM4 AC5 AG5 CR6
Do Not Stuff
Do Not Stuff
Main Func = PCH
ALL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU_(VSS)
Size A4
Document Number
Fircrest 13"
Rev X01
Date: Thursday, April 18, 2019
Sheet 23 of 106

Main Func = EC



Cap. Value	Res. Value	TYPE
4700pF	240k ohm	Single Port ACE w/o AR
	130k ohm	Single Port ACE w AR
	62k ohm	Dual Port ACE w/o AR
	33k ohm	Dual Port ACE w AR
	8.2k ohm	Dual Port ACE (w AR + w/o AR)
	4.3k ohm	
	2k ohm	
	1k ohm	

Cap. Value	Res. Value	SIZE
4700pF	240k ohm	11"
	130k ohm	12"
	62k ohm	13"
	33k ohm	14"
	8.2k ohm	15"

Cap. Value	Res. Value	BOM
4700pF	240k ohm	X00
	130k ohm	X01
	33k ohm	X02
	1k ohm	A00

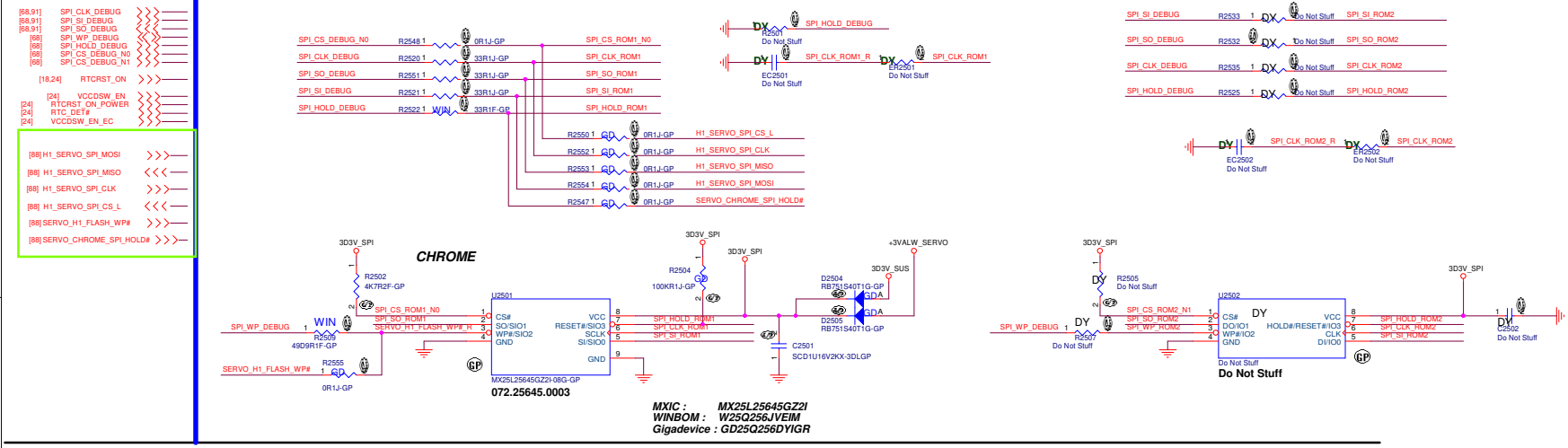
VGA_ID0	
Discrete	0
UMA	1

ENABLE_DS#	
Non-Deep Sleep	1
DeepSleep	0

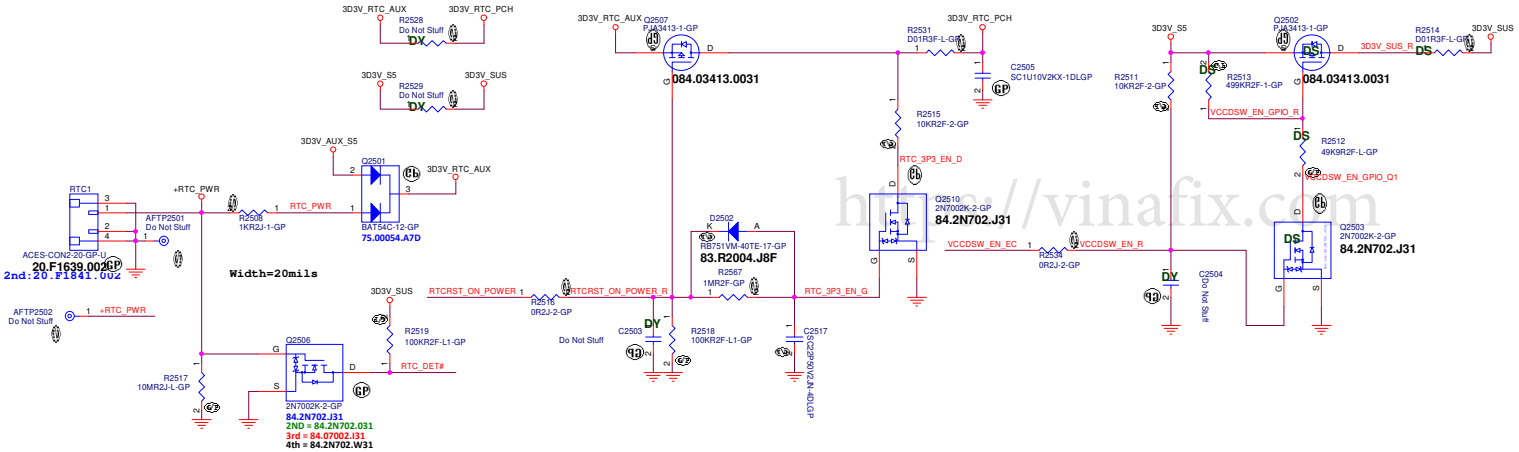
Vendor	Wistron Corporation
Title	ECIO(KBC5105)
Size	A1
Document Number	Fircrest 13"
Rev	X01
Date	Thursday, April 18, 2019
Sheet	24 of 156

Main Func = BIOS ROM/RTC

SYSTEM SPI ROM



X09 design DS3_Non-DS3 with RTC power gating



ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Flash/RTC		
Size: A2	Document Number: Fircrest 13"	Rev: X01
Date: Thursday, April 18, 2019	Sheet 25 of 106	

Main Func = Thermal / FAN

[24] REM_DIODE1_P
[24] REM_DIODE1_N
[24] REM_DIODE2_P
[24] REM_DIODE2_N

[24] REM_DIODE4_P
[24] REM_DIODE4_N
[24] PWM_FAN1
[24] TACH_FAN1

5105 Channel	Location
DP1/DN1	CPU (Q2601)
DP2/DN2	WWAN (Q2602)
DN2a/DP2a	DDR (Q2603)
DP4/DN4	V.R (Q2605)

Q2601 LMBT3904LT1G-GP
84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.03904.E11

C2601 Do Not Stuff

C2602 SC2200P50V2KX-2DLGP

REM_DIODE1_P
REM_DIODE1_N

Layout Note: Place to CPU
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC

Layout Note: Close to WWAN/2nd SSD

C2604 Do Not Stuff

Q2603 LMBT3904LT1G-GP
84.T3904.H11
3rd = 84.03904.E11
2nd = 84.T3904.K11

C2603 Do Not Stuff

Q2602 LMBT3904LT1G-GP
84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.03904.E11

C2605 SC2200P50V2KX-2DLGP

REM_DIODE2_P
REM_DIODE2_N

Layout Note:Place to DIMM
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC

Q2605 LMBT3904LT1G-GP
84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.03904.E11

C2610 Do Not Stuff

C2609 SC2200P50V2KX-2DLGP

REM_DIODE4_P
REM_DIODE4_N

Layout Note:Place to V.R
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC

3D3V_S0
U2601
PWM_FAN1
PWM_FAN1_Q
TACH_FAN1_Q
TACH_FAN1
2N7002KDW-1-GP
75.27002.F7C

5V_S0
RN2601 SRN10KJ-5-GP
FAN

AFTP2601 Do Not Stuff
C2608 SC4D7U6D3V3KX-DLGP
TACH_FAN1_Q
PWM_FAN1_Q

FAN1
ACES-CON4-29-GP
20.F1639.004
2nd:020.F0097.0004

Layout Note:
Signal Routing Guideline:
Trace width = 15mil

TACH_FAN1_Q
PWM_FAN1_Q
AFTP2602 Do Not Stuff
AFTP2603 Do Not Stuff

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (Thermal/Fan)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 26 of 106

Main Func = Audio

[29] AUD_SPK_L+
[29] AUD_SPK_L-
[29] AUD_SPK_R-
[29] AUD_SPK_R+

[29] AUD_HPJD_N
[24] NB_MUTE#

[56] DMIC_SDA_CODEC
[56] DMIC_SCL_CODEC

[17,24,40,51,68] SIO_SLP_S3#

[15,19] SPKR
[24] BEEP
[29] AUD_RING
[29] AUD_SELEEVE

[29] LINE1_R
[29] LINE1_L

[29] MIC2_VREFO_R
[29] MIC2_VREFO_L
[29] AUD_HPOUT_L
[29] AUD_HPOUT_R

[19] AUD_PWR_EN

[19] HDA_RST#
[19] HDA_SDI0
[19] HDA_SDOUT_CODEC
[19] HDA_SYNC_CODEC
[19] HDA_BITCLK_CODEC

15mA
1D8V_S0 R2725 Do Not Stuff DY 3D3V_S0 R2702 D01R3F-L-GP +3V_1D8V_AVDD
1D8V_S0 R2726 Do Not Stuff DY 3D3V_S0 R2707 D01R3F-L-GP +3V_1D8V_AVDD_IO

200mA
1D8V_S0 R2703 0R2J-2-GP CPVDD
C2701 SCD1U16V2KX-3DLGP
C2705 SC10U6D3V3MX-DL-GP
Close pin 20

+3V_1D8V_AVDD
C2719 SC10U6D3V3MX-DL-GP
C2720 SCD1U16V2KX-3DLGP
+3V_1D8V_AVDD_IO
C2722 SC10U6D3V3MX-DL-GP
C2718 SCD1U16V2KX-3DLGP
3D3V_RTC_AUX R2712 0R2J-2-GP

U2701
DVDD
DVDD-IO
AVDD1
CPVDD/AVDD2
PVDD1
PVDD2
5VSTB/AUX_MODE
I2C-DATA
I2C-CLK
AUDIOLINK_SYNC
AUDIOLINK_BCLK
AUDIOLINK_SDATA-OUT
AUDIOLINK_SDATA-IN
DC-DET/EAPD
I2S-MCLK
I2S-BCLK
I2S-LRCK
I2S-IN
I2S-OUT
HP/LINE2-JD(JD1)
I2S-IN/I2S-OUT-JD(JD2)
GPIO0/DMIC-DATA12
GPIO1/DMIC-CLK
DMIC-CLK-IN/I2S-EN/SPDIF-OUT/GPIO2/DMIC-DATA34
PDB
PCBEEP
MIC2-L(PORT-F-L)/RING2
MIC2-R(PORT-F-R)/SLEEVE
LINE2-L(PORT-E-L)
LINE2-R(PORT-E-R)
SPK-OUT-L+
SPK-OUT-L-
SPK-OUT-R+
SPK-OUT-R-
HPOUT-L(PORT-I-L)
HPOUT-R(PORT-I-R)
VREF
LDO1-CAP
LDO2-CAP
LDO3-CAP
MIC2-VREFO-L
MIC2-VREFO-R
MIC2-CAP
CPVEE
CBP
CBN
AVSS1
AVSS2
GND
ALC3254-VA3-CG-GP
071.03254.M001

SPKR BEEP R2729 1KR2J-1-GP R2730 1KR2J-1-GP
HDA_SPKR_R KBC_BEEP_R D2701 SCD1U16V2KX-3DLGP BAT54C-12-GP
75.00054.A7D
AUD_PC_BEEP_C AUD_PC_BEEP_R C2717 R2704 0R2J-2-GP R2715 2K2R2F-GP

Layout Note:
Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

HDA_SYNC_CODEC R2723 33R2F-3-GP HDA_BITCLK_CODEC_R
HDA_BITCLK_CODEC R2719 0R2J-2-GP HDA_SDOUT_CODEC_R
HDA_SDOUT_CODEC R2721 33R2F-3-GP HDA_SDIN0_CODEC
HDA_SDI0 R2722 Do Not Stuff DVSS

Layout Note:
Place close to Pin 1
+3V_1D8V_AVDD R2713 100KR2F-L-GP
R2714 200KR2F-L-GP
AUD_HPJD_N R2724 100KR2F-L-GP AUD_HPJD_N_R
AUD_IS2-IN
DMIC_SDA_CODEC R2718 0R2J-2-GP DMIC_SDA_CODEC_R
DMIC_SCL_CODEC R2720 0R2J-2-GP DMIC_SCL_CODEC_R
Close pin5
EC2721 Do Not Stuff
EC2708 Do Not Stuff

moat
5V_S0 R2710 D01R3F-L-GP +5V_AVDD
50mA
C2703 SC10U6D3V3MX-DL-GP
C2702 SCD1U16V2KX-3DLGP
AUD_AGND
Layout Note:
Place close to Pin 40

+3V_1D8V_AVDD R2716 100KR2F-L-GP R2717 0R2J-2-GP
NB_MUTE# EAPD#
HDA_RST# R2731 Do Not Stuff DY

5V_S0 R2706 D01R6F-3-GP +5V_PVDD
800mA
C2706 SC10U6D3V3MX-DL-GP
C2707 SCD1U16V2KX-3DLGP
C2708 SC10U6D3V3MX-DL-GP
C2709 SCD1U16V2KX-3DLGP
C2733 SCD1U16V2KX-3DLGP
C2734 SCD1U16V2KX-3DLGP
Layout Note:
Close pin41
Layout Note:
Close pin46

+5V_PVDD/+3V_AVDD
1500mA
C2732 SC1U10V2KX-1DLGP 5V_S5
U2702
VBIAS
VIN1#1
VIN1#2
VIN2#6
VIN2#7
ON1
ON2
GND
VOUT1#13
VOUT1#14
VOUT2#8
VOUT2#9
CT1
CT2
APE8910GN3B-GP
074.08910.0093
C2724 SC10U6D3V3MX-DL-GP
C2731 SC10U6D3V3MX-DL-GP
R2709 0R2J-2-GP
R2711 0R2J-2-GP
AUD_PWR_EN AUD_5V_EN AUD_3V_EN
C2725 Do Not Stuff
C2726 Do Not Stuff
C2723 SC10U6D3V3MX-DL-GP
C2715 SCD1U16V2KX-3DLGP
15mA
C2727 SC470P50V2KX-3DLGP
C2728 SC470P50V2KX-3DLGP
C2729 SC10U6D3V3MX-DL-GP
C2730 SCD1U16V2KX-3DLGP
R2727 0R3J-0-U-GP
R2728 0R3J-0-U-GP

moat
EC2702 SCD1U25V2KX-1-DL-GP
EC2703 SCD1U25V2KX-1-DL-GP
EC2704 SCD1U25V2KX-1-DL-GP
EC2705 SCD1U25V2KX-1-DL-GP
EC2706 SCD1U25V2KX-1-DL-GP
AUD_AGND
R2705 Do Not Stuff
Layout Note:
AUD_AGND R2705 must place nearby codec IC.

HDA_SDOUT_CODEC
EC2701 Do Not Stuff
FC2701 Do Not Stuff
HDA_BITCLK_CODEC
EC2707 SC22P50V2JN-4DLGP
FC2702 Do Not Stuff

EMI suggest change to 33p
2015/12/02
Azalia I/F EMI

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (CodecALC3253)
Size: A3
Document Number: Fircrest 13"
Rev: X01
Date: Friday, April 19, 2019
Sheet 27 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (RSVD) (Audio AMP)

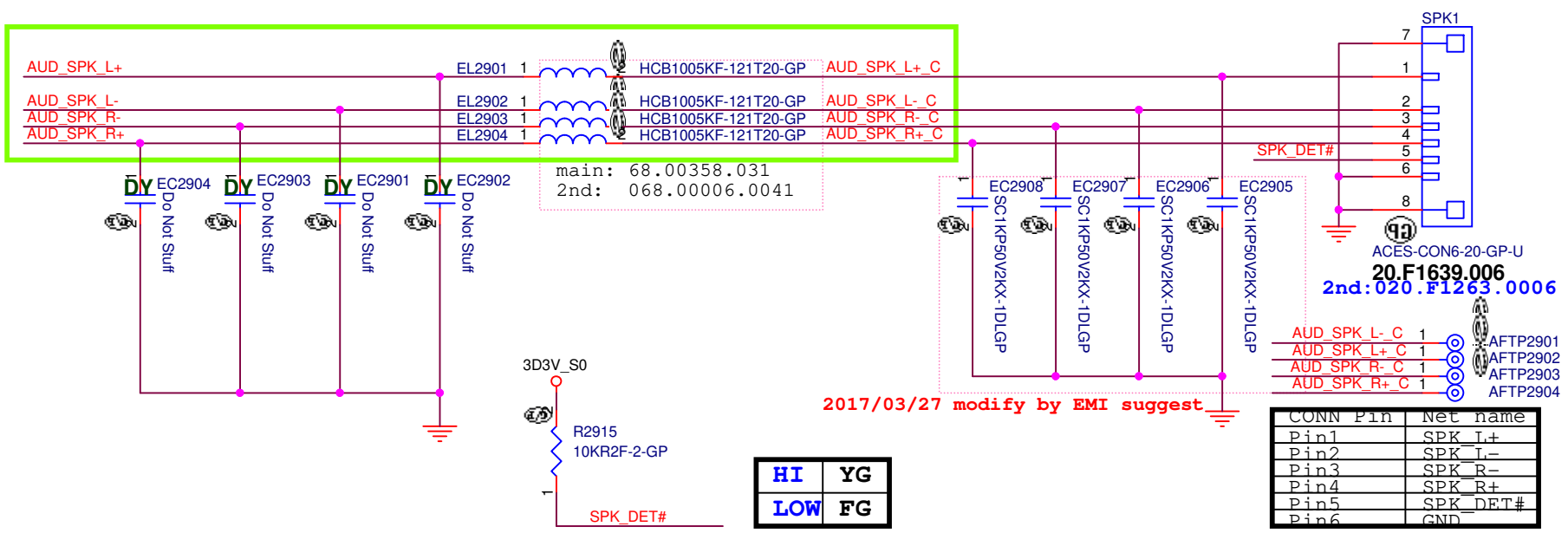
Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 28 of 106

Main Func = Audio

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

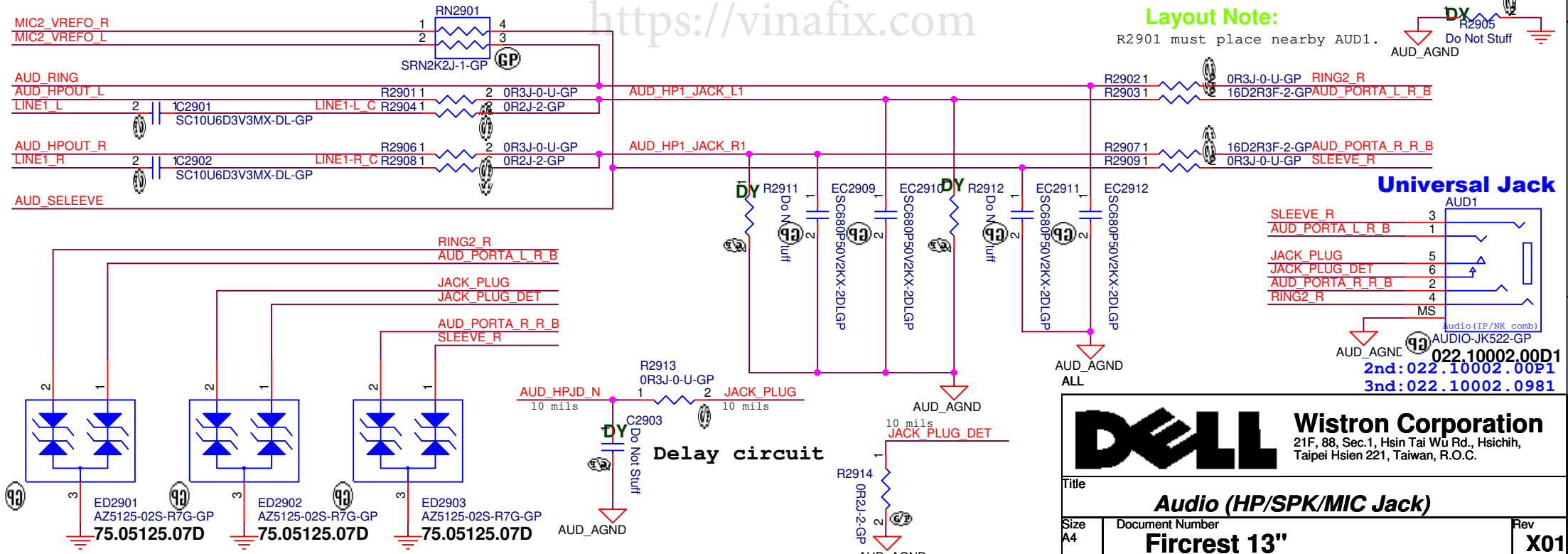


HI	YG
LOW	FG

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

[27] AUD_SPK_L+
[27] AUD_SPK_L-
[27] AUD_SPK_R-
[27] AUD_SPK_R+
[27] MIC2_VREFO_R
[27] MIC2_VREFO_L
[27] AUD_RING
[27] AUD_HPOUT_L
[27] LINE1_L
[27] AUD_HPOUT_R
[27] LINE1_R
[27] AUD_SELEEVE
[27] AUD_HPJD_N
[19] SPK_DET#

Layout Note:
R2901 must place nearby AUD1.



DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	*Audio (HP/SPK/MIC Jack)*		
Size A4	Document Number **Fircrest 13"**		Rev X01
Date: Thursday, April 18, 2019		Sheet 29 of 106	

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio (RSVD)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 30 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN (RSVD) (Giga_RTL8151GD)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 31 of 106

Main Func = LAN

[24,64] LED_MASK#
[97] LAN_0_GREEN_LINK_N
[97] LAN_1_AMBER_ACT_N

[97] LAN_MDI0_P
[97] LAN_MDI0_N

[97] LAN_MDI1_P
[97] LAN_MDI1_N

[97] LAN_MDI2_P
[97] LAN_MDI2_N

[97] LAN_MDI3_P
[97] LAN_MDI3_N

XF3201

LAN_MDI3_N 2 — 1CT:1CT — 23 MDO3-
1 — 24 MCT0
LAN_MDI3_P 3 — 22 MDO3+
LAN_MDI2_N 5 — 1CT:1CT — 20 MDO2-
4 — 21 MCT1
LAN_MDI2_P 6 — 19 MDO2+
LAN_MDI1_N 8 — 1CT:1CT — 17 MDO1-
7 — 18 MCT2
LAN_MDI1_P 9 — 16 MDO1+
LAN_MDI0_N 11 — 1CT:1CT — 14 MDO0-
10 — 15 MCT3
LAN_MDI0_P 12 — 13 MDO0+

LAN

XFORM-24P-19-GP
68.IH601.301

LOM_TCT
LAN C3202 SCD01U50V2KX-1DLGP

Layout note:
30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF

3D3V_LAN

LOM_AMB# — LAN R3202 510R2J-1-GP — LOM_AMB#_R
LOM_GRN# — LAN R3201 510R2J-1-GP — LOM_GRN#_R

Check again Lan Led behavior as ARD want

AFTP3214 Do Not Stuff

RJ45

A2 AMBER
A1
CHASSIS#12
CHASSIS#10
MDO3-
MDO3+
MDO1-
MDO2-
MDO2+
MDO1+
MDO0-
MDO0+
CHASSIS#9
CHASSIS#11
B2 GREEN
B1

LAN

RJ45-8P-293-GP
022.10008.0581

3D3V_LAN
MDO3-
MDO3+
MDO2-
MDO2+
MDO1-
MDO1+
MDO0-
MDO0+
LOM_GRN#_R
LOM_AMB#_R

AFTP3202 Do Not Stuff
AFTP3203 Do Not Stuff
AFTP3204 Do Not Stuff
AFTP3205 Do Not Stuff
AFTP3206 Do Not Stuff
AFTP3207 Do Not Stuff
AFTP3208 Do Not Stuff
AFTP3209 Do Not Stuff
AFTP3210 Do Not Stuff
AFTP3212 Do Not Stuff
AFTP3213 Do Not Stuff

ED3201

LAN_MDI3_N 1 — LINE_1 — NC#10 — 10 LAN_MDI3_N
LAN_MDI3_P 2 — LINE_2 — NC#9 — 9 LAN_MDI3_P
3 — GND — GND — 8
LAN_MDI2_N 4 — LINE_3 — NC#7 — 7 LAN_MDI2_N
LAN_MDI2_P 5 — LINE_4 — NC#6 — 6 LAN_MDI2_P

LAN

AZ1045-04F-R7G-GP
75.01045.073

ED3202

LAN_MDI1_N 1 — LINE_1 — NC#10 — 10 LAN_MDI1_N
LAN_MDI1_P 2 — LINE_2 — NC#9 — 9 LAN_MDI1_P
3 — GND — GND — 8
LAN_MDI0_N 4 — LINE_3 — NC#7 — 7 LAN_MDI0_N
LAN_MDI0_P 5 — LINE_4 — NC#6 — 6 LAN_MDI0_P

LAN

AZ1045-04F-R7G-GP
75.01045.073

MCT0
MCT1
MCT2
MCT3

RN3201 SRN75J-1-GP

LAN

MCT

LAN C3201 SC56P3KV8JN-1-GP
078.5603N.014D
Follow KS13 cap

LOM_GRN#_R — DY EC3202 Do Not Stuff
LOM_AMB#_R — DY EC3203 Do Not Stuff

LAN_1_AMBER_ACT_N 4 — 3 LOM_AMB#
LED_MASK# 5 — 2 LED_MASK#
LOM_GRN# 6 — 1 LAN_0_GREEN_LINK_N

Q3202 LAN
2N7002KDW-1-GP
75.27002.F7C

- LED0 (010): Green = Indicates Link connection established (located on left-hand side of connector)
- LED1 (011): Amber = Blinking when network activity (located on right-hand side of connector)

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN (RJ45+Transformer)	
Size A4	Document Number: Fircrest 13"	Rev X01
Date: Thursday, April 18, 2019	Sheet 32 of 106	

Main Func = Card Reader

[16] CARD_PCIE_RX_N
[16] CARD_PCIE_RX_P
[16] CARD_PCIE_TX_N
[16] CARD_PCIE_TX_P

[18] CARD_CLK_CPU_P
[18] CARD_CLK_CPU_N
[18] CARD_CLKREQ_CPU_N
[18] MEDIACARD_IRQ#

[17,61,62,91,97] PCH_PLTRST#_RIGHT
[19] HOST_SD_WP#

Layout Note:

3D3V_S0_CARD — Close to pin11 — C3301 SC10U6D3V3MX-DL-GP, C3302 SCD1U16V2KX-3DLGP
3D3V_AUX_CARD — Close to pin27 — C3303 SC4D7U6D3V3KX-DLGP, C3304 SCD1U16V2KX-3DLGP
Close to pin14
Close to pin10
1D2V_LDO — C3306 SC4D7U6D3V3KX-DLGP, C3307 SCD1U16V2KX-3DLGP, C3308 SCD1U16V2KX-3DLGP
SD_VDD1 — C3314 SCD1U16V2KX-3DLGP, C3315 SC4D7U6D3V3KX-DLGP
Layout Note:Close to Card Reader CONN
SD_VDD2 — C3316 SCD1U16V2KX-3DLGP, C3317 SC4D7U6D3V3KX-DLGP

3D3V_S0_CARD

850mA

3D3V_S0 — R3301 D01R5F-GP — 3D3V_S0_CARD
3D3V_S0_CARD — R3303 0R3J-0-U-GP — 3D3V_AUX_CARD
3D3V_AUX_CARD — R3302 10KR2F-2-GP — MEDIACARD_IRQ#

teknisi indonesia

U3301 RTS5242-GR-GP-U
071.05242.0003

SD_VDD2, SD_VDD1 — 1D2V_LDO, 3D3V_S0_CARD, 1D2V_LDO, 3D3V_AUX_CARD — C3305 SC1U10V2KX-1DLGP
CARD_PCIE_TX_P — C3309 — SCD1U16V2KX-3DLGP — CARD_PCIE_TX_P_C
CARD_PCIE_TX_N — C3310 — SCD1U16V2KX-3DLGP — CARD_PCIE_TX_N_C
CARD_PCIE_RX_P — C33111 — SCD1U16V2KX-3DLGP — CARD_PCIE_RX_P_C
CARD_PCIE_RX_N — C33121 — SCD1U16V2KX-3DLGP — CARD_PCIE_RX_N_C
CARD_CLK_CPU_P, CARD_CLK_CPU_N
SD_D0P, SD_D0N, SD_D1P, SD_D1N — For UHS-II

SD_DATA1 — R3305 0R2J-2-GP — SD_DATA1_CON
SD_DATA0 — R3306 0R2J-2-GP — SD_DATA0_CON
SD_CLK — ER3304 10R2F-L-GP — SD_CLK_CON
SD_CMD — R3307 0R2J-2-GP — SD_CMD_CON
SD_DATA3 — R3308 0R2J-2-GP — SD_DATA3_CON
SD_DATA2 — R3309 0R2J-2-GP — SD_DATA2_CON
SD_WP
SD_CD# — R3310 0R2J-2-GP
PCIE_CARD_PLT_RST# — PCH_PLTRST#_RIGHT
DEV_WAKE# — 1MEDIACARD_IRQ#
CARD_RREF — R3311 0R2J-2-GP — CARD_SDREG2
CARD_GPIO — R3312 10KR2F-2-GP — 3D3V_AUX_CARD
C3313 SC1U10V2KX-1DLGP, R3313 6K2R2F-GP

Vendor: EC3301 Closed to chip
EC3301 SC6D8P50V2CN-DL-GP

HOST_SD_WP# — Q3301 2N7002K-2-GP — SD_WP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31

ED3302 AZ5315-02F-GP — SD_CLK_CON, SD_CMD_CON — 83.05315.0A0
ED3303 AZ5315-02F-GP — SD_DATA0_CON, SD_DATA1_CON — 83.05315.0A0
ED3304 AZ5315-02F-GP — SD_DATA2_CON, SD_DATA3_CON — 83.05315.0A0
ED3305 AZ5315-02F-GP — SD_D0P, SD_D0N — 83.05315.0A0
ED3306 AZ5315-02F-GP — SD_D1P, SD_D1N — 83.05315.0A0

CARD1 CARD-PUSH-23P-GP
062.10002.0891

SD_VDD1, SD_VDD2
SD_CLK_CON, SD_CMD_CON
SD_DATA0_CON, SD_DATA1_CON, SD_DATA2_CON, SD_DATA3_CON
SD_D0P, SD_D0N, SD_D1P, SD_D1N
SD_CD# — EC3306 SC1K5P50V2KX-1DLGP
SD_DATA3_CON, SD_DATA2_CON, SD_DATA1_CON, SD_DATA0_CON
EC3303, EC3304, EC3305, EC3302 — Do Not Stuff

SD_VDD1, SD_VDD2, SD_CLK_CON, SD_CMD_CON, SD_D0P, SD_D0N, SD_D1P, SD_D1N, SD_DATA0_CON, SD_DATA1_CON, SD_DATA2_CON, SD_DATA3_CON, SD_CD#
AFTP3301 ~ AFTP3313 Do Not Stuff
以上測點不可拉分支型式

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARDREADER (SDIO/SD Conn)
Size: A3 | Document Number: Fircrest 13" | Rev: X01
Date: Thursday, April 18, 2019 | Sheet 33 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (RSVD) (USB2.0 CONN)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 34 of 106

Main Func = USB 3.0

USB3.1 PORT1

[16] USB3_USB31_RX_N
[16] USB3_USB31_RX_P
[16] USB3_USB31_TX_N
[16] USB3_USB31_TX_P

USB3.1 PORT2

[16] USB4_USB31_RX_N
[16] USB4_USB31_RX_P
[16] USB4_USB31_TX_N
[16] USB4_USB31_TX_P

USB2.0 port2

[16] USB3_USB20_N
[16] USB3_USB20_P

USB2.0 port1

[36] USB4_USB20_N
[36] USB4_USB20_P

[24] USB_PWR_EN1#
[16] USB_OC1#

USB4/USB30-3/USB20-3/PowerShare

C3504 SCD1U16V2KX-3DLGP
USB4_USB31_TX_P → USB4_USB31_TX_CMC_P
R3512 0R2J-2-GP
USB4_USB31_TX_CON_P
EL3506 Do Not Stuff
Do Not Stuff
C3503 SCD1U16V2KX-3DLGP
USB4_USB31_TX_N → USB4_USB31_TX_CMC_N
R3511 0R2J-2-GP
USB4_USB31_TX_CON_N
R3510 0R2J-2-GP
USB4_USB31_RX_P
USB4_USB31_RX_CON_P
EL3504 Do Not Stuff
Do Not Stuff
R3507 0R2J-2-GP
USB4_USB31_RX_N
USB4_USB31_RX_CON_N

R3508 Do Not Stuff
EL3505
USB4_USB20_N
USB4_USB20_P
USB4_USB20_CON_N
USB4_USB20_CON_P
DLM0NSN900HY2D-GP
068.09002.2001
R3509 Do Not Stuff

ED3503
AZ5315-02F-GP
83.05315.0A0

ED3504
LINE_1 LINE_2 GND LINE_3 LINE_4
NC#10 NC#9 GND NC#7 NC#6
AZ1045-04F-R7G-GP
75.01045.073

EXT Port1 Right Side, Support Power Share

USB30_VCCB
USB4
VBUS D- D+ SSRX- SSRX+ SSTX- SSTX+ PGND GND
CHASSIS#10 CHASSIS#11 CHASSIS#12 CHASSIS#13
USB3.0
SKT-USB13-317-GP
022.10005.04M1

USB3/USB30-3/USB20-2

C3502 SCD1U16V2KX-3DLGP
USB3_USB31_TX_P → USB3_USB31_TX_CMC_P
R3506 0R2J-2-GP
USB3_USB31_TX_CON_P
EL3503 Do Not Stuff
Do Not Stuff
C3501 SCD1U16V2KX-3DLGP
USB3_USB31_TX_N → USB3_USB31_TX_CMC_N
R3505 0R2J-2-GP
USB3_USB31_TX_CON_N
R3504 0R2J-2-GP
USB3_USB31_RX_P
USB3_USB31_RX_CON_P
EL3501 Do Not Stuff
Do Not Stuff
R3501 0R2J-2-GP
USB3_USB31_RX_N
USB3_USB31_RX_CON_N

R3502 Do Not Stuff
EL3502
USB3_USB20_N
USB3_USB20_P
USB3_USB20_CON_N
USB3_USB20_CON_P
DLM0NSN900HY2D-GP
068.09002.2001
R3503 Do Not Stuff

ED3501
I/O1 GND I/O2 I/O4 VDD I/O3
USB3_USB20_CON_N
USB3_USB20_CON_P
USB30_VCCA
AZC099-04S-2-GP
075.09904.0A7C

ED3502
LINE_1 LINE_2 GND LINE_3 LINE_4
NC#10 NC#9 GND NC#7 NC#6
USB3_USB31_RX_CON_N
USB3_USB31_RX_CON_P
USB3_USB31_TX_CON_N
USB3_USB31_TX_CON_P
AZ1045-04F-R7G-GP
75.01045.073

Low Active
C3505 SC1U10V2KX-1DLGP
5V_S5
U3502
IN EN# OUT GND OC#
USB_PWR_EN1#
USB_OC1#
SY6288DAAC-GP
074.06288.009B
C3506 SCD1U16V2KX-3DLGP
C3507 SC1U10V2KX-1DLGP
C3508 SC100U6D3V6MX-DL-GP
R3513 Do Not Stuff
USB30_VCCA

USB30_VCCA
USB3
VBUS D- D+ SSRX- SSRX+ SSTX- SSTX+ PGND GND
CHASSIS#10 CHASSIS#11 CHASSIS#12 CHASSIS#13
USB3.0
SKT-USB13-317-GP
022.10005.04M1

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (USB3.0 Conn)
Size: A3
Document Number: Fircrest 13"
Rev: X01
Date: Thursday, April 18, 2019
Sheet 35 of 106

Main Func = USB Charger

support power share on the USB3.0 port on the right side of platform

USB2.0 port2

[35] USB4_USB20_N
[35] USB4_USB20_P

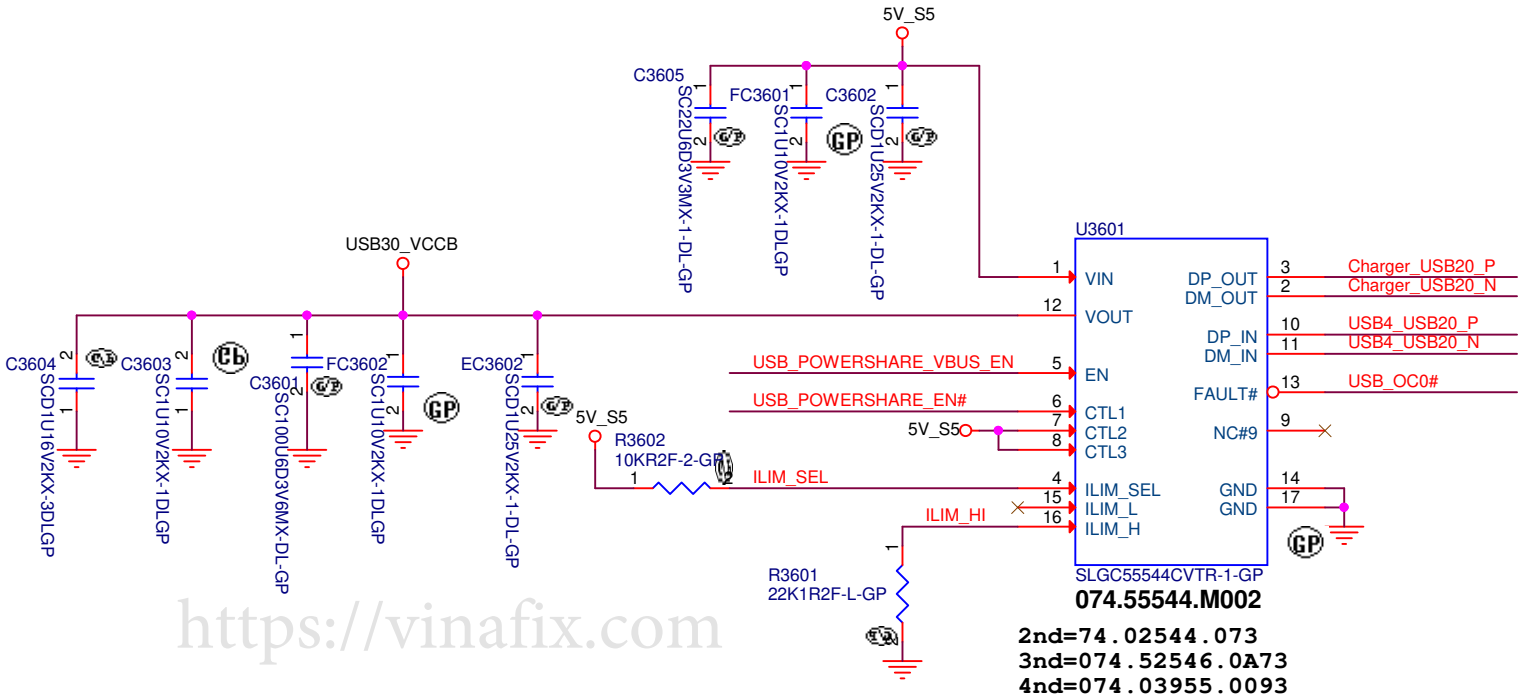
[24] USB_POWERSHARE_VBUS_EN
[24] USB_POWERSHARE_EN#

[16] USB_OC0#

USB charger

[16] Charger_USB20_N
[16] Charger_USB20_P

USB3.0 Port2



Device Control Pins				
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH(Discharge)	0	0	0	x
CDP	1	1	1	1
SDP2(No Discharge from/to CDP)	1	1	1	0
SDP1(Discharge from/to any charging state including CDP)	1	1	0	x
	0	1	0	x
DCP_Short	1	0	0	x
DCP/Divider-1A	1	0	1	x
DCP_Auto	0	1	1	x
	0	0	1	x

Current Limit	MIN	TPY	MAX
TI	2120	2275	2430
PERICOM	2120	2275	2430
NUVOTON	2235	2400	2570

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (USB Charger)

Size: A4 | Document Number: Fircrest 13" | Rev: X01

Date: Thursday, April 18, 2019 | Sheet 36 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (PCIE to USB3.0)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 37 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **USB (RSVD)(USB3.0 Redriver)**

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 38 of 106

Main Func =

ALL

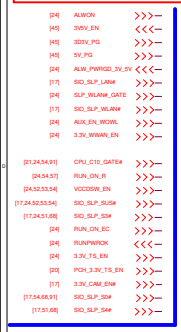
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

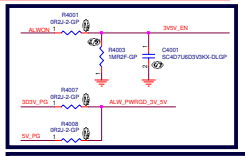
Title: *Sequence (RSVD)*

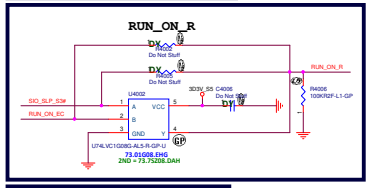
Size	Document Number	Rev
A4	*Fircrest 13"*	*X01*

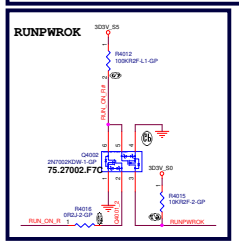
Date: Thursday, April 18, 2019 Sheet 39 of 106

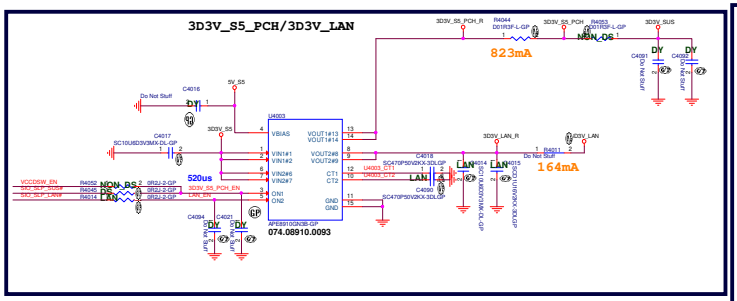
Main Func = Power Plane EN Sequence

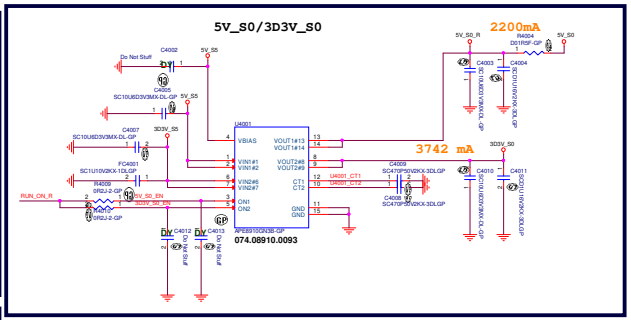


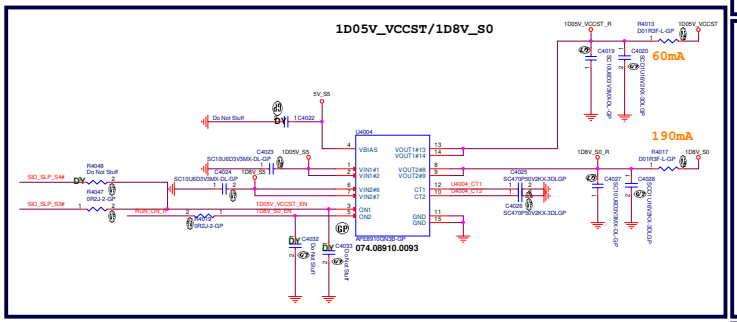


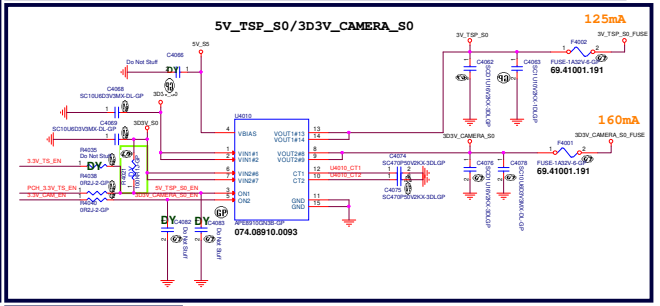


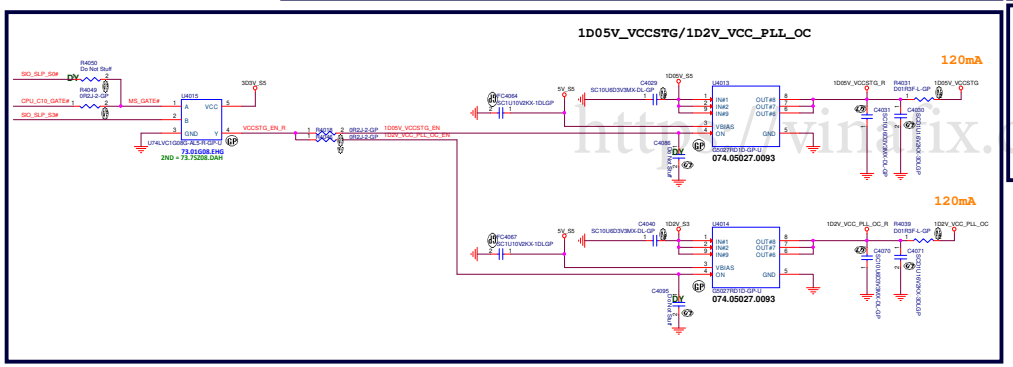


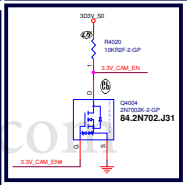


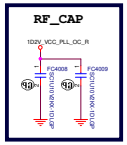


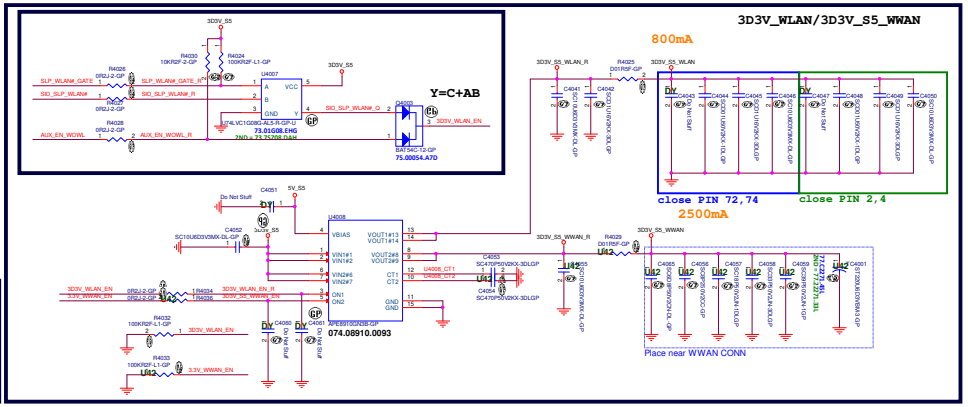


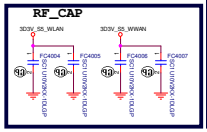












ALL

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: Sequence (Power Plane Enable)

Size: A1 | Document Number: Fircrest 13" | Rev: X01

Date: Friday, April 19, 2013 | Sheet 40 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Sequence (RSVD) (DS3/S0ix)**

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 41 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

INT IO (RSVD)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 42 of 106

Main Func = DCIN & BATT Com

[24] PS_ID
[3,24,44,46] PROCHOT#_CPU
[44] CMOUT
[24,44] AC_DIS
[24] DCIN2_EN
[24,44] PBAT_CHARGER_SMBCLK
[24,44] PBAT_CHARGER_SMBDAT
[24,44] PBAT_PRES#
[74] PWR_VBUS_OVP_OUT_R
[24,74] AC_DISC#
[24,44,74] HW_ACAVIN_NB
[24,74] VBUS1_ECOK

PSID

Layout Note:
PSID Layout width > 25mil

R4302 15KR2F-GP
Q4302_B
Q4302 LMBT3904LT1G-GP 84.T3904.H11
PSID_DISABLE#_R_C
R4305 100KR2F-L1-GP
R4303 10KR2J-3-GP
5V_S5
3D3V_S5
D4302 LBAV99LT1G-1-GP 75.00099.O7D
2nd = 75.00099.K7D
3rd = 75.00099.O7D
4th = 75.00099.D7D
R4306 2K2R2F-GP
PS_ID
R4301 0R3J-0-U-GP
PS_ID_R1
PS_ID_R2
D4301 L30ESD24VC3-2-GP 83.03024.0A1
Q4301 PJA138KA-GP 084.00138.0A31
R4308 33R2F-3-GP
R4309 Do Not Stuff DY

AC Disconnect Latch

3D3V_S5
R4304 100KR2F-L1-GP
CMOUT
R4307 Do Not Stuff
AC_DISC#
Q4303
Q4304 T2N7002BK-2-GP 084.27002.0L31
PROCHOT#_CPU
2N7002KDW-1-GP 75.27002.F7C

DC_IN

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

teknisi indonesia

DCIN1 HR-CON5-7-GP 020.F1194.0005
+DC_IN_C
PS_ID_R
EL4301 0R5J-5-GP
EL4302 0R5J-5-GP
EL4303 0R5J-5-GP
EL4304 0R5J-5-GP
JGND
EC4302 EC4303 EC4304 EC4305 SCD1U50V3KX-DL-GP
D4303 P6SMB27A-GP
C4301 SCD1U50V3KX-DL-GP
R4310 Do Not Stuff
R4311 Do Not Stuff
R4312 Do Not Stuff
Q4305_D
AC_IN#_G
Q4305
AC_IN_KBC#
AC_DIS
PQ4304 LMUN5212T1G-GP 84.05212.B11
PQ4302 LTA024EUBFS8TL-GP 084.00024.001K
AD_OFF_L
AD_OFF_R
+3D3V_VDD_DCIN
R4325 0R2J-2-GP EXT
R4324 0R2J-2-GP INT
DCIN2_EN_PU
Without Inpur LDO need to Stuff
R4322 100KR2F-L1-GP
R4319 100KR2F-L1-GP
Form EC Control
DCIN2_EN#
Q4306 2N7002KDW-1-GP 75.27002.F7C
R4318 100KR2F-L1-GP
R4331 1MR2J-1-GP
3D3V_S5

+DC_IN
PR4301 100KR2F-L1-GP
PQ4303 NTR4502PT1G-GP-U 84.04502.031
DCIN_OFF_R_G
DCIN_OFF_R_D
PC4305 SCD0U25V2KX-GP
PR4303 100KR2F-L1-GP
PR4304 0R2J-2-GP
PR4302 1MR2F-GP
PR4305 1MR2F-GP
DCIN_OFF_R
DCIN2_EN_D
PQ4301 2N7002KDW-1-GP 75.27002.F7C
DCIN_OFF
AD_OFF
PR4306 1MR2J-1-GP
PR4308 1MR2J-1-GP

S1
PU4301 ACN7403-GP-U 84.07403.037
Id=-9.6A
Qg=-25nC
Rdson=18~30mohm
AD+
EC4308 EC4303 EC4301 EC4304 EC4305 SCD1U25V2KX-1DL-GP
R4332 C4305

DCIN2_EN_PU
R4330 Do Not Stuff
Q4308
DCIN2_EN_D_R
D4309 Do Not Stuff
DCIN2_EN_D
Do Not Stuff
2nd = 084.27002.0N31
D4310 RB751VM-40TE-17-GP 83.R2004.J8F
VBUS1_ECOK

D4308 75.00054.A7D
2VBUS_OVP_OUT
1HW_ACAVIN_NB#
BAT54C-12-GP
DCIN Off Logic
PR4307 0R2J-2-GP
PWR_VBUS_OVP_OUT_R
Form OVP LPS Logic

R4326 Do Not Stuff
R4327 0R2J-2-GP
Without Inpur LDO need to Stuff
R4313 200KR2F-L-GP
R4315 150KR2F-L-GP
R4316 15KR2F-GP
C4302 SCD1U25V2KX-1DL-GP
R4317 10KR2F-L1-GP
C4303
U4301 AS331KTR-G1-GP 74.00331.H2F
INPUT- GND INPUT+ VCC OUTPUT
U4301_VCC
R4314 10KR2F-2-GP
R4323 10KR2F-2-GP
C4304 SCD1U25V2KX-1DL-GP
Q4307 2N7002K-2-GP 84.2N702.J31
2nd = 084.27002.0N31
HW_ACAVIN_NB

Batt Connecter

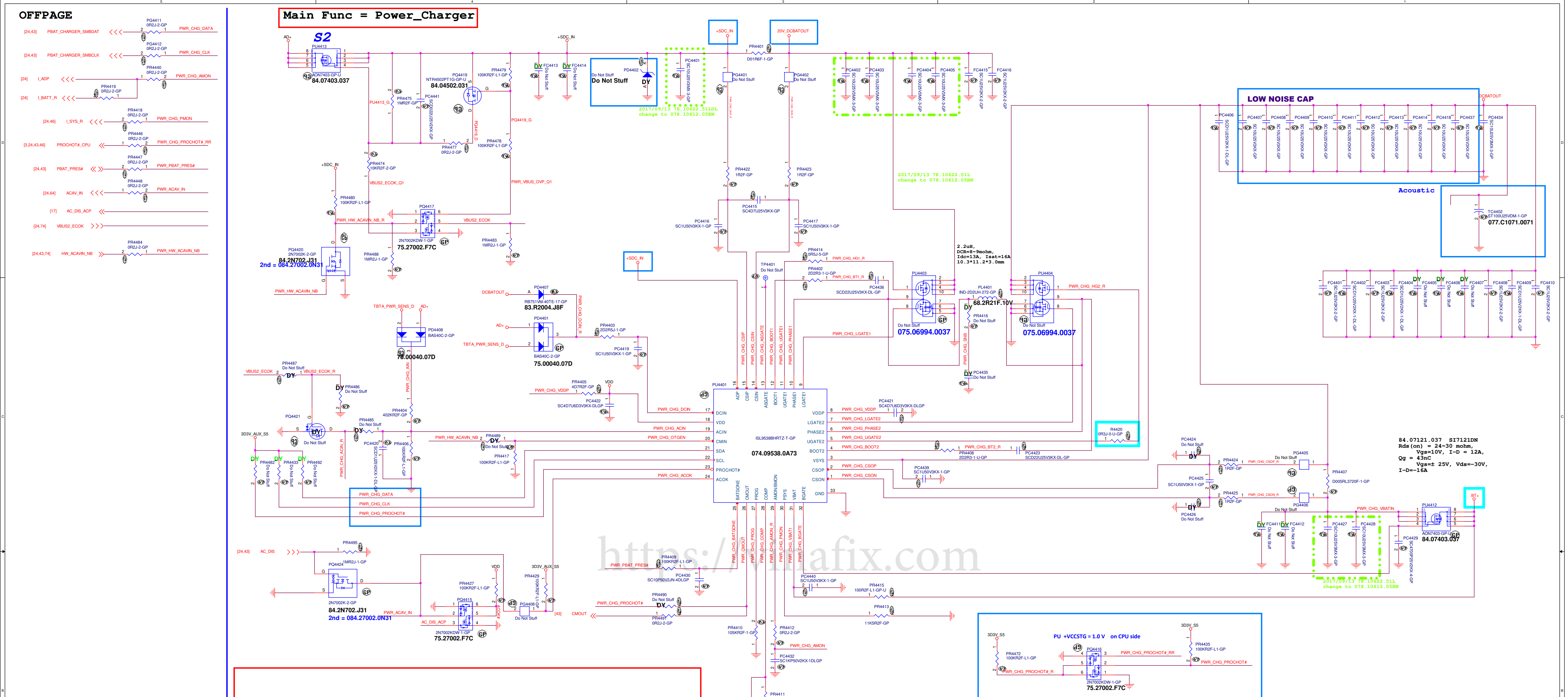
BATT1 DER-CON10-1-GP-U 020.F1229.0010
BT+
D4304 Do Not Stuff
EC4301 SCD1U25V2KX-1-DL-GP
RN4301 SRN100J-3-GP 66.10136.04L
PBAT_SMBCLK1
PBAT_SMBDAT1
PBAT_PRES1#
SYS_PRES1#
PBAT_CHARGER_SMBCLK
PBAT_CHARGER_SMBDAT
PBAT_PRES#
R4321 0R2J-2-GP
R4320 100R2F-L1-GP-U

D4305 LBAV99LT1G-1-GP 75.00099.O7D
D4306 Do Not Stuff
D4307 LBAV99LT1G-1-GP 75.00099.O7D
2nd = 75.00099.K7D
3rd = 75.00099.O7D
4th = 75.00099.D7D
3D3V_AUX_S5
Placement: Close to Batt Connector

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC IN/BATT Conn
Size: A2
Document Number: Fircrest 13"
Rev: X01
Date: Thursday, April 18, 2019
Sheet 43 of 106



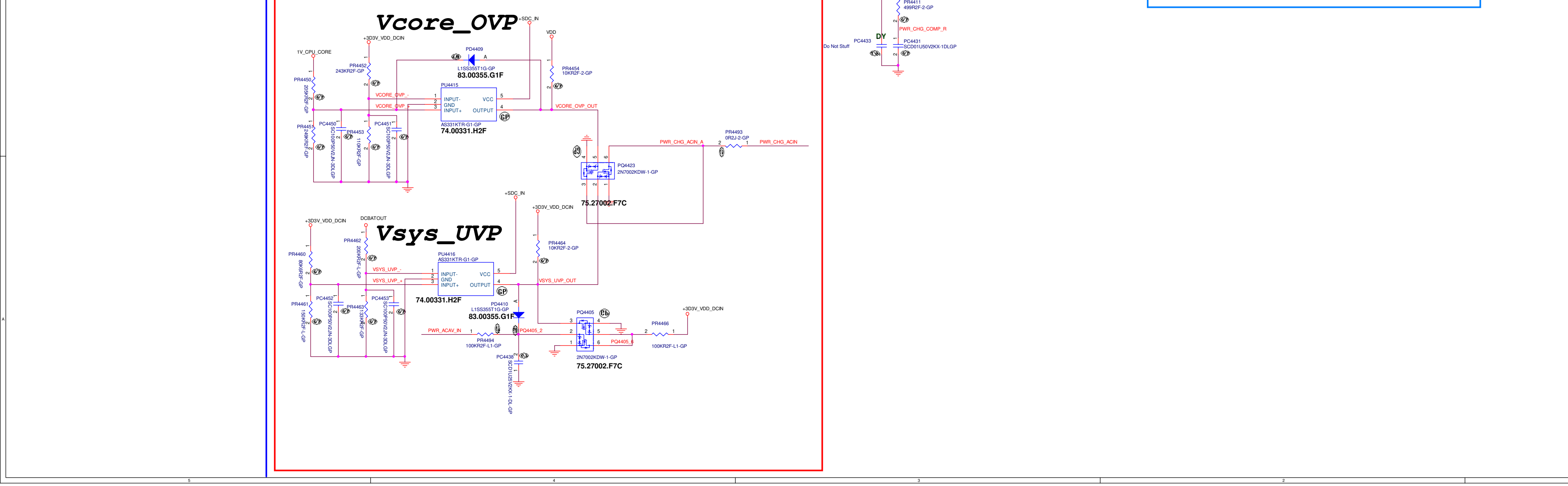


TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	Yes	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	Yes	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Charger**

Size: A1 | Document Number: **Fircrest 13"** | Rev: **X01**

Date: Thursday, April 18, 2019 |

OFFPAGE

[40] 3V5V_EN — PR4518 0R2J-2-GP — PWR_3V5V_EN

[40] 5V_PG — PR4517 0R2J-2-GP — PWR_5V_PG

[40] 3D3V_PG — PR4516 0R2J-2-GP — PWR_3V_PG

[40] SIO_SLP_S0#

Main Func = Power_System 5V/3D3V

DCBATOUT — PWR_DCBATOUT_3D3V

PG4501 Do Not Stuff (GP)
PG4504 Do Not Stuff (GP)
PG4506 Do Not Stuff (GP)
PG4508 Do Not Stuff (GP)

3D3V_AUX_S5

PR4501 Do Not Stuff (DY)
PR4502 Do Not Stuff (DY)
PR4503 0R2J-2-GP — PWR_5V_EN1_R — PWR_5V_EN1
PR4504 0R2J-2-GP
PR4505 0R2J-2-GP — PWR_3D3V_EN1
PWR_3V5V_EN

PWR_3D3V — 3D3V_S5

PG4532 PG4533 PG4534 PG4535 PG4536 PG4537 PG4538 PG4539 0R2J-2-GP

MAX:10260
TPE:7560

PR4506 0R3J-0-U-GP — PWR_3D3V_BOOT — PWR_3D3V_BOOT_A
PC4502 SCD1U25V2KX-1-DL-GP

MagLayer. 4.9 x 4.7 x 3.0mm
DCR: 13~14mOhm
Idc : 7A , Isat : 11A

Design Current=6.5A
OCP>9.75A

PU4501 SY8288BRAC-GP 074.08288.0A43
IN#2 IN#3 IN#4 IN#5 — LX#6 LX#19 LX#20 — PWR_3D3V_PH
EN1 EN2 — PWR_3D3V_EN1 PWR_3D3V_EN2
BS PG FF OUT LDO — PWR_3D3V_BOOT PWR_3V_PG PWR_3D3V_FB
NC#10 NC#15 NC#16 — PWR_3V_PG
GND GND GND GND
PWR_3D3V_LDO

PL4501 COIL-1UH-73-GP 68.1R010.20R

PC4501 SC1U10V2KX-1DLGP
PC4515 SC1U10V6KX-3-GP
PC4516 SC1U10V6KX-3-GP
PC4502 SC1U10V2KX-1DLGP
PC4501 SC1U10V2KX-1DLGP
PC4503 SC1U10V6KX-3DLGP
PC4504 SC22U6D3V3MX-1-DL-GP
PC4505 SC22U6D3V3MX-1-DL-GP
PC4506 SC22U6D3V3MX-1-DL-GP
PC4508 Do Not Stuff (DY)

PC4509 Do Not Stuff (DY)
PR4507 1MR2F-GP
PR4508 1KR2J-1-GP
PC4512 Do Not Stuff (DY)
PR4510 100KR2F-L1-GP — 3D3V_S5
OPEN DRAIN

PG4511 Do Not Stuff — 3D3V_AUX_S5
PC4510 SC4D7U6D3V3KX-DLGP

Trace used 10 mil

PC4511 SC1K50V2KX-1DLGP
PR4509 1KR2F-L-GP
PR4555 Do Not Stuff (DY)
R4501 0R1J-GP (DY)

EN rating 25V
EN Rising Threshold : 0.8V
Ilimt : 12A

Q4501 NTK3139PT1G-GP (DY)
84.03139.031

SIO_SLP_S0#

DCBATOUT — PWR_DCBATOUT_5V

PG4515 PG4517 PG4520 PG4523 0R2J-2-GP

DCBATOUT — FC4507 SC1U25V2KX-2-GP

PWR_5V — 5V_S5

PG4516 PG4519 PG4521 PG4522 PG4525 PG4529 PG4531 0R2J-2-GP

MAX:8850
TPE:7695

3D3V_S5
OPEN DRAIN
PR4511 Do Not Stuff (DY)
PR4512 0R3J-0-U-GP — PWR_5V_PG — PWR_5V_BOOT1 — PWR_5V_BOOT_A
PC4513 SCD1U25V2KX-1-DL-GP

MagLayer. 7.3 x 6.6 x 2.2mm
DCR: 11.2~13.5mOhm
Idc : 9A , Isat : 16A

Design Cureent= 7.1A
OCP>10.65A

PU4502 SY8288CRAC-GP 074.08288.0B43
PG — PWR_5V_PG
BS — PWR_5V_BOOT1
LX#6 LX#19 LX#20 — PWR_5V_PH
OUT — PWR_5V_VOUT
FF — PWR_5V_FB
LDO — PWR_5V_LDO
NC#10 NC#16
VCC — PWR_5V_VCC
EN1 EN2 — PWR_5V_EN1 PWR_5V_EN2
GND GND GND GND

PL4502 IND-1UH-186-GP 68.1R01E.10A

PWR_5V_FB_A

PC4506 SC1U25V2KX-1-DL-GP
PC4505 Do Not Stuff (DY)
PC4517 SC10U25V2KX-1-DL-GP
PC4514 SC10U25V2MX-3-GP
PC4540 SC10U25V2MX-3-GP
PC4526 SC2D2U10V3KX-1DLGP-U
PC4528 Do Not Stuff (DY)
PR4514 1MR2F-GP
PR4515 1KR2J-1-GP — DCBATOUT
PC4530 Do Not Stuff (DY)

Trace used 10 mil

PG4527 Do Not Stuff (GP)
PC4527 SC1KP50V2KX-1DLGP
PR4513 1KR2F-L-GP
PG4530 Do Not Stuff (GP) — 5V_AUX_S5
PC4529 SC4D7U6D3V3KX-DLGP

PC4504 Do Not Stuff (DY)
PC4503 Do Not Stuff (DY)
PC4518 SC10U16V2KX-3DLGP
PC4519 SC22U6D3V3MX-1-DL-GP
PC4520 SC22U6D3V3MX-1-DL-GP
PC4521 SC22U6D3V3MX-1-DL-GP
PC4522 SC22U6D3V3MX-1-DL-GP
PC4523 SC22U6D3V3MX-1-DL-GP

EN rating 25V
EN Rising Threshold : 0.8V
Ilimt : 12A

PWR_5V_FB — PR4551 560KR2F-GP

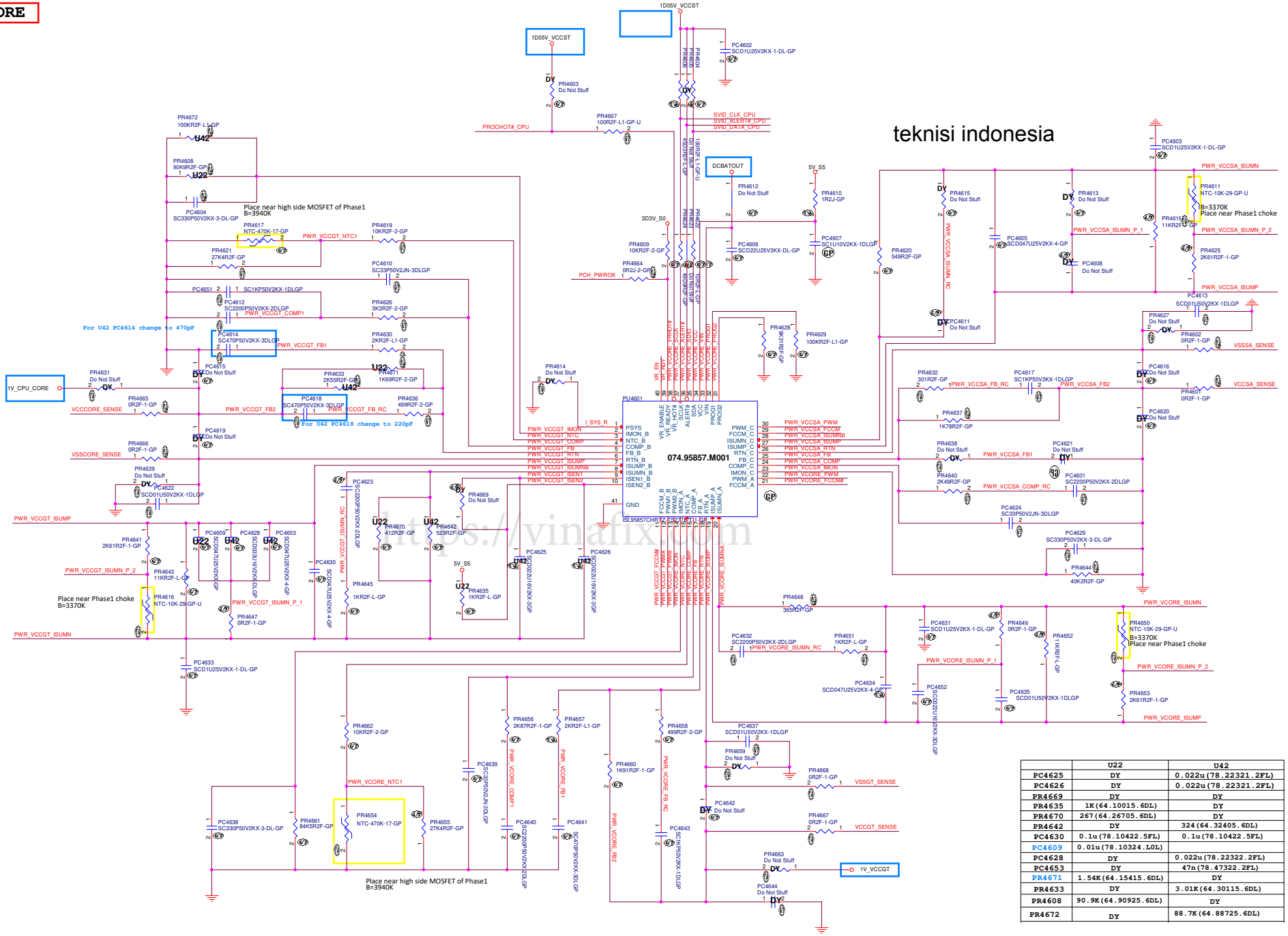
20171228 EE request

ALL

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	5V/3D3V	
Size: Custom	Document Number: Fircrest 13"	Rev: X01
Date: Thursday, April 18, 2019	Sheet 45 of 106	

Main Func = CPU_CORE



	U22	U42
PC4625	DY	0.022u(78.22321.2FL)
PC4626	DY	0.022u(78.22321.2FL)
PR4669	DY	DY
PR4635	1K(64.10015.6DL)	DY
PR4670	267(64.26705.6DL)	DY
PR4642	DY	324(64.32405.6DL)
PC4630	0.1u(78.10422.5FL)	0.1u(78.10422.5FL)
PC4609	0.01u(78.10324.L0L)	
PC4628	DY	0.022u(78.22322.2FL)
PC4653	DY	47n(78.47322.2FL)
PR4671	1.54K(64.15415.6DL)	DY
PR4633	DY	3.01K(64.30115.6DL)
PR4608	90.9K(64.90925.6DL)	DY
PR4672	DY	88.7K(64.88725.6DL)

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95859C_CPU_VCORE(1/3)

Size: A2 | Document Number: Fircrest 13" | Rev: X01

Date: Thursday, April 18, 2019 | Sheet 46 of 106

Main Func = CPU_CORE

[46] PWR_VCORE_PWM >>>—
[46] PWR_VCORE_FCCM# >>>—
[46] PWR_VCORE_ISUMP <<<—
[46] PWR_VCORE_ISUMN <<<—

DCBATOUT
PWR_DCBATOUT_VCORE
PL4702 HCB2012KF-800T50-GP-U 68.00216.191
PL4703 HCB2012KF-800T50-GP-U 68.00216.191

PWR_DCBATOUT_VCORE
LOW NOISE CAP
PC4701 PC4702 PC4703 PC4704 SC10U25V3KX-GP
EC4701 SCD1U25V2KX-1-DL-GP

For acoustic noice
PWR_DCBATOUT_VCORE
SA 1103
PT4702 ST100U25VDM-1-GP 077.C1071.0071

MAX:31000
TPE:21700

5V_S5
PC4766 SC1U10V2KX-1DLGP
PR4704 2D2R2F-GP
PWR_VCORE_VCC_R
PC4708 SC1U10V2KX-1DLGP

CYNTEC. 7*7*3
DCR: 0.90mohm +/-7%
Idc : 37 A , Isat : 41A

PU4701
PWR_DCBATOUT_VCORE
VCC VIN VIN VIN VIN VIN PVCC PWM FCCM GL#27 GL#35 BOOT PHASE NC#6 NC#30 NC#31
SW#16 SW#17 SW#18 SW#19 SW#20 SW#21 SW#22 SW#23 SW#24 SW#25 SW#26
PGND AGND
PWR_VCORE_SW
FDMF3035-GP
074.03035.0073

PL4701 COIL-D15UH-7-GP
1V_VCCGT
PT4701 ST330U2D5VBM-1-GP

PWR_VCORE_PWM PR4702 Do Not Stuff PWR_VCORE_PWM_R
PWR_VCORE_FCCM# PR4706 Do Not Stuff PWR_VCORE_FCCM#_R
PC4707 SCD22U25V3KX-DL-GP PWR_VCORE_BOOT_RC
PR4705 2D2R3-1-U-GP PWR_VCORE_BOOT PWR_VCORE_BOOTRA
TP4701 GL#35_TP1

DY PR4703 Do Not Stuff PWR_VCORE_SNB
DY PC4706 Do Not Stuff

PG4707 Do Not Stuff PWR_VCORE_ISUMP_G
PG4708 Do Not Stuff PWR_VCORE_ISUMN_G
PR4708 3K65R2F-1-GP PWR_VCORE_ISUMP
PR4701 Do Not Stuff PWR_VCORE_ISUMN

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95859C_CPU_VCORE(2/3)
Size: Custom | Document Number: Fircrest 13" | Rev: X01
Date: Thursday, April 18, 2019 | Sheet 47 of 106

Main Func = CPU_CORE

[46] PWR_VCCGT_PWMA
[46] PWR_VCCGT_FCCM#
[46] PWR_VCCGT_ISEN1
[46] PWR_VCCGT_ISUMP
[46] PWR_VCCGT_ISUMN
[46] PWR_VCCGT_ISEN2
[46] PWR_VCCGT_PWMB

DCBATOUT
PWR_DCBATOUT_VCCGTA
PL4803 HCB2012KF-800T50-GP-U 68.00216.191
PL4804 HCB2012KF-800T50-GP-U 68.00216.191

PWR_DCBATOUT_VCCGTA
LOW NOISE CAP
PC4802 PC4803 PC4804 PC4805 SC10U25V3KX-GP
EC4802 EC4803 SCD1U25V2KX-1-DL-GP

For acoustic noice
PWR_DCBATOUT_VCCGTA
PT4805 ST100U25VDM-1-GP 077.C1071.0071

1V_CPU_CORE
FC4801 FC4802 FC4803 DY Do Not Stuff

MAX : 70000
TPE : 49000

5V_S5
PC4877 SC1U10V2KX-1DLGP
PR4803 2D2R2F-GP
PWR_VCCGT_VCCDA
PC4809 SC1U10V2KX-1DLGP

teknisi indonesia

CYNTEC. 7*7*3
DCR: 0.90mohm +/-7%
Idc : 37 A , Isat : 41A

PU4801
PWR_DCBATOUT_VCCGTA
VCC VIN PVCC PWM FCCM BOOT PHASE GL#27 GL#35 NC#6 NC#30 NC#31 PGND AGND
SW#16 SW#17 SW#18 SW#19 SW#20 SW#21 SW#22 SW#23 SW#24 SW#25 SW#26
PWR_VCCGT_SWA
FDMF3035-GP
074.03035.0073

PR4805 Do Not Stuff PWR_VCCGT_SNB1
PC4810 Do Not Stuff

PL4801 COIL-D15UH-7-GP 068.R1510.2041
1V_CPU_CORE
PT4801 ST330U2D5VBM-1-GP
PG4808 Do Not Stuff
PG4809 Do Not Stuff

PWR_VCCGT_PWMA PR4802 Do Not Stuff PWR_VCCGT_PWMA_RA
PWR_VCCGT_FCCM# PR4806 Do Not Stuff PWR_VCCGT_FCCM#_RA
TP4801 GL#35_GT1
PC4808 SCD22U25V3KX-DL-GP PWR_VCCGT_BOOTA_RC PR4804 2D2R3-1-GP
PWR_VCCGT_BOOTA PWR_VCCGT_BOOTRA

PWR_VCCGT_ISEN1 U42 PR4821 100KR2F-L1-GP
PWR_VCCGT_ISUMP PR4808 3K65R2F-1-GP
PWR_VCCGT_ISUMN
PWR_VCCGT_ISEN2
PWR_VCCGT_ISUMP_GA
PWR_VCCGT_ISUMN_GA
PR4809 10R2F-L-GP
PR4822 Do Not Stuff DY

PWR_DCBATOUT_VCCGTA
LOW NOISE CAP
U42 PC4816 PC4817 PC4814 PC4815 SC10U25V3KX-GP

5V_S5
PC4866 SC1U10V2KX-1DLGP
U42 PR4813 2D2R2F-GP
PWR_VCCGT_VCCDB
U42 PC4812 SC1U10V2KX-1DLGP

PU4802
PWR_DCBATOUT_VCCGTA
VCC VIN PVCC PWM FCCM BOOT PHASE GL#27 GL#35 NC#6 NC#30 NC#31 PGND AGND
SW#16 SW#17 SW#18 SW#19 SW#20 SW#21 SW#22 SW#23 SW#24 SW#25 SW#26
PWR_VCCGT_SWB
FDMF3035-GP
074.03035.0073

PR4814 Do Not Stuff PWR_VCCGT_SNB2
PC4813 Do Not Stuff

CYNTEC. 7*7*3
DCR: 0.90mohm +/-7%
Idc : 37 A , Isat : 41A

PL4802 COIL-D15UH-7-GP U42 068.R1510.2041
1V_CPU_CORE
PT4803 SE470UF2VDM-GP 79.47719.2BL
PG4813 Do Not Stuff
PG4815 Do Not Stuff

PWR_VCCGT_PWMB PR4811 Do Not Stuff PWR_VCCGT_PWMB_RB
PWR_VCCGT_FCCM# PR4812 Do Not Stuff PWR_VCCGT_FCCM#_RB
TP4802 GL#35_GT2
PC4811 U42 SCD22U25V3KX-DL-GP PWR_VCCGT_BOOTB_RC PR4810 2D2R3-1-GP U42 PWR_VCCGT_BOOTB PWR_VCCGT_BOOTRB

PWR_VCCGT_ISEN2 U42 PR4823 100KR2F-L1-GP
PWR_VCCGT_ISUMP U42 PR4816 3K65R2F-1-GP
PWR_VCCGT_ISUMN
PWR_VCCGT_ISEN1
PWR_VCCGT_ISUMP_GB
PWR_VCCGT_ISUMN_GB
PR4817 10R2F-L-GP U42
PR4824 Do Not Stuff DY

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95859C_CPU_VCCGT(3/3)
Size: Custom
Document Number: Fircrest 13"
Rev: X01
Date: Thursday, April 18, 2019
Sheet 48 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81210MN_CPU_VCCGTUS

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 49 of 106

Main Func = CPU_VCCSA

[46] PWR_VCCSA_PWM
[46] PWR_VCCSA_ISUMP
[46] PWR_VCCSA_ISUMN
[46] PWR_VCCSA_FCCM

DCBATOUT
PWR_DCBATOUT_VCCSA
PG5002 Do Not Stuff
PG5003 Do Not Stuff

PWR_VCCSA_BST_RC
PR5001 2D2R3-1-U-GP
PC5005 SCD22U25V3KX-DL-GP
PU5001
PWR_VCCSA_DRVH
PWR_VCCSA_BST
PWR_VCCSA_PWM
UGATE
BOOT
PWM
GND
PHASE
FCCM
VCC
LGATE
GND
ISL95808HRZ-T-1-GP
074.95808.0B73
PWR_VCCSA_SW
PWR_VCCSA_FCCM
5V_S5
PC5001 SC2D2U10V3KX-1DLGP-U
PWR_VCCSA_DRVL

PC5002 SC10U25V3MX-3-GP
PC5003 SC10U25V3MX-3-GP
PC5004 SCD1U25V2KX-1-DL-GP
EC5001 SCD1U25V2KX-1-DL-GP
PU5002 AONH36334-GP
075.36334.M001

MAX : 6000
TPE : 4200

Cyntec. 4.85mm x4.7mm x3.0mm
DCR: 5.0~5.9mohm
Idc : 14A , Isat : 14.2A

1V_VCCSA
PL5001 COIL-D47UH-25-GP
068.R4710.2141
PG5011 Do Not Stuff
PG5001 Do Not Stuff

If no need support PS4 mode
please change to ISL6208C
74.06208.B73

PWR_VCCSA_SW
DY PR5002 Do Not Stuff
PWR_VCCSA_SW_C
DY PC5006 Do Not Stuff

PWR_VCCSA_ISUMP_R
PWR_VCCSA_ISUMN_R
PR5003 3K65R2F-1-GP
PR5004 Do Not Stuff
PWR_VCCSA_ISUMP
PWR_VCCSA_ISUMN

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VCCSA
Size: Custom
Document Number: Fircrest 13"
Rev: X01
Date: Thursday, April 18, 2019
Sheet 50 of 106

Main Func = Power_VDDQ/VTT/2D5V/0D6V

OFFPAGE

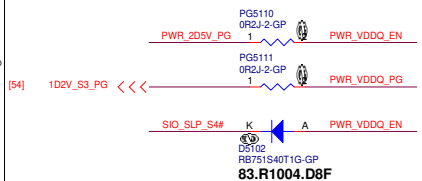
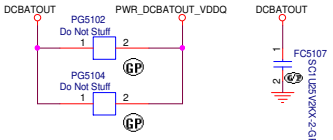


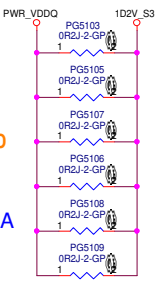
Table1. The Truth Table of S3 and S5 pins

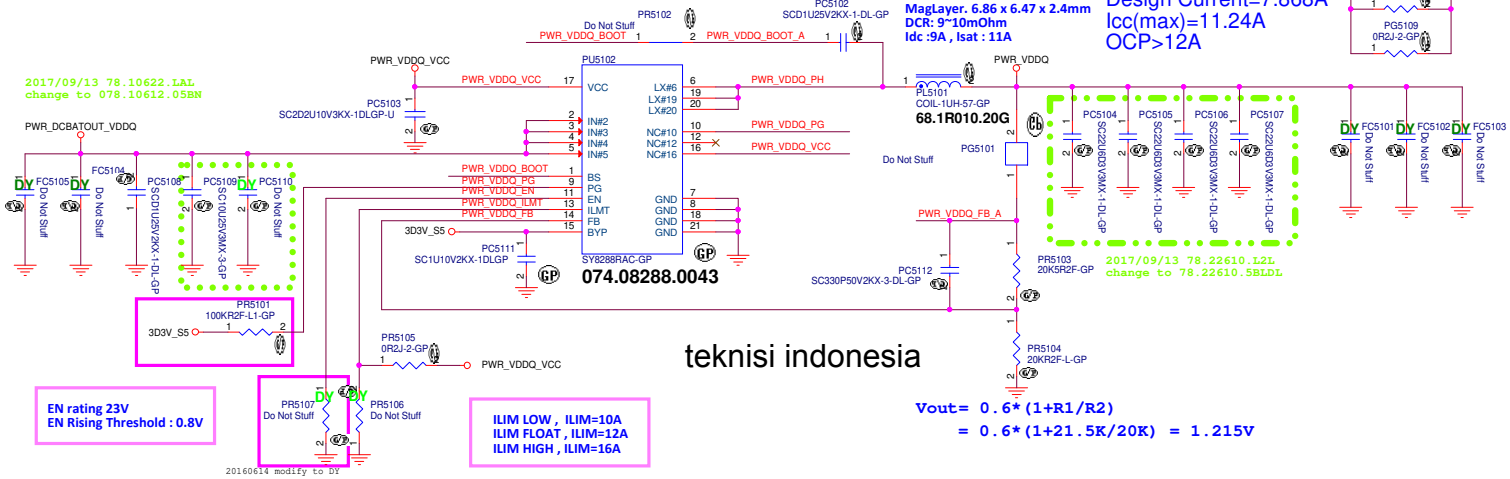
STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)



SY8288RAC for 1D2V

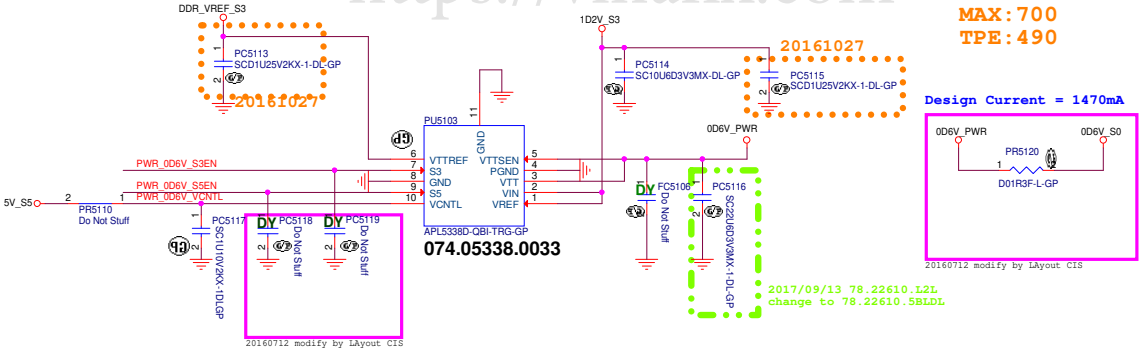
MAX:13300
TPE:9310

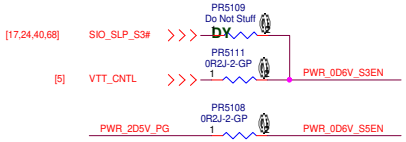




APL5338 for 0D6V

MAX:700
TPE:490

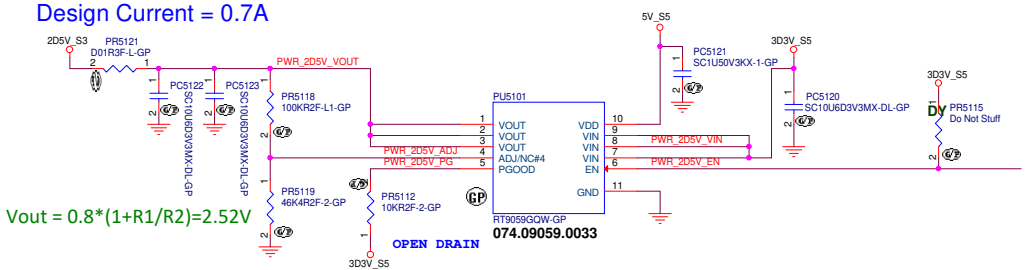


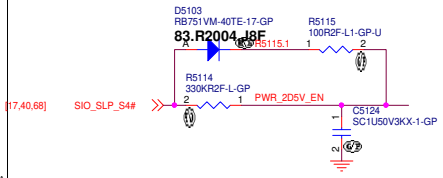


RT9059GQW for 2D5V

MAX:300
TPE:210

Design Current = 0.7A





ALL

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VDDQ/VTT

Size: Custom | Document Number: Fircrest 13" | Rev: X01

Date: Thursday, April 18, 2019 | Sheet 51 of 106

SSID = PWR.Plane.Regulator_1D05V

[24,53,54] S5_PG
[17,24,40,53,54] SIO_SLP_SUS#
[24,40,53,54] VCCDSW_EN

AOZ2260 for 1D05V

MAX:4326
TPE:3028.2

CYNTEC. 5*5*3
DCR: 12m~14mOhm
Idc : 9 A , Isat : 17A

Design Current : 4.5A

1D05V_PWR
PG5217 Do Not Stuff
PG5213 Do Not Stuff
PG5215 Do Not Stuff
PG5216 Do Not Stuff
1D05V_S5

DCBATOUT
PG5214 Do Not Stuff
PG5210 Do Not Stuff
PWR_DCBATOUT_1D0V

5V_S5
PC5202 SC4D7U6D3V3KX-DLGP

PU5201
AOZ2260QI-10-GP
074.02260.0043

21	VCC	
7	IN	
8	IN	
9	IN	
6	TON	
1	PGOOD	
2	EN	
3	PFM#	
22	SS	
	LX#18	18 PWR_1D05V_PH
	LX#17	17
	LX#16	16
	LX#11	11
	LX#10	10
	BST	20 PWR_1D05V_BT
	FB	5 PWR_1D05V_FB
	AGND	4
	PGND	19
	PGND	14
	PGND	13
	PGND	12
	PGND	15

PC5204 SCD1U25V2KX-1-DL-GP

PL5201 COIL-1UH-104-GP
068.1R010.2141

PG5223 Do Not Stuff

PWR_1D05V_FB_A

PR5201 88K7R2F-GP
PR5203 100KR2F-L1-GP
PC5213 SCD01U50V2KX-1DLGP

PR5202 3K16R2F-GP R1
PC5212 SC220P50V2KX-3DLGP
PR5204 10KR2F-2-GP R2

Vo=0.8x(1+R1/R2)
=0.8x(1+3.16/10)
=1.0528V

PWR_DCBATOUT_1D0V
PC5214 SCD1U50V3KX-DL-GP
PC5216 DY Do Not Stuff
PC5211 DY Do Not Stuff
PC5210 SC10U25V3MX-3-GP
PC5209 SC10U25V3MX-3-GP

1D05V_PWR
PC5203 SC22U6D3V3MX-1-DL-GP
PC5205 SC22U6D3V3MX-1-DL-GP
PC5201 SC22U6D3V3MX-1-DL-GP
PC5206 DY Do Not Stuff
EC5202 SCD1U25V2KX-1-DL-GP

PWR_1D05V_PH
PR5205 DY Do Not Stuff
PWR_1D05V_PH_Q
PC5217 DY Do Not Stuff

3D3V_S5
PR5208 100KR2J-1-GP
PR5209 0R2J-2-GP
S5_PG → PWR_1D05V_PG
PR5210 150KR2F-L-GP
SIO_SLP_SUS# DS
PR5211 150KR2F-L-GP
VCCDSW_EN NON_DS
PWR_1D05V_EN
PC5215 SCD1U16V2KX-3DLGP

Rail 1	Rail 2	Ramp Up
VPRIM_CORE	VCC _PRIM 1.0 V (Note 1)	VCCPRIM_CORE rail must ramp before or equal to the Primary 1.0 V rails. VCCPRIM_CORE voltage should be >= VCC_Prim 1.0 V until VCCPRIM_CORE voltage reaches 95% of its final value.

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)
Size: Custom
Document Number: Fircrest 13"
Rev: X01
Date: Thursday, April 18, 2019
Sheet 52 of 106

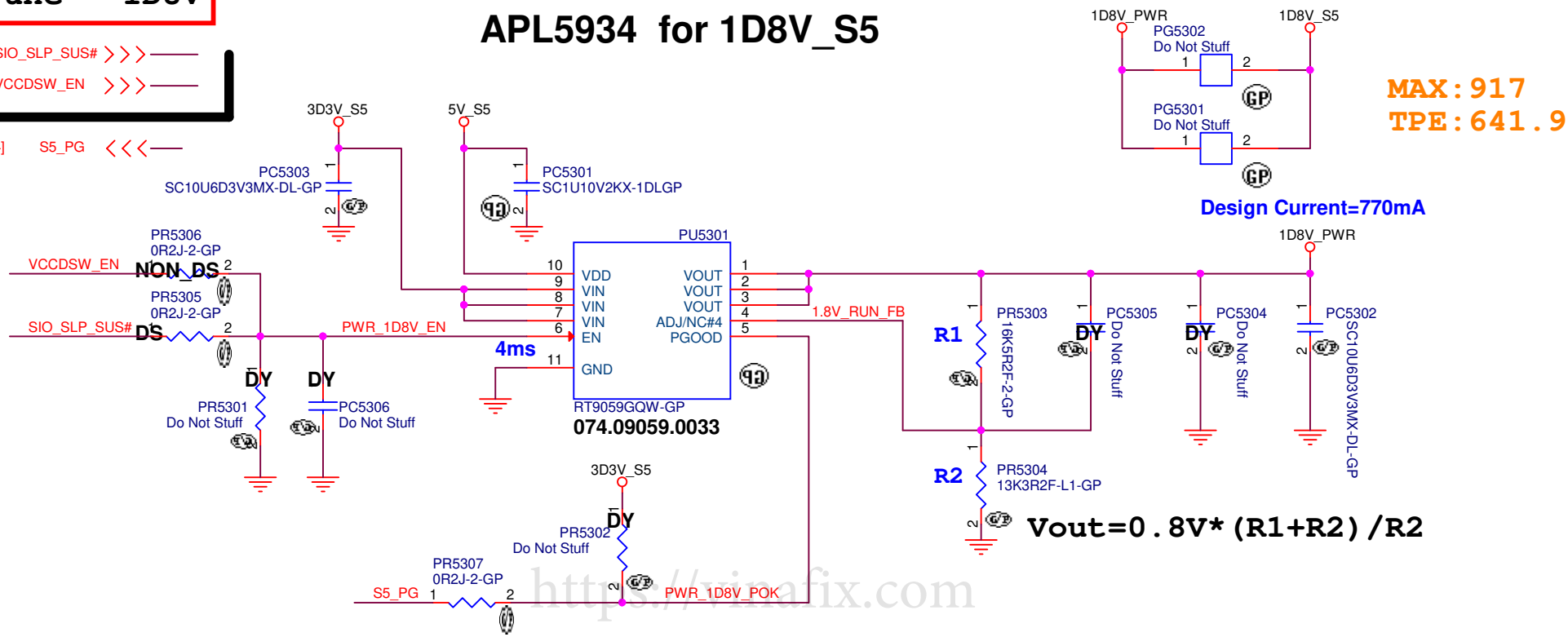
Main Func = 1D8V

APL5934 for 1D8V_S5

[17,24,40,52,54] SIO_SLP_SUS#

[24,40,52,54] VCCDSW_EN

[24,52,54] S5_PG



ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 53 of 106

Main Func = VCCIO / VCCPRIM

[8] VCCIO_SENSE
[8] VSSIO_SENSE
[24,40,57] RUN_ON_R
[51] 1D2V_S3_PG
[21,24,40,91] CPU_C10_GATE#
[17,40,68,91] SIO_SLP_S0#
[24,40,52,53] VCCDSW_EN
[17,24,40,52,53] SIO_SLP_SUS#
[22] PRIMCORE_G0
[22] PRIMCORE_G1
[20] PRIM_CORE_OPT_DIS
[24,52,53] S5_PG

VCCIO

Chillisin. 2.5*2.0*1.2
DCR: 29~39mohm
Idc : 4.4 A , Isat : 7.8A

PU5401 SY8057BQDC-GP 074.08057.0B43
PL5401 IND-D47UH-92-GP 068.R471.0.1101

MAX:1000
TPE:700

EV2 test use RC solution

LP PIN= HIGH, VCCIO= 0.95V
LP PIN = LOW, VCCIO=0V

U5402 U74LVC1G08G-AL5-R-GP-U 73.01G08.EHG 2ND = 73.7SZ08.DAH

VCCPRIM_CORE

CYNTEC. 4*4*2
DCR: 24~27mohm
Idc : 4.5A , Isat : 7A

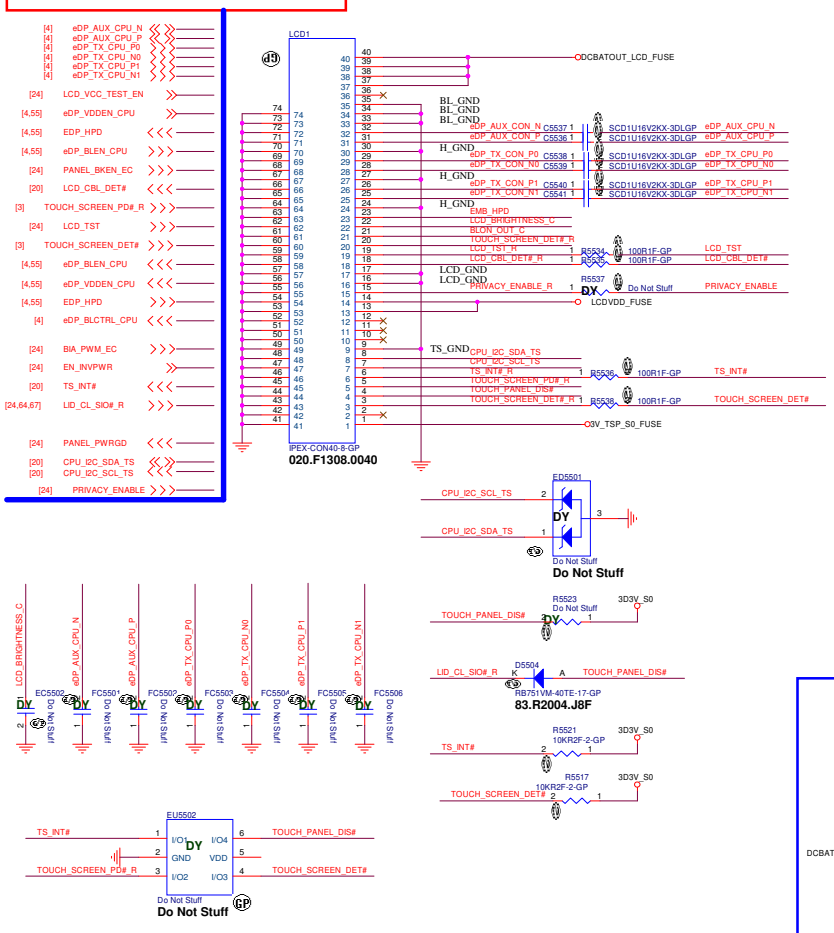
PU5402 SY8057CQDC-GP 074.08057.0C43
PL5402 IND-1UH-129-GP-U 68.1R010.20D

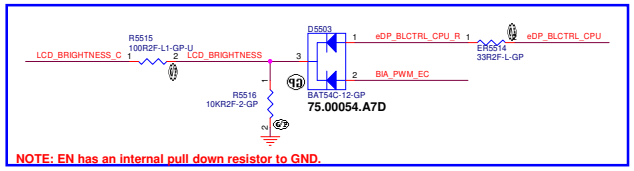
MAX:4260
TPE:2982

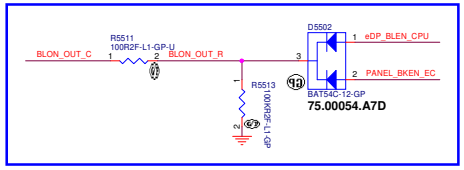
LP PIN= HIGH, PRIMCORE= 1.05V
LP PIN = LOW, PRIMCORE=0.75V

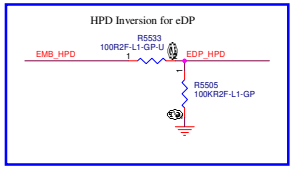
ALL			
Title	<Title>		
Size A3	Document Number Fircrest 13"		Rev X01
Date: Thursday, April 18, 2019	Sheet 54 of 106		

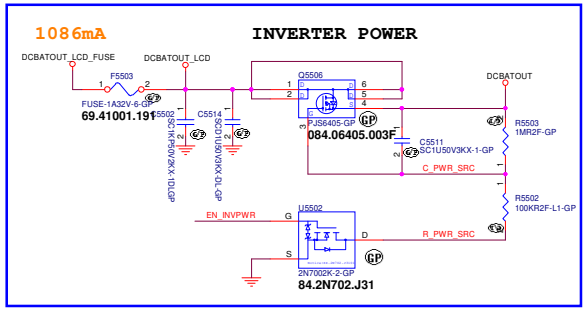
Main Func = LCD/Touch

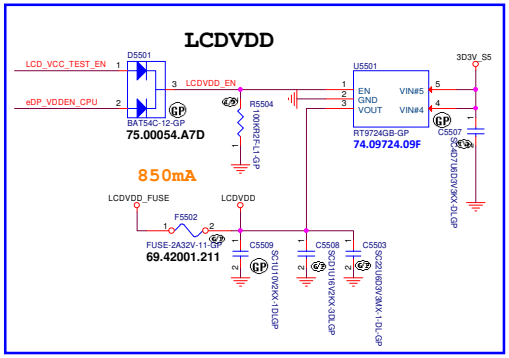


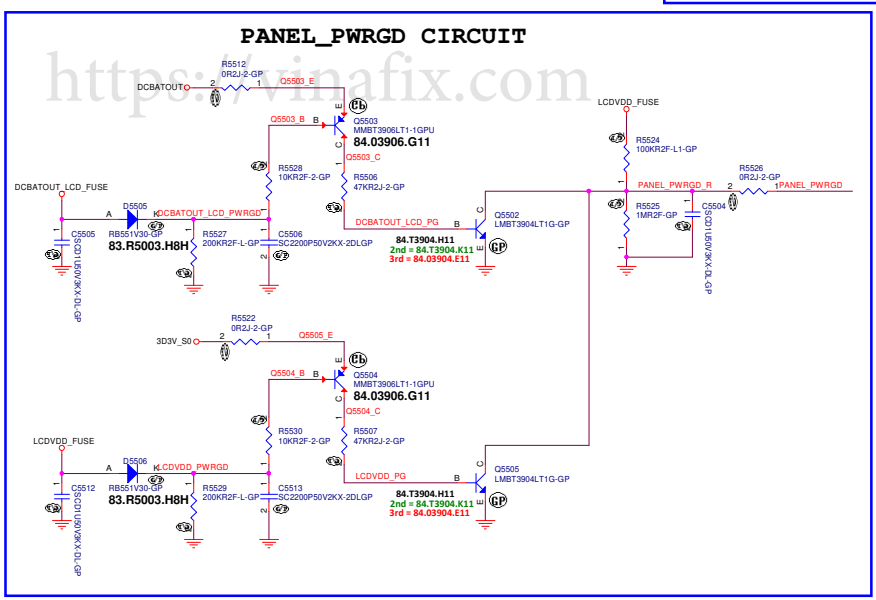












ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (LCD/Inverter)

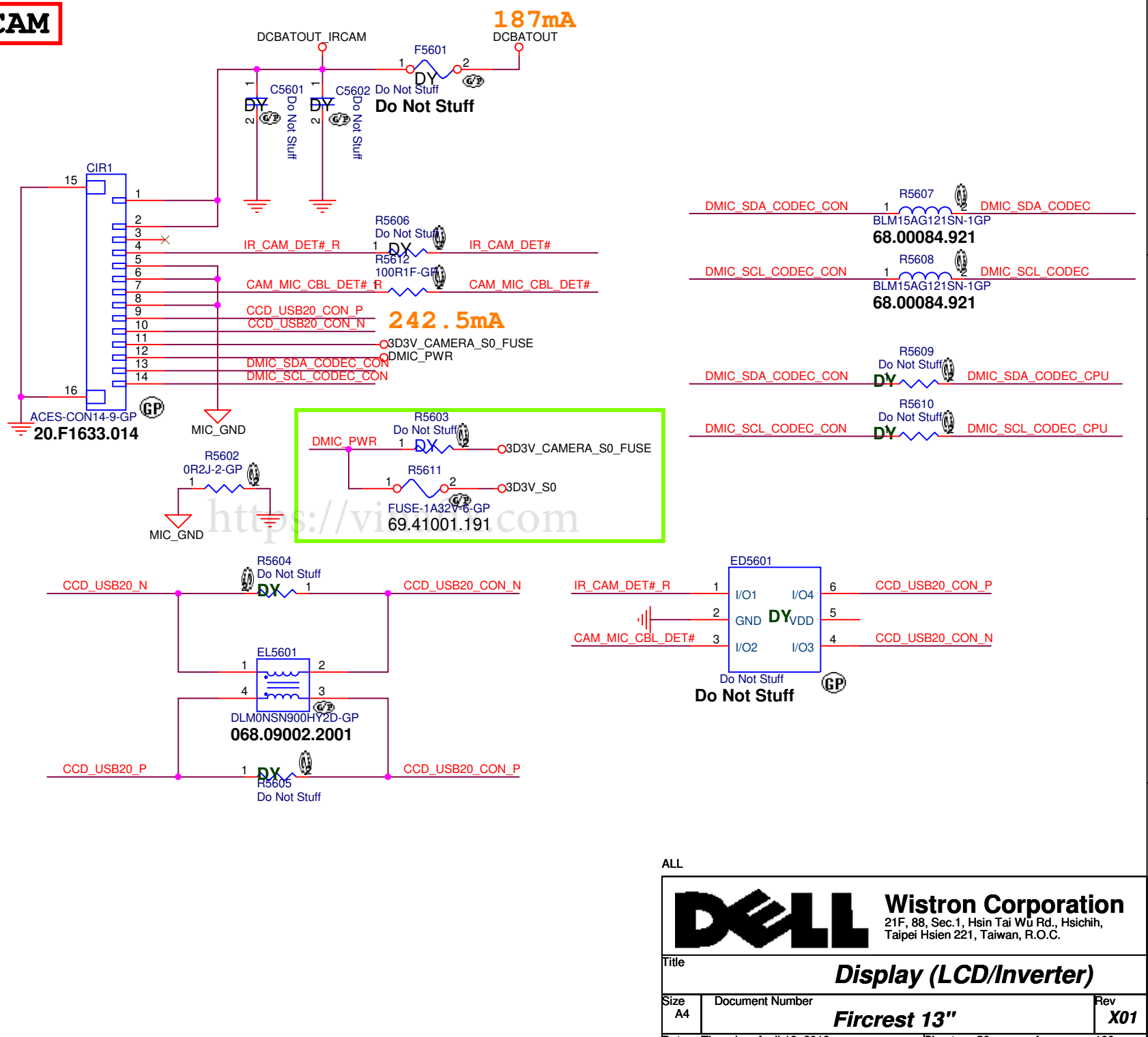
Size	Document Number	Rev
A2	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 55 of 106

Main Func = IR CAM

CAMERA

[16] CCD_USB20_N
[16] CCD_USB20_P
[27] DMIC_SDA_CODEC
[27] DMIC_SCL_CODEC
[20] IR_CAM_DET#
[19] CAM_MIC_CBL_DET#
[19] DMIC_SDA_CODEC_CPU
[19] DMIC_SCL_CODEC_CPU



ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (LCD/Inverter)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 56 of 106

Main Func = HDMI

[4] HDMI_DDI_TX_P2
[4] HDMI_DDI_TX_N2
[4] HDMI_DDI_TX_P1
[4] HDMI_DDI_TX_N1
[4] HDMI_DDI_TX_P0
[4] HDMI_DDI_TX_N0
[4] HDMI_DDI_TX_P3
[4] HDMI_DDI_TX_N3
[4] HDMI_DET_CPU
[4] HDMI_SCL_CPU
[4] HDMI_SDA_CPU
[24,40,54] RUN_ON_R

1D2V_HDMI

1D2V_HDMI_R — L5702 BLM18KG331SN1D-GP — 1D2V_HDMI
500mA
C5716 Do Not Stuff, 5V_S5
U5703 APE8910GN3B-GP 074.08910.0093
VBIAS, VOUT1#13, VOUT1#14, VIN1#1, VIN1#2, VOUT2#8, VOUT2#9, VIN2#6, VIN2#7, CT1, CT2, ON1, ON2, GND, GND
1D2V_S3, U4005_CT2, C5725 SC470P50V2KX-3DLGP
RUN_ON_R, R5715 0R2J-2-GP, 1D2V_HDMI_EN, C5726 SC470P50V2KX-3DLGP Do Not Stuff

1D2V_HDMI — FC5703 Do Not Stuff — FC5702 Do Not Stuff

HDMI CONNECTOR

3D3V_S5
Close to Pin11 — C5717 SCD1U16V1KX-GP — Close to Pin37 — C5718 SCD01U50V2KX-1DLGP
Close to Pin40 — C5719 SCD1U16V1KX-GP — Close to Pin12 — C5720 SCD01U50V2KX-1DLGP
Close to Pin20 — C5721 SCD1U16V1KX-GP — Close to Pin31 — C5722 SCD01U50V2KX-1DLGP
Close to Pin19 — C5723 SCD1U16V1KX-GP — C5724 SCD1U16V1KX-GP
1D2V_HDMI

U5702 PS8407ATQFN40GTR2-A1-GP 071.08407.0003

VDD33		OUT_D0P	HDMI_DDI_TX_CMC_P0
VDD33		OUT_D0N	HDMI_DDI_TX_CMC_N0
VDDRX		OUT_D1P	HDMI_DDI_TX_CMC_P1
VDDRX		OUT_D1N	HDMI_DDI_TX_CMC_N1
		OUT_D2P	HDMI_DDI_TX_CMC_P2
		OUT_D2N	HDMI_DDI_TX_CMC_N2
VDDTX			
VDDTX		OUT_CKP	HDMI_DDI_TX_CMC_P3
		OUT_CKN	HDMI_DDI_TX_CMC_N3
VDDTA			
		I2C_CTL_EN	PS8407A_EQ
IN_D0P	C5706 1 SCD1U16V1KX-GP	EQ/I2C_ADDR0	PS8407A_CFG
IN_D0N	C5707 1 SCD1U16V1KX-GP	CFG/I2C_ADDR1	
IN_D1P	C5704 1 SCD1U16V1KX-GP		PS8407A_PRE
IN_D1N	C5705 1 SCD1U16V1KX-GP	PRE	PS8407A_ISET
IN_D2P	C5702 1 SCD1U16V1KX-GP	ISET	
IN_D2N	C5703 1 SCD1U16V1KX-GP	PD#	
IN_CKP	C5708 1 SCD1U16V1KX-GP	DCIN_EN/SCL_CTL	PS8407A_DCIN_EN
IN_CKN	C5709 1 SCD1U16V1KX-GP	DDCBUF/SDA_CTL	PS8407A_DDCBUF
SCL_SRC	HDMI_SCL_CPU	SCL_SNK	HDMI_SCL_CON
SDA_SRC	HDMI_SDA_CPU	SDA_SNK	HDMI_SDA_CON
HPD_SRC	HDMI_DET_CPU		
HPD_SNK	HDMI_DET_CON		
		GND	
		GND	
REXT	PS8407A_REXT	GND	

R5701 4K02R2F-GP
R5743 Do Not Stuff

3D3V_S5 — R5702 Do Not Stuff — PS8407A_DCIN_EN
3D3V_S5 — R5711 Do Not Stuff — PS8407A_CFG
3D3V_S5 — R5707 4K7R2F-GP — PS8407A_DDCBUF
3D3V_S5 — R5714 Do Not Stuff — PS8407A_EQ
3D3V_S5 — R5708 Do Not Stuff — PS8407A_PRE
3D3V_S5 — R5713 Do Not Stuff — PS8407A_ISET
3D3V_S5 — R5709 Do Not Stuff — PS8407A_PRE
3D3V_S5 — R5717 Do Not Stuff — PS8407A_ISET
R5710 Do Not Stuff
R5716 Do Not Stuff

5V_S0 — R5734 0R2J-2-GP — 5V_S0_HDMI_IN
5V_S5 — R5733 Do Not Stuff
2017/11/22 Brad request
R5727 Do Not Stuff — 5V_HDMI
U5704 APL3517-AI-TRG-GP 74.03517.07B
VIN, VOUT, GND
C5710 SCD1U16V2KX-3DLGP
C5711 SC220R50V4MX-1DLGP, C5713 SC220R50V4MX-1DLGP, C5712 SCD1U16V2KX-3DLGP

HDMI_DET_CON — R5729 0R2J-2-GP — HDMI_DET_CON_R
EC5702 Do Not Stuff
R5732 20KR2F-L-GP

5V_HDMI
D5701 LBAW56LT1G-GP 83.00056.Y11
HDMI_SDA_R, HDMI_SCL_R
RN5704 SRN2K2J-1-GP
HDMI_SDA_CON, HDMI_SCL_CON

R5735 0R2J-2-GP — HDMI_DDI_TX_CMC_P2 — HDMI_DDI_TX_CON_P2
EL5702 Do Not Stuff — R5703 200R2F-L-GP
R5736 0R2J-2-GP — HDMI_DDI_TX_CMC_N2 — HDMI_DDI_TX_CON_N2
R5737 0R2J-2-GP — HDMI_DDI_TX_CMC_P1 — HDMI_DDI_TX_CON_P1
EL5704 Do Not Stuff — R5704 200R2F-L-GP
R5738 0R2J-2-GP — HDMI_DDI_TX_CMC_N1 — HDMI_DDI_TX_CON_N1

R5741 0R2J-2-GP — HDMI_DDI_TX_CMC_P0 — HDMI_DDI_TX_CON_P0
EL5705 Do Not Stuff — R5705 200R2F-L-GP
R5742 0R2J-2-GP — HDMI_DDI_TX_CMC_N0 — HDMI_DDI_TX_CON_N0
R5739 0R2J-2-GP — HDMI_DDI_TX_CMC_P3 — HDMI_DDI_TX_CON_P3
EL5703 Do Not Stuff — R5706 200R2F-L-GP
R5740 0R2J-2-GP — HDMI_DDI_TX_CMC_N3 — HDMI_DDI_TX_CON_N3

ED5701 Do Not Stuff
HDMI_DDI_TX_CON_P2 ↔ HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N2 ↔ HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_CON_P1 ↔ HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N1 ↔ HDMI_DDI_TX_CON_N1
ED5702 Do Not Stuff
HDMI_DDI_TX_CON_P0 ↔ HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N0 ↔ HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_CON_P3 ↔ HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N3 ↔ HDMI_DDI_TX_CON_N3
Do Not Stuff

5V_HDMI — HDMI1 (HDMI (A_Type)) SKT-HDMI23-193-GP-U 022.10025.0321

+5V_POWER	18	SCL	HDMI_SCL_CON
		SDA	HDMI_SDA_CON
TMDS_DATA0+	HDMI_DDI_TX_CON_P0	CEC	TP_HDMIC_OB_CEC
TMDS_DATA0-	HDMI_DDI_TX_CON_N0	DDC/CEC_GROUND	HDMI_DET_CON_R
TMDS_DATA1+	HDMI_DDI_TX_CON_P1	HOT_PLUG_DETECT	TP_UTILITY
TMDS_DATA1-	HDMI_DDI_TX_CON_N1	RESERVED#14	
TMDS_DATA2+	HDMI_DDI_TX_CON_P2		
TMDS_DATA2-	HDMI_DDI_TX_CON_N2		
TMDS_DATA0_SHIELD			
TMDS_DATA1_SHIELD			
TMDS_DATA2_SHIELD			
TMDS_CLOCK_SHIELD		GND	
TMDS_CLOCK+	HDMI_DDI_TX_CON_P3	GND	
TMDS_CLOCK-	HDMI_DDI_TX_CON_N3	GND	
		GND	

R5725 Do Not Stuff — 3D3V_S0
R5728 Do Not Stuff
AFTP5705 Do Not Stuff
HDMI_DET_CON_R, 5V_HDMI
AFTP5701 Do Not Stuff
AFTP5703 Do Not Stuff

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (HDMI Level Shifter/Conn)
Size: A2 | Document Number: Fircrest 13" | Rev: X01
Date: Thursday, April 18, 2019 | Sheet 57 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Display (RSVD) DP

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 58 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Display (RSVD) DVI*

Size	Document Number	Rev
A4	*Fircrest 13"*	*X01*

Date: Thursday, April 18, 2019 Sheet 59 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (RSVD)(HDD)*

Size	Document Number	Rev
A4	*Fircrest 13"*	*X01*

Date: Thursday, April 18, 2019 Sheet 60 of 106

Main Func = WLAN

WLAN

[16] WLAN_PCIE_RX_N
[16] WLAN_PCIE_RX_P
[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_TX_P

BT

[16] BT_USB20_N
[16] BT_USB20_P

CNVi

[21] CNV_WR_DN1
[21] CNV_WR_DP1
[21] CNV_WR_DN0
[21] CNV_WR_DP0
[21] CNV_WR_CLKN
[21] CNV_WR_CLKP
[21] CNV_WT_DN1
[21] CNV_WT_DP1
[21] CNV_WT_DN0
[21] CNV_WT_DP0
[21] CNV_WT_CLKN
[21] CNV_WT_CLKP
[20] CNV_BRI_RSP
[15,20] CNV_RGI_DT
[20] CNV_BRI_DT
[20] CNV_RGI_RSP
[19] CNV_RF_RESET#
[24] CNV_DET#

WLAN

[18] WLAN_CLK_CPU_P
[18] WLAN_CLK_CPU_N
[18] WLAN_CLKREQ_CPU_N
[24,62,63] PCIE_WAKE#_R
[21,62] CNV_COEX3
[21,62] CNV_MFUART2_TXD
[21,62] CNV_MFUART2_RXD
[18] CL_CLK
[18] CL_DATA
[18] CL_RST#
[19] CLKREQ_CNV
[24] WLAN_WIGIG60GHZ_DIS#
[24] BT_RADIO_DIS#
[18,63] SUSCLK
[17,33,62,91,97] PCH_PLTRST#_RIGHT
[18] PULSAR_38P4M_REFCLK
[19] CNV_EN
[16] BT_RADIO_DIS#_PCH

R6111 0R2J-2-GP
BT_USB20_P — EL6101 — BT_USB20_CON_P
BT_USB20_N — DY — BT_USB20_CON_N
Do Not Stuff
Do Not Stuff
R6113 0R2J-2-GP

WLAN_WIGIG60GHZ_DIS# — D6102 — WLAN_WIGIG60GHZ_DIS#_R
RB751VM-40TE-17-GP
83.R2004.J8F

BT_RADIO_DIS# — D6103 — BT_RADIO_DIS#_R
RB751VM-40TE-17-GP
83.R2004.J8F

BT_RADIO_DIS#_PCH — D6104
GD
RB751VM-40TE-17-GP
83.R2004.J8F

1D8V_S5 — DY R6143 Do Not Stuff — CNV_RGI_RSP
1D8V_S5 — DY R6144 Do Not Stuff — CNV_BRI_RSP
1D8V_S5 — DY R6145 Do Not Stuff — CNV_BRI_DT
CLKREQ_CNV — R6103 71K5R2F-1-GP

3D3V_SUS
R6120 10KR2F-2-GP
CNV_EN — R6125 Do Not Stuff — CNV_RF_RESET#_WLAN_N — R6119 0R2J-2-GP — CNV_DET#
U6102 PJA138KA-GP
084.00138.0A31
CNV_RF_RESET#_WLAN — R6118 0R2J-2-GP — CNV_RF_RESET#
R6102 75KR2F-GP

teknisi indonesia

1090mA

WLAN1
SKT-MINI67P-52-GP
062.10003.0F91

NP1		NP2	
1			
3	GND	2	3_3VAUX
5	USB_D+	4	3_3VAUX
7	USB_D-	6	LED#1
9	GND	8	PCM_CLK
11	SDIO_CLK	10	PCM_SYNC
13	SDIO_CMD	12	PCM_IN
15	SDIO_DAT0	14	PCM_OUT
17	SDIO_DAT1	16	LED#2
19	SDIO_DAT2	18	GND
21	SDIO_DAT3	20	UART_WAKE
23	SDIO_WAKE	22	UART_RX
	SDIO_RESET		
33	GND	32	UART_TX
35	PETP0	34	UART_RTS
37	PETN0	36	UART_CTS
39	GND	38	CLINK_RESET
41	PERP0	40	CLINK_DATA
43	PERN0	42	CLINK_CLK
45	GND	44	COEX3
47	REFCLKP0	46	COEX2
49	REFCLKN0	48	COEX1
51	GND	50	SUSCLK_32KHZ
53	CLKREQ0#	52	PERST0#
55	PEWAKE0#	54	RESERVED#54/W_DISABLE#2
57	GND	56	W_DISABLE#1
59	RESERVED#59/2ND_LANE_PETP1	58	NFC_I2C_SM_DATA
61	RESERVED#61/2ND_LANE_PETN1	60	NFC_I2C_SM_CLK
63	GND	62	NFC_I2C_IRQ/MGPIO5
65	RESERVED#65/2ND_LANE_PERP1	64	GPIO0_NFC_RESET#/MGPIO7
67	RESERVED#67/2ND_LANE_PERN1	66	RESERVED#66
69	GND	68	RESERVED#68
71	RESERVED#71	70	RESERVED#70
73	RESERVED#73	72	3_3VAUX
75	GND	74	3_3VAUX
77	77	76	

3D3V_S5_WLAN

BT_USB20_CON_P
BT_USB20_CON_N
CNV_WR_DN1 — R6114 0R2J-2-GP — CNV_WR_DN1_R
CNV_WR_DP1 — R6115 0R2J-2-GP — CNV_WR_DP1_R
CNV_WR_DN0 — R6116 0R2J-2-GP — CNV_WR_DN0_R
CNV_WR_DP0 — R6122 0R2J-2-GP — CNV_WR_DP0_R
CNV_WR_CLKN — R6123 0R2J-2-GP — CNV_WR_CLKN_R
CNV_WR_CLKP — R6124 0R2J-2-GP — CNV_WR_CLKP_R
WLAN_PCIE_TX_P — C6115 SCD1U16V2KX-3DLGP — WLAN_PCIE_TX_CON_P
WLAN_PCIE_TX_N — C6102 SCD1U16V2KX-3DLGP — WLAN_PCIE_TX_CON_N
WLAN_PCIE_RX_P
WLAN_PCIE_RX_N
WLAN_CLK_CPU_P
WLAN_CLK_CPU_N
WLAN_CLKREQ_CPU_N
WLAN_WAKE_N
PCIE_WAKE#_R — R6110 0R2J-2-GP
CNV_WT_DN1 — R6137 0R2J-2-GP — CNV_WT_DN1_R
CNV_WT_DP1 — R6138 0R2J-2-GP — CNV_WT_DP1_R
CNV_WT_DN0 — R6139 0R2J-2-GP — CNV_WT_DN0_R
CNV_WT_DP0 — R6140 0R2J-2-GP — CNV_WT_DP0_R
CNV_WT_CLKN — R6141 0R2J-2-GP — CNV_WT_CLKN_R
CNV_WT_CLKP — R6142 0R2J-2-GP — CNV_WT_CLKP_R

CNV_RF_RESET#_WLAN
CLKREQ_CNV
CNV_BRI_RSP
CNV_RGI_DT
CNV_RGI_RSP
CNV_BRI_DT
CL_RST#
CL_DATA
CL_CLK
WLAN_COEX3
WLAN_COEX2
WLAN_COEX1
SUS_CLK_WLAN
PLT_RST_N
BT_RADIO_DIS#_R
WLAN_WIGIG60GHZ_DIS#_R
PULSAR_38P4M_REFCLK_WLAN

R6132 DY Do Not Stuff — CNV_COEX3
R6133 DY Do Not Stuff — CNV_MFUART2_TXD
R6134 DY Do Not Stuff — CNV_MFUART2_RXD
R6135 33R2F-3-GP — SUSCLK
R6136 0R2J-2-GP — PCH_PLTRST#_RIGHT

PULSAR_38P4M_REFCLK_WLAN — ER6117 0R2J-2-GP — PULSAR_38P4M_REFCLK
R6121 DY Do Not Stuff

3D3V_S5_WLAN

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **INT IO (WLAN M.2)**
Size: A3
Document Number: **Fircrest 13"**
Rev: X01
Date: Thursday, April 18, 2019
Sheet 61 of 106

Main Func = WWAN

NGFF(WWAN/SSD)

WWAN
- [16] WWAN_USB31_RX_N
- [16] WWAN_USB31_RX_P
- [16] WWAN_USB31_TX_N
- [16] WWAN_USB31_TX_P

WWAN
- [16] WWAN_USB20_N
- [16] WWAN_USB20_P

WWAN
- [16] WWAN_SATA_RX_N
- [16] WWAN_SATA_RX_P
- [16] WWAN_SATA_TX_N
- [16] WWAN_SATA_TX_P

- [24] NGFF_CONFIG_0
- [24] NGFF_CONFIG_1
- [24] NGFF_CONFIG_2
- [24] NGFF_CONFIG_3
- [24] WWAN_WAKE#
- [24] WWAN_RADIO_DIS#
- [24] GPS_DISABLE#
- [16] M3042_DEVSLP
- [20] CPU_I2C_SDA_GNSS
- [20] CPU_I2C_SCL_GNSS
- [17,33,61,91,97] PCH_PLTRST#_RIGHT
- [21,68] SBIOS_TX
- [24,61,63] PCIE_WAKE#_R
- [18,61,63] SUSCLK
- [21,61] CNV_COEX3
- [21,61] CNV_MFUART2_TXD
- [21,61] CNV_MFUART2_RXD
- [18] WWAN_CLK_CPU_P
- [18] WWAN_CLK_CPU_N
- [18] WWAN_CLKREQ_CPU_N
- [19] WWAN_GPIO_WAKE#
- [24] WWAN_GPIO_CTRL
- [18] WWAN_GPIO_PERST#
- [18] WWAN_BB_RST#
- [17,24] PCH_PCIE_WAKE#
- [24] SAR_DRP#
- [24,63] SSD_SCP#
- [20] WWAN_FULL_PWR_EN_R
- [19] ANT_CONFIG

3D3V_S5 — R6248 100KR2F-L1-GP — 1D8V_S5
WWAN_WAKE# — Q6204 PJA138KA-GP — WWAN_WAKE#_Q
084.00138.0A31

WWAN_RADIO_DIS# — R6220 0R2J-2-GP — WWAN_RADIO_DIS#_R
M3042_DEVSLP — R6222 Do Not Stuff
GPS_DISABLE# — R6202 0R2J-2-GP — GPS_DISABLE#_R
R6244 0R2J-2-GP
WWAN_USB20_P — EL6202 — WWAN_USB20_CON_P
WWAN_USB20_N — WWAN_USB20_CON_N
Do Not Stuff
R6245 0R2J-2-GP

2500mA
WWAN1
SKT-MINI67P-GP-U1
62.10043.I71
2ND = 062.10003.0121

NGFF_CONFIG_2 — R6223 0R2J-2-GP — NGFF_CONFIG_2_R
NGFF_CONFIG_1 — R6224 0R2J-2-GP — NGFF_CONFIG_1_R
WWAN_BB_RST#
WWAN_CLK_CPU_P / WWAN_CLK_CPU_N
WWAN_SATA_TX_P — C6206 SCD1U16V1KX-GP — WWAN_SATA_TX_CON_P
WWAN_SATA_TX_N — C6203 SCD1U16V1KX-GP — WWAN_SATA_TX_CON_N
WWAN_SATA_RX_N — R6250 0R1J-GP — WWAN_SATA_RX_CON_N
WWAN_SATA_RX_P — R6251 0R1J-GP — WWAN_SATA_RX_CON_P
WWAN_USB31_TX_P — C6204 SCD1U16V1KX-GP — WWAN_USB31_TX_CON_P
WWAN_USB31_TX_N — C6205 SCD1U16V1KX-GP — WWAN_USB31_TX_CON_N
WWAN_USB31_RX_P — R6233 0R1J-GP — WWAN_USB31_RX_CON_P
WWAN_USB31_RX_N — R6249 0R1J-GP — WWAN_USB31_RX_CON_N
SAR_DRP# — R6231 0R2J-2-GP — SAR_DRP#_R
NGFF_CONFIG_0 — R6226 0R2J-2-GP — NGFF_CONFIG_0_R
WWAN_USB20_CON_N / WWAN_USB20_CON_P
NGFF_CONFIG_3 — R6227 0R2J-2-GP — NGFF_CONFIG_3_R
3D3V_S5_WWAN — R6204 Do Not Stuff — ANT_CONFIG
WWAN_GPIO_WAKE#_R — R6217 Do Not Stuff — CNV_MFUART2_RXD
WWAN_COEX2 — R6219 Do Not Stuff — CNV_MFUART2_TXD
WWAN_COEX3 — R6230 Do Not Stuff — CNV_COEX3
NC#58 — R6229 Do Not Stuff — SBIOS_TX
NC#56 — R6228 Do Not Stuff — PCIE_WAKE#_R
WWAN_WAKE# — R6206 Do Not Stuff
WWAN_CLKREQ_CPU_N
WWAN_RESET#
CPU_I2C_SDA_GNSS
CPU_I2C_SCL_GNSS
M3042_DEVSLP_R — R6215 0R2J-2-GP — M3042_DEVSLP
UIM_PWR
UIM_DATA_R — R6216 0R2J-2-GP — UIM_DATA
UIM_CLK_R — R6218 0R2J-2-GP — UIM_CLK
UIM_RESET
UIM_RFU — R6232 Do Not Stuff
GPS_DISABLE#_R
WWAN_RADIO_DIS#_R — R6221 Do Not Stuff — 3D3V_S5_WWAN
WWAN_FULL_PWR_EN_R
D6205 Do Not Stuff — SSD_SCP#

Figure 3-5 Timing Control for Start-up

Index	Minimum	Typical	Notes
t_{pr}	-	-	+3.3V power supply rises time. If power supply always ready, there is no t_{pr}
t_{on1}	10ms	30ms	If the RESET# has a residual voltage, then 30ms is necessary
t_{on2}	10ms	30ms	PERST# should de-asserted after FULL_CARD_POWER_OFF#

Figure 3-6 Software control power off timing

Index	Minimum	Typical	Maxim	Notes
t_{pd}	10ms	100ms	-	+3.3V power supply goes down time. If power supply is always on, there is no t_{pd}
t_{off1}	10ms	30ms	-	RESET# should asserted before FULL_CARD_POWER_OFF#
t_{off2}	0ms	30ms	t_{off1}	PERST# should asserted after RESET#

To use GPIO as PEWAKE without SPDT ,unstuff R6241 ,R6243 and stuff R6242 or simply un stuff the SPDT.

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

3D3V_S5 — R6211 10KR2F-GP — WWAN_GPIO_WAKE#
3D3V_S5_WWAN — R6213 Do Not Stuff
WWAN_GPIO_WAKE#_R — R6243 0R2J-2-GP — PCH_PCIE_WAKE#
U6202 TS5A3159ADCKR-1-GP
73.53159.00J
WWAN_GPIO_CTRL_Q — R6241 0R2J-2-GP — NGFF_WAKE#_R
R6242 Do Not Stuff
R6209 Do Not Stuff — R6212 Do Not Stuff — NGFF_WAKE#
1D8V_S5 — R6207 100KR2F-L1-GP — WWAN_GPIO_CTRL
R6210 100KR2F-L1-GP — WWAN_GPIO_CTRL_Q
R6202 1MR2F-GP
Q6202 PJA138KA-GP
084.00138.0A31

$Y=A*C+B*\bar{C}$

PCH_PLTRST#_RIGHT — U6203 SN74AUP1G97DCKR-GP — 073.01G97.0A0J
WWAN_GPIO_PERST#_R — R6235 0R2J-2-GP — WWAN_GPIO_PERST#
WWAN_RESET#_R — R6236 0R2J-2-GP — WWAN_RESET#
3D3V_WWAN_S5_S0_1 — R6239 0R2J-2-GP — 3D3V_S5 — 3D3V_S0
R6240 Do Not Stuff
3D3V_S5_WWAN — R6237 Do Not Stuff — 3D3V_S0
R6238 Do Not Stuff
R6205 10KR2F-2-GP
R6234 2K2R2F-GP

teknisi indonesia

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	NA	NA	Low

The M.2 module configuration as the following table:

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
GND	GND	GND	NC	WWAN--USB3.1, PCIe Gen1	0

PCH_PLTRST#_RIGHT — R6246 Do Not Stuff — WWAN_RESET#
WWAN_GPIO_PERST#_R — R6247 Do Not Stuff — WWAN_RESET#
3D3V_S5_WWAN — R6252 Do Not Stuff — Q6203
WWAN_RESET# — WWAN_GPIO_PERST#_R
Do Not Stuff

SIM
SIM1
UIM_PWR — R6220 Do Not Stuff — C1
UIM_VPP — C6
UIM_DATA — C7
UIM_CLK — C3
UIM_RESET — C2
UIM_DET — R6225 0R2J-2-GP — UIM_DET_R
U42
VCC, VPP, I/O, CLK, RST, DTSW, DLSW, GND, NP1, NP2
RFU#C4, RFU#C8, C5
AFTP6201 Do Not Stuff
GND1–GND7
CARDBUS8P-14-GP
062.10008.0401
2nd: 062.10008.0251
UIM_PWR — C6201 SCD1U16V2KX-3DLGP
UIM_DET — EC6202 Do Not Stuff

ED6203 — UIM_DATA, UIM_CLK — AZ5315-02F-GP — 83.05315.0A0
ED6204 — UIM_RESET, UIM_VPP, UIM_PWR — AZ5315-02F-GP — 83.05315.0A0
FC6215, FC6218, FC6219, FC6217 — SC3P50V2AN-3DLGP
FC6216 — Do Not Stuff

Layout Close to SIM1 Connector

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO WWAN
Size: A2 | Document Number: Fircrest 13" | Rev: X01
Date: Thursday, April 18, 2019 | Sheet 62 of 106

Main Func = m.2 SSD

SSD

[16] SSD_PCIE_RX_N1
[16] SSD_PCIE_RX_P1
[16] SSD_PCIE_TX_N1
[16] SSD_PCIE_TX_P1

[16] SSD_PCIE_RX_N2
[16] SSD_PCIE_RX_P2
[16] SSD_PCIE_TX_N2
[16] SSD_PCIE_TX_P2

[16] SSD_PCIE_RX_N3
[16] SSD_PCIE_RX_P3
[16] SSD_PCIE_TX_N3
[16] SSD_PCIE_TX_P3

[16] SSD_SATA_RX_N
[16] SSD_SATA_RX_P
[16] SSD_SATA_TX_N
[16] SSD_SATA_TX_P

[18] SSD_CLK_CPU_N
[18] SSD_CLK_CPU_P
[18] SSD_CLKREQ_CPU_N

[18,61] SUSCLK
[24,61,62] PCIE_WAKE#_R
[17,99] PCH_PLTRST#_LEFT
[16] m2280_PCIE_SATA#
[16] M2280_DEVSLP
[24,62] SSD_SCP#
[24] SSD_SCP_PWR_EN

[16] SSD_SCP_PWR_EN_PCH
[16] PCH_PLTRST#_A

3D3V_S0_SATA

Close Pin 12,14,16,18

C6324 SCD01U50V2KX-1DLGP
C6325 SCD01U16V2KX-3DLGP
C6322 SC10U6D3V3MX-DL-GP

Close Pin 2,4

C6321 SCD01U50V2KX-1DLGP
C6323 SCD01U50V2KX-1DLGP
C6328 SCD01U16V2KX-3DLGP
C6326 SC10U6D3V3MX-DL-GP

Close Pin 70,72,74

C6327 SCD01U50V2KX-1DLGP
C6331 SCD01U50V2KX-1DLGP
C6330 SCD01U16V2KX-3DLGP
C6329 SC10U6D3V3MX-DL-GP
FC6301 SC1U10V2KX-1DLGP

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	Connector Key	N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKN	53
52	CLKREQ# (I/O)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1

SUSCLK
DY EC6302 Do Not Stuff

3D3V_S0_SATA

SSD1

R6306 0R2J-2-GP
SUSCLK → SUS_CLK_SSD
PCIE_WAKE#_R
SSD_CLKREQ_CPU_N
PCH_PLTRST#_SSD

R6302 Do Not Stuff
3D3V_S0_SATA
M2280_DEVSLP
SSD_SCP# → SCP_PIN36
R6307 Do Not Stuff

SSD_SCP# → SCP_PIN8
R6308 Do Not Stuff

76	76		77	77	
74	3_3VAUX		GND	75	
72	3_3VAUX		GND	73	
70	3_3VAUX		GND	71	
68	SUSCLK_32KHZ	0:SATA NC:PCIE	GND	69	m2280_PCIE_SATA#
58	NC#58	PEDET(OC_PCIE/GND_SATA)	NC#67	67	
56	NC#56		GND	57	
54	PEWAKE#/NC#54		REFCLKP	55	SSD_CLK_CPU_P
52	CLKREQ#/NC#52		REFCLKN	53	SSD_CLK_CPU_N
50	PERST#/NC#50		GND	51	
48	NC#48		PERP0/SATA_A+	49	SSD_SATA_TX_CON_P
46	NC#46		PERN0/SATA_A-	47	SSD_SATA_TX_CON_N
44	NC#44		GND	45	
42	NC#42		PETP0/SATA_B-	43	SSD_SATA_RX_N
40	NC#40		PETN0/SATA_B+	41	SSD_SATA_RX_P
38	DEVSLP		GND	39	
36	NC#36		PERP1	37	SSD_PCIE_TX_CON_P3
34	NC#34		PERN1	35	SSD_PCIE_TX_CON_N3
32	NC#32		GND	33	
30	NC#30		PETP1	31	SSD_PCIE_RX_P3
28	NC#28		PETN1	29	SSD_PCIE_RX_N3
26	NC#26		GND	27	
24	NC#24		PERP2	25	SSD_PCIE_TX_CON_P2
22	NC#22		PERN2	23	SSD_PCIE_TX_CON_N2
20	NC#20		GND	21	
18	3_3VAUX		PETP2	19	SSD_PCIE_RX_P2
16	3_3VAUX		PETN2	17	SSD_PCIE_RX_N2
14	3_3VAUX		GND	15	
12	3_3VAUX		PERP3	13	SSD_PCIE_TX_CON_P1
10	DAS/DSS#		PERN3	11	SSD_PCIE_TX_CON_N1
8	NC#8		GND	9	
6	NC#6		PETP3	7	SSD_PCIE_RX_P1
4	3_3VAUX		PETN3	5	SSD_PCIE_RX_N1
2	3_3VAUX		GND	3	
			GND	1	

NGFF_KEY_M 75P

SKT-NGFF75P-203-GP
062.10003.00Z1
2nd:062.10003.01A1

ENG0015277

PEDET	O Host I/F Indication; To be grounded for SATA, No Connect for PCIe — 0V/NC

L	SATA
H	PCIE

SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

SSD_SATA_TX_CON_P → SCD22U10V2KX-2-GP C6301 → SSD_SATA_TX_P
SSD_SATA_TX_CON_N → SCD22U10V2KX-2-GP C6306 → SSD_SATA_TX_N
SSD_PCIE_TX_CON_P3 → SCD22U10V2KX-2-GP C6311 → SSD_PCIE_TX_P3
SSD_PCIE_TX_CON_N3 → SCD22U10V2KX-2-GP C6312 → SSD_PCIE_TX_N3
SSD_PCIE_TX_CON_P2 → SCD22U10V2KX-2-GP C6307 → SSD_PCIE_TX_P2
SSD_PCIE_TX_CON_N2 → SCD22U10V2KX-2-GP C6308 → SSD_PCIE_TX_N2
SSD_PCIE_TX_CON_P1 → SCD22U10V2KX-2-GP C6309 → SSD_PCIE_TX_P1
SSD_PCIE_TX_CON_N1 → SCD22U10V2KX-2-GP C6310 → SSD_PCIE_TX_N1

6.5.4.6 PCH PCI Express* Controller Lane Reversal

For each PCH PCIe* Controller we support end-to-end lane reversal across the four lanes mapped to a controller for the following two motherboard PCIe* configurations

2800mA

3D3V_S0
3D3V_S0_SATA
R6303 D01R6F-3-GP
C6313 SC1U10V2KX-1DLGP
5V_S5
SC10U6D3V3MX-DL-GP
C6315
3D3V_S5
U6301
IN#1 IN#2 IN#9
OUT#8 OUT#7 OUT#6
VBIAS
ON
GND
G5027RD1D-GP-U
074.05027.0093
3D3V_S0_SATA_R
R6311 Do Not Stuff
3D3V_S0_SATA
C6316 SC10U6D3V3MX-DL-GP
C6317 SCD1U16V2KX-3DLGP

SSD_SCP_PWR_EN → R6304 DY 0R1J-GP → SSD_SCP_PWR_EN_R
SSD_SCP_PWR_EN_PCH → R6301 Do Not Stuff
C6314 Do Not Stuff

R6309 Do Not Stuff
3D3V_S5
U6302
PCH_PLTRST#_A
PCH_PLTRST#_LEFT
B VCC
A NC#5
GND Y
PCH_PLTRST#_SSD
Do Not Stuff
R6310 DY 0R1J-GP

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (SSD M.2/ eMMC)
Size: A3
Document Number: Fircrest 13"
Rev: X01
Date: Friday, April 19, 2019
Sheet 63 of 106

Main Func = LED/HALL/Button

[24] BAT2_LED#
[24] BAT1_LED#
[24,32] LED_MASK#
[24,66,68] KBC_PWRBTN#
[24,55,67] LID_CL_SIO#_R
[24,67] LID_CL_SIO_TAB#_R
[24] BREATH_LED#
[24,92] FPR_DET#
[24] M_BIST
[24,44] ACAV_IN
[17,24,99] RSMRST#_KBC

R6412 0R2J-2-GP
Q6401
BAT2_LED# LED_BATCHG
LED_MASK# LED_MASK#
LED_BATLOW BAT1_LED#
Do Not Stuff
Do Not Stuff
R6411 0R2J-2-GP

Stealth mode

Battery LED2(White_LED)
LOW actived from KBC GPIO

LED board
R6402 649R2F-GP
LED_BATCHG BAT_WHITE_LED_A
LED_BATLOW BAT_AMBER_LED_A
R6406 330R2J-3-GP
5V_S5
CLEDB1
KYO-CON6-3-GP
020.K0279.0006

Battery LED1(Orange_LED)
LOW actived from KBC GPIO

Do Not Stuff AFTP6402 BAT_WHITE_LED_A
Do Not Stuff AFTP6403 BAT_AMBER_LED_A
EC6401 Do Not Stuff LED_BATLOW
EC6402 Do Not Stuff LED_BATCHG

3D3V_S5
C6402 SCD1U16V2KX-3DLGP
U6401 74LVC1G08GW-GP
LID_CL_SIO#_R
LED_MASK#
MASK_BASE_LEDS#_Q
73.01G08.AHJ
R6405 Do Not Stuff

OTHER

3D3V_S5
C6404 SCD1U16V2KX-3DLGP
U6402
FPR_DET#
MASK_BASE_LEDS#
Do Not Stuff
R6409 0R2J-2-GP

POWERBT

3D3V_S0
R6407 Do Not Stuff
LID_CL_SIO_TAB#_R
C6403 Do Not Stuff

POWER BUTTON

PWRBT1
KBC_PWRBTN#
SW-TACT-4P-7-GP
62.40009.A91
2nd:062.40001.0981
EC6410 Do Not Stuff

BREATH_LED#
MASK_BASE_LEDS#
Q6404 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31
BREATH_LED#_D
Q6405 RN2418-GP
084.02418.0011
R1=47K /R2=10K
5V_S5
R6404 1KR2J-1-GP
BREATH_LED#_C
BREATH_SWLED1#_A
LED1 LED-W-45-GP
83.19213.H70

Resistor already reserve on EC side

Power LED
LOW actived from KBC GPIO

BREATH_SWLED1#_A
EC6411 Do Not Stuff

M-BIST

3D3V_S5
RSMRST#_KBC
R6410 Do Not Stuff
R6403 1MR2F-GP
M_BIST
ACAV_IN
D6403 Do Not Stuff
C6405 SC2D2U10V3KX-1DLGP-U
R6408 Do Not Stuff
Q6407 DDTA144EUA-7-F-GP
Q6407_B
Q6407_C
BAT_AMBER_LED_A
R6413 150R2F-1-GP
Q6406 MMBT3904WT1G-1-GP
84.M3904.D11
KBC_PWRBTN#

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED / Button / Power Button
Size: Custom
Document Number: Fircrest 13"
Rev: X01
Date: Thursday, April 18, 2019
Sheet 64 of 106

Main Func = Key Board/Touch Pad

10mA

[19] KB_DET#

[24] BC_INT#_ECE1117
[24] BC_DAT_ECE1117
[24] BC_CLK_ECE1117
[3,24] TOUCHPAD_INTR#

[24] CLK_TP_SIO_I2C_DAT
[24] DAT_TP_SIO_I2C_CLK

[20] CPU_I2C_SDA_TP
[20] CPU_I2C_SCL_TP
[24] TP_DISABLE#

[88] KSI_02
[88] KSO_02
[88] EC_KSO_02_INV
[88] EC_KSI_02

3D3V_S0 R6511 3D3V_TP
D01R3F-L-GP

TPAD1
KB_DET#
KSO_02_R
KSI_02
5V_S0
3D3V_S5
BC_INT#_ECE1117
BC_DAT_ECE1117
BC_CLK_ECE1117
TP_DISABLE#
3D3V_TP
EC_KSO_02_INV
EC_KSI_02
TOUCHPAD_INTR#
I2C1_SDA_TP_R
I2C1_SCK_TP_R
ACES-CON20-29-GP-U
20.K0637.020
2nd:020.K0339.0020

R6501 KSO_02 0R1J-GP
R6502 DY Do Not Stuff

3D3V_TP
R6514 10KR2F-GP GD
R6515 Do Not Stuff DY

R6517 Do Not Stuff DY
R6516 Do Not Stuff DY

Reserve for future use
DAT_TP_SIO_I2C_CLK
CLK_TP_SIO_I2C_DAT

C6506 SC10P50V2JN-4DLGP
C6507 SC10P50V2JN-4DLGP

KSO_02 R6507 0R1J-GP WIN EC_KSO_02_INV
KSI_02 R6508 0R1J-GP WIN EC_KSI_02

3D3V_TP C6503 SCD1U25V2KX-1-DL-GP
3D3V_S5 C6504 SCD1U25V2KX-1-DL-GP
5V_S0 C6505 SCD1U25V2KX-1-DL-GP
KB_DET# EC6502 DY Do Not Stuff

3D3V_TP 1 AFTP6501 Do Not Stuff
EC_KSO_02_INV 1 AFTP6502 Do Not Stuff
EC_KSI_02 1 TP6503 Do Not Stuff

3D3V_TP
R6505 2K2R2F-GP
R6506 2K2R2F-GP

R6513 0R2J-2-GP CLK_TP_SIO_I2C_DAT
R6512 0R2J-2-GP DAT_TP_SIO_I2C_CLK

R6503 0R2J-2-GP I2C1_SDA_TP_R CPU_I2C_SDA_TP
R6504 0R2J-2-GP I2C1_SCK_TP_R CPU_I2C_SCL_TP

ALL

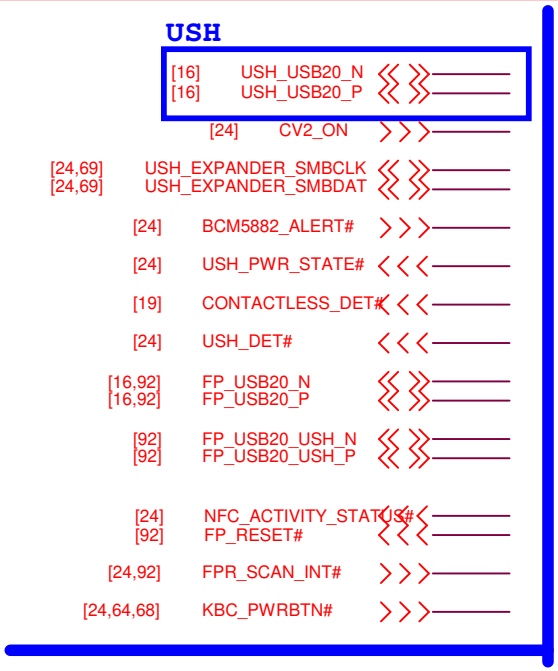
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

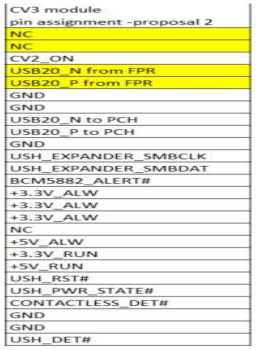
Title: INT IO (KB/TP)

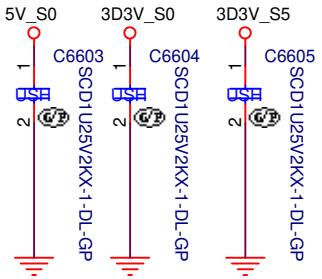
Size	Document Number	Rev
A4	Fircrest 13"	X01

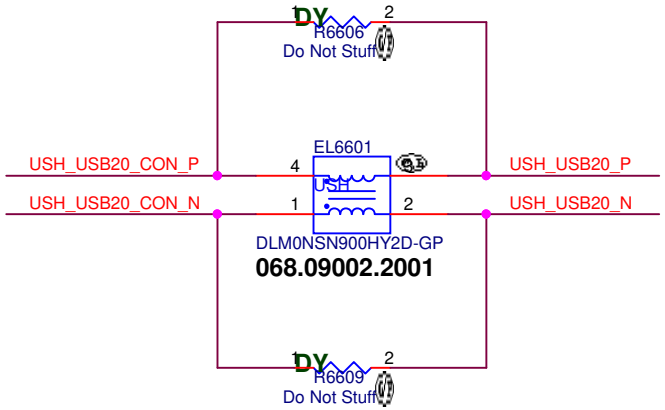
Date: Thursday, April 18, 2019 Sheet 65 of 106

Main Func = USH BD









ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Conn (USH)		
Size: A4	Document Number: Fircrest 13"	Rev: X01
Date: Thursday, April 18, 2019	Sheet 66 of 106	

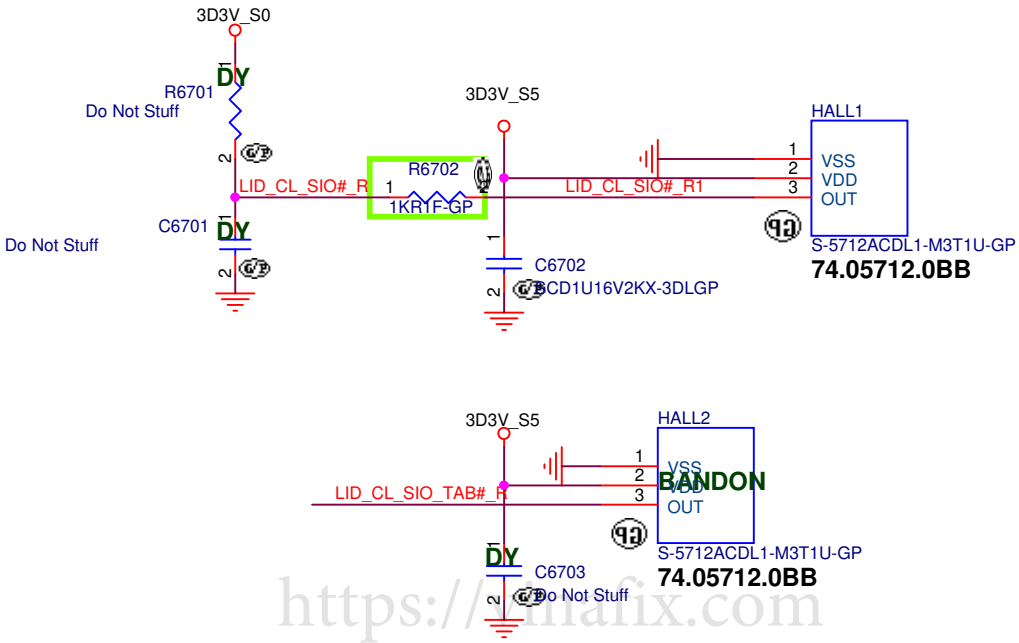
Main Func = Sensor (Hall-Sensor)

[24,55,64] LID_CL_SIO#_R

[24,64] LID_CL_SIO_TAB#_R

BANDON
TCS40DLR
[074.TCS40.M001]

NORTHBAY
APX8131A
[074.08131.007B]



ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Sensor (Hall-Sensor)*

Size	Document Number	Rev
A4	*Fircrest 13"*	*X01*

Date: Thursday, April 18, 2019 Sheet 67 of 106

Main Func = Debug

[19] ME_FWP_PCH
[24] ME_FWP
[24] ME_FWP_SW
[20] CPU_UART2_TXD
[20] CPU_UART2_RXD

[17,24,40,51] SIO_SLP_S3#
[17] SIO_SLP_S5#
[17,40,51] SIO_SLP_S4#
[17] SIO_SLP_A#
[18] RTC_RST#
[24,64,66] KBC_PWRBTN#
[17,99] SYS_RESET#
[17,40,54,91] SIO_SLP_S0#

[18,24] ESPI_IO0
[18,24] ESPI_IO1
[18,24] ESPI_IO2
[18,24] ESPI_IO3
[18,24] ESPI_CS#
[18,24] ESPI_RESET#
[18,24] ESPI_CLK

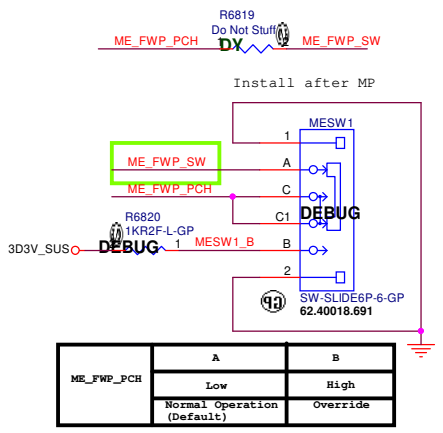
[24] JTAG_TDI
[24] JTAG_TMS
[24] JTAG_CLK
[24] JTAG_TDO
[24] MSCLK
[24] MSDATA
[24] HOST_DEBUG_TX
[21,62] SBIOS_TX

[25,91] SPI_CLK_DEBUG
[25,91] SPI_SI_DEBUG
[25,91] SPI_SO_DEBUG
[25] SPI_WP_DEBUG
[25] SPI_HOLD_DEBUG
[25] SPI_CS_DEBUG_N0
[25] SPI_CS_DEBUG_N1

[18] SPI_CLK_CPU
[15,18,99] SPI_SI_CPU
[18] SPI_SO_CPU
[15,18,99] SPI_WP_CPU
[15,18] SPI_HOLD_CPU
[18] SPI_CS_CPU_N0
[18] SPI_CS_CPU_N1

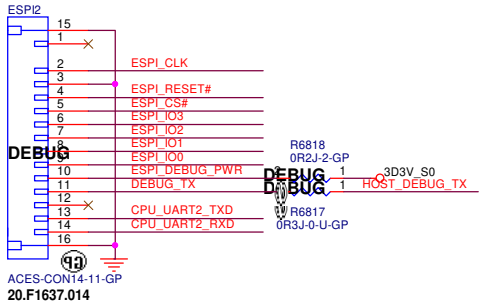
[24] PCH_RSMRST#

Firmware SW

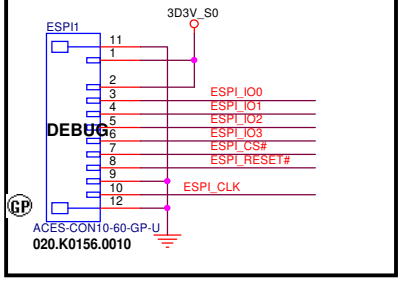


ME_FWP_PCH	A	B
	Low	High
	Normal Operation (Default)	Override

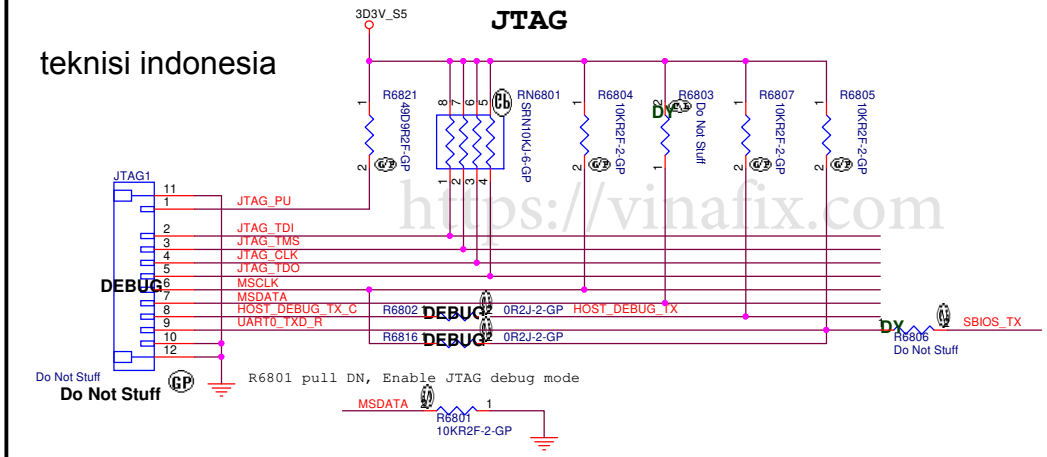
ESPI DEBUG (Wistron)



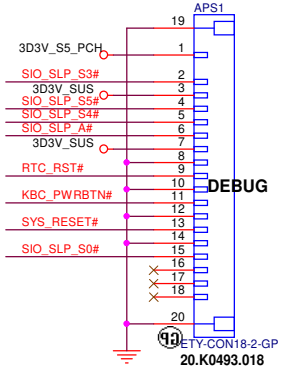
ESPI DEBUG (DELL)



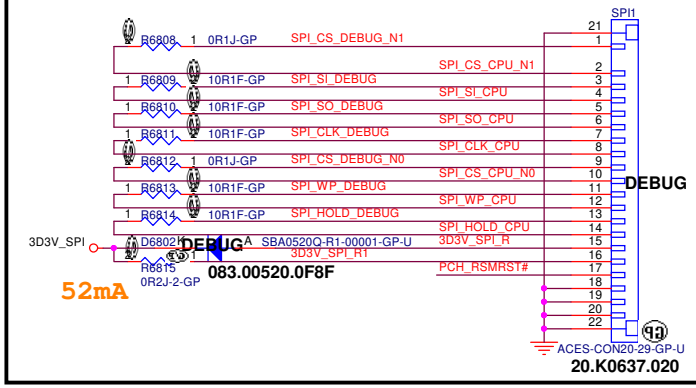
JTAG



APS DEBUG



SPI DEBUG



58mA

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Debug (LPC debug)	
Size A3	Document Number Fircrest 13"	Rev X01
Date: Thursday, April 18, 2019	Sheet 68 of 106	

Main Func = Sensor (E-compass/A+Gyro/SAR)

[20] GSEN_INT1

[20,70] CPU_I2C_SDA_SENSOR
[20,70] CPU_I2C_SCL_SENSOR

[24,66] USH_EXPANDER_SMBDAT
[24,66] USH_EXPANDER_SMBCLK

3D3V_SEN_S0 — F6901 — 3D3V_S0
FUSE-D5A63V-1-GP
069.4R500.0091

3D3V_S5_WWAN

CPU_I2C_SDA_SAR_CON — R6902 2K2R2F-GP — BANDON
CPU_I2C_SCL_SAR_CON — R6903 2K2R2F-GP — BANDON

3D3V_SEN_S0

CPU_I2C_SDA_SENSOR — R6904 2K2R2F-GP — BANDON
CPU_I2C_SCL_SENSOR — R6905 2K2R2F-GP — BANDON

SENBD1
3D3V_SEN_S0
3D3V_S5_WWAN
BANDON
11
1
2
3
4
5
6
7
8
9
10
12
CPU_I2C_SDA_SAR_CON
CPU_I2C_SCL_SAR_CON
CPU_I2C_SDA_SENSOR
CPU_I2C_SCL_SENSOR
GSEN_INT1
ACES-CON10[illegible]-GP-U
20.F2255.010

Q6902
CPU_I2C_SDA_SAR_CON — 6 — 1 — CPU_I2C_SDA_SENSOR
3D3V_S0 — 5 — DY — 2 — 3D3V_S0
CPU_I2C_SCL_SENSOR — 4 — 3 — CPU_I2C_SCL_SAR_CON
Do Not Stuff
Do Not Stuff

Q6901
CPU_I2C_SDA_SAR_CON — 1 — 6 — USH_EXPANDER_SMBDAT
3D3V_S5_WWAN — 5 — BANDON — 5 — 3D3V_S5_WWAN
USH_EXPANDER_SMBCLK — 3 — 4 — CPU_I2C_SCL_SAR_CON
2N7002KDW-1-GP
75.27002.F7C

ED6901
CPU_I2C_SDA_SENSOR — 2
DY — 3
CPU_I2C_SCL_SENSOR — 1
Do Not Stuff
Do Not Stuff

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

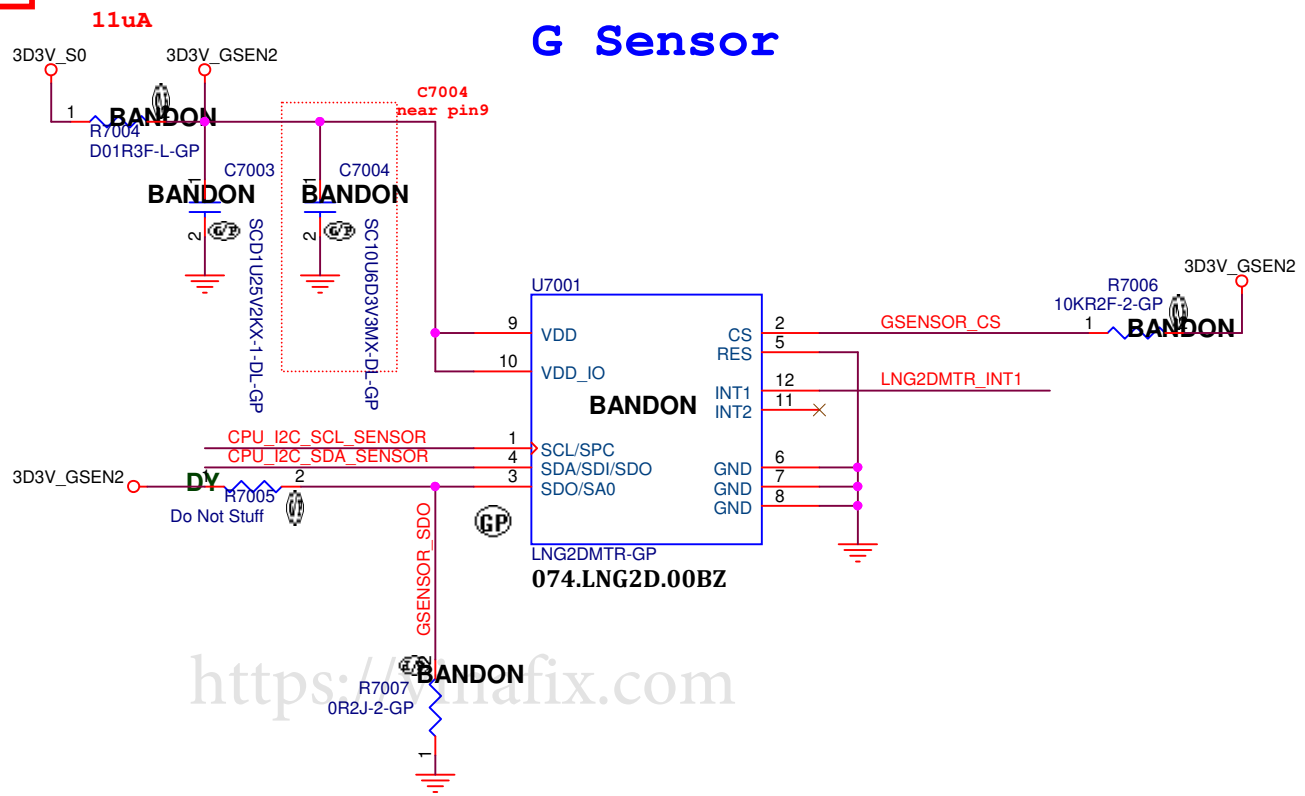
Title
Sensor (GYROSCOPE/PRESSUE/ALS)

Size	Document Number	Rev
A4	***Fircrest 13"***	***X01***

Date: Thursday, April 18, 2019 Sheet 69 of 106

Main Func = G-sensor

[20,69] CPU_I2C_SDA_SENSOR
[20,69] CPU_I2C_SCL_SENSOR
[20] LNG2DMTR_INT1



ALL

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Sensor (G-sensor)		
Size: A4	Document Number: Fircrest 13"	Rev: X01
Date: Thursday, April 18, 2019	Sheet 70 of 106	

Main Func = TypeC

USB1

[16] USB1_USB31_RX_N
[16] USB1_USB31_RX_P
[16] USB1_USB31_TX_N
[16] USB1_USB31_TX_P

[72] PS8802_CSDA_R
[72] PS8802_CSCL_R

[73] USB1_CON_SBU1
[73] USB1_CON_SBU2

[4] DP2_DDI_TX_P0
[4] DP2_DDI_TX_N0

[4] DP2_DDI_TX_P1
[4] DP2_DDI_TX_N1

[4] DP2_DDI_TX_P2
[4] DP2_DDI_TX_N2

[4] DP2_DDI_TX_P3
[4] DP2_DDI_TX_N3

[4] DP2_AUX_CPU_P
[4] DP2_AUX_CPU_N

[4,72] DP2_HPD_CPU

[73] USB1_SSTX_CON_P0
[73] USB1_SSTX_CON_N0

[73] USB1_SSTX_CON_P1
[73] USB1_SSTX_CON_N1

[73] USB1_SSRX_AR_P0
[73] USB1_SSRX_AR_N0

[73] USB1_SSRX_AR_P1
[73] USB1_SSRX_AR_N1

[72] PS8802_FLIP_R
[72] PS8802_DP_R
[72] PS8802_USB_R

[72] PS8802_CSCL
[72] PS8802_CSDA

D7101 DY A K Do Not Stuff
R7104 100KR2F-L1-GP
R7105 100KR2F-L1-GP
R7102 100KR2F-L1-GP
DP2_AUX_CON_N
DP2_AUX_CON_P
DP2_HPD_CON
3D3V_MUX

R7103 4K7R2F-GP PS8802_USB
R7140 10KR2F-2-GP PS8802_RESET#
C7193 SC1U10V2KX-1DLGP

R7146 R7147 R7148 R7149 Do Not Stuff
R7150 R7151 R7152 R7153 Do Not Stuff
PS8802_ADDR
PS8802_DPEQ
PS8802_CEQ
PS8802_SSEQ

ADDR: I2C control bus address. Internally pull down at 150kΩ, 3.3V I/O.
L: Slave address 0x10-0x2F(default)
H: Slave address 0x30-0x4F

DPEQ:DP Receiver equalization setting; Internally pull down at 150kΩ, 3.3V I/O.
L: Compensation for channel loss up to 12dB(Default)
H: Compensation for channel loss up to 18dB

CEQ: USB Type-C Connector facing Rx channel receiver equalization setting;
Internally pull down at 150kΩ, 3.3V I/O.
L: Compensation for channel loss up to 16dB(Default)
H: Compensation for channel loss up to 18dB

SSEQ: USB Host facing Rx channel receiver equalization setting;
Internally pull down at 150kΩ, 3.3V I/O.
L: Compensation for channel loss up to 12dB(Default)
H: Compensation for channel loss up to 18dB

R7142 4K7R2F-GP R7143 4K7R2F-GP

U7101 PS8802QFN52GTR-A1-GP
071.08802.0003

PS8802_CSCL_R R7118 DY Do Not Stuff PS8802_CSCL
PS8802_CSDA_R R7119 DY Do Not Stuff PS8802_CSDA
RN7103 SRN2K2J-1-GP 8802_DCI_CLK 8802_DCI_DATA
DP2_DDI_TX_P0 C7127 SCD22U10V2KX-2-GP DP2_DDI_TX_CON_P0
DP2_DDI_TX_N0 C7128 SCD22U10V2KX-2-GP DP2_DDI_TX_CON_N0
DP2_DDI_TX_P1 C7129 SCD22U10V2KX-2-GP DP2_DDI_TX_CON_P1
DP2_DDI_TX_N1 C7130 SCD22U10V2KX-2-GP DP2_DDI_TX_CON_N1
DP2_DDI_TX_P2 C7131 SCD22U10V2KX-2-GP DP2_DDI_TX_CON_P2
DP2_DDI_TX_N2 C7132 SCD22U10V2KX-2-GP DP2_DDI_TX_CON_N2
DP2_DDI_TX_P3 C7134 SCD22U10V2KX-2-GP DP2_DDI_TX_CON_P3
DP2_DDI_TX_N3 C7133 SCD22U10V2KX-2-GP DP2_DDI_TX_CON_N3
USB1_CON_SBU1
USB1_CON_SBU2
PS8802_FLIP_R R7115 0R2J-2-GP PS8802_FLIP
PS8802_DP_R R7116 0R2J-2-GP PS8802_DP
PS8802_USB_R R7117 0R2J-2-GP PS8802_USB
PS8802_CEQ
PS8802_DPEQ
PS8802_SSEQ
PS8802_ADDR
DP2_HPD_CPU R7114 0R2J-2-GP DP2_HPD_CON
PS8802_RESET#
PS8802_REXT R7141 4K99R2F-L-GP
CSCL CSDA DCI_CLK DCI_DATA ML0P ML0N ML1P ML1N ML2P ML2N ML3P ML3N SBU1 SBU2 FLIP CE_DP CE_USB CEQ DPEQ SSEQ ADDR TEST IN_HPD RESET# RSV REXT GND
VDD33 VDD33 VDD_A1 VDD_A2 VDD_D1 VDD_DCI VDD_DM VDD_DM VDD_DM VDD_DM VDD_R1 VDD_R2
RX1P RX1N RX2P RX2N TX1P TX1N TX2P TX2N SSRXP SSRXN SSTXP SSTXN AUXP AUXN
USB1_SSRX_AR_P0 USB1_SSRX_AR_N0 USB1_SSRX_AR_P1 USB1_SSRX_AR_N1
USB1_SSTX_CON_P0 USB1_SSTX_CON_N0 USB1_SSTX_CON_P1 USB1_SSTX_CON_N1
USB1_USB31_RX_CON_P C7146 SCD22U10V2KX-2-GP USB1_USB31_RX_P
USB1_USB31_RX_CON_N C7144 SCD22U10V2KX-2-GP USB1_USB31_RX_N
USB1_USB31_TX_CON_P C7147 SCD22U10V2KX-2-GP USB1_USB31_TX_P
USB1_USB31_TX_CON_N C7148 SCD22U10V2KX-2-GP USB1_USB31_TX_N
DP2_AUX_CON_P C7135 SCD1U16V1KX-GP DP2_AUX_CPU_P
DP2_AUX_CON_N C7136 SCD1U16V1KX-GP DP2_AUX_CPU_N

3D3V_MUX L7102 BLM18KG331SN1D-GP 3D3V_S5 INT
L7104 BLM18KG331SN1D-GP +3D3V_VDD_PIC EXT
Close Pin49
1D2V_MUX C7160 SC1U10V2KX-1DLGP
C7177 SC1U10V2KX-1DLGP C7178 SC5D1U16V1KX-GP

3D3V_S5 G7104 Do Not Stuff PWR_1D2V_VIN
1D2V_MUX L7103 BLM18KG331SN1D-GP 1D2V_S5

1D2V_S5

IDC = 550mA
22u 0805 total 2pcs (DY 0 pcs)

5V_S5 C7149 SC1U10V2KX-L1-GP
PWR_1D2V_VIN C7150 SC10U6D3V3MX-L-GP
3D3V_S5 R7144 10KR2F-2-GP
R7133 Do Not Stuff
1D2V_EN_PU R7134 0R2J-2-GP
PWR_1D2V_PG
PWR_1D2V_EN
U7103 APL5934KAI-TRG-GP-U
074.05934.003D
VCNTL POK EN VIN#9 VIN#5 VOUT#4 VOUT#3 FB GND
PWR_1D2V_FB
PWR_1D2V G7102 Do Not Stuff 1D2V_S5
G7103 Do Not Stuff
C7151 DY Do Not Stuff
C7153 SC10U6D3V3MX-L-GP
C7154 SC10U6D3V3MX-L-GP
PWR_1D2V_FB_A
R1 R7132 7K32R2F-GP
R2 R7126 14K3R2F-GP
Vout=0.8V*(R1+R2)/R2

1D2V_MUX
C7187 SC4D7U6D3V3KX-DLGP
C7173 C7167 C7168 C7176 SCD01U50V2KX-1DLGP
C7171 C7174 C7185 C7188 C7191 SCD1U16V1KX-GP

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (Thunderbolt(1/3)/Type C Re-driver)
Size: A3
Document Number: Fircrest 13"
Rev: X01
Date: Thursday, April 18, 2019
Sheet 71 of 106

Main Func = TypeC

[24] UPD1_SMBCLK
[24] UPD1_SMBDAT
[24] UPD1_SMBINT#

[73] USB1_CON_CC1
[73] USB1_CON_CC2

[16,72] USB1_USB20_N
[16,72] USB1_USB20_P

[74] AC1_DISC#

[74] EN_PD_HV_1

[71] PS8802_CSDA_R
[71] PS8802_CSCL_R

[16,72] USB1_USB20_P
[16,72] USB1_USB20_N

[73] USB1_USB20_CMCT_P
[73] USB1_USB20_CMCT_N
[73] USB1_USB20_CMCB_P
[73] USB1_USB20_CMCB_N

[71] PS8802_CSCL
[71] PS8802_CSDA

[71,73] USB1_CON_SBU1
[71,73] USB1_CON_SBU2

[71] PS8802_FLIP_R
[71] PS8802_DP_R
[71] PS8802_USB_R

[4,71] DP2_HPD_CPU

R7201 0R2J-2-GP
UPD1_SMBCLK — Q7201 — UPD1_SMBCLK_Q
+3D3V_VDD_PIC — DY — +3D3V_VDD_PIC
UPD1_SMBDA_Q — UPD1_SMBDAT
Do Not Stuff
R7202 0R2J-2-GP

3D3V_S5 — R7232 D01R3F-L-GP — +3D3V_VDD_PIC_PD
INT
+3D3V_VDD_PIC — R7239 0R2J-2-GP
EXT
3D3V_FLASH — R7238 0R2J-2-GP — +3D3V_VDD_PIC
INT

U7202
TBT_EE_CS_N_PD — CS#
TBT_EE_DO_PD — DO/IO1
TBT_EE_WP_N_PD — WP#/IO2
GND
VCC — 3D3V_FLASH
HOLD#/IO3 — TBT_HOLD_N_PD
CLK — TBT_EE_CLK_PD
DI/IO0 — TBT_EE_DI_PD
W25Q80DVSSIGT-GP
072.25Q80.M003
C7214 SCD1U16V2KX-3DLGP

RN7203 SRN3K3J-1-GP
TBT_EE_CS_N_PD
TBT_EE_DO_PD
TBT_EE_WP_N_PD
TBT_HOLD_N_PD
3D3V_FLASH
R7235 Do Not Stuff DY — UPD1_SMBDA_Q — PS8802_CSDA
R7236 Do Not Stuff DY — UPD1_SMBCLK_Q — PS8802_CSCL
R7237 Do Not Stuff DY — UPD1_SMBINT# — TBTA_I2C_INT

TBTA_LDO_BMC
VCC1V8D_TBTA
VCC1V8A_TBTA
+3D3V_VDD_PIC_PD
C7205 SC2D2U10V3KX-1DLGP-U
C7206 SC4D7U6D3V3KX-DLGP
C7207 SC4D7U6D3V3KX-DLGP
C7208 SC1U10V2KX-1DLGP

TBTA_VBUS_L
5V_S5 — R7240 D01R5F-GP — 5V_S5_PD
R7203 0R2J-2-GP — SENSEP
R7204 0R2J-2-GP — SENSEN
TBTA_VBUS_L — L7201 UPB201209T-330Y-NP01-GP — TBTA_VBUS20
DY C7209 Do Not Stuff

R7208 0R2J-2-GP
0.PRI 1.Sec
3D3V_S5 — R7206 100KR2F-L1-GP
Follow Andy mail

U7201
H1 VIN_3V3
B1 VDDIO
K1 LDO_1V8A
A2 LDO_1V8D
E1 LDO_BMC
H10 PP_CABLE
A11 B11 C11 D11 PP_5V0 PP_5V0 PP_5V0 PP_5V0
A6 A7 A8 B7 GND GND GND GND
B10 SENSEP
A10 SENSEN
B9 HV_GATE1
A9 HV_GATE2

I2C_ADDR — F1
PS8802_CSDA_R — D1
PS8802_CSCL_R — D2
TBTA_I2C_INT — C1
I2C_SDA1
I2C_SCL1
I2C_IRQ1#
UPD1_SMBDA_Q — A5
UPD1_SMBCLK_Q — B5
UPD1_SMBINT# — B6
I2C_SDA2
I2C_SCL2
I2C_IRQ2#

PS8802_FLIP_R — B2
EN_PD_HV_1 — C2
TBTA_ACE_GPIO2 — D10
AC1_DISC# — G11
TBTA_HPD — C10
TBTA_ACE_GPIO5 — E10
TBTA_ACE_GPIO6 — G10
TBTA_ACE_GPIO7 — D7
TBTA_ACE_GPIO8 — H6
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8

3D3V_FLASH — R7209 10KR2J-3-GP — R7210 43KR2J-GP
DP2_HPD_CPU — R7207 1MR2F-L-GP — R7234 0R2J-2-GP
TP7203 TP7204 TP7205

TBT_EE_CLK_PD — A3
TBT_EE_DI_PD — B4
TBT_EE_DO_PD — A4
TBT_EE_CS_N_PD — B3
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SSZ

USB1_USB20_P — R7250 0R1J-GP — USB1_USB20_PD_P — L5
USB1_USB20_N — R7251 0R1J-GP — USB1_USB20_PD_N — K5
USB_RP_P
USB_RP_N

R7211 0R2J-2-GP
TBTA_UART_TX — E2
TBTA_UART_RX — F2
UART_TX
UART_RX

R7212 Do Not Stuff DY — R7213 100KR2F-L1-GP
TP7206 TP7207
SWD_DAT — F4
SWD_CLK — G4
SWD_DATA
SWD_CLK

TBTA_MRESET — E11
MRESET

R7216 0R2J-2-GP — TBTA_LSTX_R — L4
R7217 0R2J-2-GP — TBTA_LSRX_R — K4
LSX_R2P
LSX_P2R

PS8802_DP_R — R7218 0R2J-2-GP — TBTA_DIG_AUD_P — L3
PS8802_USB_R — R7219 0R2J-2-GP — TBTA_DIG_AUD_N — K3
DEBUG3
DEBUG4

UPD1_SMBCLK_Q — R7221 0R2J-2-GP — TBTA_DEBUG1 — L2
UPD1_SMBDA_Q — R7222 0R2J-2-GP — TBTA_DEBUG2 — K2
DEBUG1
DEBUG2

USB1_AUX_PD_P — J1
USB1_AUX_PD_N — J2
AUX_P
AUX_N

3D3V_FLASH — DY R7225 Do Not Stuff — BUSPOWERZ — F10
VCC1V8D_TBTA — DY R7226 Do Not Stuff
BUSPOWERZ
TBTA_ROSC — G2
R_OSC
R7228 0R2J-2-GP
R7229 15KR2D-GP

SN1804044ZBHR-GP
071.18040.000U

GND A1 GND E5 GND E6 GND F5 GND G5 GND H4 GND H5 GND B8 GND D8 GND E8 GND F6 GND F7 GND F8 GND G6 GND G7 GND G8 GND H8 GND L1 GND L11 NC#11 SS H7
NC#11 — TBTA_SS — C7215 SCD22U10V2KX-2-GP — TP7201

3D3V_VOUT — C7210 SC1U10V2KX-1DLGP
3D3V_FLASH — C7211 SC10U6D3V3MX-DL-GP

VBUS H11
VBUS J11
VBUS J10
VBUS K11
VOUT_3V3 H2
LDO_3V3 G1

C_USB_TP K6 — USB1_USB20_CMCT_P
C_USB_TN L6 — USB1_USB20_CMCT_N
C_USB_BP K7 — USB1_USB20_CMCB_P
C_USB_BN L7 — USB1_USB20_CMCB_N

C_CC1 L9 — USB1_PD_CC1 — R7230 0R2J-2-GP — USB1_CON_CC1
C_CC2 L10 — USB1_PD_CC2 — R7231 0R2J-2-GP — USB1_CON_CC2
C7212 SC220P50V2KX-3DLGP
C7213 SC220P50V2KX-3DLGP
Tie RPD_Gn to C_CCn pins to support no-power or dead-battery modes
Dead Battery Mode

RPD_G1 K9 — RPD_G1 — R7214 0R2J-2-GP
RPD_G2 K10 — RPD_G2 — R7215 0R2J-2-GP

DEBUG_CTL1 E4 — TBTA_DBG_CTL1
DEBUG_CTL2 D5 — TBTA_DBG_CTL2

C_SBU1 K8 — USB1_PD_SBU1 — R7220 0R2J-2-GP
C_SBU2 L8 — USB1_PD_SBU2 — R7222 0R2J-2-GP

RESET# F11 — PD_RESET# — DY R7224 Do Not Stuff
HRESET D6 — HRESET
R7227 100KR2F-L1-GP
ALL

5V_S5_PD
C7201 SC220U6D3V9MX-1-DL-GP
C7202 SC220U6D3V9MX-1-DL-GP
C7203 SC220U6D3V9MX-1-DL-GP
C7204 SC220U6D3V9MX-1-DL-GP

3D3V_FLASH — RN7201 — DY — Do Not Stuff
UPD1_SMBDA_Q
UPD1_SMBCLK_Q
RN7202 SRN10KJ-5-GP
TBTA_DBG_CTL1
TBTA_DBG_CTL2

R7205 1MR1F-GP — TBTA_MRESET

3D3V_S5 — R7233 10KR2F-2-GP — TBTA_I2C_INT

RN7112 SRN100KJ-6-GP
USB1_AUX_PD_P
USB1_AUX_PD_N

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (Thunderbolt(2/3)/Type C CC Logic)
Size: A3 | Document Number: Fircrest 13" | Rev: X01
Date: Thursday, April 18, 2019 | Sheet 72 of 106

Main Func = TypeC

USB1

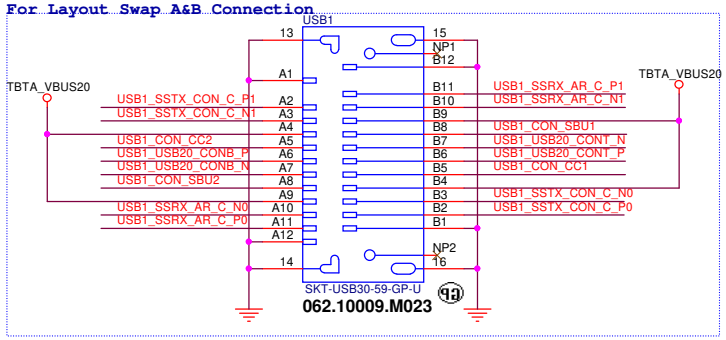
[71] USB1_SSTX_CON_P0
[71] USB1_SSTX_CON_N0
[71] USB1_SSTX_CON_P1
[71] USB1_SSTX_CON_N1
[71] USB1_SSRX_AR_P0
[71] USB1_SSRX_AR_N0
[71] USB1_SSRX_AR_P1
[71] USB1_SSRX_AR_N1

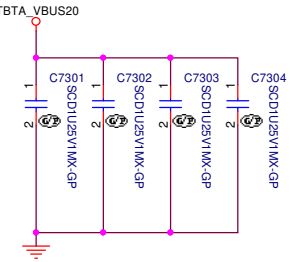
[72] USB1_USB20_CMCT_P
[72] USB1_USB20_CMCT_N
[72] USB1_USB20_CMCB_P
[72] USB1_USB20_CMCB_N

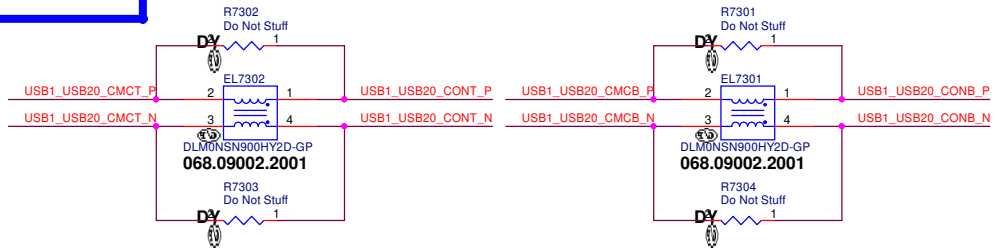
[72] USB1_CON_CC1
[72] USB1_CON_CC2

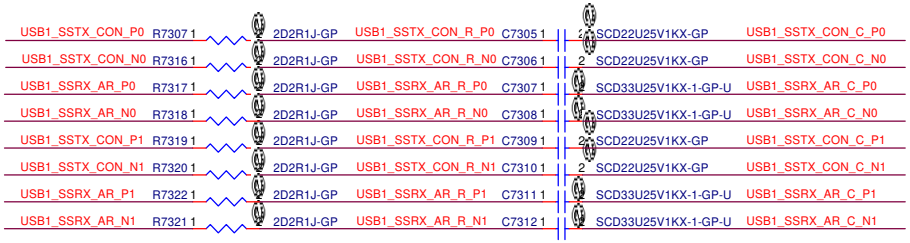
[71] USB1_CON_SBU1
[71] USB1_CON_SBU2

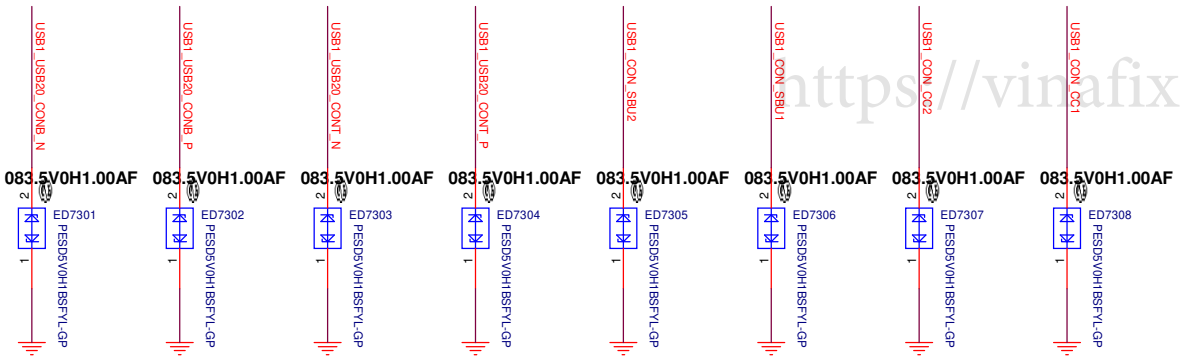
For Layout Swap A&B Connection

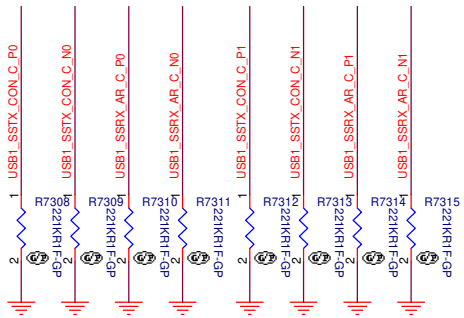


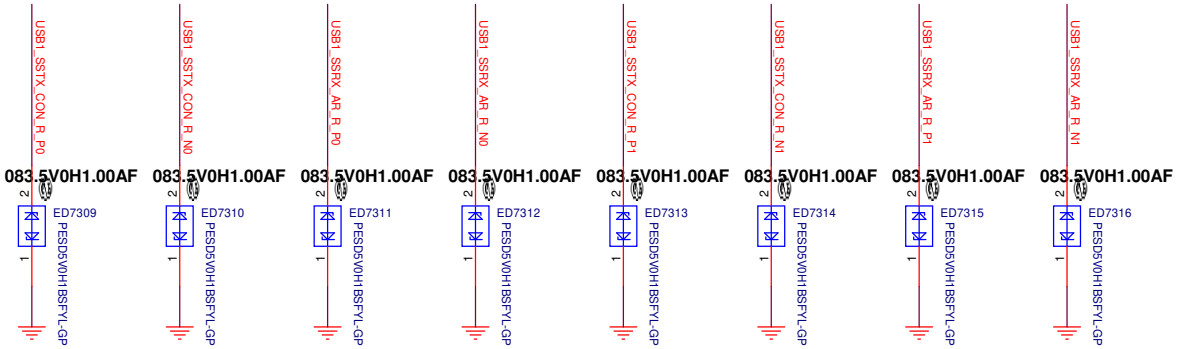












ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EXT IO (Thunderbolt(3/3)/Type C Conn)**

Size	Document Number	Rev
A3	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 73 of 106

Main Func = TypeC

[24,43,44] HW_ACAVIN_NB
[72] AC1_DISC#
[24,43] VBUS1_ECOK
[72] EN_PD_HV_1
[24,43] AC_DISC#
[24] DCIN1_EN
[43] PWR_VBUS_OVP_OUT_R
[24,44] VBUS2_ECOK

+3D3V_VDD_DCIN

20V>+DC_IN>4.7V
D7406 BAT54C-12-GP 75.00054.A7D
U7401 AP2204K-ADJTRG1-GP 74.02204.03F
Vout=1.24*(1+(R1/R2))

+3D3V_VDD_PIC

20V>LDO_5V_VIN>4.7V
U7402 AP2204K-ADJTRG1-GP 74.02204.03F
D7401 RB751S-40-2-GP 83.R2004.B8F
Vout=1.24*(1+(R1/R2))
high Actie, EN >2.6V
D7402 RB751VM-40TE-17-GP 83.R2004.J8F
D7403 RB751VM-40TE-17-GP 83.R2004.J8F
U7403 APL5315BI-TRG-GP 74.05315.A3F
high Actie, EN >1.6V
Vout=0.8*(1+(R1/R2))

AC_Disconect_Logic

DC-IN
TYPE-C
Q1 Q2 Q3 Q4 Q5 Q6
2N7002KDW-1-GP 75.27002.F7C
Need to Charger

VBUS_OVP

U7404 L1S5263T1G-GP 83.00355.G1F
U7404 AS331K1T6-G1-GP 74.00331.H2F
T2N7002BK-2-GP 084.27002.0L31

TYPE-C

S4 ACN7403-GP-U 84.07403.037
S5 ACN7403-GP-U 84.07403.037
Q7407 NTR4502PT1G-GP-U 84.04502.031
Q7408 NTR4502PT1G-GP-U 84.04502.031
Q7409 2N7002KDW-1-GP 75.27002.F7C
Q7410 2N7002KDW-1-GP 75.27002.F7C
Q7411 T2N7002BK-2-GP 084.27002.0L31
Q7412 T2N7002BK-2-GP 084.27002.0L31
Q7413 2N7002KDW-1-GP 75.27002.F7C
Form Type-C PD Control
Form EC Control
Without Input LDO need to Stuff
Do Not Stuff
2nd = 084.27002.0N31
2nd = 73.75208.0AH

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: EXT IO (TYPEC PD)
Size: Custom | Document Number: Fircrest 13" | Rev: X01
Date: Thursday, April 18, 2019 | Sheet 74 of 108

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (RSVD)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 75 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (PEG 1/5)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 76 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (DIGITAL 2/5)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 77 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (RSVD) (VRAM 3/5)***

Size	Document Number	Rev
A4	***Fircrest 13"***	***X01***

Date: Thursday, April 18, 2019 Sheet 78 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (GPIO 4/5)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 79 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (PWR/GND 5/5)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 80 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (VRAM1,2 1/4)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 81 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (VRAM3,4 2/4)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 82 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (VRAM5,6 3/4)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 83 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (VRAM7,8 4/4)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 84 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (VGA_CORE)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 85 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD) (Sequence)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 86 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

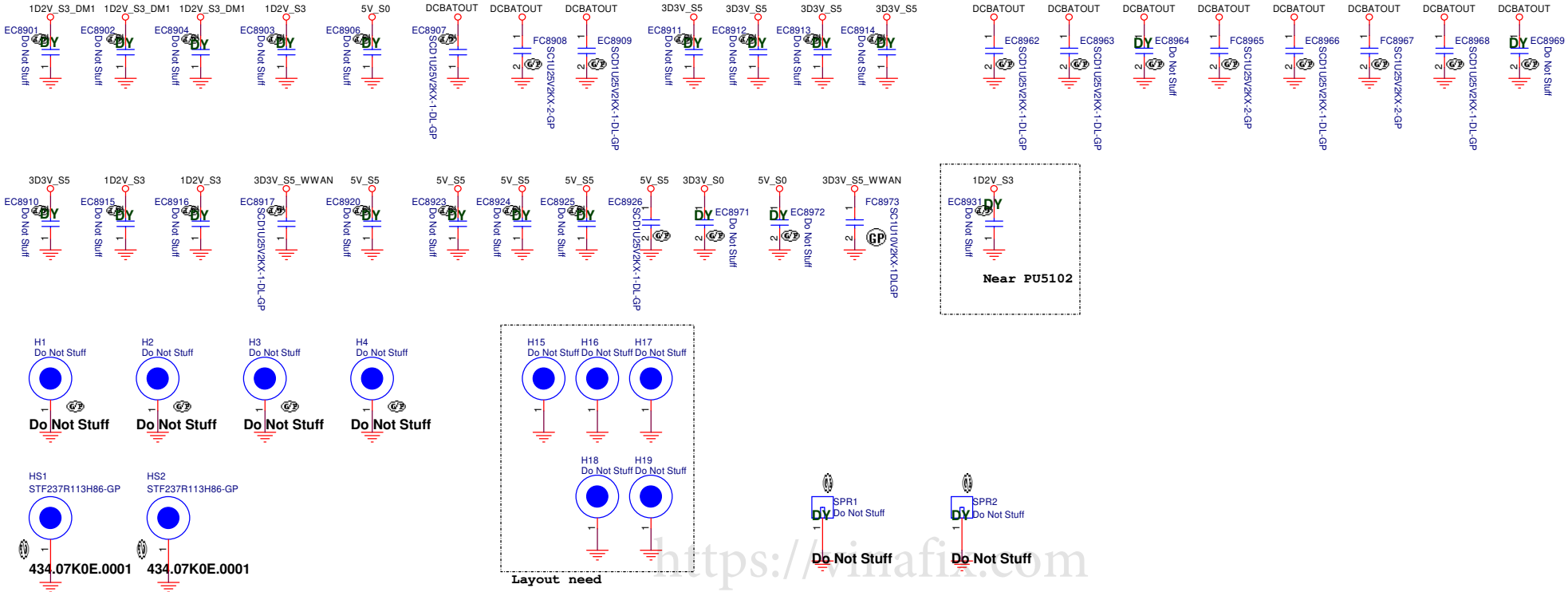
Size	Document Number	Rev
A4	Fircrest 13"	X01

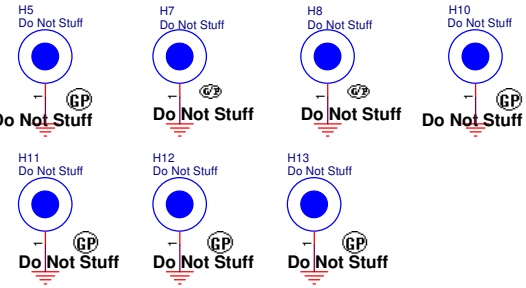
Date: Thursday, April 18, 2019 Sheet 87 of 106

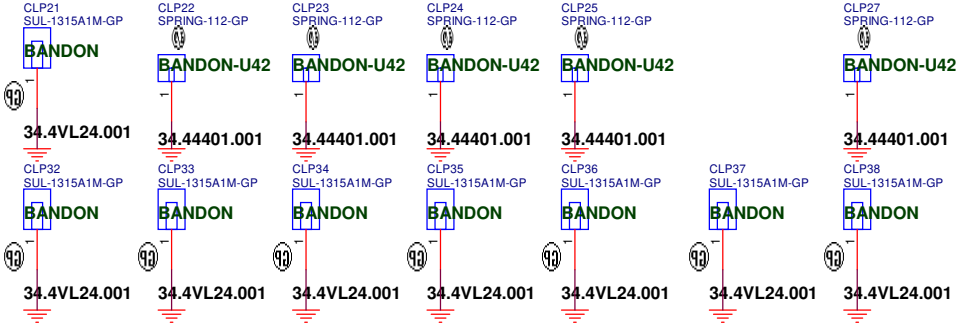
Main Func = H1 SECURE MICROCONTROLLER

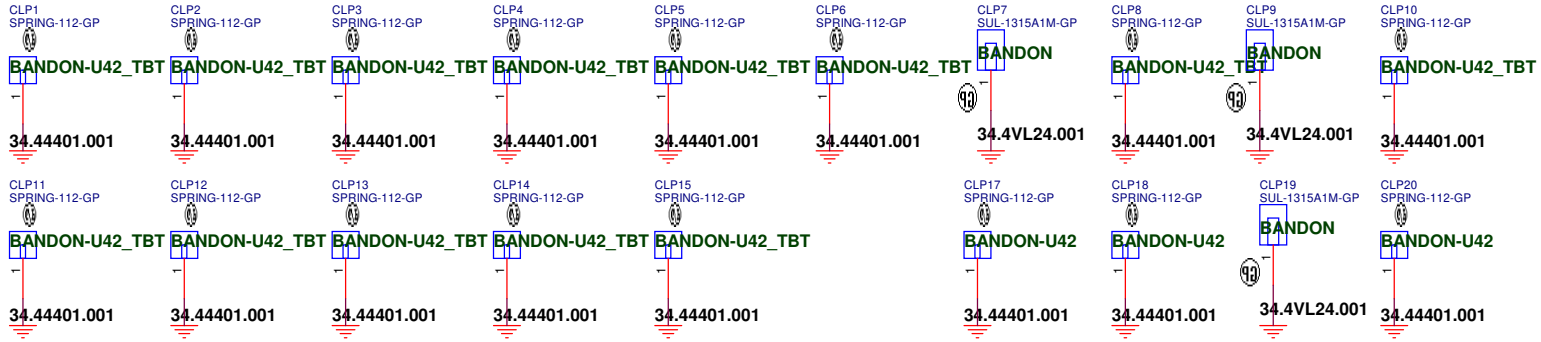
SERVO HEADER

Main Func = EMC/ RF









ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS (RF/EMI Capacitors)

Size	Document Number	Rev
A3	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 89 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

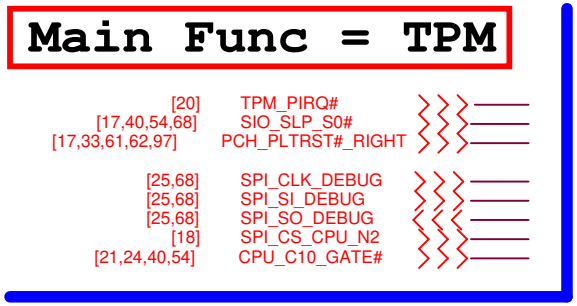
Title: INT IO (RSVD) (NFC)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 90 of 106

Main Func = TPM

[20]	TPM_PIRQ#
[17,40,54,68]	SIO_SLP_S0#
[17,33,61,62,97]	PCH_PLTRST#_RIGHT
[25,68]	SPI_CLK_DEBUG
[25,68]	SPI_SI_DEBUG
[25,68]	SPI_SO_DEBUG
[18]	SPI_CS_CPU_N2
[21,24,40,54]	CPU_C10_GATE#



Colay
ST33HTPH2032AHC1-GP
071.33203.0A03
NPCT750JAAYX-1-GP
071.00750.M001

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (TPM)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 91 of 106

Main Func = Finger Printer

[16] FP_USB20_N
[16] FP_USB20_P
[24,64] FPR_DET#
[66] FP_USB20_USH_N
[66] FP_USB20_USH_P
[24] FPR_PWR_EN#
[24,66] FPR_SCAN_INT#
[24] FPR_SSO_EN#
[24] FPR_UEFI_MGMT#
[24] FPR_LOW_PWR_MODE#
[66] FP_RESET#

Pin 1	GND
Pin 2	FPR_DET(GND)
Pin 3	USB_DP
Pin 4	NA
Pin 5	USB_DM
Pin 6	NA
Pin 7	GND
Pin 8	NA
Pin 9	RESERVED
Pin 10	NA
Pin 11	FP_RESET#
Pin 12	LOW_POW_MODE#
Pin 13	VDDD_CHICLET
Pin 14	UEFI_MGMT#
Pin 15	SSO_EN#
Pin 16	FPR_SCAN_INTR#

3D3V_S5 R9204 10KR2F-2-GP FP
FPR_DET# EC9202 DY Do Not Stuff
FP1 FOX-CONN16D-1-GP GP
FPR_LOW_PWR_MODE# FPR_UEFI_MGMT# FPR_SCAN_INT#
FP_USB20_CON_P FP_USB20_CON_N SLEEP_N FP_RESET# FPR_SSO_EN#
3D3V_S0_FP R9215 10KR2F-2-GP FP
R9210 DY Do Not Stuff
20.F2321.016
2nd:20.F2448.016

3D3V_S0 R9218 0R2J-2-GP FP
3D3V_S0_FP R9216 DY Do Not Stuff
FP_PH
R9211 10KR2F-2-GP FPR_SCAN_INT#
R9212 10KR2F-2-GP FPR_UEFI_MGMT#
R9213 10KR2F-2-GP FPR_SSO_EN#
R9214 10KR2F-2-GP FPR_LOW_PWR_MODE#

www.teknisi-indonesia.com

3D3V_S5 R9205 D01R3F-L-GP FP
3D3V_S0 R9203 Do Not Stuff DY
Q9202 PJA3413-1-GP
3D3V_FP_PWR 3D3V_S0_FP_R
R9217 D01R3F-L-GP FP 3D3V_S0_FP
100mA
084.03413.0031
R9219 0R2J-2-GP FP
FPR_PWR_EN# FPR_PWR_EN#_R
C9202 DY Do Not Stuff

https://vinafix.com

PCH

R9208 Do Not Stuff DY
FP_USB20_N FP_USB20_R_N
R9209 Do Not Stuff DY
FP_USB20_P FP_USB20_R_P

USH

R9206 0R2J-2-GP FR
FP_USB20_R_N FP_USB20_USH_N
R9207 0R2J-2-GP FR
FP_USB20_R_P FP_USB20_USH_P

R9202 0R2J-2-GP FR
EL9201
FP_USB20_CON_P FP_USB20_R_P
FP_USB20_CON_N FP_USB20_R_N
Do Not Stuff DY
Do Not Stuff
R9201 0R2J-2-GP FR

EU9202
FP_USB20_CON_P
FP_USB20_CON_N
FP AZ5315-02F-GP
83.05315.0A0

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (Finger Printer)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 92 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
EXT IO (RSVD) (Express Card/PCIE slot)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 93 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EXT IO (RSVD) (Smart Card/COM/PS2)***

Size	Document Number	Rev
A4	***Fircrest 13"***	***X01***

Date: Thursday, April 18, 2019 Sheet 94 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
EXT IO (RSVD) (Docking/LPT)

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 95 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Commercial (RSVD) (SW GFX eDP)*

Size	Document Number	Rev
A4	*Fircrest 13"*	*X01*

Date: Thursday, April 18, 2019 Sheet 96 of 106

Main Func = LAN

LAN

[16] LAN_PCIE_RX_N
[16] LAN_PCIE_RX_P
[16] LAN_PCIE_TX_N
[16] LAN_PCIE_TX_P
[18,61] WLAN_CLKREQ_CPU_N
[17,33,61,62,91] PCH_PLTRST#_RIGHT
[17,24] LAN_WAKE#
[17] PM_LANPHY_ENABLE
[18] SML0_SMBCLK
[18] SML0_SMBDATA
[32] LAN_0_GREEN_LINK_N
[32] LAN_1_AMBER_ACT_N
[24] LOM_CABLE_DETECT#
[32] LAN_MDI0_P
[32] LAN_MDI0_N
[32] LAN_MDI1_P
[32] LAN_MDI1_N
[32] LAN_MDI2_P
[32] LAN_MDI2_N
[32] LAN_MDI3_P
[32] LAN_MDI3_N
[18] LAN_CLK_CPU_N
[18] LAN_CLK_CPU_P
[18] LAN_CLKREQ_CPU_N

3D3V_LAN
DY R9701 Do Not Stuff
PM_LANPHY_ENABLE
DY R9702 Do Not Stuff

DESIGN NOTE: LAN_DISABLE_N must be connected to PCH's GPIO/LANPHYPC output. This GPIO pin must be set as "LANPHYPC" function through FITC tool. The signal does not require pull-up. R15 resistor is no-stuff default (for testing purpose).

NOTE:DESIGN NOTE: LANWAKE_N must be connected to PCH's LANWAKE input.

U9701

LAN_PCIE_RX_P C9701 SCD1U16V2KX-3DLGP LAN_PCIE_RX_C_P 38
LAN_PCIE_RX_N C9702 SCD1U16V2KX-3DLGP LAN_PCIE_RX_C_N 39
LAN_PCIE_TX_P C9703 SCD1U16V2KX-3DLGP LAN_PCIE_TX_C_P 41
LAN_PCIE_TX_N C9704 SCD1U16V2KX-3DLGP LAN_PCIE_TX_C_N 42
PCIE MDI
PETP PETN PERP PERN

SML0_SMBCLK R9704 0R2J-2-GP CPU_SMB_SCL_LAN 28
SML0_SMBDATA R9706 0R2J-2-GP CPU_SMB_SDA_LAN 31
SMBUS
SMB_CLK SMB_DATA

LAN_WAKE# R9708 0R2J-2-GP LAN_WAKE#_R 2
PM_LANPHY_ENABLE R9710 0R2J-2-GP LAN_DISABLE# 3
LANWAKE# LAN_DISABLE#

LAN_CLKREQ_CPU_N 48
PCH_PLTRST#_RIGHT 36
LAN_CLK_CPU_P 44
LAN_CLK_CPU_N 45
CLK_REQ# PE_RST# PE_CLKP PE_CLKN

LAN_0_GREEN_LINK_N 26
LAN_1_AMBER_ACT_N 27
LAN_LED2 25
LED0 LED1 LED2 LED

TP9703 Do Not Stuff
TP9701 Do Not Stuff
TP9702 Do Not Stuff
LAN_JTAG_TDI 32
LAN_JTAG_TDO 34
LAN_JTAG_TMS 33
LAN_JTAG_TCK 35
JTAG_TDI JTAG_TDO JTAG_TMS JTAG_TCK JTAG

XTL_25M_X2_LAN 9
XTL_25M_X1_LAN 10
XTAL_OUT XTAL_IN

R9713 1KR2F-L-GP
TEST_EN 30
R9714 3K01R2F-3-GP
RBIAS 12
TEST_EN RBIAS

MDI_PLUS0 13 LAN_MDI0_P
MDI_MINUS0 14 LAN_MDI0_N
MDI_PLUS1 17 LAN_MDI1_P
MDI_MINUS1 18 LAN_MDI1_N
MDI_PLUS2 20 LAN_MDI2_P
MDI_MINUS2 21 LAN_MDI2_N
MDI_PLUS3 23 LAN_MDI3_P
MDI_MINUS3 24 LAN_MDI3_N

SVR_EN# 6 SVR_EN_N
RSVD1_VSS3P3 1 RSVD1_VCC3P3
VDD3P3_IN 5
VDD3P3 4 15 19 29
VDD0P9 8 11 16 22 37 40 43 46 47
CTRL0P9 7
GND 49

R9703 0R2J-2-GP
DY R9705 Do Not Stuff
LAN R9707 4K7R2F-GP
3D3V_LAN

teknisi indonesia

3D3V_LANOUT
C9705 SC22U6D3V3MX-1-DL-GP
C9714 SCD1U16V2KX-3DLGP
C9707 Do Not Stuff
R9709 0R3J-0-U-GP
3D3V_LAN

VDD0P9_LAN
L9701 IND-4D7UH-200-GP-U
68.4R71D.10E
CTRL_0P9
C9708 SC22U6D3V3MX-1-DL-GP
C9709 SCD1U16V2KX-3DLGP
C9710 Do Not Stuff

WGI219LM-GP
071.219LM.0003

3D3V_LAN R9711 1MR2F-GP LAN_0_GREEN_LINK_N
Refer RoundRock

3D3V_LAN
DY R9715 Do Not Stuff LAN_JTAG_TMS
DY R9716 Do Not Stuff LAN_JTAG_TCK
DY R9718 Do Not Stuff LAN_CLKREQ_CPU_N
DY R9719 Do Not Stuff LAN_WAKE#_R

C9711 SC15P50V2JN-2-GP
XTL_25M_X2_LAN_R
R9717 0R2J-2-GP
XTL_25M_X2_LAN

X9701 XTAL-25MHZ-202-GP
82.30020.I61

R9720 1MR2F-GP

C9713 SC15P50V2JN-2-GP
XTL_25M_X1_LAN

R9712 0R2J-2-GP
LAN_0_GREEN_LINK_N LOM_CABLE_DETECT#

ALL

DELL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Commercial (Intel LAN)**

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 97 of 106

ALL

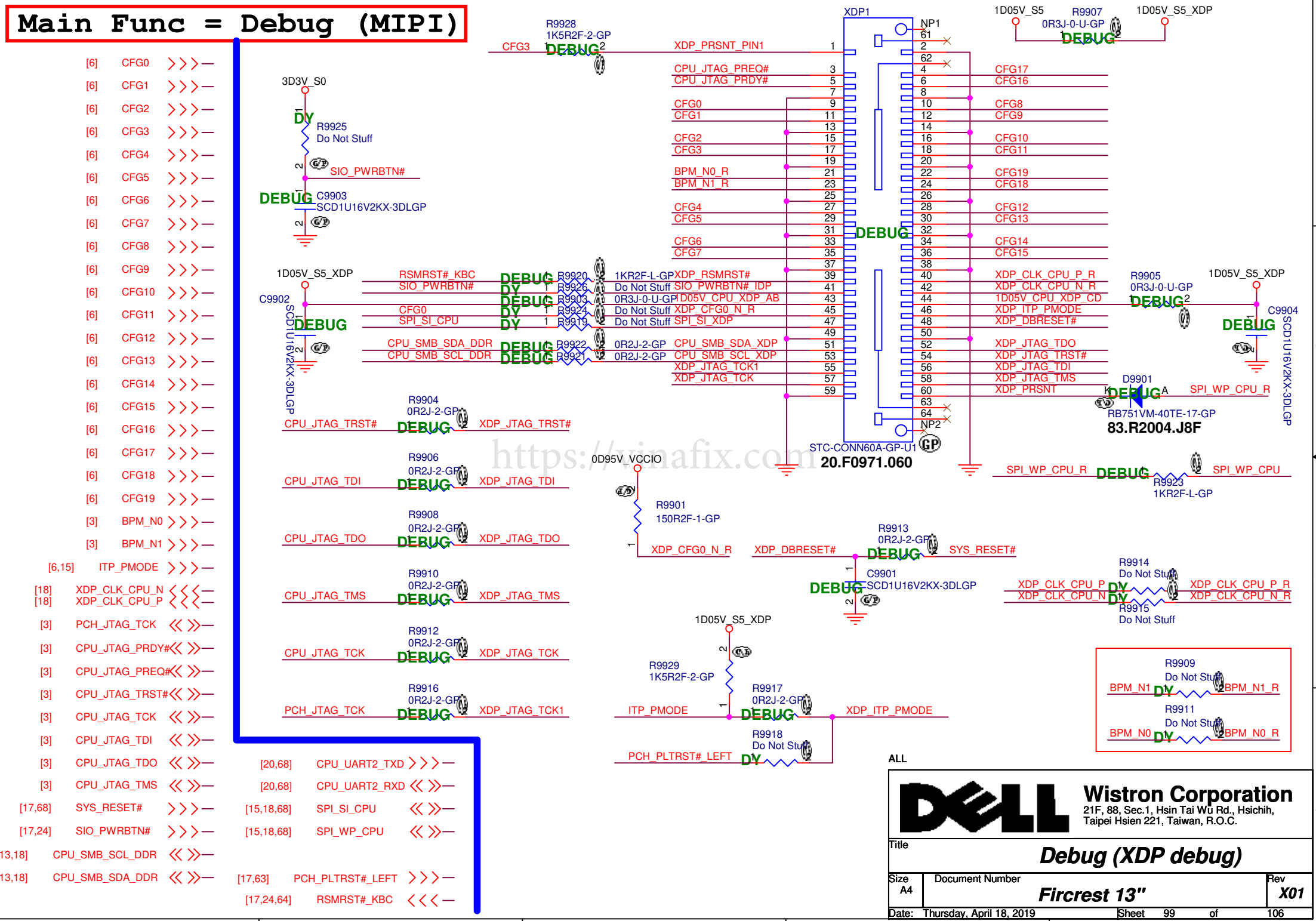
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Commercial (LAN Switch)*

Size	Document Number	Rev
A4	*Fircrest 13"*	*X01*

Date: Thursday, April 18, 2019 Sheet 98 of 106

Main Func = Debug (MIPI)



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Debug (XDP debug)
Size: A4	Document Number: Fircrest 13"
Rev: X01	
Date: Thursday, April 18, 2019	Sheet 99 of 106

Table of Content

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content
Size: A4 | Document Number: Fircrest 13" | Rev: X01
Date: Thursday, April 18, 2019 | Sheet 100 of 106

Change notes –

DATE	VERSON	DATE	Page	Modify List	OWNER
	X00				
	X00				
	X00				
	X00				
	X00				
	X00				
	X00				
	X00				
	X00				
	X00				
	X00				
	X00				
	X00				
	X00				

ALL

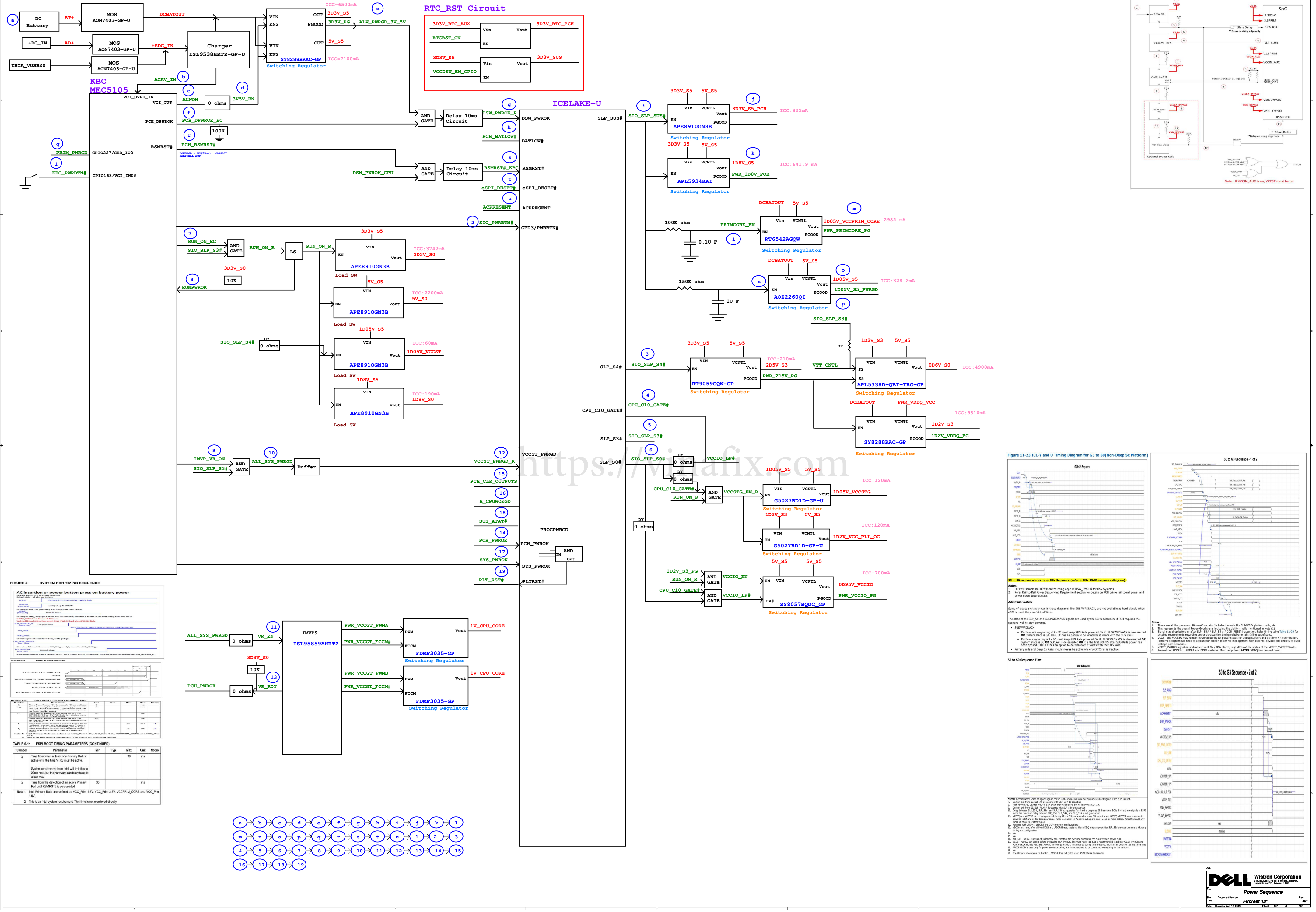
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

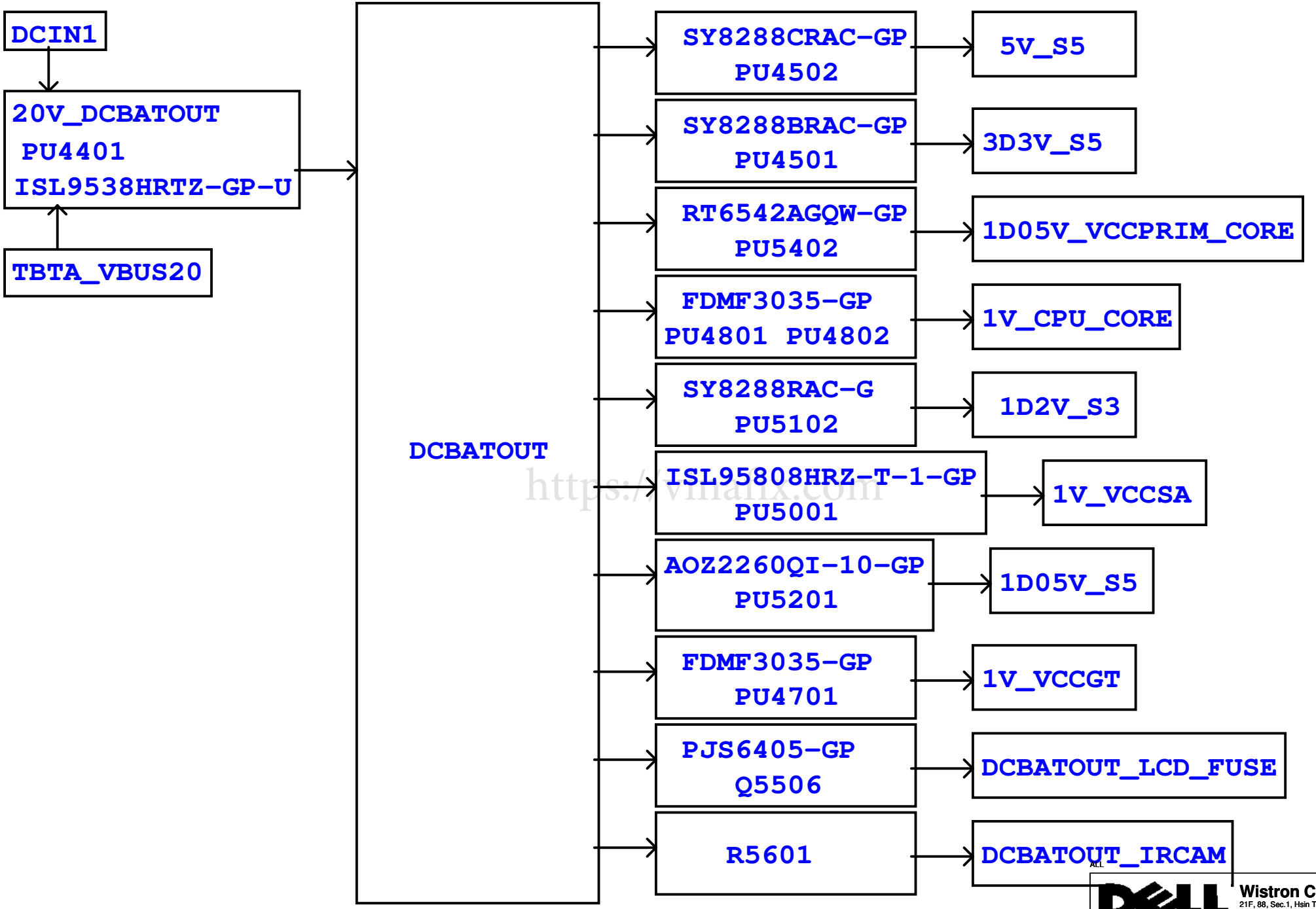
Title: Change History

Size: A3 | Document Number: Fircrest 13" | Rev: X01

Date: Thursday, April 18, 2019 | Sheet 101 of 106

Bandon /NorthBay Power up sequence diagram (deep Sx Platform)





ALL

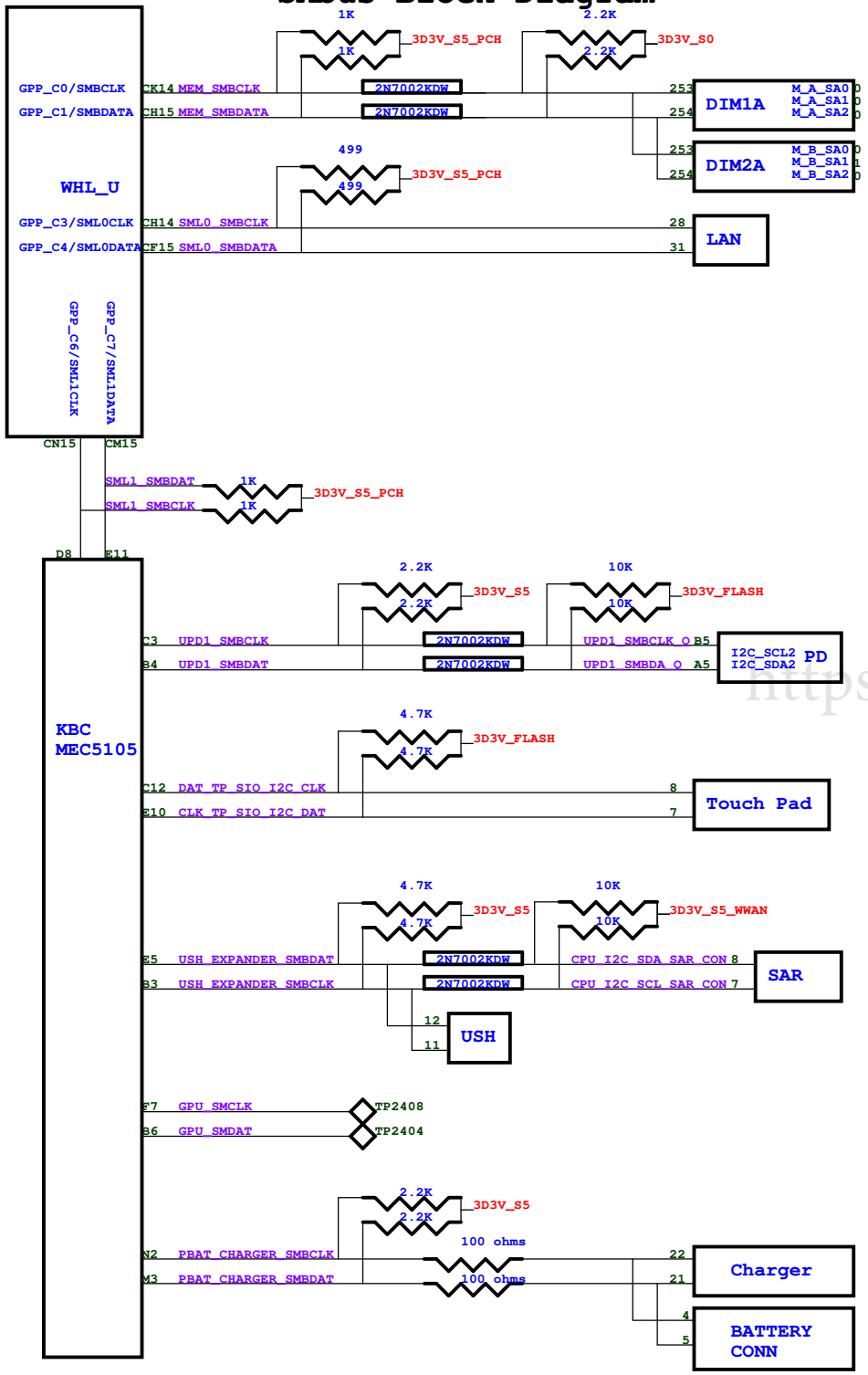
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
A3	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 103 of 106

SMbus Block Diagram



I2C Block Diagram

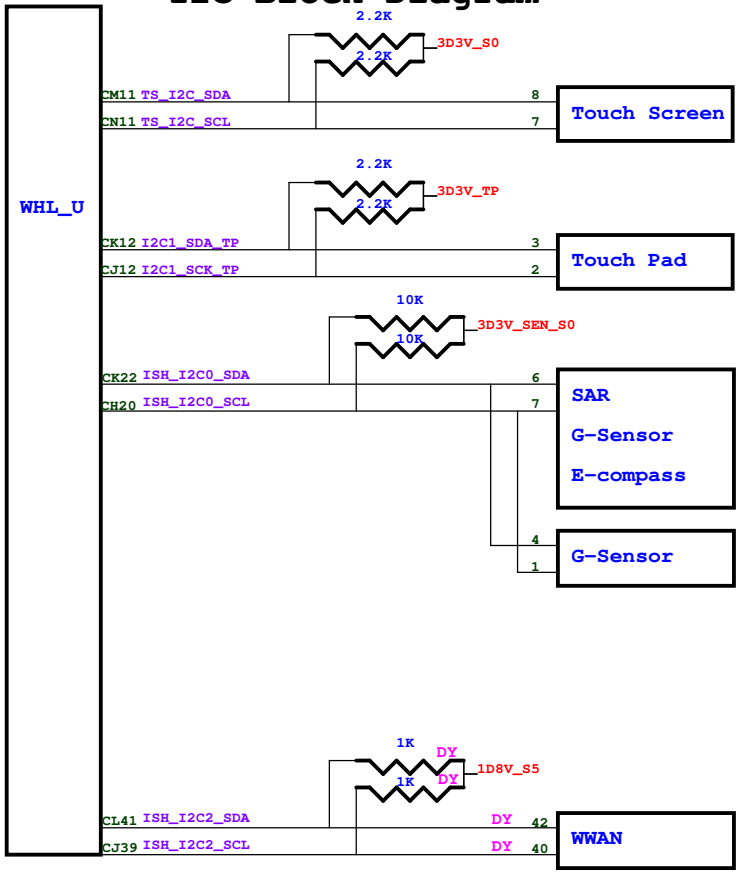


Table 6-103. Bus Capacitance/Pull-Up Resistor Relationship

Standard Mode (100kHz) - Pull-up / Pull-down Resistor Settings		
Total Bus Capacitance (C_b)	External Pull-up	PCH Pull Down Strength (Refer EDS)
Upto 400 pF	2.2KΩ	100Ω
Fast Mode (400kHz) - Mode Pull-up/ Pull-down Strength Settings		
Total Bus Capacitance (C_b)	External Pull-up	PCH Pull Down Strength
Upto 100pF	2.7KΩ	100Ω
Upto 200pF	1.5KΩ	
Upto 300pF	1KΩ	
Upto 400 pF	680Ω	
Fast mode Plus (1MHz) - Pull-up/Pull-down strength Settings		
Total Bus Capacitance (C_b)	External Pull-up	PCH Pull Down Strength
Upto 50pF	2.2KΩ	100Ω
Upto 100pF	1.2KΩ	
Upto 200pF	560Ω	
Upto 300pF	390Ω	
Upto 400 pF	270Ω	67Ω

LAN DATASHEET

Pin Name	Pin #	Type	Op Mode	Name and Function
SMB_CLK	28	O/d	Bi-dir	SMBus clock. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 499Ω resistor (while in Sx mode).
SMB_DATA	31	O/d	Bi-dir	SMBus data. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 499Ω resistor (while in Sx mode).

ALL

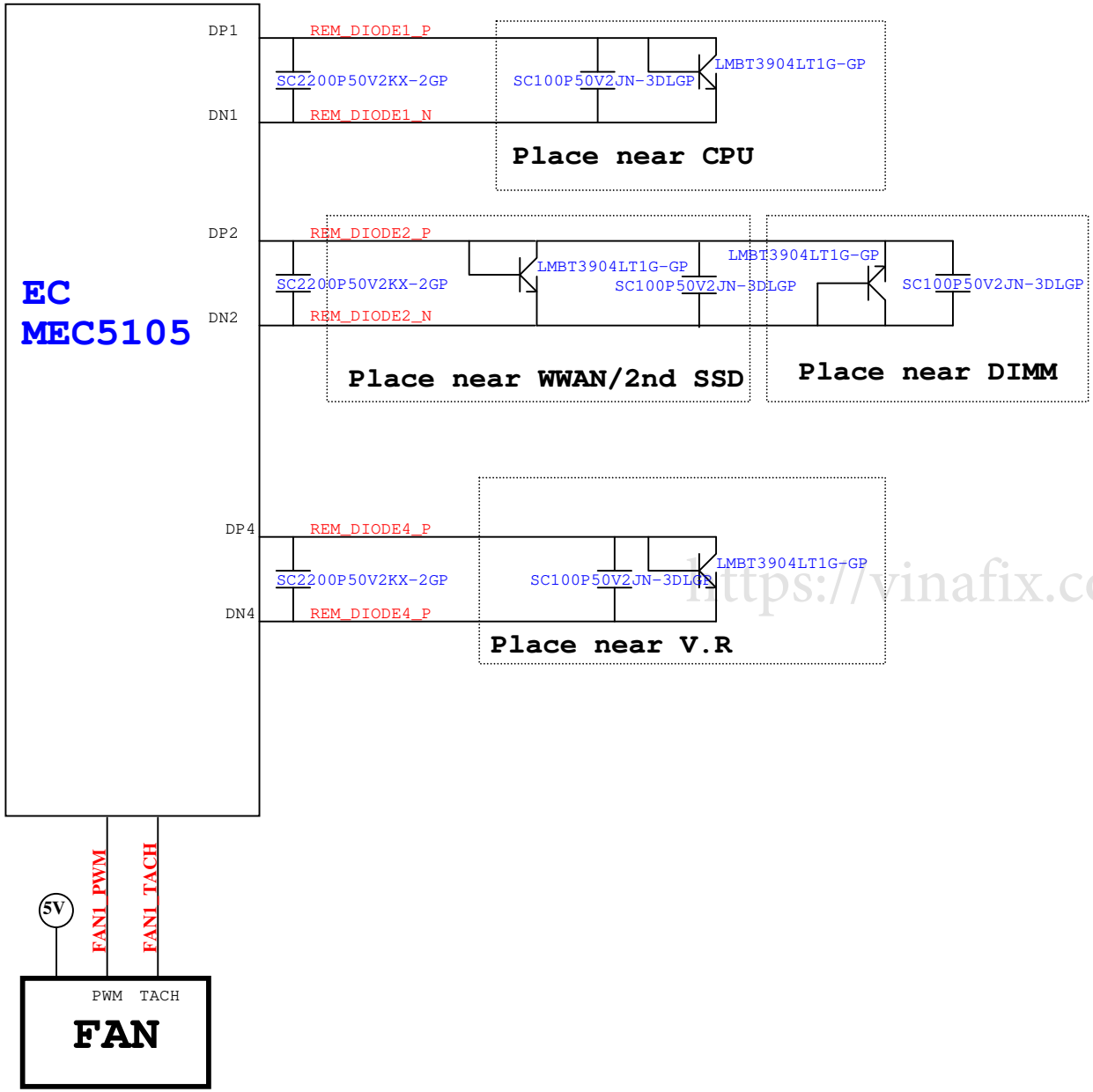
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS/I2C BLOCK DIAGRAM

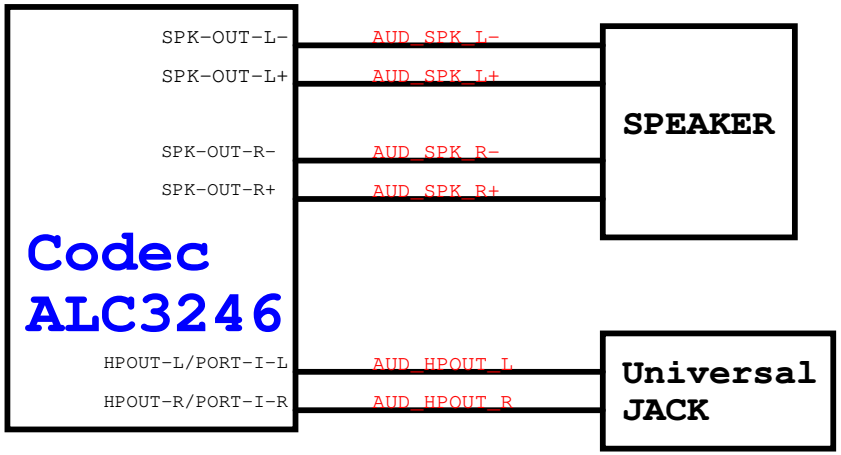
Size: A3 | Document Number: Fircrest 13" | Rev: X01

Date: Thursday, April 18, 2019 | Sheet 104 of 106

Thermal Block Diagram



Audio Block Diagram



ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL/AUDIO BLOCK DIAGRAM

Size	Document Number	Rev
A4	Fircrest 13"	X01

Date: Thursday, April 18, 2019 Sheet 105 of 106

ALL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CLK Block***

Size	Document Number	Rev
A4	***Fircrest 13"***	***X01***

Date: Thursday, April 18, 2019 Sheet 106 of 106