Tiger&Serval AMD Gen2 Logic Schematics

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Title	Cover Page	LCFC	
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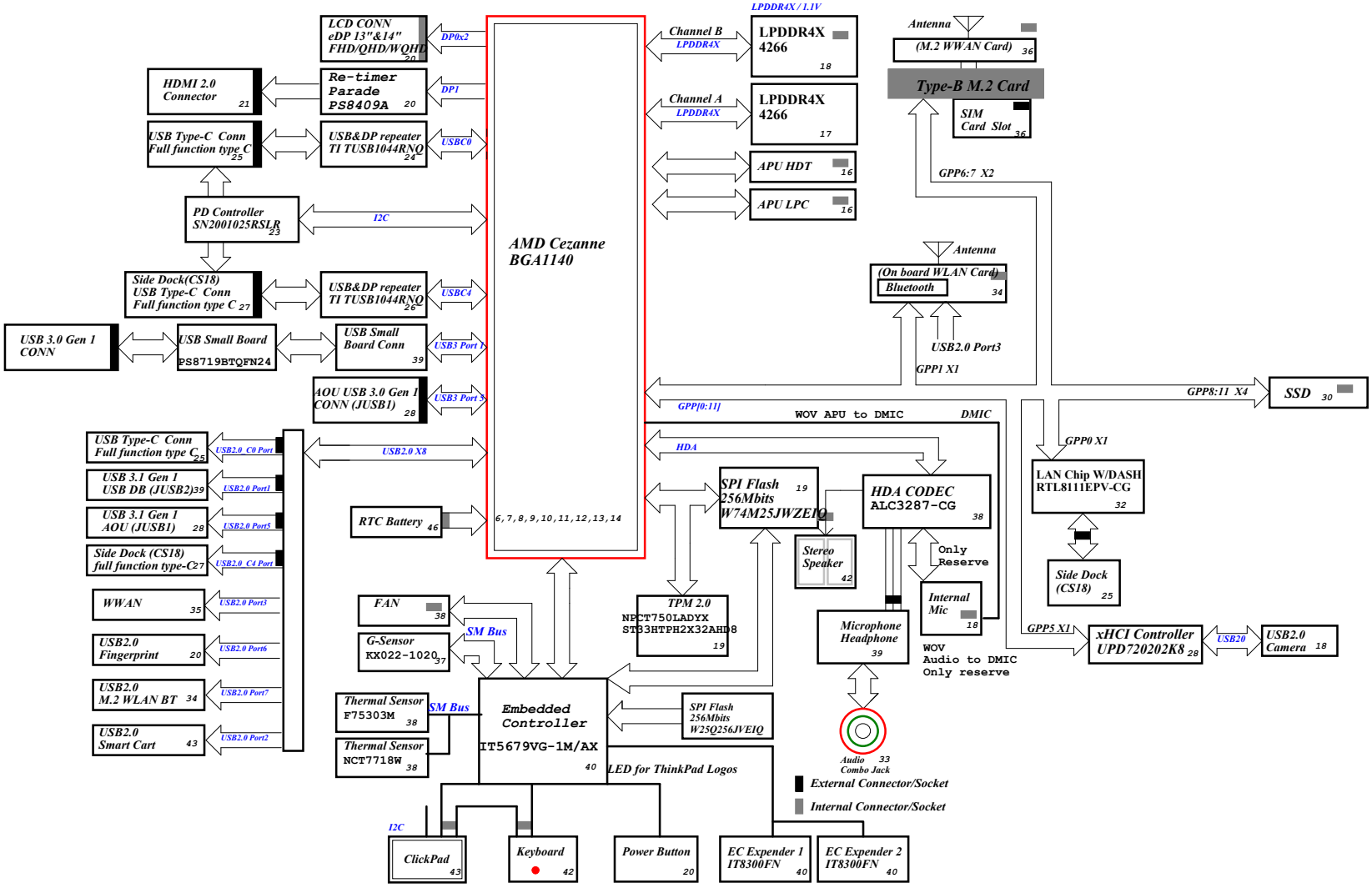

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Title: Block Diagram_EE

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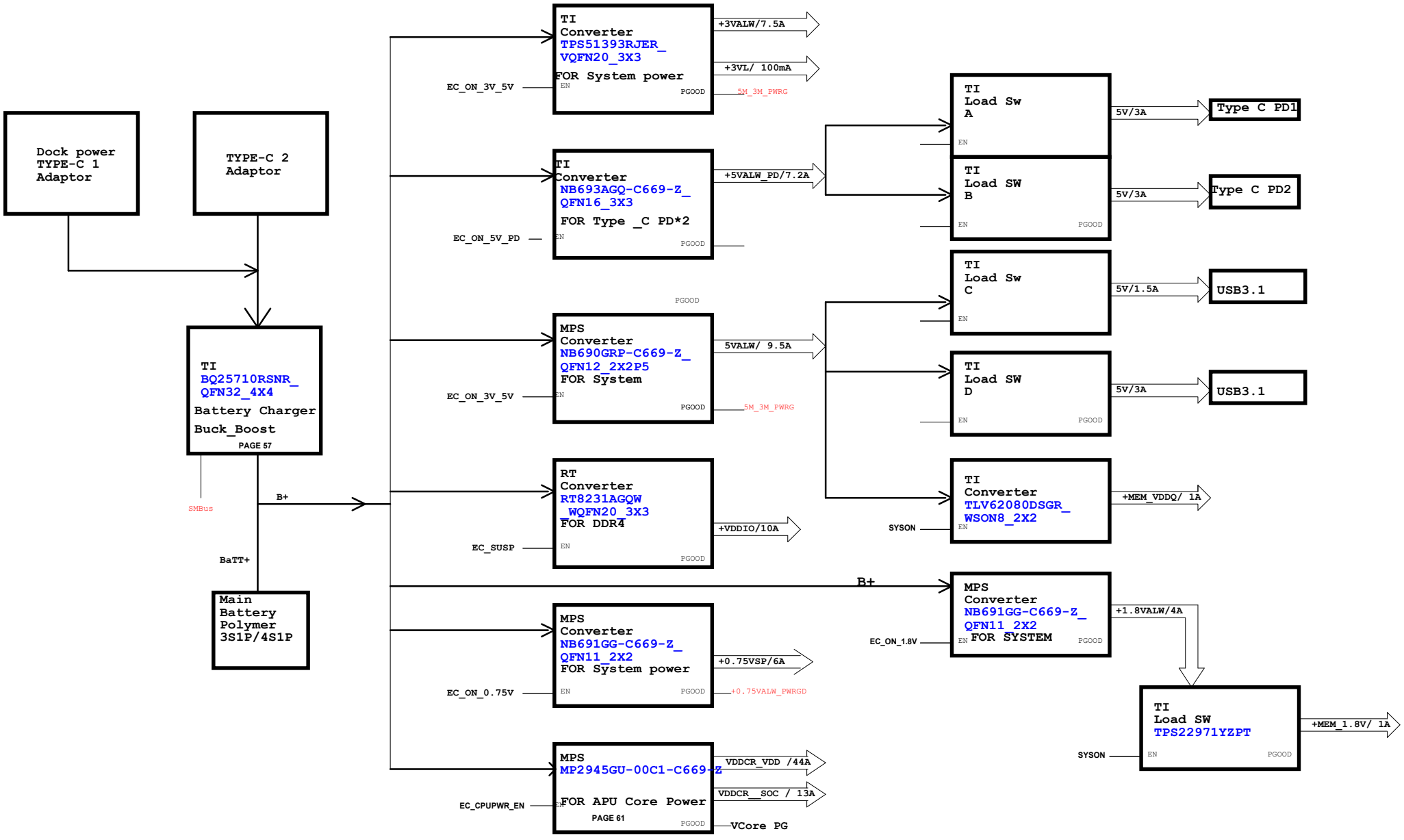

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Title: Block Diagram_PWR

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PD I2C address table

Port	Master	Slave	End Port	Address	Description
I2C_EC	EC	PD	PORTA	0x23	ADCIN1=0.1079#2 ; ADCIN2=1#7 ADCIN1 decoded value = 2 ADCIN2 decoded value = 7 I2C address index = #4 A port: 0100011 B port: 0100111
			PORTB	0x27	
I2C2S	APU	PD	PORTA	0x23	Confirm with Max
			PORTB	0x27	
I2C3M	PD	APU	USBC0	0x5C	The USB PD I2C Slave responds to a 7-bit address.
			USBC4	0x52	
	PD	EEPROM	EEPROM	0x50	The first 4 bits of the Slave address are set to 1010 The next 3 bits, A2, A1 and A0, A2=A1=A0=0 Address:1010000
	PD	Redriver-C	Redriver-C	0x47	UEQ1/A1 = 0 UEQ0/A0 = 1 Address:1000111
		Redriver-D	Redriver-D	0x44	UEQ1/A1 = 0 UEQ0/A0 = 0 Address:1000100

EC I2C address table

Port	Master	Slave	End Port	Address	Description
SMBUS0	DASH LAN	EC	DASH LAN	0x1C	confirm with David Liu
			APU	N/A	Not communicate with EC;confirm with David Liu
SMBUS1	EC	VRM	VRM	0x20	To support multiple VR devices used with the same PMBusTM interface, PMBusTM address programming either by ADDR
	EC	CHARGER	CHARGER	0x12	The device performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus.
	EC	Battery	Battery	0x16	Confirm with Luodi
SMBUS2	APU	PD	PD	N/A	Refer to PD table
SMBUS3	EC	APU	APU Thermal	0x98	confirm with David Liu
	EC	P sensor	P sensor	0x44	The I2C device has a 7 bit Slave Address (default 0x44H) in the control byte
SMBUS4	EC	HDMI	HDMI	0x10-0x2F	I2C address selection. Internally pulled down at ~150kohm L:Slave address 0x10-0x2F(default) H:Slave address 0x90-0x9F;0xD0-0xDF
	EC	TS 1	TS 1	0x4D	1001_101xb
	EC	TS 2	TS 2 (SMBUS)	0x4C	NCT7718W I2C/ SMBusTM address is 1001100xb
	EC	G sensor	G sensor (I2C)	0x18(ST) 0x18(BOSCH)	The Slave Address (SAD) associated to the LIS2DWL is 001100xb where the x bit is modified by the SA0/SDO pin in order to modify the device address(0011000)
SMBUS5 (I2C)	EC	Expander1	Expander1	0x20	The I2C slave address is {01000, CHIP_ID1,CHIP_ID0} Address:0100000
	EC	Expander2	Expander2	0x23	Address:0100011

APU I2C address table

Port	Master	Slave	End Port	Address	Description
I2C0	APU	PD	PORTA	0x23	Confirm with Max
			PORTB	0x27	
		NFC	NFC	0x29	
I2C1	APU	T_PANEL	T_PANEL	0x10 ELAN 0x34 Melfas 0x39 Raydium	
I2C2	APU	CP	CP	0x15	I2C device address: 0x15
I2C3 (SMBUS)	APU	DASH LAN	DASH LAN	0xC8	Confirm with David Zhou
			EC	N/A	Not communicate with EC;confirm with David Liu

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Title: *I2C/SMBUS*

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UC1 Pro R7@
S IC RYZEN 100-000000289 1.9G CPU IP 01!
SA0000BM110

UC1 Pro R5@
S IC RYZEN 100-000000290 2.3G CPU IP 01!
SA0000BM610

UC1 non Pro R5@
S IC RYZEN 100-000000287 2.3G CPU IP 01!
SA0000B9G20

UC1 Pro R3@
S IC RYZEN 100-000000291 2.6G CPU IP 01!
SA0000BM710

APU PN

ZZZ1 PCB@
PCB HX3B5 NM-D441 NS-D441/D442
DAZ22900101

ZZZ2 MB PCB@
PCB 229 NM-D441 REV2 M/B
DAB00004Q20

ZZZ3 USB PCB@
PCB 229 NS-D441 REV1 USB/B
DAB00004R10

ZZZ4 PWR PCB@
PCB 229 NS-D442 REV1 PWR/B
DAB00004S10

PCB PN

ZZZ5 HDMI_LOGO@
HDMI LOGO
RO0000040J

HDMI LOGO PN

DRAM X76

M32GX4@ ZZZ14
MICRON 32G
X764BK01001

H32GX4@ ZZZ16
HYNIX 32G
X764BK01002

M16GX4@ ZZZ17
MICRON 16G
X764BK01003

H16GX4@ ZZZ18
HYNIX 16G
X764BK01004

S16GX4@ ZZZ19
SAMSUNG 16G
X764BK01005

M8GX4@ ZZZ20
MICRON 8G
X764BK01006

H8GX4@ ZZZ21
HYNIX 8G
X764BK01007

S8GX4@ ZZZ22
SAMSUNG 8G
X764BK01008

CONFIGURE

DRAM PN

BOARD ID

Hynix 32G

UD1 H32G@ H9HCNNNFAMMLXR-NEE SA0000AXB00
UD2 H32G@ H9HCNNNFAMMLXR-NEE SA0000AXB00
UD3 H32G@ H9HCNNNFAMMLXR-NEE SA0000AXB00
UD4 H32G@ H9HCNNNFAMMLXR-NEE SA0000AXB00
RC263 H32G@ 1/20W_10K_5%_0201 SD0431002YT
RC273 H32G@ 1/20W_10K_5%_0201 SD0431002YT
RC265 H32G@ 1/20W_10K_5%_0201 SD0431002YT
RC275 H32G@ 1/20W_10K_5%_0201 SD0431002YT

Micron 32G

UD1 M32G@ MT53E2G32D4NQ-046-WTA_VFBGA200 SA0000ANA10
UD2 M32G@ MT53E2G32D4NQ-046-WTA_VFBGA200 SA0000ANA10
UD3 M32G@ MT53E2G32D4NQ-046-WTA_VFBGA200 SA0000ANA10
UD4 M32G@ MT53E2G32D4NQ-046-WTA_VFBGA200 SA0000ANA10
RC272 M32G@ 1/20W_10K_5%_0201 SD0431002YT
RC273 M32G@ 1/20W_10K_5%_0201 SD0431002YT
RC274 M32G@ 1/20W_10K_5%_0201 SD0431002YT
RC266 M32G@ 1/20W_10K_5%_0201 SD0431002YT

Micron 16G

UD1 M16G@ MT53E1G32D2NP-046-WTA_WFBGA200 SA0000AN910
UD2 M16G@ MT53E1G32D2NP-046-WTA_WFBGA200 SA0000AN910
UD3 M16G@ MT53E1G32D2NP-046-WTA_WFBGA200 SA0000AN910
UD4 M16G@ MT53E1G32D2NP-046-WTA_WFBGA200 SA0000AN910
RC263 M16G@ 1/20W_10K_5%_0201 SD0431002YT
RC264 M16G@ 1/20W_10K_5%_0201 SD0431002YT
RC265 M16G@ 1/20W_10K_5%_0201 SD0431002YT
RC275 M16G@ 1/20W_10K_5%_0201 SD0431002YT

Micron 8G

UD1 M8G@ MT53E512M32D2NP-046-WTE_WFBGA200 SA00009ET00
UD2 M8G@ MT53E512M32D2NP-046-WTE_WFBGA200 SA00009ET00
UD3 M8G@ MT53E512M32D2NP-046-WTE_WFBGA200 SA00009ET00
UD4 M8G@ MT53E512M32D2NP-046-WTE_WFBGA200 SA00009ET00
RC272 M8G@ 1/20W_10K_5%_0201 SD0431002YT
RC264 M8G@ 1/20W_10K_5%_0201 SD0431002YT
RC265 M8G@ 1/20W_10K_5%_0201 SD0431002YT
RC275 M8G@ 1/20W_10K_5%_0201 SD0431002YT

Samsung 16G

UD1 S16G@ K4UBE3D4AA-MGCR_FBGA200 SA0000AMQ10
UD2 S16G@ K4UBE3D4AA-MGCR_FBGA200 SA0000AMQ10
UD3 S16G@ K4UBE3D4AA-MGCR_FBGA200 SA0000AMQ10
UD4 S16G@ K4UBE3D4AA-MGCR_FBGA200 SA0000AMQ10
RC263 S16G@ 1/20W_10K_5%_0201 SD0431002YT
RC273 S16G@ 1/20W_10K_5%_0201 SD0431002YT
RC274 S16G@ 1/20W_10K_5%_0201 SD0431002YT
RC275 S16G@ 1/20W_10K_5%_0201 SD0431002YT

Hynix 16G

UD1 H16G@ H9HCNNNCPMMLXR-NEE_FBGA200 SA0000AMB10
UD2 H16G@ H9HCNNNCPMMLXR-NEE_FBGA200 SA0000AMB10
UD3 H16G@ H9HCNNNCPMMLXR-NEE_FBGA200 SA0000AMB10
UD4 H16G@ H9HCNNNCPMMLXR-NEE_FBGA200 SA0000AMB10
RC272 H16G@ 1/20W_10K_5%_0201 SD0431002YT
RC273 H16G@ 1/20W_10K_5%_0201 SD0431002YT
RC265 H16G@ 1/20W_10K_5%_0201 SD0431002YT
RC275 H16G@ 1/20W_10K_5%_0201 SD0431002YT

Samsung 8G

UD1 S8G@ K4U6E3S4AA-MGCR_FBGA200 SA0000AMP10
UD2 S8G@ K4U6E3S4AA-MGCR_FBGA200 SA0000AMP10
UD3 S8G@ K4U6E3S4AA-MGCR_FBGA200 SA0000AMP10
UD4 S8G@ K4U6E3S4AA-MGCR_FBGA200 SA0000AMP10
RC272 S8G@ 1/20W_10K_5%_0201 SD0431002YT
RC273 S8G@ 1/20W_10K_5%_0201 SD0431002YT
RC274 S8G@ 1/20W_10K_5%_0201 SD0431002YT
RC275 S8G@ 1/20W_10K_5%_0201 SD0431002YT

Hynix 8G

UD1 H8G@ H9HCNNNBKMMLXR-NEE_FBGA200 SA0000AMA10
UD2 H8G@ H9HCNNNBKMMLXR-NEE_FBGA200 SA0000AMA10
UD3 H8G@ H9HCNNNBKMMLXR-NEE_FBGA200 SA0000AMA10
UD4 H8G@ H9HCNNNBKMMLXR-NEE_FBGA200 SA0000AMA10
RC263 H8G@ 1/20W_10K_5%_0201 SD0431002YT
RC264 H8G@ 1/20W_10K_5%_0201 SD0431002YT
RC274 H8G@ 1/20W_10K_5%_0201 SD0431002YT
RC275 H8G@ 1/20W_10K_5%_0201 SD0431002YT

BOM Structure	Description	BOM Structure	Description
Pro R7@	Pro R7 CPU	non Pro R7@	non Pro R7 CPU
Pro R5@	Pro R5 CPU	non Pro R5@	non Pro R5 CPU
Pro R3@	Pro R3 CPU	non Pro R3@	non Pro R3 CPU
M32GX4@	Micron 32GB DRAM of X76	EC_CD@	EC cost down part
H32GX4@	Hynix 32GB DRAM of X76	LPC@	LPC related part
M16GX4@	Micron 16GB DRAM of X76	CAM_FW@	For IR camera FW flash
H16GX4@	Hynix 16GB DRAM of X76	DASH@	Dash LAN related part
S16GX4@	Samsung 16GB DRAM of X76	NDASH@	Dash LAN not stuff
M8GX4@	Micron 8GB DRAM of X76	MS@	Modern standby part
H8GX4@	Hynix 8GB DRAM of X76	MS_NS@	Modern standby not stuff
S8GX4@	Samsung 8GB DRAM of X76	WOV@	Wake on voice
TPM@	TPM related part	WOV_R@	Resistor for wake on voice
TPM_NUV@	NUVOTON TPM part	XHCI_CD@	XHCI cost down
TPM_ST@	ST TPM part	Debug@	Debug related part
GSE_BOS@	BOS G sensor	Debug_NS@	Debug not stuff part
GSE_ST@	ST G sensor	WLAN@	WLAN related part
EMC@	EMC related part	UART@	UART related part
EMC_CD@	EMC related part cost down		
EMC_NS@	EMC related part not stuff		
EMC_NWOV@	No wake on voice		
RF@	RF related part		
RF_NEW@	RF new request part		
RF_NS@	RF not stuff part		
CD@	Cost down part		
HDT@	HDT related part		
HDMI_LOGO@	HDMI logo related part		

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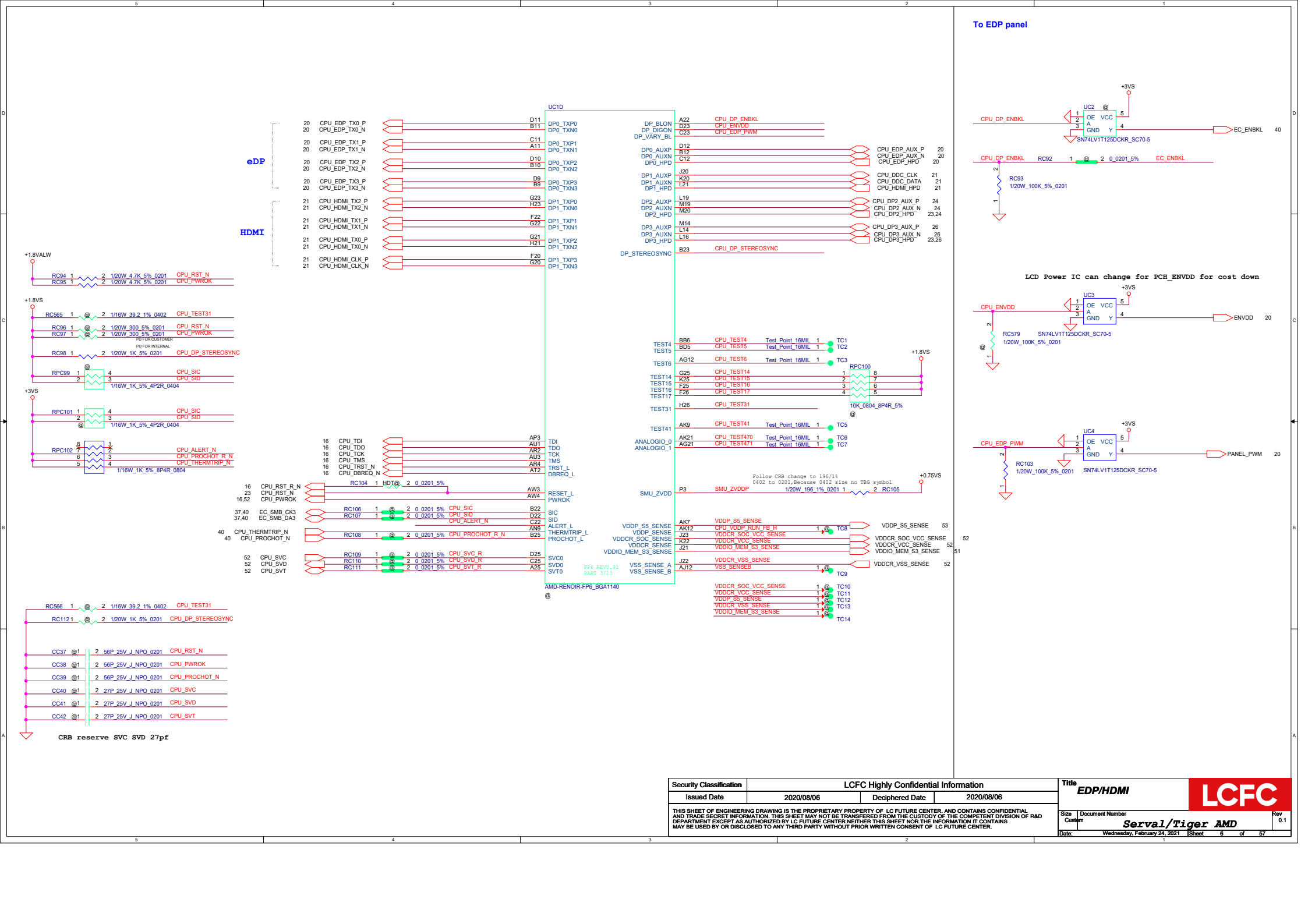
To EDP panel
eDP
HDMI
UC1D
AMD-RENOIR-FP6_BGA1140
LCD Power IC can change for PCH_ENVDD for cost down
CRB reserve SVC SVD 27pf
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2020/08/06
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2020/08/06
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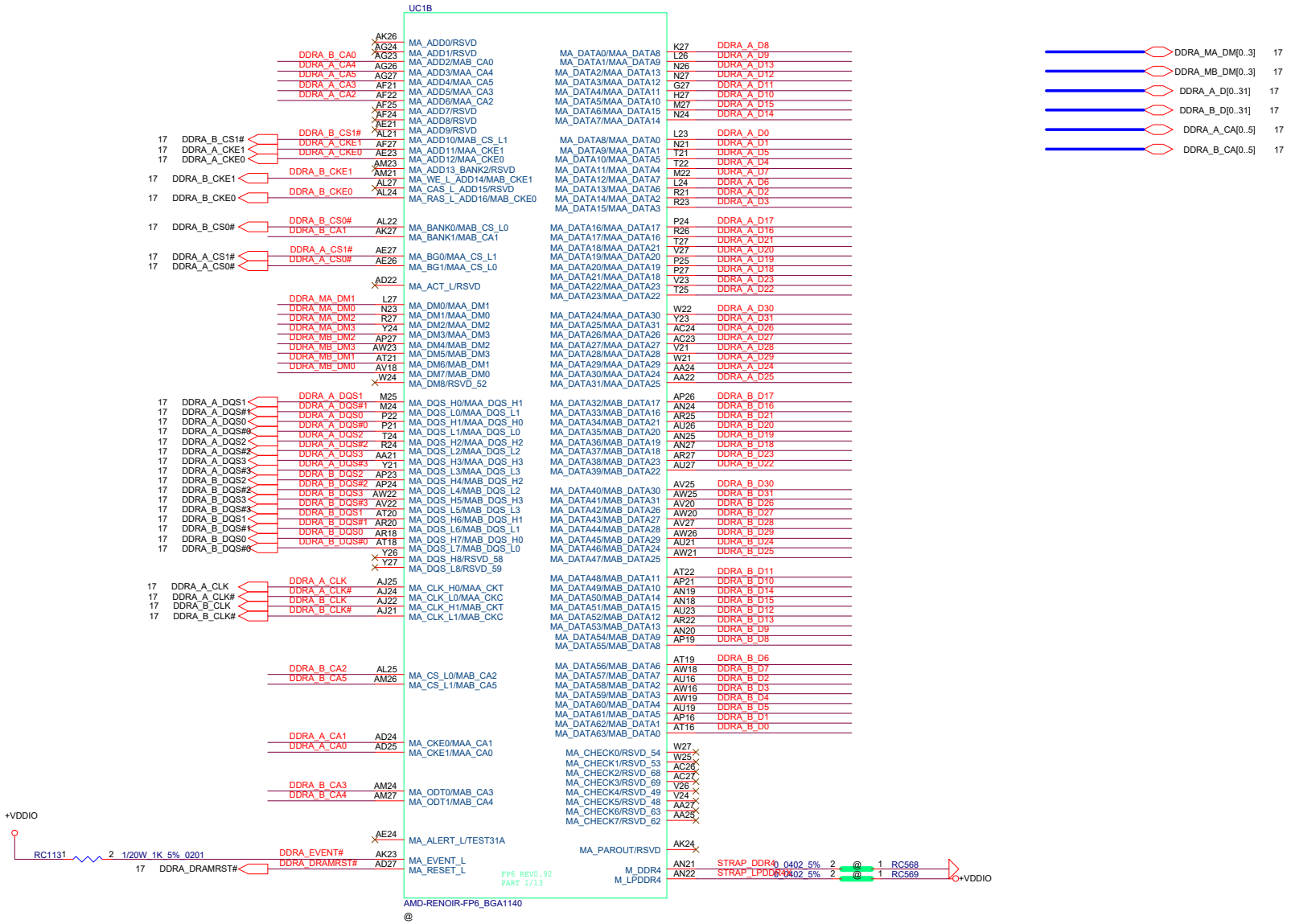

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Title: LPDDR4X-CHA

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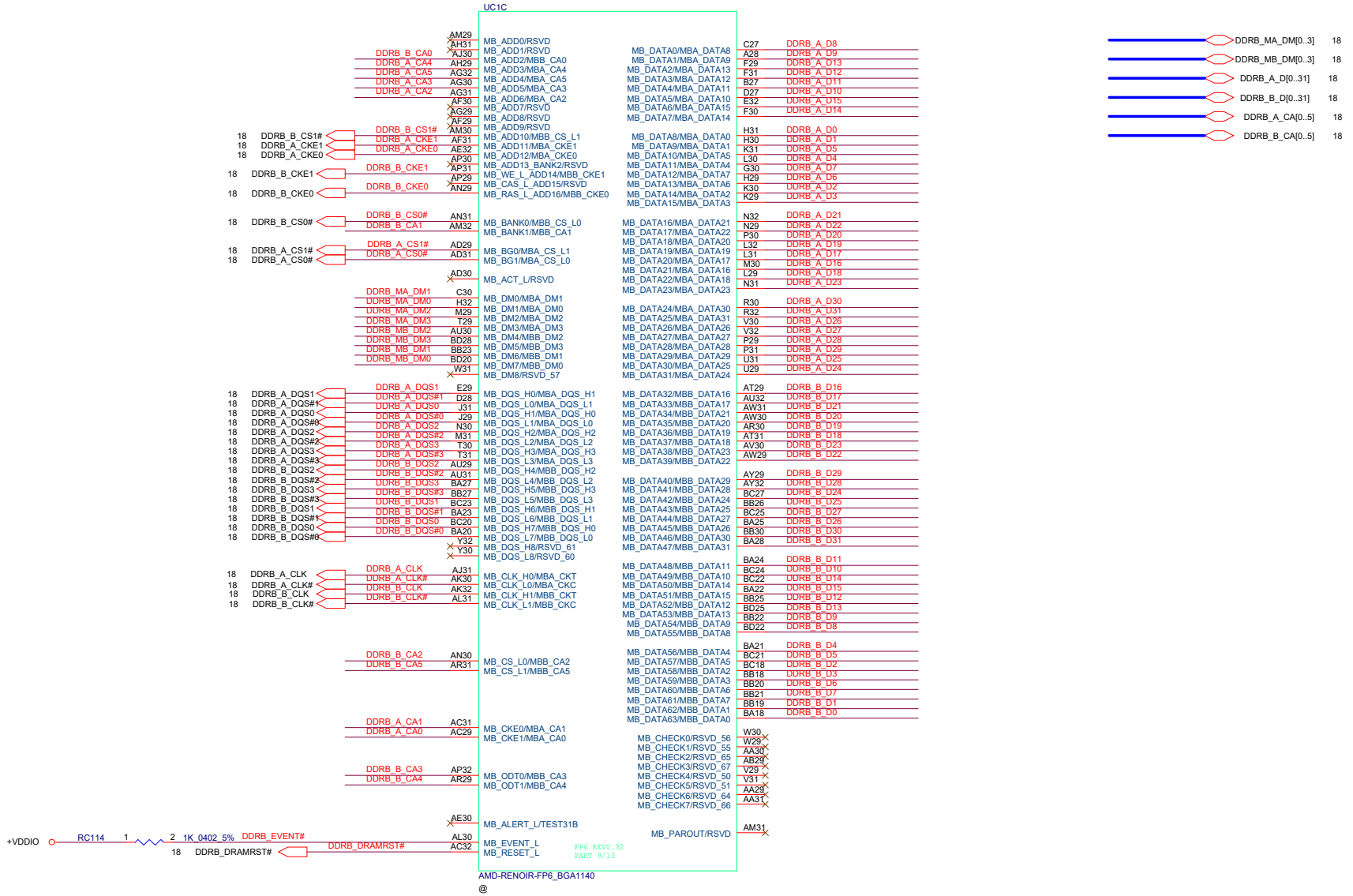

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Title: LPDDR4X-CHB

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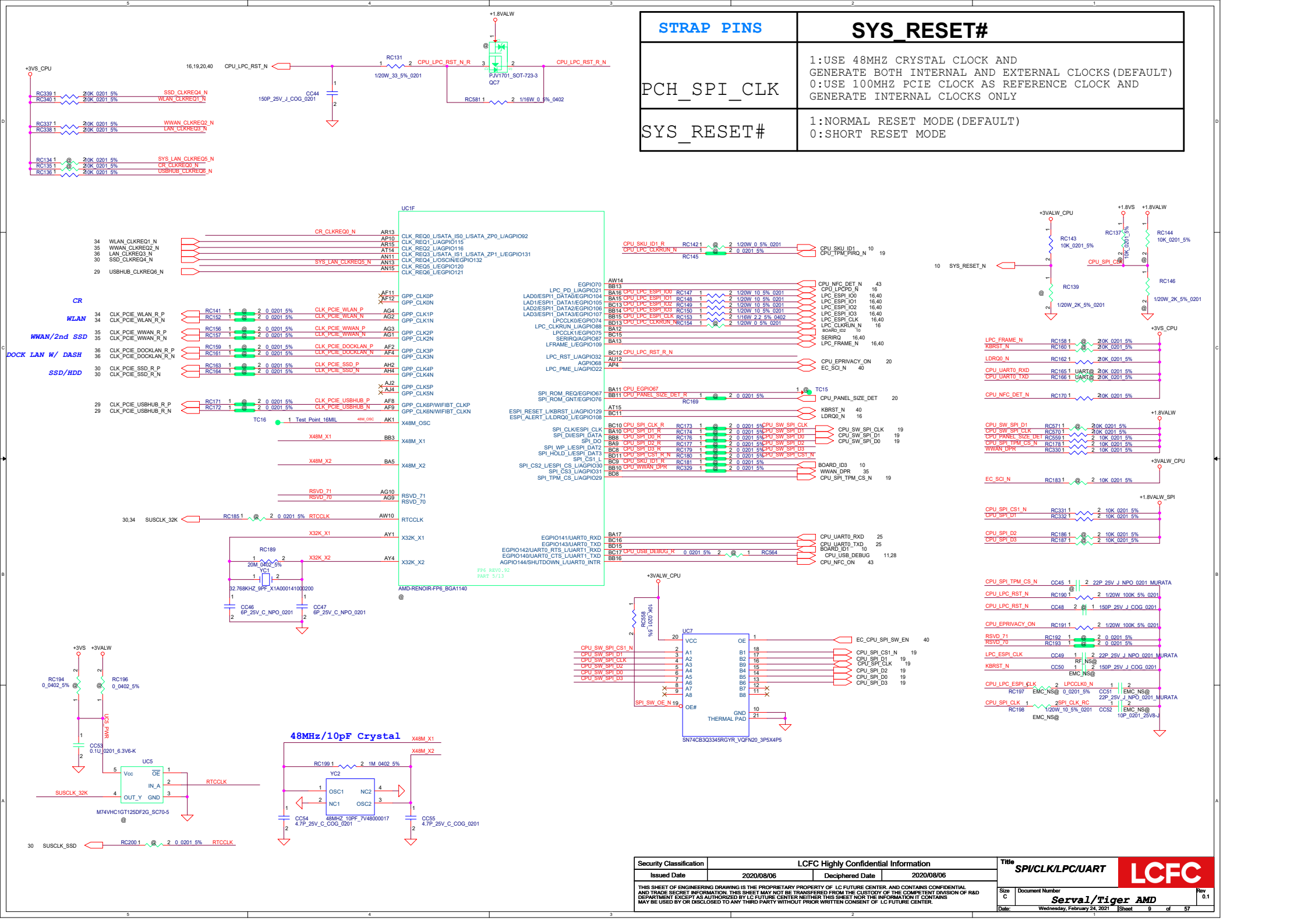
STRAP PINS	SYS_RESET#
PCH_SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE



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Title: SPI/CLK/LPC/UART

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Board ID	Description		Stuff R			
Board ID [3, 2, 1, 0]	0000	Samsung 8G	RC272	RC273	RC274	RC275
	0001	Samsung 16G	RC263	RC273	RC274	RC275
	0010	Samsung 32G	RC272	RC264	RC274	RC275
	0011	Hynix 8G	RC263	RC264	RC274	RC275
	0100	Hynix 16G	RC272	RC273	RC265	RC275
	0101	Hynix 32G	RC263	RC273	RC265	RC275
	0110	Micron 8G	RC272	RC264	RC265	RC275
	0111	Micron 16G	RC263	RC264	RC265	RC275
	1000	Micron 32G	RC272	RC273	RC274	RC266

Security Classification	LCFC Highly Confidential Information		
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Title: I2C/HDA/GPIO

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Title	PCIE/USB		
Size	Document Number		Rev
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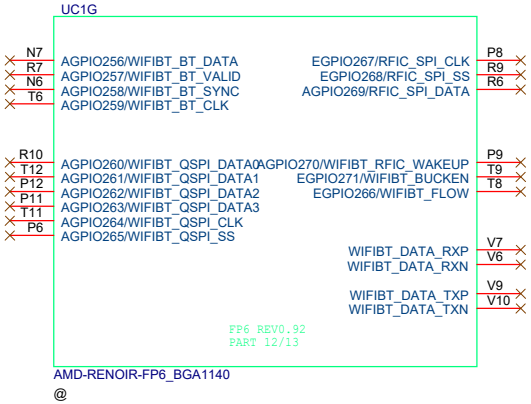

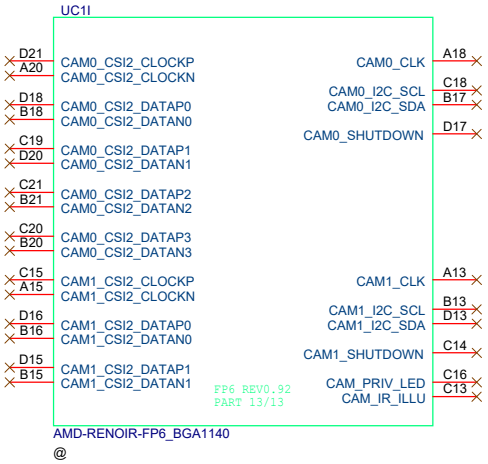

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Title: ***WIFIBT/CAM***

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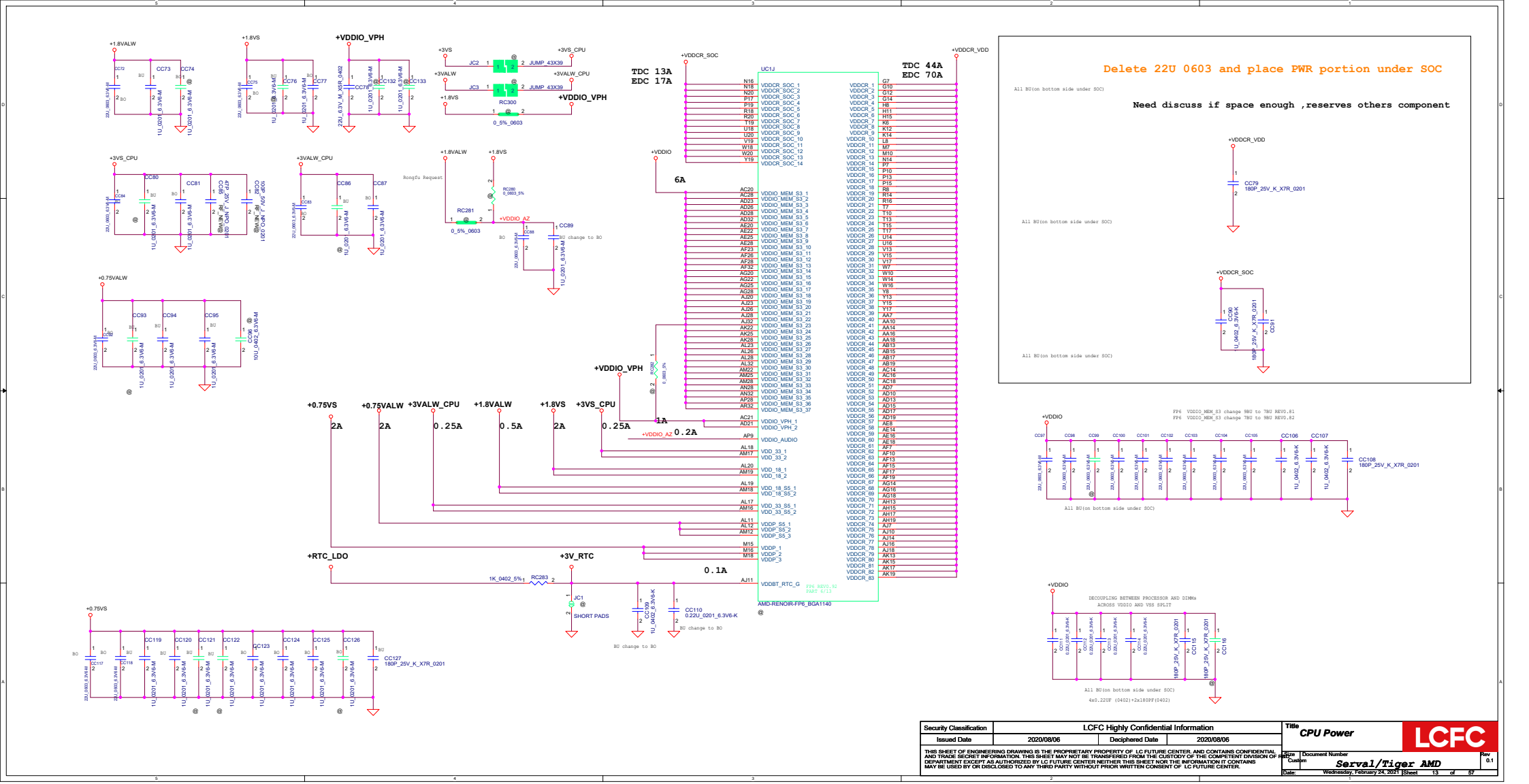

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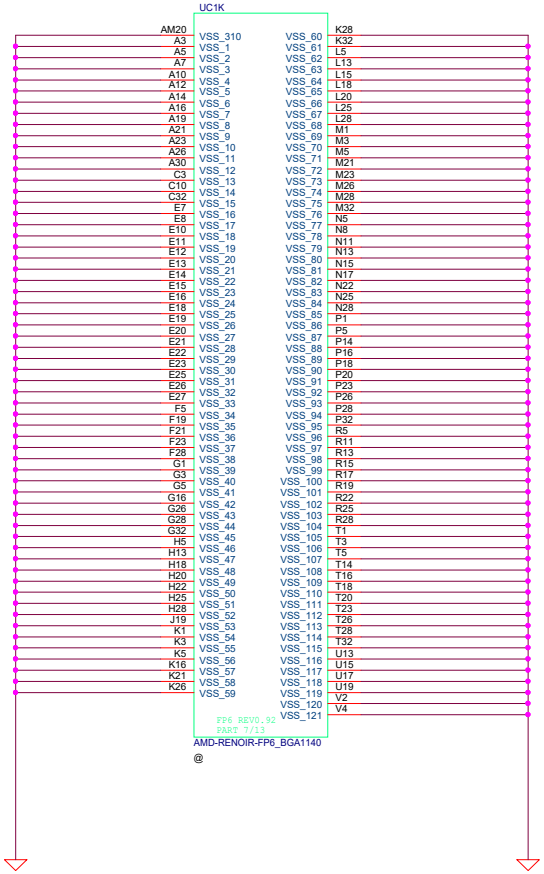

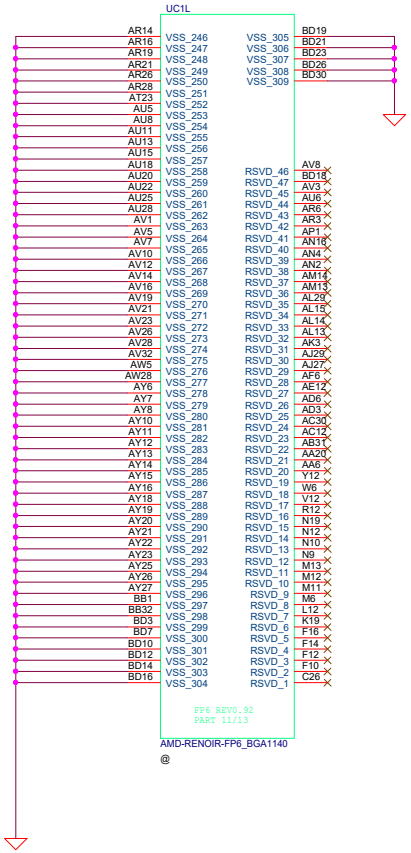

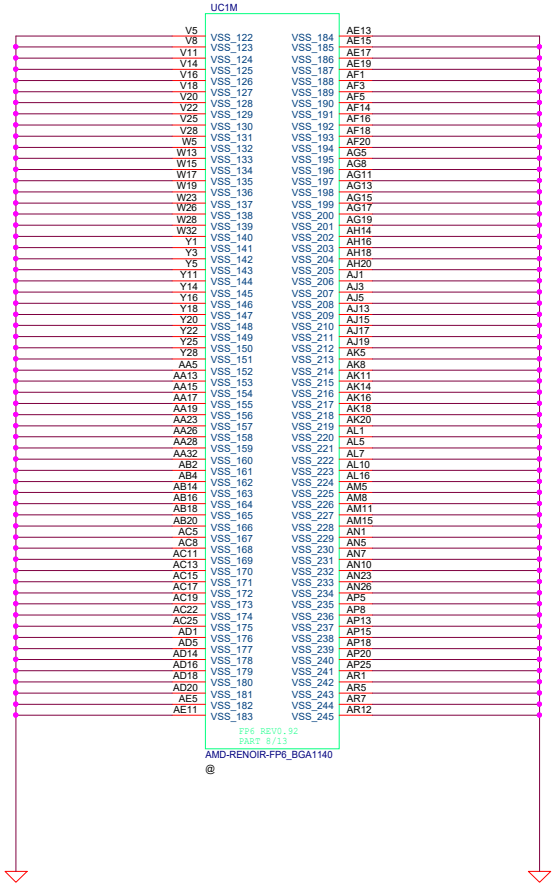

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Title: **GND**

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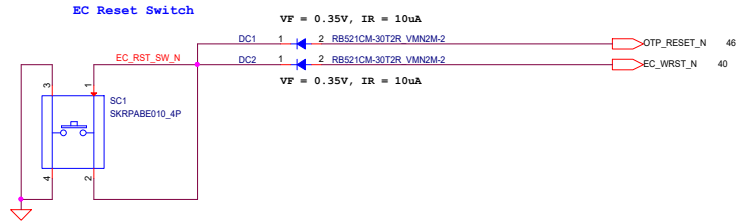
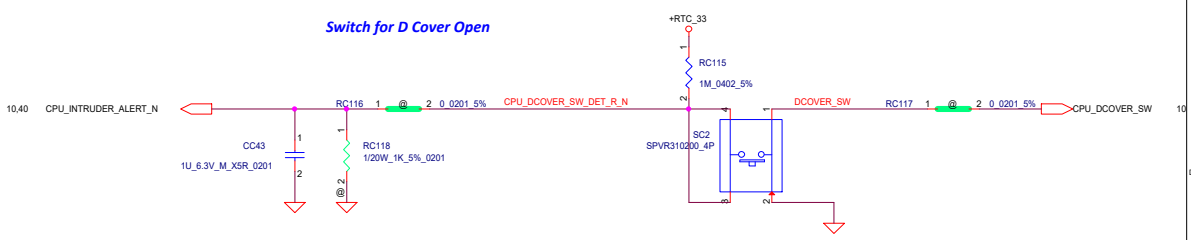




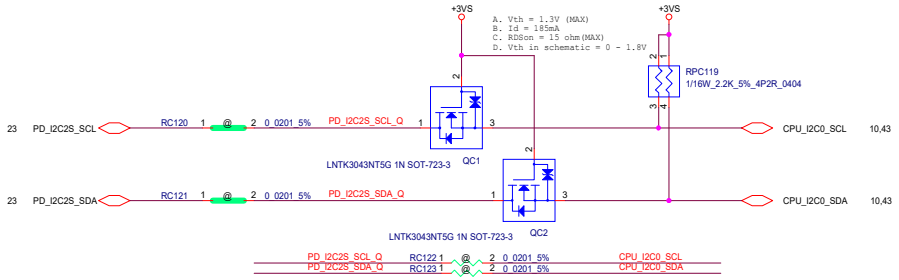
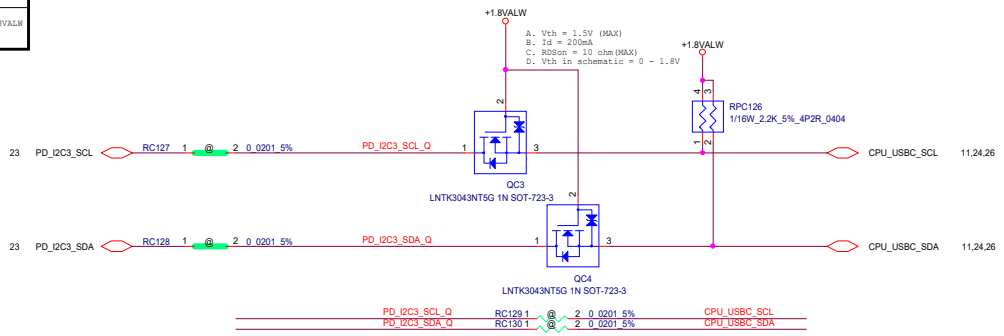


TABLE:

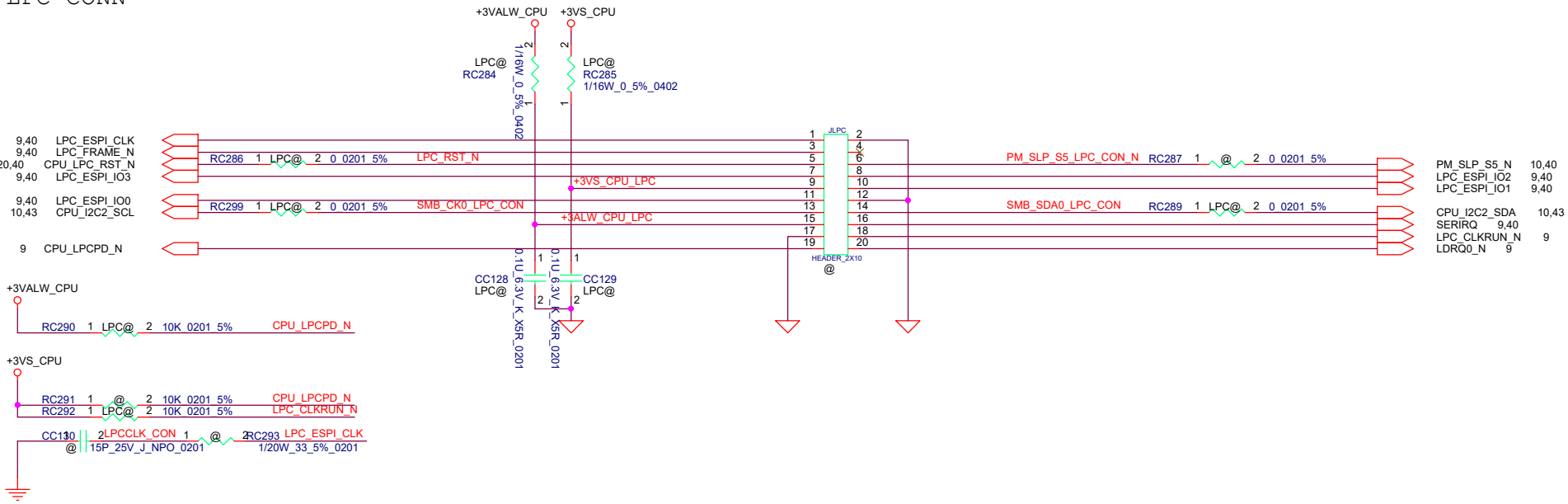
I2C1	Level Shift	PD SIDE I2C1 Slave	PU	APU SIDE I2C0 Master	PU	**NA**	**NA**
PD update FW	QC50 QC51	PD_I2C1_SCL PD_I2C1_SDA	PU_VCC3_LDO_DOCK 4.7K	APU_I2C0_SCL APU_I2C0_SDA	PU_1.8VS 2.2K	**NA**	**NA**
I2C2	Level Shift	PD SIDE I2C2 Slave	PU	EC SIDE Smbus2 Master	PU	**NA**	**NA**
PD to EC	**NA**	PD_I2C2_SCL_R PD_I2C2_SDA_R	PU_+3VL 4.7K	EC_SMB_CK2 EC_SMB_DA2	PU_+3VL 4.7K	**NA**	**NA**
I2C3	Level Shift	PD SIDE I2C3 Master	PU	APU SIDE USBC_I2C Slave	PU	USBC Redriver SIDE Slave	PU
PD for USBC redriver and APU Mux	QC14 QC5	PD_I2C3_SCL_R PD_I2C3_SDA_R	PU_V1P8_LDO_DOCK 4.7K	APU_USBC_SCL APU_USBC_SDA	PU_+1.8VALW 4.7K	APU_USBC_SCL APU_USBC_SDA	PU_+1.8VALW 4.7K



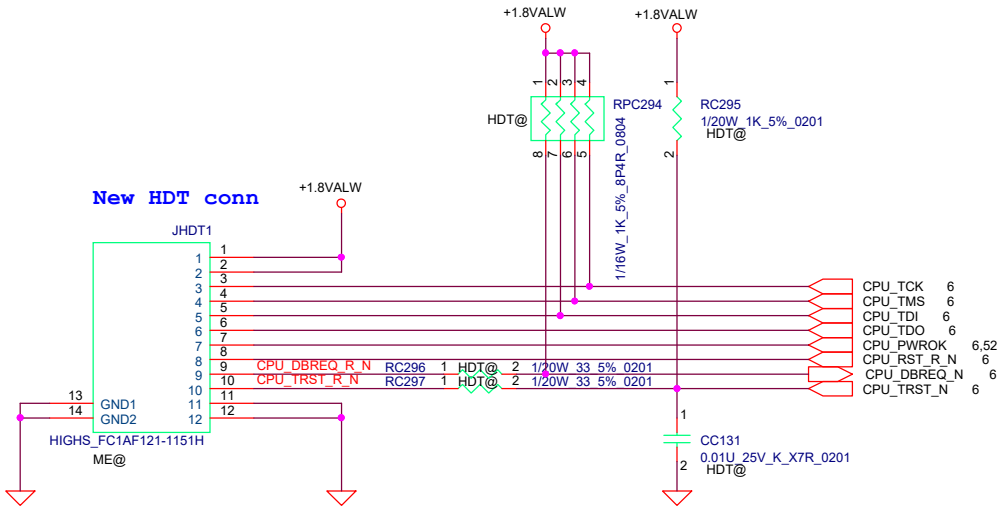
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	SMBUS/SW	LCFC	
Size C	Document Number Serval/Tiger AMD		Rev 0.1
Date: Wednesday, February 24, 2021	Sheet 15 of 57		

LPC CONN



HDT CONN



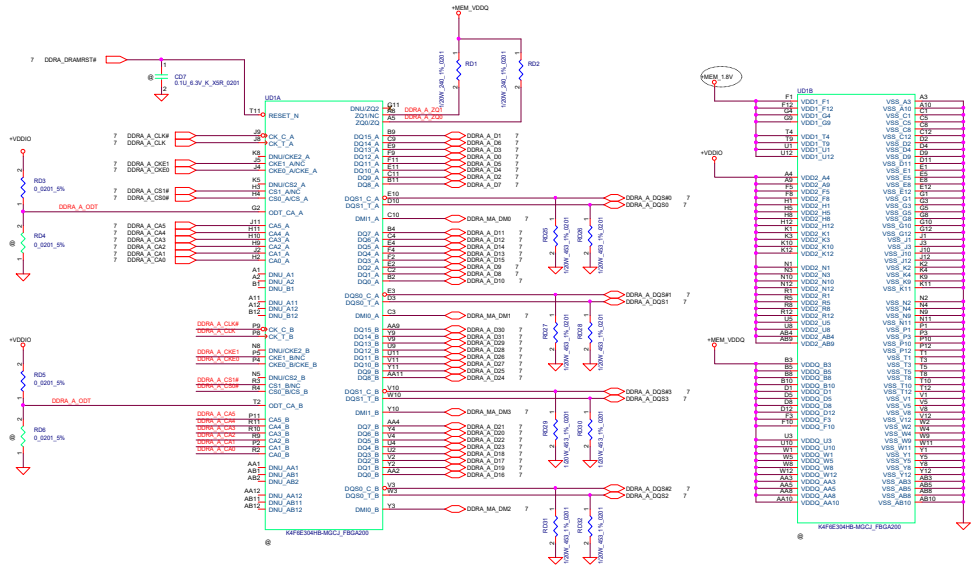
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

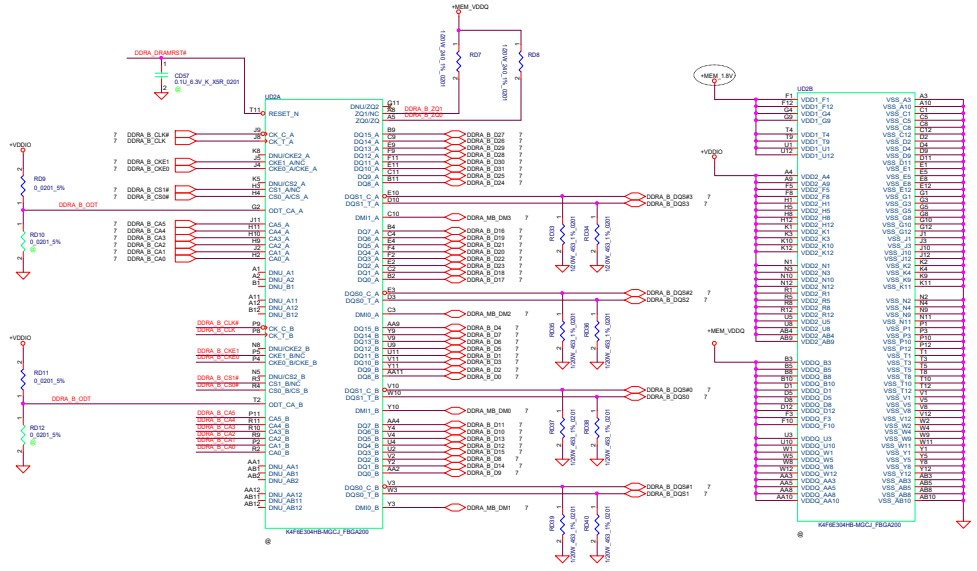
Title: **HDT/LPC Debug**

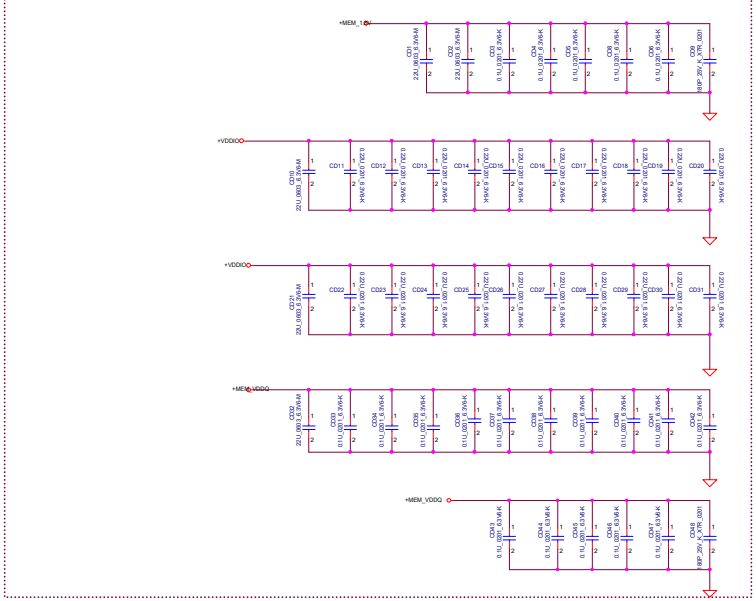
LCFC

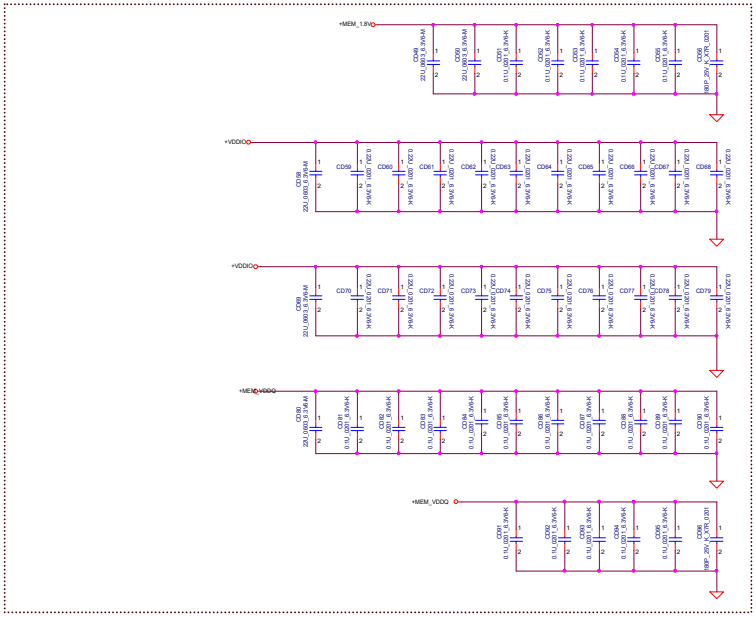
Size	Document Number	Rev
B	Serval/Tiger AMD	0.1

Date: Wednesday, February 24, 2021 Sheet 16 of 57



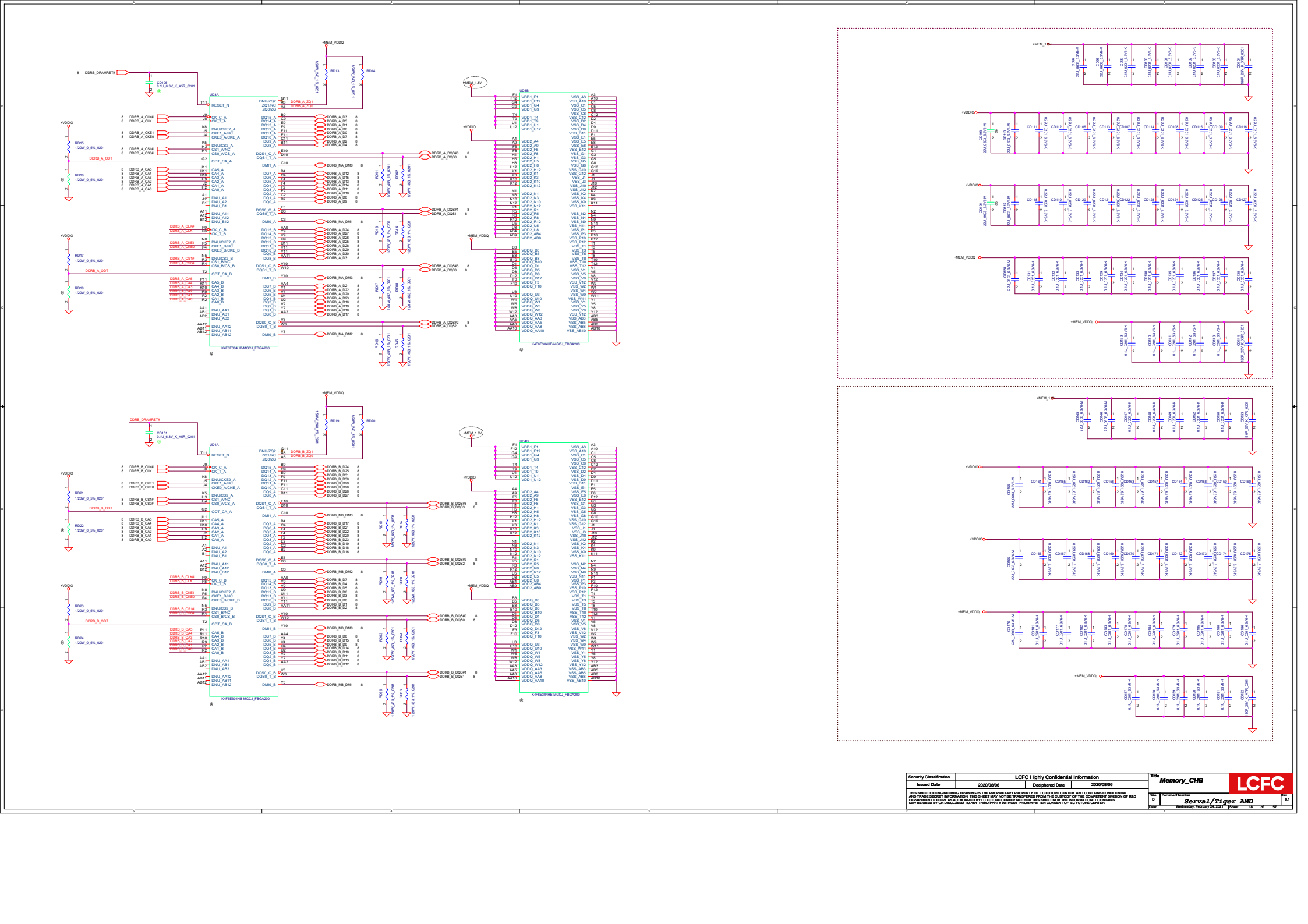






Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	Memory_CHA		LCFC
Size	Document Number		Rev
D	Serval/Tiger AMD		0.1
Date:	Wednesday, February 24, 2021	Sheet 17 of 57	



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

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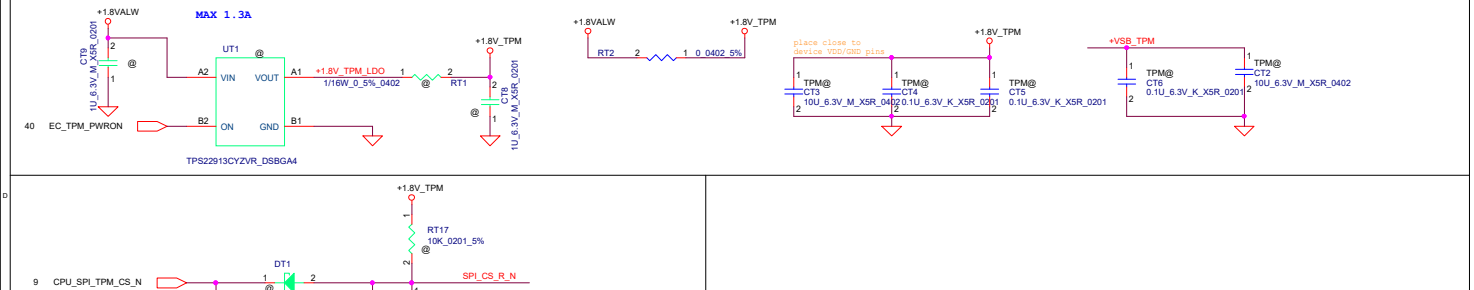
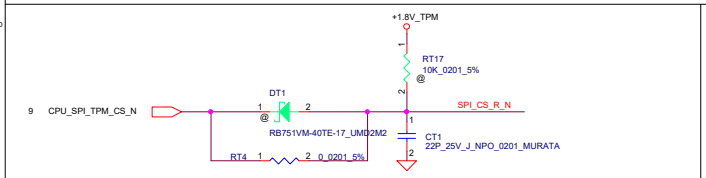
Title: Memory_CHB

LCFC

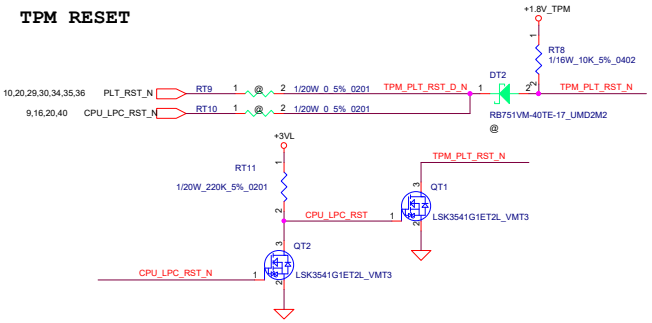
Size	Document Number	Rev
D	Serval/Tiger AMD	0.1

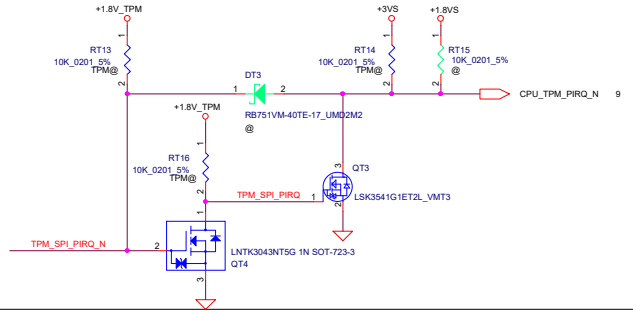
Date: Wednesday, February 24, 2021 Sheet 18 of 57





TPM RESET





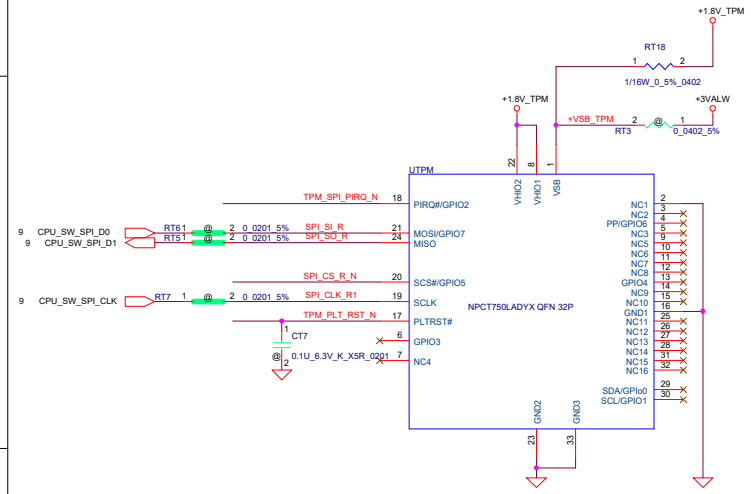
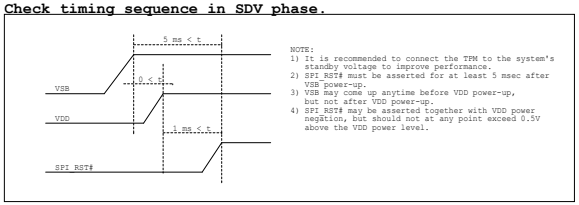


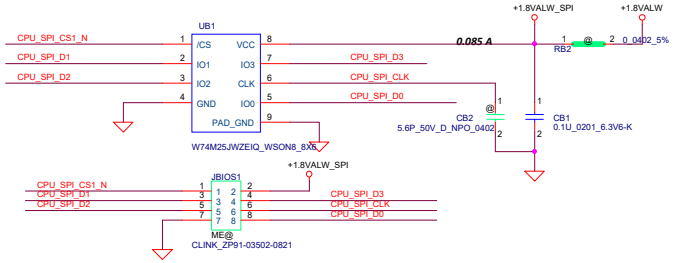
TABLE of TPM (U9801)		
Vendor	P/N	LCFC P/N
Nuvoton	NPCT750LABYX	SA00008KS20
ST Micro	ST33HTPH2E32AHC0	SA000089E20

NOTE:
Check timing sequence in SDV phase.



TABLE

Pin No	TCG PTP Spec (v38)	Nuvoton NPCT750LABYX	ST Micro ST33HTPH2E32AHC0
1	VDD	VSB	NC
2	GND	NC	GND
3	NC	NC	NC
4	GPIO	GPIO/PP	PP
5	NC	NC	NC
6	GPIO	GPIO3	NC
7	GPIO	NC	GPIO
8	VDD	VHIO	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	GPIO	GPIO4	NC
14	NC	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI/GPIO7	MOSI
22	VDD	VHIO	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO1	NC
30	SDA/GPIO0	SDA/GPIO0	NC
31	NC	NC	NC
32	NC	NC	NC



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: SPI ROM/TPM

LCFC

Size: Custom | Document Number: Serval/Tiger AMD | Rev: 0.1

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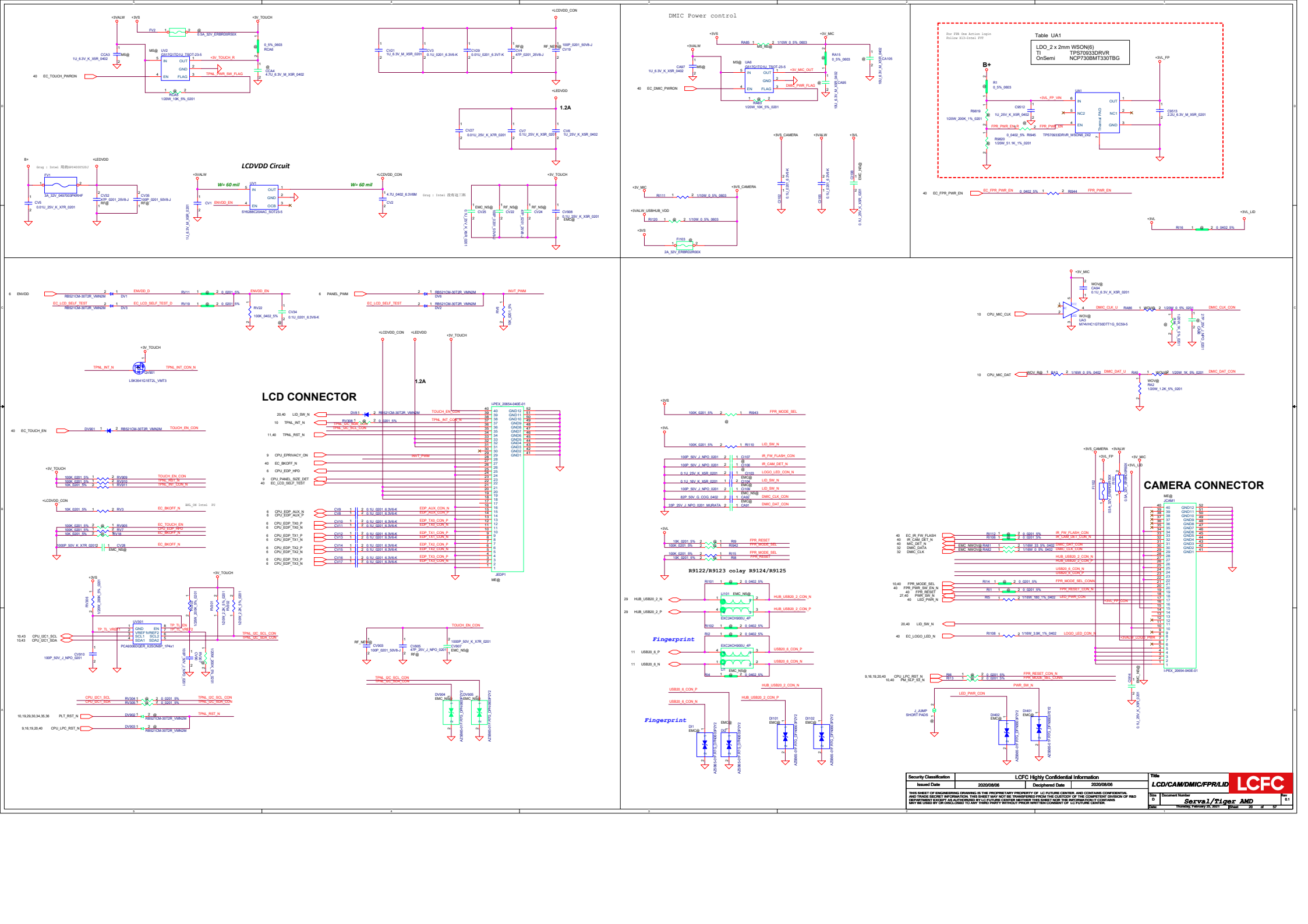

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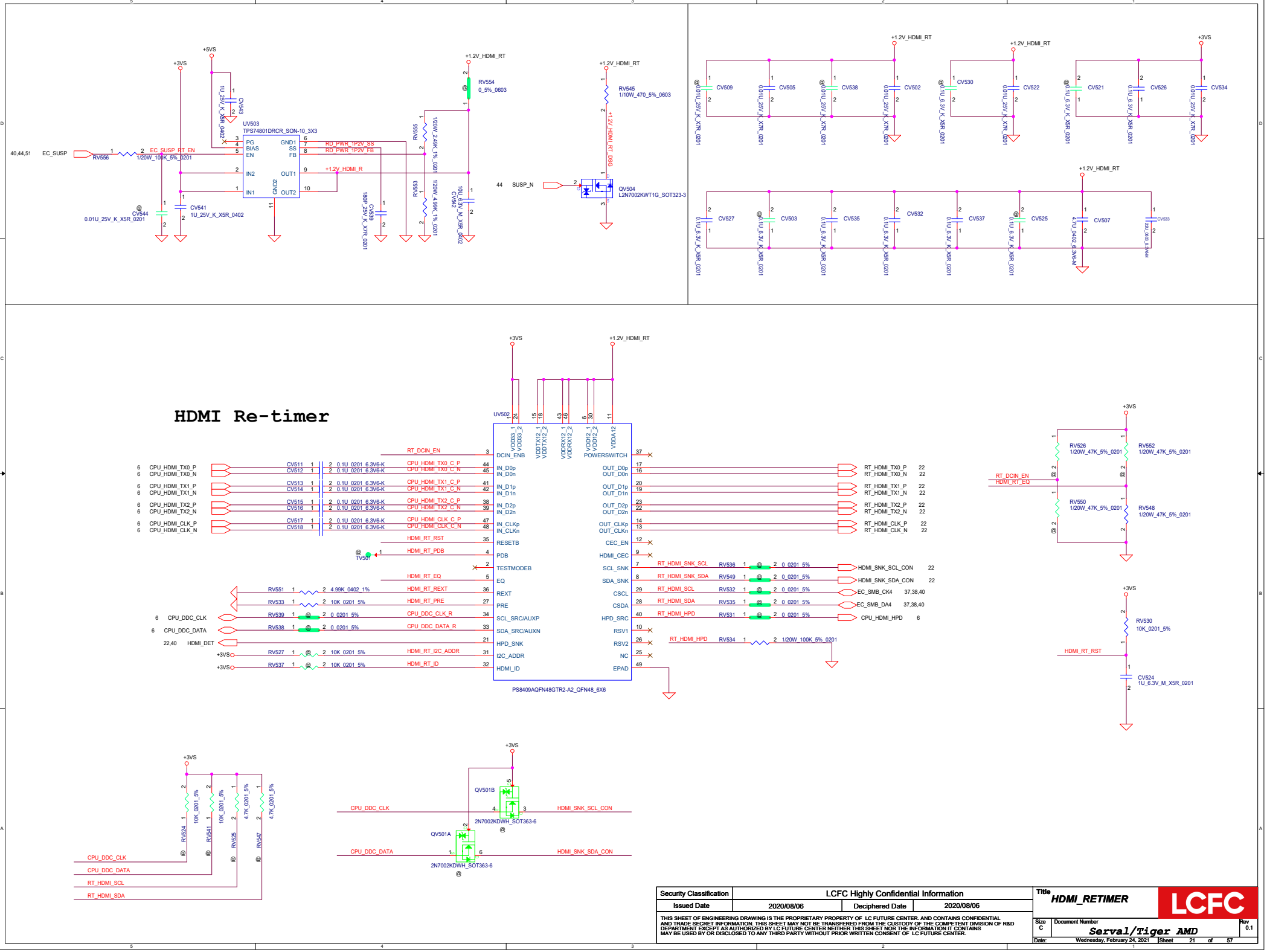
Title: LCD/CAM/DMIC/FPR/LID

LCFC

Size: D | Document Number: Serval/Tiger AMD | Rev: 0.1

Date: Thursday, February 04, 2021 | Sheet 20 of 57



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: HDMI_RETIMER

LCFC

Size	Document Number	Rev
C	Serval/Tiger AMD	0.1

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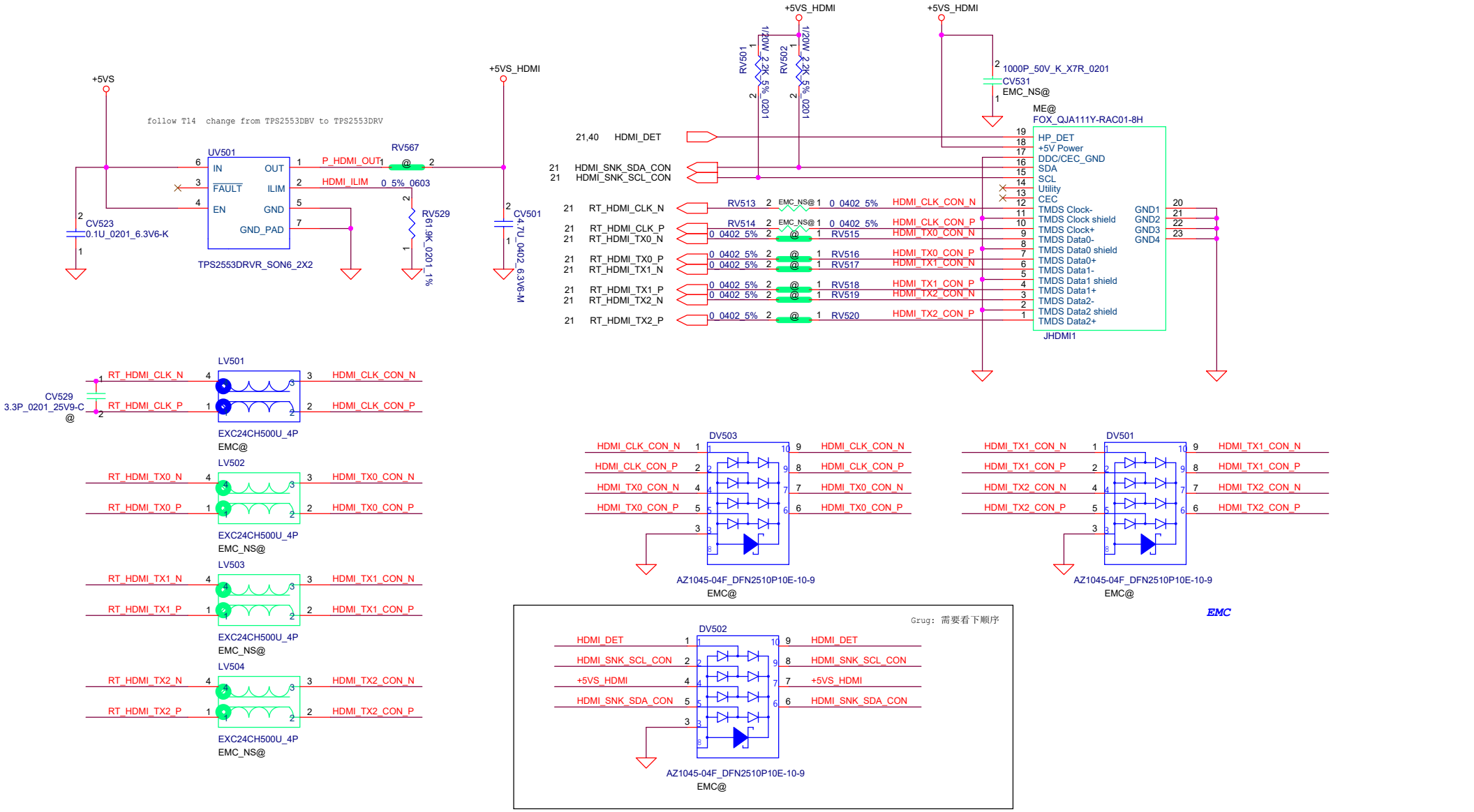


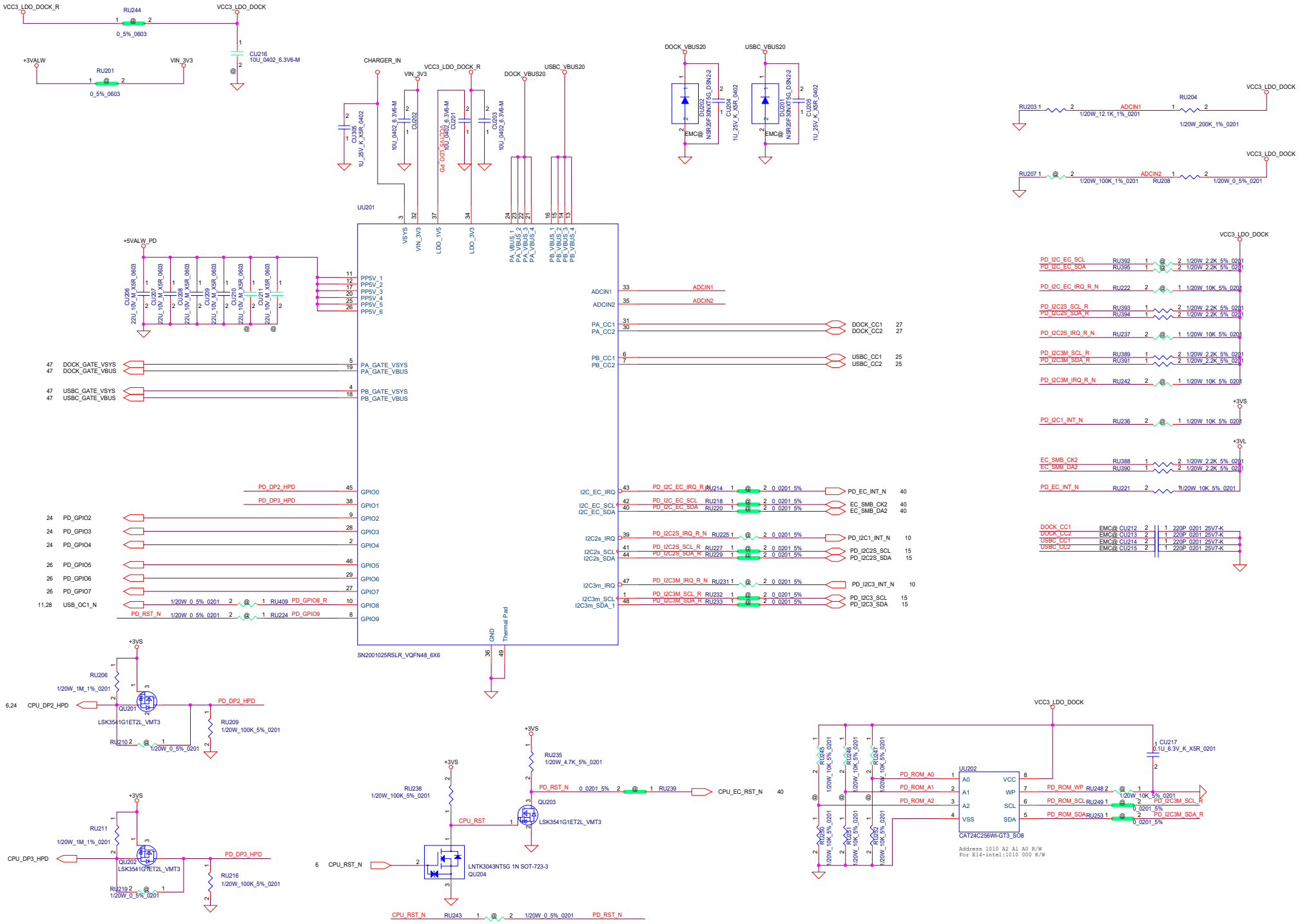
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: HDMI_CONN

LCFC

Size	Document Number	Rev
B	Serval/Tiger AMD	0.1

Date: Wednesday, February 24, 2021 Sheet 22 of 57



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	PD_Controller		
Size	Document Number		Rev
C	Serval/Tiger AMD		0.1
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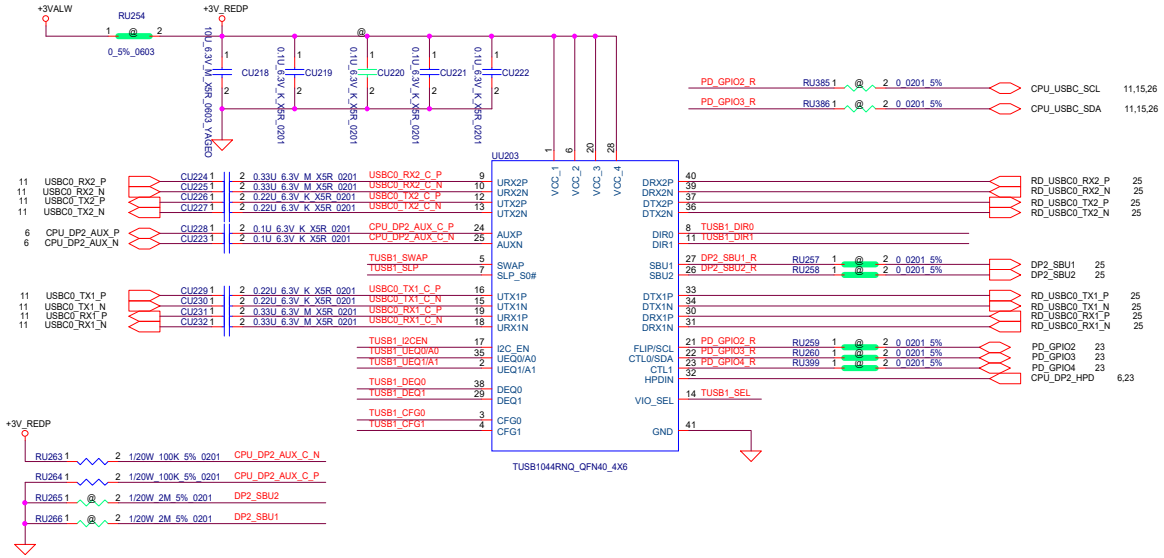
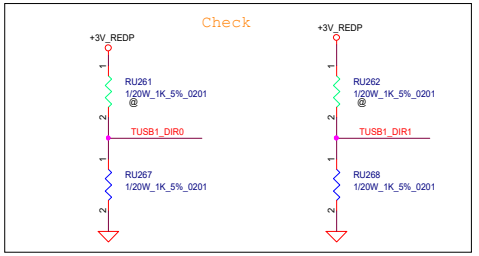
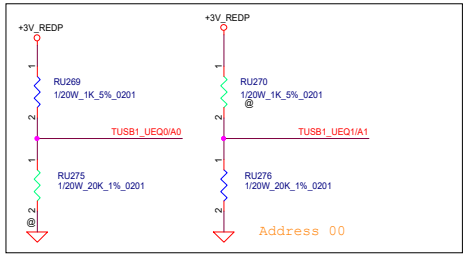
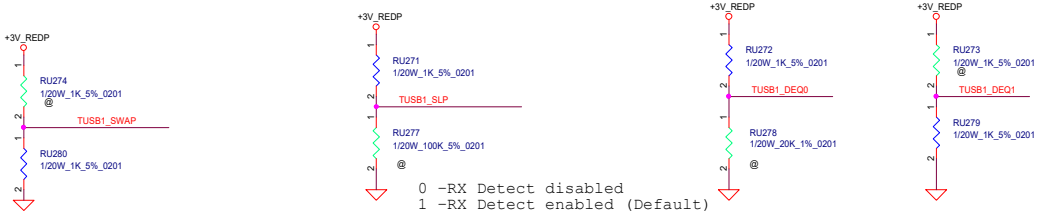






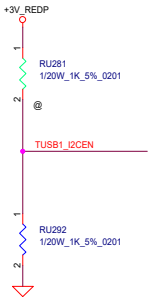
Will change to unstuff!!!

0 - Do not swap channel directions and EQ settings (Default)
1. - Swap channel directions and EQ settings

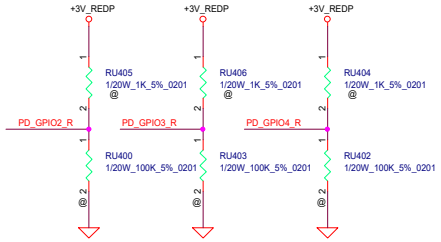


0 -RX Detect disabled
1 -RX Detect enabled (Default)

EQ setting



This PIN selects I/O valtage levels for the 2-level GPIO and I2C
0 = 3.3-V configuration I/O voltage, 3.3-V I2C interface (Default)
R = 3.3-V configuration I/O voltage, 1.8-V I2C interface
F = 1.8V configuration I/O voltage,3.3-V I2C interface
1 = 1.8-V configuration I/O voltage, 1.8-V I2C interface



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	TYPEC_REDRIVER1		
Size	C	Document Number	Serval/Tiger AMD
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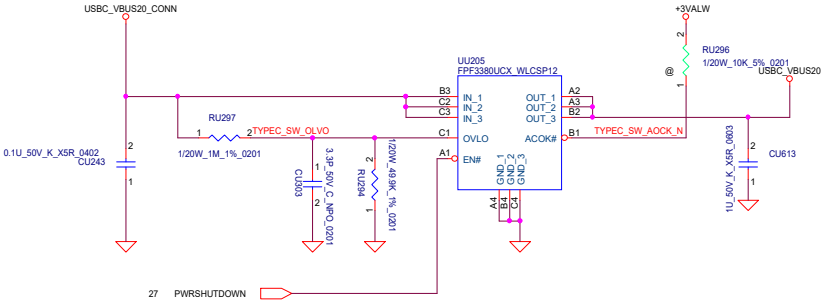
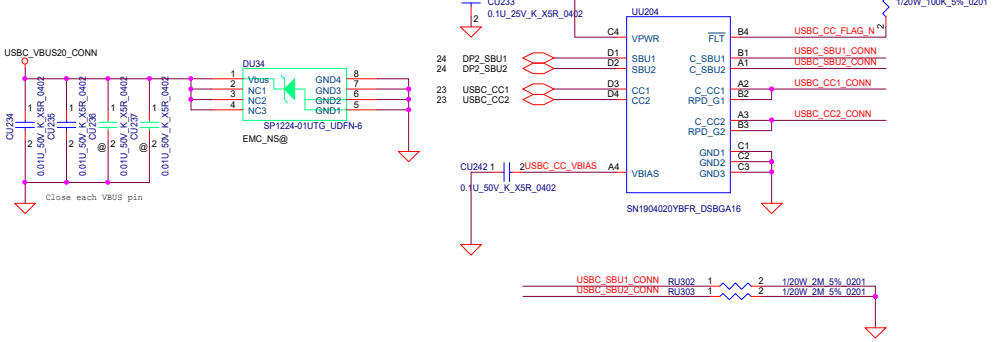
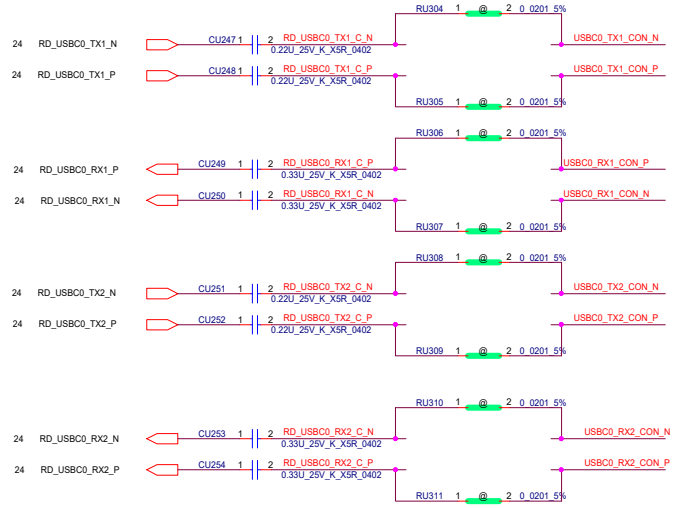
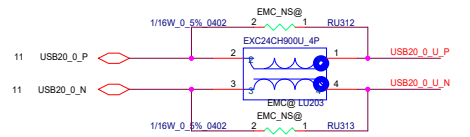
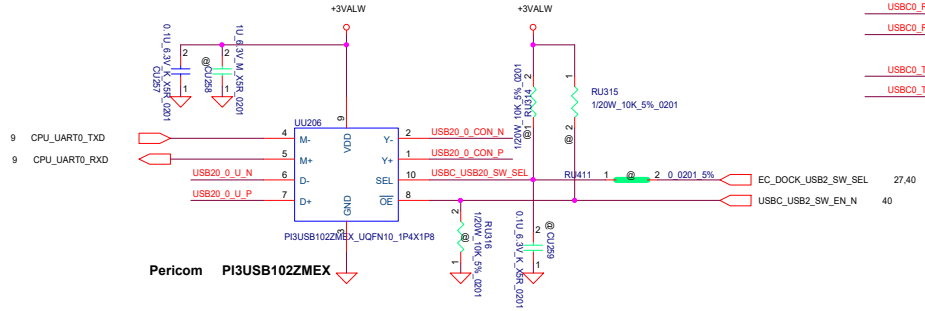
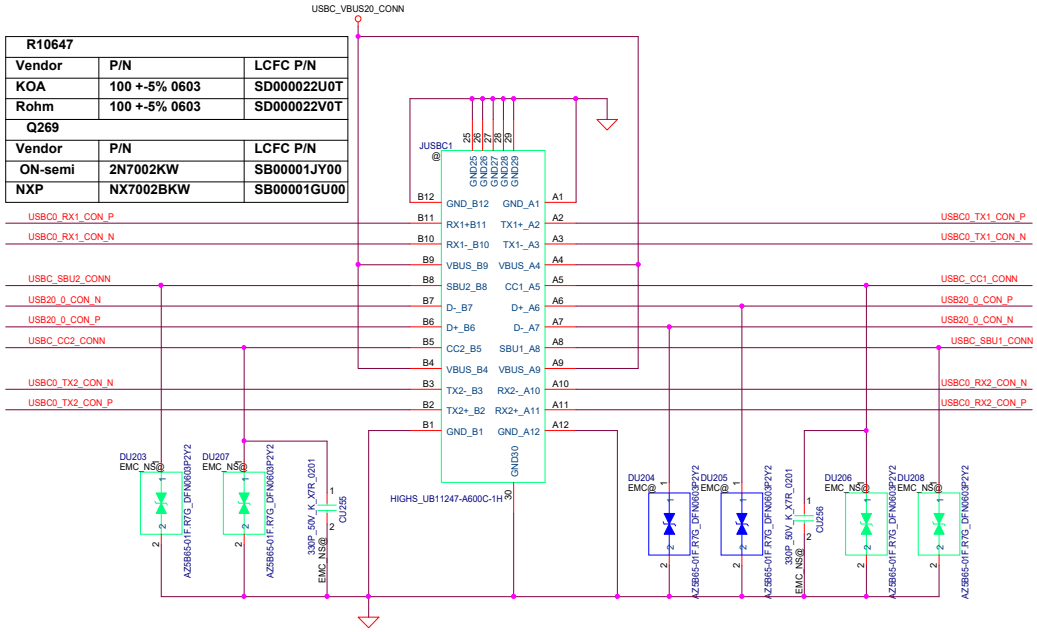




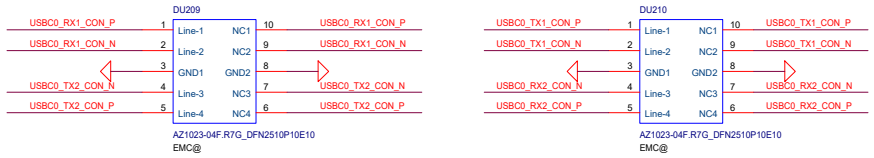








R10647		
Vendor	P/N	LCFC P/N
KOA	100 +-5% 0603	SD000022U0T
Rohm	100 +-5% 0603	SD000022V0T
Q269		
Vendor	P/N	LCFC P/N
ON-semi	2N7002KW	SB00001JY00
NXP	NX7002BKW	SB00001GU00



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: TYPEC_CONN

LCFC

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C	Serval/Tiger AMD	0.1

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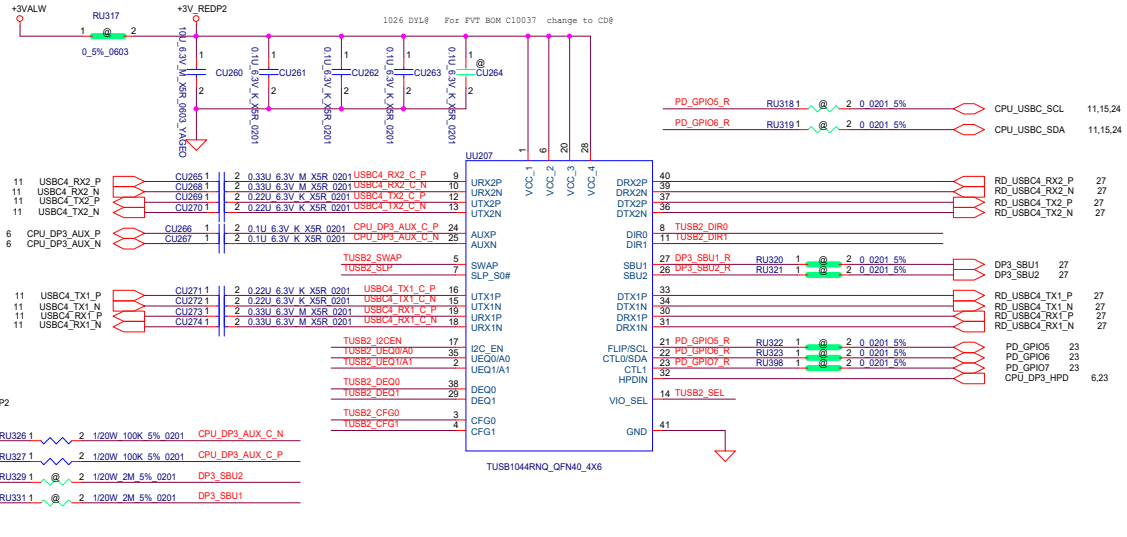
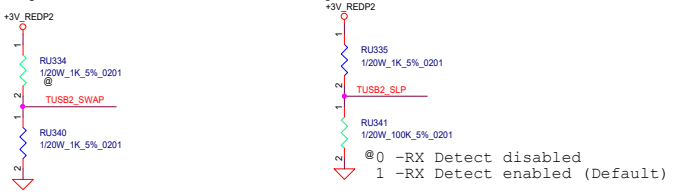
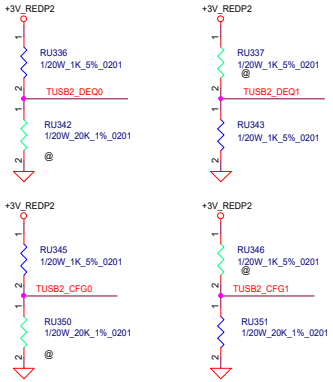
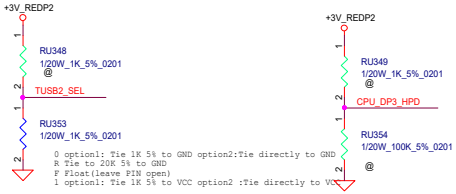


0 - Do not swap channel directions and EQ settings (Default)
1. - Swap channel directions and EQ settings

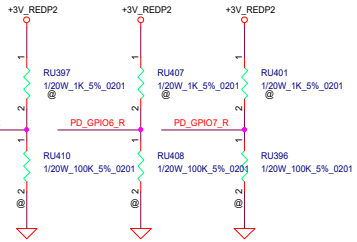


EQ setting

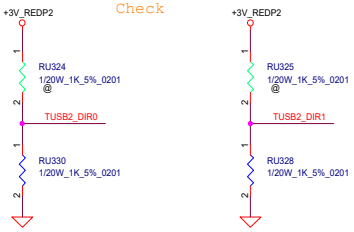


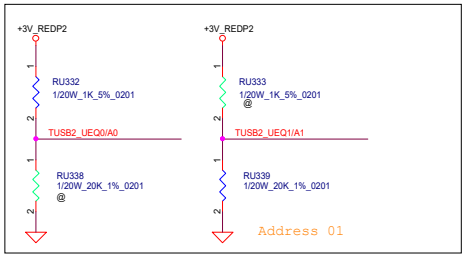


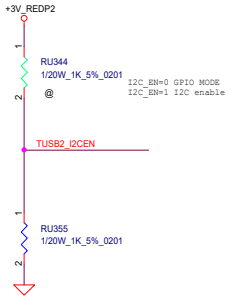
This PIN selects I/O valtage levels for the 2-level GPIO and I2C
0 = 3.3-V configuration I/O voltage, 3.3-V I2C interface (Default)
R = 3.3-V configuration I/O voltage, 1.8-V I2C interface
F = 1.8V configuration I/O voltage,3.3-V I2C interface
1 = 1.8-V configuration I/O voltage, 1.8-V I2C interface



Check

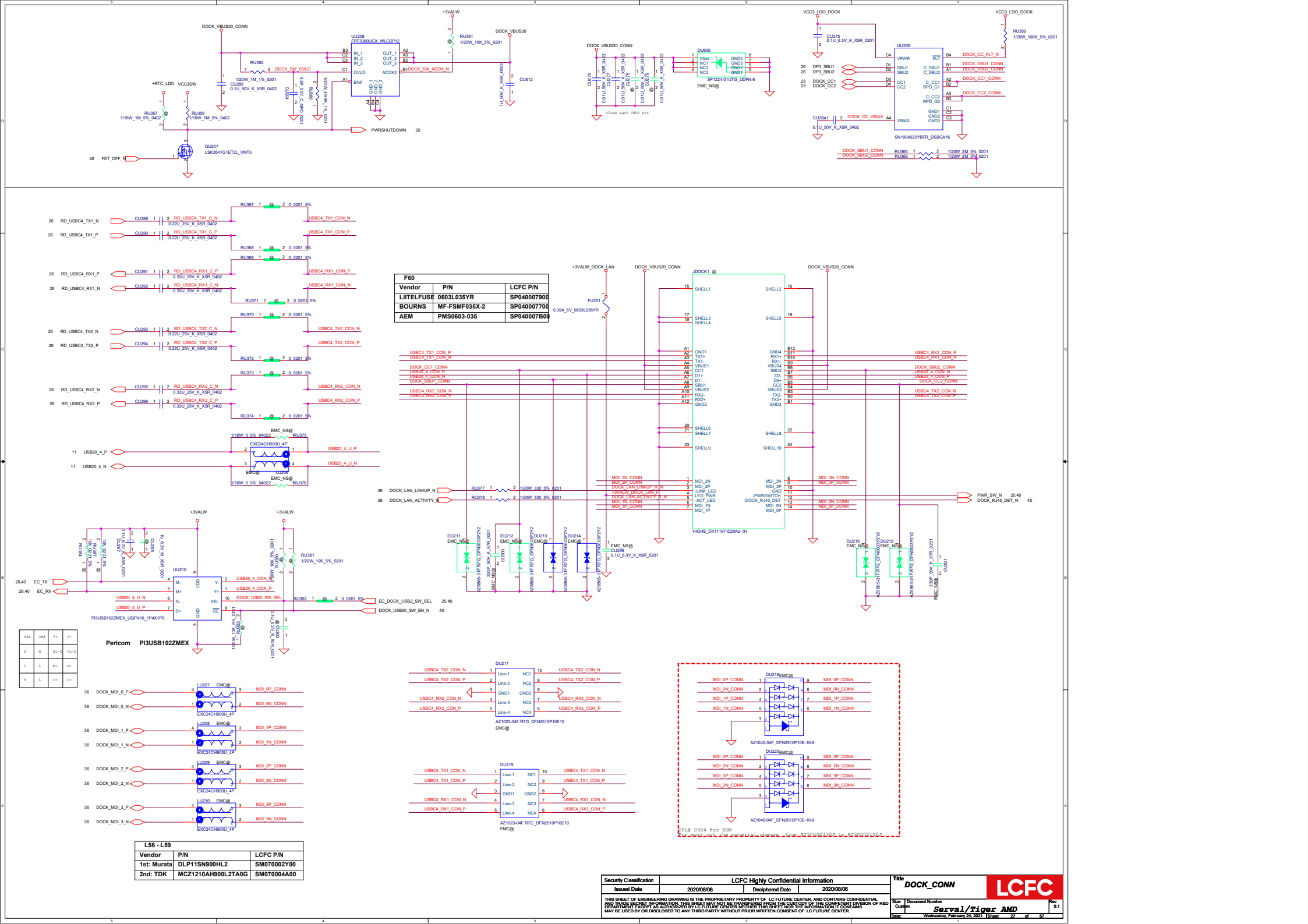






Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	TYPEC_REDRIVER2		
Size	Document Number		Rev
C	Serval/Tiger AMD		0.1
Date:	Wednesday, February 24, 2021	Sheet	26 of 57



F60		
Vendor	P/N	LCFC P/N
LIITELFUSE	0603L035YR	SP040007900
BOURNS	MF-FSMF035X-2	SP040007700
AEM	PMS0603-035	SP040007B00

L56 - L59		
Vendor	P/N	LCFC P/N
1st: Murata	DLP11SN900HL2	SM070002Y00
2nd: TDK	MCZ1210AH900L2T A0G	SM070004A00

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: DOCK_CONN

LCFC

Size: Custom | Document Number: Serval/Tiger AMD | Rev: 0.1

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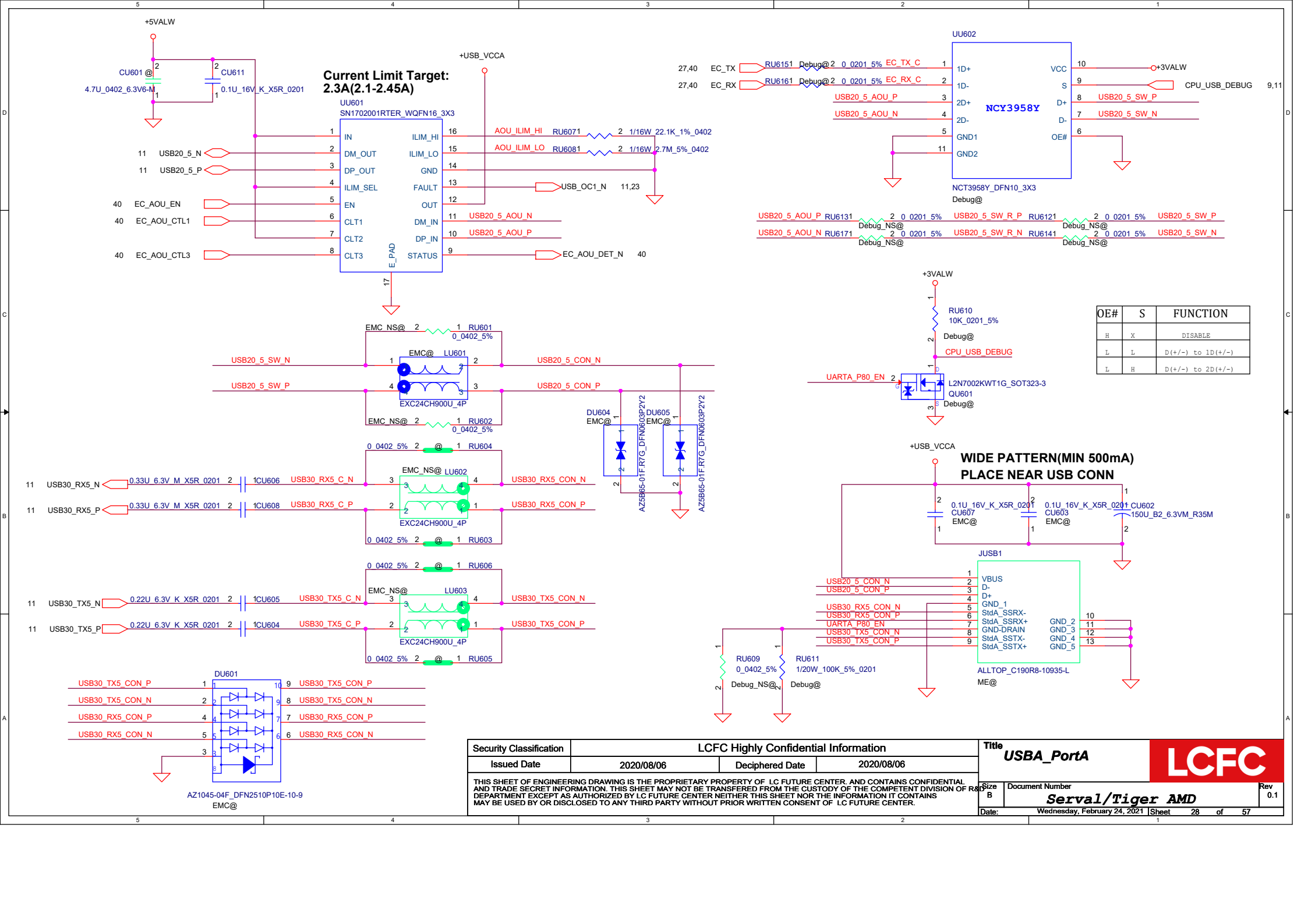

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: *USBA_PortA*

LCFC

Size	Document Number	Rev
B	*Serval/Tiger AMD*	0.1

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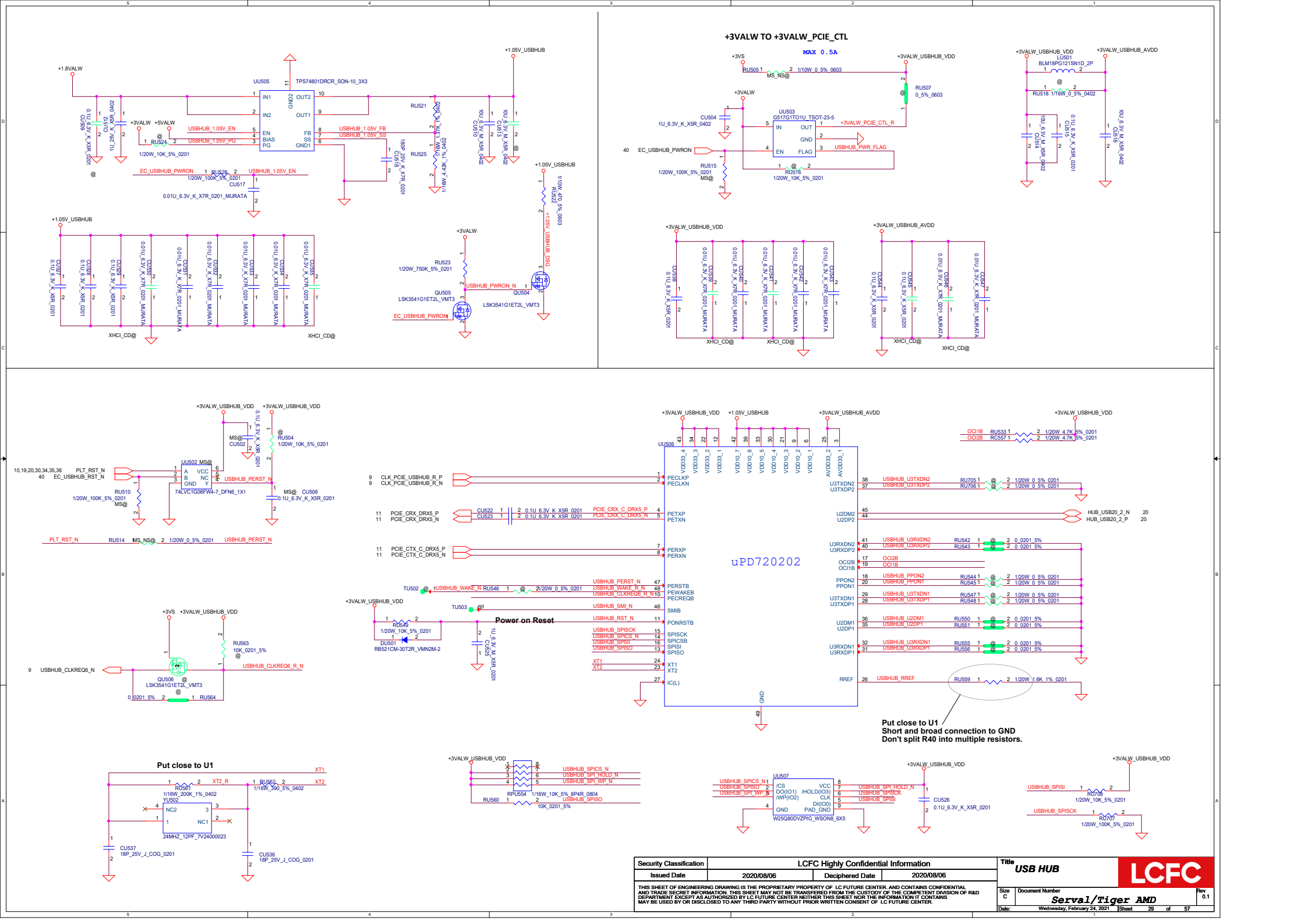
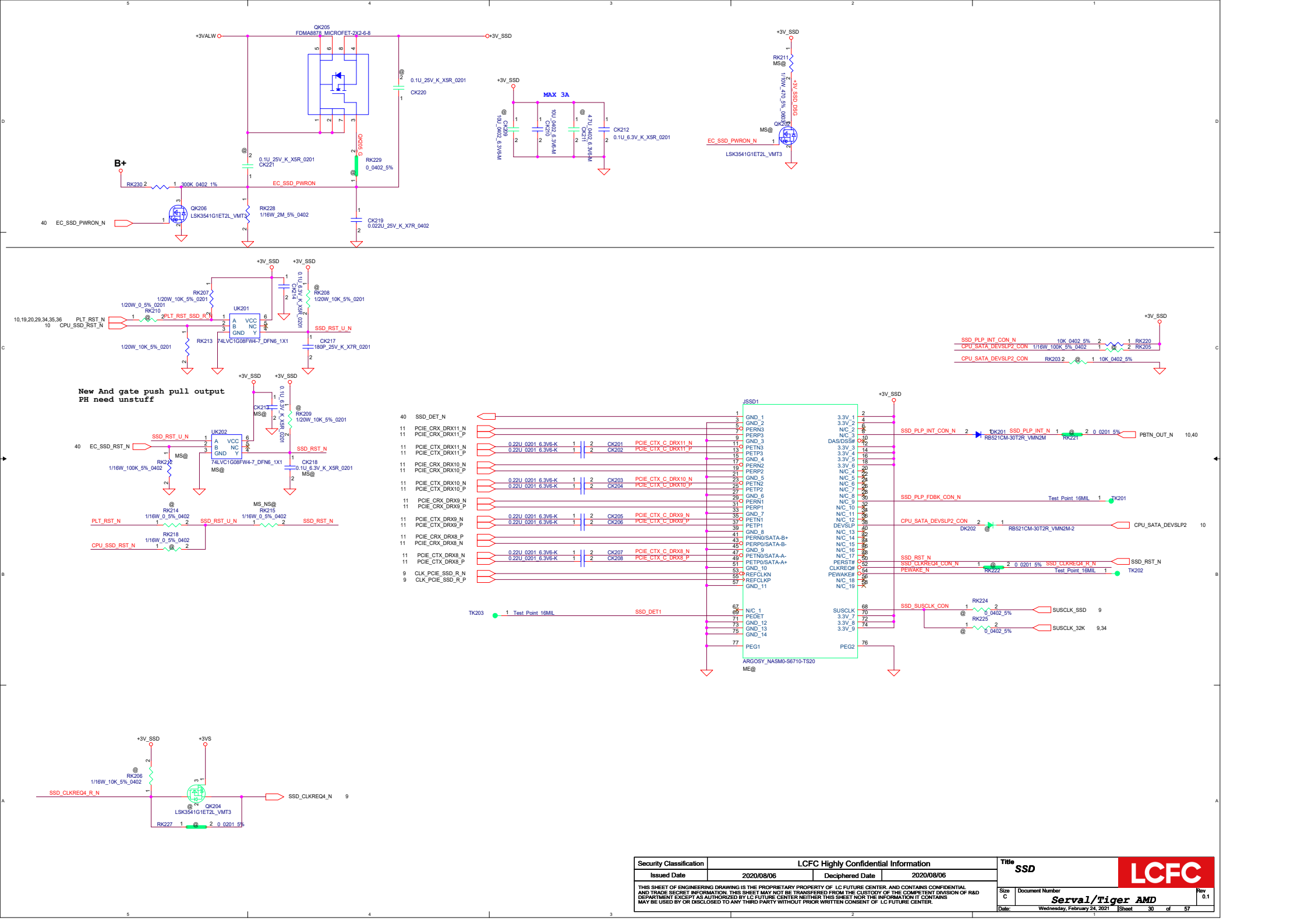

+3VALW TO +3VALW_PCIE_CTL
MAX 0.5A
uPD720202
Power on Reset
Put close to U1
Short and broad connection to GND
Don't split R40 into multiple resistors.
Put close to U1
LCFC Highly Confidential Information
USB HUB
Serval/Tiger AMD
Wednesday, February 24, 2021



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	SSD		
Size	C	Document Number	Serval/Tiger AMD
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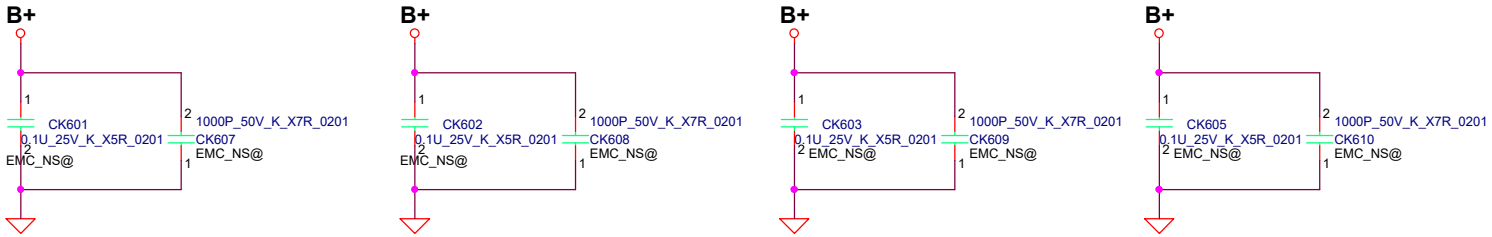

Title: ***EMI CAP***

LCFC

Size	Document Number	Rev
B	***Serval/Tiger AMD***	0.1

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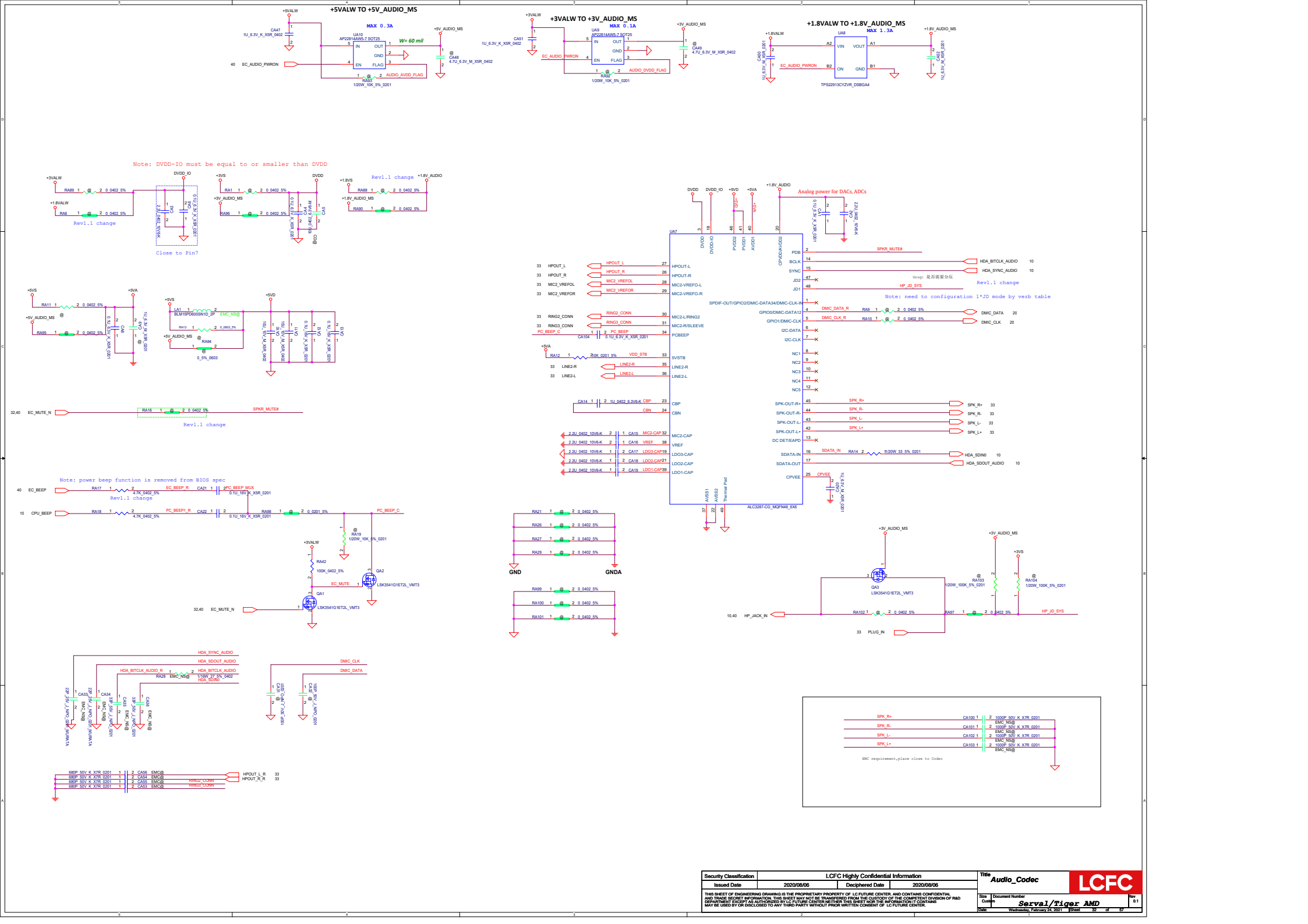

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	Audio_Codec		
Size	Document Number		Rev
Custom	Serval/Tiger AMD		0.1
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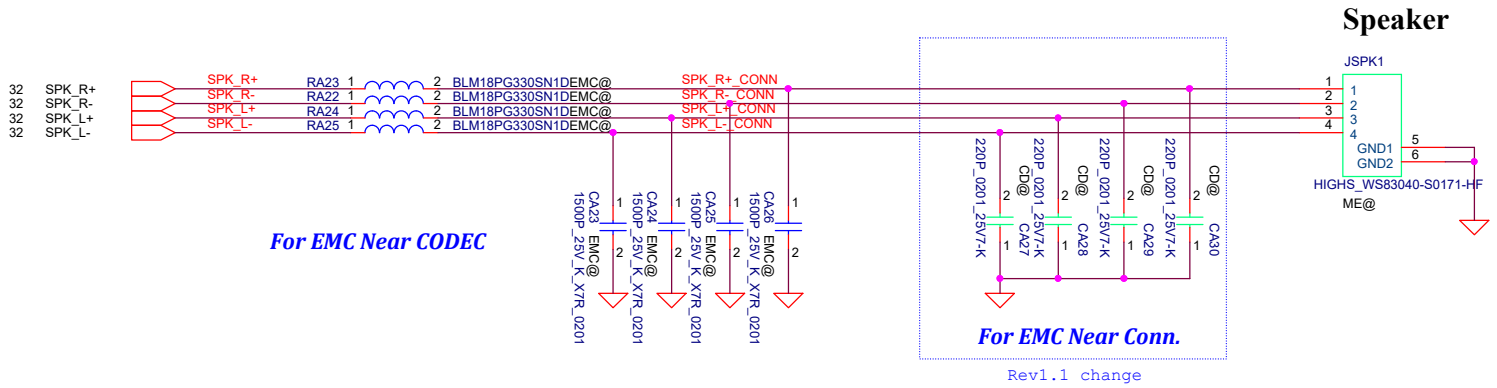
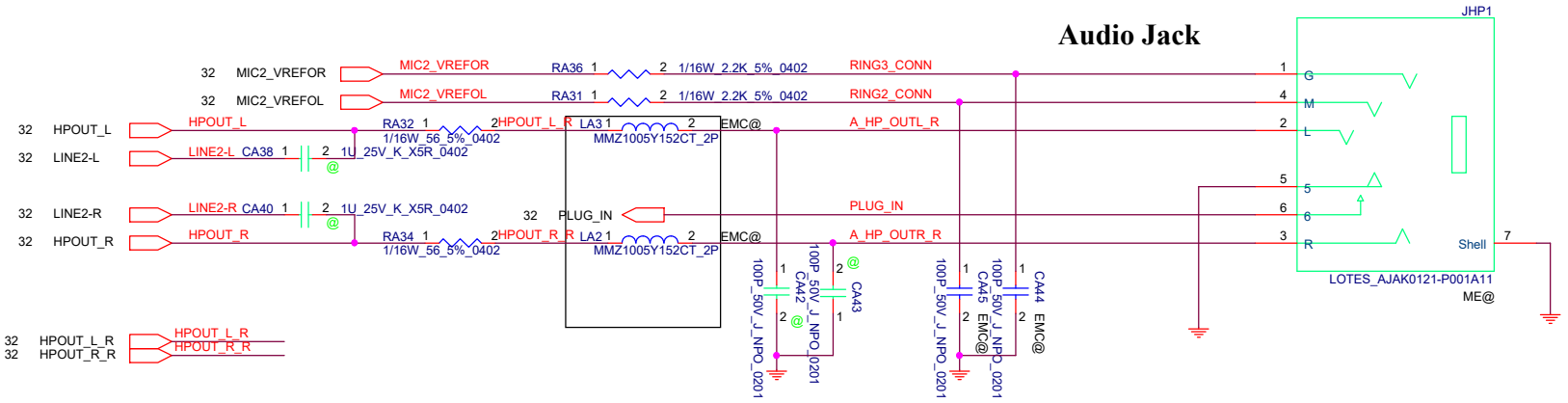
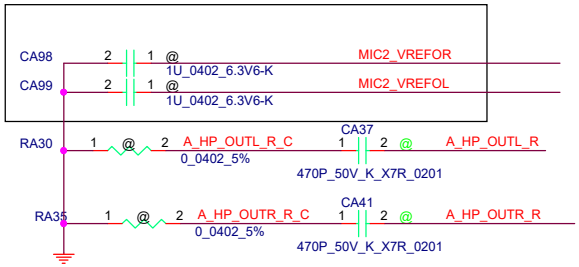
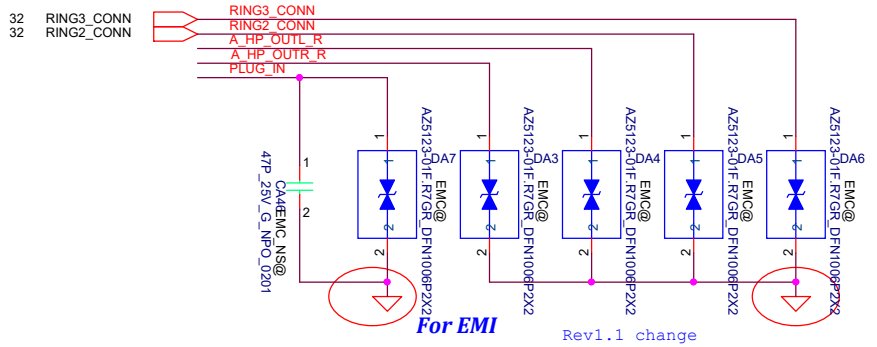
Speaker



Audio Jack

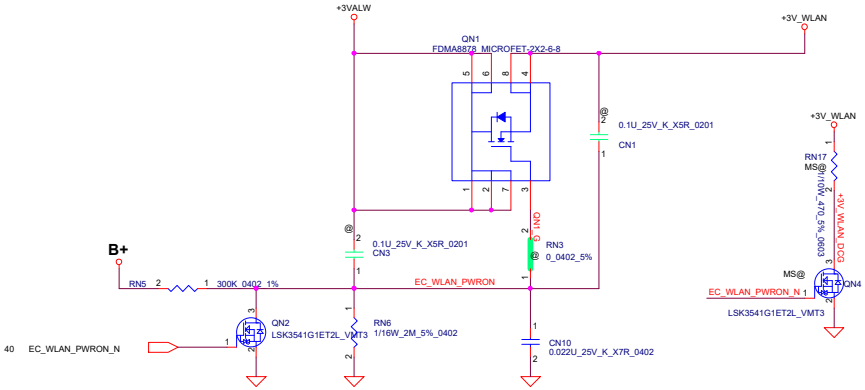


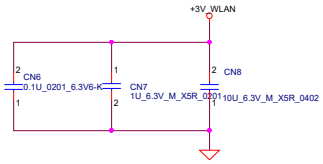


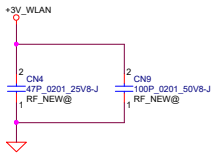


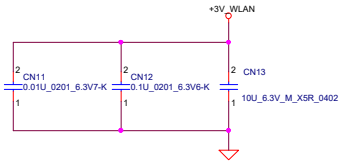
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	Audio_SPK/Jack		LCFC
Size B	Document Number	Serval/Tiger AMD	Rev 0.1
Date:	Wednesday, February 24, 2021	Sheet 33 of 57	

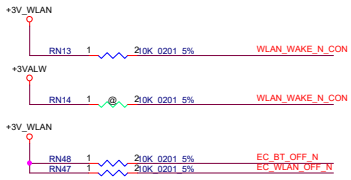


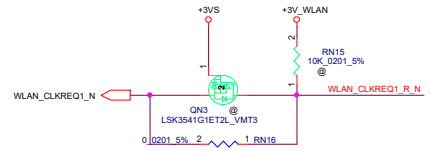


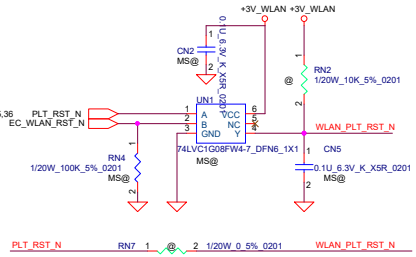


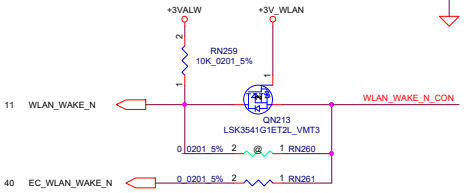


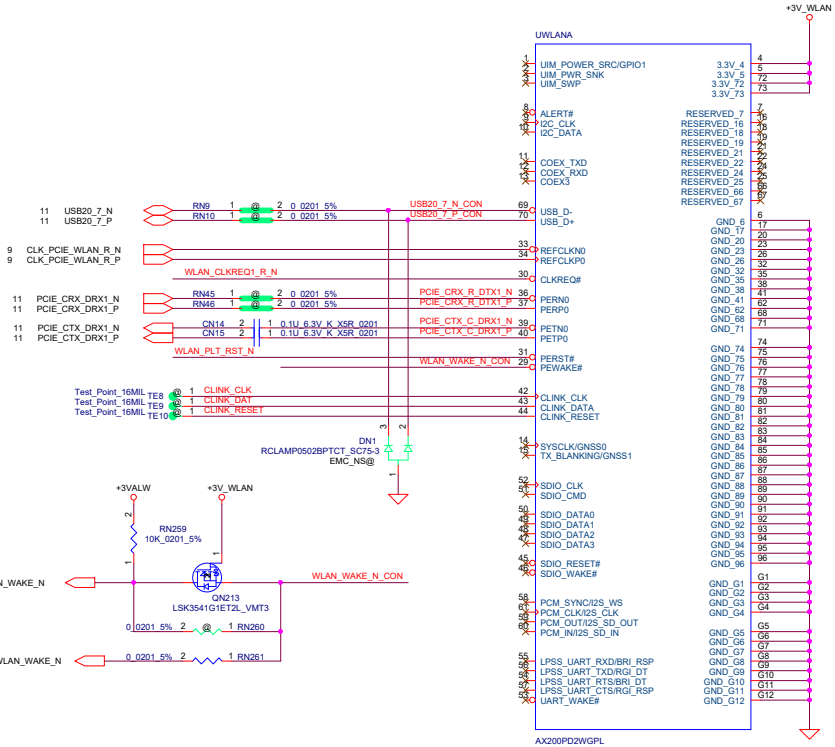
M.2 Type 1216 Module for WLAN / Bluetooth

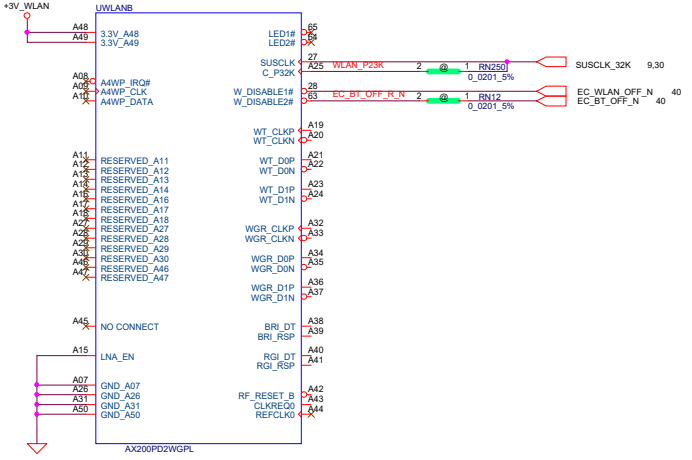












Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	WLAN		
Size	Document Number		Rev
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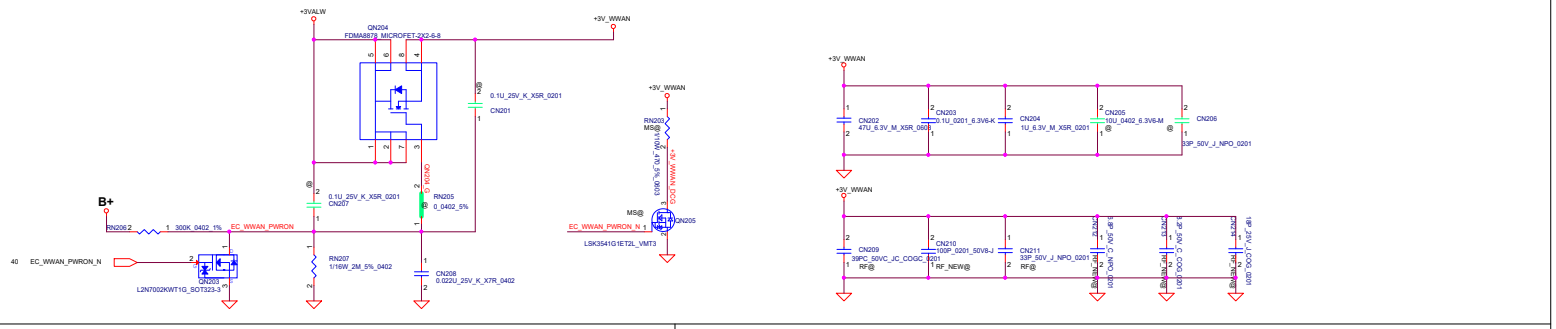

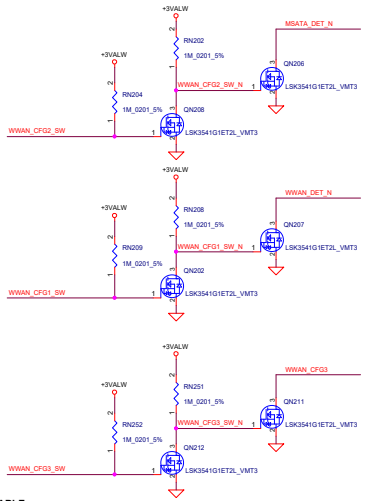

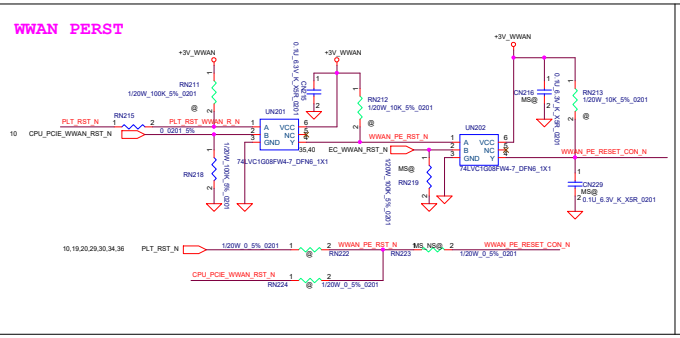

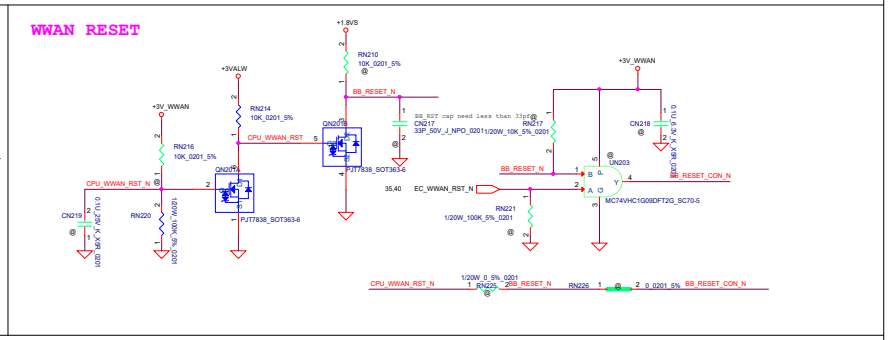

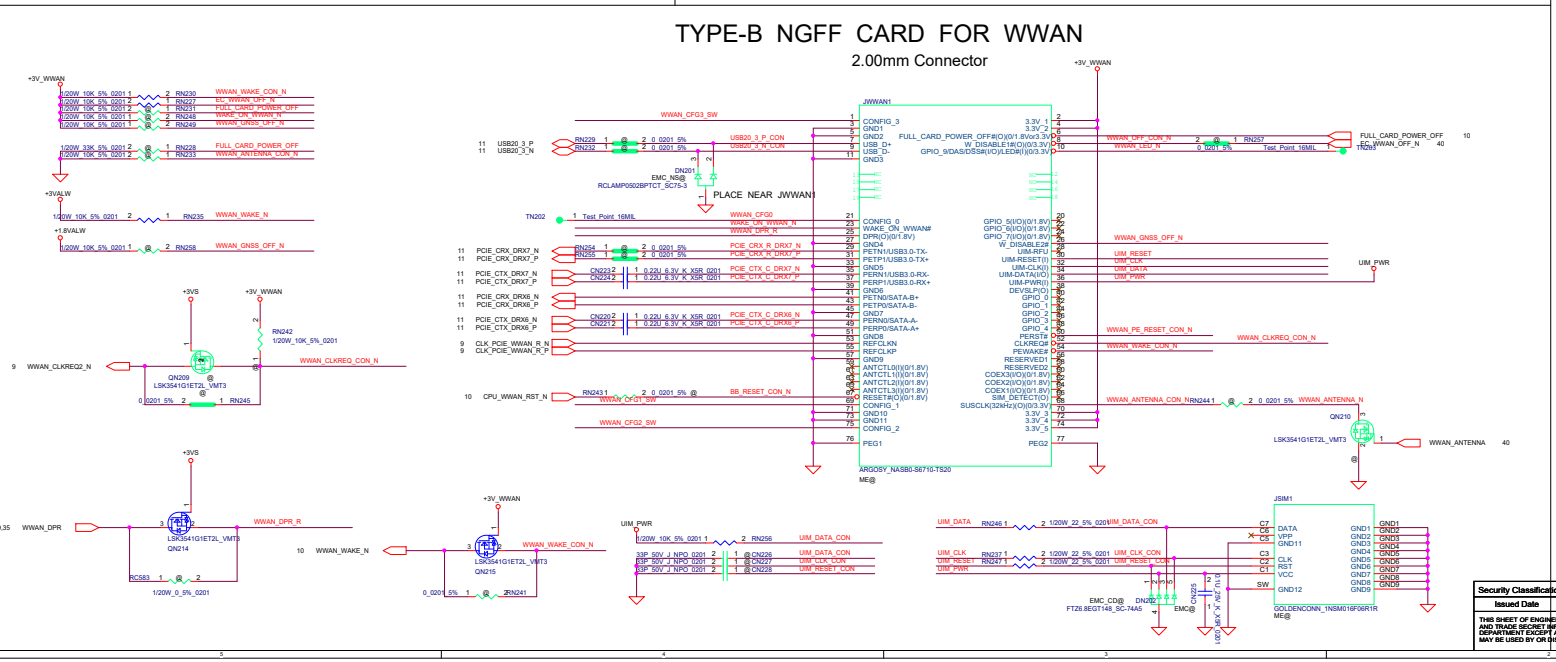

TABLE:

State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - USB 3.0	0
5	GND	NC	GND	NC	WWAN - USB 3.0	1
6	GND	NC	NC	GND	WWAN - USB 3.0	2
7	GND	NC	NC	NC	WWAN - USB 3.0	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	GND	RFU	N/A
15	NC	NC	NC	NC	No Module Present	N/A

TABLE:

	Module Configuration Decodes				
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)	
Fibcom L830-EB	GND	NC	GND	GND	
Sierra EM7565	GND	NC	NC	GND	
2242 PCIe SSD	GND	GND	GND	NC	Detect -WWAN_SSD_DTCT

Vcc	3.32V							
RN234	10K +/- 1%							
DEVICE_DETECT1#	1.533V	1.686V	1.782V	1.992V	2.215V	2.548V	2.776V	3.32V
WWAN_CFG3	V	V	V	V	X	X	X	X
WWAN_CFG2	V	V	X	X	V	V	X	X
WWAN_CFG1	V	X	V	X	V	X	V	X
Configuration	EM05	SSD			Foxconn SG		EM120	NA

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Title	Size	Document Number	Rev
WWAN	Custom	Serval/Tiger AMD	0.1
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+3VALW_LAN_TOTAL
RL31
+3VALW_DOCK_LAN
0_5%_0603
+LAN_VDD
RL2 1/10W_0_5%_0603
+LAN_SROUT1.05
W=60mils
LL1 2.2UH_LQM2HPN2R2MG0L_20%
These components close to UL1 : Pin 36
(Should be place within 200 mils)
CL6 0.1U_6.3V_K_X5R_0201
CL1 W=60mils
CL4 4.7U_6.3V_M_X5R_0402
+3VALW_DOCK_LAN
RL3
+LAN_VDDREG
0_5%_0603
CL2 4.7U_0402_6.3V6M
CL3 1U_6.3V_K_X5R_0201

+3VALW_LAN Rising time (10%~90%) >0.5mS and <100mS.

+3VALW_DOCK_LAN
CL9 CL10 CL11 CL12 CL13 1U_6.3V_K_X5R_0201
NDASH@ CL21 1U_6.3V_K_X5R_0201
Close to UL1 Pin 12, 42, 47, 48, 39 & 27.
+LAN_VDD
CL14 CL15 CL22 CL16 CL17 CL18 CL19 1U_6.3V_K_X5R_0201
NDASH@
Close to UL1 Pin 3, 6, 9, 45, 13, 41.
Close to UL1 Pin 29.
CL20 1U_6.3V_K_X5R_0201
CL23 1U_0402_6.3V6K
Close to UL1 Pin 21.

+3VALW_DOCK_LAN
MS@ CL26 0.1U_6.3V_K_X5R_0201
+3VALW_DOCK_LAN
RL32 1/20W_10K_5%_0201
UL3 74LVC1G08FW4-7_DFN6_1X1
10,19,20,29,30,34,35 PLT_RST_N
40 EC_DOCK_LAN_RST_N
DOCK_LAN_RST_N
RL33 1/20W_100K_5%_0201 MS@
CL27 MS@ 0.1U_6.3V_K_X5R_0201
PLT_RST_N RL34 MS_NS@2 1/20W_0_5%_0201 DOCK_LAN_RST_N

+3VALW
+3VALW_DOCK_LAN
RL1 10K_0201_5%
10 DOCK_LAN_SMI_N
SMB_ALERT
QL1 LSK3541G1ET2L_VMT3

+3VS
+3VALW_DOCK_LAN
RL35 10K_0201_5%
9 LAN_CLKREQ3_N
LAN_CLKREQ_R_N
QL2 LSK3541G1ET2L_VMT3
0_0201_5% RL15

+3VALW_DOCK_LAN
RL36 DASH@ 20K_0201_5% DASH_SPI_WP_N
RL37 DASH@ 20K_0201_5% DASH_SPI_CST_N
RL38 DASH@ 20K_0201_5% DASH_SPI_HOLD_N
RL7 20K_0201_5% DOCK_LAN_WAKE_R_N
RL8 @ 20K_0201_5% DOCK_LAN_ACTIVITY_N
RL9 @ 20K_0201_5% JTDI
RL12 @ 20K_0201_5% DOCK_LAN_LINKUP_N
RL14 @ 20K_0201_5% SMB_ALERT
RL16 @ 20K_0201_5% EC_DASHLAN_CAB_DET_N
+3VS
RL20 2/20W_1K_5%_0201 DOCKLAN_ISOLATE_N
RL24 1/20W_15K_5%_0201 DOCKLAN_ISOLATE_N
RL30 @ 20K_0201_5% JTDO

Close to UL4 Pin 22, 23

11 PCIE_CRX_DRX0_P
11 PCIE_CRX_DRX0_N
CL7 CL5 0.1U_0201_16V6-K
PCIE_CRX_C_DRX0_P
PCIE_CRX_C_DRX0_N
11 PCIE_CTX_C_DRX0_P
11 PCIE_CTX_C_DRX0_N
LAN_CLKREQ_R_N
DOCK_LAN_RST_N
9 CLK_PCIE_DOCKLAN_R_P
9 CLK_PCIE_DOCKLAN_R_N
XTLI
XTLO
40 DOCK_LAN_WAKE_N
RL10 @ 0_0201_5% DOCK_LAN_WAKE_R_N
DOCKLAN_ISOLATE_N
10,40 CPU_SMB_SCL1
10,40 CPU_SMB_SDA1
10,40 EC_WAKE_N
JTDO
RL19 @ 1/20W_0_5%_0201 SMB_ALERT
+3VALW_DOCK_LAN
+LAN_VDDREG
TL2 @ DOCK_LAN_NC_TP
RL221 2/20W_2.49K_1%_0201 DOCK_LAN_RSET
DASH_SPI_CS1_N
RL23 @ 0_0201_5% SPICSB
RL25 1/20W_0_5%_0201 NDASH@

UL1 RTL8111EPV-CG_QFN48_6X6
HSOP HSON HSIP HSIN CLKREQB PERSTB REFCLK_P REFCLK_N XTAL1 XTAL2 LANWAKEB ISOLATEB SMBCLK SMBDATA GPIO0/JTDO GPIO1/SMBALERT/JCLK VDDREG_1 VDDREG_2 NC RSET SPICSB GND

RL29 for DSAH debug.

JTDO RL27 2/1/20W_33_5%_0201 JTDO_R TL3 Test_Point_12MIL
JTDO RL29 @ 2/1/20W_0_5%_0201 EC_DASHLAN_CAB_DET_N 40
DOCK_LAN_LINKUP_N RL4 2/0_0201_5% EC_DASHLAN_CAB_DET_N
SPISI RL13 NDASH@ 2/0_0201_5% +LAN_VDD
SPISK RL18 NDASH@ 2/0_0201_5% +3VALW_DOCK_LAN

LED0/JTRSTN 40
LED1/JTDI 37 JTDI Test_Point_12MIL TL1 DOCK_LAN_ACTIVITY_N 27
LED2/JTMS 31 DOCK_LAN_LINKUP_N 27
SPISO 30 SPISO RL5 @ 2/0_0201_5% DASH_SPI_DI
MDIP0 1 MDIN0 2 DOCK_MDI_0_P 27 DOCK_MDI_0_N 27
MDIP1 4 MDIN1 5 DOCK_MDI_1_P 27 DOCK_MDI_1_N 27
MDIP2 7 MDIN2 8 DOCK_MDI_2_P 27 DOCK_MDI_2_N 27
MDIP3 10 MDIN3 11 DOCK_MDI_3_P 27 DOCK_MDI_3_N 27
SPISI 29 SPISI RL11 @ 2/0_0201_5% DASH_SPI_DO
DVDD10_1 13 DVDD10_2 41 +LAN_VDD
SPISK 27 SPISK RL17 @ 2/0_0201_5% DASH_SPI_CLK
DVDD33 39 +3VALW_DOCK_LAN
AVDD33_1 12 AVDD33_2 42 AVDD33_3 47 AVDD33_4 48
EVDD10 21 +LAN_VDD
AVDD10_1 3 AVDD10_2 6 AVDD10_3 9 AVDD10_4 45
REGOUT 36 +LAN_SROUT1.05

change to SA00008DU00 2M ROM

+3VALW_DOCK_LAN
DASH_SPI_CS1_N 1
DASH_SPI_DI 2
DASH_SPI_WP_N 3
4
UL2 W25Q16JVZPIQ_WSON8_6X5
/CS VCC 8
DO(IO1) IO3 7 DASH_SPI_HOLD_N
IO2 CLK 6 DASH_SPI_CLK
GND DI(IO0) 5 DASH_SPI_DO
NC 9
CL8 0.1U_16V_K_X5R_0201 DASH@

XTLI RL26 @ 2/1/16W_0_5%_0402 XTLO
0_0201_5% RL28
YL1 25MHZ_10PF_7V25000014
OSC1 GND2 OSC2 GND1
CL24 10P_25V_J_NPO_0201
CL25 10P_25V_J_NPO_0201

Title	LAN_Chipset	LCFC
Size C	Document Number Serval/Tiger AMD	Rev 0.1
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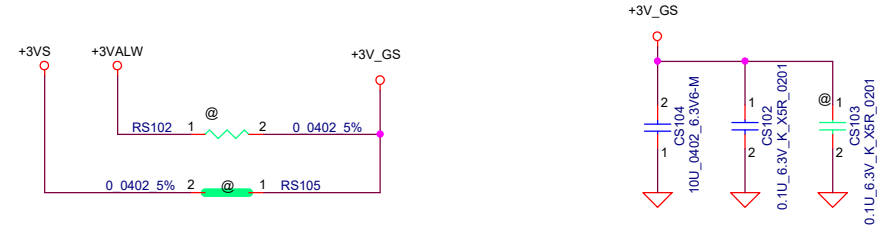
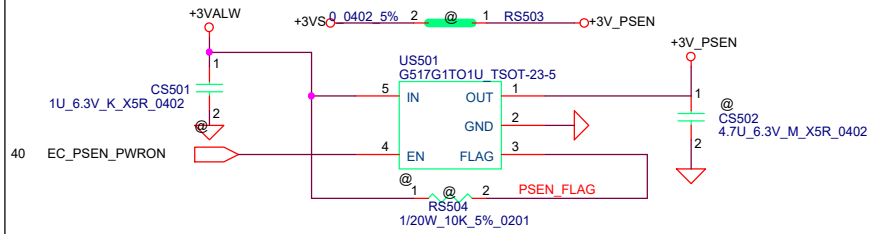
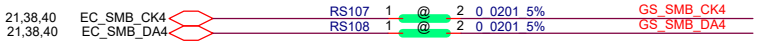
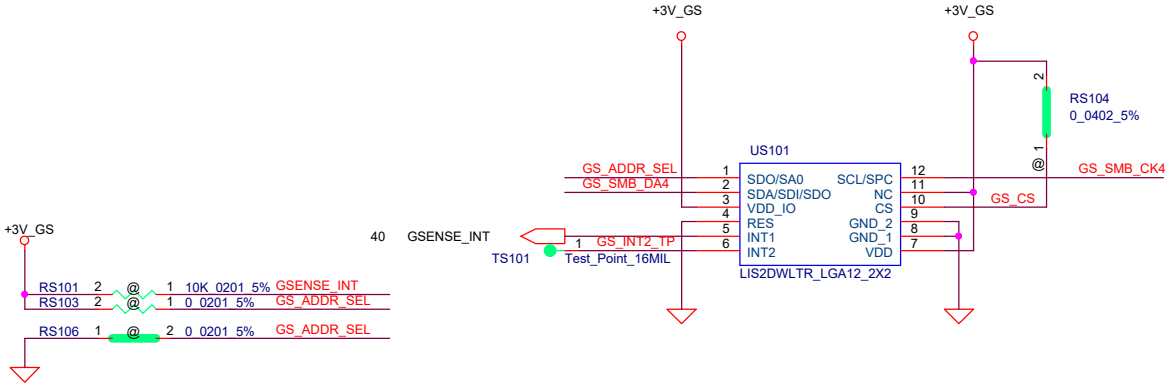




G sensor



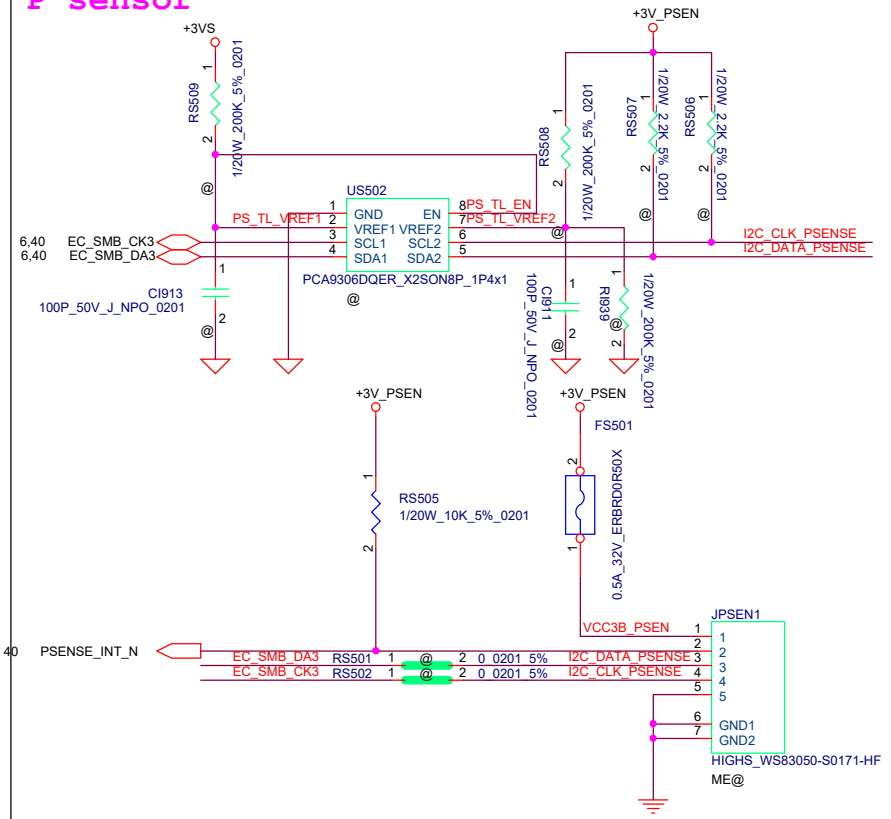


TABLE

P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
BMA280	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

TABLE of G-Sensor (U148)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
BOSCH	BMA280	SA0000A1600

P sensor



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: Sensor

LCFC

Size	Document Number	Rev
B	Serval/Tiger AMD	0.1

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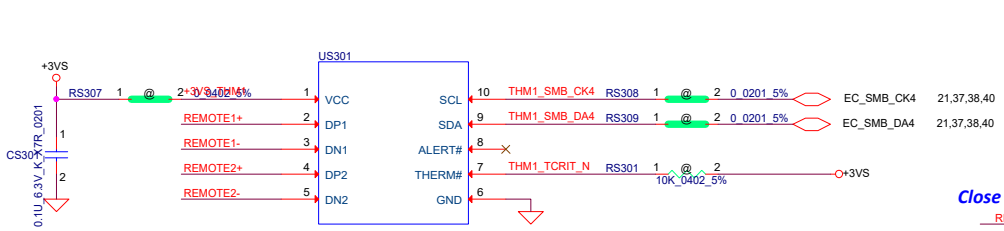
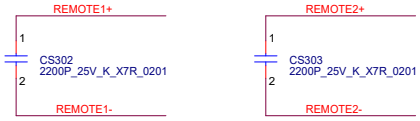


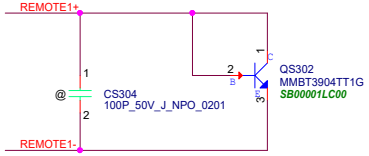
Address 1001_101xb

Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

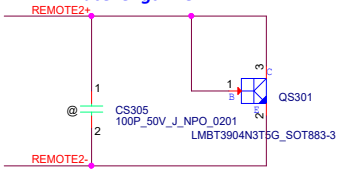
Close to UTH1

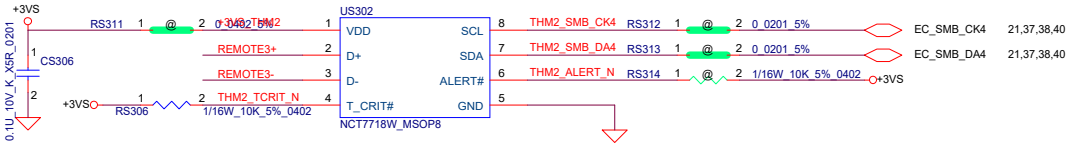


Close to FIN



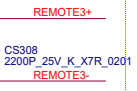
REMOTE2+/-:
Close CPU Trace width/space:10/10 mil
Trace length:<8"



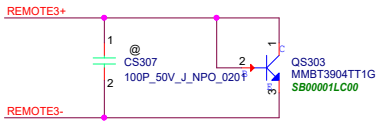


NCT7718W I2
C/ SMBusTM address is 1001100xb (x is R/W bit).

Close to UTH2



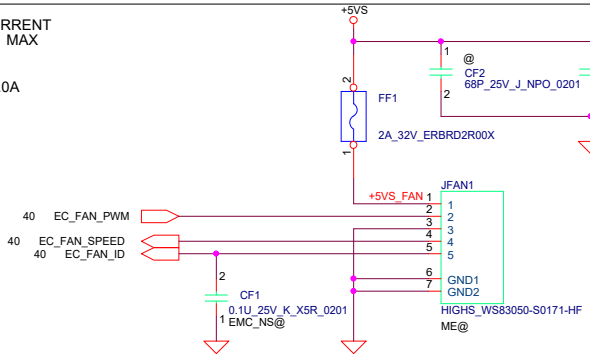
Near



REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN CURRENT
IS 0.5A MAX

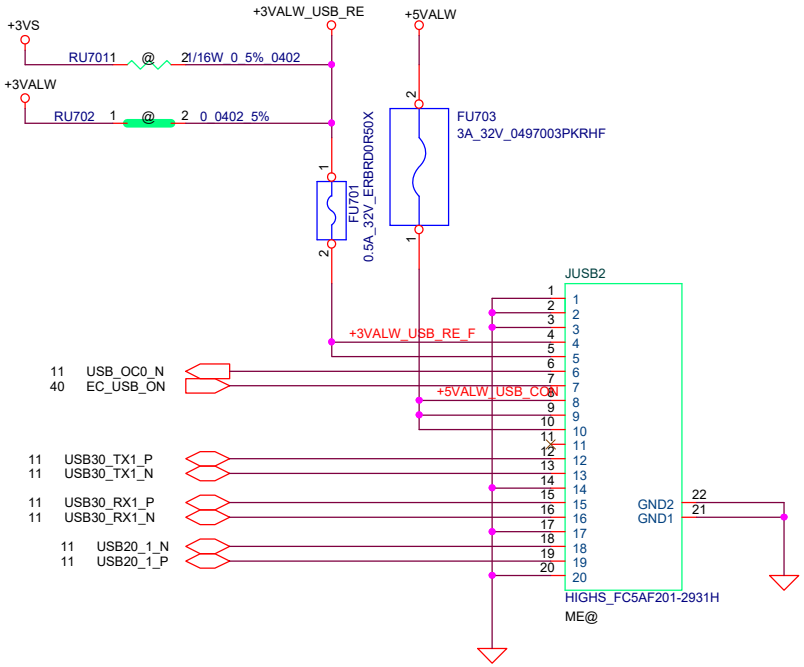
FUSE 2.0A



FAN ID	X13	T14s
0	DELTA 0v, Low	DELTA 0v, Low
1	Toshiba 1.65v, Middle	SUNON 1.65v, Middle
2	AVC 3.2v, high	AVC 3.2v, High

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	Thermal		
Size	Document Number		Rev
Custom	Serval/Tiger AMD		0.1
Date:	Wednesday, February 24, 2021	Sheet	38 of 57



need to check

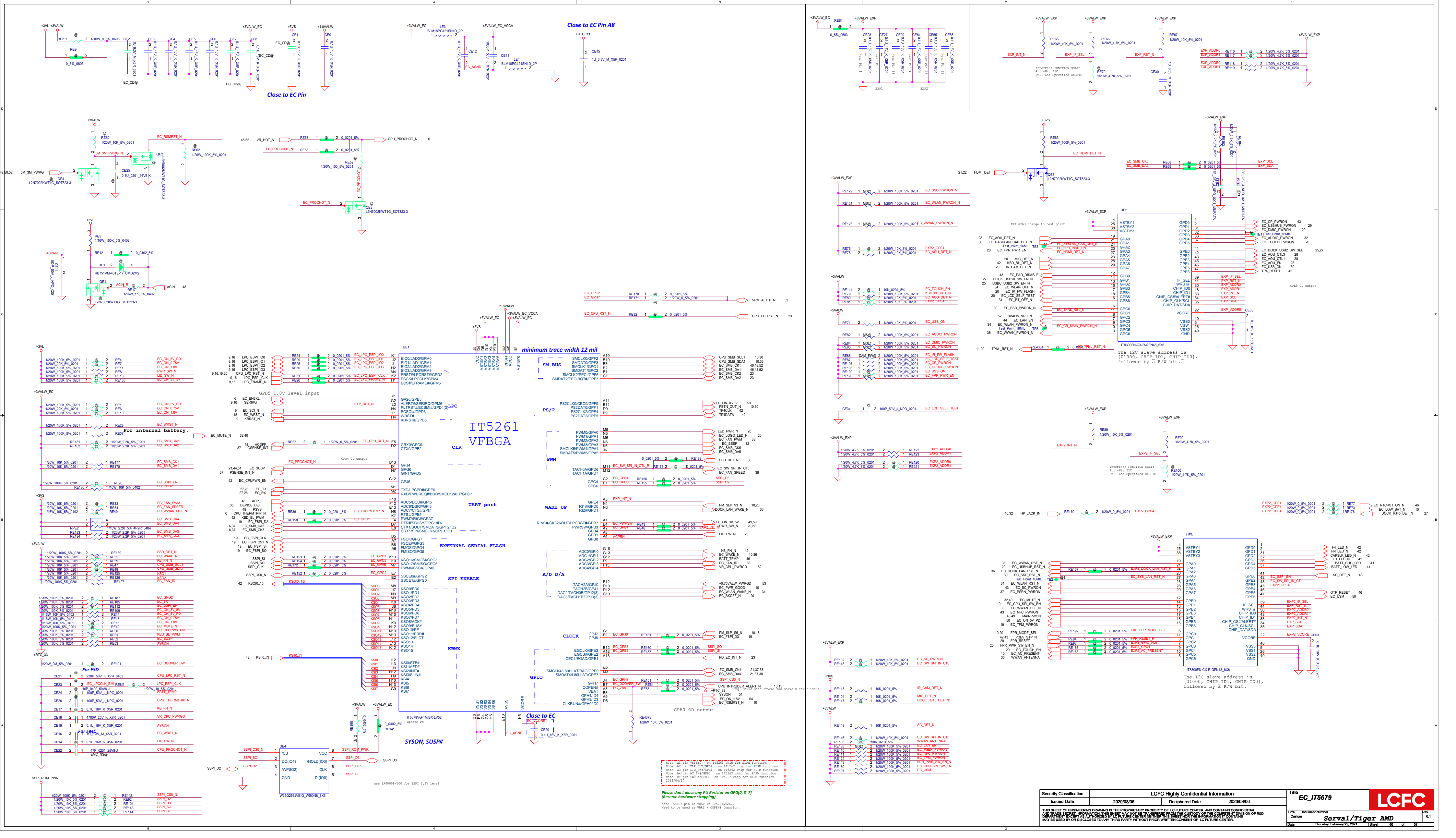
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: **Sub Board CONN**

LCFC

Size	Document Number	Rev
B	Serval/Tiger AMD	0.1

Date: Wednesday, February 24, 2021 Sheet 39 of 57



Close to EC Pin A8
Close to EC Pin
IT5261
VFBGA
minimum trace width 12 mil
SM BUS
LPC
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
A/D D/A
KBMX
CLOCK
GPIO
GPB5 1.8V level input
GPH0 OD output
For internal battery.
For ESD
For EMC
Close to EC
SYSON, SUSP#
IT8300FN-CX-R-QFN48_6X6
The I2C slave address is (01000, CHIP_ID1, CHIP_ID0), followed by a R/W bit.
Please don't place any PU Resistor on GPG[0, 3~7] (Reserve hardware strapping)
W25Q256JVEIQ_WSON8_8X6
Security Classification
LCFC Highly Confidential Information
Issued Date 2020/08/06
Deciphered Date 2020/08/06
Title EC_IT5679
Document Number Serval/Tiger AMD
Rev 0.1
Date: Thursday, February 25, 2021 Sheet 40 of 57
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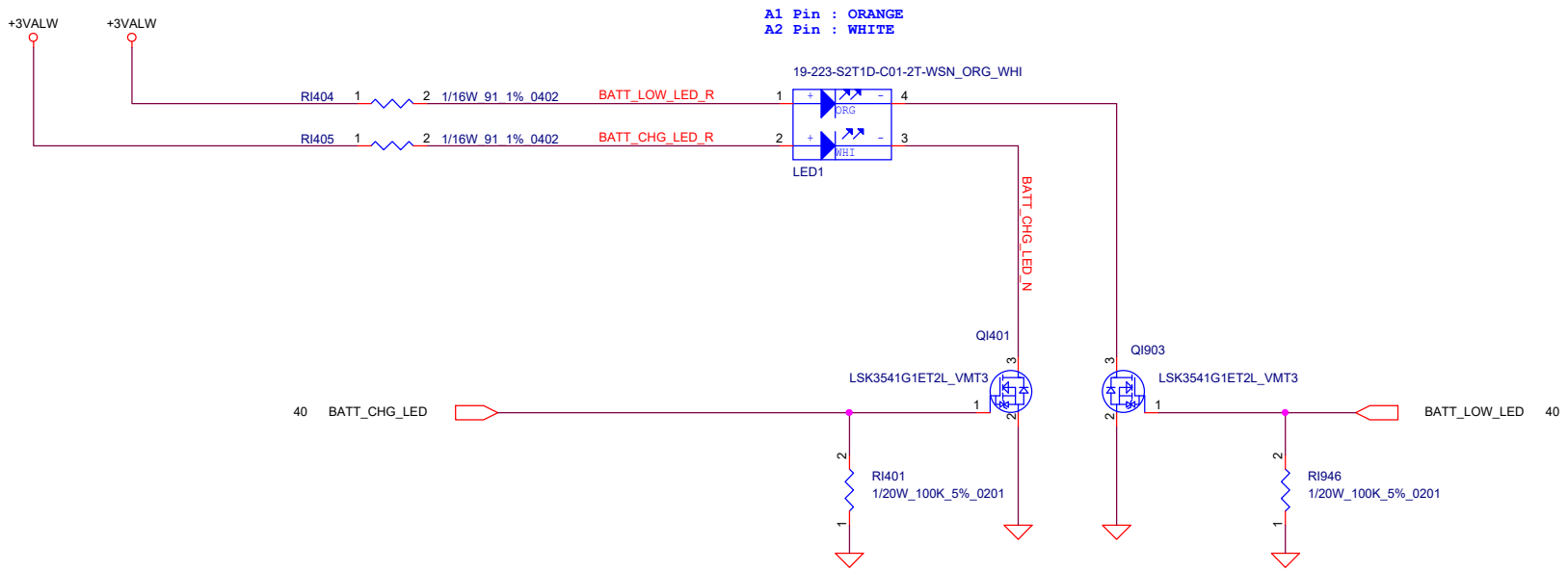
LCFC



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

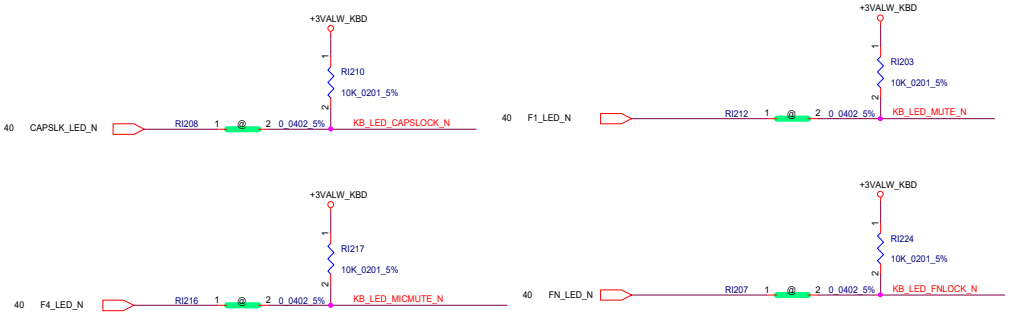
Title: LED/Button

LCFC

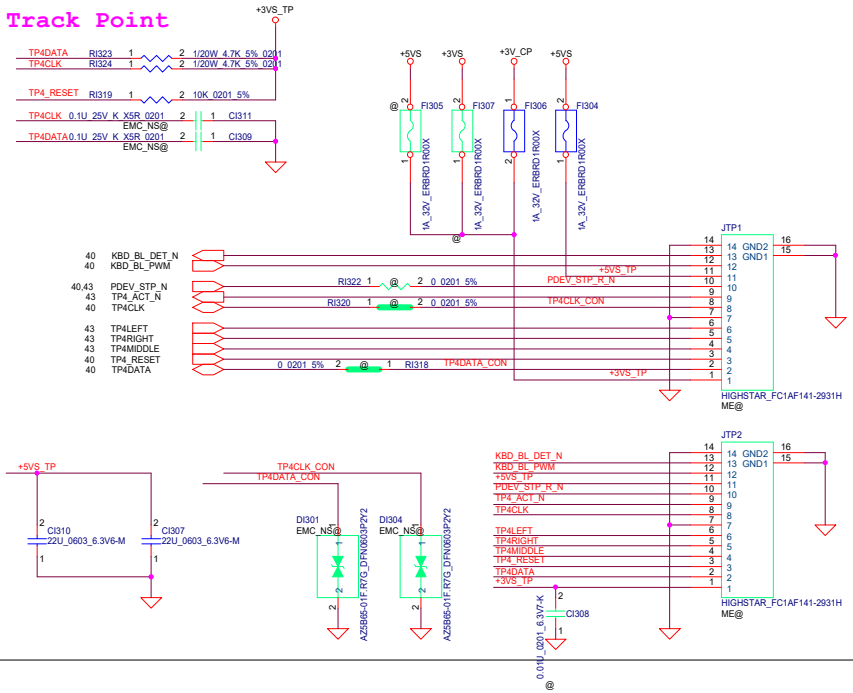
Size	Document Number	Rev
B	Serval/Tiger AMD	0.1

Date: Wednesday, February 24, 2021 Sheet 41 of 57

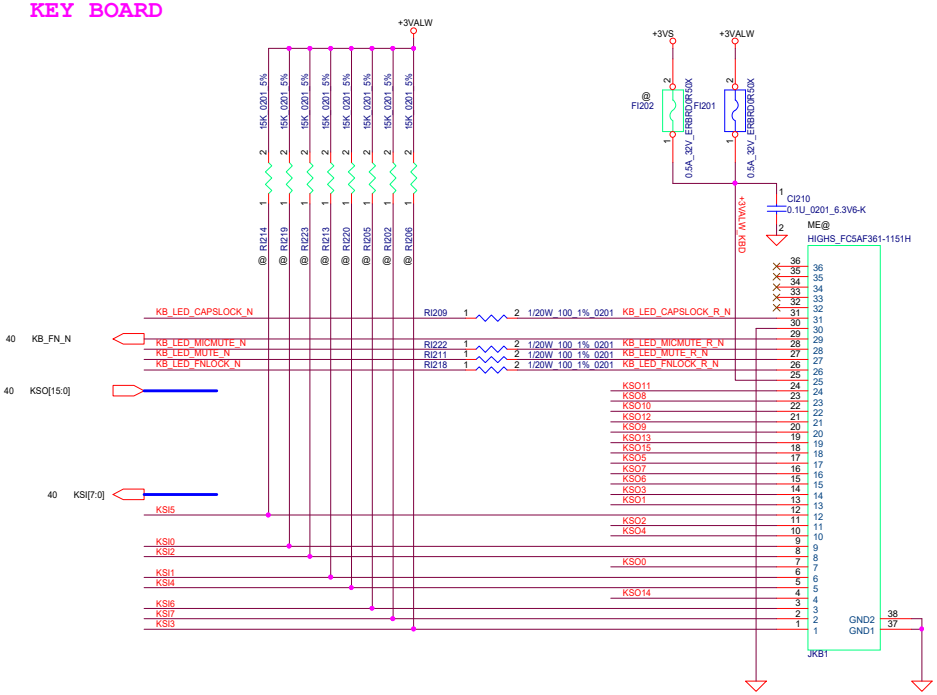
KB LED CONTROL

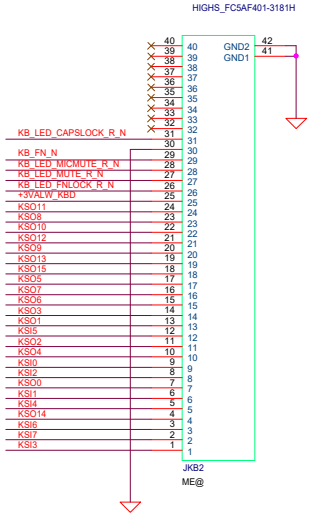


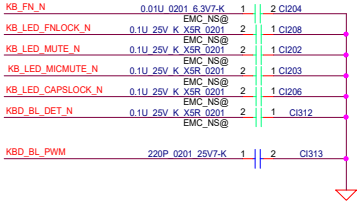
Track Point



KEY BOARD



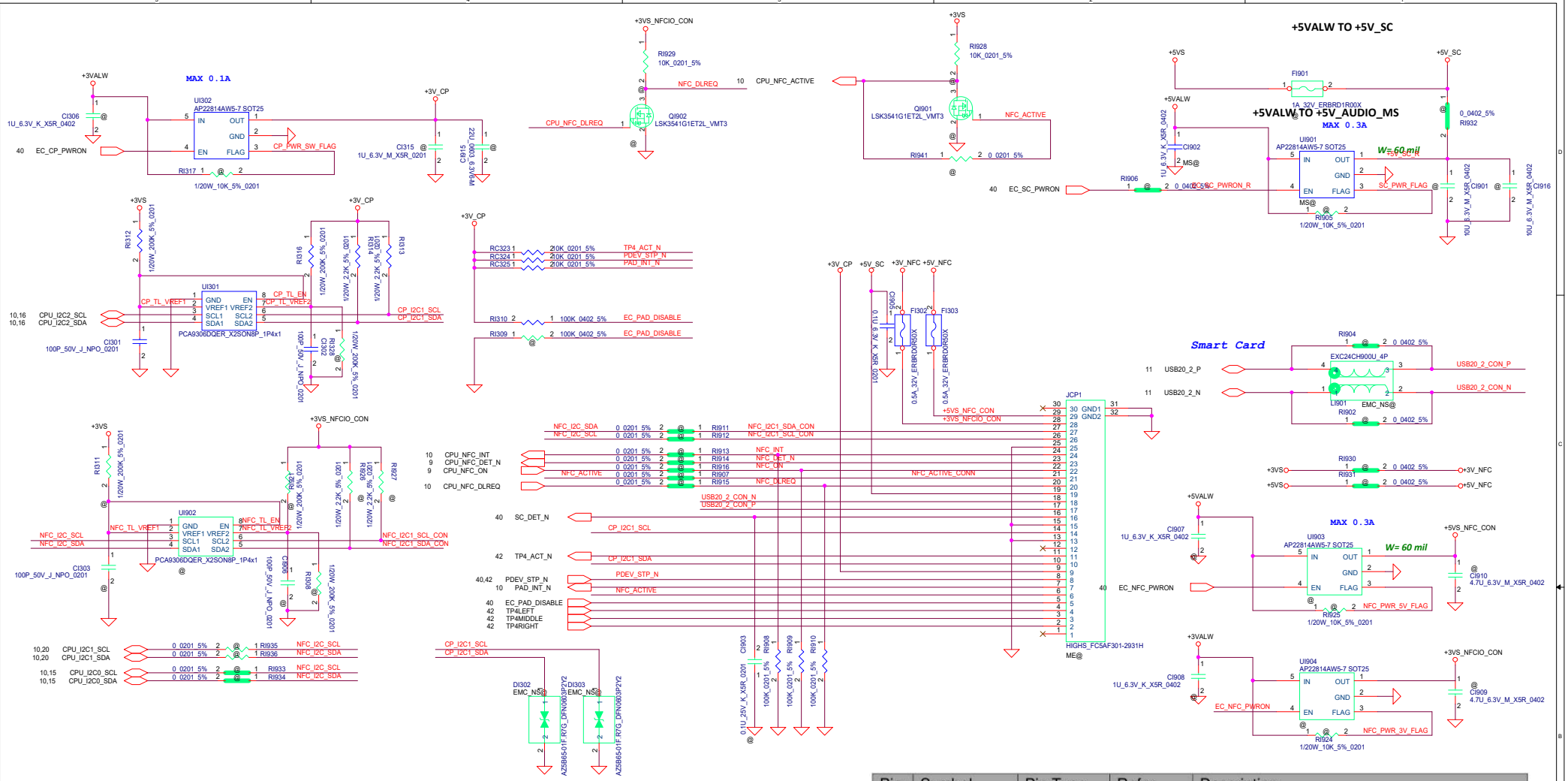




JKBL1 JTP1: Serval_X13
JKBL2 JTP2: Tiger_T14s

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	KB/KBBL CONN		LCFC
Size C	Document Number Serval/Tiger AMD		Rev 0.1
Date: Wednesday, February 24, 2021	Sheet 42 of 57		



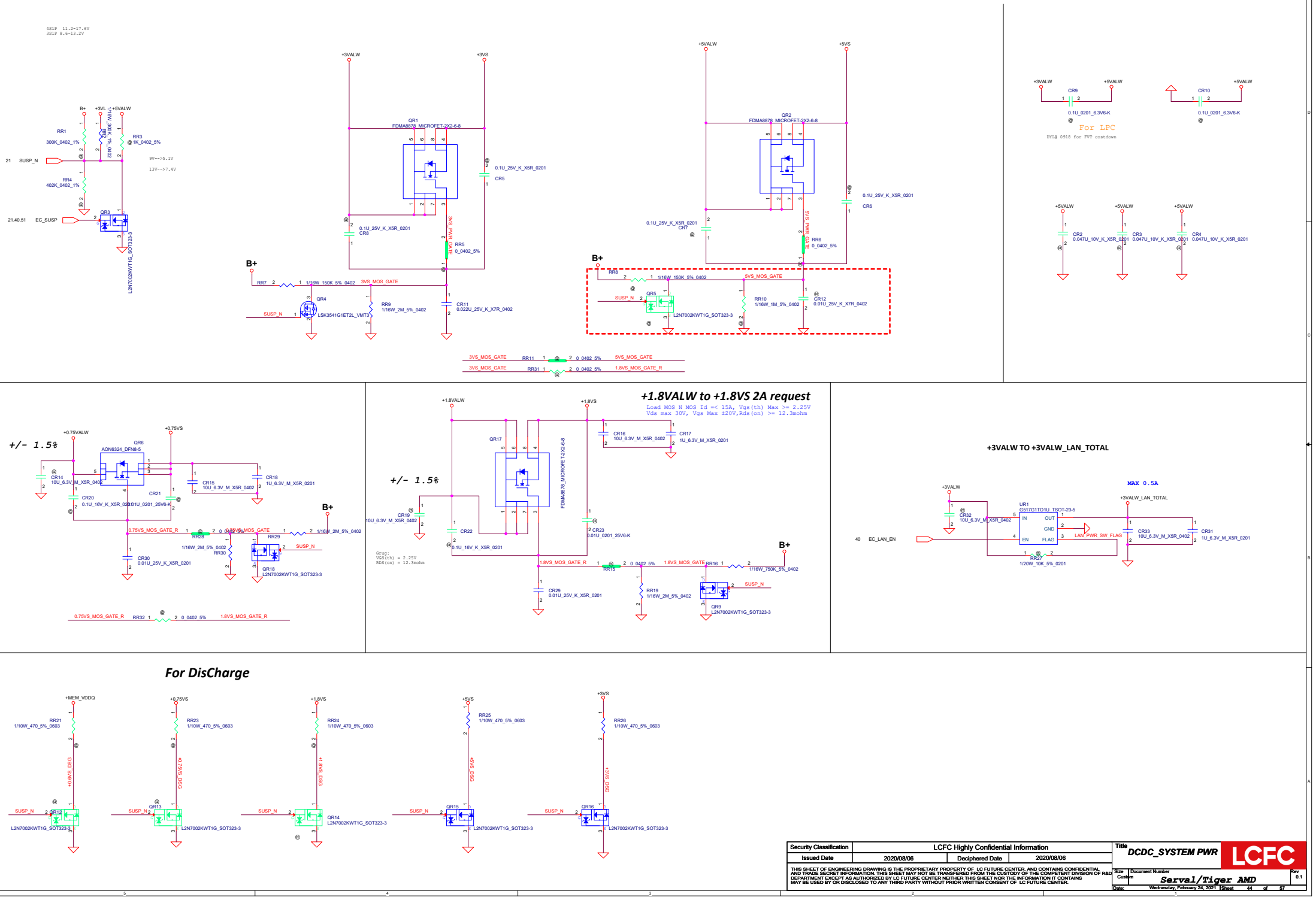
Original pin assign

Name	Pin#	Type	Function
GND	1	Power	Signal Ground
I2C_CLK	2	IN/OUT	I2C Clock to System I2C I/F on CPU/PCH
IPD_GND	3	IN	TrackPoint ground
NC	4		
-TP4_ACT	5	IN	TrackPoint Activity status. Please refer to “4.2.8”
I2C_DAT	6	IN/OUT	I2C Data to System I2C I/F on CPU/PCH
VDD	7	Power	Supply power from system. Power is not supplied when system is in S3, S4, S5 and G5 state. (Refer to electrical requirement)
- PDEV_STP	8	IN	This signal is used to disable to report button status and finger status to system when system LCD lid is closed or is in Tent /Stand /Tablet modes (Yoga case). Please refer to “4.2.5-PDEV_STP”
-I2C_INT	9	OUT	Interrupt for I2C communication
NFC_Active	10	IN	This signal should use if NFC Antenna is implemented under touch pad PCBA. This signal should be NC or not be used in touch pad PCBA if NFC antenna is not implemented under touch pad PCBA. Please refer to “4.2.6 NFC_Active”
PAD_DISABLE	11	IN	This signal is used to disable touch pad. Please refer to “4.2.4 PAD_DISABLE”.
TP4LEFT	12	IN	TrackPoint button signal
TP4MIDDLE	13	IN	TrackPoint button signal
TP4RIGHT	14	IN	TrackPoint button signal

Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V – 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C_SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	TouchPad CONN		
Size	C	Document Number	Serval/Tiger AMD
Rev	0.1		
Date:	Wednesday, February 24, 2021	Sheet	43 of 57



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

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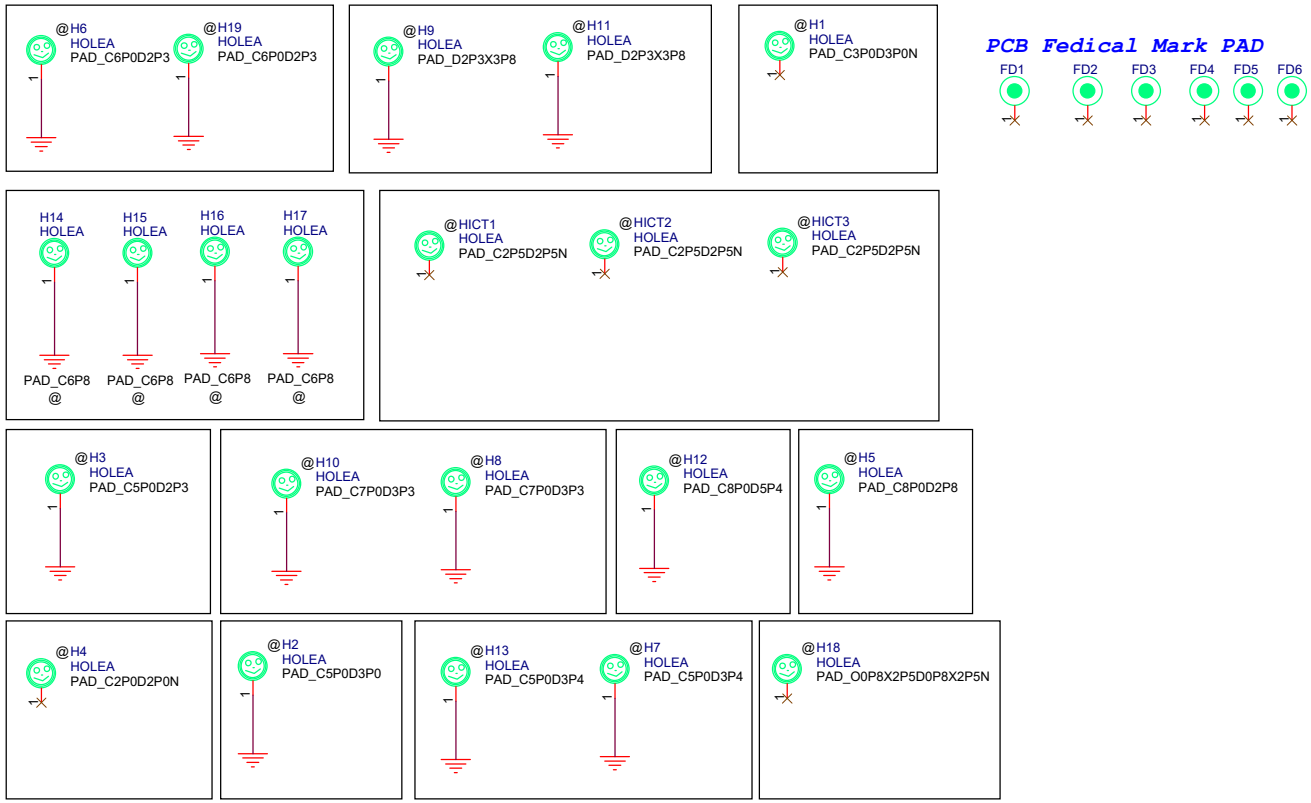
Title: DCDC_SYSTEM PWR

LCFC

Size	Document Number	Rev
Custom	Serval/Tiger AMD	0.1

Date: Wednesday, February 24, 2021 Sheet 44 of 57



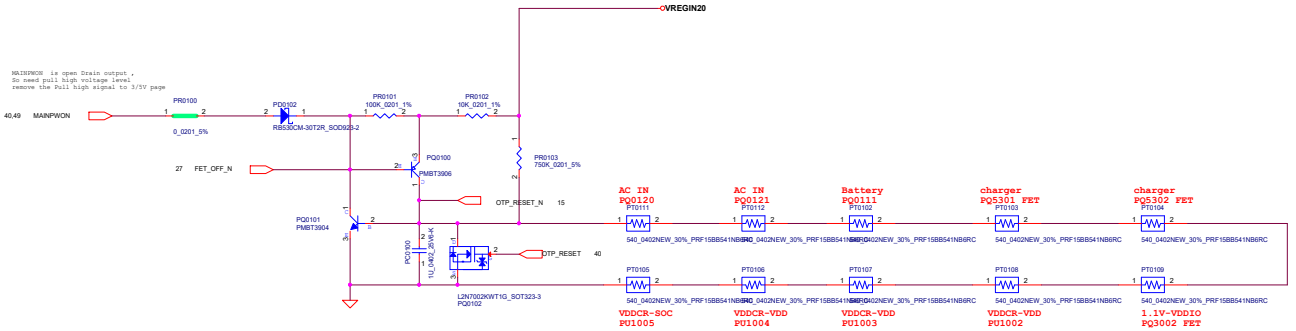
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

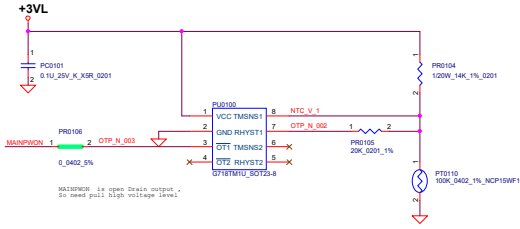
Title: *Hole/Shielding*

LCFC

Size	Document Number	Rev
B	*Serval/Tiger AMD*	0.1

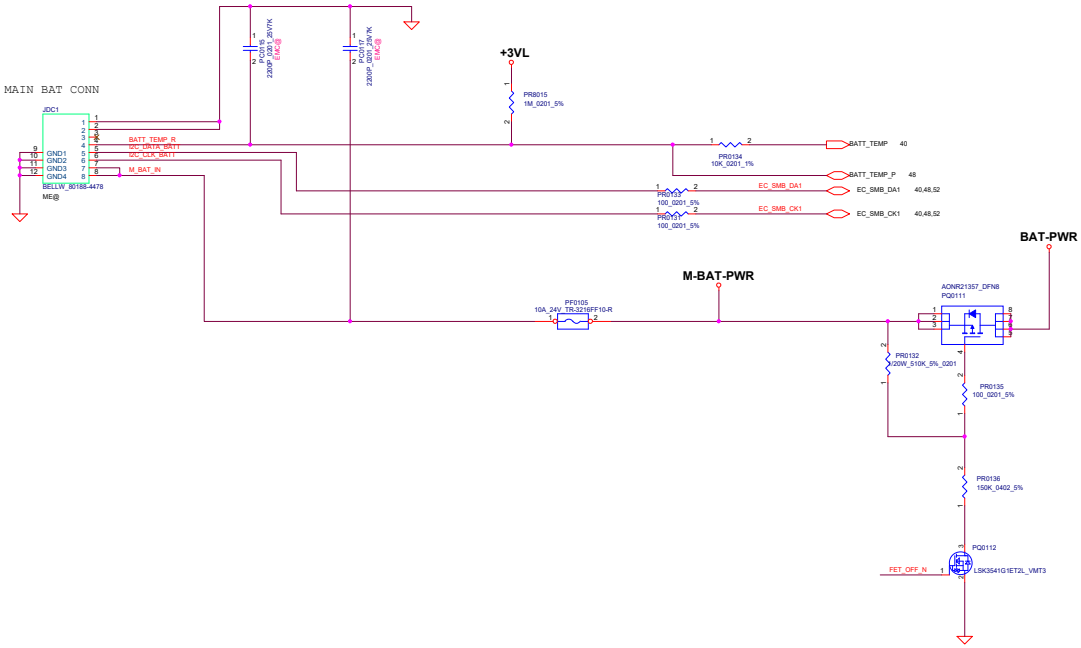
Date: Wednesday, February 24, 2021 Sheet 45 of 57

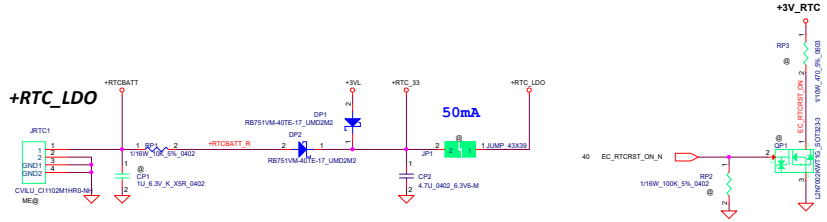




PRT0110 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

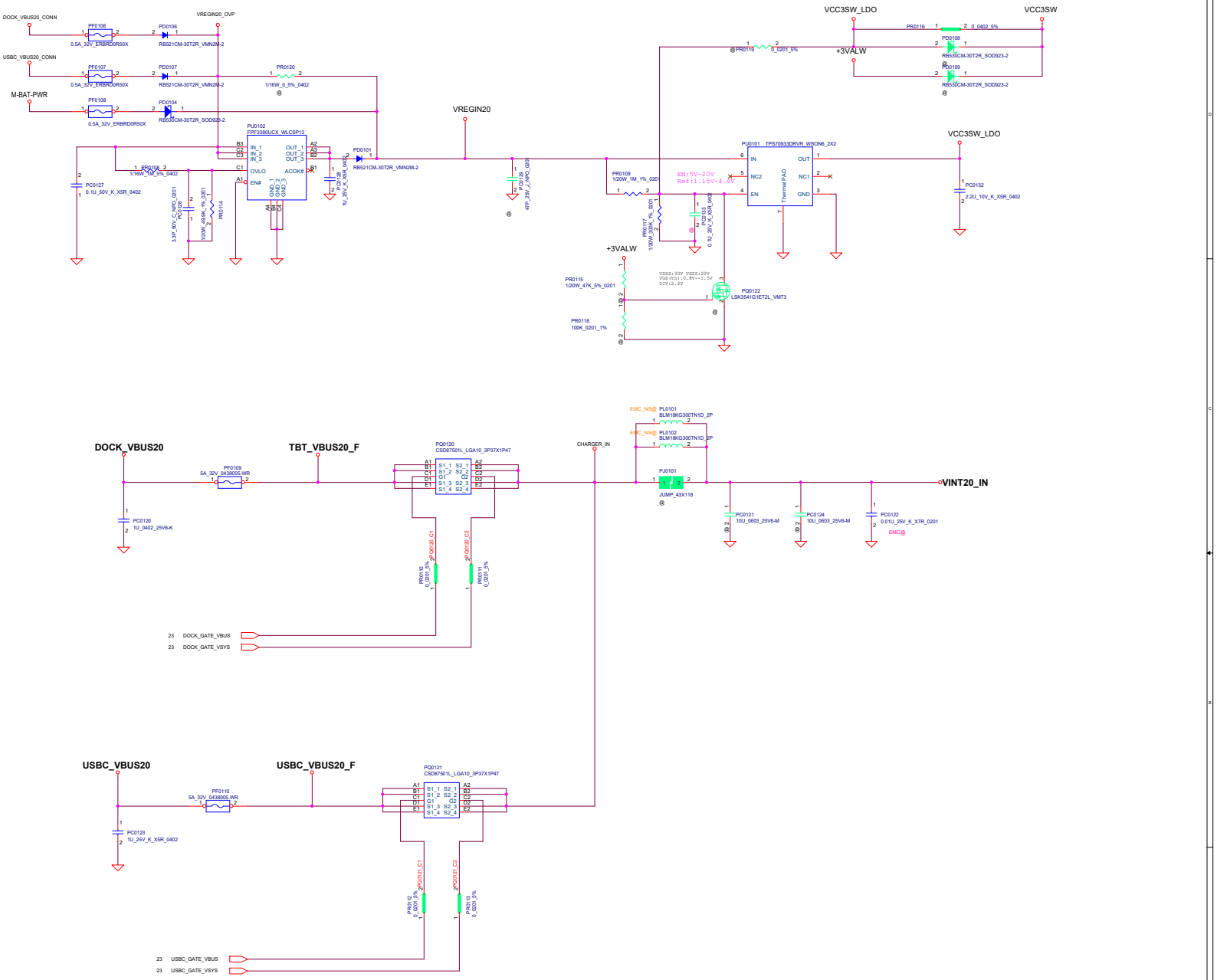
```
540_0402NEW_30%_PRF15BB541NB6RC
25~100Degree
0.54@25 Degree
1.2*0.54*k@85Degree
2*0.54 k@100 Degree
20*0.54 k@120Degree
100*0.54 k@130Degree
350*0.54 k@140Degree
Vbattrey min =9V,Vbattery max =12.6V
Vthreshold min=0.65V,Vthreshold min=0.85V,
TotalR ( PTC)*(VBatt-1.25)/(TotalR ( PTC)+750)=0.65V
TotalR ( PTC)max=59.8K~==110 times 0.54 k
TotalR ( PTC)min=43.72K~==80times 0.54 k
Normal run 3Dmark
the max T maybe 85 Degree
the total R PTC= 1.2*0.54*10=12*0.54  k
if only one PTC over 130 degree,
the total PTC is 100*0.54K+11*0.54k,>80*0.54K
and over the min Vthreshold,and active the OTP
if  only one PTC over 140 degree,
the total PTC is 350*0.54K>>80*0.54K
,can over the min Vthreshold
and active the OTP
so,the OTP function is ok
```





Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title	PWR_DCIN/RTC	LCFC	
Size	Document Number	Rev	
Custom	Serval/Tiger AMD	0.1	
Date: Wednesday, February 24, 2021	Sheet 46 of 57		



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: PWR_ACIN

LCFC

Size: Custom | Document Number: Serval/Tiger AMD | Rev: 0.1

Date: Wednesday, February 24, 2021 | Sheet 47 of 57

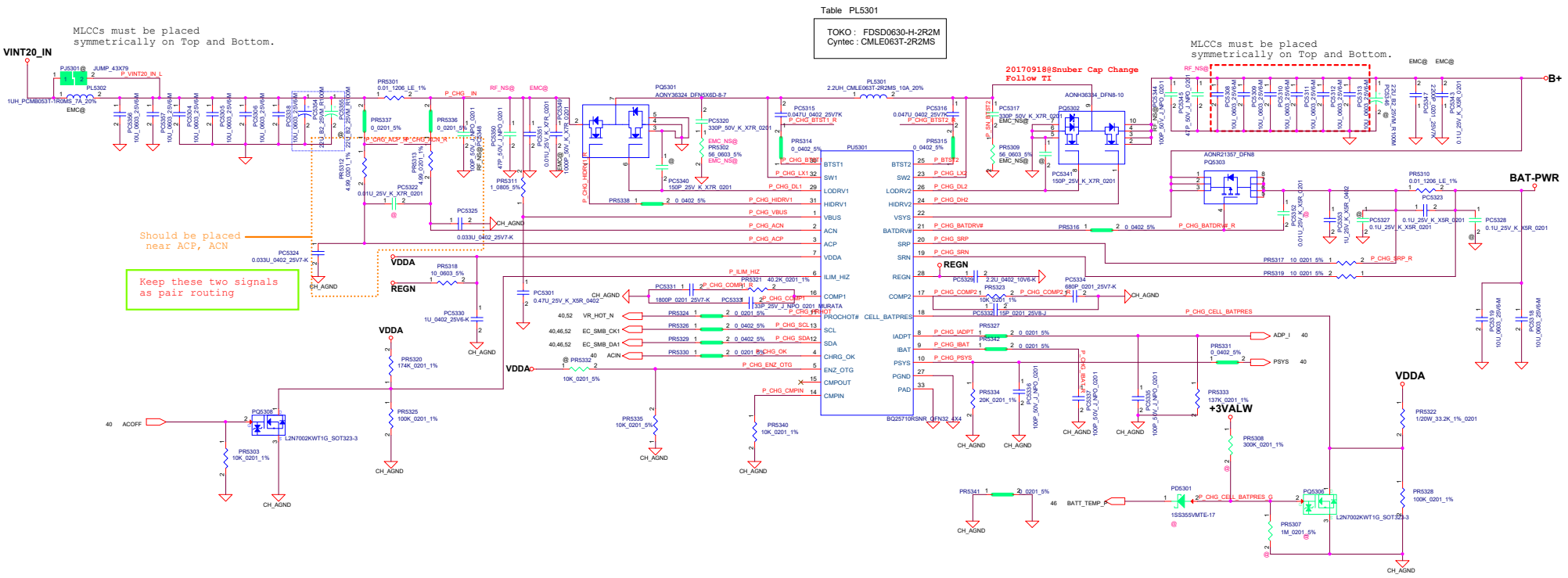


Table PL5301

TOKO :	FDSD0630-H-2R2M
Cyntec :	CMLE063T-2R2MS

IDPM	V(ILIM)	PR147
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

← LOGIC

# of CELL	VCELL_PRES	PR5332
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

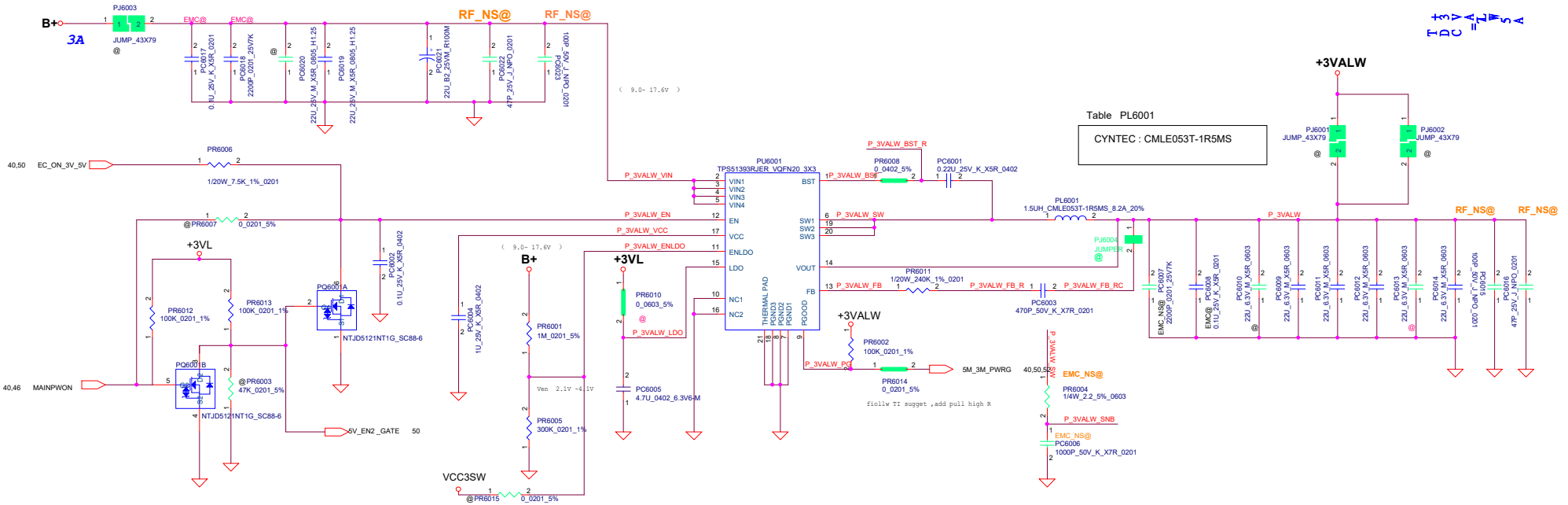
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: PWR_CHARGER

LCFC

Size: Custom | Document Number: Serval/Tiger AMD | Rev: 0.1

Date: Wednesday, February 24, 2021 | Sheet 48 of 57



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

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Title: +3VALW

LCFC

Size	Document Number	Rev
Custom	Serval/Tiger AMD	0.1

Date: Wednesday, February 24, 2021 Sheet 49 of 57

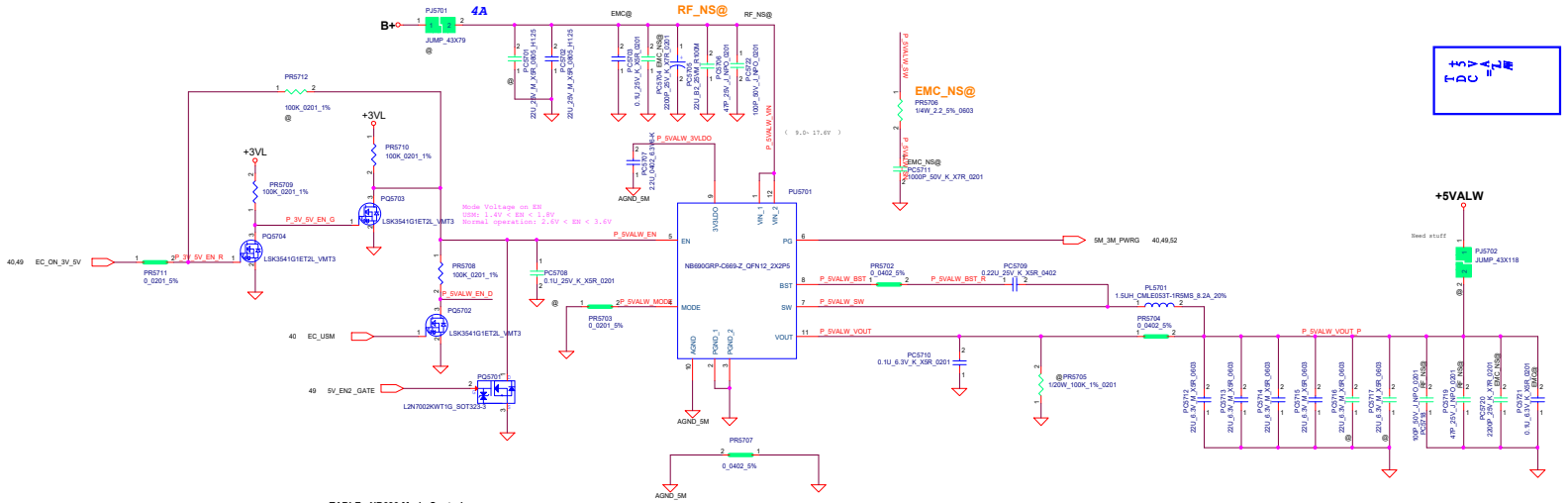


TABLE : NB690 Mode Control

RMode	MODE	VOUT	3V3LDO
0	Ceramic Cout	5.1V	3.3V
60K	POSCAP Cout	5.1V	3.3V
120K	Ceramic Cout	5V	3.3V
180K	POSCAP Cout	5V	3.3V
Floating	X	3.3V	3.3V

LOGIC

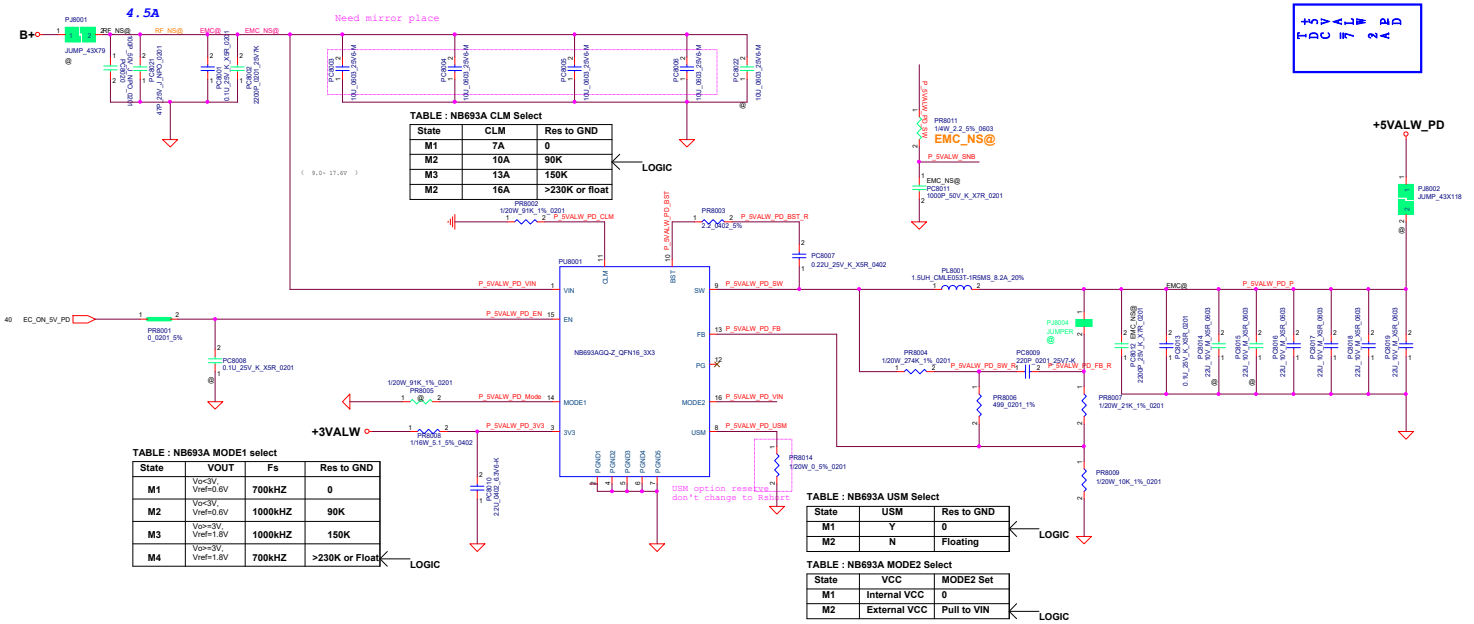


TABLE : NB693A MODE1 select

State	VOUT	Fs	Res to GND
M1	Vo<3V, Vref=0.6V	700kHZ	0
M2	Vo<3V, Vref=0.6V	1000kHZ	90K
M3	Vo>=3V, Vref=1.8V	1000kHZ	150K
M4	Vo>=3V, Vref=1.8V	700kHZ	>230K or Float

LOGIC

TABLE : NB693A USM Select

State	USM	Res to GND
M1	Y	0
M2	N	Floating

LOGIC

TABLE : NB693A MODE2 Select

State	VCC	MODE2 Set
M1	Internal VCC	0
M2	External VCC	Pull to VIN

LOGIC

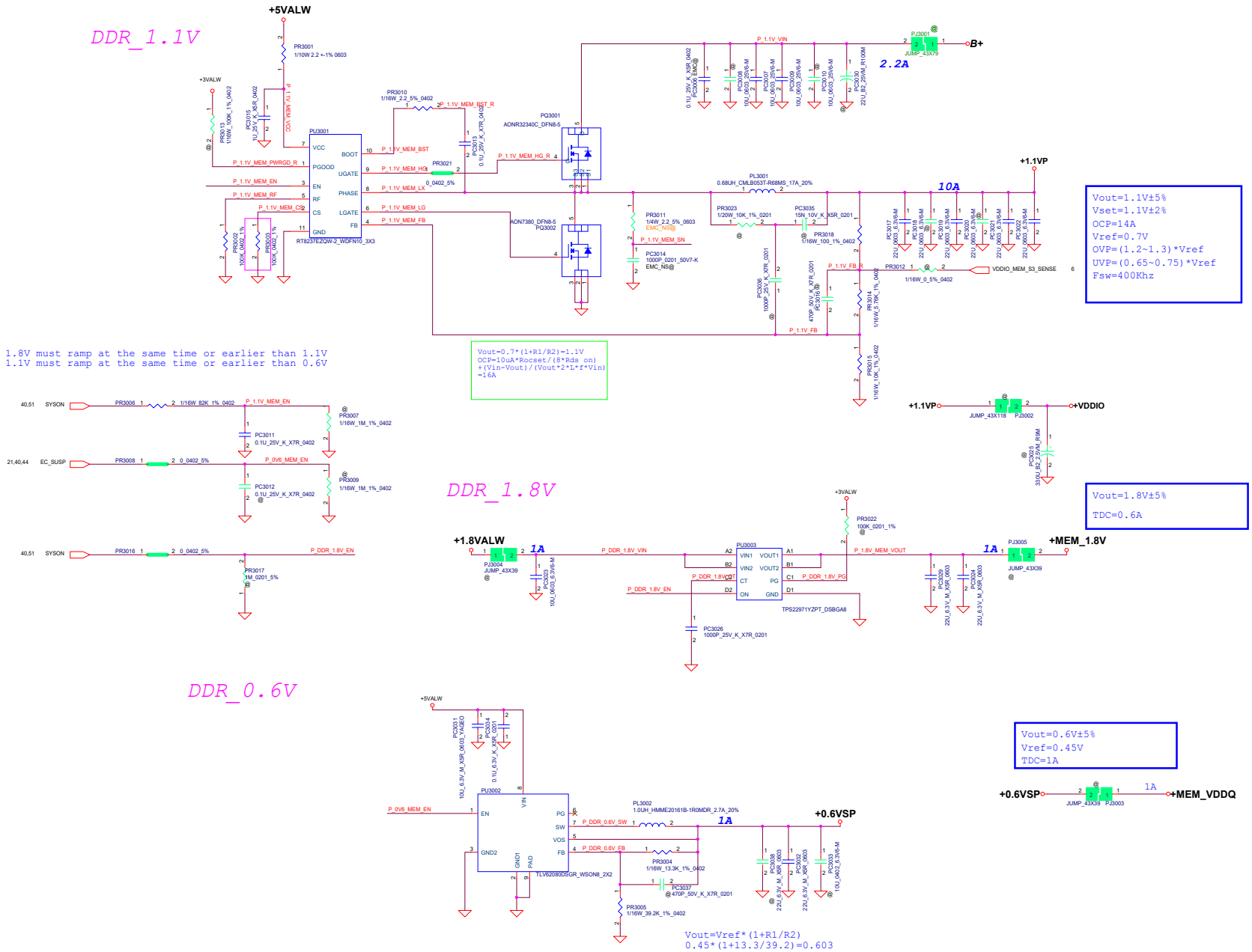
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: 5VALW&+5VALW_PD

LCFC

Size: Custom | Document Number: Serval/Tiger AMD | Rev: 0.1

Date: Wednesday, February 24, 2021 | Sheet 50 of 57



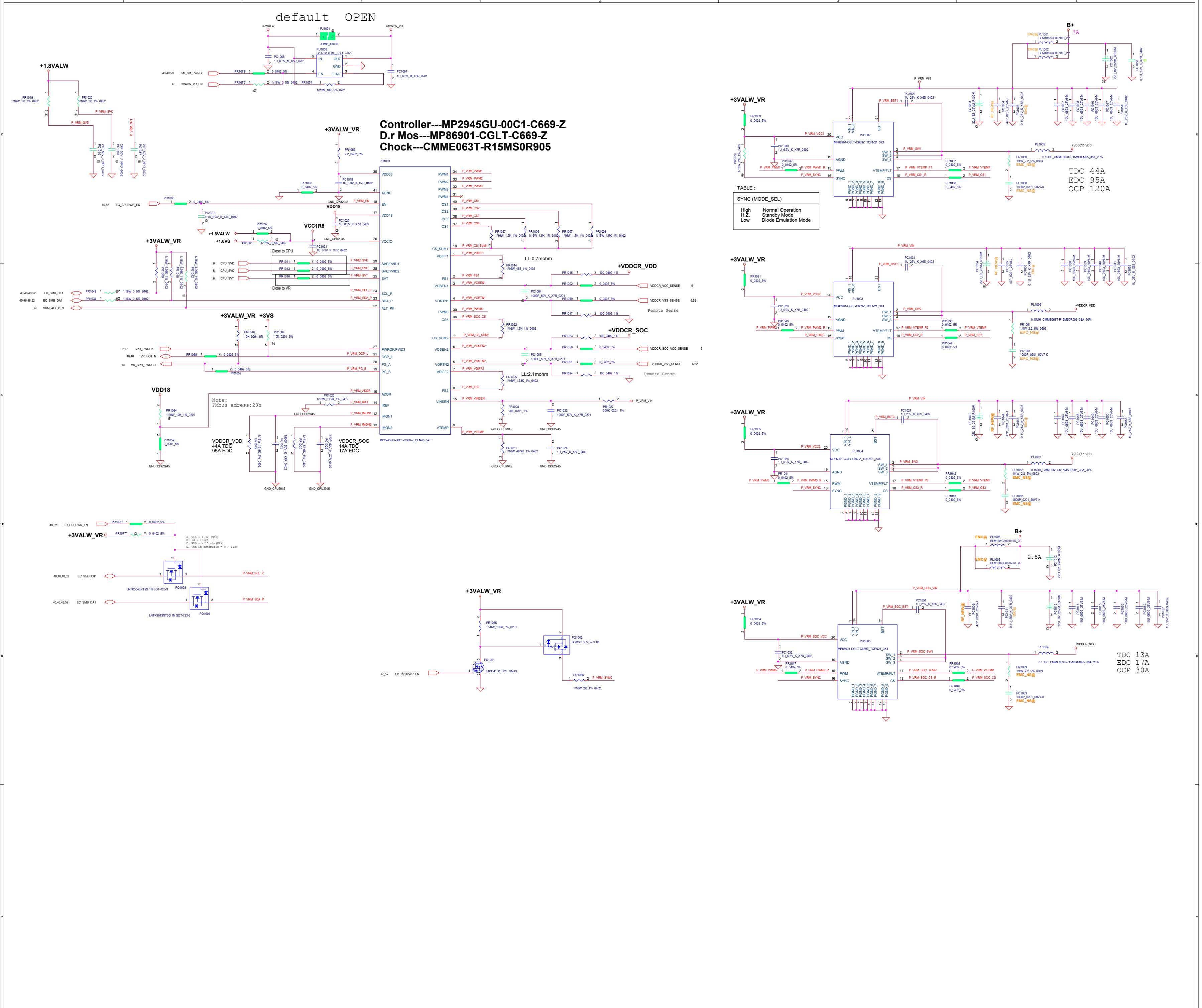
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: PWR_Memory PWR

LCFC

Size: Custom | Document Number: Serval/Tiger AMD | Rev: 0.1

Date: Wednesday, February 24, 2021 | Sheet 51 of 57



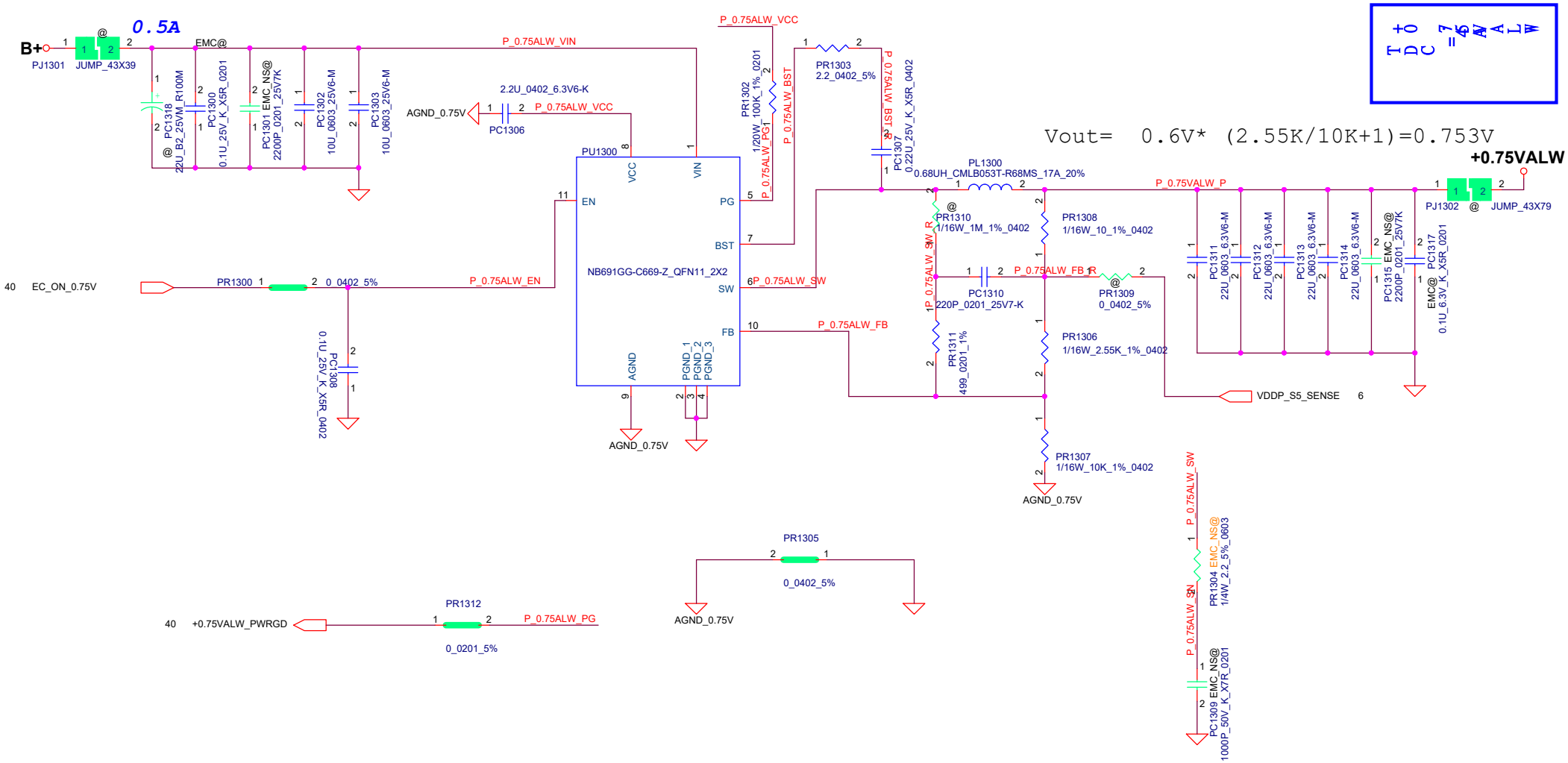
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: CPU PWR Controller

Document Number: Serval/Tiger AMD

Date: Wednesday, February 24, 2021 Sheet 52 of 57

LCFC



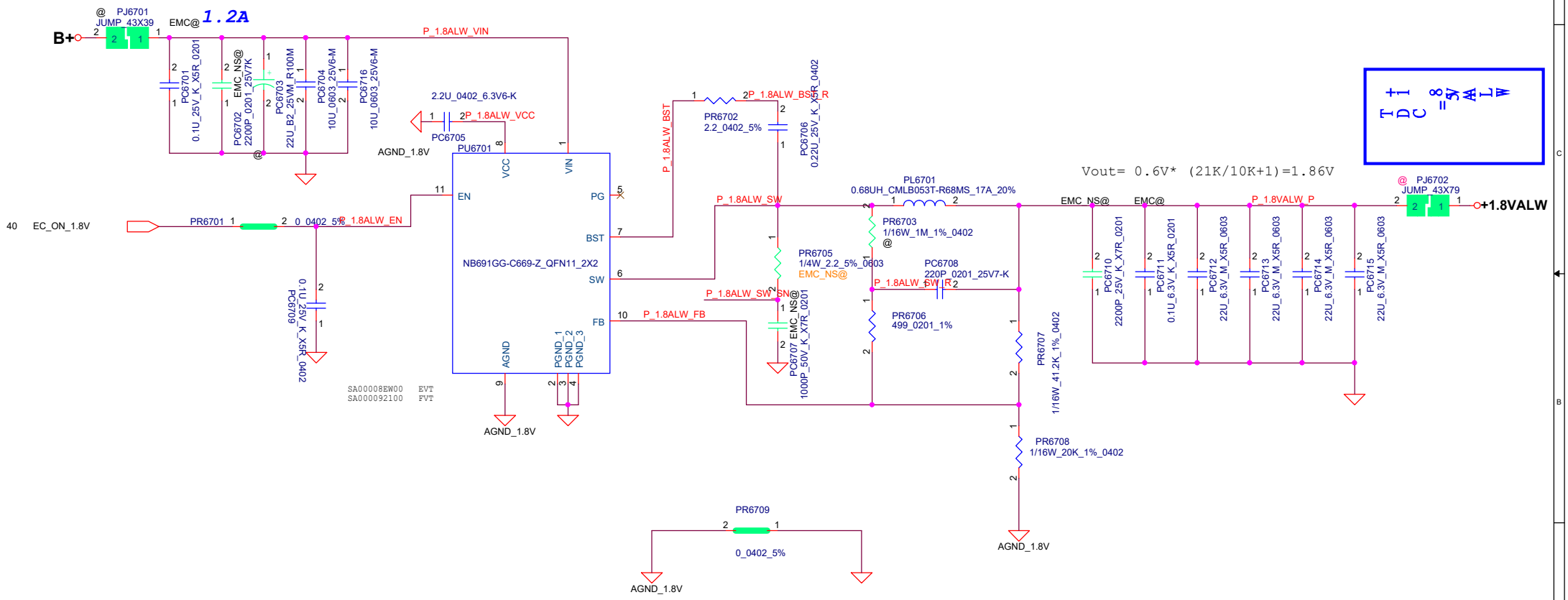
Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: PWR1_+0.75VALW

LCFC

Size	Document Number	Rev
B	Serval/Tiger AMD	0.1

Date: Wednesday, February 24, 2021 Sheet 53 of 57



Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

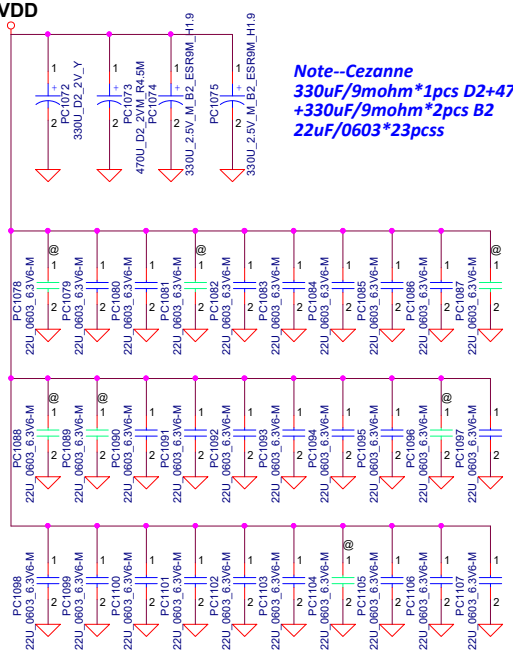
Title: PWR2_+1.8VALW

LCFC

Size	Document Number	Rev
B	Serval/Tiger AMD	0.1

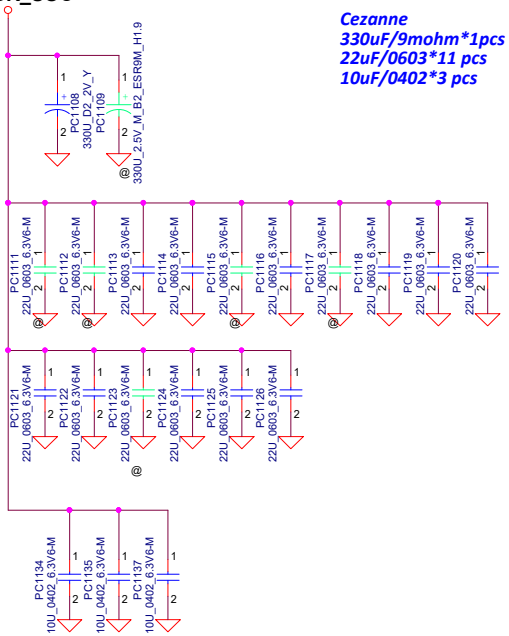
Date: Wednesday, February 24, 2021 Sheet 54 of 57

+VDDCR_VDD



Note--Cezanne
*330uF/9mohm*1pcs D2+470uF/4.5mohm 1pcs D2*
*+330uF/9mohm*2pcs B2*
*22uF/0603*23pcss*

+VDDCR_SOC



Cezanne
*330uF/9mohm*1pcs D2*
*22uF/0603*11 pcs*
*10uF/0402*3 pcs*

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: ***PWR Decoupling***

LCFC

Size	Document Number	Rev
Custom	***Serval/Tiger AMD***	0.1

Date: Wednesday, February 24, 2021 Sheet 55 of 57

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Title		
Change List_EE	LCFC	
Size: C	Document Number: *Serval/Tiger AMD*	Rev: 0.1
Date: Wednesday, February 24, 2021	Sheet 56 of 57	

BLANK

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

Title: *Change List_PWR*	LCFC	
Size: C	Document Number: *Serval/Tiger AMD*	Rev: 0.1
Date: Wednesday, February 24, 2021	Sheet 57 of 57	