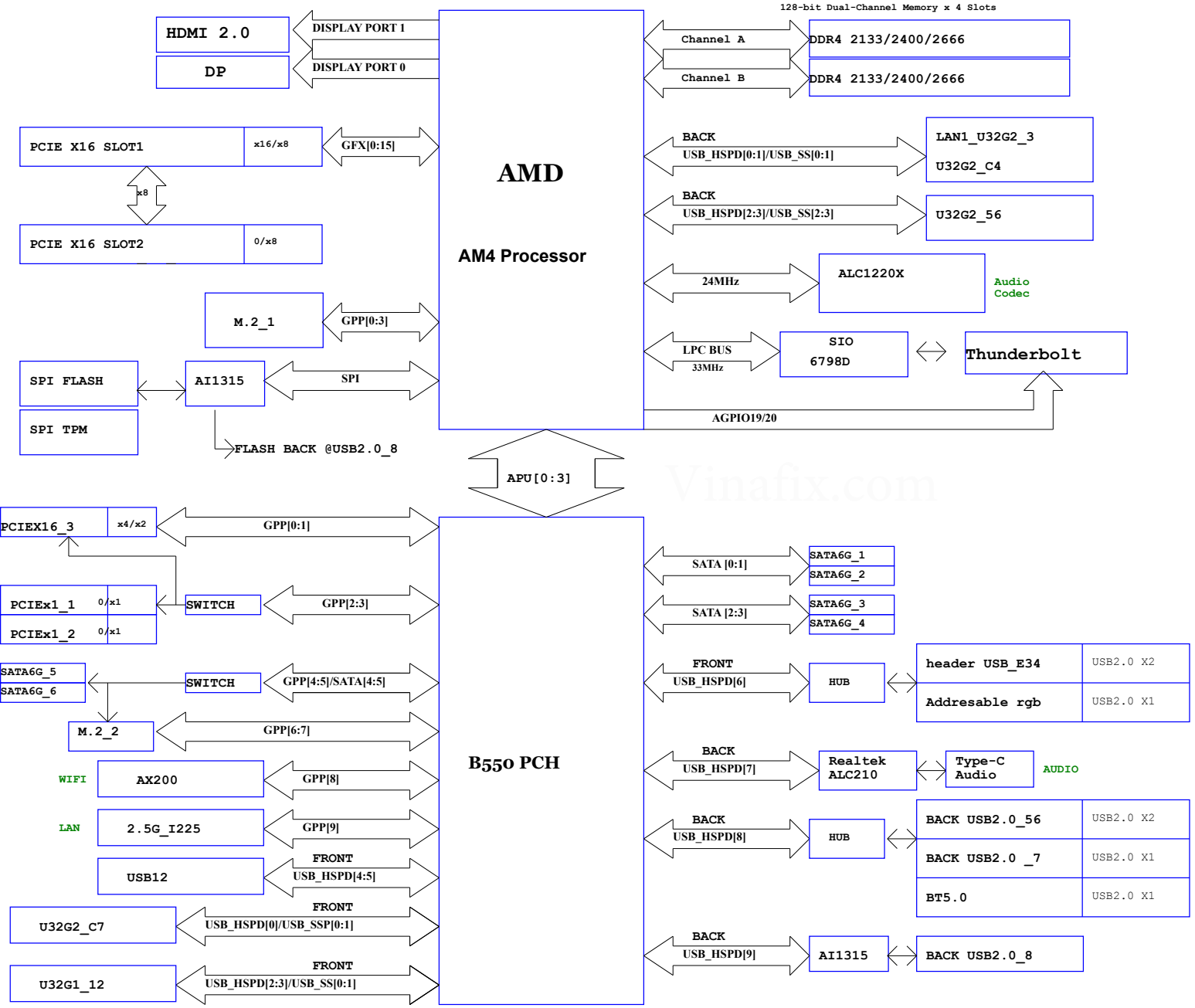
ACONITUM

Rev 1.0 2019



ASUSTek Computer Inc.

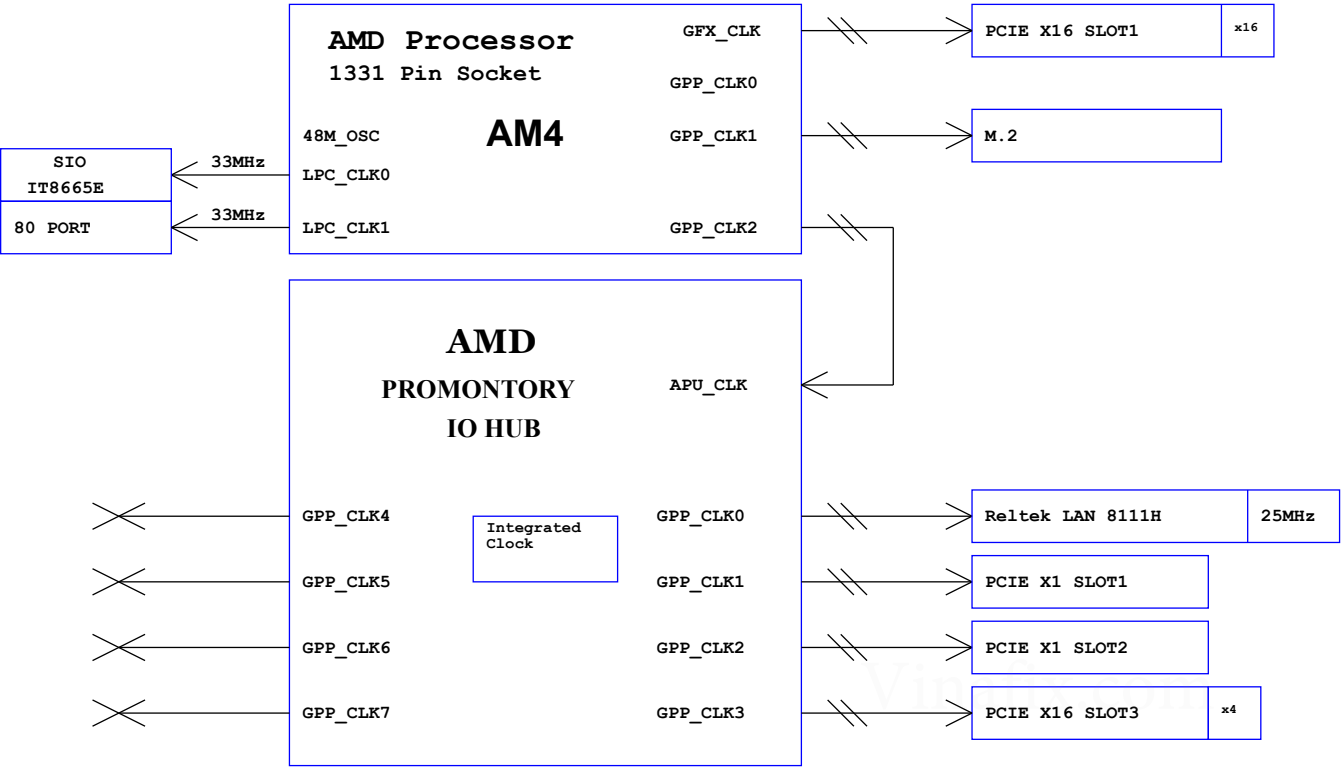
Title : Block Diagram

Engineer: Leoric_Chen

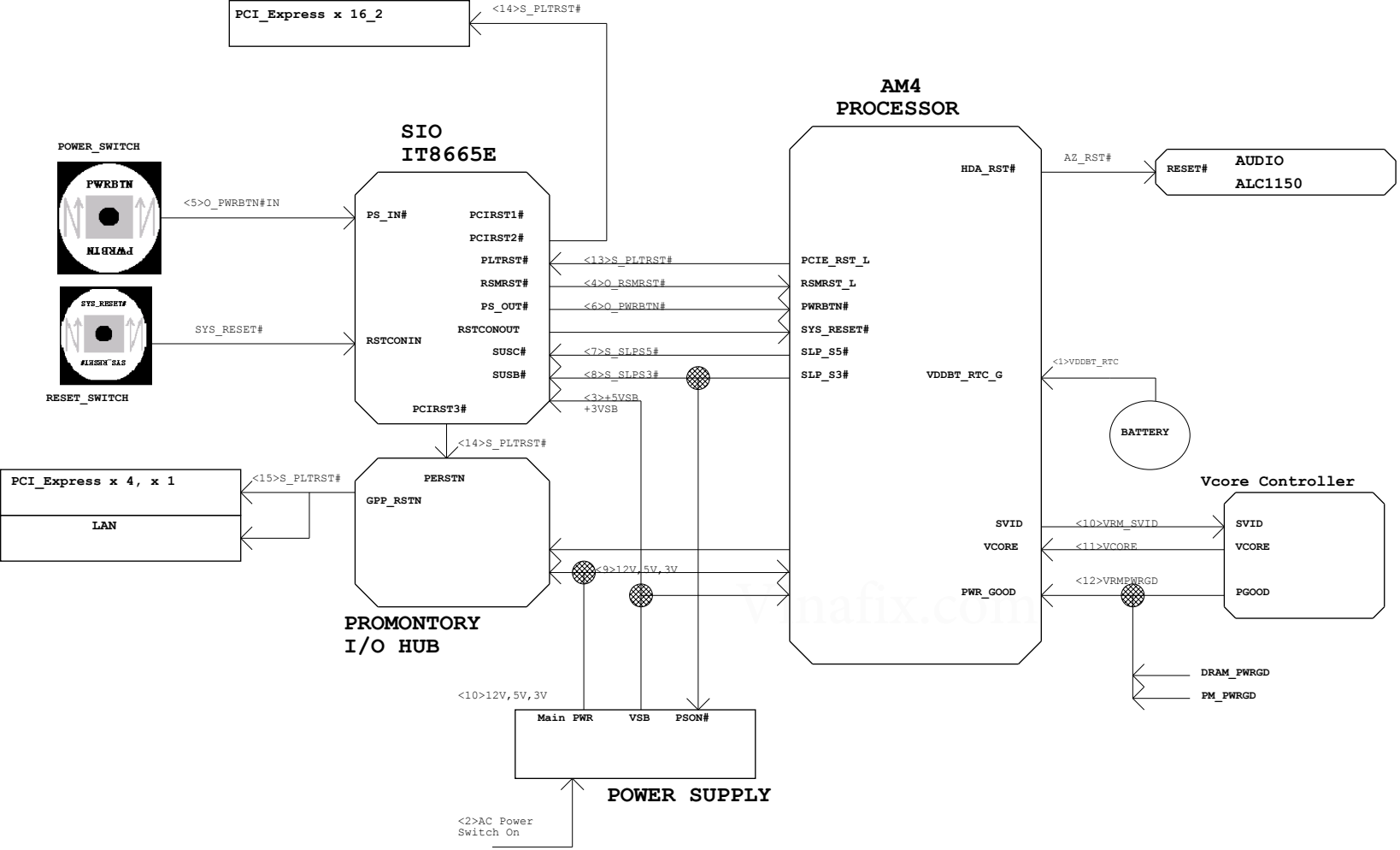
Size	Project Name	Rev
A3	AM4	R1.00

Date: Tuesday, March 03, 2020 Sheet 1 of 127

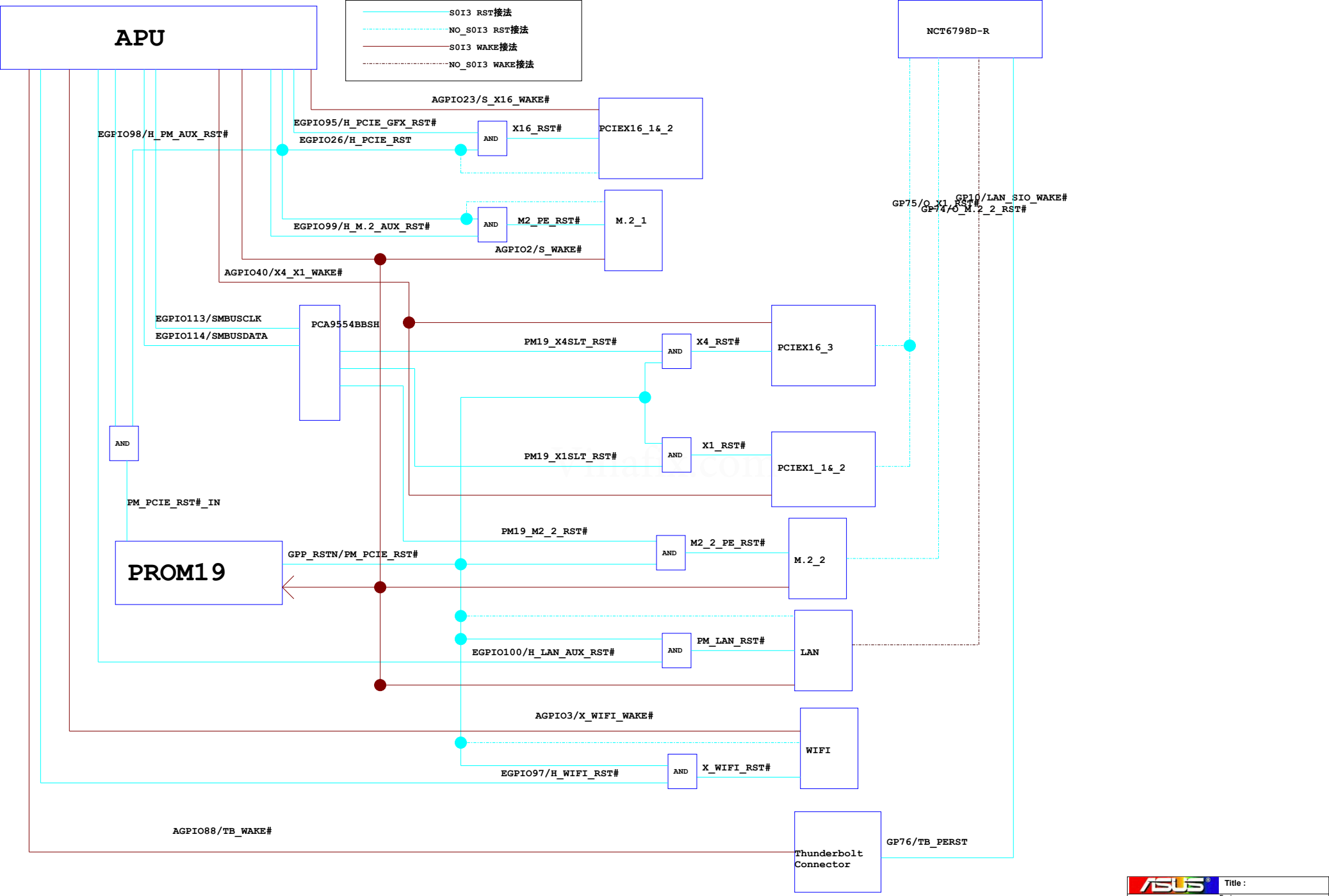
ICG : Integrated Clock Gen.



ASUSTek Computer Inc.	Title : CLOCK DISTRIBUTION	
	Engineer: Elainelx_Li	
Size: A3	Project Name: AM4	Rev: R1.00
Date: Tuesday, March 03, 2020	Sheet 2 of 127	



ASUSTek Computer Inc.	Title :	
	Engineer:	Elainelx_Li
Size: A3	Project Name: AM4	Rev: R1.00
Date: Tuesday, March 03, 2020	Sheet 3 of 127	



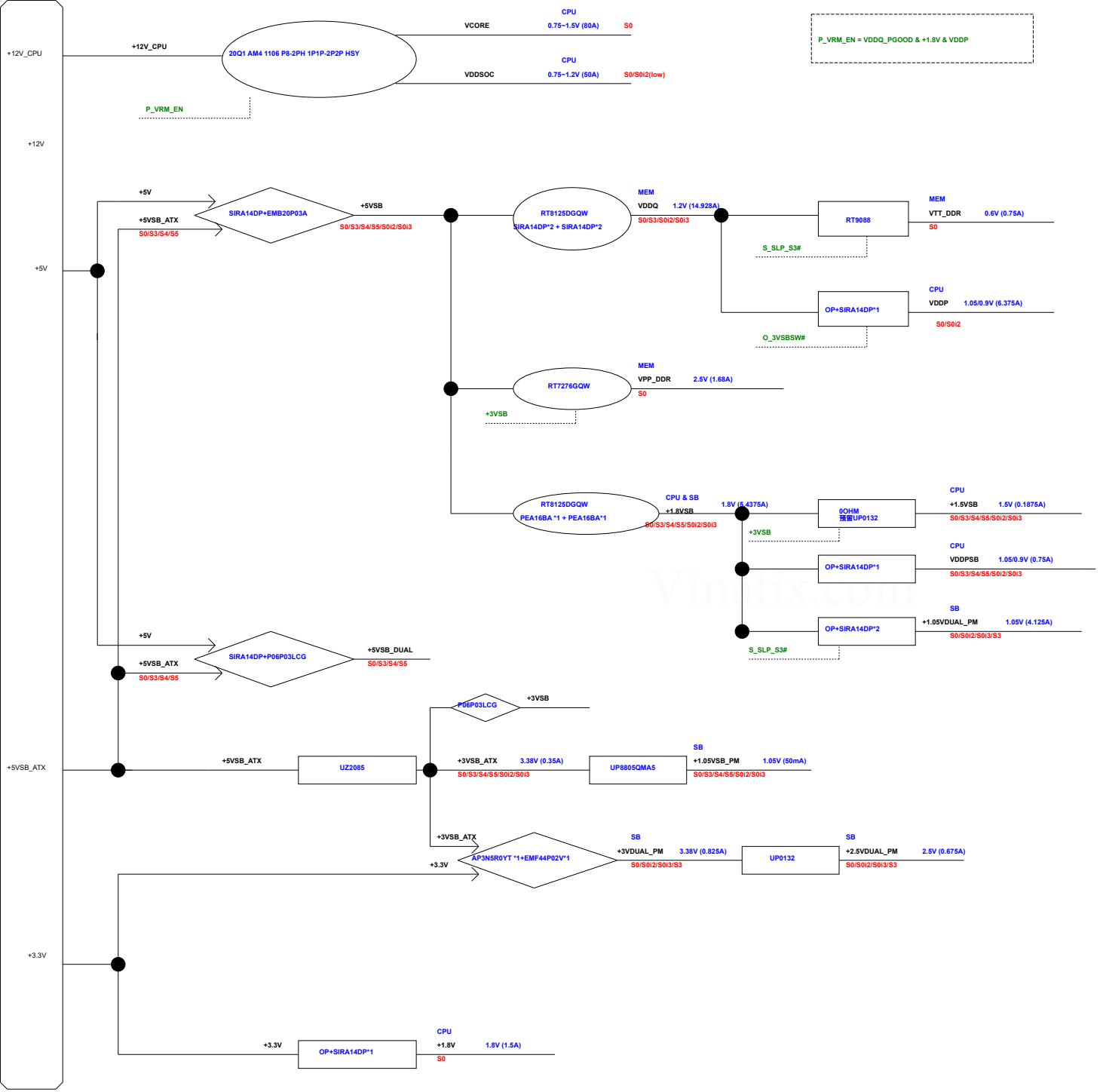
Title :

Engineer: Leoric_Chen

ASUSTek Computer Inc.

Size: A2 | Project Name: AM4 | Rev: R1.00

Date: Tuesday, March 03, 2020 | Sheet 4 of 127



AM4 Power Rail	S0	S0i2	S0i3	S3
VCORE	ON	OFF	OFF	OFF
VDDSOC	ON	Low	OFF	OFF
VDDQ	ON	ON	ON	ON
VTT_DDR	ON	OFF	OFF	OFF
VPP_DDR	ON	OFF	OFF	OFF
+1.8VSB	ON	ON	ON	ON
+1.5VSB	ON	ON	ON	ON
VDDPSB	ON	ON	ON	ON
+1.05VSB_PM	ON	ON	ON	ON
VDDP	ON	ON	OFF	OFF
+1.8V	ON	ON	OFF	OFF
+3VDUAL_PM	ON	ON	ON	OFF
+2.5VDUAL_PM	ON	ON	ON	OFF
+1.05VDUAL_PM	ON	ON	ON	OFF

<Variant Name>

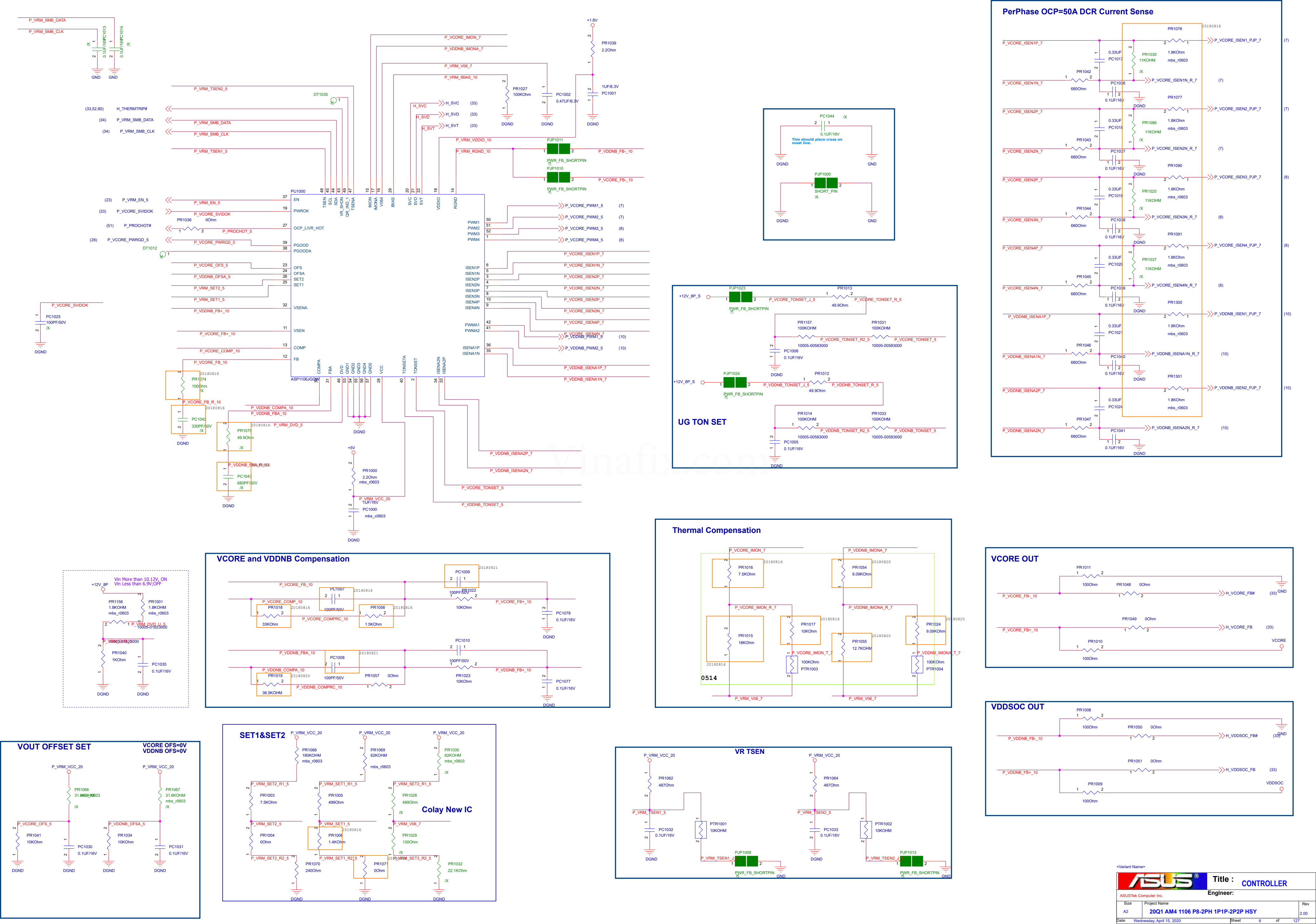
Title : Power Flow

<OrgName>

Engineer:

Size	Project Name	Rev
A1	AM4 B550	1.00

Date: Tuesday, March 03, 2020 Sheet 5 of 127



PerPhase OCP=50A DCR Current Sense
UG TON SET
Thermal Compensation
VCORE OUT
VDDSOC OUT
VCORE and VDDNB Compensation
VOUT OFFSET SET
VCORE OFS=0V
VDDNB OFS=0V
SET1&SET2
Colay New IC
VR TSEN
0514
Vin More than 10.12V, ON
Vin Less than 6.9V,OFF
This should place cross on moat line.
PU1000
ASP1106JGQW
Title : CONTROLLER
Engineer:
ASUSTek Computer Inc.
Size A2
Project Name
20Q1 AM4 1106 P8-2PH 1P1P-2P2P HSY
Rev 2.00
Date: Wednesday, April 15, 2020
Sheet 6 of 127

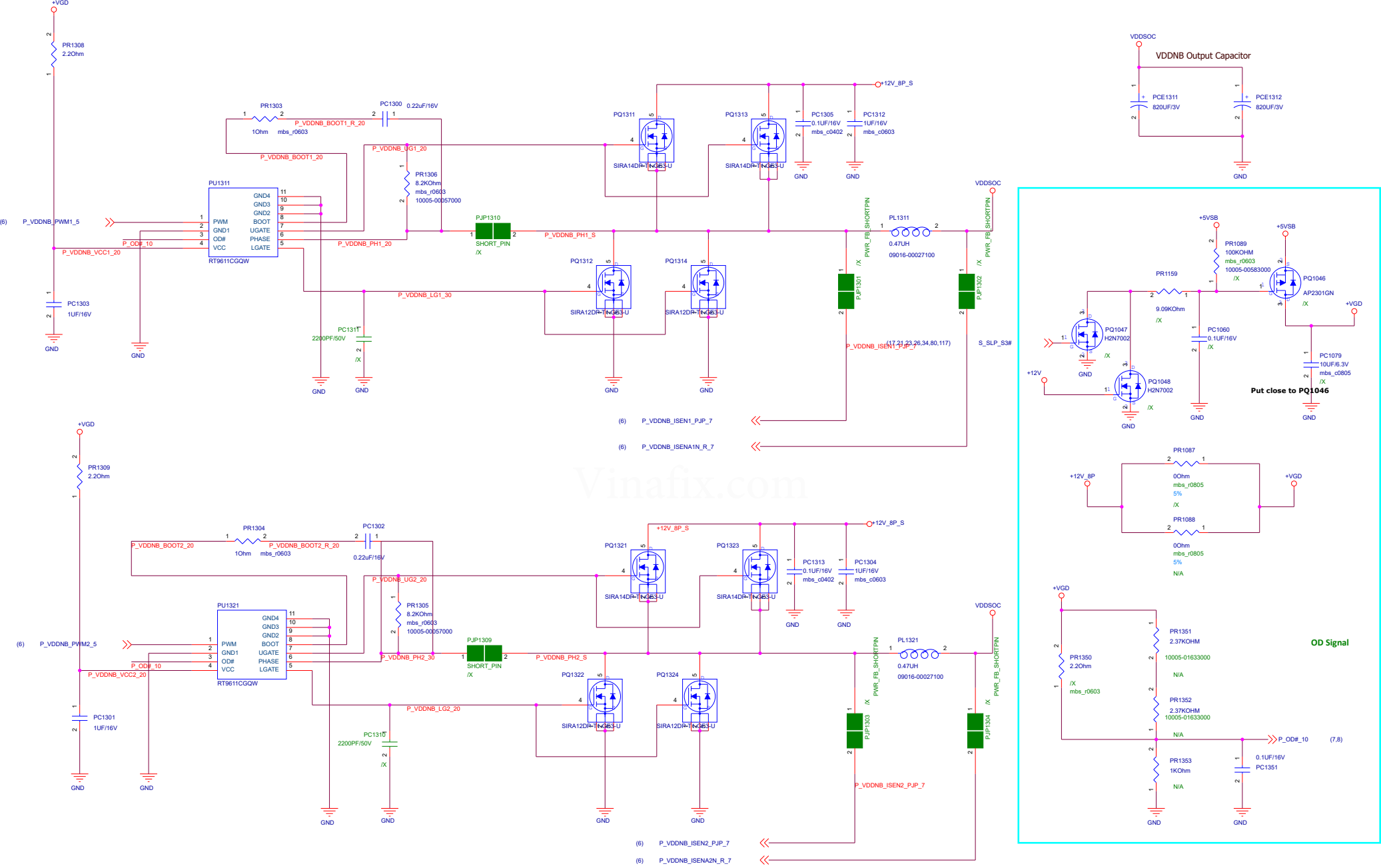
Title : VDDSOC Controller

ASUSTek Computer Inc.

Engineer:

Size	Project Name	Rev
A3	**20Q1 AM4 1106 P8-2PH 1P1P-2P2P HSY**	2.00

Date:	Tuesday, March 03, 2020	Sheet	9	of	127


VDDNB Output Capacitor
Put close to PQ1046
OD Signal
Title : DRIVER
Engineer:
ASUSTek Computer Inc.
Size A3
Project Name 20Q1 AM4 1106 P8-2PH 1P1P-2P2P HSY
Rev 2.00
Date: Thursday, March 05, 2020
Sheet 10 of 127

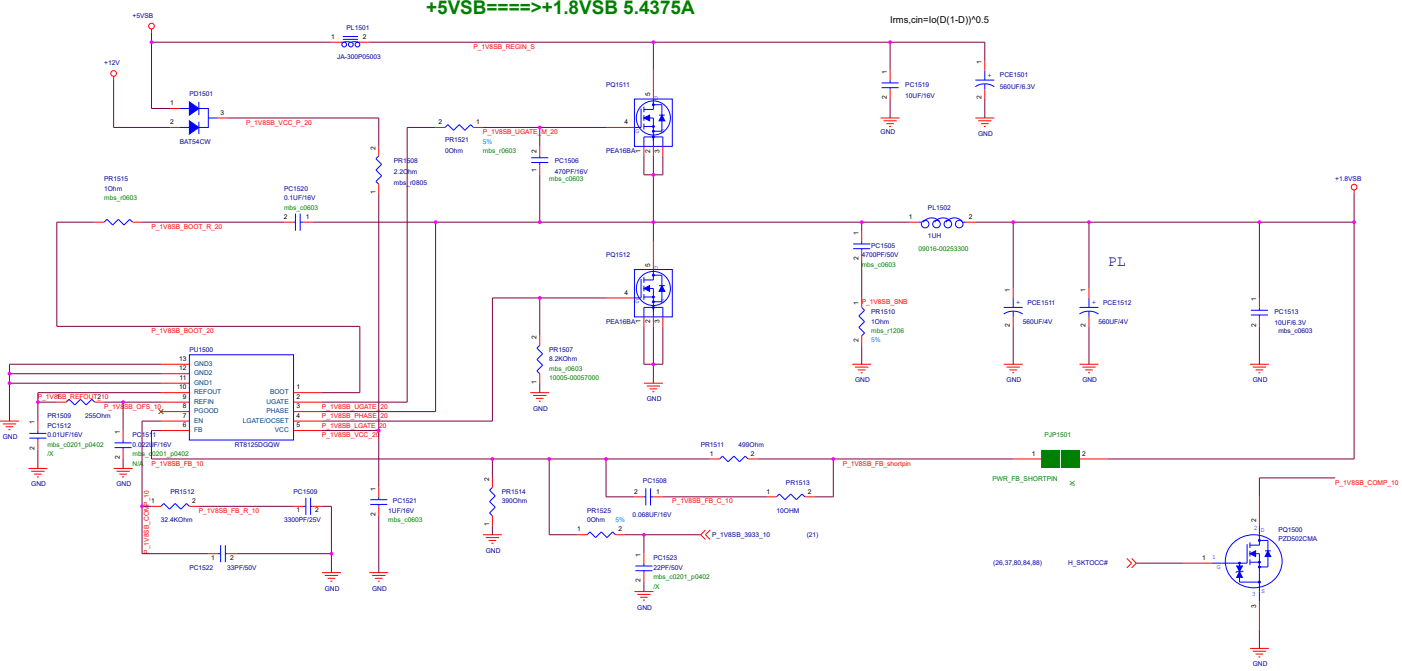
Title : VDDSOCSB

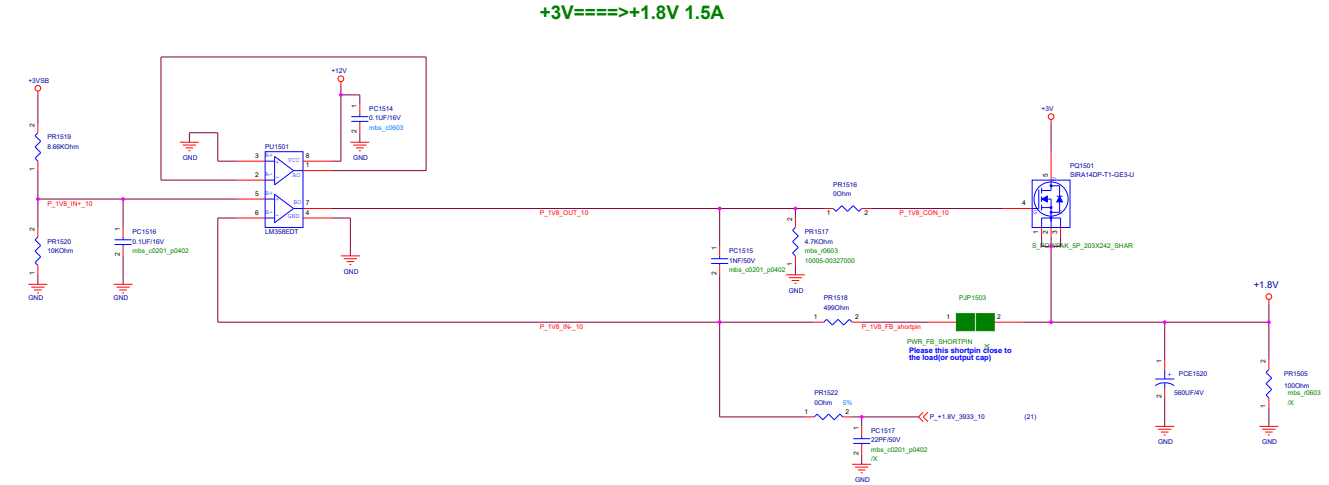
ASUSTek Computer Inc.

Engineer:

Size	Project Name	Rev
A2	**AM4**	1.00

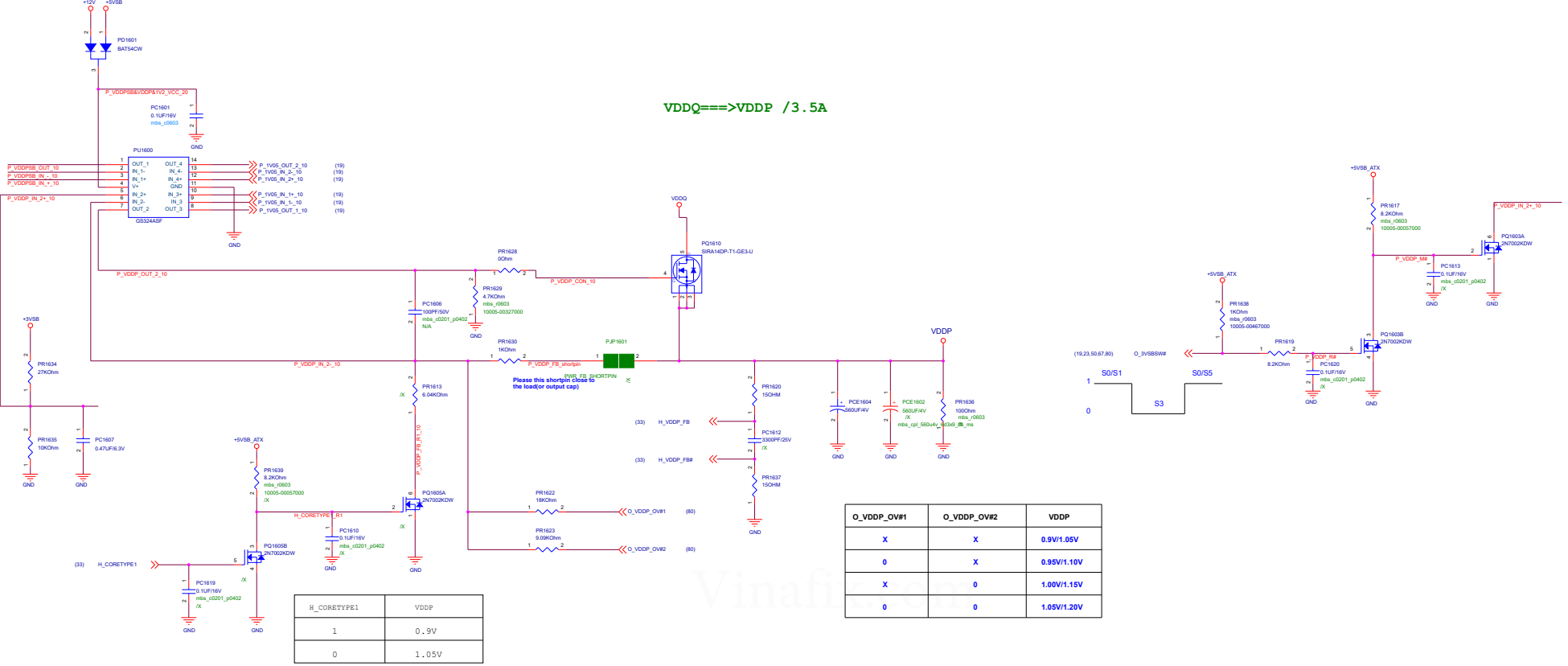
Date:	Tuesday, March 03, 2020	Sheet	11	of	127





ASUSTek Computer Inc.	Title : +1.8VSB&+1.8V	
	Engineer:	
Size: A2	Project Name: AM4	Rev: 1.00
Date: Thursday, March 05, 2020	Sheet 12 of 127	

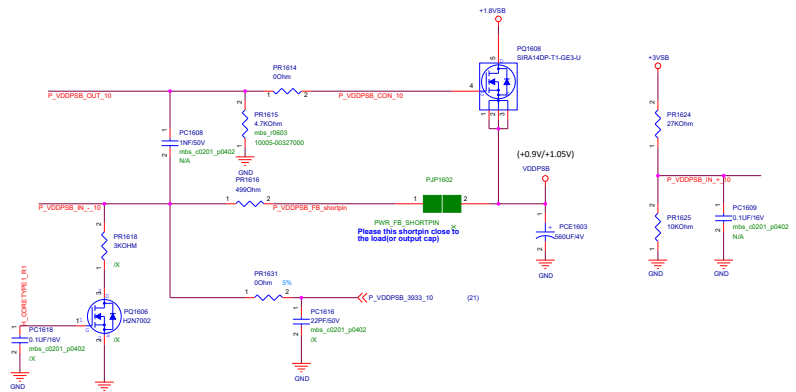
VDDQ===>VDDP /3.5A



H_CORETYPE1	VDDP
1	0.9V
0	1.05V

O_VDDP_OV#1	O_VDDP_OV#2	VDDP
X	X	0.9V/1.05V
0	X	0.95V/1.10V
X	0	1.00V/1.15V
0	0	1.05V/1.20V

+1.8VSB===>VDDPSB 1.65A(0.75A)



H_CORETYPE1	VDDPSB
1	0.9V
0	1.05V

ASUSTek Computer Inc.

Title : VDDP&VDDPSB

Engineer:

Size	Project Name	Rev
A2	AM4	1.00

Date: Thursday, March 05, 2020 Sheet 13 of 127

Title : NA

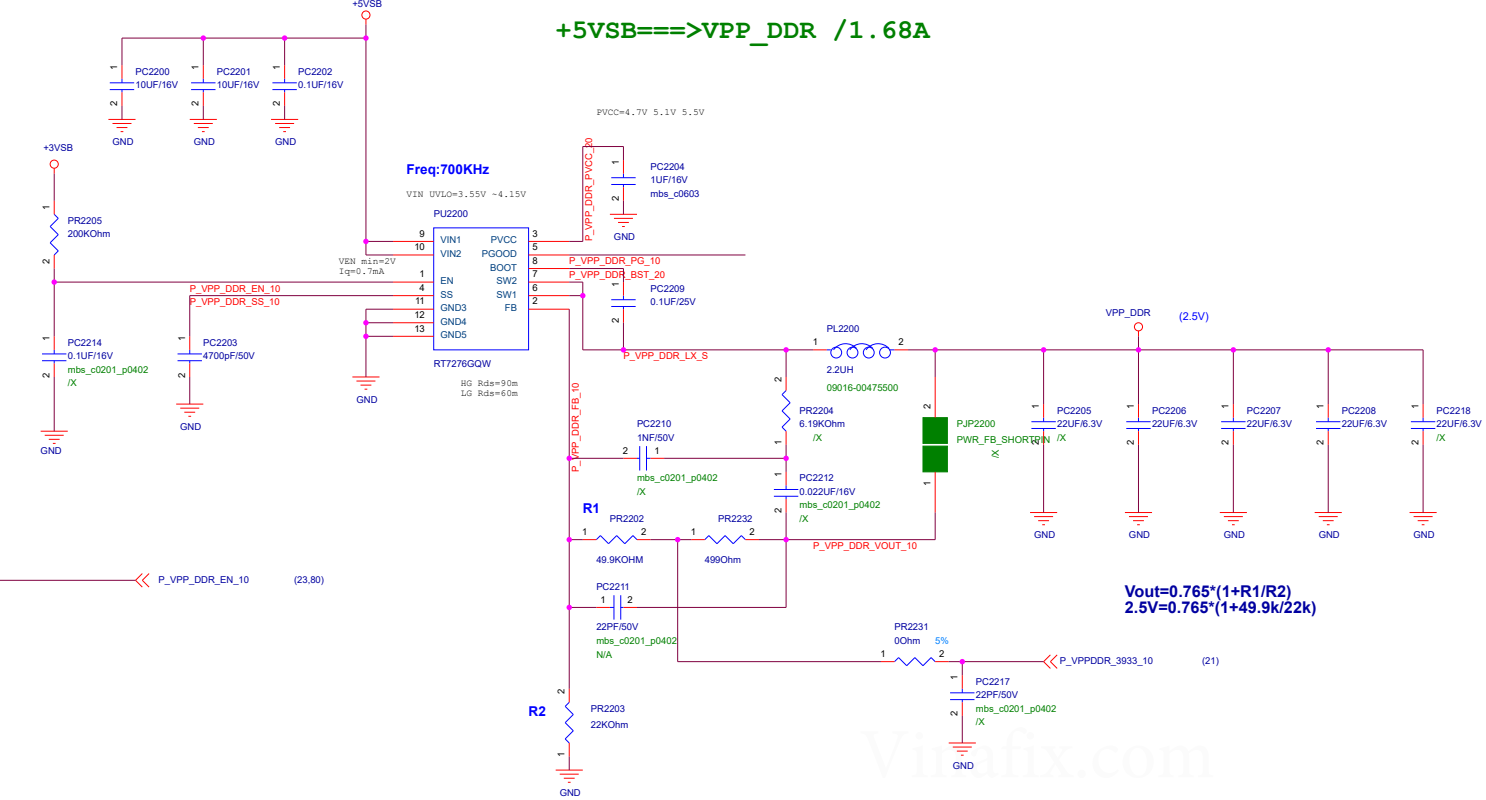
ASUSTek Computer Inc.

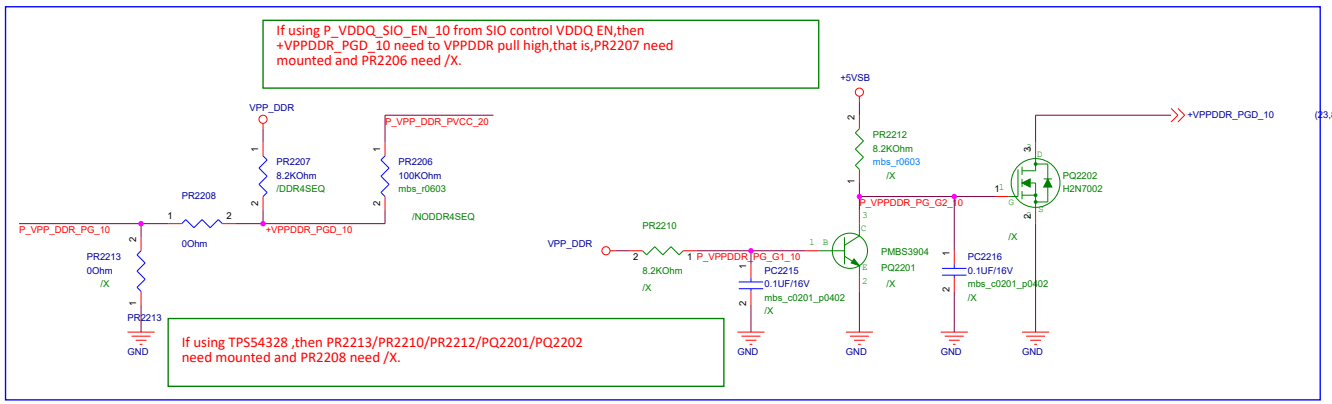
Engineer:

Size	Project Name	Rev
A2	**AM4**	1.00

Date:	Tuesday, March 03, 2020	Sheet	14	of	127

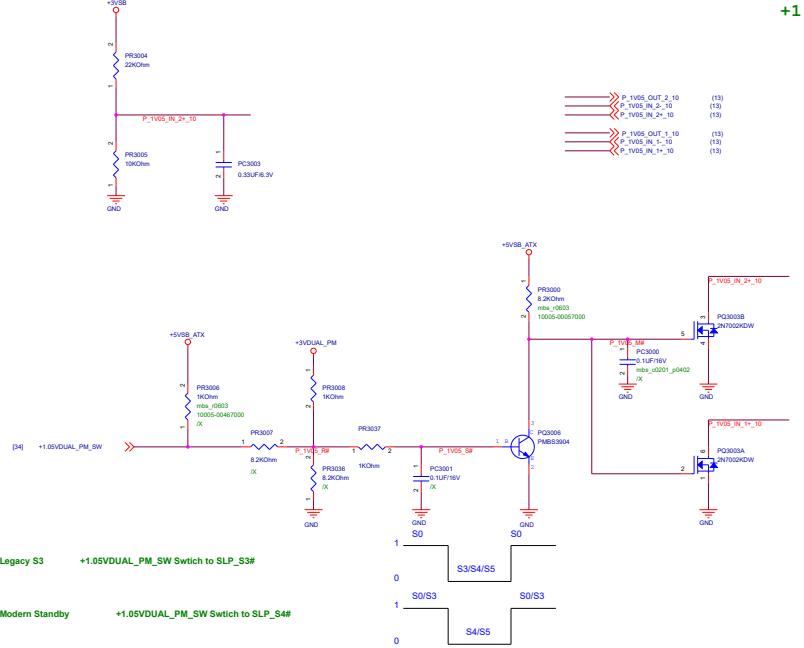
+5VSB===>VPP_DDR /1.68A

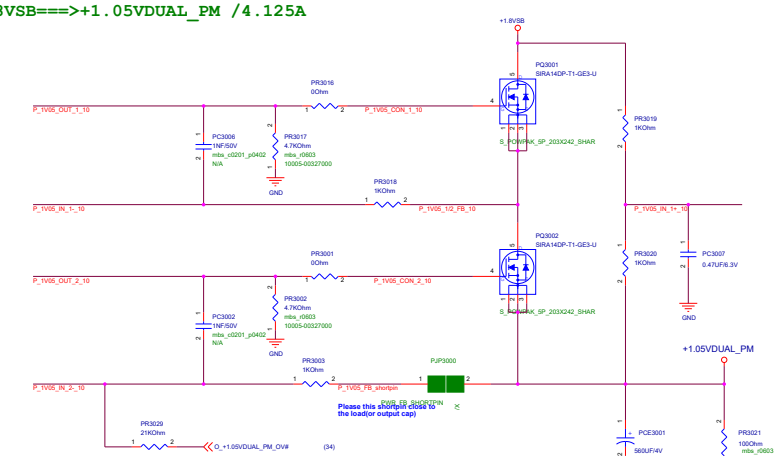




ASUSTek Computer Inc.	Title : VPP_DDR	
	Engineer:	
Size: A3	Project Name: AM4	Rev: 1.00
Date: Thursday, March 05, 2020	Sheet 18 of 127	

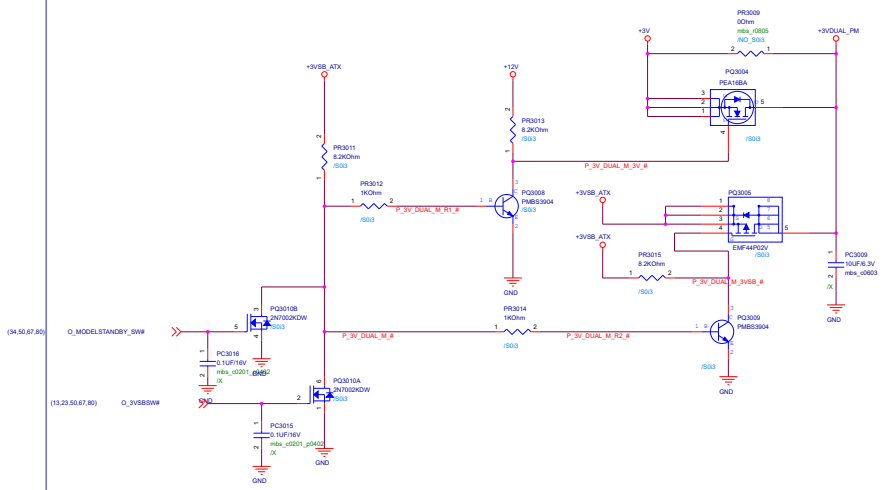
+1.8VSB===>+1.05VDUAL_PM /4.125A



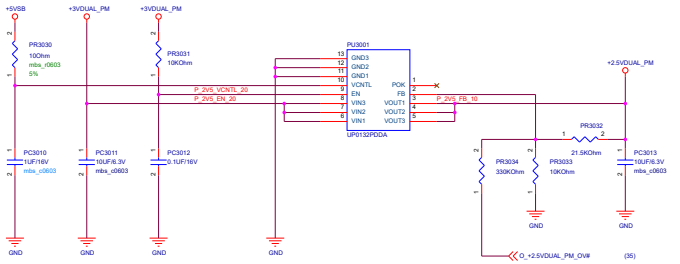


O_+1.05VDUAL_PM_OV#	+1.05VDUAL_PM
X	1.05V
0	1.10V

+3VDUAL_PM VOLTAGE SWITCH & POWER CIRCUIT 0.825A



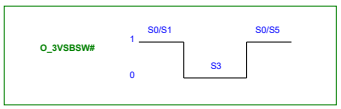
+3VDUAL_PM====>+2.5VDUAL_PM 0.675A



O_+2.5VDUAL_PM_OV#	+2.5V
X	2.50V
0	2.55V

Legacy S3 O_MODELSTANDBY_SW# H

Modern Standby O_MODELSTANDBY_SW# L



ASUSTek Computer Inc.

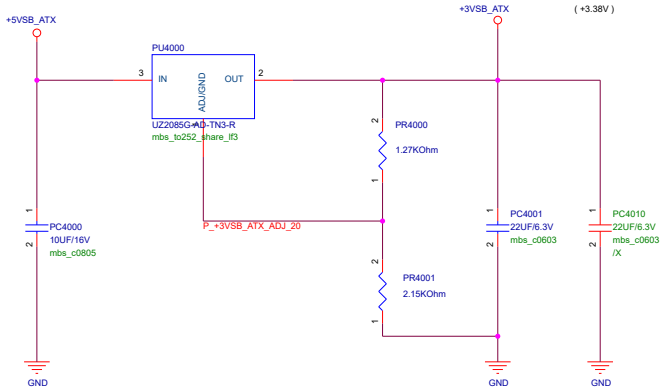
Title : +1.2V_PM & +1.0V_PM

Engineer:

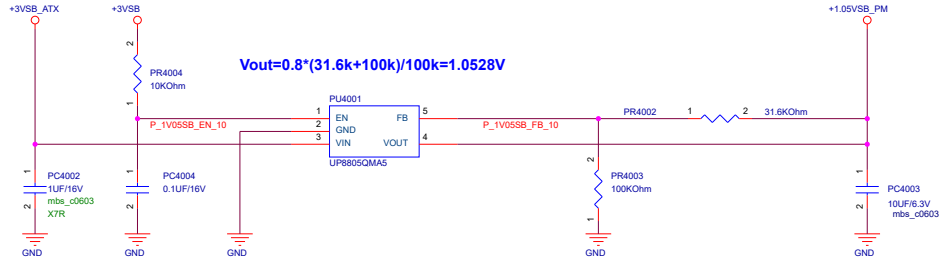
Size	Project Name	Rev
A2	AM4	1.00

Date: Thursday, April 09, 2020 Sheet 19 of 127

+5VSB_ATX ====>+3VSB_ATX_LDO 0.35A

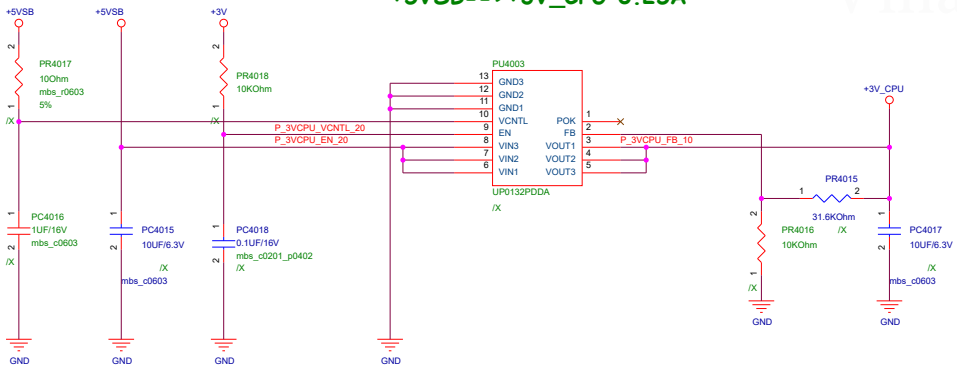


+3VSB_ATX ====>+1.05VSB_PM 50mA

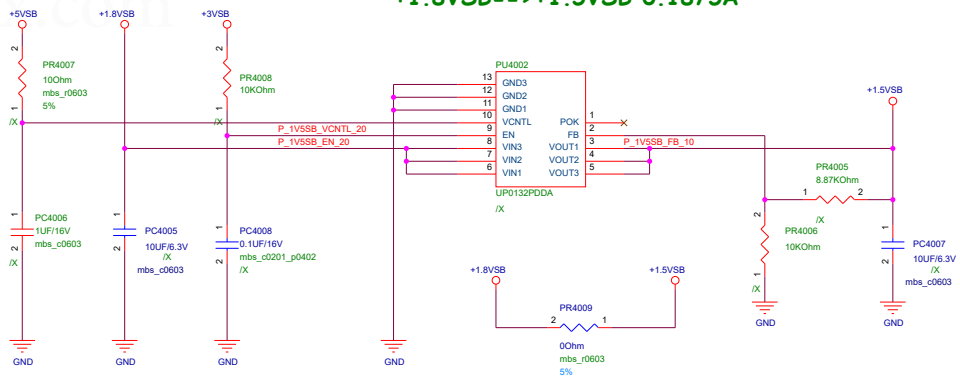


Power Component place near each other!

+5VSB==>+3V_CPU 0.25A



+1.8VSB==>+1.5VSB 0.1875A



ASUSTek Computer Inc.	Title : SBATX&1.0VSB_PM&1.5VSB	
	Engineer:	
Size: A3	Project Name: AM4	Rev: 1.00
Date: Tuesday, March 03, 2020	Sheet 20 of 127	

NOTE:which power rail powerd to audio ic should be confirmed by EE.

1.Vin and Vout keep more than 30mils away.

2.Input cap and Output cap can't use same GND.

3.P_5VSB_GATE_10 is away from Vin more than 15mils ,from Vout more than 30mils.

If OVP protection circuit isn't mounted,then PC4500 and PC4501 aren't also mounted.

FOR O_PWROK

S0

1

0

DS5/S5/S4/S3 DS5/S5/S4/S3

FOR O_DEEP_S5

DS5

1

0

S5/S4/S3/S0 S5/S4/S3/S0

Note:

P_5VSB_GATE_10 is about 15mil or more distance apart from other power rail.

Note:

PC4501靠近PQ4505放置

Inrush circuit is available as matching UVP circuit.

S5 ----> S0 S0 ----> S3

P_5VSB_USB_GATE_10

P_5VSB_USB_GATE_10_1

S_SLP_A#

S_SLP_S3#

+5V

S_PWROK

ITE: 150 ms

NCT: 300 ms

PR4530 and O1_5VSB_GATE# offpage can be deleted without SIO Control Sequence.

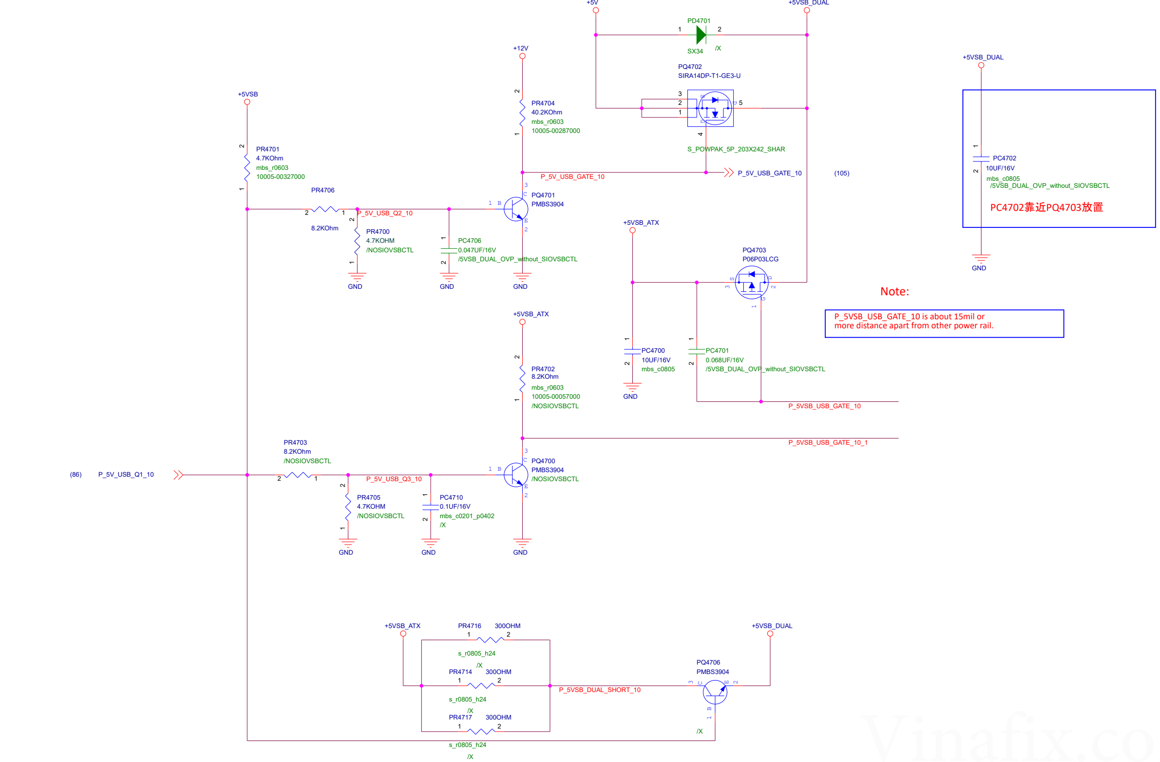
S_PWROK_SB

don't need for Flash Back

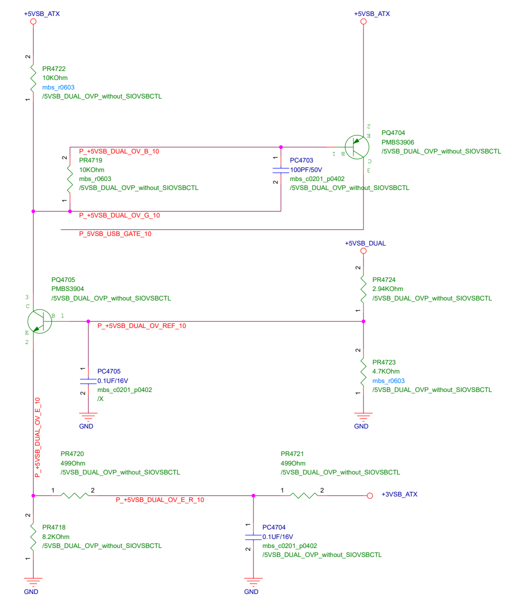
Address : 0x26

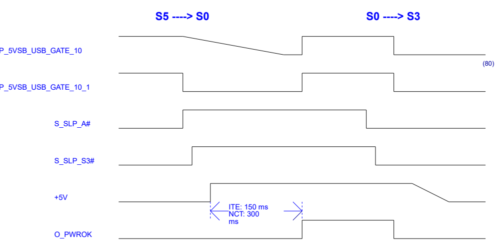
Address : 0x20

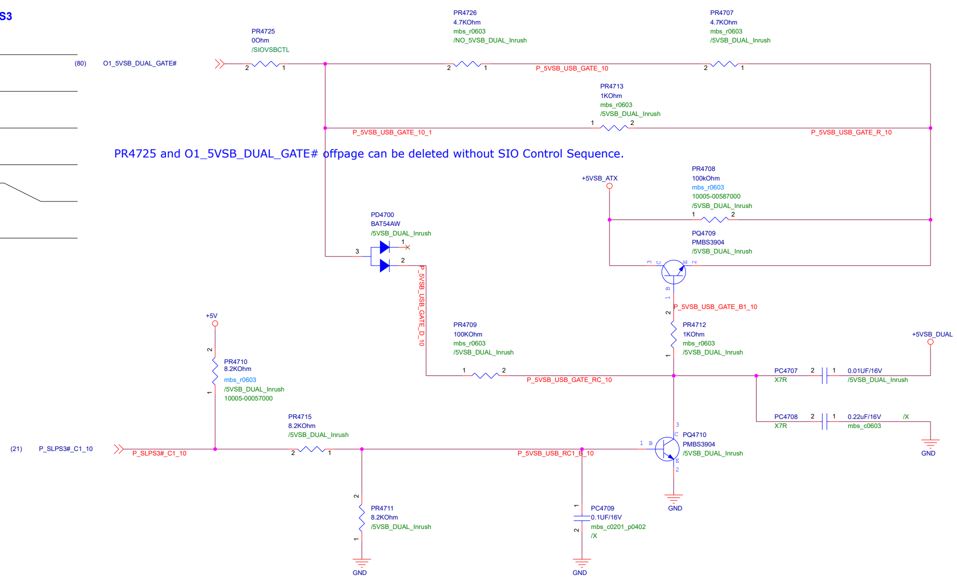
Title :	+5VSB&+5VSB Inrush
Engineer:	
ASUSTek Computer Inc.	
Size: A2	Project Name: AM4
Rev: 1.00	
Date: Thursday, March 05, 2020	Sheet 21 of 127


+5V
+5VSB_DUAL
PD4701
SX34
/X
PQ4702
SIRA14DP-T1-GE3-U
S_POWPAK_5P_203X242_SHAR
+12V
PR4704
40.2KOhm
mbs_r0603
10005-00287000
P_5V_USB_GATE_10
(105)
+5VSB
PR4701
4.7KOhm
mbs_r0603
10005-00327000
PR4706
8.2KOhm
P_5V_USB_Q2_10
PR4700
4.7KOHM
/NOSIOVSBCTL
PC4706
0.047UF/16V
/5VSB_DUAL_OVP_without_SIOVSBCTL
PQ4701
PMBS3904
+5VSB_ATX
PQ4703
P06P03LCG
+5VSB_DUAL
PC4702
10UF/16V
mbs_c0805
/5VSB_DUAL_OVP_without_SIOVSBCTL
PC4702靠近PQ4703放置
Note:
P_5VSB_USB_GATE_10 is about 15mil or more distance apart from other power rail.
PC4700
10UF/16V
mbs_c0805
PC4701
0.068UF/16V
/5VSB_DUAL_OVP_without_SIOVSBCTL
PR4702
8.2KOhm
mbs_r0603
10005-00057000
/NOSIOVSBCTL
P_5VSB_USB_GATE_10
P_5VSB_USB_GATE_10_1
(86) P_5V_USB_Q1_10
PR4703
8.2KOhm
/NOSIOVSBCTL
P_5V_USB_Q3_10
PQ4700
PMBS3904
/NOSIOVSBCTL
PR4705
4.7KOHM
/NOSIOVSBCTL
PC4710
0.1UF/16V
mbs_c0201_p0402
/X
+5VSB_ATX
PR4716 300OHM
s_r0805_h24
/X
PR4714 300OHM
PR4717 300OHM
P_5VSB_DUAL_SHORT_10
PQ4706
PMBS3904
GND

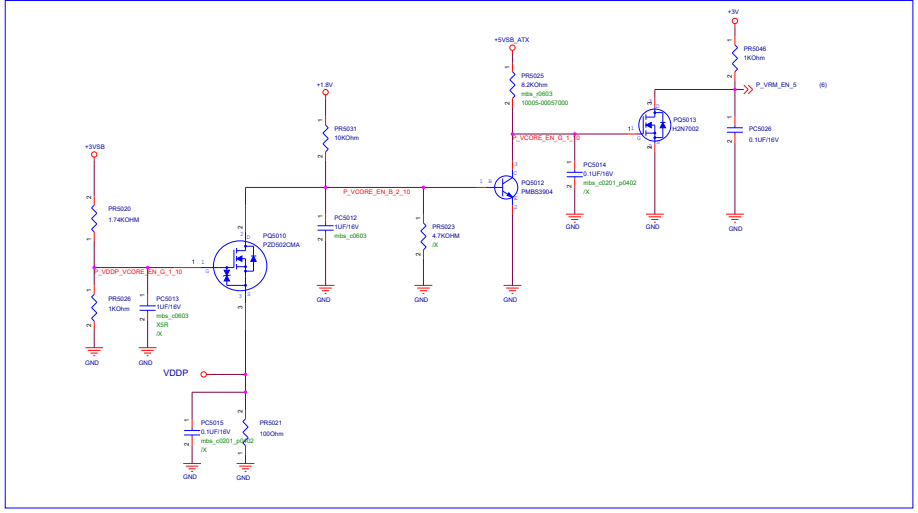
BOM	主板上+5VSB_DUAL上有接不耐12V高壓的元件且上件，例如用在Type-C上的Power Switch G517 06016-01100500	主板上+5VSB_DUAL上沒有接不耐12V高壓的元件或者主板上+5VSB_DUAL上有接不耐12V高壓的元件但不上件
/5VSB_DUAL_OVP	mount	unmount

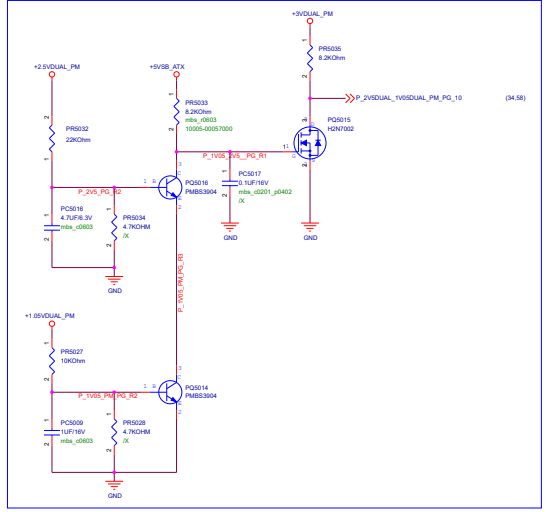

+5VSB_ATX
PR4722
10KOhm
mbs_r0603
/5VSB_DUAL_OVP_without_SIOVSBCTL
PQ4704
PMBS3906
P_+5VSB_DUAL_OV_B_10
PR4719
10KOhm
PC4703
100PF/50V
mbs_c0201_p0402
P_+5VSB_DUAL_OV_G_10
P_5VSB_USB_GATE_10
+5VSB_DUAL
PQ4705
PMBS3904
PR4724
2.94KOhm
P_+5VSB_DUAL_OV_REF_10
PC4705
0.1UF/16V
PR4723
4.7KOhm
PR4720
499Ohm
PR4721
499Ohm
P_+5VSB_DUAL_OV_E_R_10
+3VSB_ATX
PR4718
8.2KOhm
PC4704
0.1UF/16V
GND

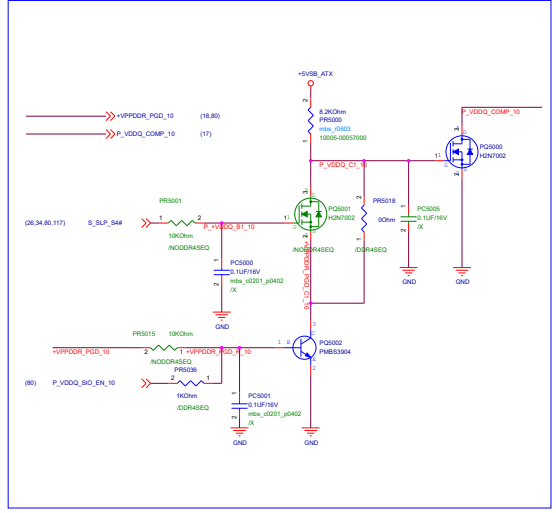


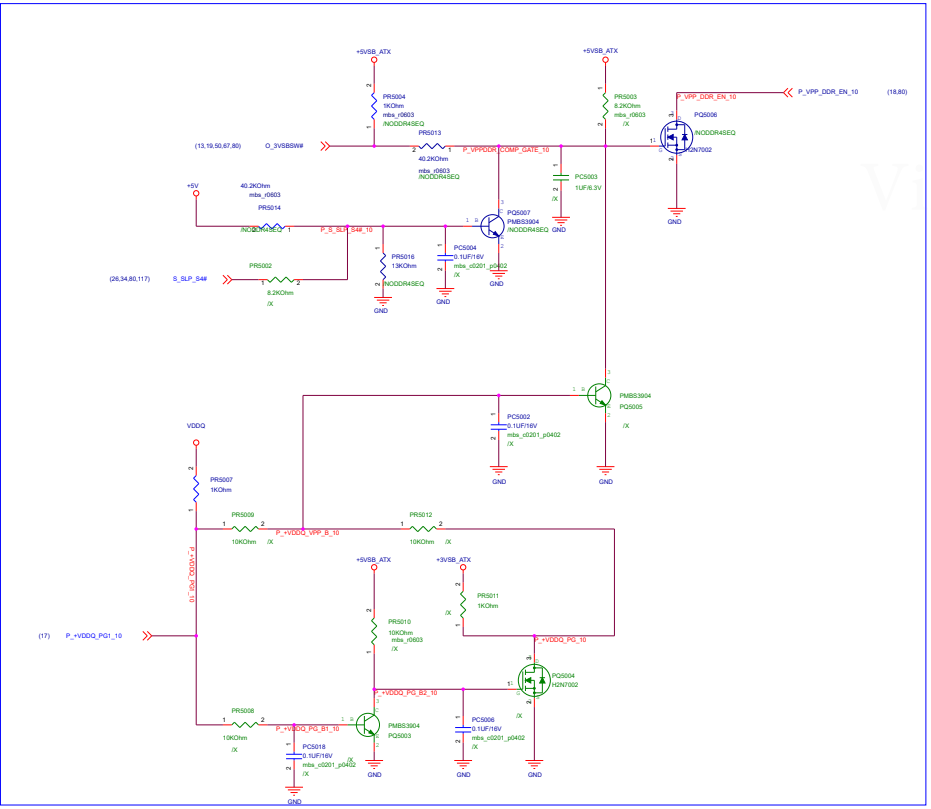

(80) O1_5VSB_DUAL_GATE#
PR4725
0Ohm
/SIOVSBCTL
PR4726
4.7KOhm
mbs_r0603
/NO_5VSB_DUAL_Inrush
PR4707
4.7KOhm
/5VSB_DUAL_Inrush
PR4713
1KOhm
P_5VSB_USB_GATE_R_10
PR4725 and O1_5VSB_DUAL_GATE# offpage can be deleted without SIO Control Sequence.
PR4708
100kOhm
10005-00587000
PD4700
BAT54AW
PQ4709
PMBS3904
PR4709
100KOhm
P_5VSB_USB_GATE_RC_10
P_5VSB_USB_GATE_B1_10
PR4712
1KOhm
PC4707 X7R 0.01UF/16V
PC4708 X7R 0.22uF/16V
PR4710
8.2KOhm
10005-00057000
PR4715
8.2KOhm
(21) P_SLPS3#_C1_10
P_5VSB_USB_RC1_B_10
PQ4710
PMBS3904
PR4711
8.2KOhm
PC4709
0.1UF/16V
GND

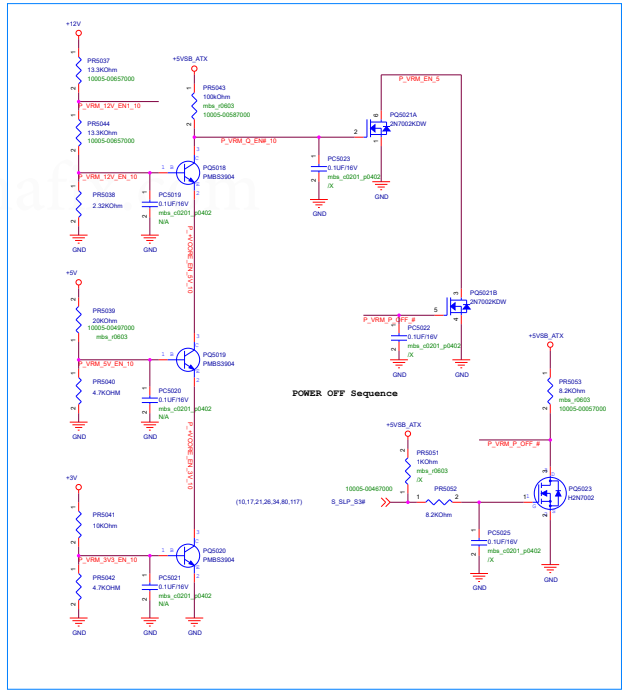
ASUS	Title : +5VSB_DUAL	
ASUSTek Computer Inc.	Engineer:	
Size: A2	Project Name: AM4	Rev: 1.00
Date: Thursday, March 05, 2020	Sheet 22 of 127	

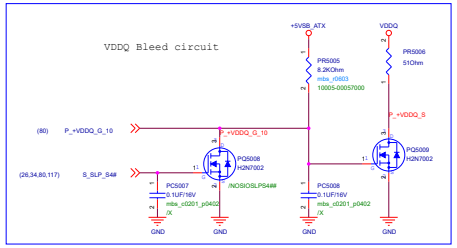












ASUSTeK Computer Inc.	Title :	
	Engineer:	
Size: A2	Project Name	Rev
Date: Thursday, March 05, 2020	Sheet 23 of 127	

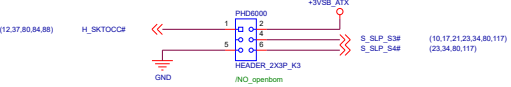
Title : NA

ASUSTek Computer Inc.

Engineer:

Size	Project Name	Rev
A3	**AM4**	1.00

Date: Tuesday, March 03, 2020



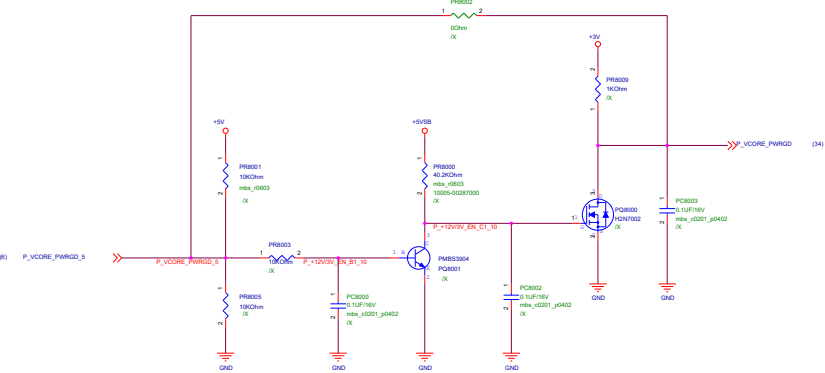
ASUSTek Computer Inc.

Title : NA

Engineer:

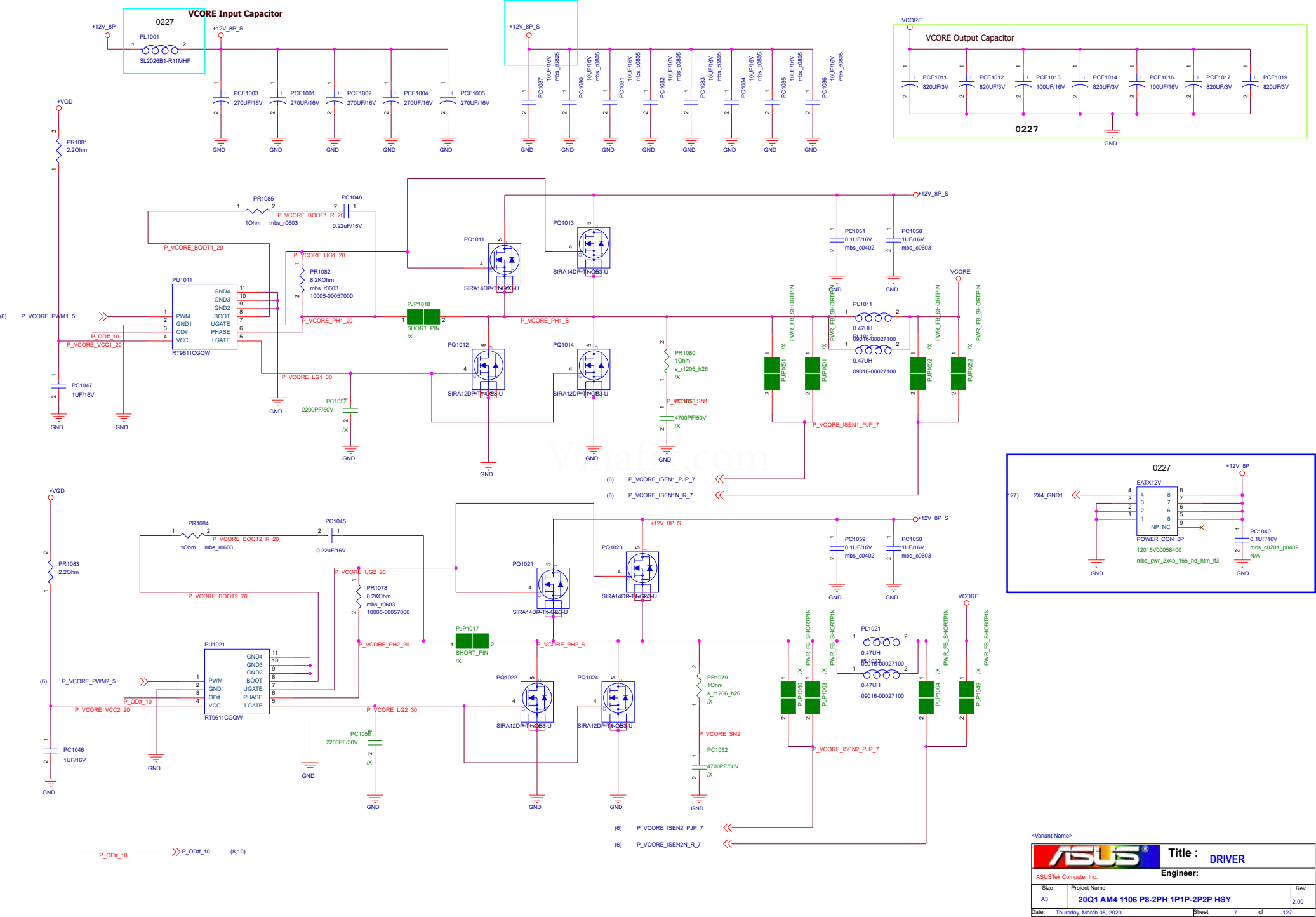
Size	Project Name	Rev
A2	AM4	1.00

Date: Thursday, March 05, 2020 Sheet 26 of 127



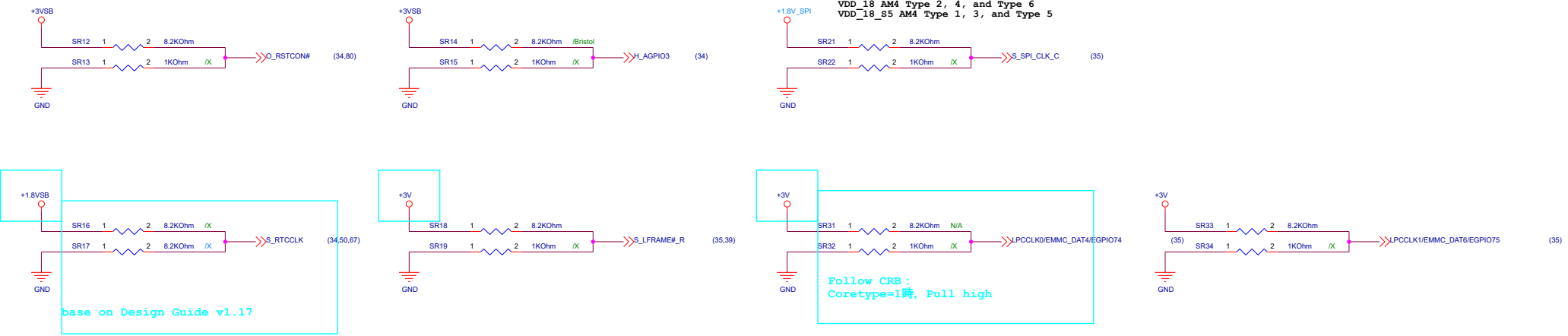
ASUSTek Computer Inc.	Title : VCORE PWRGD Glitch		
	Engineer:		
Size: C	Project Name: AM4		Rev: 1.00
Date: Thursday, March 05, 2020	Sheet 28 of 127		

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 03, 2020	Sheet 29 of 127	



<Variant Name>

ASUSTek Computer Inc.	Title : DRIVER	
	Engineer:	
Size: A3	Project Name: 20Q1 AM4 1106 P8-2PH 1P1P-2P2P HSY	Rev: 2.00
Date: Thursday, March 05, 2020	Sheet 7 of 127	



PIN	SPI_CLK	LFRAME_L	LPCCLK0		RTCCLK		AGPIO3
NET	S_SPI_CLK_C	S_LFRAME#_R	LPCCLK0/EMMC_DAT4/EGPIO74		S_RTCCLK		H_AGPIO3
CPU TYPE	1,2,3,4,5,6	0,2,4,6	4,6	0	4,6	0	0
Pull High	Configured for internal clock-generator Default	SPI ROM Default	32MB ROM: PSP should modify SPI page register bits[25:24] to remap physical ROM to upper image Default	Boot Fail Timer Enabled		RTC Coin Battery is implemented Default	Enhanced Reset logic for faster resume from S5 Default
Pull Low	Reserved	LPC ROM	<=16MB ROM: PSP should not modify SPI page register bits [25:24]	Boot Fail Timer Disabled Default	pull-down resistor (DNI) to VSS Default	RTC Coin Battery is not implemented	Traditional Reset logic

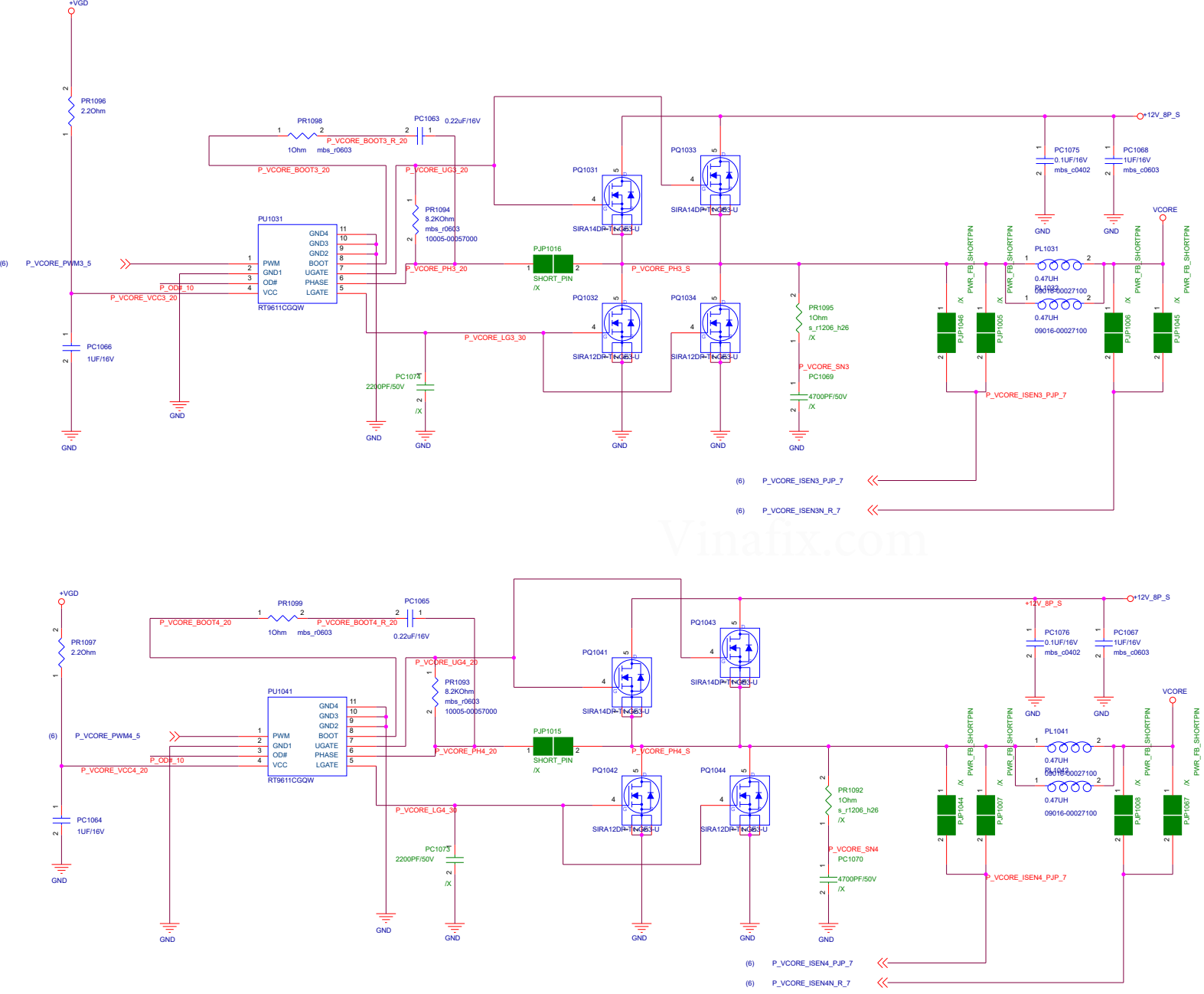
ASUSTek Computer Inc.

Title : <Title>

Engineer: ElaineIx_Li

Size	Project Name	Rev
A3	AM4	0.01

Date: Thursday, March 05, 2020 Sheet 38 of 127



<Variant Name>

ASUSTek Computer Inc.

Title : DRIVER

Engineer:

Size	Project Name	Rev
A3	20Q1 AM4 1106 P8-2PH 1P1P-2P2P HSY	2.00

Date: Thursday, March 05, 2020 Sheet 8 of 127

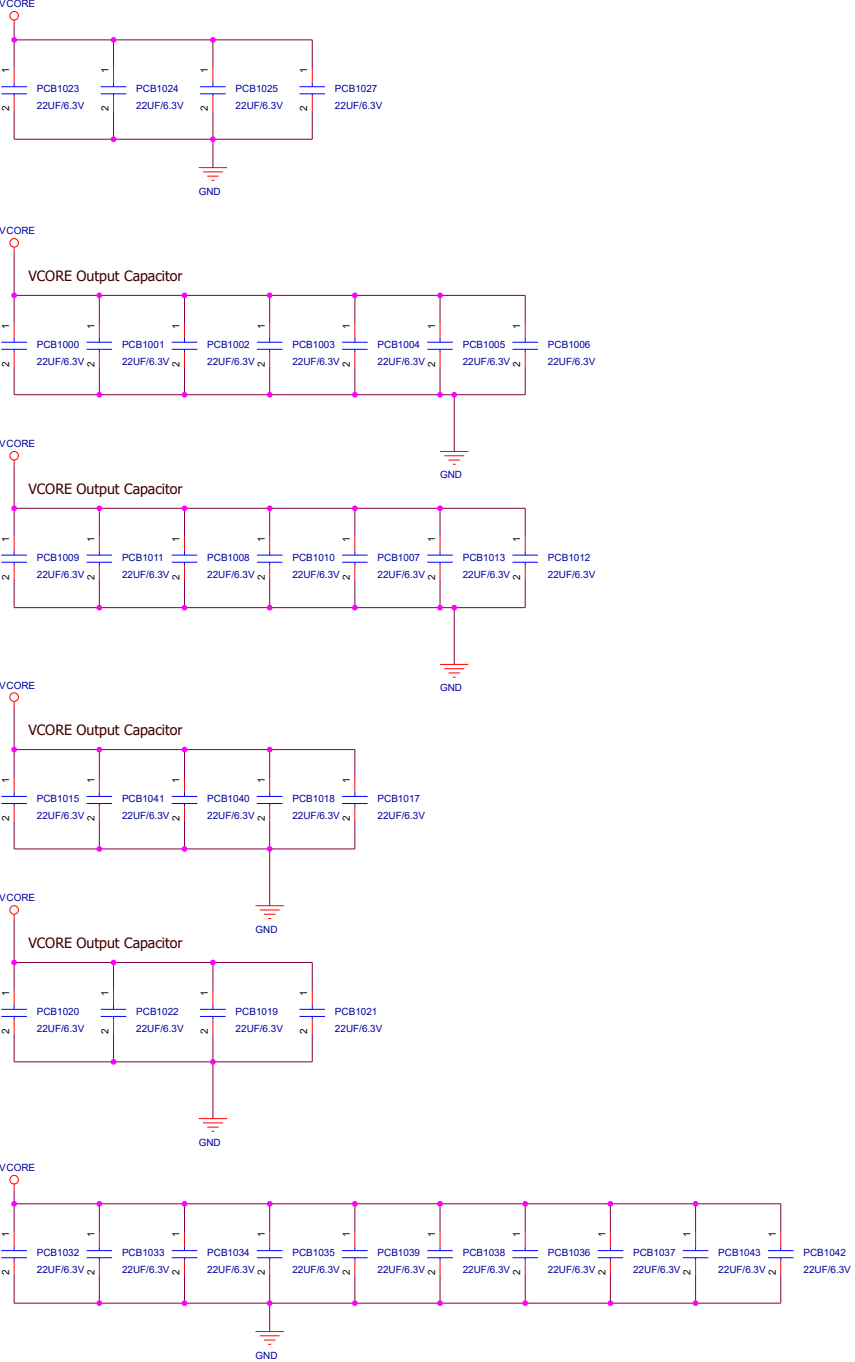
Title : NA

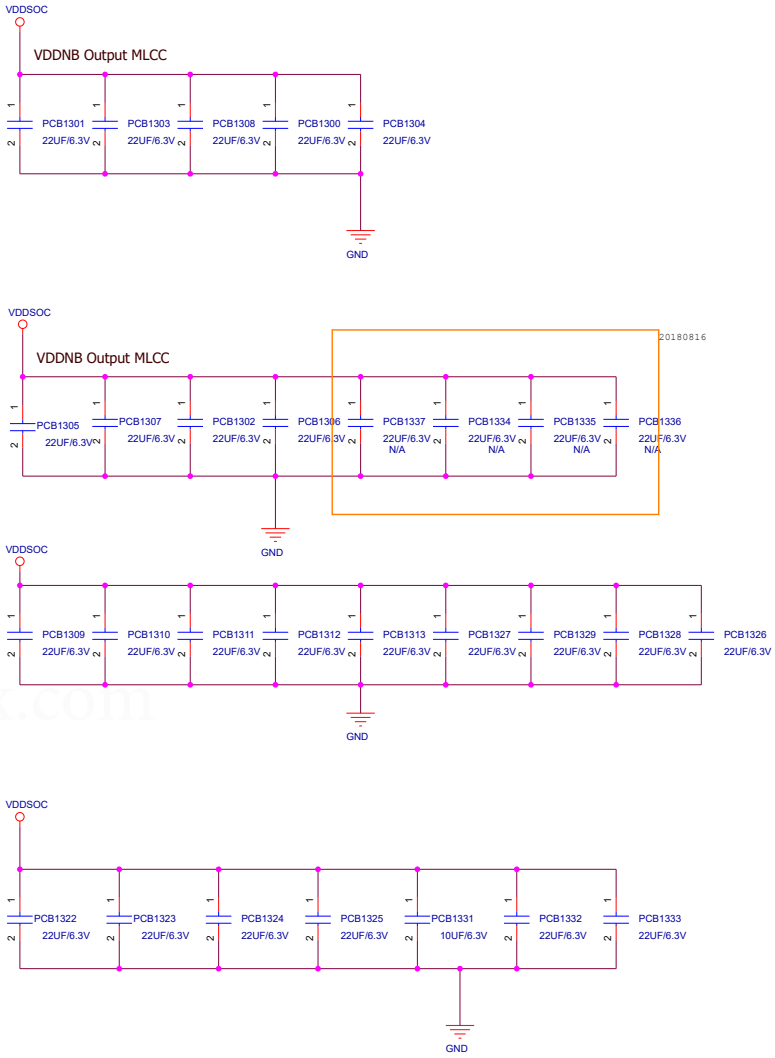
ASUSTek Computer Inc.

Engineer:

Size	Project Name	Rev
A3	**AM4**	1.00

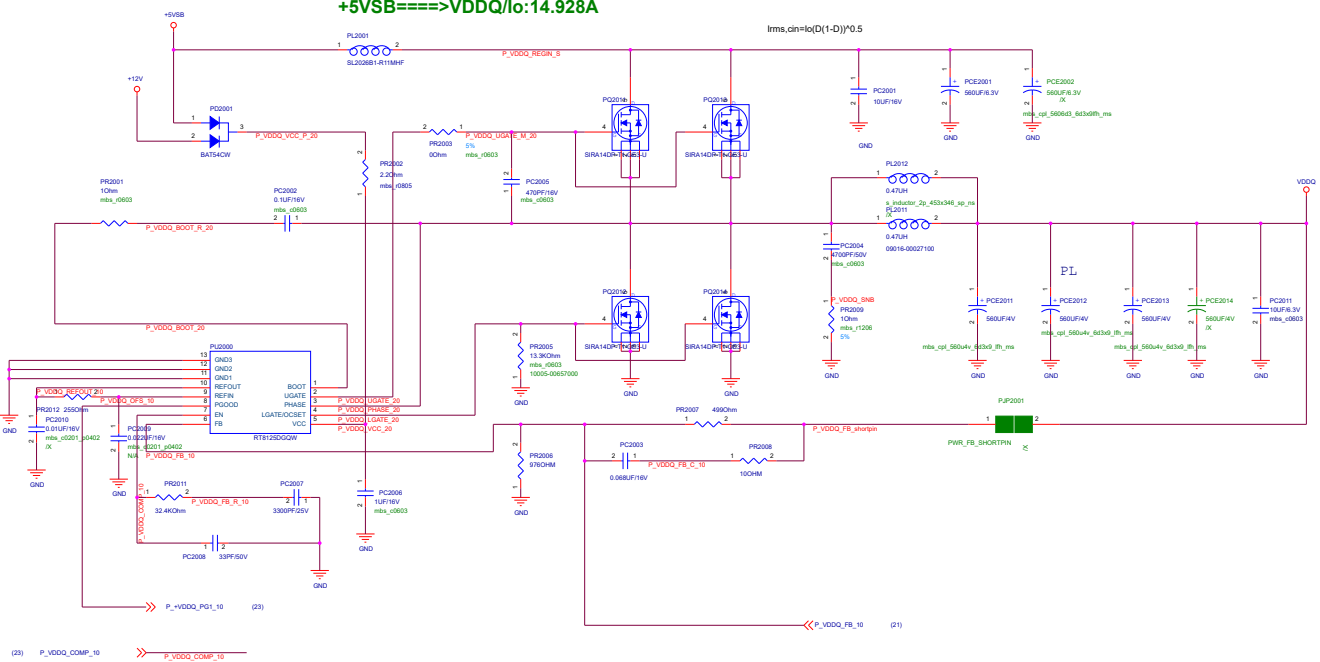
Date:	Tuesday, March 03, 2020	Sheet	15	of	127



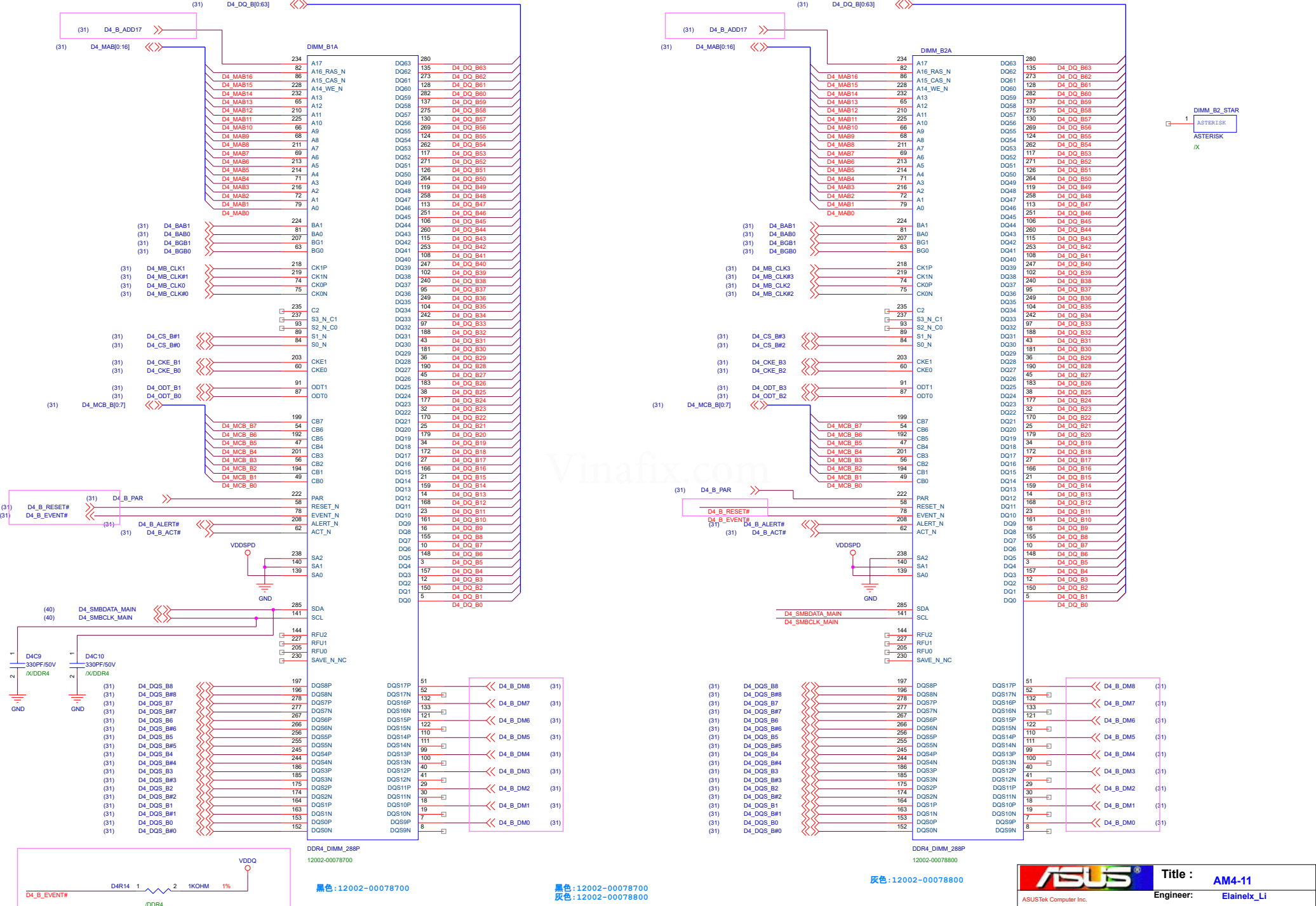


<Variant Name>

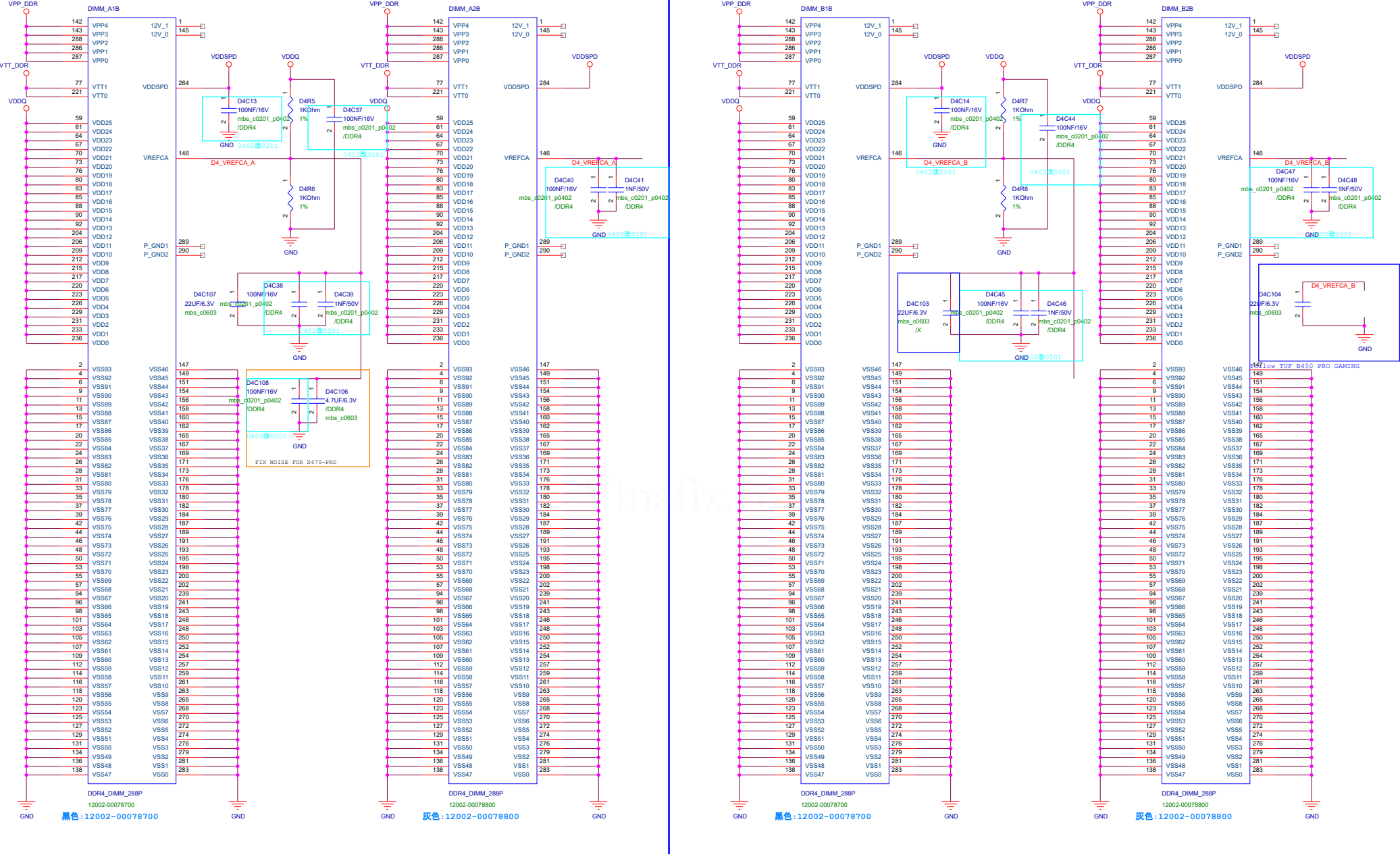
ASUSTek Computer Inc.	Title : Socket MLCC Engineer:	
Size: A3	Project Name: 20Q1 AM4 1106 P8-2PH 1P1P-2P2P HSY	Rev: 2.00
Date: Tuesday, March 03, 2020	Sheet 16 of 127	



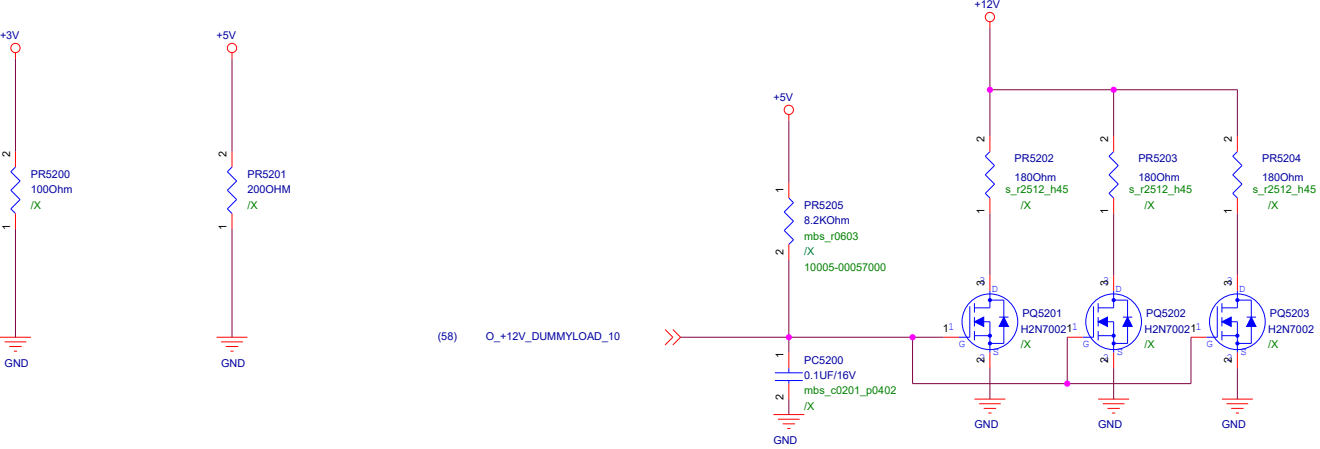
ASUSTek Computer Inc.	Title : VDDQ&VTT_DDR		
	Engineer:		
Size: A2	Project Name: AM4		Rev: 1.00
Date: Thursday, March 05, 2020	Sheet 17 of 127		



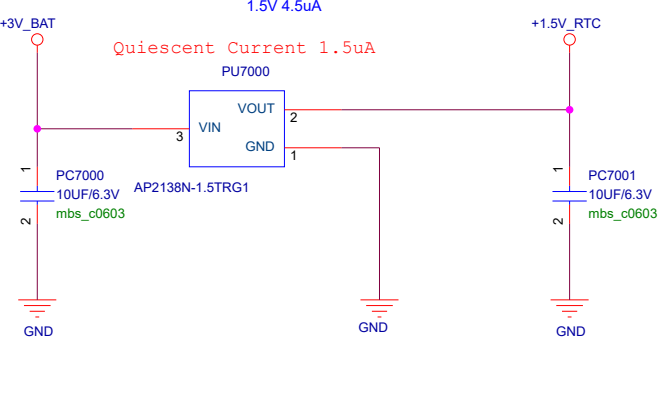
ASUSTek Computer Inc.	Title :	AM4-11	
	Engineer:	Elainelx_Li	
Size: A3	Project Name: AM4		Rev: 0.01
Date: Thursday, March 05, 2020	Sheet 41 of 127		



ASUSTek Computer Inc.	Title : AM4-12		
	Engineer: Elainelx_Li		
Size: A3	Project Name: AM4		Rev: 0.01
Date: Tuesday, March 03, 2020	Sheet 42 of 127		

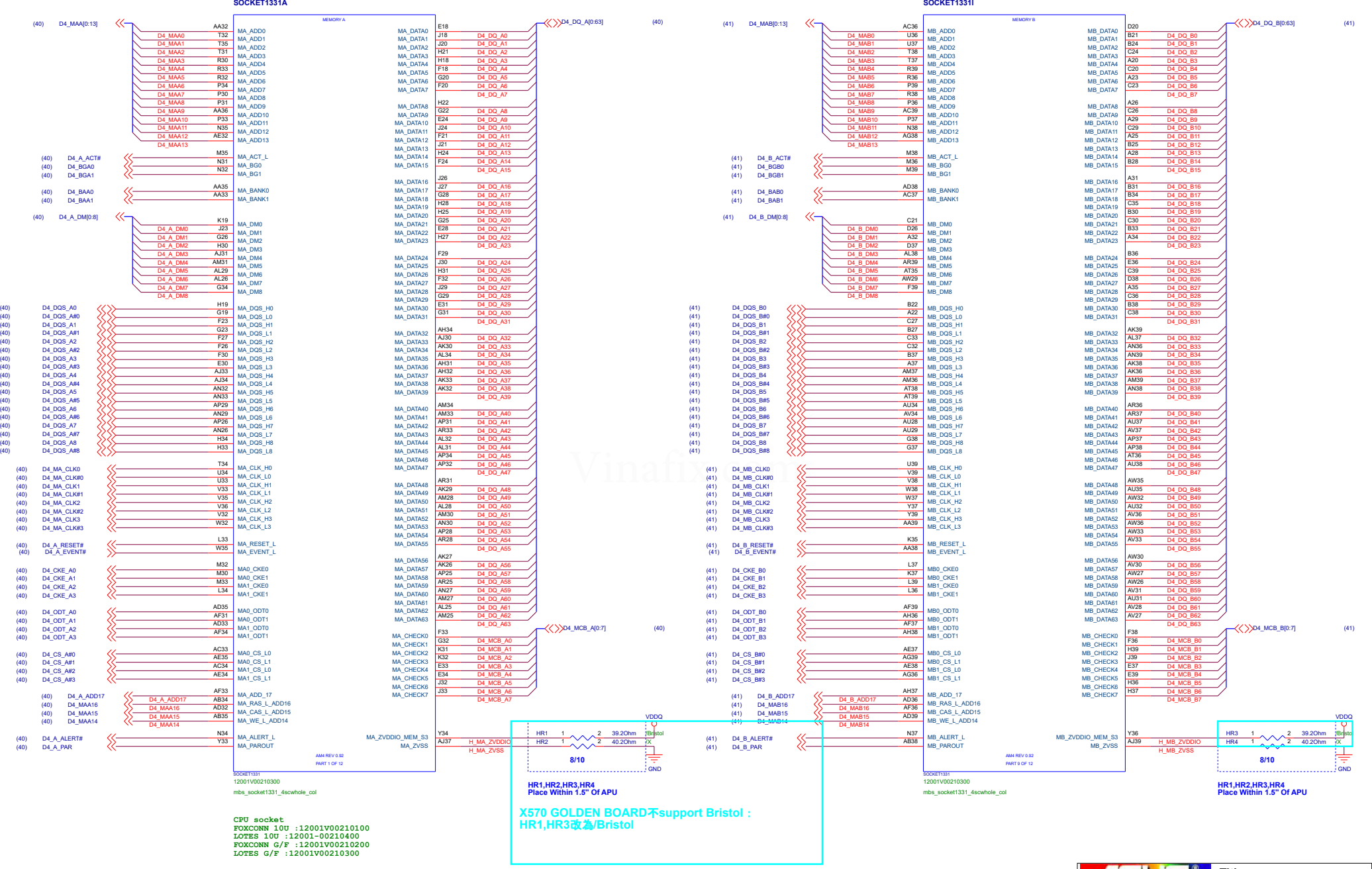


ASUSTek Computer Inc.	Title :	
	Engineer:	
Size: A3	Project Name	Rev
Date: Thursday, March 05, 2020	Sheet 25 of 127	



ASUSTek Computer Inc.	Title : +1.5V_RTC	
	Engineer:	
Size: A3	Project Name: AM4	Rev: 1.00
Date: Tuesday, March 03, 2020	Sheet 27 of 127	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 03, 2020	Sheet 30 of 127	

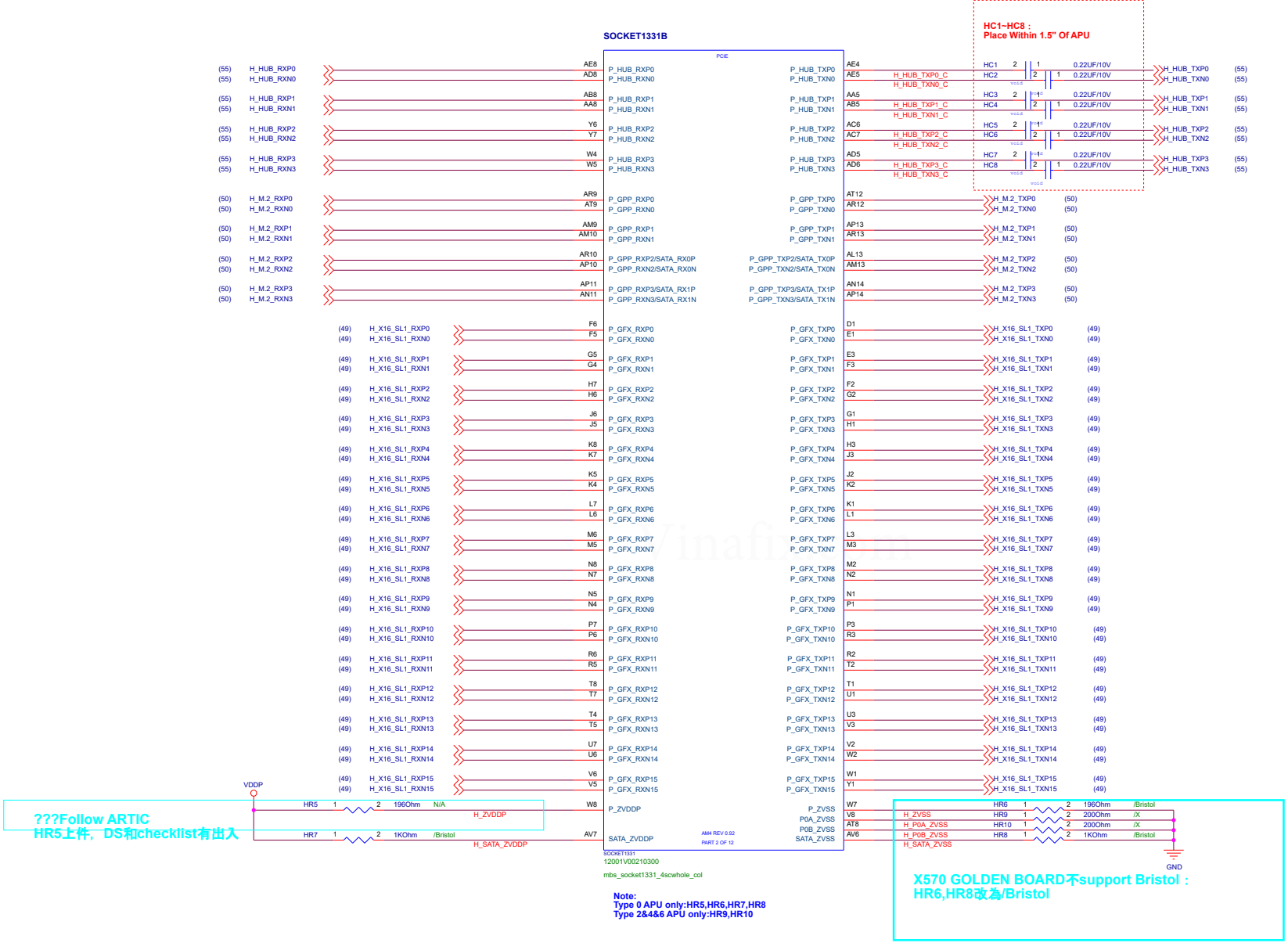


CPU socket
FOXCONN 10U :12001V00210100
LOTES 10U :12001-00210400
FOXCONN G/F :12001V00210200
LOTES G/F :12001V00210300

X570 GOLDEN BOARD不support Bristol :
HR1,HR3改為/Bristol

Note:
Type0 APU only:HR1,HR3

ASUSTek Computer Inc.	Title :	AM4-01	
	Engineer:	Elainelx_Li	
Size: A3	Project Name: AM4		Rev: 0.01
Date: Tuesday, April 07, 2020	Sheet 31 of 127		



		Type 0	Type 1	Type 2	Type 3	Type 4	Type 5	Type 6
GFX[15:0]	X16			V		V	V	V
	X8	V			V			
	X4		V					
GPP[3:0]	X4			V	V	V	V	V
	X2	V	V					

	CPU SSID INFO.
87E2H	AMD APU: AM4 socket1331 Vermeer
87E1H	AMD APU: AM4 socket1331 Renoir
87C0H	AMD CPU: MATISS MATISS
877CH	AMD APU: AMD APU AM4 PINNACLE APU,SOCKET1331
876BH	AMD APU: AMD APU AMD AM4 RAVEN APU,SOCKET1331

ASUSTek Computer Inc.

Title : AM4-02

Engineer: Elainelx_Li

Size	Project Name	Rev
A3	AM4	0.01

Date: Tuesday, April 07, 2020 Sheet 32 of 127

0719

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 03, 2020	Sheet 44 of 127	

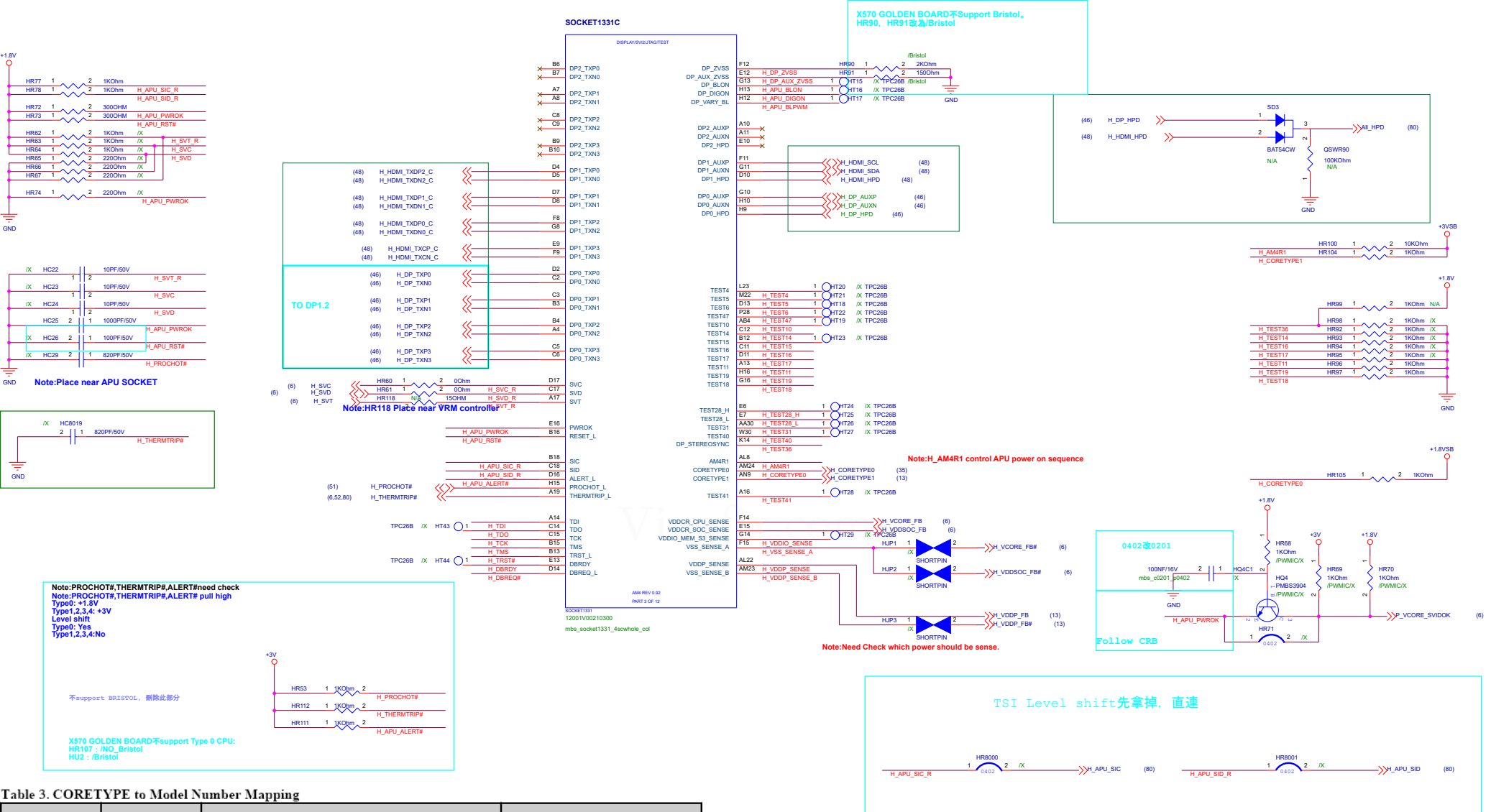
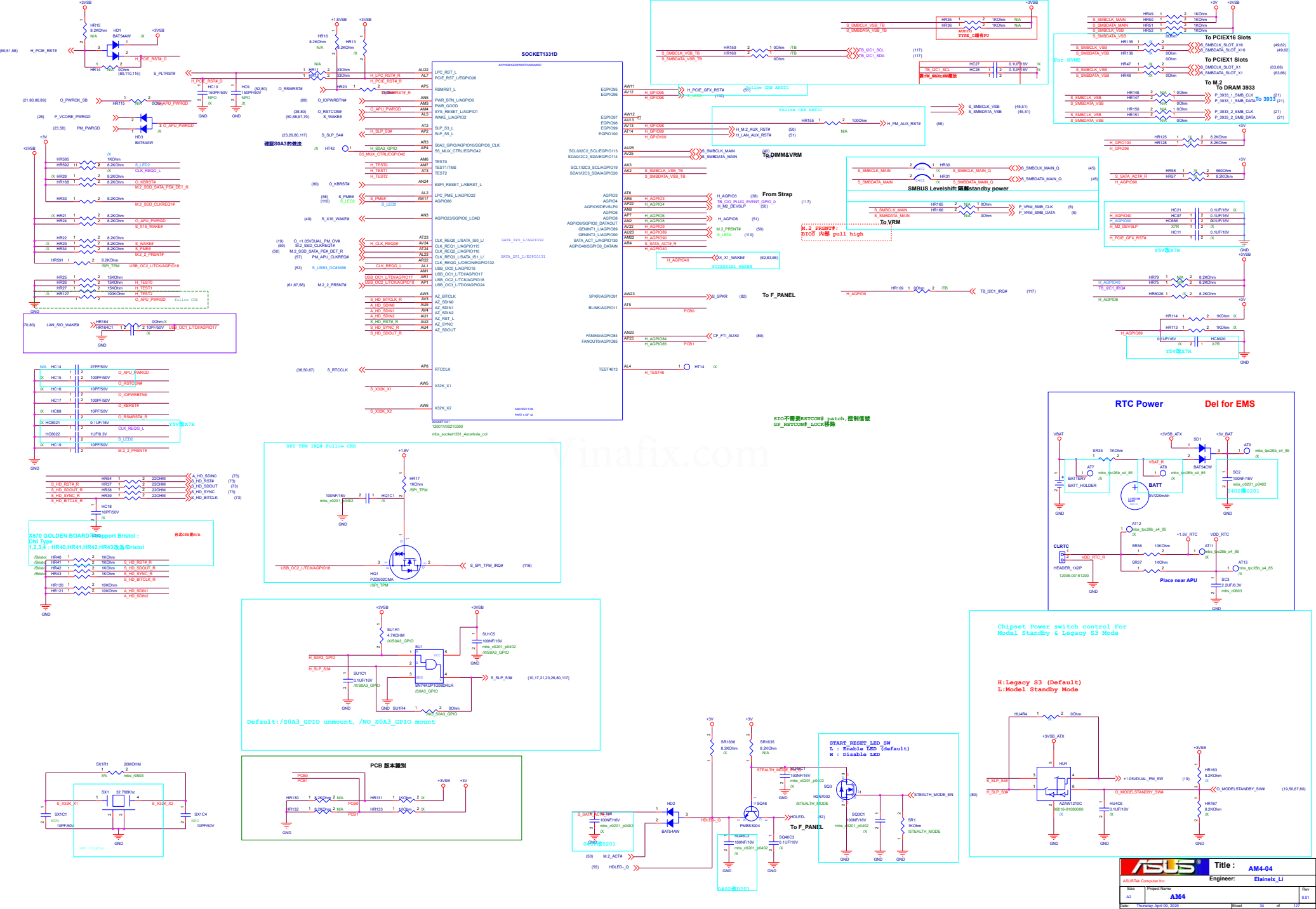


Table 3. CORETYPE to Model Number Mapping

CORETYPE1	CORETYPE0	Family/Model Numbers	AM4 Processor Type
0	0	Family 15h/Models 60h-6Fh	Type 0
0	1	Reserved	Reserved
1	1	Family 17h/Models 20h-2Fh	Type 1
1	0	Family 17h/Models 00h-0Fh	Type 2
1	1	Family 17h/Models 10h-1Fh	Type 3
1	0	Family 17h/Models 70h-7Fh	Type 4
1	1	Family 17h/Models 60h-6Fh	Type 5
1	0	Family 19h/Models 20h-2Fh	Type 6

Title :	AM4-03
Engineer:	Elainelx_Li
ASUSTek Computer Inc.	
Size: Custom	Project Name: AM4
Rev:	0.01
Date: Tuesday, April 07, 2020	Sheet 33 of 127


SOCKET1331D
To DIMM&VRM
From Strap
To F_PANEL
To VRM
SMBUS Levelshift:隔離standby power
M.2 PRSNT#:
BIOS 內部 pull high
To PCIEX16 Slots
To PCIEX1 Slots
To M.2
To DRAM 3933
To 3933
RTC Power
Del for EMS
Place near APU
Chipset Power switch control For
Model Standby & Legacy S3 Mode
H:Legacy S3 (Default)
L:Model Standby Mode
START_RESET_LED SW
L : Enable LED (default)
H : Disable LED
PCB 版本識別
Default:/S0A3_GPIO unmount, /NO_S0A3_GPIO mount
SIO不需要RSTCON# patch,控制信號
GP_RSTCON#_LOCK移除
確認S0A3的做法
XS70 GOLDEN BOARD Support Bristol :
DNI Type
1,2,3,4 : HR40,HR41,HR42,HR43改為/Bristol
Title : AM4-04
Engineer: Elaineix_Li
ASUSTek Computer Inc.
Project Name
AM4
Rev
0.01
Date: Thursday, April 09, 2020
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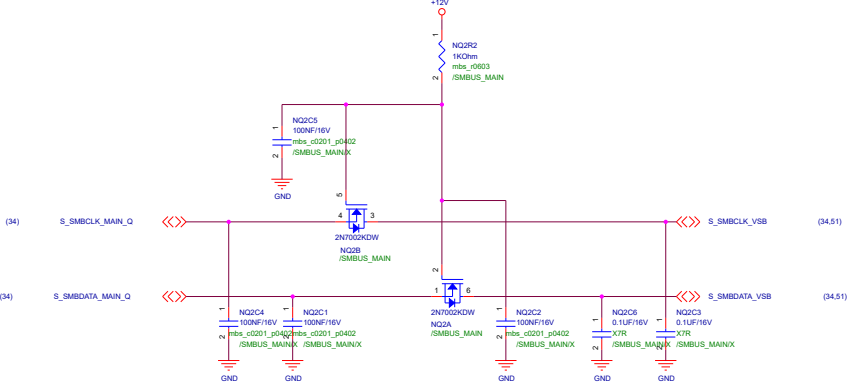
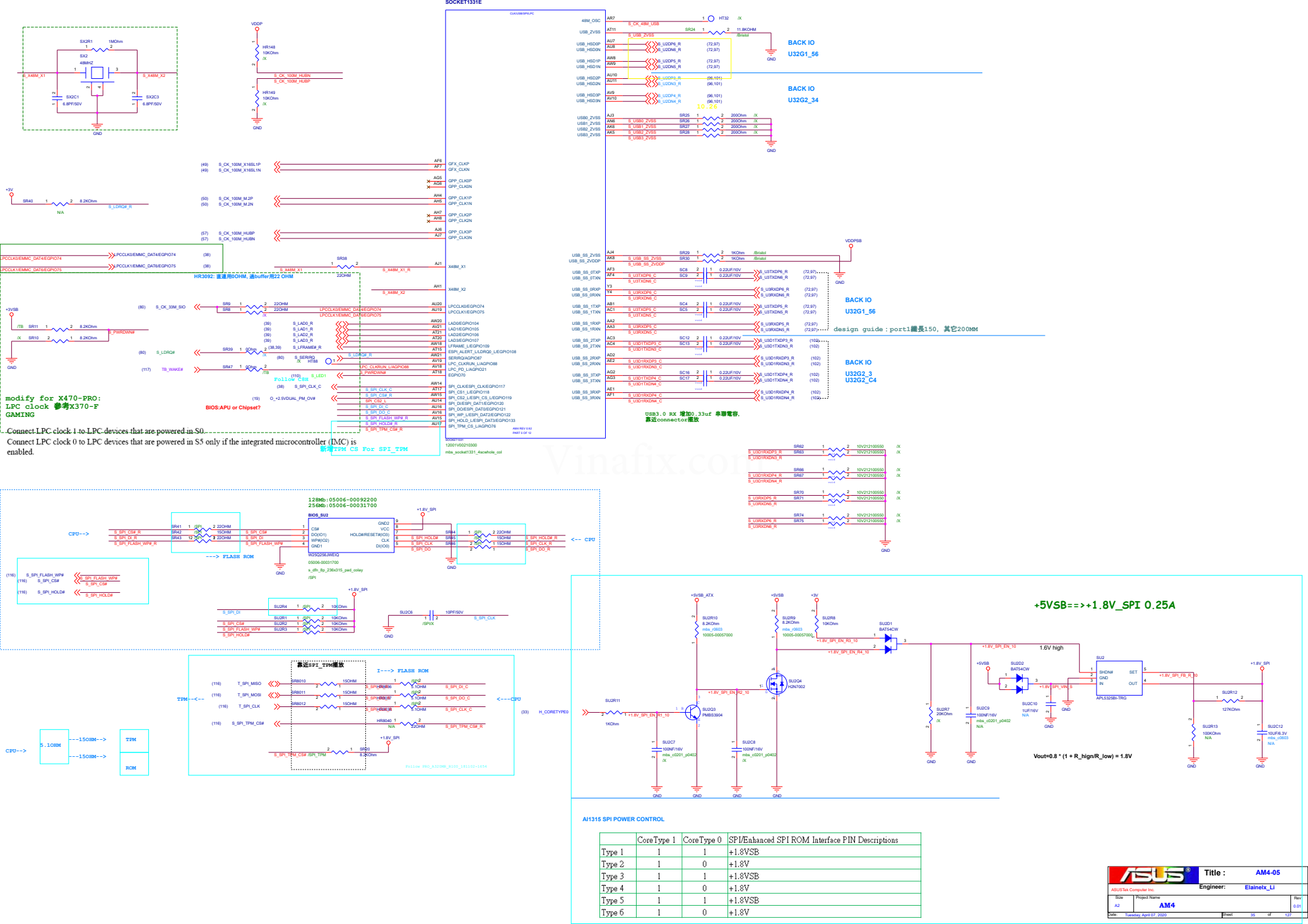


<Variant Name>

ASUSTeK COMPUTER INC	Title : DP1.4_RE-DRIVER	
	Engineer:	
Size: A2	Project Name: AM4	Rev: R1.00
Date: Thursday, March 05, 2020	Sheet 45 of 127	



	CoreType 1	CoreType 0	SPI/Enhanced SPI ROM Interface PIN Descriptions
Type 1	1	1	+1.8VSB
Type 2	1	0	+1.8V
Type 3	1	1	+1.8VSB
Type 4	1	0	+1.8V
Type 5	1	1	+1.8VSB
Type 6	1	0	+1.8V

ASUSTeK Computer Inc.	Title :	AM4-05
	Engineer:	Elainelx_Li
Size: A2	Project Name: AM4	Rev: 0.01
Date: Tuesday, April 07, 2020	Sheet 35 of 127	

<Variant Name>

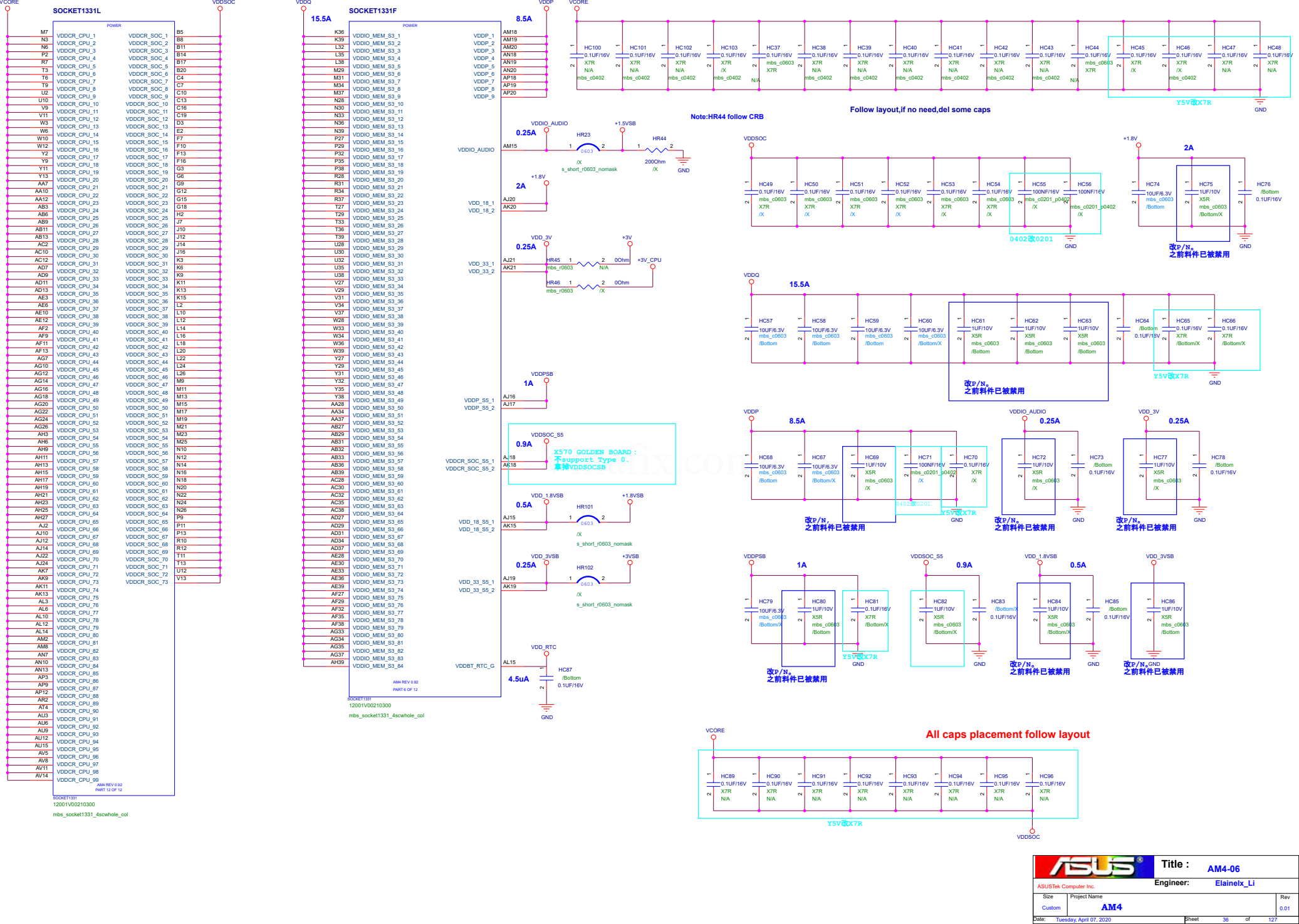
Title : AM4-16

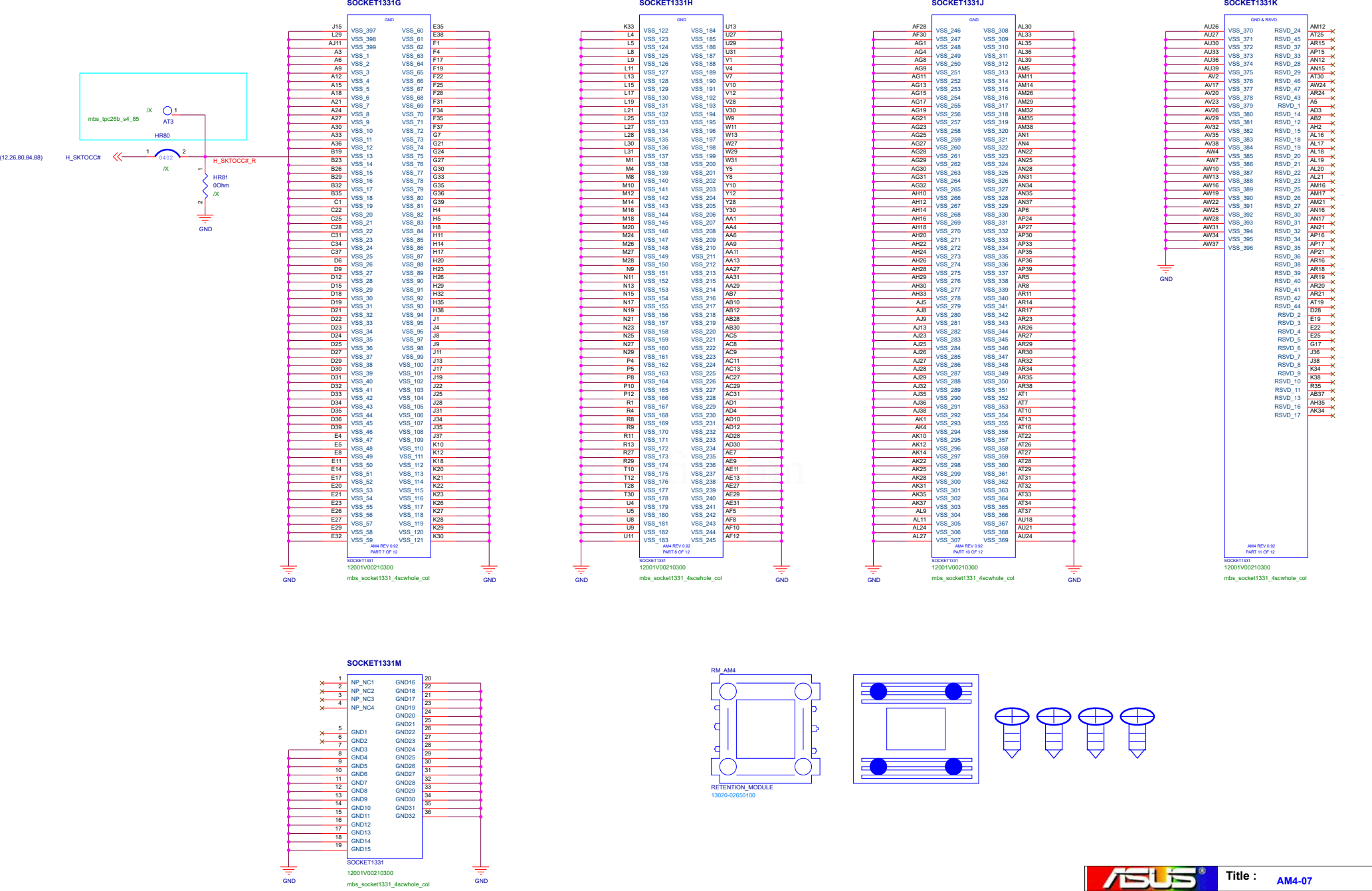
ASUSTek Computer Inc.

Engineer: ElaineIx_Li

Size	Project Name	Rev
A2	AM4	0.01

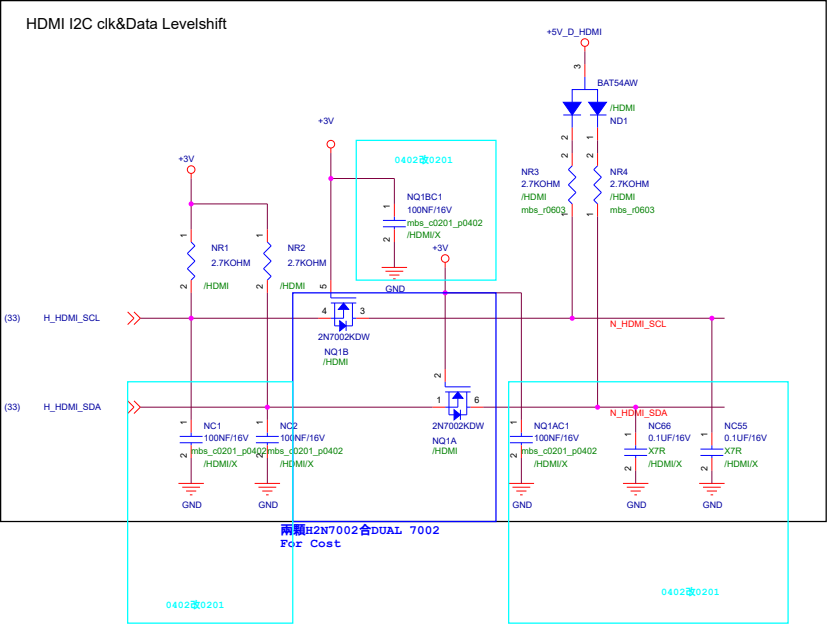
Date:	Tuesday, March 03, 2020	Sheet	47	of	127

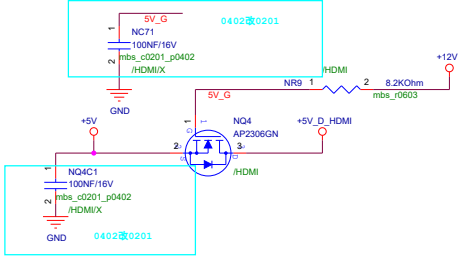

SOCKET1331L
SOCKET1331F
VCORE
VDDSOC
VDDQ
VDDP
15.5A
8.5A
Follow layout,if no need,del some caps
Note:HR44 follow CRB
All caps placement follow layout
X570 GOLDEN BOARD :
不support Type 0.
拿掉VDDSOCSB
改P/N。
之前料件已被禁用
Y5V改X7R
0402改0201
12001V00210300
mbs_socket1331_4scwhole_col
Title : AM4-06
Engineer: Elainelx_Li
ASUSTek Computer Inc.
Project Name AM4
Rev 0.01
Date: Tuesday, April 07, 2020
Sheet 36 of 127

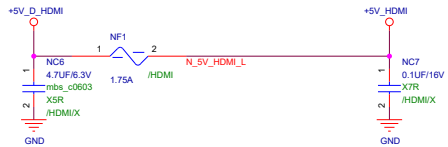


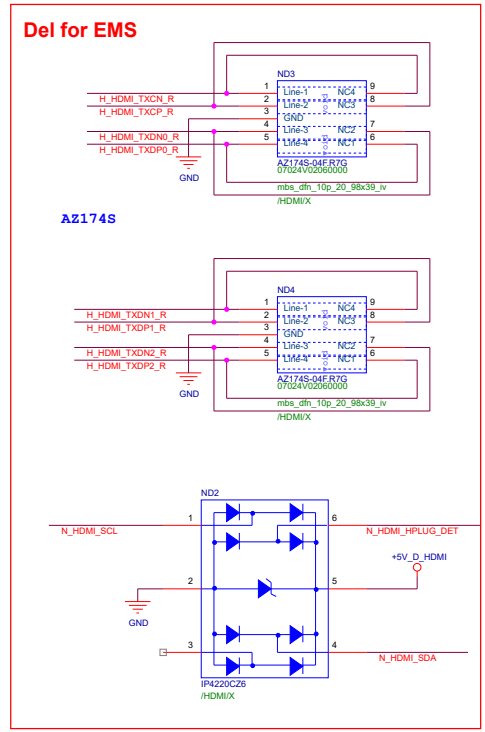
COST DOWN VER

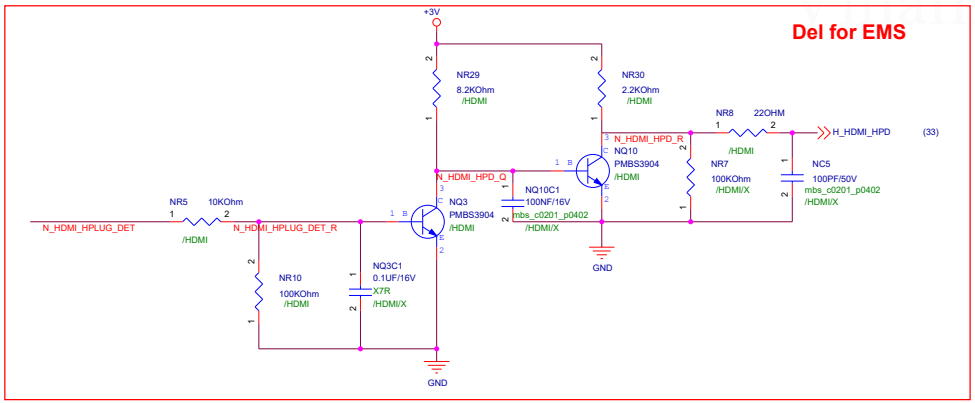
ASUSTek Computer Inc.	Title : AM4-07	
	Engineer: Elainelx_Li	
Size: A3	Project Name: AM4	Rev: 0.01
Date: Tuesday, April 07, 2020	Sheet 37 of 127	

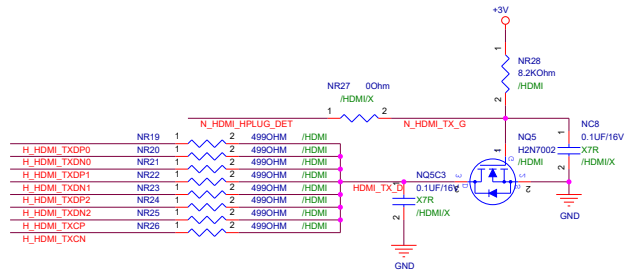












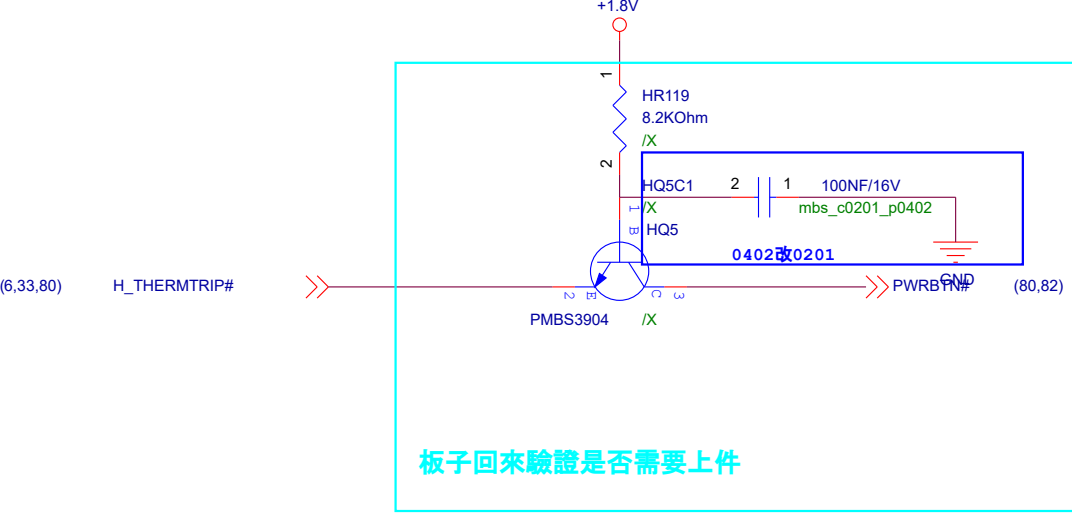
ASUSTek Computer Inc.

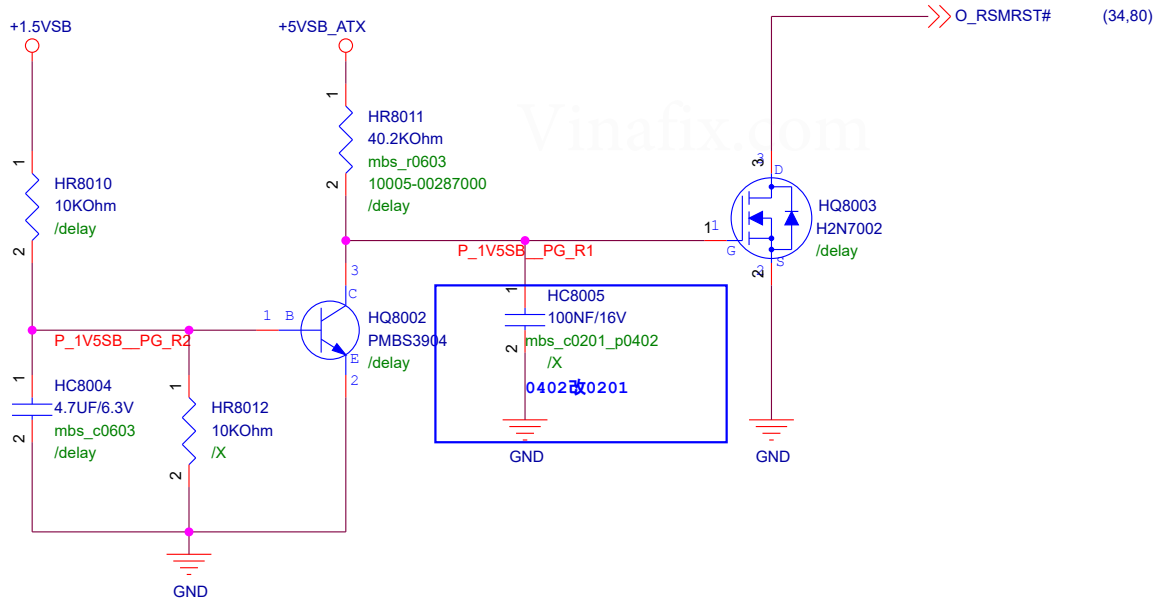
Title : AM4-16

Engineer: Elainelx_Li

Size	Project Name	Rev
A3	AM4	0.01

Date: Thursday, March 05, 2020 Sheet 48 of 127





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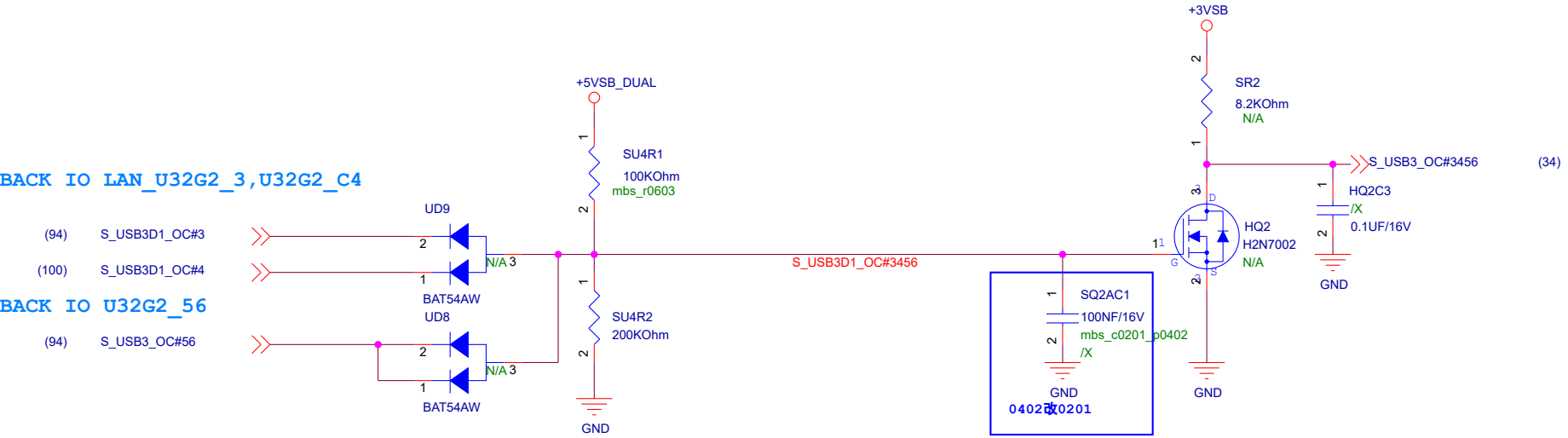
Size: A	Document Number: <Doc>	Rev: <RevCode>
Date: Thursday, March 05, 2020	Sheet 52 of 127	

不Support Type 0



<Variant Name>

ASUSTEK COMPUTER INC	Title : Patch For USBOC	
	Engineer:	
Size: A4	Project Name	Rev: 0.0
Date: Thursday, March 05, 2020	Sheet 53 of 127	

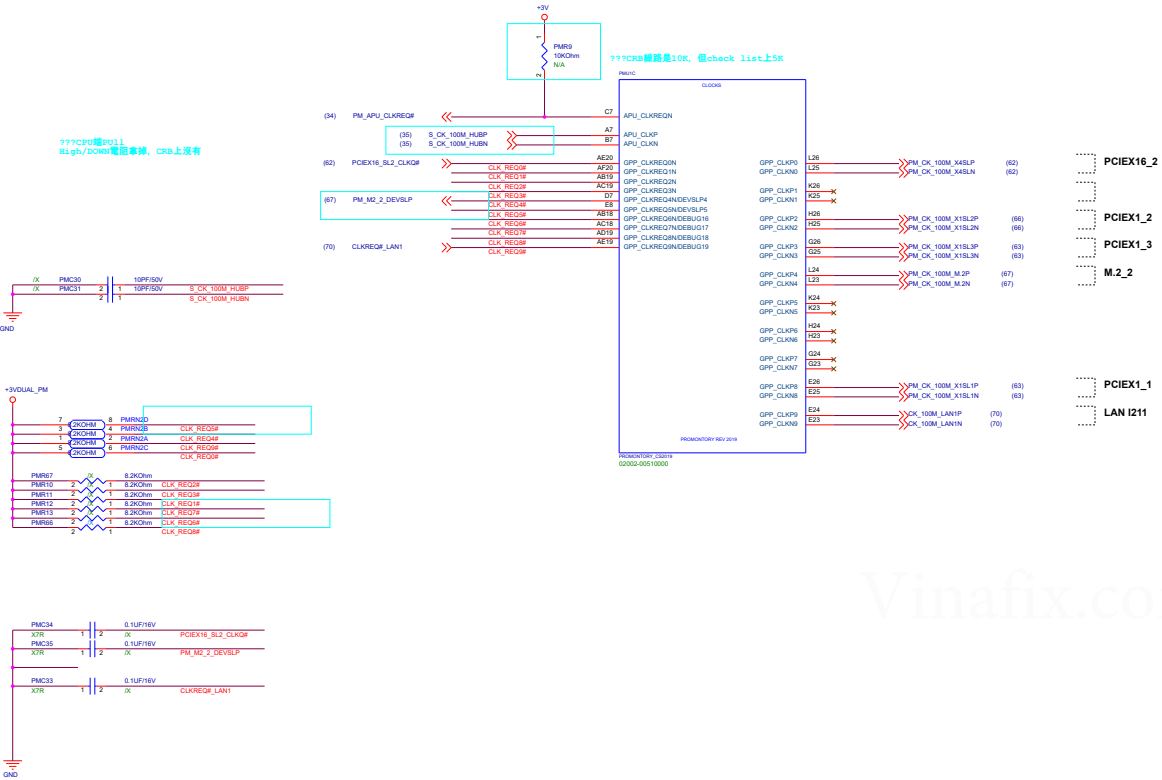


Table 11. CLK and CLKREQ to PCIe® GPP Port Pin Mapping

GPP Port	CLK	CLKREQ#
GPP_TX/RX[0]	GPP_CLKP/N0	GPP_CLKREQ0N
GPP_TX/RX[1]	GPP_CLKP/N1	GPP_CLKREQ1N
GPP_TX/RX[2]	GPP_CLKP/N2	GPP_CLKREQ2N
GPP_TX/RX[3]	GPP_CLKP/N3	GPP_CLKREQ3N
GPP_TX/RX[4]	GPP_CLKP/N4	GPP_CLKREQ4N/DEVSLP4
GPP_TX/RX[5]	GPP_CLKP/N5	GPP_CLKREQ5N/DEVSLP5
GPP_TX/RX[6]	GPP_CLKP/N6	GPP_CLKREQ6N/DEBUB16
GPP_TX/RX[7]	GPP_CLKP/N7	GPP_CLKREQ7N/DEBUG17
GPP_TX/RX[8]	GPP_CLKP/N8	GPP_CLKREQ8N/DEBUG18
GPP_TX/RX[9]	GPP_CLKP/N9	GPP_CLKREQ9N/DEBUB19

Table 10. General Purpose PCI Express® Interface

Pin Name	Type	Voltage	Functional Description	Variant		
				A	C	D
GPP_CLKP[5:0]	A-O		General purpose PCIe 5:0 clock output positive	X	X	X
GPP_CLKN[5:0]	A-O		General purpose PCIe 5:0 clock output negative	X	X	X
GPP_CLKP[9:6]	A-O		General purpose PCIe 9:6 clock output positive		X	X
GPP_CLKN[9:6]	A-O		General purpose PCIe 9:6 clock output negative		X	X
GPP_CLKREQ[3:0]N	OD	VCC33	General purpose clock request 3:0 (No Internal Pull)	X	X	X
GPP_CLKREQ[5:4]/DEVSLP[5:4]	OD		General purpose clock request 5:4 (No Internal Pull)	X	X	X
GPP_CLKREQ[9:6]N/DEBUG[19:16]	OD		General purpose clock request 9:6 (No Internal Pull)		X	X

<Variant Name>

Title : PROMONTORY2019(CLOCK)

ASUSTek COMPUTER INC.

Engineer:

Size	Project Name	Rev
A2	AM4	R1.00

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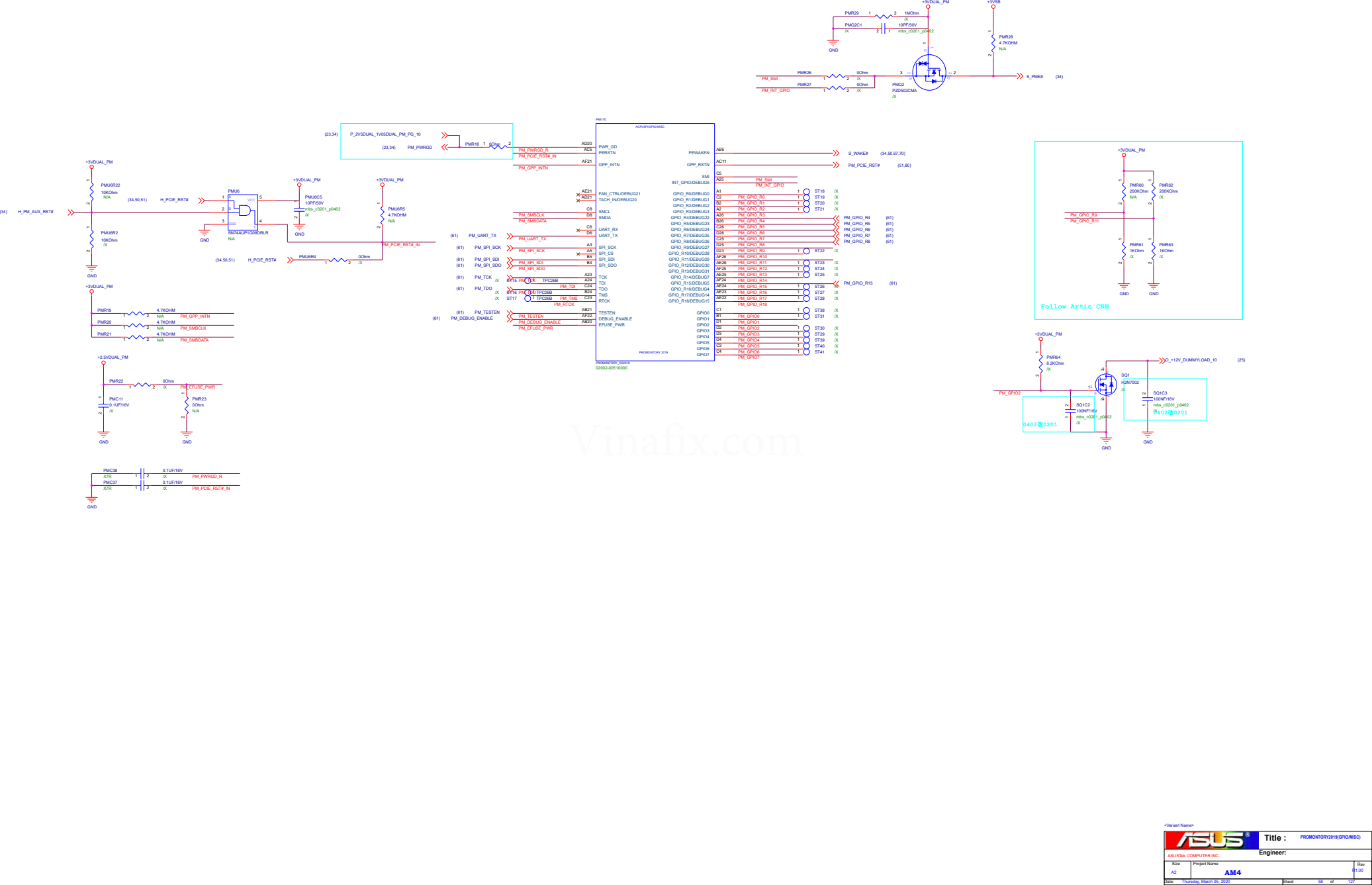

PROMONTORY 2019
Follow Artic CRB
Vinafix.com

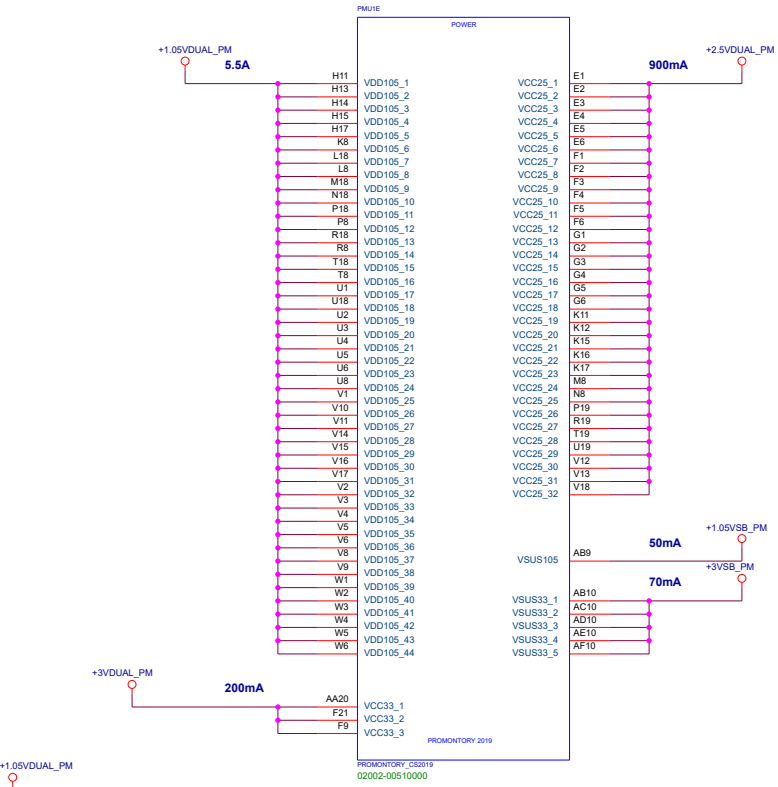
Table 22. Recommended Operating Conditions

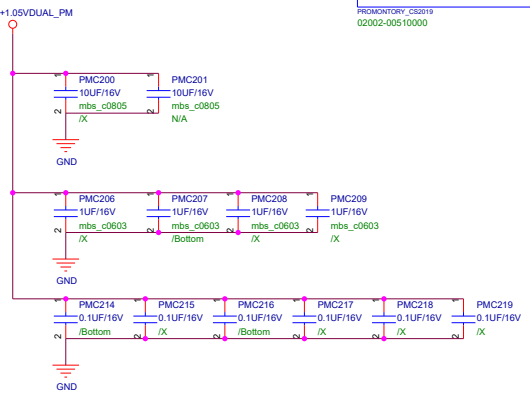
Symbol	Parameter	Min	Typical	Max	Units	Max Current Design
VCC33	Normal power supply	3.0	3.3	3.6	V	200 mA
VCC25	Normal power supply	2.25	2.5	2.75	V	900 mA
VDD105	Normal power supply	1.00	1.05	1.1	V	5.5 A
VSUS33	Suspend power supply	3.0	3.3	3.6	V	70 mA
VSUS105	Suspend power supply	1.00	1.05	1.1	V	50 mA
T_J	Operating junction temperature	0	25	90	°C	–
T_C	Operating case temperature	–	25	85	°C	–

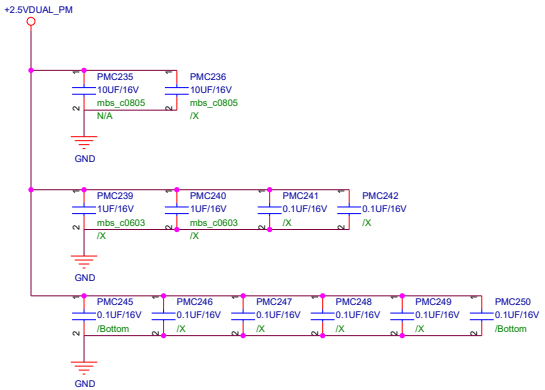
Table 17. Power/Ground Pins

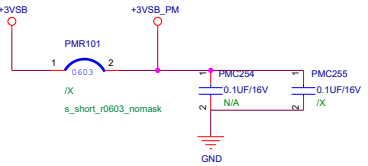
Pin Name	Voltage/GND	GND Reference	S* State	Description
VCC25	2.5 V	GNDA	S0 Note 1	PHY power
VCC33	3.3 V	GND	S0 Note 1	Digital I/O power
VDD105	1.05 V	GND	S0 Note 1	Core Logic power
VSUS33	3.3 V	GNDA	S0/S3/S4/S5	Suspend power
VSUS105	1.05 V	GNDA	S0/S3/S4/S5	Suspend power
EFUSE_PWR	2.5 V	GND	S0	EFUSE power (Recommend to pull down or leave float on PCB)
GND	Ground			Ground for core logic and digital I/O
GNDA	Ground			Ground for PHYs

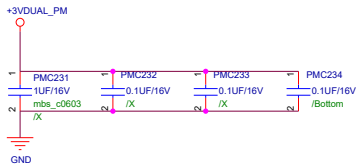
Note 1: *For systems supporting Modern Standby this rail must be supplied while the device in the S3 equivalent alternative sleep state.*

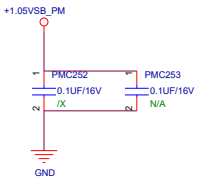












<Variant Name>

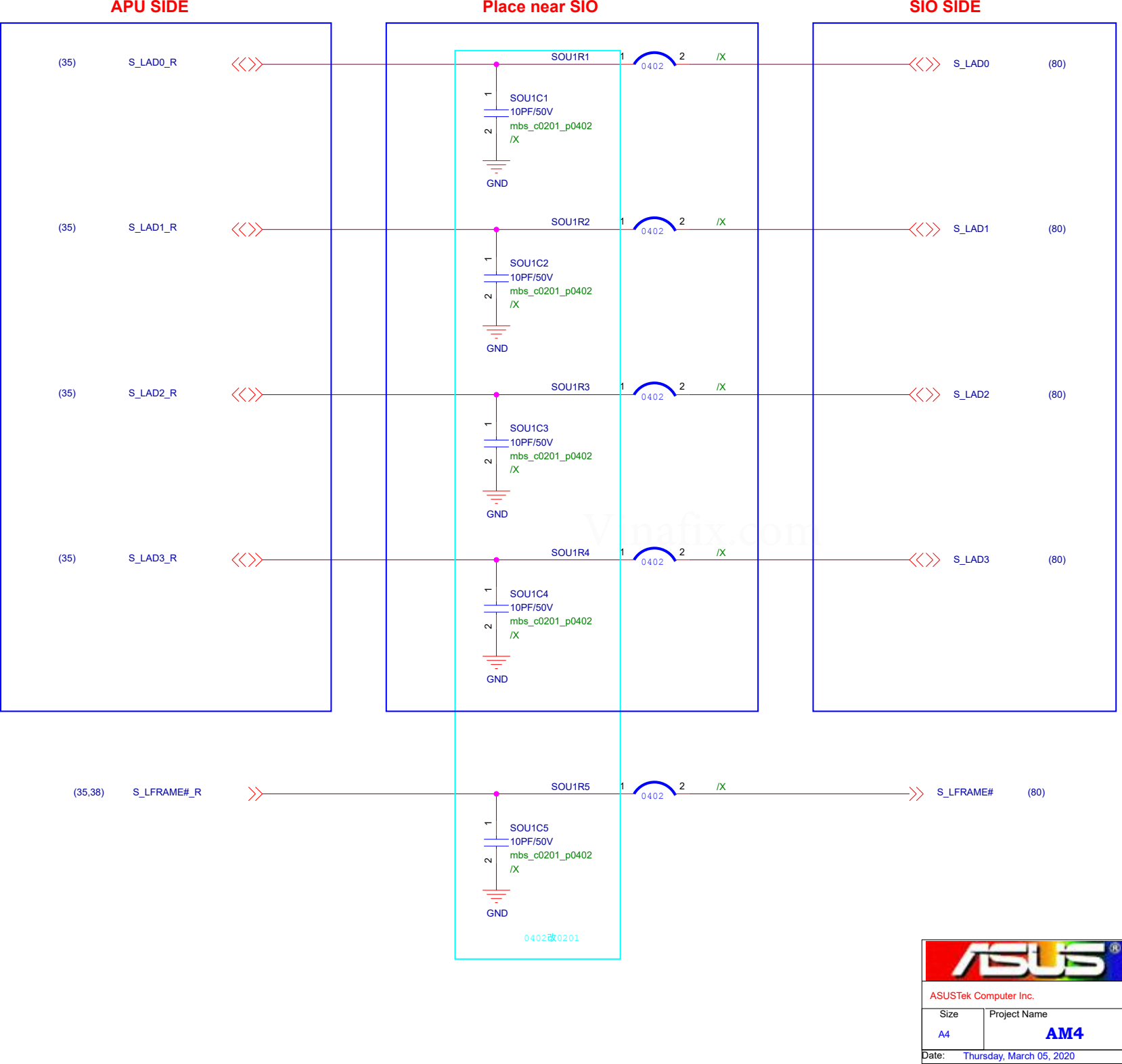
ASUSTek COMPUTER INC.

Title : PROMONTORY2019(PWR)

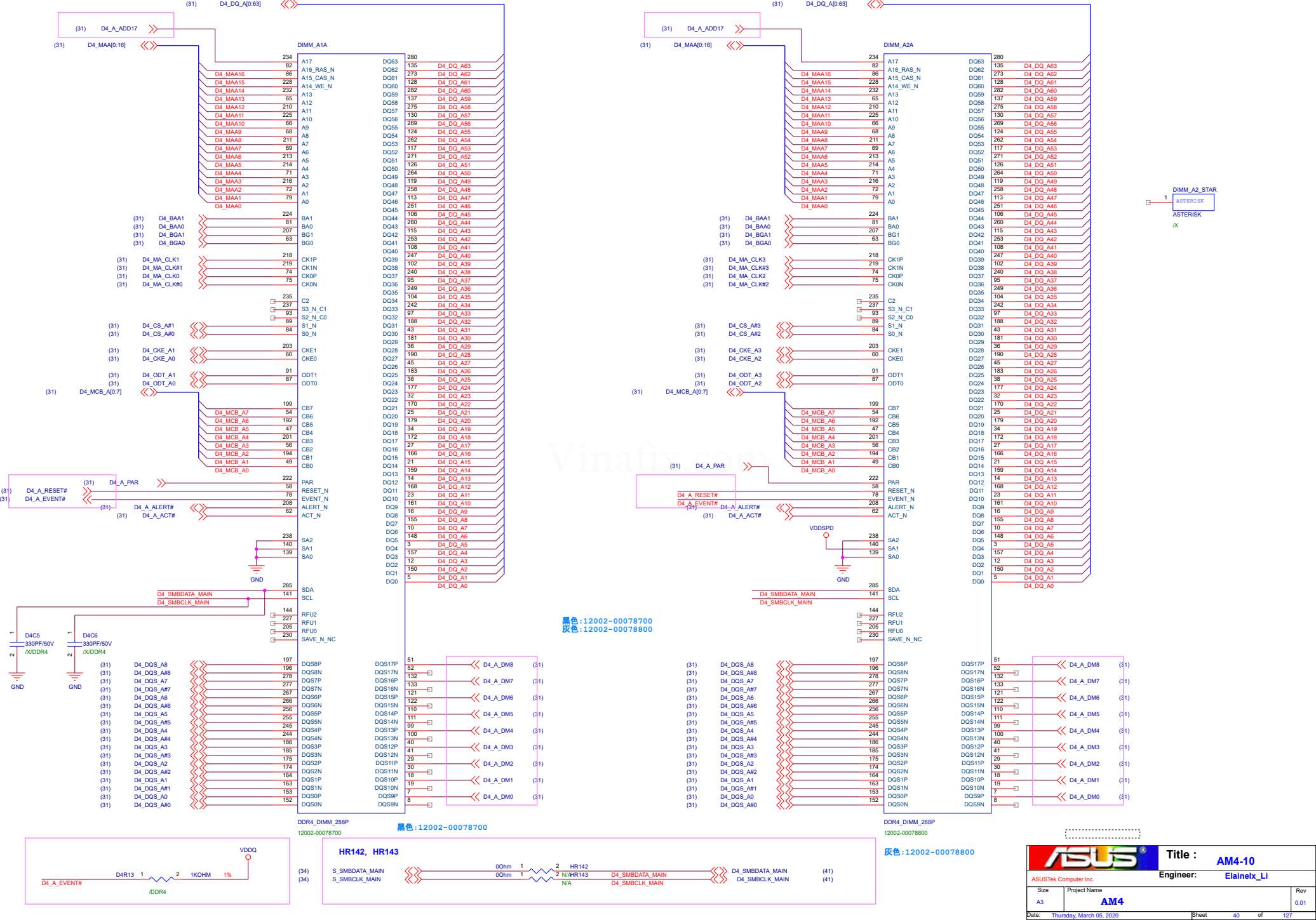
Engineer:

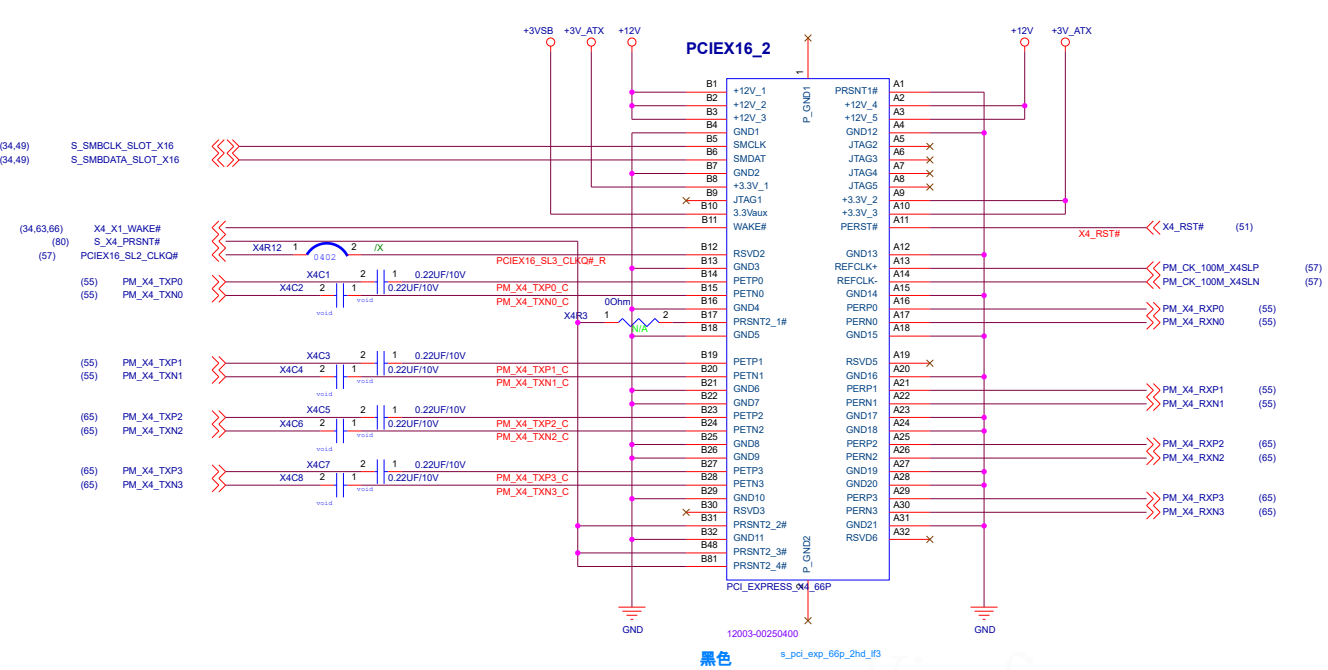
Size: A3 | Project Name: AM4 | Rev: R1.00

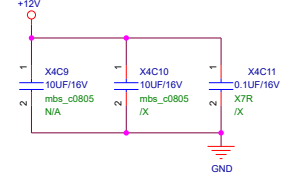
Date: Tuesday, March 03, 2020 | Sheet 59 of 127

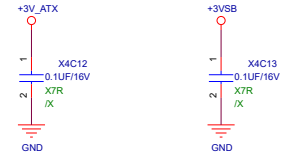


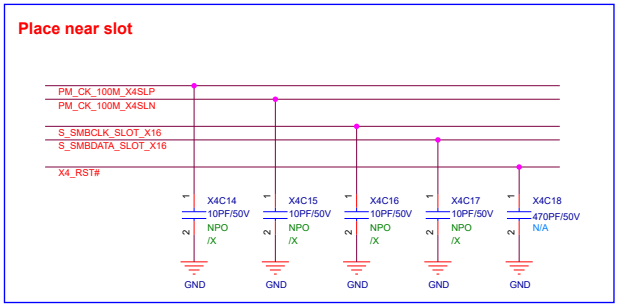
ASUSTek Computer Inc.	Title : AM4-09	
	Engineer: Elainelx_Li	
Size: A4	Project Name: AM4	Rev: 0.01
Date: Thursday, March 05, 2020	Sheet 39 of 127	


DIMM_A1A
DIMM_A2A
DDR4_DIMM_288P
12002-00078700
12002-00078800
黑色:12002-00078700
反色:12002-00078800
HR142, HR143
D4C5 330PF/50V /X/DDR4
D4C6 330PF/50V /X/DDR4
D4R13 1KOHM 1% /DDR4
0Ohm HR142
0Ohm HR143
N/A
DIMM_A2_STAR
ASTERISK
/X
Title : AM4-10
Engineer: Elainelx_Li
ASUSTek Computer Inc.
Size A3
Project Name AM4
Rev 0.01
Date: Thursday, March 05, 2020
Sheet 40 of 127



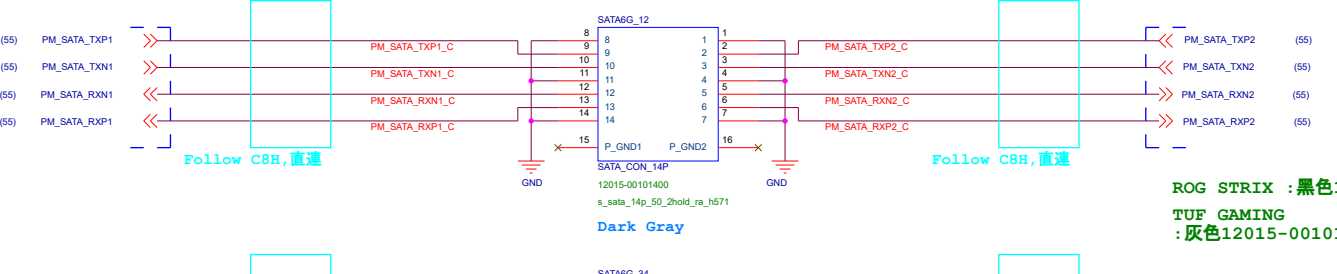






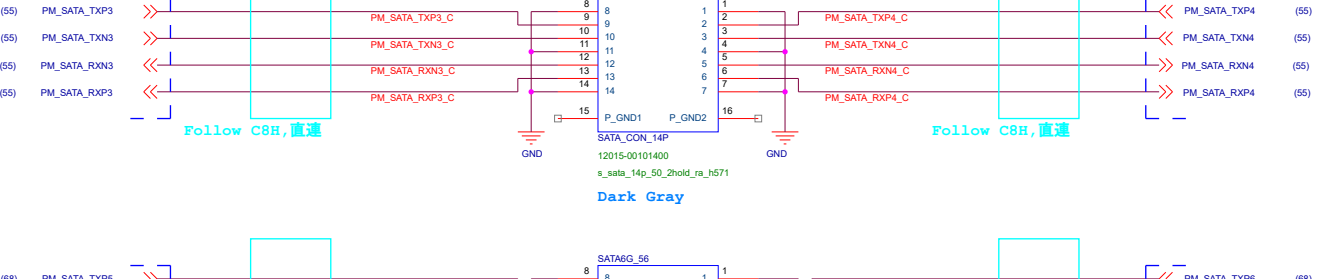
From SIO

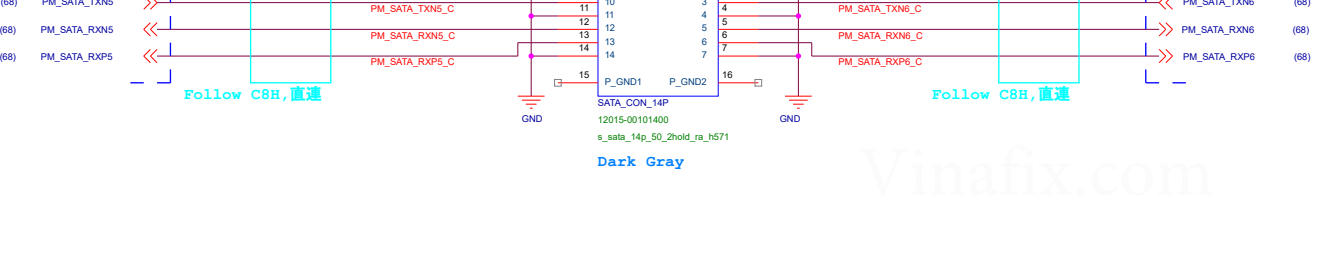
ASUSTek Computer Inc.	Title :	Premium-08	
	Engineer:	Elainelx_Li	
Size: A3	Project Name: AM4		Rev: 0.01
Date: Monday, March 23, 2020	Sheet 62 of 127		



ROG STRIX :黑色12015-00101900

TUF GAMING
:灰色12015-00101400





ASUSTek Computer Inc.

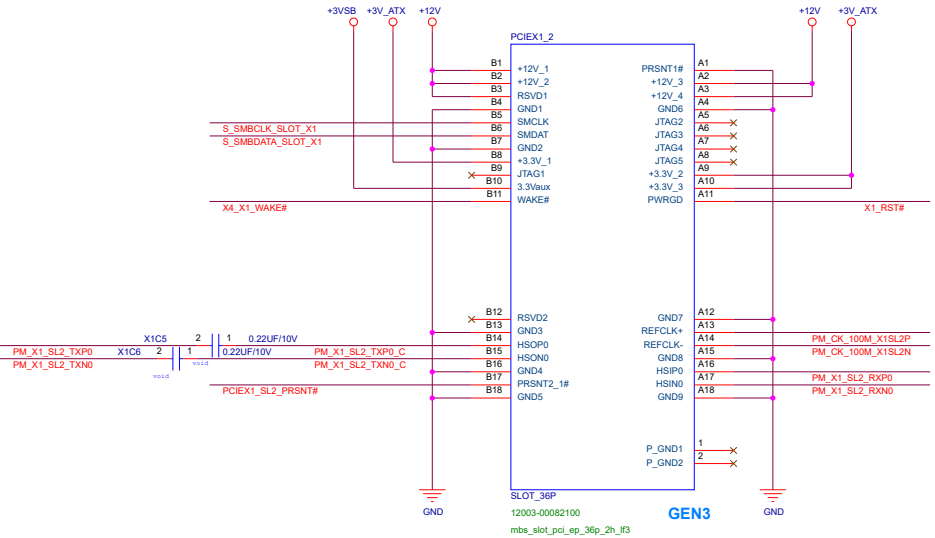
Title : Premium-10

Engineer: Elainelx_Li

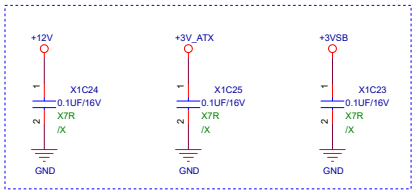
Size	Project Name	Rev
A3	AM4	0.01

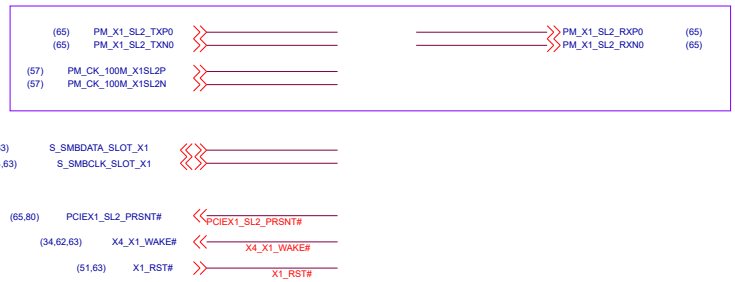
Date: Thursday, March 05, 2020 Sheet 64 of 127

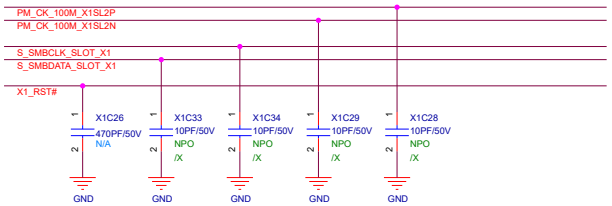
PIEX1_2



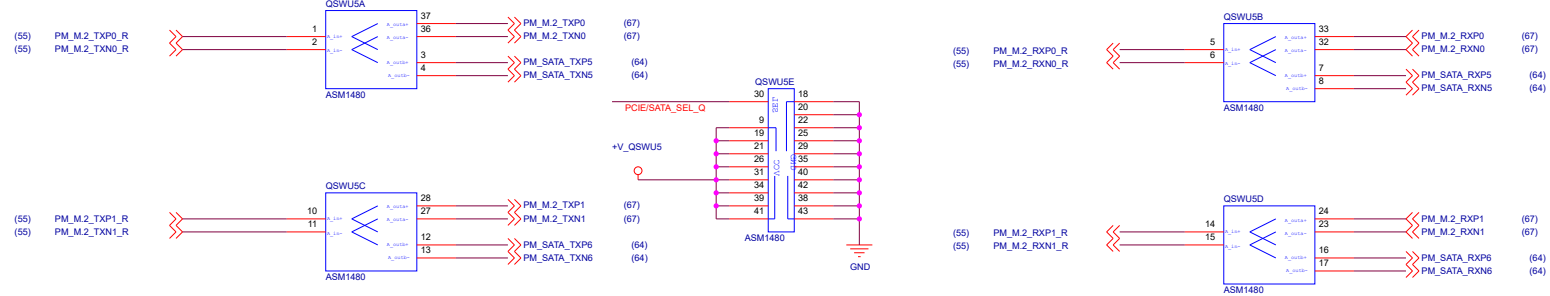
For Slot2







ASUSTek Computer Inc.	Title : Premium-12	
	Engineer: Elainelx_Li	
Size: A3	Project Name: AM4	Rev: 0.01
Date: Monday, March 23, 2020	Sheet 66 of 127	

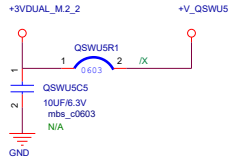


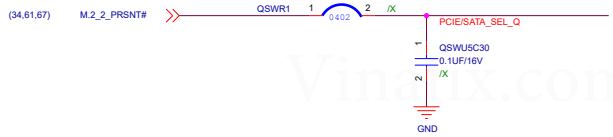
PCIE/SATA_SEL_Q	Function	
L	N_in to N_outa	M.2_2
H	N_in to N_outb	SATA6G_5&_6

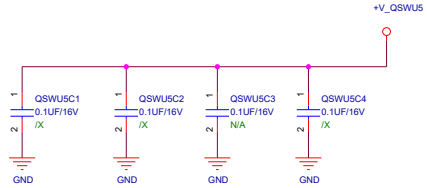
Default

BIOS chose by M.2_2 PRSNT#

3.3V for 1440 new version
1.8V for 1440 old version







ASUSTek Computer Inc.	Title : PROMONTORY2019-14		
	Engineer: Elainelx_Li		
Size: A3	Project Name: AM4		Rev: 0.01
Date: Thursday, March 05, 2020	Sheet 68 of 127		

RTL8111H/L8200A Circuit

A. Modify PCIE Reset Signal Net Name by Project

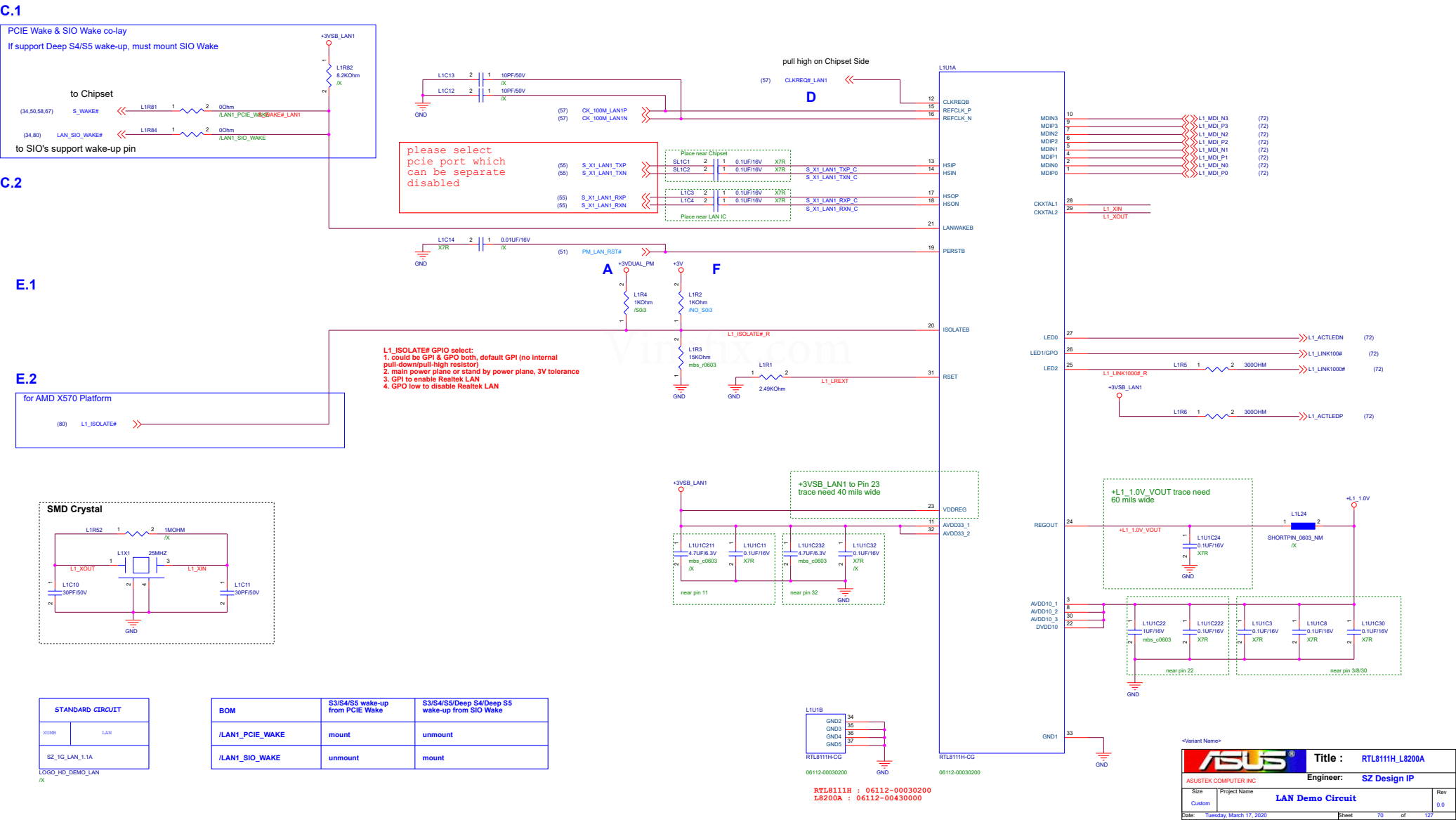
B. Modify L1U1 Part Number by Project

C. Choose Wake-up Signal Circuit by Project

D. Delete CLKREQ#_LAN1 if not need

E. Choose L1_ISOLATE# Circuit by Project

F. Modify +3V to +3V_S0IX if support Intel S0ix



STANDARD CIRCUIT	
XIMB	LAN
SZ_1G_LAN_1.1A	

LOGO_HD_DEMO_LAN
/X

BOM	S3/S4/S5 wake-up from PCIE Wake	S3/S4/S5/Deep S4/Deep S5 wake-up from SIO Wake
/LAN1_PCIE_WAKE	mount	unmount
/LAN1_SIO_WAKE	unmount	mount

<Variant Name>

ASUSTEK COMPUTER INC

Title : RTL8111H_L8200A

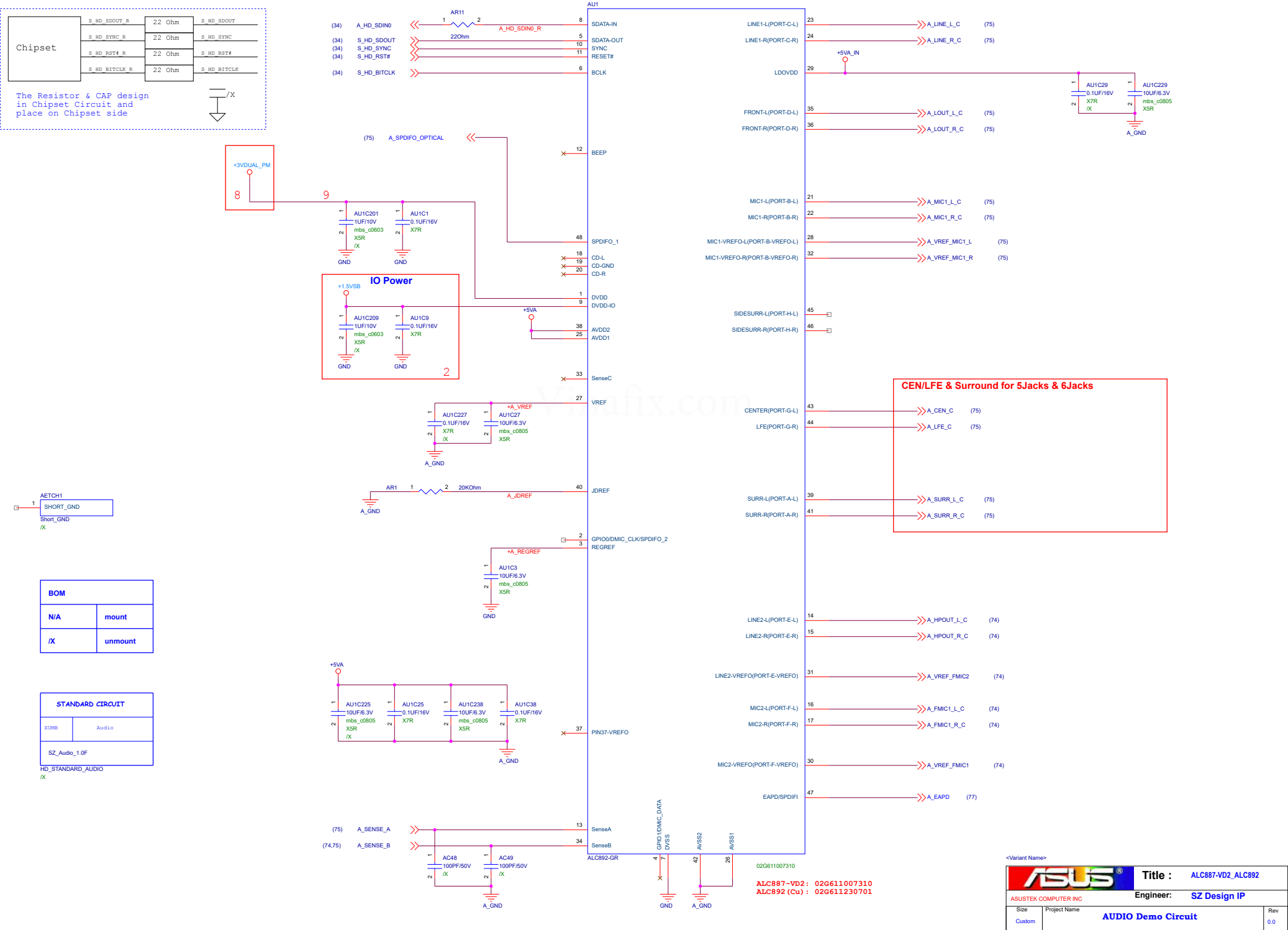
Engineer: SZ Design IP

Size: Custom | Project Name: LAN Demo Circuit | Rev: 0.0

Date: Tuesday, March 17, 2020 | Sheet 70 of 127

ALC887-VD2 & ALC892 Circuit

1. Modify AU1 Part Number by Project
2. Modify IO Power by Project
3. Delete A_EAPD if not need
4. Delete A_SPDIFO_HEADER if not need
5. Delete A_SPDIFO_OPTICAL if not need
6. Delete Side Surround for Rear 3 Jacks or 5Jacks
7. Delete CEN/LFE & Surround for Rear 3 Jacks
8. Block 8,9, select one of them according if support s0ix



<Variant Name>

ASUSTEK COMPUTER INC	Title : ALC887-VD2_ALC892	
	Engineer: SZ Design IP	
Size: Custom	Project Name: AUDIO Demo Circuit	Rev: 0.0
Date: Thursday, March 05, 2020	Sheet 73 of 127	

Rear 5Jacks Circuit

1. Choose Jack Detect Circuit by Codec,block 1,2,3

2. Choose LOUT DIP CAP Type by Codec & Project,block 4,5,,6

3. Choose LOUT Circuit with De-POP/Switch or not by Project,block 7,8

4. Modify ACE1, ACE2 Part Number by Project

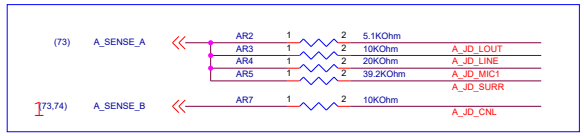
5 if you use 1220 ,Modify AC1,AC2,AC3, AC4, ,AC5,AC6, AC7, AC8, AC9, AC10 Part Number to varistor and Optional to N/A

6. Choose CEN/LFE & Surround CAP Type by Project,Block 9,10

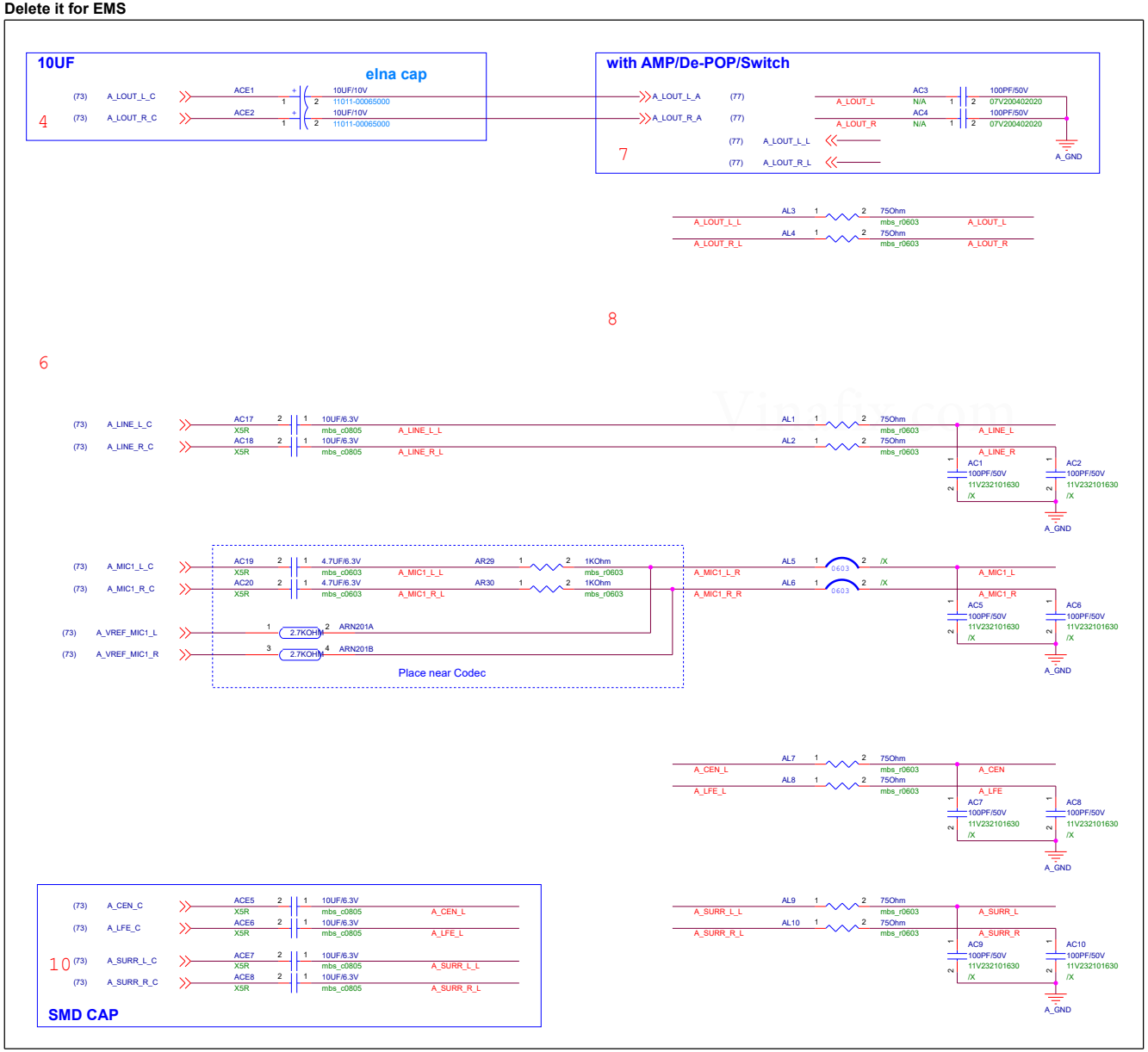
7 If choose DIP CAP, modify ACE5, ACE6, ACE7, ACE8 Part Number by Project

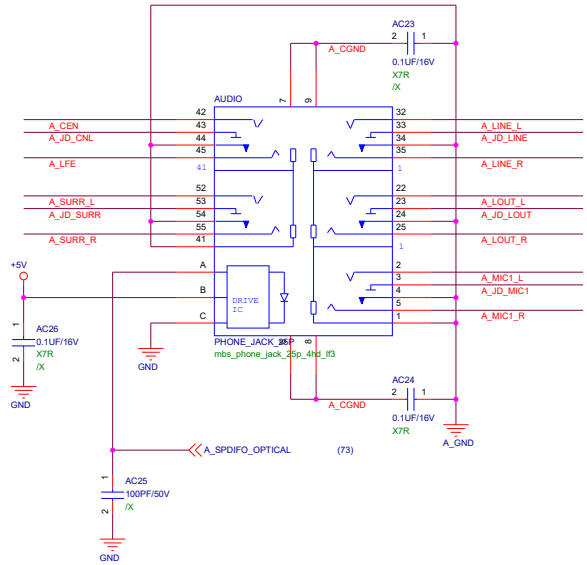
8. For Gamer/Gaming Project, Line In use DIP CAP ACE11, ACE12 replace AC17, AC18

for ALC887-VD2/ALC892



Delete it for EMS





Audio CAP using rule,pls change all dip caps partnumber according bellow rule

Z390,B450 ROG / Strix series	Nichicon
Z390,B450 PRIME / TUF Series	ELNA
Intel H310,H310C,H110&AMD A320 series	Chemicon
other chipsets except above series	Nichicon

DIP CAP
EL 10U : 11G040822620
PL 10U : 11V090106207

Taping DIP CAP
Chemicon 10U T: 11011-00064100
Elan 10U:11011-00065000
Nichicon 10U T: 11011-00066200

DIP CAP
EL 100U : 11V040107321
PL 100U : 11031V0001F000

Taping DIP CAP
Chemicon 100U T: 11011-00024100
Elan 100U :11011-00025000
Nichicon 100U T: 11011-00026200

AC1, AC2, AC3, AC4, AC5,
AC6, AC7, AC8, AC9, AC10
100PF : 11V232101630
Varistor: 07V200402020

Taping DIP CAP
PL 100U T:11031V0001F400

<Variant Name>

ASUSTEK COMPUTER INC

Title : 5 Jacks

Engineer: SZ Design IP

Size	Project Name	Rev
Custom	AUDIO Demo Circuit	0.0

Date: Thursday, March 05, 2020 Sheet 75 of 127

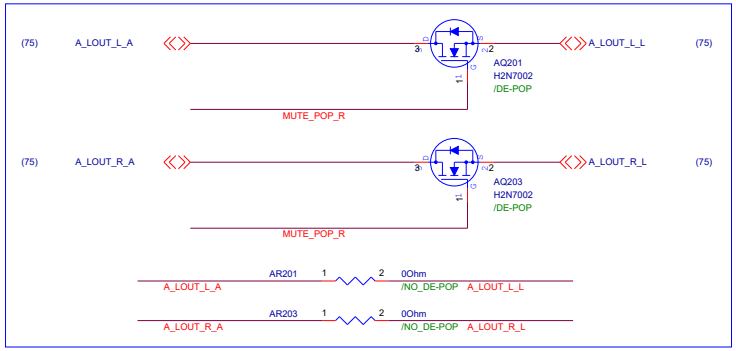
De-POP Circuit

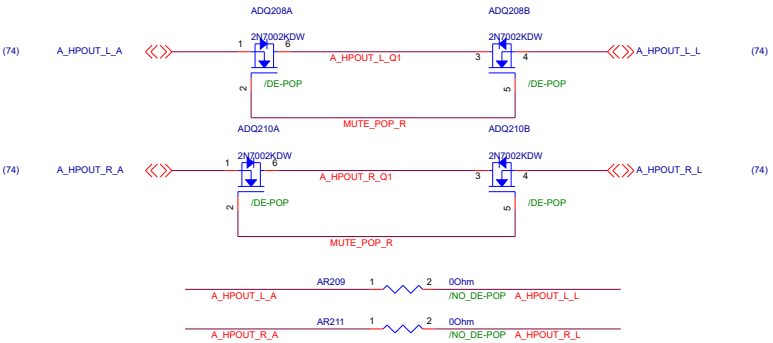
1. Choose De-POP Circuit by Project

2. Choose Resistor over GAP Circuit by Project

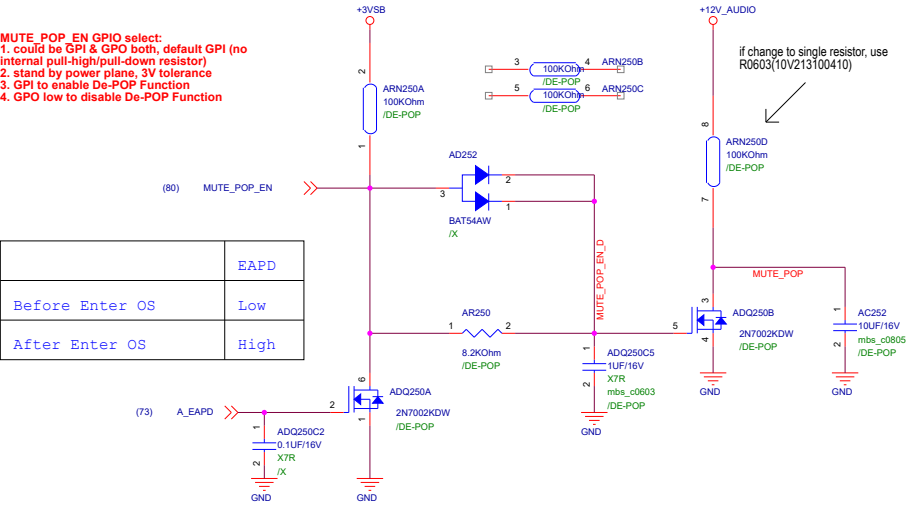
3. select Support s0ix or not support s0ix

for ACE1 & ACE2 use 10UF





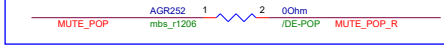
MUTE_POP_EN GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-high/pull-down resistor)
2. stand by power plane, 3V tolerance
3. GPI to enable De-POP Function
4. GPO low to disable De-POP Function



	EAPD
Before Enter OS	Low
After Enter OS	High

NOT Support S0IX

40 mils Gap for XU unmount AMP or Gamer/Gaming



<Variant Name>

ASUSTEK COMPUTER INC

Title : De-POP

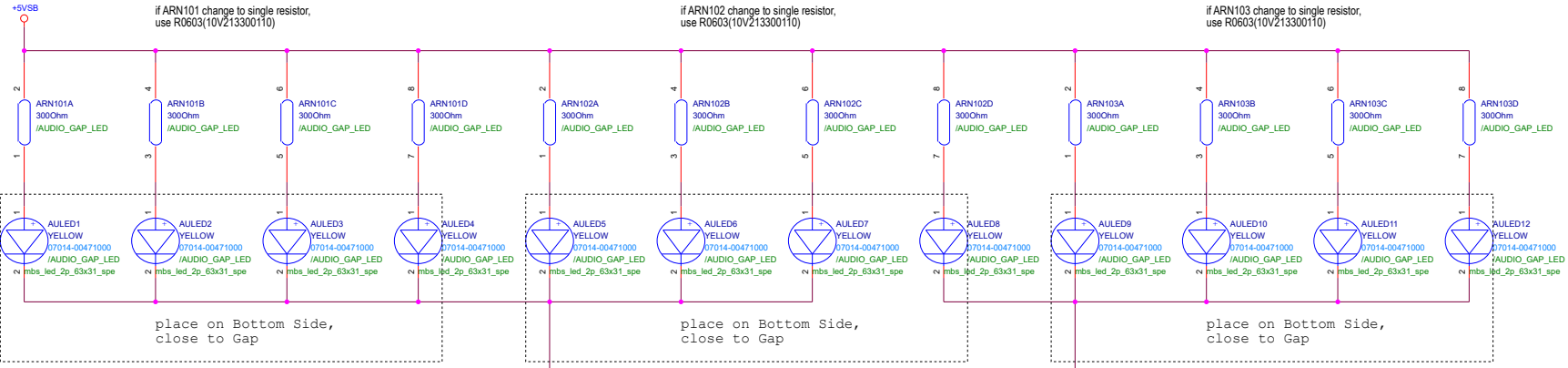
Engineer: SZ Design IP

Size	Project Name	Rev
Custom	AUDIO Demo Circuit	0.0

Date: Thursday, March 05, 2020 Sheet 77 of 127

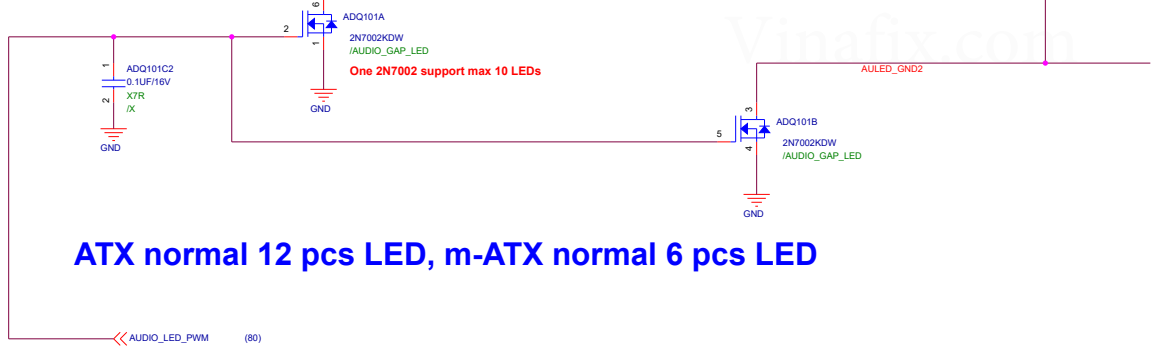
AUDIO LED Circuit

1. Modify Audio LED Color by Project
2. Choose or delete Codec Cover by Project
3. Keep or delete Codec Cover LED by Project
4. Modify Codec Cover Part Number by Project



Audio LED
Yellow: 07014-00091400
Red : 07VA010R0000

Audio LED
White: 07014-00471000



ATX normal 12 pcs LED, m-ATX normal 6 pcs LED

AUDIO_LED_PWM GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down resistor)
2. could mapping to Fading PWM function
3. stand by power plane, 3V tolerance
4. GPI to turn on Audio LED
5. GPO low to turn off Audio LED
6. Fading PWM to be Breathing LED

AUDIO COVER

Big Cover Small Cover TUF Cover

with LED under Cover : 13020-01430000
without LED under Cover: 13020-01430400

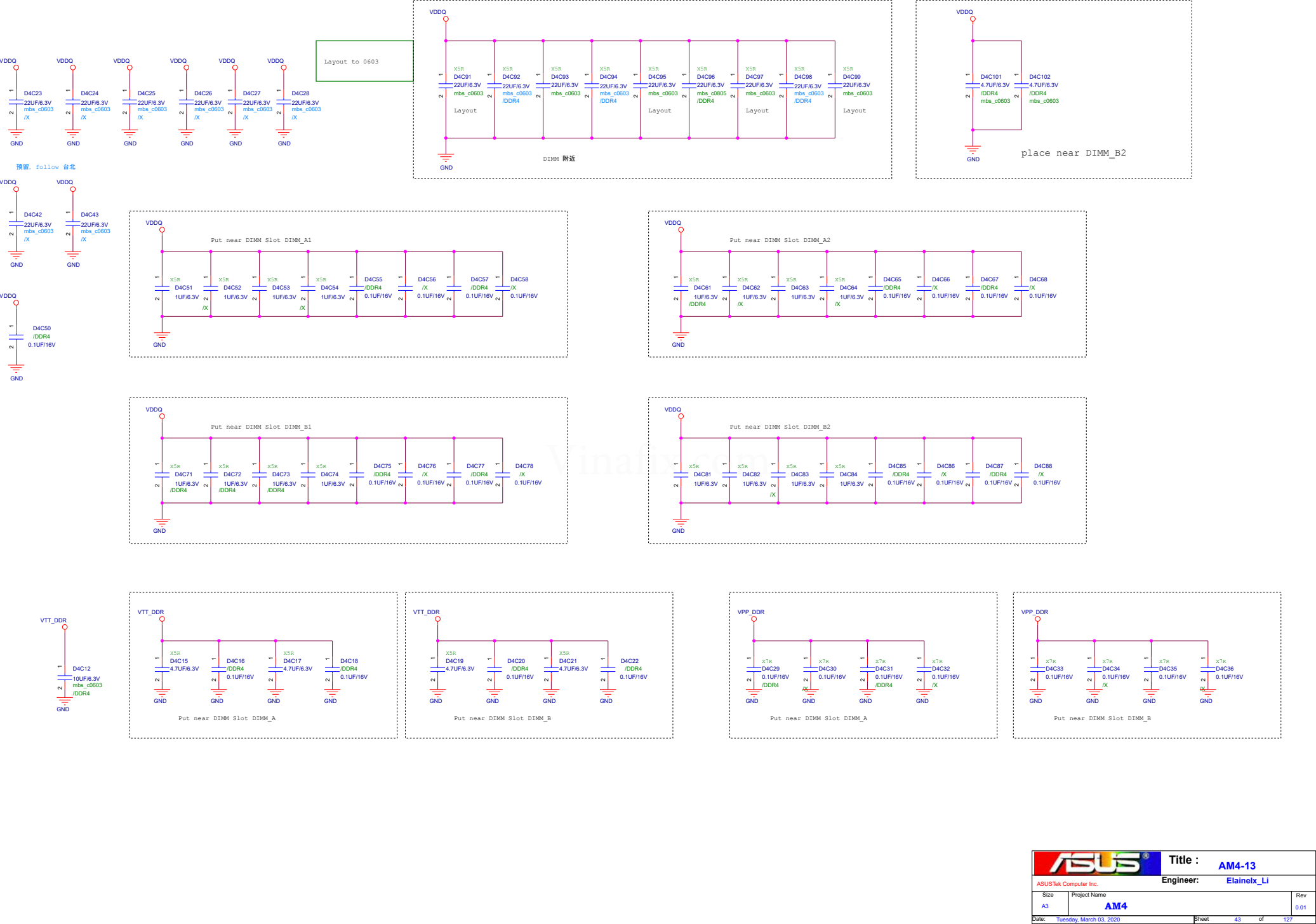
if ARN105 change to single resistor, use R0603(10V213300110)

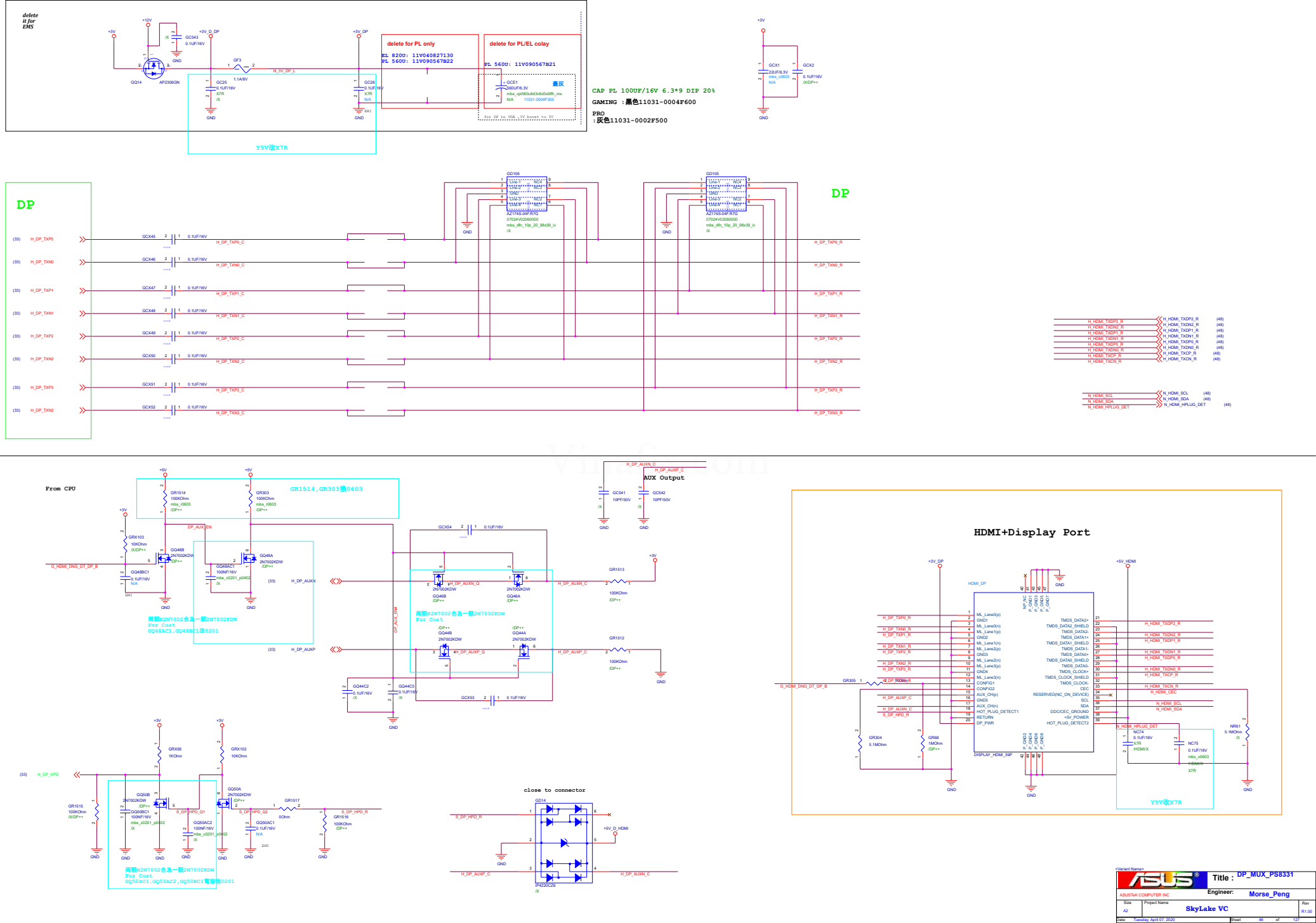
place under Audio Cover

Codec Cover LED

<Variant Name>

ASUSTEK COMPUTER INC	Title : Cover_LED	
	Engineer: SZ Design IP	
Size: A3	Project Name: AUDIO Demo Circuit	Rev: 0.0
Date: Monday, March 09, 2020	Sheet 79 of 127	


Layout to 0603
預留, follow 台北
DIMM 附近
place near DIMM_B2
Put near DIMM Slot DIMM_A1
Put near DIMM Slot DIMM_A2
Put near DIMM Slot DIMM_B1
Put near DIMM Slot DIMM_B2
Put near DIMM Slot DIMM_A
Put near DIMM Slot DIMM_B
Put near DIMM Slot DIMM_A
Put near DIMM Slot DIMM_B
Title : AM4-13
ASUSTek Computer Inc.
Engineer: Elainelx_Li
Size A3
Project Name AM4
Rev 0.01
Date: Tuesday, March 03, 2020
Sheet 43 of 127

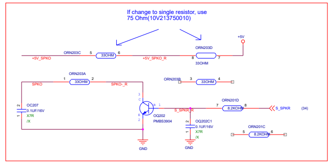


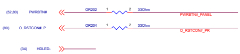
<Variant Name>
ASUSTeK COMPUTER INC
Title : DP_MUX_PS8331
Engineer: Morse_Peng
Size: A2
Project Name: SkyLake VC
Rev: R1.00
Date: Tuesday, April 07, 2020
Sheet 46 of 127

Panel Circuit

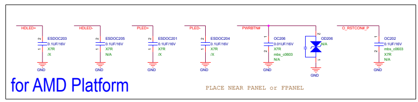
A. Choose PANEL/F_PANEL Signal ESD Solution by Project
B. Choose PANEL/F_PANEL Circuit + Chassis Inturder Circuit by Project
C. Choose Chassis Inturder Signal connect to SIO or Chipset by Project
D. Choose SPEAKER Header Circuit + BUZZER Circuit by Project
E. Choose PLED Circuit by Project
F. Choose PLED control by SIO or Chipset
G. If use Memory Power control PLED, check Memory Power Net Name
H. Modify Part Number of PANEL/F_PANEL/SPEAKER Header by Color

D.1



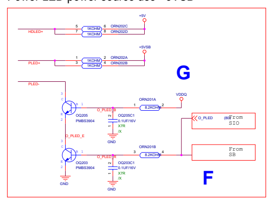


A.2



E.1

Power LED power source use +5VSB



BOM	need SPEAKER	no SPEAKER
/SPEAKER_4PIN	mount	unmount

BOM	need BUZZER	no BUZZER
/BUZZER	mount	unmount

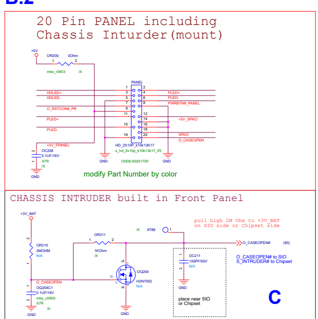
BOM	need CHASSIS	no CHASSIS
/CHASSIS	mount	unmount

O_PLED/S_PLED GPIO select:
1. GPIO with blink function, default GPI(no internal pull-down resistor)
2. stand by power plane, 3V tolerance
3. Porting Guide: default keep GPI, enable blink 0.5Hz or 1Hz function when enter S3, disable blink function and back to GPI when resume from S3

<Variant Name>

ASUSTEK COMPUTER INC	Title :	PANEL	
	Engineer:	SZ Design IP	
Size: Custom	Project Name	Super I/O Demo Circuit	Rev 0.0
Date: Friday, April 10, 2020	Sheet 82	of 127	

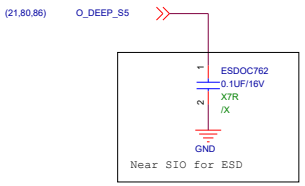
B.2



ERP Circuit

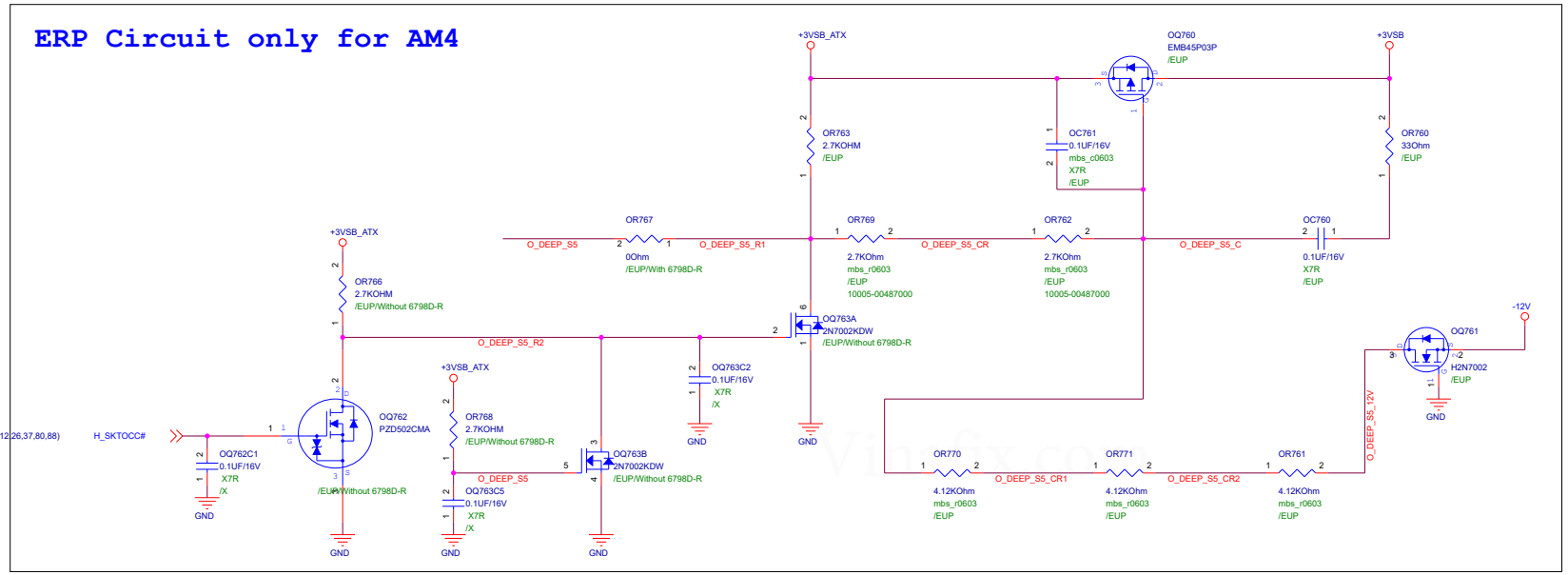
A. Choose ERP Circuit by Project

B. OR764, OR765 choose Short-Pin, Resistor or delete by Project

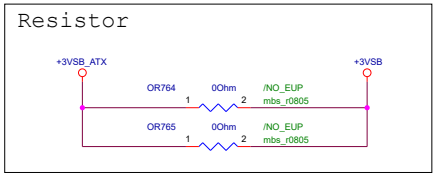


BOM	no SIO ERP & SIO DSW	SIO ERP	SIO DSW
/NO_EUP	mount	unmount	unmount
/EUP	unmount	mount	mount
/NO_SIODSW	mount	mount	unmount
/SIODSW	unmount	unmount	mount

A.3



B.2



<Variant Name>

ASUSTEK COMPUTER INC	Title : ERP	
	Engineer: SZ Design IP	
Size: A3	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Thursday, March 05, 2020	Sheet 84 of 127	

USBPWR_SW# Circuit for Nuvoton SIO GPIO

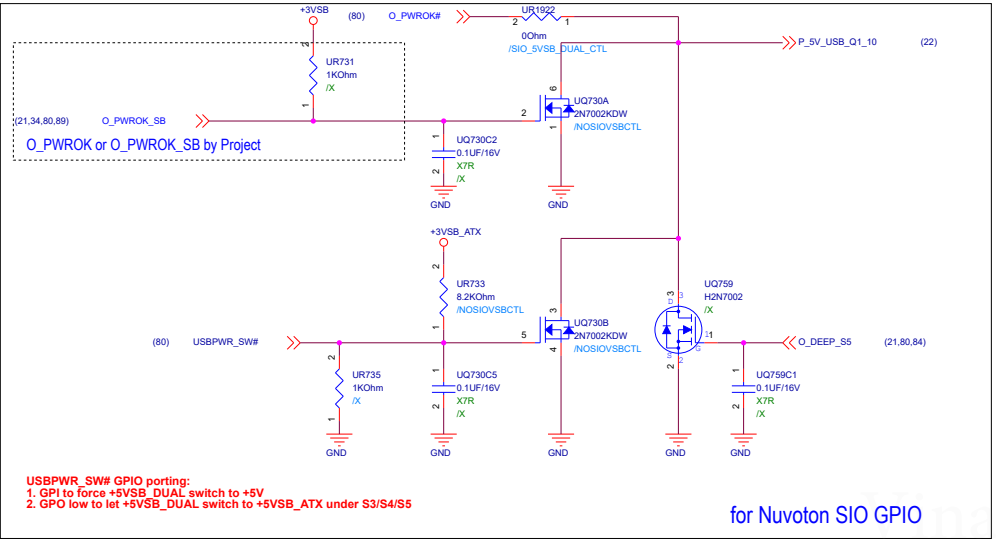
A. Choose USBPWR_SW# Circuit by Project

B. Modify PWROK Signal Name by Project

USBPWR_SW# GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor)
2. stand by power plane, 3V tolerance

A.1

+5VSB_DUAL default no power, reserve USB Inrush Circuit



A.2

+5VSB_DUAL default no power

A.3

+5VSB_DUAL default power on, mount USB Inrush Circuit

A.4

+5VSB_DUAL default power on, don't need GPIO control

<Variant Name>

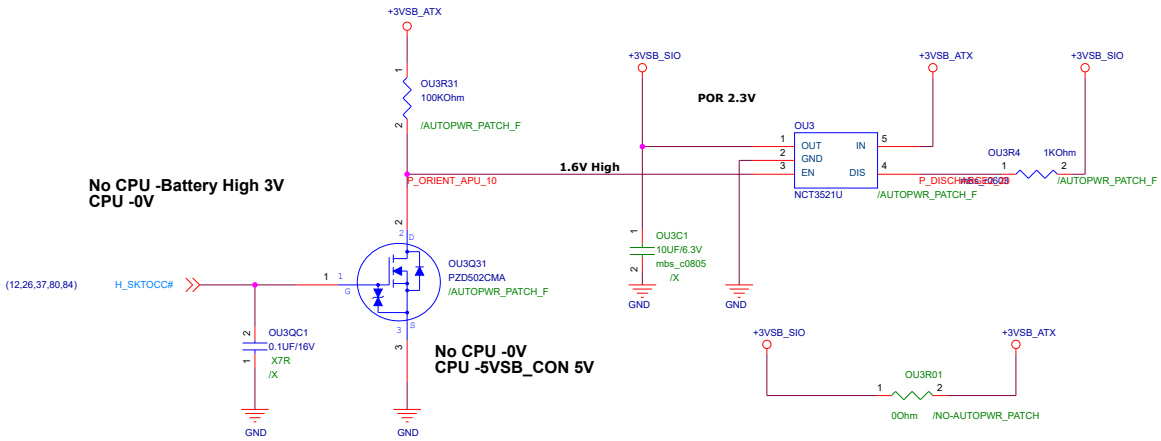
ASUSTEK COMPUTER INC	Title : USB Power Control	
	Engineer: SZ Design IP	
Size: Custom	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Wednesday, March 25, 2020	Sheet 86 of 127	

Onboard Debug LED Circuit

A. Move Debug LED Signal Off-Page Net Name to SIO IC Page

AUTO POWER ON PATCH Circuit

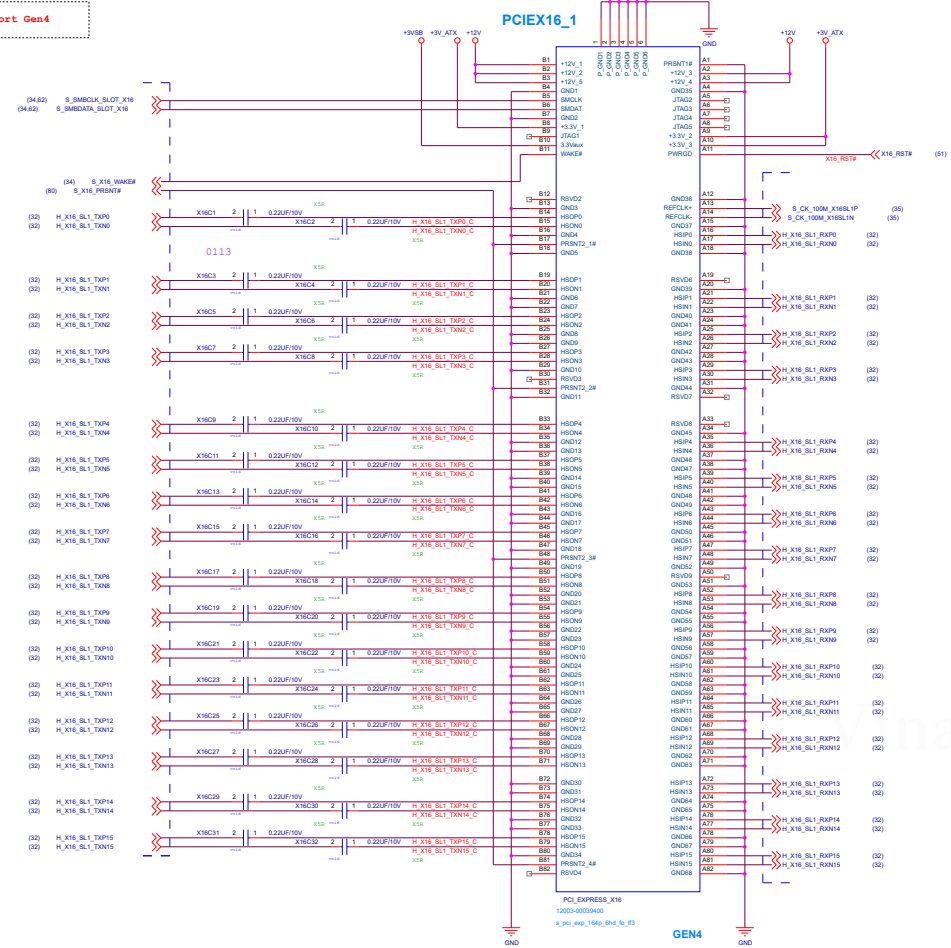
C.1

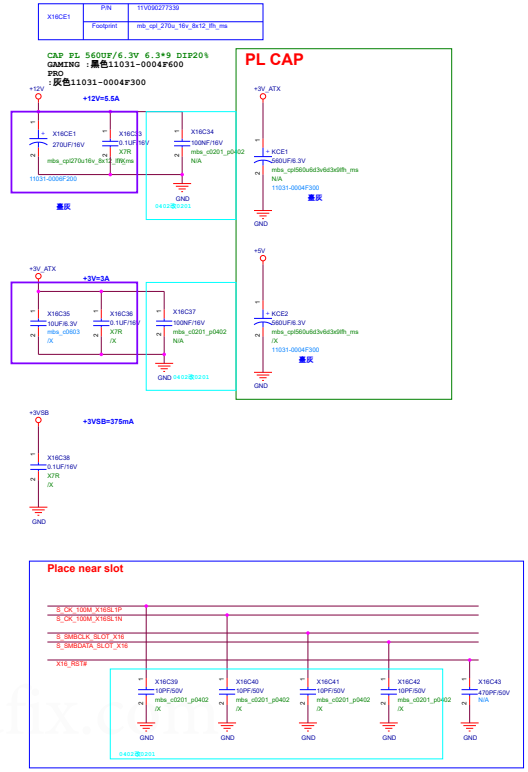


<Variant Name>

ASUSTEK COMPUTER INC	Title :	Debug LED	
	Engineer:	SZ Design IP	
Size: A3	Project Name: Super I/O Demo Circuit		Rev: 0.0
Date: Thursday, March 05, 2020	Sheet 88 of 127		

Support Gen4

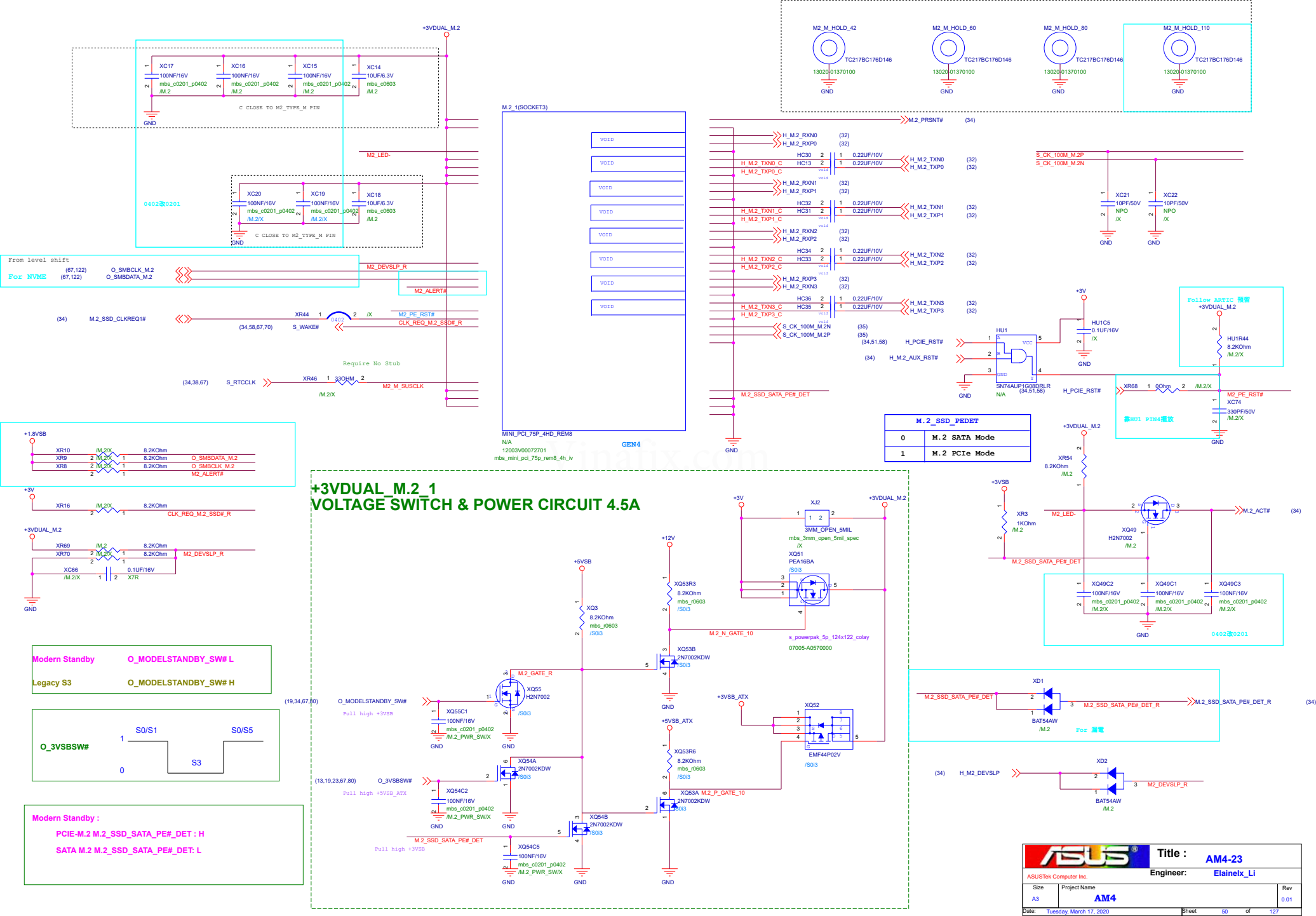


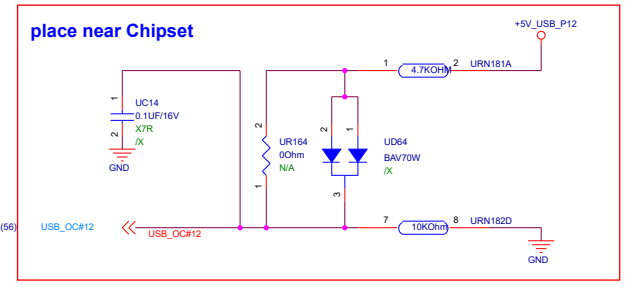


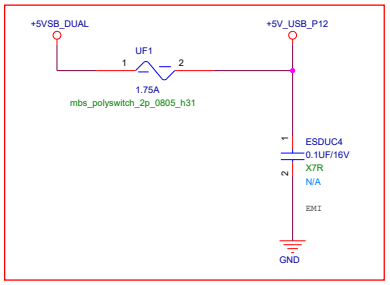
GEN3(GEN3本體+GEN4耳扣) 一般slot:12003-00381400

ROG STRIX: 12003-00039700 (黑色 鐵殼 亮線)
TUF GAMING: 12003-00039400 (灰色 鐵殼 亮線)

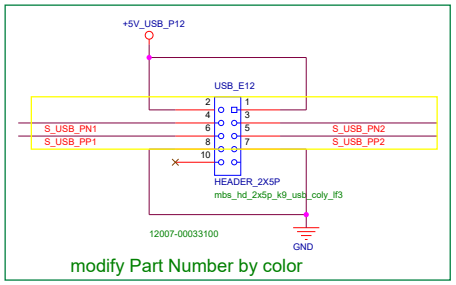
ASUSTek Computer Inc.	Title : AM4-21		
	Engineer: Elainelx_Li		
Size: A2	Project Name: AM4		Rev: 0.01
Date: Thursday, March 05, 2020	Sheet 49 of 127		


+3VDUAL_M.2_1
VOLTAGE SWITCH & POWER CIRCUIT 4.5A
M.2_1(SOCKET3)
MINI_PCI_75P_4HD_REM8
GEN4
M.2_SSD_PEDET
0 M.2 SATA Mode
1 M.2 PCIe Mode
Modern Standby O_MODELSTANDBY_SW# L
Legacy S3 O_MODELSTANDBY_SW# H
O_3VSBSW#
S0/S1
S0/S5
S3
Modern Standby :
PCIE-M.2 M.2_SSD_SATA_PE#_DET : H
SATA M.2 M.2_SSD_SATA_PE#_DET: L
From level shift
For NVME
Require No Stub
Title : AM4-23
Engineer: Elainelx_Li
ASUSTek Computer Inc.
Size A3
Project Name AM4
Rev 0.01
Date: Tuesday, March 17, 2020
Sheet 50 of 127

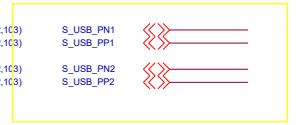


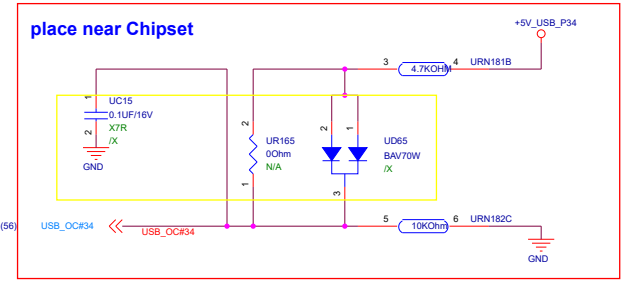


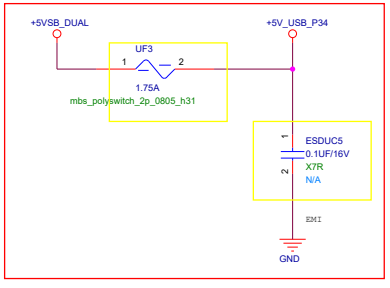
USB2 Header



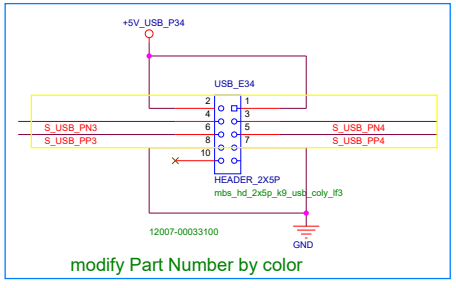
HUB USB



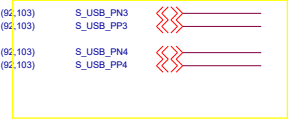


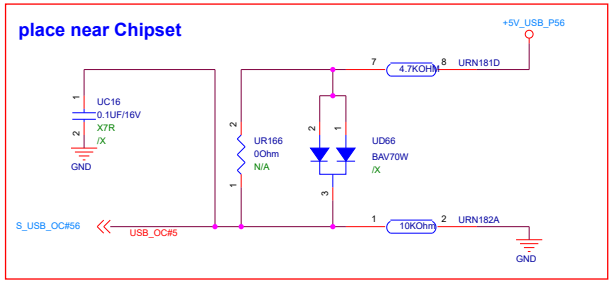


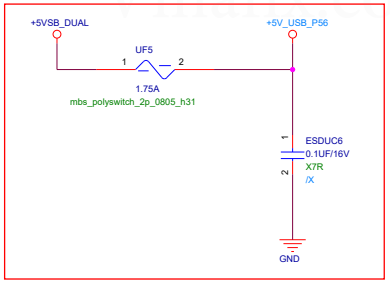
USB2 Header



HUB USB







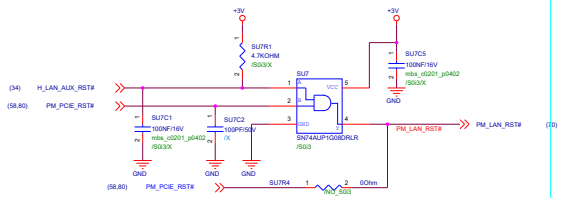
<Variant Name>

ASUSTEK COMPUTER INC	Title :	USB2 Port
	Engineer:	Kell_Huang
Size: A3	Project Name:	Chipset USB Demo Circuit
Rev: 0.0		
Date: Tuesday, April 07, 2020	Sheet 91 of 127	

WIFI

support S0i3:/X0i3 mount, /NO_S0i3 unmount
don't support S0i3:/X0i3 unmount, /NO_S0i3 mount

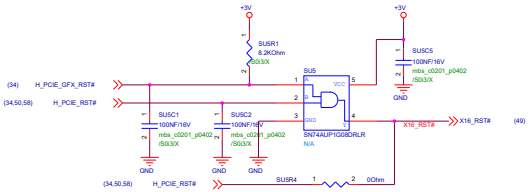
Onboard LAN



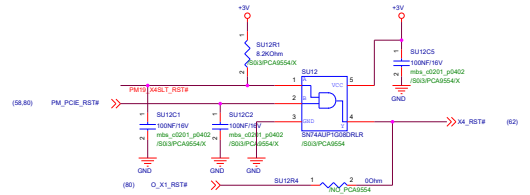
support S0i3:/X0i3 mount, /NO_S0i3 unmount
don't support S0i3:/X0i3 unmount, /NO_S0i3 mount

PCIEX16_1

@ CPU MOUNT

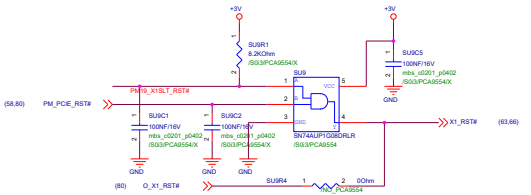


PCIEX16_2



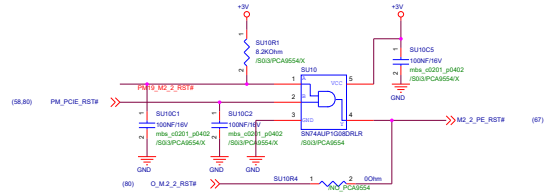
Default不走PCA9554:
1.Unmount:/PCA9554,/S0i3/PCA9554,/PCA9554/X,/S0i3/PCA9554/X
2.Mount:/NO_PCA9554

PCIEX1_1
PCIEX1_2

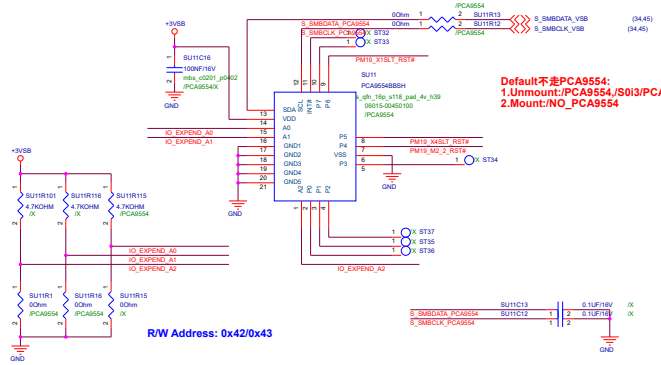


Default不走PCA9554:
1.Unmount:/PCA9554,/S0i3/PCA9554,/PCA9554/X,/S0i3/PCA9554/X
2.Mount:/NO_PCA9554

PCH M.2_2



Default不走PCA9554:
1.Unmount:/PCA9554,/S0i3/PCA9554,/PCA9554/X,/S0i3/PCA9554/X
2.Mount:/NO_PCA9554

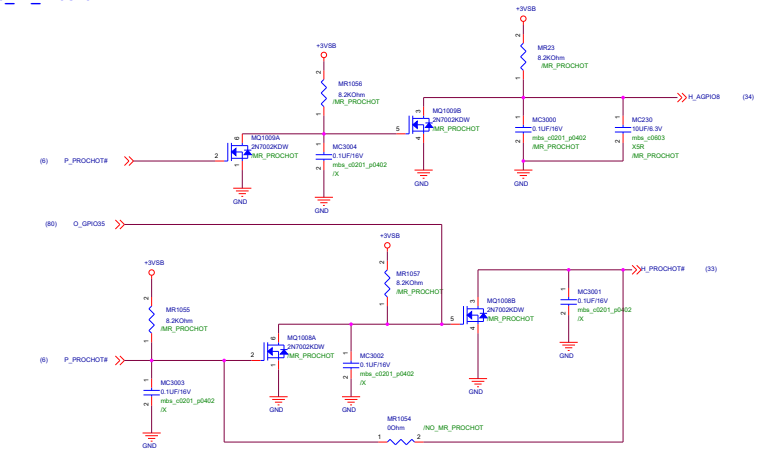


Default不走PCA9554:
1.Unmount:/PCA9554,/S0i3/PCA9554,/PCA9554/X,/S0i3/PCA9554/X,/X
2.Mount:/NO_PCA9554

MR PROCHOT

/MR_PROCHOT:
/NO_MR_PROCHOT:

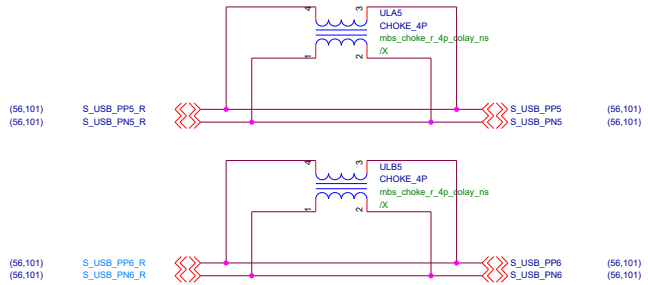
Default
unmount
mount



ASUSTek Computer Inc.	Title : M.2 SW		
	Engineer: Elainelx_Li		
Size: A2	Project Name: AM4		Rev: 0.01
Date: Friday, April 10, 2020	Sheet 51 of 127		

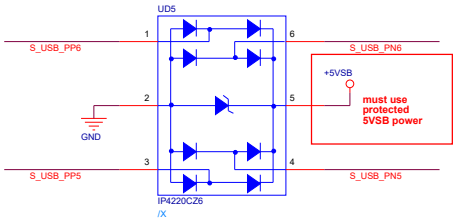
BACK LAN_USB56

Reserve Location (Single RES)



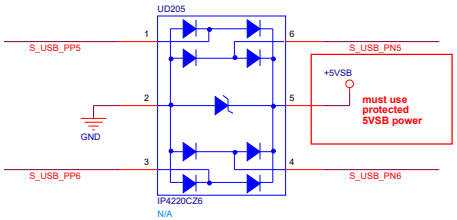
Delete it for EMS

ESD Diode



Delete it for EMS

ESD Diode



<Variant Name>

ASUSTEK COMPUTER INC

Title : USB3.1 Port

Engineer: Kell_Huang

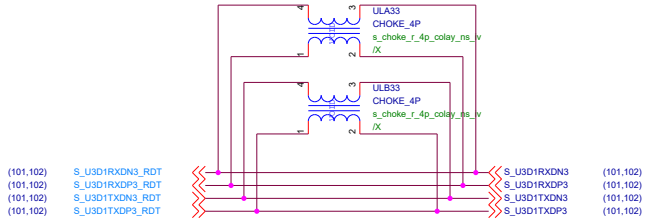
Size	Project Name	Rev
A3	Chipset USB Demo Circuit	0.0

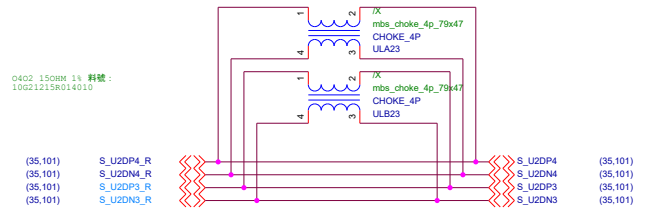
Date: Tuesday, March 17, 2020 Sheet 93 of 127

BACK IO

U32G2_3

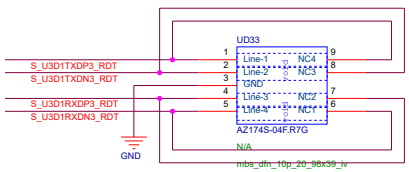
Reserve Location (Single RES)



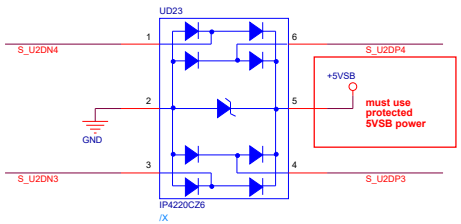


Delete it for EMS

ESD Diode

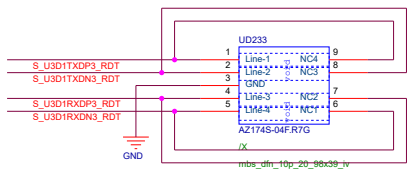


AZ174S

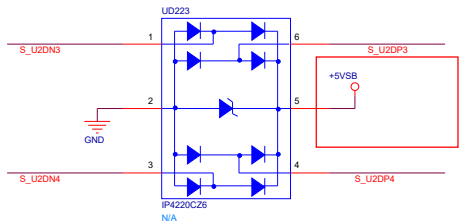


Delete it for EMS

ESD Diode



AZ174S



<Variant Name>

ASUSTEK COMPUTER INC

Title : USB3 Port

Engineer: Kell_Huang

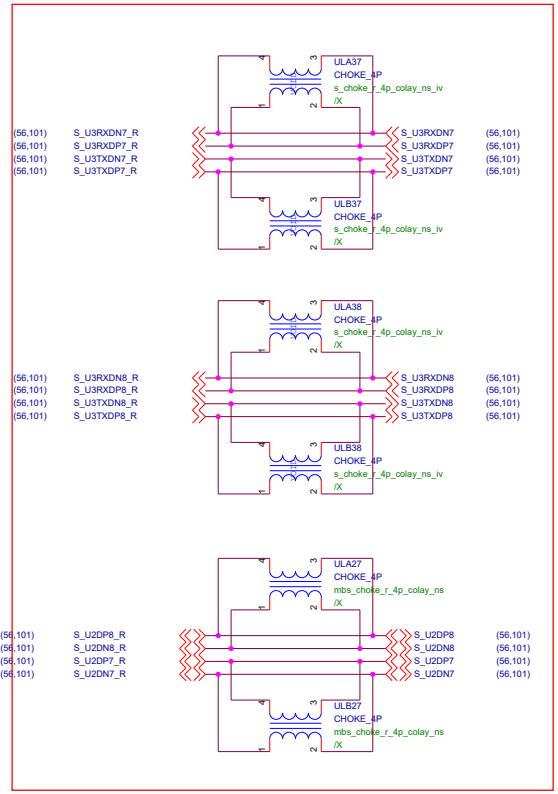
Size	Project Name	Rev
A3	Chipset USB Demo Circuit	0.0

Date: Tuesday, March 17, 2020 Sheet 96 of 127

PT PORT U32G1_78

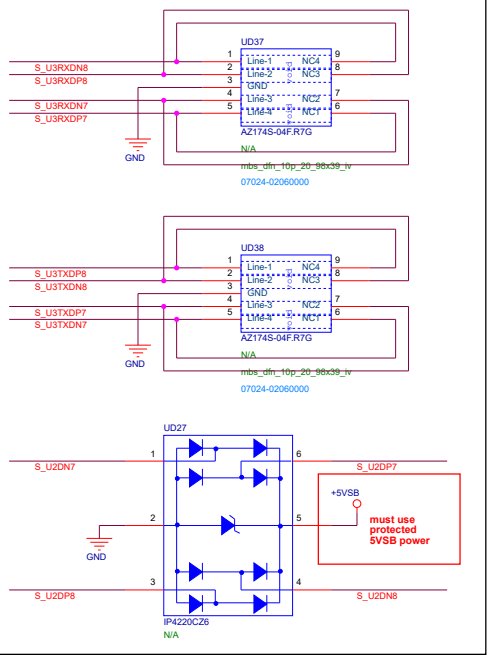
REDRIVER

Reserve Location (RES A)



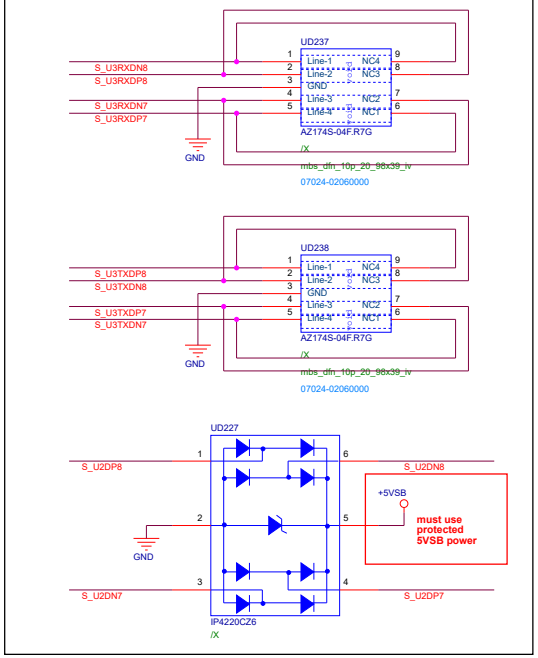
Delete it for EMS

ESD Diode



Delete it for EMS

ESD Diode



<Variant Name>

ASUSTEK COMPUTER INC	Title : USB3 Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Thursday, March 05, 2020	Sheet 98 of 127	

One USB 3.x Ports to One Type-C Connector/USB 3.1 Front Header Circuit_1

A. If don't need use or reserve Power Switch to control Type-C Connector Power, delete this block

B. Choose Single Port OC# Signal Circuit Type

C. Modify OC# Signal Net Name by Project

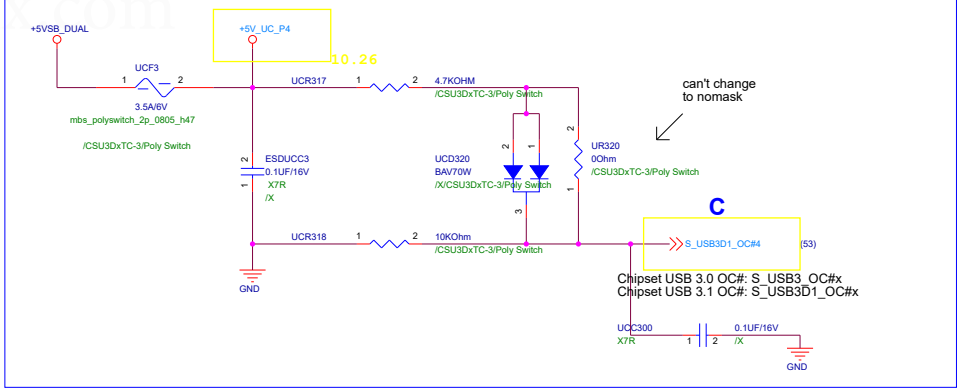
D. Choose DIP CAP Type

E. Modify Part Number of UCCE3 by Project

B.1

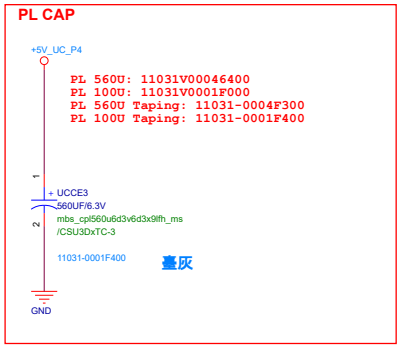
B.2

for Chipset OC# Pin with internal pull high



D.1

PL CAP



D.2

BOM	Type-C with Power Switch	Type-C with Poly Switch
/CSU3DxTC-3	mount	mount
/CSU3DxTC-3/Power Switch	mount	unmount
/CSU3DxTC-3/Poly Switch	unmount	mount

<Variant Name>

ASUSTEK COMPUTER INC

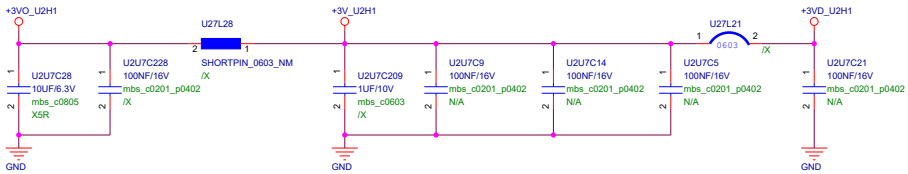
Title : CS U3.x Type-C

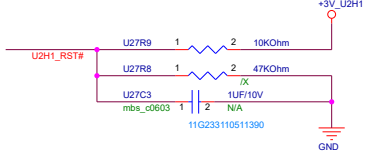
Engineer: SZ Design IP

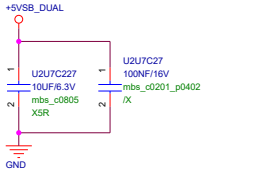
Size	Project Name	Rev
A3	Chipset USB Type-C Port	1.1A

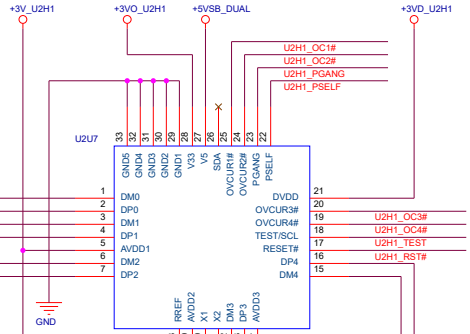
Date: Thursday, March 05, 2020 Sheet 100 of 127

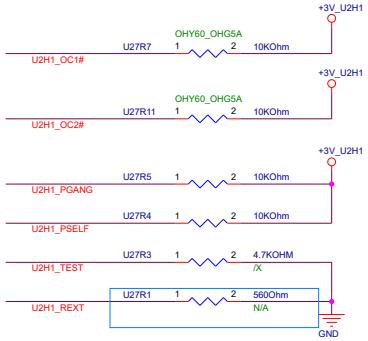
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 03, 2020	Sheet 54 of 127	











Manufacturer's suggested U27R1 680 OHM

chipset usb port

(56)	S_USB_PN6_HUB1
(56)	S_USB_PP6_HUB1

To Header USB_E34

(91,92)	U2H_DN3_R
(91,92)	U2H_DP3_R
(91,92)	U2H_DN4_R
(91,92)	U2H_DP4_R

Please refer to the current chipset demo for the hub to connector circuit

To Header USB_E12

(91,92)	U2H_DN1_R
(91,92)	U2H_DP1_R
(91,92)	U2H_DN2_R
(91,92)	U2H_DP2_R

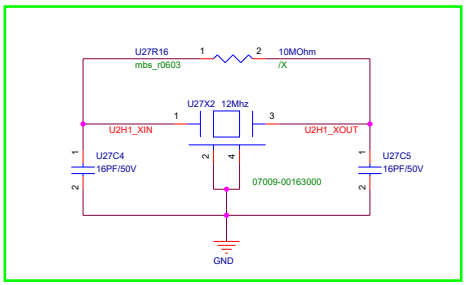
06039-00160200 C.S GL852G-OHY60

06039-00160000 C.S GL852G-OHG5A

02G730001401 C.S GL852G-OHG12

Select one to delete the other

SMD CRYSTAL



<Variant Name>

ASUSTEK COMPUTER INC	Title : GL852	
	Engineer: sky_tang	
Size: A3	Project Name: USB2 HUB Demo Circuit	Rev: 0.1B
Date: Tuesday, March 17, 2020	Sheet 103 of 127	

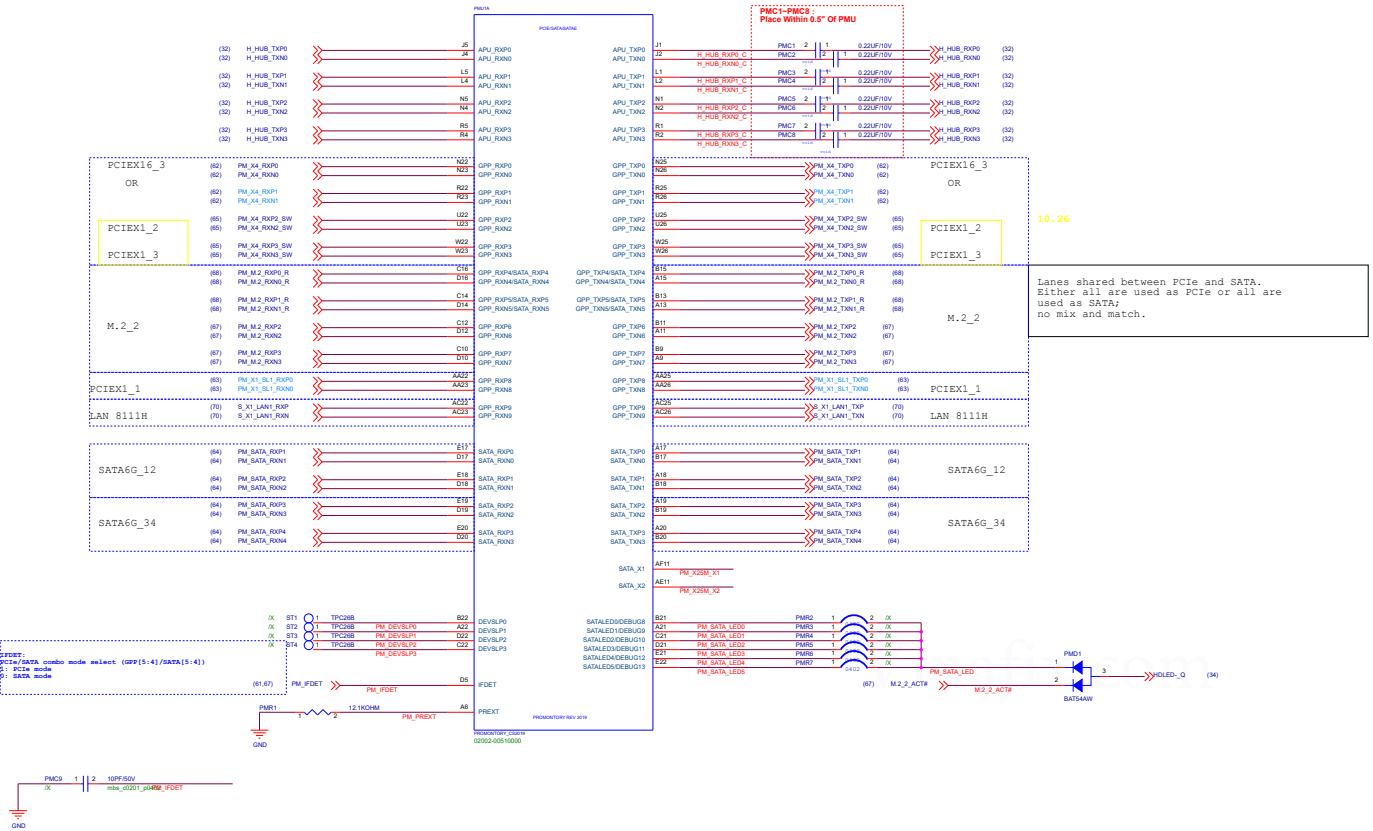


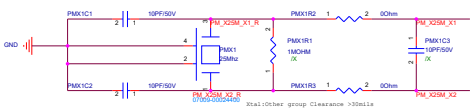
Table 1. GPP Configurations (Group 0-2)

Configuration	Group 0			
	LANE0	LANE1	LANE2	LANE3
0	X 1	X 1	X 1	X 1
1	X 2		X 1	X 1
2	X 1	X 1	X 2	
3	X2		X 2	
4	X 4			
Configuration	**Group 1**			
	LANE4	LANE5	LANE6	LANE7
0	X 1	X 1	X 1	X 1
1	X 2		X 1	X 1
2	X1	X1	X2	
3	X2		X2	
4	X 4			
Configuration	**Group 2**			
	LANE8	LANE9		
0	X1	X1		
1	X2			

Table 10. General Purpose PCI Express® Interface

Pin Name	Type	Voltage	Functional Description	Variant		
				A	C	D
GPP_RXP[3:0]	A-I	VDD105 VCC25	General purpose PCIe® Lane 3:0 receive positive	X	X	X
GPP_RXN[3:0]	A-I		General purpose PCIe Lane 3:0 receive negative	X	X	X
GPP_TXP[3:0]	A-O		General purpose PCIe Lane 3:0 transmit positive	X	X	X
GPP_TXN[3:0]	A-O		General purpose PCIe Lane 3:0 transmit negative	X	X	X
GPP_RXP[5:4]/SATA_RXP[5:4]	A-I		General purpose PCIe Lane 5:4 receive positive	X	X	X
GPP_RXN[5:4]/SATA_RXN[5:4]	A-I		General purpose PCIe Lane 5:4 receive negative	X	X	X
GPP_TXP[5:4]/SATA_TXP[5:4]	A-O		General purpose PCIe Lane 5:4 transmit positive	X	X	X
GPP_TXN[5:4]/SATA_TXN[5:4]	A-O		General purpose PCIe Lane 5:4 transmit negative	X	X	X
GPP_RXP[9:6]	A-I		General purpose PCIe Lane 9:6 receive positive		X	X
GPP_RXN[9:6]	A-I		General purpose PCIe Lane 9:6 receive negative		X	X
GPP_TXP[9:6]	A-O		General purpose PCIe Lane 9:6 transmit positive		X	X
GPP_TXN[9:6]	A-O		General purpose PCIe Lane 9:6 transmit negative		X	X

SMD Crystal



Crystal Intel在使用的用料

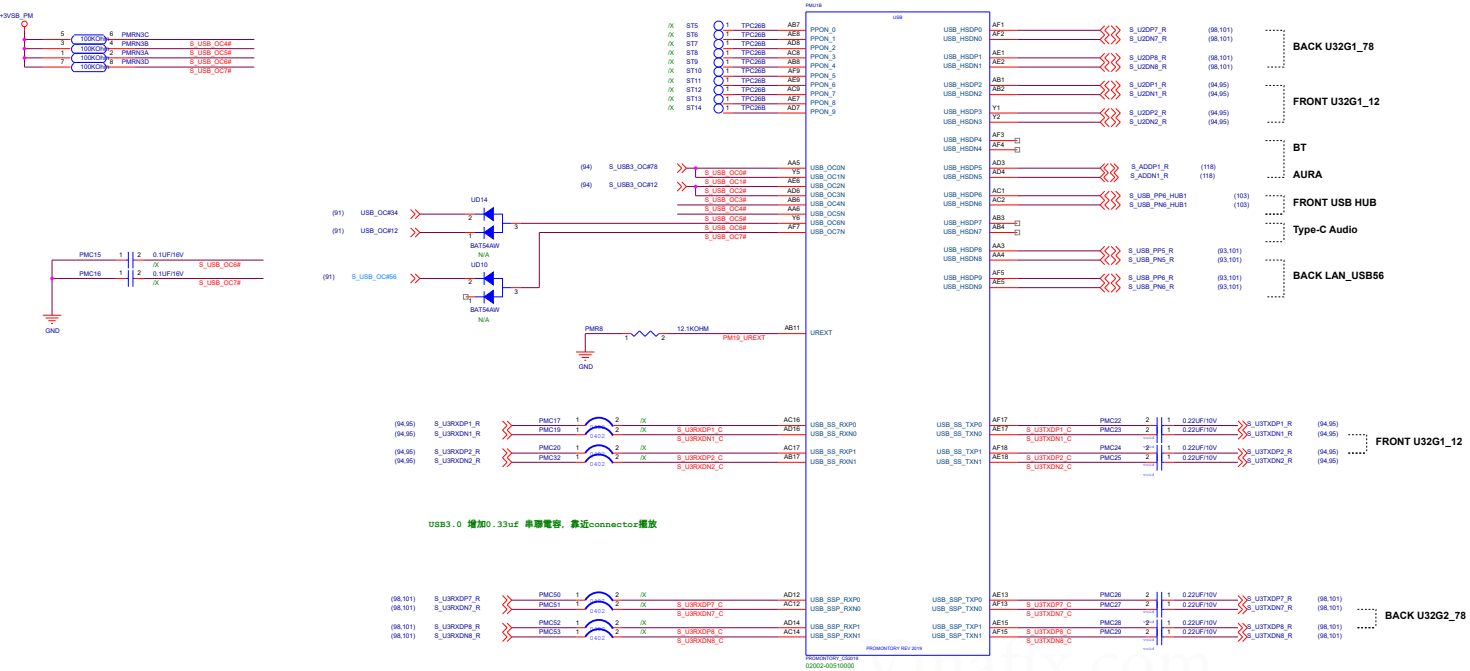


Table 13. USB Port to OC Pin Mapping

USB 3.2 G2 (10 Gbps)	USB2.0	USB_OC
USB_SSP_TX/RX[0]	USB_HSDP/N[0]	USB_OC0N
USB_SSP_TX/RX[1]	USB_HSDP/N[1]	USB_OC1N
USB 3.2 G1 (5 Gbps)	**USB2.0**	**USB_OC**
USB_SS_TX/RX[0]	USB_HSDP/N[2]	USB_OC2N
USB_SS_TX/RX[1]	USB_HSDP/N[3]	USB_OC3N
	USB_HSDP/N[4]	USB_OC4N
	USB_HSDP/N[5]	USB_OC5N
	USB_HSDP/N[6]	USB_OC6N
	USB_HSDP/N[7]	USB_OC7N
	USB_HSDP/N[8]	USB_OC7N
	USB_HSDP/N[9]	USB_OC7N

<Variant Name>

Title : PROMONTORY 2019 CHIPSET USB

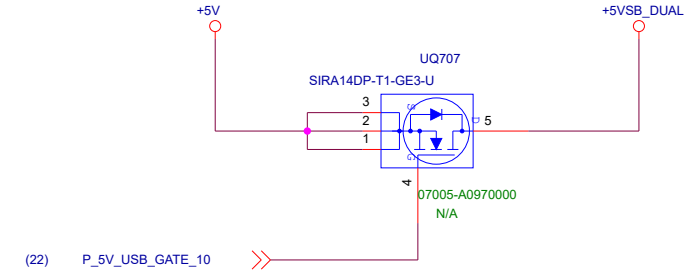
ASUSTek COMPUTER INC.

Engineer:

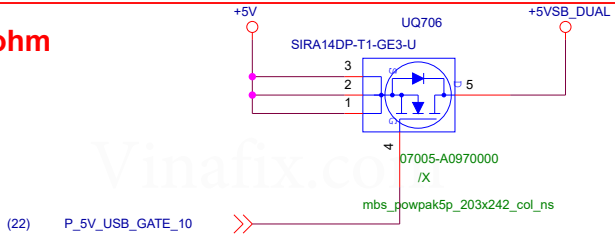
Size	Project Name	Rev
A2	AM4	01.00

Date: Thursday, March 05, 2020 Sheet 56 of 127

DPAK MOS 9 mohm



DPAK MOS 9 mohm



NIKO DPAK 9mohm: 07005-00380000

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, April 10, 2020	Sheet 105 of 127	

<Core Design>

Title : EEPROM/SMBus/USB

ASUSTek Computer Inc.

Engineer: Tom Yang

Size	Project Name	Rev
Custom	**Standard Circiut**	0.5A

Date:	Tuesday, March 03, 2020	Sheet	107	of	127

<Variant Name>

	Title :	ALC210
ASUSTEK COMPUTER INC	Engineer:	SZ Design IP

Size	Project Name	Rev
Custom	AUDIO Demo Circuit	0.0

Date:	Tuesday, March 03, 2020	Sheet	109	of 127

ASUS PCB Logo Circuit

A. Choose ASUS Logo by Project

B. Choose KCC Logo by Project

C. Choose Model Name text size by Project

D. Keep or remove NEED_COMP_SILK by Project

A

with R

1.5mm without R

2mm without R

2.5mm without R

3mm without R

3.5mm without R

4mm without R

4.5mm without R

5mm without R

5.5mm without R

6mm without R

LOGO2 — FCC — FCC /X

LOGO7 — PCB MADE IN CHINA — PCB_MADE_IN_CHINA /X

PCB MADE IN CHINA

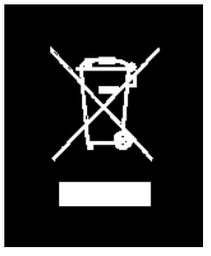
LOGO3 — RCM — RCM /X

LOGO9 — CAN ICES-3(B)/NMB-3(B) — CAN_ICES_3B_NMB_3B /X

LOGO1 — EMI_D33005_H — EMI_D33005_H /X

LOGO8 — VCCI — VCCI /X

LOGO5 — WEEE_LOGO — WEEE_LOGO /X



LOGO6 — CE — CE /X

LOGO11 — SFIS LABEL — SFIS_LABEL /X

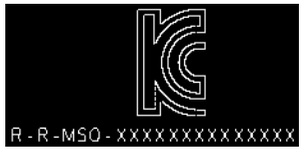
SFIS

B

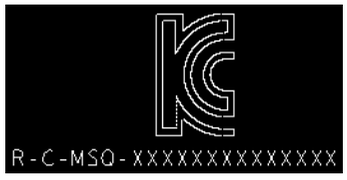
KCC R-R 10mm

LOGO10 — KC R-R-MSQ-XXXXXXXXXXXXXX — KC_R_R_LOGO /X

KCC Logo R-R



KCC Logo R-C



C

Model Name on PCB Bottom Side

Size 2 for Motherboard

MN4 — RX. XX — RX_XX_T4 /X

Size 4 for Add-on Card

LOGO12 — UKRAINE LOGO — UKRAINE LOGO /X

D

<Variant Name>

ASUSTEK COMPUTER INC	Title :	PCB Logo
	Engineer:	SZ Design IP
Size: Custom	Project Name:	Silkscreen Demo Circuit
Rev: 1.1A		
Date: Friday, April 10, 2020	Sheet 111 of 127	

Fiducial Mask
(光學點)

Delete it for EMS

圓形光學點

LayoutRD會依空間大小，
擺放大顆或小顆光學點；
所以兩種光學點都需畫入線路中，
最後再做刪除.

大顆光學點

小顆光學點

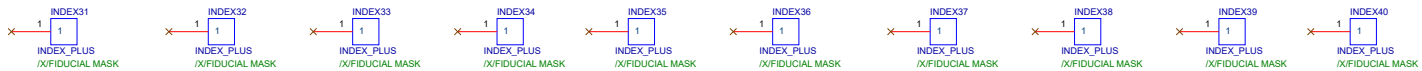
Delete it for EMS

十字光學點

LayoutRD會依空間大小，
擺放大顆或小顆光學點；
所以兩種光學點都需畫入線路中，
最後再做刪除.

大顆光學點

小顆光學點



<Variant Name>

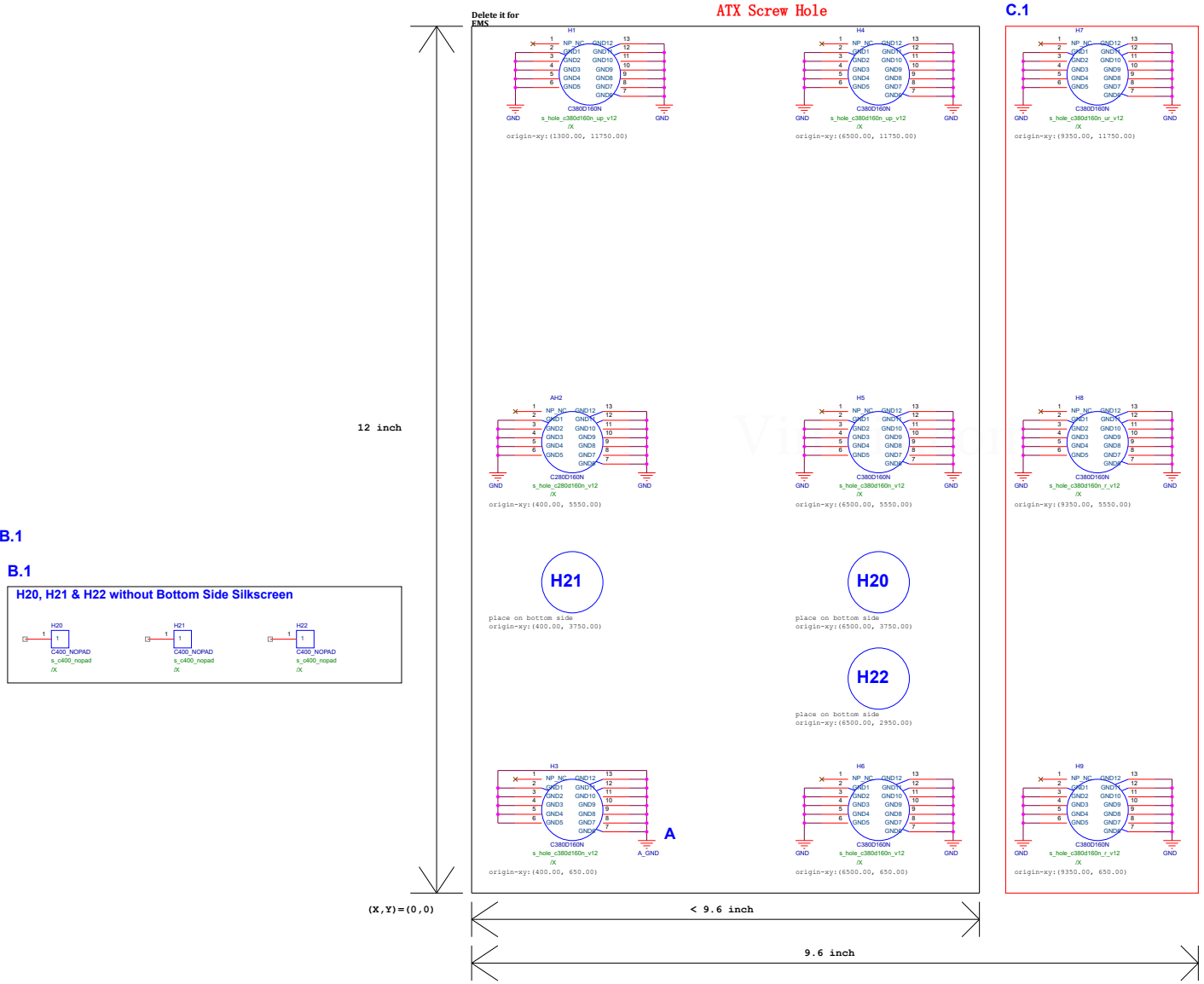
ASUSTEK COMPUTER INC	Title : Fiducial Mask	
	Engineer: SZ Design IP	
Size: A3	Project Name: Silkscreen Demo Circuit	Rev: 1.1A
Date: Tuesday, March 03, 2020	Sheet 113 of 127	

ATX Screw Hole Circuit

A. Connect H3 to GND or A_GND by Project

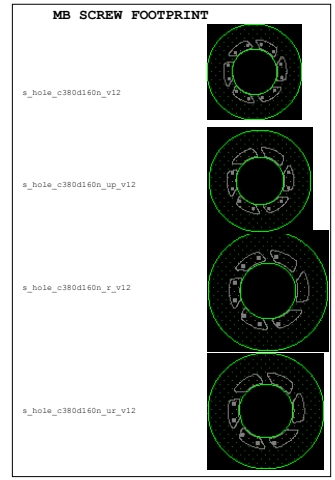
B. Choose Bottom Side Silkscreen of H20, H21 & H22 by Project

C. Choose H7, H8, H9 by Project



B.1

B.1



ATX Screw Select

	Standard (12 x 9.6)	Scale down (12 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	V
H7	V	X
H8	V	X
H9	V	X
H20	V	V
H21	V	V
H22	V	V

<Variant Name>

ASUSTEK COMPUTER INC

Title : Screw Hole

Engineer: SZ Design IP

Size: Custom | Project Name: Other Demo Circuit | Rev: 1.1C

Date: Wednesday, April 15, 2020 | Sheet 115 of 127

SPI TPM Circuit

A. Del SPI TPM Header if don't need

B. Modify Part Number of SPI TPM Header by Color

C. Del Onboard SPI TPM IC if don't need

D. Modify Onboard SPI TPM IC's Part Number by Project

E. If have 2nd BIOS Flash, connect 2nd BIOS Flash's CS# signal to SPI_TPM Header Pin 5

F. Check +VCC_SPI_TPM should have the same power source with SPI Controller

G. Check pull high power of S_SPI_TPM_IRQ# by Project

H. Modify Onboard SPI TPM IC Pin18's BOM by Project

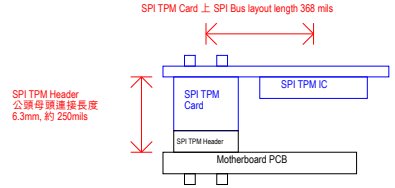
BOM	TMR22	TMQ22, TMR25 & TMR26
+VCC_SPI_TPM use 3V level Power S_SPI_TPM_IRQ# use 3V level Pin	mount	unmount
+VCC_SPI_TPM use 1.8V level Power S_SPI_TPM_IRQ# use 1.8V level Pin	mount	unmount
+VCC_SPI_TPM use 3V level Power S_SPI_TPM_IRQ# use 1.8V level Pin	unmount	mount
+VCC_SPI_TPM use 1.8V level Power S_SPI_TPM_IRQ# use 3V level Pin	unmount	mount

I. Modify Onboard SPI TPM IC Pin17's BOM by Project

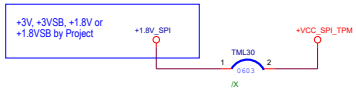
BOM	TMR21	TMQ21, TMR23 & TMR24
+VCC_SPI_TPM use 3V level Power PLTRST# use 3V level signal	mount	unmount
+VCC_SPI_TPM use 1.8V level Power PLTRST# use 1.8V level signal	mount	unmount
+VCC_SPI_TPM use 3V level Power PLTRST# use 1.8V level signal	unmount	mount
+VCC_SPI_TPM use 1.8V level Power PLTRST# use 3V level signal	unmount	mount

J. Check Off-page Signals & Power Net Name by Project

K. SPI Bus Trace length of SPI TPM Header & SPI TPM Card is 618 mils as below

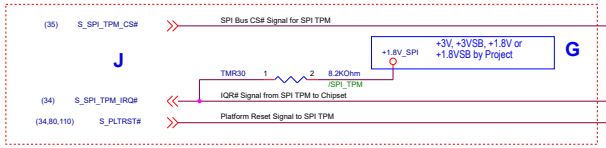


F

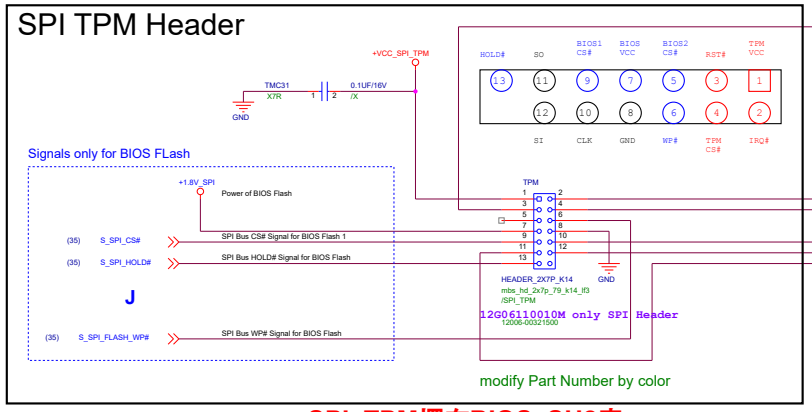


BOM	SPI TPM Header	Onboard SPI TPM
/SPI TPM	mount	mount
/X	unmount	unmount
/SPI TPM HEADER	mount	unmount
/SPI TPM IC	unmount	mount

Signals only for SPI TPM



A



SPI_TPM擺在BIOS_SU2旁

Signals for both BIOS Flash and SPI TPM

BOM	LPC TPM Header	Onboard LPC TPM
N/A	mount	mount
/X	unmount	unmount
/LPC TPM HEADER	mount	unmount
/LPC TPM IC	unmount	mount

<Variant Name>

ASUSTEK COMPUTER INC

Title : SPI TPM

Engineer: SZ Design IP

Size: Custom | Project Name: Other Demo Circuit | Rev: 1.0G

Date: Thursday, April 09, 2020 | Sheet 116 of 127

Addressable Header

Ver 1.6

LED Driver對LED內部的Net

LED Driver需連接外部的Net

根據ID規格可更換其他功能的Pin腳

依據Intel/AMD平台修改Power net

依據ID規格/空間，刪減LED組數/顆數/Header

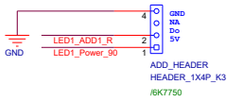
註解

Addressable Header(支援1組)

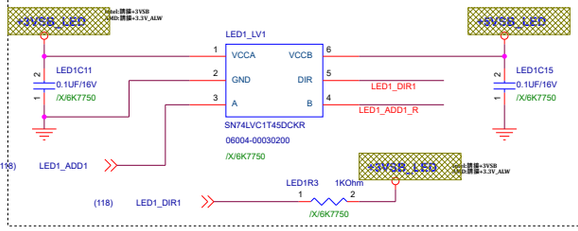
第1組

ADD LED Power

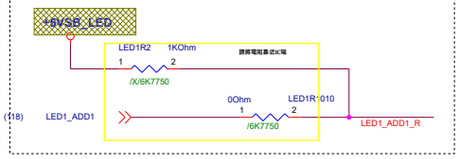
Addreesable LED Header



ADD訊號接雙向LVS



ADD訊號接pu high (預設上件)

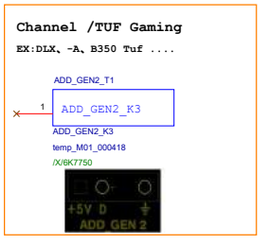


20190312修改

20190219修改

ADD_HEADER 反白文字面

(請依主機板類型選擇對應的文字面)



<Variant Name>

ASUSTek Computer Inc.

Title : ADD_Header

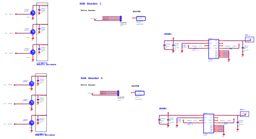
Engineer: Kaizer_Luo

Size	Project Name	Rev
Custom	LED Standard Circiut	1.0

Date: Thursday, March 05, 2020 Sheet 119 of 127

Ver 1.0

5.兩組燈條以上的情境



預留M.2的SMBUS接至SIO的Pin51、Pin52

Ver 1.4

(支援未來有AURA的M.2 Device)

LED Driver對LED內部的Net

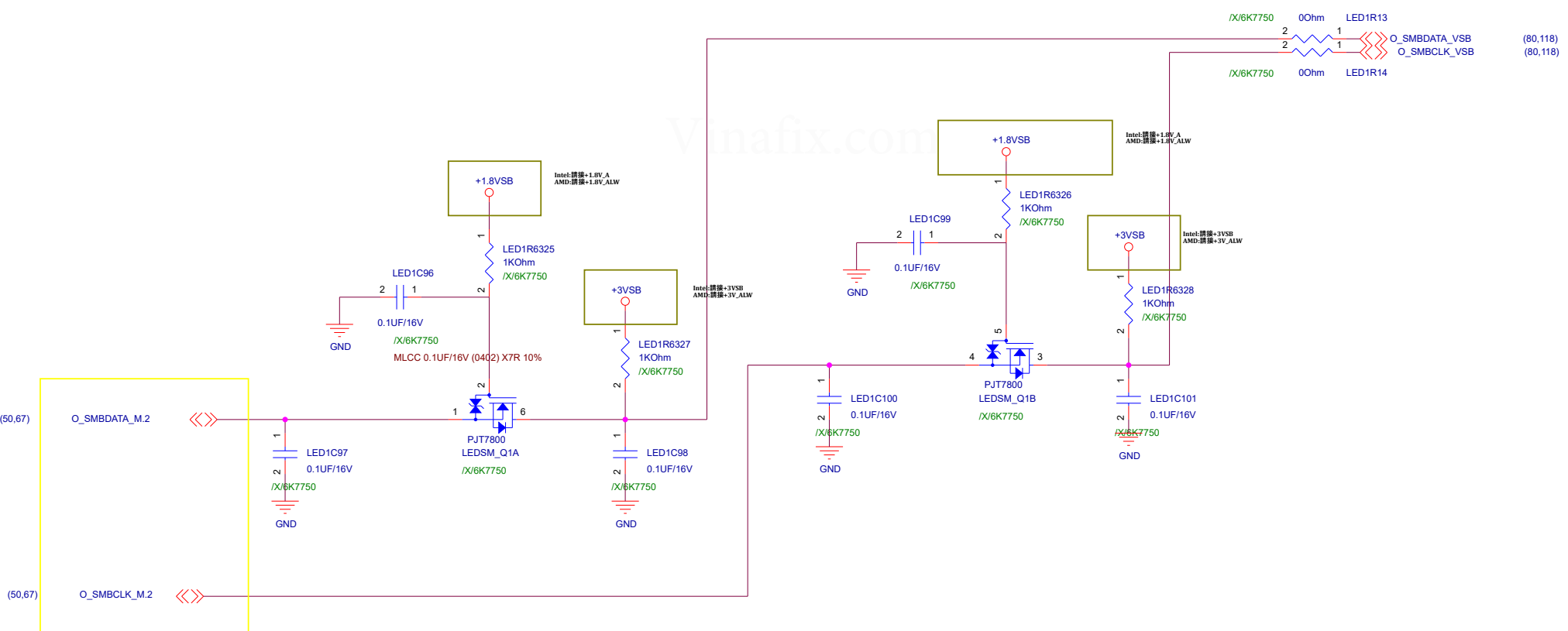
LED Driver需連接外部的Net

根據ID規格可更換其他功能的Pin腳

依據Intel/AMD平台修改Power net

依據ID規格/空間，刪減LED組數/顆數/Header

註解



若有1個或2個M.2 connector
請各預留pu high1.8V電阻在M.2端的pin40/42/44

<Variant Name>

ASUSTek Computer Inc.	Title : M.2_SMBUS	
	Engineer: Kaizer_Luo	
Size: Custom	Project Name: LED Standard Circiut	Rev: 1.0
Date: Thursday, March 05, 2020	Sheet 122 of 127	

<Variant Name>

Title : M.2 Key E

ASUSTeK COMPUTER INC

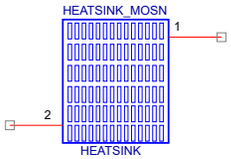
Engineer: Likes_Li

Size	Project Name	Rev
A2	M.2 Key E	0.4A

Date:	Tuesday, March 03, 2020	Sheet	123	of	127

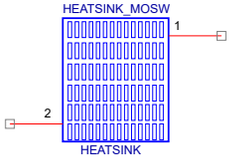
heatsink thermal symbol

MN HS



PRIME B550-PLUS_MOS-N_SINK
temp_T_003895
s_hsk_2p_3210x102
/X

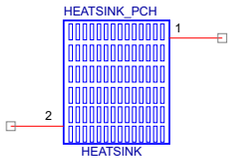
MW HS



temp_T_003894
s_hsk_2p_1834x3952
PRIME B550-PLUS_MOS-W_SINK
/X

M2 HS

PCH HS

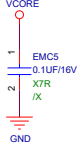


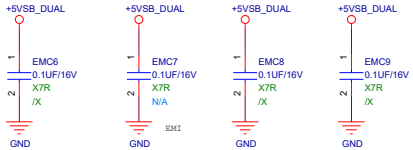
temp_T_003808
s_hsk_2p_1890x3071_mole
/X

TUF B450M PRO GAMING MOS HS

<Variant Name>

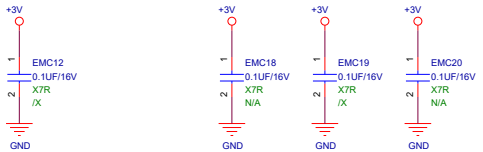
ASUSTeK COMPUTER INC	Title : HEAT SINK	
	Engineer: KENNY_CHEN	
Size: A3	Project Name: Z87-PRO	Rev: R1.02A
Date: Monday, March 09, 2020	Sheet 125 of 127	

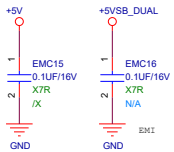




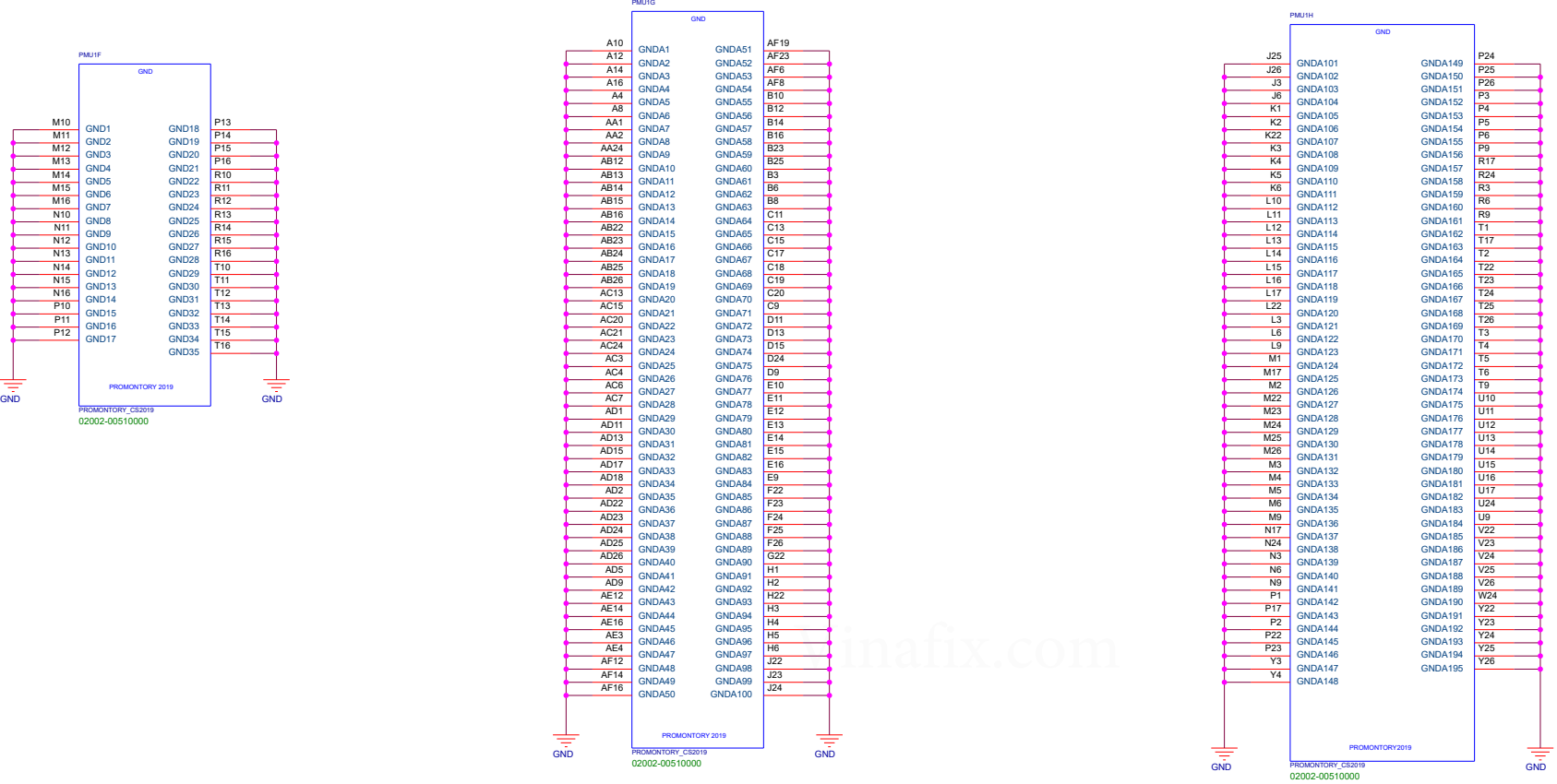
EMI: 0.1UF: ESDUC4, ESDUC5, ESDUC31, GC26, GQ48BC1, GQ50AC1, EMC7, EMC16, ESDUC34

擺放在differential信號換層處





Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 07, 2020	Sheet 126 of 127	



<Variant Name>

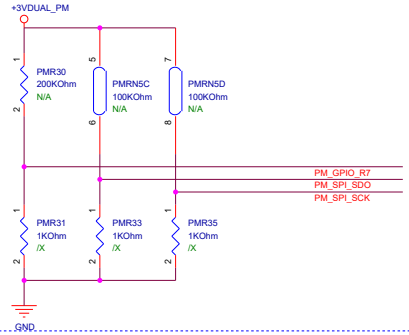
ASUSTek COMPUTER INC.

Title : PROMONTORY2019(GND)

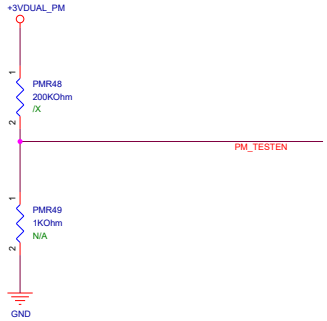
Engineer:

Size	Project Name	Rev
A3	AM4	R1.00

Date: Tuesday, March 03, 2020 Sheet 60 of 127

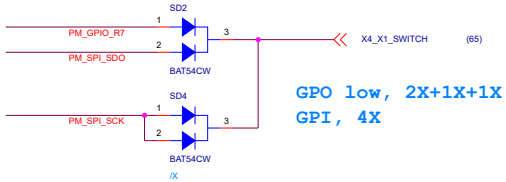


GPP Group 0 (Lanes 3:0)			
PM_GPIO_R7	PM_SPI_SDO	PM_SPI_SCK	Function
1	1	1	1 PCIe x4
0	1	1	1 PCIe x2 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	0	0	4 PCIe x1
Others:Reserved			

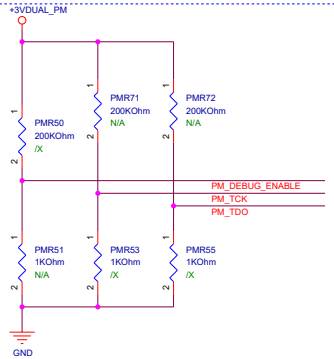


Test mode enable	
PM_TESTEN	Function
1	Test mode
0	Function Mode

PCIEX4與PCIEX1切換

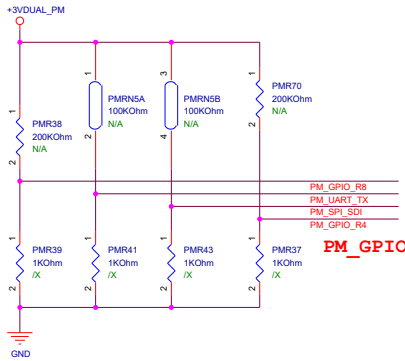


GPO low, 2X+1X+1X
GPI, 4X



Debug mode enable	
PM_DEBUG_ENABLE	Function
1	Debug mode
0	Function Mode

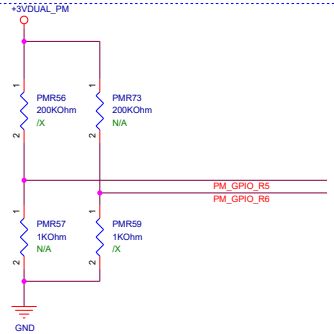
Debug mode		
PM_TCK	PM_TDO	Function
1	1	Debug signal group 3 output
1	0	Debug signal group 2 output
0	1	Debug signal group 1 output
0	0	Debug signal group 0 output



GPP Group 1 (Lanes 7:4)			
PM_GPIO_R8	UART_TX	PM_SPI_SDI	Function
1	1	1	1 PCIe x4
0	1	1	1 PCIe x2 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	0	0	4 PCIe x1
Others:Reserved			

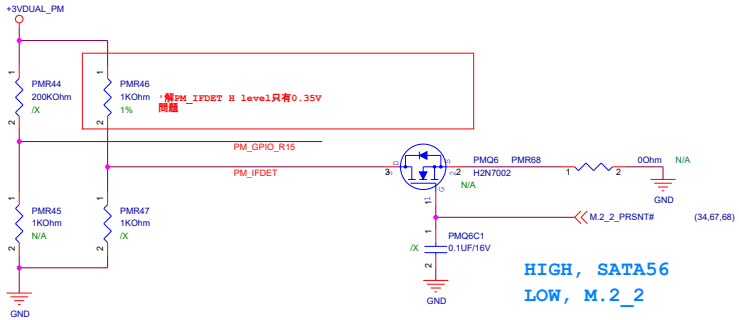
PM_GPIO_R8 can work only when PM_GPIO_R4 strap =0.

PM_GPIO_R4	Function
1	GPP / Clock buffer clock source from APU_CLKP/N
0	GPP / Clock buffer clock source from Crystal



USB SSC Enable	
PM_GPIO_R5	Function
1	USBC SSC disable
0	USBC SSC enable

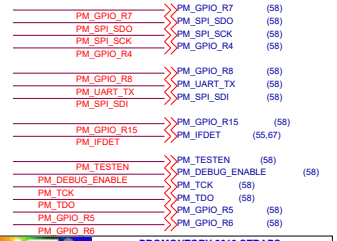
SATA SSC Enable	
PM_GPIO_R6	Function
1	SATA SSC disable
0	SATA SSC enable



HIGH, SATA56
LOW, M.2_2

GPP Group 2 (Lanes 9:8)	
PM_GPIO_R15	Function
1	1 PCIe x2
0	2 PCIe x1

PCIe/SATA combo mode select (GPP[5:4]/SATA[5:4])	
PM_IFDET	Function
1	PCIe mode
0	SATA Mode



ASUSTek Computer Inc.

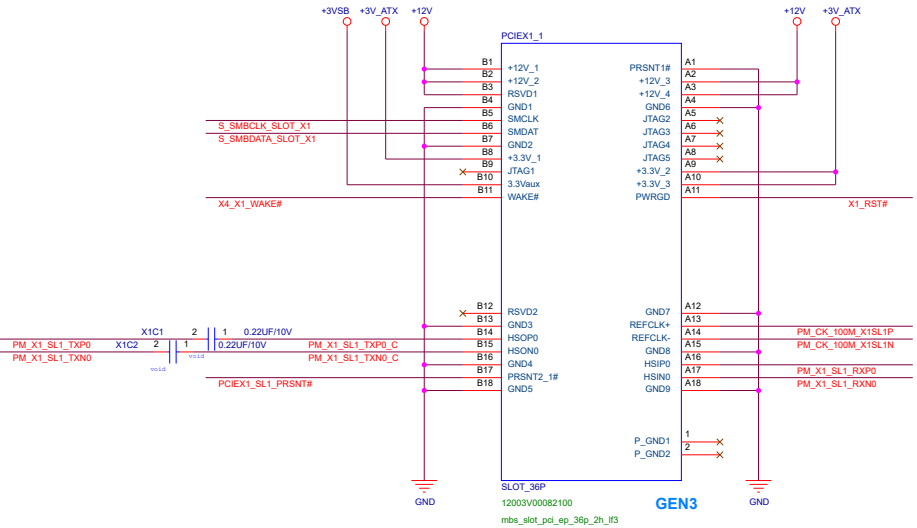
Title: PROMONTORY 2019 STRAPS

Engineer: ElaineIx_Li

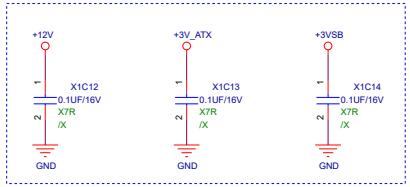
Size	Project Name	Rev
A3	AM4	0.01

Date: Thursday, April 09, 2020 Sheet 61 of 127

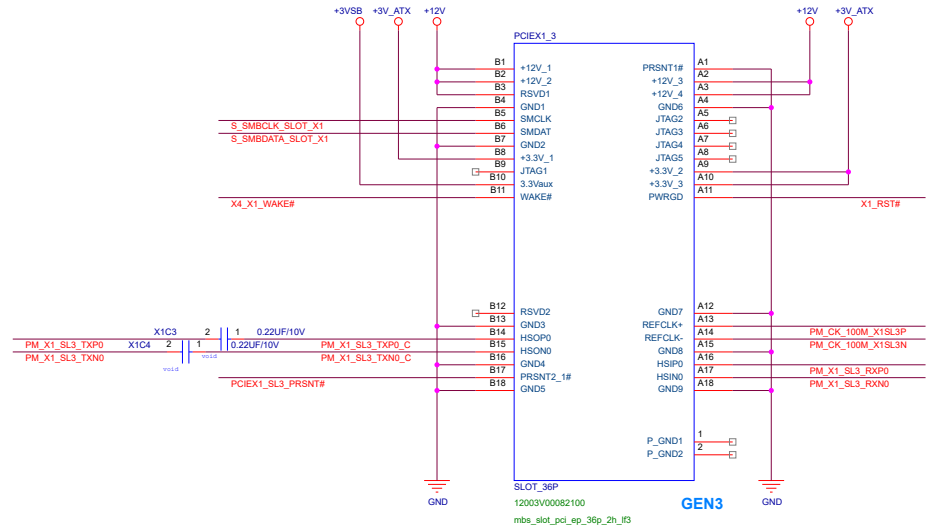
PIEX1_1



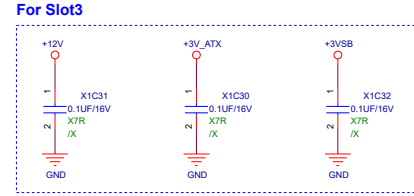
For Slot1

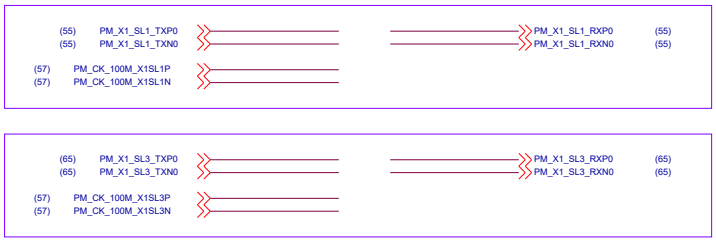


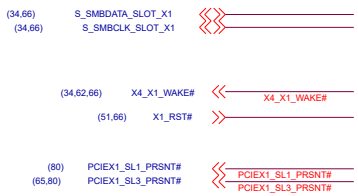
PIEX1_3

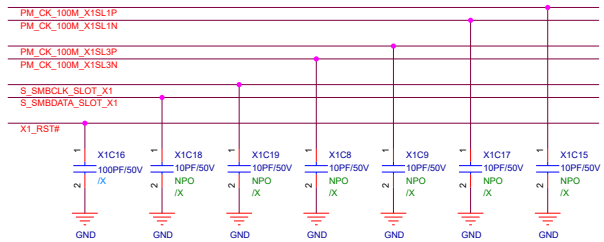


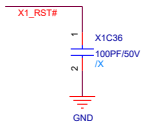
For Slot3











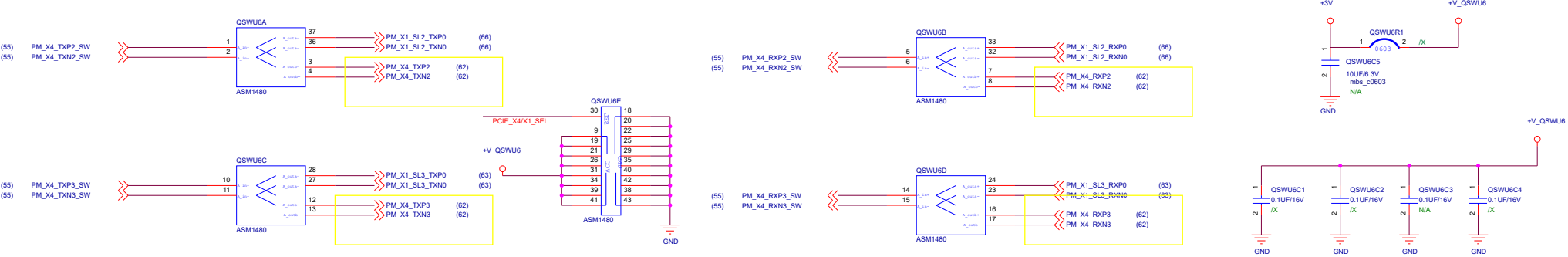
ASUSTek Computer Inc.

Title : Premium-09

Engineer: Elainelx_Li

Size	Project Name	Rev
A3	AM4	0.01

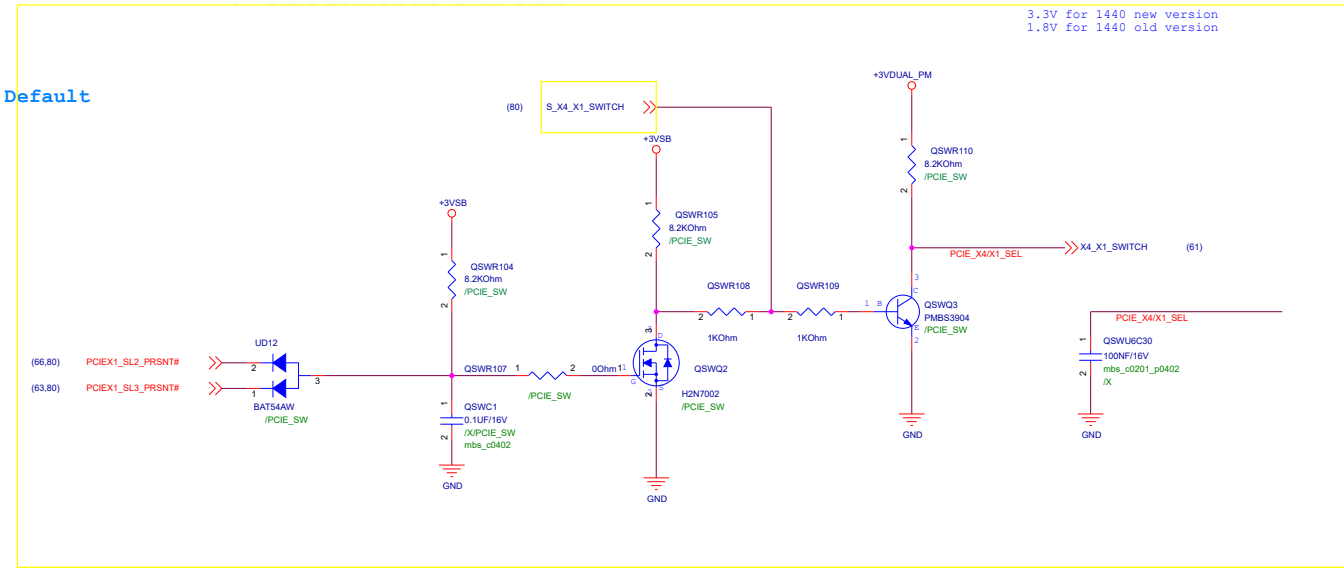
Date: Friday, April 10, 2020 Sheet 63 of 127



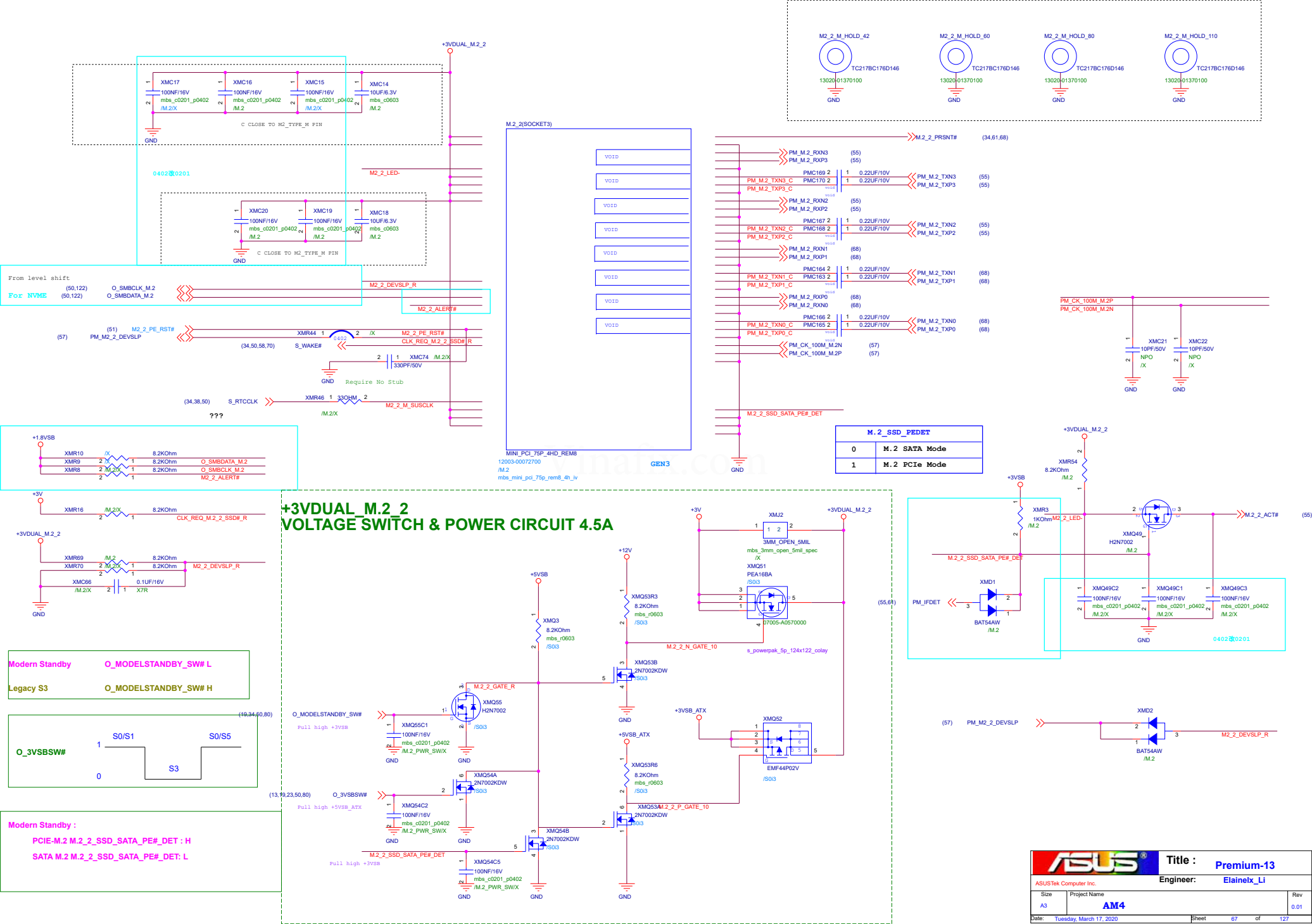
PCIEE_X4/X2#_SEL	Function	
L	N_in to N_outa	X1+X1*3
H	N_in to N_outb	PCIE_X4

BIOS chose by PCIE PRSNT#

Default



ASUSTek Computer Inc.	Title : PROMONTORY2019-11	
	Engineer: ElaineIx_Li	
Size: A3	Project Name: AM4	Rev: 0.01
Date: Thursday, March 05, 2020	Sheet 65 of 127	


+3VDUAL_M.2_2
VOLTAGE SWITCH & POWER CIRCUIT 4.5A
M.2_2_M_HOLD_42
M.2_2_M_HOLD_60
M.2_2_M_HOLD_80
M.2_2_M_HOLD_110
TC217BC176D146
13020001370100
GND
M.2_2(SOCKET3)
VOID
MINI_PCI_75P_4HD_REM8
12003-00072700
/M.2
mbs_mini_pci_75p_rem8_4h_iv
GEN3
M.2_2_PRSNT#
(34,61,68)
PM_M.2_RXN3
PM_M.2_RXP3
PM_M.2_TXN3
PM_M.2_TXP3
PM_M.2_RXN2
PM_M.2_RXP2
PM_M.2_TXN2
PM_M.2_TXP2
PM_M.2_RXN1
PM_M.2_RXP1
PM_M.2_TXN1
PM_M.2_TXP1
PM_M.2_RXP0
PM_M.2_RXN0
PM_M.2_TXN0
PM_M.2_TXP0
PM_CK_100M_M.2N
PM_CK_100M_M.2P
M.2_2_SSD_SATA_PE#_DET
From level shift
For NVME
O_SMBCLK_M.2
O_SMBDATA_M.2
M2_2_DEVSLP_R
M2_2_ALERT#
M2_2_PE_RST#
PM_M2_2_DEVSLP
S_WAKE#
CLK_REQ_M.2_2_SSD#_R
Require No Stub
S_RTCCLK
M2_2_M_SUSCLK
???
M.2_2_SSD_PEDET
0 M.2 SATA Mode
1 M.2 PCIe Mode
+3VDUAL_M.2_2
+1.8VSB
+3V
+3VSB
O_SMBDATA_M.2
O_SMBCLK_M.2
M2_2_ALERT#
CLK_REQ_M.2_2_SSD#_R
M2_2_DEVSLP_R
M2_2_LED-
M.2_2_ACT#
PM_IFDET
BAT54AW
Modern Standby O_MODELSTANDBY_SW# L
Legacy S3 O_MODELSTANDBY_SW# H
O_3VSBSW#
S0/S1
S0/S5
S3
Modern Standby :
PCIE-M.2 M.2_2_SSD_SATA_PE#_DET : H
SATA M.2 M.2_2_SSD_SATA_PE#_DET: L
Title : Premium-13
Engineer: Elainelx_Li
ASUSTek Computer Inc.
Size A3
Project Name AM4
Rev 0.01
Date: Tuesday, March 17, 2020
Sheet 67 of 127

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 03, 2020	Sheet 69 of 127	

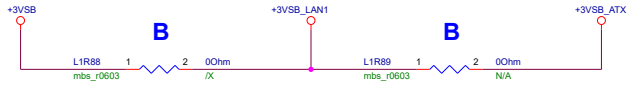
LAN1 Power Circuit

A. Choose LAN1 Power Solution by Project

B. Modify BOM Optional by Project

A.3

0 Ohm Resistor for with Deep S4/S5 wake up



Optional	not support Deep S4/S5 wake up	support Deep S4/S5 wake up
L1R88	N/A	/X
L1R89	/X	N/A

<Variant Name>

ASUSTEK COMPUTER INC

Title : LAN Power

Engineer: SZ Design IP

Size	Project Name	Rev
A3	LAN Demo Circuit	0.0

Date: Tuesday, March 03, 2020 Sheet 71 of 127

LAN1 POE Connector Circuit

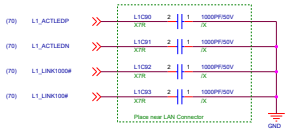
A. Choose LAN Connector by Project

B. Modify LAN Connector Part Reference by Project

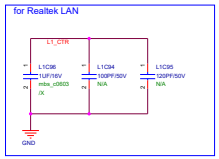
C. Modify USB Power Net Name by Project

D. Modify USB Signal Net Name by Project

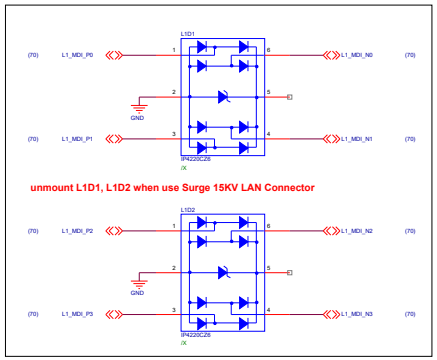
E. Choose EMI CAP Circuit by LAN



E.2



Delete it for EMS



LAN POE Connector built in Transformer

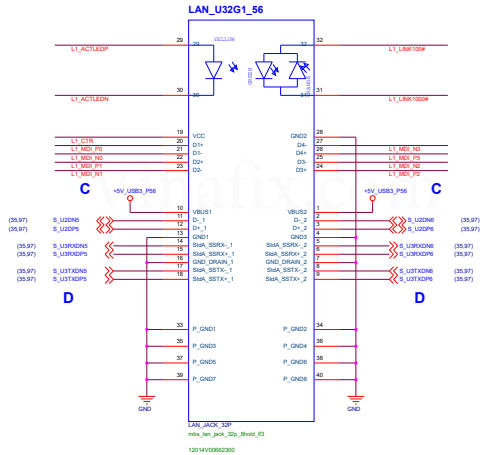
A.1

A.2

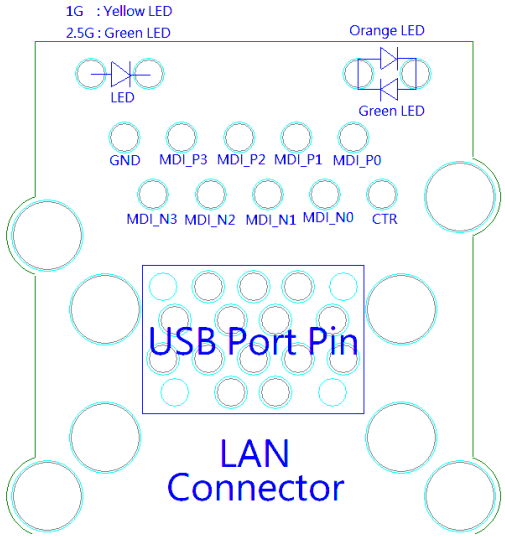
1G LAN + USB 3.0 *2 Ports Connector built in Transformer

single LAN named LAN_U32G1_xx or LAN_U32G1_Exx

dual LAN named LAN1_U32G1_xx or LAN1_U32G1_Exx



Sky Blue USB & Black 1G POE LAN: 12014V00662300



A.4

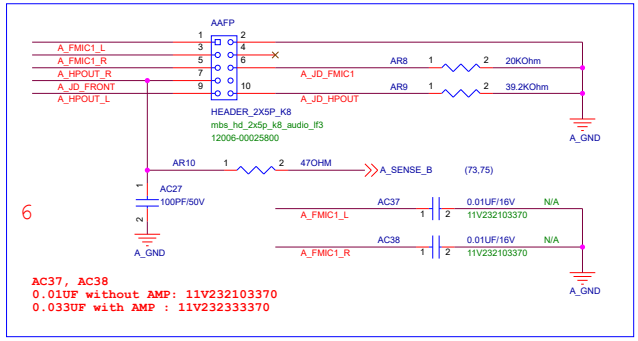
A.3

AAFP Circuit

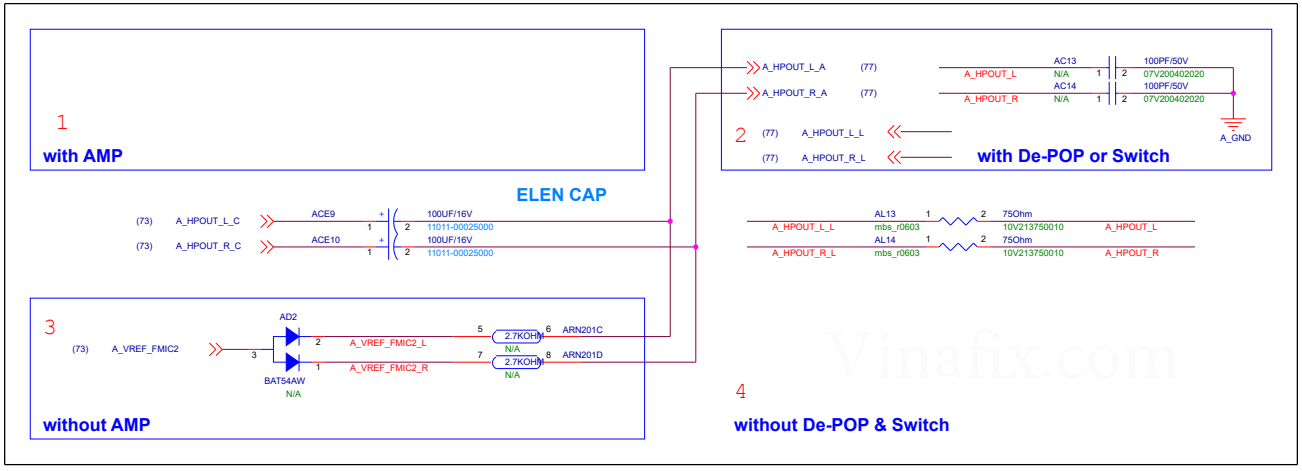
1. Choose AAFP Header Circuit by Codec,and change AAFP part number by your request,block 6,7, or 8
2. Choose HP Circuit with or without AMP/De-POP/Switch by Project,block 1,2,3,4
3. Modify ACE9, ACE10 Part Number by Project
4. IF you use 1220, AC13,AC14,AC15,AC16 option must change to N/A and change part number to varistor
5. Modify ARN202 value to 4.7k if you use 887,block 5
6. For Gamer Project with ALC1150, AL13, AL14 change to 47Ohm
7. change AC37,AC38 part number if you have AMP,block 6

AAFP

for ALC887-VD2/ALC892



for ALC887-VD2/ALC892/ALC1150/ALC1220X



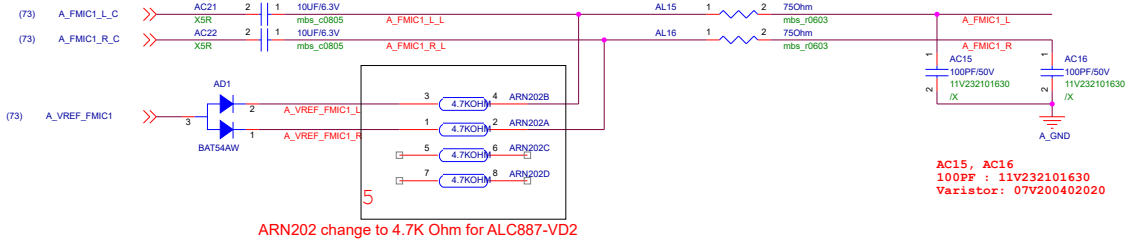
DIP CAP
EL 100U : 11V040107321
PL 100U : 11031V0001F000

AL13, AL14
75 Ohm: 10V213750010
47 Ohm: 10V213470010

AC13, AC14
100PF : 11V232101630
Varistor: 07V200402020

Taping DIP CAP
Chemicon 100U T: 11011-00024100
Elan 100U :11011-00025000
Nichicon 100U T: 11011-00026200

Taping DIP CAP
PL 100U T:11031V0001F400



ARN202 change to 4.7K Ohm for ALC887-VD2

AC15, AC16
100PF : 11V232101630
Varistor: 07V200402020

Delete it for EMS

<Variant Name>

ASUSTEK COMPUTER INC

Title : AAFP
Engineer: SZ Design IP
Size: A3
Project Name: AUDIO Demo Circuit
Rev: 0.0
Date: Monday, March 09, 2020
Sheet 74 of 127

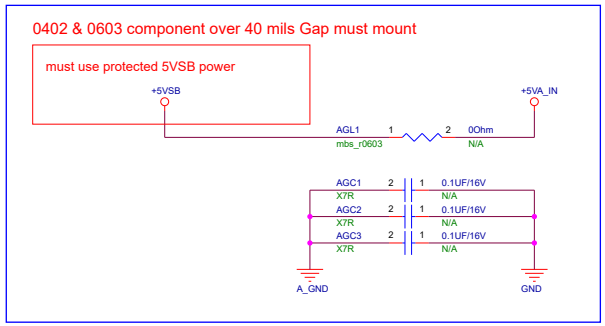
Audio GAP & Power Circuit

1. Choose Resistor & Capacitor over GAP Circuit by Project

2. Keep or delete Audio Power LDO Circuit by Project

3. Modify APCE4 Part Number by Project

40 mils Gap for XU



BOM	Audio Power from 5VSB	Audio Power from 12V LDO 5V
/AUDIO_PWR_5VSB	mount	unmount
/AUDIO_PWR_LDO	unmount	mount

<Variant Name>

ASUSTEK COMPUTER INC

Title : GAP_Power

Engineer: SZ Design IP

Size	Project Name	Rev
A3	AUDIO Demo Circuit	0.0

Date: Tuesday, March 03, 2020 Sheet 76 of 127

SPDIF

1. select block 1,2, or 3 by project

SPDIF Header

3

<Variant Name>

ASUSTEK COMPUTER INC	Title : SPDIF	
	Engineer: SZ Design IP	
Size: A	Project Name: AUDIO Demo Circuit	Rev: 0.0
Date: Wednesday, March 04, 2020	Sheet 78 of 127	

NCT6798D-R Circuit

A. Delete LPC Bus Signal Pull High Resistor if don't need

B. Choose RSMRST# Circuit by Project

C. Choose 32.768KHz Crystal by Project

D. Choose Pin 99 THERMTRIP#/CASEOPEN0# circuit by Project

E. Choose Pin 73 SLP_S4##/CASEOPEN1# circuit by Project, could NC if unused

F. Delete LPT Port Signal if don't need

G. Delete COM1 Port Signal if don't need, but keep Strapping Pin Signal

H. Delete COM2 Port Signal if don't need, but keep Strapping Pin Signal

I. 5VSB & 5VSB_DUAL Monitor for 5VSB & 5VSB_DUAL Power Control Signals Circuit, keep or delete this block by Project

J. Choose Pin 64, 65, 66 uesd as 5VSB & 5VSB_DUAL Power Control Signals Circuit by Project

SIO Pins \ Strapping Pin	VSB_CTL_EN=1	VSB_CTL_EN=0
Pin 64	5VSB_GATE# Inrush CAP	GPIO
Pin 65	5VSB_DUAL_GATE# with UVP & OVP	FANIN/OUT, GPIO
Pin 66	5VSB_GATE# with OVP & Inrush	
Pin 106	+5VSB Monitor	VIN
Pin 110	+5VSB_DUAL Monitor	VIN/TIN
Pin 115	+5VSB_ATX Monitor	VIN/TIN

K. Modify FAN IN/PWM/GPP/GPL Signal by Project

L. If use MS as FAN or GPIO, remove pull high resistor ORN404A/ORN404D, but keep MS Signal default pull high with other resistor to main power

M. If use KB as FAN or GPIO, remove pull high resistor ORN404B/ORN404C, but keep KB Signal default pull high with other resistor to main power

N. Modify VIN Signal by Project

O. Modify TIN Signal by Project

P. Unused TIN Pin connect to O_TR_MB

Q. Add SMBUS (not Master, only Slave) Circuit by Project, could copy from Page SIO_IC_Optional

R. If support LAN wake-up from SIO, LAN_SIO_WAKE# choose from GP31, GP32, GP35, GP46, RIA#, RIB#

S. Choose LAN_SIO_WAKE# Pull High Circuit by Project

T. SIO RGB LED Signals, keep or delete this block by Project

U. Delete AUDIO_LED_PWM Signal if don't need

V. If SIO Breathing LED is reserved, unmount AUDIO_LED_PWM pull high resistor

W. AUDIO_LED_PWM use GRN_LED or MLED or YLW_LED

X. O_PLED could use YLW_LED or MLED or GRN_LED, but not same with AUDIO_LED_PWM

Y. Delete O_PLED Signal if don't need

Z. Delete Pin 81 O_PWROK# if don't need

AA. Choose COM Debug Signal by Project, could use Pin 102, 12 or 33

AB. Add/Choose OVT#/SMI# Signal by Project, use Pin 128(push pull) or use GPIO which could mapping to SMI# Function(open drain)

AC. Add BEEP Signal by Project, first use Pin 118, or use other GPIO which could mapping to BEEP Function

AD. Add O_I2XX_RST# for Intel PCIE LAN I211 & I225 if have unused RSTOUT# Pin

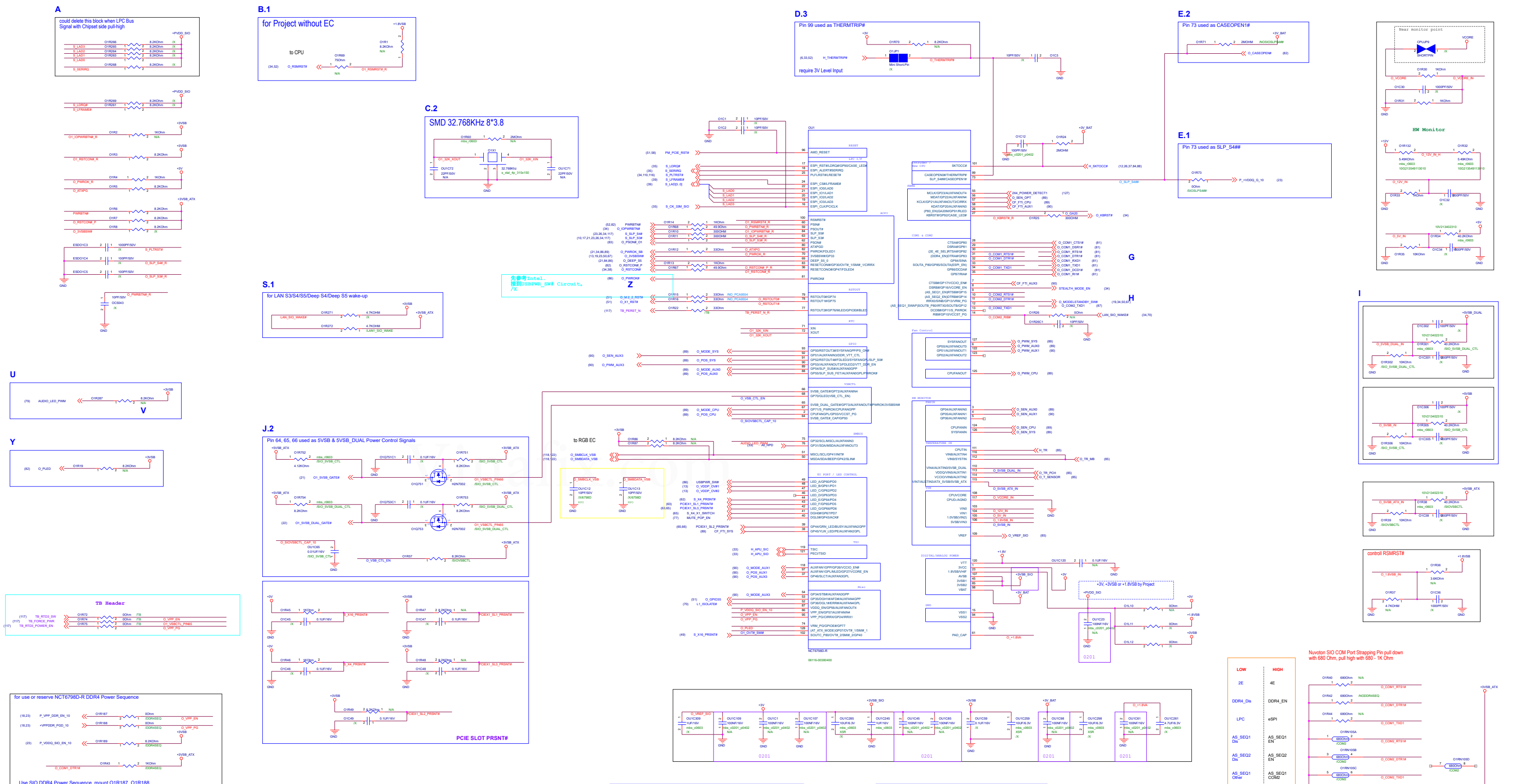
AE. Add Onboard Debug P80 LED if need, and modify Strapping Circuit to make Strapping Pin LPT_P80_EN default enable(pull high to +3VSB_ATX)

AF. For AT Mode Project, modify Strapping Circuit to make Strapping Pin AT_ATX_MODE pull down with resistor & unmount O1R55

AG. Could connect Power Supply PWROK to Pin 80 ATXPGD through 0 Ohm resistor by Project requirement

AH. If need turn off Stand By Power LED, choose a SIO GPIO connect to O_SBPWRLED; if the GPIO default output high, could unmount O1R207

AI. If use SIO Anti Surge Function, mount O1C32, O1C34



NCT6798D-R FAN Header Pin Table

SIO FAN	FAN IN	FAN PWM	GPP	GPL	FAN Header
CPUFAN	Pin 124	Pin 125	Pin 67	Pin 2	CPU_FAN
SYSFAN	Pin 126	Pin 127	Pin 93	Pin 91	CHA_FAN/CHA_FAN1
AUXFAN0	Pin 3	Pin 6	Pin 89	Pin 88	CHA_FAN2
AUXFAN1	Pin 4	Pin 122	Pin 118	Pin 97	M.2_FAN
AUXFAN2	Pin 5	Pin 123	Pin 39	Pin 38	AIO_PUMP
AUXFAN3	Pin 92 or 75 or 58	Pin 90 or 76 or 57	Pin 54	Pin 37	W_PUMP+/W_PUMP+1
AUXFAN4	Pin 66 or 86 or 56	Pin 65 or 87 or 55	Pin 53	Pin 52	W_PUMP+2/AMP_PUMP

FAN Net Name Table

FAN	FAN IN	FAN PWM	FAN GPP with 3949	FAN GPL with 3949
CPUFAN	O_SEN_CPU	O_PWM_CPU	O_MODE_CPU	O_POS_CPU
CPU_OPT	O_SEN_OPT			
SYSFAN	O_SEN_SYS	O_PWM_SYS	O_MODE_SYS	O_POS_SYS
AUXFAN0	O_SEN_AUX0	O_PWM_AUX0	O_MODE_AUX0	O_POS_AUX0
AUXFAN1	O_SEN_AUX1	O_PWM_AUX1	O_MODE_AUX1	O_POS_AUX1
AUXFAN2	O_SEN_AUX2	O_PWM_AUX2	O_MODE_AUX2	O_POS_AUX2
AUXFAN3	O_SEN_AUX3	O_PWM_AUX3	O_MODE_AUX3	O_POS_AUX3
AUXFAN4	O_SEN_AUX4	O_PWM_AUX4	O_MODE_AUX4	O_POS_AUX4

NCT6798D-R SMBUS Table

	SMBUS Slave to EC	SMBUS Master to RGB LED EC
SIO SMBUS	Pin 75, 76	Pin 50, 51

NCT6798D-R TIN Table

SIO TIN	CPUTIN	SYSTIN	AUXTIN0	AUXTIN1	AUXTIN2	AUXTIN3	AUXTIN4
TIN IN	CPU	MB					

NCT6798D-R VIN Table

SIO VIN	CPUVCORE	VIN0	VIN1	VIN2	VIN3	VIN4	VIN5	VIN6	VIN7	VIN8	VIN9
VIN IN	VCORE	+12V	+5V	+1.8VSB	+5VSB	+5VSB_DUAL			+5VSB_ATX		

BOM	use SIO DDR4 Sequence	unuse SIO DDR4 Sequence
/DDR4SEQ	mount	unmount
/NODDR4SEQ	unmount	mount

BOM	use SIO SLP_S4##	unuse SIO SLP_S4##
/SIOSLPS4##	mount	unmount
/NOSIOSLPS4##	unmount	mount

BOM	NCT6798D-R Pin 64, 65, 66, 110, 115, 106 uesd as 5VSB & 5VSB_DUAL Power Control Signals	NCT6798D-R Pin 64, 66, 115, 106 uesd as 5VSB Power Control Signals	NCT6798D-R Pin 65, 110, 115 uesd as 5VSB_DUAL Power Control Signals	Do not use SIO Pins as 5VSB & 5VSB_DUAL Power Control Signals
/SIOVSBCTL	mount	mount	mount	unmount
/SIO_5VSB_CTL	mount	mount	unmount	unmount
/SIO_5VSB_DUAL_CTL	mount	unmount	mount	unmount
/NOSIOVSBCTL	unmount	unmount	unmount	mount

BOM	
N/A	mount
/X	unmount

STANDARD CIRCUIT	
XUMB	Super I/O
SZ_SIO_1.1D	

<Variant Name>

ASUS — ASUSTEK COMPUTER INC	Title : NCT6798D-R_AMD	
	Engineer: SZ Design IP	
Size: Custom	Project Name: Super I/O Demo Circuit	Rev 0.0
Date: Tuesday, March 17, 2020	Sheet 80 of 127	

COM Circuit

A. Choose COM Port Connector/Header Type

B. Choose use RI# to do LAN wake-up from SIO or not by Project

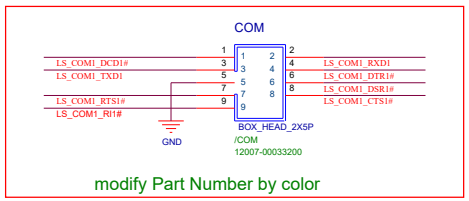
C. Modify Part Number of COM Connector/Header by Color

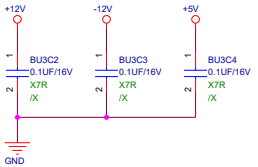
D. Keep or delete O_RI# Circuit by Project

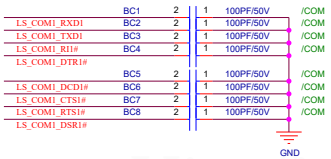
E. Modify O_RI# pill-high power by Project

COM PORT

A.1
COM Box Header





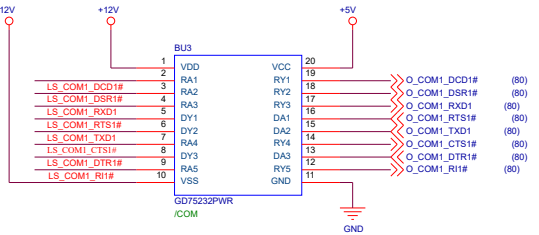


for use COM Port RI# to do LAN wake-up from SIO function

modify SIO RI# Pin net name to LAN_SIO_WAKE#

for not use COM Port RI# to do LAN wake-up from SIO function

B.2



When mount /COM

LAN wake-up from SIO	O1R171	O1Q171 & O1D171
support	unmount	mount
not support	mount	unmount

BOM	need COM Port	no COM Port
/COM	mount	unmount

When unmount /COM

LAN wake-up from SIO	O1R171	O1Q171 & O1D171
support	unmount	unmount
not support	unmount	unmount

<Variant Name>

ASUSTEK COMPUTER INC	Title : COM	
	Engineer: SZ Design IP	
Size: A3	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Thursday, March 05, 2020	Sheet 81 of 127	

EATX Power Circuit

A. Choose EATX Power Circuit by Project

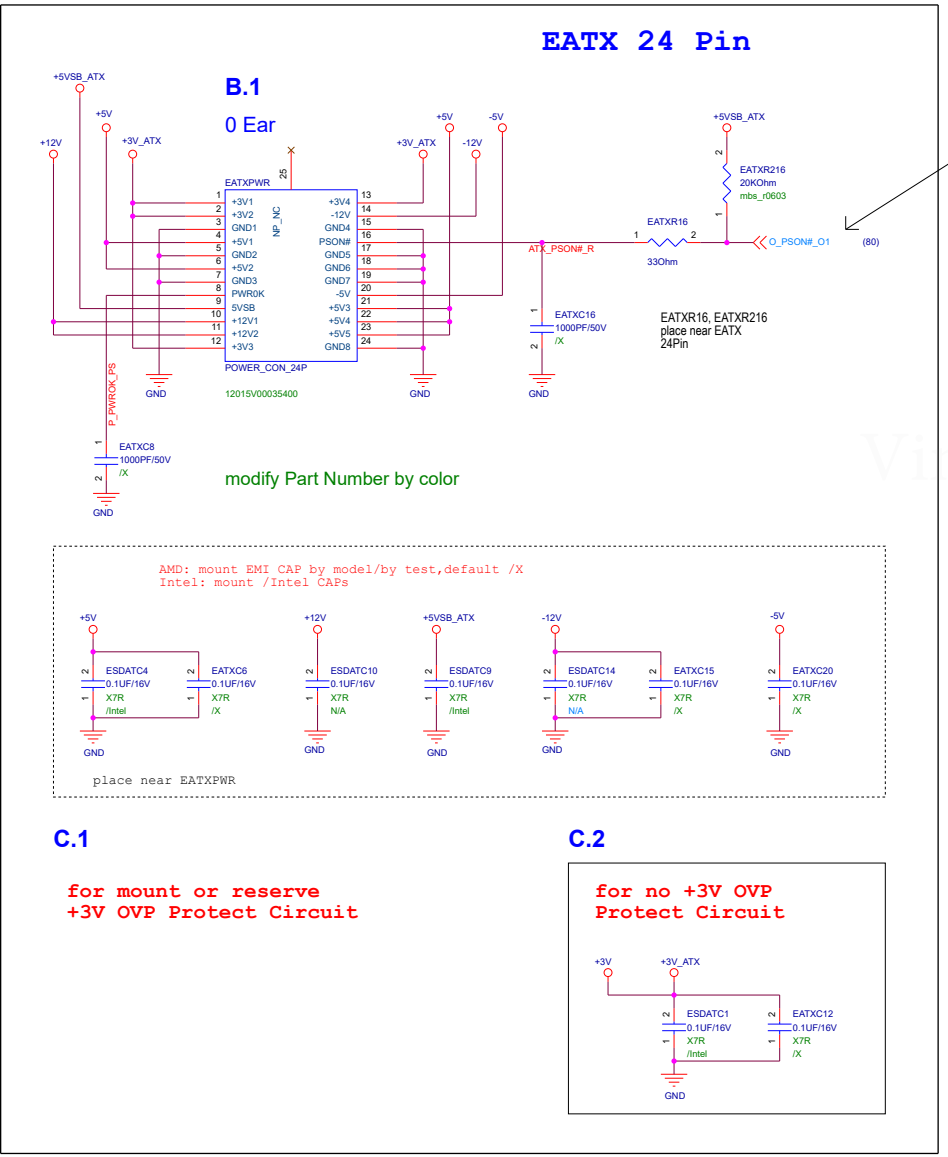
B. If choose EATX 24Pin Circuit, choose EATX Connector with 0 Ear, 1 Ear or 2 Ears by Project

C. If choose EATX 24Pin Circuit, choose +3V_ATX & +3V Circuit by Project

D. If support Intel S0ix, add SC945, SC946 & Off-Page Net O_PSON#_O1 change to ATX_PSON#

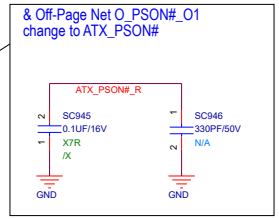
E. Modify Part Number of EATX Connector by Color

A.1



D

for S0ix



<Variant Name>

ASUSTEK COMPUTER INC	Title : EATX	
	Engineer: SZ Design IP	
Size: Custom	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Wednesday, April 15, 2020	Sheet 83 of 127	

Stand By LED & HW Monitor Circuit

A. Choose Stand By LED Circuit by Project

B. Keep or delete TR_PCH Circuit by Project

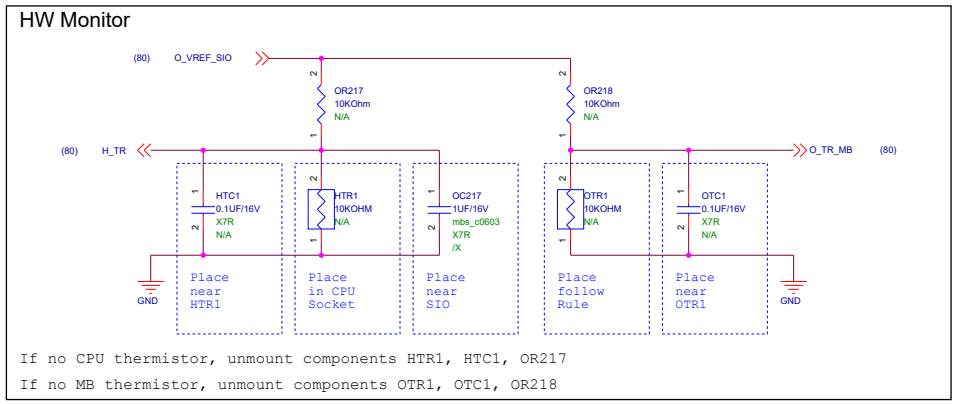
C. Keep or delete T_SENSOR Circuit by Project

D. Keep or delete VCORE Power Controller TEMP Detect Circuit by Project

E. Keep or delete GFX Power Controller TEMP Detect Circuit by Project

F. Modify Part Number of T_SENSOR Header by Color

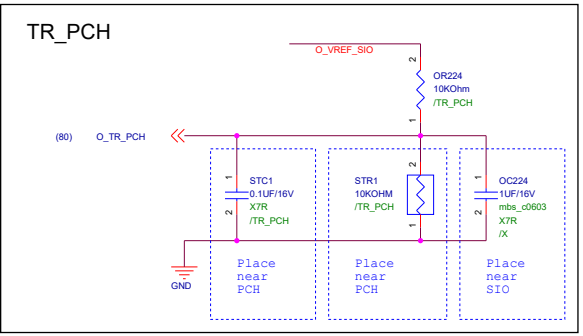
BOM	no Stand By LED	need Stand By LED without GPIO control	need Stand By LED with GPIO control
/StandByLED	unmount	mount	mount
/StandByLED_without_GPIO	unmount	mount	unmount
/StandByLED_with_GPIO	unmount	unmount	mount



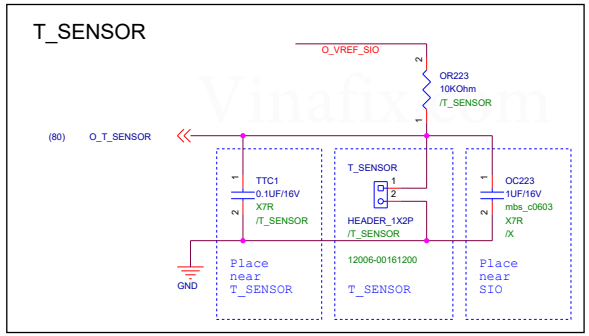
BOM	need TR_PCH	no TR_PCH
/TR_PCH	mount	unmount

BOM	need T_SENSOR	no T_SENSOR
/T_SENSOR	mount	unmount

B



C



<Variant Name>

ASUSTEK COMPUTER INC

Title : SBLED_HWM

Engineer: SZ Design IP

Size: Custom | Project Name: Super I/O Demo Circuit | Rev: 0.0

Date: Thursday, March 05, 2020 | Sheet 85 of 127

Debug Header Circuit

A. Choose Debug Header by Project

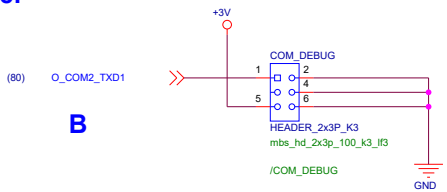
B. If choose COM Debug Header, take care Debug Signal Net Name is different by Project

C. If choose LPC Debug Header, modify Clock Signal Net Name by Project

A.1

Delete it for EMS

COM Debug Header



COM Debug Signal share Nuvoton SIO COM1 TX Signal

BOM	need COM Debug Header	no COM Debug Header
/COM_DEBUG	mount	unmount

BOM	need LPC Debug Header	no LPC Debug Header
/LPC_DEBUG	mount	unmount

<Variant Name>

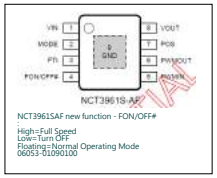
ASUSTEK COMPUTER INC

Title : Debug Header

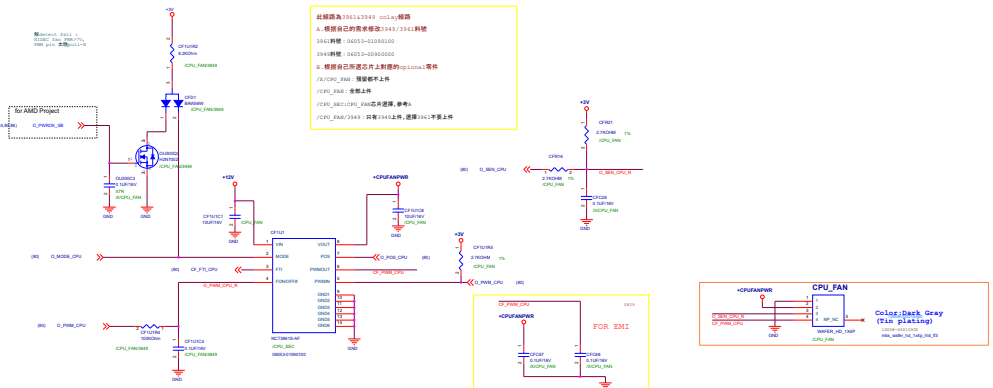
Engineer: SZ Design IP

Size	Project Name	Rev
B	Super I/O Demo Circuit	0.0

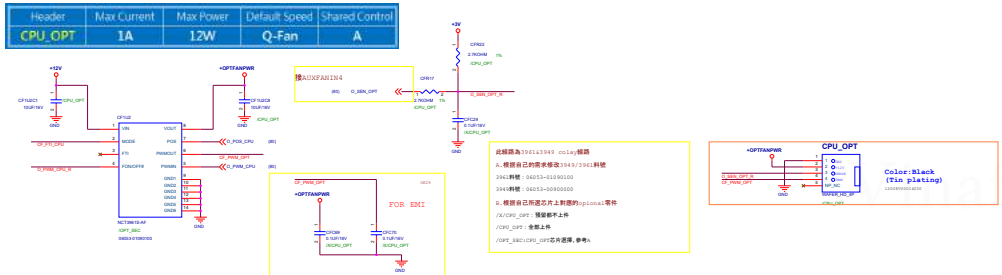
Date: Thursday, March 05, 2020 Sheet 87 of 127



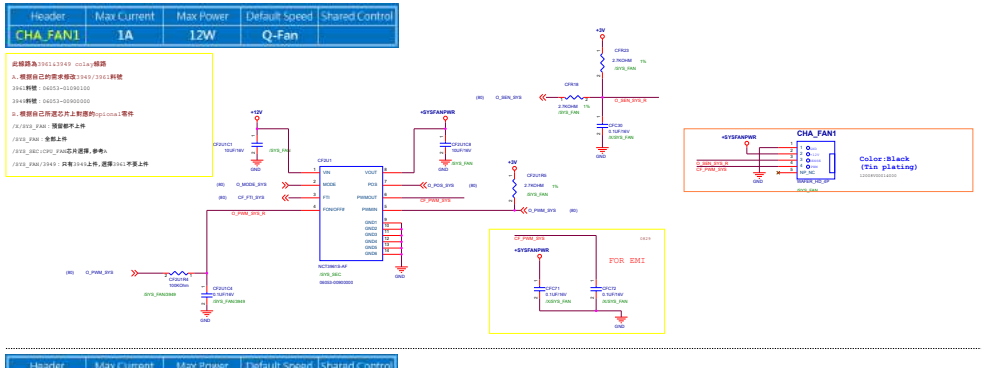
Header	Max Current	Max Power	Default Speed	Shared Controll
CPU_FAN	1A	12W	Q-Fan	A



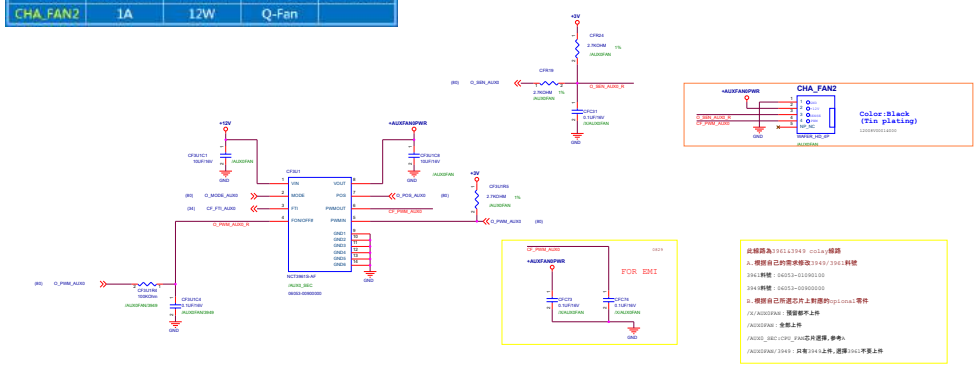
Header	Max Current	Max Power	Default Speed	Shared Control
CPU_OPT	1A	12W	Q-Fan	A



Header	Max Current	Max Power	Default Speed	Shared Control
CHA_FAN1	1A	12W	Q-Fan	



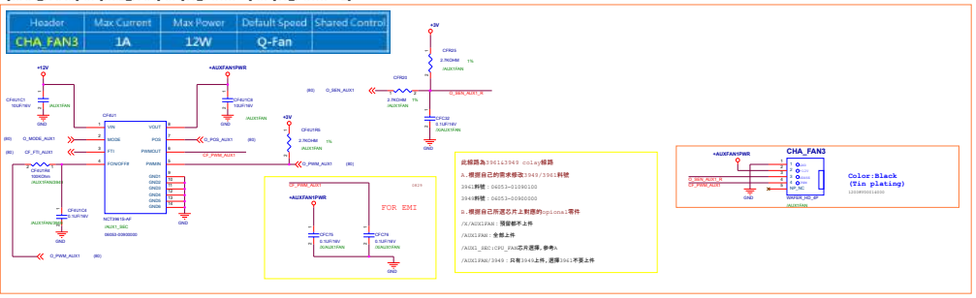
Header	Max Current	Max Power	Default Speed	Shared Control
CHA_FAN2	1A	12W	Q-Fan	



ASUSTeK COMPUTER INC.	Title :	FAN	
	Engineer:	Yodream_Chen	
Size	Project Name		Rev
Custom	Innovation Circuit		
Date: Friday, April 10, 2020	Sheet	68 of 137	

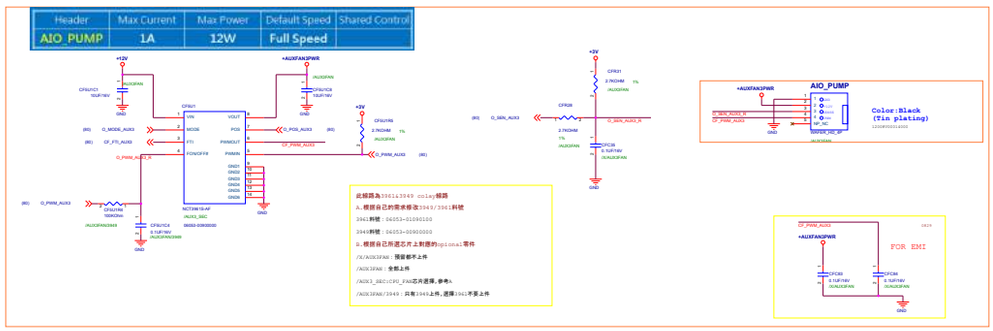
[CHA_FAN3] or [M.2_FAN] or [W_PUMP+] or [W_PUMP+1]

Header	Max Current	Max Power	Default Speed	Shared Control
CHA_FAN3	1A	12W	Q-Fan	



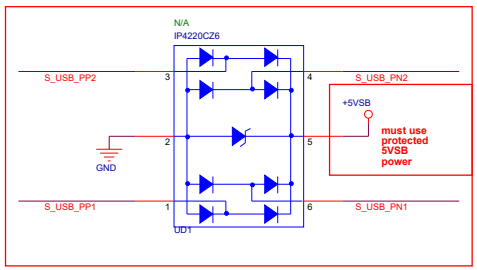
[AIO_PUMP] or [W_PUMP+2]

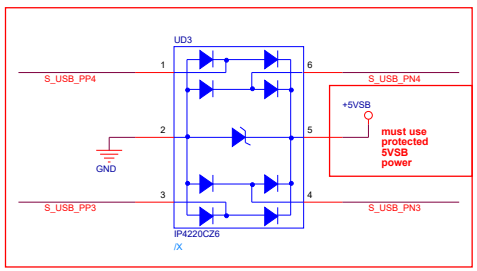
Header	Max Current	Max Power	Default Speed	Shared Control
AIO_PUMP	1A	12W	Full Speed	

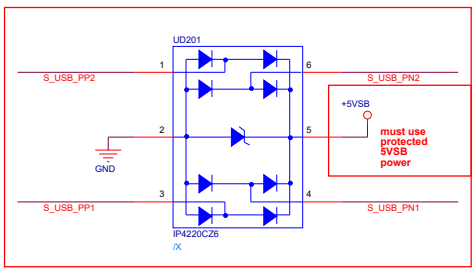


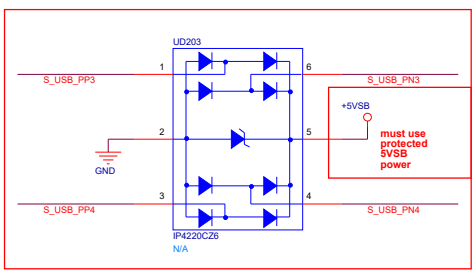
Title :	FAN	
Engineer:	Yodream_Chen	
Size	Project Name	Rev
Custom	Innovation Circuit	
Date: Thursday, March 28, 2019	Sheet 46 of 57	

Delete it for EMS

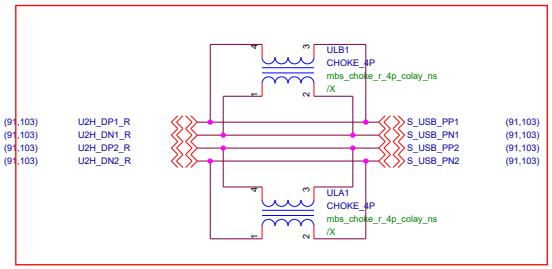




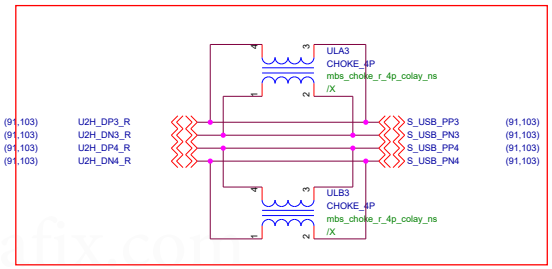




HUB FRONT USB12



HUB FRONT USB34



10.26

<Variant Name>

ASUSTEK COMPUTER INC

Title : USB2 Port

Engineer: Kell_Huang

Size	Project Name	Rev
A3	Chipset USB Demo Circuit	0.0

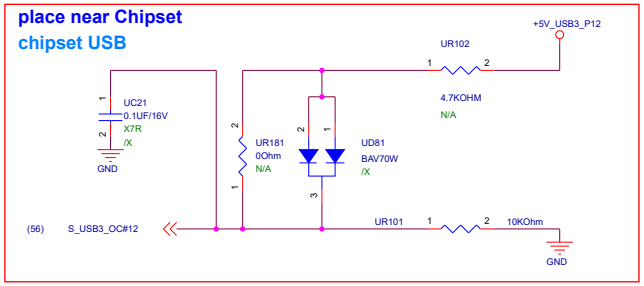
Date: Tuesday, March 17, 2020 Sheet 92 of 127

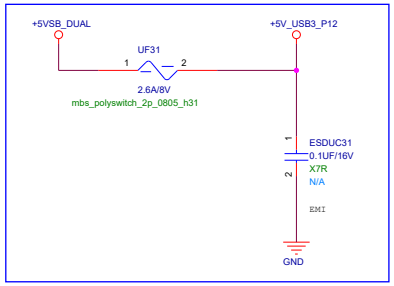
Delete it for EMS

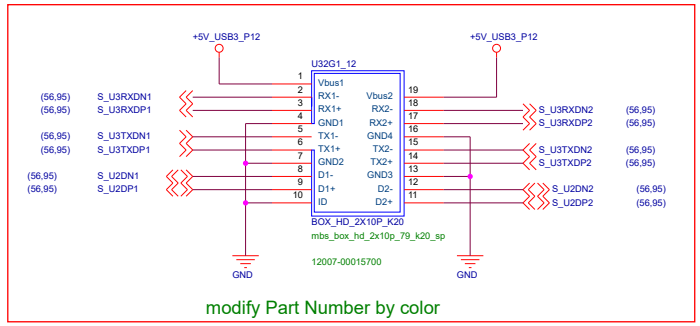
OC# circuit for AMD

place near Chipset

chipset USB



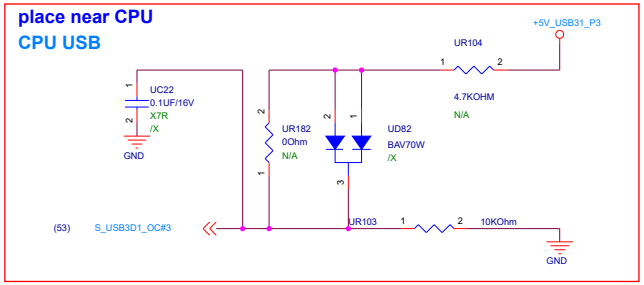


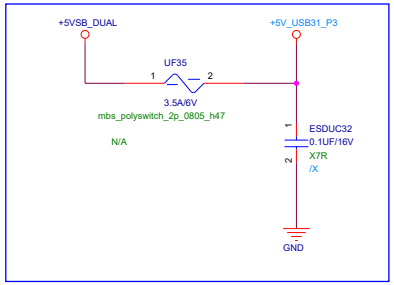


modify Part Number by color

place near CPU

CPU USB

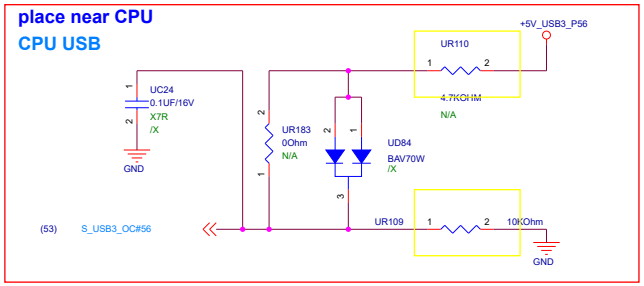


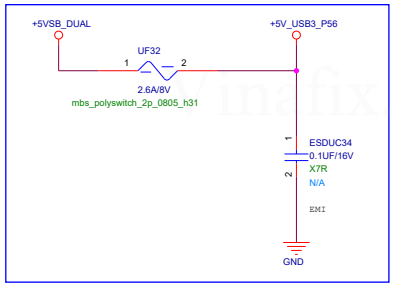


BACKIO U32G2_3 + U32G2_C4

place near CPU

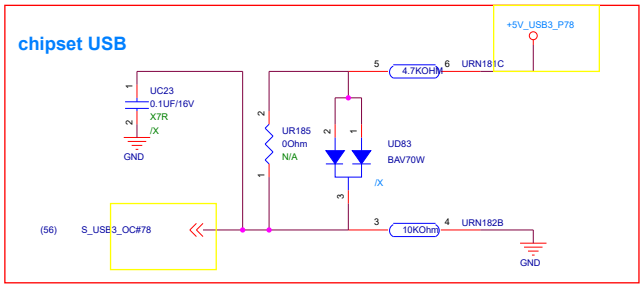
CPU USB

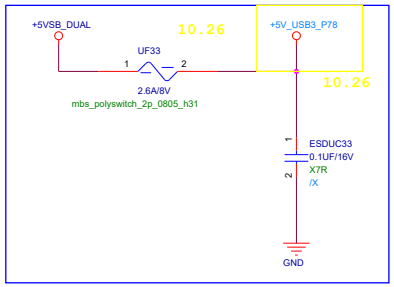




BACKIO U32G1_34_G2_56 PORT56

chipset USB





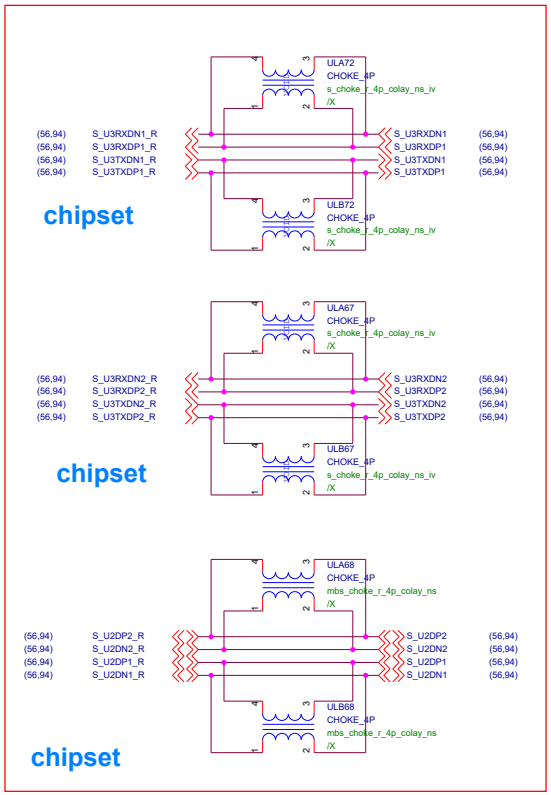
BACKIO U32G1_78

<Variant Name>

ASUSTEK COMPUTER INC	Title : USB3 Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Tuesday, April 07, 2020	Sheet 94 of 127	

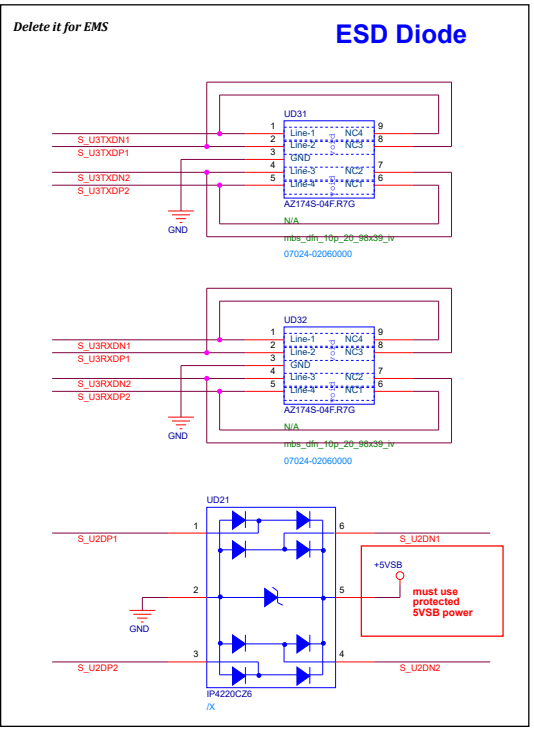
FRONT U32G1_12

Reserve Location (RES A)



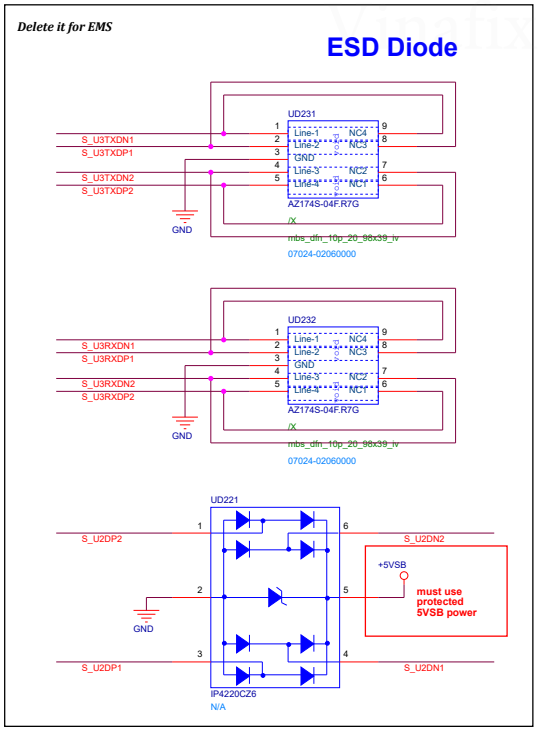
Delete it for EMS

ESD Diode



Delete it for EMS

ESD Diode



10.26

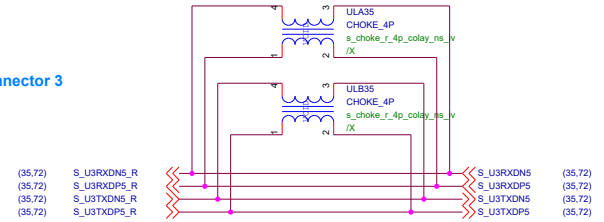
<Variant Name>

ASUSTEK COMPUTER INC	Title : USB3 Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Tuesday, March 17, 2020	Sheet 95 of 127	

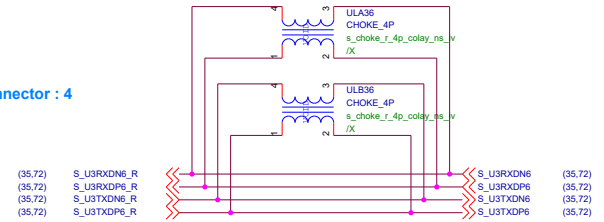
BACK IO U32G1_56

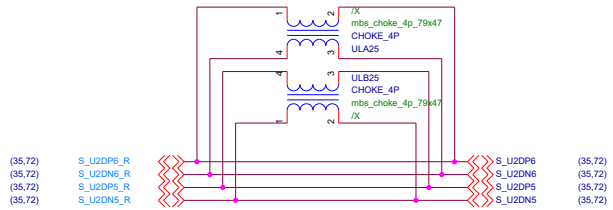
Reserve Location (Single RES)

CPU USB 3.1 Type-A Connector 3



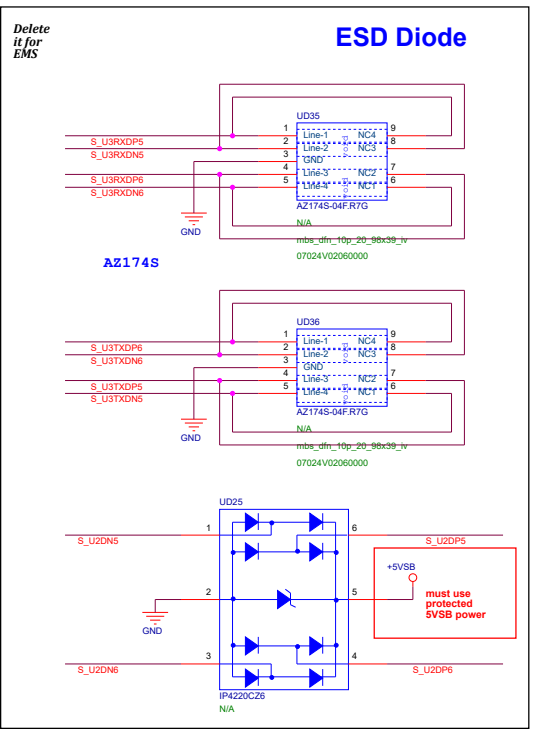
CPU USB 3.1 Type-A Connector : 4





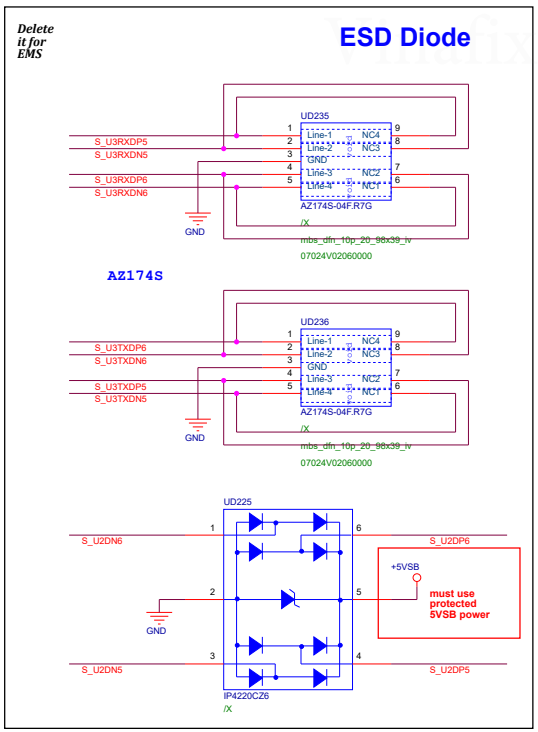
Delete it for EMS

ESD Diode



Delete it for EMS

ESD Diode



<Variant Name>

ASUSTEK COMPUTER INC

Title : USB3 Port

Engineer: Kell_Huang

Size	Project Name	Rev
A3	Chipset USB Demo Circuit	0.0

Date: Thursday, March 05, 2020 Sheet 97 of 127

One USB 3.x Ports to One Type-C Connector/USB 3.1 Front Header Circuit_1

A. If don't need use or reserve Power Switch to control Type-C Connector Power, delete this block

B. Modify Input USB 3.x TX/RX Signal Net Name by Project

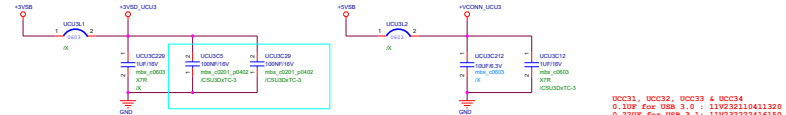
C. Modify Part Number of UCC31, UCC32, UCC33 & UCC34 by Project

D. Choose ESD Diode by Project

E. Choose EMI Choke Circuit by Project

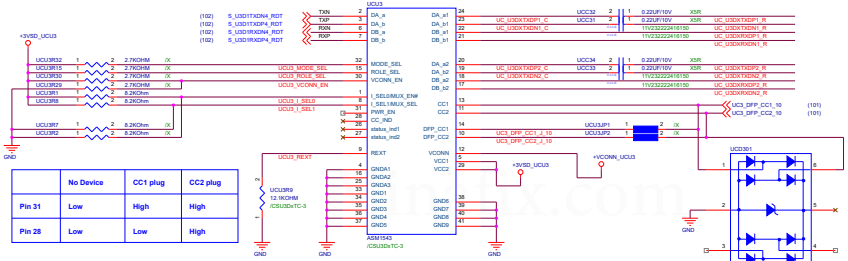
BOM	Type-C with Power Switch	Type-C with Poly Switch
/CSU3DxTC-3	mount	mount
/CSU3DxTC-3/Power Switch	mount	unmount
/CSU3DxTC-3/Poly Switch	unmount	mount

3.1 TYPEC @ BACK IO



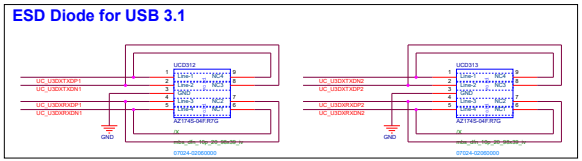
UCC31, UCC32, UCC33 & UCC34
0.10UF for USB 3.0 : 11V232110411320
0.220UF for USB 3.1: 11V232222416150

B

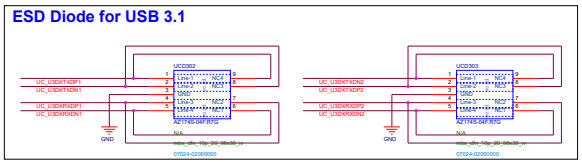


	No Device	CC1 plug	CC2 plug
Pin 31	Low	High	High
Pin 28	Low	Low	High

D.1



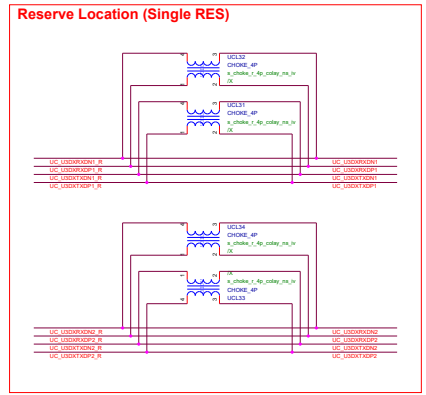
D.2



E.1

EMI Choke for USB 3.1

E.6



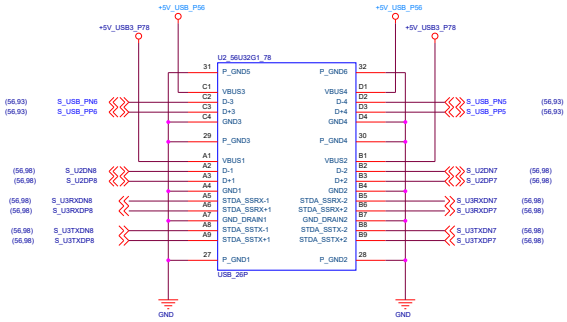
E.7

PORT D

PORT C

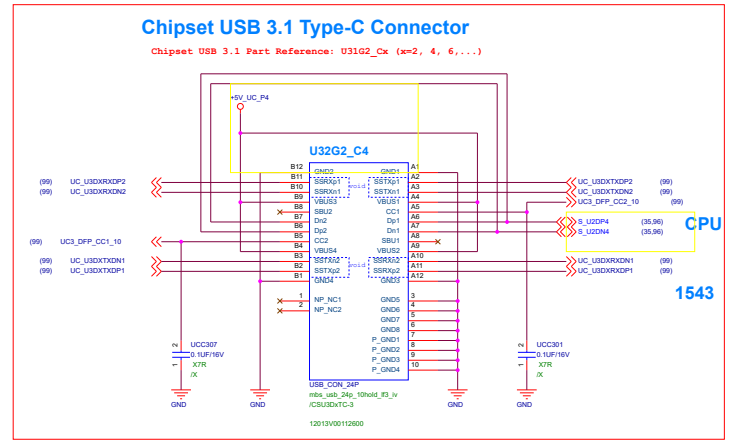
PORT B

PORT A



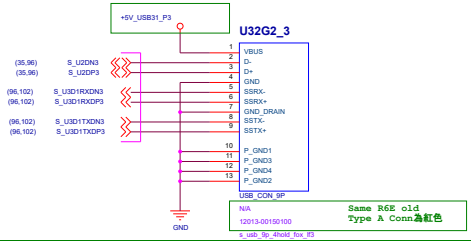
A.2 B

PT BACKIO 3.1 TYPE C



Chipset USB 3.1 Part Reference: U31G2_Cx (x=1, 3, 5,...)

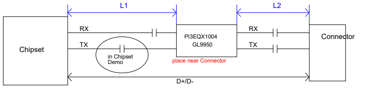
1 port Type A USB3.1 (CE team update)



<Variant Name>

ASUSTEK COMPUTER INC	Title : CS U3.x Type-C	
	Engineer: SZ Design IP	
Size: A2	Project Name: Chipset USB Type-C Port	Rev: 1.1A
Date: Thursday, March 05, 2020	Sheet 101 of 127	

USB 3.1 Re-Driver PI3EQX1004/GL9950 Circuit



Net	Impedance/Width	Space	Length
TX/RX L1	follow USB 3.1 Controller Rule	30 mils	< 10", prefer 5" - 9"
TX/RX L2		30 mils	< 2.5", prefer 0.5" - 1.5"
+3V_RDP2	>= PI3EQX1004/GL9950 IC Count *20 mils		
Other Power Net	>= 20 mils		

A. Delete the Re-Driver IC which is not needed by Project

B. Modify Input USB 3.1 TX/RX Signal Net Name by Project

C. Modify Output USB 3.1 TX/RX Signal Net Name by Project

D. for AMD Platform, RX signal's AC CAP between CPU/Chipset & Re-Driver change Part Number from 11V232222416150 to 11V232334150

E. If UU41 TXA output signals send to ASM1543, UU41C34 & UU41C35 change from 11V232222416150 to 11V232334150 & mount UU41R34, UU41R35, otherwise could delete UU41R34, UU41R35

F. If UU41 TXB output signals send to ASM1543, UU41C26 & UU41C27 change from 11V232222416150 to 11V232334150 & mount UU41R26, UU41R27, otherwise could delete UU41R26, UU41R27

G. If UU42 TXA output signals send to ASM1543, UU42C34 & UU42C35 change from 11V232222416150 to 11V232334150 & mount UU42R34, UU42R35, otherwise could delete UU42R34, UU42R35

H. If UU42 TXB output signals send to ASM1543, UU42C26 & UU42C27 change from 11V232222416150 to 11V232334150 & mount UU42R26, UU42R27, otherwise could delete UU42R26, UU42R27

I. If UU43 TXA output signals send to ASM1543, UU43C34 & UU43C35 change from 11V232222416150 to 11V232334150 & mount UU43R34, UU43R35, otherwise could delete UU43R34, UU43R35

J. If UU43 TXB output signals send to ASM1543, UU43C26 & UU43C27 change from 11V232222416150 to 11V232334150 & mount UU43R26, UU43R27, otherwise could delete UU43R26, UU43R27

K. Modify EQ/FG Pins' pull high/pull down BOM by layout

L. Choose PI3EQX1004/GL9950 Power Solution by PI3EQX1004/GL9950 IC count

BOM	PI3EQX1004/GL9950 Power generated by LDO	PI3EQX1004/GL9950 Power from LAN1	PI3EQX1004/GL9950 Power from LAN2	PI3EQX1004/GL9950 Power from Wifi
/P1004_GL9950_PWR_from_LDO	mount	unmount	unmount	unmount
/P1004_GL9950_PWR_from_LAN1	unmount	mount	unmount	unmount
/P1004_GL9950_PWR_from_LAN2	unmount	unmount	mount	unmount
/P1004_GL9950_PWR_from_WIFI	unmount	unmount	unmount	mount

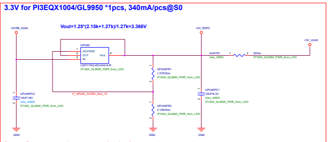
M. UU41, UU42 & UU43 default use PI3EQX1004B1

EQ/FG Setting Table for Intel Platform	L2 < 2.5"			
	TX EQ	TX FG	RX EQ	RX FG
L1 < 7"	R	R	R	0
7" <= L1 <= 9" (demo default)	F	R	R	F
9" < L1 < 10"	1	R	R	1

EQ/FG Setting Table for AMD Platform	L2 < 2"			
	TX EQ	TX FG	RX EQ	RX FG
L1 < 7"	R	R	R	0
7" <= L1 <= 9"	F	R	R	F
9" < L1 < 10"	1	R	R	1

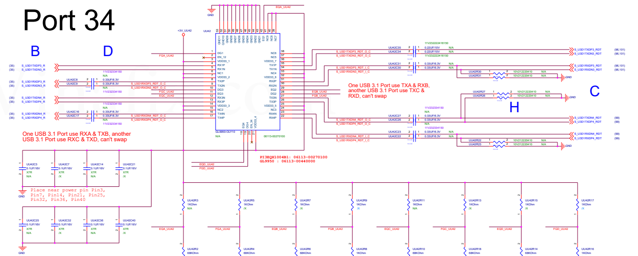
L.1

3.3V for PI3EQX1004/GL9950 *1pcs, 340mA/pcs@S0



Power Component place near each other!

Port 34



	1st Port	2nd Port
TX EQ	EQA	EQC
TX FG	FGA	FGC
RX EQ	EQB	EQD
RX FG	FGB	FGD

EQ, FG Pin	
0	1K Ohm pull down
R	68K Ohm pull down
F	Floating
1	1K Ohm pull high

1RFF 1FFF

<Variant Name>

ASUSTEK COMPUTER INC	Title : PI3EQX1004		
	Engineer: SZ Design IP		
Size: Custom	Project Name: Chipset USB Re-Driver		Rev: 1.1E
Date: Tuesday, April 07, 2020	Sheet 102 of 127		

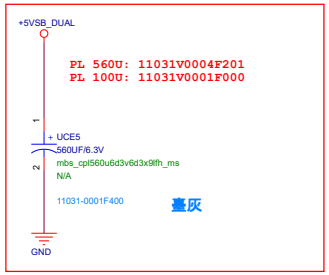
PL CAP

PL 560U: 11031V0004F201
PL 100U: 11031V0001F000

FOR LAYOUT, 刪除

臺黑

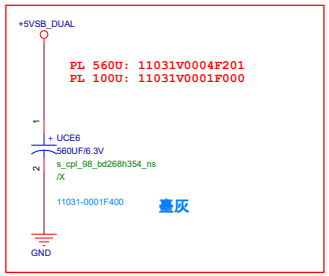
PL CAP



PL 560U: 11031V0004F201
PL 100U: 11031V0001F000

刪除UCE2, 將BIOS FLASH BACK LED 移過來

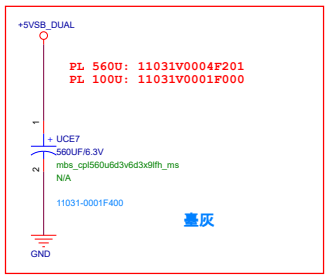
臺黑



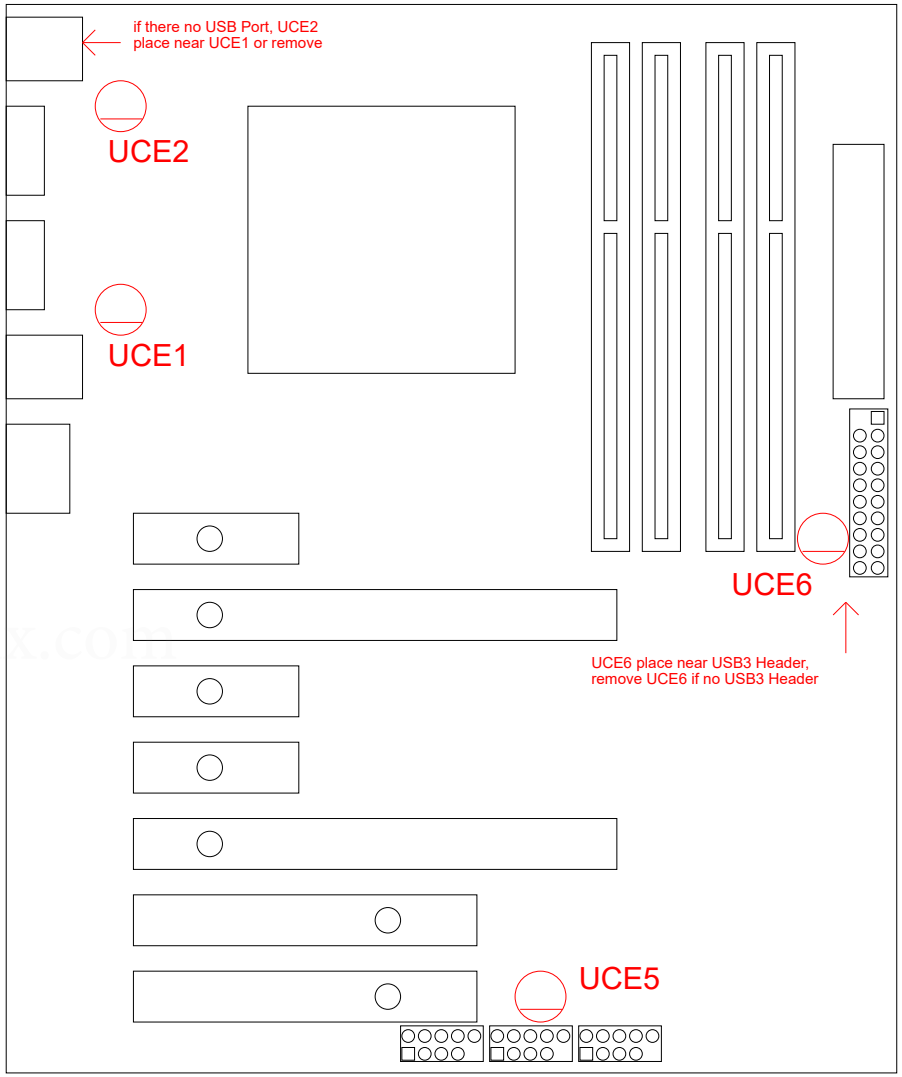
CAP PL 100UF/16V 6.3*9 DIP 20%

GAMING ：黑色11031-0001F500

PRO
：灰色11031-0001F400



USB Power CAP recommend placement



BOM	
N/A	mount
/X	unmount

STANDARD CIRCUIT	
XUMB	USB
CS_USB_0.2E	

HD_DEMO_USB
/X

<Variant Name>

ASUSTEK COMPUTER INC

Title : USB Power CAP

Engineer: Kell_Huang

Size	Project Name	Rev
A3	Chipset USB Demo Circuit	0.0

Date: Friday, April 10, 2020 Sheet 104 of 127

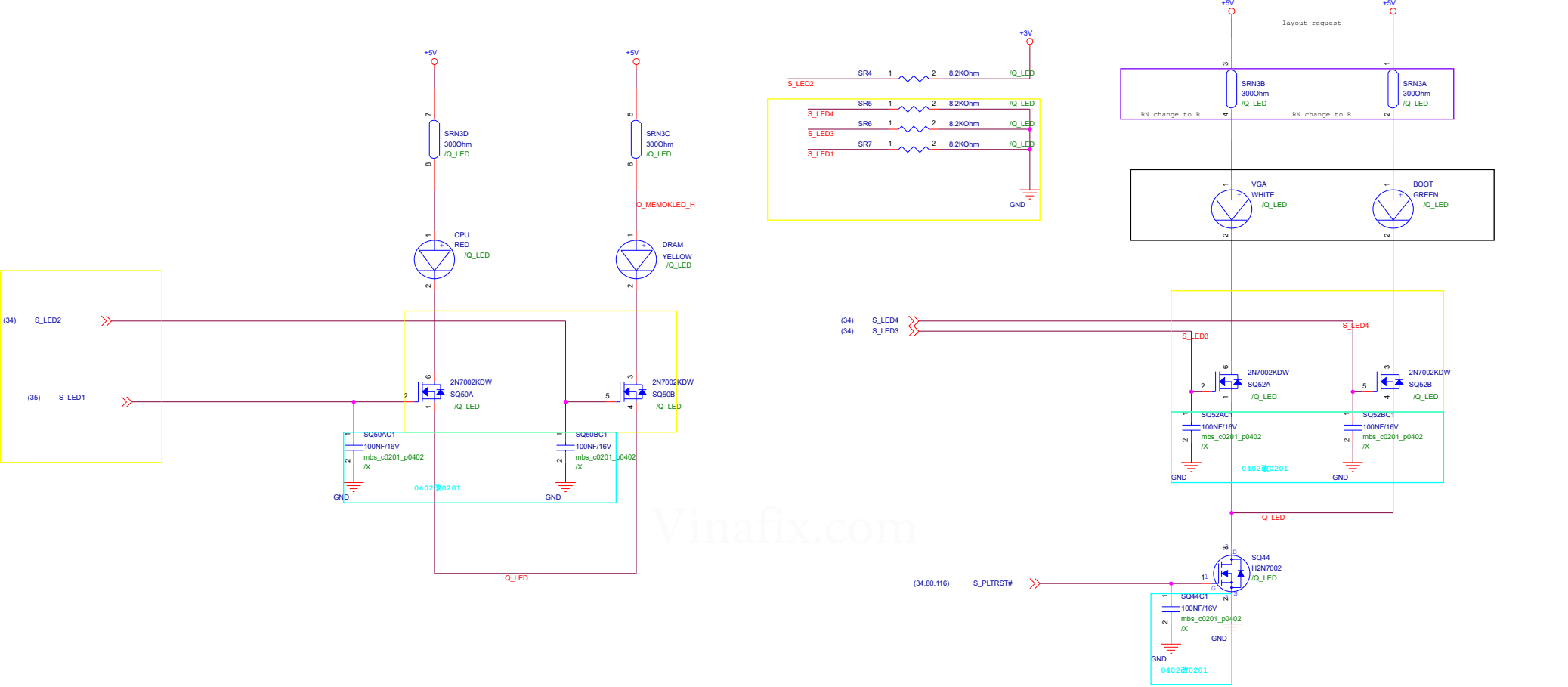
<Core Design>

ASUSTek Computer Inc.	Title : AI1315 IC	
	Engineer: Tom Yang	
Size: Custom	Project Name: Standard Circiut	Rev: 0.5A
Date: Tuesday, March 03, 2020	Sheet 106 of 127	

0.5A

<Core Design>

ASUSTek Computer Inc.	Title : BTN/LED	
	Engineer: Tom Yang	
Size: A3	Project Name: Standard Circiut	Rev: 0.5A
Date: Tuesday, March 03, 2020	Sheet 108 of 127	



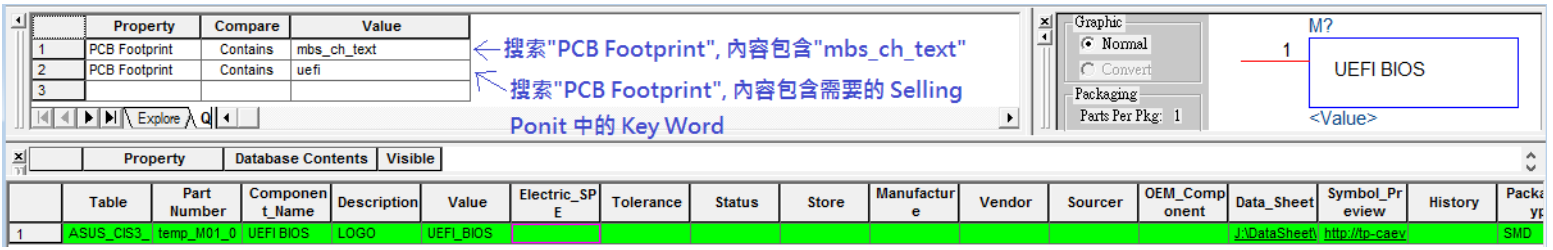
<Variant Name>

ASUSTeK COMPUTER INC	Title: SPTH EUP/LED Control	
	Engineer: Eason	
Size: A3	Project Name	Rev: R1.00
Date: Thursday, March 05, 2020	Sheet 110 of 127	

Selling Point

1. Selling Point 新增流程及窗口人員

2. 如何抓取 Selling Point Part, 如下圖



3. Example

<Variant Name>

ASUSTEK COMPUTER INC

Title : Selling Point

Engineer: SZ Design IP

Size A3 | Project Name: Silkscreen Demo Circuit | Rev 1.1A

Date: Tuesday, March 03, 2020 | Sheet 112 of 127

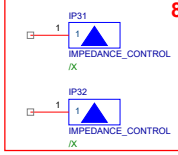
AMD Platform

You can only choose **8** pcs PCB Impedance point for your project

0 (must choose if use ASM1142/1143/2142/3142)

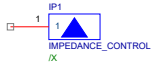
ASMedia USB 3.1 TX/RX

80 Ohm +/- 10%



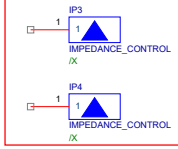
1

DRAM CMD



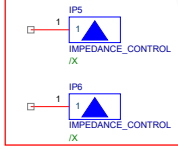
2

DRAM Clock



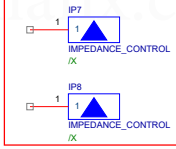
3

PCIE



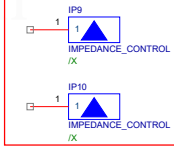
4

USB2.0



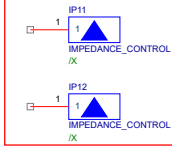
5

DRAM DQS



6

LAN



*** You can only choose 1 function to place point follow table ***

7

by Project

8

by Project

Delete it for EMS

<Variant Name>

ASUSTEK COMPUTER INC

Title : PCB Impedance Point

Engineer: SZ Design IP

Size	Project Name	Rev
A3	Silkscreen Demo Circuit	1.1A

Date: Tuesday, March 03, 2020 Sheet 114 of 127

Connect to EC is support UCSI / to PCH is support UCM

TB_I2C1_SDA
Please check I2C is dedicated
CFL(connection to PCH ISH_I2C2_SDA)
請在南橋端pull up 3.3VSB
CML(Connect to PCH GPP_C18)

TB_I2C1_SCL
Please check I2C is dedicated
CFL(connection to PCH ISH_I2C2_SCL2)
請在南橋端pull up 3.3VSB
CML(Connect to PCH GPP_C19)

TB_I2C1_IRQ#
CFL(Connect to PCH GPIO GPP_K0)
Make sure PCH supports SCI
請在南橋端pull up 3.3VSB
CML(Connect to PCH GPP_K13)

For S0IX PWR contorl

SLP_S0_PLT_N_10
Connect to S0IX Circuit

For RTD3 Support

TB_RTD3_POWER_EN
1.CFL(Connect to PCH GPP_I5)
2.請確認Platform
是否有支援RTD3
3.請接DGW GPIO
4.CML(Connect to PCH GPP_G5)

TB_CLKREQ#
1. 請確認是否有重複pull high
2. Pull up power well需要與PCH相同
3. need to connect to Dedicated CLKREQ

TB_PERST_N
1.CFL(Connect to GPIO GPP_F3)
2.請連接DGW GPIO
3.CML(Connect to GPIO GPP_G0)

TB_WAKE#
1.請連接DGW GPIO
2.需在pch端 pull high 3VSB
3.CML(Connect to GPIO GPP_G1)

限高區尚未定義在symbol中.
旁邊零件高度請勿高過11.5mm

TB_HEADER
HEADER_2X7P_K11
TBR205 8.2KOhm
TBR203 0Ohm 預留for debug
TB_I2C1_SCL
TB_I2C1_SDA
TB_I2C1_IRQ#
TB_RTD3_POWER_EN
TB_PERST_N
TB_WAKE#
SLP_S0_PLT_N_10
TB_FORCE_PWR
S_SLP_S3#
S_SLP_S4#
TB_RTD3_SW
GND

TB_FORCE_PWR
CML(Connect to PCH GPP_K16)

TB_RTD3_SW
請在南橋端pull up 3.3VSB
Default High ,Low is RTD3 support
CML(Connect to PCH GPP_G3)

TB_CIO_PLUG_EVENT_GPIO_0
CML(Connect to PCH GPP_K12)

c料號
待驗證完改v料

注意 : TB_Header 2nd source需注意是否有拉拔力過小
導致header housing太容易被拔起的問題,QTR
spec為5.5kg

TB_CIO_PLUG_EVENT
TBR202 0Ohm
TB_CIO_PLUG_EVENT_GPIO_0

TBR204 0Ohm /TB
S_SLP_S3#
SLP_S0_PLT_N_10

注意: 支援RTD3需要TB_CLKREQ#, 請確認各個PCIE solt需要將CLKREQ#接出來

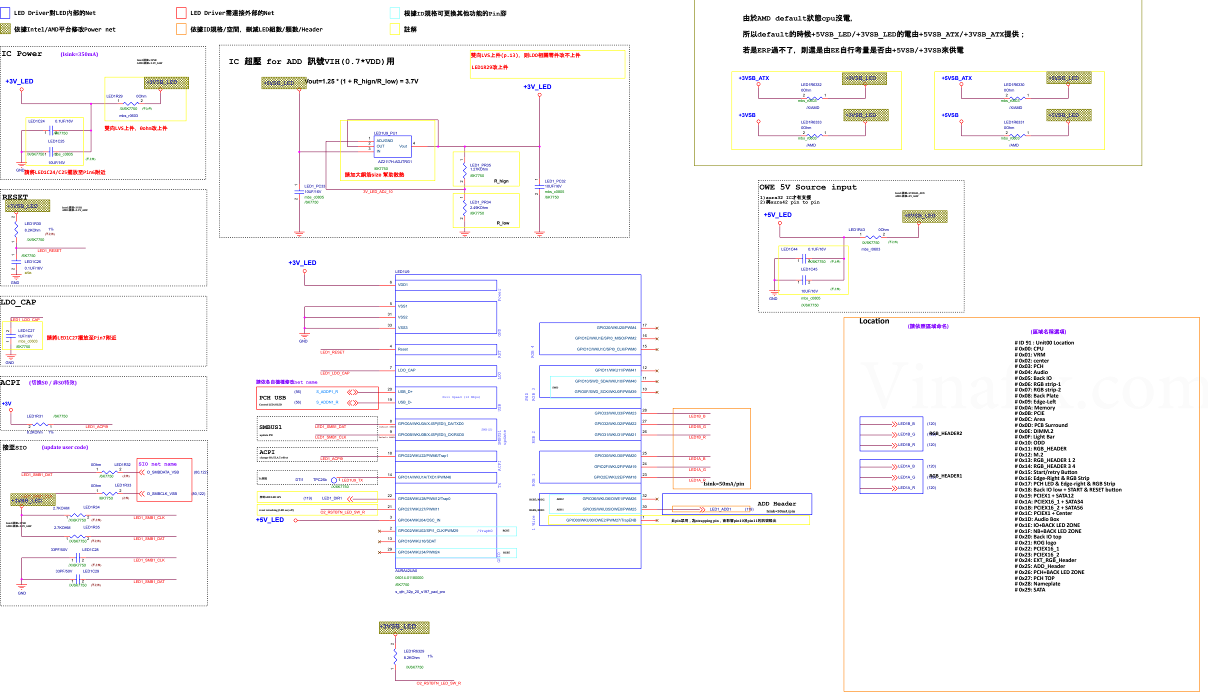
+3VSB
For ESD-Protection
TBD100 BAV99W /X/TB
TBR201 1MOhm
GND

TBR201 主要是當cable沒上時 , 讓PCH的TB_CIO_PLUG_EVENT input pin不要floating.

<Variant Name>

ASUSTeK Computer Inc.

Title : TR_TB_HEADER
Engineer: Brian Hsieh
Size: A2
Project Name: THUNDERBOLT
Rev: 0.5I
Date: Thursday, March 05, 2020
Sheet 117 of 127


LED Driver對LED內部的Net
LED Driver需連接外部的Net
根據ID規格可更換其他功能的Pin腳
依據Intel/AMD平台修改Power net
依據ID規格/空間，刪減LED組數/顆數/Header
註解
IC Power (Isink=350mA)
+3V_LED
+3VSB_LED
雙向LVS上件，0ohm改上件
請將LED1C24/C25擺放靠Pin6附近
RESET
LDO_CAP
請將LED1C27擺放靠Pin7附近
ACPI (切換S0 / 非S0時效)
接至SIO (update user code)
IC 超壓 for ADD 訊號VIH(0.7*VDD)用
Vout=1.25 * (1 + R_hign/R_low) = 3.7V
雙向LVS上件(p.13)，則LDO相關零件改不上件
LED1R29改上件
請加大銅箔size 幫助散熱
R_hign
R_low
由於AMD default狀態cpu沒電,
所以default的時候+5VSB_LED/+3VSB_LED的電由+5VSB_ATX/+3VSB_ATX提供；
若是ERP過不了，則還是由EE自行考量是否由+5VSB/+3VSB來供電
+3VSB_ATX
+5VSB_ATX
+3VSB
+5VSB
OWE 5V Source input
+5V_LED
+5VSB_LED
PCH USB
SMBUS1
ACPI
請依各自機種修改net name
+5V_LED
Isink=50mA/pin
ADD Header
Location
(請依照區域命名)
(區域名稱選項)
ID 91 : Unit00 Location
0x00: CPU
0x01: VRM
0x02: center
0x03: PCH
0x04: Audio
0x05: Back IO
0x06: RGB strip-1
0x07: RGB strip-2
0x08: Back Plate
0x09: Edge-Left
0x0A: Memory
0x0B: PCIE
0x0C: Area
0x0D: PCB Surround
0x0E: DIMM.2
0x0F: Light Bar
0x10: ODD
0x11: RGB_HEADER
0x12: M.2
0x13: RGB_HEADER 1 2
0x14: RGB_HEADER 3 4
0x15: Start/retry Button
0x16: Edge-Right & RGB Strip
0x17: PCH LED & Edge-right & RGB Strip
0x18: Back IO low + START & RESET button
0x19: PCIEX1 + SATA12
0x1A: PCIEX16_1 + SATA34
0x1B: PCIEX16_2 + SATA56
0x1C: PCIEX1 + Center
0x1D: Audio Box
0x1E: IO+BACK LED ZONE
0x1F: NB+BACK LED ZONE
0x20: Back IO top
0x21: ROG logo
0x22: PCIEX16_1
0x23: PCIEX16_2
0x24: EXT_RGB_Header
0x25: ADD_Header
0x26: PCH+BACK LED ZONE
0x27: PCH TOP
0x28: Nameplate
0x29: SATA
RGB_HEADER2
RGB_HEADER1
LED1B_B
LED1B_G
LED1B_R
LED1A_B
LED1A_G
LED1A_R

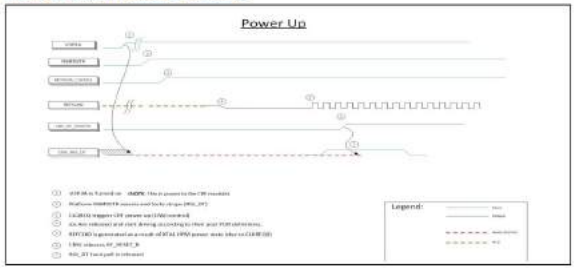
<Variant Name>

ASUSTek Computer Inc.		Title :	AURA42(32Pin)
		Engineer:	Kaizer_Luo
Size: Custom	Project Name: LED Standard Circiut		Rev: 1.6
Date: Thursday, March 05, 2020		Sheet 118	of 127

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 03, 2020	Sheet 121 of 127	

Power/Reset Sequence :

Figure 42-12.CNVi Power up Sequence



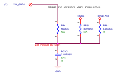
Name	Description	Value [mA]	Notes
Peak current	Peak current from 3.3 V supply, including Wi-Fi and BT. Averaged over 25 use cases.	1540mA	

+3.3VSB_WLAN_SWITCH & POWER CIRCUIT

I217_I218

ASUSTek COMPUTER INC.	Title : M.2_KEY_E Power	
	Engineer: Likes_Li	
Size: A2	Project Name: M.2_KEY_E Power	Rev: 0.01E
Date: Tuesday, March 03, 2020	Sheet 124 of 127	

0.1A Beta



<Variant Name>

ASUS	Title : PWM_Port_G		
ASUSTek Computer Inc.	Engineer: Kaizer_Luo		
Size: A3	Project Name: LED Standard Circiut		Rev: 1.0
Date: Thursday, March 05, 2020	Sheet: 127	of 127	