

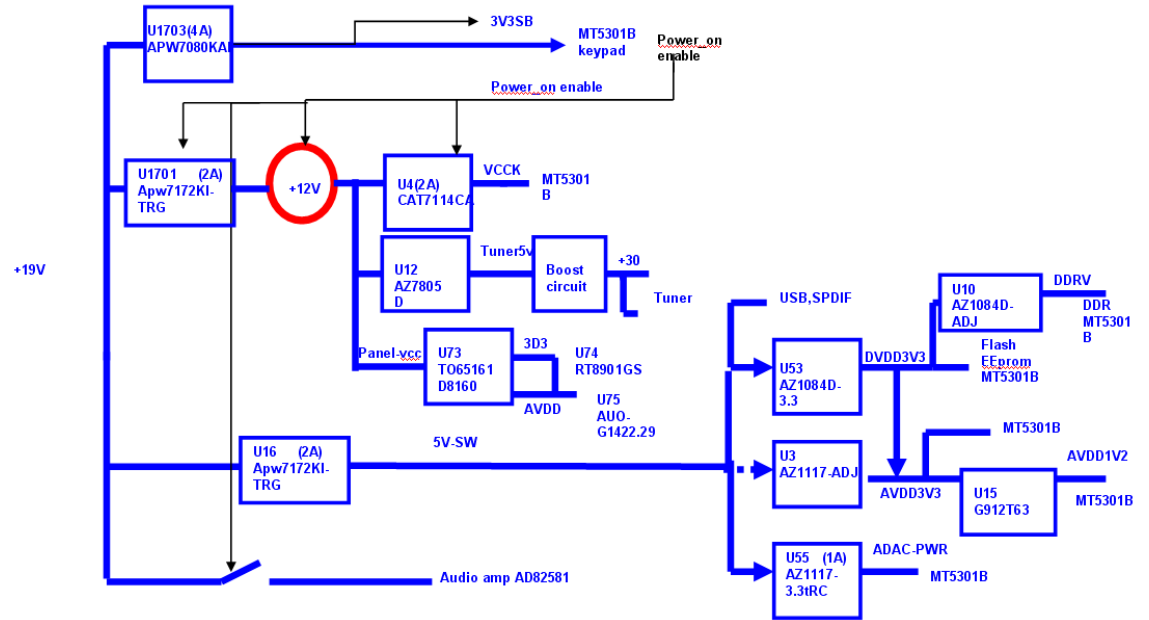
MT5301B (DDR2)

VERSION V1.0

CASE	MT5301B 公版			MT5301B(Briviw)	
	Scaler Pin No.	To	Description	To	Description
GPI00	246	JK3 (16) JK4 (18)	GOE_A	J18 (57)	GOE_A
GPI01	247	JK3 (21) JK4 (23)	POL_A	J19 (21)	POL_A
GPI02	248	JK3 (18) JK4 (20)	GSC_A	J18 (55)	GSC_A
GPI03	250	JK3 (20) JK4 (22)	GSP_A	J18 (54)	GSP_A
GPI04	256	UK3 (5)	FLK_A	X	FLK_A
GPI06	252	JK3 (20) JK4 (22)	GSP_R_A	J18 (58)	GSP_R_A
GPI07	254	JK3 (22) JK4 (24)	SOE_A	J19 (20)	SOE_A
GPI08	255	UK3 (32)	DPM_A	U74 (6)	DPM_A
GPI010	249	JK4 (46)	OPT_P	X	OPT_P
GPI011	251	JK4 (45)	OPT_N	X	OPT_N
GPI012	253	JK3 (19) JK4 (21)	H_CONV	U75 (16)	H_CONV for PG nWR
GPI013	243	PA2 (3)	HPDET#	J90 (4)	HPDETr
GPI014	2	QL3 (1)	LVDS_PWR_EN	Q15 (G)	LVDS_PWR_EN
OPCTRL0	137	UH4 (32)	HDMI_SW_CTRL1	J6 (10)	if Keypad I2C: SDA else Keypad DAC: LED_B
OPCTRL1	138	UH4 (33)	HDMI_SW_CTRL2	J6 (12)	Keypad I2C SCL
OPCTRL2	132	DH31 (2)	2PWR5V_1	X	X
OPCTRL3	130	DH15 (2)	1PWR5V_1	J6 (8)	LED_R
OPCTRL4 (AIN_CTL1)	131	QA24 (1) KJP1 (2)	Audio MUX CTRL: MUX_CTLB STRAPPING	R69	STRAPPING
OPCTRL5	129	QA27 (1) RW1	Audio MUX CTRL: MUX_CTLC STRAPPING	R67	STRAPPING
ADIN2_SRV	145	QA25 (1)	Audio MUX CTRL: MUX_CTLA	X	X
ADIN3_SRV	146	QL2 (1)	BL_ON/OFF	X	X
ADIN4_SRV	147	JT1 (48)	RF_AGC1	X	X
PWR5V	127	DH9 (2)	3PWR5V_1	U51 (49)	PWR5V_1
OPWM0	104	QL1 (1)	BL_DIMMING	Q1 (B)	BL_DIMMING
AOSDATA1	207	KJP2 (2) UA4 (7)	STRAPPING SCT2 Audio Out	R71	STRAPPING
PDD0	227	UM5 (7)	SYS_EEPROM_WP	U6 (7)	SYS_EEPROM_WP
PDD1	228	QH1 (1) QH9 (1) QH6 (1)	EDID_EEPROM_WP	QH1 (B) QH2 (B) QH3 (B)	EDID_EEPROM_WP
PDD2	229	UU1 (4)	USB_PWR_EN0	Q4 (B)	BL_ON/OFF
PDD3	230	UU2 (4)	USB_PWR_EN1	U51 (17)	U1TX HDMI Switch Reset
PDD4	231	UU1 (5)	USB_PWR_OCP0	J10 (32)	MEMCSEL0
PDD5	232	UU2 (5)	USB_PWR_OCP1	X	X
POCE1_	239	UM2 (7)	POCE1#	X	X
PARB_	238	X	X	X	X
POWE_	242	QA12 (1)	MUTE_CTL	Q25 (B)	MUTE_CTL
PAALE	241	X	X	X	X
PACLE	240	X	X	X	X
DEM0D_TSCCLK	7	JT2 (56)	DEM0D_TSCCLK	J6 (7)	Keypad Inetruprt
DEM0D_TSSYNC	219	JT2 (54)	DEM0D_TSSYNC	Q13 (E)	AMP Power Down
DEM0D_TSVAL	218	JT2 (21)	DEM0D_TSVAL	J10 (26)	PANEL_SEL
DEM0D_TSDATA0	220	JT2 (19)	DEM0D_TSDATA0	X	X
DEM0D_RST	214	JT2 (23)	DEM0D_RST	X	X
SPI_CLK	223	JT2 (9)	SPI_CLK	Q11 (B)	Audio MUX CTRL: MUX_CTLA(AIN_CTL0)
SPI_CLE	225	JT2 (7)	SPI_CLE	J10 (34)	MEMC_SEL1
SPI_DATA	224	JT2 (42)	SPI_DATA	Q10 (B)	Audio MUX CTRL: MUX_CTLB(AIN_CTL1)

Power tree(MT5301B)

BriView



<Variant Name>

BriView

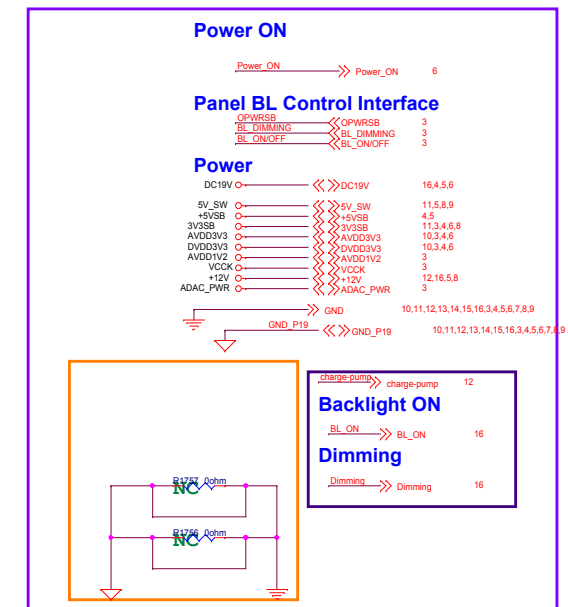
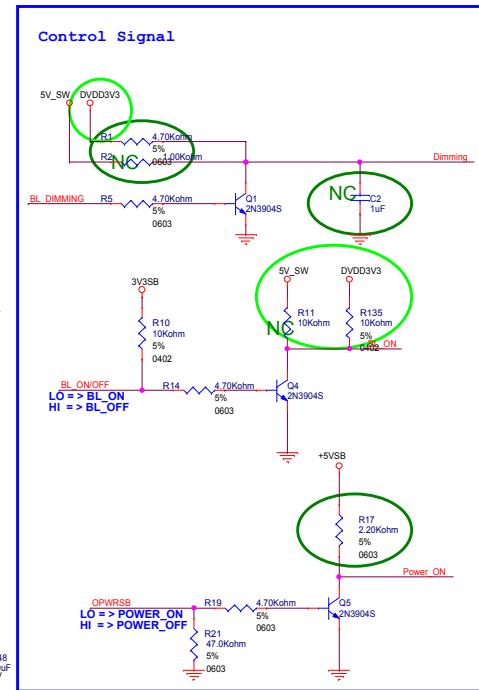
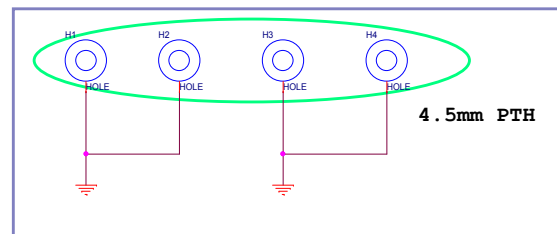
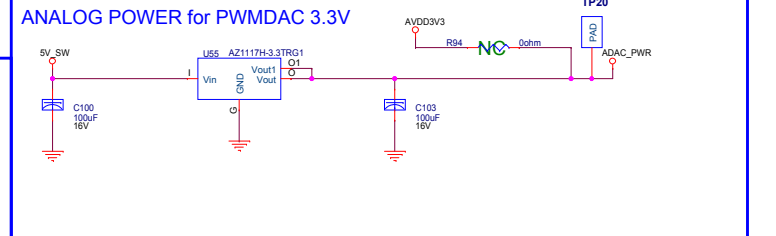
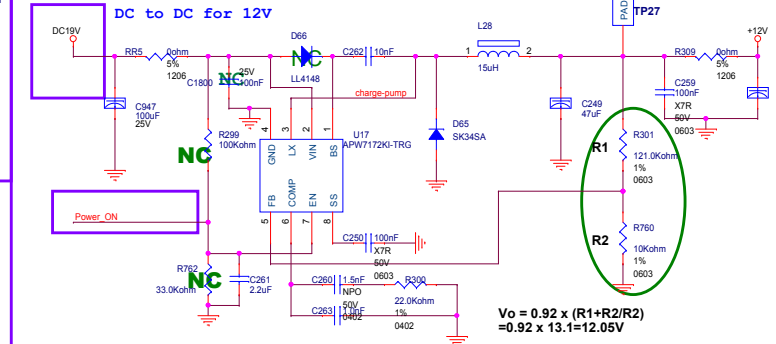
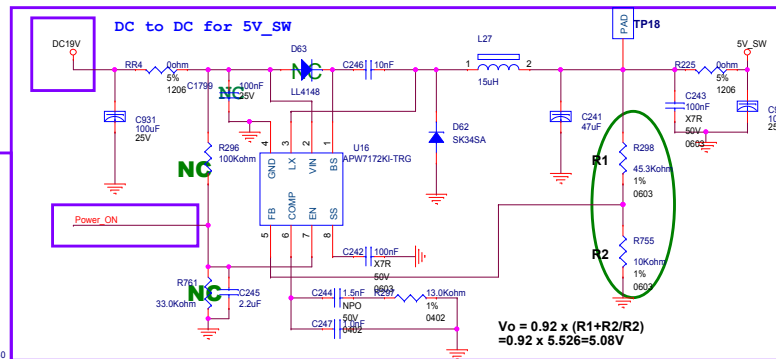
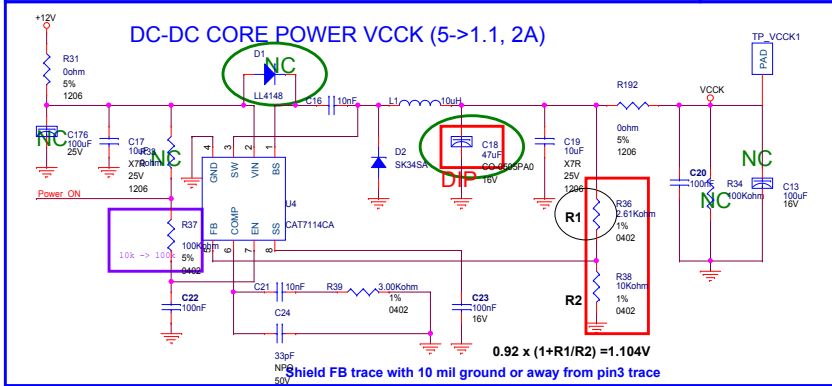
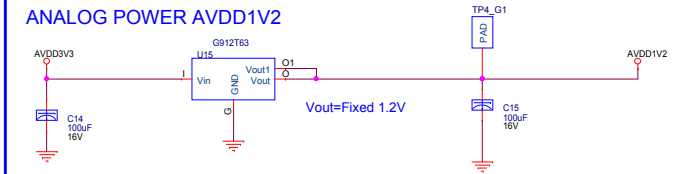
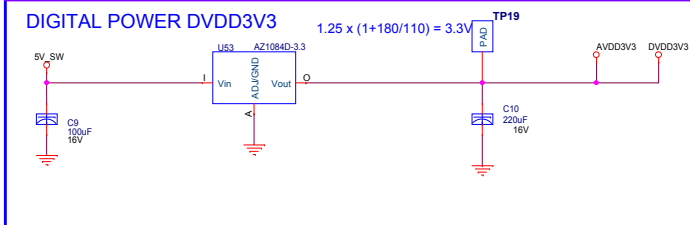
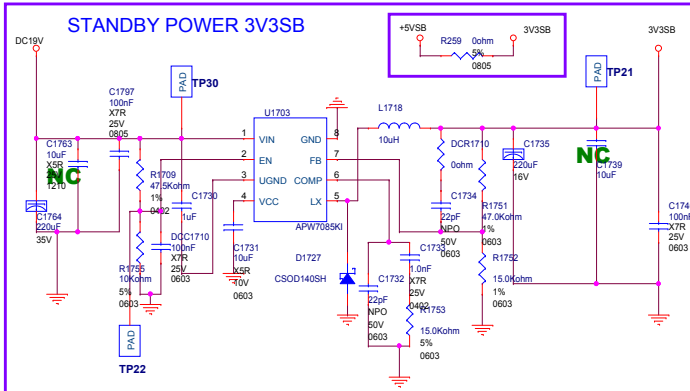
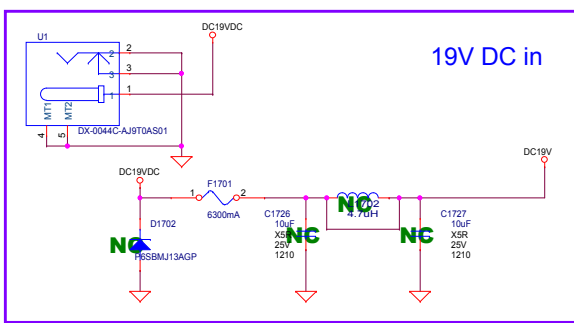
Model Name
MT5301B for G2.0-32"

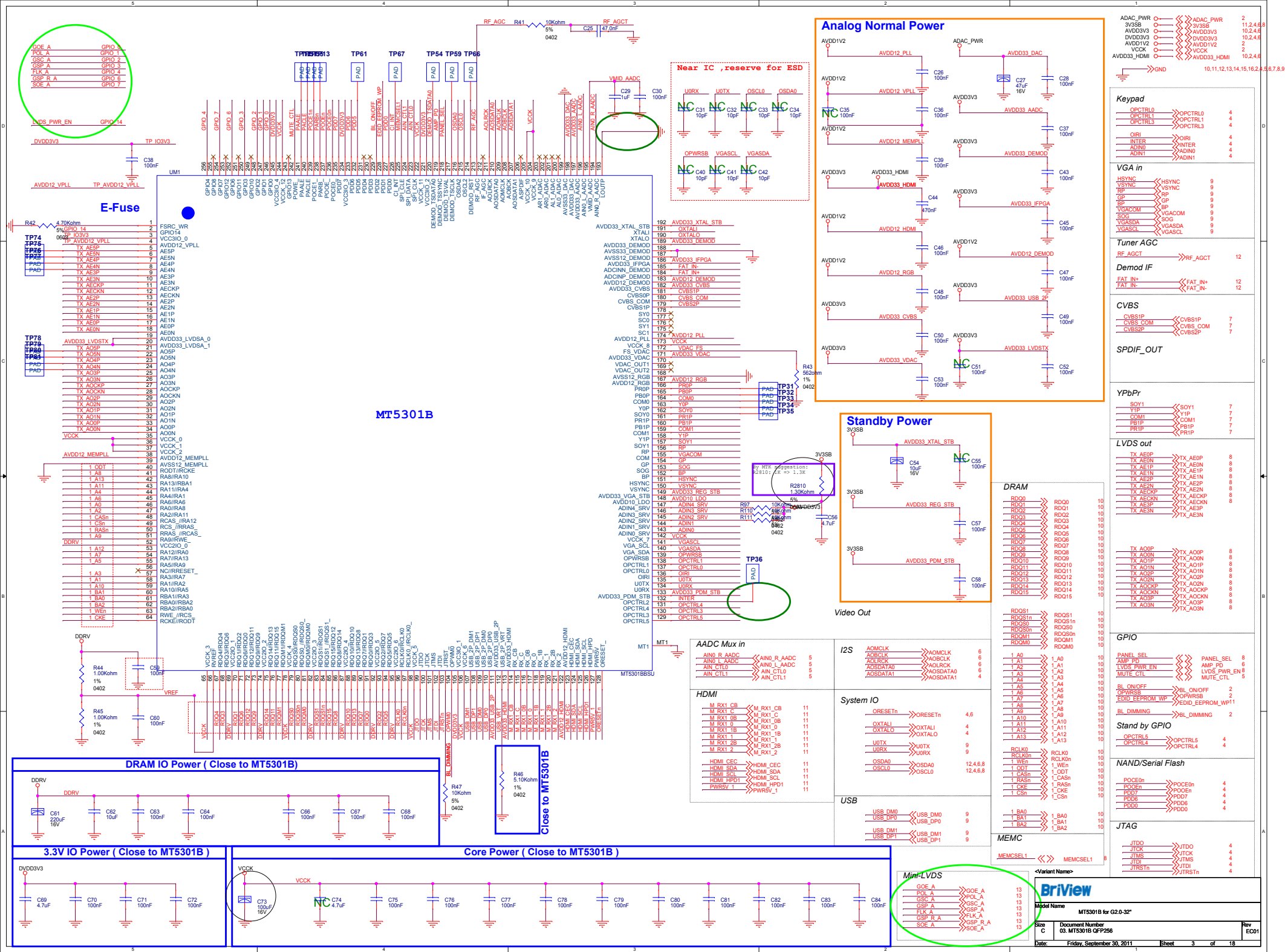
Size
Custom 01: Block Diagram/GPIO List

Date: Friday, September 30, 2011

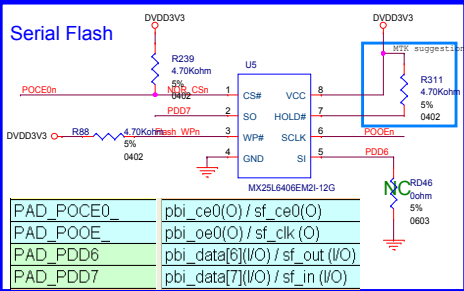
Sheet 1 of 18

Rev
EC01



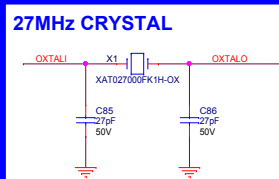


Serial Flash

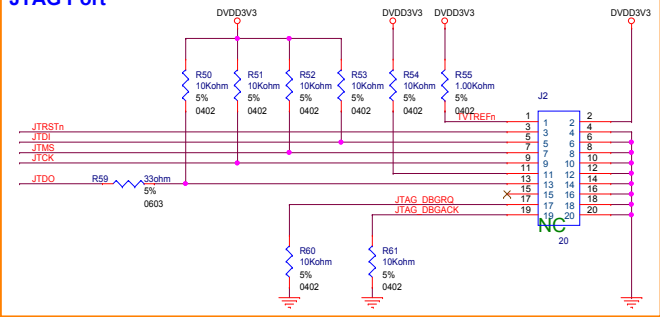


PAD_POCE0	pbi_ce0(O) / sf_ce0(O)
PAD_POE0	pbi_oe0(O) / sf_clk(O)
PAD_PDD6	pbi_data[6](I/O) / sf_out(I/O)
PAD_PDD7	pbi_data[7](I/O) / sf_in(I/O)

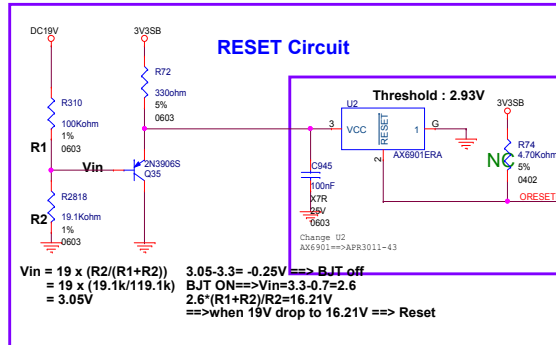
27MHz CRYSTAL



JTAG Port



RESET Circuit



$V_{in} = 19 \times (R2 / (R1 + R2))$
 $= 19 \times (19.1k / 119.1k)$
 $= 3.05V$
 $3.05 - 3.3 = -0.25V \Rightarrow$ **BJT off**
BJT ON $\Rightarrow V_{in} = 3.3 - 0.7 = 2.6$
 $2.6 \times (R1 + R2) / R2 = 16.21V$
 $\Rightarrow$ when 19V drop to 16.21V $\Rightarrow$ Reset



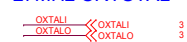
Serial Flash



JTAG Port



27MHz CRYSTAL



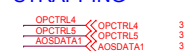
UART0



RESET Circuit



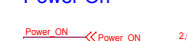
STRAPPING



Keypad



Power On



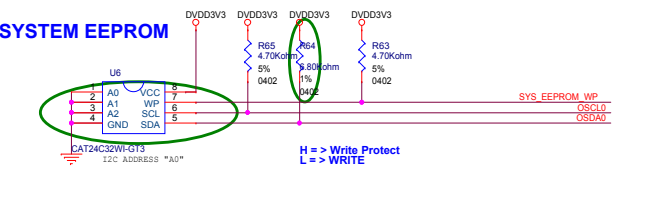
<Variant Name>

Briview

Model Name MT5301B for G2.0-32"

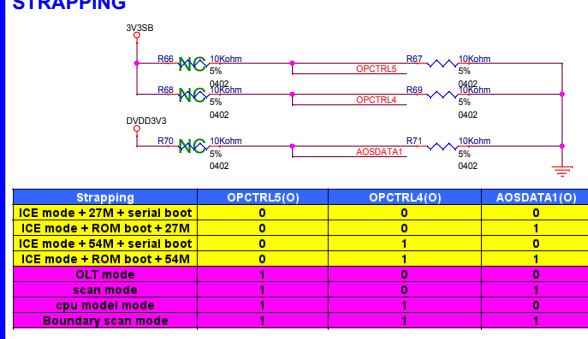
Size	Document Number	Rev
C	04_Peripheral	E001
Date:	Friday, September 30, 2011	Sheet 4 of 18

SYSTEM EEPROM



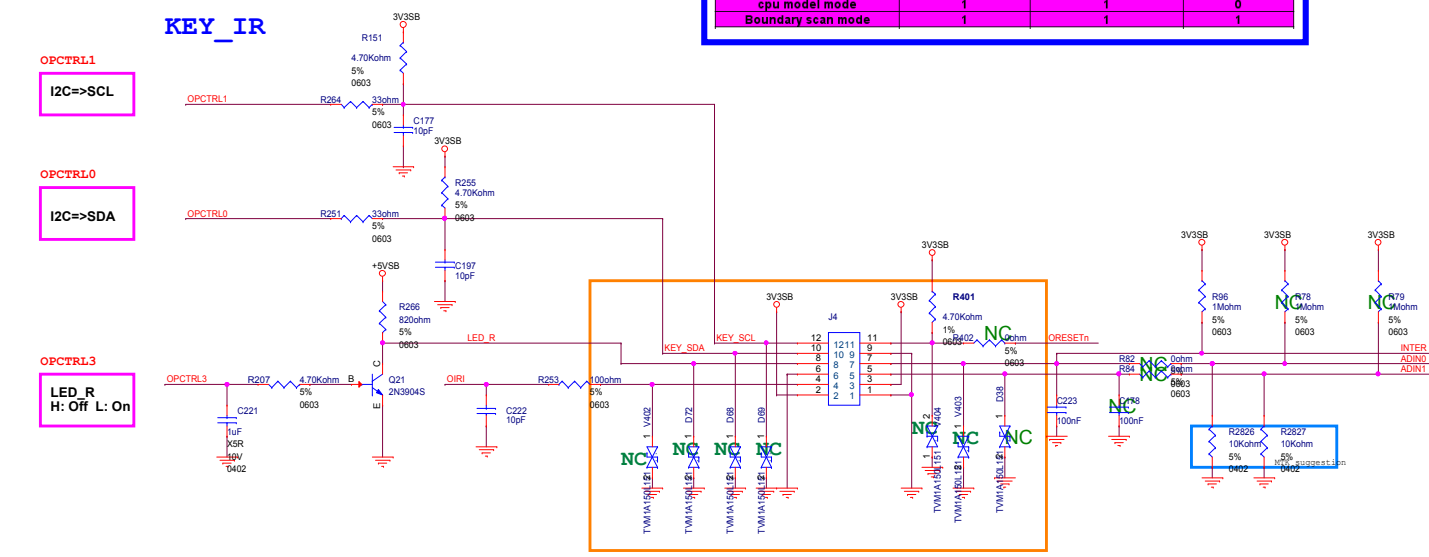
H => Write Protect
L => WRITE

STRAPPING



Strapping	OPCTRL5(O)	OPCTRL4(O)	AOSDATA1(O)
ICE mode + 27M + serial boot	0	0	0
ICE mode + ROM boot + 27M	0	0	1
ICE mode + 54M + serial boot	0	1	0
ICE mode + ROM boot + 54M	0	1	1
OLT mode	1	0	0
scan mode	1	0	1
cpu model mode	1	1	0
Boundary scan mode	1	1	1

KEY_IR



OPCTRL1

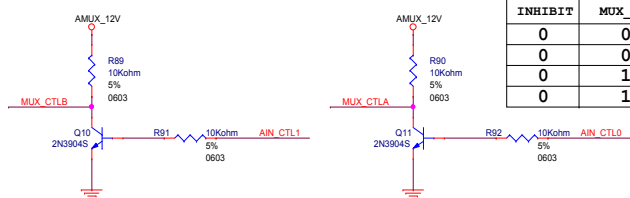
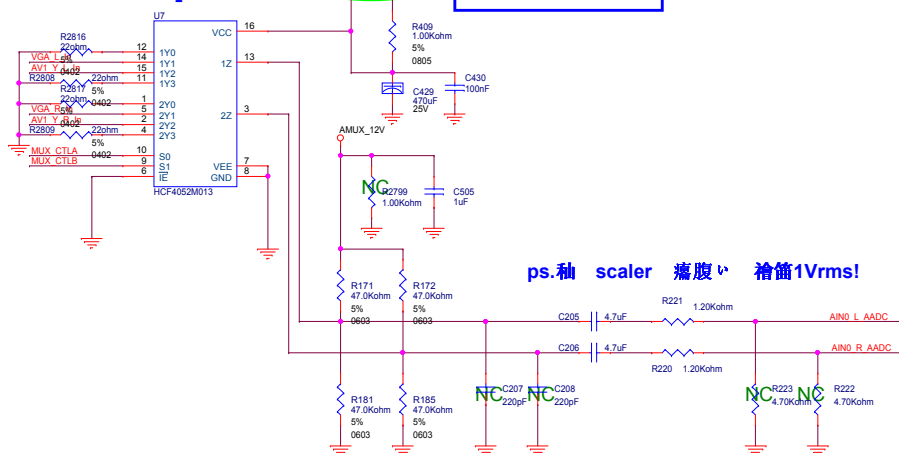
I2C=>SCL

OPCTRL0

I2C=>SDA

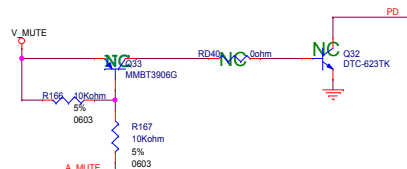
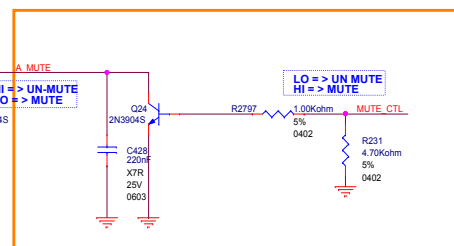
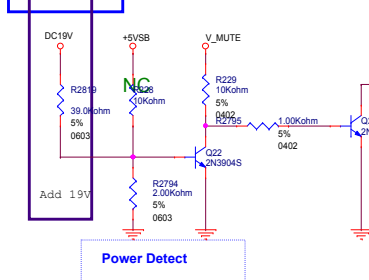
OPCTRL3

LED_R
H: Off L: On

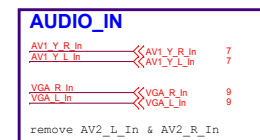
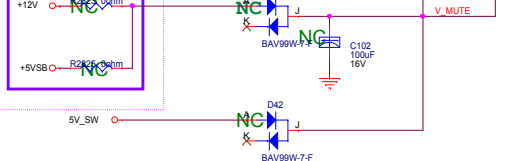


INHIBIT	MUX_CTLA	MUX_CTLB	
0	0	0	X
0	0	1	VGA
0	1	0	YPbPr/AV1
0	1	1	X

For AC ON Pop Noise
DC ON Pop Nose
DC OFF Pop Noise

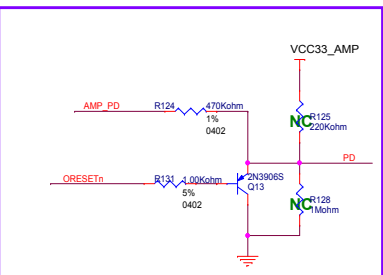
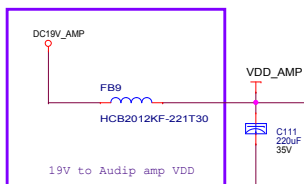
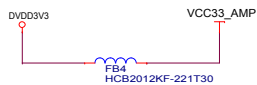


B2026 Oshun

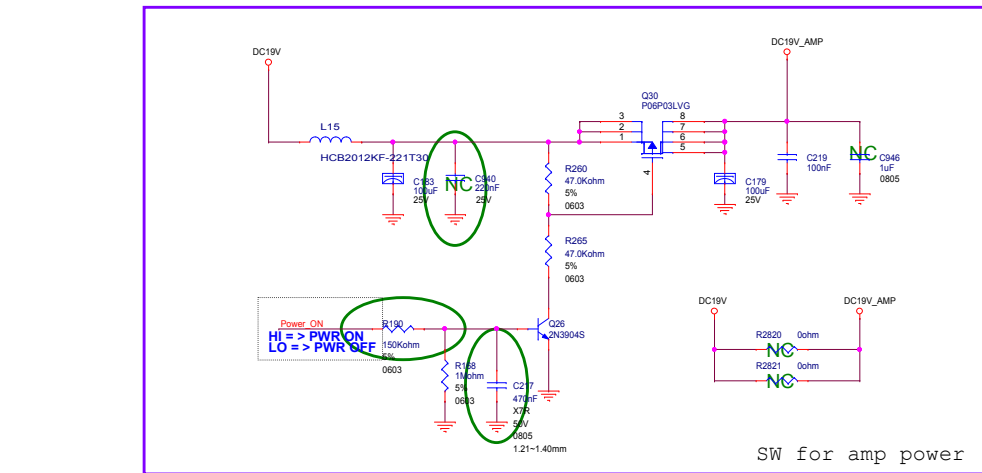


<u>AIN0_R_AADC</u>	→	AIN0_R_AADC	3
<u>AIN0_L_AADC</u>	→	AIN0_L_AADC	3
<u>AIN_CTL0</u>	←	AIN_CTL0	3
<u>AIN_CTL1</u>	←	AIN_CTL1	3
<u>PD</u>	↔	PD	6
<u>MUTE_CTL</u>	↔	MUTE_CTL	3

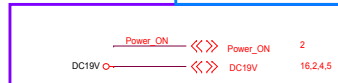
DC19V	DC19V	16,2,4,6
5V_SW	5V_SW	3,4
AVDD03V3	AVDD03V3	11,2,8,9
+12V	+12V	10,2,3,4,6
VCC0	VCC0	12,16,2,8
	GND	2,3
		10,11,12,13,14,15,16,2,3,4,6,7,8,9



19V - 15V = 4V => Vbe = 4V - 3.3V = 0.7V => BJT OFF When
+19V Drop to 17.6V => 17.6V - 15V = 2.6V => Vbe = 2.6V -
3.3V = - 0.7V => BJT ON => AMP Mute



SW for amp power



Power_ON <<> Power_ON 2
DC19V <<> DC19V 16,2,4,5

AOMCLK <<> AOMCLK 3
AOBCLK <<> AOBCLK 3
AOLRCK <<> AOLRCK 3
AOSDATA0 <<> AOSDATA0 3

AMP_PD <<> AMP_PD 3
PD <<> PD 5

OSDA0 <<> OSDA0 12,3,4,8
OSCL0 <<> OSCL0 12,3,4,8

<<> GND 10,11,12,13,14,15,16,2,3,4,5,7,8,9

DVDD3V3 <<> DVDD3V3 10,2,3,4
3V3SB <<> 3V3SB 11,2,3,4,8
+12V <<> +12V 12,16,2,5,8

ORESETn <<> ORESETn 3,4
DC19V_AMP <<> DC19V_AMP 12

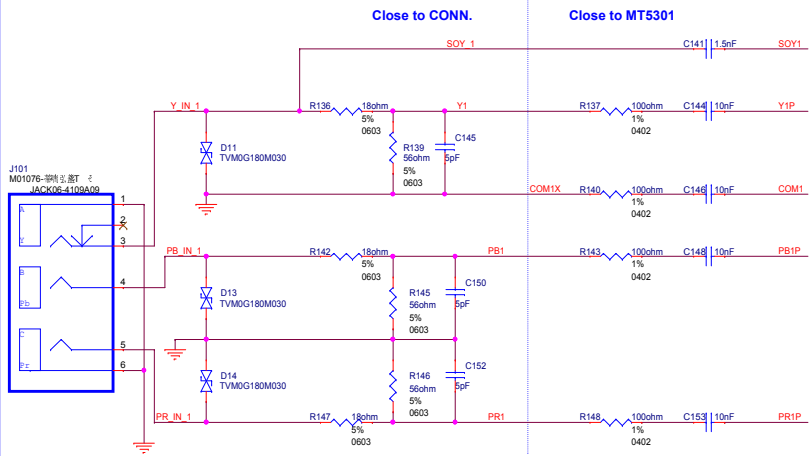
<Variant Name>

Briview

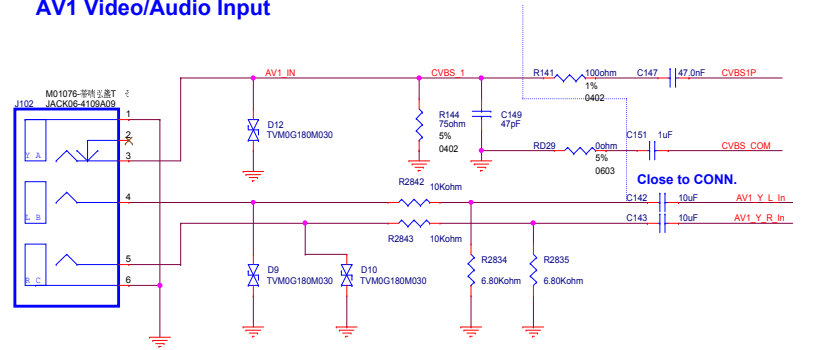
Model Name MT5301B for G2.0-32"

Size C Document Number 06_Audio AMP_AD82581B Rev EC01
Date: Friday, September 30, 2011 Sheet 6 of 18

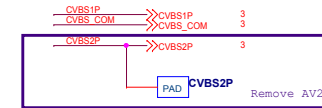
YPbPr1 Video Input



AV1 Video/Audio Input



AV in



YPbPr in



AV1 Audio shared YPbPr Audio



<Variant Name>

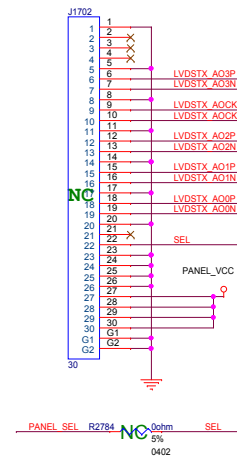
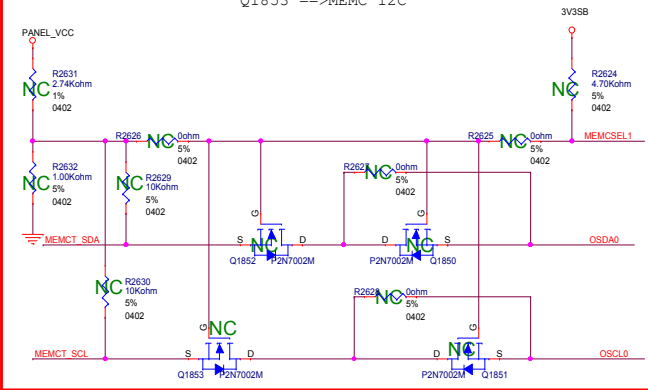
Briview

Model Name
MT5301B for G2.0-32"

Size C	Document Number 07_YPbPr/CVBS	Rev EC01
Date:	Friday, September 30, 2011	Sheet 7 of 18

MEMC I2C Buffer

Stuff R2625 , Q1850 , Q1851 , Q1852 ,
Q1853 ==>MEMC I2C

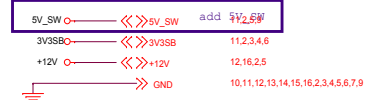
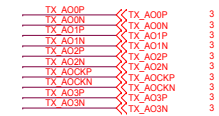
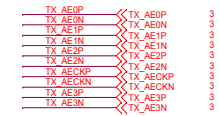
 友達光電
AUO OptoelectronicT315XW06 V4 Product Specification
Rev. 0.0

3-2Interface Connections:

- LCD connector: 196337-30041-3 (P-TWO, FFC connector)

Pin	Symbol	Description
1	V _{DD}	Power Supply, +12V DC Regulated
2	V _{DD}	Power Supply, +12V DC Regulated
3	V _{DD}	Power Supply, +12V DC Regulated
4	V _{DD}	Power Supply, +12V DC Regulated
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	LVDS_SEL	OpenH3(3.3V) for NS, Low (nD) for JEIDA
10	N.C.	ALU Internal Use Only
11	GND	Ground
12	CH1_0-	LVDS Channel 1, Signal 0-
13	CH1_0+	LVDS Channel 1, Signal 0+
14	GND	Ground
15	CH1_1-	LVDS Channel 1, Signal 1-
16	CH1_1+	LVDS Channel 1, Signal 1+
17	GND	Ground
18	CH1_2-	LVDS Channel 1, Signal 2-
19	CH1_2+	LVDS Channel 1, Signal 2+
20	GND	Ground
21	CH1_CLK-	LVDS Channel 1, Clock -
22	CH1_CLK+	LVDS Channel 1, Clock +
23	GND	Ground
24	CH1_3-	LVDS Channel 1, Signal 3-
25	CH1_3+	LVDS Channel 1, Signal 3+
26	GND	Ground
27	N.C.	ALU Internal Use Only
28	N.C.	ALU Internal Use Only
29	N.C.	ALU Internal Use Only
30	GND	Ground

Note: N.C. : please leave this pin unoccupied. It can not be connected by any signal (Low/GND/High)

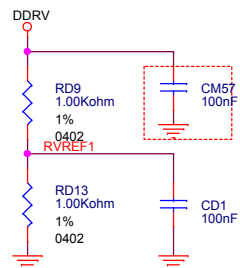


<Variant Name>

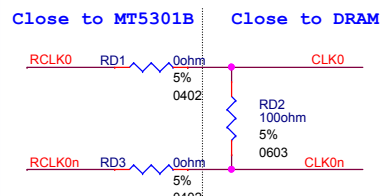
BriView

Model Name	MT5301B for G2.0-32"
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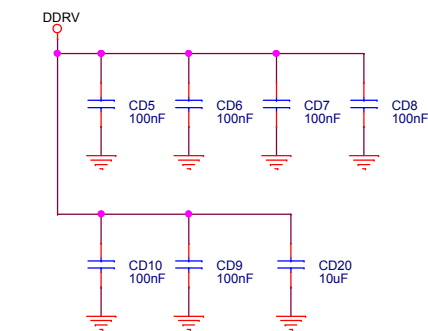
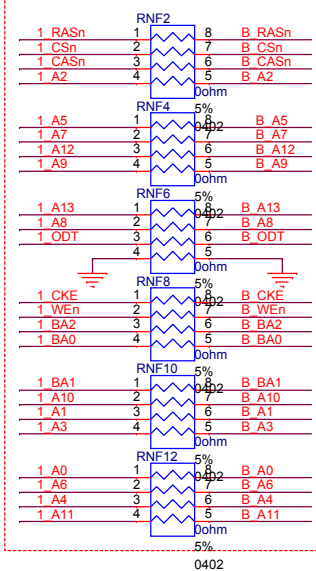
Size C	Document Number 08.LVDS	Rev EC01
Date:	Friday, September 30, 2011	Sheet 8 of 18



Close to MT5301B Close to DRAM

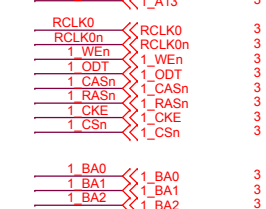
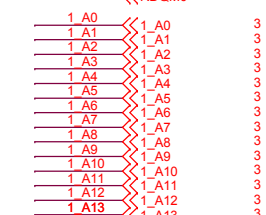
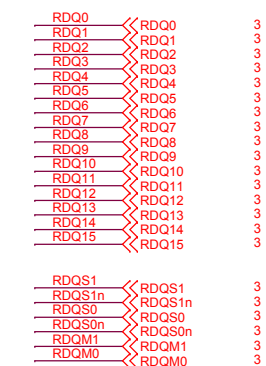
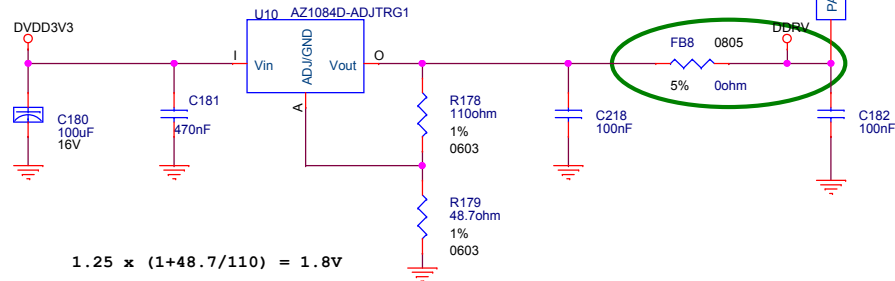


The schematic diagram illustrates a 16-channel transceiver architecture. At the center is a 0.402-GHz oscillator. This oscillator is connected to two 5% dividers. Each divider's output is fed into a series of 8-channel multiplexers (RNF2, RNF4, RNF6, RNF8, RNF10, RNF12). The multiplexers are connected to two sets of 8-channel multiplexers (RNF2, RNF4, RNF6, RNF8, RNF10, RNF12). Each multiplexer is connected to a 5% divider and a 0.402-GHz oscillator. The multiplexers are connected to two sets of 8-channel multiplexers (RNF2, RNF4, RNF6, RNF8, RNF10, RNF12). Each multiplexer is connected to a 5% divider and a 0.402-GHz oscillator. The multiplexers are connected to two sets of 8-channel multiplexers (RNF2, RNF4, RNF6, RNF8, RNF10, RNF12). Each multiplexer is connected to a 5% divider and a 0.402-GHz oscillator.



$1.25 \times (1 + 48.7 / 110) = 1.8\text{V}$

$$1.25 \times (1 + 48.7/110) = 1.8V$$



<Variant Name>

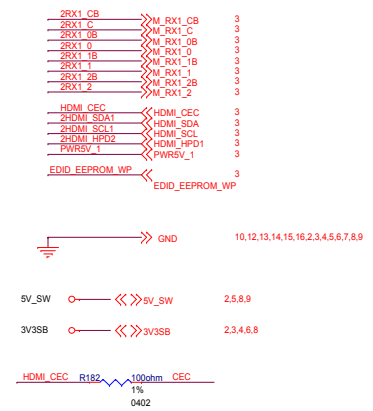
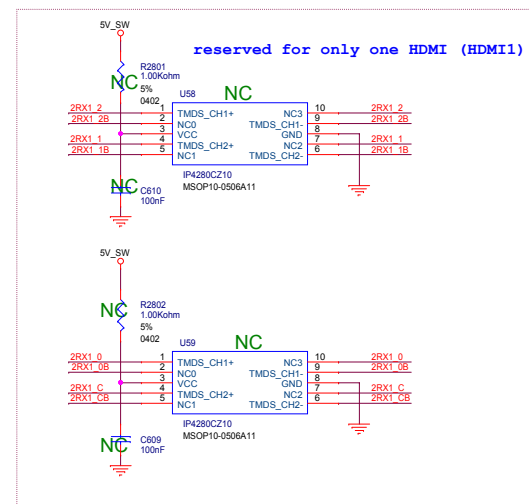
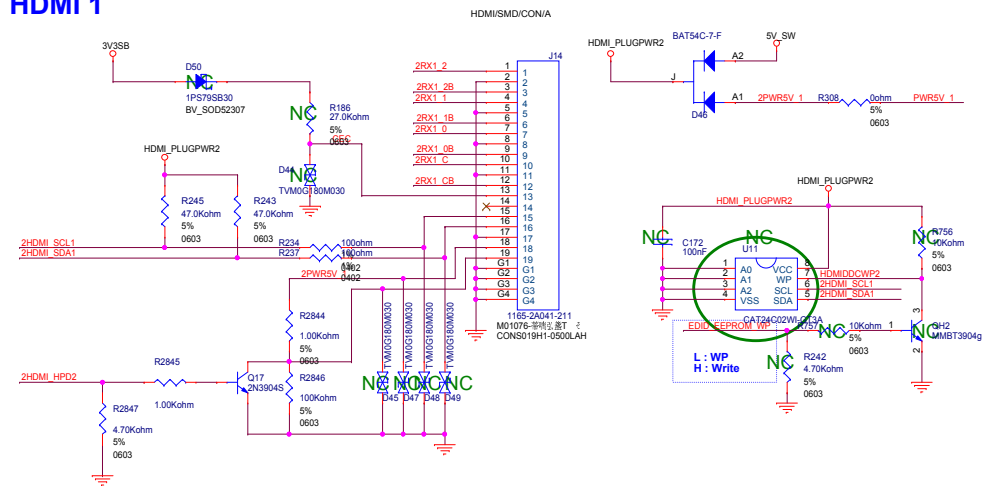
Model Name	MT5301B for G2.0-32"
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Size B	Document Number 10. DRAM Interface
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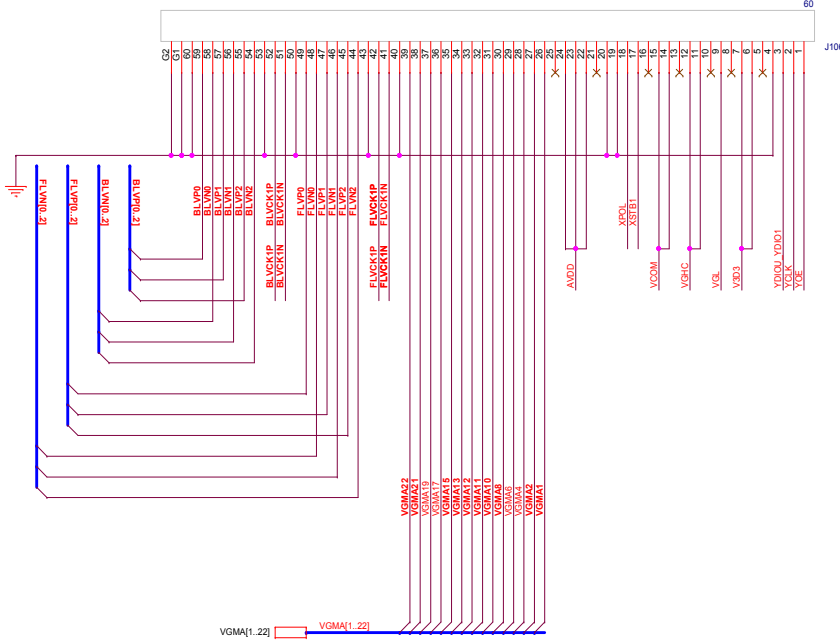
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HDMI 1

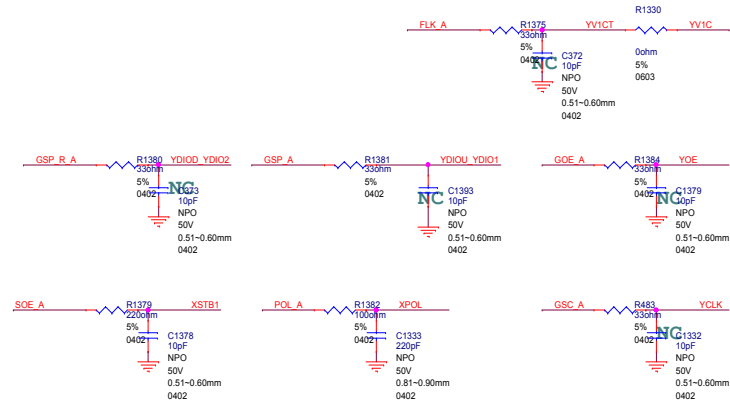


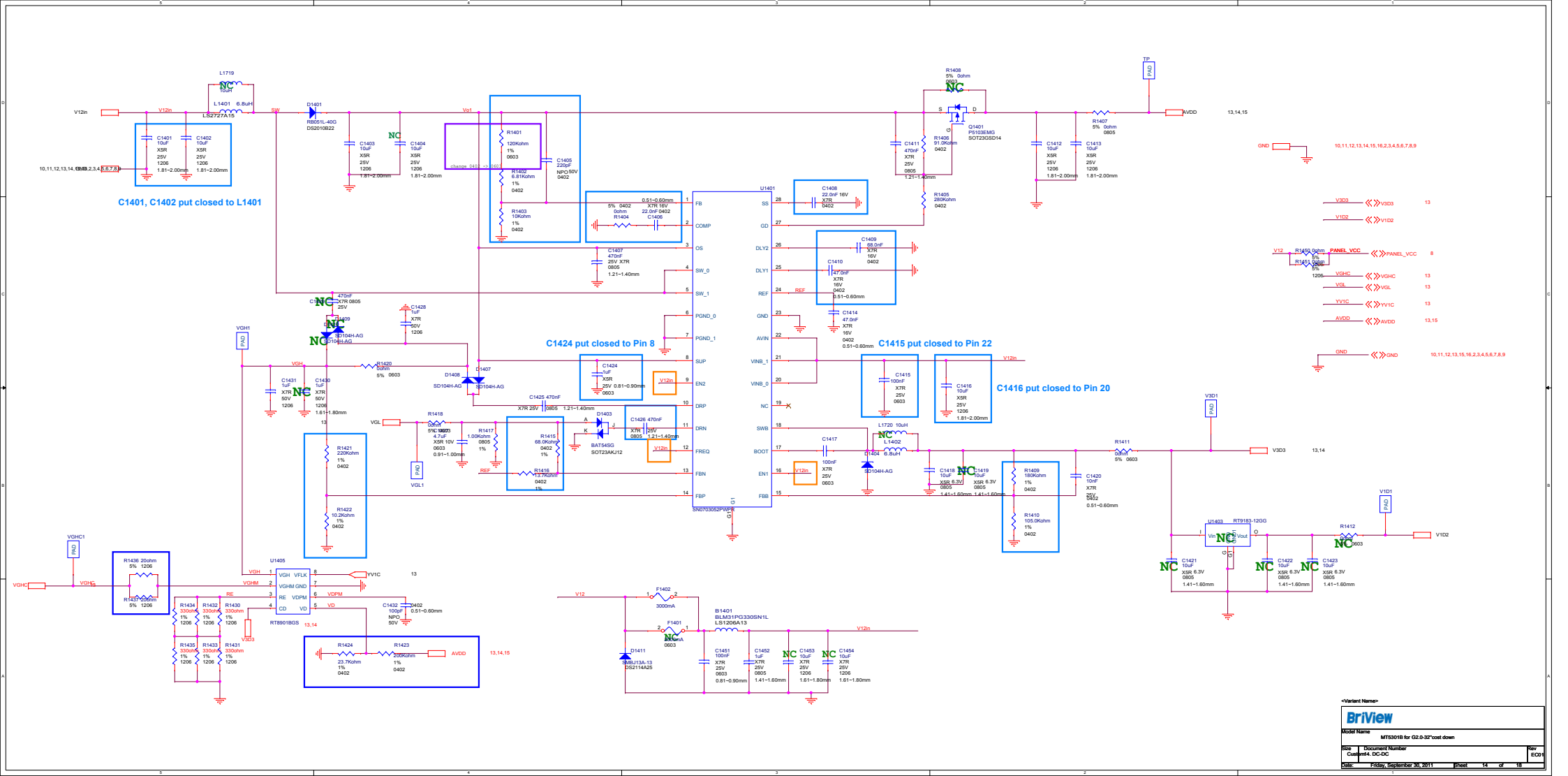
T315XF03 V0 Interface Connection

24PHD22HD 58 58 PFC pin assignment			
1	GND	31	VGMA5
2	BLVP0	32	VGMA4
3	FLVN0	33	VGMA3
4	BLVP1	34	VGMA2
5	FLVN1	35	VGMA1
6	BLVP2	36	NC
7	BLVN2	37	AVDD
8	GND	38	AVDD
9	BLVCKP	39	AVDD
10	BLVCKIN	40	NC
11	GND	41	GND
12	FLVP0	42	GND
13	FLVN0	43	XPOL
14	FLVP1	44	XSTB1
15	FLVN1	45	NC
16	FLVP2	46	VGHC
17	FLVN2	47	VGDM
18	GND	48	NC
19	FLVCKP	49	VGHC
20	FLVCKIN	50	VGHC
21	GND	51	NC
22	VGMA14	52	VGL
23	VGMA13	53	NC
24	VGMA12	54	VGC
25	VGMA11	55	VGC
26	VGMA10	56	NC
27	VGMA9	57	GND
28	VGMA8	58	YDIO1
29	VGMA7	59	YCLK
30	VGMA6	60	YOE

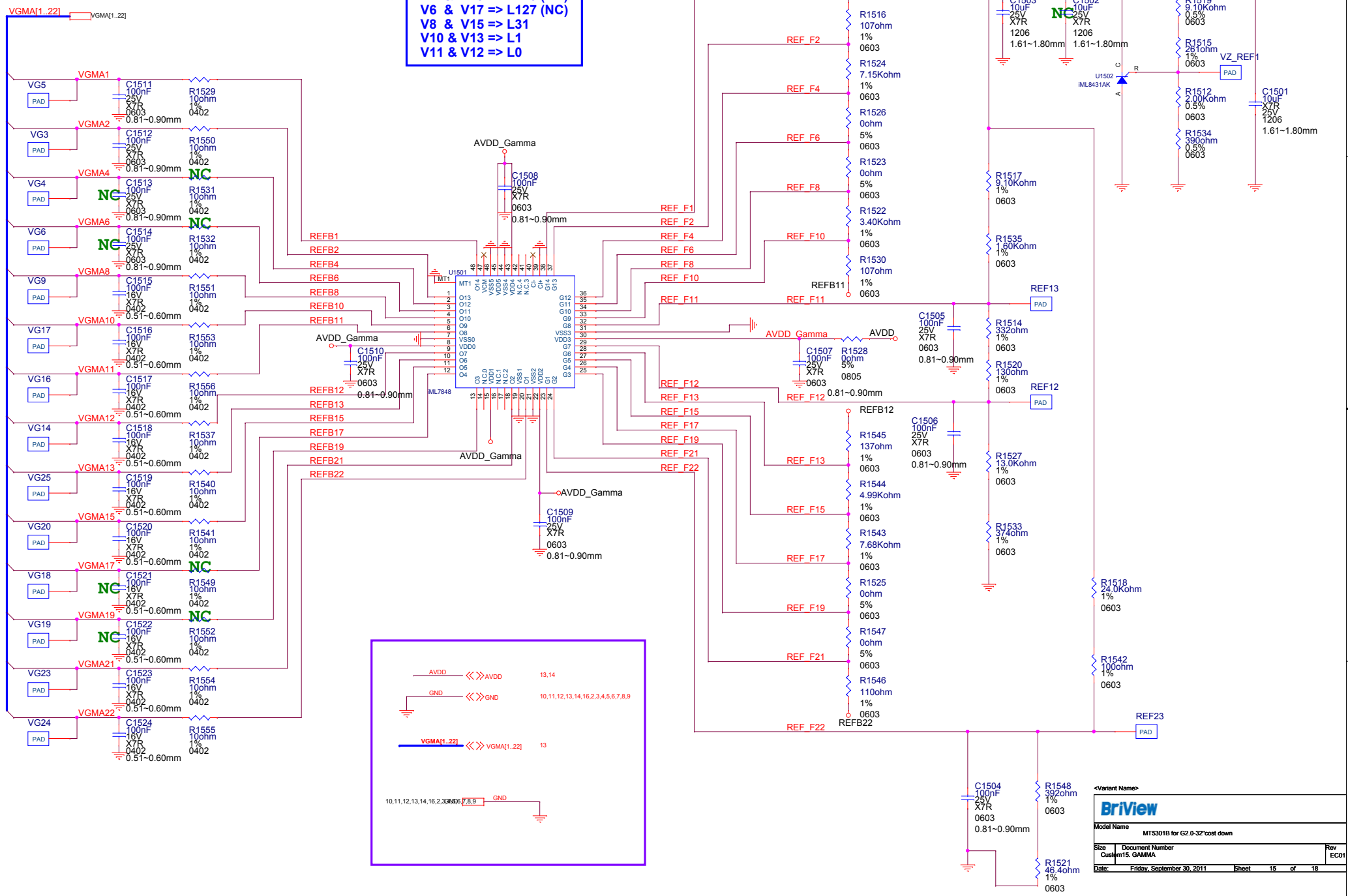


BLVCKIP	<<>>	BLVCKIP	8
BLVCKIN	<<>>	BLVCKIN	8
FLVCKIP	<<>>	FLVCKIP	8
FLVCKIN	<<>>	FLVCKIN	8
BLVP[0..2]	<<>>	BLVP[0..2]	8
BLVN[0..2]	<<>>	BLVN[0..2]	8
FLVP[0..2]	<<>>	FLVP[0..2]	8
FLVN[0..2]	<<>>	FLVN[0..2]	8
VGMA[1..22]	<<>>	VGMA[1..22]	15
AVDD	<<>>	AVDD	14,15
GND	<<>>	GND	10,11,12,14,15,16,2,3,4,5,6,7,8,9
V3D3	<<>>	V3D3	14
VGHC	<<>>	VGHC	14
VGL	<<>>	VGL	14
YVIC	<<>>	YVIC	14
GOE_A	<<>>	GOE_A	9
POL_A	<<>>	POL_A	9
GSC_A	<<>>	GSC_A	9
FLK_A	<<>>	FLK_A	9
GSP_R_A	<<>>	GSP_R_A	9
SOE_A	<<>>	SOE_A	9

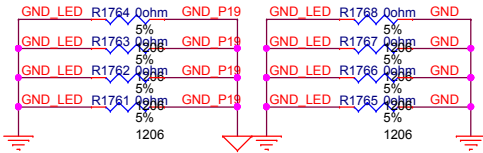
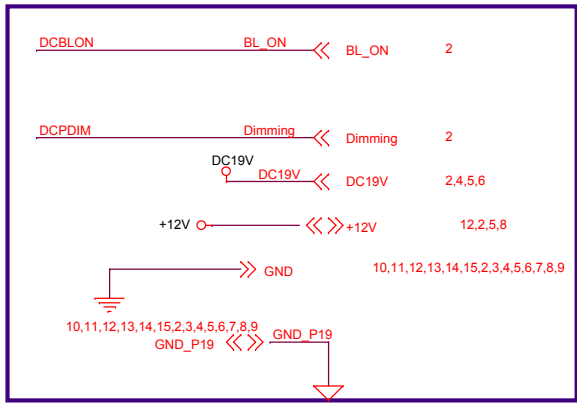
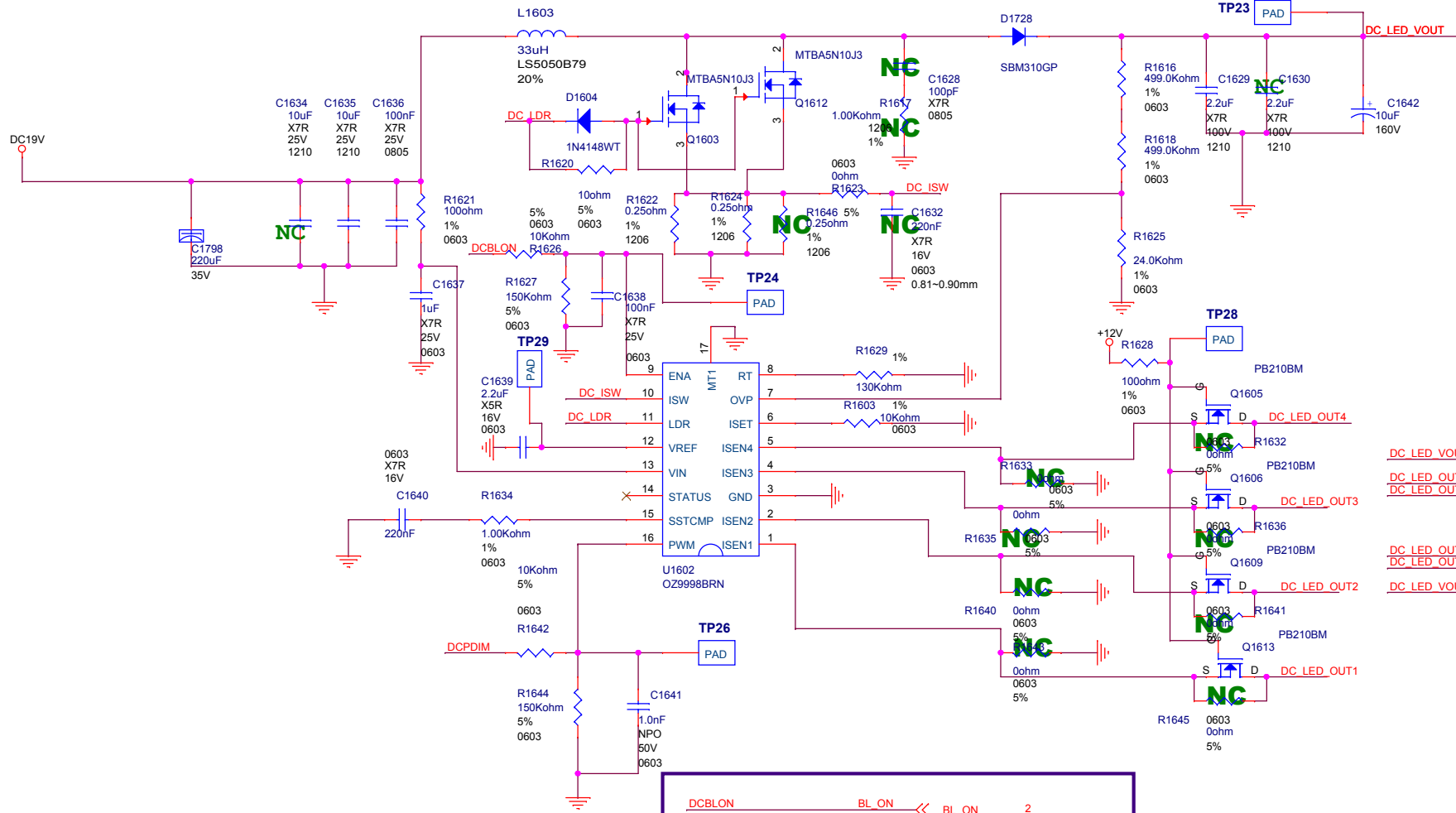




V1 & V22 => L255
V2 & V21 => L254
V4 & V19 => L223 (NC)
V6 & V17 => L127 (NC)
V8 & V15 => L31
V10 & V13 => L1
V11 & V12 => L0



BriView			
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MT5301B for G2.0-32'cost down			
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<Variant Name>

BrView

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MT5301B for G2.0-32"cost down

Size
B Document Number
16_LED Driver

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EC01

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20100714

- 1.change R298 from 12.4 to 7.5K; change R755 from 2.74 to 1.69K
- 2.NC D1
- 3.add R192, R257, R225, R258, R255-->0ohm
- 4.add RD52, RD53==> 0ohm
- 5.Change R17 From 20K to 7.5K
- 6.NC C2, R2; change R1 from 1K to 4.7Kohm; change R3 from 10K to 0ohm
7. R26 NC,R28改为0ohm, 删除C13
- 8.用OPCTRL2 (pin132)代替pin217 pin217 add TP point TP59
- 9.R2807由NC改为上件
- 10.Q20/Q21,C191,C194,R197,R198 NC; C192修改为82PF,C193修改为47PF; R64 修改为 6.8K,R207,R214上件OR
- 11.R206 改成1.5K ohm, L12 改成100uH, ; 这样30V带载能力会更稳定。C196 请用4.7uF X5R 电, ; 滤除Tuner5V 上的PWM noise
- 12.新增RD50,RD51==> 0ohm。其中RD51 NC
- 13.Change R155 from 20K to 150K; change C159 from 100nf to 0.47uF; add C932 220nf(NC预留用)
- 14.修改C88为10uF
- 15.change R749,R750from 10K to 47K
- 16.add TP15,TP16,TP17,TP18,TP19,TP20,TP25
- 17.add C174 100uf,C175 100uf
- 18.SQ42 AC ON/OFF模块加入 Add Q35,Q36,Q37,Q38,R168,R330,R331,R329,R327,R328,R325,R326,C99,D78,D79,L15
- 19.add RD56; NC R2796,R230,Q25
- 20.NC page 13,14,15

2010/8/2

1. delete T-con schematics page 13~15
- 2010/8/5
2. add 0 ohm for GND and tuner GND RS13~RS20 & RS21~RS28
3. add R259 between C201 and D38 for BT_30
4. RNF6 pin4 & pin5 connect to GND
5. Add R2807 for reset circuit
6. Add ESD protection D15 for key reset
7. change C61 from 100uF to 220uF (09.227E6.H01)

2010/8/6

1. U12 Vin & GND connect to GND, Vout connect to tuner GND
2. BT_30V: before C201 is GND, after D38 is tuner GND
3. Add RS29~RS32 (1206 package) to connect GND & GND; R48, R49, R133 (0805 package) to connect GND & GND
4. modify Q18 power to USB_VCC1; Q29 power to USB_VCC2

2010/8/10

1. Add C933 & C934 for+12V; C935~C937 for 5V_SW ; C938, C939 for DVDD3V3
2. del R48, R49, R133
3. change amp GND to normal GND
4. add C940 & C941 for Vcck

2010/8/11

1. add C13 for Vcck; C176 for +12V (12V->Vcck)
2. add C177 & C178 for 5V_SW
3. change R168 net to RESET_IN that connect to Q6 C
4. Add RS33~RS37 to connect GND and GND
5. add C942 for DVDD3V3

2010/8/12

1. Add R2808 & R2809 reserved for U7 pin 4 & pin11
2. R2799 NC;
3. Add D16 reserved for J6 pin 12 ESD protection
4. Add C943 reserved for keypad 5Vsb
5. Del C940, C65, R48, R49, R133, RS31, RS33

2010/8/13

1. Add C944 reserved for PANEL_VCC

2010/09/20

- 1.R36由2.00K/0402/ 1%更改为2.61K/0402/1%
- 2.R17由7.5k/0402/5%更改为2.2k/0402/5%
- 3.R259 0欧/0603 更换为 L16 FCI1608F-1R8K LS0603A10磁珠; C201由330P/0603更改为1UF/50V/0805
- 4.增加C65 100UF/25V, CB1位置调整到靠近U12前
- 5.R255由0欧/0805更改FB8 HCB2012KF-221T30/0805
- 6.C413, C414由10uf/0805更改为1uf/0805
- 7.c73由NC改为上件
- 8.AVDD10 LDO(pin148) 增加1kohm/0603电阻上拉到3V3SB
- 9.VGA ddC电路,在VGASCL和VGASDA电路上串联R2811100OHM/0603与R2812/100OHM/0603, 并上拉10KOHM
- 10.R409由0ohm/0805改为1kohm/0805

2010/10/11

1. Change D-sub location to J11
2. Change AMP P/N to 05.82581.DQ1

2010/10/26

1. change HDMI_SDA & HDMI_SCL net name
2. change keypad I2C pull-high voltage to 3V3SB
2. remove RS13~RS20 form NC parts

<Variant Name>

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Verify History

2011.2.11

- 1.Add TCON function for 42" panel
- 2.Change PG to IML AUO G1422.2H
- 3.Add driver BD circuit
- 4.Change DDR to Hynix 1066MHz
- 5.Reserve common use 3.3V for source and main BD
- 6.Add PG I2C control from D_sub connector
- 7.Reserve by pass resistor from 5VSB to 3.3VSB
- 8.JTAG replaced by TP, pls group layout
- 9.Change Mini-LVDS pin define for smoothly layout

2011.2.17

- 1.Delete Adapter to 12V(Page16), Adapter to 5V(Page17), LED Driver(Page18)
- 2.Modify H1,H2,H3,H4,H5 (screw 4.0mm to 4.3mm), Delete H6 (5.0mm)

2011.4.15

- 1.Change keypad / IR circuit
- 2.Change R755,R760 to 10K,R72 to330

<Variant Name>

BriView

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MT5301B for G2.0-32"

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A

Document Number
18. Note TW

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