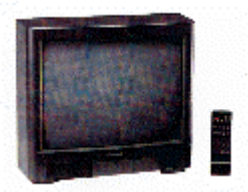
DAEWOO ELECTRONICS

SERVICE MANUAL
CHASSIS: CP-315

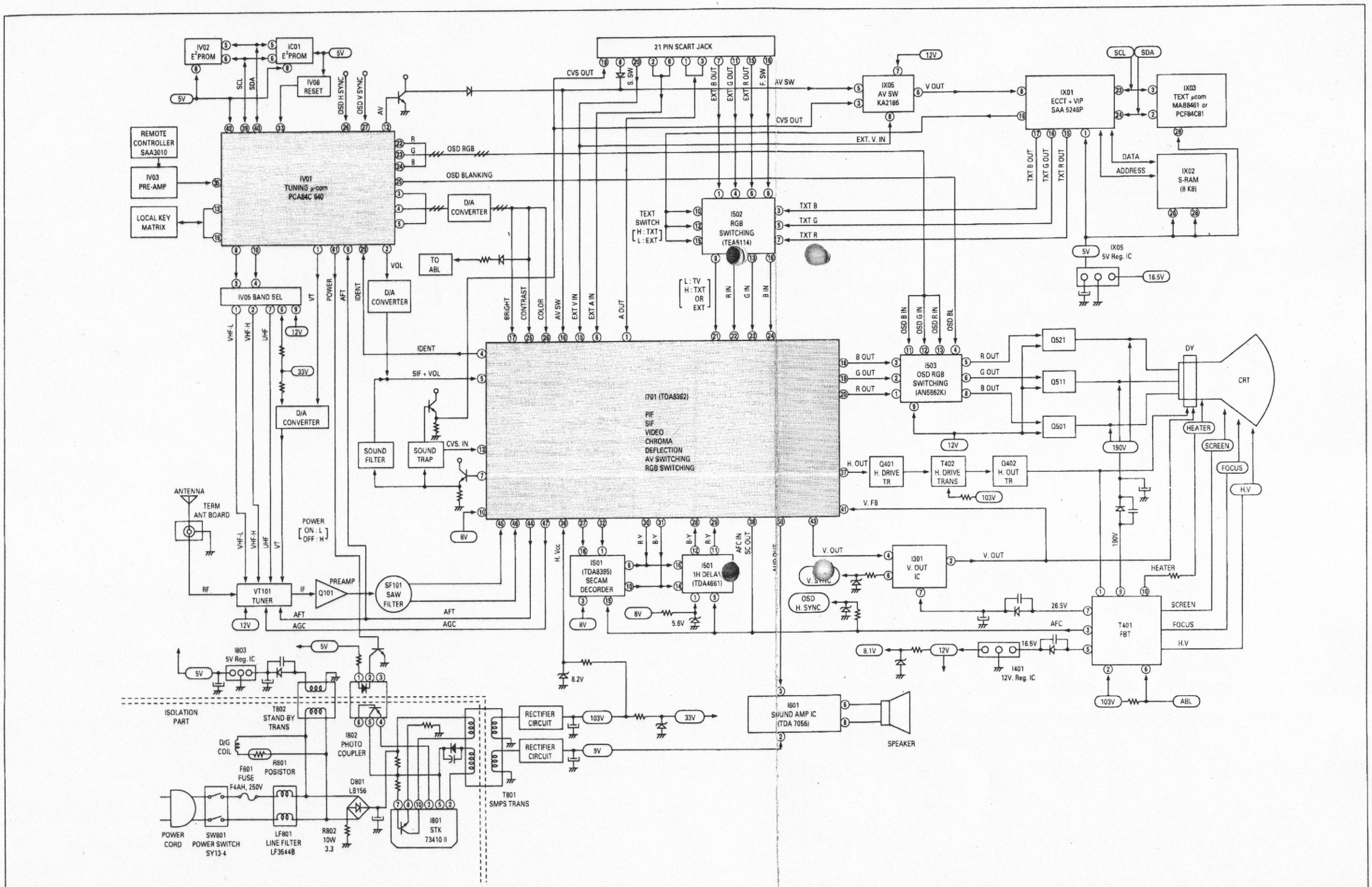
Model: DTD-1457TFP



1. Main Feature

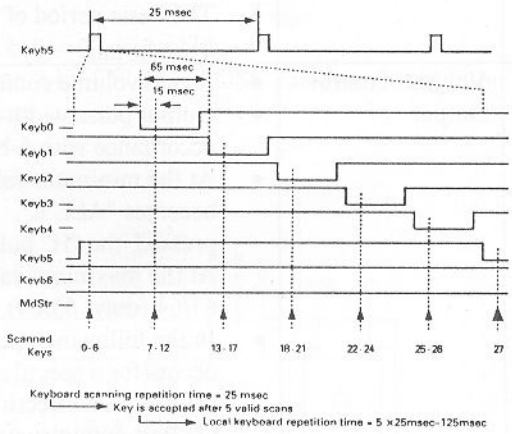
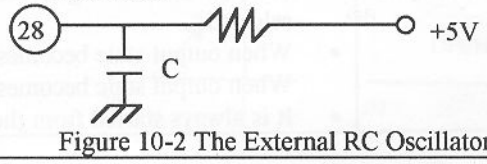
Model	TFB/TFF	TK	TS	TU
Receiving System	PAL/SECAM-B/G	P/S-B/G,D/K	PAL-B/G	PAL-I
Main Voltage	230V AC 50Hz			
Power Consumption	69W Approx. (14 inch) 85W Approx. (20 inch and 21 inch)			
Sound Output	2.0W Approx. (at 60% MOD. 10% THD)			
Antenna Impedance	75 ohm unbalanced 300 ohm balanced with supplied balun			
Tuning System	Voltage Synthesis Tuning System			
Number of Program	90 Programs			
Reception Channel	Refer to the TUNER description			
Remote Control Unit	Type R-10W			
Screen Size (Diagonal)	14" : 340mm 20" : 480mm 21" : 510mm (FST)			
Teletext System	4 page memory FASTEXT (FLOF & LIST)			
Indication	On-Screen Display -Program No. -Tuning Voltage -Picture Control (Contrast, Brightness. Color) -Volume Control -Mute State -Sleep Timer -AV			

2. Block Diagram



3-1-4. Pin Description

<table>
<tr><th>Pin</th><th>Symbol</th><th>Name</th><th>Description</th><th>DC</th></tr>
<tr><td>1</td><td>VT</td><td>Tuning Voltage Control Output</td><td>• The VT output is the Pulse Width Modulated output of a 14 bit digital to analog converter which is split-up in 7 bits for coarse adjustment and another 7 bits for fine adjustment.
• The basic period of the tuning output signal is $2^{14} \times f_{x\text{-}tal}/3=4915.2\mu sec$ ($f_{x\text{-}tal}=10MHz$).</td><td>-</td></tr>
<tr><td>2</td><td>VOL</td><td>Volume Control Output</td><td>• Sound volume control output terminal.
• Output pulse width modulated wave form in 64 levels in accordance with 6-bit latch data (active "H").
• At the minimum value of VOL, the output wave form becomes "ALL L". After that, whenever the VOL(+) key is pressed, the "H" pulse is increased by 1.
At the maximum value of VOL, the period of "H" becomes 63/64 (duty: 63/64).
• In the following operations, the mute state (minimum value) occurs for a specific time.
(1) Program selecting operation.
(2) Port output switching.
• Using the mute key operation, the sound volume output state and mute state can be switched.</td><td>-</td></tr>
<tr><td>3</td><td>BRI</td><td>Brightness Control Output</td><td rowspan="3">• Outputs the pulse width modulated signal in 64 levels in accordance with 6-bit latch data (active "H").</td><td>-</td></tr>
<tr><td>4</td><td>COL</td><td>Color Control Output</td><td>-</td></tr>
<tr><td>5</td><td>CON</td><td>Contrast Control Output</td><td>-</td></tr>
<tr><td>6</td><td>BAL</td><td>Balance Control Output</td><td>• Not used.</td><td>0</td></tr>
<tr><td>7
8
10</td><td>BL
BH
BU</td><td>Band Control Output</td><td>• There are control band signal output terminal for a tuner.
• Assignment for bands is as follows:
<table><tr><td>Band</td><td>BL</td><td>BH</td><td>BU</td></tr><tr><td>VHF-L</td><td>H</td><td>L</td><td>L</td></tr><tr><td>VHF-H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>UHF</td><td>L</td><td>L</td><td>H</td></tr></table></td><td>-
-
-</td></tr>
<tr><td>9</td><td>AFC</td><td>Comparison Voltage Input</td><td>• Comparison voltage input terminal connected to built-in comparator.
• Input AFC Signal from TV with level conversion (0 to Vdd).
• The results of the comparison are used when the auto search and digital AFT (described later) works.</td><td>2.4</td></tr>
<tr><td>11</td><td>VTR</td><td>VTR timer Constant Control Output</td><td>• This pin controls the VTR time constant of the first PLL in the horizontal synchronizing circuit of the TV receiver.
• This chassis is connected to GND.</td><td>4.1</td></tr>
<tr><td>12</td><td>AV</td><td>TV/VIDEO Selection Output</td><td>• Output pin AV defines whether internal audio/video signals (TV) or external signal from peripheral TV connector are selected.
• When output state becomes "H", TV mode is set.
When output state becomes "L", AV mode is set.
• It is always started from the TV mode.</td><td>5</td></tr>
</table>

Pin	Symbol	Name	Description	DC
13 14 15 16 17 18 19	P00-P06	Local Keyboard Control	• Input and output pins P00 ~ P06 are used to scan to local keyboard matrix. • The keyboard is scanned every 25msec; for timing see as follows.  • If a keypress is detected for 5 periods, it is recognized as a valid key command. • The repetition of the local keyboard is 125msec, which is almost equal to the repetition time of the remote control unit.	5 5 5 5 0 0 5
20	MDSTR	System Mode Strobe Output	• This pin is used to scan the various system options. • An active low signal is generated at the first switch-on ("Cold Start"). • Local keyboard control inputs P00 to P06 are read first; all keys on the local keyboard must be released, otherwise it will wait until they are released. • The pins that have a diode connected to MDSTR are read back as 0, the pins that do not have such diode connection are read back as a logic 1.	5
21	GND	GND Terminal	• This is connected to 0V power supply.	0
22 23 24 25	R G B BLANK	R.G.B Output Blank Output	• Outputs R.G and B deliver the color components for the OSD while output BK is used as a fast blanking signal. • The output polarity of the R.G.B and BK terminals are active "H".	0 0 0 0
26	H.SYNC	Horizontal Synchronous Signal Input	• Input terminal for CRT display horizontal synchronous signal. • Input rectangular pulses whose amplitude is in the range from 0 to 5V. • The input polarity is active "H".	0.4
27	V.SYNC	Vertical Synchronous Signal Input	• Input terminal for CRT Display vertical synchronous signal. • Input rectangular pulses whose amplitude is in the range from 0 to 5V. • The signal state should be active for the time more than that required for three scanning lines. • The input polarity is active "H".	0.2
28	DOSC	OSD Oscillator Input	• Input DOSC has to be connected to an external RC network which controls the oscillation frequency of the internal OSD oscillator.  Figure 10-2 The External RC Oscillator	5

Pin	Symbol	Name	Description	DC
29	IDENT	Video Recognition Input Signal	• Input terminal of image synchronous signal is necessary for auto search and AFT operation. • In case of the determination of the level signal synchronization, the signal state ("H" or "L") which is input at this terminal is determined in every 4ms. "H"----------Presence of synchronization "L" ----------Absence of synchronization	5
30	TEST	Test Input	• Test Input has to be connected to GND.	0
31 32	XTAL 1 XTAL 2	Micro controller Oscillator Control	• The XTAL 1 and XTAL 2 are used to control the on-chip oscillator of the μ-controller. • XTAL 1 is the input terminal and XTAL 2 is the output terminal. • All internal timing of the μ-controller (except for the OSD part) is derived from this oscillator. • The oscillator frequency has to be 10MHz.	2.3 2.3
33	RESET	Reset Input/Output	• This pin is used to reset the μ-controller after a power-on reset. In order to make sure that the μ-controller starts from an initialized state after the supply voltage is available, a reset signal has to be applied. This reset signal has to be low until a stable 5V supply voltage is available.	5
34	SNDI	Sound Mode Input	• This pin is used to define whether the system is decoding a dual language transmission or a mono/stereo transmission. H: Dual Language L: Mono/Stereo	0
35	IR	Remote Control Signal Input	• Remote control signal input terminal.	3.2
36	SNDO	Sound Mode Select Input	• This pin is used to define what kind of sound system is controlled. • The selection of spatial and pseudo stereo sound effect is only possible in a full stereo system.	0
37	EFFECT	Pseudo/Spatial Stereo Control Output	• This pin is used to control the spatial, pseudo stereo or only other sound effect in a stereo sound. • After power-on reset of the μ-controller, pin EFFECT is tested to define whether the fifth analog control DAC is to be used or not.	0
38	SYSTEM	System Standard Control Output	• This pin is used to control the sound and IF part for two different TV transmission standard.	0
39 40	SCL SDA	I^2C-bus Control Input/Output	• Pins SCL and SDA are respectively the data and clock wire of the multi-master two-wire bidirection I^2C control bus. • If a transmission does not succeed, the controller will retry it for up to 5 times. If the bus is occupied for longer than 1.18 seconds, the μ-controller will generate bursts of nine clock pulses with intervals of 1.18 seconds until bus is free again.	3 3
41	POWER	STAND BY ON/OFF Control	• The switch-mode power supply is controlled. "L"---------- Power ON "H"----------Power OFF	0
42	Vcc	Power Supply Terminal	• Connected to the 5V power supply.	5

3-2-4. Pin Description

<table>
<tr><th>Pin.</th><th>Name</th><th>Description</th><th>DC</th></tr>
<tr><td>1</td><td>Audio De-emphasis</td><td>On this pin, the audio signal is available for scart. The signal having an amplitude of 350mVrms (at δf=50kHz) is non volume controlled and has to be buffered. (notice the output impedance influences the de- emphasis). For scart requirements, the buffer should be dimensioned as an amplifier in order to increase the output signal.
A third function of this pin is the positive modulation switch. When the voltage at this pin is above Vcc-1V, the positive modulation is selected. The required current is 100μA typical.</td><td>3</td></tr>
<tr><td>2,3</td><td>IF Demodulator Tuned Circuit</td><td>Because the demodulator performance depends on the Q factor, we want to keep the Q factor as high as possible. But this means that the steepness of the AFC will change with the Q factor of the tuned circuit itself and also with the impedance of the IC. A compromise has to be made. The input impedance of the IC has to be as large as possible (about 12 kOhms) and the Q factor of normal tuned circuits is varied from 70 to 90. By means of an external resistor, it is possible to damp the circuit to Q of 40 to reduce the steepness variation of the AFC.</td><td>5.9
5.9</td></tr>
<tr><td>4</td><td>Video Identification Output</td><td>The identification output has a three level output, 0.5, 6 or 8V.
<table><tr><td>Output voltage "video not identified"</td><td>0.5V max</td></tr><tr><td>Output voltage "video identified" and Colour signal available with fsc=3.5 MHz</td><td>6V</td></tr><tr><td>Output voltage "video identified" and Colour signal available with fsc=4.4 MHz or no Colour signal detected</td><td>8V</td></tr></table>The maximum load current on this pin is 25μA.
The output impedance is 20KΩ.</td><td>6.7</td></tr>
<tr><td>5</td><td>SIF input+ Volume control</td><td>The sound input impedance is 8k5Ω/5pF, which has to be taken into account for the ceramic filters. The impedance for DC is very high. The PLL is sensitive for high freq. AC signal>1mVrms. Because of the chosen principle: an adjustment free PLL, it is needed to have an internal PLL with a large bandwidth (catching range). This implies the system is also sensitive for suprious frequencies. Both layout and sound band pass filters need special attention.
The volume can be controlled on this pin by means of a DC voltage of 0.2-5V for min-max gain.</td><td>4</td></tr>
<tr><td>6</td><td>External Audio Input</td><td>External sound signals for example from scart can be applied to this pin via a capacitor. The input impedance is 25kΩ.</td><td>3.9</td></tr>
<tr><td>7</td><td>IF Video Output</td><td>A multistandard concept requires several filters at the video output (sound-trap and sound-bandpass filters). This causes a too big capacitive load at the video output so an emitter follower as buffer should be added.
The required emitter current depends on the number of filters applied.</td><td>3.2</td></tr>
<tr><td>8</td><td>Decoupling digital Supply</td><td>Decoupling Digital Supply</td><td>1.7</td></tr>
<tr><td>9</td><td>Ground</td><td>Ground 1 (IF, H sync, RGB output, Digital, H output)</td><td>0</td></tr>
<tr><td>10</td><td>Positive Supply (8V)</td><td>Supply (IF, Sound, H sync, Chroma, Filters, RGB output, Digital)</td><td>8</td></tr>
<tr><td>11</td><td>Ground</td><td>Ground 2 (Sound, Chroma, Filters, Hosc, PHI-1, PHI-2)</td><td>0</td></tr>
</table>

<table>
<tr><th>Pin.</th><th>Name</th><th>Description</th><th>DC</th></tr>
<tr><td>12</td><td>Decoupling filter tuning</td><td>Variations in the tuning voltage outside of calibration (i.e. during field scan) due to external leakage current or interference sources, will result in mistuning of the luminance notch filter, chroma bandpass filter and luminance delay stage.
Unwanted voltage signals on Pin No.12 due to external leakage currents or crosstalk from interference sources should be less than 100mV. A capacitor of 100nF requires that external leakage currents on Pin No.12 should be less than 0.5μA.</td><td>3.1</td></tr>
<tr><td>13

15</td><td>Internal CVS input

External CVS Input</td><td>The internal and external CVBS amplitudes should be 2Vpk-pk and 1Vpk-pk respectively; their source impedance should be low so as to minimize crosstalk from interference sources. The internal CVBS input is derived from the IF video output (pin 7) and the external CVBS input can be derived from either SCART CVBS or YSVHS; they should be ac coupled to Pins No.13 and 15 respectively. The coupling capacitors are chosen in order to have fast clamping and minimum line/field sag.</td><td>4.4

3.5</td></tr>
<tr><td>14</td><td>Peaking control input</td><td>The input impedance of Pin No.14 is very high (MOS input). The DC voltage at the peaking control input controls the gain of the peaking amplifier. The peaking control input voltage should have DC voltage range from 0 to 5V.</td><td>3.7</td></tr>
<tr><td>16</td><td>AV switch input + Chroma (SVHS) input</td><td>The input impedance of chroma and A/V switch input (Pin No. 16) are 15kΩ in parallel with 5pF.
DC voltage on this pin controls the internal/external CVBS and AUDIO selection where the following table gives the various possibilities:
<table>
<tr><th>Vpin16 (dc)</th><th>Internal CVBS</th><th>External CVBS/Y</th><th>CSVHS signal</th><th>Luminance notch</th><th>Audio signal</th><th>Mode</th></tr>
<tr><td><0.5V</td><td>on</td><td>off</td><td>off</td><td>on</td><td>Internal</td><td>TV</td></tr>
<tr><td>Between 3V&5V</td><td>off</td><td>on</td><td>on</td><td>off</td><td>External</td><td>S VHS</td></tr>
<tr><td>>7.5V</td><td>off</td><td>on</td><td>off</td><td>on</td><td>External</td><td>AV</td></tr>
</table></td><td>0.3</td></tr>
<tr><td>17</td><td>Brightness Control input</td><td>The brightness control voltage presented to Pin No.17 controls the DC level of the RGB outputs. So this voltage of 0→5V at Pin No.17 results in a black level shift at the RGB outputs of □V about the nominal</td><td>3.7</td></tr>
<tr><td>18
19
20</td><td>B-output
G-output
R-output</td><td>The RGB output signals are supplied to the video output stages. For nominal input signals (i.e. CVBS and-(R-Y)/-(B/Y) signals) and for nominal gain settings the RGB output signal amplitudes (black-to-white) are typically 4V with a black level at approximately 1.3V.
The blanking level is 0.8V and maximum peak white level is 6.0V.
Since the RGB output stages are made with emitter followers, the maximum sink current is limited to 1.5mA. Therefore the current delivered from the video output stages to the RGB pins must not exceed 1.5mA.
When the RGB switch control (Pin No.21) voltage exceeds 4V, then the RGB outputs are blanked and consequently on-screen display signals (OSD) can be supplied to the video output stages.</td><td>2.3
2.3
2.3</td></tr>
<tr><td>21</td><td>RGB insertion + Blanking input</td><td>The RGB insertion signals are selected by means of a switch control.
With the conditions that:
0.3V< Vpin21 < 3V, then the RGB insertion signals are selected.
And input voltage to blank the RGB-outputs is 4.5V (min), so the OSD signals can be applied to these outputs .</td><td>0.2</td></tr>
</table>

Pin.	Name	Description	DC
22	R-input for insertion	The RGB insertion signal information is coupled via 100nF to Pins No.22, 23 and 24 respectively. The coupling/clamping capacitors should always have a low impedance path to ground for proper clamping operation.	3.3
23	G-input for insertion		3.3
24	B--input for insertion		3.3
25	Contrast Control Input	The contrast control input of 0→5V at Pin No.25 gives a 20dB gain range at the RGB outputs. When one of the RGB output signals exceed 6V, then it is clipped to 6V and also the gain of the RGB output amplifiers can be reduced by adapting the contrast voltage using the peak white limiter (PWL) current. The PWL current during PWL operation is 100μA.	2
26	Saturation Control Input	The saturation control input voltage presented to Pin No.26 is 0→5V. This corresponds to a 52dB gain range of the -(R-Y)/-(B-Y) signals.	2.7
27	Chroma output + Hue Control Input	If the Vpin27 > 6V, the ASM does not search for NTSC signals and the decoder application can only be PAL/SECAM. The output impedance with an external resistance of 22kΩ to 8V is approximately 500Ω. The hue control input pin should be provided with a voltage of 0 to 5V for NTSC decoder applications; within this voltage range the input impedance is very high (MOS input).	5.7
28	B-Y input	The -(R-Y)/-(B-Y) signals presented to Pins No.11 and 12 of the TDA4661 are coupled via 100nF (these capacitor are also clamping capacitors) to Pins No.29 and 28. The maximum input current of both pins is 1μA. With 100nF coupling capacitors, the voltage drop over a line period is less than 0.5mV. Since the output impedance of Pin No.11 and 12 of the TDA4661 is maximal 400Ω, then the signal tracks between the TDA4661 and the TDA8362 should have good ground shielding and be as short as possible.	3.9
29	R-Y input		3.9
30	R-Y output	The output impedance of Pins No.30&31 are approximately 250Ω when PAL/NTSC signals are identified. For SECAM signals the output impedance is very high (output switch is open) and any external circuitry is not loaded (i.e. the demodulator outputs of the TDA8395). During the line/field blanking periods of the sandcastle pulse, the demodulator outputs are set to the correct DC levels so as no offsets exist. The -(R-Y)/-(B-Y) outputs are coupled via 1nF to Pins No. 16&14 of the TDA4661 respectively.	1.5
31	B-Y output		1.5
32	4.43 MHz output for TDA8395	A SECAM reference signal (4.43 MHz only) is delivered directly from Pin No.32 of the TDA8362 to Pin No.1 of the TDA8395. When SECAM signals are identified by the TDA8395, it withdraws a current of 150μA from pin 32. The SECAM interface communicates the ident information via this current to the ASM. If PAL/NTSC signals are not already identified by the ASM and the identified signal is 50 Hz, then an acknowledge will be given by the ASM to the TDA8395 by setting the voltage of Pin No.32 to 5V. With SECAM identified, the SECAM reference signal is gated and is presented to Pin No.32 only during the field retrace period. When PAL/NTSC is identified, the output level is 1.5V.	1.7

Pin.	Name	Description	DC
33	Loop Filter (Burst Phase Detector)	One of the important aspects of the PLL is the loop filter connected to Pin No.33. It ensures that the PLL synchronizes the VCXO, in both frequency and phase, with the incoming burst (average burst for PAL standards). It also determines the dynamic performance of the loop where the important parameters are: — Noise immunity — Transient response — Acquisition behavior The remaining aspects of the PLL/VCXO are static phase error and XTAL type used at Pin No.34 or 35. For small static phase errors (less than 5^{o}) the requirements are: — The combined burst phase detector and VCXO sensitivity is high — The offset of the burst phase detector output is small — The external leakage current of Pin No.33 is small The TDA8362 determines the first two; the third is determined by the external leakage resistance of Pin No.33 to ground. Deviations in the VCXO free running frequency due to XTAL or XTAL load capacitance spreads have negligible influence on the static phase error because the combined phase detector and VCXO sensitivity are high. The static phase error is due to the internal offset of the phase detector output and the external leakage current at Pin No.33. Static phase errors much less than 5^{o} are measured.	4.5
34 35	3.58MHz X-TAL Connection 4.43MHz X-TAL Connection	To ensure the correct operation of both color processing and sync calibration circuits in the TDA8362, then 4.43 XTAL must be connected to Pin No.34 and 3.58 XTAL must be connected to Pin No.35. Check if they get changed.	2.9 2.1
36	Start Horizontal Oscillator	The minimum current required for the start function is 6.5mA, then the voltage will be approx. > 7.2V. The voltage of Pin No.36 may not exceed 8.8V, so the dependence on the application external clamping is necessary. If the start voltage is below approximately 5.8V, then the horizontal output will be disabled. The decoupling should be sufficient because the start pin supplies the circuitry needed for the horizontal output. (The oscillator references, however, are supplied by the bandgap) This pin must be connected directly to the supply pin when no start function is used.	8.1
37	Horizontal Output	This open collector output drives the horizontal output stage. The maximum allowable current is 10mA. Then the saturation voltage will be 0.3V.	0.4
38	Flyback input + Sandcastle Output	A sandcastle signal is available at this pin for external use. The signal levels are: Burst typ 5.3V, the output impedance is approx. 1k2Ω Flyback typ 3V, impedance defines by the flyback circuit Field blanking typ 2V, the output impedance is approx. 4kΩ The flyback input signal is used for the PHI-2 loop and RGB line blanking. Pin No.38 requires a current of only a few μA in order to reach the 3V flyback clamping level. But detection of the flyback pulse (thus RGB blanking) only occurs when the current is at least 100μA. (The maximum allowable current is 300μA.) Additional remarks: — Due to an internal base current at Pin No.38, the voltage level becomes 3V when the pin is not loaded. — During start-up Pin No.38 is forced to be low by 2mA.	

Pin.	Name	Description	DC
39	ϕ-2 loop Filter + X-ray Protection	The phase error on screen due to storage time variations depends on the PHI-2 loopgain. In principle, this figure is fixed but will decrease when an additional resistor becomes in parallel with the capacitor of Pin No.39. The time constant is defined by the external capacitor. The voltage to switch on the X-ray protection is 6V. (min.)	3.4
40	ϕ-1 loop Filter	The PHI-1 behavior depends on both the loop filter externally connected to Pin No.40 and the PHI-1 output currents. The PHI-1 output current has been made switchable during scan (a fixed current ratio) in order to avoid the need of switching the loop filter for normal-and-noisy-signals. This implies the loop filter can be optimized for both VCR-and-noisy-signals.	3.8
41	Vertical Feedback Input	The feedback signal is derived by sensing the deflection coil current by means of a resistor. The feedback signal is related to the vertical ramp signal. The ramp amplitude should be 1Vpp while the DC level is 2.5V typical. The guard levels are 1 and 4Vtyp. In order to filter horizontal influences, a capacitor is mounted on the input.	2.2
42	Vertical Ramp Generator	The vertical ramp is defined as: — DC clamping voltage of 2V — AC amplitude of 1.5Vpp for a 50Hz field signal — AC amplitude of 1.25Vpp for a 60Hz field signal The AC amplitude of 1.5V is important for optimal pre-correction and 50/60Hz gain correction.	2.9
43	Vertical Output	The vertical drive output is fed to the deflection-IC. The available output current is minimal 1mA and the available output voltage is 4-5V. During retrace, the drive output has to be constant and equal to the low level of 0.3V	2.6
44	AFC Output	The AFC steepness can be influenced by the Q of the tuned circuit and output resistors at the AFC output pin (60kΩ output impedance internally). Due to current reserve, the steepness can be reduced by a factor 4-5 while the output voltage swing remains 6V. Some small video information can still be presented to the AFC output pin although S&H function is applied. This video information can be filtered by an external capacitor at this pin. The AFC output voltage changes from approximately 0.5-6.3V. The output impedance of AFC circuit is 50kΩ.	3.8
45 46	IF Input	DC coupling is allowed, so no series capacitors are necessary. The circuit matches the required load impedance for commonly used SAW filters(2k/3pF).	4 4
47	Tuner AGC Output	The tuner AGC is an open collector output which is acting as a variable current source to ground. Normally the output application circuit is designed for an output current swing 1-2mA. In order to improve the dynamic behavior during channel switching, it is possible to sink with a current of approximately 12mA maximal. The max voltage is Vcc + 1V.	4.5
48	AGC Decoupling Capacitor	Increasing of the AGC time constant is achieved by increasing the AGC capacitor on pin 48. Increasing this capacitor also results in an improvement in the catching and holding range of the ident circuit.	3.6

Pin.	Name	Description	DC
49	Tuner Take-Over Adjustment	The control range of this pin is 0.5-4.5V. Characteristic: The tuner take-over adjustment voltage versus IF input signal is a linear function with a slope of approximately 20mV/dB (Measured at an AGC output current of 1mA). In order to achieve a stable AGC control at strong signals, decoupling capacitor of at least 1nF on this pin is required. Alignment: With the potentiometer connected to Pin No.49 of the TDA8362, the tuner take-over point can be adjusted when RF signal is applied to the input of the tuner.	2
50	Audio Input	The DC output voltage is 3.3V. The volume controlled output signal is AC coupled to the sound output amplifier. The output impedance is 250Ω.	3.7
51	Decoupling Sound Demodulator	This pin defines the DC voltage at the de-emphasis and sound output. The pin forms a low pass filter in the DC feedback loop. This implies that the sound amplitude for lower frequencies, < fk is attenuated. A bigger capacitor, in order to decrease fk, is allowed but increases the DC setting time.	4.6
52	Decoupling Bandgap Supply	Decoupling Bandgap Supply	6.6

- Local Oscillator

  The function of the local oscillator is to generate unmodulated sine wave voltage, or CW output to beat with the RF signal in the mixer.
  For each station, the oscillator operates at only the one frequency needed to convert the RF picture and sounds to the intermediate frequencies of the receiver.

- AFT (Automatic Fine Tuning)

  The AFT circuit is actually automatic frequency control (AFC) on the local oscillator in the RF tuner.
  The tuning is generally needed when changing channels, especially with the remote control unit.
  The key to AFT operation is having the local oscillator in order to convert the picture carrier to exact IF frequency.

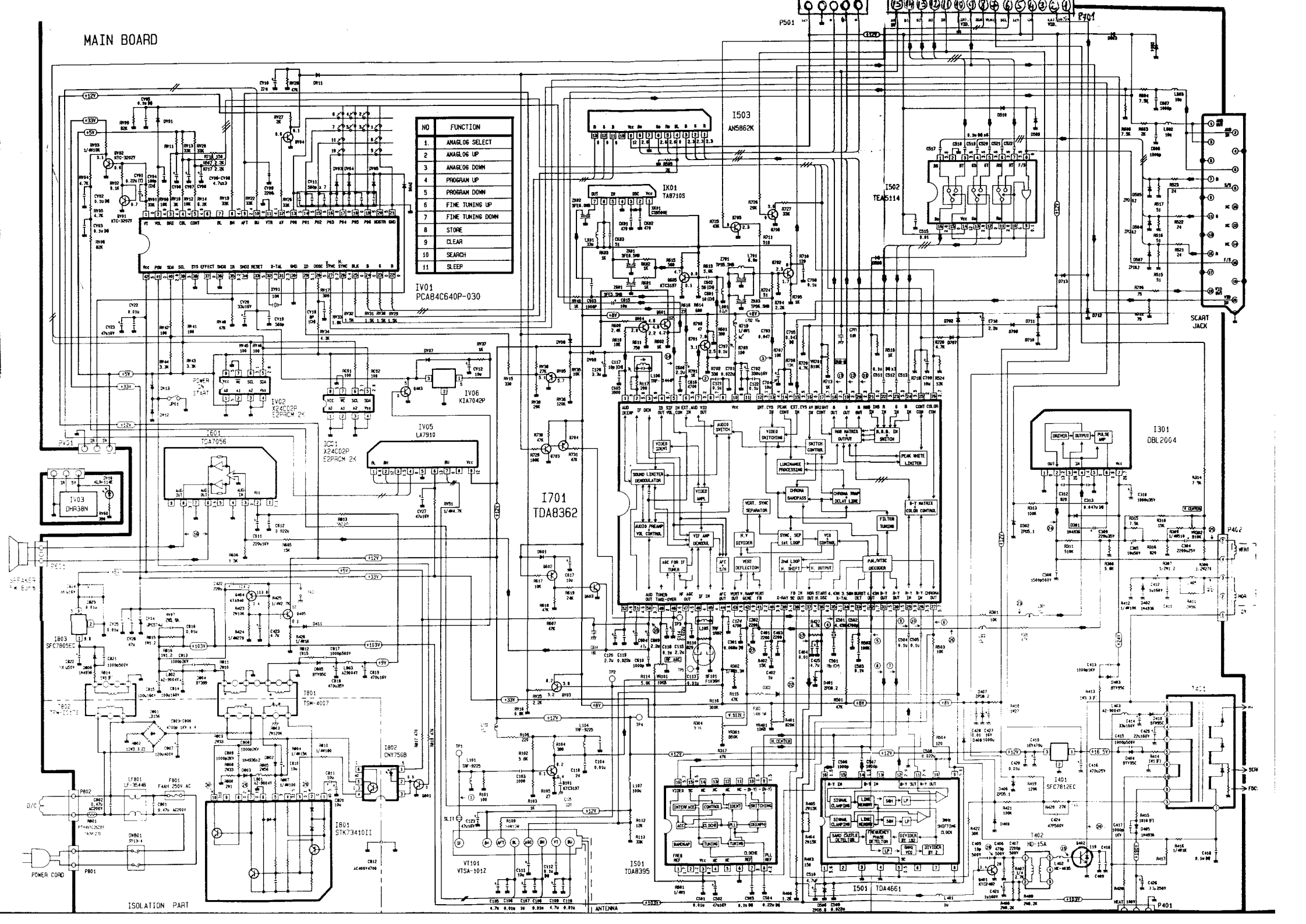
- AGC (Automatic Gain Control)

  The AGC circuit varies the gain of the receiver according to signal strength. Less gain is needed for strong signals. Therefore the AGC reduces the gain by changing the bias on the IF and RF stage to maintain a relating constant level for the video detector output.

3) Channel Coverage

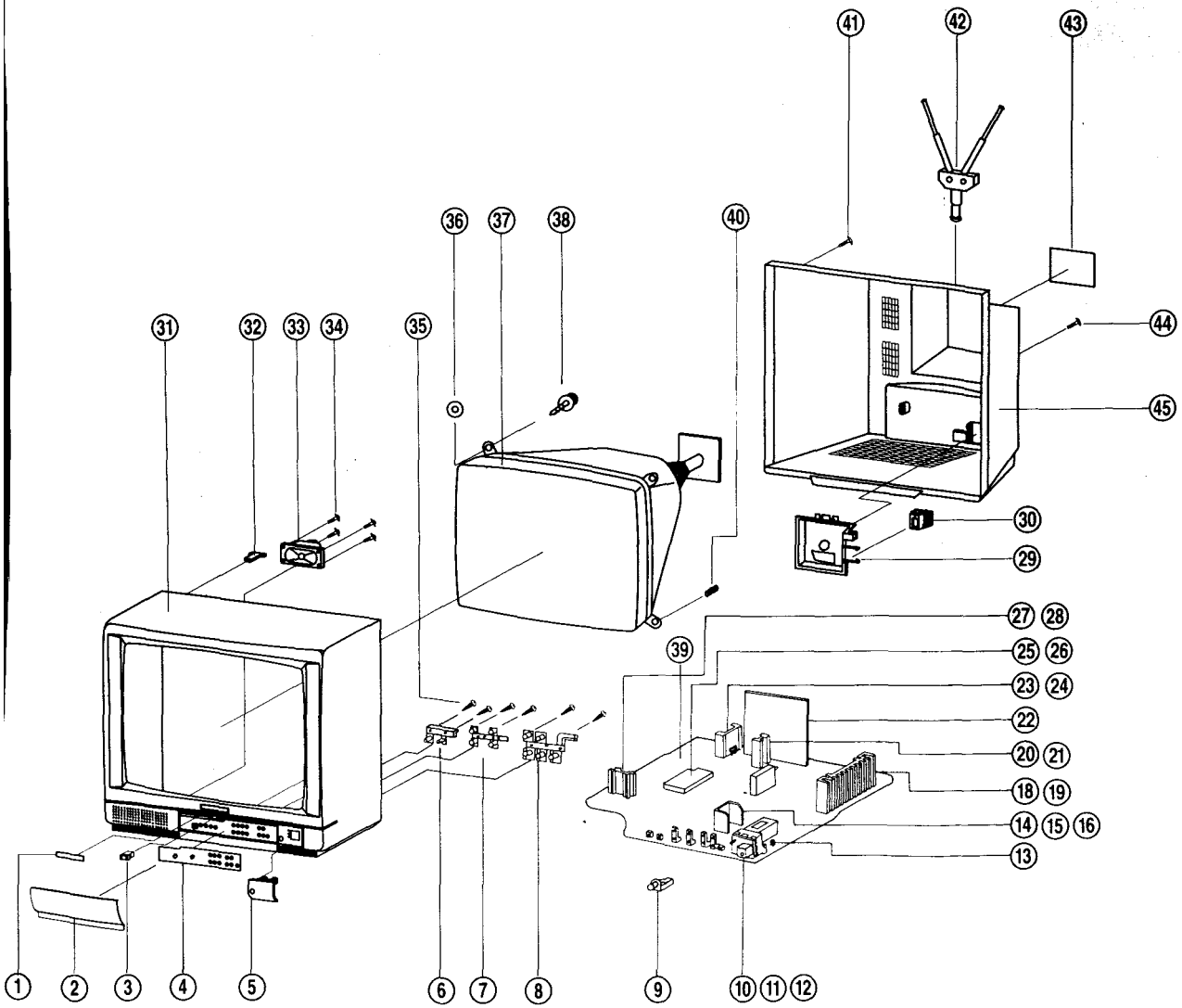
MODEL	TUNER	SYSTEM	BAND	CHANNEL	PIF
TFB/TFF TS	VTSS-7SZ3	B/G	VHF-L	CH 2 - CH 4 CH S1'- CH S3' CH S1 - CH S2	38.9MHz
			VHF-H	CH S3 - CH S10 CH 5 - CH 12 CH S11-CH S20	
			UHF	CH 21 - CH 69	
TK	VTSS-702Z (VTSA-101Z)	B/G	VHF-L VHF-H UHF	Same as Above	38.0MHz
		D/K	VHF-L	CH I - CH V	
			VHF-H	CH VI - CH XII	
			UHF	CH 21 - CH 69	
TU	DET-7BZ	I	UHF	CH 21 - CH 69	39.5MHz

MAIN BOARD



NO	FUNCTION
1.	ANAGLOG SELECT
2	ANAGLOG UP
3	ANAGLOG DOWN
4	PROGRAM UP
5	PROGRAM DOWN
6	FINE TUNING UP
7	FINE TUNING DOWN
8	STORE
9	CLEAR
10	SEARCH
11	SLEEP

■ DTD-1457TFB, TU



NO	PART CORD	PART NAME	Q'ty	DESCRIPTION	REMARK
1	4855613600	MARK BRAND	1	COPPER T0.4	
2	4852810001	DOOR	1	ABS BK	
3	4857923300	DOOR LOCK	1	LA701 (KIFCO)	
4	4855050217	DECO CTRL	1	PVC T0.2	
5	4855512911	DECO SENSOR	1	P.C SMOG SILK	
6	4854827703	BUTTON CONTROL	1	HG ABS BK	
7	4854916607	BUTTON	1	HG ABS BK	
8	4854813901	BUTTON PUSH	1	ABS BK	
9	4854831301	BUTTON	1	HG ABS BK	
10		PCB P-AMP	1		
11	97P2306800	LED HOLDER-A	3	PP BLK	
12	4853734900	RETA P-AMP	3	PP BLK	
13	4857415000	CLIP PUSE	2	BSP3 SN 5.2	
14	4857025400	HEAT SINK	1	A1050P-H24 T2.0	
15	4856012310	SCREW SPECIAL	1	PAN 3×10 MFZN	
16	4856215200	WASHER	1	SPCC	
17	7391300011	NUT HEX	1	6N-1-3 MFZN	
18	4857023304	HEAT SINK	1	AL EX	
19	7128301211	SCREW TAPPING	1	T2S WAS 3×12 MFZN	
20	4857024900	HEAT SINK	1	AL EX	
21	7121301011	SCREW TAPPING	1	T2S PAN 3×10 MFZN	
22	4859820223	PCB TEXT	1	T1.6×231×139/2	
23	4857024600	HEAT SINK	1	AL EX	
24	7121301011	SCREW TAPPING	1	T2S PAN 3×10 MFZN	
25	48572301011	SHIELD CASE	1	SPTH-C T0.3	
26	4857230700	SHIELD PLATE	1	SPTH-C T0.3	
27	4857024500	HET SINK	1	AL EX	
28	7121301011	SCREW TAPPING	1	T2S PAN 3×10 MFZN	
29	4853621601	TERMINAL ANT	1	HIPS BK	
30	4853514400	STOPPER CORD	1	P.P BLACK	
31	4852039901	MASK FRONT	1	HIPS BK TAINTING	
32	4853311601	RETAINER BACK	2	HIPS NC	
33		SPEAKER	1		
34	7128301011	SCREW TAPPING	4	T2S WAS 3×12 MFZN	
35	7128301211	SCREW TAPPING	6	T2S WAS 3×12 MFZN	
36	4856214900	WASHER RUBBER	4	RUBBER BK	
37		CRT	1		
38	4856212000	SCREW CRT FIX	4	SWRM+SK-5 (L=30)	
39		PCB MAIN AS	1		
40	4856716200	SPRING COIL	1	SUS	
41	7122401411	SCREW TAPPING	5	T2S TRS 4×14 MFZN	
42		ANT ROD	1		
43	4855415800	SPEC PLATE	1	150ART P/E FILM (C/TV)	
44	7122401411	SCREW TAPPING	2	T2S TRS 4×14 MFZN	
45	4852128921	COVER BACK	1	HIPS BK	