Rev. No

VENICE

CPU : DOTHAN
Chip Set : ALVISO (GMCH)
Remarks : 915GM

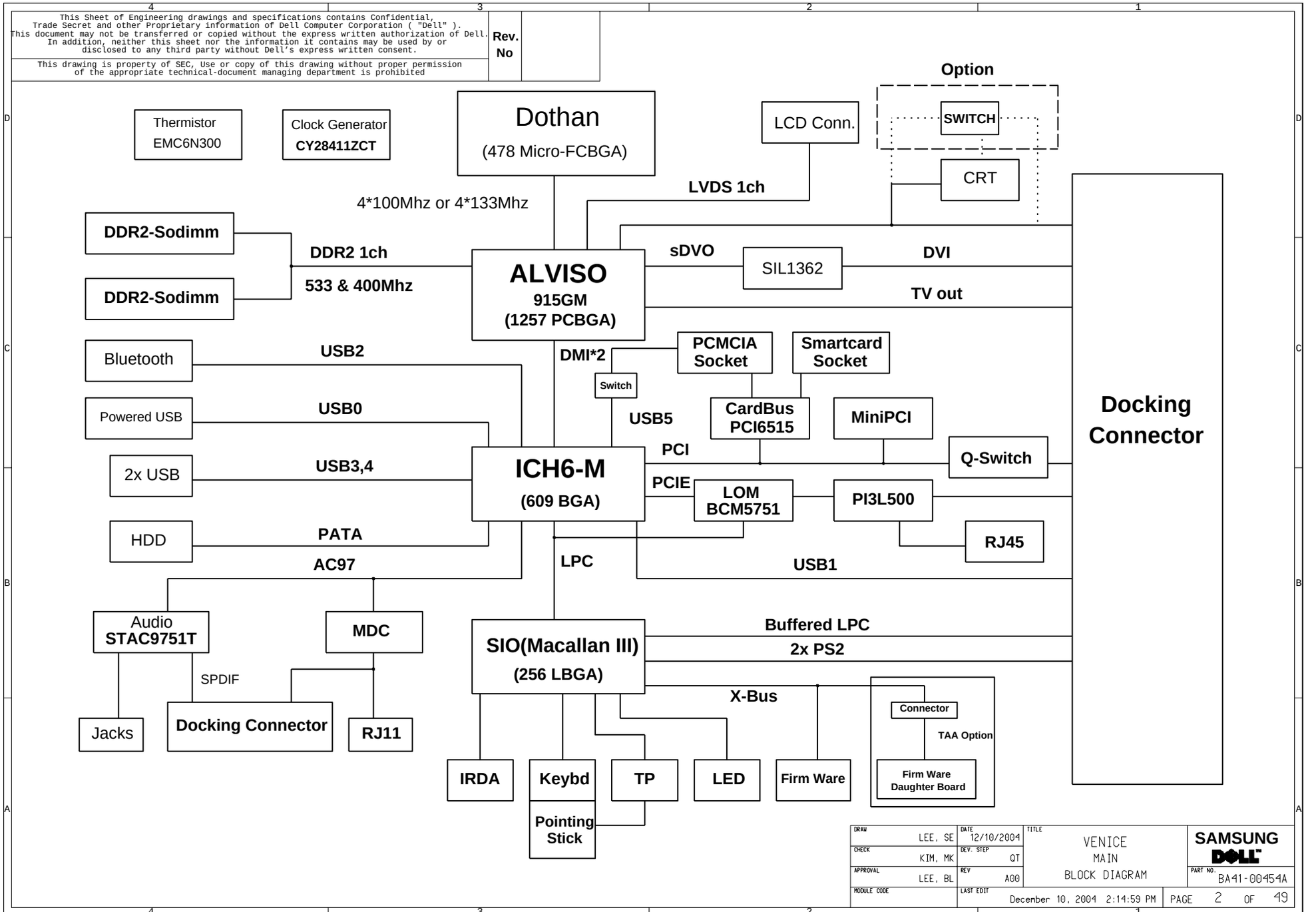
Model Name : VENICE Main
PCB Code : BA41-00454A
Dev. Step : QT
Revision : A00
Update : 2004.12.10

DRAW	CHECK	APPROVAL
SE LEE	MK KIM	BL LEE

Table of Contents

DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN COVER	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 1 OF 49	

Rev. No



DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN BLOCK DIAGRAM	SAMSUNG / DELL
CHECK: KIM, MK	DEV. STEP: QT		
APPROVAL: LEE, BL	REV: A00		PART NO.: BA41-00454A
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 2 OF 49	

Rev. No

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Docking	AD24	0	A
Cardbus	AD17	1	D,C
MiniPCI SLOT	AD19	3	B,D
USB	AD29(internal)	Programable	
Hub to PCI	AD30(internal)		
LPC bridge/IDE/AC97/SMBUS	AD31(internal)		
AGP	AD17(internal)		
Internal MAC	AD24(internal)		
AC Link	-		

I2 C / SMB Address

Devices	Address	Hex	Bus
ICH6	**Master**	**-**	**SMBUS Master**
CK-410M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 001X	A2h	-
SSCG	1101-010x	D4h	Spread spectrum Clock Generator
BCM	1100-100x	C8h	-
PWR USB	-	-	-
MAC III	**Master**	**-**	
On b'd Diagnostic	1010 001x	A2h	-
Inverter	0101 100x	58h	-
Battery	0001 011h	16h	-
Smart Charger	0001 001x	12h	-
THERMISTER	0101 111x	5Eh	-
GMCH	**Master**	**-**	**I2C Bus**
EDID	1010 000x	A0h	LCD information
DVI	0111 000x	70h	

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT (Left, Powered USB)
1	Docking
2	BLUETOOTH
3	SYSTEM PORT #1 (Rear)
4	SYSTEM PORT #2 (Rear)
5	Expresscard
6	RFU
7	RFU

Voltage Rails

VDC	Primary DC system power supply (9 to 21V)
P5V_ALW	5.0V LDO power rail for MAC III(off in S4-S5 without AC Adapter)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_LAN	3.3V power rail (off in S4-S5 without AC ADAPTER)
P2.5V_LAN	2.5V power rail (off in S4-S5 without AC adapter)
P1.2V_LAN	1.25V power rail (off in S4-S5 without AC adapter)
P3.3V_ALW	3.3V LDO power rail for MAC III(off in S4-S5 without AC Adapter
P1.8V_AUX	GMCH/DDR II Power Source(off in S4-S5)
VCC_CORE	Core voltage for DOTHAN CPU (0.74~1.30V)
VTT	GMCH core, CPU/GMCH FSB Termination.
P5V	5.0V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5) SIL1362(DVI)
P2.5V	2.5V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
MEM_0.9V	DDR2 Termination (off in S3-S5)

POWER

P5V_ALW P3.3V_ALW	P3.3V_LAN P2.5V_LAN P1.2V_LAN	P5V_AUX	P3.3V_AUX	P1.8V_AUX	P1.5V_AUX	MEM_VREF	P5V	P3.3V	P2.5V	P1.8V	P1.5V	MEM_0.9	VTT	VCC_CORE
MAC III ICH6-M Flash Memory Thermistor	BCM5751M LED	ICH6 USB STAC9751	ICH6 MINI-PCI THERMISTOR	G MCH SODIMM	ICH6	Memory	ICH4 PCI6515 MINI-PCI STAC9751 MDC MAC III HDD TOUCHPAD PCI BUFFER	ICH6 PCI6515 MINI-PCI STAC9751 SODIMM MAC III LED MDC HDD FIR CLOCK BLUETOOTH	GMCH ICH DVI	DVI	MGM ICH6	Memory	CPU GMCH	CPU

DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN BOARD INFORMATION	SAMSUNG / DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 3 OF 49	

Rev. No

2 Chips solution are propsed by ICS.

CY28411ZXCT : Lead free version

CK-410M
ICS954201
CY28411ZC

CPU FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

Bus Selection for CK-410M (133MHz)
FSB/FSC : by CPU/ MCH BSEL(Page 6)
FSA : P3.3V PU

U523
CY28411ZXCT

Trace Width *2

SMBUS Address "D2h"

Place 14.318MHz within 500mils of CK-410M

Place Termination close to CK-410M

SSCD
MK1493-05
CY25823ZC

U9
CY25823ZC

Place SSCG close to ALVISO. in order to minize the stub.

DRAW	LEE, SE	DATE	12/10/2004
CHECK	KIM, MK	DEV. STEP	QT
APPROVAL	LEE, BL	REV	A00
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM

TITLE: VENICE MAIN CLOCK GENERATOR

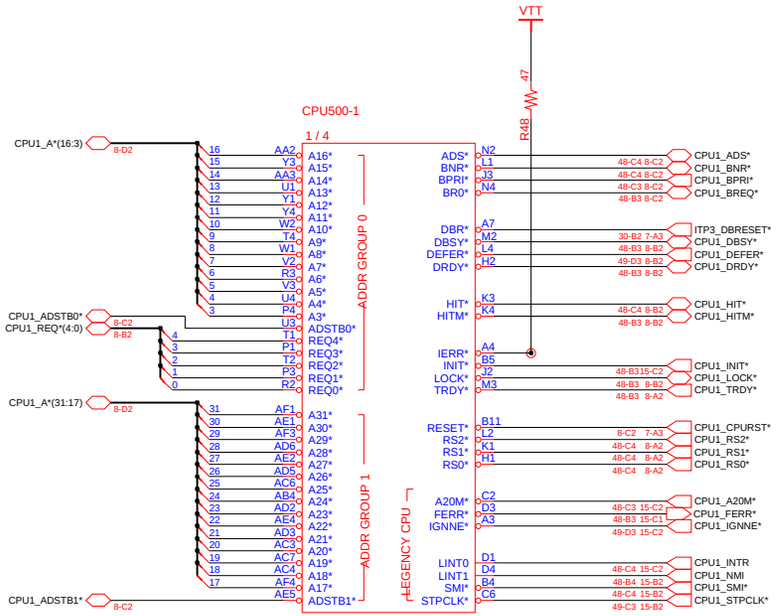
SAMSUNG DELL

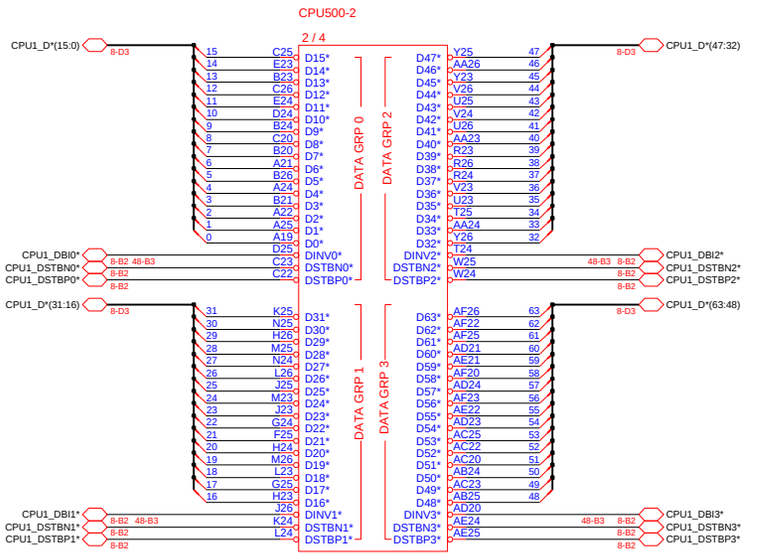
PART NO. BA41-00454A

COM-22C-015(1996.6.5) REV. 3

d:/users/desk27/mentor/venice/gt/venice_gt

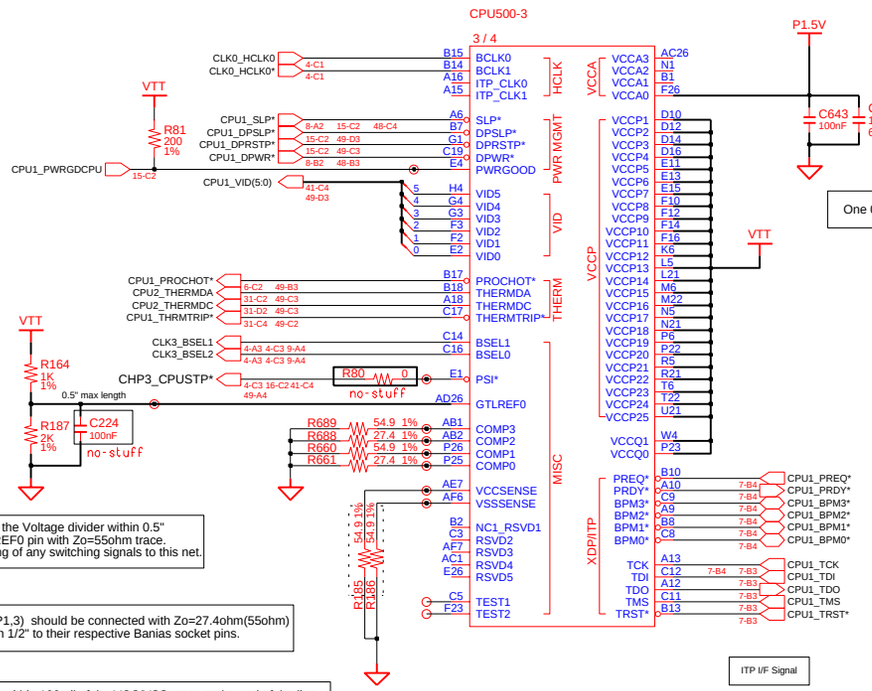
Rev. No	



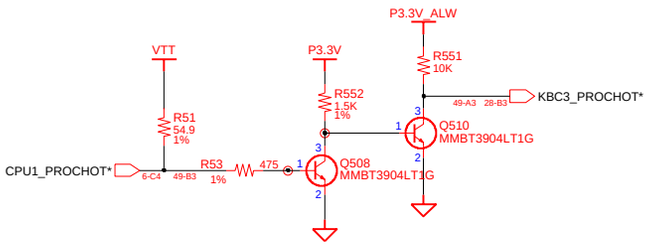


DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN DOTHAN_YONAH (1/3)	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 5 OF 49	

Rev. No	



One 0.1uF & 10uF cap for each VCCA pin.



GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

Std Voltage Dothan with 533 Mhz FSB updates
VCC (High Frequency Mode) = 1.26 V - 1.356 V (VID values)
TDP (Highest Frequency Mode) =27W (no change)
VCC (Lowest Frequency Mode) = 0.988 V (VID value)
TDP (Lowest Frequency Mode) = 13.8 W

CPU Core Voltage Table

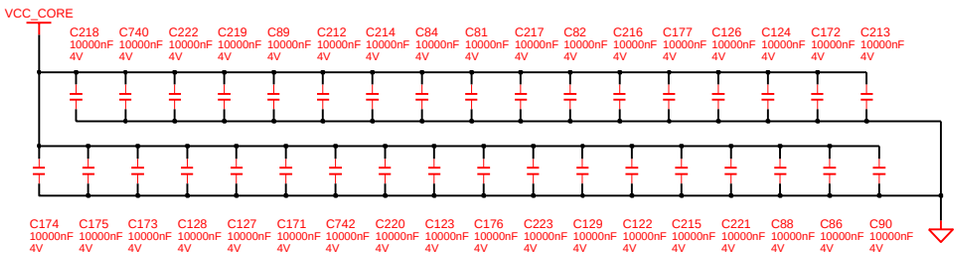
VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.708 V	1 0 0 0 0 0	1.196 V
0 0 0 0 0 1	1.692 V	1 0 0 0 0 1	1.180 V
0 0 0 0 1 0	1.676 V	1 0 0 0 1 0	1.164 V
0 0 0 0 1 1	1.660 V	1 0 0 0 1 1	1.148 V
0 0 0 1 0 0	1.644 V	1 0 0 1 0 0	1.132 V
0 0 0 1 0 1	1.628 V	1 0 0 1 0 1	1.116 V
0 0 0 1 1 0	1.612 V	1 0 0 1 1 0	1.100 V
0 0 0 1 **1** **1**	1.596 V	1 0 0 1 **1** **1**	1.084 V
0 0 1 0 0 0	1.580 V	1 0 1 0 0 0	1.068 V
0 0 1 0 0 1	1.564 V	1 0 1 0 0 1	1.052 V
0 0 1 0 1 0	1.548 V	1 0 1 0 1 0	1.036 V
0 0 1 0 1 1	1.532 V	1 0 1 0 1 1	1.020 V
0 0 1 1 0 0	1.516 V	1 0 1 1 0 0	1.004 V
0 0 1 1 0 1	1.500 V	1 0 1 1 0 1	0.988 V LFM
0 0 1 1 1 0	1.484 V	1 0 1 1 1 0	0.972 V
0 0 1 1 1 1	1.468 V	1 0 1 1 1 1	0.956 V
0 1 0 0 0 0	1.452 V	1 1 0 0 0 0	0.940 V
0 1 0 0 0 1	1.436 V	1 1 0 0 0 1	0.924 V
0 1 0 0 1 0	1.420 V	1 1 0 0 1 0	0.908 V
0 1 0 0 1 1	1.404 V	1 1 0 0 1 1	0.892 V
0 1 0 1 0 0	1.388 V	1 1 0 1 0 0	0.876 V
0 1 0 1 0 1	1.372 V	1 1 0 1 0 1	0.860 V
0 1 0 1 1 0	1.356 V	1 1 0 1 1 0	0.844 V
0 **1** 0 **1** **1**	1.340 V	**1** **1** 0 **1** **1**	0.828 V
0 1 1 0 0 0	1.324 V	1 1 1 0 0 0	0.812 V
0 1 1 0 0 1	1.308 V	1 1 1 0 0 1	0.796 V
0 1 1 0 1 0	1.292 V	1 1 1 0 1 0	0.780 V
0 1 1 0 1 1	1.276 V	1 1 1 0 1 1	0.764 V
0 1 1 1 0 0	1.260 V	1 1 1 1 0 0	0.748 V
0 1 1 1 0 1	1.244 V	1 1 1 1 0 1	0.732 V
0 1 1 1 1 0	1.228 V	1 1 1 1 1 0	0.716 V
0 1 1 1 1 1	1.212 V	1 1 1 1 1 1	0.700 V

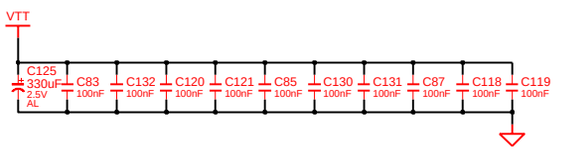
HFM Voltage
770 : 1.26V ~ 1.372V
730,740,750,760 : 1.26 ~ 1.356
In case of Deeper sheep, core voltage is 0.726V.

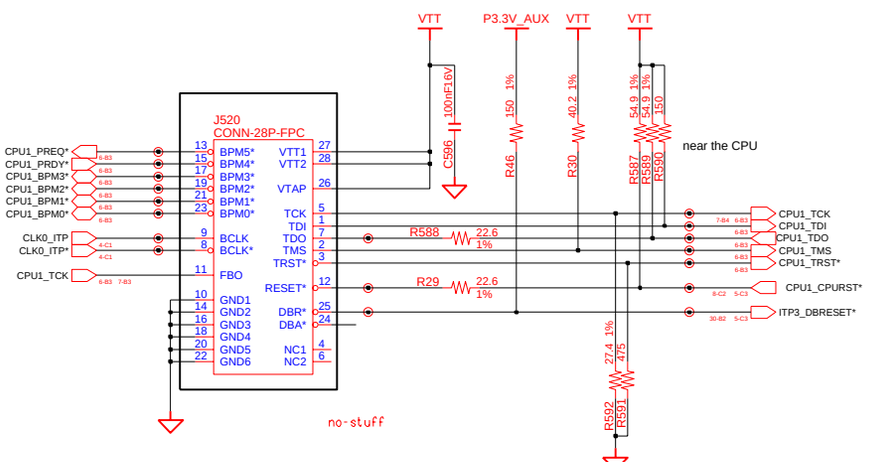
DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN DOTHAN_YONAH (2/3)
CHECK	KIM, MK	DEV. STEP	QT		
APPROVAL	LEE, BL	REV	A00		
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	6 OF 49

SAMSUNG DELL
PART NO. BA41-00454A

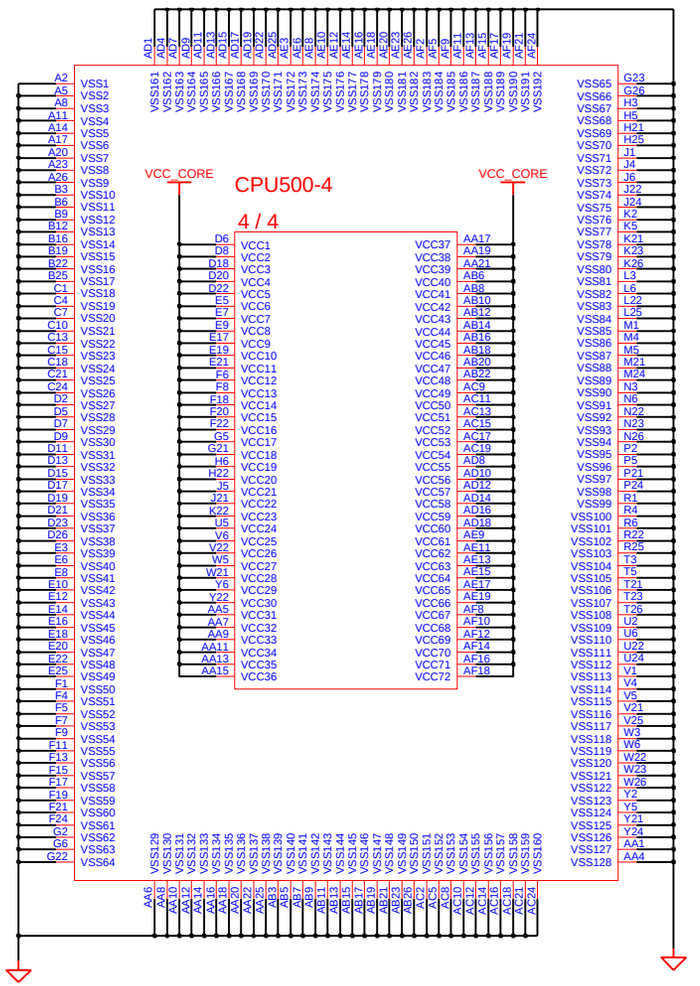
Rev. No	







J520 connector didn't place in the board.



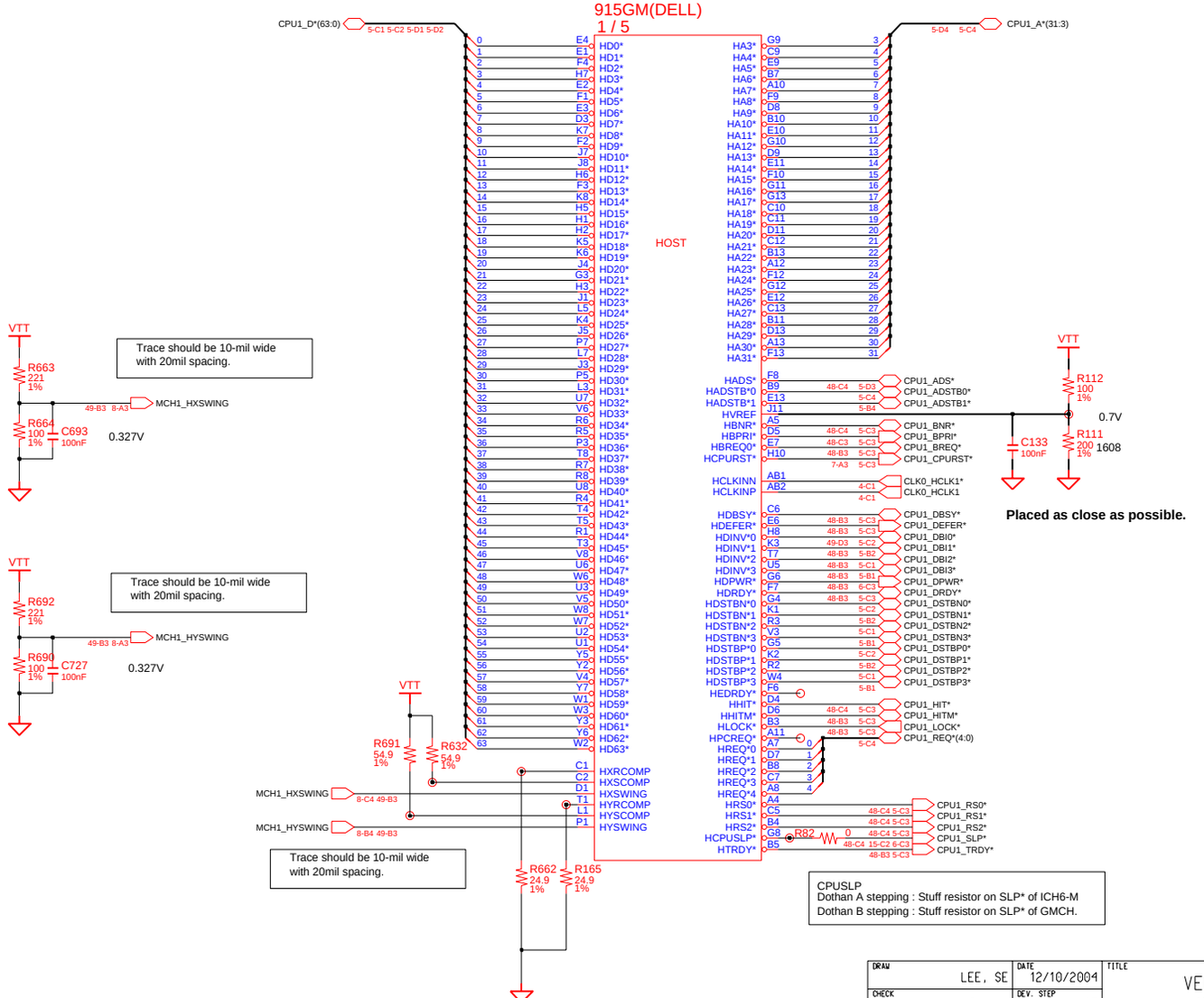
DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN DOTHAN_YONAH (3/3)
CHECK	KIM, MK	DEV. STEP	QT		
APPROVAL	LEE, BL	REV	A00		
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	7 OF 49

SAMSUNG DELL

PART NO. BA41-00454A

Rev. No

U514-1
915GM(DELL)
1 / 5



DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN GMCH-M (1/5)	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 8 OF 49	

Rev. No

U514-2
915GM(DELL)
2 / 5

TV DAC		
	Component	Composite
A	Pb	CVBS
B	Y	
C	Pr	

Place 75 ohm termination resistors close to GMCH

RED, GREEN, BLUE are GND referenced

Route as short as possible 1608

Place these close to SSCD.

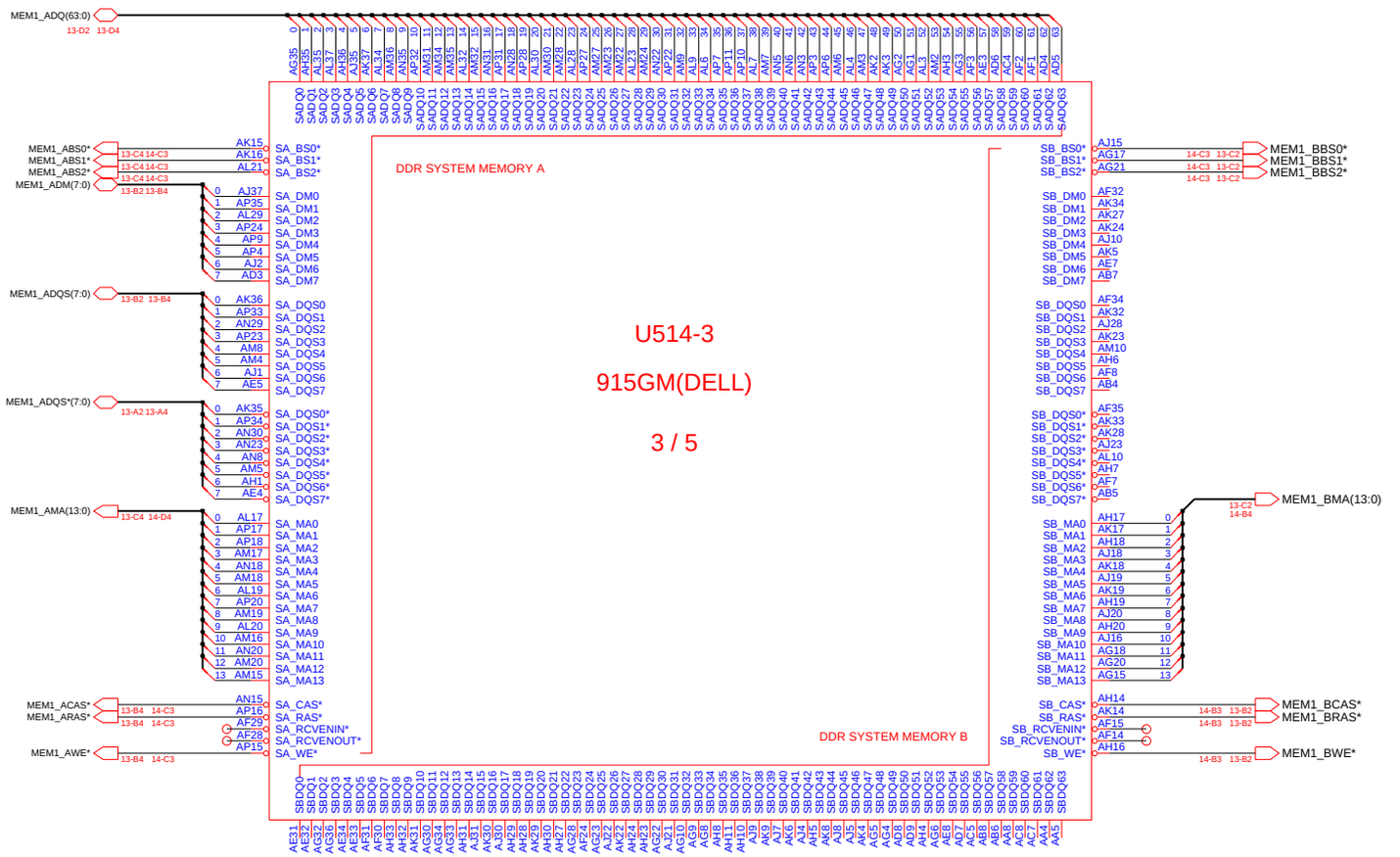
Current Setting (def. : default Option)

CFG#	Low	High
CFG(5)	***DMIx2***	DMIx4 (def.)
CFG(6)	***DDR-2***	DDR-1
CFG(7)	DT/Transportable	***Mobile CPU (def.)***
CFG(9)	PEG Reversal	***Normal***
CFG(16)	Dynamic ODT Disabled	***Enabled (def.)***
CFG(18)	***VCC 1.05V (def.)***	VCC 1.5V
CFG(19)	***VTT 1.05V (def.)***	VTT 1.2V
SDVODTA	***No (def.)***	SDVO Present

CFG(17:3) Internal Pull-up
CFG(20:18) Internal Pull-down

DRAW	LEE, SE	DATE 12/10/2004	TITLE VENICE MAIN GMCH-M (2/5)
CHECK	KIM, MK	DEV. STEP QT	SAMSUNG DELL
APPROVAL	LEE, BL	REV A00	PART NO. BA41-00454A
MODULE CODE		LAST EDIT December 10, 2004 2:14:59 PM	PAGE 9 OF 49

Rev. No	



DDR/DDR2 Common Signal Mappping

Single Channel Mode Signal Mapping

Single Channel Signal Mapping.	
SO-DIMM 0	**SO-DIMM 1**
SM_CK [1:0]	SM_CK [4:3]
SM_CK* [1:0] (DDR2 support)	SM_CK* [4:3] (DDR2 support)
SM_CS* [1:0]	SM_CS* [3:2]
SM_CKE [1:0]	SM_CK [3:2]
SM_ODT [1:0] (DDR2 support)	SM_ODT [3:2] (DDR2 support)
SA_BS [2:0]	SB_BS [2:0]
SA_MA [13:0]	SB_MA [13:0]
SA_RAS*	SB_RAS*
SA_CAS*	SB_CAS*
SA_WE*	SB_WE*
SA_DQ [63:0]	
SA_DQS [7:0]	
SA_DQS* [7:0]	
SA_DM [7:0]	

DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN GMCH-M (3/5)	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 10 OF 49	

Rev. No

U514-4
915GM(DELL)
4 / 5

POWER

Route VSSA_CRTDAC gnd from GMCH to decoupling cap gnd lead and then connect to the gnd plane.

Place C17 closest to GMCH

From CRTDAC pin , max. 0.25" max. 3"

VSSA_CRTDAC : Route caps within 250 mil of GMCH.
Route FB within 3" of GMCH.
Route VSSA_CRTDAC gnd from GMCH to decoupling cap gnd lead and then connect to the gnd plane

DRAW	LEE, SE	DATE	12/10/2004
CHECK	KIM, MK	DEV. STEP	QT
APPROVAL	LEE, BL	REV	A00
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM

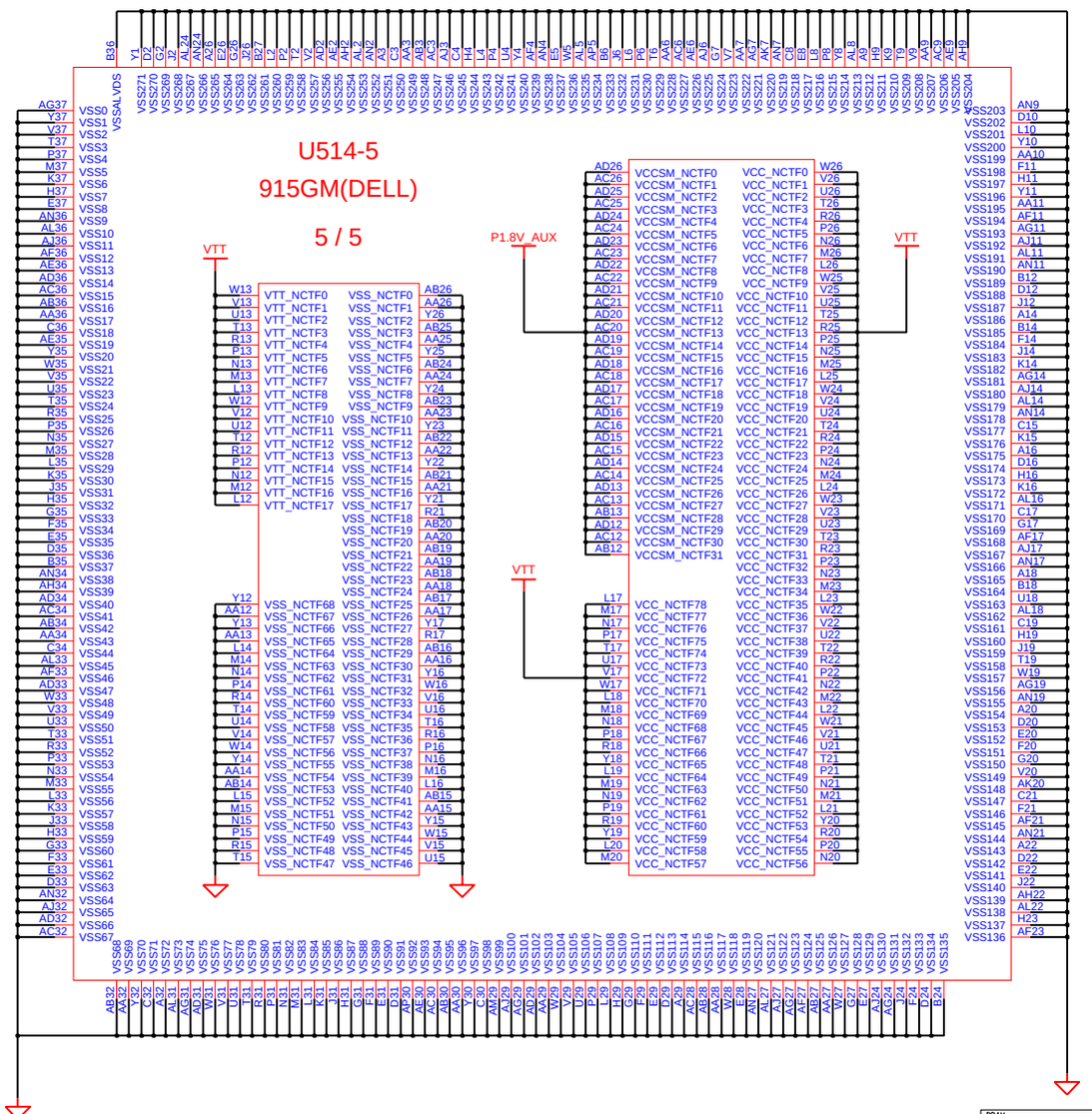
TITLE: VENICE MAIN GMCH-M (4/5)

SAMSUNG DELL

PART NO. BA41-00454A

PAGE 11 OF 49

Rev. No	

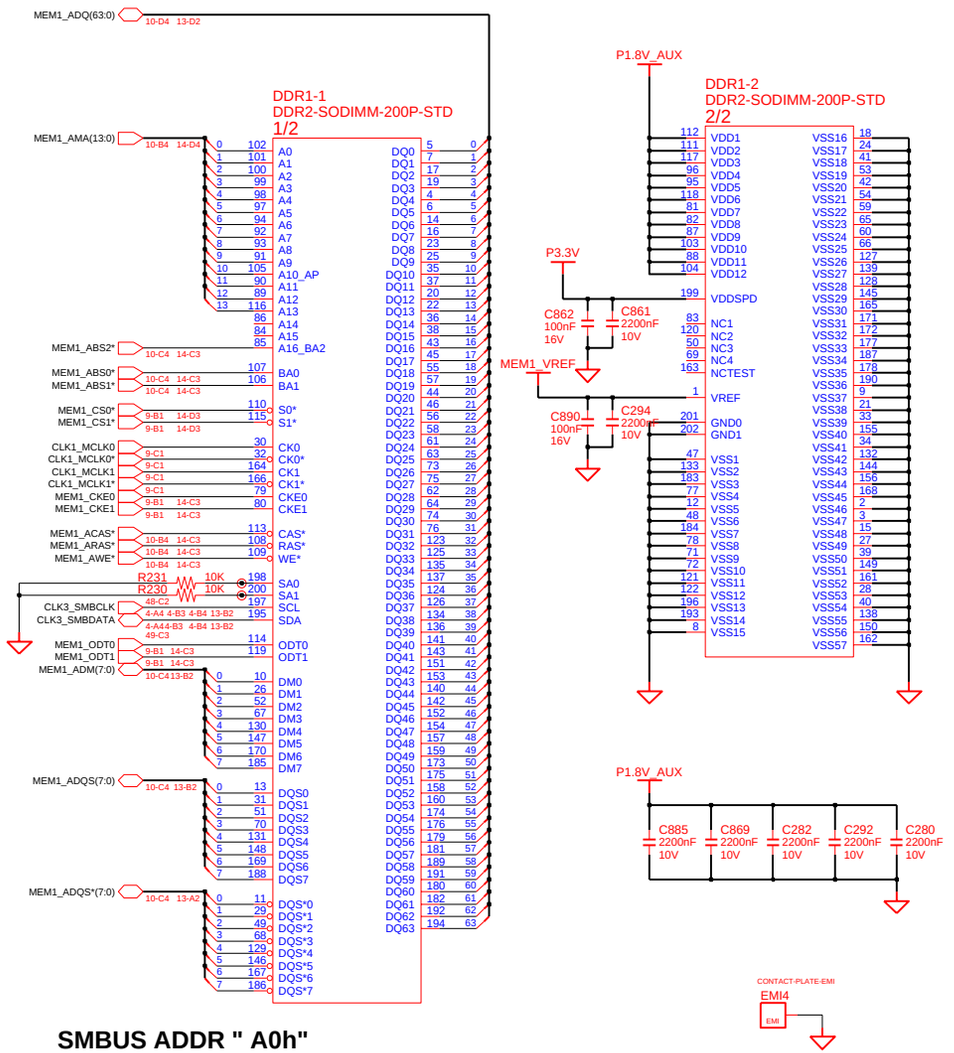


DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN GMCH-M (5/5)
CHECK	KIM, MK	DEV. STEP	QT		
APPROVAL	LEE, BL	REV	A00		
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	12 OF 49

SAMSUNG
DELL
PART NO. BA41-00454A

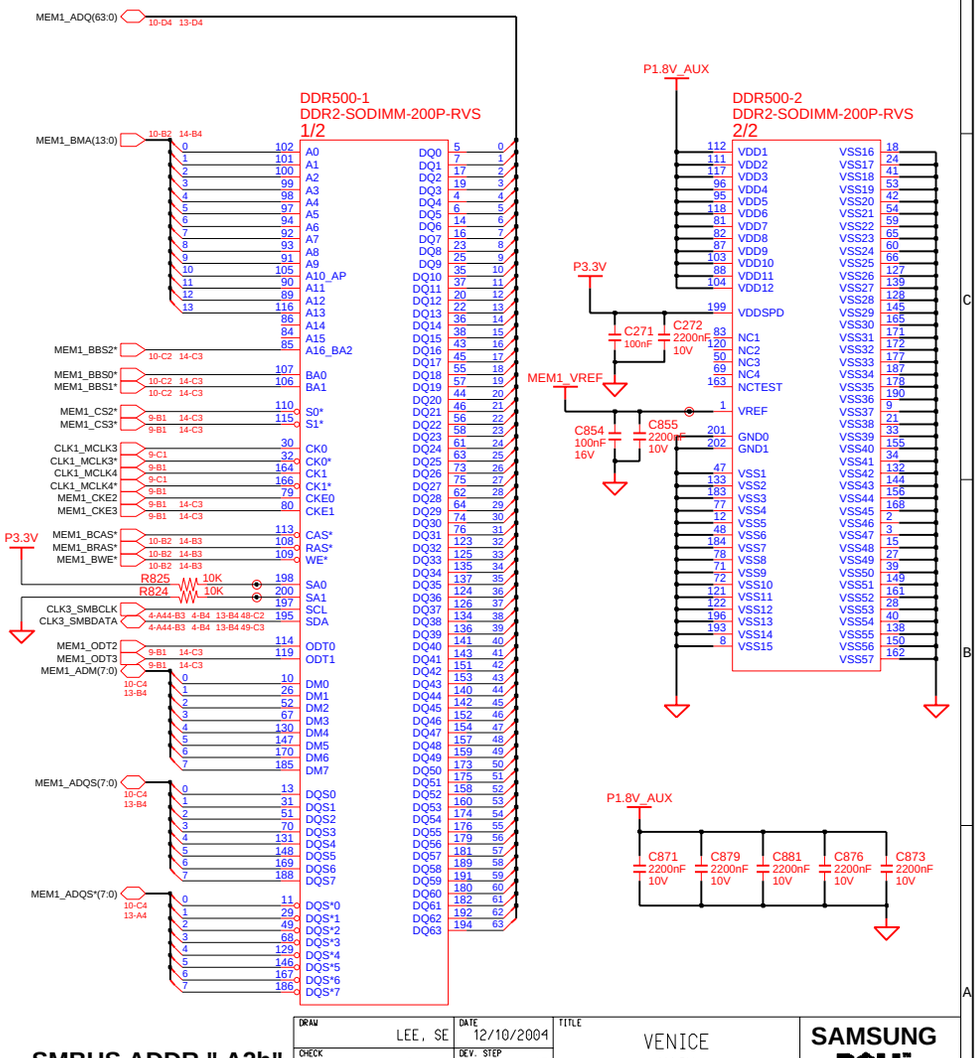
Rev. No

DDR2 SO-DIMM #0 Bottom



SMBUS ADDR " A0h"

DDR2 SO-DIMM #1 Top

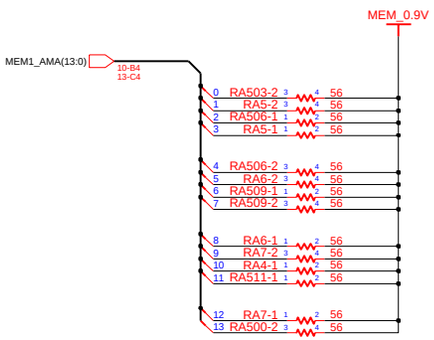


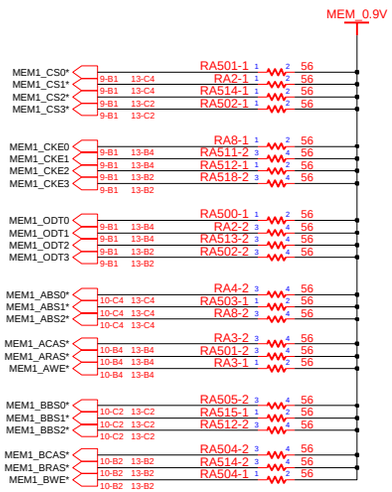
SMBUS ADDR " A2h"

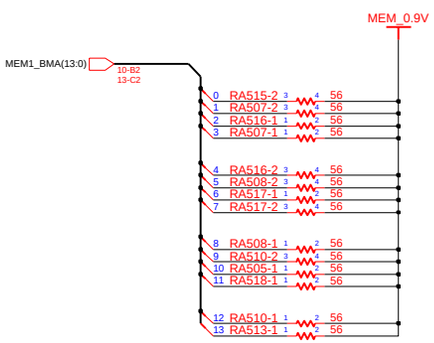
DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN DDR 2 SODIMM	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 13 OF 49	

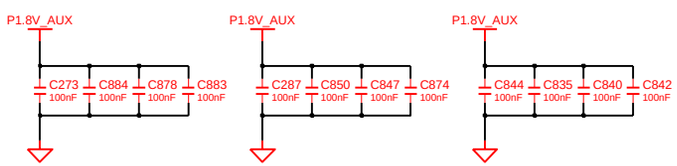
Rev. No	

Array resistors & Single resistors used to improve layout & routing.





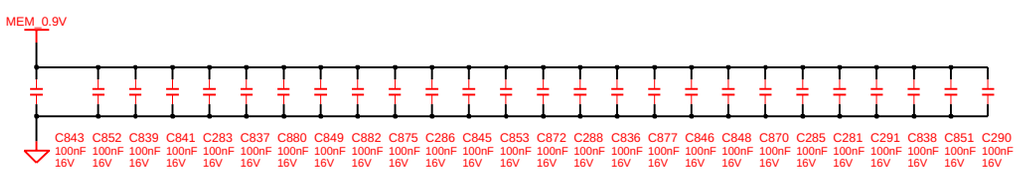




Place near GMCH

Place near SO-DIMM0

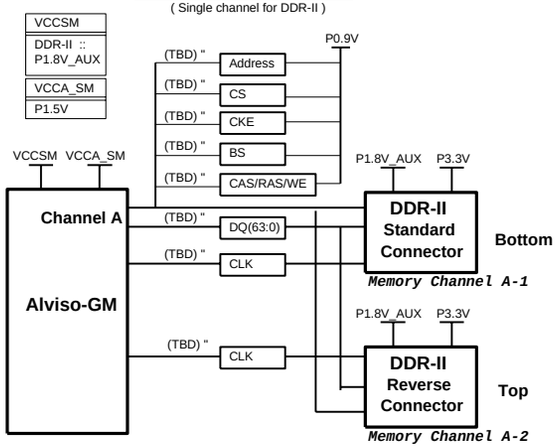
Place near SO-DIMM1



Place one cap close to every 2 pull-up resistors terminated to P0.9V

Memory Topology

(Single channel for DDR-II)



DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN TERMINATION	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 14 OF 49	

Rev. No

U515-1
82801FBM(DELL)
1 / 5

CPUSLP*
Dothan A stepping : Stuff resistor on SLP* of ICH6-M
Dothan B stepping ~ : Stuff resistor on SLP of GMCH.

DPRSTP*
Dothan : No stuff
Yonah : Stuff

For RTC reset

Place 56 ohm resistor within 2" of ICH6-M
Place PU resistor within 2" of ICH6-M

DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN ICH6-M (1/4)	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 15 OF 49	

Rev. No

AC caps : PCIE need to be within 250mils of the driver
Resistor for Test : Place Stuffing Option to minimize stubs

U515-2 82801FBM(DELL) 2 / 5

PCI3_AD(31:0) — AD0 … AD31

PCI3_FRAME* — FRAME*

PCI3_INTA* — PIRQA*
PCI3_INTB* — PIRQB*
PCI3_INTC* — PIRQC*
PCI3_INTD* — PIRQD*

PCI3_REQ0* — REQ0*
PCI3_GNT0* — GNT0*
PCI3_REQ1* — REQ1*
PCI3_GNT1* — GNT1*
PCI3_REQ2* — REQ2*
PCI3_GNT2* — GNT2*
PCI3_REQ3* — REQ3*
PCI3_GNT3* — GNT3*
REQ4*_GPI40
GNT4*_GPO48
REQ5*_GPI1
GNT5*_GPO17
REQ6*_GPI0
GNT6*_GPO16

CHP3_REQ5*
LCD5_LAMPSTAT

PCI3_CBE0* — C_BE0*
PCI3_CBE1* — C_BE1*
PCI3_CBE2* — C_BE2*
PCI3_CBE3* — C_BE3*

PCI3_IRDY* — IRDY*
PCI3_PAR — PAR
PCI3_RST* — PCIRST*
PCI3_DEVSEL* — DEVSEL*
PCI3_PERR* — PERR*
PCI3_PLOCK* — PLOCK*
PCI3_SERR* — SERR*
PCI3_STOP* — STOP*
PCI3_TRDY* — TRDY*

PLT3_RSTF* — PLTRST*
CLK3_PCLKICH6M — PCICLK
CHP3_PME* — PME*

PCI
INTERRUPT I/F
RESERVED

PIRQE*_GPI2
PIRQF*_GPI3
PIRQG*_GPI4
PIRQH*_GPI5

RSVD1_SATA1RXN
RSVD2_SATA1RXP
RSVD3_SATA1TXN
RSVD4_SATA1TXP
RSVD5_SATA3RXN
RSVD6_SATA3RXP
RSVD7_SATA3TXN
RSVD8_SATA3TXP
RSVD9_TP3

R143 33 1% no-stuff
C158 0.027nF no-stuff

P3.3V_AUX
U14 7SZ08
PLT3_RSTF* → PLT3_RST*

CLK3_ICH14
CLK3_USB48
ICH_PWROK
R85 100K
R207 10
R144 10
C244 0.01nF 0.5pF
C159 0.0033nF
no-stuff
PGND

Place near the ICH6-M

U515-3 82801FBM(DELL) 3 / 5

P3.3V P3.3V_AUX
R169 10K R136 10K R88 10K R91 10K

SMB3_CLK
SMB3_DATA
SMB3_LINKALERT*
SMBCLK SMBDATA LINKALERT* SMLINK0 SMLINK1 MCH_SYNC* SPKR
CHP3_SPKR

SUS_STAT*_LPCPD*
SYS_RESET*
R90 10K

MCH2_BMBUSY*
BMBUSY*_GPI6
R172 10K no-stuff
KBC3_EXTSMI*
SMBALERT*_GPI11
SMB3_ALERT*
KBC3_WAKESCI*
KBC3_RUNSCI*
GPI12 GPI13
CHP3_PCISTP*
STP_PCI*_GPO18
R175 10K no-stuff
GPO19
CHP3_CPUSTP*
STP_CPU*_GPO20
TPM_RST*
R177 0 no-stuff
GPO21 GPO23
GPIO24
R138 10K no-stuff
GPIO25 GPIO27 GPIO28
PCI3_CLKRUN*
CLKRUN*_GPIO32 GPIO33 GPIO34

KBC3_PCIE_WAKE*
CHP3_SERIRQ
KBC3_THRM*
IMVP_PWRGD
CLK3_ICH14
CLK3_USB48
WAKE* SERIRQ THRM* VRMPWRGD CLK14 CLK48 SUSCLK
R171 49.9

CHP3_SLPS3*
CHP3_SLPS5*
ICH_PWROK
CHP3_DPRSLPVR
SLP_S3* SLP_S4* SLP_S5* PWROK DPRSLPVR_TP1 BATLOW*_TP0
R173 100 1%
R89 10K

KBC3_PWRBTN*
PLT3_RST*
SUSPWROK
PWRBTN* LAN_RST* RSMRST*
R87 100 1%
R168 100K
R131 100K

PCI-EXPRESS
GPIO
DIRECT MEDIA INTERFACE
CLOCKS
USB
POWER MGT

PERN1 PERP1 PETN1 PETP1 — PEX1_RXN1 PEX1_RXP1 PEX1_TXN1 PEX1_TXP1
C239 100nF 10V
C238 100nF 10V
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4

DMI0RXN DMI0RXP DMI0TXN DMI0TXP — DMI1_RXN0 DMI1_RXP0 DMI1_TXN0 DMI1_TXP0
DMI1RXN DMI1RXP DMI1TXN DMI1TXP — DMI1_RXN1 DMI1_RXP1 DMI1_TXN1 DMI1_TXP1
DMI2RXN DMI2RXP DMI2TXN DMI2TXP
DMI3RXN DMI3RXP DMI3TXN DMI3TXP

Place 24.9ohm wthin 500 mils of ICH6-M

DMI_CLKN DMI_CLKP — CLK1_PCIEICH* CLK1_PCIEICH
DMI_ZCOMP
DMI_IRCOMP
R197 24.9 1%

P3.3V_AUX
10K R203 10K R198 10K R199 10K R200 10K R202 10K R204 10K R206
P1.5V

OC4*_GPI9
OC5*_GPI10
OC6*_GPI14
OC7*_GPI15
OC0*
OC1*
OC2*
OC3*
USB3_OC4*
USB3_OC0*
USB3_OC3*

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P
USB3_P0- USB3_P0+ USB3_P1- USB3_P1+ USB3_P2- USB3_P2+ USB3_P3- USB3_P3+ USB3_P4- USB3_P4+ USB3_P5- USB3_P5+

USBRBIAS* USBRBIAS
R179 22.6 1%

Place within 500 mils of ICH6-M

DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN ICH6-M (2/4)	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 16 OF 49	

Rev. No

4 / 5

U515-4
82801FBM(DELL)

Place caps within 100mils of ICH6-M near F27, P27, AB27

Place near pin AA19 of the ICH6-M

Place 100nF within 100 mils near pin AG13, AG16

Distribute in PCI section near pin A2-A6, near D1-H1

Place near pin U7,R7

Place near pin G19

Place 100nF near pin A8

Place 100nF near pin F21

Place 100nF within 100 mils near pin AG9

Place 100nF within 100 mils near pin AG5

Place 10nF within 100 mils of ICH6-M

Place both within 100 mils near pin D27

Place near pin AB18

Place 100nF within 100mils pin E26,E27
Place 100nF within 100mils pin AE1

Place 100nF within 100 mils near pin AG10

Place 100nF within 100 mils near pin A13

Place 100nF within 100 mils of ICH6-M pin V7

Place both within 100 mils near pin A17

Place both within 100 mils near pin G10

Place near pin AB3

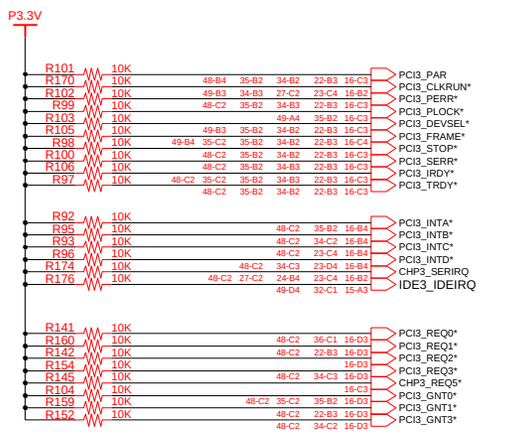
Place within 100 mils of ICH6-M (Pin A24)

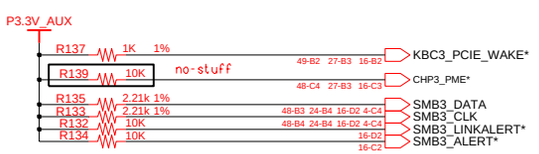
Place both within 100 mils near pin AG23

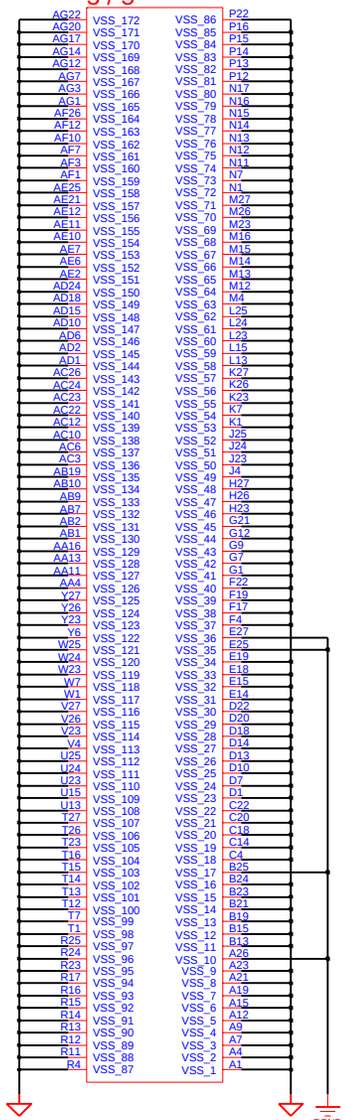
Place 10nF within 100 mils of ICH6-M

DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN ICH6-M (3/4)	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 17 OF 49	

Rev. No	



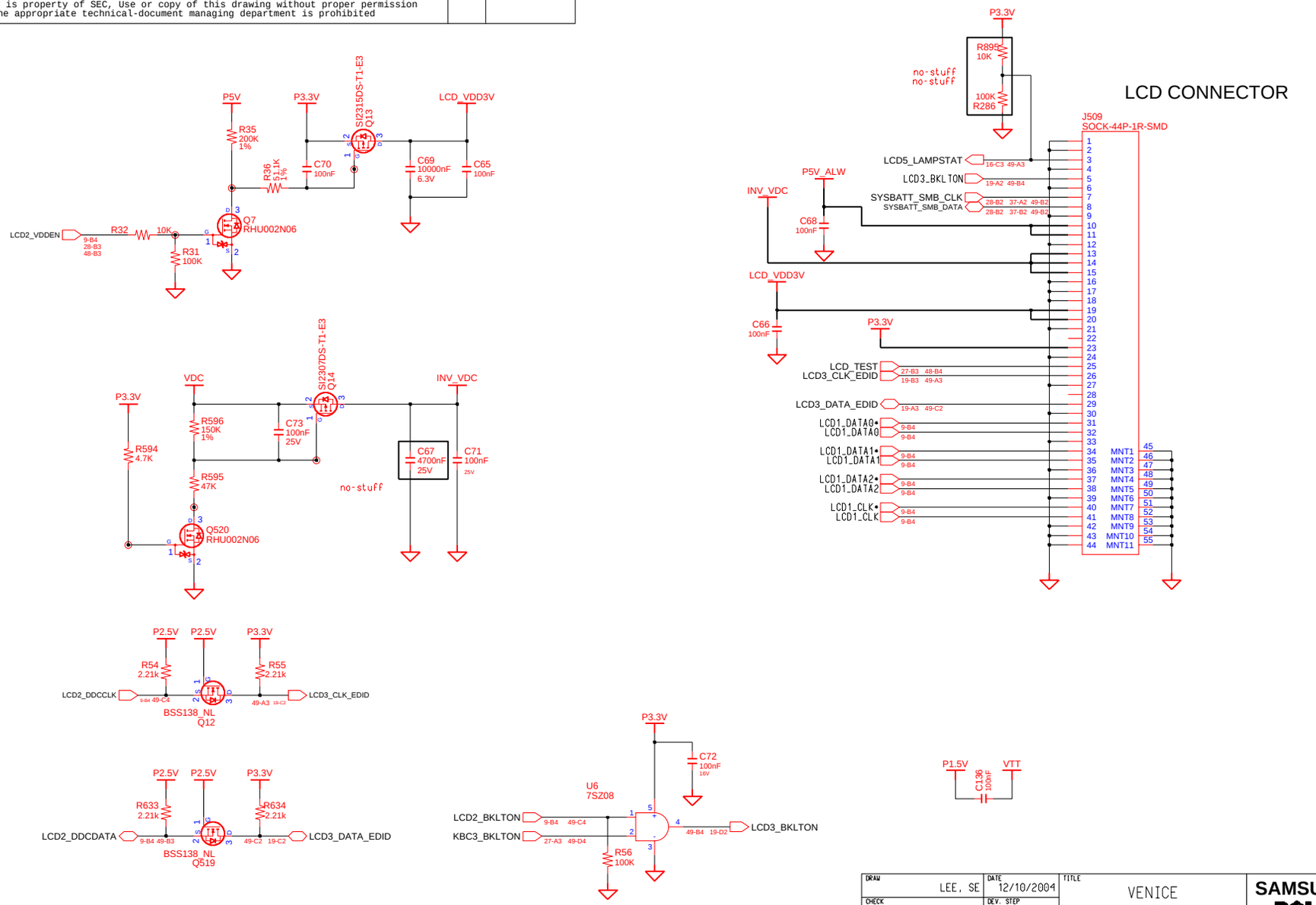




DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN ICH6-M (4/4)	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 18 OF 49	

Rev. No

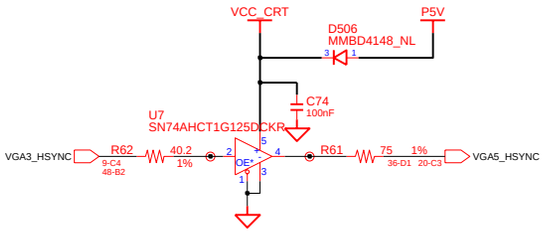
LCD CONNECTOR

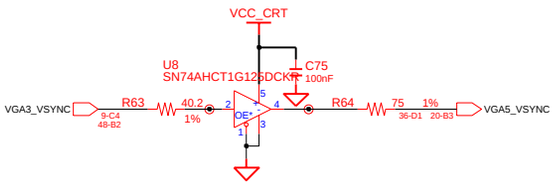


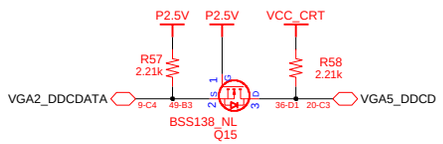
DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN LCD INTERFACE	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 19 OF 49	

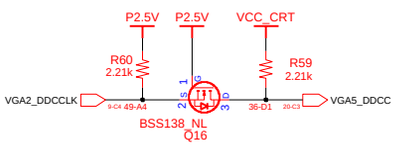
Rev. No	

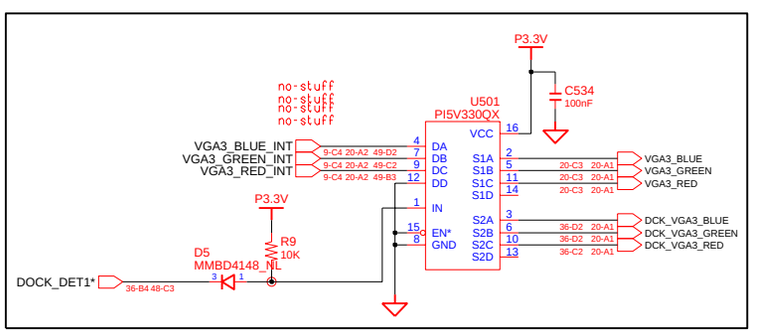
CRT CONNECTOR

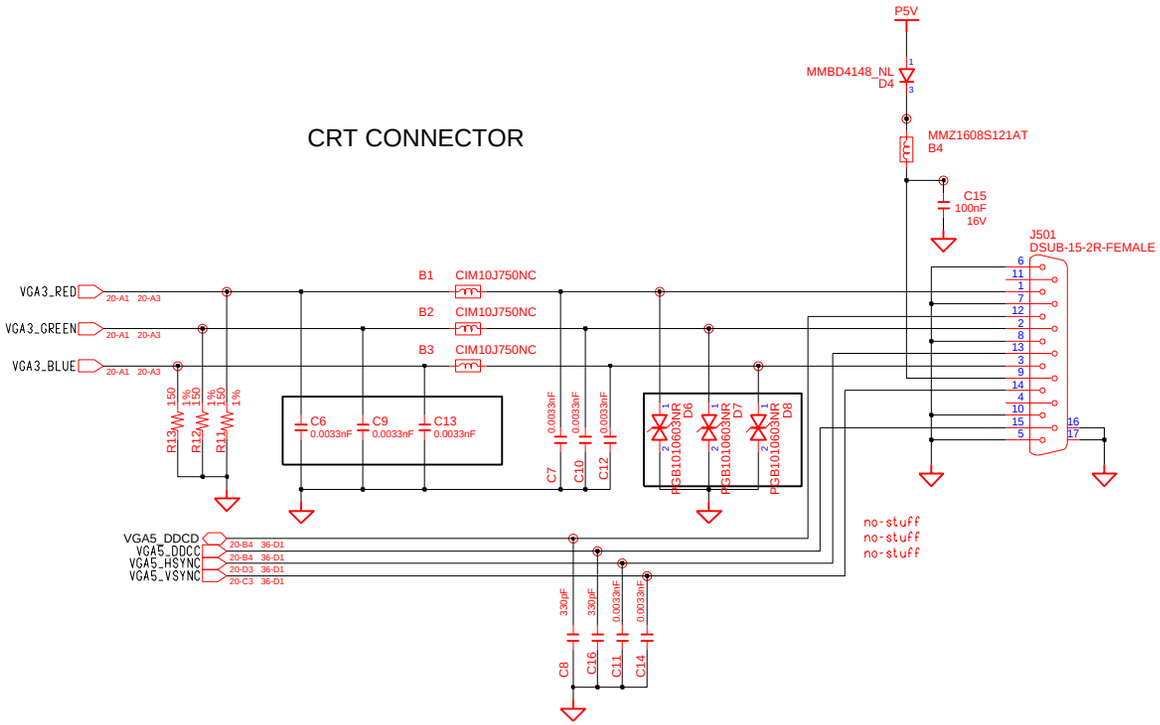






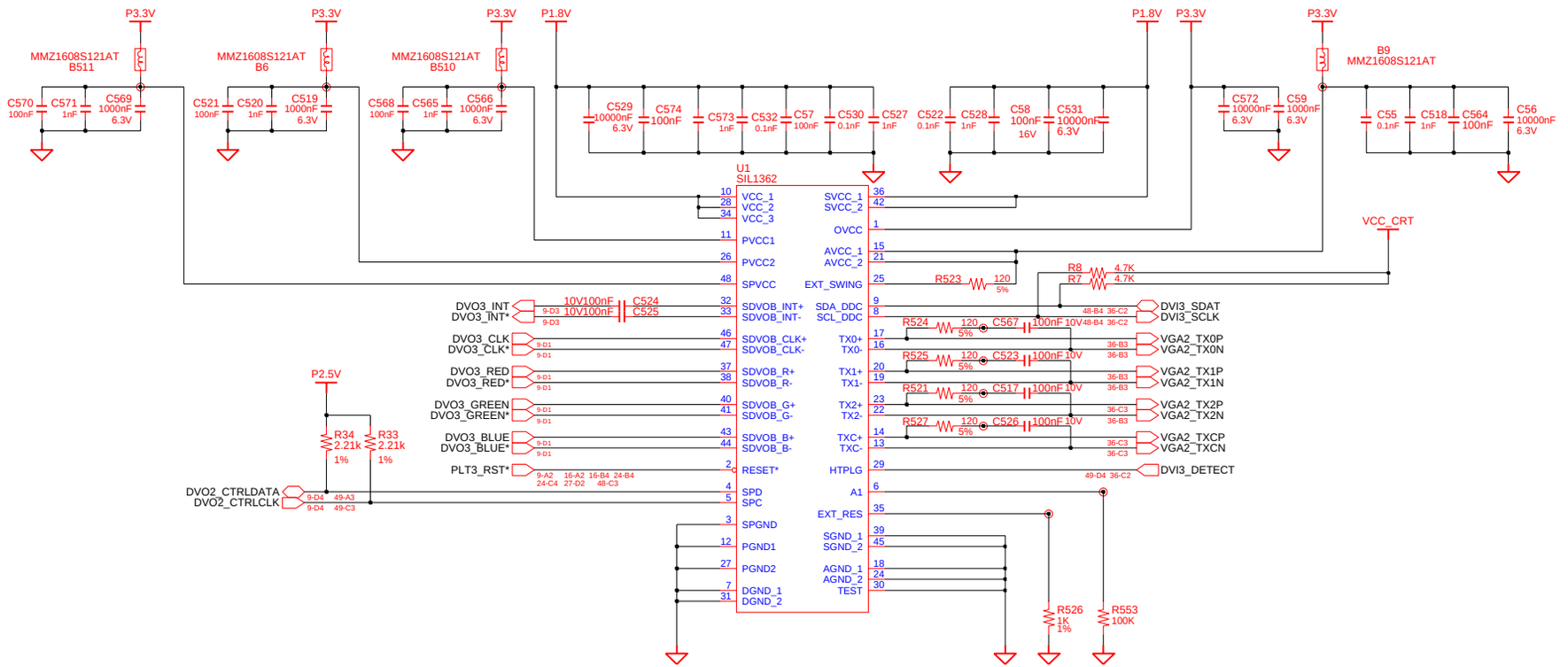






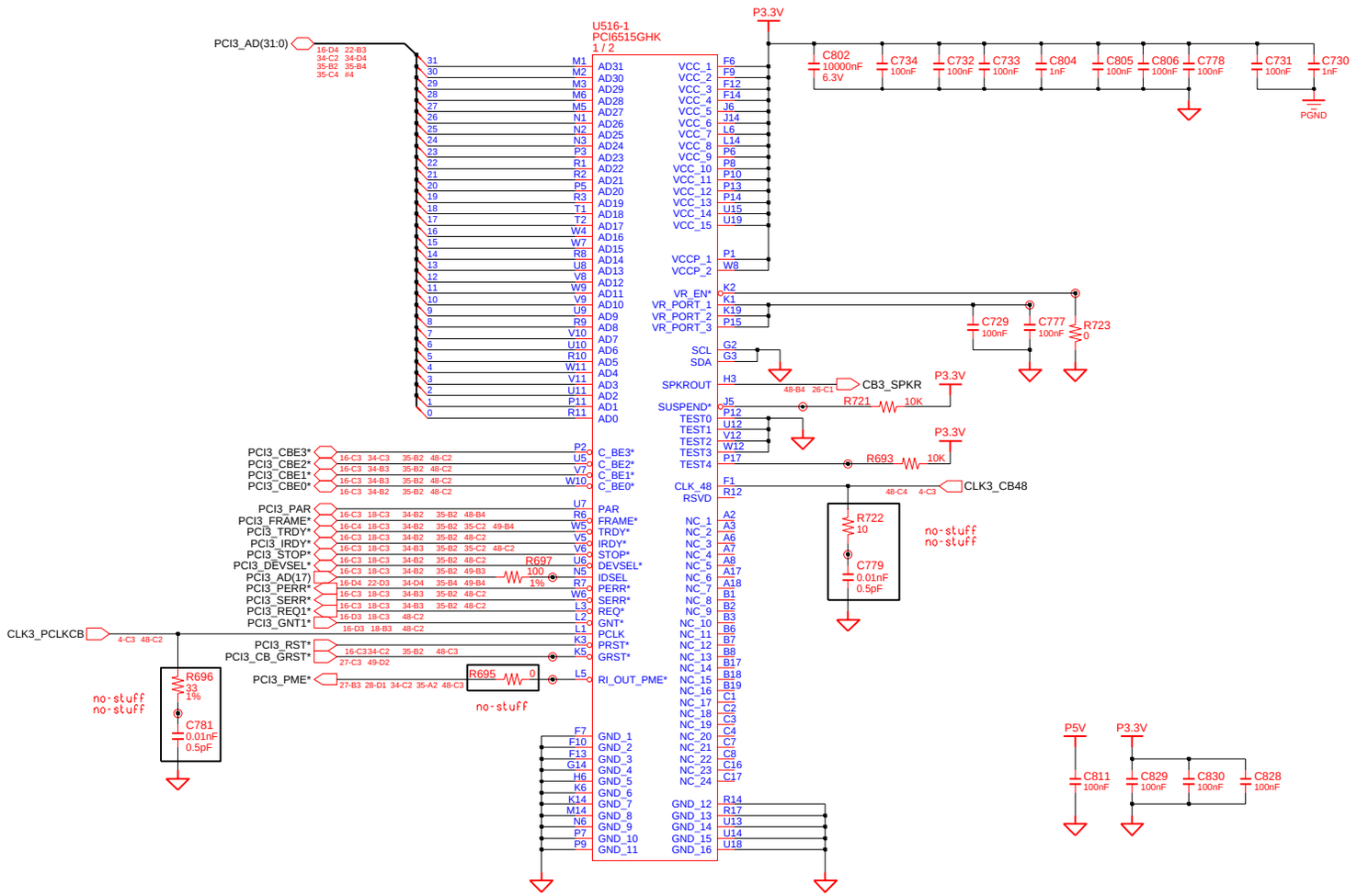
DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN CRT INTERFACE	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 20 OF 49	

Rev. No	



DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN DVI	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 21 OF 49	

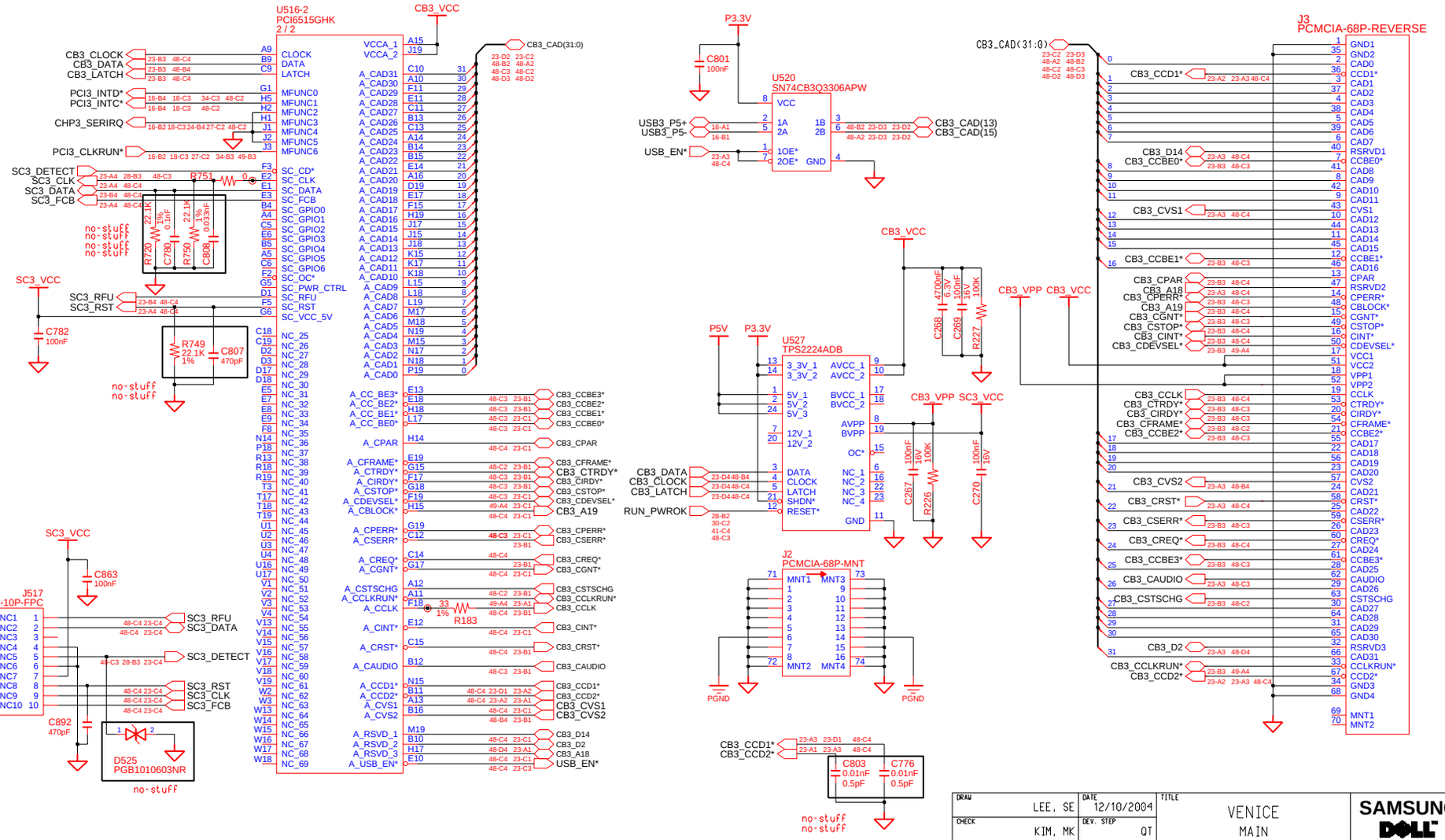
Rev. No	



DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN CARDBUS (1/2)	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 22 OF 49	

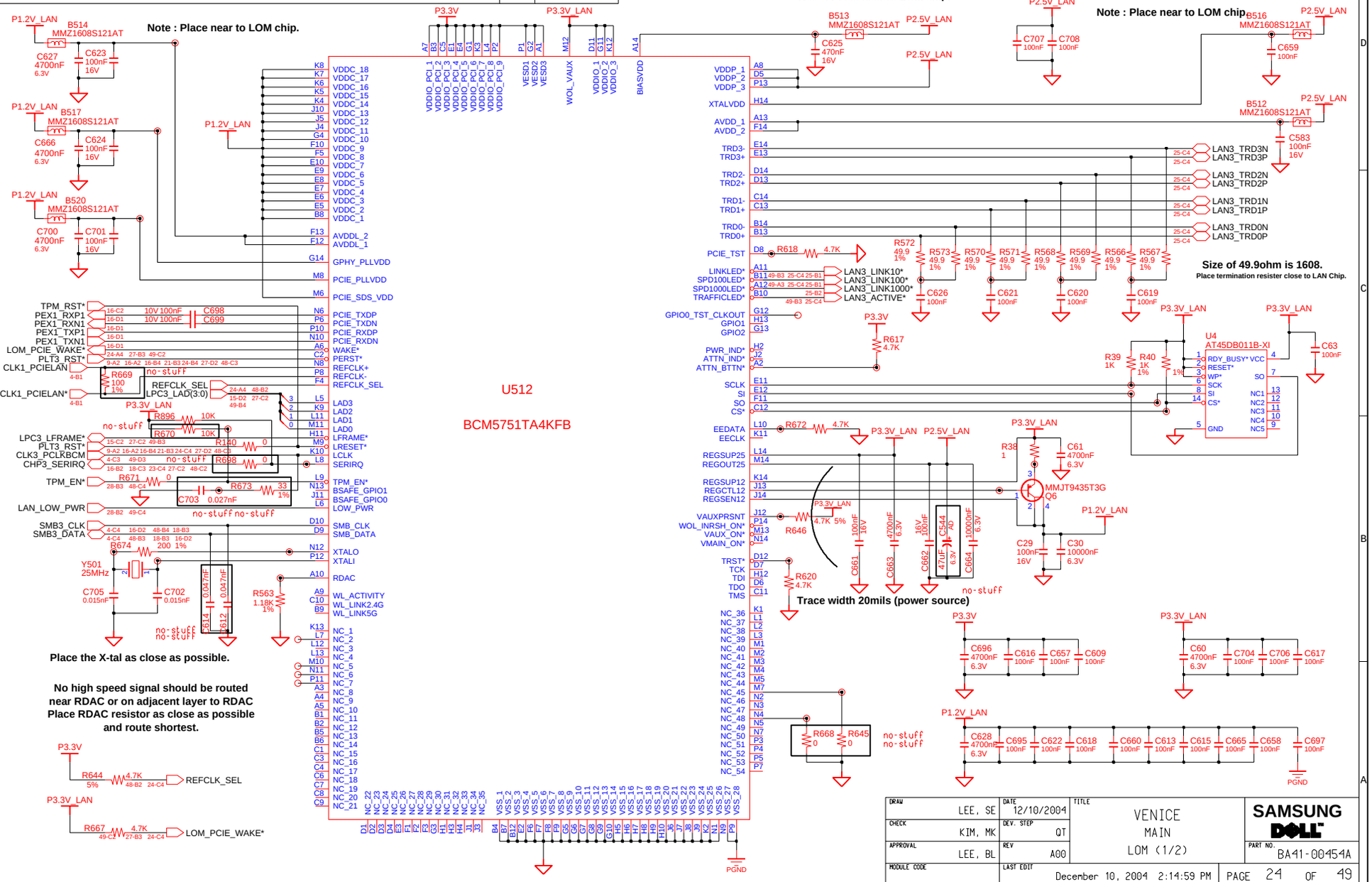
Rev. No

Place this near PCI6515 J18,J17 in order to minimize the stub.
These signals impedance should be differential 110ohm, and are treated like USB2.0 signal.



DRAW	LEE, SE	DATE 12/10/2004	TITLE VENICE MAIN CARDBUS (2/2)
CHECK	KIM, MK	DEV. STEP QT	SAMSUNG DELL
APPROVAL	LEE, BL	REV A00	PART NO. BA41-00454A
MODULE CODE		LAST EDIT December 10, 2004 2:14:59 PM	PAGE 23 OF 49

Rev. No



DRAW	LEE, SE	DATE	12/10/2004
CHECK	KIM, MK	DEV. STEP	QT
APPROVAL	LEE, BL	REV	A00
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM

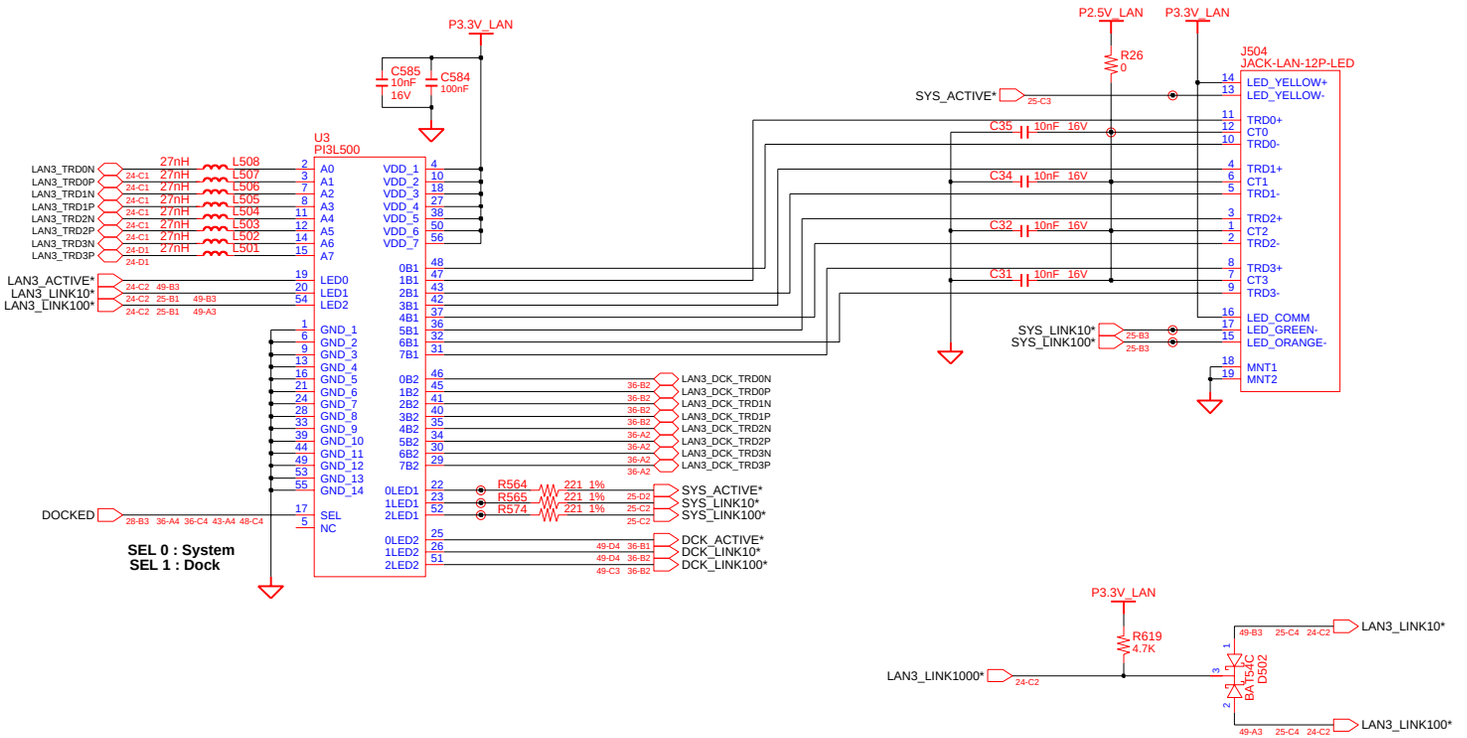
TITLE: VENICE MAIN LOM (1/2)

SAMSUNG DELL

PART NO. BA41-00454A

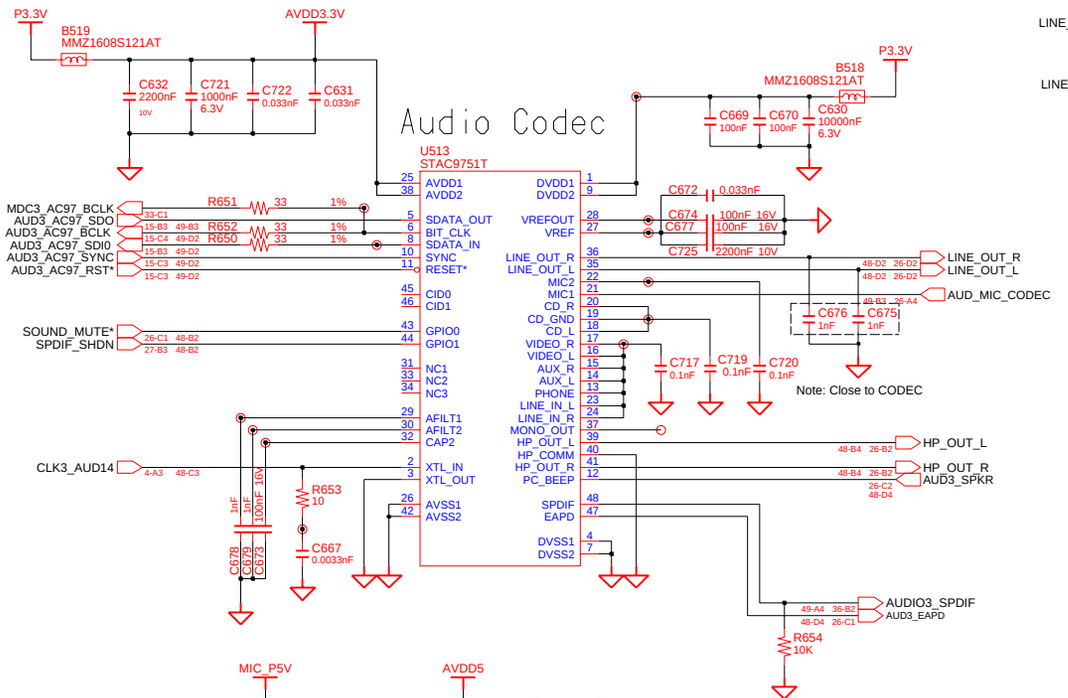
PAGE 24 OF 49

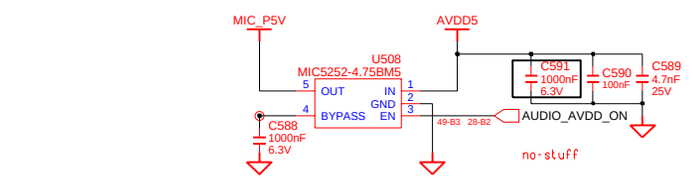
Rev. No

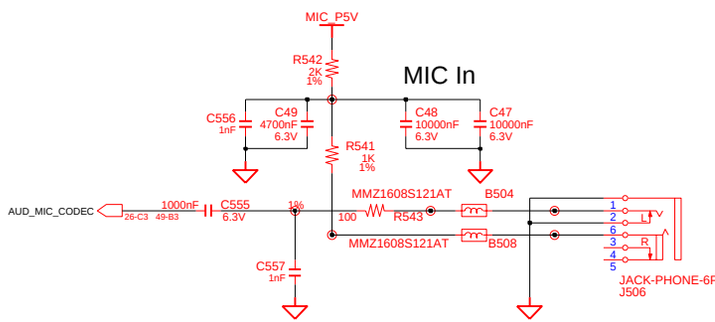


DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN LOM (2/2)	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 25 OF 49	

Rev. No

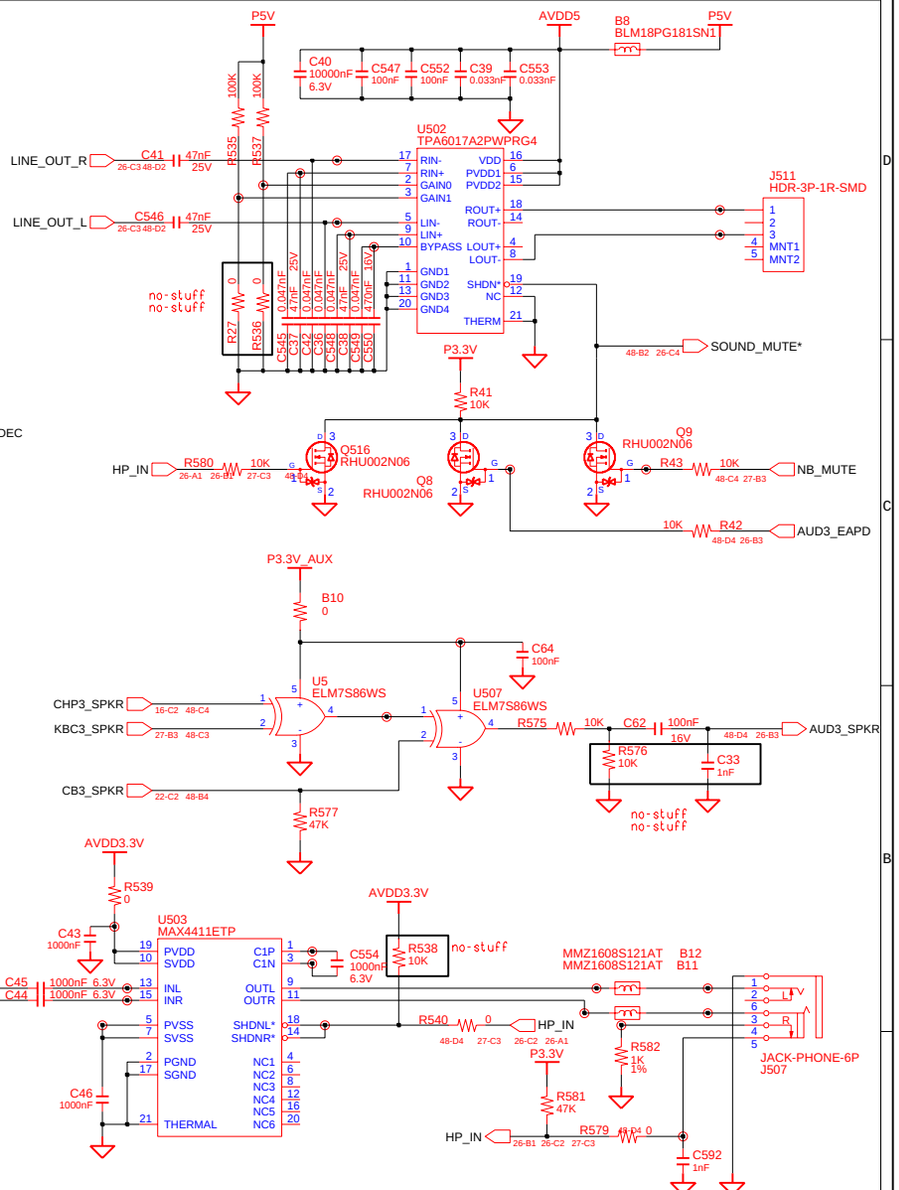






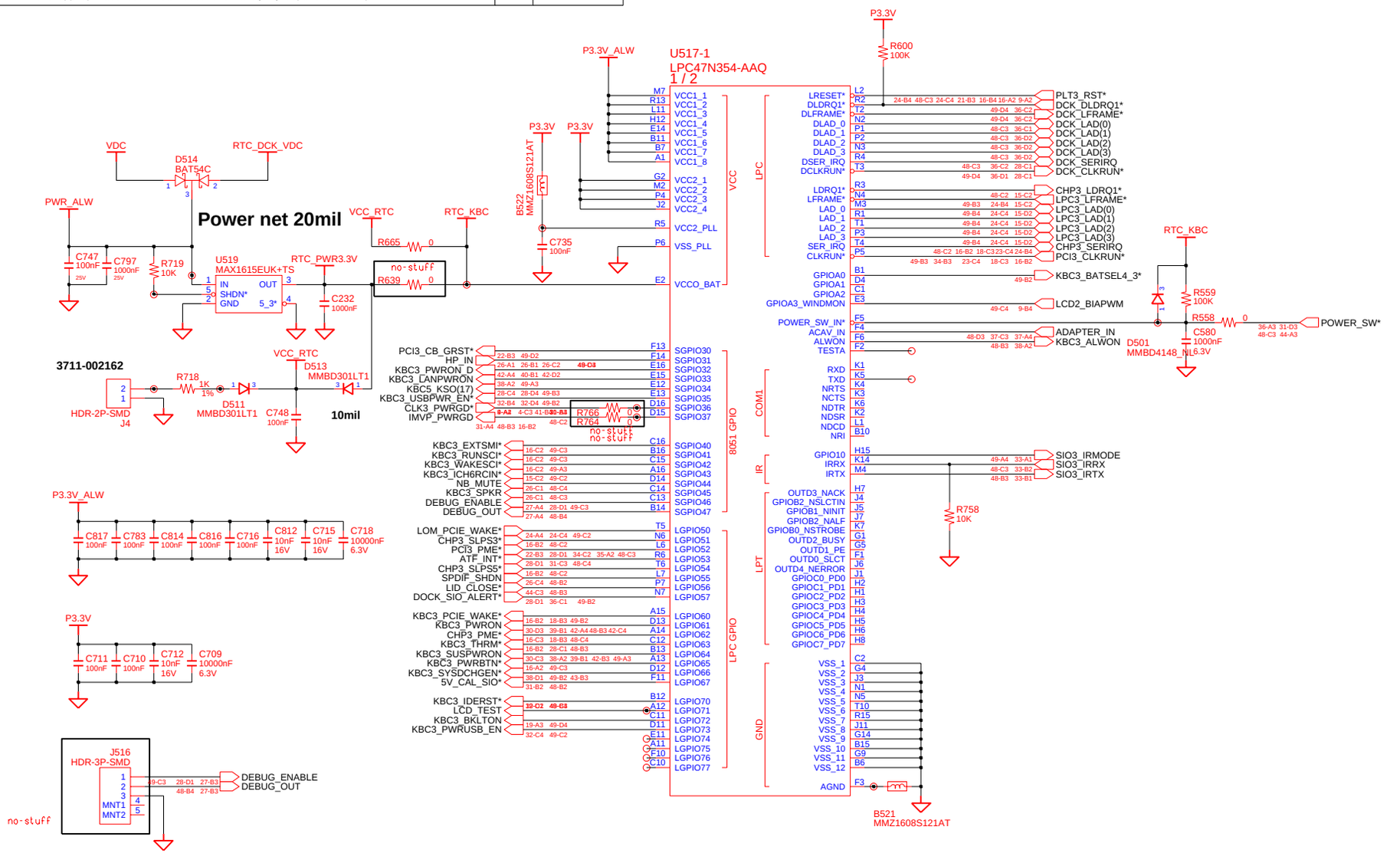
HEADPHONE

Note : Route HP_OUT_R/L/COMM together



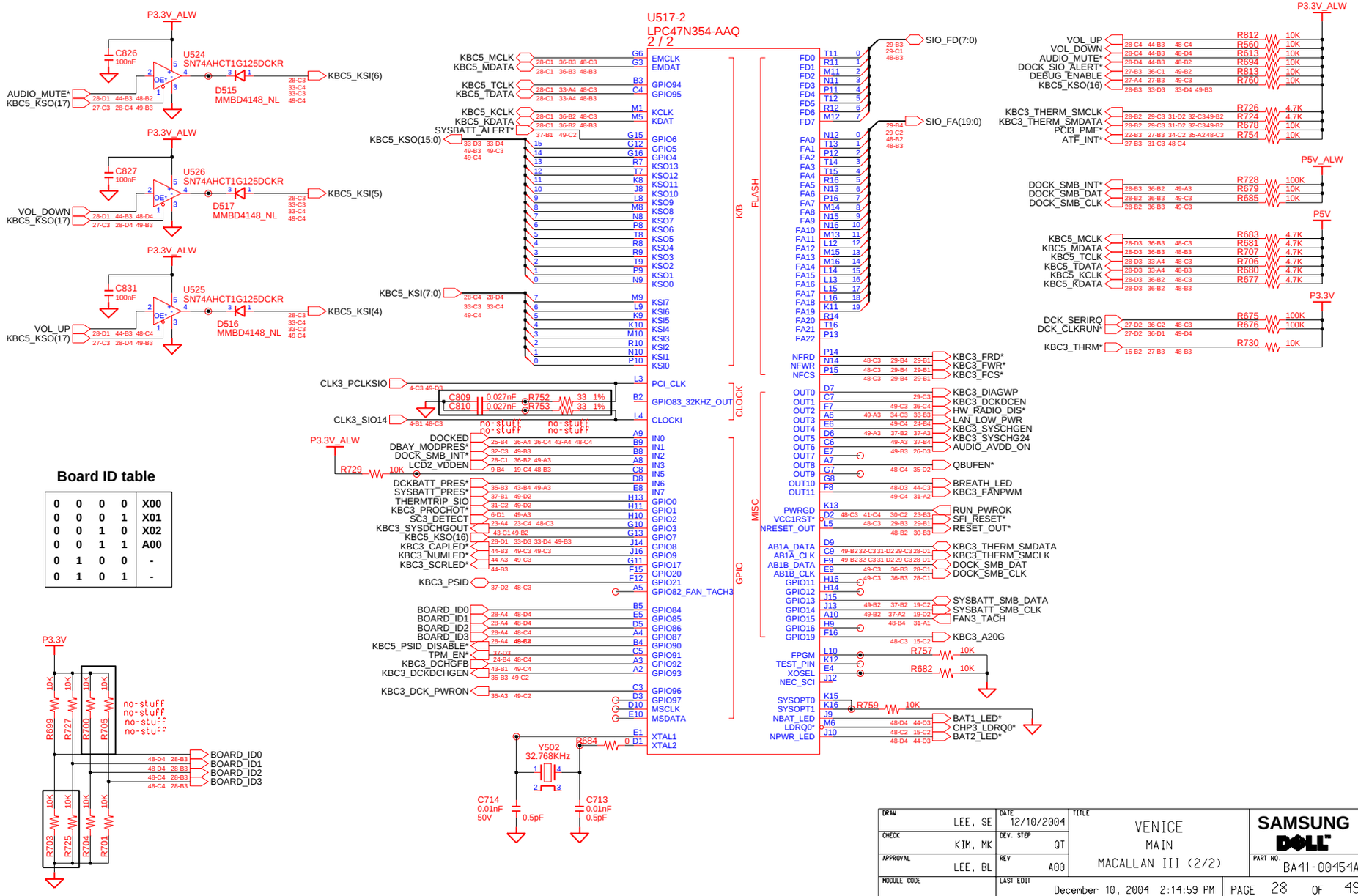
DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN AUDIO	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 26 OF 49	

Rev. No



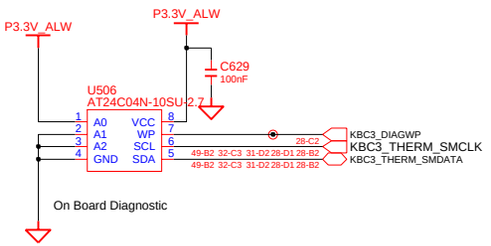
DRAW	LEE, SE	DATE 12/10/2004	TITLE VENICE MAIN MACALLAN III (1/2)
CHECK	KIM, MK	DEV. STEP QT	SAMSUNG DELL
APPROVAL	LEE, BL	REV A00	PART NO. BA41-00454A
MODULE CODE		LAST EDIT December 10, 2004 2:14:59 PM	PAGE 27 OF 49

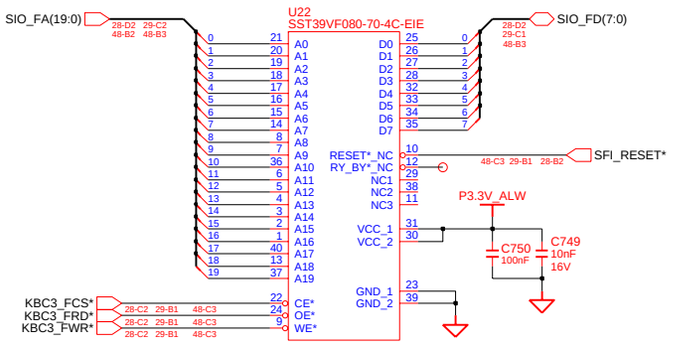
Rev. No

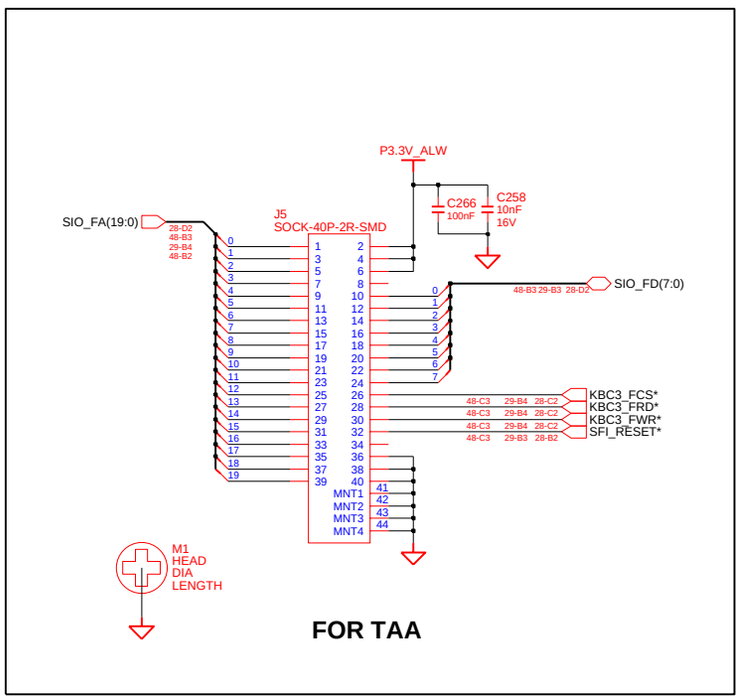


DRAW		DATE	TITLE	
	LEE, SE	12/10/2004	VENICE	SAMSUNG DELL
CHECK	KIM, MK	DEV. STEP	MAIN	
APPROVAL	LEE, BL	REV A00	MACALLAN III (2/2)	PART NO. BA41-00454A
MODULE CODE		LAST EDIT December 10, 2004 2:14:59 PM	PAGE 28 OF 49	

Rev. No





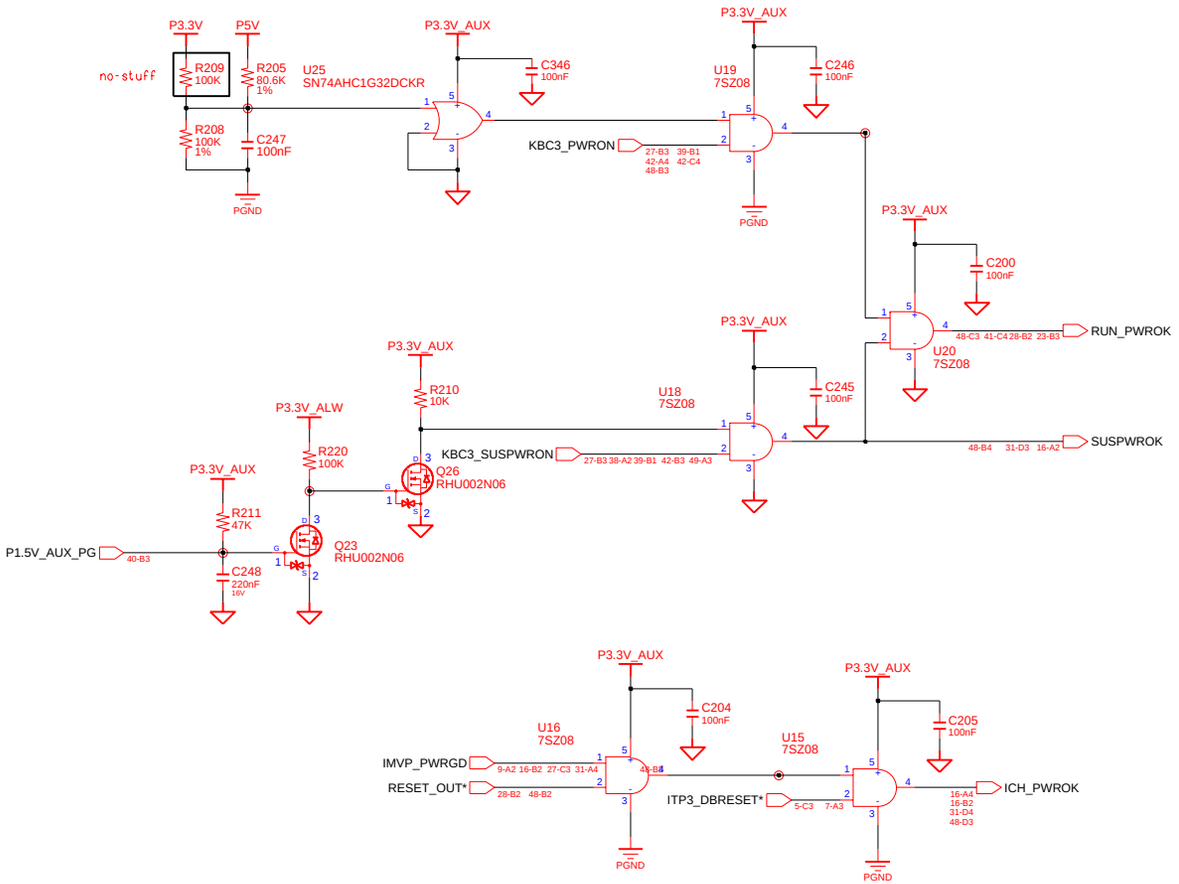


AMD : Pin 10 is RESET* ; Pin12 is RY/BY*
SST : Pin 10, 12 are NC.

1. **AMD-29LV081B require MAX 500ms Tready for it's hardware reset. And MAX6326_UR29 has > 100ms reset timing. So we can tie it's reset* pin to +3VALW directly.**
2. **SIO has internal 20ms dela of VCC1_p\PWROK.**

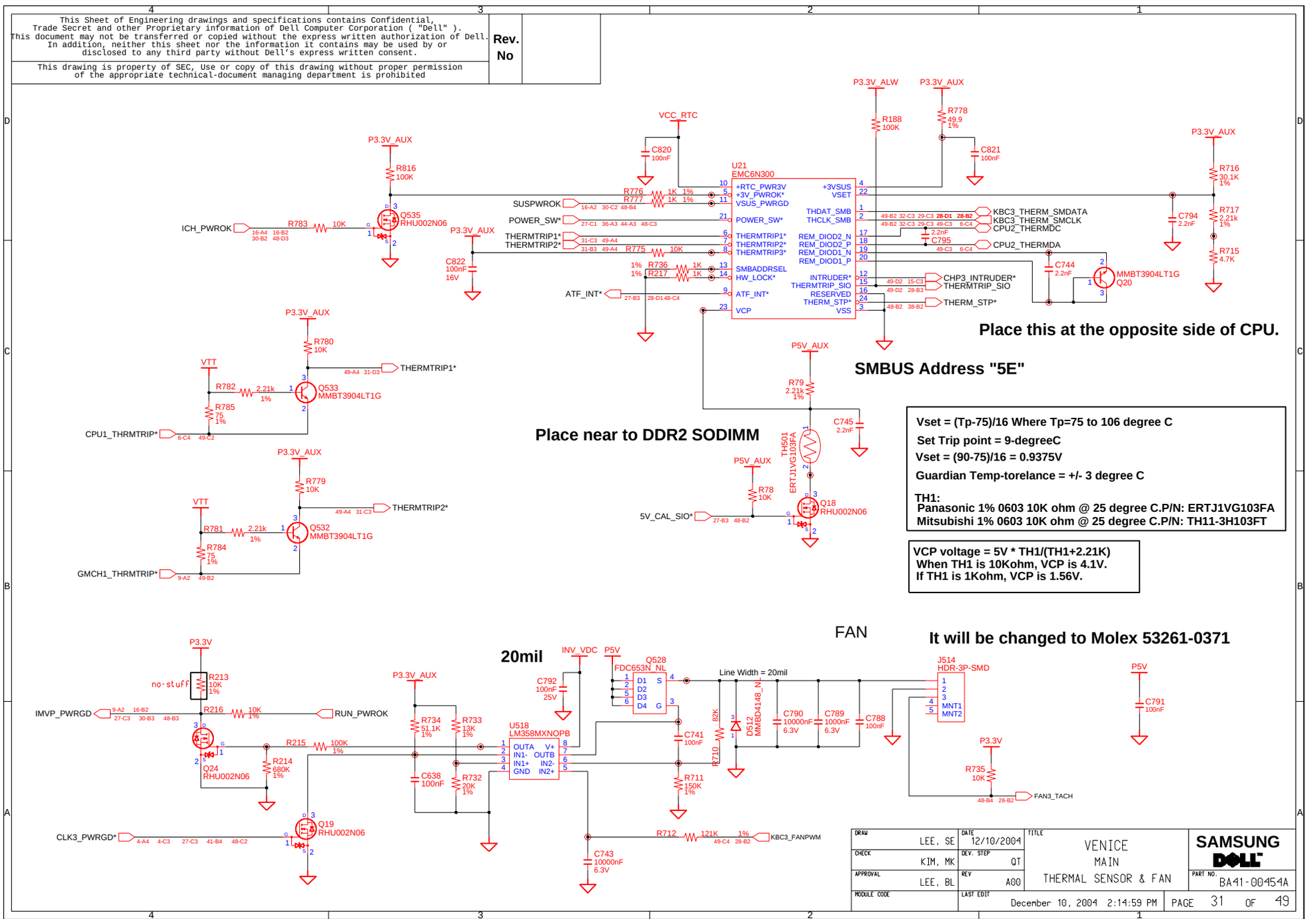
DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN Firmware&Onb'd Diagnostic	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		
APPROVAL: LEE, BL	REV: A00		PART NO.: BA41-00454A
MODULE CODE: undefined	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 29 OF 49	

Rev. No	



DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN SEQUENTIAL POWER	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 30 OF 49	

Rev. No



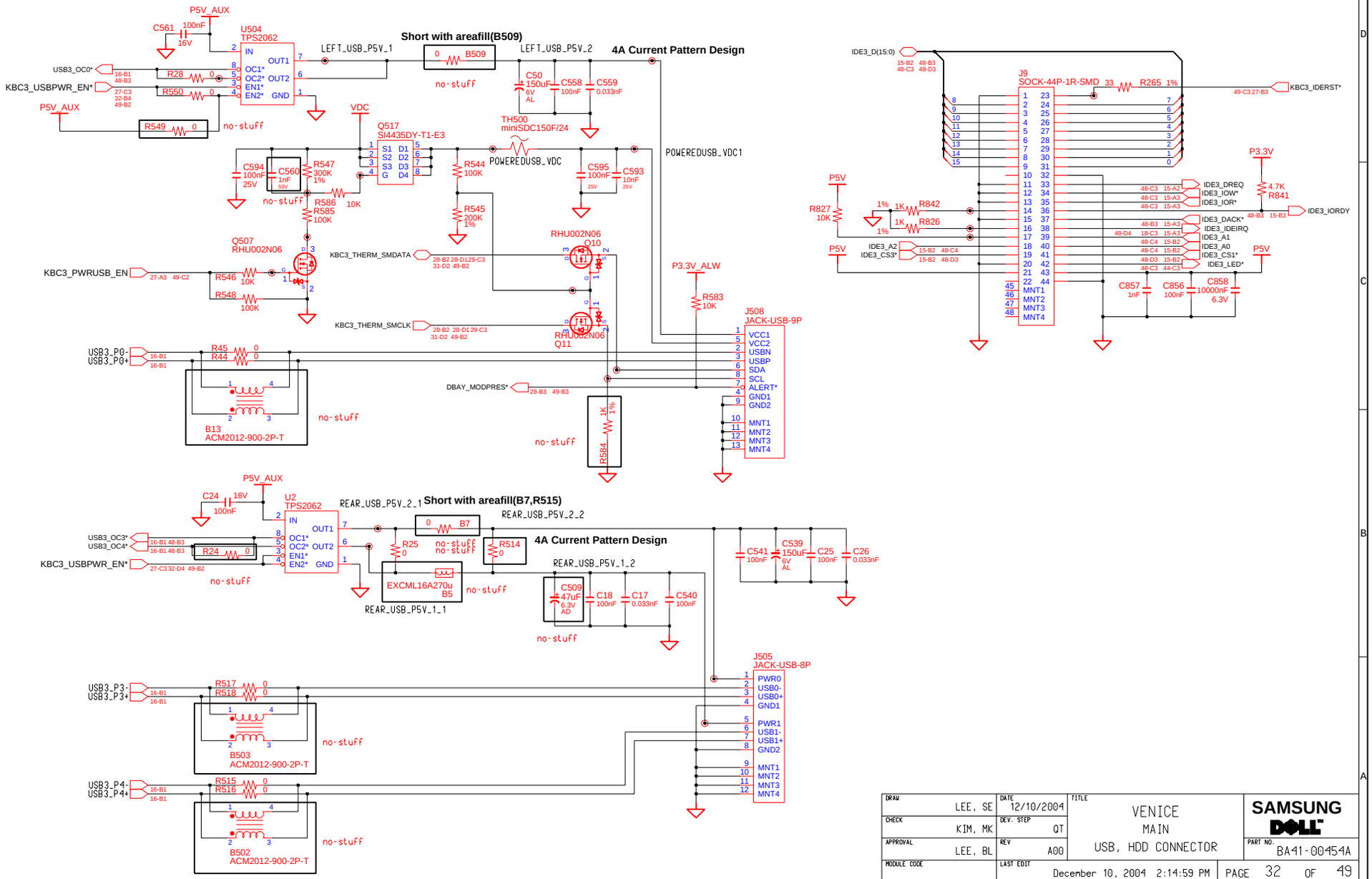
DRAW	LEE, SE	DATE	12/10/2004
CHECK	KIM, MK	DEV. STEP	QT
APPROVAL	LEE, BL	REV	A00
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM

TITLE: VENICE MAIN THERMAL SENSOR & FAN

SAMSUNG DELL

PART NO. BA41-00454A

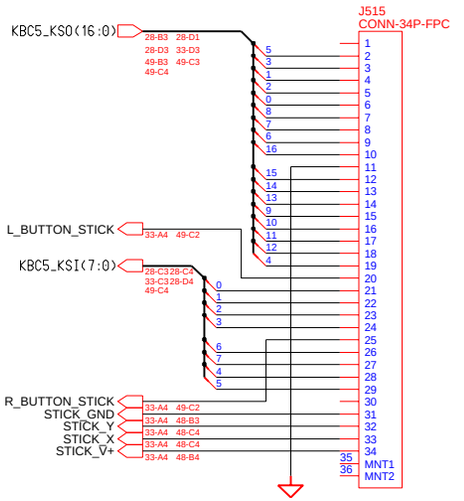
Rev. No	

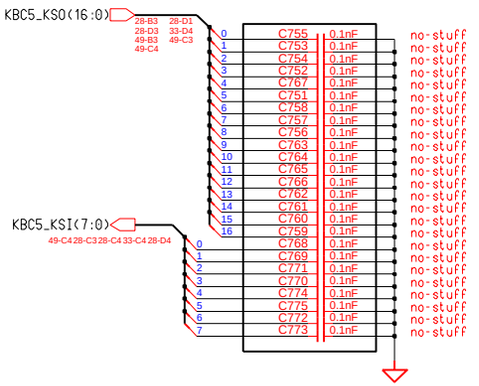


DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN USB, HDD CONNECTOR	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 32 OF 49	

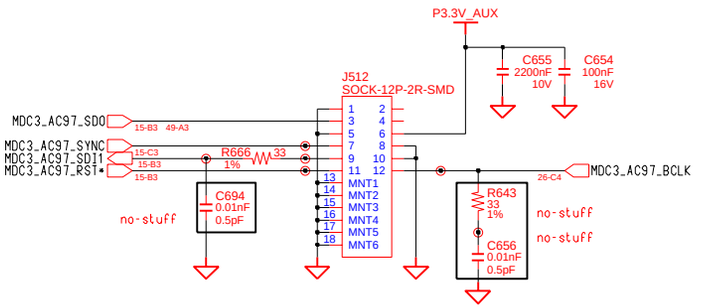
Rev. No

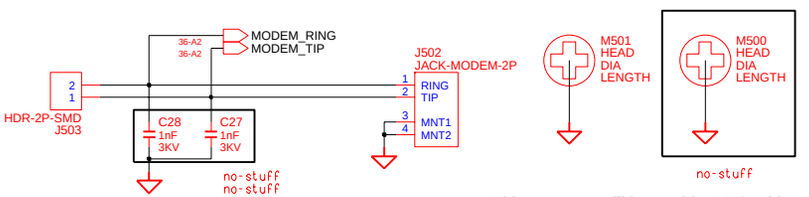
KEYBOARD





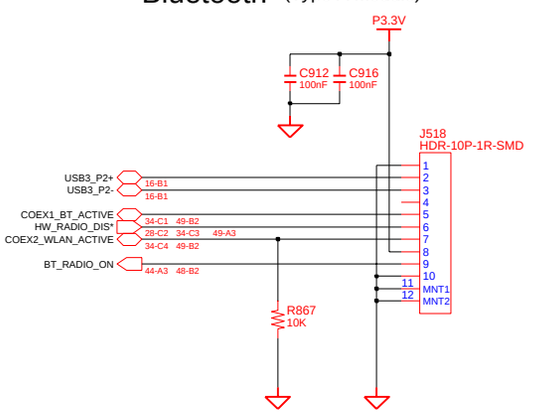
MDC connector



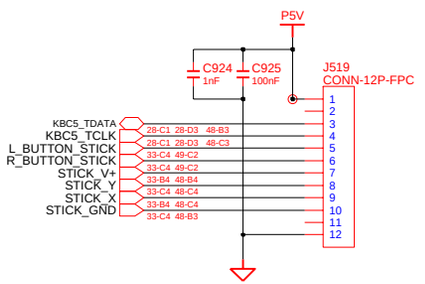


This supporter will be used for MDC cable.

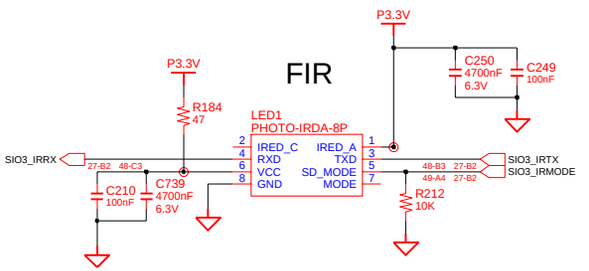
Bluetooth (Type A Module)



TOUCHPAD IF BD



FIR

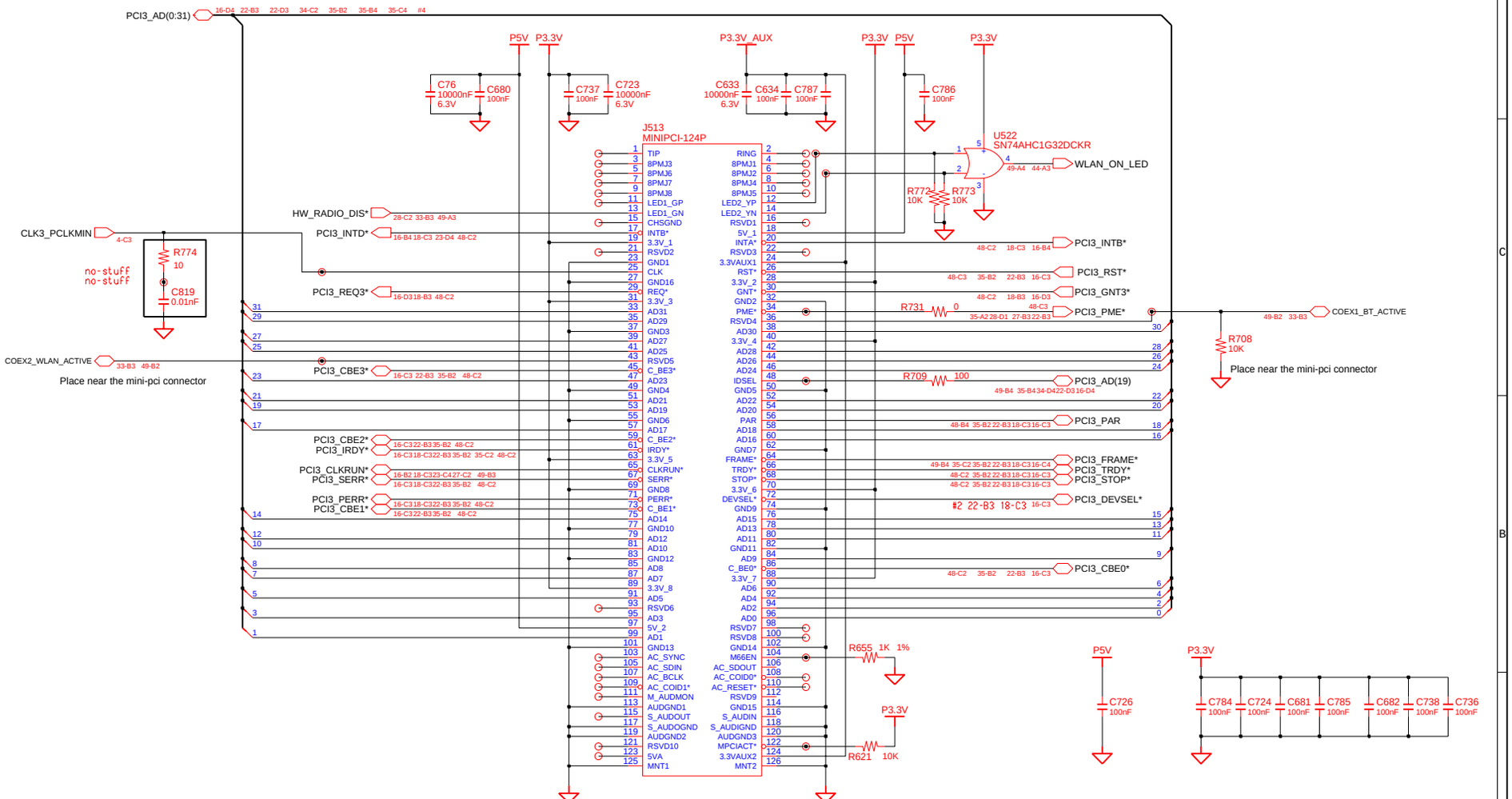


DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN KEYBOARD,TOUCHPAD,MDC,FIR	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 33 OF 49	

Rev. No

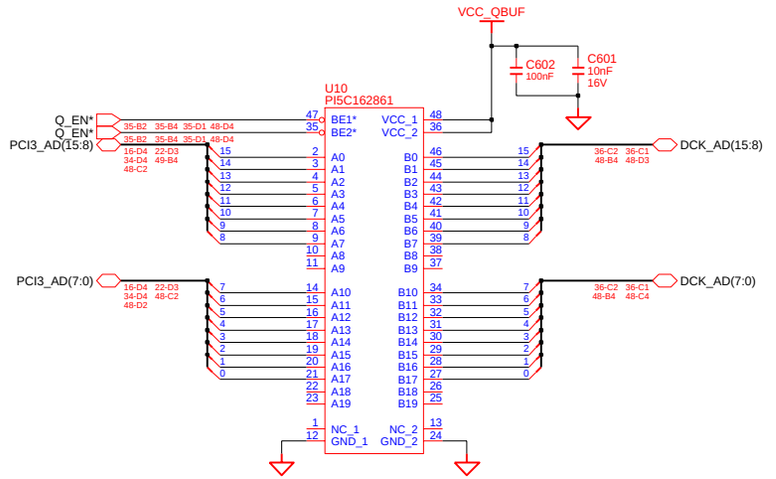
MINIPCI

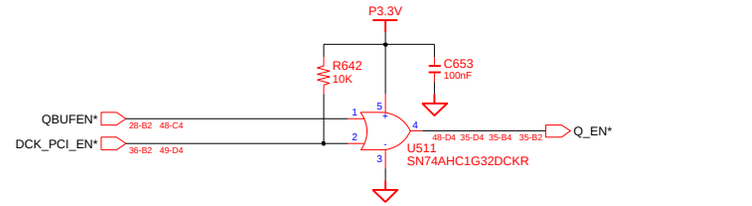
No Wake On Wireless LAN

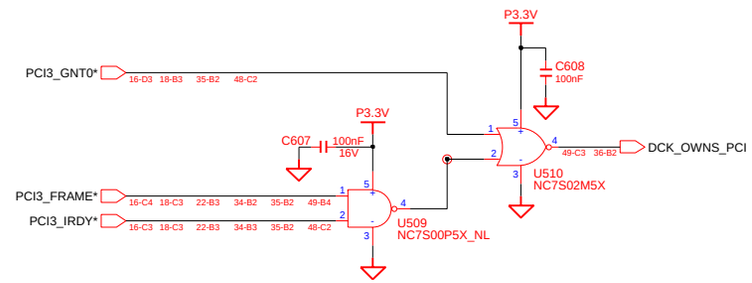


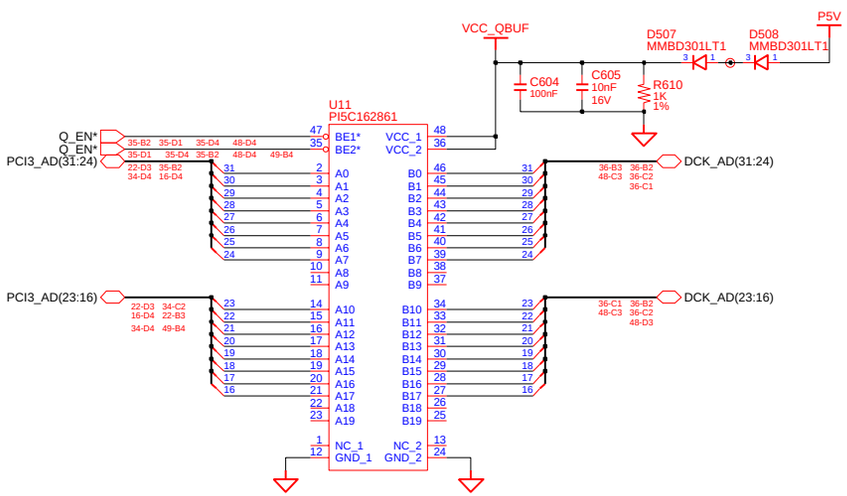
DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN MINI-PCI	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 34 OF 49	

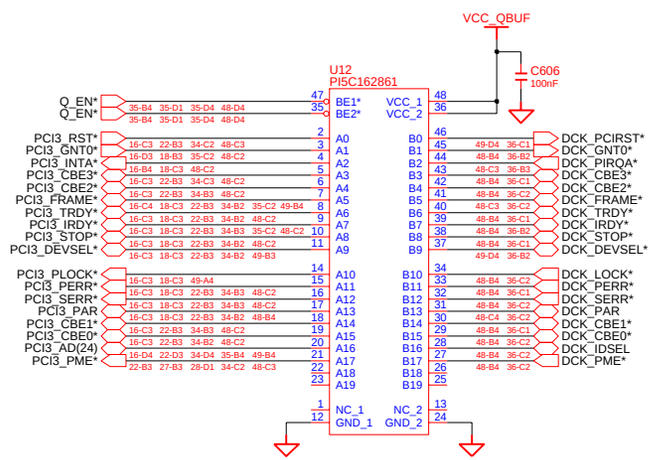
Rev. No	











DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN QUICK SWITCH	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 35 OF 49	

Rev. No

DVI TERMINATION

J1-1 SOCK-DOCKING-280P 1 / 2

J1-2 SOCK-DOCKING-280P 2 / 2

DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN DOCKING CONNECTOR	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 36 OF 49	

Rev. No

"Charge Current & Voltage Setting."

		3S2P/3S3P
KBC3_SYSCHG24	HI (2400)	3.78A
	LO (2600)	4.17A
VCHG		12.94V

Ilimit = (Vcls/Vref)*(0.075/Rsense1)
= 3.0A

ICHG=4.2A(MAX)
VCHG=12.94V
ICHG=4.2A
R1=68KOHM
R2=613KOHM

ICHG=3.8A
R1=680KOHM
R2=513KOHM

CHARGE CURRENT RATING
FAST_CHARGE:4.2A

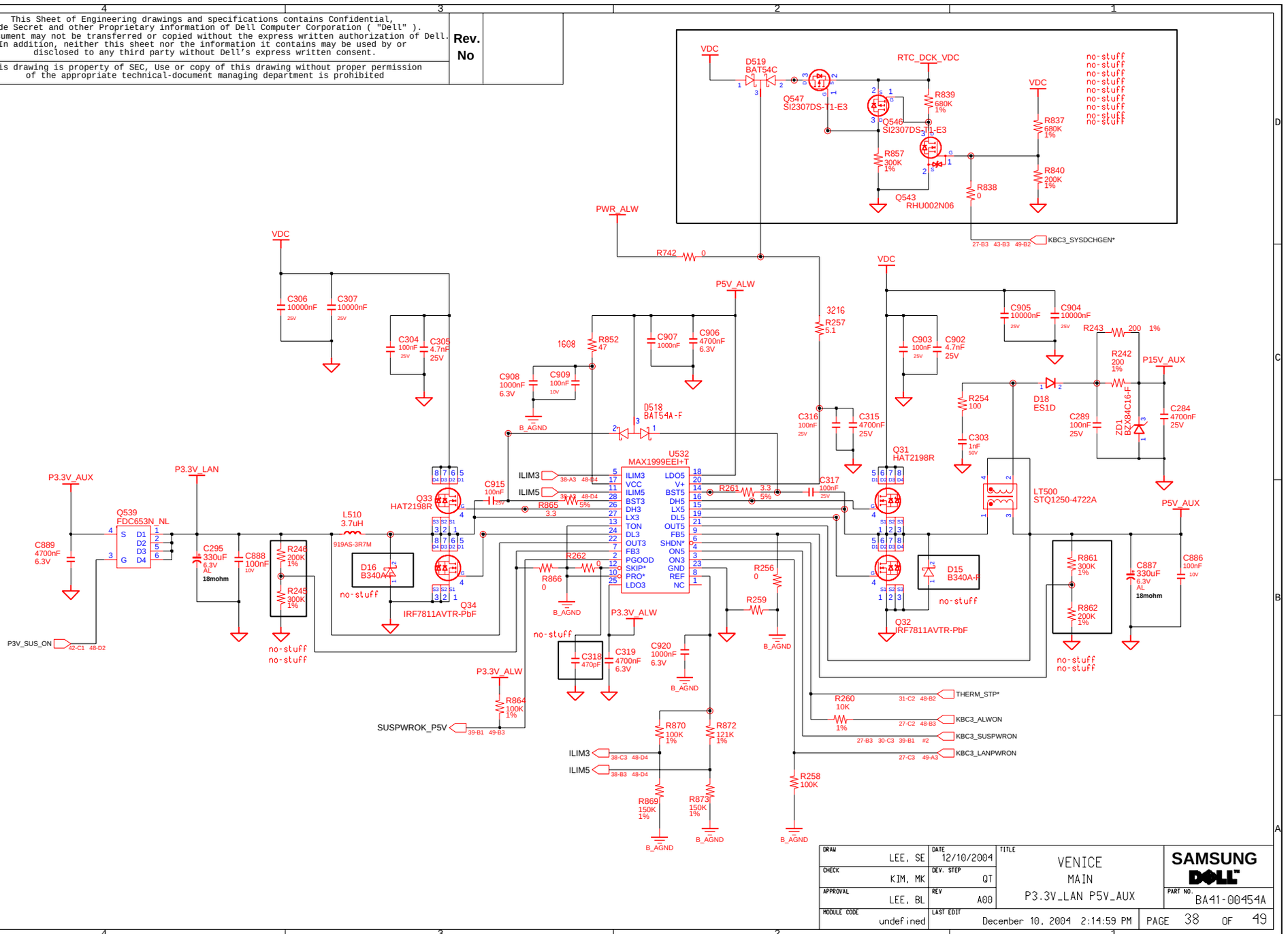
DRAW	LEE, SE	DATE	12/10/2004
CHECK	KIM, MK	DEV. STEP	QT
APPROVAL	LEE, BL	REV	A00
MODULE CODE	undefined	LAST EDIT	December 10, 2004 2:14:59 PM

TITLE: VENICE MAIN CHARGER DC-IN JACK

SAMSUNG DELL

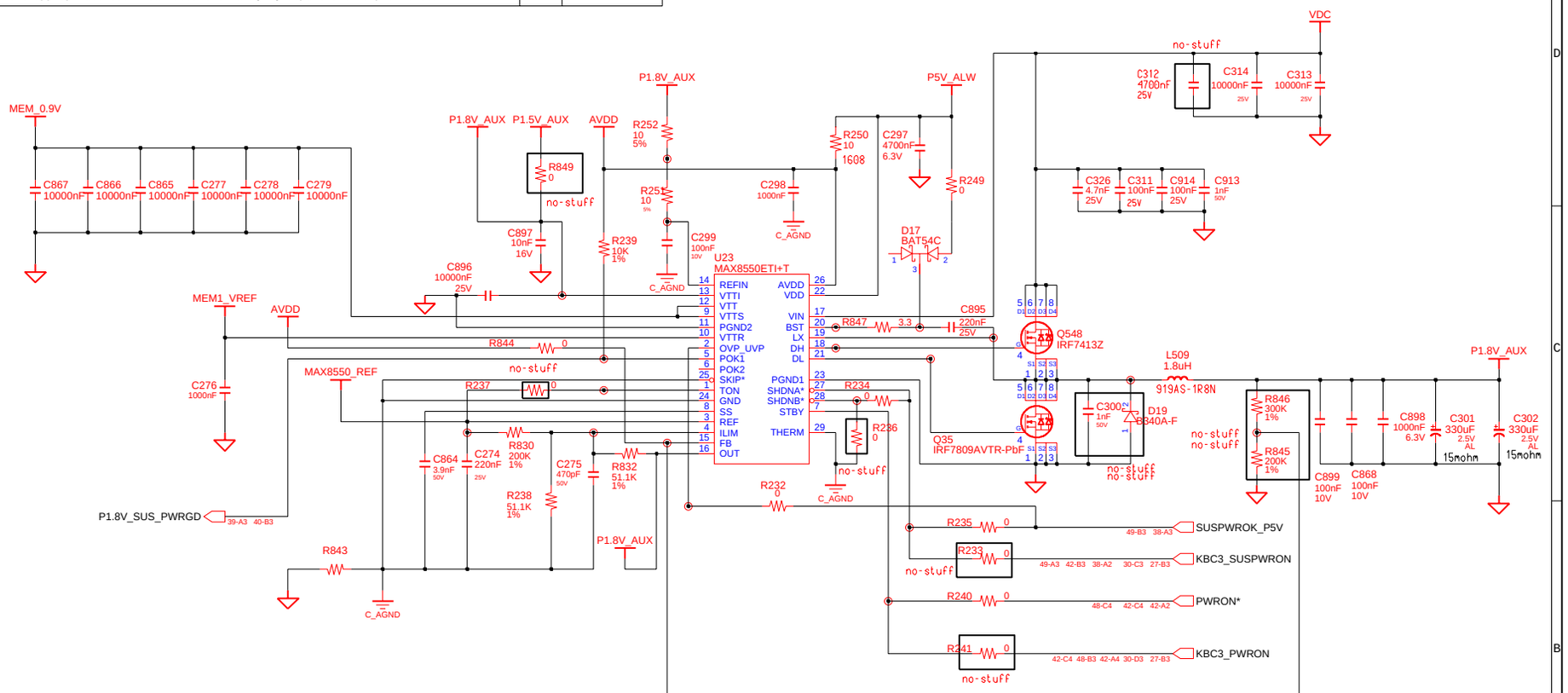
PART NO. BA41-00454A

Rev. No

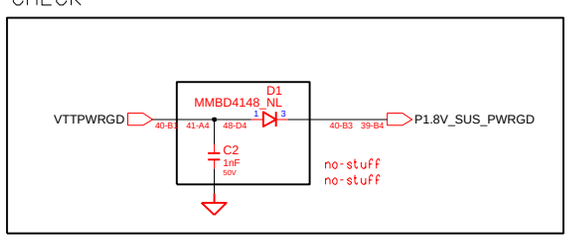


DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN P3.3V_LAN P5V_AUX	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE: undefined	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 38 OF 49	

Rev. No

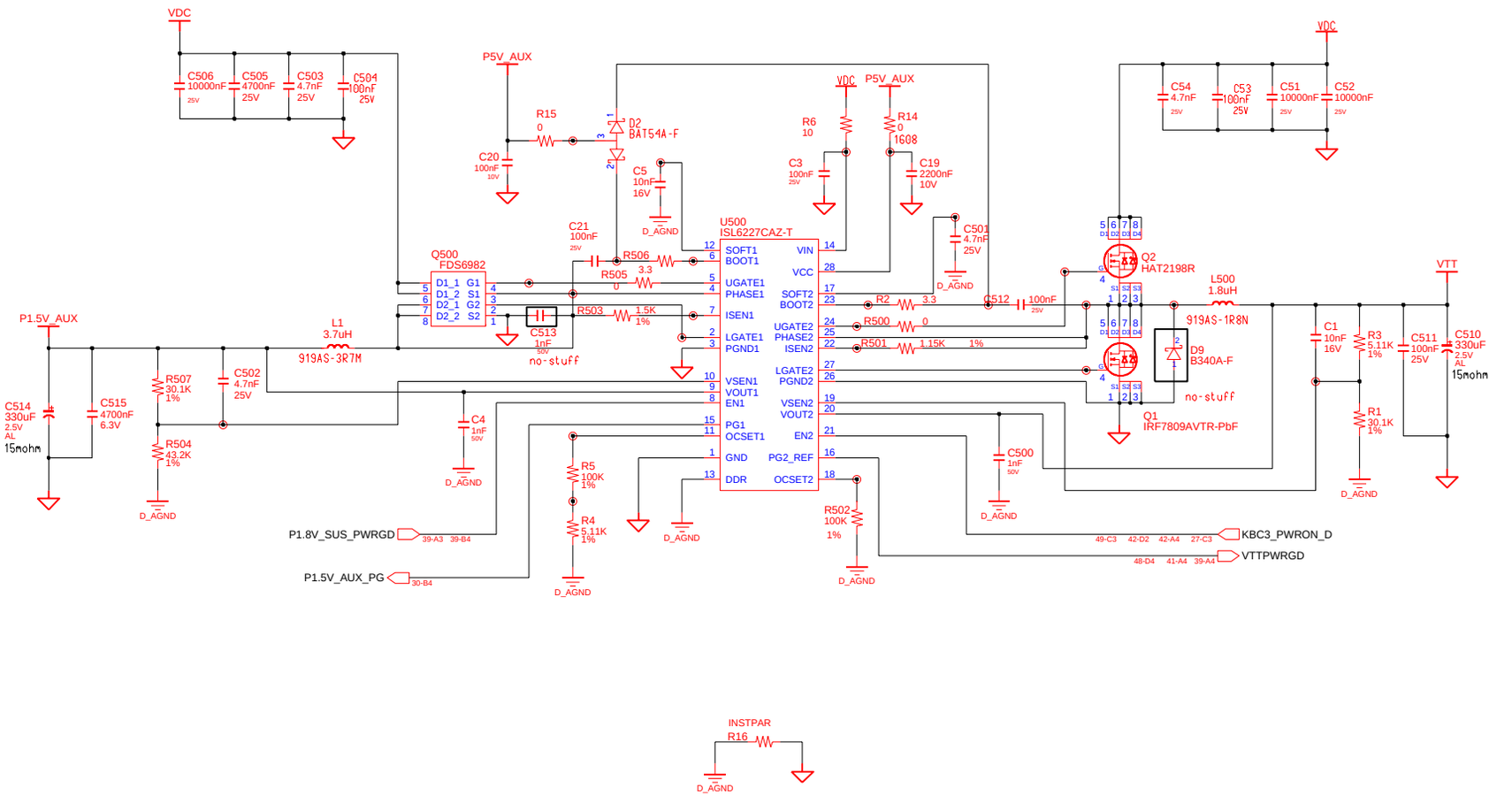


CHECK



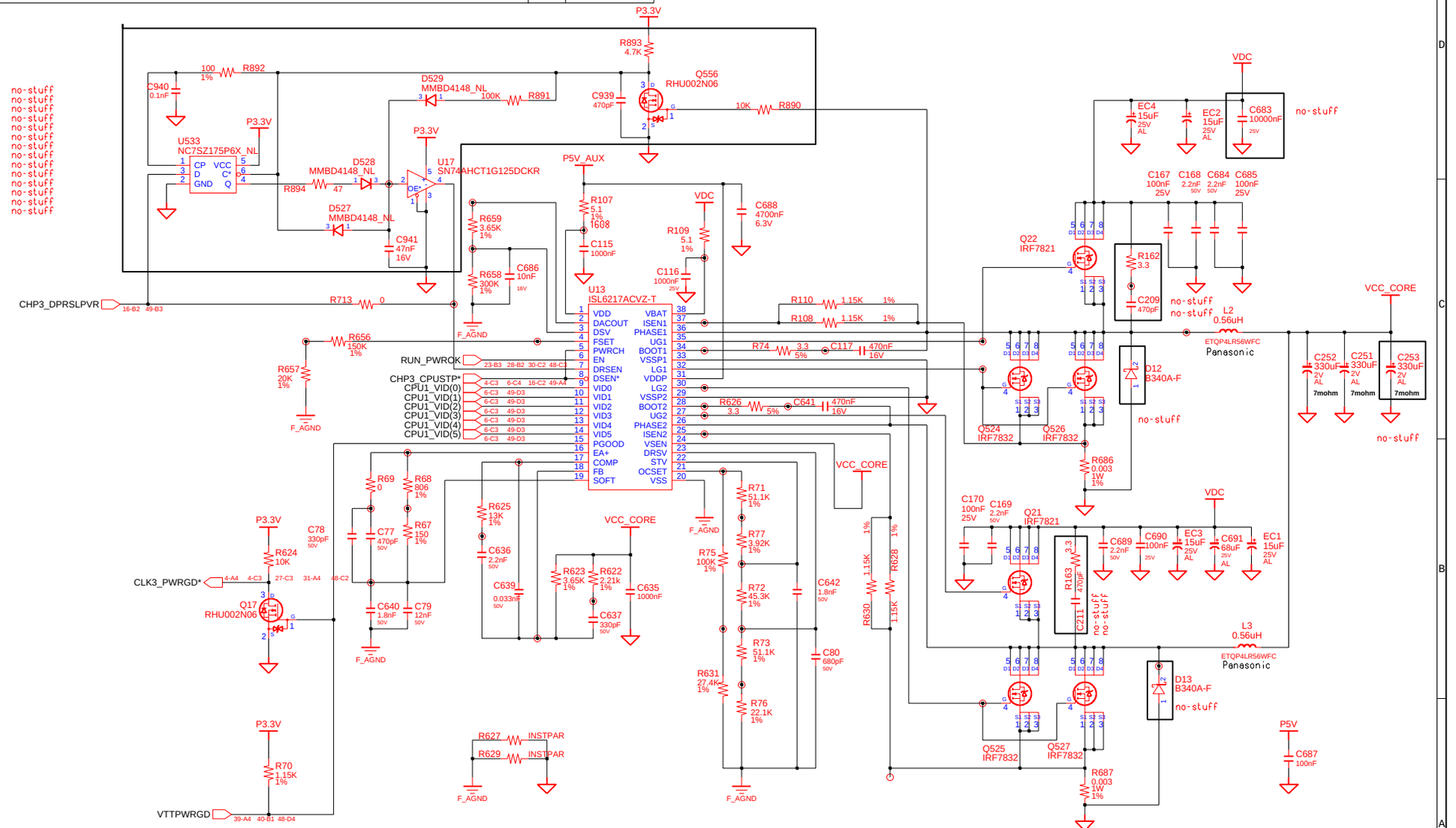
DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN P1.8V_AUX	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 39 OF 49	

Rev. No	



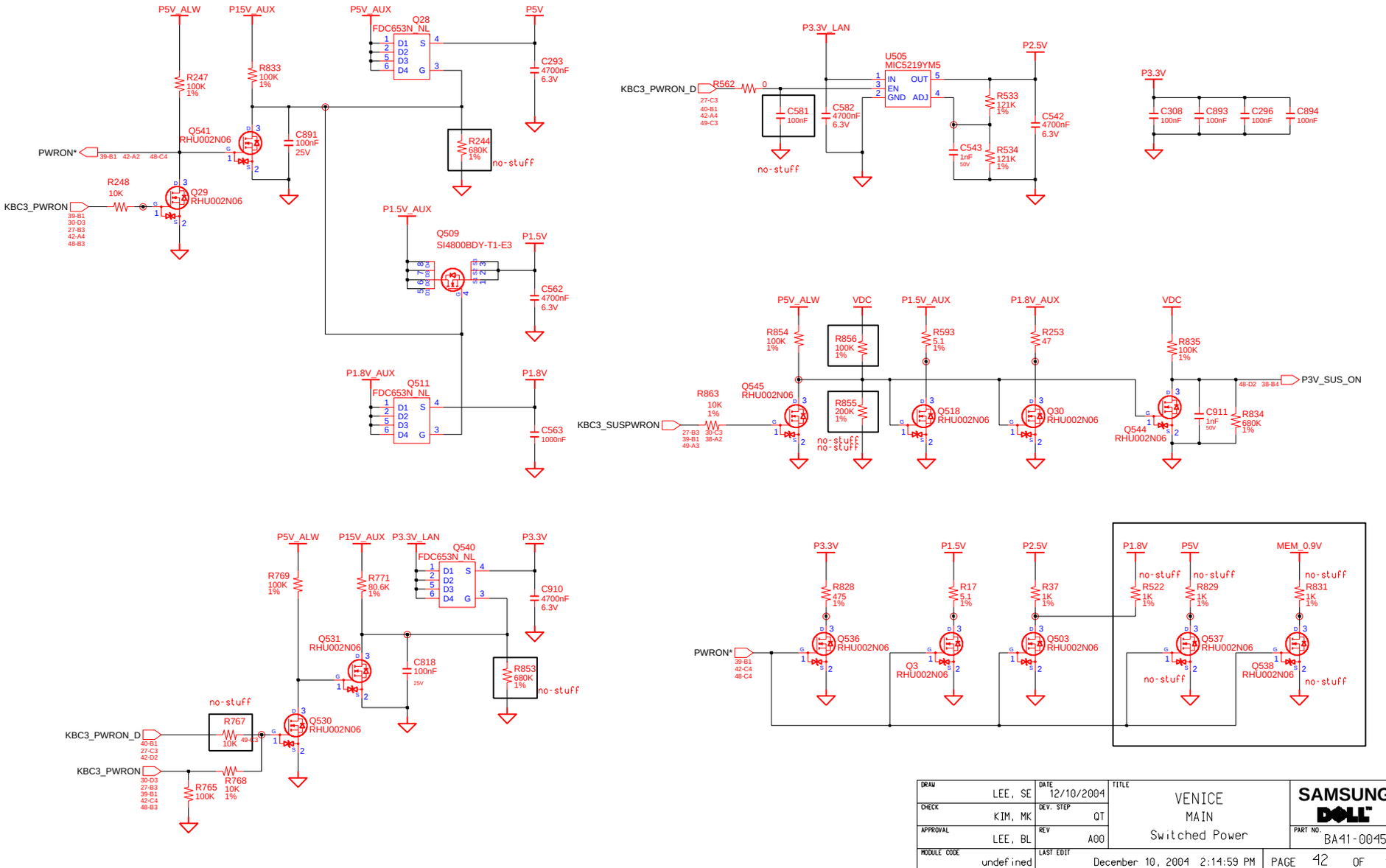
DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN VTT/P1.5V_AUX	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE: undefined	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 40 OF 49	

Rev. No



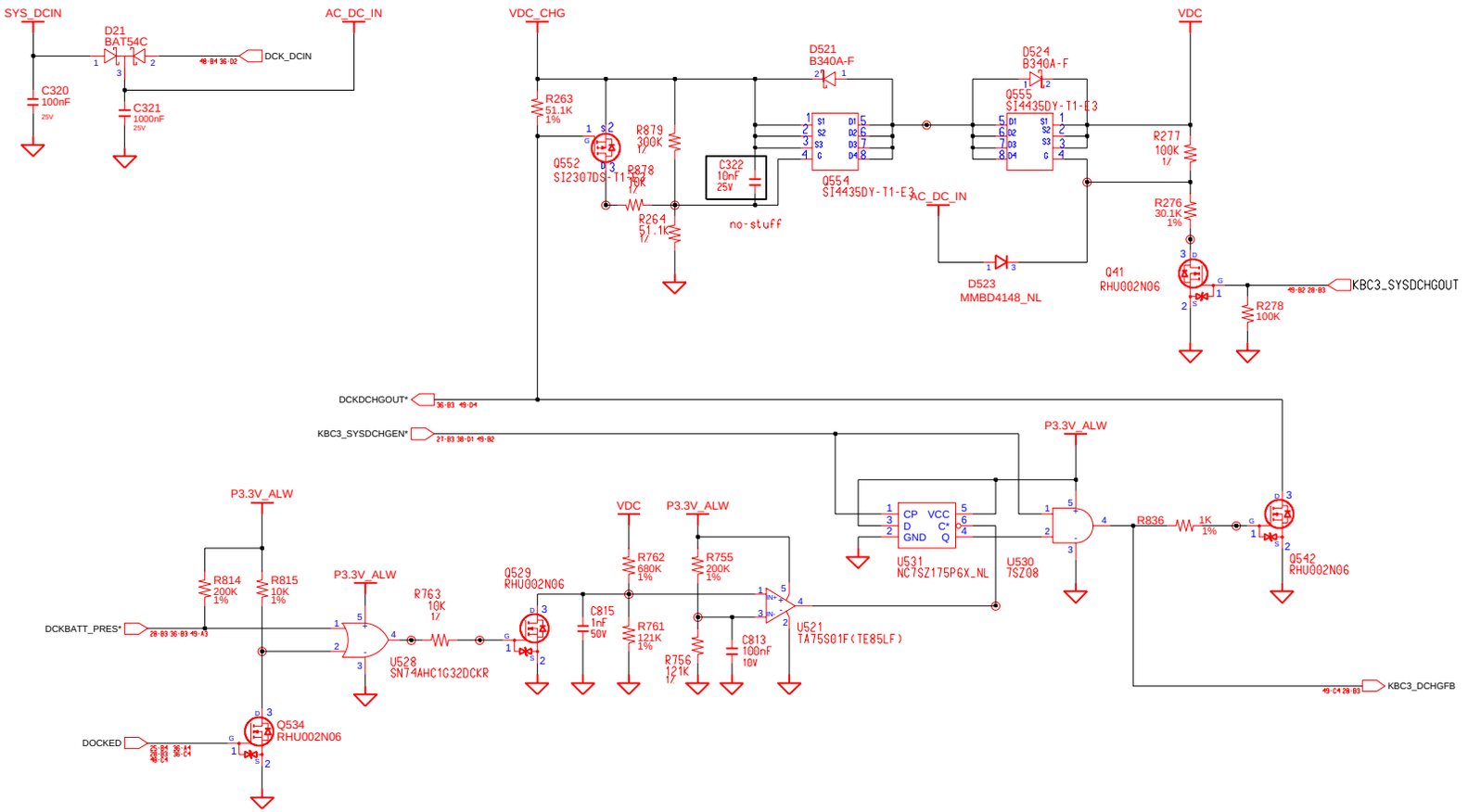
DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN VCC_CORE	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 41 OF 49	

Rev. No



DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN Switched Power	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE: undefined	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 42 OF 49	

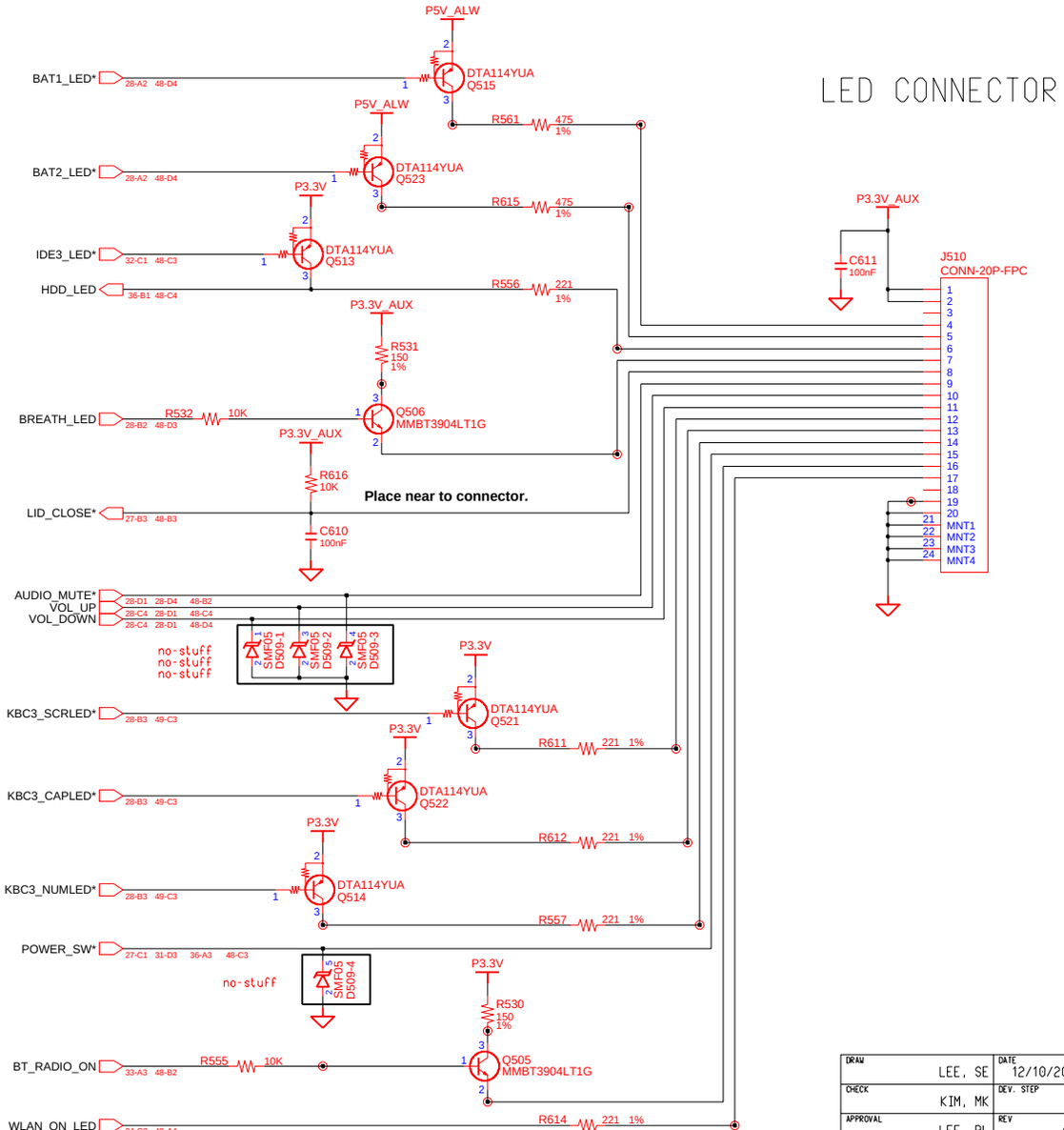
Rev. No	



DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN Sequential Changing	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE: undefined	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 43 OF 49	

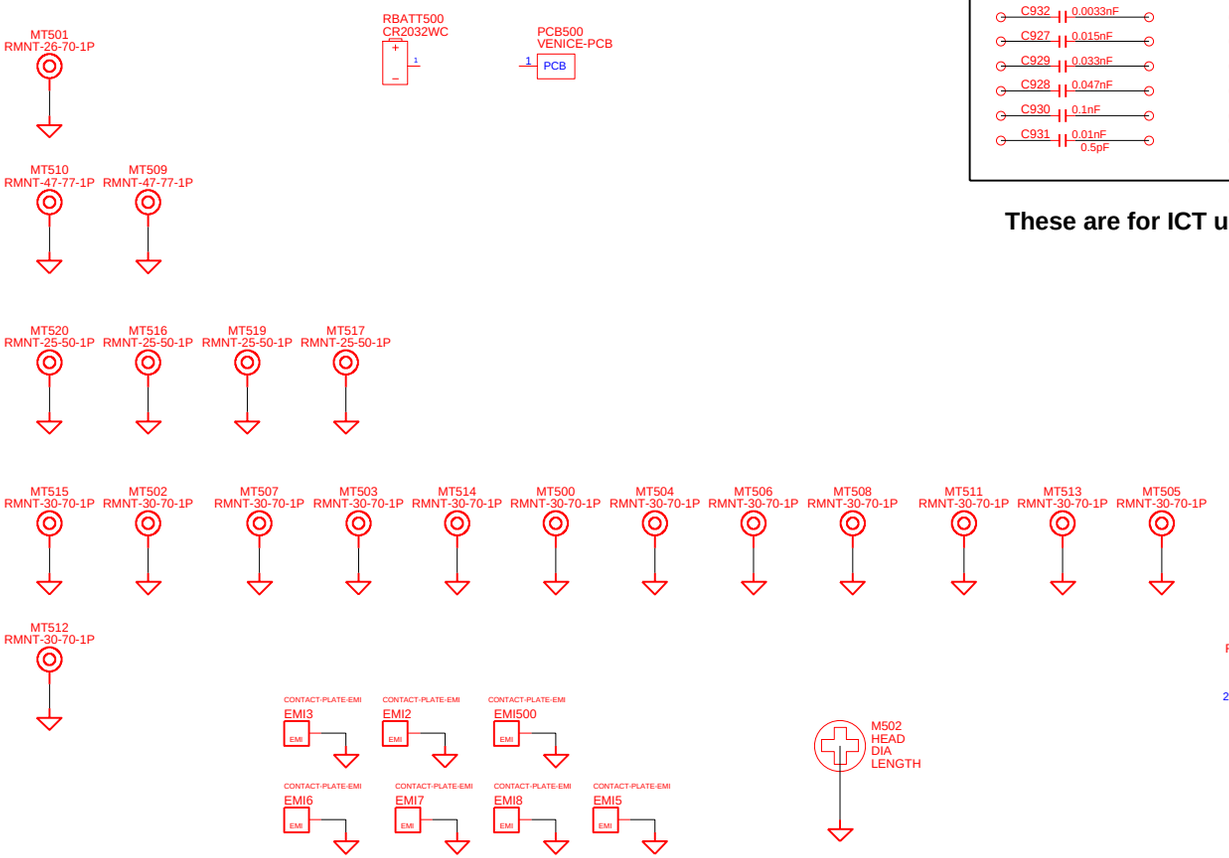
Rev. No

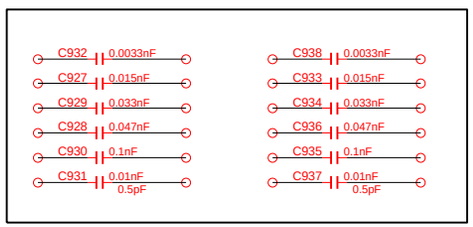
LED CONNECTOR



DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN LED Connector	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE: undefined	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 44 OF 49	

Rev. No	





These are for ICT using.

PCB REVISION CONTROL (ICT)

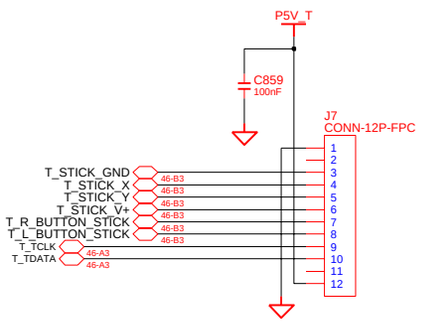
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.	04/04/02	0.1	X00
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	LEE, SE	DATE	12/10/2004	TITLE: VENICE MAIN MOUNT HOLE
CHECK	KIM, MK	DEV. STEP	QT	SAMSUNG DELL
APPROVAL	LEE, BL	REV	A00	PART NO. BA41-00454A
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE 45 OF 49

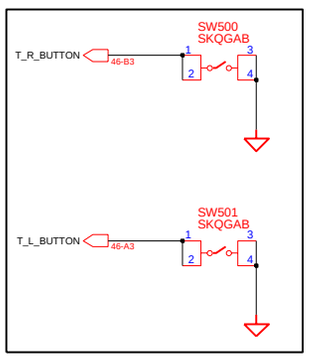
Rev. No	

TOUCHPAD IF BOARD

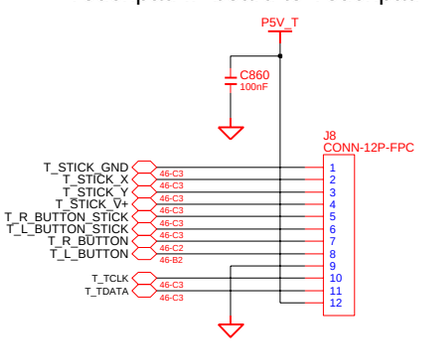
Main to Touchpad IF board



Place on Top side



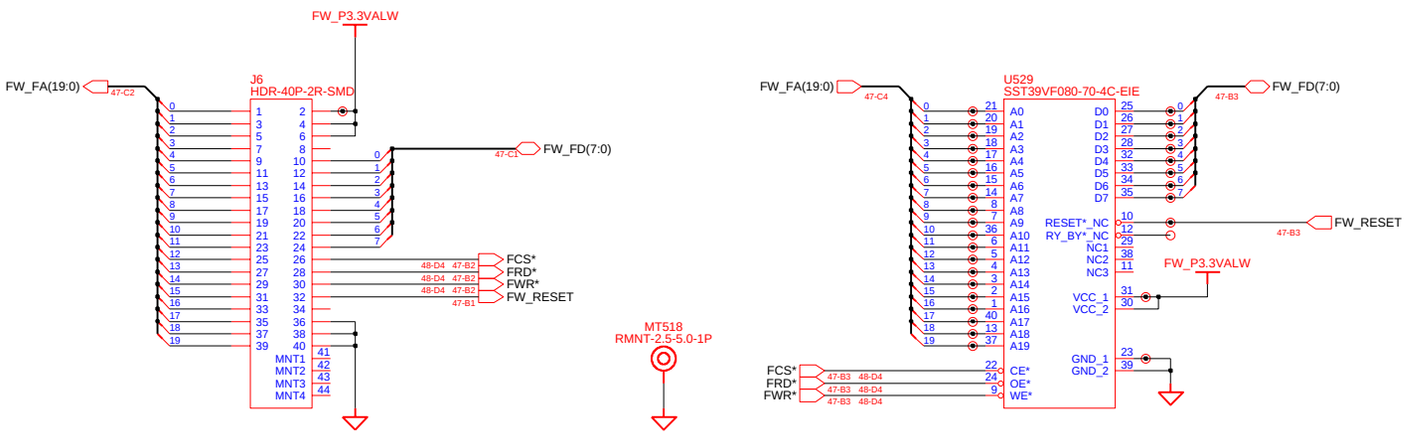
Touchpad IF board to Touchpad



DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN TOUCHPAD IF BOARD	SAMSUNG DELL		
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A		
APPROVAL: LEE, BL	REV: A00				
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM		PAGE 46 OF 49		

Rev. No

Firm Ware Daughter Board



AMD : Pin 10 is RESET* ; Pin12 is RY/BY*
SST : Pin 10, 12 are NC.

DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN Firmware DAUGHTER BOARD	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE: undefined	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 47 OF 49	

Rev. No	

- FCS•
- FRD•
- FWR•
- HP_IN
- ILIM3
- ILIM5
- Q_EN•
- CB3_D2
- DOCKED
- PWRON•
- SC3_CLK
- SC3_FCB
- SC3_RFU
- SC3_RST

- VOL_UP
- CB3_A18
- CB3_A19
- CB3_D14
- DCK_PAR
- HDD_LED
- IDE3_A0
- IDE3_A1
- IDE3_A2
- NB_MUTE
- QBUFEN•
- SC3_DATA
- STICK_X
- STICK_Y
- TPM_EN•

- USB_EN•
- ATF_INT•
- CB3_CCLK
- CB3_CPAR
- CB3_CVS1
- CB3_CVS2
- CB3_DATA
- CB3_SPKR
- CPU1_NMI
- DCK_DCIN
- DCK_PME•
- HP_OUT_L
- HP_OUT_R

- LCD_TEST
- PCI3_PAR

- SMB3_CLK
- STICK_V+
- SUSPWROK
- TV03_C_R
- TV03_Y_G

- VOL_DOWN
- VTTPWRGD
- AUD3_EAPD
- AUD3_SPKR
- BAT1_LED•
- BAT2_LED•
- BOARD_ID0
- BOARD_ID1
- BOARD_ID2
- BOARD_ID3
- CB3_CCD1•
- CB3_CCD2•
- CB3_CGNT•
- CB3_CINT•
- CB3_CLOCK
- CB3_CREQ•
- CB3_CRST•
- CB3_LATCH
- CHP3_PME•
- CHP3_SPKR
- CLK3_CB48
- CPU1_ADS•
- CPU1_BNR•
- CPU1_HIT•
- CPU1_INTR
- CPU1_RS0•
- CPU1_RST•
- CPU1_RS2•
- CPU1_SLP•
- CPU1_SMI•
- DCK_AD(0)
- DCK_AD(1)
- DCK_AD(2)
- DCK_AD(3)
- DCK_AD(4)
- DCK_AD(5)
- DCK_AD(6)
- DCK_AD(7)
- DCK_AD(8)
- DCK_AD(9)
- DCK_CBE0•
- DCK_CBE1•
- DCK_CBE2•
- DCK_CBE3•
- DCK_GNT0•
- DCK_IDSEL
- DCK_IRDY•
- DCK_LOCK•
- DCK_PERR•
- DCK_SERR•
- DCK_STOP•
- DCK_TRDY•
- DEBUG_OUT
- DOCK_DET•
- DOCK_PSID
- DVI3_SCLK
- DVI3_SDAT
- FAN3_TACH

- ICH_PWROK
- IDE3_CS1•
- IDE3_CS3•
- IDE3_D(0)
- IDE3_D(1)
- IDE3_D(2)
- IDE3_D(3)
- IDE3_D(4)
- IDE3_D(5)
- IDE3_D(6)
- IDE3_D(7)
- IDE3_D(8)
- IDE3_D(9)
- IDE3_DREQ
- IDE3_IOR•
- IDE3_IOW•
- IDE3_LED•
- KBC3_A20G
- KBC3_FCS•
- KBC3_FRD•
- KBC3_FWR•
- KBC3_PSID
- KBC3_SPKR
- KBC5_KCLK
- KBC5_MCLK
- KBC5_TCLK

- PCI3_PME•
- PCI3_RST•
- PLT3_RST•
- POWER_SW•
- RUN_PWROK
- SC3_DETECT
- SFI_RESET•
- SIO3_IRRX
- SIO3_IRTX
- SIO_FA(0)
- SIO_FA(1)
- SIO_FA(2)
- SIO_FA(3)
- SIO_FA(4)
- SIO_FA(5)
- SIO_FA(6)
- SIO_FA(7)
- SIO_FA(8)
- SIO_FA(9)
- SIO_FD(0)
- SIO_FD(1)
- SIO_FD(2)
- SIO_FD(3)
- SIO_FD(4)
- SIO_FD(5)
- SIO_FD(6)
- SIO_FD(7)
- SMB3_DATA
- STICK_GND
- TV03_COMP

- USB3_OC0•
- USB3_OC3•
- USB3_OC4•

- ADAPTER_IN
- BREATH_LED
- CB3_CAD(0)
- CB3_CAD(1)
- CB3_CAD(2)
- CB3_CAD(3)
- CB3_CAD(4)
- CB3_CAD(5)
- CB3_CAD(6)
- CB3_CAD(7)
- CB3_CAD(8)
- CB3_CAD(9)
- CB3_CAUDIO
- CB3_CCBE0•
- CB3_CCBE1•
- CB3_CCBE2•
- CB3_CCBE3•
- CB3_CIRDY•
- CB3_CPERR•
- CB3_CSERR•
- CB3_CSTOP•
- CB3_CTRDY•

- CLK3_AUD14
- CLK3_ICH14
- CLK3_SIO14
- CLK3_SSCIN
- CLK3_USB48
- CPU1_A20M•
- CPU1_BPRI•
- CPU1_BREQ•
- CPU1_DB10•
- CPU1_DB11•
- CPU1_DB12•
- CPU1_DB13•
- CPU1_DBSY•
- CPU1_DPWR•
- CPU1_DRDY•
- CPU1_FERR•
- CPU1_HITM•
- CPU1_INIT•
- CPU1_LOCK•
- CPU1_TRDY•

- DCK_AD(10)
- DCK_AD(11)
- DCK_AD(12)
- DCK_AD(13)
- DCK_AD(14)
- DCK_AD(15)
- DCK_AD(16)
- DCK_AD(17)
- DCK_AD(18)
- DCK_AD(19)
- DCK_AD(20)
- DCK_AD(21)
- DCK_AD(22)
- DCK_AD(23)
- DCK_AD(24)
- DCK_AD(25)
- DCK_AD(26)
- DCK_AD(27)

- DCK_AD(30)
- DCK_AD(31)
- DCK_FRAME•
- DCK_LAD(0)
- DCK_LAD(1)
- DCK_LAD(2)
- DCK_LAD(3)
- DCK_PIRQA•
- DCK_SERIRQ
- DOCK_DET1•

- IDE3_D(10)
- IDE3_D(11)
- IDE3_D(12)
- IDE3_D(13)
- IDE3_D(14)
- IDE3_D(15)
- IDE3_DACK•
- IDE3_IORDY
- IMVP_PWRGD
- KBC3_ALWON
- KBC3_PWRON
- KBC3_THRM•
- KBC5_KDATA
- KBC5_MDATA
- KBC5_TDATA

- LCD2_VDDEN
- LID_CLOSE•

- LINE_OUT_L
- LINE_OUT_R

- P3V_SUS_ON
- PCI3_AD(0)
- PCI3_AD(1)
- PCI3_AD(2)
- PCI3_AD(3)
- PCI3_AD(4)
- PCI3_AD(5)
- PCI3_AD(6)
- PCI3_AD(7)
- PCI3_AD(8)
- PCI3_AD(9)
- PCI3_CBE0•
- PCI3_CBE1•
- PCI3_CBE2•
- PCI3_CBE3•
- PCI3_GNT0•
- PCI3_GNT1•
- PCI3_GNT3•
- PCI3_INTA•
- PCI3_INTB•
- PCI3_INTC•
- PCI3_INTD•
- PCI3_IRDY•
- PCI3_PERR•
- PCI3_REQ0•
- PCI3_REQ1•

- PCI3_REQ3•
- PCI3_SERR•
- PCI3_STOP•
- PCI3_TRDY•
- PLT3_RSTF•
- REFCLK_SEL
- RESET_OUT•
- SIO_FA(10)
- SIO_FA(11)
- SIO_FA(12)
- SIO_FA(13)
- SIO_FA(14)
- SIO_FA(15)
- SIO_FA(16)
- SIO_FA(17)
- SIO_FA(18)
- SIO_FA(19)
- SOUND_MUTE•
- SPDIF_SHDN
- THERM_STP•

- VGA3_HSYNC
- VGA3_VSYNC
- 5V_CAL_SIO•
- AUDIO_MUTE•
- BT_RADIO_ON
- CB3_CAD(10)
- CB3_CAD(11)
- CB3_CAD(12)
- CB3_CAD(13)
- CB3_CAD(14)
- CB3_CAD(15)
- CB3_CAD(16)
- CB3_CAD(17)
- CB3_CAD(18)
- CB3_CAD(19)
- CB3_CAD(20)
- CB3_CAD(21)

- CB3_CAD(22)
- CB3_CAD(23)
- CB3_CAD(24)
- CB3_CAD(25)
- CB3_CAD(26)
- CB3_CAD(27)
- CB3_CAD(28)
- CB3_CAD(29)
- CB3_CAD(30)
- CB3_CAD(31)
- CB3_CFRAME•
- CB3_CSTSCHG
- CHP3_LDRQ0•
- CHP3_LDRQ1•
- CHP3_SERIRQ
- CHP3_SLPS3•
- CHP3_SLPS5•

- CLK3_PCLKCB
- CLK3_PWRGD•
- CLK3_SMBCLK

DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN TEST POINT	SAMSUNG / DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 48 OF 49	

Rev. No	

DCKDCHGOUT•
DCK_ACTIVE•
DCK_CLKRUN•
DCK_DEVSEL•
DCK_DLDRQ1•
DCK_LFRAME•
DCK_LINK10•
DCK_PCIRST•
DCK_PCI_EN•
DVI3_DETECT

IDE3_IDEIRQ

KBC3_BKLTON
KBC3_DCHGFB
KBC3_FANPWM
KBC5_KSI(0)
KBC5_KSI(1)
KBC5_KSI(2)
KBC5_KSI(3)
KBC5_KSI(4)
KBC5_KSI(5)
KBC5_KSI(6)
KBC5_KSI(7)

KBC5_KSO(1)
KBC5_KSO(2)
KBC5_KSO(3)
KBC5_KSO(4)
KBC5_KSO(5)
KBC5_KSO(6)
KBC5_KSO(7)
KBC5_KSO(8)
KBC5_KSO(9)

LAN_LOW_PWR

LCD2_BIAPWM
LCD2_BKLTON
LCD2_DDCCLK
LCD3_BKLTON
LPC3_LAD(0)
LPC3_LAD(1)
LPC3_LAD(2)
LPC3_LAD(3)
PCI3_AD(10)
PCI3_AD(11)
PCI3_AD(12)
PCI3_AD(13)
PCI3_AD(14)
PCI3_AD(15)
PCI3_AD(16)
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PCI3_AD(25)
PCI3_AD(26)
PCI3_AD(27)
PCI3_AD(28)
PCI3_AD(29)
PCI3_AD(30)
PCI3_AD(31)
PCI3_FRAME•
PCI3_PLOCK•
SIO3_IRMODE

THERMTRIP1•
THERMTRIP2•

VGA2_DDCCLK
WLAN_ON_LED
AUDIO3_SPDIF
CB3_CCLKRUN•
CB3_CDEVSEL•
CHP3_CPUSTP•
CHP3_PCISTP•
CHP3_RTCRST•

CPU1_DEFER•
CPU1_DPSLP•
CPU1_IGNNE•
CPU1_VID(0)
CPU1_VID(1)
CPU1_VID(2)
CPU1_VID(3)
CPU1_VID(4)
CPU1_VID(5)
CLK3_AUD14_1
CLK3_PCLKBCM
CLK3_PCLKSIO
CLK3_SMBDATA

CPU1_DPRSTP•
CPU1_STPCLK•
CPU2_THERMDA
CPU2_THERMDC
DCK_LINK100•
DCK_OWNS_PCI

DEBUG_ENABLE
DOCK_SMB_CLK
DOCK_SMB_DAT
DVO2_CTRLCLK
KBC3_CAPLED•
KBC3_DCKDCEN
KBC3_EXTSMI•
KBC3_IDERST•
KBC3_NUMLED•
KBC3_PWRBTN•
KBC3_PWRON_D
KBC3_RUNSCI•
KBC3_SCRLED•
KBC5_KSO(10)
KBC5_KSO(11)
KBC5_KSO(12)
KBC5_KSO(13)
KBC5_KSO(14)
KBC5_KSO(15)
KBC5_KSO(16)
KBC5_KSO(17)
LAN3_ACTIVE•
LAN3_LINK10•

LCD2_DDCDATA
LPC3_LFRAME•
MCH1_HXSWING
MCH1_HYSWING
MCH2_BMBUSY•
PCI3_CLKRUN•
PCI3_DEVSEL•
SUSPWROK_P5V

VGA2_DDCDATA
VGA3_RED_INT
AUD3_AC97_SDO
AUDIO_AVDD_ON
AUD_MIC_CODEC
CHP3_DPRSLPVR

CLK3_PCLKDOCK
CPU1_PROCHOT•
DBAY_MODPRES•
DCKBATT_PRES•

DOCK_SMB_INT•
DVO2_CTRLDATA
HW_RADIO_DIS•
KBC3_LANPWRON
KBC3_PROCHOT•
KBC3_SUSPWRON
KBC3_SYSCHG24
KBC3_SYSCHGEN
KBC3_WAKESCI•
LAN3_LINK100•
LCD3_CLK_EDID
LCD5_LAMPSTAT
MDC3_AC97_SDO

PCI3_CB_GRST•
SYSBATT_PRES•
THERMTRIP_SIO
VGA3_BLUE_INT
AUD3_AC97_BCLK
AUD3_AC97_RST•
AUD3_AC97_SDIO
AUD3_AC97_SYNC
CHP3_INTRUDER•

CLK3_PCLKICH6M
CPU1_THRMTRIP•

KBC3_DCKDCHGEN
KBC3_DCK_PWRON
KBC3_ICH6RCIN•
KBC3_PWRUSB_EN

LCD3_DATA_EDID
LOM_PCIE_WAKE•
L_BUTTON_STICK

R_BUTTON_STICK
SYSBATT_ALERT•
VGA3_GREEN_INT

COEX1_BT_ACTIVE
DOCK_SIO_ALERT•
GMCH1_THRMTRIP•
KBC3_BATSEL4_3•
KBC3_PCIE_WAKE•
KBC3_SYSDCHGEN•
KBC3_SYSDCHGOUT
KBC3_USBPWR_EN•

SYSBATT_SMB_CLK
KBC3_THERM_SMCLK
SYSBATT_SMB_DATA

COEX2_WLAN_ACTIVE
KBC3_THERM_SMDATA
KBC5_PSID_DISABLE•
AGND

AVDD

AVDD5

AC_DC_IN

AVDD3.3V

B_AGND

C_AGND

CB3_VCC

CB3_VPP

D_AGND

DOCK_PWR_SRC

DCK_P2.5V_LAN

F_AGND
INV_VDC
LCD_VDD3V
LDO_P5.4V
MEM_0.9V
MCH_P1.5V
MAX1909_REF
PGND
P1.5V

P1.8V

P2.5V

PWR_DC

P5V_ALW

P5V_AUX

P15V_AUX

P1.2V_LAN

P1.5V_AUX

P1.8V_AUX

P2.5V_LAN

P3.3V_ALW

P3.3V_AUX

P3.3V_LAN

RTC_DCK_VDC

RTC_PWR3.3V

SC3_VCC

SYS_DCIN

VDC

VTT

VCC_CRT

VCC_RTC

VDC_CHG

VCC_CORE

VCC_QBUF

DRAW: LEE, SE	DATE: 12/10/2004	TITLE: VENICE MAIN TEST POINT	SAMSUNG DELL
CHECK: KIM, MK	DEV. STEP: QT		PART NO.: BA41-00454A
APPROVAL: LEE, BL	REV: A00		
MODULE CODE:	LAST EDIT: December 10, 2004 2:14:59 PM	PAGE 49 OF 49	