Fonseca UMA Schematics Document

rPGA988A Mobile Arrandale

Intel Ibex Peak-M

2009-11-03

REV : X01

DY : Nopop Component
B_TPM:Use Lom TPM
C_TPM:Use China TPM

<Core Design>

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Title: *Cover Page*

Size: Custom | Document Number: *Fonseca UMA* | Rev: *X01*

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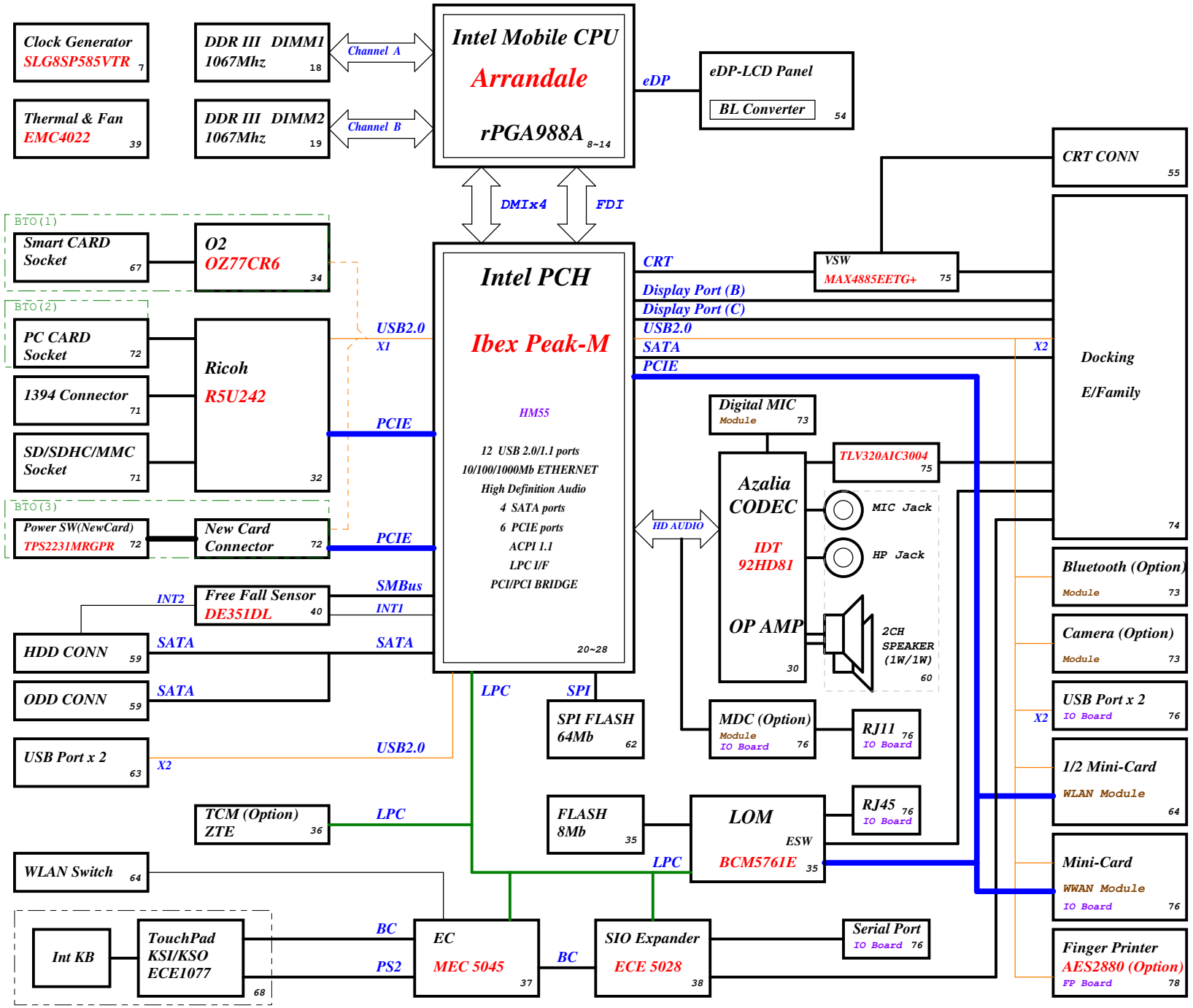
Fonseca UMA Block Diagram

	DF3-14	DF3
Project code	91.4GN01.001	91.4EQ01.001
PCB P/N	48.?????.0SB	48.?????.0SB
Revision	09276 - SB	09226 - SB



CPU DC/DC 47
ISL62883

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC 46
TPS51125

INPUTS	OUTPUTS
+PWR_SRC	+3.3V_ALW +5V_ALW

SYSTEM DC/DC 50
TPS51116

INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT

SYSTEM DC/DC 52
TPS51218

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM LDO 51
RT9035

INPUTS	OUTPUTS
+3.3V_SUS	+1.8V_RUN

SYSTEM DC/DC 53
ADP3211

INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

BATTERY CHARGER 45
TI BQ24745
(AC, Battery Existence)

INPUTS	OUTPUTS
+DC_IN_SS	+PBATT

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Title: Block Diagram

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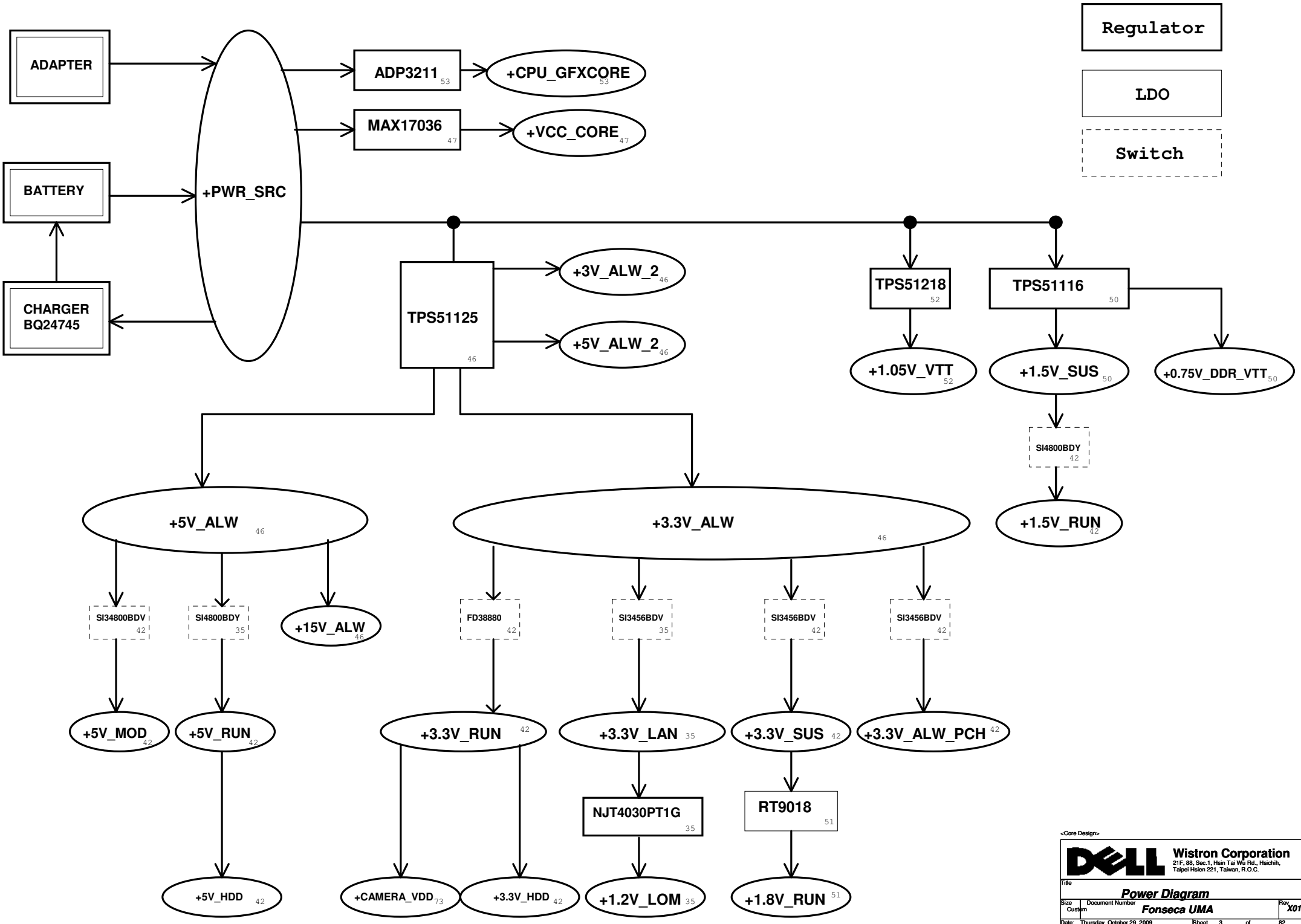

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Title: Power Diagram

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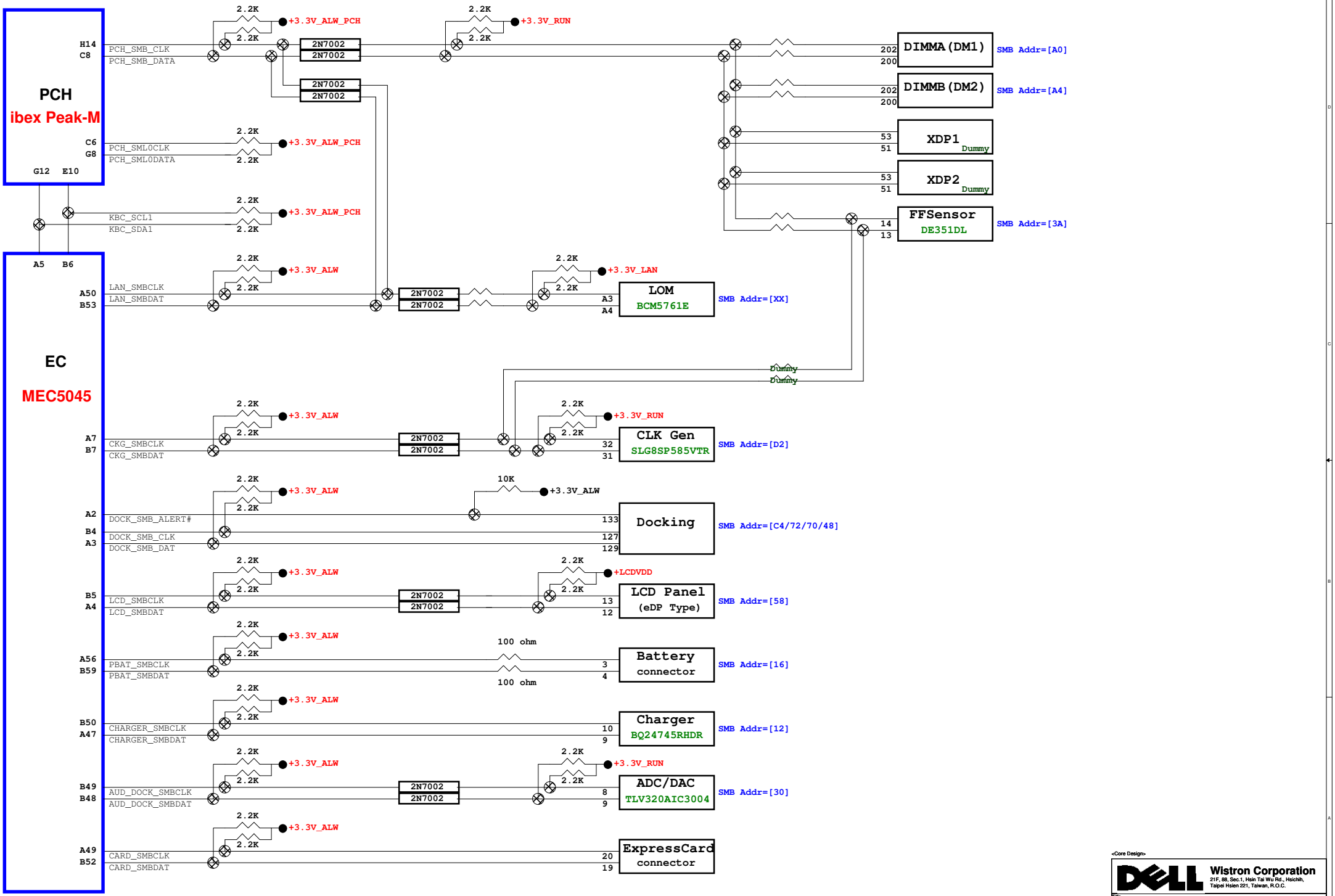

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Title: SMBus Diagram

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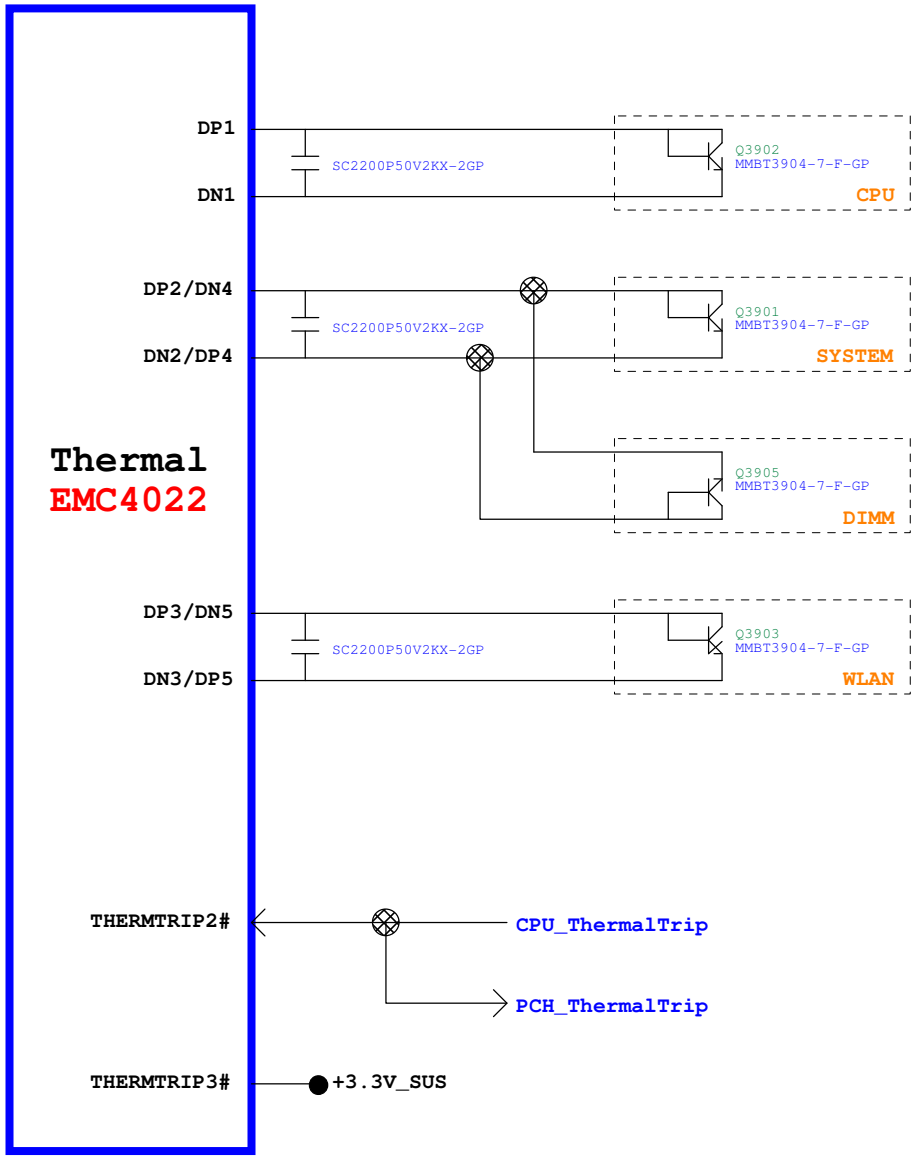
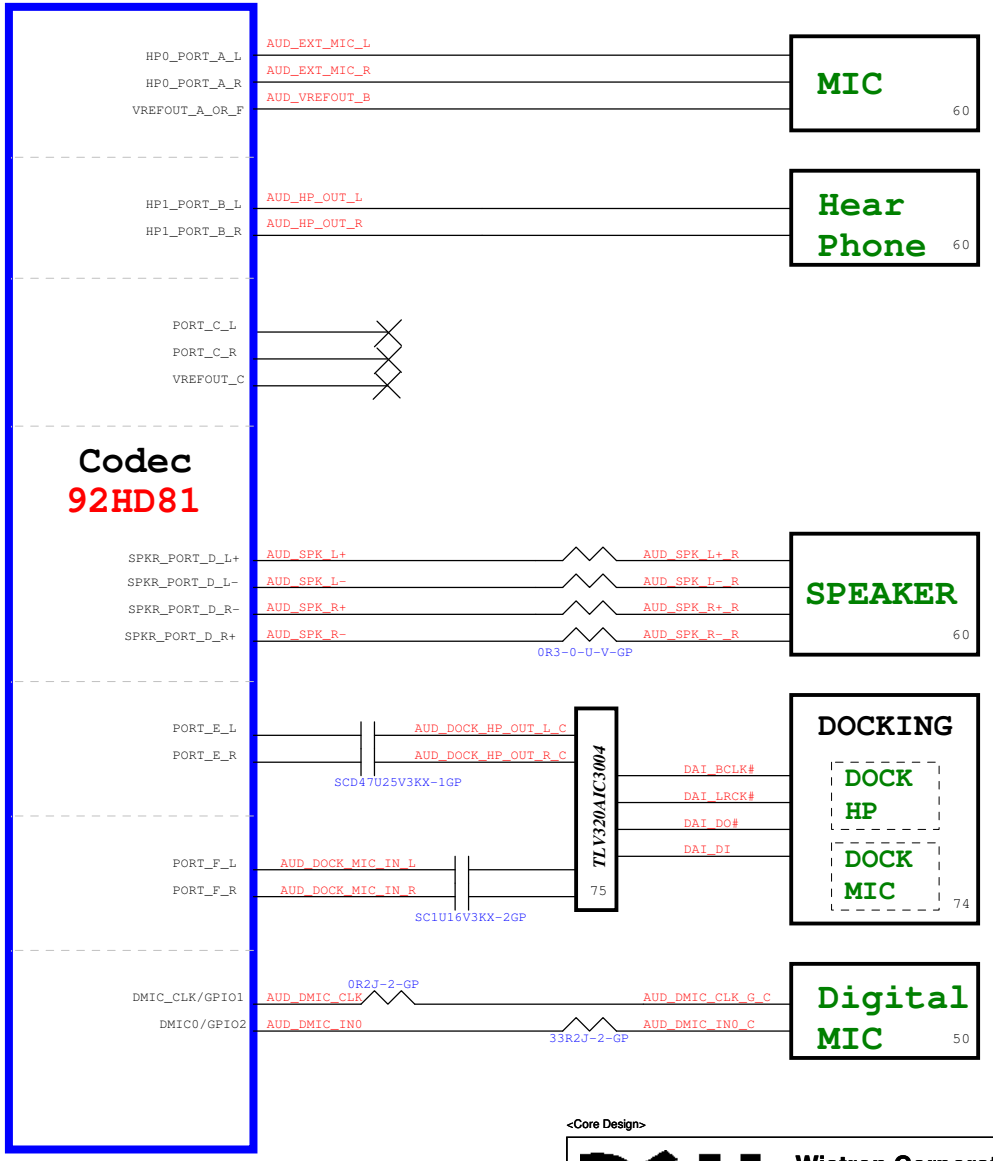
Thermal Block Diagram



Audio Block Diagram



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Title: AUDIO/THERMAL Diagram

Size	Document Number	Rev
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PCH Strapping

Calpella Schematic Checklist Rev: 1.6

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ ~ 10-kΩ weak pull-up resistor.
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** **Note:** Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ ; do not stuff resistor
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled** **Note:** CRB uses a 330-k resistor.
GNT0#, GNT1#	**Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default –** Internal pull-up. **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	**Enable Intel Anti-Theft Technology:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Intel Anti-Theft Technology:** Left floating, no pull-down required.
NV_ALE	**Enable Intel Anti-Theft Technology:** Connect to +NVRAM_VCCQ with 8.2-kΩ weak pull-up resistor [CRB has it pulled up with 1-kΩ no-stuff resistor] **Disable Intel Anti-Theft Technology:** Leave floating (internal pull-down).
NV_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HDA_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. **High (1):** Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. **Note:** CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) – Intel ME Crypto Transport Layer Security TLS) cipher suite with no confidentiality. High (1) – Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note: This is an unmuxed signal. This signal has a weak internal pull-down of 20KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1K pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	**Default =** Do not connect (floating). Internal pull-up. High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev: 1.6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**

PCIE Routing

LANE1	WWAN
LANE2	WLAN
LANE3	PCMCIA
LANE4	Express Card
LANE5	None
LANE6	10M/100M/1G LAN
LANE7	**Not available for HM55**
LANE8	**Not available for HM55**

USB Routing

USB	
Pair	**Device**
0	**USB0 @ MB**
1	**USB1 @ MB**
2	**USB2 @ IO Board**
3	**USB3 @ IO Board**
4	**WLAN**
5	**Bluetooth**
6	**Not available for HM55**
7	**Not available for HM55**
8	**DOCKING PORT1**
9	**DOCKING PORT2**
10	**Finger Printer**
11	**Camera**
12	**PCCard / SmartCard**
13	**WWAN**

<Core Design>

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Title: ***Table of Content***

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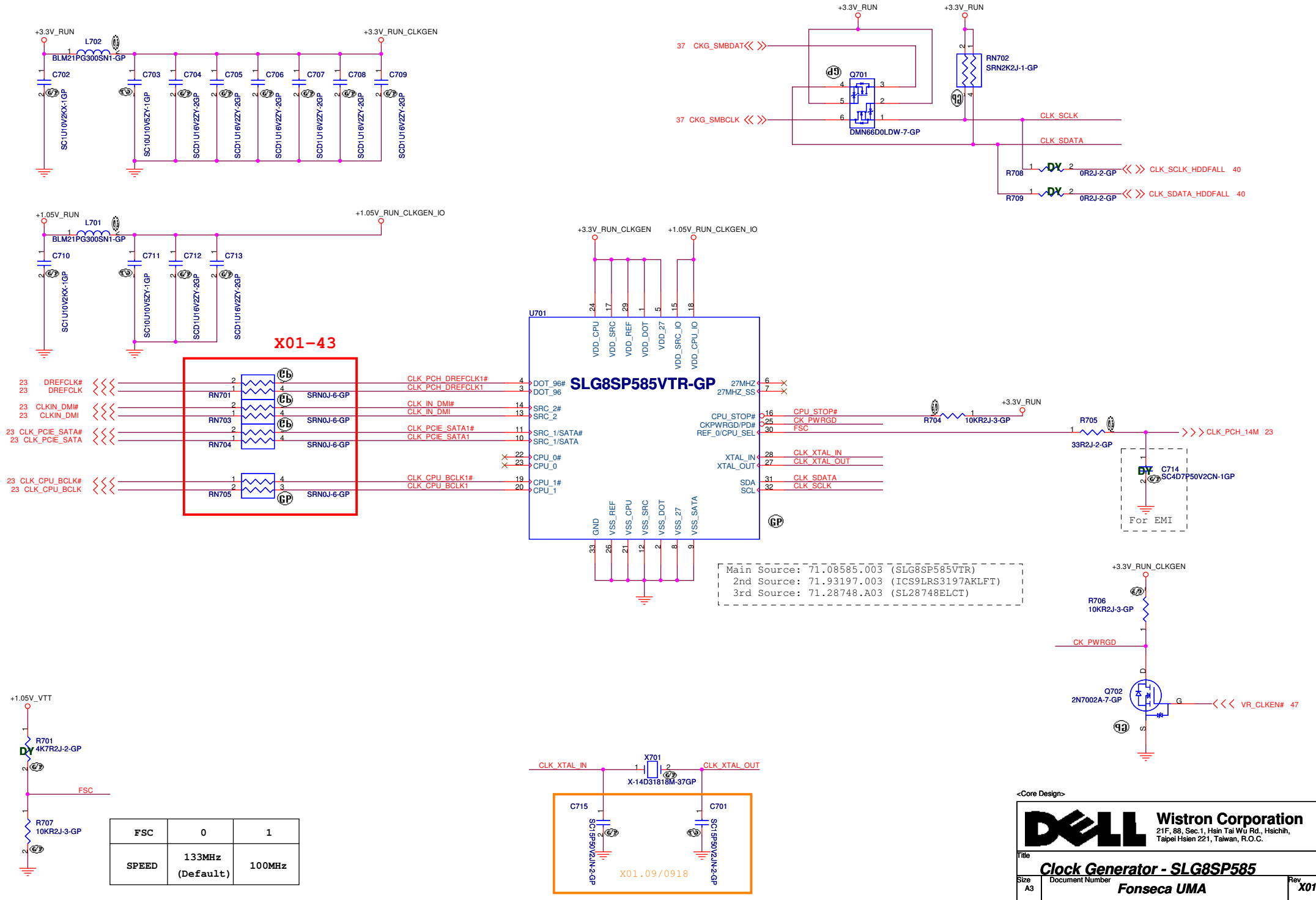
SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator - SLG8SP585

Size	Document Number	Rev
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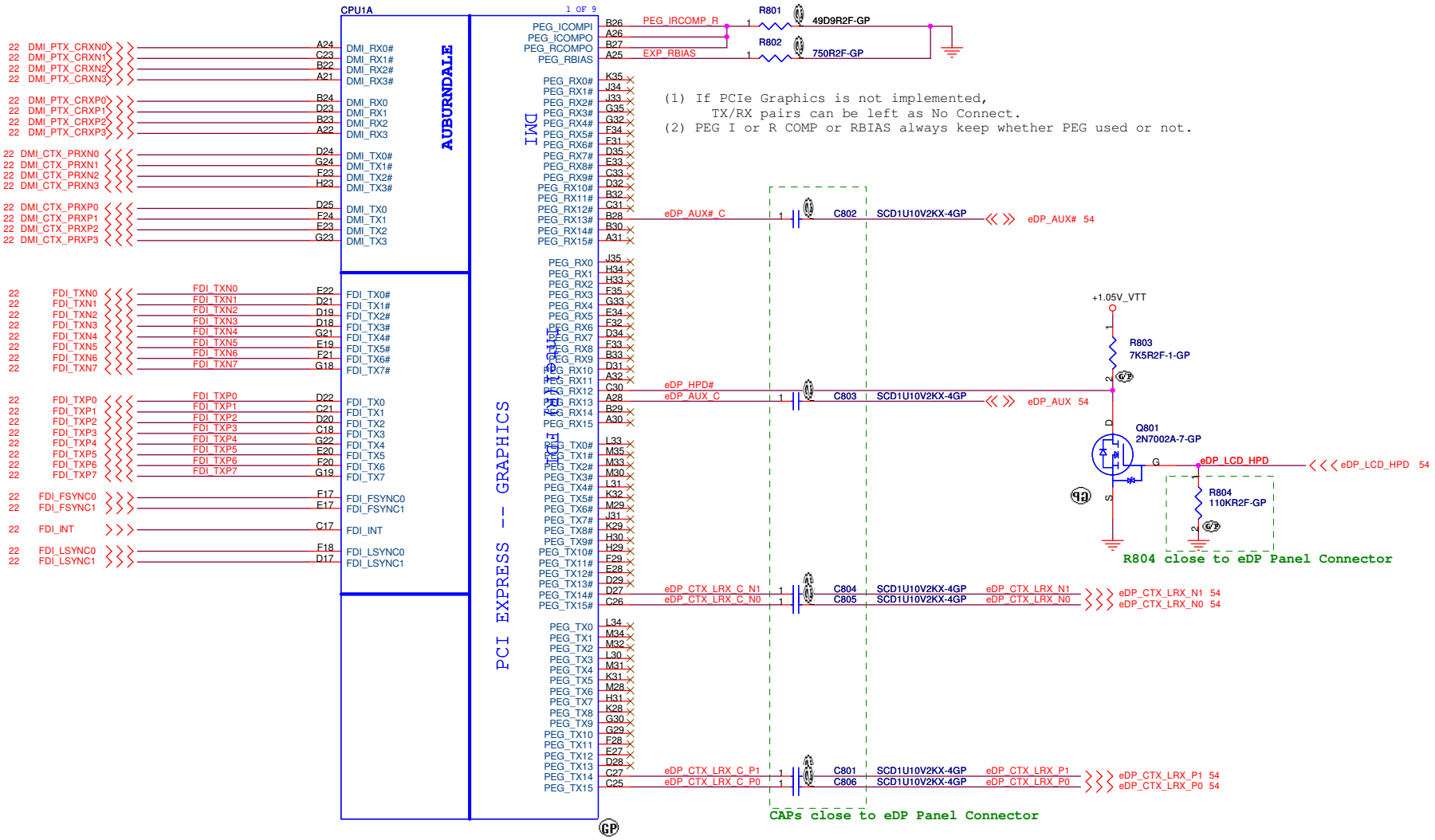
SSID = CPU



<Core Design>

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Title: CPU - PCIE/DMI/FDI (1/7)

Size	Document Number	Rev
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SSID = CPU

Processor Pullups

+1.05V_VTT

R903 49D9R2F-GP H_CATERR#
R906 49D9R2F-GP H_PROCHOT#
R908 68R2-GP DY H_CPURST#

Processor Compensation Signals

R902 20R2F-GP H_COMP3
R904 20R2F-GP H_COMP2
R905 49D9R2F-GP H_COMP1
R907 49D9R2F-GP H_COMP0

X01.09/0819

37 H_SKTOCC# H_SKTOCC#

CPU1B

2 OF 9

COMP3 AT23
COMP2 AT24
COMP1 G16
COMP0 AT26
SKTOCC# AH24
CATERR# AK14
PECI AT15
PROCHOT# AN26
THERMTRIP# AK15
RESET_OBS# AP26
PM_SYNC AL15
VCCPWRGOOD_1 AN14
VCCPWRGOOD_0 AN27
SM_DRAMPWROK AK13
VTTPWRGOOD AM15
TAPPWRGOOD AM26
RSTIN# AL14

H_CATERR# H_PECI H_PROCHOT# H_THERMTRIP# H_CPURST# H_PM_SYNC H_PWRGD VCCPWRGOOD DRAM_PWROK H_VTTPWRGD H_PWRGD_XDP PLT_RST#_R

CLOCKS

BCLK CPU_P_R BCLK CPU_N_R
BCLK_ITP BCLK_ITP_P_R BCLK_ITP_N_R
PEG_CLK PEG_CLK_R PEG_CLK#_R
DPLL_REF_SSCLK DPLL_REF_SSCLK_R DPLL_REF_SSCLK#_R

THERMAL, DDR3 MISC

SM_DRAMRST# SM_RCOMP0 SM_RCOMP1 SM_RCOMP2 PM_EXT_TS0# PM_EXT_TS1#

PWR MANAGEMENT

PRDY# PREQ# TCK TMS TRST# TDI TDO TDI_M TDO_M DBR#

JTAG & BPM

BPM0# BPM1# BPM2# BPM3# BPM4# BPM5# BPM6# BPM7#

X01-43

RN903 SRN0J-6-GP

BCLK_CPU_P_R 25
BCLK_CPU_N_R 25
BCLK_ITP_P 58
BCLK_ITP_N 58
PEG_CLK_R 23
PEG_CLK#_R 23
DPLL_REF_SSCLK_R 23
DPLL_REF_SSCLK#_R 23

DDR_HVREF_RST_GATE 37

+1.5V_SUS

R934 1KR2J-1-GP
Q902 2N7002A-7-GP
R935 0R2J-2-GP DY
DDR3_DRAMRST# 18,19

X01.09/0917

R939 100KR2J-1-GP DY

R914 10KR2J-3-GP

+1.05V_VTT

XDP_PRDY# XDP_PREQ# XDP_TCLK XDP_TMS XDP_TRST# XDP_TDI_R XDP_TDO_R XDP_TDI_M XDP_TDO_M H_DBR#_R

R918 0R2J-2-GP XDP_DBRESET# 22,38,58

XDP_OBS0 XDP_OBS1 XDP_OBS2 XDP_OBS3 XDP_OBS4 XDP_OBS5 XDP_OBS6 XDP_OBS7

DDR3 Compensation Signals

SM_RCOMP_0 R909 100R2F-L1-GP-U
SM_RCOMP_1 R910 24D9R2F-L-GP
SM_RCOMP_2 R911 130R2F-1-GP

Place near U3801

+3.3V_RUN +1.05V_VTT

R912 8K2R2J-3-GP
R913 2K2R2J-2-GP
1.05V_VTT_Q901
Q901 MMBT3904-2-F-GP
38 CPU_CATERR# H_CATERR#
C901 SCD1U10V2KX-4GP

R917 0R2J-2-GP H_PWRGD
R919 0R2J-2-GP VCCPWRGOOD_0
R921 1K5R2F-2-GP PLTRST1#
R924 750R2F-GP

22 DRAM_PWROK
52 H_VTTPWRGD
58 H_PWRGD_XDP
21,58 PLTRST1#

JTAG MAPPING

XDP_TDI_R R929 0R2J-2-GP XDP_TDI 58
XDP_TDO_M R930 0R2J-2-GP DY XDP_TDO 58
R901 0R2J-2-GP
XDP_TDI_M R931 0R2J-2-GP DY
XDP_TDO_R R932 0R2J-2-GP

Scan Chain (Default)	Stuff --> R929, R901, R932 No Stuff --> R930, R931
CPU Only	Stuff --> R929, R930 No Stuff --> R901, R931, R932
GMCH Only	Stuff --> R931, R932 No Stuff --> R929, R930, R901

XDP_TRST# R933 51R2J-2-GP

+1.05V_VTT

XDP_TMS R922 51R2J-2-GP DY
XDP_TDI_R R923 51R2J-2-GP DY
XDP_PREQ# R925 51R2J-2-GP DY
XDP_TCLK R926 51R2J-2-GP DY

X01-4

22,35,38,50 SIO_SLP_S3#
37,38,58 RUNPWROK

R915 0R2J-2-GP
R920 0R2J-2-GP RUNPWROK_C

U901 74LVC1G08GW-1-GP

+3.3V_ALW_PCH
+3.3V_SUS
R938 0R2J-2-GP DY
DRAM_PWROK_R
R936 1K5R2F-2-GP
DRAM_PWROK
R937 750R2F-GP

X01.09/0917

<Core Design>

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Title: CPU Thermal/Clock/PM (2/7)
Size: A3 | Document Number: Fonseca UMA | Rev: X01
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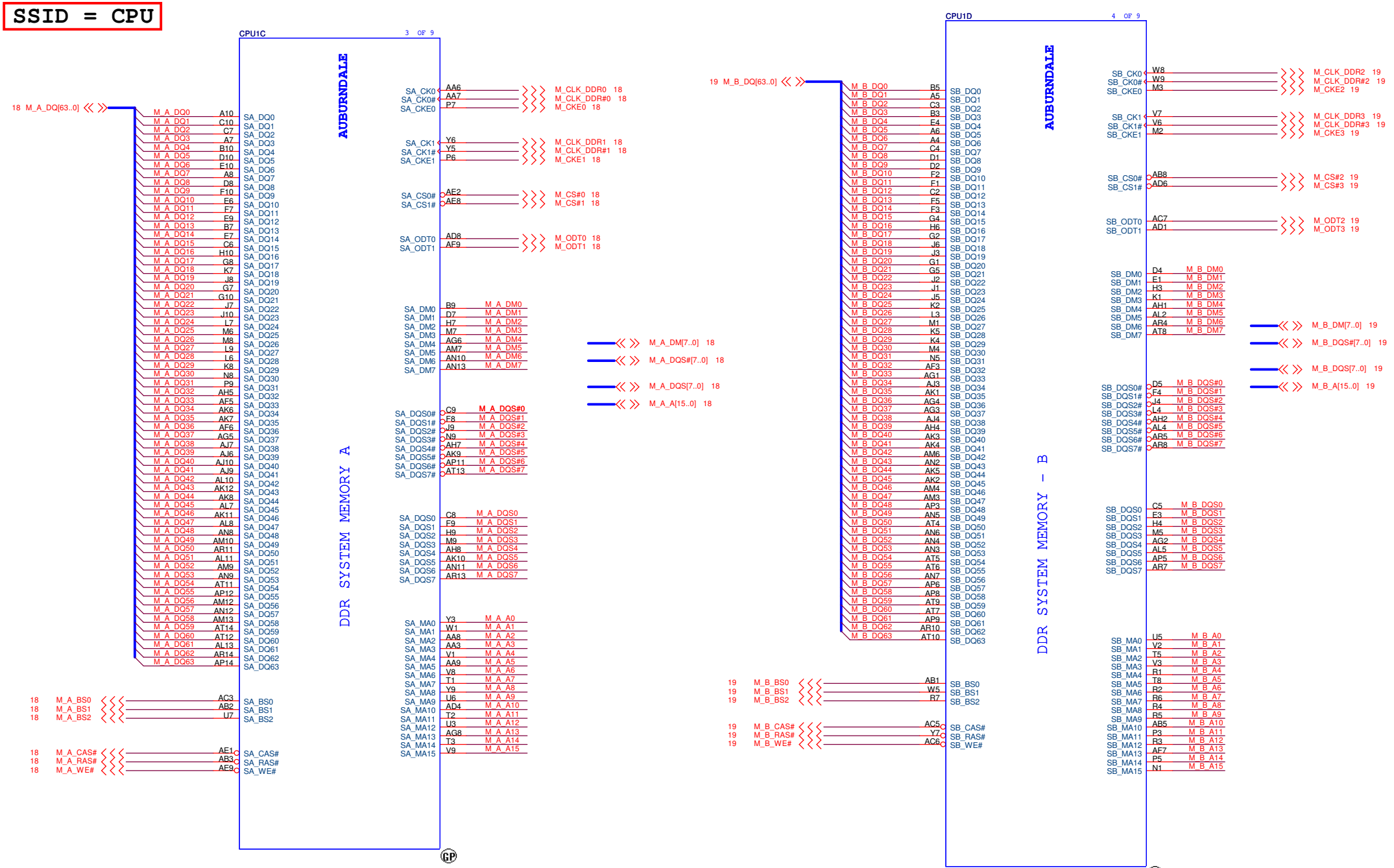
SSID = CPU



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Title: CPU - DDR (3/7)		
Size: A3	Document Number: Fonseca UMA	Rev: X01
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SSID = CPU

SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor

CPU1E — 5 OF 9 — AUBURNDALE

CPU Piin AJ13 and AJ12:
Core voltage sense line.
Via from PGA pad to the back of the MB and provide test point.
Do not route any additional trace.

RSVD#AJ13 AJ13 — H_RSVD32 — TP1118
RSVD#AJ12 AJ12 — H_RSVD33 — TP1117
RSVD#AH25 AH25
RSVD#AK26 AK26 — H_RSVD35 — TP1119
RSVD#AL26 AL26 — H_RSVD36 — TP1120
RSVD_NCTF#AR2 AR2
RSVD#AJ26 AJ26
RSVD#AJ27 AJ27

TP1115 VREF_CH_A_DIMM — J17 SA_DIMM_VREF#
TP1116 VREF_CH_B_DIMM — H17 SB_DIMM_VREF#

AP25 RSVD#AP25
AL25 RSVD#AL25
AL24 RSVD#AL24
AL22 RSVD#AL22
AJ33 RSVD#AJ33
AG9 RSVD#AG9
M27 RSVD#M27
L28 RSVD#L28
G25 RSVD#G25
G17 RSVD#G17
E31 RSVD#E31
E30 RSVD#E30

RSVD#AL28 AL28
RSVD#AL29 AL29
RSVD#AP30 AP30
RSVD#AP32 AP32
RSVD#AL27 AL27
RSVD#AT31 AT31
RSVD#AT32 AT32
RSVD#AP33 AP33
RSVD#AR33 AR33

CFG0 AM30 CFG0
TP1101 CFG1 AM28 CFG1
TP1102 CFG2 AP31 CFG2
CFG3 AL32 CFG3
CFG4 AL30 CFG4
TP1103 CFG5 AM31 CFG5
TP1104 CFG6 AN29 CFG6
CFG7 AM32 CFG7
TP1105 CFG8 AK32 CFG8
TP1106 CFG9 AK31 CFG9
TP1107 CFG10 AK28 CFG10
TP1108 CFG11 AJ28 CFG11
TP1109 CFG12 AN30 CFG12
TP1110 CFG13 AN32 CFG13
TP1111 CFG14 AJ32 CFG14
TP1112 CFG15 AJ29 CFG15
TP1113 CFG16 AJ30 CFG16
TP1114 CFG17 AK30 CFG17
H16 RSVD_TP#H16

RSVD#AR32 AR32

RSVD_TP#E15 E15
RSVD_TP#F15 F15
KEY A2
RSVD#D15 D15
RSVD#C15 C15
RSVD#AJ15 AJ15
RSVD#AH15 AH15

B19 RSVD#B19
A19 RSVD#A19
A20 RSVD#A20
B20 RSVD#B20
U9 RSVD#U9
T9 RSVD#T9
AC9 RSVD#AC9
AB9 RSVD#AB9

RSVD_TP#AA5 AA5
RSVD_TP#AA4 AA4
RSVD_TP#R8 R8
RSVD_TP#AD3 AD3
RSVD_TP#AD2 AD2
RSVD_TP#AA2 AA2
RSVD_TP#AA1 AA1
RSVD_TP#R9 R9
RSVD_TP#AG7 AG7
RSVD_TP#AE3 AE3

RSVD_TP#V4 V4
RSVD_TP#V5 V5
RSVD_TP#N2 N2
RSVD_TP#AD5 AD5
RSVD_TP#AD7 AD7
RSVD_TP#W3 W3
RSVD_TP#W2 W2
RSVD_TP#N3 N3
RSVD_TP#AE5 AE5
RSVD_TP#AD9 AD9

J29 RSVD#J29
J28 RSVD#J28

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

VSS AP34 — RSVD_VSS — R1117 0R2J-2-GP

RESERVED

CFG0 — R1102 3K01R2F-3-GP

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled (Clarkfiled only)

CFG3 — R1105 3K01R2F-3-GP

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 — R1109 3K3R2J-3-GP

X01-47

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7 — R1103 3K01R2F-3-GP

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

<Core Design>

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Title: CPU - Reserve (4/7)
Size: Custom | Document Number: Fonseca UMA | Rev: X01
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SSID = CPU

PROCESSOR CORE POWER

48A

+VCC_CORE

CPU1F

6 OF 9

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

CPU VIDS

SENSE LINES

POWER

X01-37

X01-16

X01-24

14ONLY 15ONLY 14ONLY

15ONLY 14/15 15ONLY

14/15 14/15 DY

14/15 14ONLY

+1.05V_VTT

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that
The VTT Rail values are
Arrandale for VTT=1.05V
Clarksfield for VTT=1.1V

PSI# AN33 PSI# 47

VID0 AK35 H_VID0
VID1 AK33 H_VID1
VID2 AK34 H_VID2
VID3 AL35 H_VID3
VID4 AL33 H_VID4
VID5 AM33 H_VID5
VID6 AM35 H_VID6
PROC_DPRSLPVR AM34 PM_DPRSLPVR 47

VTT_SELECT G15 H_VTTVID1 TP1201

Arrandale drives this pin High for 1.05V
Clarksfield drives this pin Low for 1.1V

ISENSE AN35 CPU_IMON_R R1205 0R2J-2-GP CPU_IMON 39,47

VCC_SENSE AJ34 VCC_SENSE_R
VSS_SENSE AJ35 VSS_SENSE_R

VTT_SENSE B15 VTT_SENSE_R R1206 0R2J-2-GP VTT_SENSE 52
VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT TP1202

R1202 100R2F-L1-GP-U
R1203 0R2J-2-GP VCC_SENSE 47
R1201 0R2J-2-GP VSS_SENSE 47
VSS_SENSE_R 47
Place near PU4701
R1204 100R2F-L1-GP-U
R1207 27D4R2F-L1-GP
R1208 27D4R2F-L1-GP

<Core Design>

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Title: CPU - VCC_CORE (5/7)

Size: Custom | Document Number: Fonseca UMA | Rev: X01

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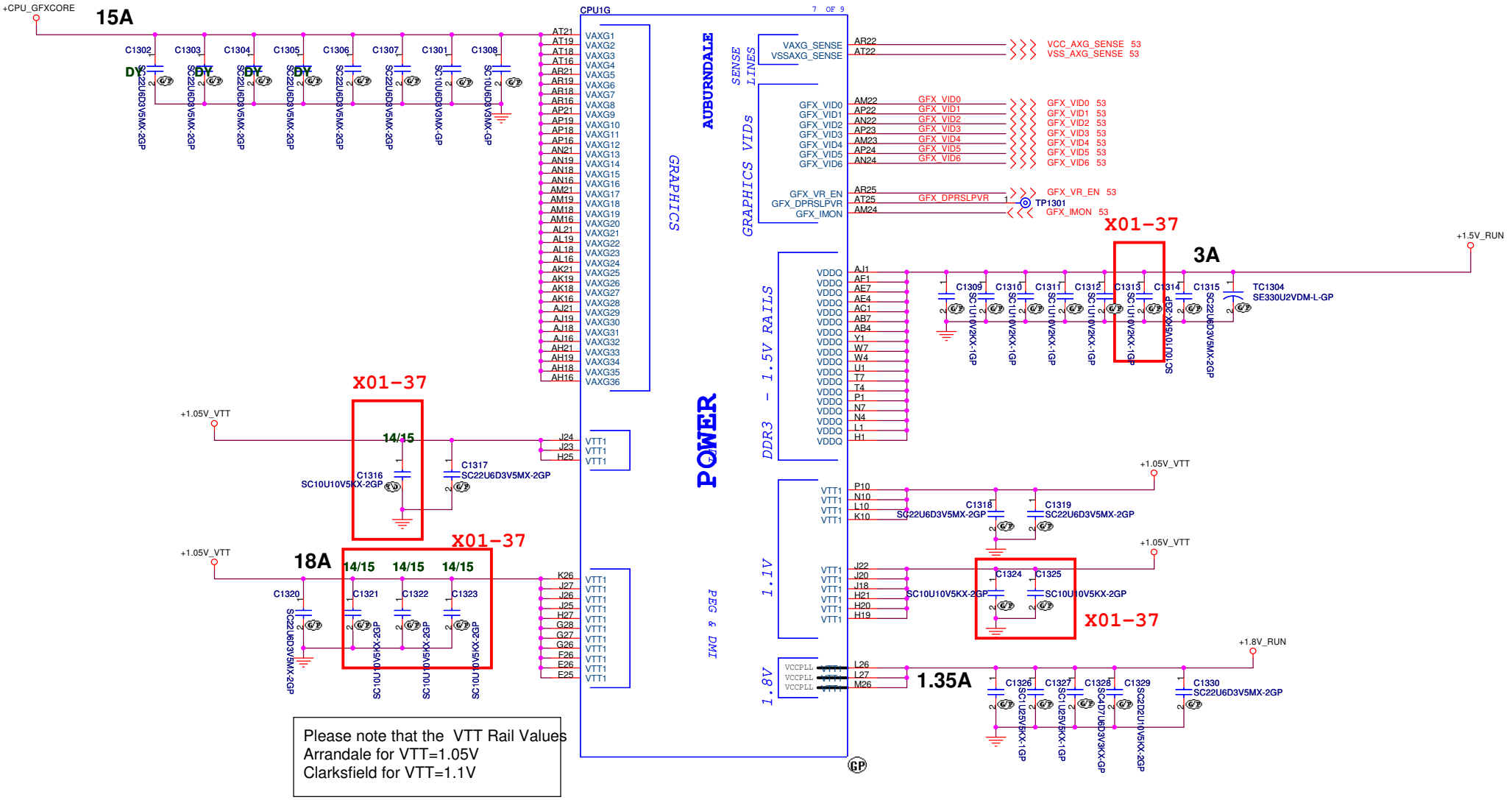
SSID = CPU



<Core Design>

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Title: CPU - GFXCORE (6/7)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

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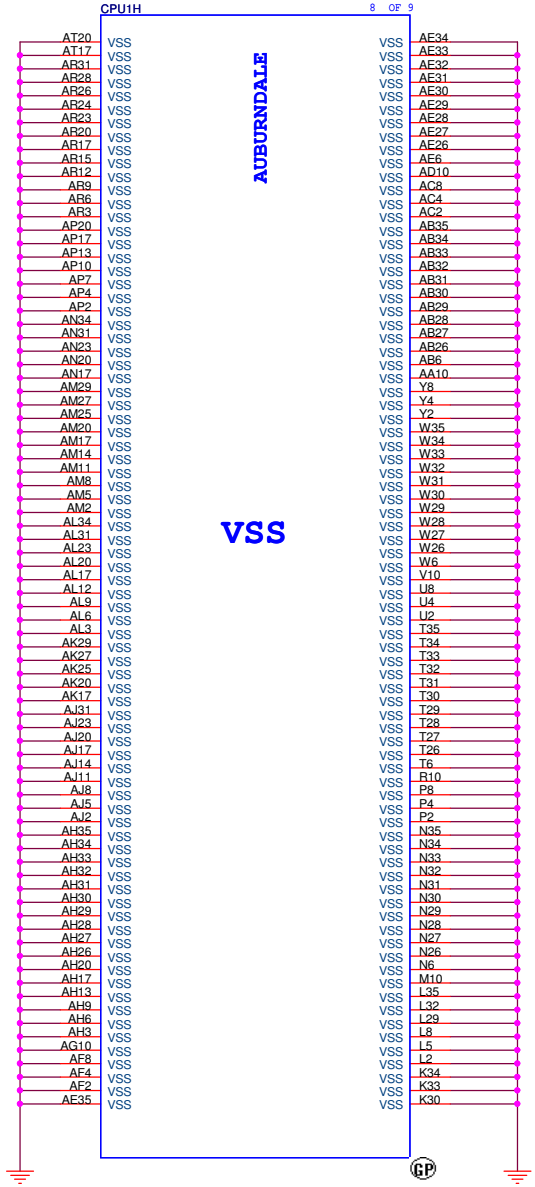
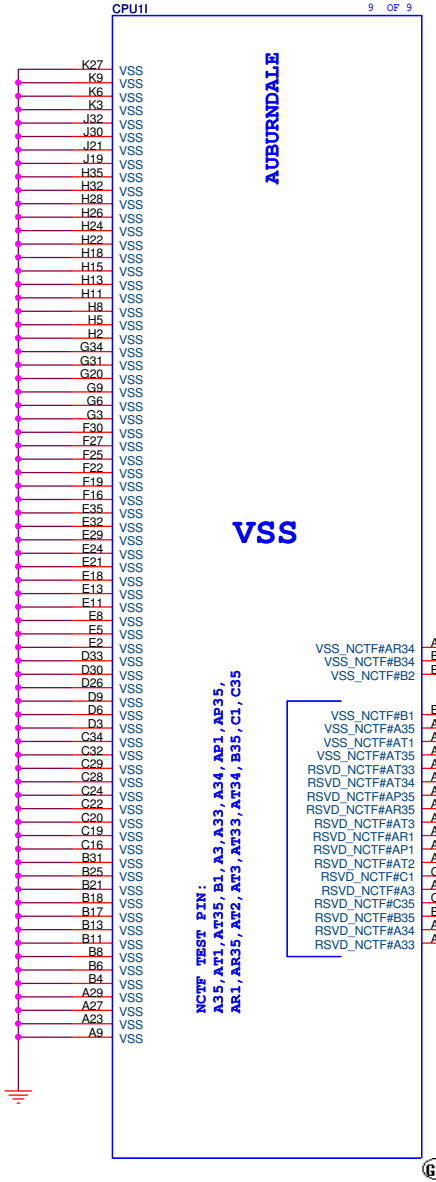
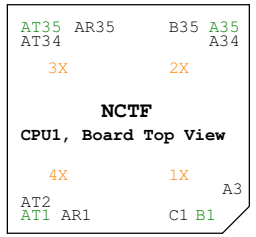
SSID = CPU







VSS_NCTF#AR34 VSS_NCTF#B34 VSS_NCTF#B2 → AR34 B34 B2

VSS_NCTF#B1	B1	TP_MCP_VSS_NCTF11	TP1401
VSS_NCTF#A35	A35	TP_MCP_VSS_NCTF21	TP1404
VSS_NCTF#AT1	AT1	TP_MCP_VSS_NCTF41	TP1410
VSS_NCTF#AT35	AT35	TP_MCP_VSS_NCTF31	TP1407
RSVD_NCTF#AT33	AT33		
RSVD_NCTF#AT34	AT34	TP_MCP_VSS_NCTF33	TP1409
RSVD_NCTF#AP35	AP35		
RSVD_NCTF#AR35	AR35	TP_MCP_VSS_NCTF32	TP1408
RSVD_NCTF#AT3	AT3		
RSVD_NCTF#AR1	AR1	TP_MCP_VSS_NCTF43	TP1412
RSVD_NCTF#AP1	AP1		
RSVD_NCTF#AT2	AT2	TP_MCP_VSS_NCTF42	TP1411
RSVD_NCTF#C1	C1	TP_MCP_VSS_NCTF12	TP1402
RSVD_NCTF#A3	A3	TP_MCP_VSS_NCTF13	TP1403
RSVD_NCTF#C35	C35		
RSVD_NCTF#B35	B35	TP_MCP_VSS_NCTF23	TP1406
RSVD_NCTF#A34	A34	TP_MCP_VSS_NCTF22	TP1405
RSVD_NCTF#A33	A33		

All NCTF pins should be Test Points and should be routed as trace.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU - VSS (7/7)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

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(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserve

Size	Document Number	Rev
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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserve

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserve

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SSID = Memory

SO-DIMMA
H = 9.2mm

DM1

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

SODIMM A DECOUPLING

X01-37

Layout Note:
Place these Caps near SO-DIMMA.

14ONLY

15ONLY

Place between DM1 and DM2.

Place these caps close to VTT1 and VTT2.

Near Memory +1.5V_SUS Plane

Near CPU +1.5V_RUN Plane

Reverse Type

DDR3-204P-42-GP

62.10017.N61

<Core Design>

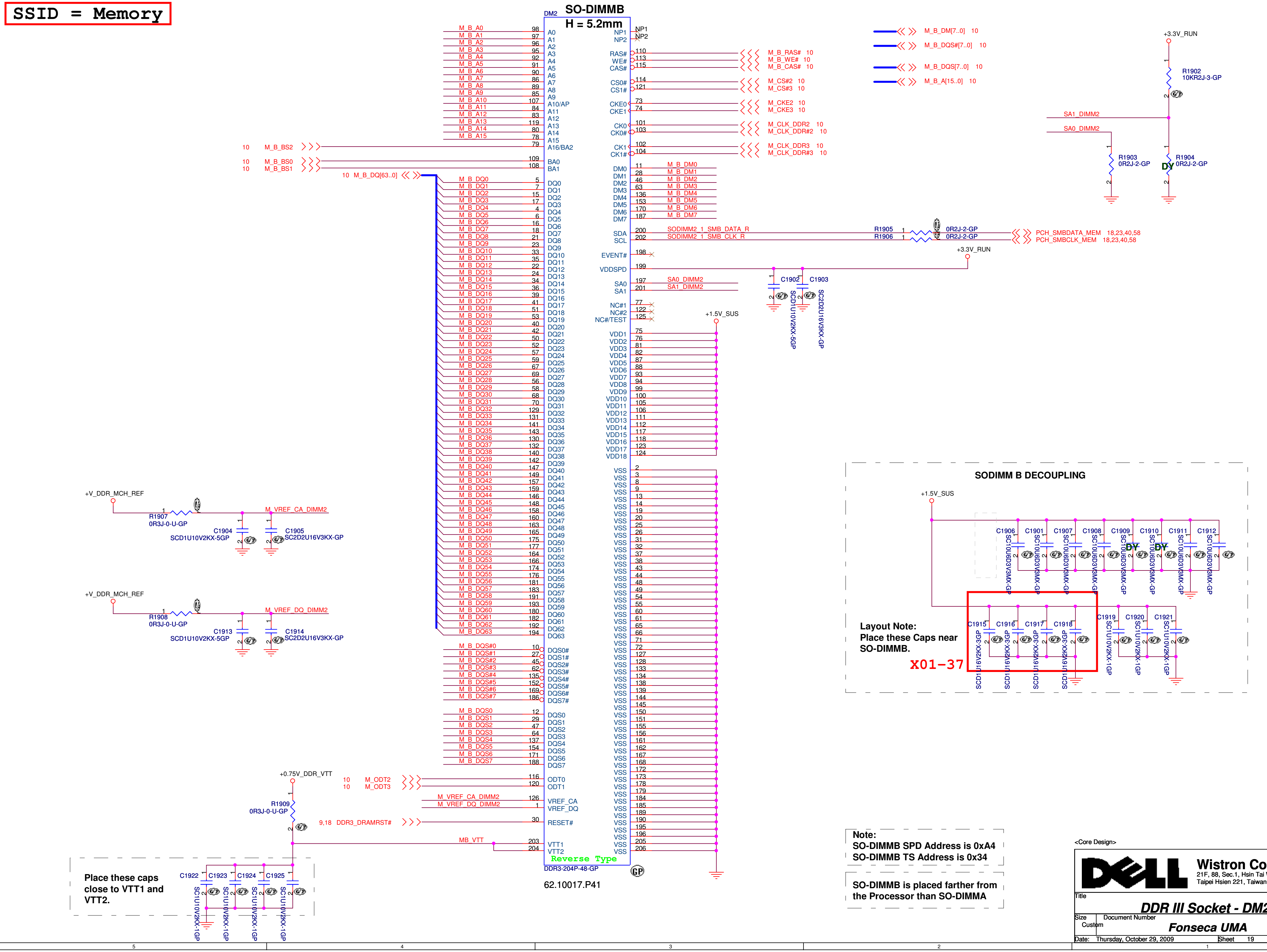
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR III Socket - DM1

Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 18 of 82

SSID = Memory



DM2
SO-DIMMB
H = 5.2mm
M_B_A0 … M_B_A15
M_B_BS2
M_B_BS0
M_B_BS1
10 M_B_DQ[63..0]
M_B_DQ0 … M_B_DQ63
M_B_DQS#0 … M_B_DQS#7
M_B_DQS0 … M_B_DQS7
M_B_RAS# 10
M_B_WE# 10
M_B_CAS# 10
M_CS#2 10
M_CS#3 10
M_CKE2 10
M_CKE3 10
M_CLK_DDR2 10
M_CLK_DDR#2 10
M_CLK_DDR3 10
M_CLK_DDR#3 10
M_B_DM0 … M_B_DM7
SODIMM2_1_SMB_DATA_R
SODIMM2_1_SMB_CLK_R
R1905
R1906
0R2J-2-GP
PCH_SMBDATA_MEM 18,23,40,58
PCH_SMBCLK_MEM 18,23,40,58
+3.3V_RUN
SA0_DIMM2
SA1_DIMM2
C1902
C1903
SCD1U10V2KX-5GP
SC2D2U16V3KX-GP
+1.5V_SUS
M_B_DM[7..0] 10
M_B_DQS#[7..0] 10
M_B_DQS[7..0] 10
M_B_A[15..0] 10
R1902
10KR2J-3-GP
R1903
0R2J-2-GP
R1904
0R2J-2-GP
DY
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2
BA0 BA1
DQ0 … DQ63
DQS0# … DQS7#
DQS0 … DQS7
ODT0 ODT1
VREF_CA VREF_DQ
RESET#
VTT1 VTT2
NP1 NP2
RAS# WE# CAS#
CS0# CS1#
CKE0 CKE1
CK0 CK0# CK1 CK1#
DM0 … DM7
SDA SCL
EVENT#
VDDSPD
SA0 SA1
NC#1 NC#2 NC#/TEST
VDD1 … VDD18
VSS
Reverse Type
DDR3-204P-48-GP
62.10017.P41
+V_DDR_MCH_REF
R1907
0R3J-0-U-GP
M_VREF_CA_DIMM2
C1904
SCD1U10V2KX-5GP
C1905
SC2D2U16V3KX-GP
R1908
0R3J-0-U-GP
M_VREF_DQ_DIMM2
C1913
SCD1U10V2KX-5GP
C1914
SC2D2U16V3KX-GP
+0.75V_DDR_VTT
R1909
0R3J-0-U-GP
10 M_ODT2
10 M_ODT3
9,18 DDR3_DRAMRST#
MB_VTT
C1922 C1923 C1924 C1925
SC1U10V2KX-1GP
Place these caps close to VTT1 and VTT2.
SODIMM B DECOUPLING
C1906 C1901 C1907 C1908 C1909 C1910 C1911 C1912
SC10U6D3V3MX-GP
C1915 C1916 C1917 C1918
SCD1U16V2KX-3GP
C1919 C1920 C1921
SC1U10V2KX-1GP
Layout Note:
Place these Caps near SO-DIMMB.
X01-37
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	***DDR III Socket - DM2***
Size	Custom
Document Number	***Fonseca UMA***
Rev	***X01***
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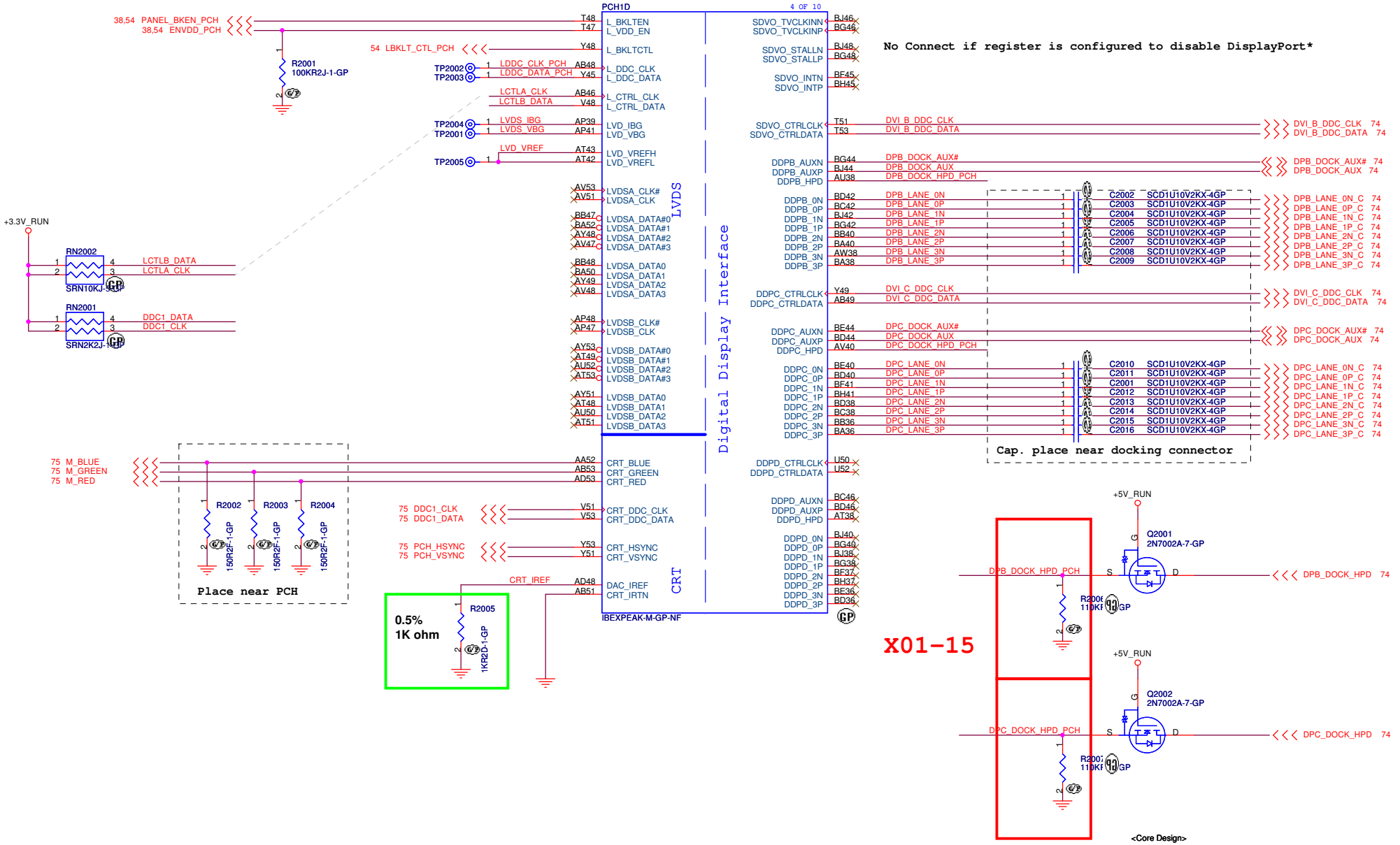
SSID = PCH



<Core Design>

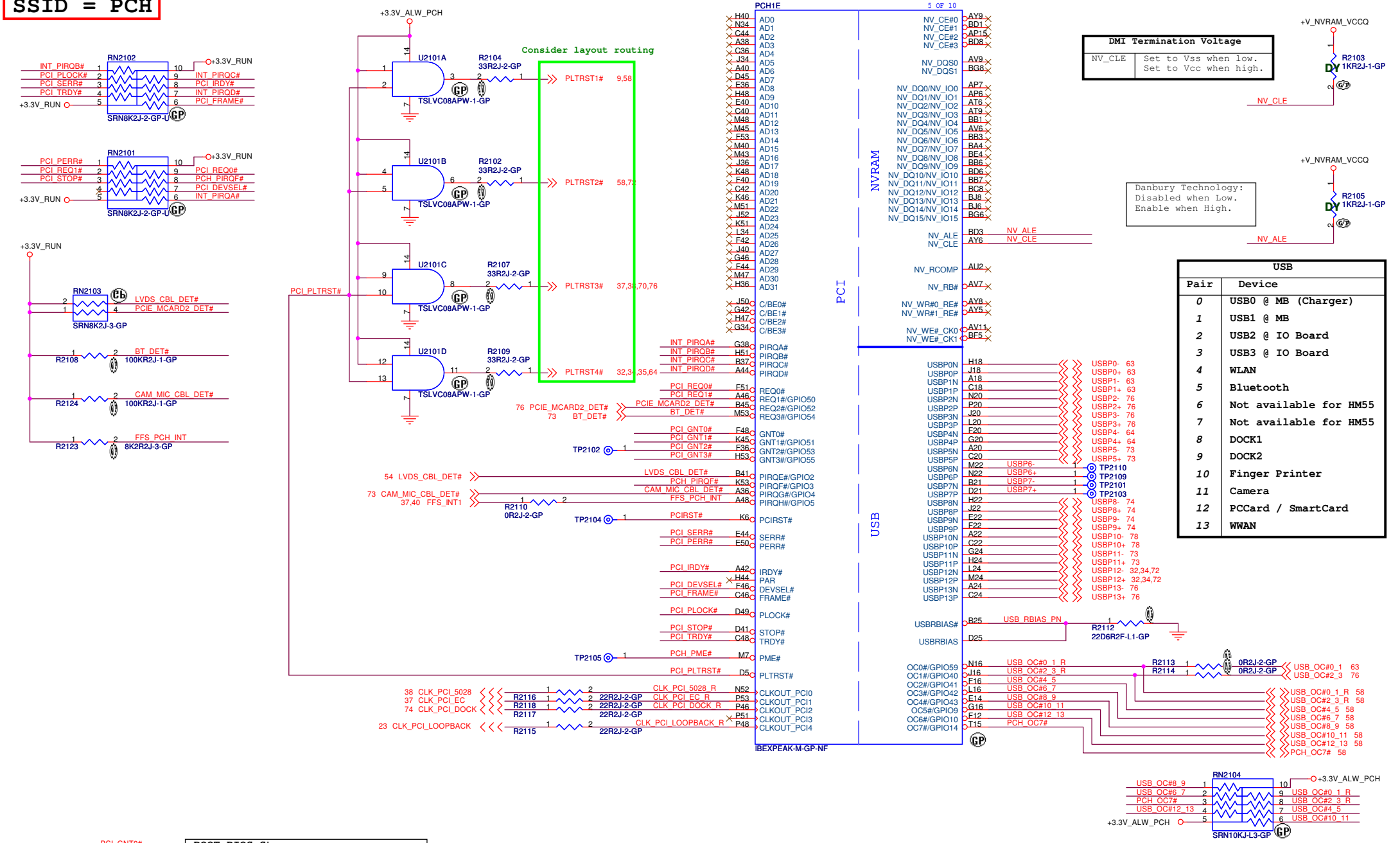
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - LVDS/CRT/DDI (1/9)

Size	Document Number	Rev
A3	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 20 of 82

SSID = PCH



DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:
Disabled when Low.
Enable when High.

USB	
Pair	Device
0	USB0 @ MB (Charger)
1	USB1 @ MB
2	USB2 @ IO Board
3	USB3 @ IO Board
4	WLAN
5	Bluetooth
6	Not available for HM55
7	Not available for HM55
8	DOCK1
9	DOCK2
10	Finger Printer
11	Camera
12	PCCard / SmartCard
13	WWAN

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI(Default)

PCI_GNT[3:0]#: Internal pull high during Strap

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - PCI/USB/NVRAM (2/9)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

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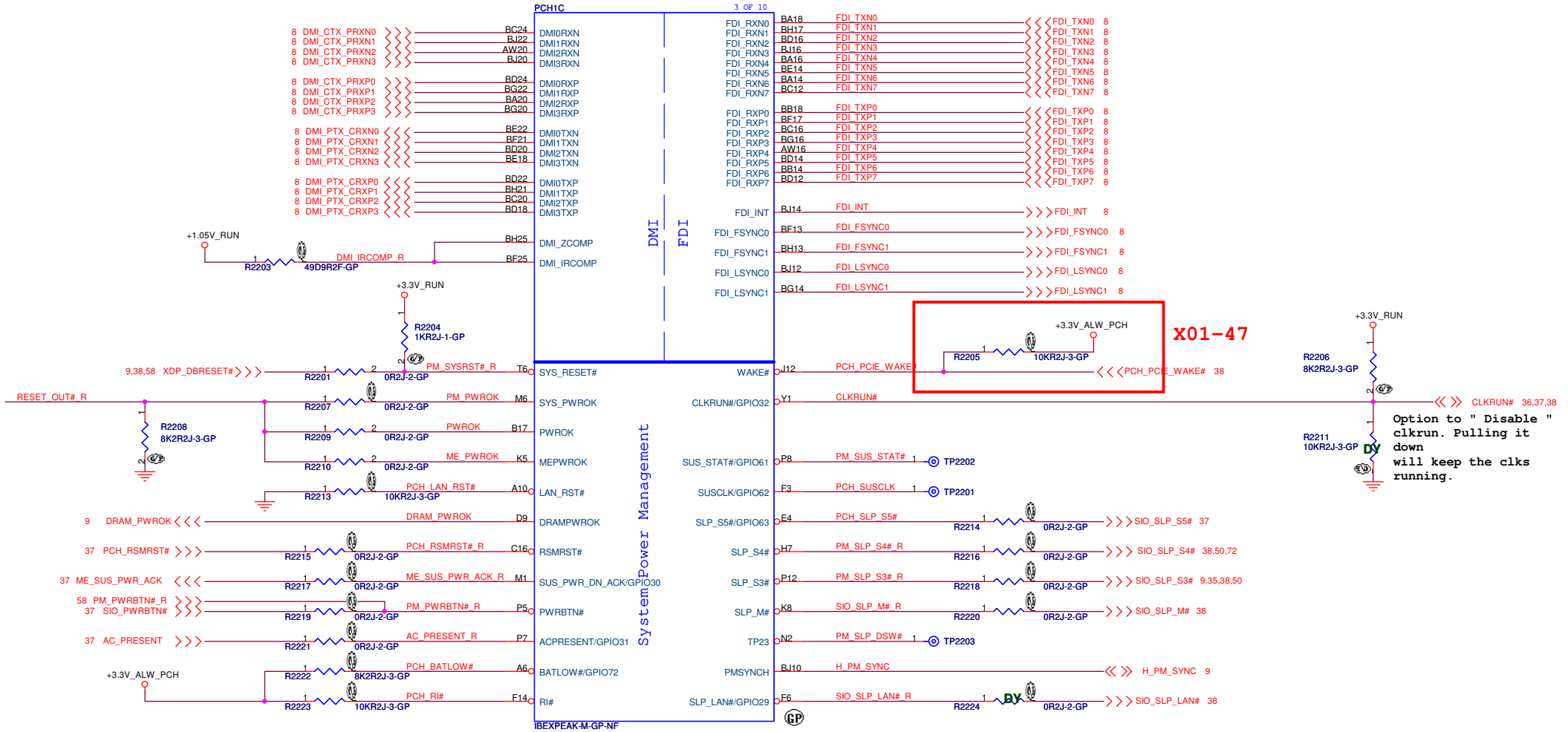
SSID = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - DMI/FDI/PM (3/9)

Size	Document Number	Rev
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SSID = PCH

PCH1B

2 OF 10

PCIe port 7 and 8 may not be available for all Ibex Peak SKUs.

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

X01-43

X01-41

14ONLY

X01-33

15ONLY

From Intel DG 1.6
CLKOUTFLEX{3:0}
RS on PCI/NonPCI Routing (for single / double-load)
=> 22 ohm series resistor

IBEXPEAK-M-GP-NF

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - PCIE/SMBUS/CLOCK/CL (4/9)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 23 of 82

SSID = PCH

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

PCH1A — 1 OF 10 — IBEXPEAK-M-GP-NF

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
LPC: FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME#, LDRQ0#, LDRQ1#/GPIO23, SERIRQ
IHDA: HDA_BCLK, HDA_SYNC, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO13
SATA: SATA0RXN/RXP/TXN/TXP, SATA1RXN/RXP/TXN/TXP, SATA2RXN/RXP/TXN/TXP, SATA3RXN/RXP/TXN/TXP, SATA4RXN/RXP/TXN/TXP, SATA5RXN/RXP/TXN/TXP, SATAICOMPO, SATAICOMPI, SATALED#, SATA0GP/GPIO21, SATA1GP/GPIO19
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

SRTCRST# new signal Pin

SATA port 2 and 3 may not be available for all Ibex Peak SKUs.

HDD: SATA_PRX_HTX0- 59, SATA_PRX_HTX0+ 59, SATA_PTX_HRX0- 59, SATA_PTX_HRX0+ 59
ODD: SATA_PRX_OTX1- 59, SATA_PRX_OTX1+ 59, SATA_PTX_ORX1- 59, SATA_PTX_ORX1+ 59
DOCKING eSATA: SATA_PRX_DTX_5- 74, SATA_PRX_DTX_5+ 74, SATA_PTX_DRX_5- 74, SATA_PTX_DRX_5+ 74

X01-47
X01-30
X01-48

For EMI, RF Cap.

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

Place near PCH side

Form DG1.5
TRST# on PCH does not belong to JTAG interface.
For ES1 silicon, an ext. pull up 3.3-V Sus is required for bias internal state.
A 20-K/10-K voltage divider to this signal to 1.1 V.
However, from ES2 silicon onward, this signal is a No Connect regardless if JTAG interface on PCH is enabled or not.

Pull up +3.3V_M enable iAMT(DY disable)

Internal pull-up of 20K for HDA_DOCK_EN#,

integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - SPI/RTC/LPC/SATA/IHDA (5/9)
Size: A3 | Document Number: Fonseca UMA | Rev: X01
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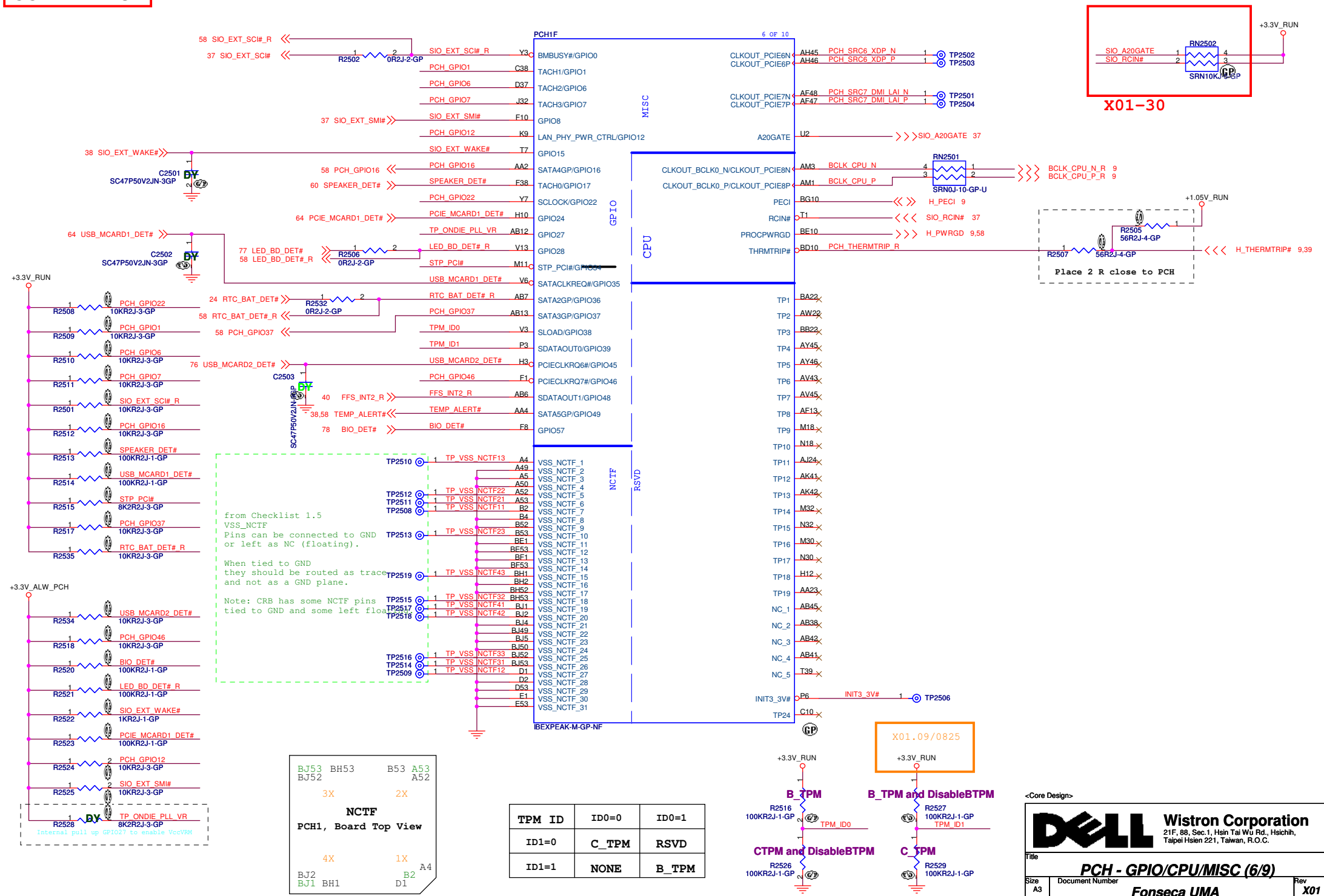
20.F1000.003

SSID = PCH



TPM ID	ID0=0	ID0=1
ID1=0	C_TPM	RSVD
ID1=1	NONE	B_TPM

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - GPIO/CPU/MISC (6/9)

Size	Document Number	Rev
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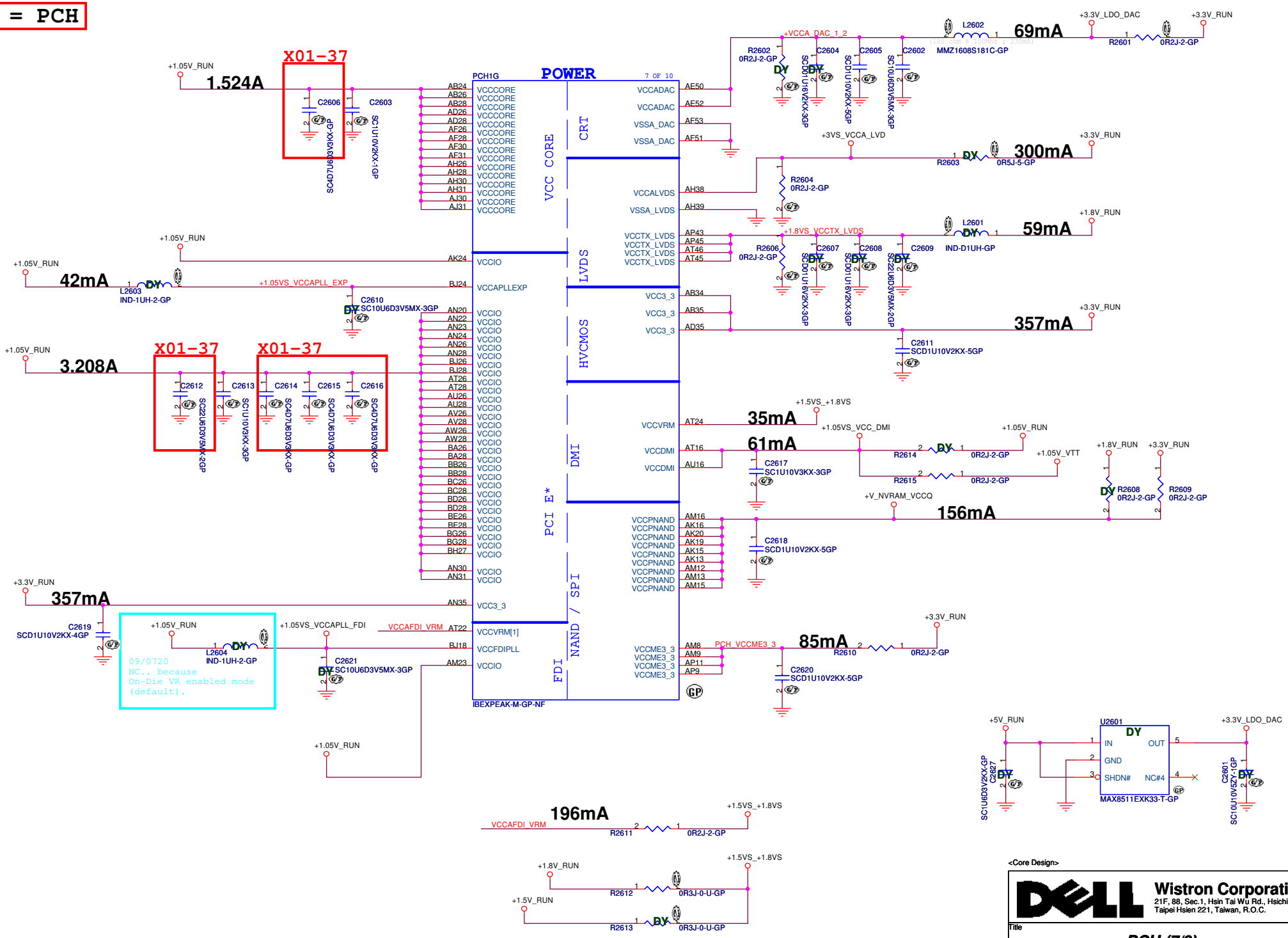
SSID = PCH



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (7/9)

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SSID = PCH

PCH1J

POWER

10 OF 10

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

CPU

RTC

HDA

IBEXPEAK-M-GP-NF

+1.05V_RUN 52mA L2701 IND-10UH-30-GP C2702 SC1U10V2KX-1GP C2703 SC1U10V2KX-1GP

+1.05VS_VCCA_CLK

VCC_LAN_PCH (344mA) R2708 0R2J-2-GP C2709 SCD1U10V2KX-4GP

DCPSUSBYP

+1.05V_RUN 1.998A X01-37 C2705 SC220U6D3V5MX-2GP C2710 SC10U10V5KX-2GP C2706 SC1U10V2KX-1GP C2711 SC1U10V2KX-1GP

+1.05V_RUN L2702 COIL-10UH-9-GP TC2702 ST220U2D5VBM-LGP C2712 SC1U10V2KX-1GP +1.05VS_VCCA_A_DPL

X01.09/0819

L2703 COIL-10UH-9-GP TC2701 ST220U2D5VBM-LGP C2716 SC1U10V2KX-1GP +1.05VS_VCCA_B_DPL

C2714 SCD1U10V2KX-4GP +1.5VS_+1.8VS +VCCRTCEXT

72mA +1.05VS_VCCA_A_DPL

73mA +1.05VS_VCCA_B_DPL

+1.05V_RUN C2719 SC1U10V2KX-1GP C2720 SC1U10V2KX-1GP C2721 SC1U10V2KX-1GP

+1.5V_PCH_DcpSST C2724 SCD1U10V2KX-4GP

+1.05V_PCH_DcpSUS C2726 SCD1U10V2KX-4GP

+3.3V_ALW_PCH 163mA C2727 SCD1U10V2KX-4GP

+3.3V_RUN C2728 SCD1U10V2KX-4GP

X01-37 14/15

+1.05V_VTT 1mA C2729 SC10U6D3V3MX-GP C2730 SC1U16V2KX-3GP C2731 SC1U16V2KX-3GP

+RTC_CELL 2mA C2735 SC1U10V2KX-1GP C2733 SCD1U10V2KX-4GP C2734 SCD1U10V2KX-4GP

+1.05V_RUN C2707 SC1U10V2KX-1GP

+3.3V_ALW_PCH C2708 SCD1U10V2KX-4GP

+3.3V_ALW_PCH C2701 SCD1U10V2KX-4GP

+1.05V_RUN

+5VALW_PCH_VCC5REFSUS

+3.3V_ALW_PCH X01.09/0819 D2702 SDMK0340L-7-F-GP

+5V_ALW_PCH R2701 100R2J-2-GP C2713 SC1U10V2KX-1GP

+5VS_PCH_VCC5REF

+3.3V_RUN C2717 SCD1U10V2KX-4GP

X01-47

+3.3V_RUN X01.09/0819 D2701 SDMK0340L-7-F-GP

+5V_RUN R2702 100R2J-2-GP C2715 SC1U10V2KX-1GP

C2718 SCD1U10V2KX-4GP +3.3V_RUN

+1.05VS_VCCAPLL L2704 IND-10UH-30-GP 32mA +1.05V_RUN C2722 SC1U10V2KX-1GP C2723 SC1U10V2KX-1GP

+1.05V_RUN C2725 SC1U10V2KX-1GP

+1.5VS_+1.8VS

+1.05V_RUN

PCH_VCC_1_1_20 R2703 0R2J-2-GP
PCH_VCC_1_1_21 R2704 0R2J-2-GP
PCH_VCC_1_1_22 R2705 0R2J-2-GP
PCH_VCC_1_1_23 R2706 0R2J-2-GP

+3VS_+1.5VS_HDA_IO R2707 0R2J-2-GP

+3.3V_ALW_PCH C2732 SC1U10V2KX-1GP

6mA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (8/9)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

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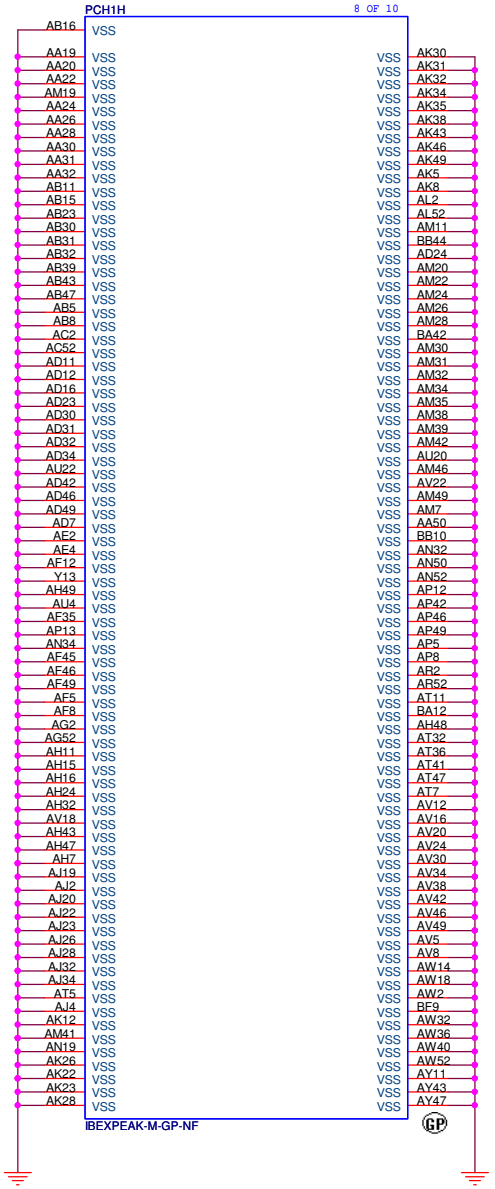
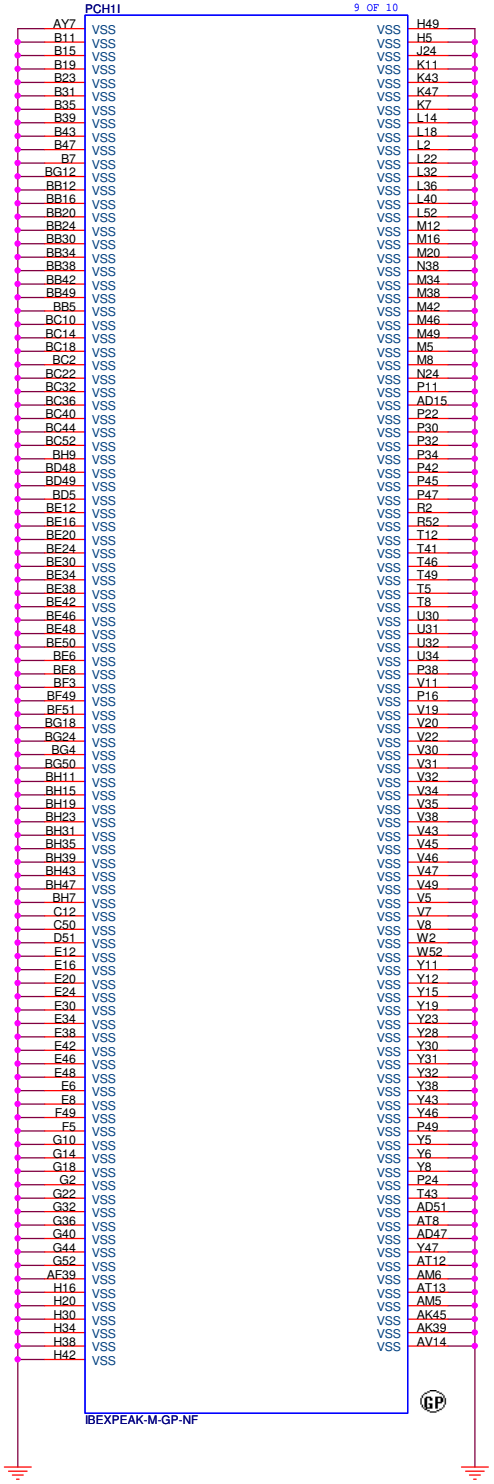
SSID = PCH





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (9/9)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserve

Size	Document Number	Rev
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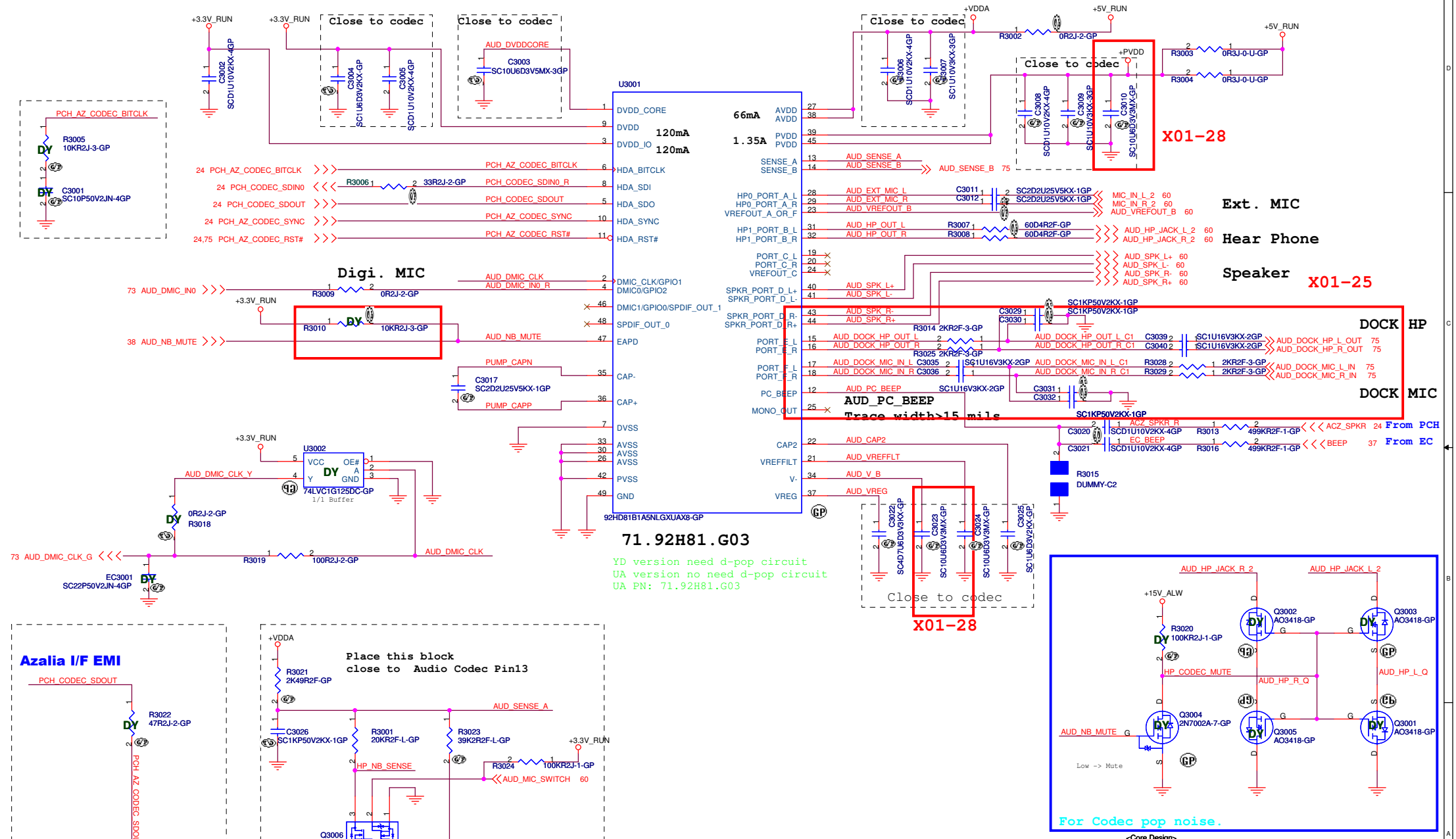
SSID = AUDIO


U3001
92HD81B1A5NLGXUAX8-GP
71.92H81.G03
YD version need d-pop circuit
UA version no need d-pop circuit
UA PN: 71.92H81.G03
Digi. MIC
Close to codec
Close to codec
Close to codec
Close to codec
X01-28
X01-28
X01-25
Ext. MIC
Hear Phone
Speaker
DOCK HP
DOCK MIC
AUD_PC_BEEP
Trace width>15 mils
Azalia I/F EMI
Place this block
close to Audio Codec Pin13
For Codec pop noise.
Low -> Mute
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec
Fonseca UMA
X01
Thursday, October 29, 2009
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82

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<Core Design>

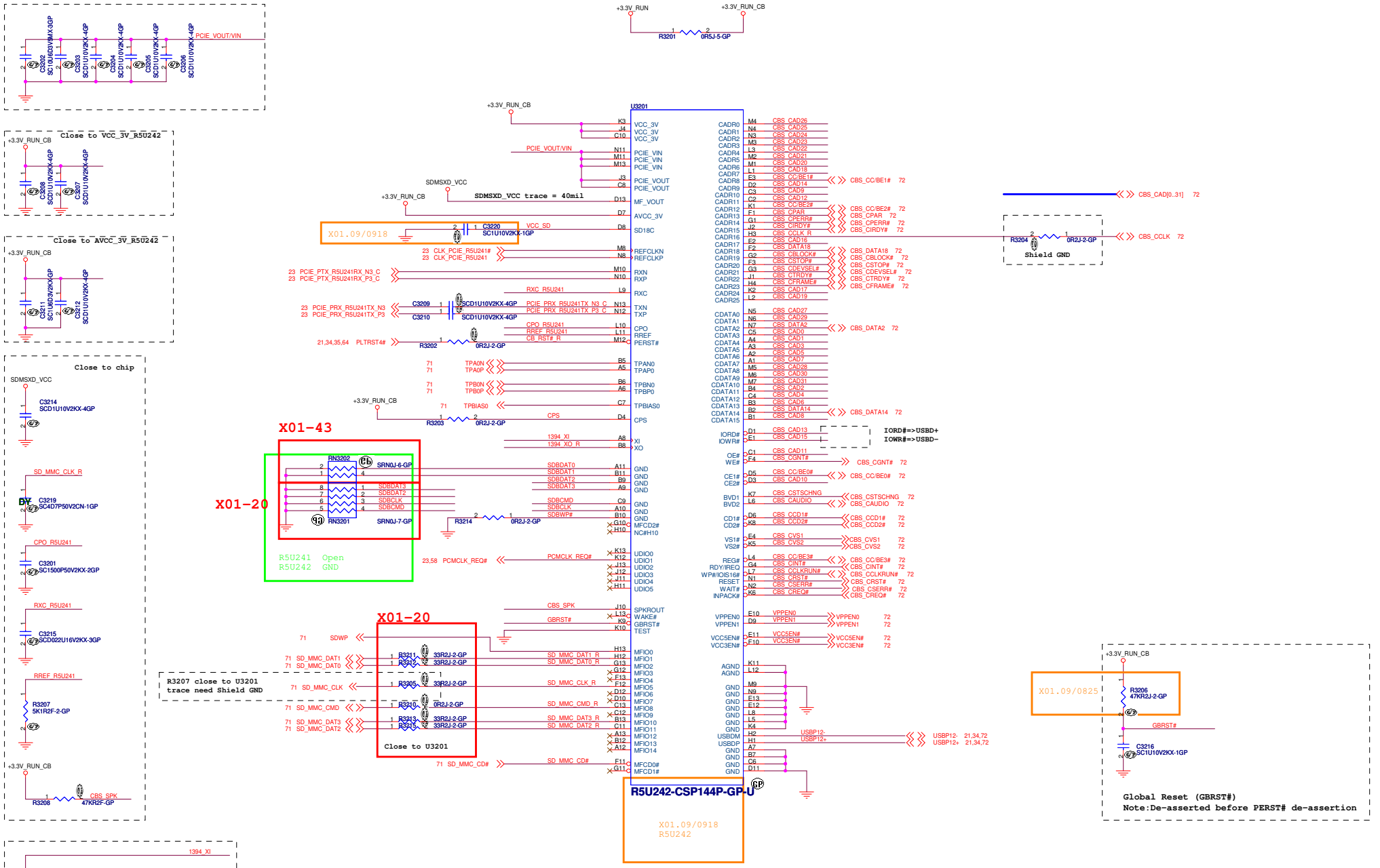
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserve

Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 31 of 82

SSID = 1394



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Flash Reader / 1394 / PCMCIA**

Size	Document Number	Rev
C	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 32 of 82

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

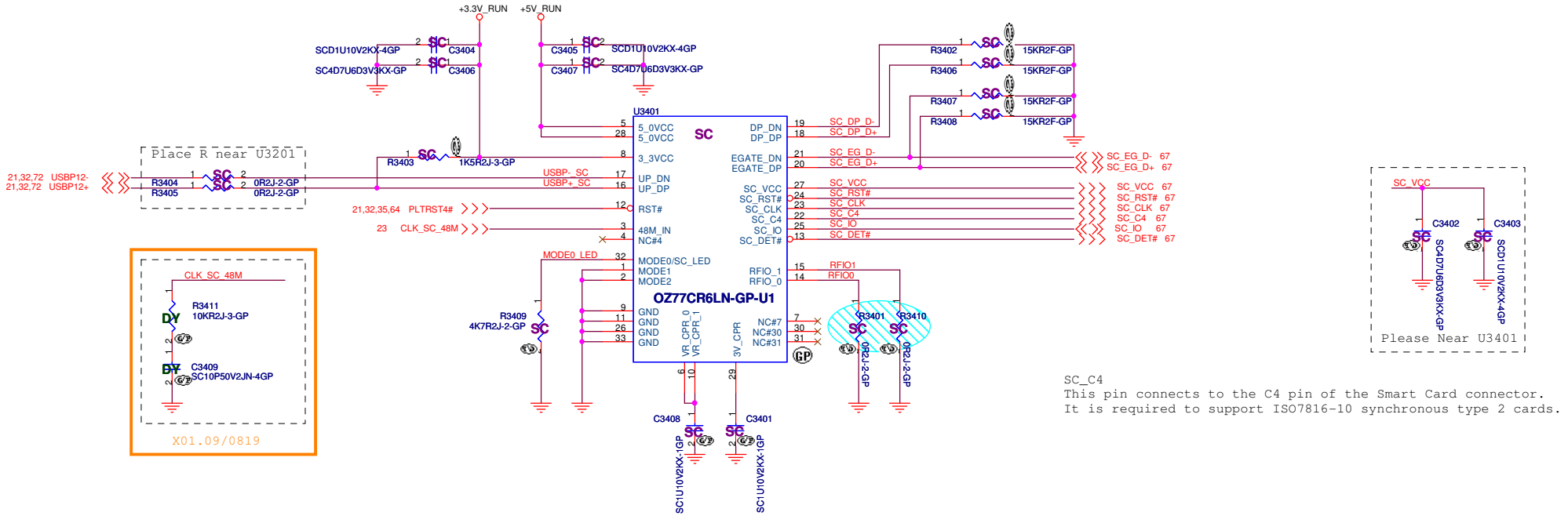
Title: *Reserve*

Size: Custom | Document Number: *Fonseca UMA* | Rev: *X01*

Date: Thursday, October 29, 2009 | Sheet 33 of 82

SSID = SmartCard

SmartCard Chip



VR filter.
An external capacitor shall connect to this terminal.

SC_C4
This pin connects to the C4 pin of the Smart Card connector.
It is required to support ISO7816-10 synchronous type 2 cards.

MODE0 / SC_LED	This terminal is an output indicating Smart Card activity; capable to drive an external LED device. The SC_LED terminal drives a low logic level during Smart Card data read/write activity, and is capable to source 12mA of IOL current to drive an external LED circuit. When RST# is asserted, this terminal is sampled to select the downstream port configuration for DP_DP and DP_DN (Internal Port 1). When sampled low (4.7k), the downstream port device is removable. When sampled high, the downstream port is a non-removable device. Includes internal input pull-up resistor.
MODE1	Test Pin. This terminal shall be externally connected to GND.
MODE2	Test Pin. This terminal shall be externally connected to GND.

RFIO_0 **RFIO_1**	Contactless Smart Card Interface Signal 0 and 1. This signal provides detection and data communication with an external RF device. If contactless is disabled, then this terminal shall be pulled-down to GND through a pull-down resistor, or directly connected to GND.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Smart Card (OZ77CR6LN)*

Size: Custom | Document Number: *Fonseca UMA* | Rev: *X01*

Date: Thursday, October 29, 2009 | Sheet 34 of 82

SSID = LOM

Symbol : 71.05761.00U
Product : P802H (Rev:B0)

X01.09/0825

Core Power Decoupling

VDDIOPower Decoupling

Put 0.1u cap close to Chip

Co-Layout

U3505

U3506

X01-22

Populate resister for debug

Close to the power pins and
0.1u cap should be closer to Chip

X01-39

Design current: 89.6mA
Max current: 128mA

DOCKED
SEL 0:RJ45.
SEL 1:Dock.

8Mb for 5761E:
Main source: 72.45081.C01(Big PAD)
2nd source: 72.45081.B01(Small PAD)

X01.09/0917

CTPM and DisableBTPM

X01.09/0819

Reserve for EMI

Logic High Voltage must
be 0.7V to 2.75V

X01.09/0918

Place crystal less
than 0.75" (~1.9cm)
from LAN Controller

Design Current: 627mA

U3501A

U3501B

BCM5761EA0KFBG-GP

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GLAN - BCM5761E

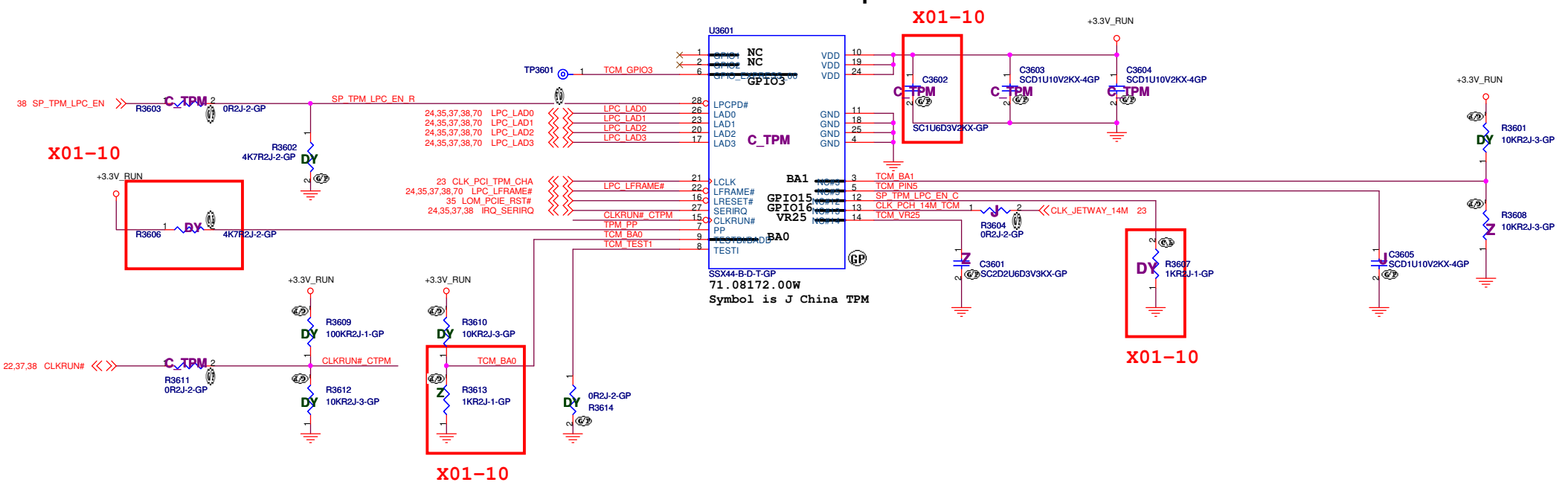
Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 35 of 82

SSID = TCM

Symbol : Jetway, but linked to ZTE
Product : 71.08172.00W (ZTE)

China TPM Chip



Z

Base Address	BA1 PIN3	BA0 PIN9
EE/EF	0	0
7E/7F	0	1
2E/2F	1	0
4E/4F	1	1

Default EE/EF as Amy recommended

J

	1(default)	0
PIN12	FLASH	SRAM

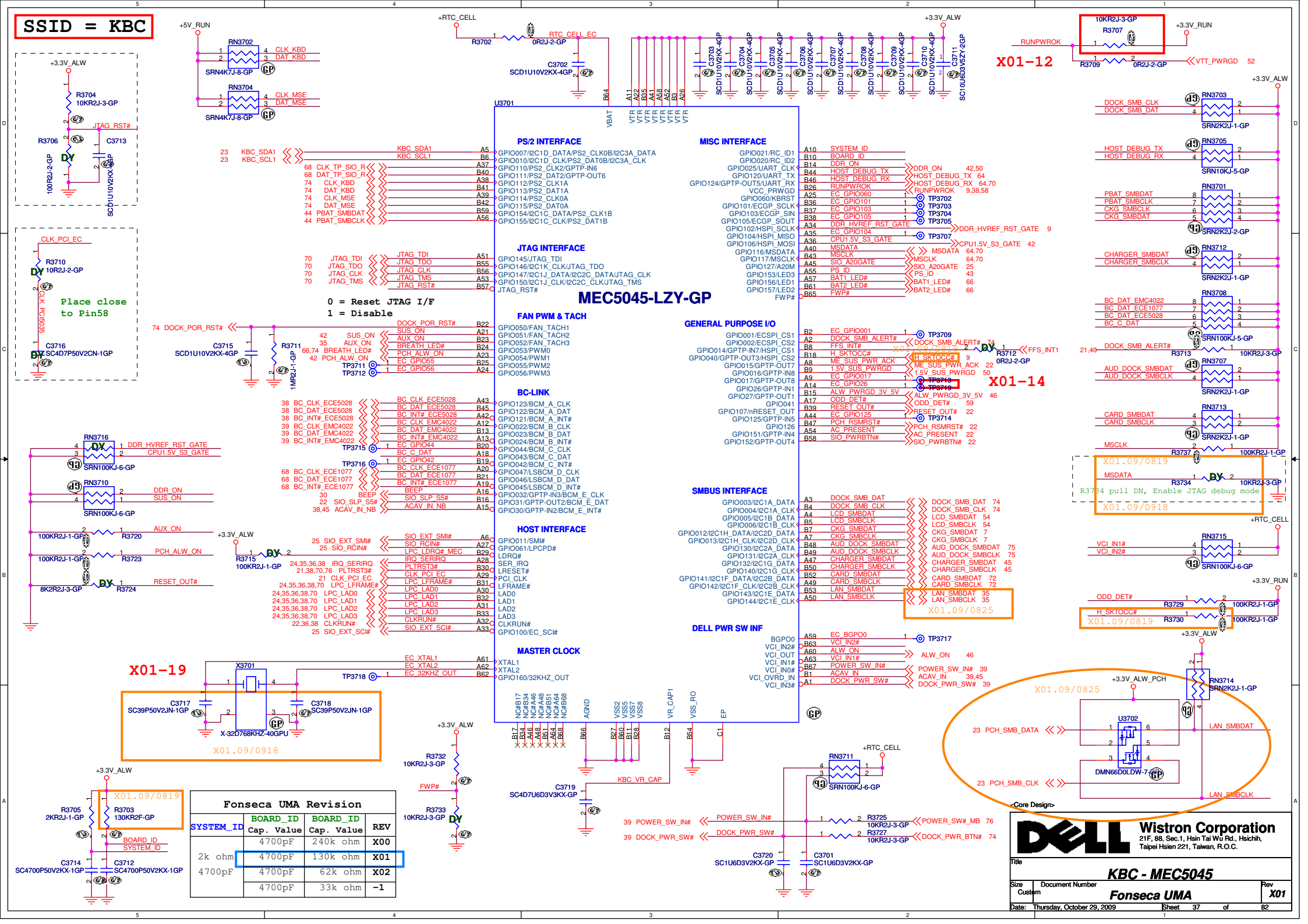
J has internal PU with PIN12.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TCM
Size: Custom | Document Number: Fonseca UMA | Rev: X01
Date: Thursday, October 29, 2009 | Sheet 36 of 82

SSID = KBC


MEC5045-LZY-GP
U3701
PS/2 INTERFACE
JTAG INTERFACE
FAN PWM & TACH
BC-LINK
HOST INTERFACE
MASTER CLOCK
MISC INTERFACE
GENERAL PURPOSE I/O
SMBUS INTERFACE
DELL PWR SW INF
0 = Reset JTAG I/F
1 = Disable
Place close to Pin58
X01-12
X01-14
X01-19
Fonseca UMA Revision
Wistron Corporation
KBC - MEC5045
Fonseca UMA

SSID = KBC

X01-30

X01.09/0917

X01.09/0918

VGA_IDENTIFY
High = Discrete
Low = UMA

Place close to Pin.A28

Place close to Pin.A32

CRD_DET1	CRD_DET0	Function
Low	Low	No Option Installed
Low	High	Smartcard
High	Low	Cardbus
High	High	Express Card

<Core Design>

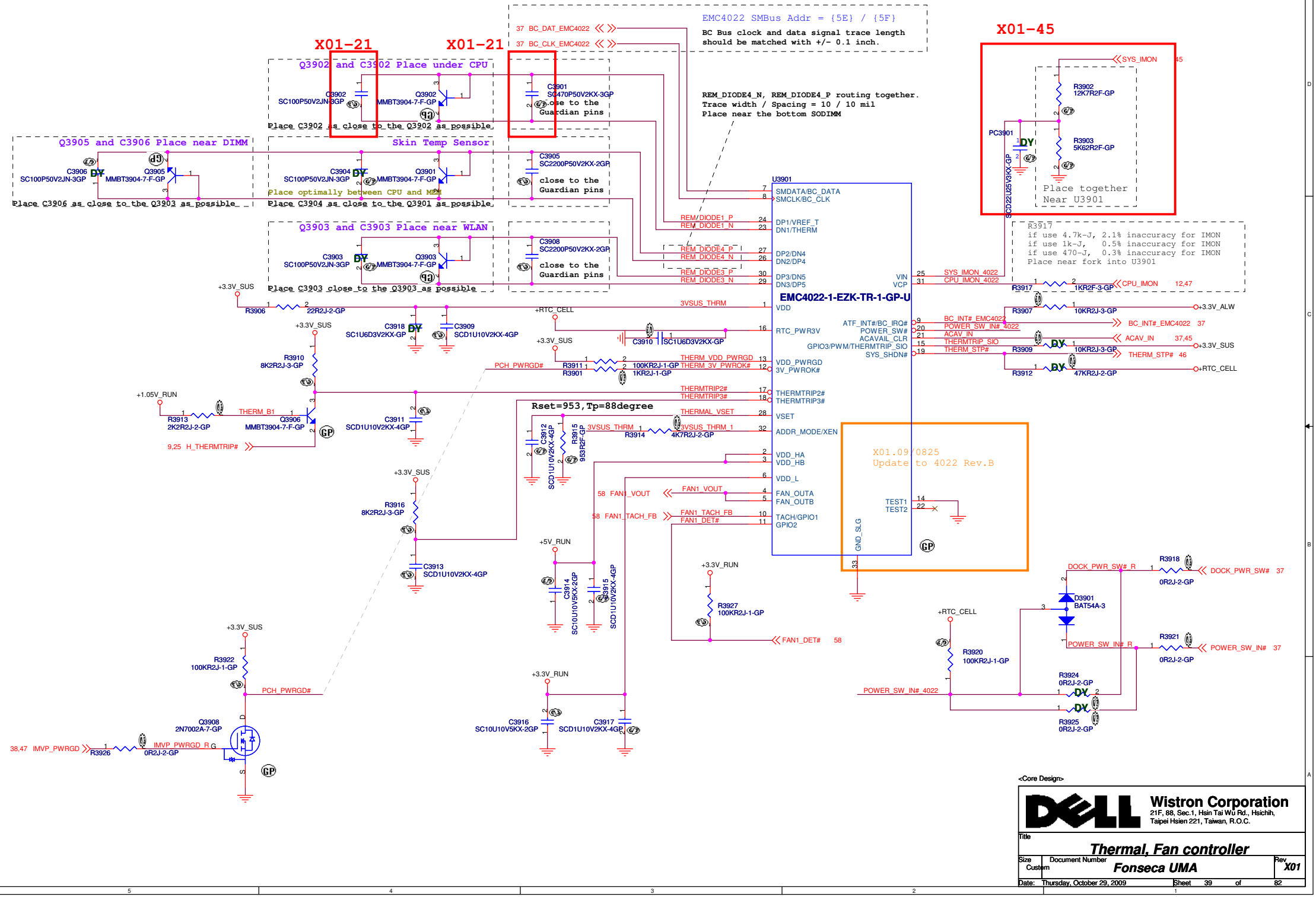
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SIO - MEC5028

Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 38 of 82

SSID = Thermal



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

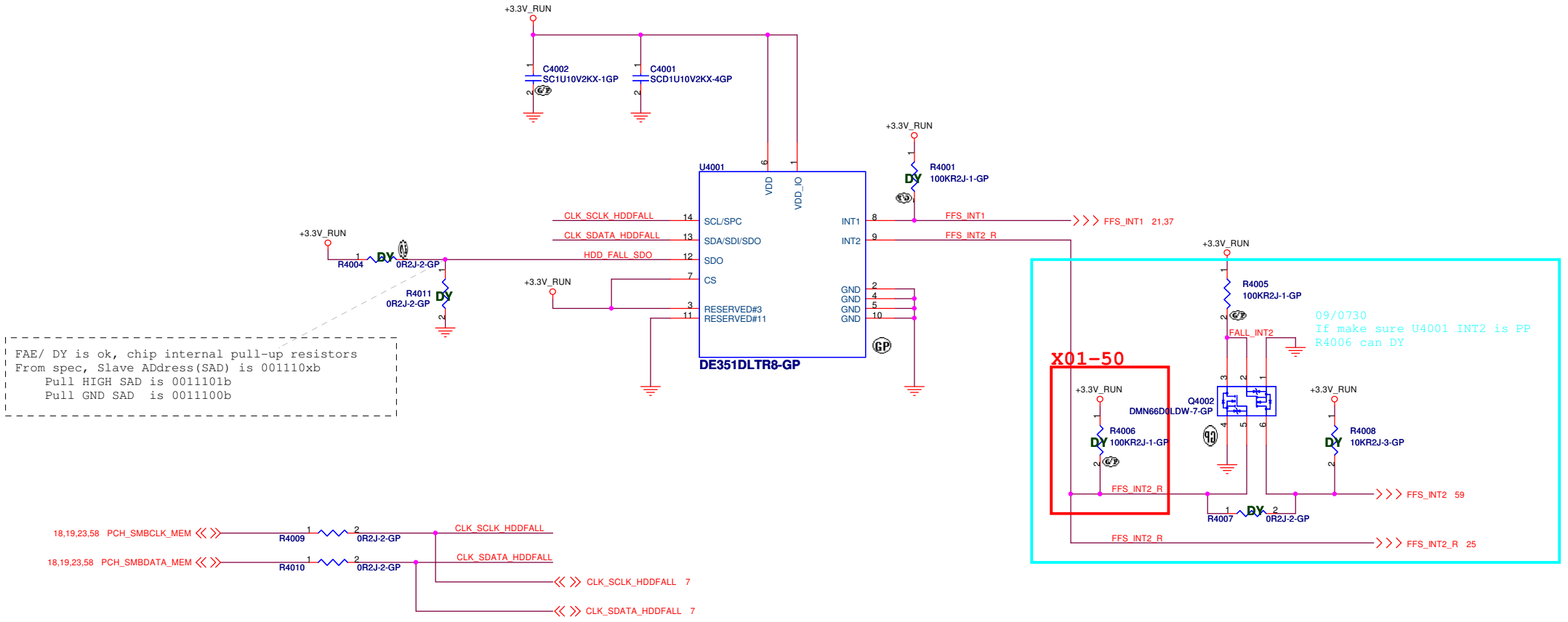
Title: Thermal, Fan controller

Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 39 of 82

SSID = User.Interface

Free Fall Sensor



Layout Note
- no via, trace, under the sensor
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor
Size: A3 | Document Number: Fonseca UMA | Rev: X01
Date: Thursday, October 29, 2009 | Sheet 40 of 82

SSID = Reset.Suspend

<Core Design>

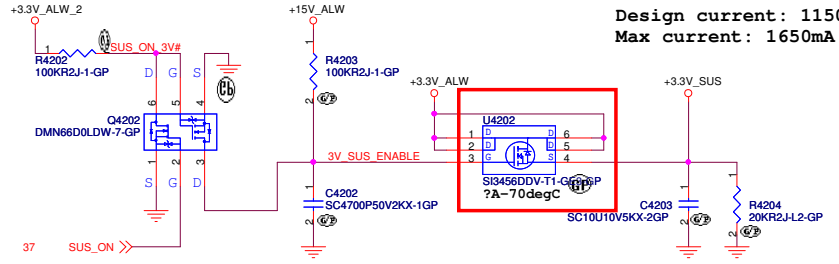
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power On Logic

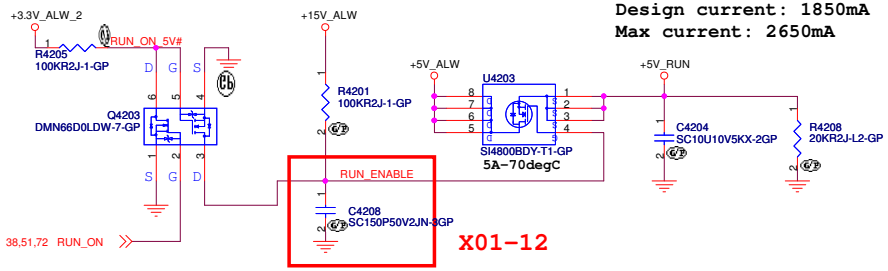
Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 41 of 82

SSID = Reset.Suspend

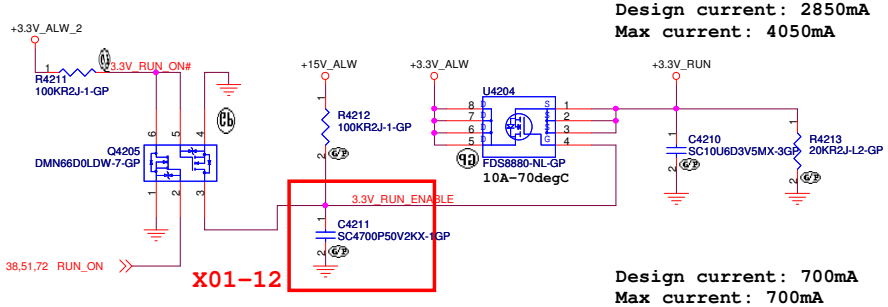


Design current: 1150mA
Max current: 1650mA



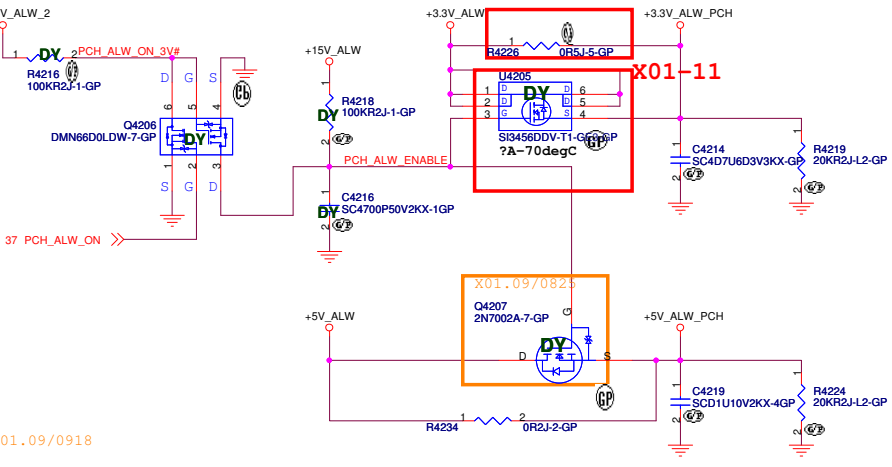
Design current: 1850mA
Max current: 2650mA

X01-12



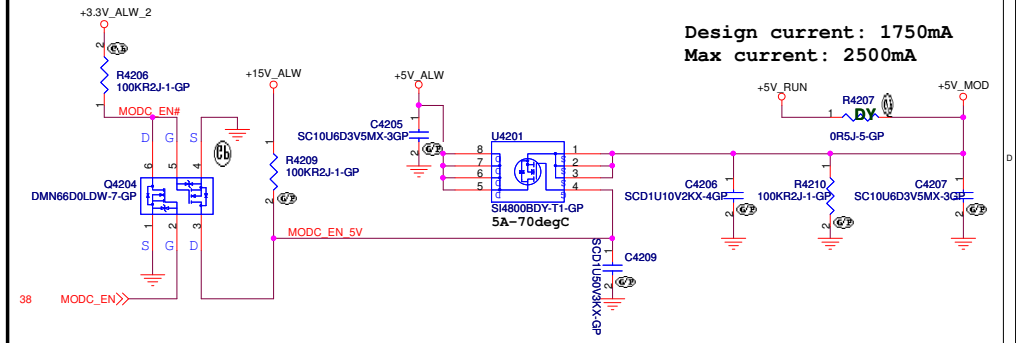
Design current: 2850mA
Max current: 4050mA

X01-12

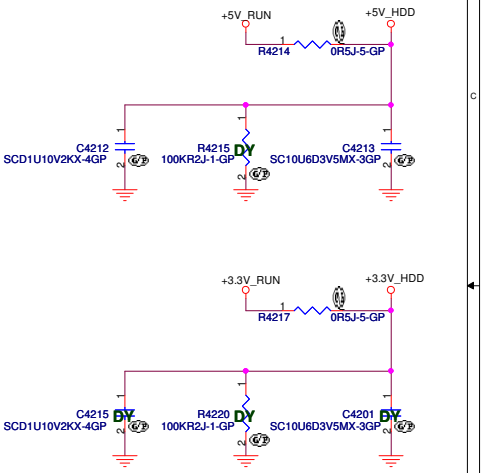


Design current: 700mA
Max current: 700mA

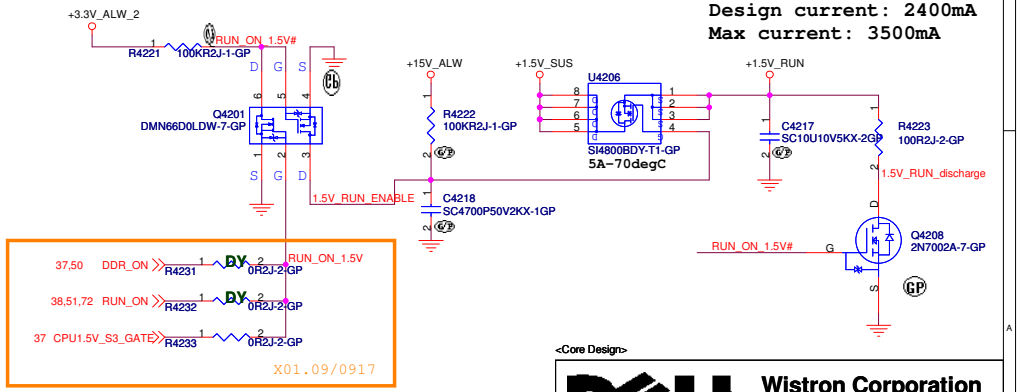
X01-11



Design current: 1750mA
Max current: 2500mA



Design current: 700mA
Max current: 1000mA



Design current: 2400mA
Max current: 3500mA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
Custom	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 42 of 82

SSID = PWR.Support

Adapter In

DC_IN CONN	
PIN 1,2,3	DC_IN+
PIN 4,5	DC_IN-
PIN 1	ID
PIN 6,7,8,9	GND

PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL	BQ24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMP	FBO
7	DAC	NC	CE
8	IINP	ICM	VICM
11	VDD	VDDSMB	VDDSMB
14	BATSEL	NC	NC
15	FBSA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSON	CSON
18	CSIP	CSOP	CSOP
20	DLO	LGATE	LGATE
21	LDO	VDDP	VDDP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGSTE
25	BST	BOOT	BOOT
26	VCC	VCC	ICOUT

"NC" means no-connect

TABLE
MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL	TI
R411	8.45K 1%	DUMMY	DUMMY
C98	0.01uF	0.1uF	0.1uF
C459	0.1uF 10V	DUMMY	200P 10V
C5	1uF 10V	DUMMY	1uF 10V
R16	365K 1%	215K 1%	309K 1%
R434	0 5%	10 5%	0 5%
R414	0 5%	10 5%	0 5%
C473	DUMMY	0.22uF	0.1uF
C457	DUMMY	0.22uF	0.1uF
C442	0.01uF	DUMMY	DUMMY
C453	0.1uF 10V	DUMMY	DUMMY
C36	220pF 50V	DUMMY	DUMMY
D23	RB751V-40	DUMMY	RB751V-40
C58	3.3nF	DUMMY	DUMMY
R64	1 1%	0 5%	0 5%
R394	100 5%	0 5%	0 5%
R110	0 5%	8.45K 1%	8.45K 1%
R401	10K 5%	2.2K 5%	4.7K 5%
C441	0.01uF	0.01uF	DUMMY
C449	0.01uF	0.01uF	DUMMY
R397	1K 5%	DUMMY	DUMMY
Q41	ISS355	DUMMY	DUMMY
C16	1uF 10V	1uF 10V	DUMMY
R30	33 1%	33 1%	DUMMY
R408	DUMMY	DUMMY	0 5%
R400	DUMMY	DUMMY	200K 5%
R403	DUMMY	DUMMY	7.5K 5%
C450	DUMMY	DUMMY	51P 10V
C444	DUMMY	DUMMY	2000P 10V
C448	DUMMY	DUMMY	130P 10V
C446	DUMMY	DUMMY	0.1uF
C483	DUMMY	DUMMY	0.1uF
R438	10K 1%	10K 1%	DUMMY
R412	DUMMY	DUMMY	10k 5%
R440	15.8K 1%	15.8K 1%	DUMMY
R407	DUMMY	10K 5%	DUMMY
R9	0 5%	10 5%	0 5%
C482	DUMMY	DUMMY	DUMMY
C12	DUMMY	DUMMY	DUMMY
R435	0 5%	10 5%	0 5%

MAX 8731A/ISL88731

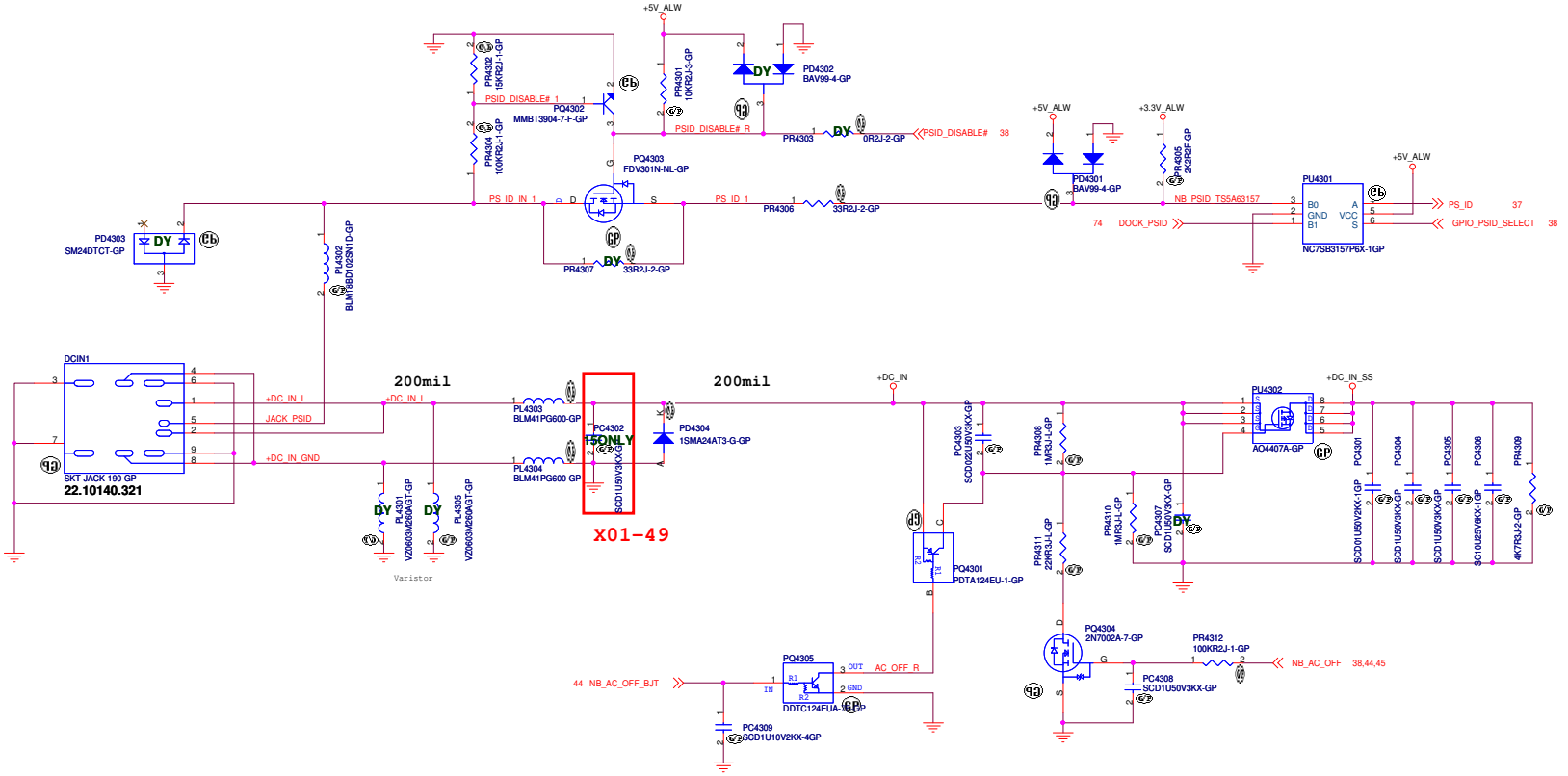
Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	13.0K	105	24.9K
90	4.43	51.1K	17.8K	348	33.2K

*R504 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

BQ247451

Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	12.4K	205	24.3K
90	4.43	51.1K	16.9K	499	32.4K

*R504 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.



<Core Design>

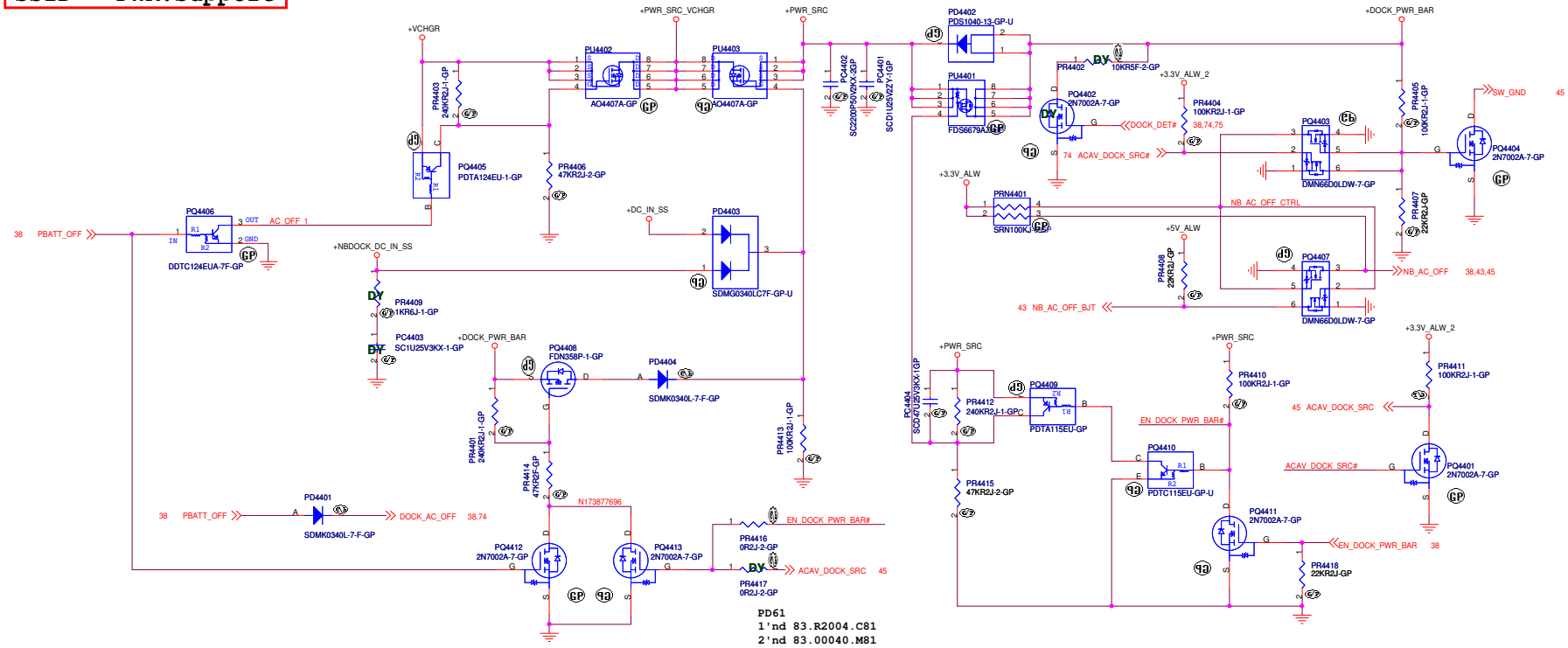
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC IN Jack

Size	Document Number	Rev
C	Fonseca UMA	X01

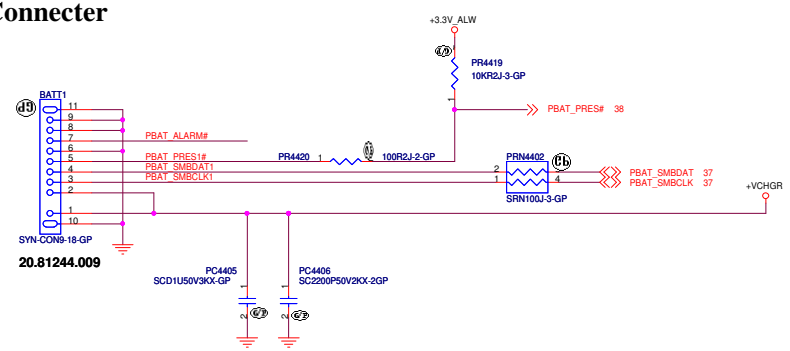
Date: Thursday, October 29, 2009 Sheet 43 of 82

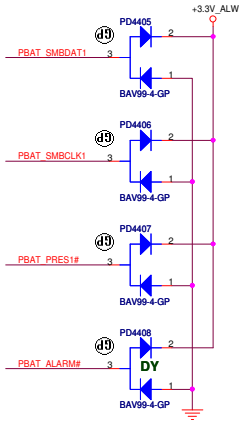
SSID = PWR.Support



SSID = RBATT

Batt Connecter





<Core Design>

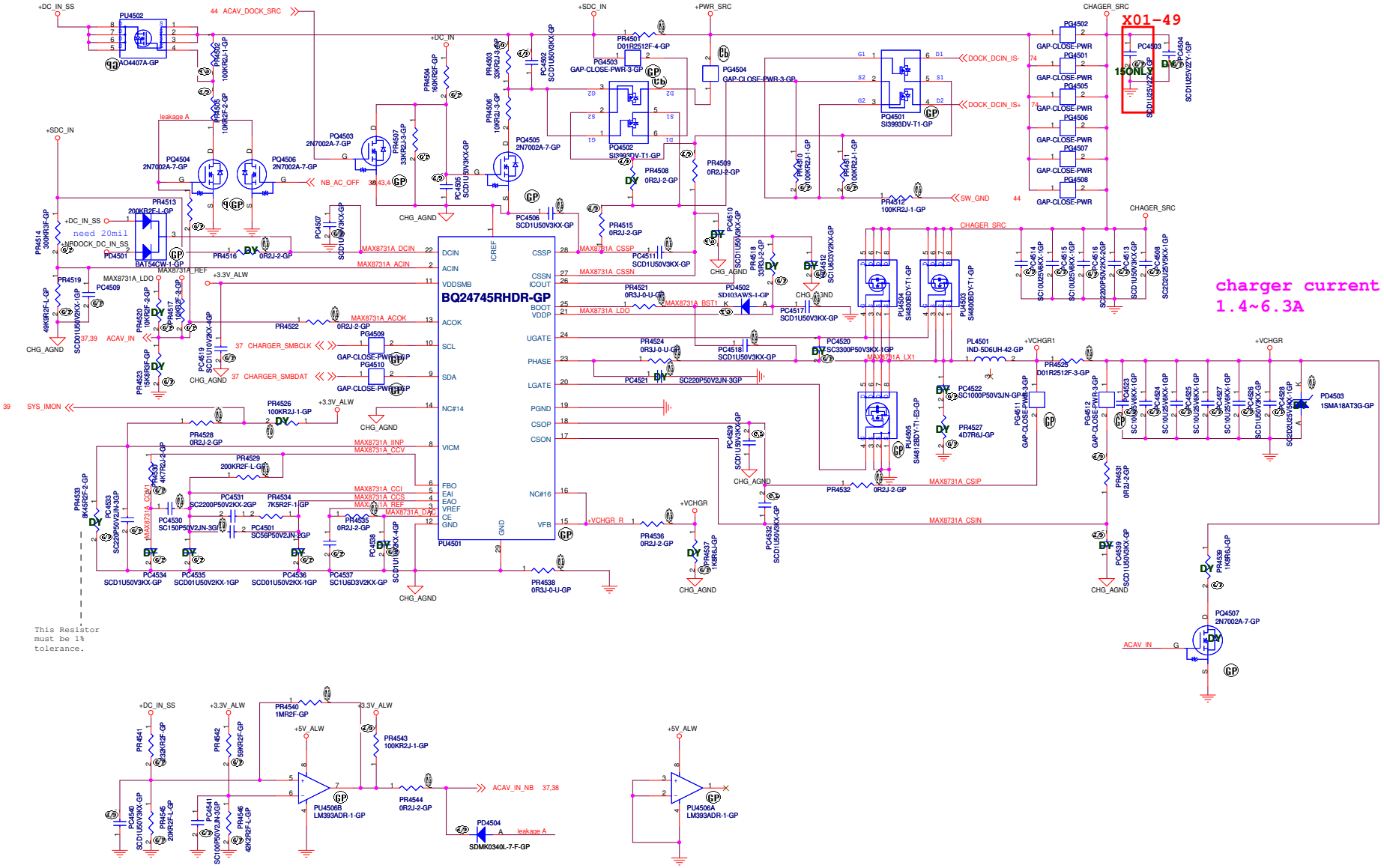
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DOCK DCIN/BATT Connector

Size	Document Number	Rev
C	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 44 of 82

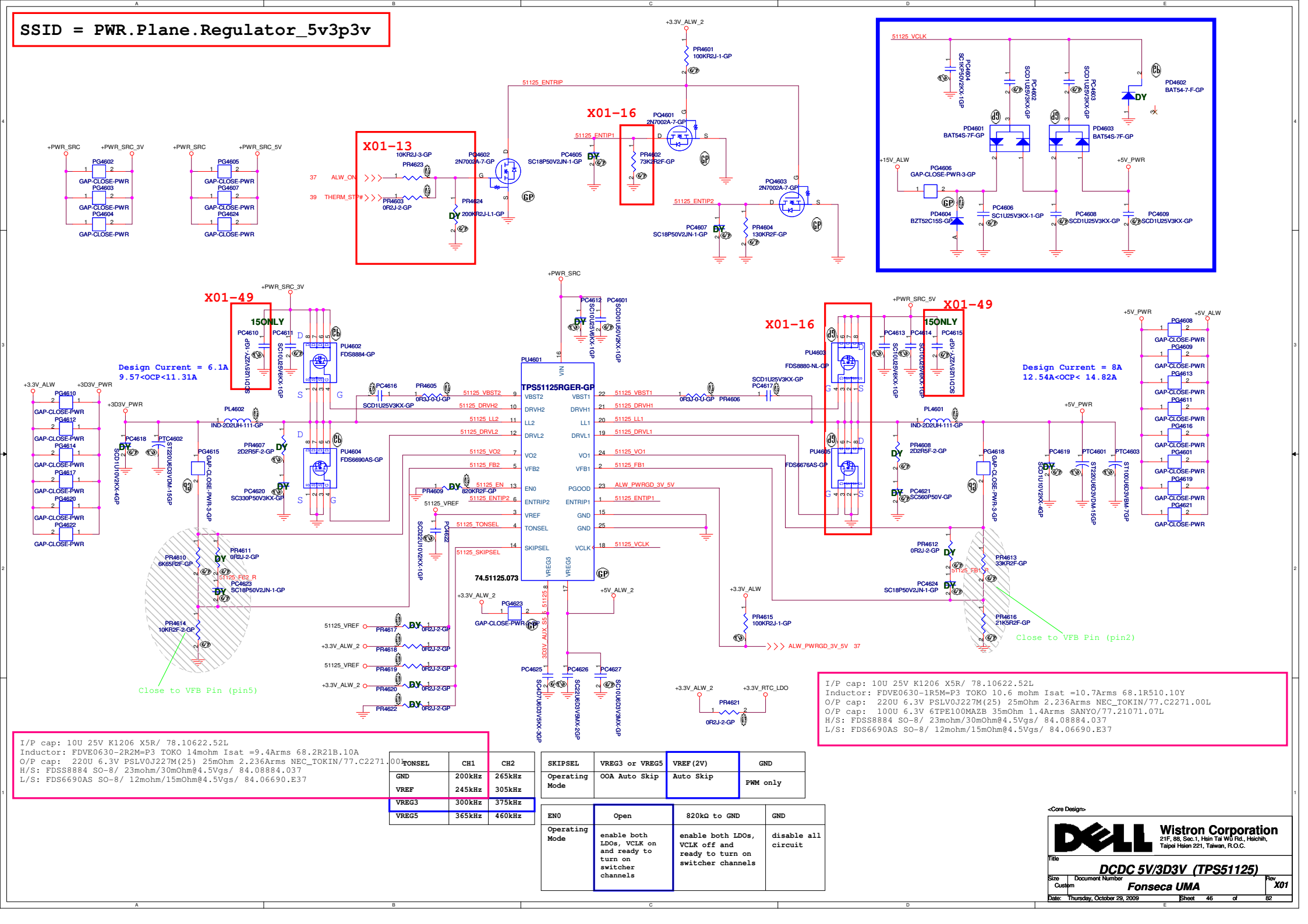
SSID = Charger



<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **Battery Charger**		
Size: C	Document Number: Fonseca UMA	Rev: X01
Date: Thursday, October 29, 2009	Sheet 45 of 82	

SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: FDVE0630-2R2M=P3 TOKO 14mohm Isat =9.4Arms 68.2R21B.10A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: FDVE0630-1R5M=P3 TOKO 10.6 mohm Isat =10.7Arms 68.1R510.10Y
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V 6TPE100MAZB 35mOhm 1.4Arms SANYO/77.21071.07L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

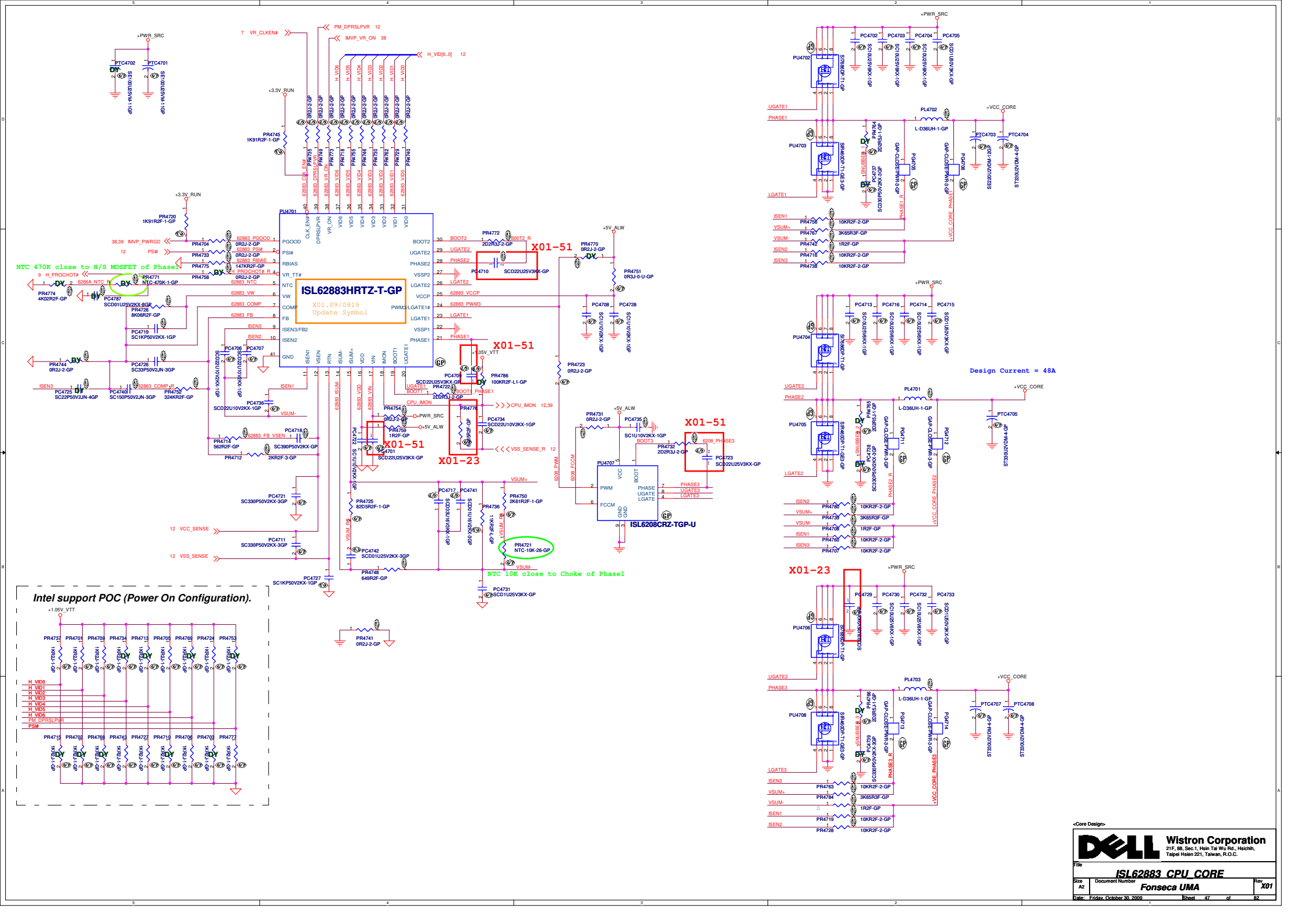
SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 5V/3D3V (TPS51125)
Size: Custom | Document Number: Fonseca UMA | Rev: X01
Date: Thursday, October 29, 2009 | Sheet 46 of 82



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE

Size: A2 | Document Number: Fonseca UMA | Rev: X01

Date: Friday, October 30, 2009 | Sheet 47 of 82

<Core Design>

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: A3 | Document Number: *Fonseca UMA* | Rev: *X01*

Date: Thursday, October 29, 2009 | Sheet 48 of 82

SSID = PWR.Plane.Regulator_1p05v

(Blank)

<Core Design>

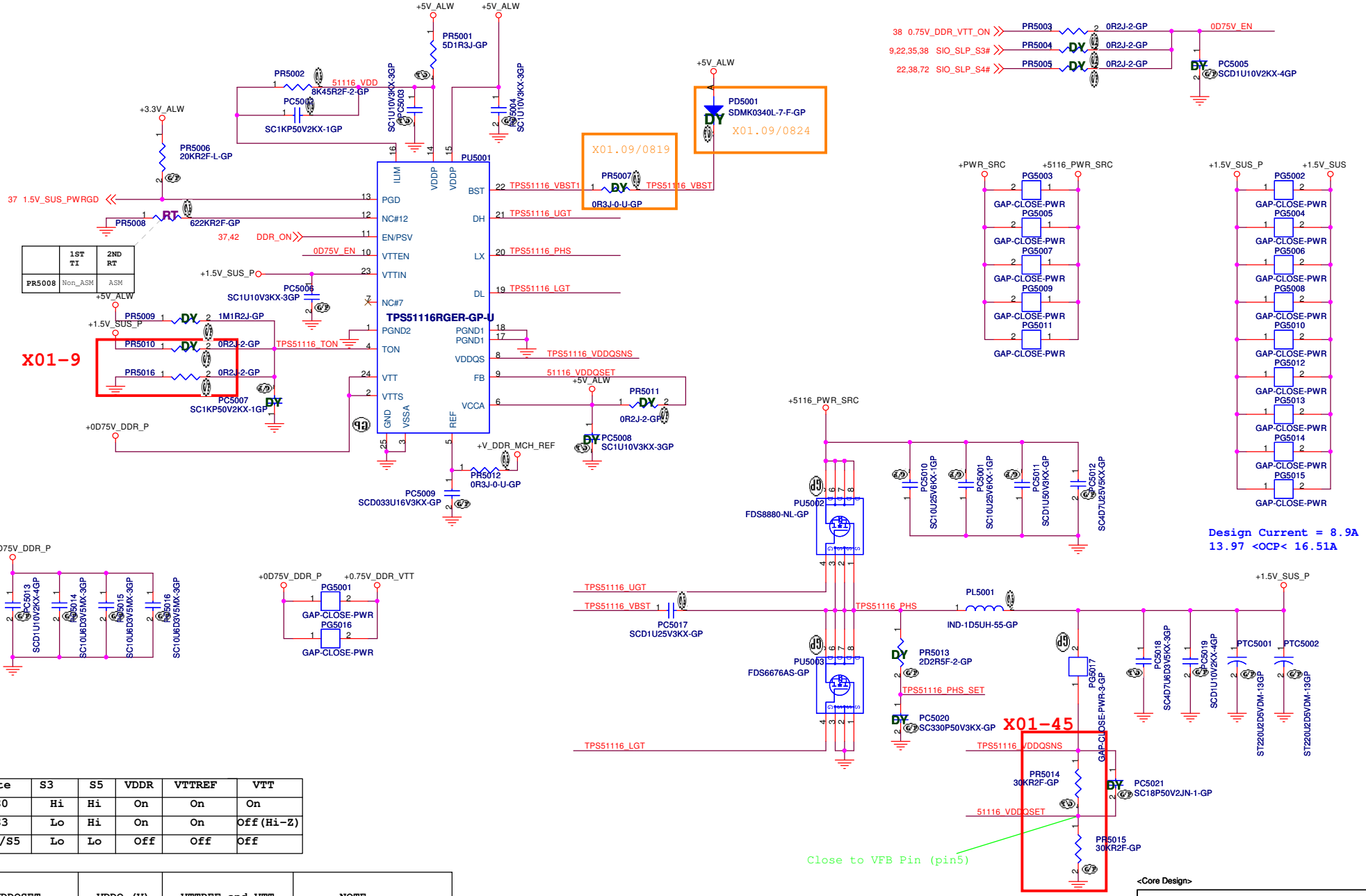
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.05V

Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 49 of 82

SSID = PWR.Plane.Regulator_1p5v0p75v



	1ST TI	2ND RT
PR5008	Non_ASM	ASM

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: FDV1040-1R5M=P3 TOKO DCR:3.86 mohm Isat =19.7Arms 68.1R510.10Q
O/P cap: TLPSLV0G227M(25)12RE 25mOhm 2.5Arms NEC_TOKIN/ 77.C2271.07L
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->400KHz

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

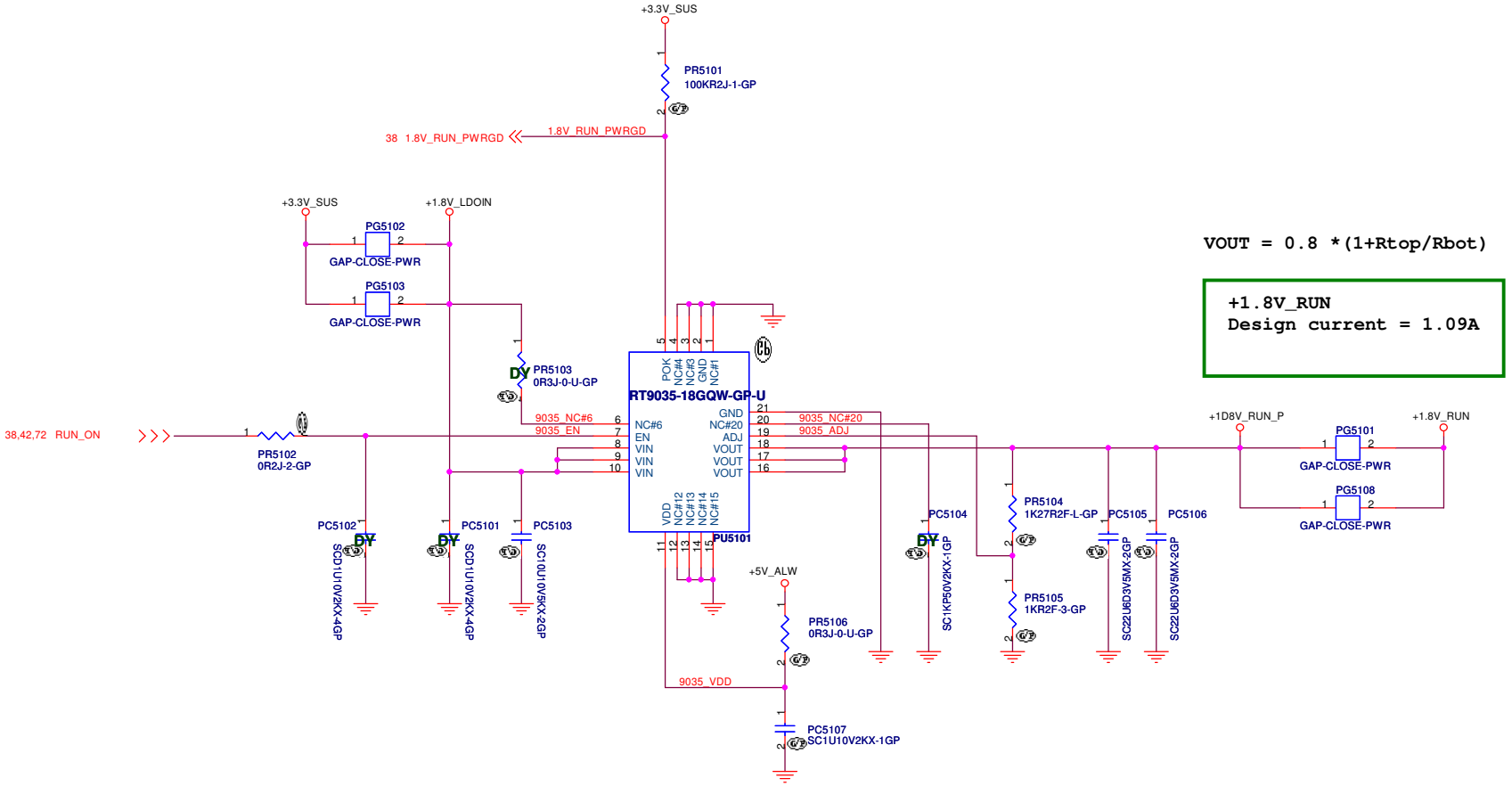
Title: DC to DC 1.5V / 0.75V

Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 50 of 82

SSID = PWR.Plane.Regulator_1p8v

LDO for +1.8V_RUN



VOUT = 0.8 *(1+Rtop/Rbot)

+1.8V_RUN
Design current = 1.09A

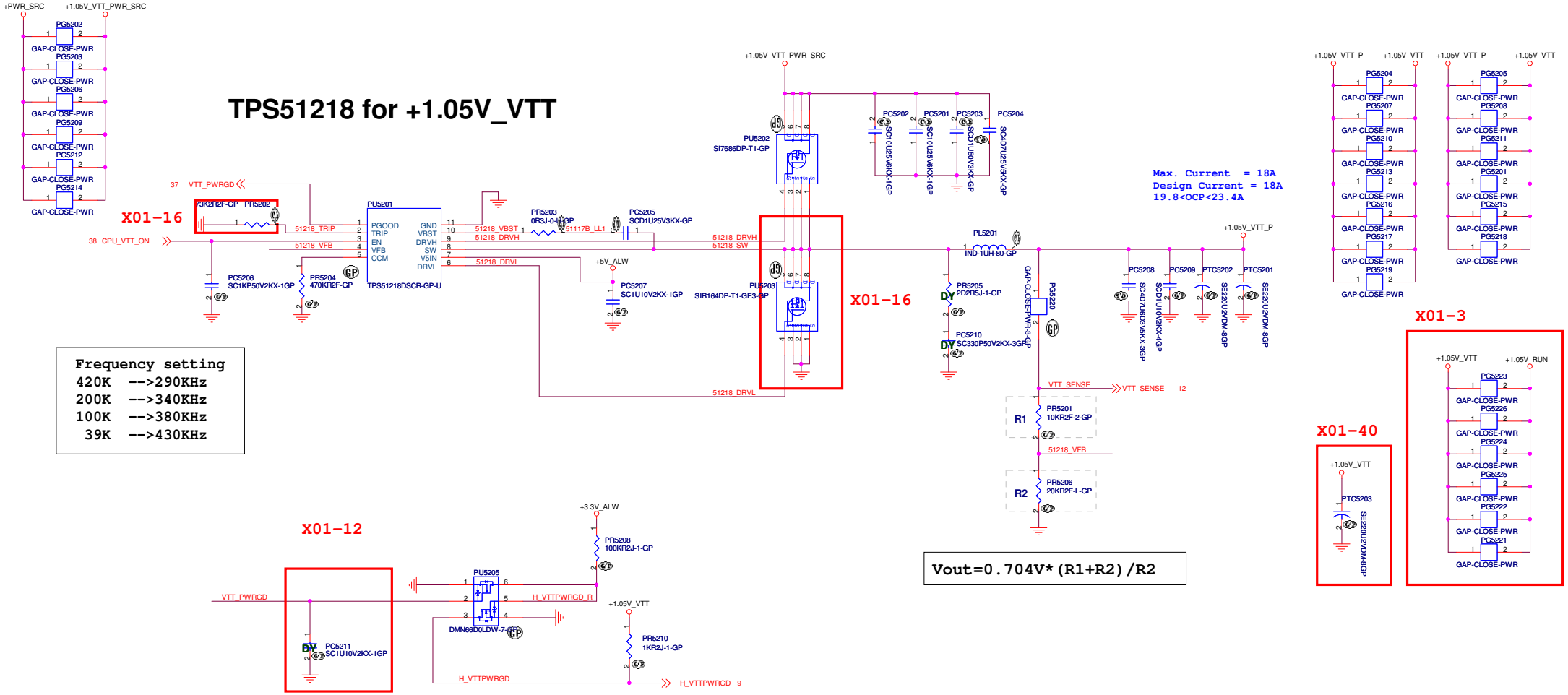
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC to DC +1.8V_RUN	
Size: A3	Document Number: Fonseca UMA	Rev: X01
Date: Thursday, October 29, 2009	Sheet 51 of 82	

SSID = PWR.Plane.Regulator_1p05v

TPS51218 for +1.05V_VTT



Frequency setting

420K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

<Core Design>

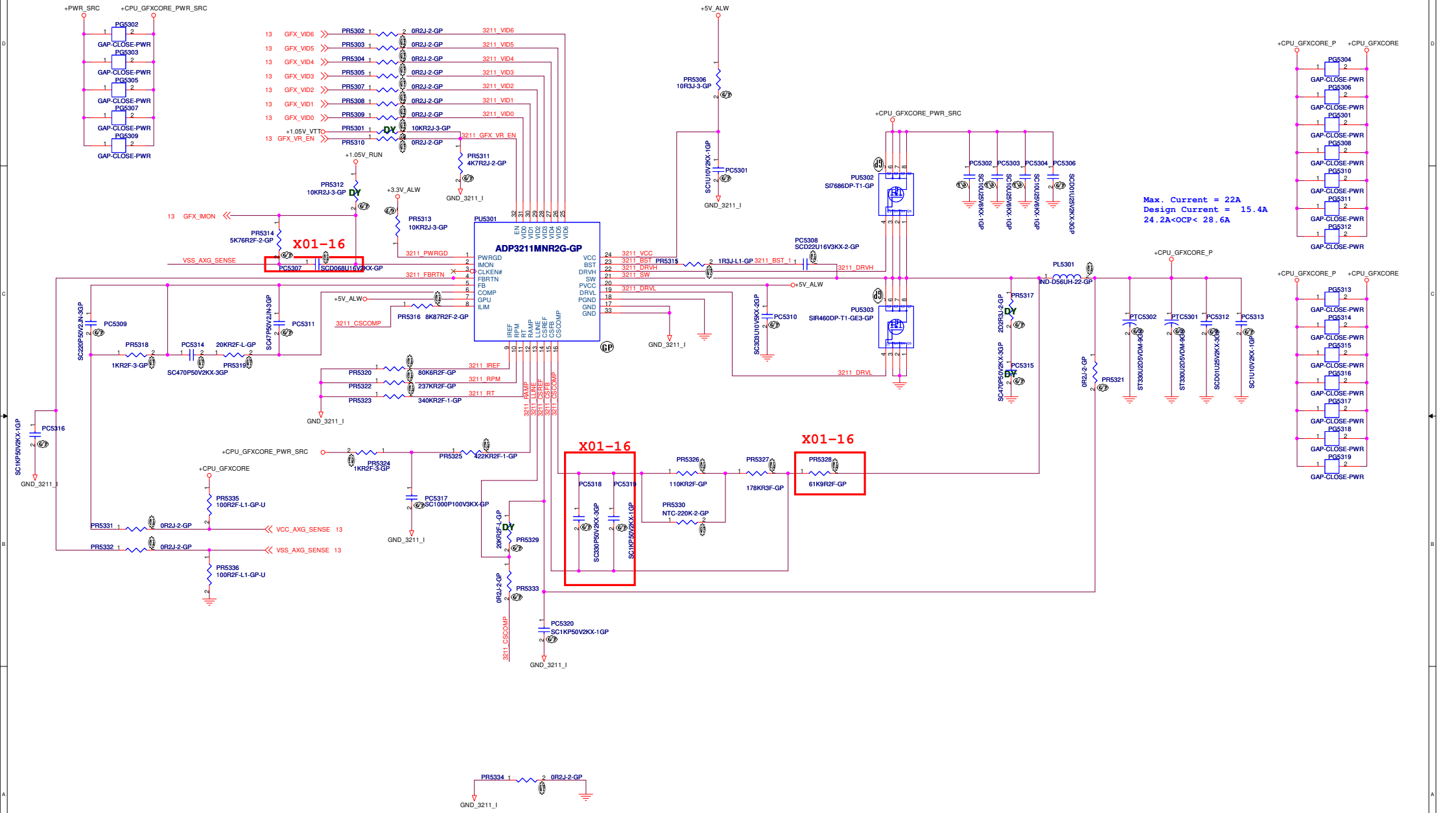
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC +1.05V_VTT

Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 52 of 82

SSID = CPU.GFX.Regulator



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP3211 CPU_GFXCORE

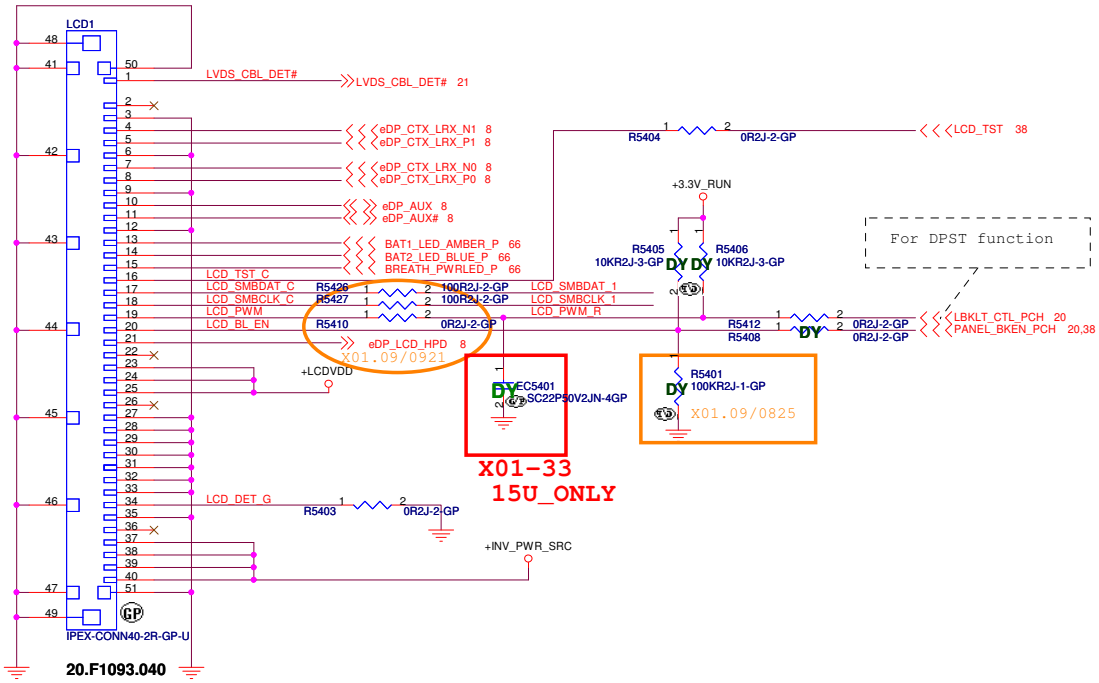
Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 53 of 82

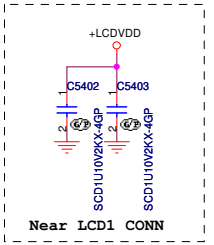
SSID = VIDEO

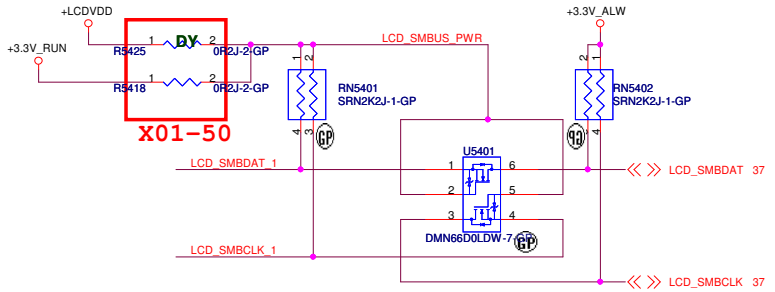
LED Location from left to right

HDD | BATTERY

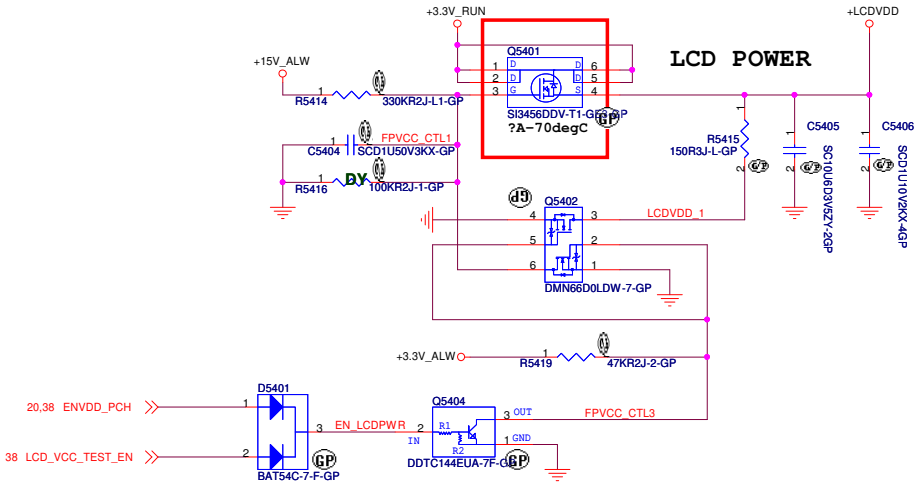


X01.09/0825



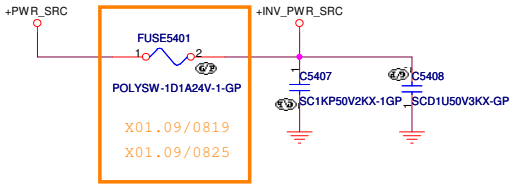


SSID = VIDEO



SSID = Inverter

LED BACKLIGHT CONVERTER POWER



<Core Design>

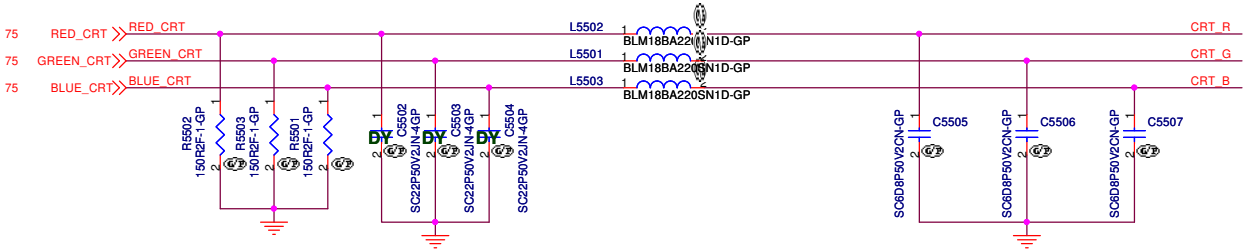
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

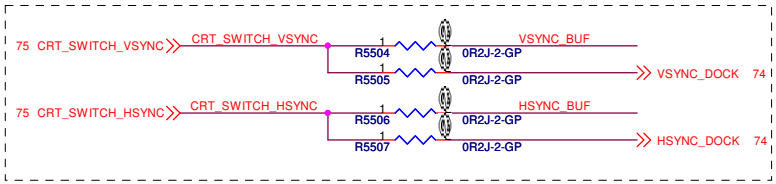
Title: LCD

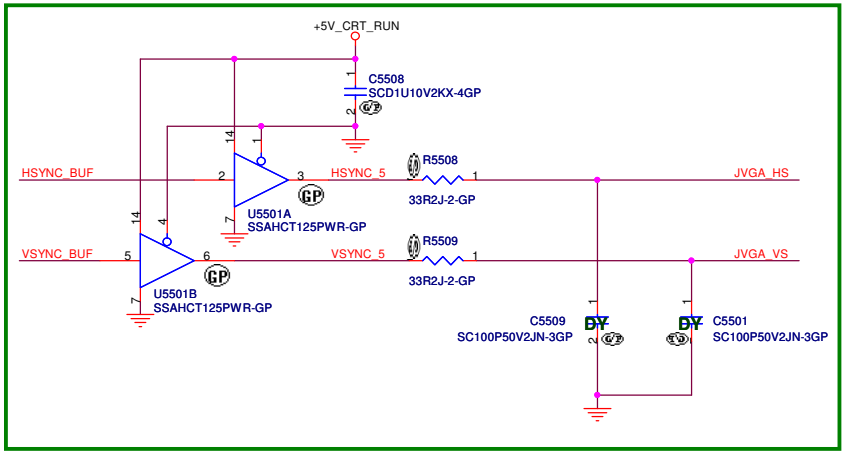
Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 54 of 82

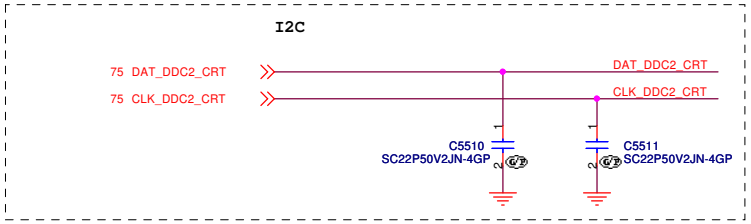
SSID = VIDEO



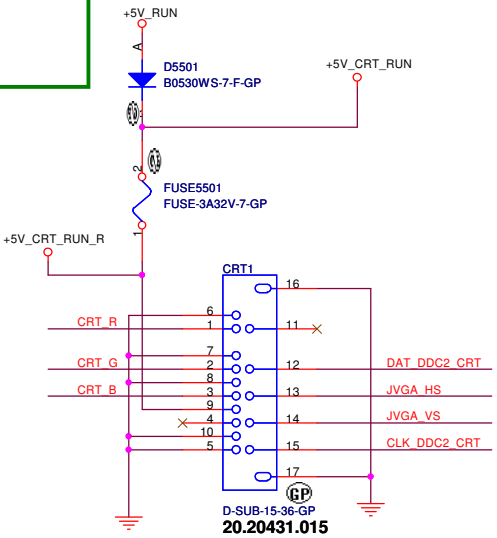




Layout Note:
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



MAX4885E has internal ESD protection and internal level shift



CRT Connector

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT		
Size: A3	Document Number: Fonseca UMA	Rev: X01
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: A3 | Document Number: *Fonseca UMA* | Rev: *X01*

Date: Thursday, October 29, 2009 | Sheet 56 of 82

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

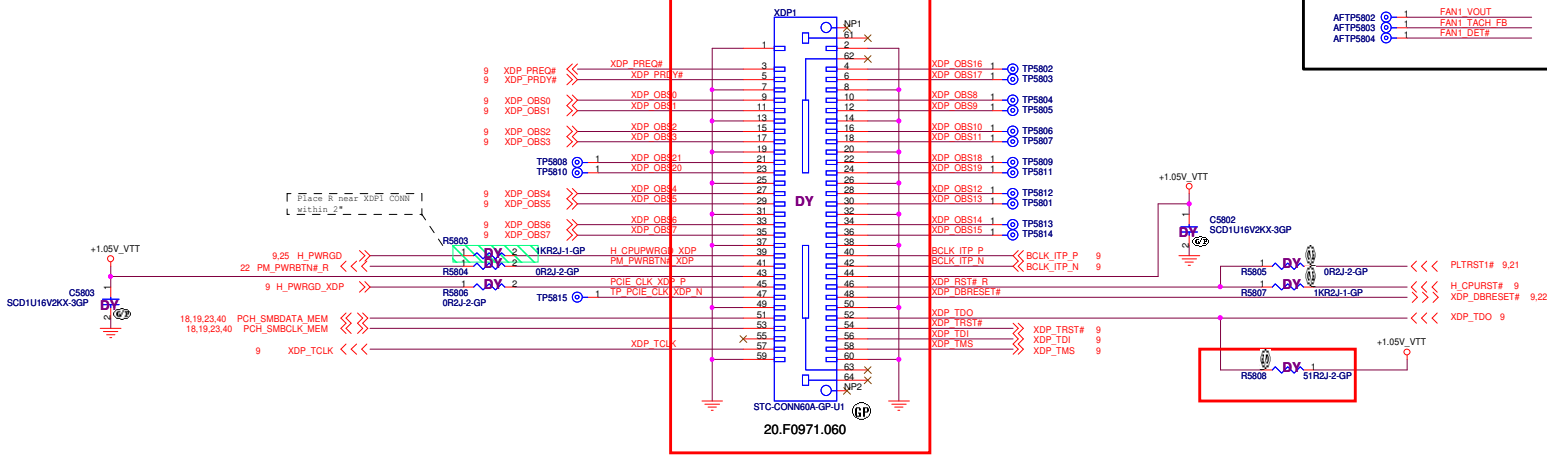
Size: A3 | Document Number: *Fonseca UMA* | Rev: *X01*

Date: Thursday, October 29, 2009 | Sheet 57 of 82

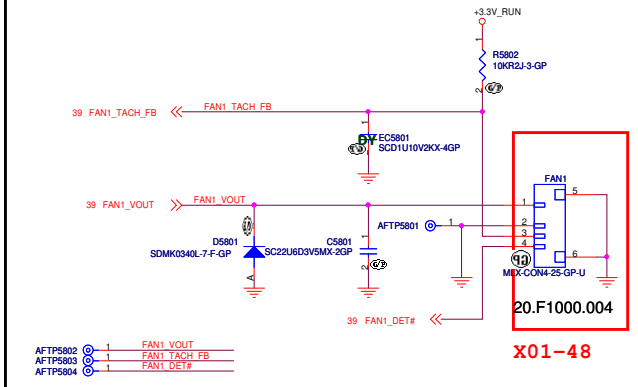
SSID = CPU

X01-7

CPU XDP



SSID = Thermal

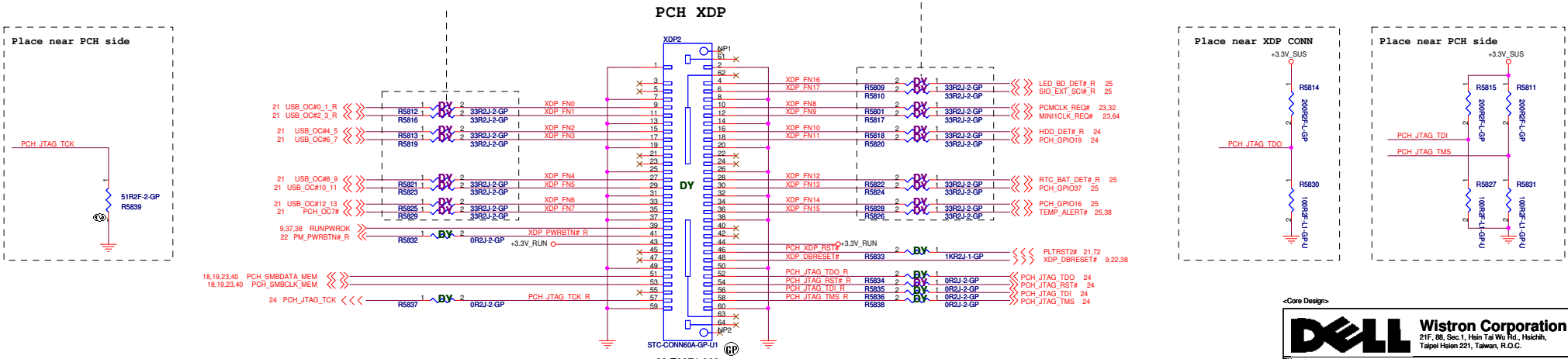


X01-48

SSID = PCH

A 33 ohm series resistor should be placed within 1 inch (or 25.4 mm) of the PCH to source terminate the interface.

PCH XDP



<Core Design>

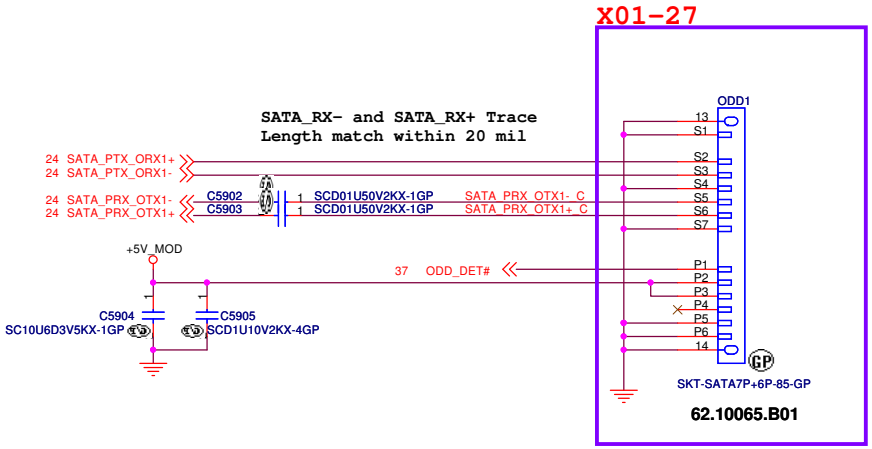
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserve

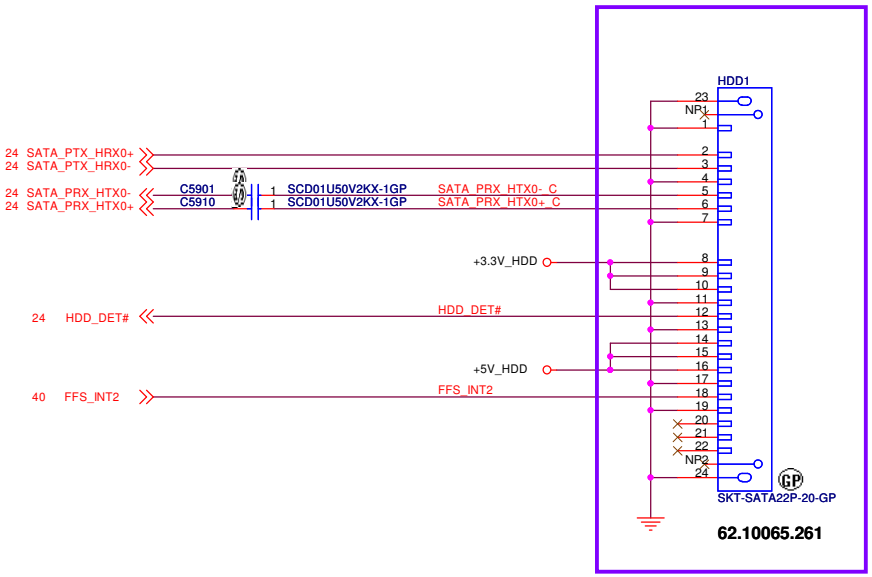
Size	Document Number	Rev
C	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 58 of 82

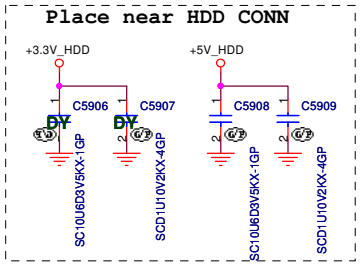
SSID = SATA SATA ODD Connector



SSID = SATA SATA HDD Connector




```
SATA HDD Interface comment
******************************
--- GND
RX+
RX-
--- GND
TX-
TX+
--- GND
******************************
------------ 3.3V
------------ 3.3V
------------ 3.3V
--- GND
--- GND / Dell Detected Pin
--- GND
------------ 5V
------------ 5V
------------ 5V
--- GND
(Dell: FFS_INT for supported HDD)
--- GND
------------ 12V (No support)
------------ 12V (No support)
------------ 12V (No support)
******************************
```



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

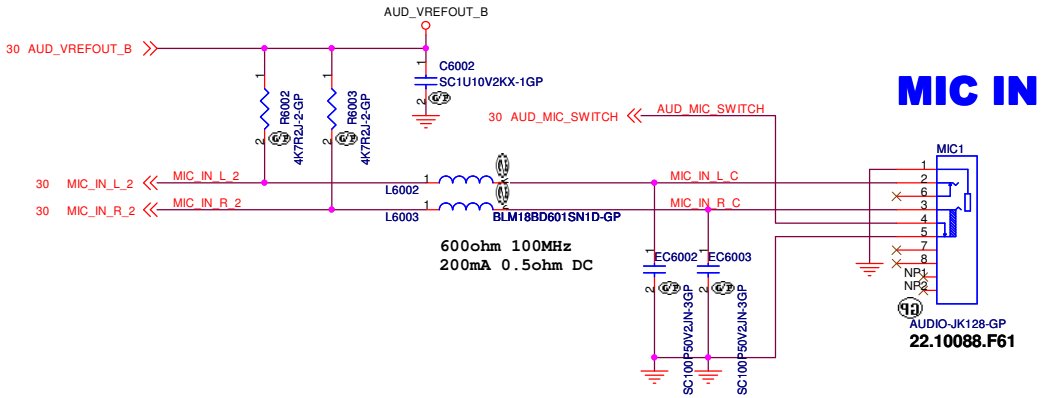
Title: HDD / ODD Connector

Size	Document Number	Rev
A3	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 59 of 82

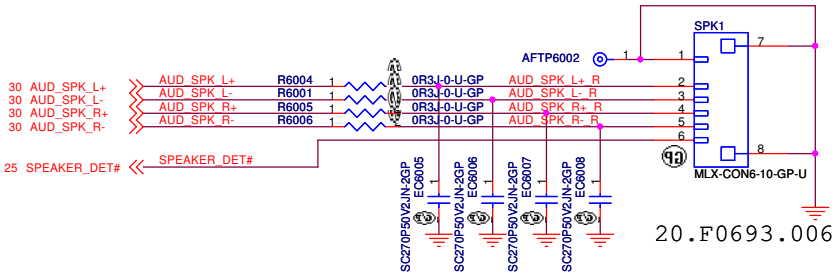
SSID = AUDIO

MIC IN



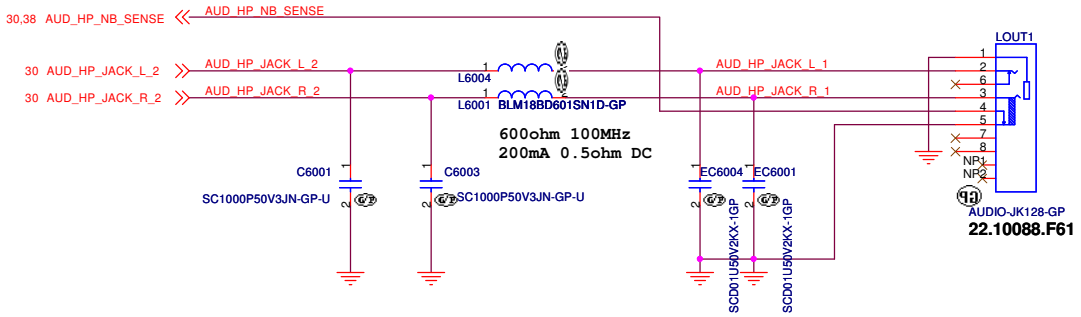
SSID = AUDIO

SPEAKER



SSID = AUDIO

Hear Phone



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack / Speaker Connector

Size	Document Number	Rev
A3	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 60 of 82

SSID = LOM

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserve

Size	Document Number	Rev
C	Fonseca UMA	X01

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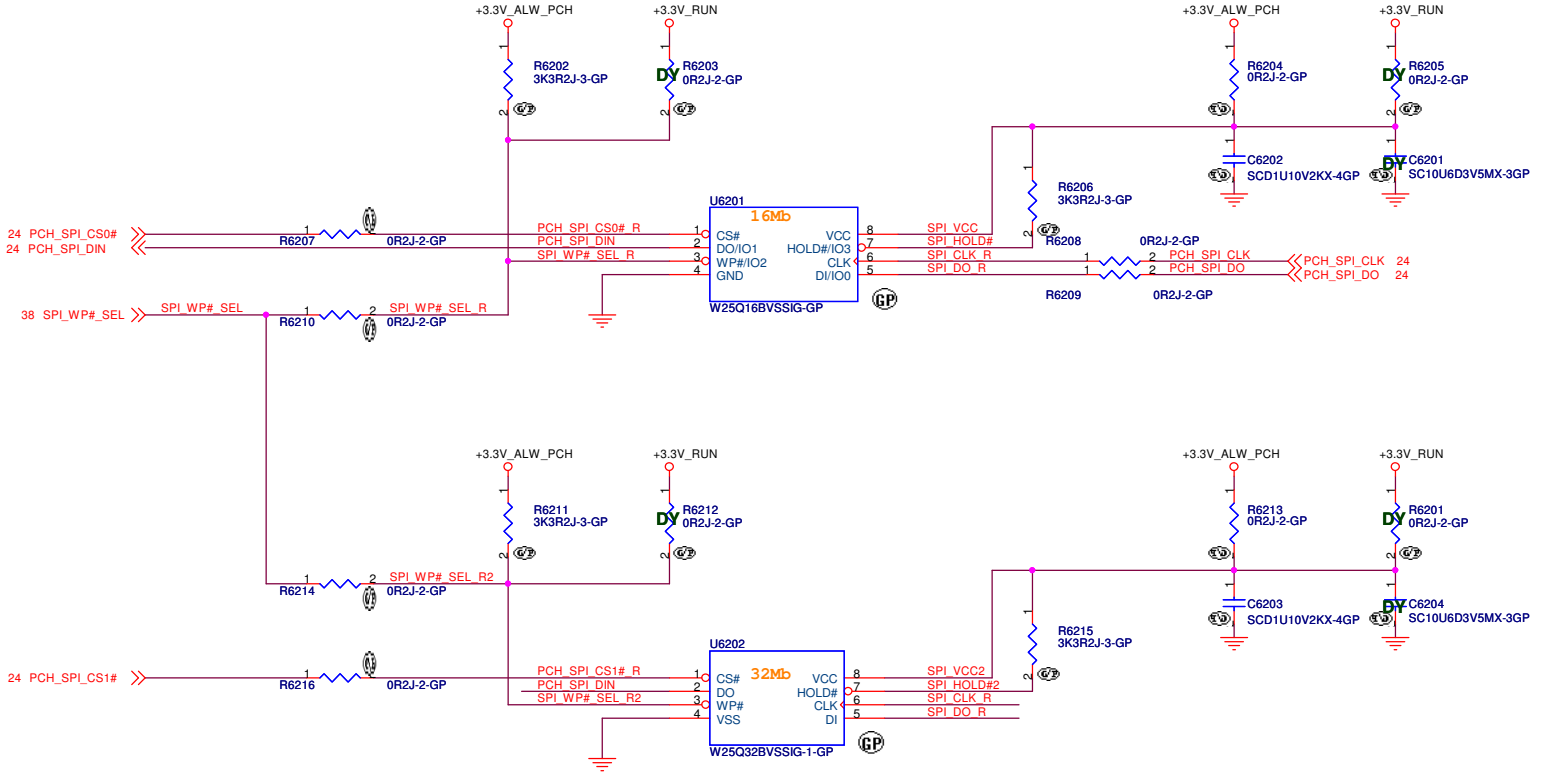
SSID = Flash.ROM

Pin.2
From Intel checklist,
SPI_CS0#/CS1#
No series resistor required
if routing length is 1.5"-6.5"
(with 1 or 2 SPI device)

Pin.6
Intel checklist
No series resistor required if routing length is 1.5"-6.5"
(with 1 or 2 SPI device)



X01-2

```
#1 source: 72.25Q16.001 (2MB, Winbond)
#2 source: 72.25165.A01 (2MB, MXIC)
#3 source: 72.25016.D01 (2MB, SST)

#1 source: 72.25Q32.A01 (4MB, Winbond)
#2 source: 72.25325.A01 (4MB, MXIC)
```

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

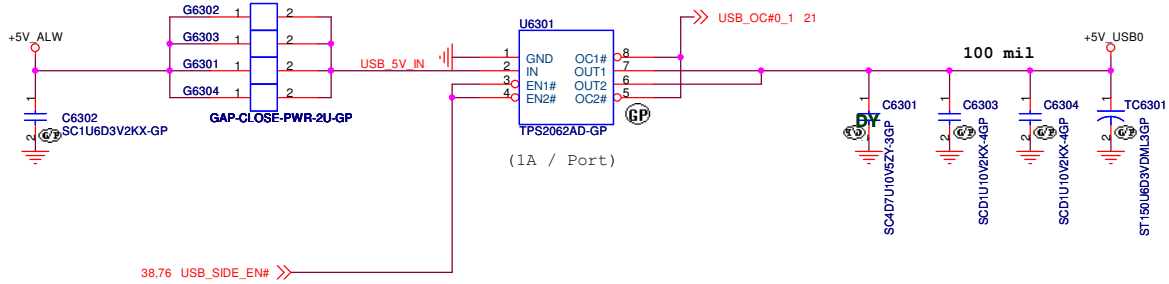
Title: Flash / EEPROM

Size	Document Number	Rev
A3	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 62 of 82

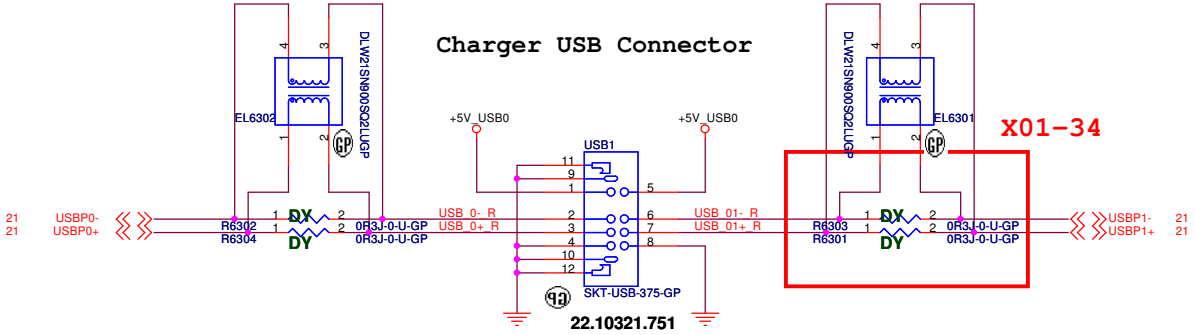
SSID = USB

Charger USB



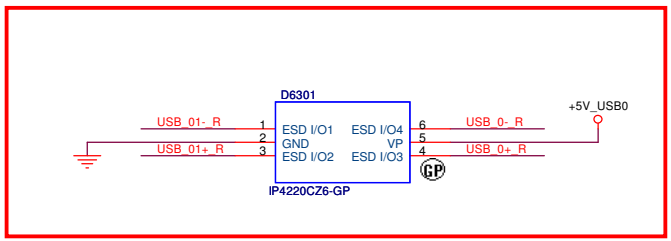
S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

Charger USB Connector



22.10321.751

X01-32



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB

Size	Document Number	Rev
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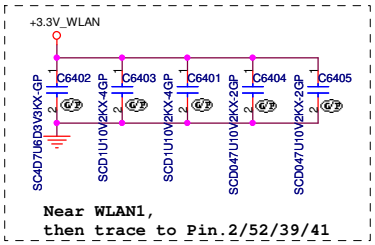
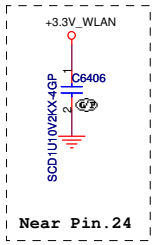
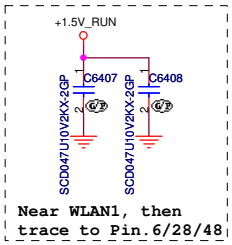
SSID = Wireless



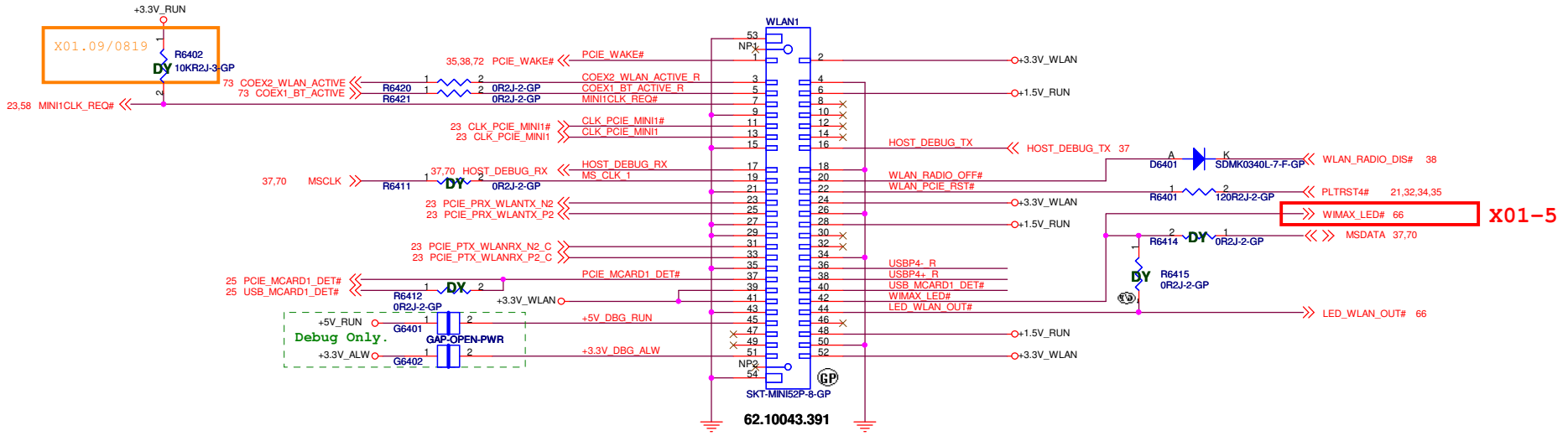


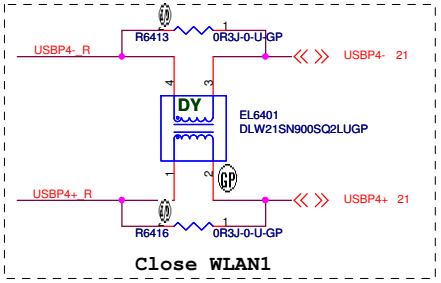


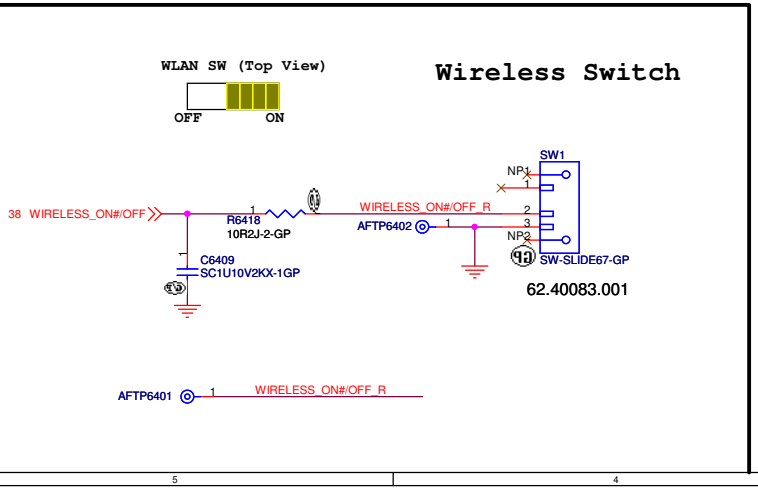
DEBUG PINS

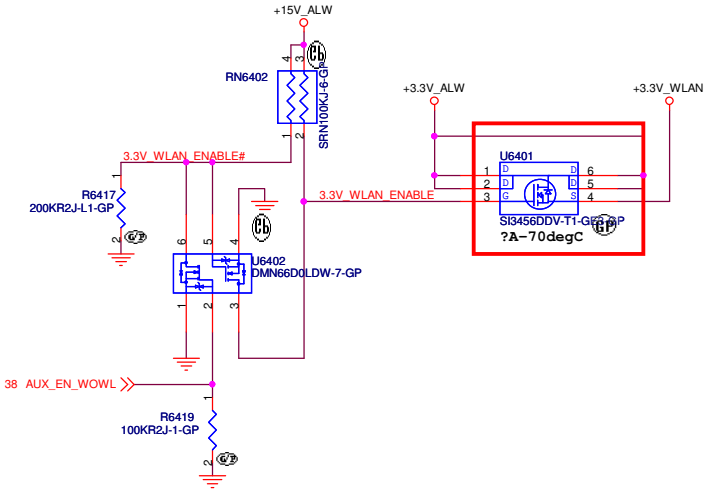
JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	B44
17	HOST_DEBUG_RX	B46
19	8051_TX	B43
42	8051_RX	A40

MiniCard WLAN connector









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN / Serial Out Connector

Size: Custom | Document Number: Fonseca UMA | Rev: X01

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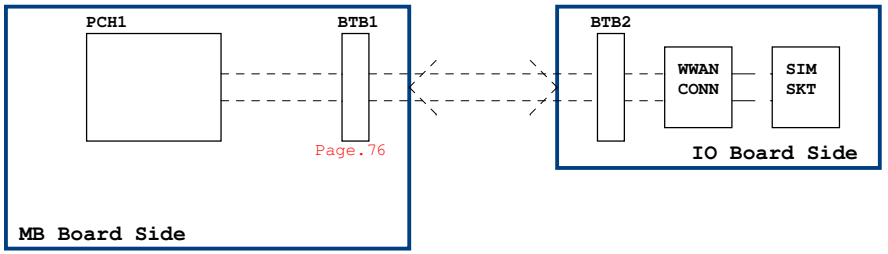
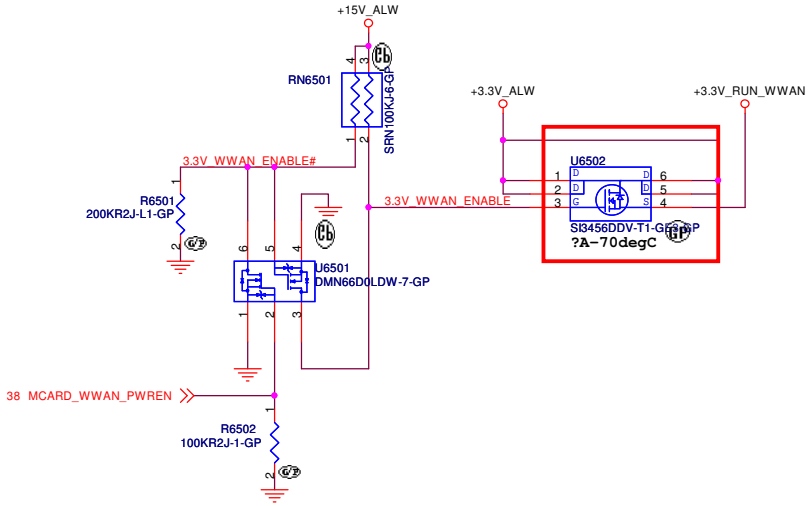
SSID = Wireless





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN

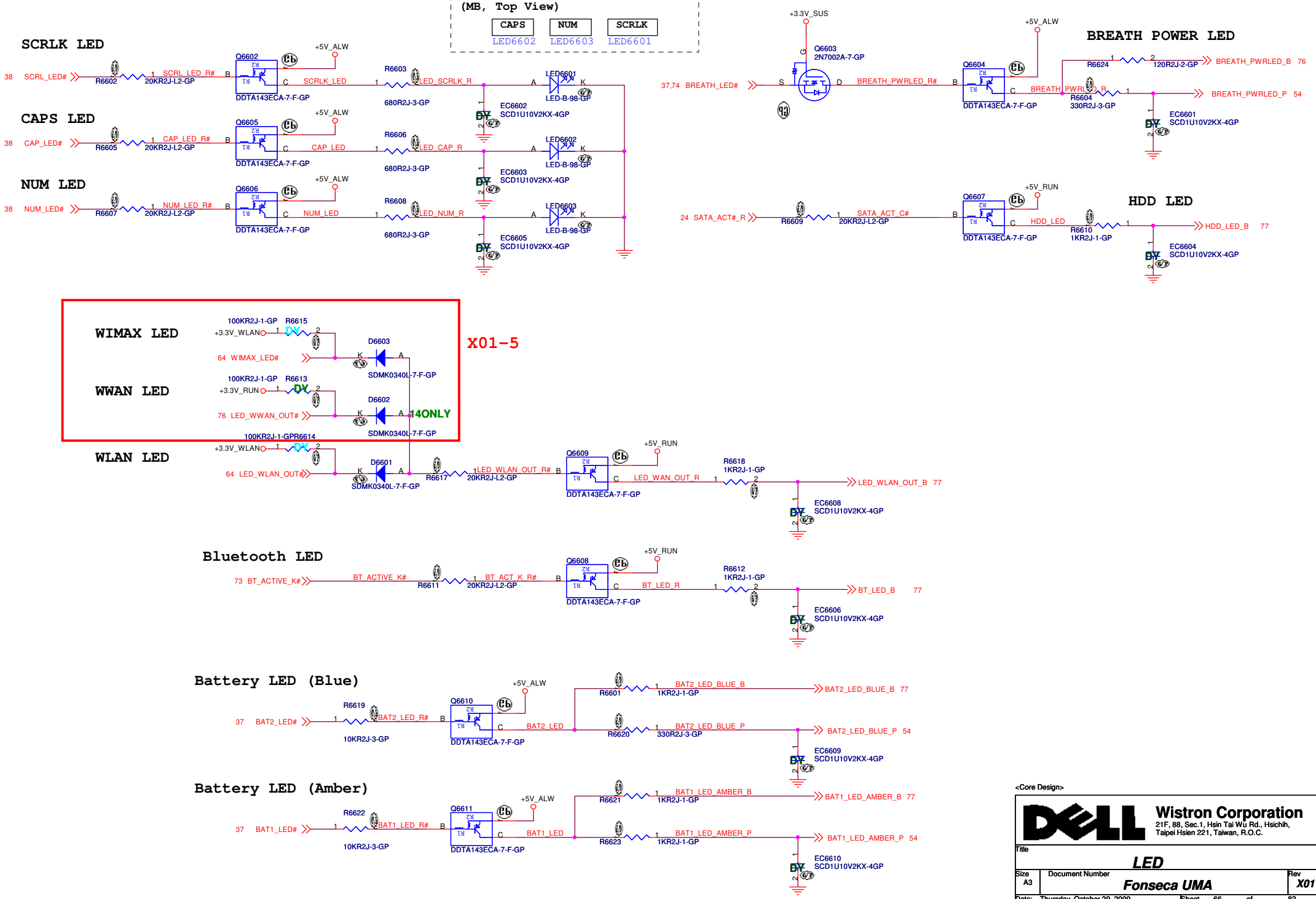
Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 65 of 82

SSID = User.interface

LED Location from left to right
(MB, Top View)

CAPS	NUM	SCRLK
LED6602	LED6603	LED6601



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LED

Size	Document Number	Rev
A3	Fonseca UMA	X01

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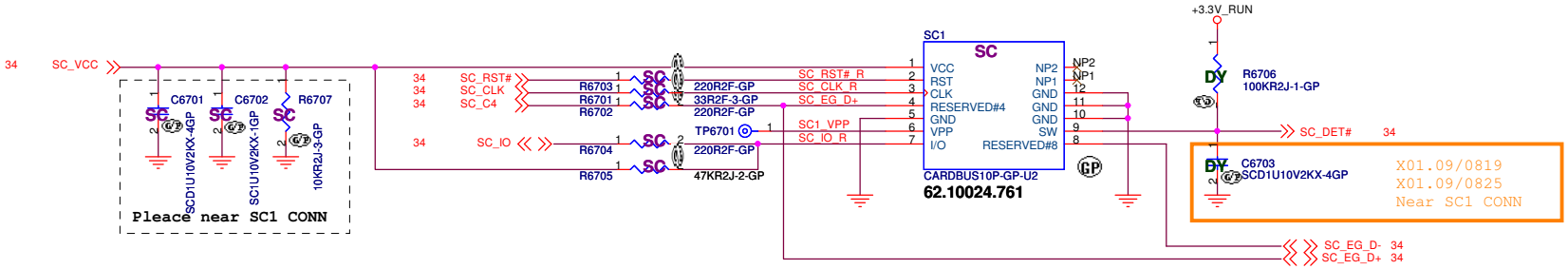
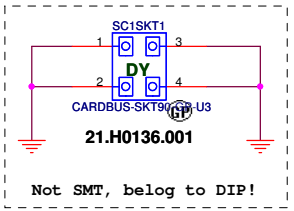
SSID = SmartCard

SmartCard



SmartCard Socket



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Smart Card Socket*		
Size: A3	Document Number: *Fonseca UMA*	Rev: *X01*
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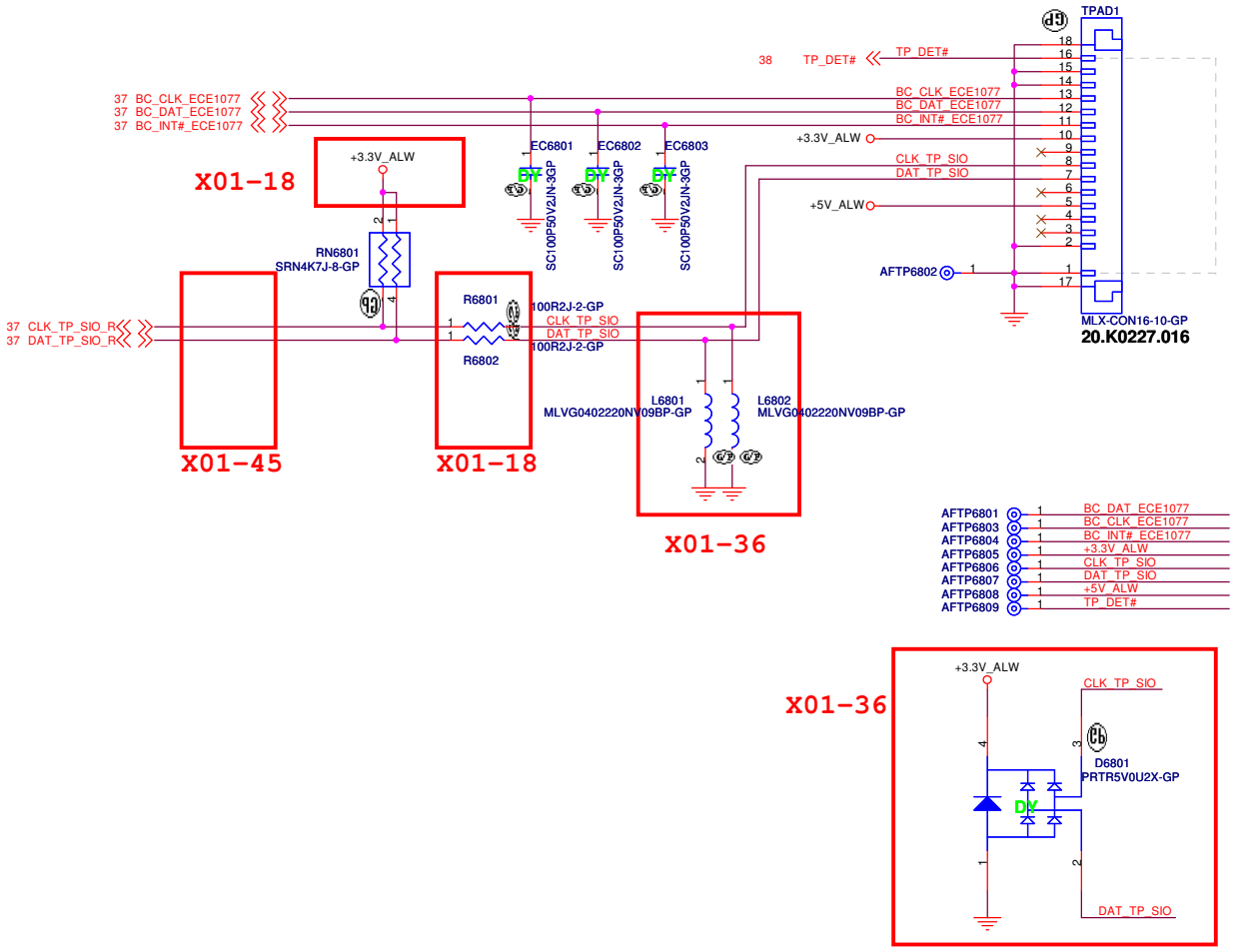
SSID = Touch.Pad

TouchPad Connector




```
Touch PAD Module Side
---------------------------------
16  TP_DET#
15  GND
14  GND
13  BC_CLK (ECE1077)
12  BC_DAT (ECE1077)
11  BC_INT# (ECE1077)
10  3.3V_ALW
09  3.3V_RUN (Internal NC)
08  PS2_CLK
07  PS2_DATA
06  5V_RUN (Backlight, No Use)
05  5V_ALW (Chip change to use 3V, NC)
04  PWM (Backlight, No Use)
03  GND (Backlight, No Use)
02  GND
01  Diag_loop
```

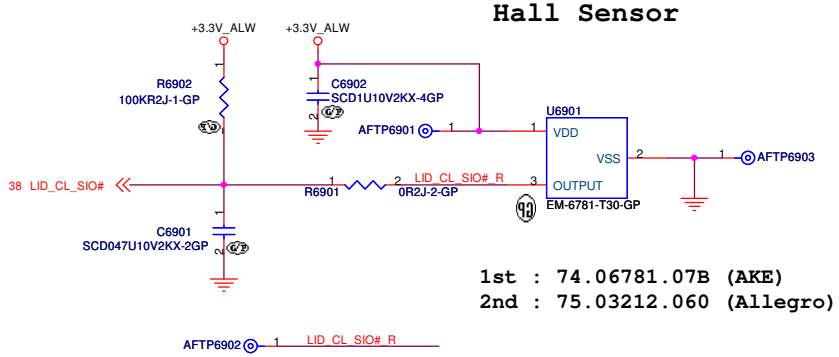
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch Pad Connector		
Size: A3	Document Number: Fonseca UMA	Rev: X01
Date: Thursday, October 29, 2009	Sheet 68 of 82	

SSID = User.interface

Hall Sensor



1st : 74.06781.07B (AKE)
2nd : 75.03212.060 (Allegro)

<Core Design>

Wistron Corporation
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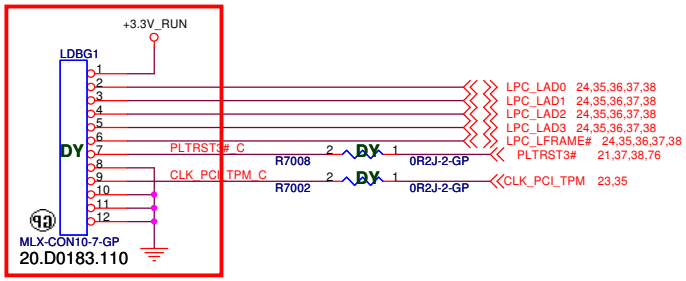
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Sensor		
Size: A3	Document Number: Fonseca UMA	Rev: X01
Date: Thursday, October 29, 2009	Sheet 69 of 82	

SSID = User.Interface

LPC Debug port

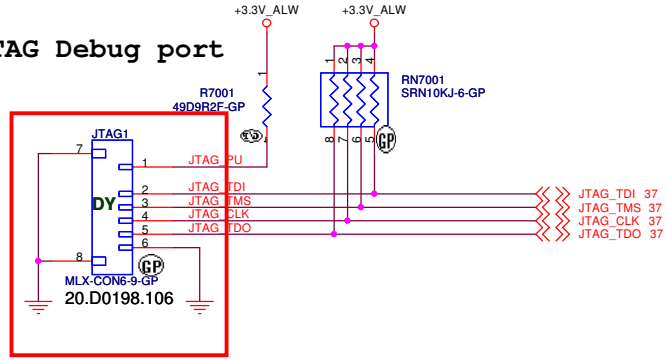
X01-8

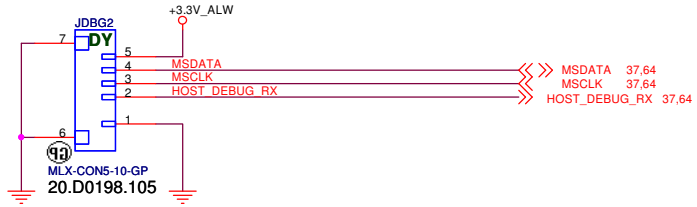


LDBG1, need pop R7008, R7002

JTAG Debug port

X01-8





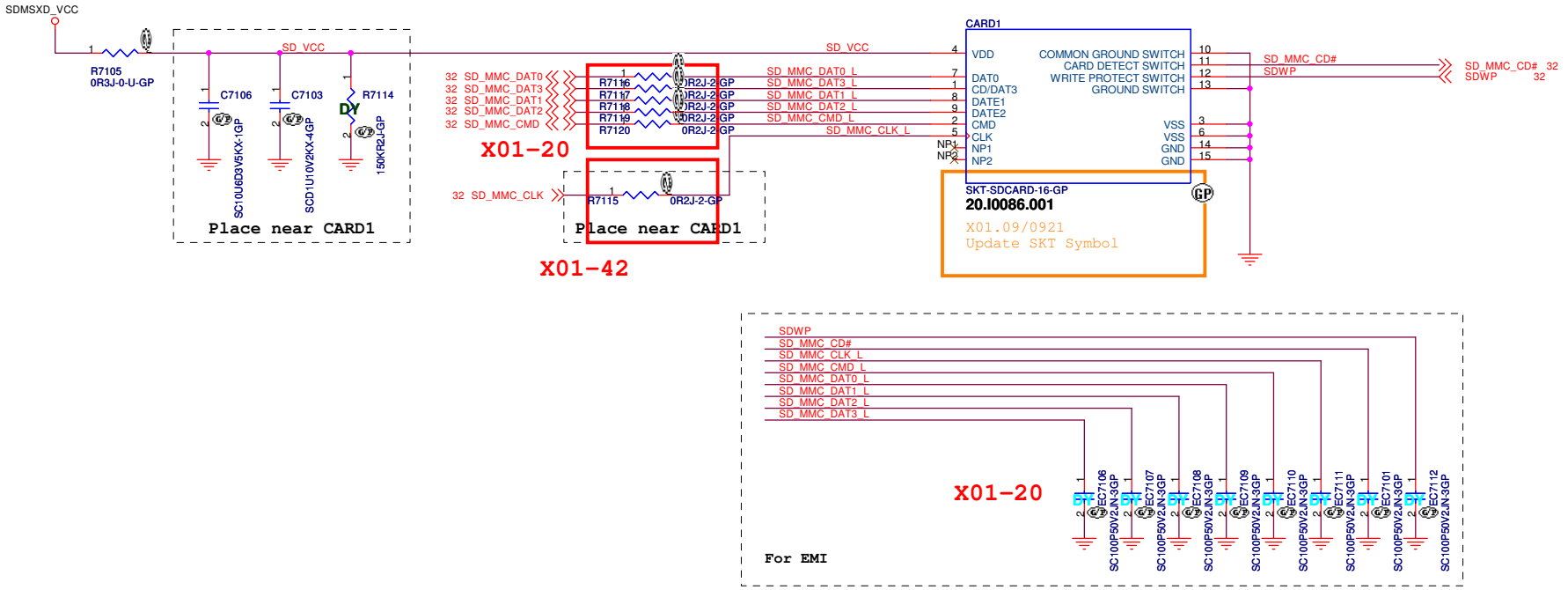
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

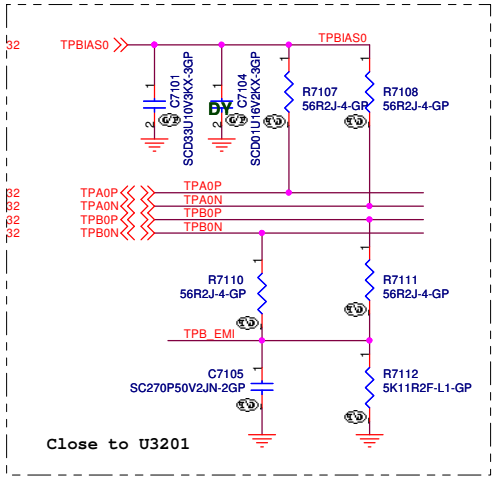
Title: JTAG Debug		
Size: A3	Document Number: Fonseca UMA	Rev: X01
Date: Thursday, October 29, 2009	Sheet 70 of 82	

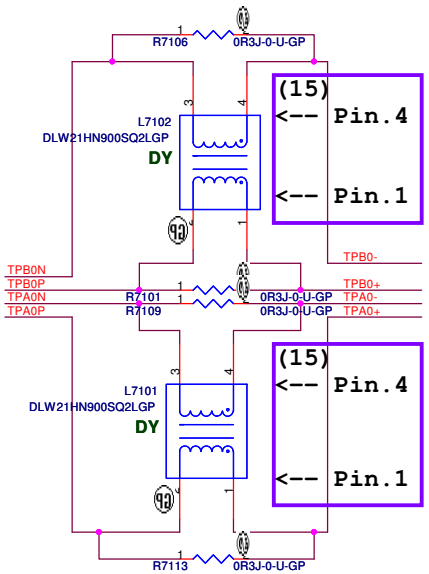
SSID = 1394

Flash Reader Socket

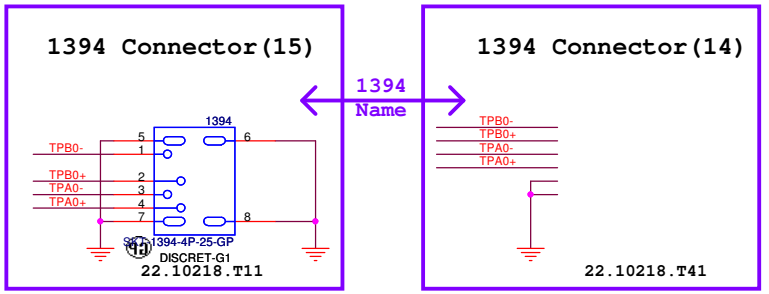


SSID = 1394





Shield GND separately for pairs of
TPA+ & TPA- and TPB+ & TPB-



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1394 Connector / Flash Socket

Size	Document Number	Rev
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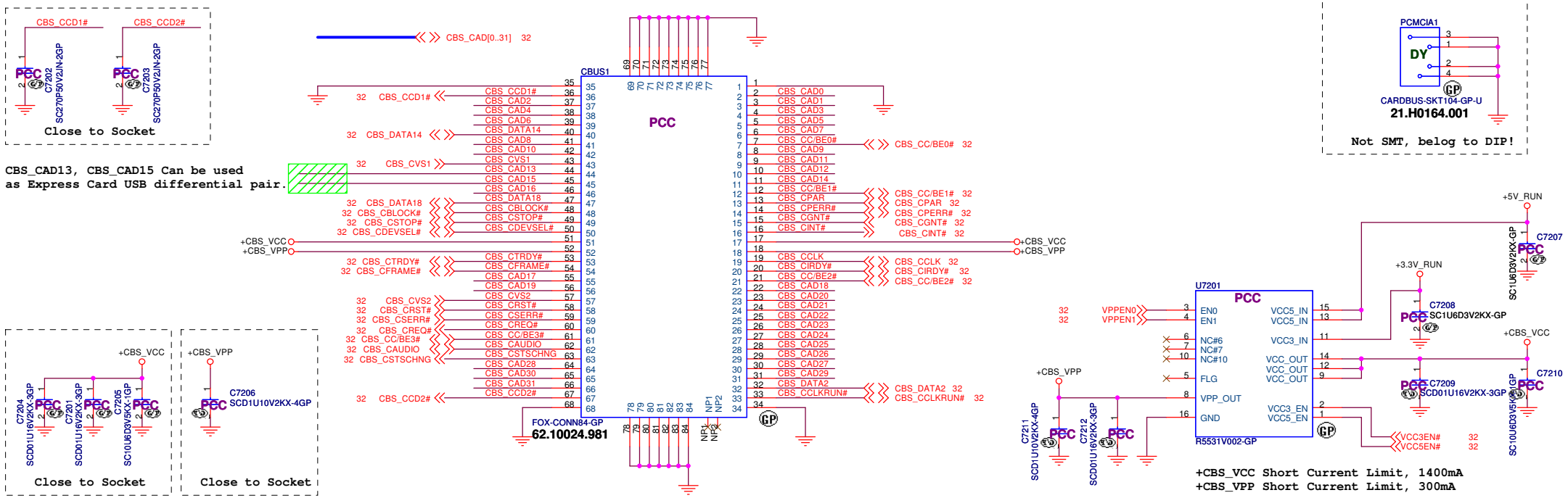
Date: Tuesday, November 03, 2009 Sheet 71 of 82

SSID = CARDBUS

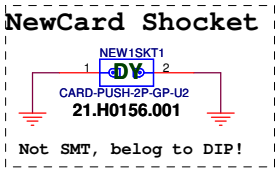
Cardbus Connector

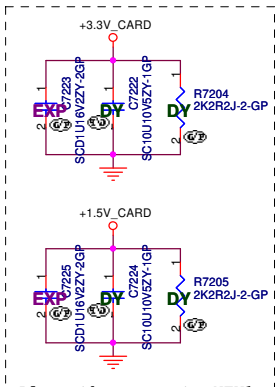


Cardbus Shocket

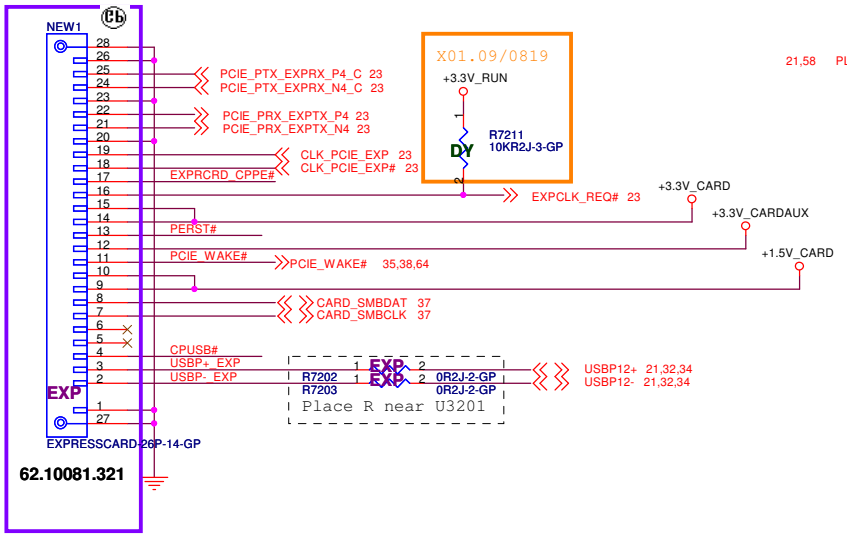
SSID = ExpressCard

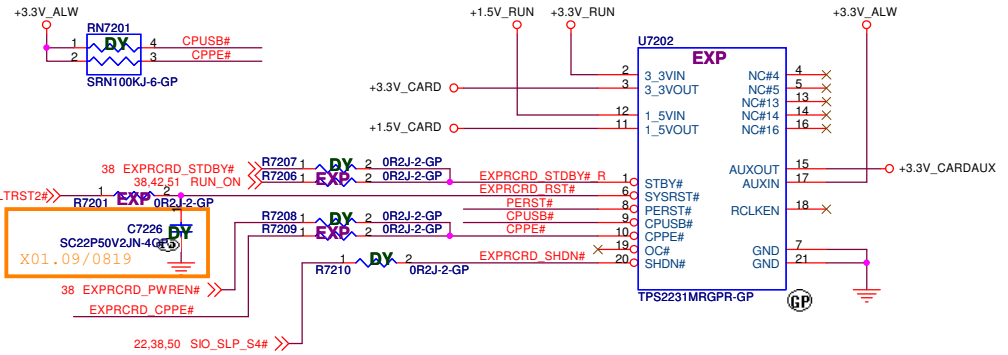
NewCard Shocket

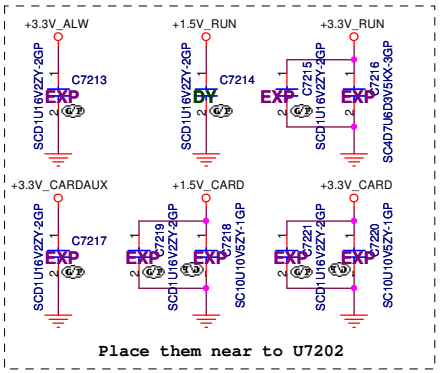




NewCard Connector







+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / ExpressCard

Size	Document Number	Rev
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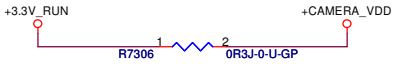
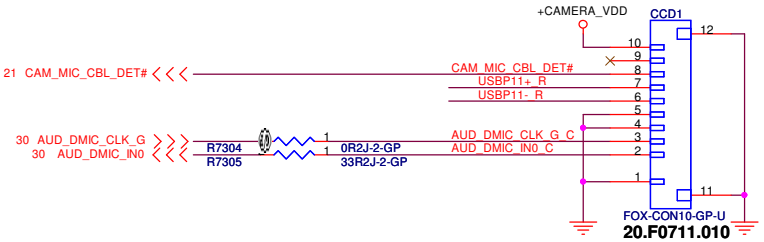
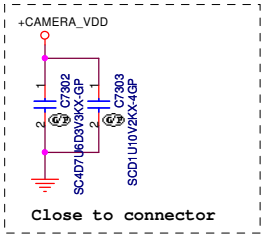
User.interface

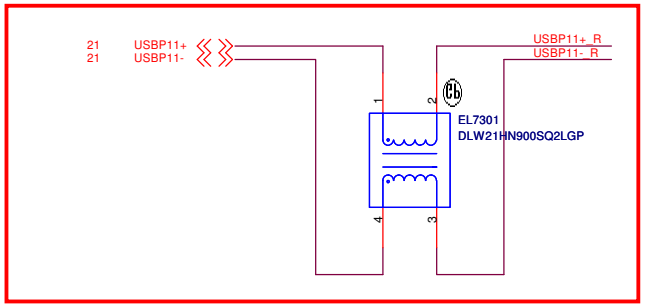
Camera Power CTRL

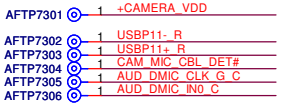


Camera Connector



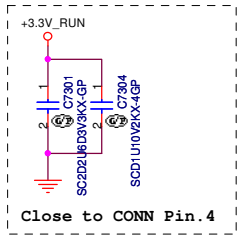


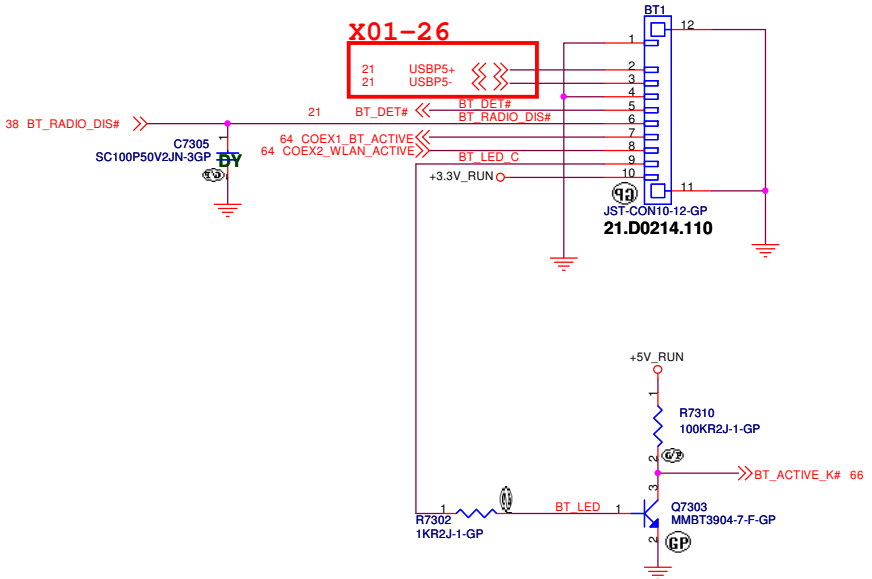


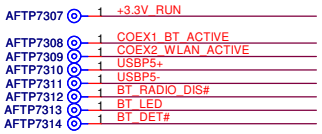


User.interface

Bluetooth Connector







MB BT CONN / BT Module CONN

PIN	Define	PIN	Define
1	GND	1	GND
2	USBP5+_R	12	USB_DP
3	USBP5-_R	11	USB_DN
4	GND	10	GND
5	BT_DET#	2	MOD_DET
6	BT_RADIO_DIS#	7	RADIO_DIS
7	COEX1_BT_ACTIVE	3	COEX1_BT_ACTIVE
8	COEX2_WLAN_ACTIVE	8	COEX2_WLAN_ACT
9	BT_LED	6	LINK_IND
10	+3.3V_RUN	9	3.3V
11	NC		
12	NC		

<Core Design>

Wistron Corporation
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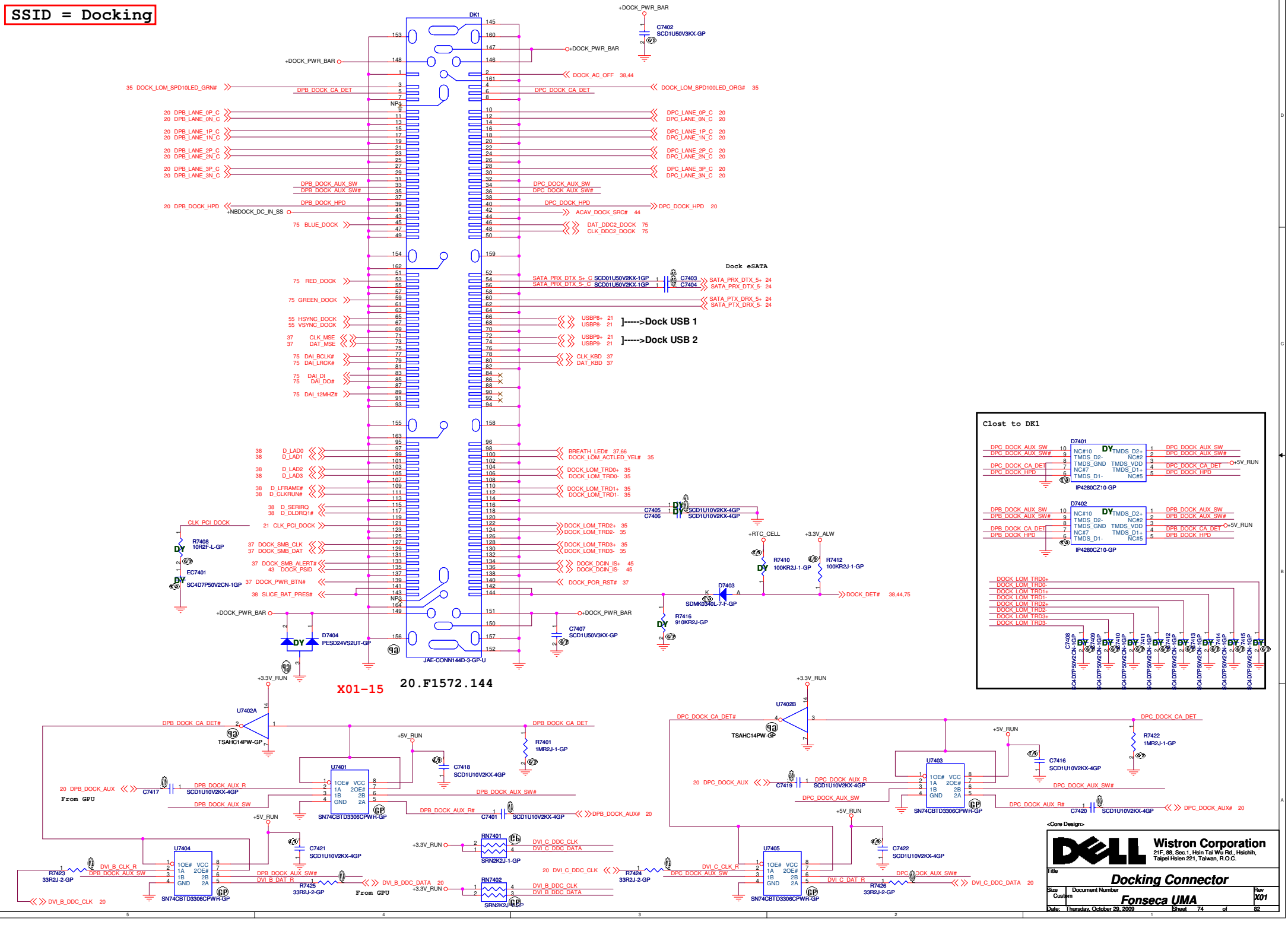
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth / Camera / DMIC

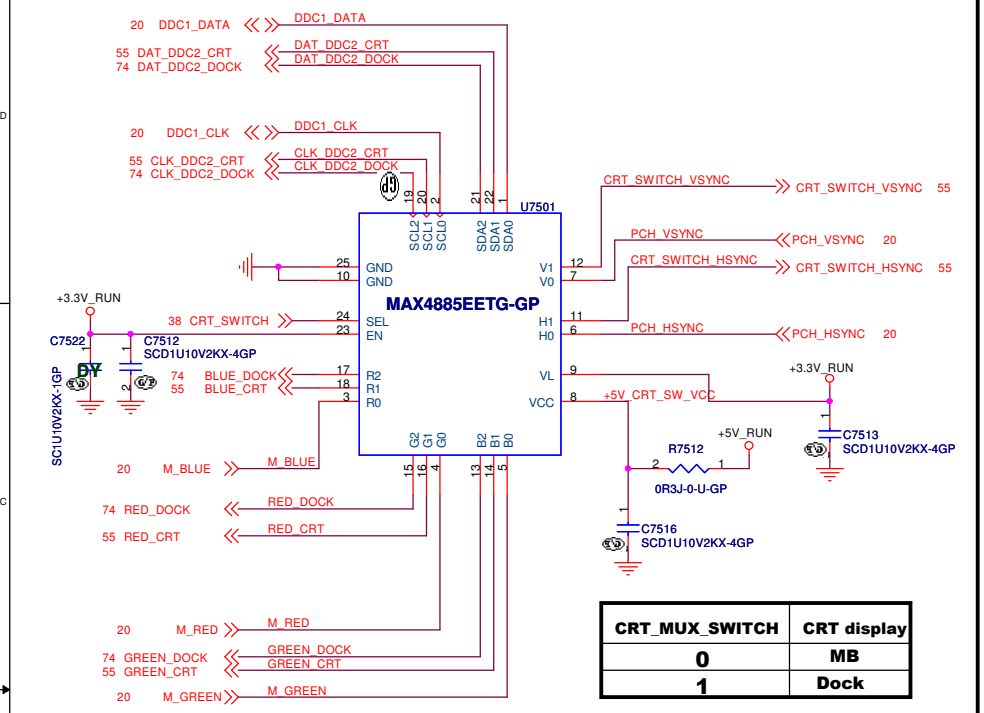
Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 73 of 82

SSID = Docking

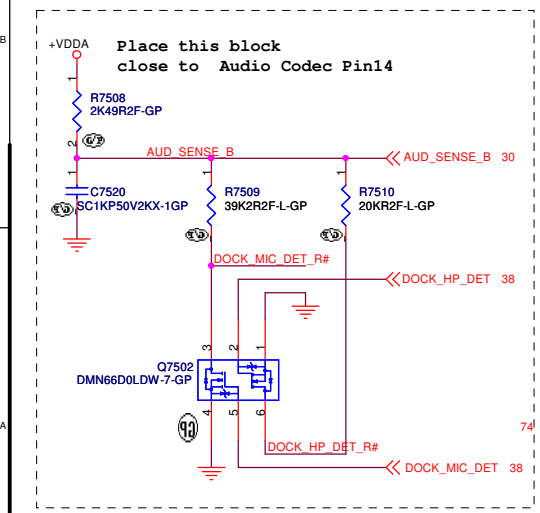


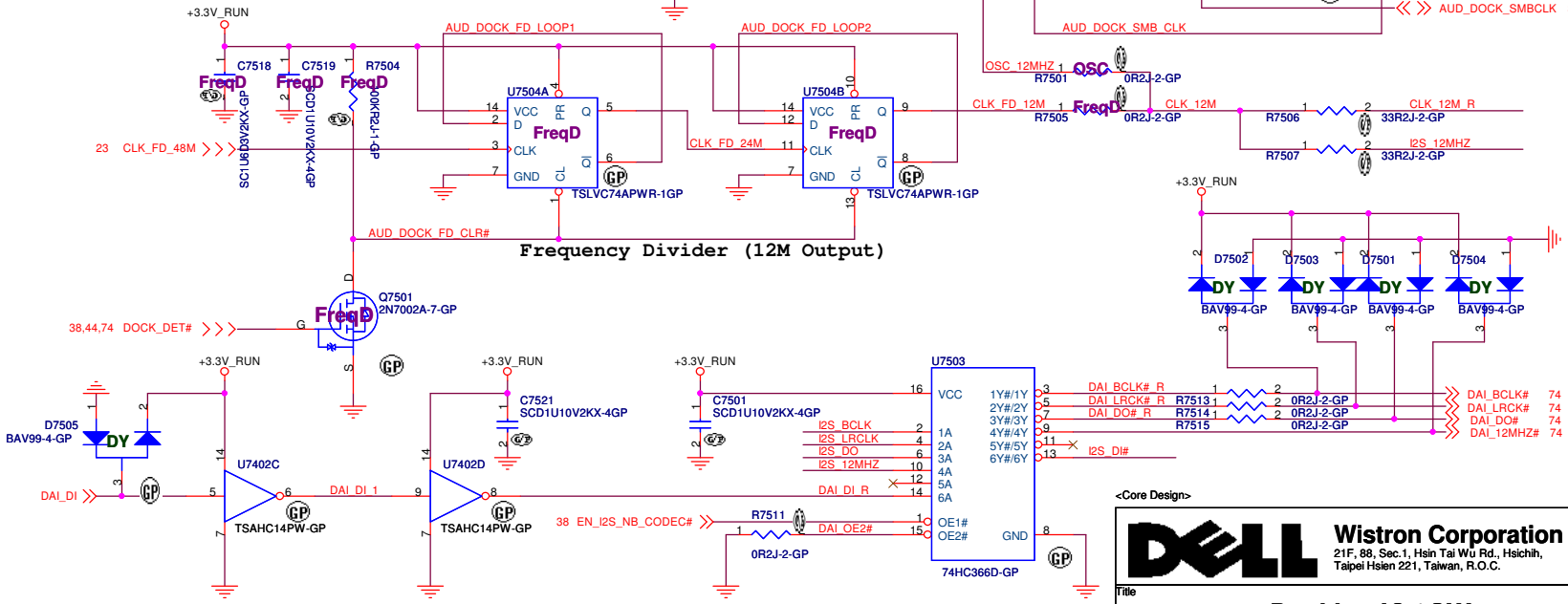
SSID = DOCK CRT SWITCH

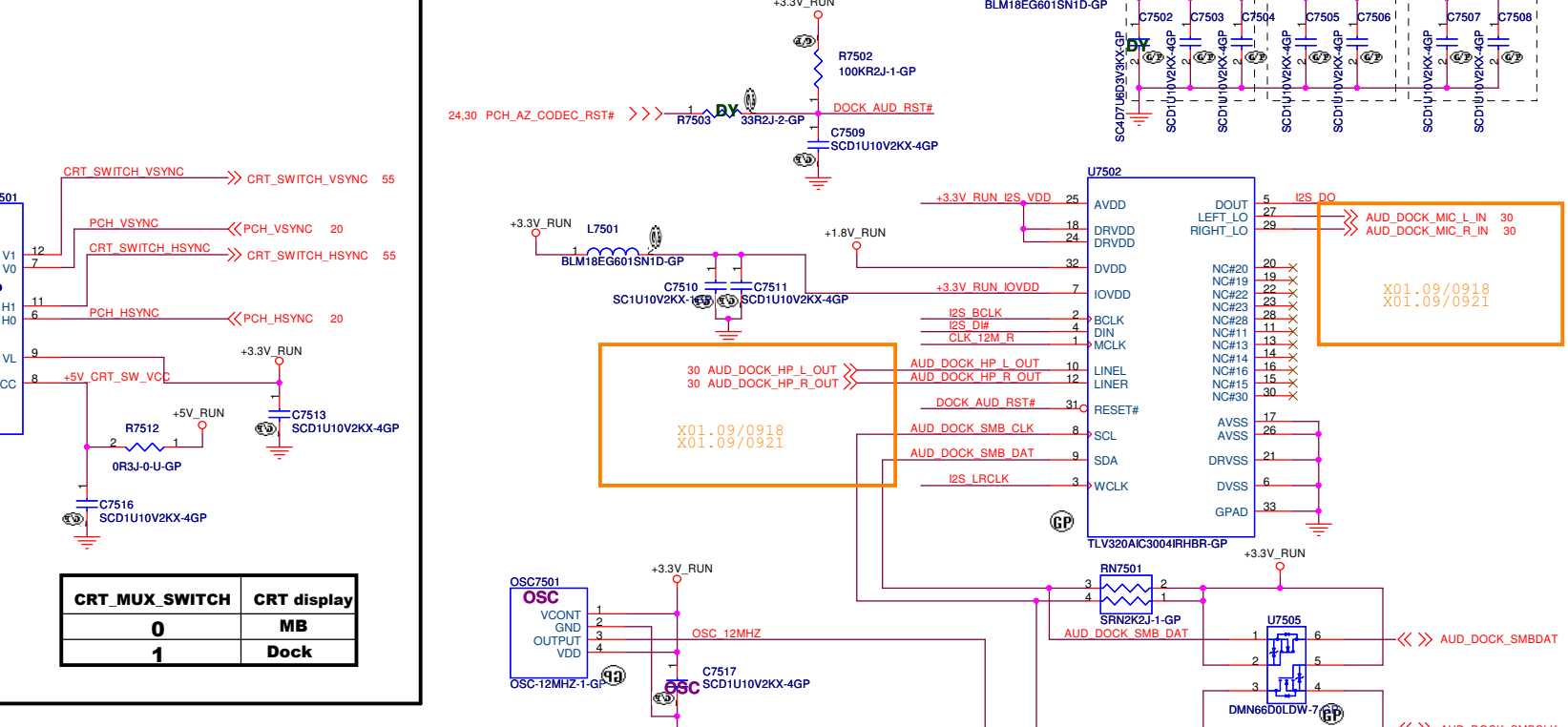


CRT_MUX_SWITCH	CRT display
0	MB
1	Dock

SSID = DOCK AUDIO







<Core Design>

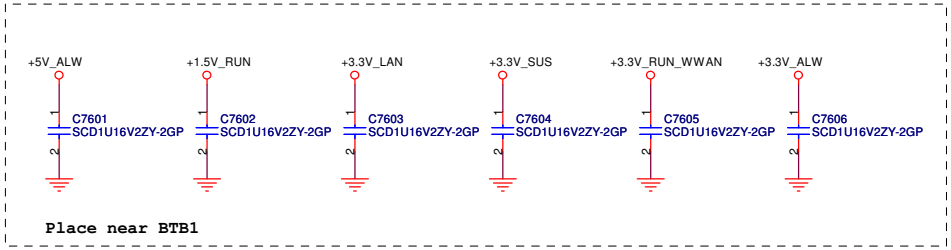
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Docking IC / SW

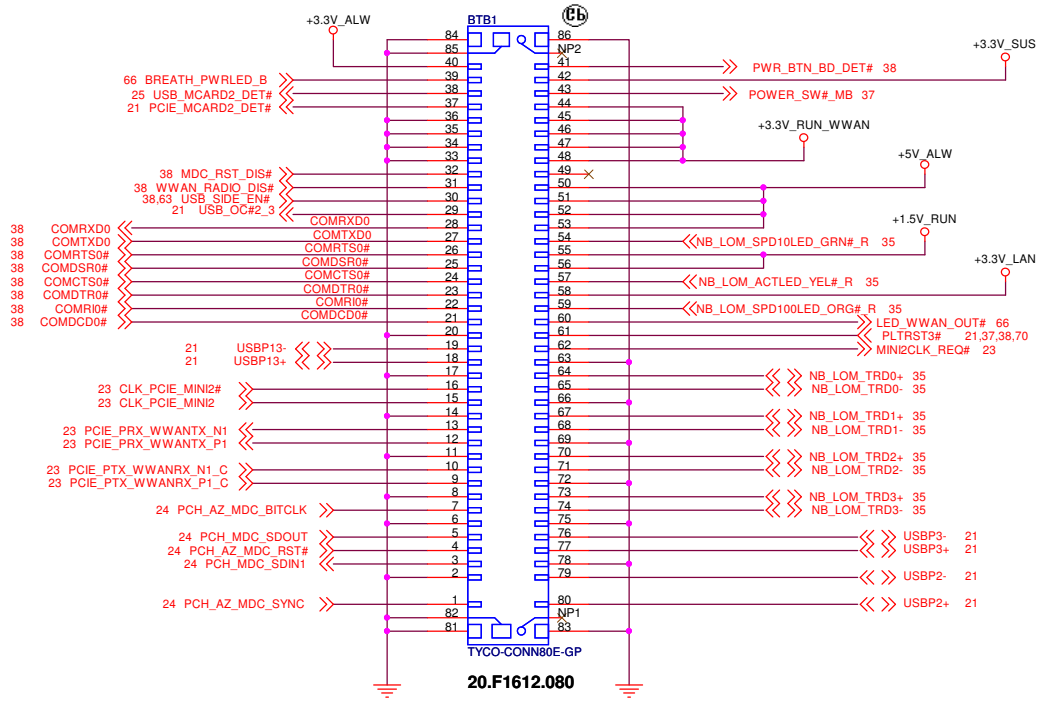
Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 75 of 82

SSID = User.Interface



IO Board Connector



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

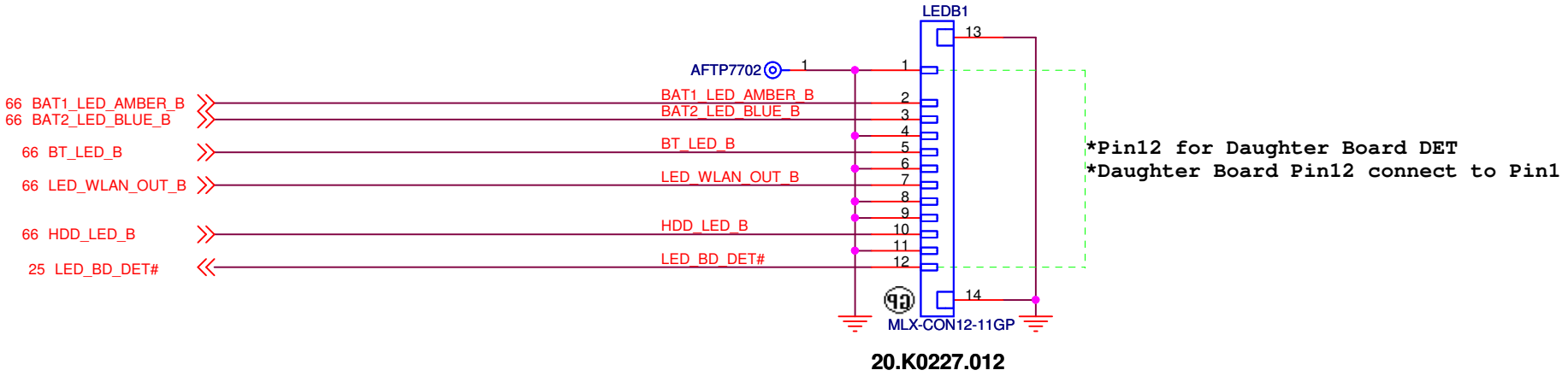
Title: IO Board CONN

Size: A3 | Document Number: Fonseca UMA | Rev: X01

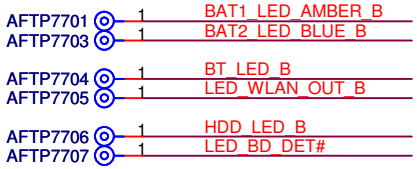
Date: Thursday, October 29, 2009 | Sheet 76 of 82

SSID = User.interface

LED BD Connector



20.K0227.012



LED Location from left to right

HDD	BATTERY	WLAN	BLUE TOOTH

<Core Design>

Wistron Corporation
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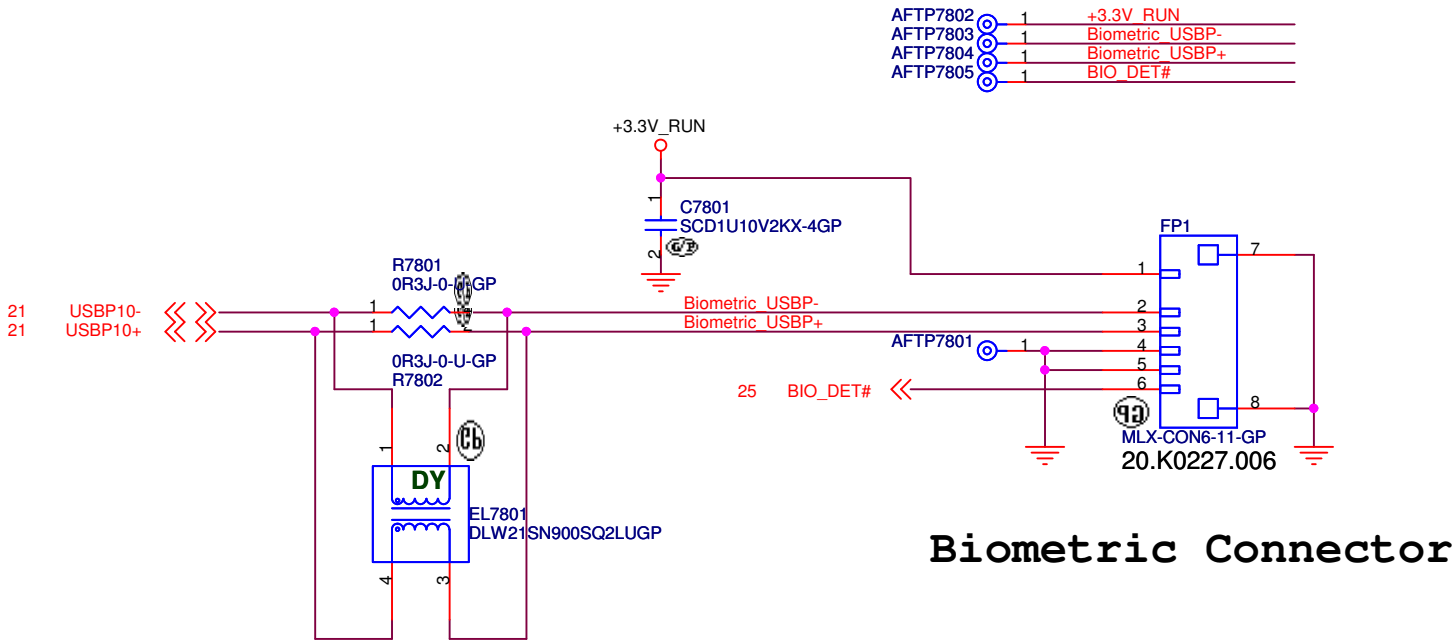
Title: LED Board Connector

Size	Document Number	Rev
A4	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 77 of 82

SSID = User.Interface



Biometric Connector

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Finger Printer Board CONN

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SSID = Mechanical

Hole

Hole

Hole

Spring

Unused Parts

RF Cap.

RF Cap.

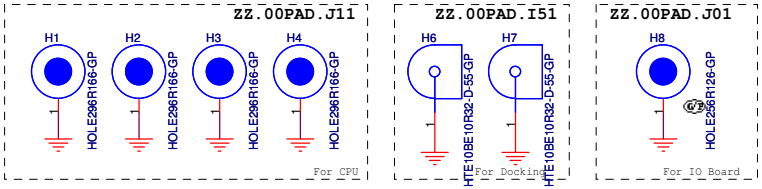
RF Cap.

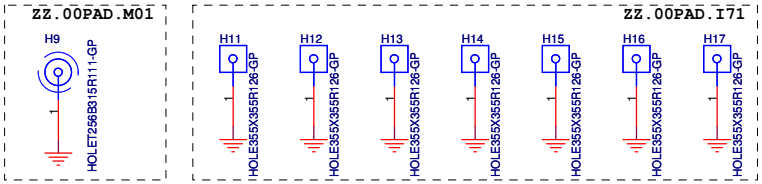
RF Cap.

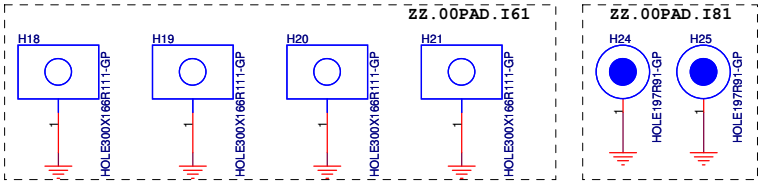
RF Cap.

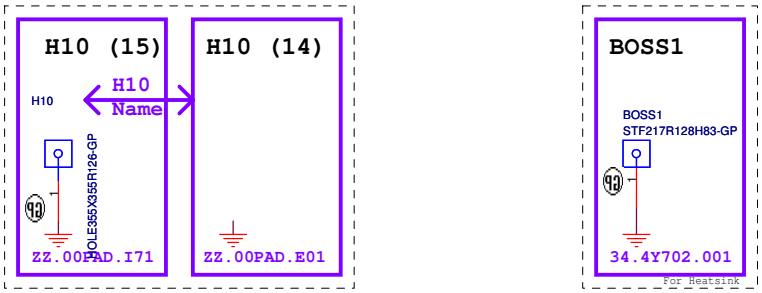
EMI Cap.

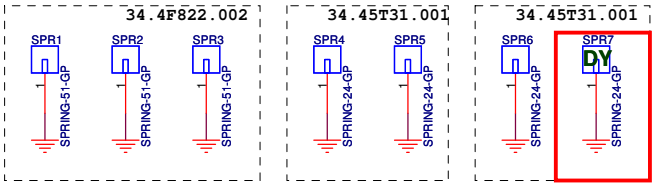
EMI Cap.

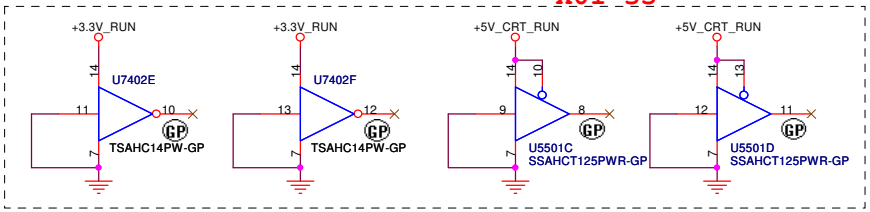


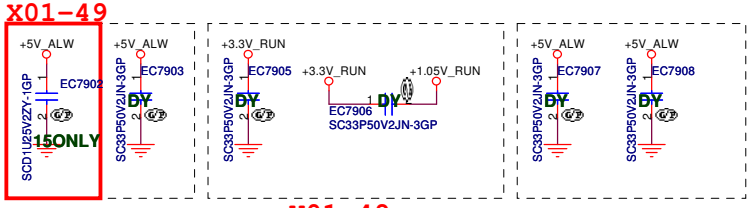


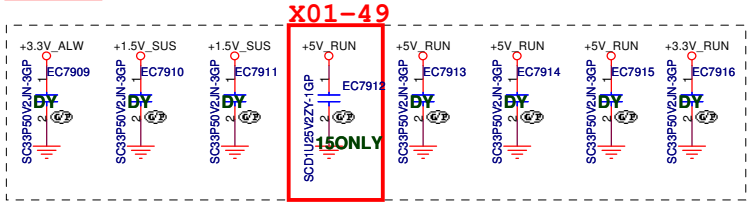


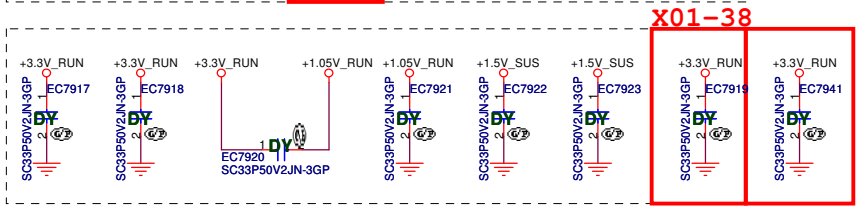


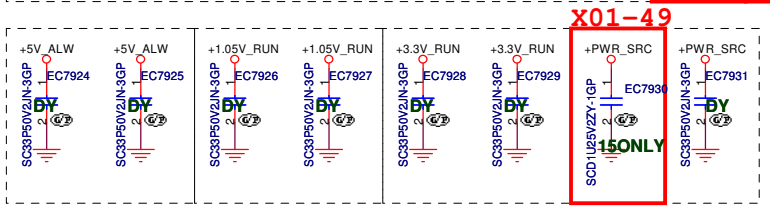


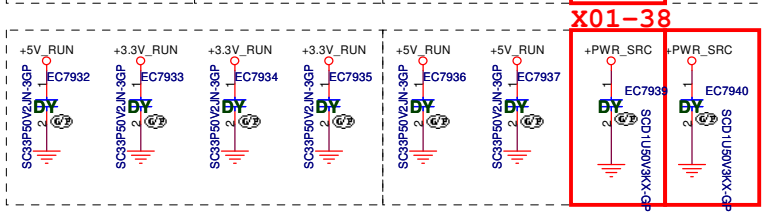


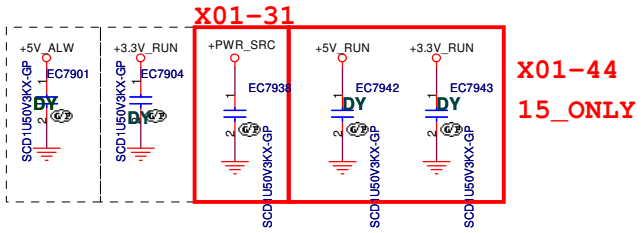












<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Unused Parts / EMI RF Cap.

Size: A3 | Document Number: Fonseca UMA | Rev: X01

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VERSON	DATE	NO	PAGE	Modified List	Issue Description	OWNER
X01	08/19	1	35	(remove) R3541 ; (change) R3537 to B_TPM group	LOM_TPM_EN# for B_TPM group control	EE
		2	54,64,72	(rename) F1 to FUSE5401 ; (rename) R2323 to (DY) R6402 (rename) R2320 to (DY) R7211 ; (rename) C7802 to (DY) C7226	Rename for schematic standardization Dummy R6402 and R7211 because traces already pull high.	EE
		3	27	(change) L2702, L2703 part.	Change coil for intel requirment.	EE
		4	27	(change) D2701, D2702 part.	Change diode for PSL vender.	EE
		5	9,37	(remove) TP3710 (add) R3730 for H_SKTOCC# traces.	Dell requires add CPU socket detect function.	EE
		6	37	(remove) R3738	Just for JTAG debug, remove R3738 pull high.	EE
		7	37	(change) R3703 to 130k.	Board Version (X01).	EE
		8	34,67	(add) R3411, C3409 to DY for CLK_SC_48M. (add) 0.1uF C6703 to DY for SC_DET#.	Remain AC term for SmartCard 48Mhz clock. Add 0.1uF for SC_DET#.	EE
		9	47	Update PU4701 symbol.	Correct error vender component P/N.	Power EE
	08/25	10	50	(DY) PR5007. (change) (DY) PD5001 part.	TPS51116 already built-in BST circuit. Change PD5001 to PSL vender.	Power EE
		11	42	(change) Q4207 part.	Change MOS part due to power demand.	EE
		12	54	(change) FUSE5401 part.	Use Poly-fuse instead of one time fuse.	EE
		13	54	(add) 100k R5401 to (DY) to GND.	Reserved dummy location for panel backlight control.	EE
		14	25	(change) TPM_ID1 pull high to +3.3V_RUN	Intel PCH EDS.	EE
		15	39	(change) U3901(SMSC EMC4002) to Rev.B	SMSC Version Change.	EE
		16	4,35,37	(modify) SMBus Diagram for LAN (change) KBC I2C1E group link to PCH1 and U3701 pull high +3.3V_ALW_PCH. (change) LAN SMBus from U3503 link to U3701.	Modify LAN SMBus for leakage from +3.3V_LAN to +3.3V_ALW_PCH.	EE
		17	54	(remove) R5423, R5424.	No need R pull high / down for eDP_AUX and eDP_AUX#.	EE
		18	32	(change) R3206 from 100k to 47k ohm.	For Ricoh R5U24x sequence (GBRST#).	EE
		19	32	(stuff) R2316, C2309, C2310, X2301, X2301.	Intel recommends use 25M Xtal for DCI signals.	EE
						ME

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VERSON	NO	PAGE	ACTION	reference	Issue Description	OWNER
X01	X01-1	79	Change	H10	14U change H10 PAD size	EE
	X01-2	62	Change	U6201,U6202	change BIOS part number	EE
	X01-3	52	ADD	PG5221~PG5226	combin 1.05V_RUN and 1.05V_VTT Circuit	EE
		49	remove	+1.05V_RUN Circuit		
	X01-4	9	Change	R915-->0 ohm,R920-->0 ohm		EE
	X01-5	66	ADD	D6603,D6602	combin WWAN ,WIMAX and WLAN LED circuit	EE
			DY	R6615,Q6601,R6616,R6613		
	X01-7	58	DY	XDP1,R5808		EE
	X01-8	70	DY	LDBG1,JTAG1		EE
	X01-9	50	DY	PR5010	change discharge mode	EE
			ADD	PR5016		
	X01-10	36	Change	R3616-->1k, C360200>1U	modify TCM circuit	EE
			DY	R3606,R3607		
			remove	R3605		
	X01-11	42	Change	R4226--> 0805 size		EE
	X01-12	42,37	Change	C4208-->150P,C4211-->4700P,R3707-->10K	Tuning S3 power sequence.	EE
		52	DY	PC5211		
	X01-13	46	ADD	PR4623,PR4624	Tuning power sequence.	EE
			DY	PR4624		
	X01-14	37	Change	change 1.05V_RUN_PWRGD to test pad	combin 1.05V_RUN and 1.05V_VTT Circuit	EE
	X01-15	20	Change	R2006-->110K,R2007-->110K		EE
	X01-16	74	Change	change DK1 part number	update dock connector	ME
	X01-17	46,52 53,12	Change	PU460-->FDS8880,PU4605-->FDS6676AS,PR4602-->73K2R2F PU5203-->SI7658ADP,PC5307-->SCD068U16V2KX PR5202-->73K2R2F,PR5328-->61K9R2F PC5319-->SC1KP50V2KX,PC5318-->SC330P50V2KX R1203-->0R2J-2	Power team suggest	power-EE
		52	remove	PU5204		
	X01-18	68	ADD	R6801,R6802	EMC team suggest	EMC
	X01-19	37	modfiy	connect X3701 pin2 and pin3 to GND		EE
	X01-20	32	modfiy	R3211,R3212,R3205,R3213,R3215-->33 ohm	Tuning signal	EE
			ADD	R7116,R7117,R7118,R7119,R7120		
		71	DY	EC7106,EC7107,EC7108,EC7109		
	X01-21	39	Change	C3901-->470P,C3902-->100P		EE
	X01-22	35	ADD	U3507	add LAN EEPROM 2nd source	EE
	X01-23	47	Change	PC4729-->SCD22U25V3KX,PR4776-->6K65R2F	Power team suggest	power-EE
	X01-24	12	ADD	R1207,R1208	Power team suggest	power-EE
	X01-25	30	Change	R3014-->2K,R3025-->2K,C3029-->1KP C3030-->1KP,C3039-->1U,C3040-->1U C3035-->1U,C3036-->1U,C3031-->1KP C3032-->1KP,R3028-->2K,R3029-->2K	modify DOCK MIC and HP circuit	EE
	X01-26	73	remove	R7308,R7309	USB1.1 does not need resistors in USB pair.	EE
	X01-27	59	Change	ODD1	change dock connector	EE
	X01-28	30	Change	C3010,C3023,C3024	Factory request, create spacing.	EE
	X01-29	79	ADD	BOSS1	new part for combin pad and boss	ME
	X01-30	38,24 25	modfiy	RN3805-->100K*2,RN2401-->10K*2,RN2502-->10K*2	combin resister	EE
	X01-31	79	ADD	EC7919	EMC team suggest	EMC
	X01-32	63	modfiy	D6301	swap	EE

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VERSON	NO	PAGE	ACTION	reference	Issue Description	OWNER
X01	X01-33	23,54	ADD	EC2301,EC2302,EC5401	EMC team suggest	EMC
	X01-34	63	modfiy	EL6301	swap	EE
	X01-35	79	DY	SPR7	EMC team suggest	EMC
	X01-36	49	ADD	D6801	EMC team suggest	EMC
			modfiy	L6801,L6802		
	X01-38	79	ADD	EC7919,EC7939,EC7940,EC7941	EMC team suggest	EMC
	X01-39	35	ADD	D3502,R3548	Prevent leakage of +3.3V_RUN.	EE
	X01-40	52	ADD	PTC5203		EE
	X01-41	23	modfiy	Q2303,RN2301	14U ONLY	EE
	X01-42	71	modfiy	R7115	change R7115.2 net name to SD_MMC_CLK_L	EE
	X01-43	7,9,32 23	Change	RN3202,RN2311,RN903,RN703 RN704,RN701,RN705	change size	EE
	X01-44	79	ADD	EC7942,EC7943	EMC team suggest	
	X01-45	39	ADD	PC3901	Power team suggest	EE
		39,50	Change	R3902-->12K7R2F,R3903-->5K62R2F PR5014-->30K1R2F,PR5015-->29K4R2F		
	X01-47	22,27 24,11	Change	R2205-->10K,C2713-->1U,R2407-->8.2K,R1109-->3.3K		EE
	X01-48	24,58	Change	FAN1,RTC1 connector	ME suggest	
	X01-49	43,79 45,46	stuff	EC4301,EC7930,PC4503,PC4610,PC4615,EC7912,EC7902	EMC team suggest, 15 inch only	EMC
	X01-50	37,40 54	DY	R3734,R4006,R5425		EE
		54	stuff	R5418		
	X01-51	47	Change	PC4710,PC4709,PC4723--> 0.22U25V	Power team suggest	power-EE
	X01-52	63	DY	R6301,R6302,R6303,R6304	EMC team suggest	EMC
		63	stuff	EL6301,EL6302		

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