Fonseca 14 UMA Schematics Document

rPGA988A Mobile Arrandale

Intel Ibex Peak-M

2010-03-19

REV : -1

DY : Nopop Component
B_TPM:Use Lom TPM
C_TPM:Use China TPM

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

Size: Custom | Document Number: Fonseca UMA | Rev: X02

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Fonseca 14" UMA Block Diagram

	DF3-14
Project code	91.4GN01.001
PCB P/N	48.4GN01.0SC
Revision	09276 - SC

Clock Generator
SLG8SP585VTR 7

Thermal & Fan
EMC4022 39

DDR III DIMM1
1067Mhz 18

DDR III DIMM2
1067Mhz 19

Channel A

Channel B

Intel Mobile CPU
Arrandale
rPGA988A 8~14

eDP

eDP-LCD Panel
BL Converter 54

DMIx4

FDI

Intel PCH
Ibex Peak-M
HM55
12 USB 2.0/1.1 ports
10/100/1000Mb ETHERNET
High Definition Audio
4 SATA ports
6 PCIE ports
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
20~28

BTO(1)
Smart CARD Socket 67

O2
OZ77CR6 34

BTO(2)
PC CARD Socket 72

1394 Connector 71

SD/SDHC/MMC Socket 71

Ricoh
R5U242 32

BTO(3)
Power SW(NewCard)
TPS2231MRGPR 72

New Card Connector 72

USB2.0
X1

PCIE

PCIE

SMBus

INT1

INT2

Free Fall Sensor
DE351IDL 40

HDD CONN 59

SATA

SATA

ODD CONN 59

SATA

USB Port x 2 63

X2

USB2.0

TCM (Option)
ZTE 36

LPC

WLAN Switch 64

Int KB

TouchPad
KSI/KSO
ECE1077 68

BC

PS2

EC
MEC 5045 37

BC

SIO Expander
ECE 5028 38

Serial Port
IO Board 76

LPC

SPI

SPI FLASH
64Mb 62

FLASH
8Mb 35

LOM
ESW
BCM5761E 35

RJ45 76
IO Board

CRT

Display Port (B)

Display Port (C)

USB2.0

SATA

PCIE

X2

VSW
MAX4885EETG+ 75

CRT CONN 55

Docking
E/Family 74

Digital MIC
Module 73

HD AUDIO

Azalia
CODEC
IDT
92HD81
OP AMP 30

TLV320AIC3004 75

MIC Jack

HP Jack

2CH SPEAKER (1W/1W) 60

MDC (Option)
Module
IO Board 76

RJ11 76
IO Board

Bluetooth (Option)
Module 73

Camera (Option)
Module 73

USB Port x 2
IO Board 76

X2

1/2 Mini-Card
WLAN Module 64

Mini-Card
WWAN Module
IO Board 76

Finger Printer
AES2880 (Option)
FP Board 78

CPU DC/DC 47
ISL62883

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC 46
TPS51125

INPUTS	OUTPUTS
+PWR_SRC	+3.3V_ALW +5V_ALW

SYSTEM DC/DC 50
TPS51116

INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT

SYSTEM DC/DC 52
TPS51218

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM LDO 51
RT9035

INPUTS	OUTPUTS
+3.3V_SUS	+1.8V_RUN

SYSTEM DC/DC 53
ADP3211

INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

BATTERY CHARGER 45
TI BQ24745
(AC, Battery Existence)

INPUTS	OUTPUTS
+DC_IN_SS	+PBATT

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Title: Block Diagram

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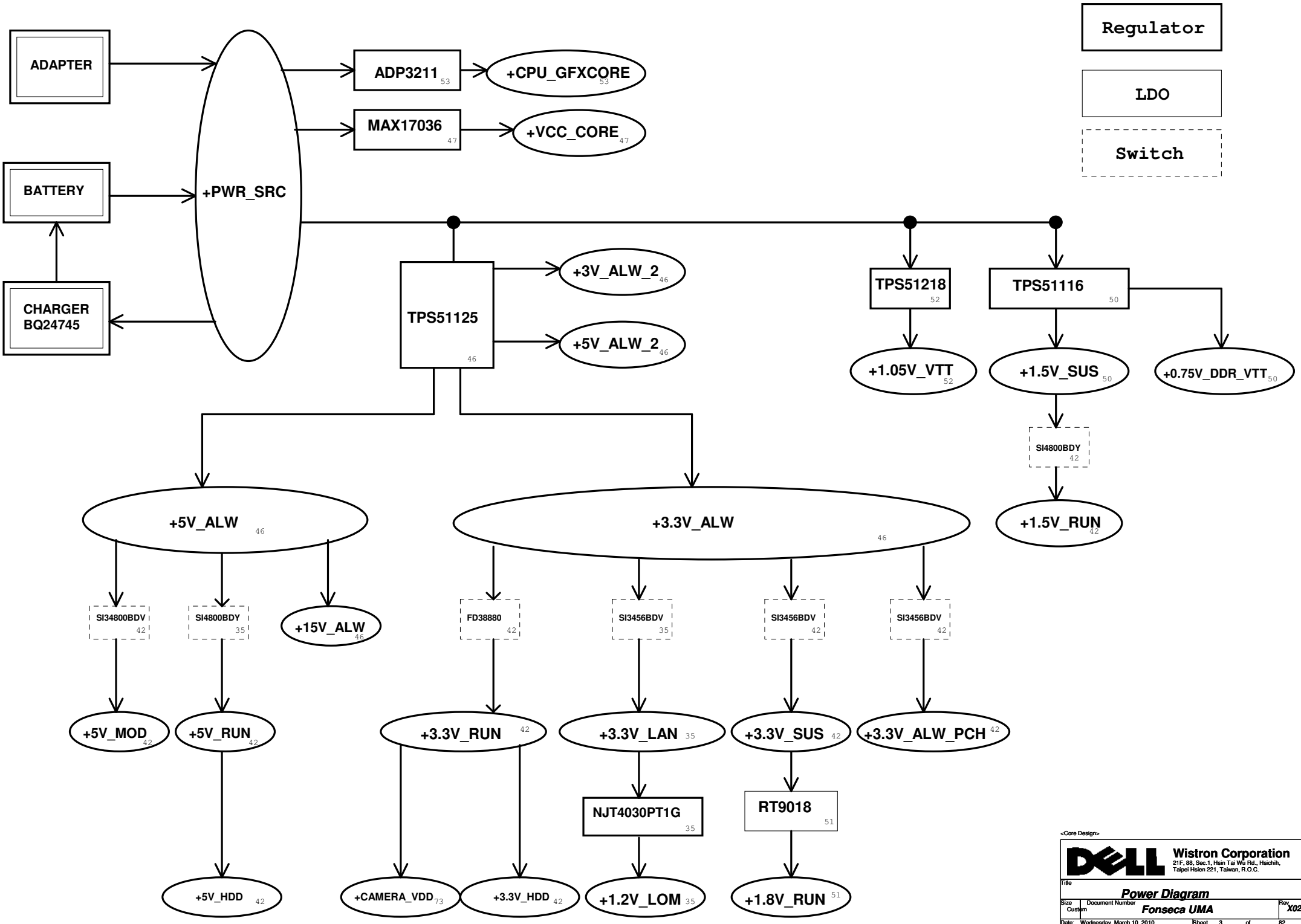

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Title: Power Diagram

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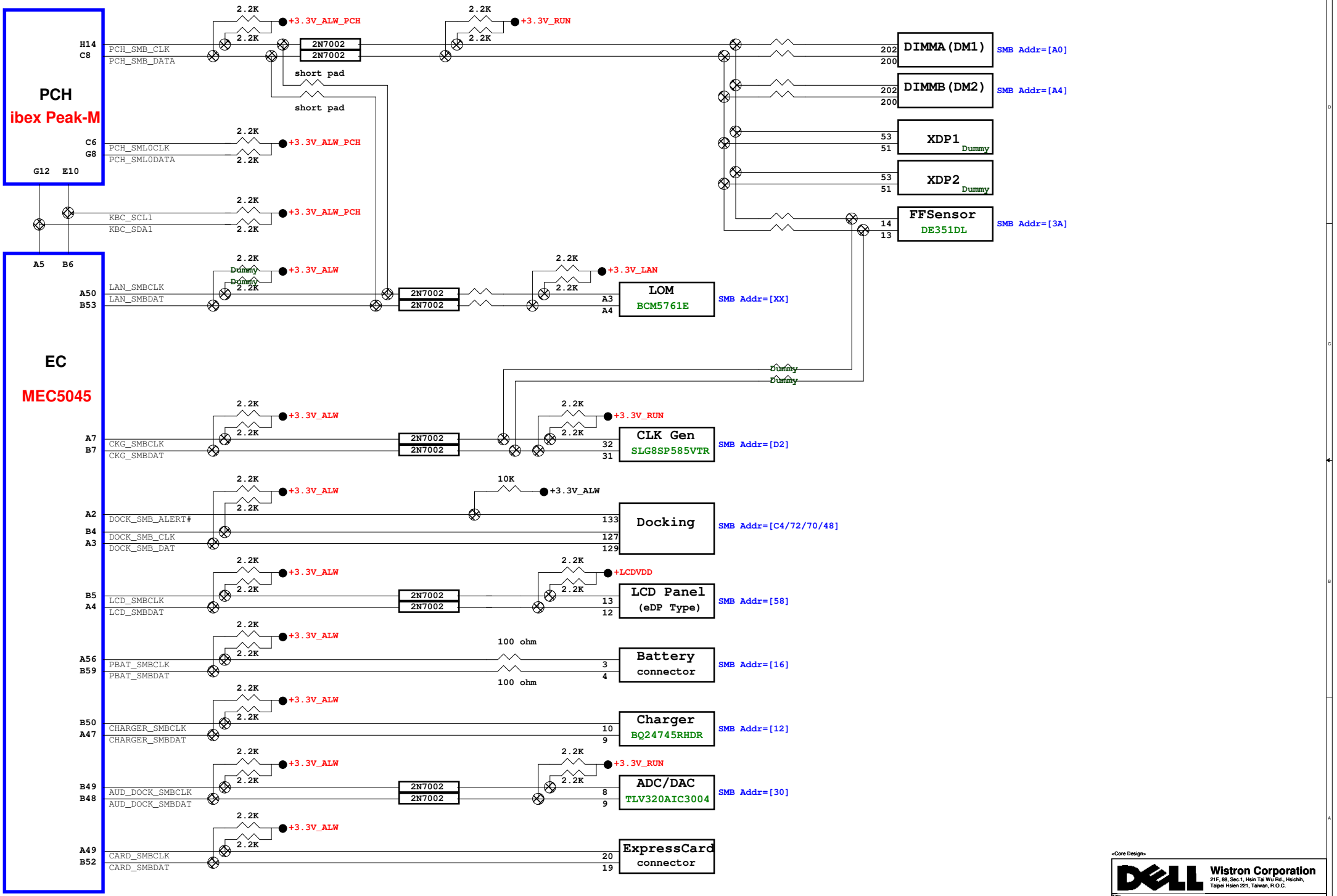

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Title: SMBus Diagram

Size: A2 | Document Number: Fonseca UMA | Rev: X02

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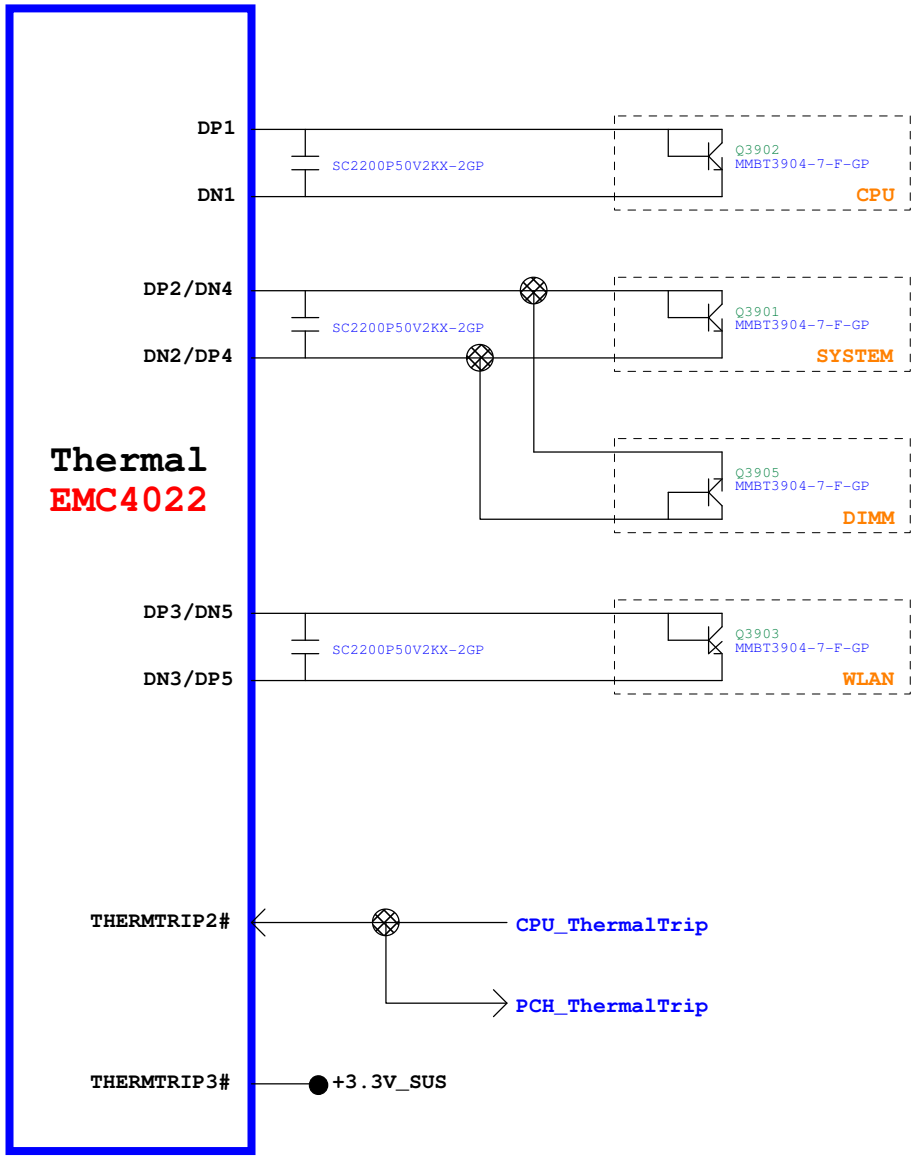
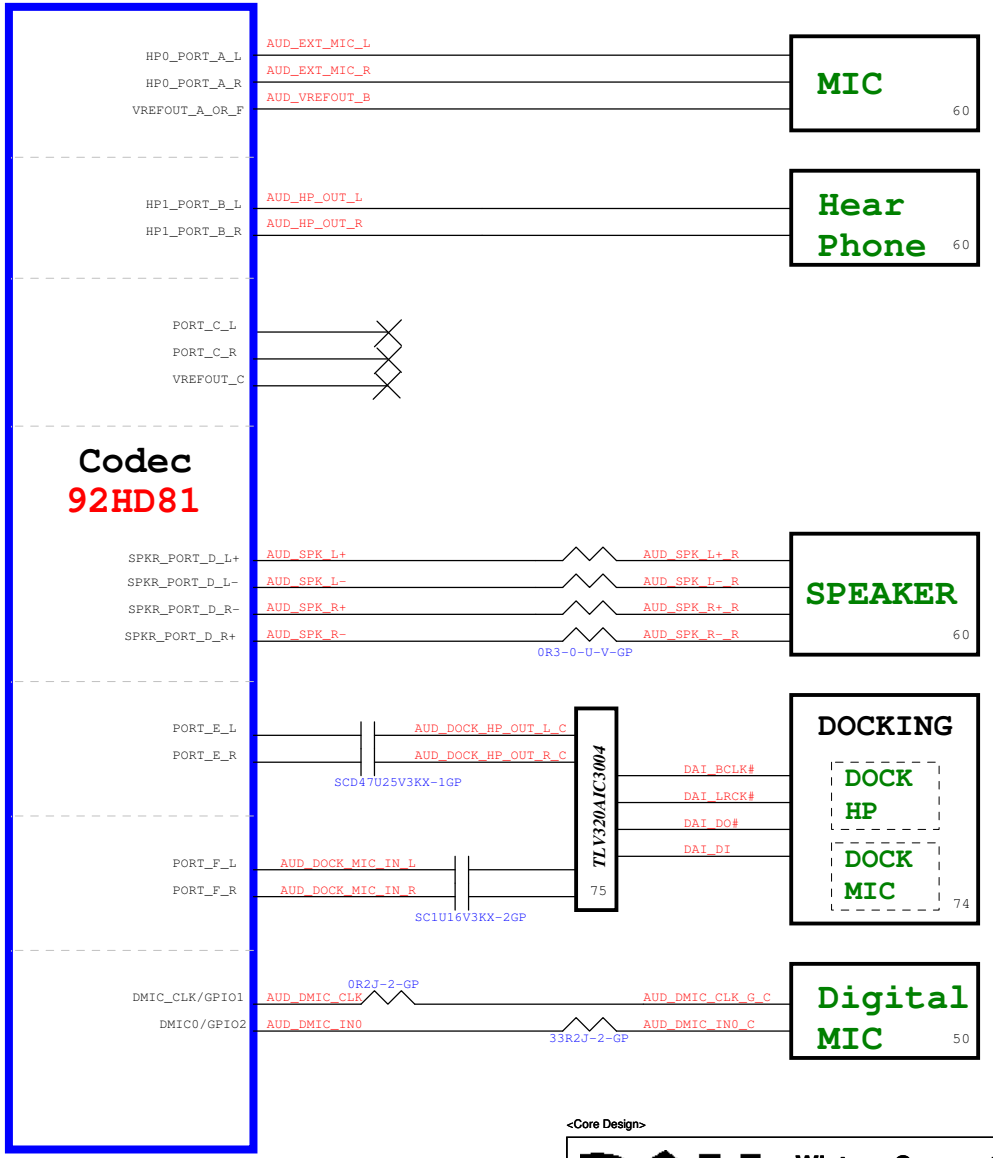
Thermal Block Diagram



Audio Block Diagram



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Title: AUDIO/THERMAL Diagram

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PCH Strapping

Calpella Schematic Checklist Rev: 1.6

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ ~ 10-kΩ weak pull-up resistor.
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** **Note:** Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ ; do not stuff resistor
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled** **Note:** CRB uses a 330-k resistor.
GNT0#, GNT1#	**Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default –** Internal pull-up. **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	**Enable Intel Anti-Theft Technology:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Intel Anti-Theft Technology:** Left floating, no pull-down required.
NV_ALE	**Enable Intel Anti-Theft Technology:** Connect to +NVRAM_VCCQ with 8.2-kΩ weak pull-up resistor [CRB has it pulled up with 1-kΩ no-stuff resistor] **Disable Intel Anti-Theft Technology:** Leave floating (internal pull-down).
NV_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HDA_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. **High (1):** Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. **Note:** CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) – Intel ME Crypto Transport Layer Security TLS) cipher suite with no confidentiality. High (1) – Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note: This is an unmuxed signal. This signal has a weak internal pull-down of 20KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1K pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	**Default =** Do not connect (floating). Internal pull-up. High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev: 1.6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**

PCIE Routing

LANE1	WWAN
LANE2	WLAN
LANE3	PCMCIA
LANE4	Express Card
LANE5	None
LANE6	10M/100M/1G LAN
LANE7	**Not available for HM55**
LANE8	**Not available for HM55**

USB Routing

USB	
Pair	**Device**
0	**USB0 @ MB**
1	**USB1 @ MB**
2	**USB2 @ IO Board**
3	**USB3 @ IO Board**
4	**WLAN**
5	**Bluetooth**
6	**Not available for HM55**
7	**Not available for HM55**
8	**DOCKING PORT1**
9	**DOCKING PORT2**
10	**Finger Printer**
11	**Camera**
12	**PCCard / SmartCard**
13	**WWAN**

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Title: Table of Content

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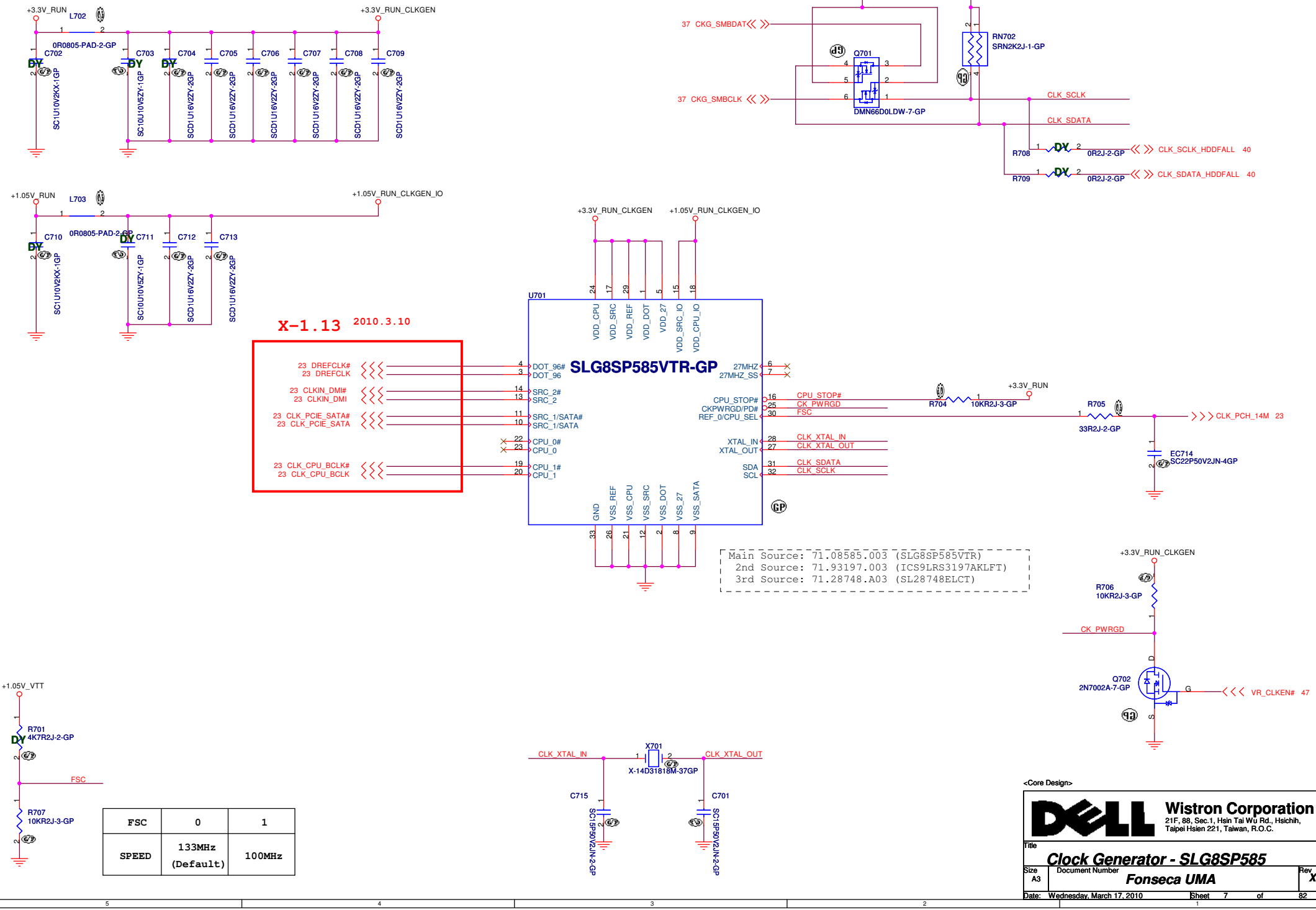
SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator - SLG8SP585

Size	Document Number	Rev
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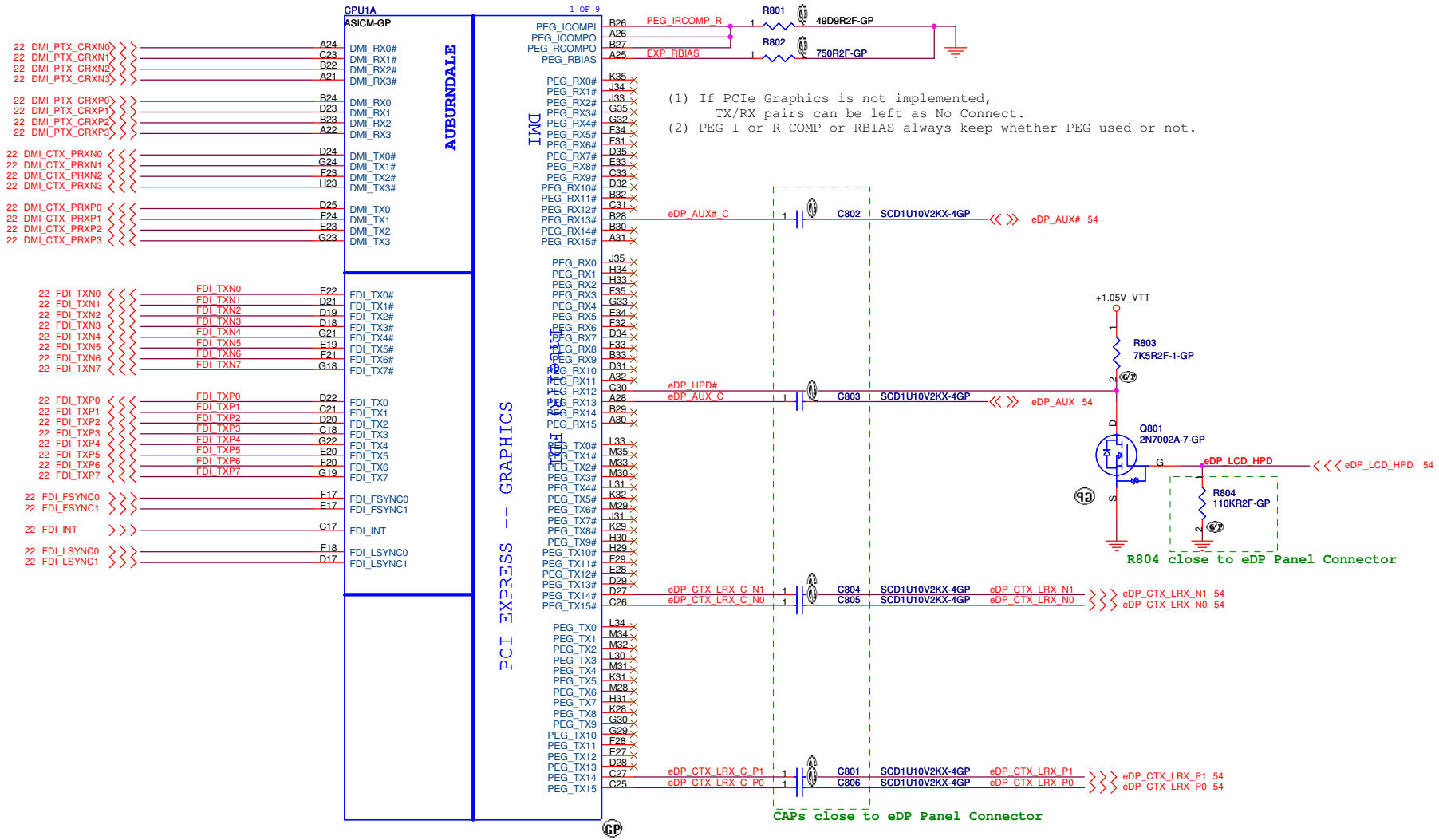
SSID = CPU



<Core Design>

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Title: CPU - PCIE/DMI/FDI (1/7)

Size: A3 | Document Number: Fonseca UMA | Rev: X02

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SSID = CPU

X-1.28 2010.3.18

Processor Pullups

+1.05V_VTT

R903 DY 49D9R2F-GP H_CATERR#

R906 DY 49D9R2F-GP H_PROCHOT#

R908 DY 68R2-GP H_CPURST#

X-1.28 2010.3.18

+3.3V_RUN +1.05V_VTT

R912 8K2R2J-3-GP

R913 DY 2K2R2J-2-GP

1.05V_VTT_Q901

Q901 MMBT3904-2-F-GP

38 CPU_CATERR#

C901 DY SCD1U10V2KX-4GP

Place near U3801

Processor Compensation Signals

R902 20R2F-GP H_COMP3

R904 20R2F-GP H_COMP2

R905 49D9R2F-GP H_COMP1

R907 49D9R2F-GP H_COMP0

37 H_SKTOCC#

H_CATERR#

25 H_PECI

47 H_PROHOT#

25,39 H_THERMTRIP#

58 H_CPURST#

H_PM_SYNC

25,58 H_PWRGD

R917 0R0402-PAD-2-GP

R919 0R0402-PAD-2-GP

22 DRAM_PWROK

52 H_VTTPWRGD

58 H_PWRGD_XDP

21,58 PLTRST1#

R921 1K5R2F-2-GP

R924 750R2F-GP

CPU1B

COMP3	AT23	ASICM-GP
COMP2	AT24	
COMP1	G16	
COMP0	AT26	
SKTOCC#	AH24	
CATERR#	AK14	
PECI	AT15	
PROCHOT#	AN26	
THERMTRIP#	AK15	
RESET_OBS#	AP26	
PM_SYNC	AL15	
VCCPWRGOOD_1	AN14	
VCCPWRGOOD_0	AN27	
SM_DRAMPWROK	AK13	
VTTPWRGOOD	AM15	
TAPPWRGOOD	AM26	
RSTIN#	AL14	

2 OF 9

AUBURNDALE MISC CLOCKS

DDR3 THERMAL MISC

PWR MANAGEMENT & JTAG

BCLK	A16	BCLK_CPU_P_R
BCLK#	B16	BCLK_CPU_N_R
BCLK_ITP	AR30	BCLK_ITP_P_R
BCLK_ITP#	AT30	BCLK_ITP_N_R
PEG_CLK	E16	PEG_CLK_R
PEG_CLK#	D16	PEG_CLK#_R
DPLL_REF_SSCLK	A18	DPLL_REF_SSCLK_R
DPLL_REF_SSCLK#	A17	DPLL_REF_SSCLK#_R
SM_DRAMRST#	F6	SM_DRAMRST#
SM_RCOMP0	AL1	SM_RCOMP_0
SM_RCOMP1	AM1	SM_RCOMP_1
SM_RCOMP2	AN1	SM_RCOMP_2
PM_EXT_TS0#	AN15	PM_EXT_TS#
PM_EXT_TS1#	AP15	
PRDY#	AT28	XDP_PRDY#
PREQ#	AP27	XDP_PREQ#
TCK	AN28	XDP_TCLK
TMS	AP28	XDP_TMS
TRST#	AT27	XDP_TRST#
TDI	AT29	XDP_TDI_R
TDO	AR27	XDP_TDO_R
TDI_M	AP29	XDP_TDI_M
TDO_M	AP29	XDP_TDO_M
DBR#	AN25	H_DBR#_R
BPM0#	AJ22	XDP_OBS0
BPM1#	AK22	XDP_OBS1
BPM2#	AK24	XDP_OBS2
BPM3#	AJ24	XDP_OBS3
BPM4#	AJ25	XDP_OBS4
BPM5#	AH22	XDP_OBS5
BPM6#	AK23	XDP_OBS6
BPM7#	AH23	XDP_OBS7

RN903 0R4P2R-PAD

R914 10KR2J-3-GP

R918 0R0402-PAD-2-GP

XDP_DBRESET# 22,38,58

DDR_HVREF_RST_GATE 37

C903 SCD047U10V2KX-2GP

+1.5V_SUS

R934 1KR2J-1-GP

DDR3_DRAMRST# 18,19

Q902 2N7002A-7-GP

R935 DY 0R2J-2-GP

R939 DY 100KR2J-1-GP

C902 SC470P50V2KX-3GP

DDR3 Compensation Signals

SM_RCOMP_0 R909 100R2F-L1-GP-U

SM_RCOMP_1 R910 24D9R2F-L-GP

SM_RCOMP_2 R911 130R2F-1-GP

+1.05V_VTT

XDP_TMS R922 DY 51R2J-2-GP

XDP_TDI_R R923 DY 51R2J-2-GP

XDP_PREQ# R925 DY 51R2J-2-GP

XDP_TCLK R926 DY 51R2J-2-GP

22,35,38,50 SIO_SLP_S3#

37,38,58 RUNPWROK

R915 0R0402-PAD-2-GP

R920 0R0402-PAD-2-GP

RUNPWROK_C

U901 74LVC1G08GW-1-GP

+3.3V_ALW_PCH

+3.3V_SUS

R938 0R2J-2-GP DY

DRAM_PWROK_R

R936 1K5R2F-2-GP

DRAM_PWROK

R937 750R2F-GP

JTAG MAPPING

XDP_TDI_R R929 0R0402-PAD-2-GP XDP_TDI

XDP_TDI XDP_TDI 58

XDP_TDO_M R930 DY 0R2J-2-GP XDP_TDO

XDP_TDO XDP_TDO 58

R901 0R0402-PAD-2-GP

XDP_TDI_M R931 DY 0R2J-2-GP R932

XDP_TDO_R 0R0402-PAD-2-GP

XDP_TRST# R933 51R2J-2-GP

Scan Chain (Default)	Stuff --> R929, R901, R932 No Stuff --> R930, R931
CPU Only	Stuff --> R929, R930 No Stuff --> R901, R931, R932
GMCH Only	Stuff --> R931, R932 No Stuff --> R929, R930, R901

X01.09/0917

<Core Design>

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Title: CPU Thermal/Clock/PM (2/7)

Size: A3 | Document Number: Fonseca UMA | Rev: X02

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SSID = CPU

CPU1C
ASICM-GP
3 OF 9

AUBURNDALE

DDR SYSTEM MEMORY A

18 M_A_DQ[63..0]

M_A_DQ0	A10	SA_DQ0
M_A_DQ1	C10	SA_DQ1
M_A_DQ2	C7	SA_DQ2
M_A_DQ3	A7	SA_DQ3
M_A_DQ4	B10	SA_DQ4
M_A_DQ5	D10	SA_DQ5
M_A_DQ6	E10	SA_DQ6
M_A_DQ7	A8	SA_DQ7
M_A_DQ8	D8	SA_DQ8
M_A_DQ9	F10	SA_DQ9
M_A_DQ10	E6	SA_DQ10
M_A_DQ11	F7	SA_DQ11
M_A_DQ12	E9	SA_DQ12
M_A_DQ13	B7	SA_DQ13
M_A_DQ14	E7	SA_DQ14
M_A_DQ15	C6	SA_DQ15
M_A_DQ16	H10	SA_DQ16
M_A_DQ17	G8	SA_DQ17
M_A_DQ18	K7	SA_DQ18
M_A_DQ19	J8	SA_DQ19
M_A_DQ20	G7	SA_DQ20
M_A_DQ21	G10	SA_DQ21
M_A_DQ22	J7	SA_DQ22
M_A_DQ23	J10	SA_DQ23
M_A_DQ24	L7	SA_DQ24
M_A_DQ25	M6	SA_DQ25
M_A_DQ26	M8	SA_DQ26
M_A_DQ27	L9	SA_DQ27
M_A_DQ28	L6	SA_DQ28
M_A_DQ29	K8	SA_DQ29
M_A_DQ30	N8	SA_DQ30
M_A_DQ31	P9	SA_DQ31
M_A_DQ32	AH5	SA_DQ32
M_A_DQ33	AF5	SA_DQ33
M_A_DQ34	AK6	SA_DQ34
M_A_DQ35	AK7	SA_DQ35
M_A_DQ36	AF6	SA_DQ36
M_A_DQ37	AG5	SA_DQ37
M_A_DQ38	AJ7	SA_DQ38
M_A_DQ39	AJ6	SA_DQ39
M_A_DQ40	AJ10	SA_DQ40
M_A_DQ41	AJ9	SA_DQ41
M_A_DQ42	AL10	SA_DQ42
M_A_DQ43	AK12	SA_DQ43
M_A_DQ44	AK8	SA_DQ44
M_A_DQ45	AL7	SA_DQ45
M_A_DQ46	AK11	SA_DQ46
M_A_DQ47	AL8	SA_DQ47
M_A_DQ48	AN8	SA_DQ48
M_A_DQ49	AM10	SA_DQ49
M_A_DQ50	AR11	SA_DQ50
M_A_DQ51	AL11	SA_DQ51
M_A_DQ52	AM9	SA_DQ52
M_A_DQ53	AN9	SA_DQ53
M_A_DQ54	AT11	SA_DQ54
M_A_DQ55	AP12	SA_DQ55
M_A_DQ56	AM12	SA_DQ56
M_A_DQ57	AN12	SA_DQ57
M_A_DQ58	AM13	SA_DQ58
M_A_DQ59	AT14	SA_DQ59
M_A_DQ60	AT12	SA_DQ60
M_A_DQ61	AL13	SA_DQ61
M_A_DQ62	AR14	SA_DQ62
M_A_DQ63	AP14	SA_DQ63

18 M_A_BS0	AC3	SA_BS0
18 M_A_BS1	AB2	SA_BS1
18 M_A_BS2	U7	SA_BS2

18 M_A_CAS#	AE1	SA_CAS#
18 M_A_RAS#	AB3	SA_RAS#
18 M_A_WE#	AE9	SA_WE#

SA_CK0	AA6	M_CLK_DDR0 18
SA_CK0#	AA7	M_CLK_DDR#0 18
SA_CKE0	P7	M_CKE0 18
SA_CK1	Y6	M_CLK_DDR1 18
SA_CK1#	Y5	M_CLK_DDR#1 18
SA_CKE1	P6	M_CKE1 18
SA_CS0#	AE2	M_CS#0 18
SA_CS1#	AE8	M_CS#1 18
SA_ODT0	AD8	M_ODT0 18
SA_ODT1	AF9	M_ODT1 18

SA_DM0	B9	M_A_DM0
SA_DM1	D7	M_A_DM1
SA_DM2	H7	M_A_DM2
SA_DM3	M7	M_A_DM3
SA_DM4	AG6	M_A_DM4
SA_DM5	AM7	M_A_DM5
SA_DM6	AN10	M_A_DM6
SA_DM7	AN13	M_A_DM7

M_A_DM[7..0] 18
M_A_DQS#[7..0] 18
M_A_DQS[7..0] 18
M_A_A[15..0] 18

SA_DQS0#	C9	M_A_DQS#0
SA_DQS1#	F8	M_A_DQS#1
SA_DQS2#	J9	M_A_DQS#2
SA_DQS3#	N9	M_A_DQS#3
SA_DQS4#	AH7	M_A_DQS#4
SA_DQS5#	AK9	M_A_DQS#5
SA_DQS6#	AP11	M_A_DQS#6
SA_DQS7#	AT13	M_A_DQS#7

SA_DQS0	C8	M_A_DQS0
SA_DQS1	F9	M_A_DQS1
SA_DQS2	H9	M_A_DQS2
SA_DQS3	M9	M_A_DQS3
SA_DQS4	AH8	M_A_DQS4
SA_DQS5	AK10	M_A_DQS5
SA_DQS6	AN11	M_A_DQS6
SA_DQS7	AR13	M_A_DQS7

SA_MA0	Y3	M_A_A0
SA_MA1	W1	M_A_A1
SA_MA2	AA8	M_A_A2
SA_MA3	AA3	M_A_A3
SA_MA4	V1	M_A_A4
SA_MA5	AA9	M_A_A5
SA_MA6	V8	M_A_A6
SA_MA7	T1	M_A_A7
SA_MA8	Y9	M_A_A8
SA_MA9	U6	M_A_A9
SA_MA10	AD4	M_A_A10
SA_MA11	T2	M_A_A11
SA_MA12	U3	M_A_A12
SA_MA13	AG8	M_A_A13
SA_MA14	T3	M_A_A14
SA_MA15	V9	M_A_A15

CPU1D
ASICM-GP
4 OF 9

AUBURNDALE

DDR SYSTEM MEMORY - B

19 M_B_DQ[63..0]

M_B_DQ0	B5	SB_DQ0
M_B_DQ1	A5	SB_DQ1
M_B_DQ2	C3	SB_DQ2
M_B_DQ3	B3	SB_DQ3
M_B_DQ4	E4	SB_DQ4
M_B_DQ5	A6	SB_DQ5
M_B_DQ6	A4	SB_DQ6
M_B_DQ7	C4	SB_DQ7
M_B_DQ8	D1	SB_DQ8
M_B_DQ9	D2	SB_DQ9
M_B_DQ10	F2	SB_DQ10
M_B_DQ11	F1	SB_DQ11
M_B_DQ12	C2	SB_DQ12
M_B_DQ13	F5	SB_DQ13
M_B_DQ14	F3	SB_DQ14
M_B_DQ15	G4	SB_DQ15
M_B_DQ16	H6	SB_DQ16
M_B_DQ17	G2	SB_DQ17
M_B_DQ18	J6	SB_DQ18
M_B_DQ19	J3	SB_DQ19
M_B_DQ20	G1	SB_DQ20
M_B_DQ21	G5	SB_DQ21
M_B_DQ22	J2	SB_DQ22
M_B_DQ23	J1	SB_DQ23
M_B_DQ24	J5	SB_DQ24
M_B_DQ25	K2	SB_DQ25
M_B_DQ26	L3	SB_DQ26
M_B_DQ27	M1	SB_DQ27
M_B_DQ28	K5	SB_DQ28
M_B_DQ29	K4	SB_DQ29
M_B_DQ30	M4	SB_DQ30
M_B_DQ31	N5	SB_DQ31
M_B_DQ32	AF3	SB_DQ32
M_B_DQ33	AG1	SB_DQ33
M_B_DQ34	AJ3	SB_DQ34
M_B_DQ35	AK1	SB_DQ35
M_B_DQ36	AG4	SB_DQ36
M_B_DQ37	AG3	SB_DQ37
M_B_DQ38	AJ4	SB_DQ38
M_B_DQ39	AH4	SB_DQ39
M_B_DQ40	AK3	SB_DQ40
M_B_DQ41	AK4	SB_DQ41
M_B_DQ42	AM6	SB_DQ42
M_B_DQ43	AN2	SB_DQ43
M_B_DQ44	AK5	SB_DQ44
M_B_DQ45	AK2	SB_DQ45
M_B_DQ46	AM4	SB_DQ46
M_B_DQ47	AM3	SB_DQ47
M_B_DQ48	AP3	SB_DQ48
M_B_DQ49	AN5	SB_DQ49
M_B_DQ50	AT4	SB_DQ50
M_B_DQ51	AN6	SB_DQ51
M_B_DQ52	AN4	SB_DQ52
M_B_DQ53	AN3	SB_DQ53
M_B_DQ54	AT5	SB_DQ54
M_B_DQ55	AT6	SB_DQ55
M_B_DQ56	AN7	SB_DQ56
M_B_DQ57	AP6	SB_DQ57
M_B_DQ58	AP8	SB_DQ58
M_B_DQ59	AT9	SB_DQ59
M_B_DQ60	AT7	SB_DQ60
M_B_DQ61	AP9	SB_DQ61
M_B_DQ62	AR10	SB_DQ62
M_B_DQ63	AT10	SB_DQ63

19 M_B_BS0	AB1	SB_BS0
19 M_B_BS1	W5	SB_BS1
19 M_B_BS2	R7	SB_BS2

19 M_B_CAS#	AC5	SB_CAS#
19 M_B_RAS#	Y7	SB_RAS#
19 M_B_WE#	AC6	SB_WE#

SB_CK0	W8	M_CLK_DDR2 19
SB_CK0#	W9	M_CLK_DDR#2 19
SB_CKE0	M3	M_CKE2 19
SB_CK1	V7	M_CLK_DDR3 19
SB_CK1#	V6	M_CLK_DDR#3 19
SB_CKE1	M2	M_CKE3 19
SB_CS0#	AB8	M_CS#2 19
SB_CS1#	AD6	M_CS#3 19
SB_ODT0	AC7	M_ODT2 19
SB_ODT1	AD1	M_ODT3 19

SB_DM0	D4	M_B_DM0
SB_DM1	E1	M_B_DM1
SB_DM2	H3	M_B_DM2
SB_DM3	K1	M_B_DM3
SB_DM4	AH1	M_B_DM4
SB_DM5	AL2	M_B_DM5
SB_DM6	AR4	M_B_DM6
SB_DM7	AT8	M_B_DM7

M_B_DM[7..0] 19
M_B_DQS#[7..0] 19
M_B_DQS[7..0] 19
M_B_A[15..0] 19

SB_DQS0#	D5	M_B_DQS#0
SB_DQS1#	F4	M_B_DQS#1
SB_DQS2#	J4	M_B_DQS#2
SB_DQS3#	L4	M_B_DQS#3
SB_DQS4#	AH2	M_B_DQS#4
SB_DQS5#	AL4	M_B_DQS#5
SB_DQS6#	AR5	M_B_DQS#6
SB_DQS7#	AR8	M_B_DQS#7

SB_DQS0	C5	M_B_DQS0
SB_DQS1	E3	M_B_DQS1
SB_DQS2	H4	M_B_DQS2
SB_DQS3	M5	M_B_DQS3
SB_DQS4	AG2	M_B_DQS4
SB_DQS5	AL5	M_B_DQS5
SB_DQS6	AP5	M_B_DQS6
SB_DQS7	AR7	M_B_DQS7

SB_MA0	U5	M_B_A0
SB_MA1	V2	M_B_A1
SB_MA2	T5	M_B_A2
SB_MA3	V3	M_B_A3
SB_MA4	R1	M_B_A4
SB_MA5	T8	M_B_A5
SB_MA6	R2	M_B_A6
SB_MA7	R6	M_B_A7
SB_MA8	R4	M_B_A8
SB_MA9	R5	M_B_A9
SB_MA10	AB5	M_B_A10
SB_MA11	P3	M_B_A11
SB_MA12	R3	M_B_A12
SB_MA13	AF7	M_B_A13
SB_MA14	P5	M_B_A14
SB_MA15	N1	M_B_A15

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU - DDR (3/7)**

Size	Document Number	Rev
A3	Fonseca UMA	X02

Date: Thursday, March 18, 2010 Sheet 10 of 82

SSID = CPU

SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor

CPU Piin AJ13 and AJ12:
Core voltage sense line.
Via from PGA pad to the back of the MB and provide test point.
Do not route any additional trace.

CPU1E
ASICM-GP
5 OF 9

AUBURNDALE

RESERVED

RSVD#AJ13	AJ13	H_RSVD32	TP1118
RSVD#AJ12	AJ12	H_RSVD33	TP1117
RSVD#AH25	AH25		
RSVD#AK26	AK26	H_RSVD35	TP1119
RSVD#AL26	AL26	H_RSVD36	TP1120
RSVD_NCTF#AR2	AR2		
RSVD#AJ26	AJ26		
RSVD#AJ27	AJ27		

TP1115	VREF_CH_A_DIMM	AP25	RSVD#AP25
TP1116	VREF_CH_B_DIMM	AL25	RSVD#AL25
		AL24	RSVD#AL24
		AL22	RSVD#AL22
		AJ33	RSVD#AJ33
		AG9	RSVD#AG9
		M27	RSVD#M27
		L28	RSVD#L28
		J17	SA_DIMM_VREF#
		H17	SB_DIMM_VREF#
		G25	RSVD#G25
		G17	RSVD#G17
		E31	RSVD#E31
		E30	RSVD#E30

	CFG0	AM30	CFG0
TP1101	CFG1	AM28	CFG1
TP1102	CFG2	AP31	CFG2
	CFG3	AL32	CFG3
	CFG4	AL30	CFG4
TP1103	CFG5	AM31	CFG5
TP1104	CFG6	AN29	CFG6
	CFG7	AM32	CFG7
TP1105	CFG8	AK32	CFG8
TP1106	CFG9	AK31	CFG9
TP1107	CFG10	AK28	CFG10
TP1108	CFG11	AJ28	CFG11
TP1109	CFG12	AN30	CFG12
TP1110	CFG13	AN32	CFG13
TP1111	CFG14	AJ32	CFG14
TP1112	CFG15	AJ29	CFG15
TP1113	CFG16	AJ30	CFG16
TP1114	CFG17	AK30	CFG17
		H16	RSVD_TP#H16

RSVD#AL28	AL28	
RSVD#AL29	AL29	
RSVD#AP30	AP30	
RSVD#AP32	AP32	
RSVD#AL27	AL27	
RSVD#AT31	AT31	
RSVD#AT32	AT32	
RSVD#AP33	AP33	
RSVD#AR33	AR33	
RSVD#AR32	AR32	
RSVD_TP#E15	E15	
RSVD_TP#F15	F15	
KEY	A2	
RSVD#D15	D15	
RSVD#C15	C15	
RSVD#AJ15	AJ15	
RSVD#AH15	AH15	

	B19	RSVD#B19
	A19	RSVD#A19
	A20	RSVD#A20
	B20	RSVD#B20
	U9	RSVD#U9
	T9	RSVD#T9
	AC9	RSVD#AC9
	AB9	RSVD#AB9

RSVD_TP#AA5	AA5	
RSVD_TP#AA4	AA4	
RSVD_TP#R8	R8	
RSVD_TP#AD3	AD3	
RSVD_TP#AD2	AD2	
RSVD_TP#AA2	AA2	
RSVD_TP#AA1	AA1	
RSVD_TP#R9	R9	
RSVD_TP#AG7	AG7	
RSVD_TP#AE3	AE3	
RSVD_TP#V4	V4	
RSVD_TP#V5	V5	
RSVD_TP#N2	N2	
RSVD_TP#AD5	AD5	
RSVD_TP#AD7	AD7	
RSVD_TP#W3	W3	
RSVD_TP#W2	W2	
RSVD_TP#N3	N3	
RSVD_TP#AE5	AE5	
RSVD_TP#AD9	AD9	
VSS	AP34	RSVD_VSS

	J29	RSVD#J29
	J28	RSVD#J28

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

R1117 0R0402-PAD-2-GP

CFG0
R1102 3K01R2F-3-GP

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled (Clarkfiled only)

CFG3
R1105 3K01R2F-3-GP

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4
R1109 3K3R2J-3-GP

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7
R1103 3K01R2F-3-GP

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU - Reserve (4/7)

Size	Document Number	Rev
Custom	Fonseca UMA	X02

Date: Thursday, March 18, 2010 Sheet 11 of 82

SSID = CPU

PROCESSOR CORE POWER

48A

+VCC_CORE

CPU1F
ASICM-GP
6 OF 9

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that
The VTT Rail values are
Arrandale for VTT=1.05V
Clarksfield for VTT=1.1V

Arrandale drives this pin High for 1.05V
Clarksfield drives this pin Low for 1.1V

Place near PU4701

<Core Design>

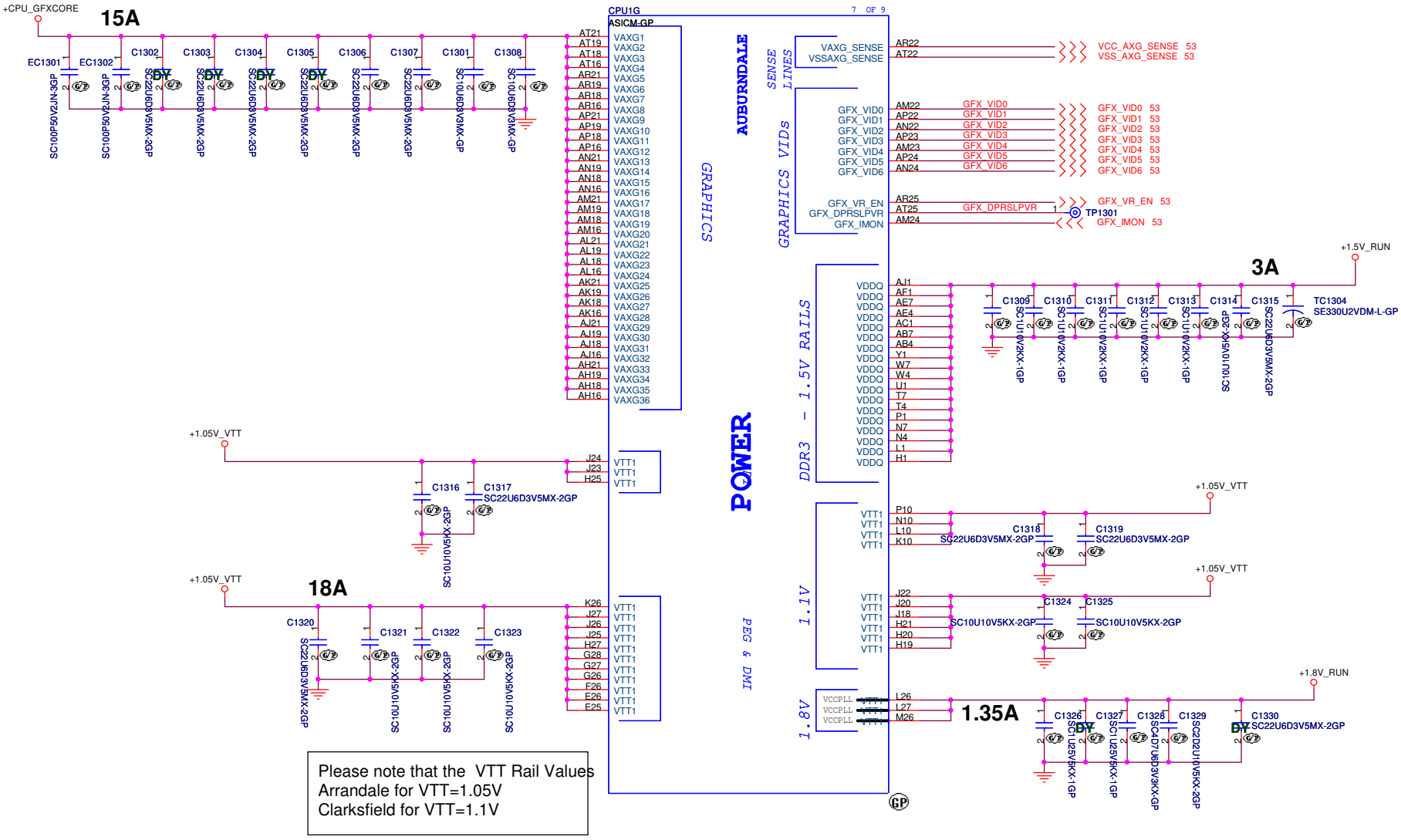
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU - VCC_CORE (5/7)

Size: Custom | Document Number: Fonseca UMA | Rev: X02

Date: Thursday, March 18, 2010 | Sheet 12 of 82

SSID = CPU



<Core Design>

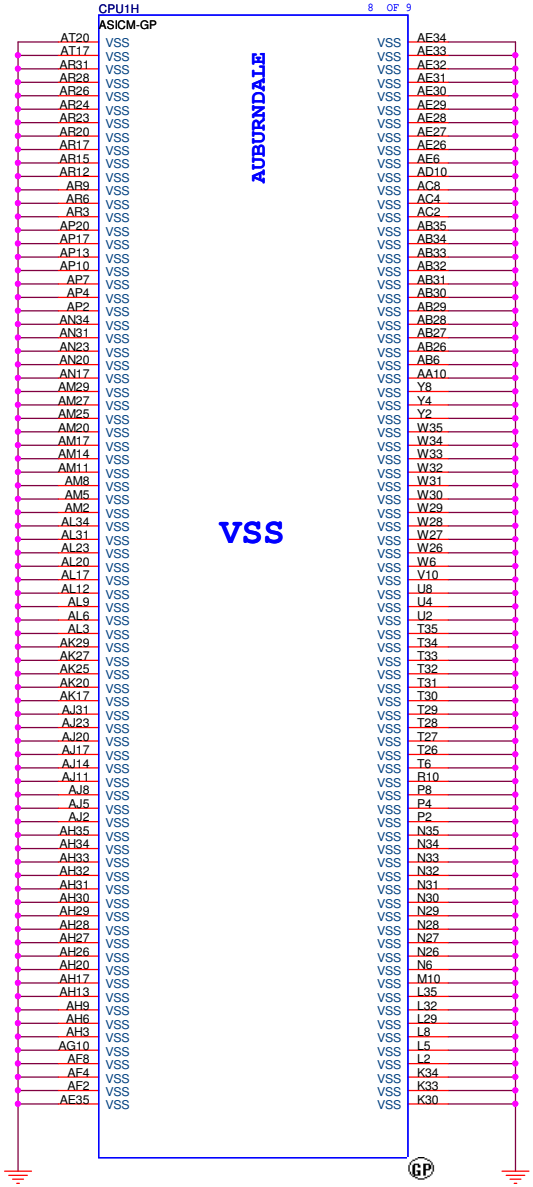
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

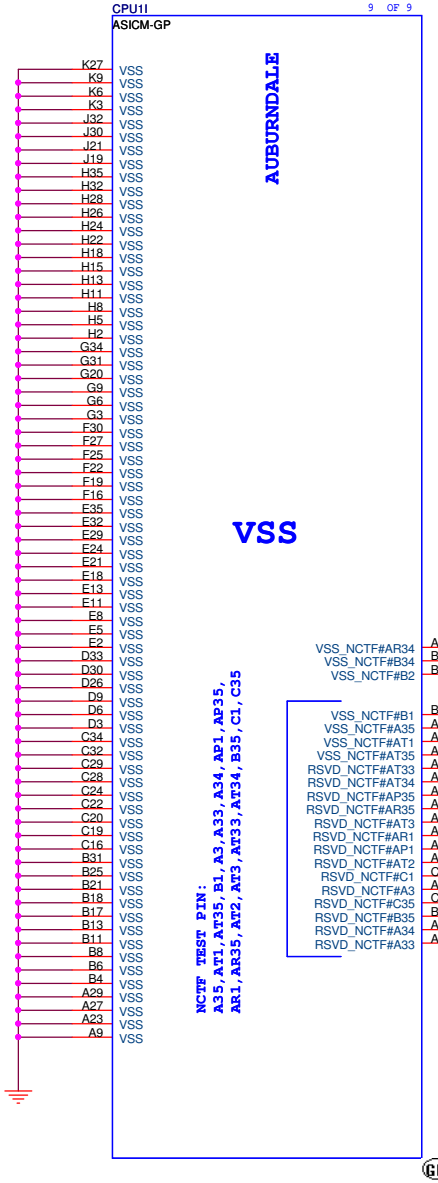
Title: CPU - GFXCORE (6/7)

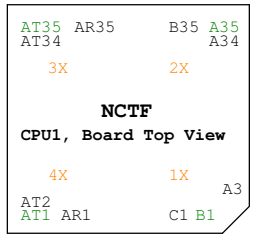
Size: A3 | Document Number: Fonseca UMA | Rev: X02

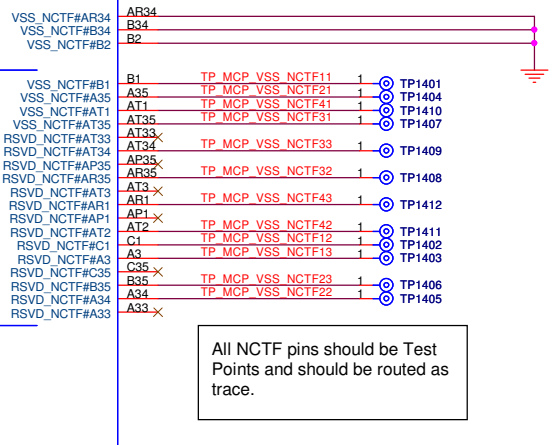
Date: Thursday, March 18, 2010 | Sheet 13 of 82

SSID = CPU









All NCTF pins should be Test Points and should be routed as trace.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*CPU - VSS (7/7)*	
Size: A3	Document Number: *Fonseca UMA*	Rev: *X02*
Date: Thursday, March 18, 2010	Sheet 14 of 82	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserve

Size	Document Number	Rev
Custom	***Fonseca UMA***	***X02***

Date:	Wednesday, March 10, 2010	Sheet	15	of	82

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserve

Size	Document Number	Rev
Custom	*Fonseca UMA*	*X02*

Date:	Wednesday, March 10, 2010	Sheet	16	of	82

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserve

Size	Document Number	Rev
Custom	***Fonseca UMA***	***X02***

Date:	Wednesday, March 10, 2010	Sheet	17	of	82

SSID = Memory

SO-DIMMA
H = 9.2mm

DM1

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15
10 M_A_BS2 79 A16/BA2
10 M_A_BS0 109 BA0
10 M_A_BS1 108 BA1

10 M_A_DQ[63..0]

M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 15 DQ2
M_A_DQ3 17 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 16 DQ6
M_A_DQ7 18 DQ7
M_A_DQ8 21 DQ8
M_A_DQ9 23 DQ9
M_A_DQ10 33 DQ10
M_A_DQ11 35 DQ11
M_A_DQ12 22 DQ12
M_A_DQ13 24 DQ13
M_A_DQ14 34 DQ14
M_A_DQ15 36 DQ15
M_A_DQ16 39 DQ16
M_A_DQ17 41 DQ17
M_A_DQ18 51 DQ18
M_A_DQ19 53 DQ19
M_A_DQ20 40 DQ20
M_A_DQ21 42 DQ21
M_A_DQ22 50 DQ22
M_A_DQ23 52 DQ23
M_A_DQ24 57 DQ24
M_A_DQ25 59 DQ25
M_A_DQ26 67 DQ26
M_A_DQ27 69 DQ27
M_A_DQ28 56 DQ28
M_A_DQ29 58 DQ29
M_A_DQ30 68 DQ30
M_A_DQ31 70 DQ31
M_A_DQ32 129 DQ32
M_A_DQ33 131 DQ33
M_A_DQ34 141 DQ34
M_A_DQ35 143 DQ35
M_A_DQ36 130 DQ36
M_A_DQ37 132 DQ37
M_A_DQ38 140 DQ38
M_A_DQ39 142 DQ39
M_A_DQ40 147 DQ40
M_A_DQ41 149 DQ41
M_A_DQ42 157 DQ42
M_A_DQ43 159 DQ43
M_A_DQ44 146 DQ44
M_A_DQ45 148 DQ45
M_A_DQ46 158 DQ46
M_A_DQ47 160 DQ47
M_A_DQ48 163 DQ48
M_A_DQ49 165 DQ49
M_A_DQ50 175 DQ50
M_A_DQ51 177 DQ51
M_A_DQ52 164 DQ52
M_A_DQ53 166 DQ53
M_A_DQ54 174 DQ54
M_A_DQ55 176 DQ55
M_A_DQ56 181 DQ56
M_A_DQ57 183 DQ57
M_A_DQ58 191 DQ58
M_A_DQ59 193 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63

M_A_DQS#0 10 DQS0#
M_A_DQS#1 27 DQS1#
M_A_DQS#2 45 DQS2#
M_A_DQS#3 62 DQS3#
M_A_DQS#4 135 DQS4#
M_A_DQS#5 152 DQS5#
M_A_DQS#6 169 DQS6#
M_A_DQS#7 186 DQS7#

M_A_DQS0 12 DQS0
M_A_DQS1 29 DQS1
M_A_DQS2 47 DQS2
M_A_DQS3 64 DQS3
M_A_DQS4 137 DQS4
M_A_DQS5 154 DQS5
M_A_DQS6 171 DQS6
M_A_DQS7 188 DQS7

10 M_ODT0 116 ODT0
10 M_ODT1 120 ODT1

M_VREF_CA_DIMM1 126 VREF_CA
M_VREF_DQ_DIMM1 1 VREF_DQ

9,19 DDR3_DRAMRST# 30 RESET#

MA_VTT 203 VTT1
204 VTT2

Reverse Type

DDR3-204P-42-GP

NP1 NP1
NP2 NP2

RAS# 110 M_A_RAS# 10
WE# 113 M_A_WE# 10
CAS# 115 M_A_CAS# 10

CS0# 114 M_CS#0 10
CS1# 121 M_CS#1 10

CKE0 73 M_CKE0 10
CKE1 74 M_CKE1 10

CK0 101 M_CLK_DDR0 10
CK0# 103 M_CLK_DDR#0 10

CK1 102 M_CLK_DDR1 10
CK1# 104 M_CLK_DDR#1 10

DM0 11 M_A_DM0
DM1 28 M_A_DM1
DM2 46 M_A_DM2
DM3 63 M_A_DM3
DM4 136 M_A_DM4
DM5 153 M_A_DM5
DM6 170 M_A_DM6
DM7 187 M_A_DM7

SDA 200 SODIMM1_1_SMB_DATA_R
SCL 202 SODIMM1_1_SMB_CLK_R

EVENT# 198
VDDSPD 199

SA0 197 SA0_DIMM1
SA1 201 SA1_DIMM1

NC#1 77
NC#2 122
NC#TEST 125

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

VSS 2
VSS 3
VSS 8
VSS 9
VSS 13
VSS 14
VSS 19
VSS 20
VSS 25
VSS 26
VSS 31
VSS 32
VSS 37
VSS 38
VSS 43
VSS 44
VSS 48
VSS 49
VSS 54
VSS 55
VSS 60
VSS 61
VSS 65
VSS 66
VSS 71
VSS 72
VSS 127
VSS 128
VSS 133
VSS 134
VSS 138
VSS 139
VSS 144
VSS 145
VSS 150
VSS 151
VSS 155
VSS 156
VSS 161
VSS 162
VSS 167
VSS 168
VSS 172
VSS 173
VSS 178
VSS 179
VSS 184
VSS 185
VSS 189
VSS 190
VSS 195
VSS 196
VSS 205
VSS 206

M_A_DM[7..0] 10
M_A_DQS#[7..0] 10
M_A_DQS[7..0] 10
M_A_A[15..0] 10

+3.3V_RUN
R1802 10KR2J-3-GP DY
SA0_DIMM1
SA1_DIMM1
R1803 0R0402-PAD-2-GP
R1801 0R0402-PAD-2-GP

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

R1804 0R0402-PAD-2-GP
R1805 0R0402-PAD-2-GP
PCH_SMBDATA_MEM 19,23,40,58
PCH_SMBCLK_MEM 19,23,40,58

+3.3V_RUN
C1802 SCD1U10V2KX-3GP DY
C1803 SC2D2U16V3KX-GP DY

+1.5V_SUS

+V_DDR_MCH_REF
R1807 0R0603-PAD-2-GP
M_VREF_CA_DIMM1
C1811 SCD1U10V2KX-5GP
C1812 SC2D2U16V3KX-GP

+V_DDR_MCH_REF
R1808 0R0603-PAD-2-GP
M_VREF_DQ_DIMM1
C1820 SCD1U10V2KX-5GP
C1821 SC2D2U16V3KX-GP

Place between DM1 and DM2.
+0.75V_DDR_VTT
C1822 SC10U10V5KX-2GP

+0.75V_DDR_VTT
R1809 0R0603-PAD-2-GP
MA_VTT

Place these caps close to VTT1 and VTT2.
C1823 SC1U10V2KX-1GP
C1824 SC1U10V2KX-1GP
C1825 SC1U10V2KX-1GP
C1826 SC1U10V2KX-1GP

SODIMM A DECOUPLING

+1.5V_SUS
TC1801 SP230U2D5VDM-2GP DY
C1804 SC1U6D3V6MX-GP
C1805 SC1U6D3V6MX-GP
C1806 SC470U6D3VM3G-GP
C1807 SC1U6D3V6MX-GP
C1808 SC1U6D3V6MX-GP
C1801 SC1U6D3V6MX-GP
C1809 SC1U6D3V6MX-GP DY
C1810 SC1U6D3V6MX-GP DY

Layout Note:
Place these Caps near SO-DIMMA.

C1813 SC1U6D3V6MX-GP
C1814 SC1U6D3V6MX-GP
C1815 SCD1U10V2KX-3GP
C1816 SC1U6D3V6MX-GP
C1817 SC1U10V2KX-1GP
C1818 SC1U10V2KX-1GP
C1819 SC1U10V2KX-1GP DY

+1.5V_SUS
+1.5V_RUN
Near Memory +1.5V_SUS Plane
Near CPU +1.5V_RUN Plane
C1827 SCD1U16V2ZY-2GP DY
C1828 SCD1U16V2ZY-2GP DY
C1829 SCD1U16V2ZY-2GP DY
C1830 SCD1U16V2ZY-2GP DY

62.10017.N61

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR III Socket - DM1**
Size: Custom | Document Number: **Fonseca UMA** | Rev: **X02**
Date: Wednesday, March 17, 2010 | Sheet 18 of 82

SSID = Memory

SO-DIMMB
H = 5.2mm

DM2

DDR3-204P-48-GP

Reverse Type

62.10017.P41

M_B_DM[7..0] 10
M_B_DQS#[7..0] 10
M_B_DQS[7..0] 10
M_B_A[15..0] 10

+3.3V_RUN
R1902 10KR2J-3-GP
SA1_DIMM2
SA0_DIMM2
R1903 0R0402-PAD-2-GP
R1904 0R2J-2-GP DY

SODIMM2_1_SMB_DATA_R
SODIMM2_1_SMB_CLK_R
R1905 0R0402-PAD-2-GP
R1906 0R0402-PAD-2-GP
PCH_SMBDATA_MEM 18,23,40,58
PCH_SMBCLK_MEM 18,23,40,58

+3.3V_RUN
C1902 SCD1U10V2KX-5GP DY
C1903 SC2D2U16V3KX-GP DY

+1.5V_SUS

+V_DDR_MCH_REF
R1907 0R0603-PAD-2-GP
M_VREF_CA_DIMM2
C1904 SCD1U10V2KX-5GP
C1905 SC2D2U16V3KX-GP

+V_DDR_MCH_REF
R1908 0R0603-PAD-2-GP
M_VREF_DQ_DIMM2
C1913 SCD1U10V2KX-5GP
C1914 SC2D2U16V3KX-GP

+0.75V_DDR_VTT
R1909 0R0603-PAD-2-GP
MB_VTT

Place these caps close to VTT1 and VTT2.
C1922 C1923 C1924 C1925 SC1U10V2KX-1GP

SODIMM B DECOUPLING
+1.5V_SUS
C1906 C1901 C1907 C1908 C1909 C1910 C1911 C1912 SC10U6D3V6MX-GP DY
C1915 C1916 C1917 C1918 SGX-XR2R91N1CDS
C1919 C1920 C1921 SC1U10V2KX-1GP

Layout Note:
Place these Caps near SO-DIMMB.

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

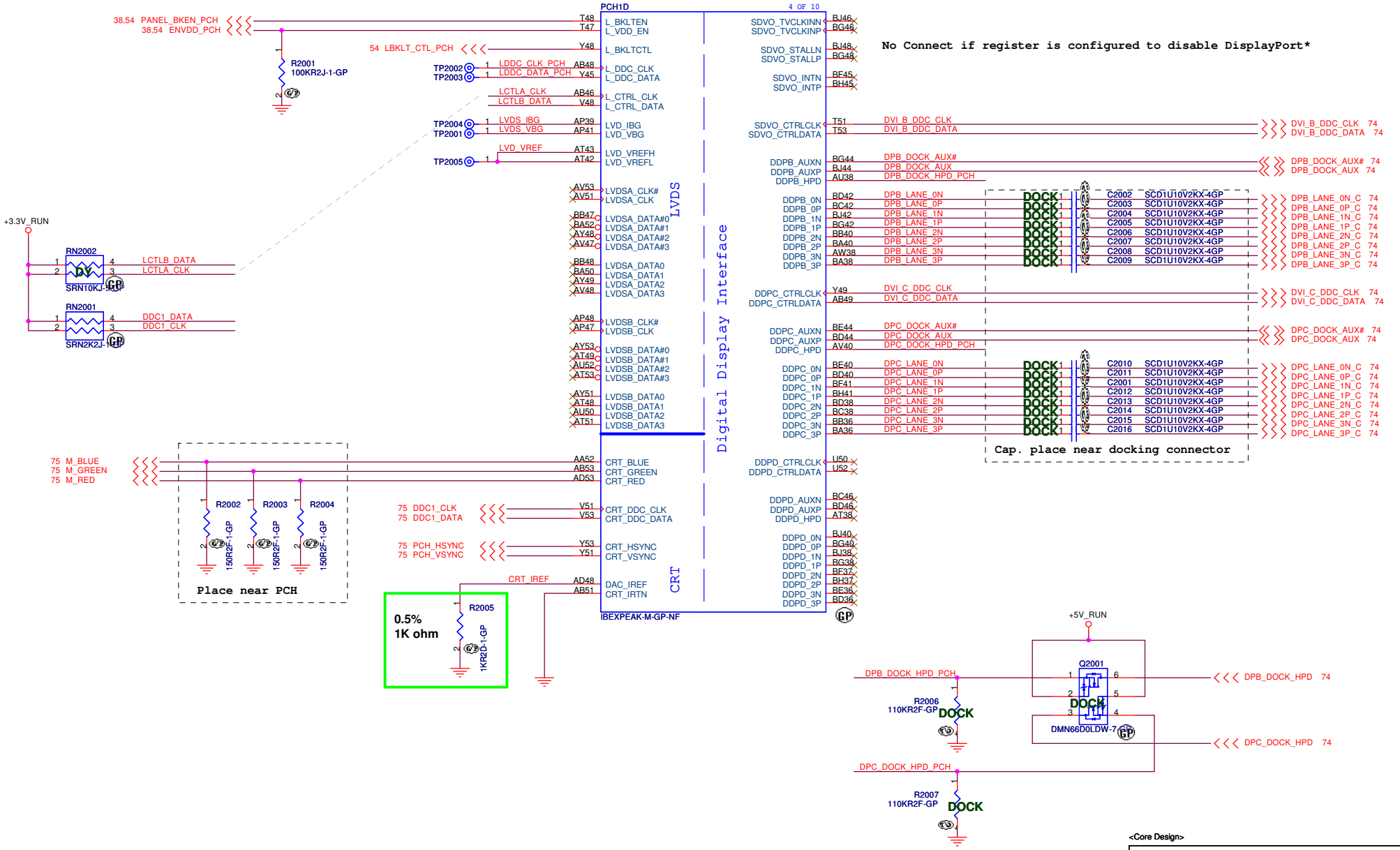
SO-DIMMB is placed farther from the Processor than SO-DIMMA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR III Socket - DM2
Size: Custom
Document Number: Fonseca UMA
Rev: X02
Date: Wednesday, March 17, 2010
Sheet 19 of 82

SSID = PCH



<Core Design>

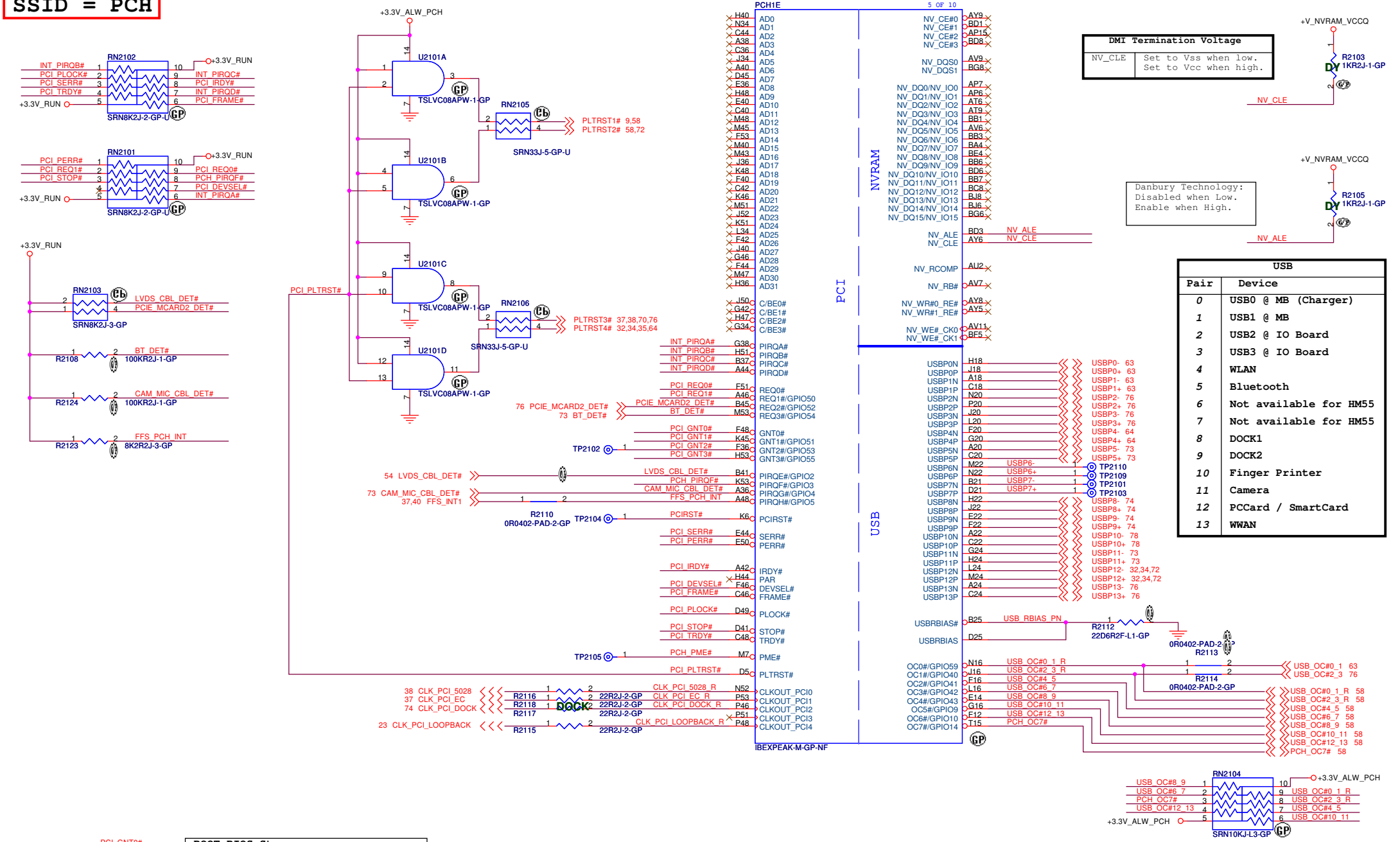
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - LVDS/CRT/DDI (1/9)

Size	Document Number	Rev
A3	Fonseca UMA	X02

Date: Thursday, March 18, 2010 Sheet 20 of 82

SSID = PCH



DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:
Disabled when Low.
Enable when High.

USB	
Pair	Device
0	USB0 @ MB (Charger)
1	USB1 @ MB
2	USB2 @ IO Board
3	USB3 @ IO Board
4	WLAN
5	Bluetooth
6	Not available for HM55
7	Not available for HM55
8	DOCK1
9	DOCK2
10	Finger Printer
11	Camera
12	PCCard / SmartCard
13	WWAN

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI(Default)

PCI_GNT[3:0]#: Internal pull high during Strap

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

<Core Design>

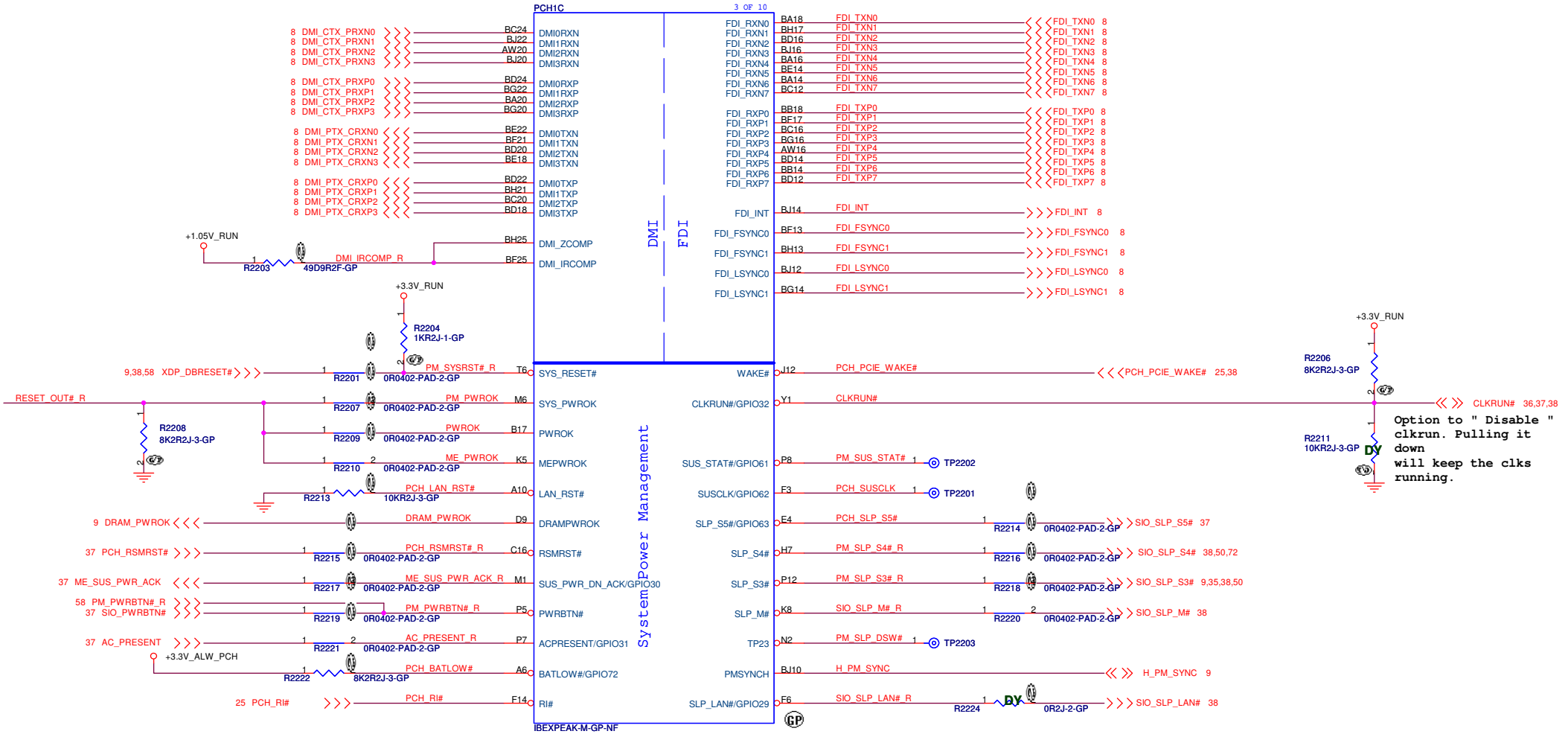
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

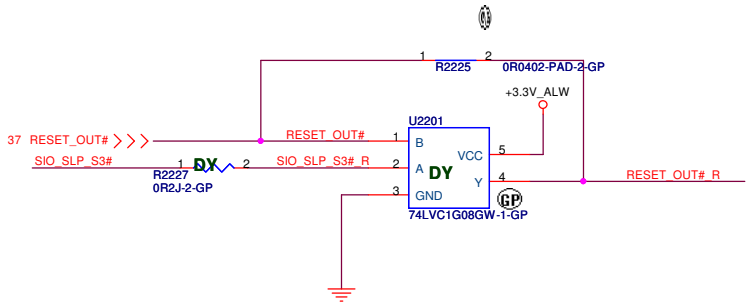
Title: PCH - PCI/USB/NVRAM (2/9)

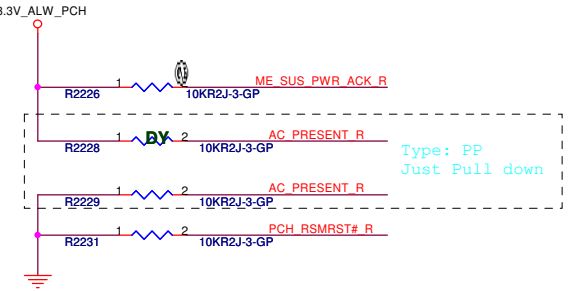
Size	Document Number	Rev
A3	Fonseca UMA	X02

Date: Thursday, March 18, 2010 Sheet 21 of 82

SSID = PCH







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - DMI/FDI/PM (3/9)

Size	Document Number	Rev
A3	Fonseca UMA	X02

Date: Thursday, March 18, 2010 Sheet 22 of 82

SSID = PCH

PCH1B

2 OF 10

PCIE_PRX_WWANTX_N1
PCIE_PRX_WWANTX_P1
PCIE_PTX_WWANRX_N1_C
PCIE_PTX_WWANRX_P1_C
C2301
C2302
PCIE_PTX_WWANRX_N1
PCIE_PTX_WWANRX_P1
SCD1U10V2KX-4GP
BG30 PERN1
BJ30 PERP1
BF29 PETN1
BH29 PETP1
WWAN

PCIE_PRX_WLANTX_N2
PCIE_PRX_WLANTX_P2
PCIE_PTX_WLANRX_N2_C
PCIE_PTX_WLANRX_P2_C
C2305
C2306
PCIE_PTX_WLANRX_N2
PCIE_PTX_WLANRX_P2
SCD1U10V2KX-4GP
AW30 PERN2
BA30 PERP2
BC30 PETN2
BD30 PETP2
WLAN

PCIE_PRX_R5U241TX_N3
PCIE_PRX_R5U241TX_P3
PCIE_PTX_R5U241RX_N3_C
PCIE_PTX_R5U241RX_P3_C
C2307
C2304
PCIE_PTX_R5U241RX_N3
PCIE_PTX_R5U241RX_P3
SCD1U10V2KX-4GP
AU30 PERN3
AT30 PERP3
AU32 PETN3
AV32 PETP3
PCMCIA

PCIE_PRX_EXPTX_N4
PCIE_PRX_EXPTX_P4
PCIE_PTX_EXPRX_N4_C
PCIE_PTX_EXPRX_P4_C
C2312
C2311
PCIE_PTX_EXPRX_N4
PCIE_PTX_EXPRX_P4
SCD1U10V2KX-4GP
BA32 PERN4
BB32 PERP4
BD32 PETN4
BE32 PETP4
Express Card

BF33 PERN5
BH33 PERP5
BG32 PETN5
BJ32 PETP5
WPAN

PCIE_PRX_GLANTX_N6
PCIE_PRX_GLANTX_P6
PCIE_PTX_GLANRX_N6_C
PCIE_PTX_GLANRX_P6_C
C2303
C2308
PCIE_PTX_GLANRX_N6
PCIE_PTX_GLANRX_P6
SCD1U10V2KX-4GP
BA34 PERN6
AW34 PERP6
BC34 PETN6
BD34 PETP6
LAN

PCIe port 7 and 8 may not be available for all Ibex Peak SKUs.

AT34 PERN7
AU34 PERP7
AU36 PETN7
AV36 PETP7

BG34 PERN8
BJ34 PERP8
BG36 PETN8
BJ36 PETP8

PCI-E* Controller Link

SMBus

SMBALERT#/GPIO11 B9 PCH_GPIO11
SMBCLK H14 PCH_SMB_CLK → PCH_SMB_CLK 37
SMBDATA C8 PCH_SMB_DATA → PCH_SMB_DATA 37
SML0ALERT#/GPIO60 J14 PCH_GPIO60
SML0CLK C6 PCH_SML0CLK
SML0DATA G8 PCH_SML0DATA
SML1ALERT#/GPIO74 M14 PCH_GPIO74
SML1CLK/GPIO58 E10 KBC_SCL1 → KBC_SCL1 37
SML1DATA/GPIO75 G12 KBC_SDA1 → KBC_SDA1 37

+3.3V_ALW_PCH
RN2309 SRN2K2J-4-GP

+3.3V_ALW_PCH
PCH_GPIO11 R2302 10KR2J-3-GP
PCH_GPIO60 R2303 10KR2J-3-GP
PCH_GPIO74 R2301 10KR2J-3-GP
PCH_GPIO47 R2304 10KR2J-3-GP

CL_CLK1 T13 CL_CLK → TP2301
CL_DATA1 T11 CL_DATA → TP2302
CL_RST1# T9 CL_RST# → TP2303

PEG_A_CLKRQ#/GPIO47 H1 PCH_GPIO47

X-1.14 2010.3.10

CLKOUT_PEG_A_N AD43
CLKOUT_PEG_A_P AD45
CLKOUT_DMI_N AN4 → PEG_CLK#_R 9
CLKOUT_DMI_P AN2 → PEG_CLK_R 9
CLKOUT_DP_N/CLKOUT_BCLK1_N AT1 → DPLL_REF_SSCLK#_R 9
CLKOUT_DP_P/CLKOUT_BCLK1_P AT3 → DPLL_REF_SSCLK_R 9

PEG

18,19,40,58 PCH_SMBCLK_MEM
18,19,40,58 PCH_SMBDATA_MEM

+3.3V_RUN
RN2310 SRN2K2J-1-GP
+3.3V_ALW_PCH
RN2305 SRN2K2J-1-GP
U2301
DMN66D0LDW-7
PCH_SMB_CLK
PCH_SMB_DATA

X-1.15 2010.3.10

+3.3V_ALW_PCH
R2307 DY PCIE_CLK_RQ0# → P9
10KR2J-3-GP

CLKIN_DMI_N AW24 CLKIN_DMI# → CLKIN_DMI# 7
CLKIN_DMI_P BA24 CLKIN_DMI → CLKIN_DMI 7
CLKIN_BCLK_N AP3 CLK_CPU_BCLK# → CLK_CPU_BCLK# 7
CLKIN_BCLK_P AP1 CLK_CPU_BCLK → CLK_CPU_BCLK 7
CLKIN_DOT_96N F18 DREFCLK# → DREFCLK# 7
CLKIN_DOT_96P E18 DREFCLK → DREFCLK 7
CLKIN_SATA_N/CKSSCD_N AH13 CLK_PCIE_SATA# → CLK_PCIE_SATA# 7
CLKIN_SATA_P/CKSSCD_P AH12 CLK_PCIE_SATA → CLK_PCIE_SATA 7
REFCLK14IN P41 CLK_PCH_14M → CLK_PCH_14M 7
CLKIN_PCILOOPBACK J42 CLK_PCI_LOOPBACK → CLK_PCI_LOOPBACK 21

35 CLK_PCIE_LOM#
35 CLK_PCIE_LOM
AK48 CLKOUT_PCIE0N
AK47 CLKOUT_PCIE0P
PCIECLKRQ0#/GPIO73

AM43 CLKOUT_PCIE1N
AM45 CLKOUT_PCIE1P
LAN
35 LOM_CLKREQ# → LOM_CLKREQ# U4
PCIECLKRQ1#/GPIO18

32 CLK_PCIE_R5U241#
32 CLK_PCIE_R5U241
AM47 CLKOUT_PCIE2N
AM48 CLKOUT_PCIE2P
PCMCIA
32,58 PCMCLK_REQ# → PCMCLK_REQ# N4
PCIECLKRQ2#/GPIO20
+3.3V_RUN
R2319 10KR2J-3-GP

+3.3V_ALW_PCH
AH42 CLKOUT_PCIE3N
AH41 CLKOUT_PCIE3P
WPAN
R2308 PCIE_CLK_RQ3# → A8
10KR2J-3-GP
PCIECLKRQ3#/GPIO25

72 CLK_PCIE_EXP#
72 CLK_PCIE_EXP
RN2311
CLK_PCIE_EXP_N
CLK_PCIE_EXP_P
SRN0J-6-GP
AM51 CLKOUT_PCIE4N
AM53 CLKOUT_PCIE4P
Express Card
EXPCLK_REQ#_PCH → M9
PCIECLKRQ4#/GPIO26

64 CLK_PCIE_MINI1#
64 CLK_PCIE_MINI1
AJ50 CLKOUT_PCIE5N
AJ52 CLKOUT_PCIE5P
WLAN
MINI1CLK_REQ#_PCH → H6
PCIECLKRQ5#/GPIO44

76 CLK_PCIE_MINI2#
76 CLK_PCIE_MINI2
AK53 CLKOUT_PEG_B_N
AK51 CLKOUT_PEG_B_P
WWAN
MINI2CLK_REQ#_PCH → P13
PEG_B_CLKRQ#/GPIO56

Clock Flex

XTAL25_IN AH51 XTAL25_IN
XTAL25_OUT AH53 XTAL25_OUT
XCLK_RCOMP AF38 XCLK_RCOMP
+1.05V_RUN
R2317 90D9R2F-1-GP

CLKOUTFLEX0/GPIO64 T45 CLK_SIO_14M_R
R2314 22R2J-2-GP → CLK_SIO_14M 38
CLKOUTFLEX1/GPIO65 P43 CLK_PCI_TPM_CHA_R
R2315 22R2J-2-GP → CLK_JETWAY_14M 36
R2309 22R2J-2-GP → CLK_PCI_TPM_CHA 36
CLKOUTFLEX2/GPIO66 T42 CLK_PCI_TPM_R
R2313 22R2J-2-GP → CLK_PCI_TPM 35,70
CLKOUTFLEX3/GPIO67 N50 CLK48_PCH
R2311 22R2J-2-GP → CLK_SC_48M 34
R2312 22R2J-2-GP → CLK_FD_48M 75

J_TPM
C_TPM
B_TPM
SC
DOCK

XTAL25_IN
XTAL25_OUT
R2316 1MR2J-1-GP
X2301 XTAL-25MHZ-96GP
C2310 SC12P50V2JN-3GP
C2309 SC12P50V2JN-3GP

From Intel DG 1.6
CLKOUTFLEX{3:0}
RS on PCI/NonPCI Routing (for single / double-load)
=> 22 ohm series resistor

EC2301 SC22P50V2JN-4GP
EC2302 SC56P50V2JN-2GP

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

IBEXPEAK-M-GP-NF

+3.3V_ALW_PCH
RN2314 SRN10KJ-5-GP
EXPCLK_REQ#_PCH
MINI2CLK_REQ#_PCH

+3.3V_RUN
Q2303 2N7002A-7-GP
76 MINI2CLK_REQ# → MINI2CLK_REQ#_PCH

+3.3V_RUN
Q2304 2N7002A-7-GP
72 EXPCLK_REQ# → EXPCLK_REQ#_PCH

+3.3V_RUN
+3.3V_ALW_PCH
Q2302 2N7002A-7-GP
R2305 10KR2J-3-GP
58,64 MINI1CLK_REQ# → MINI1CLK_REQ#_PCH

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - PCIE/SMBUS/CLOCK/CL (4/9)
Size: A3
Document Number: Fonseca UMA
Rev: X02
Date: Thursday, March 18, 2010
Sheet 23 of 82

SSID = PCH

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

PCH1A — 1 OF 10 — IBEXPEAK-M-GP-NF

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
LPC: LPC_LAD[0..3], LPC_LFRAME#, LPC_LDRQ0#, LPC_LDRQ1#, SERIRQ
IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO13
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO
SATA: SATA0RXN/RXP/TXN/TXP, SATA1RXN/RXP/TXN/TXP, SATA2RXN/RXP/TXN/TXP, SATA3RXN/RXP/TXN/TXP, SATA4RXN/RXP/TXN/TXP, SATA5RXN/RXP/TXN/TXP, SATAICOMPO, SATAICOMPI, SATALED#, SATA0GP/GPIO21, SATA1GP/GPIO19

HDD
ODD
DOCKING eSATA

SATA port 2 and 3 may not be available for all Ibex Peak SKUs.

For EMI, RF Cap.

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

Place near PCH side

Form DG1.5
TRST# on PCH does not belong to JTAG interface.
For ES1 silicon, an ext. pull up 3.3-V Sus is required for bias internal state.
A 20-K/10-K voltage divider to this signal to 1.1 V.
However, from ES2 silicon onward, this signal is a No Connect regardless if JTAG interface on PCH is enabled or not.

Pull up +3.3V_M enable iAMT(DY disable)

Internal pull-up of 20K for HDA_DOCK_EN#,

integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

<Core Design>

20.F1000.003

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - SPI/RTC/LPC/SATA/IHDA (5/9)
Size: A3 | Document Number: Fonseca UMA | Rev: X02
Date: Thursday, March 18, 2010 | Sheet 24 of 82

SSID = PCH

PCH1F

6 OF 10

X-1.16 2010.3.10

Place 2 R close to PCH

from Checklist 1.5
VSS_NCTF
Pins can be connected to GND or left as NC (floating).

When tied to GND they should be routed as trace and not as a GND plane.

Note: CRB has some NCTF pins tied to GND and some left float

Internal pull up GPIO27 to enable VccVRM

NCTF
PCH1, Board Top View

TPM ID	ID0=0	ID0=1
ID1=0	C_TPM	RSVD
ID1=1	NONE	B_TPM

B_TPM

CTPM and DisableBTPM

B_TPM and DisableBTPM

C_TPM

<Core Design>

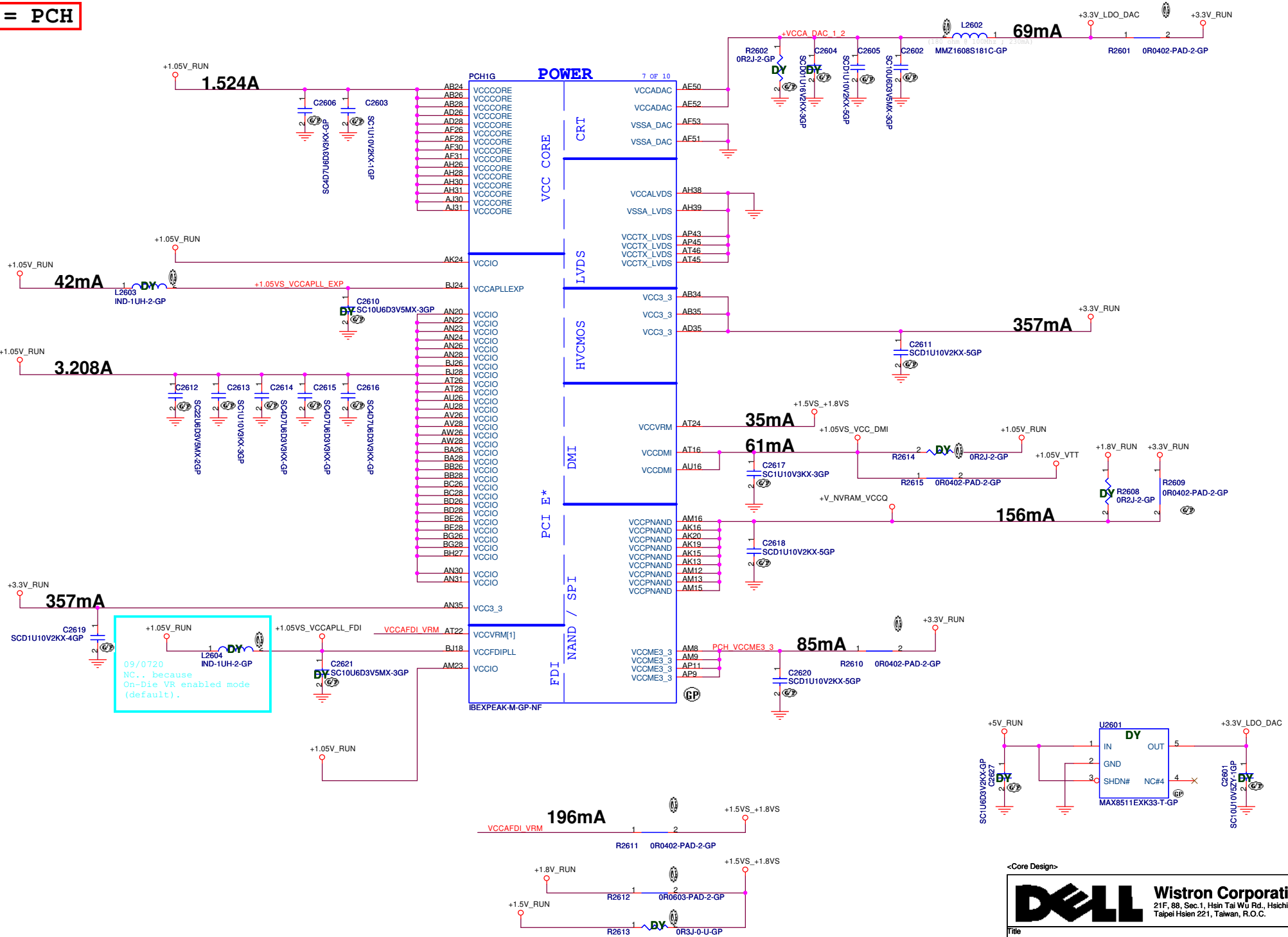
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - GPIO/CPU/MISC (6/9)

Size: A3 | Document Number: Fonseca UMA | Rev: X02

Date: Thursday, March 18, 2010 | Sheet 25 of 82

SSID = PCH



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Title: PCH (7/9)

Size	Document Number	Rev
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Date: Wednesday, March 17, 2010 Sheet 26 of 82

SSID = PCH

PCH1J

POWER

10 OF 10

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

CPU

RTC

HDA

IBEXPEAK-M-GP-NF

52mA

1.998A

(344mA)

72mA

73mA

163mA

1mA

2mA

6mA

32mA

<Core Design>

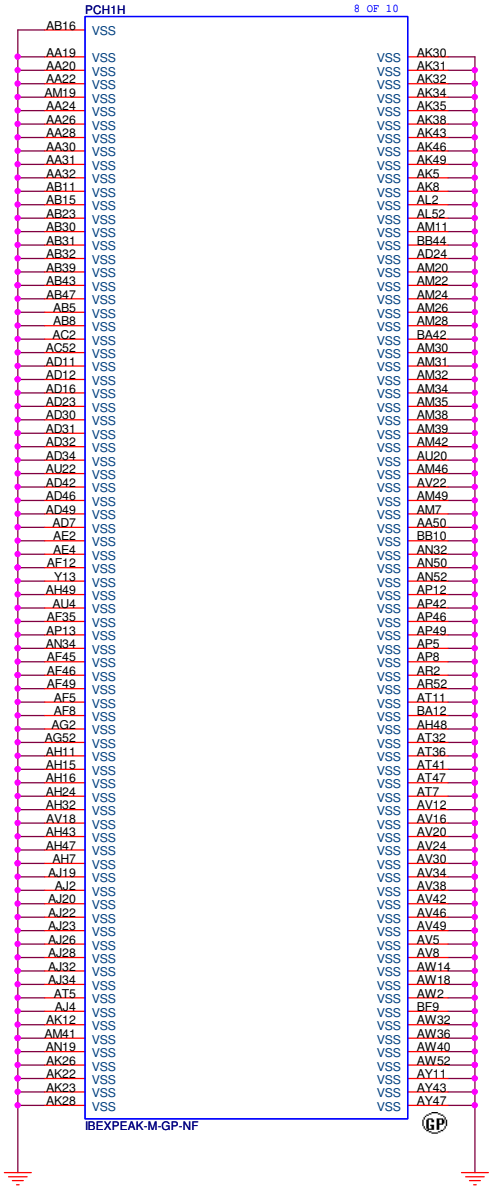
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

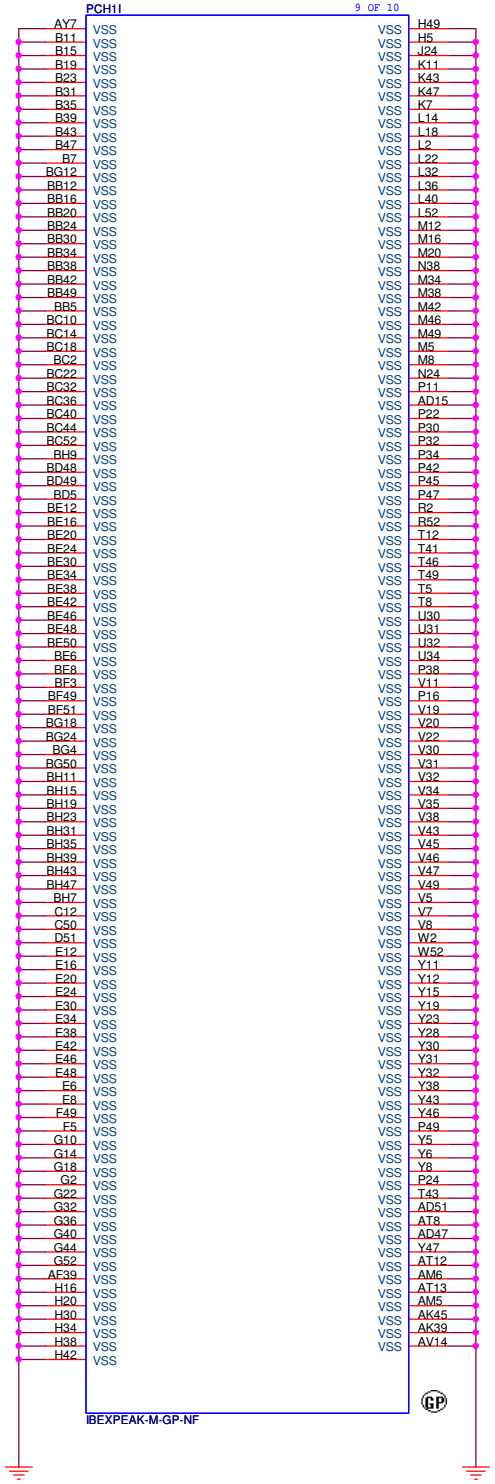
Title: PCH (8/9)

Size: A3 | Document Number: Fonseca UMA | Rev: X02

Date: Wednesday, March 17, 2010 | Sheet 27 of 82

SSID = PCH





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *PCH (9/9)*		
Size: A3	Document Number: *Fonseca UMA*	Rev: *X02*
Date: Wednesday, March 17, 2010	Sheet 28 of 82	

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<Core Design>

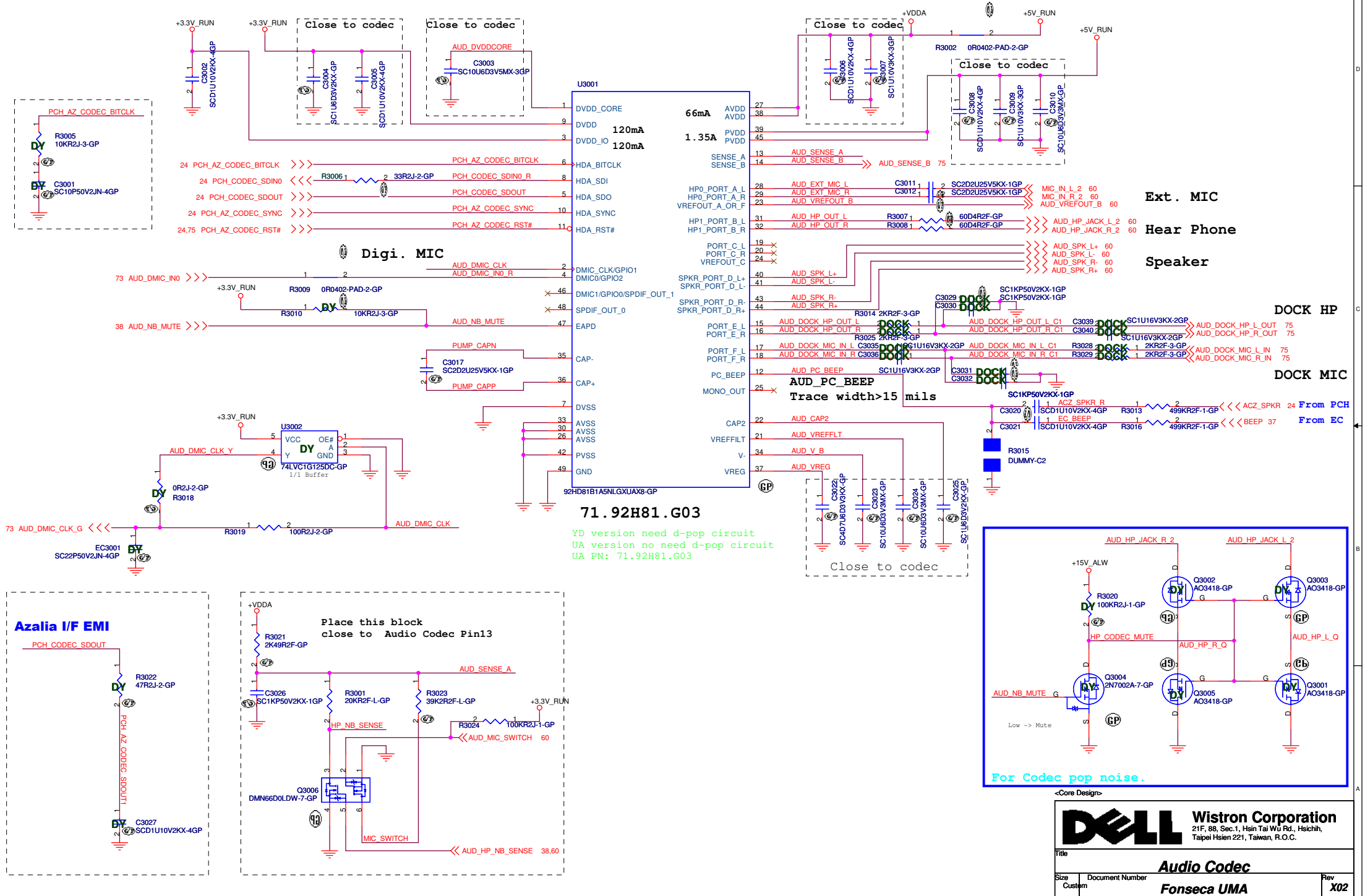
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserve

Size: Custom | Document Number: *Fonseca UMA* | Rev: *X02*

Date: Wednesday, March 10, 2010 | Sheet 29 of 82

SSID = AUDIO



<core_design>
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec

Size: Custom | Document Number: Fonseca UMA | Rev: X02

Date: Wednesday, March 17, 2010 | Sheet 30 of 82
</core_design>

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

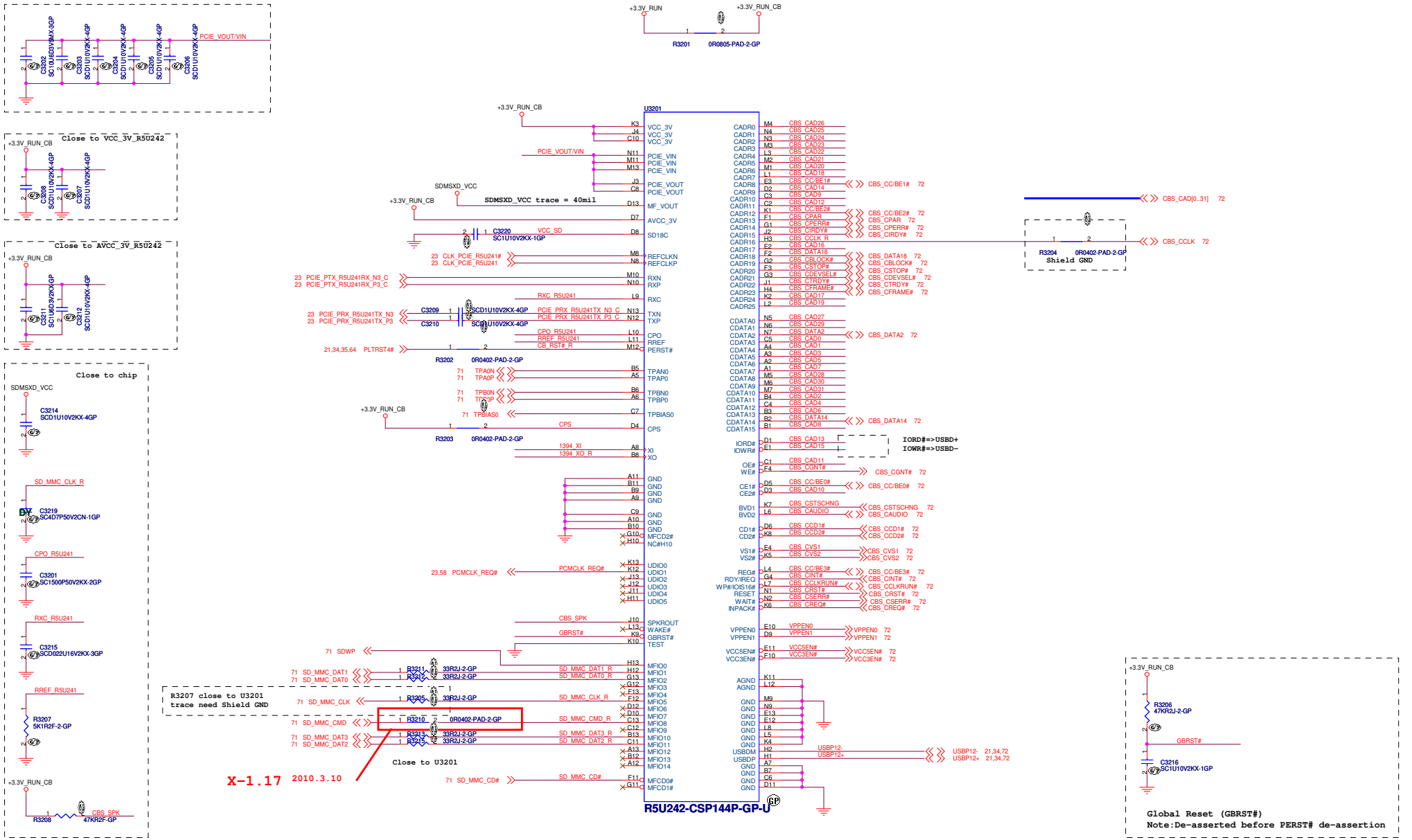
Title

Reserve

Size	Document Number	Rev
Custom	***Fonseca UMA***	***X02***

Date:	Wednesday, March 10, 2010	Sheet	31	of	82

SSID = 1394



<core_design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash Reader / 1394 / PCMCIA

Size: C | Document Number: Fonseca UMA | Rev: X02

Date: Wednesday, March 17, 2010 | Sheet 32 of 82

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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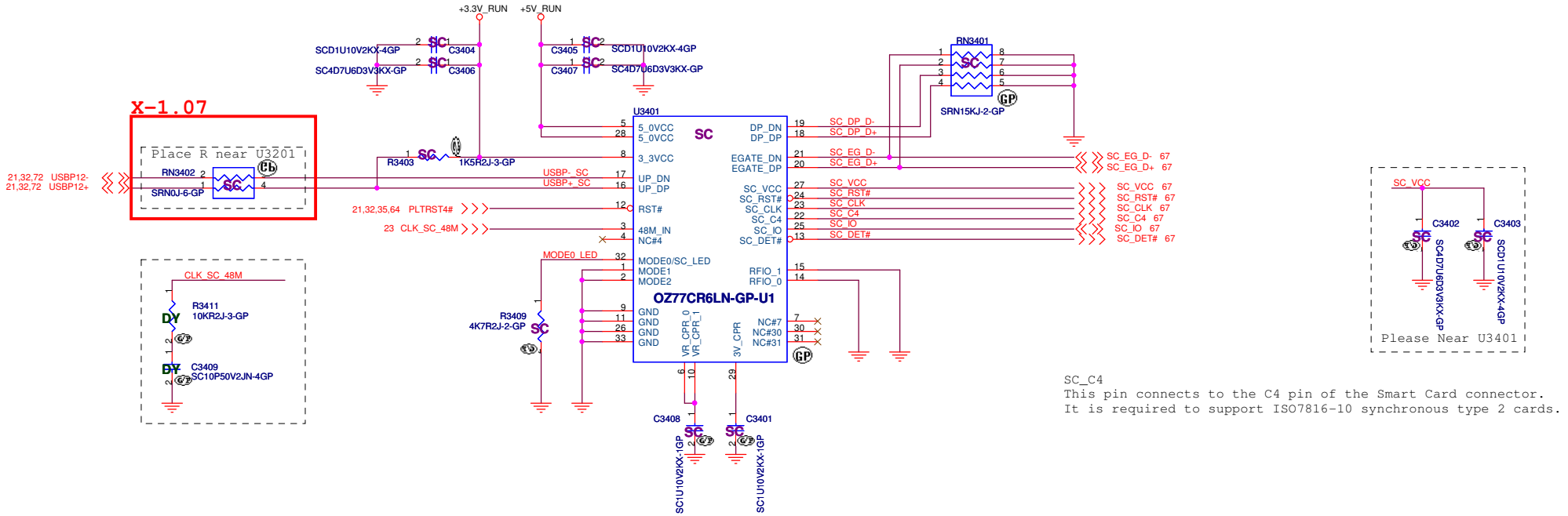
Title: *Reserve*

Size: Custom | Document Number: *Fonseca UMA* | Rev: *X02*

Date: Wednesday, March 10, 2010 | Sheet 33 of 82

SSID = SmartCard

SmartCard Chip



SC_C4
This pin connects to the C4 pin of the Smart Card connector.
It is required to support ISO7816-10 synchronous type 2 cards.

MODE0 / SC_LED	This terminal is an output indicating Smart Card activity; capable to drive an external LED device. The SC_LED terminal drives a low logic level during Smart Card data read/write activity, and is capable to source 12mA of IOL current to drive an external LED circuit. When RST# is asserted, this terminal is sampled to select the downstream port configuration for DP_DP and DP_DN (Internal Port 1). When sampled low (4.7k), the downstream port device is removable. When sampled high, the downstream port is a non-removable device. Includes internal input pull-up resistor.
MODE1	Test Pin. This terminal shall be externally connected to GND.
MODE2	Test Pin. This terminal shall be externally connected to GND.

RFIO_0 **RFIO_1**	Contactless Smart Card Interface Signal 0 and 1. This signal provides detection and data communication with an external RF device. If contactless is disabled, then this terminal shall be pulled-down to GND through a pull-down resistor, or directly connected to GND.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Smart Card (OZ77CR6LN)*

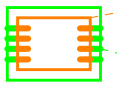
Size: Custom | Document Number: *Fonseca UMA* | Rev: *X02*

Date: Wednesday, March 17, 2010 | Sheet 34 of 82

SSID = LOM

Symbol : 71.05761.00U
Product : P802H (Rev:B0)

Co-Layout



Core Power Decoupling

VDDIOPower Decoupling

Put 0.1u cap close to Chip

Populate resister for debug

Close to the power pins and
0.1u cap should be closer to Chip

Design current: 89.6mA
Max current: 128mA

Design Current: 627mA

Place crystal less
than 0.75" (~1.9cm)
from LAN Controller

Logic High Voltage must
be 0.7V to 2.75V

DOCKED
SEL 0:RJ45.
SEL 1:Dock.

8Mb for 5761E:
Main source: 72.45081.C01(Big PAD)
2nd source: 72.45081.B01(Small PAD)

CTPM and DisableBTPM

Reserve for EMI

X01.09/0819

Wistron Corporation
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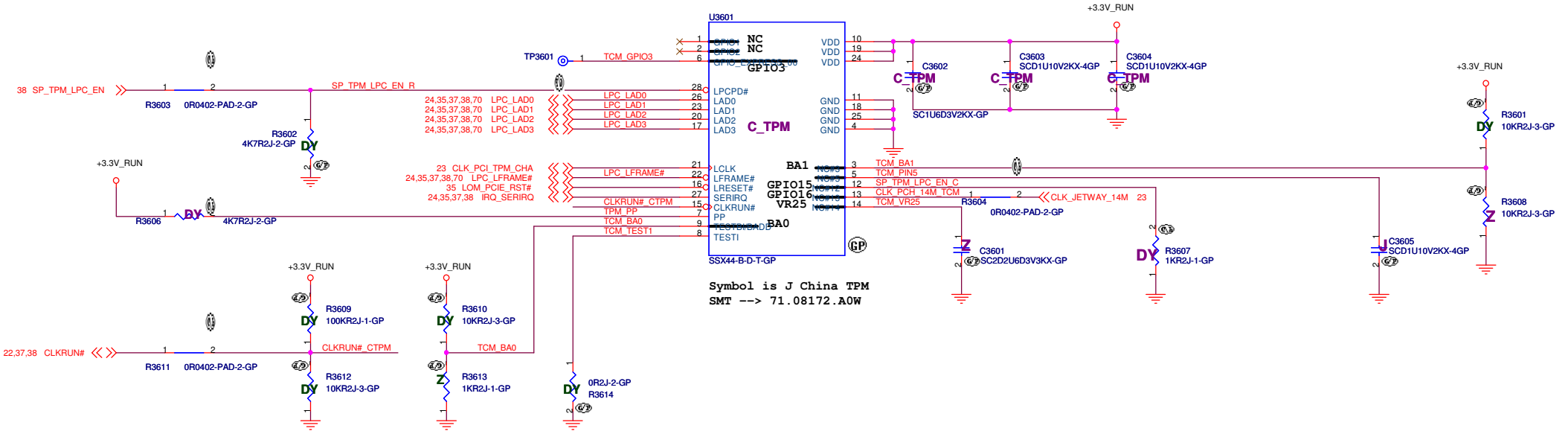
Taipei Hsien 221, Taiwan, R.O.C.

Title: GLAN - BCM5761E
Size: Custom | Document Number: Fonseca UMA | Rev: X02
Date: Thursday, March 18, 2010 | Sheet 35 of 82

SSID = TCM

Symbol : Jetway, but linked to ZTE
Product : 71.08172.00W (ZTE)

China TPM Chip



Symbol is J China TPM
SMT --> 71.08172.A0W

Z

Base Address	BA1 PIN3	BA0 PIN9
EE/EF	0	0
7E/7F	0	1
2E/2F	1	0
4E/4F	1	1

Default EE/EF as Amy recommended

J

	1(default)	0
PIN12	FLASH	SRAM

J has internal PU with PIN12.

<Core Design>

Wistron Corporation
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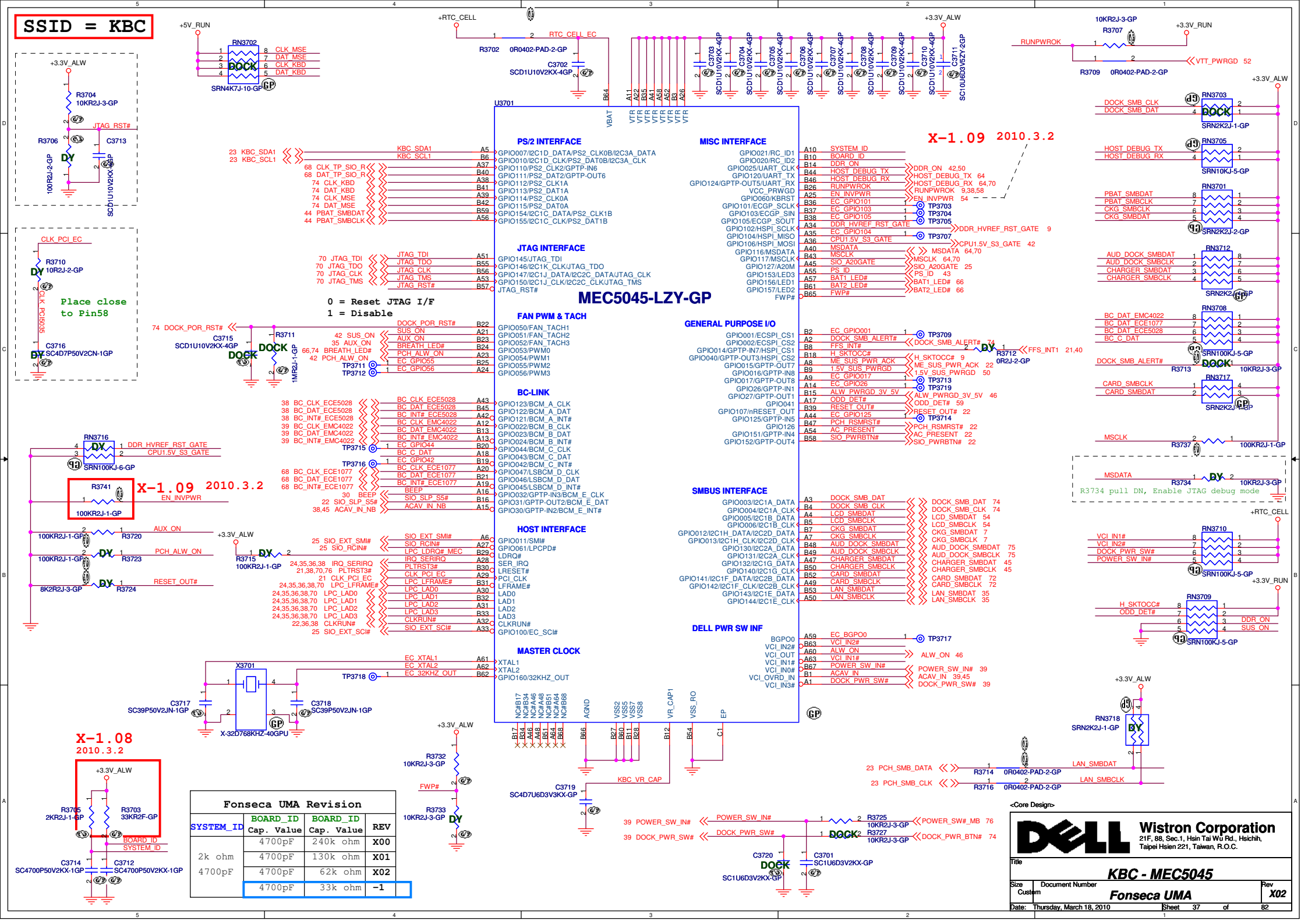
Taipei Hsien 221, Taiwan, R.O.C.

Title: TCM
Size: Custom | Document Number: Fonseca UMA | Rev: X02
Date: Thursday, March 18, 2010 | Sheet 36 of 82

SSID = KBC


U3701
MEC5045-LZY-GP
PS/2 INTERFACE
JTAG INTERFACE
FAN PWM & TACH
BC-LINK
HOST INTERFACE
MASTER CLOCK
MISC INTERFACE
GENERAL PURPOSE I/O
SMBUS INTERFACE
DELL PWR SW INF
X-1.09 2010.3.2
0 = Reset JTAG I/F
1 = Disable
Place close to Pin58
X-1.08 2010.3.2
X-1.09 2010.3.2
R3734 pull DN, Enable JTAG debug mode
Fonseca UMA Revision
SYSTEM_ID | BOARD_ID Cap. Value | BOARD_ID Cap. Value | REV
2k ohm / 4700pF | 4700pF | 240k ohm | X00
2k ohm / 4700pF | 4700pF | 130k ohm | X01
2k ohm / 4700pF | 4700pF | 62k ohm | X02
2k ohm / 4700pF | 4700pF | 33k ohm | -1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC - MEC5045
Size Custom
Document Number
Fonseca UMA
Rev X02
Date: Thursday, March 18, 2010
Sheet 37 of 82

SSID = KBC

U3801

ECE5028-LZY-GP

CRD_DET1	CRD_DET0	Function
Low	Low	No Option Installed
Low	High	Smartcard
High	Low	Cardbus
High	High	Express Card

<Core Design>

Wistron Corporation
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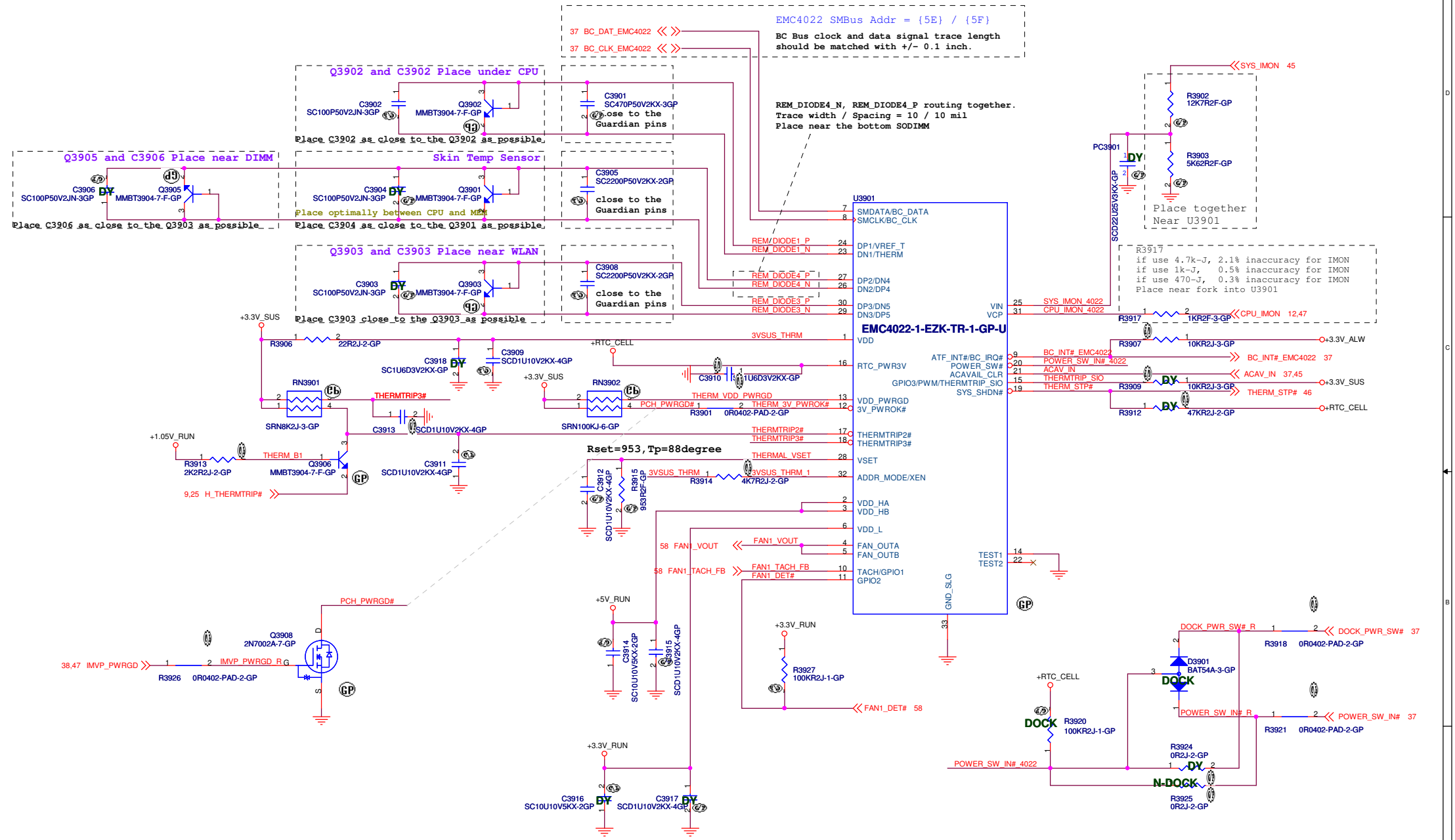
Taipei Hsien 221, Taiwan, R.O.C.

Title: SIO - MEC5028

Size: Custom | Document Number: Fonseca UMA | Rev: X02

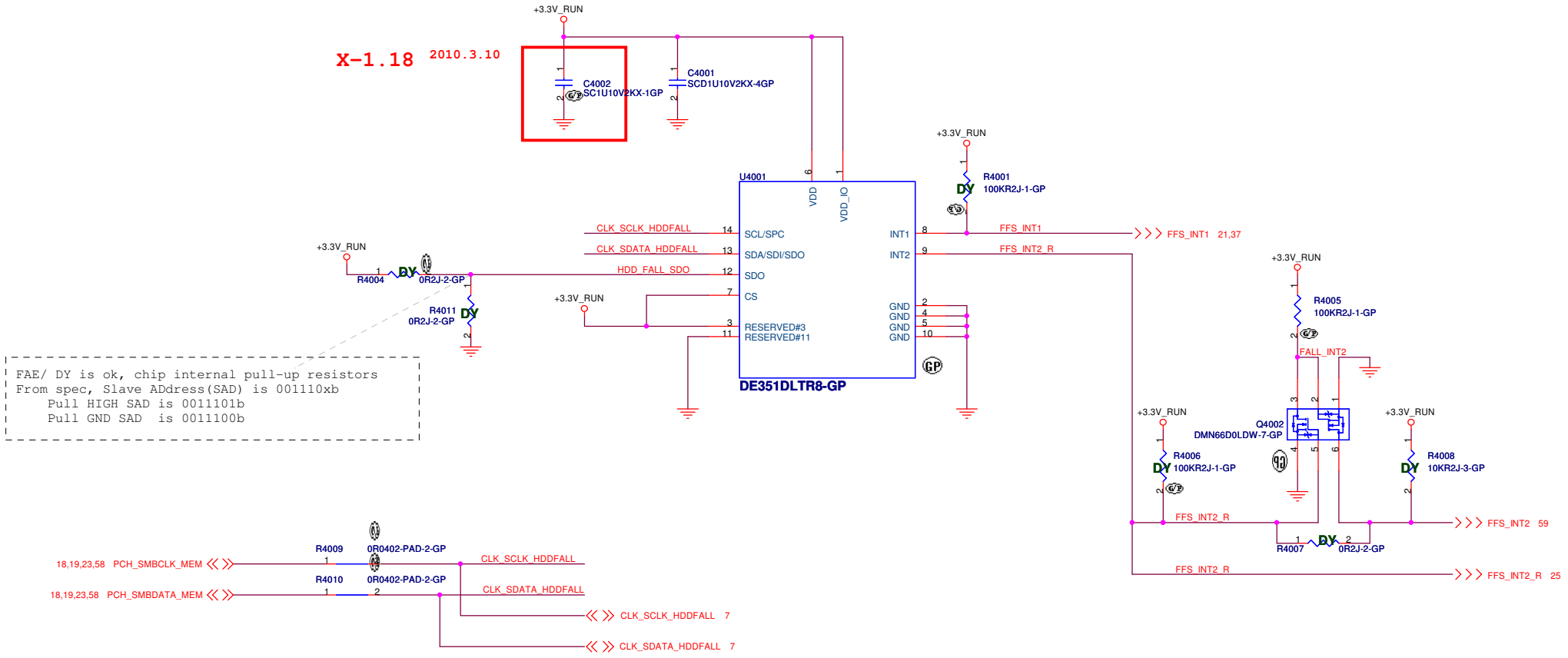
Date: Thursday, March 18, 2010 | Sheet 38 of 82

SSID = Thermal



SSID = User.Interface

Free Fall Sensor



Layout Note
- no via, trace, under the sensor
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor

Size: A3 | Document Number: Fonseca UMA | Rev: X02

Date: Wednesday, March 17, 2010 | Sheet 40 of 82

SSID = Reset.Suspend

<Core Design>

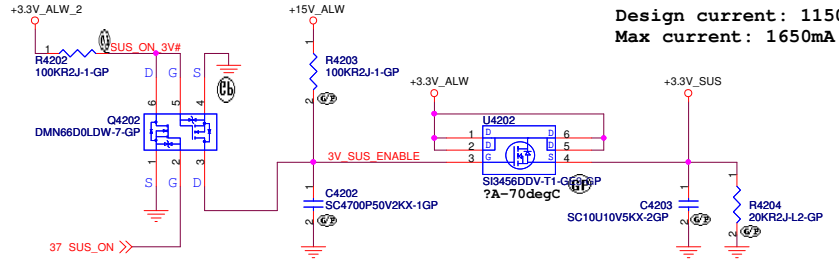
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power On Logic

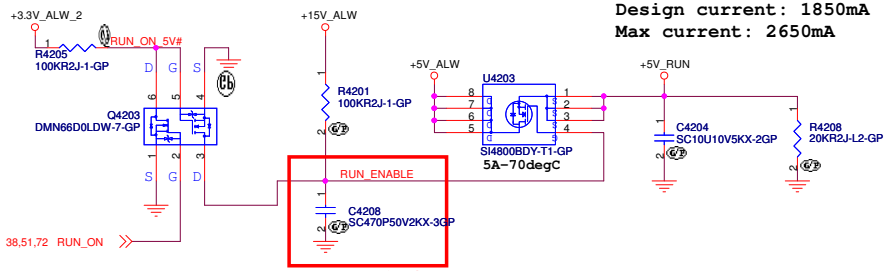
Size: A3 | Document Number: Fonseca UMA | Rev: X02

Date: Wednesday, March 10, 2010 | Sheet 41 of 82

SSID = Reset.Suspend

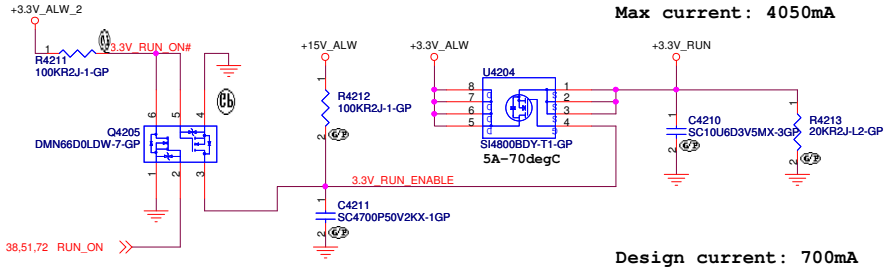


Design current: 1150mA
Max current: 1650mA

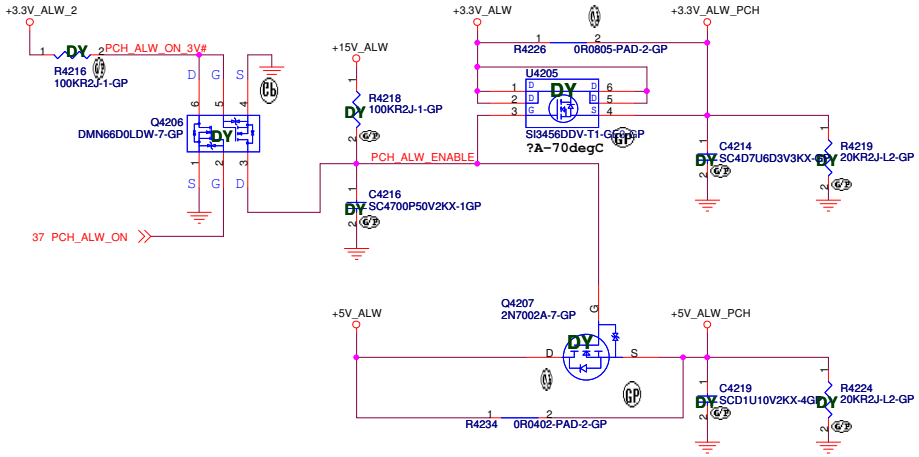


Design current: 1850mA
Max current: 2650mA

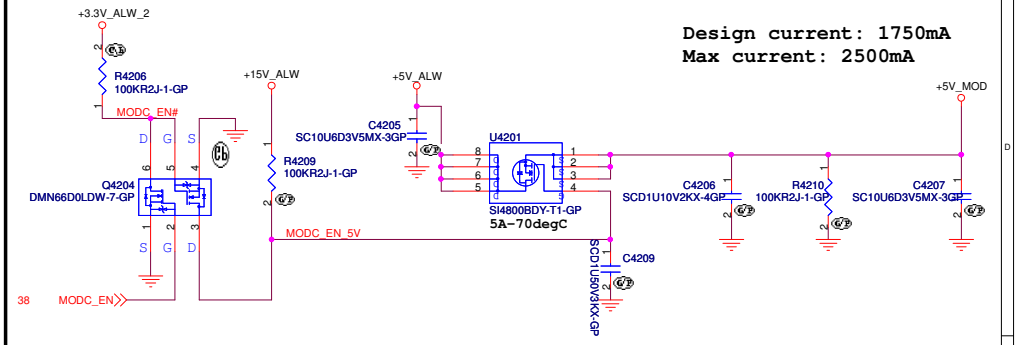
X-1.05
2010.3.2



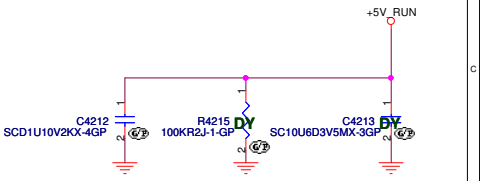
Design current: 2850mA
Max current: 4050mA



Design current: 700mA
Max current: 700mA

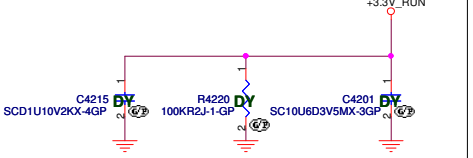


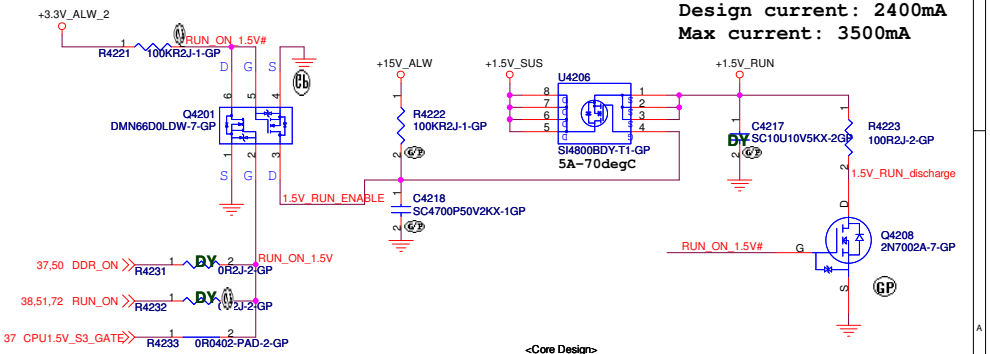
Design current: 1750mA
Max current: 2500mA



Design current: 700mA
Max current: 1000mA

place to HDD connector side





Design current: 2400mA
Max current: 3500mA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
Custom	Fonseca UMA	X02

Date: Wednesday, March 17, 2010 Sheet 42 of 82

SSID = PWR.Support

Adapter In

DC_IN CONN	
PIN 3,4	DC_IN+
PIN 4,5	DC_IN-
PIN 1	ID
PIN 6,7,8,9	GND

PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL	BQ24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMP	FBO
7	DAC	NC	CE
8	IINP	ICM	VICM
11	VDD	VDDSMB	VDDSMB
14	BATSEL	NC	NC
15	FBSA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSON	CSON
18	CSIP	CSOP	CSOP
20	DLO	LGATE	LGATE
21	LDO	VDDP	VDDP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGSTE
25	BST	BOOT	BOOT
26	VCC	VCC	ICOUT

"NC" means no-connect

TABLE
MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL	TI
R411	8.45K 1%	DUMMY	DUMMY
C98	0.01uF	0.1uF	0.1uF
C459	0.1uF 10V	DUMMY	200P 10V
C5	1uF 10V	DUMMY	1uF 10V
R16	365K 1%	215K 1%	309K 1%
R434	0 5%	10 5%	0 5%
R414	0 5%	10 5%	0 5%
C473	DUMMY	0.22uF	0.1uF
C457	DUMMY	0.22uF	0.1uF
C442	0.01uF	DUMMY	DUMMY
C453	0.1uF 10V	DUMMY	DUMMY
C36	220pF 50V	DUMMY	DUMMY
D23	RB751V-40	DUMMY	RB751V-40
C58	3.3nF	DUMMY	DUMMY
R64	1 1%	0 5%	0 5%
R394	100 5%	0 5%	0 5%
R110	0 5%	8.45K 1%	8.45K 1%
R401	10K 5%	2.2K 5%	4.7K 5%
C441	0.01uF	0.01uF	DUMMY
C449	0.01uF	0.01uF	DUMMY
R397	1K 5%	DUMMY	DUMMY
Q41	ISS355	DUMMY	DUMMY
C16	1uF 10V	1uF 10V	DUMMY
R30	33 1%	33 1%	DUMMY
R408	DUMMY	DUMMY	0 5%
R400	DUMMY	DUMMY	200K 5%
R403	DUMMY	DUMMY	7.5K 5%
C450	DUMMY	DUMMY	51P 10V
C444	DUMMY	DUMMY	2000P 10V
C448	DUMMY	DUMMY	130P 10V
C446	DUMMY	DUMMY	0.1uF
C483	DUMMY	DUMMY	0.1uF
R438	10K 1%	10K 1%	DUMMY
R412	DUMMY	DUMMY	10k 5%
R440	15.8K 1%	15.8K 1%	DUMMY
R407	DUMMY	10K 5%	DUMMY
R9	0 5%	10 5%	0 5%
C482	DUMMY	DUMMY	DUMMY
C12	DUMMY	DUMMY	DUMMY
R435	0 5%	10 5%	0 5%

MAX 8731A/ISL88731

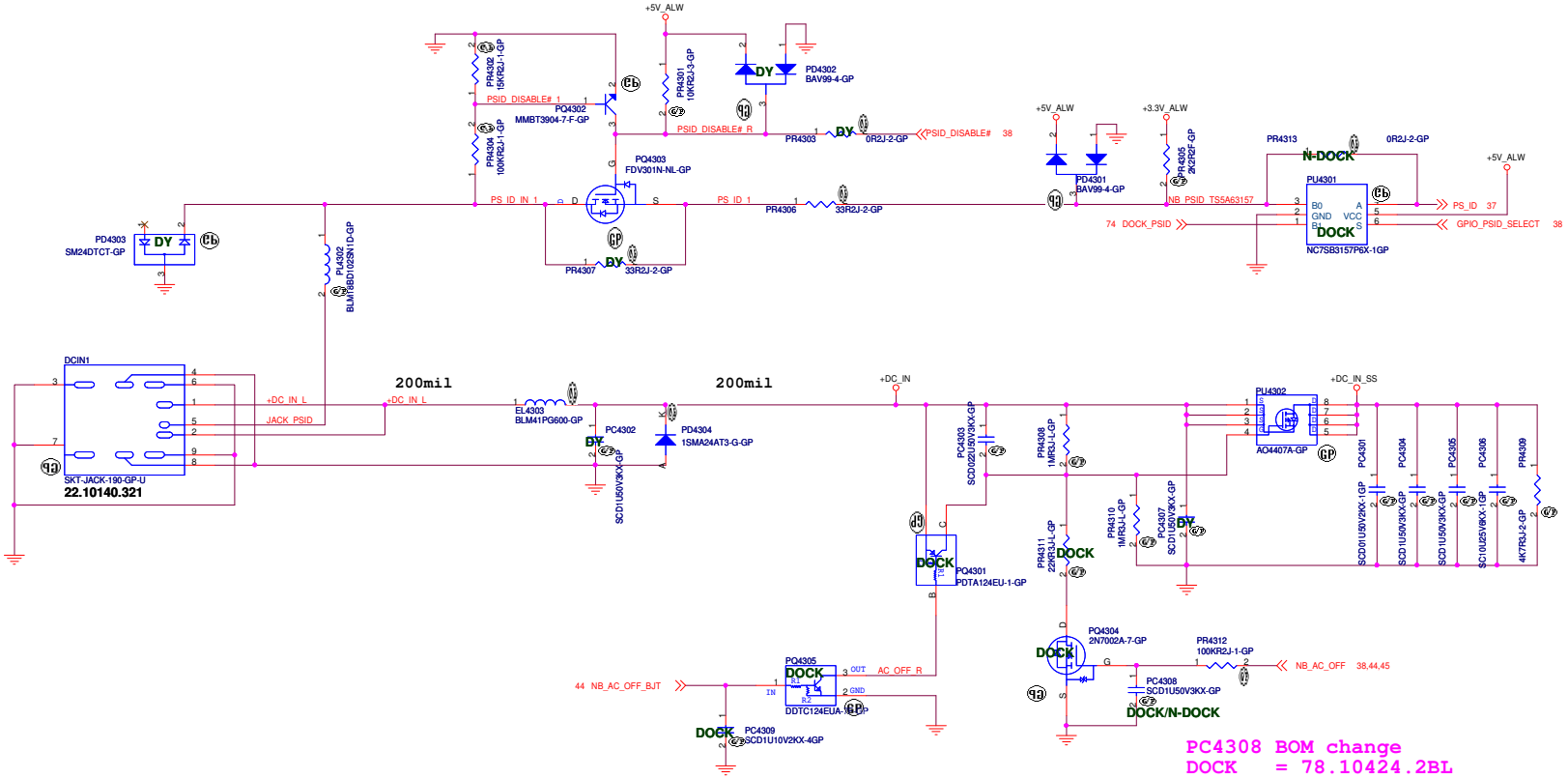
Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	13.0K	105	24.9K
90	4.43	51.1K	17.8K	348	33.2K

*R504 is populated if ADAPT_TRIP_SEL is used
to program for the next lower adapter.

BQ247451

Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	12.4K	205	24.3K
90	4.43	51.1K	16.9K	499	32.4K

*R504 is populated if ADAPT_TRIP_SEL is used
to program for the next lower adapter.



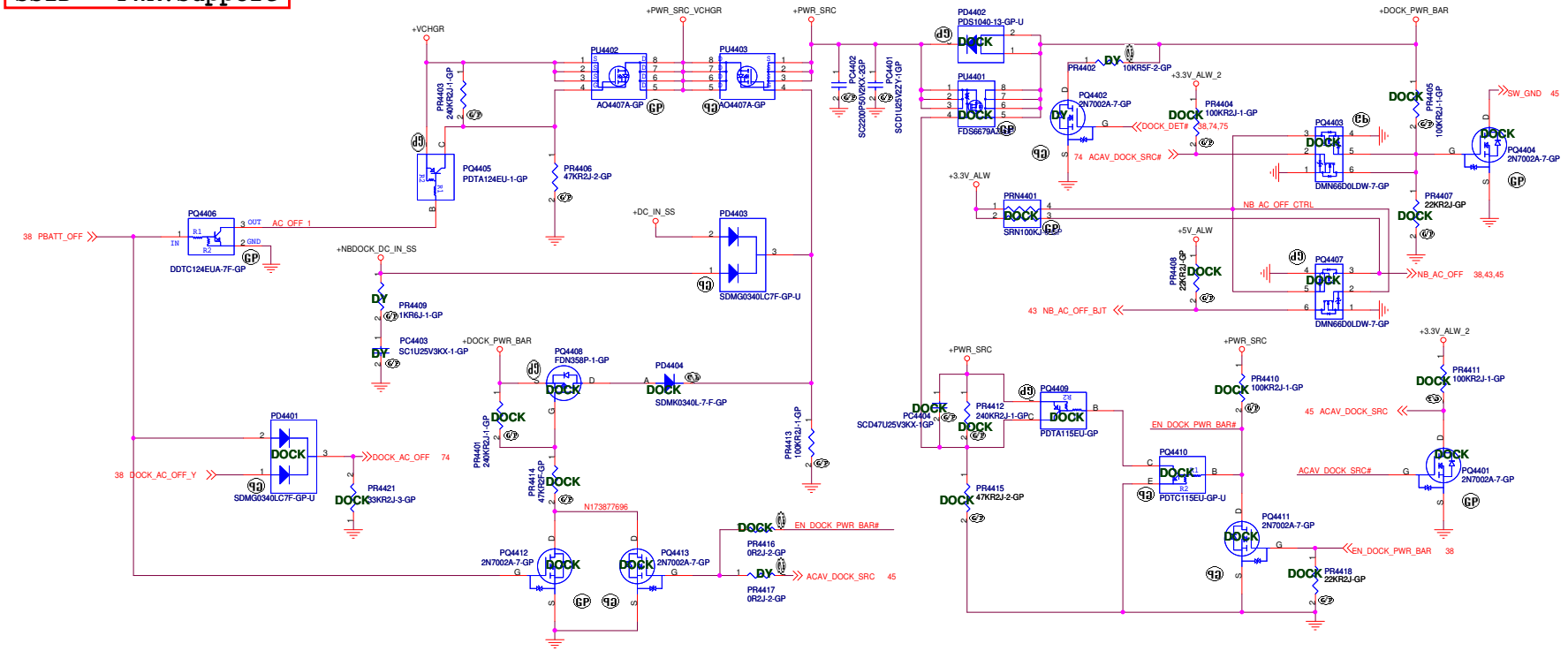
PC4308 BOM change
DOCK = 78.10424.2BL
N-DOCK = 63.00000.00L

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

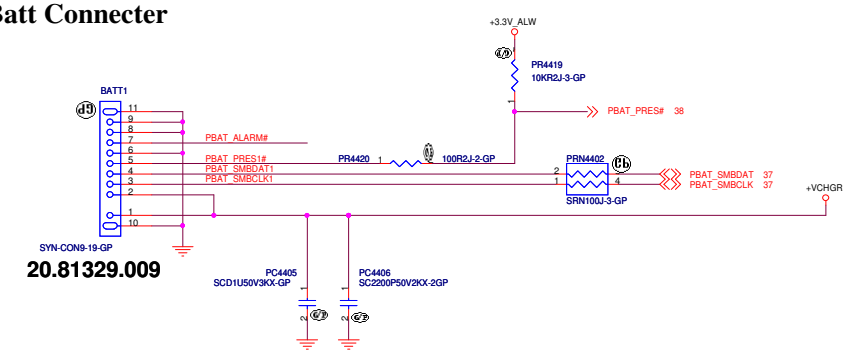
Title: DC IN Jack
Size: C
Document Number: Fonseca UMA
Rev: X02
Date: Wednesday, March 17, 2010
Sheet 43 of 82

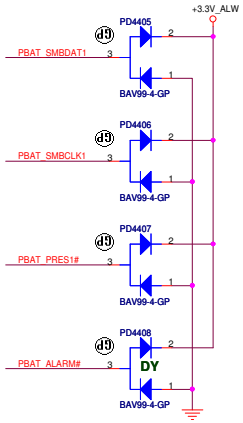
SSID = PWR.Support



SSID = RBATT

Batt Connecter





<Core Design>

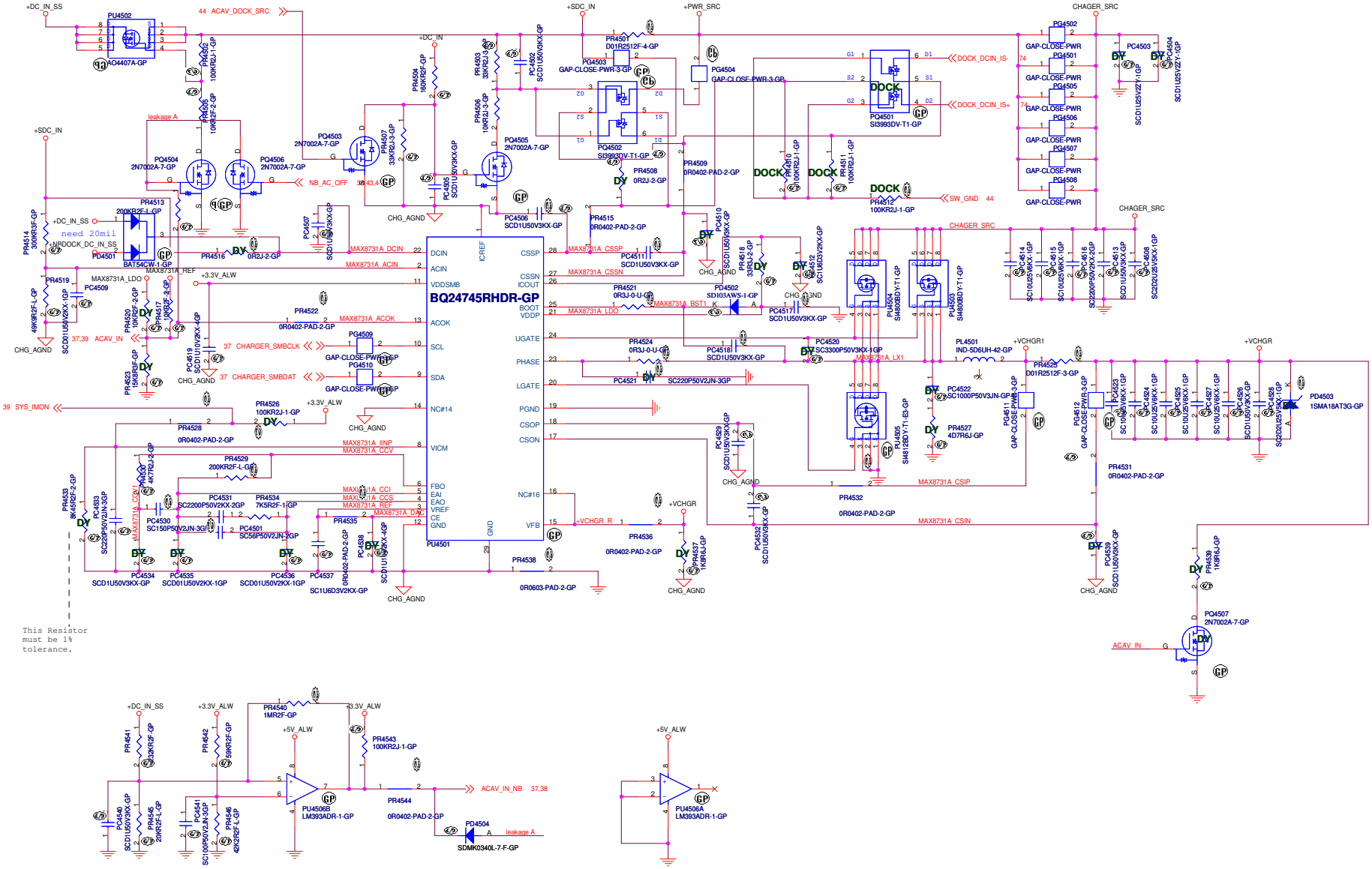
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DOCK DCIN/BATT Connector

Size	Document Number	Rev
C	Fonseca UMA	X02

Date: Thursday, March 18, 2010 Sheet 44 of 82

SSID = Charger



<Core Design>

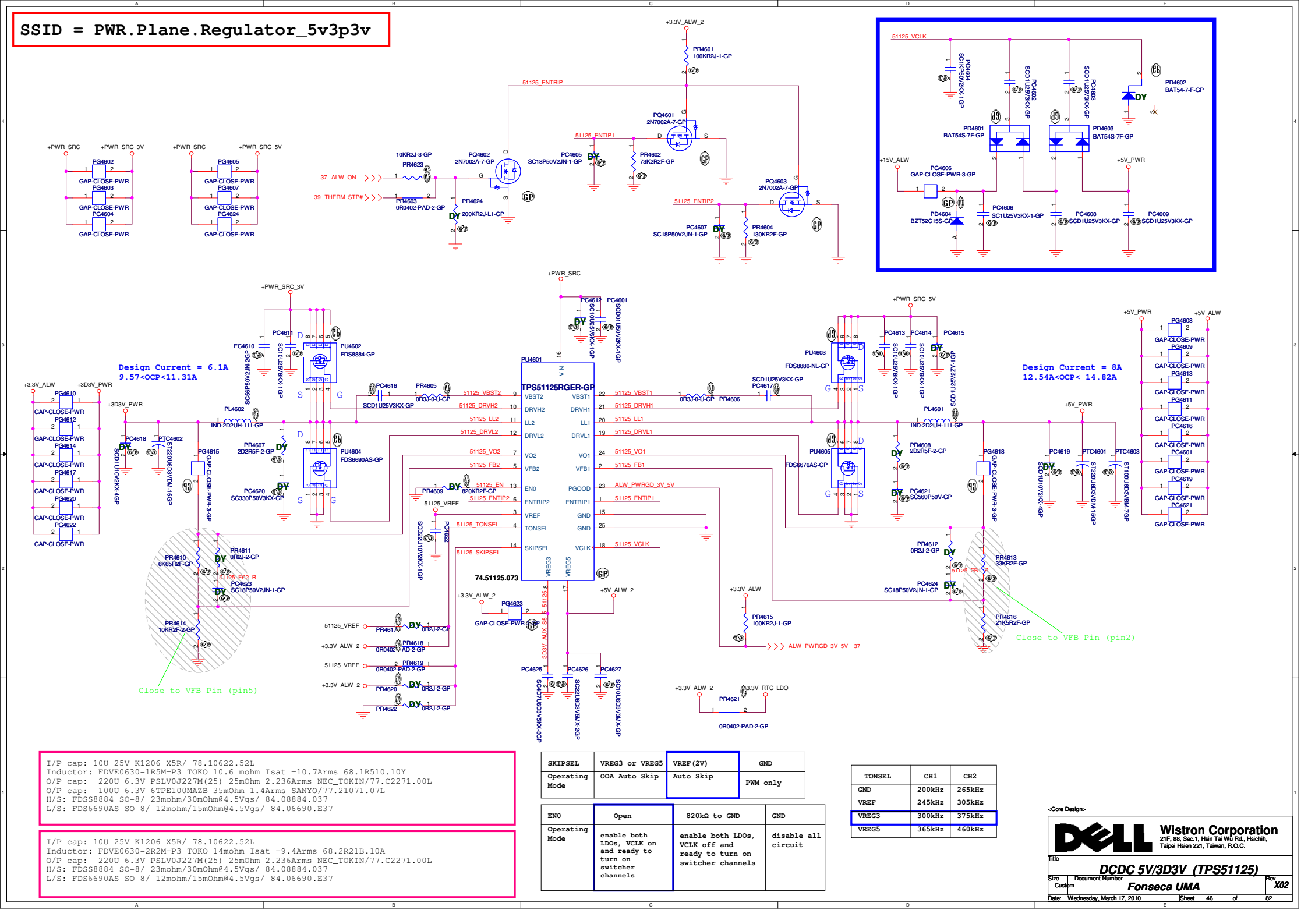
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Battery Charger**

Size	Document Number	Rev
C	Fonseca UMA	X02

Date: Thursday, March 18, 2010 Sheet 45 of 82

SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: FDVE0630-1R5M=P3 TOKO 10.6 mohm Isat =10.7Arms 68.1R510.10Y
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V 6TPE100MAZB 35mOhm 1.4Arms SANYO/77.21071.07L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: FDVE0630-2R2M=P3 TOKO 14mohm Isat =9.4Arms 68.2R21B.10A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

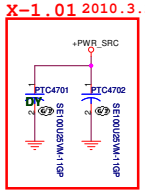
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 5V/3D3V (TPS51125)
Size: Custom | Document Number: Fonseca UMA | Rev: X02
Date: Wednesday, March 17, 2010 | Sheet 46 of 82

SSID = CPU.Regulator

X-1.01 2010.3.2



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE

Size: A2 | Document Number: Fonseca UMA | Rev: X02

Date: Wednesday, March 17, 2010 | Sheet 47 of 82

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: A3 | Document Number: *Fonseca UMA* | Rev: *X02*

Date: Wednesday, March 10, 2010 | Sheet 48 of 82

SSID = PWR.Plane.Regulator_1p05v

(Blank)

<Core Design>

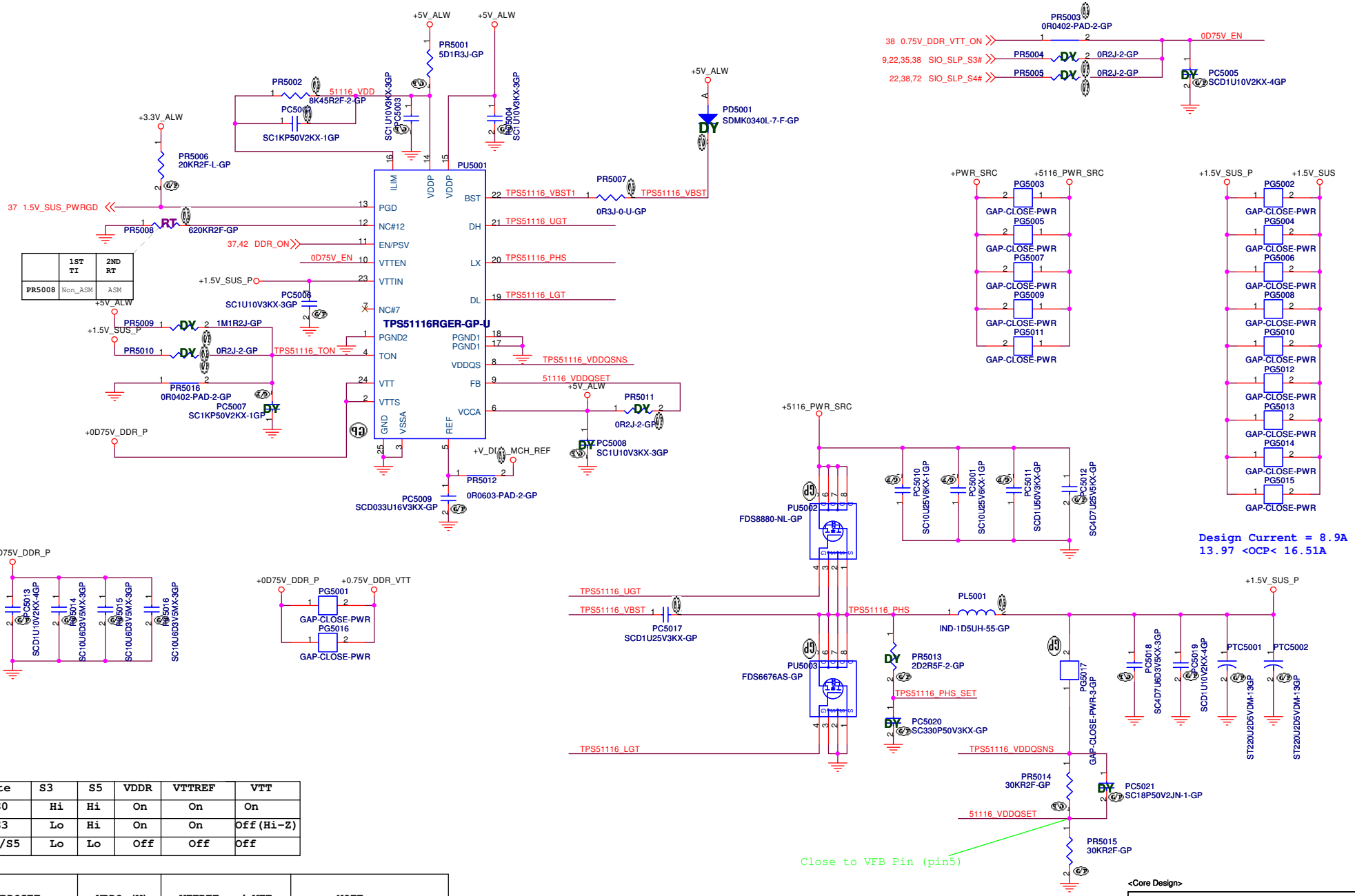
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.05V

Size: A3 | Document Number: Fonseca UMA | Rev: X02

Date: Wednesday, March 10, 2010 | Sheet 49 of 82

SSID = PWR.Plane.Regulator_1p5v0p75v



	1ST TI	2ND RT
PR5008	Non_ASM	ASM

Design Current = 8.9A
13.97 <OCP< 16.51A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: FDV1040-1R5M=P3 TOKO DCR:3.86 mohm Isat =19.7Arms 68.1R510.10Q
O/P cap: TLPSLV0G227M(25)12RE 25mOhm 2.5Arms NEC_TOKIN/ 77.C2271.07L
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->400KHz

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

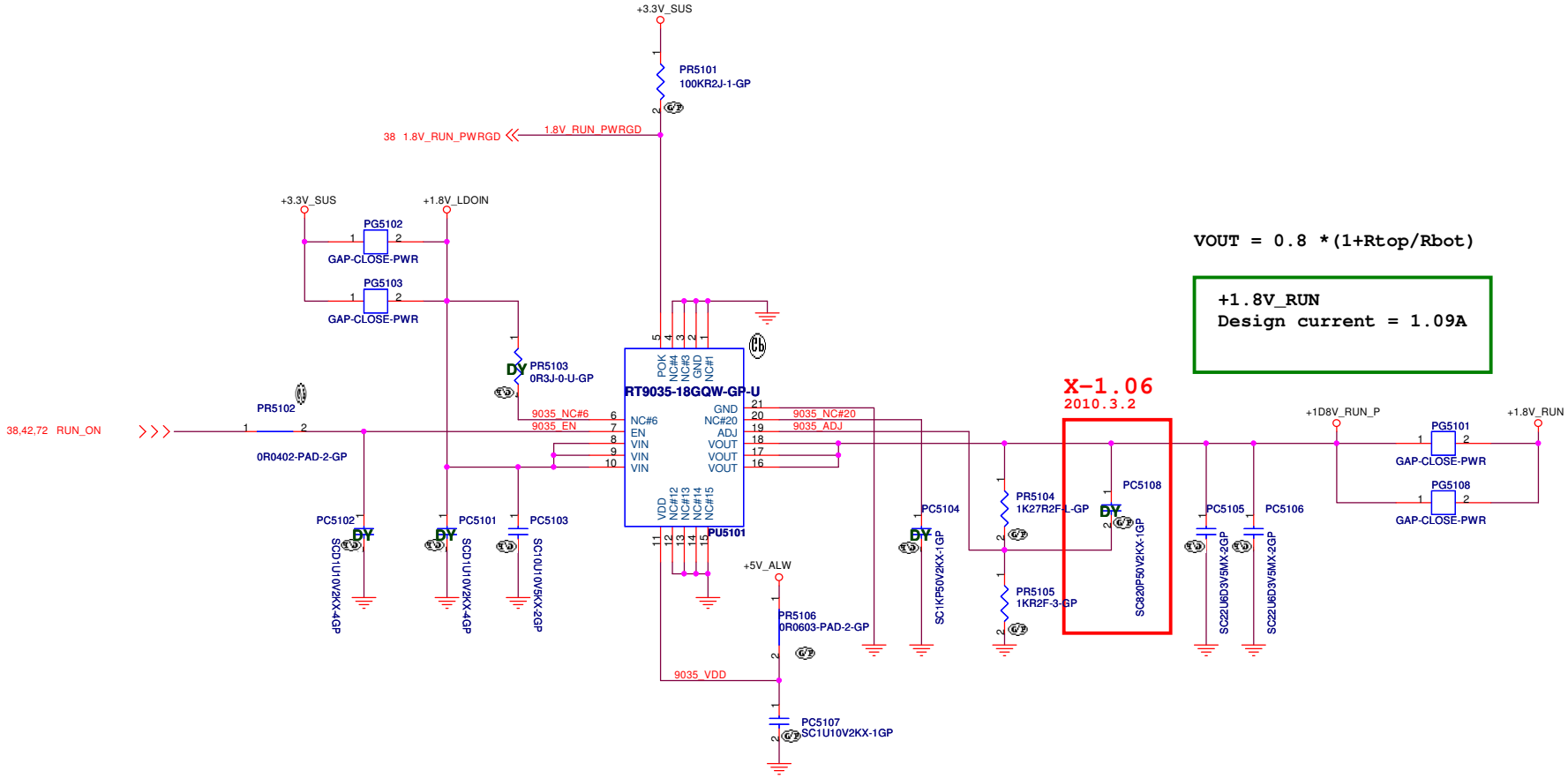
Title: DC to DC 1.5V / 0.75V

Size: Custom | Document Number: Fonseca UMA | Rev: X02

Date: Wednesday, March 17, 2010 | Sheet 50 of 82

SSID = PWR.Plane.Regulator_1p8v

LDO for +1.8V_RUN



<Core Design>

Wistron Corporation
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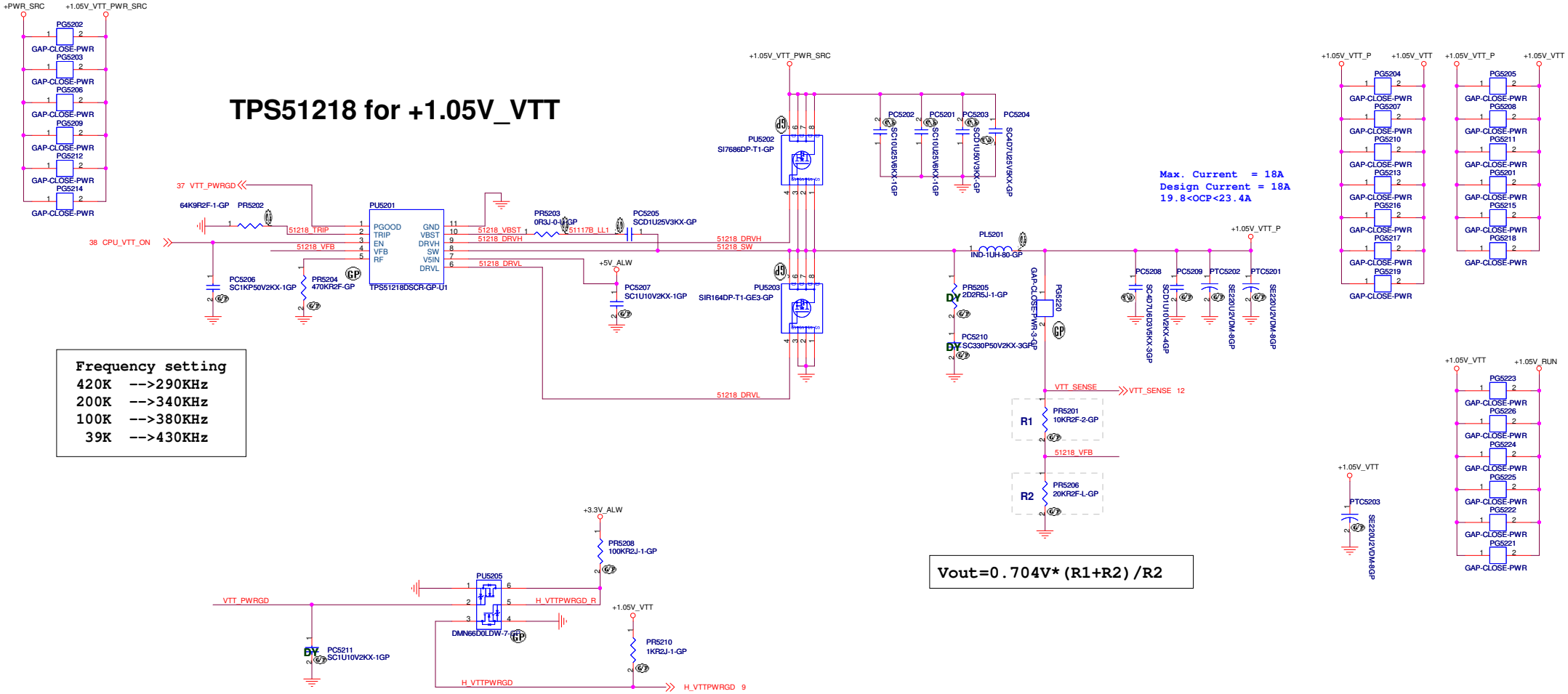
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC to DC +1.8V_RUN	
Size: A3	Document Number: Fonseca UMA	Rev: X02
Date: Wednesday, March 17, 2010	Sheet 51 of 82	

SSID = PWR.Plane.Regulator_1p05v

TPS51218 for +1.05V_VTT



Frequency setting	
420K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

<Core Design>

Wistron Corporation
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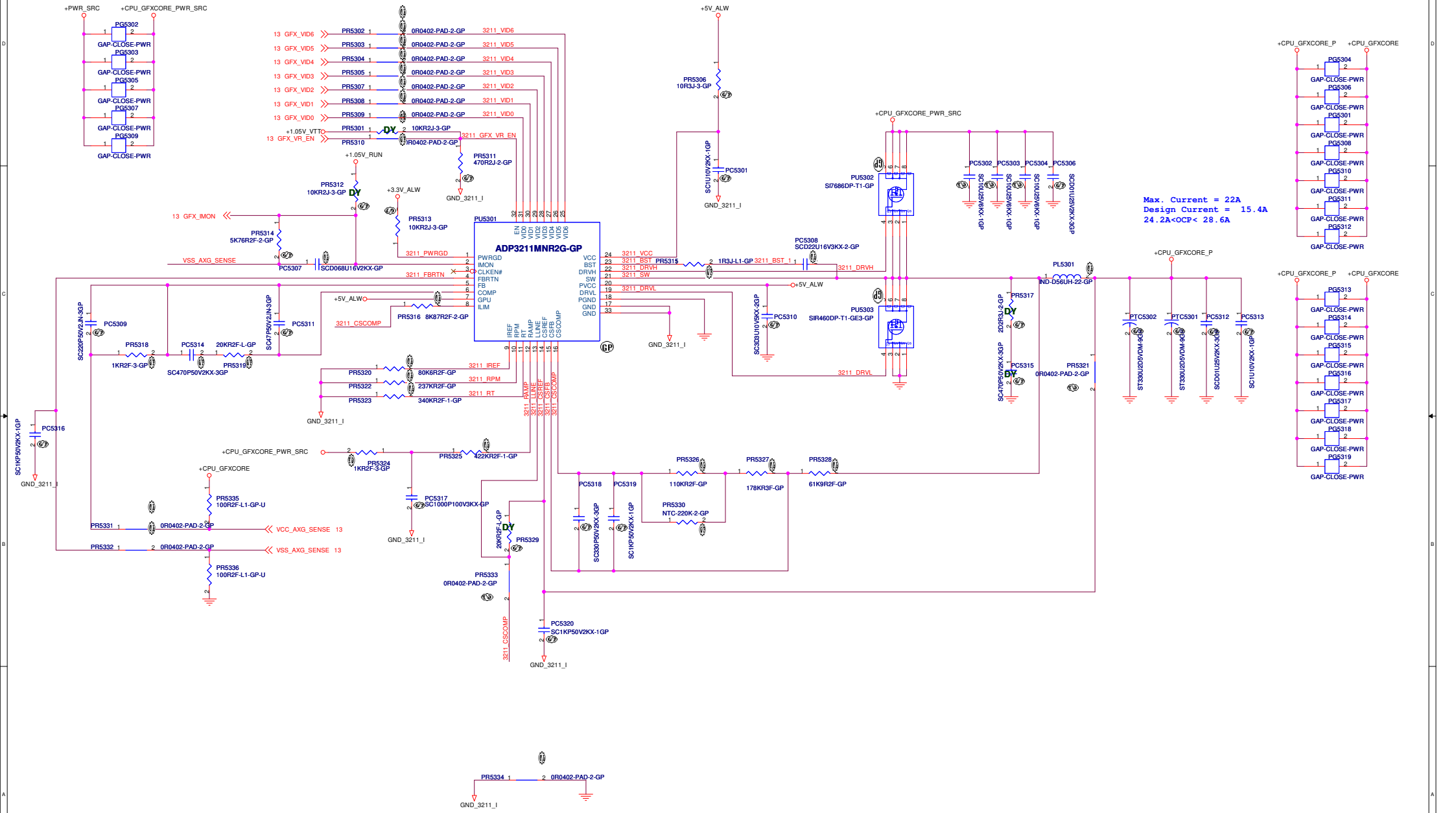
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC +1.05V_VTT

Size: Custom | Document Number: Fonseca UMA | Rev: X02

Date: Wednesday, March 17, 2010 | Sheet 52 of 82

SSID = CPU.GFX.Regulator



<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP3211 CPU_GFXCORE

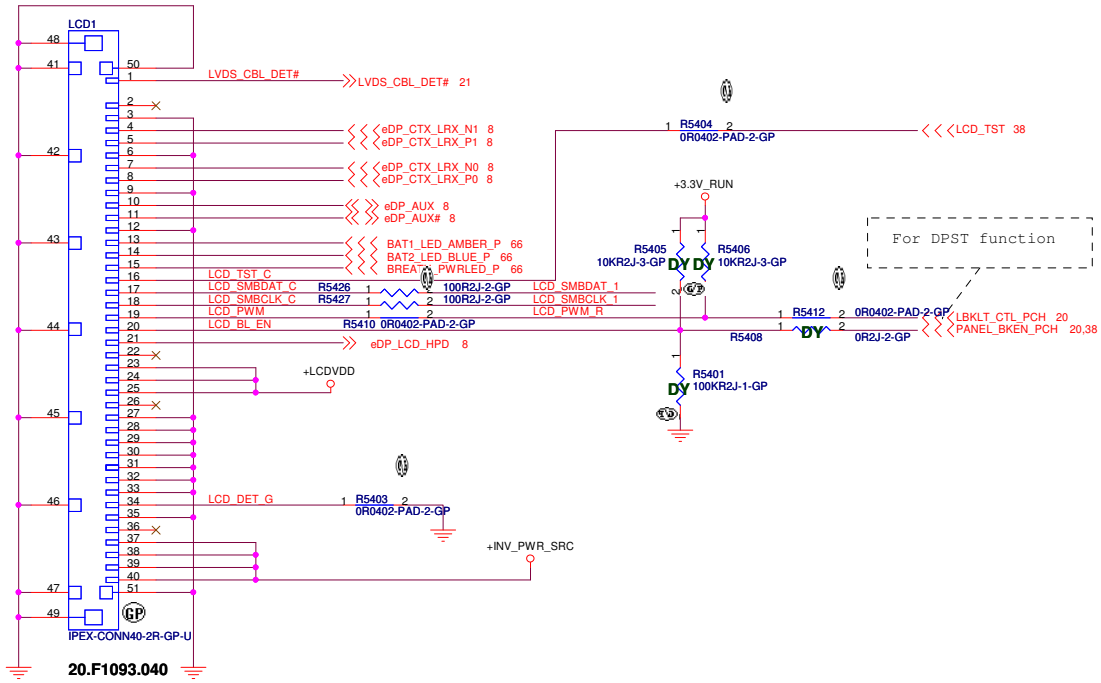
Size: Custom | Document Number: Fonseca UMA | Rev: X02

Date: Wednesday, March 17, 2010 | Sheet 53 of 82

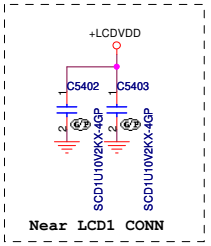
SSID = VIDEO

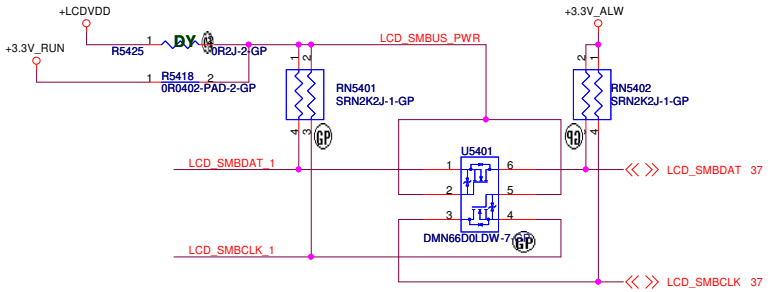
LED Location from left to right

HDD | BATTERY



20.F1093.040

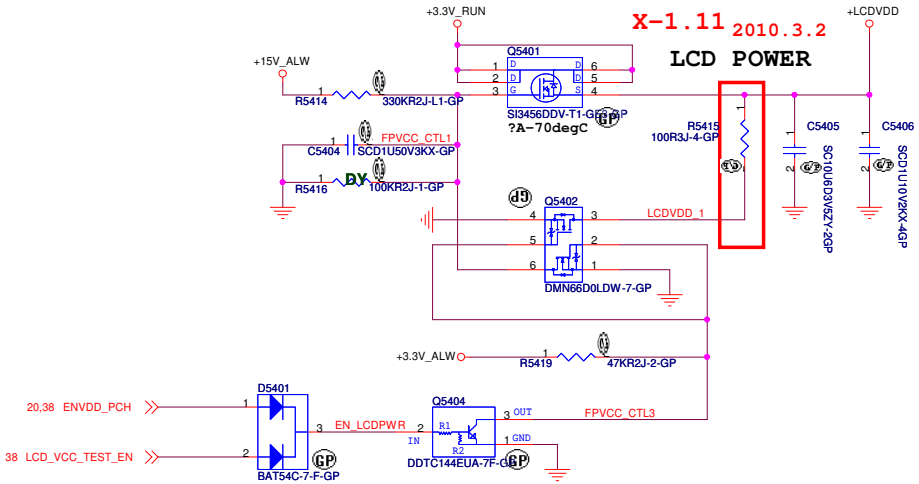




SSID = VIDEO

X-1.11 2010.3.2

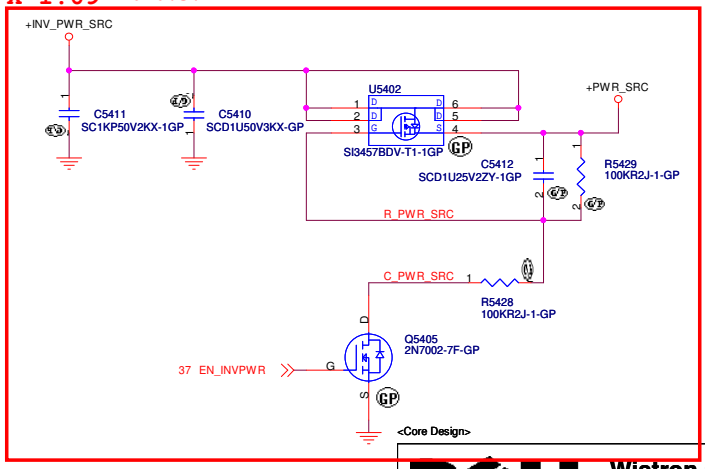
LCD POWER



SSID = Inverter

LED BACKLIGHT CONVERTER POWER

X-1.09 2010.3.2



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Title: LCD

Size: Custom | Document Number: Fonseca UMA | Rev: X02

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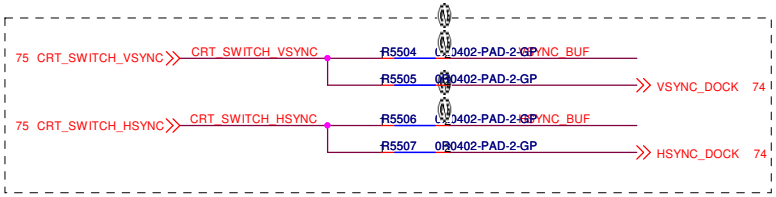
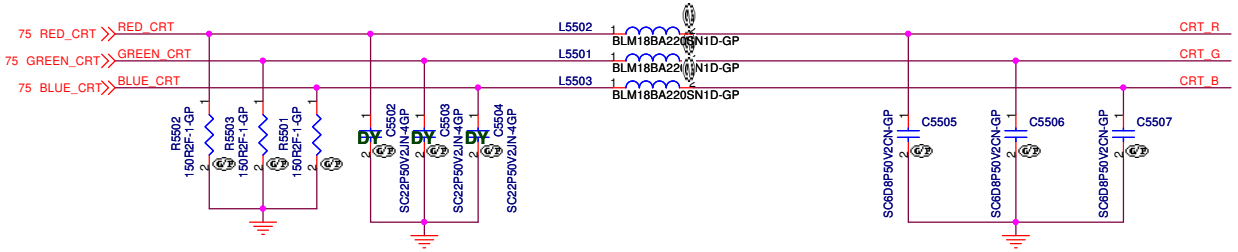
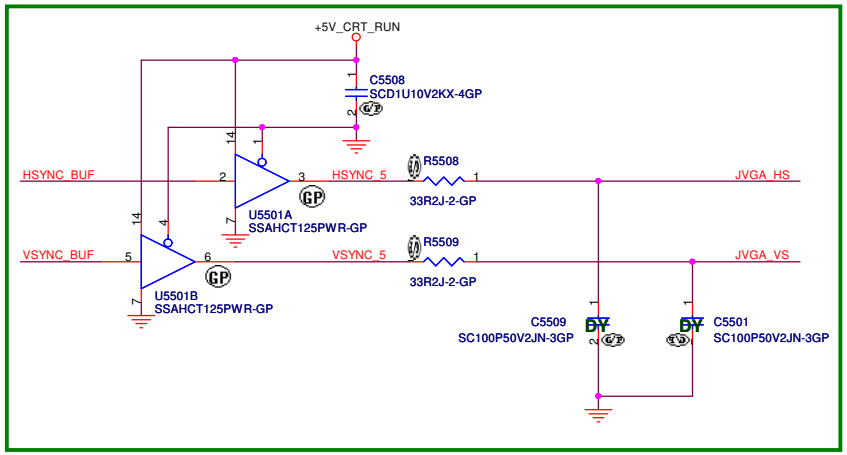
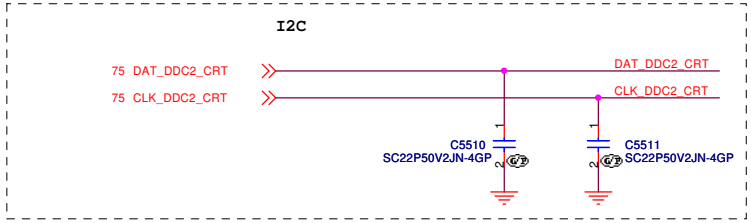
SSID = VIDEO



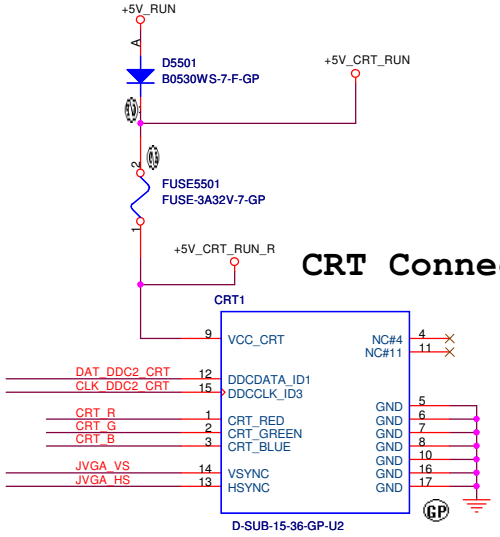




Layout Note:
*Pi-filter & 150 Ohm pull-down
resistors should be as close
as to CRT CONN.
* RGB signal will hit 75 Ohm
first, then pi-filter, finally
CRT CONN.



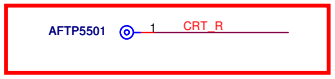
MAX4885E has internal ESD protection
and internal level shift



CRT Connector

20.20431.015

X-1.20 2010.3.10



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT		
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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: A3 | Document Number: *Fonseca UMA* | Rev: *X02*

Date: Wednesday, March 10, 2010 | Sheet 56 of 82

(Blank)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: A3 | Document Number: *Fonseca UMA* | Rev: *X02*

Date: Wednesday, March 10, 2010 | Sheet 57 of 82

SSID = CPU

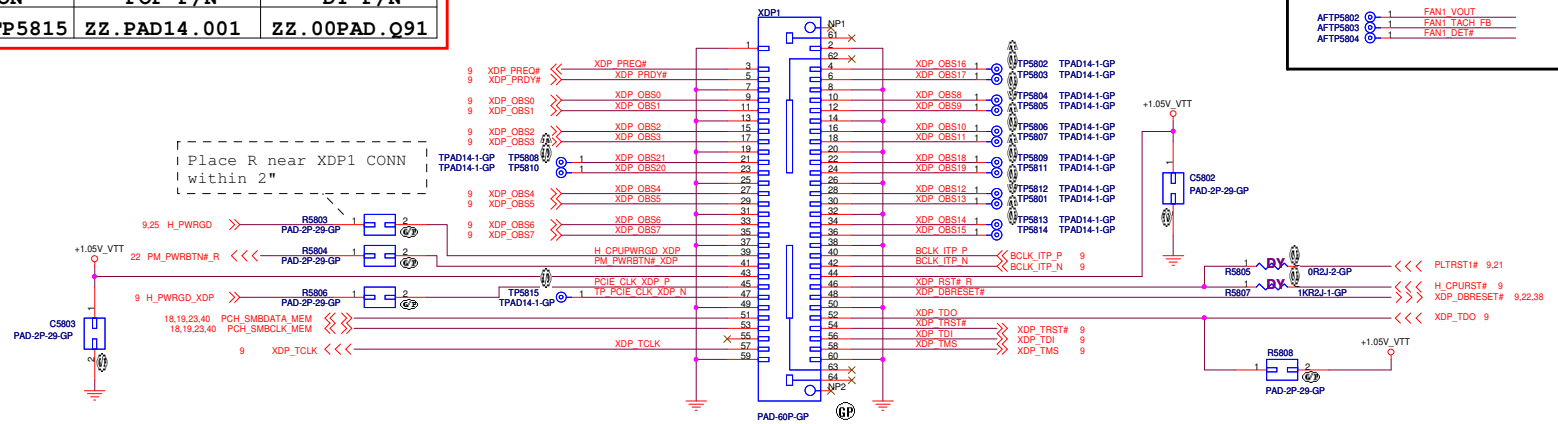
X-1.02 2010.3.2

LOCATION	POP P/N	DY P/N
XDP1,XDP2	20.F0971.060	ZZ.00PAD.Q81
C5802	78.10421.2FL	ZZ.00PAD.Q71
C5803	78.10421.2FL	ZZ.00PAD.Q71
R5803	63.10234.1DL	ZZ.00PAD.Q71
R5804	63.R0034.1DL	ZZ.00PAD.Q71
R5806	63.R0034.1DL	ZZ.00PAD.Q71
R5808	63.51034.1DL	ZZ.00PAD.Q71

X-1.12 2010.3.10

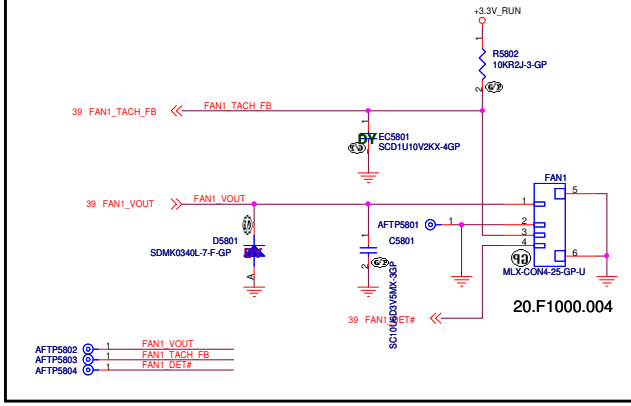
LOCATION	POP P/N	DY P/N
TP5801~TP5815	ZZ.PAD14.001	ZZ.00PAD.Q91

CPU XDP



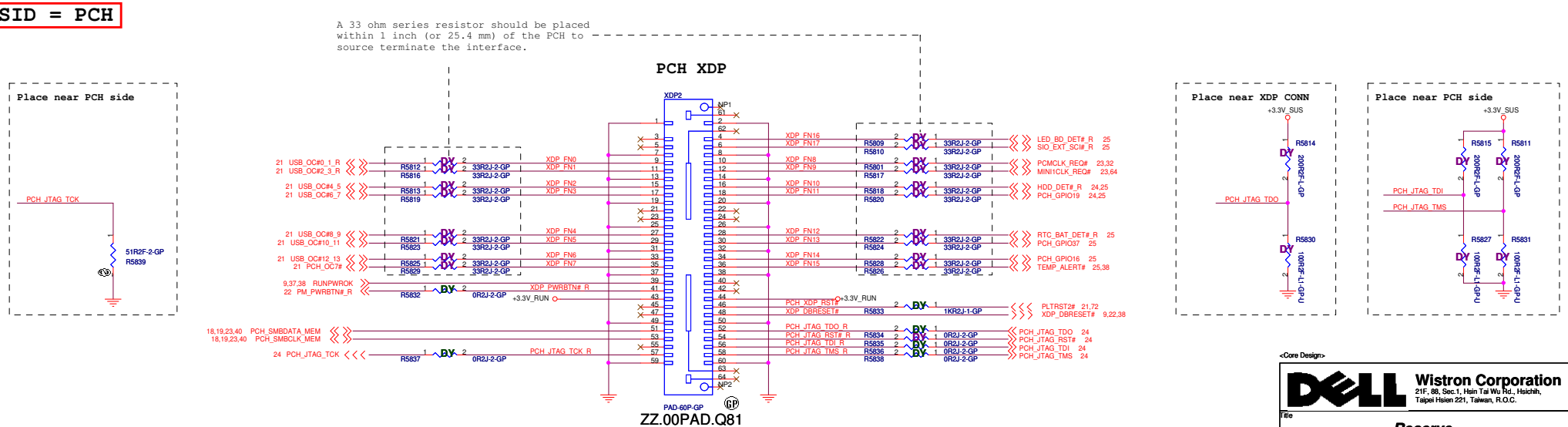
ZZ.00PAD.Q81

SSID = Thermal



20.F1000.004

SSID = PCH



ZZ.00PAD.Q81

<Core Design>

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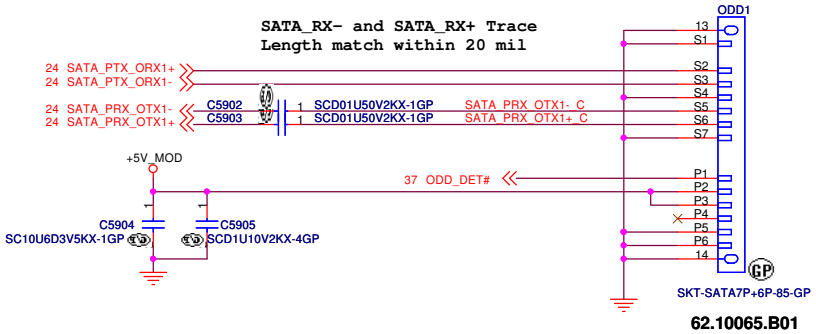
Title: Reserve

Size	Document Number	Rev
C	Fonseca UMA	X02

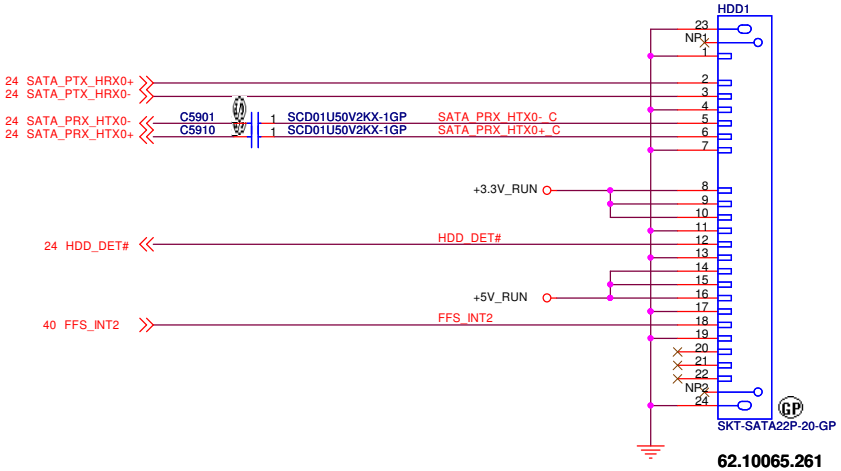
Date: Thursday, March 18, 2010 Sheet 58 of 82

SSID = SATA SATA ODD Connector



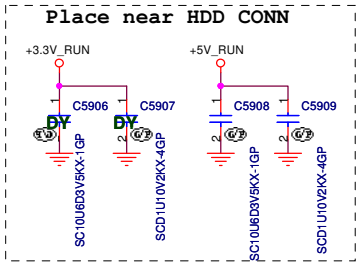
62.10065.B01

SSID = SATA SATA HDD Connector



62.10065.261

```
SATA HDD Interface comment
*****************************
--- GND
RX+
RX-
--- GND
TX-
TX+
--- GND
*****************************
------------ 3.3V
------------ 3.3V
------------ 3.3V
--- GND
--- GND / Dell Detected Pin
--- GND
------------ 5V
------------ 5V
------------ 5V
--- GND
(Dell: FFS_INT for supported HDD)
--- GND
------------ 12V (No support)
------------ 12V (No support)
------------ 12V (No support)
*****************************
```



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD / ODD Connector

Size	Document Number	Rev
A3	Fonseca UMA	X02

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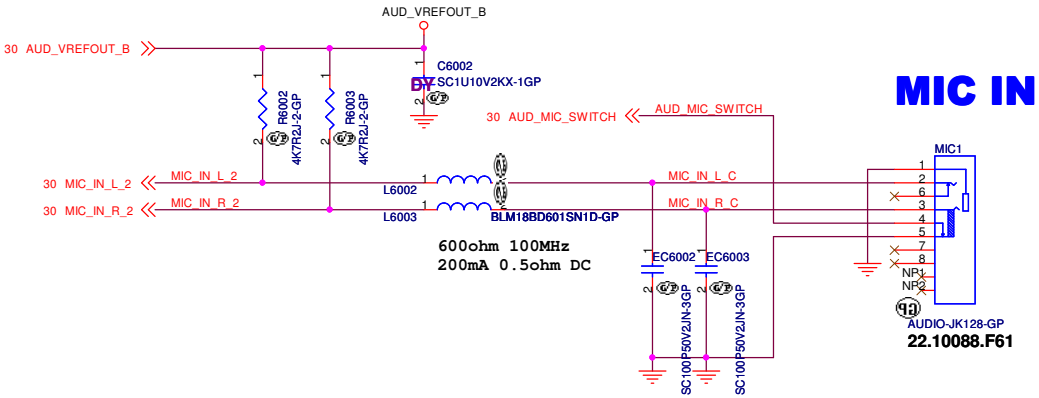
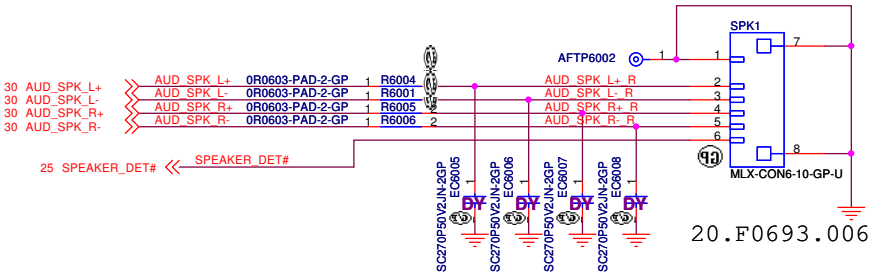
SSID = AUDIO

MIC IN



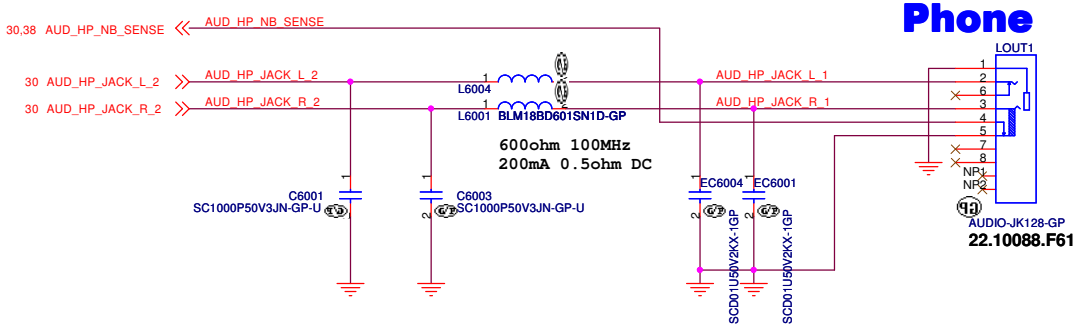
SSID = AUDIO

SPEAKER



SSID = AUDIO

Hear Phone



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack / Speaker Connector

Size	Document Number	Rev
A3	Fonseca UMA	X02

Date: Thursday, March 18, 2010 Sheet 60 of 82

SSID = LOM

(Blank)

<Core Design>

Wistron Corporation
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Title: Reserve

Size	Document Number	Rev
C	Fonseca UMA	X02

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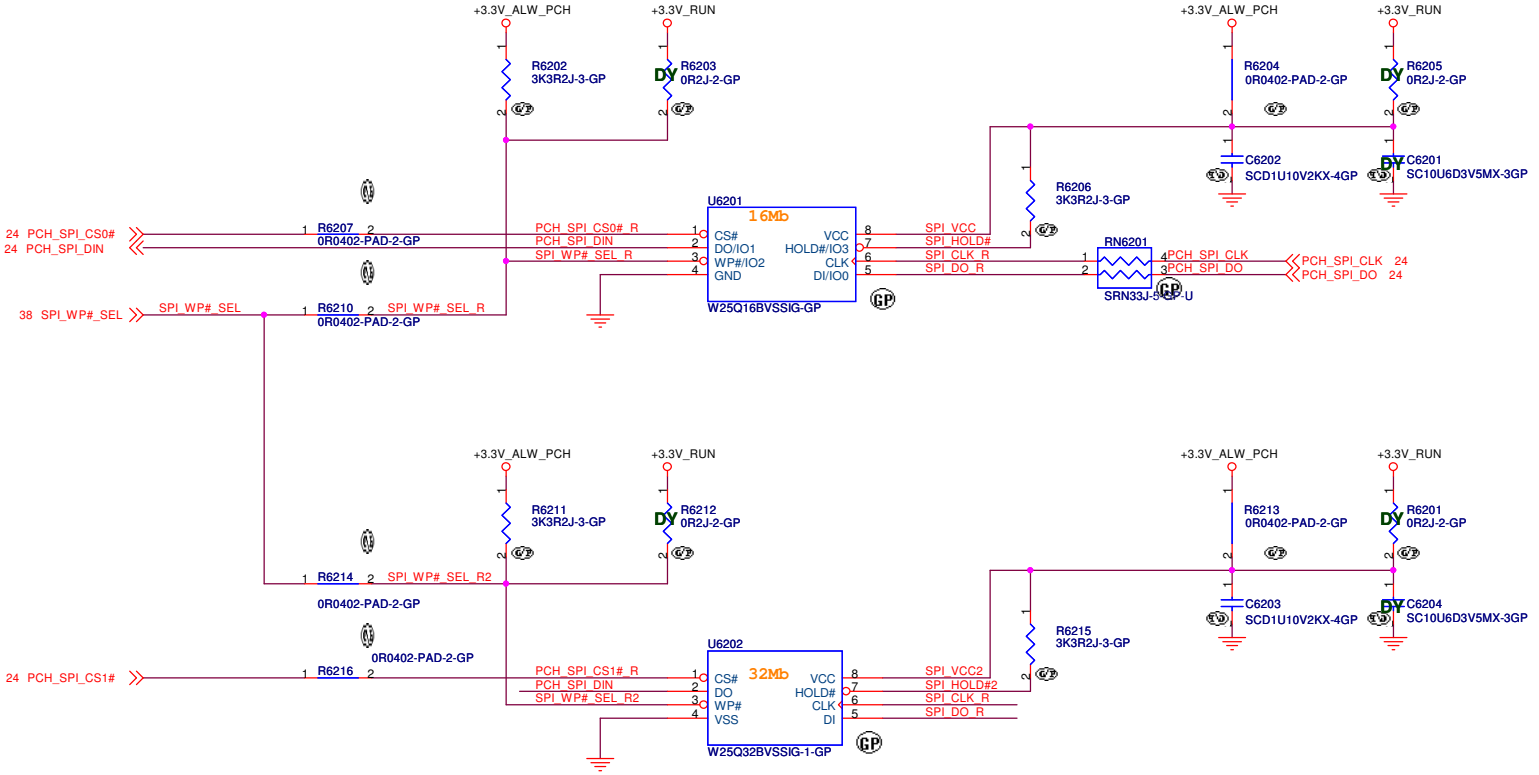
SSID = Flash.ROM



#1 source: 72.25Q16.001 (2MB, Winbond)
#2 source: 72.25165.B01 (2MB, MXIC)
#3 source: 72.02516.A01 (2MB, Numonyx)

#1 source: 72.25Q32.A01 (4MB, Winbond)
#2 source: 72.25325.A01 (4MB, MXIC)
#3 source: 72.25P32.B01 (4MB, Numonyx)

Pin.2
From Intel checklist,
SPI_CS0#/CS1#
No series resistor required
if routing length is 1.5"-6.5"
(with 1 or 2 SPI device)

Pin.6
Intel checklist
No series resistor required if routing length is 1.5"-6.5"
(with 1 or 2 SPI device)

<Core Design>

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Title: Flash / EEPROM

Size	Document Number	Rev
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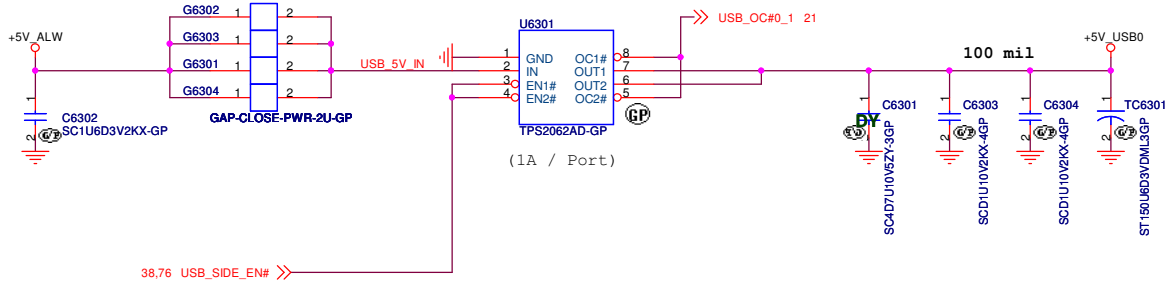
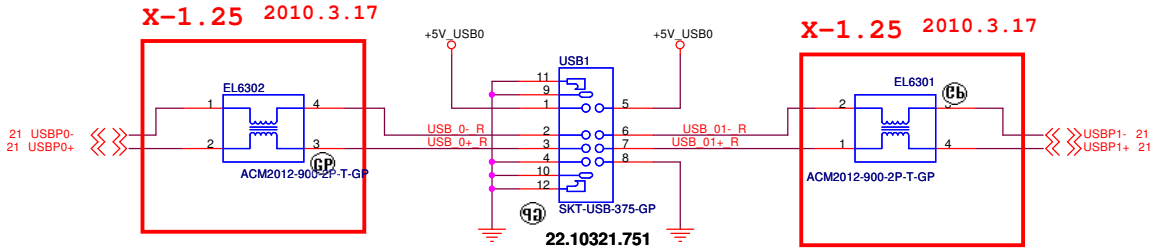
SSID = USB

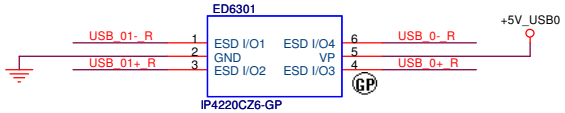
Charger USB



Charger USB Connector

S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D





<Core Design>

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Title: USB

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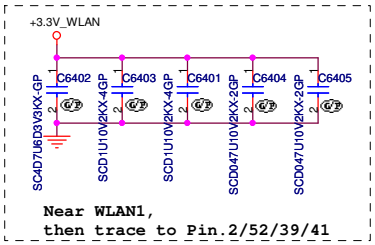
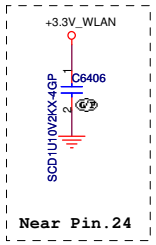
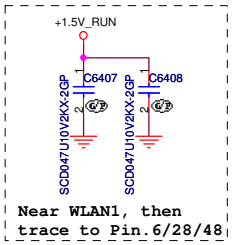
SSID = WLAN



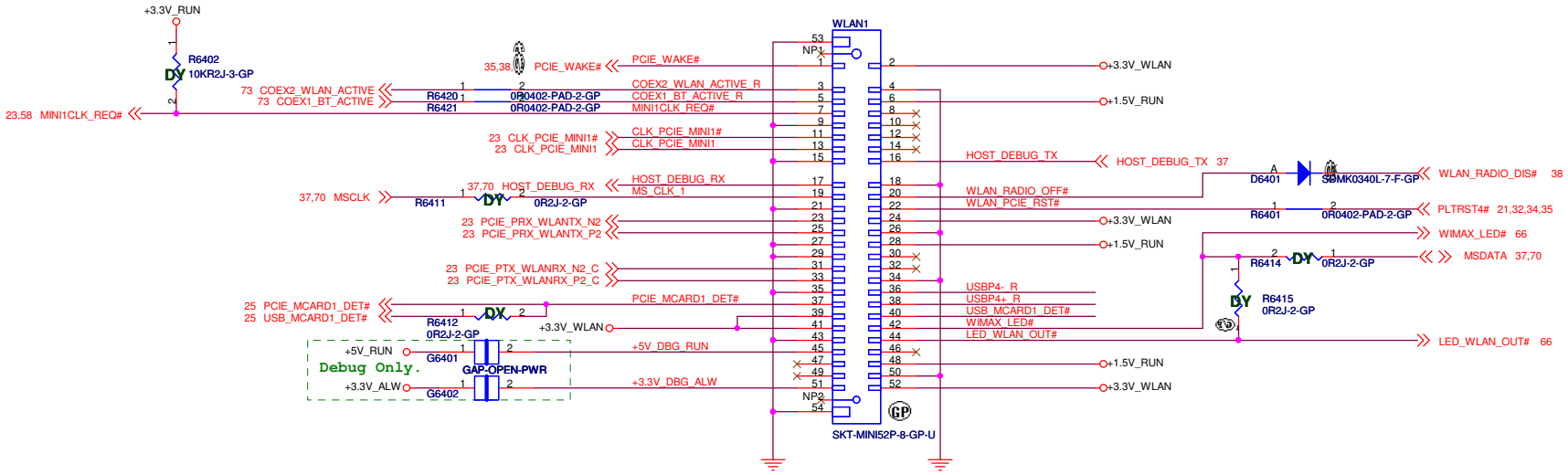




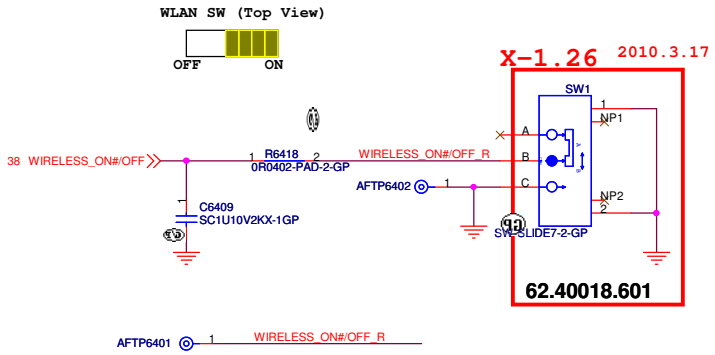
DEBUG PINS

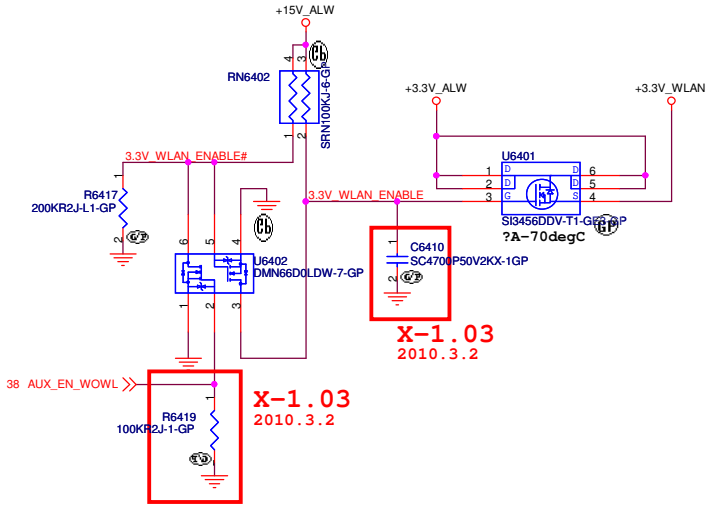
JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	B44
17	HOST_DEBUG_RX	B46
19	8051_TX	B43
42	8051_RX	A40

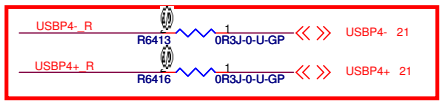
MiniCard WLAN connector



Wireless Switch







Close WLAN1

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: WLAN / Serial Out Connector

Size: Custom | Document Number: Fonseca UMA | Rev: X02

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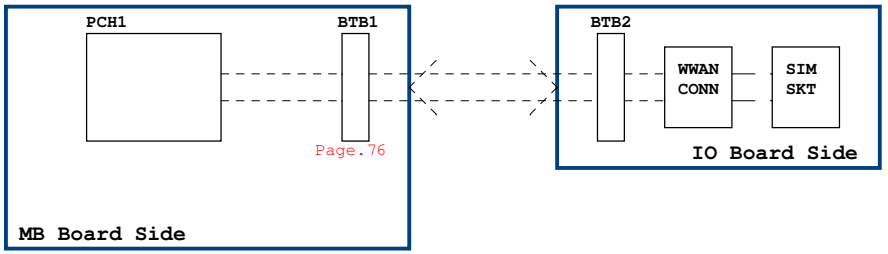
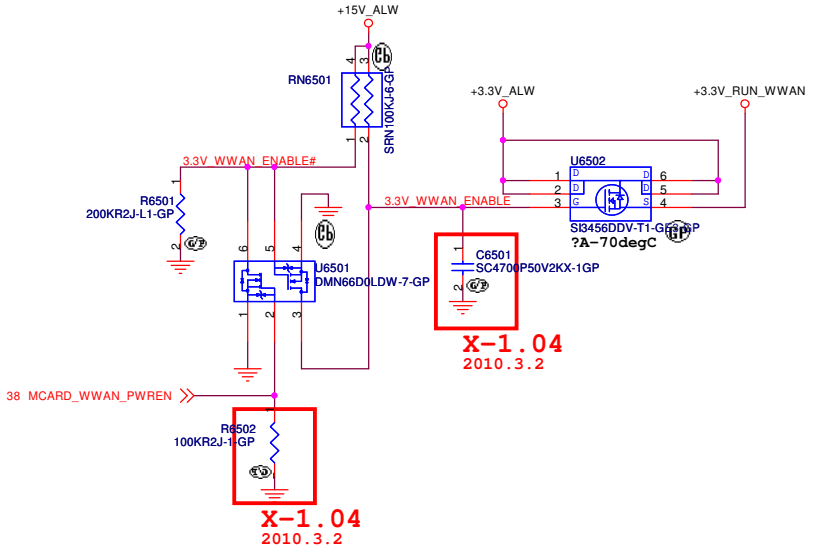
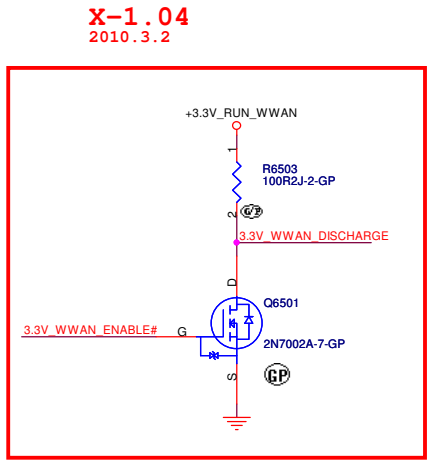
SSID = WWAN







<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN

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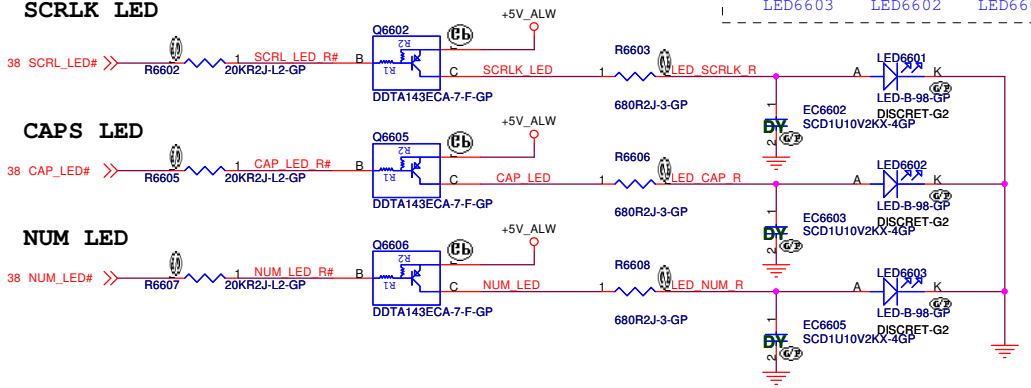
SSID = User.interface

LED Location from left to right (MB, Top View)

NUM	CAPS	SCRLK
LED6603	LED6602	LED6601

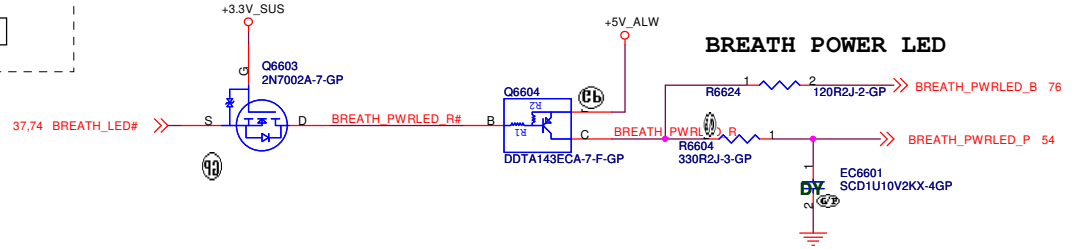
SCRLK LED



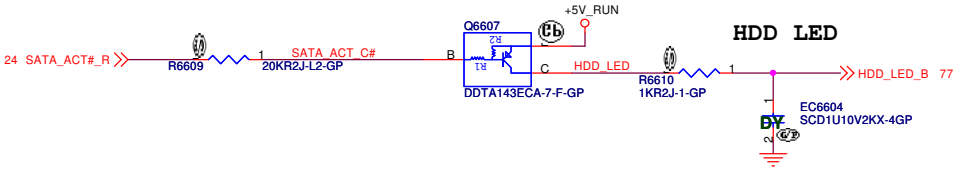
CAPS LED

NUM LED

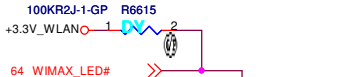
BREATH POWER LED



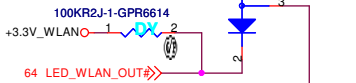
HDD LED



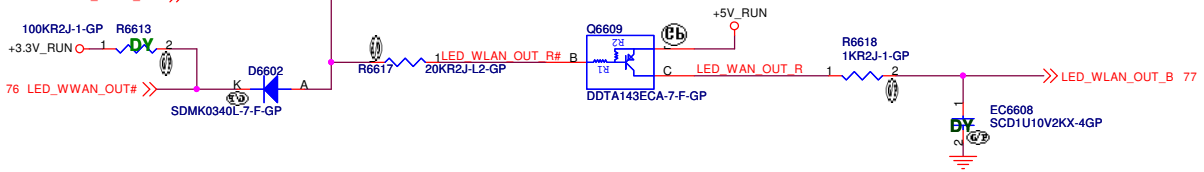
WIMAX LED



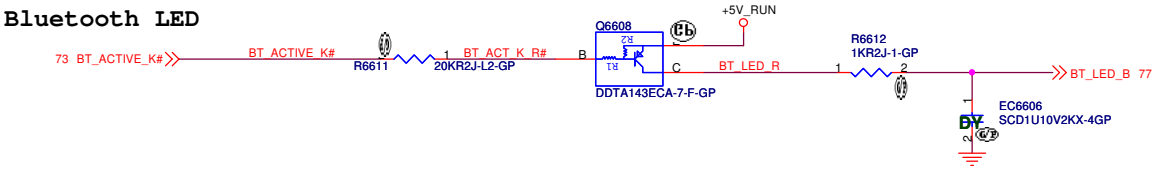
WLAN LED



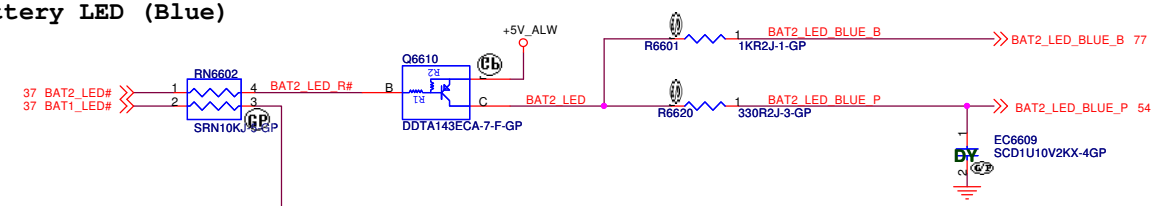
WWAN LED



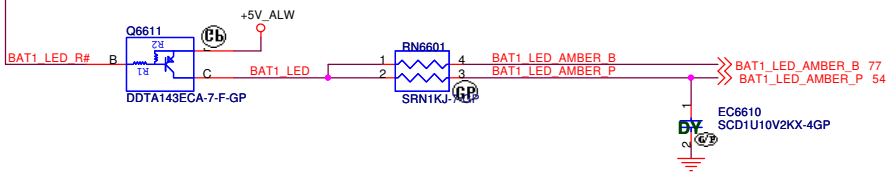
Bluetooth LED



Battery LED (Blue)



Battery LED (Amber)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED

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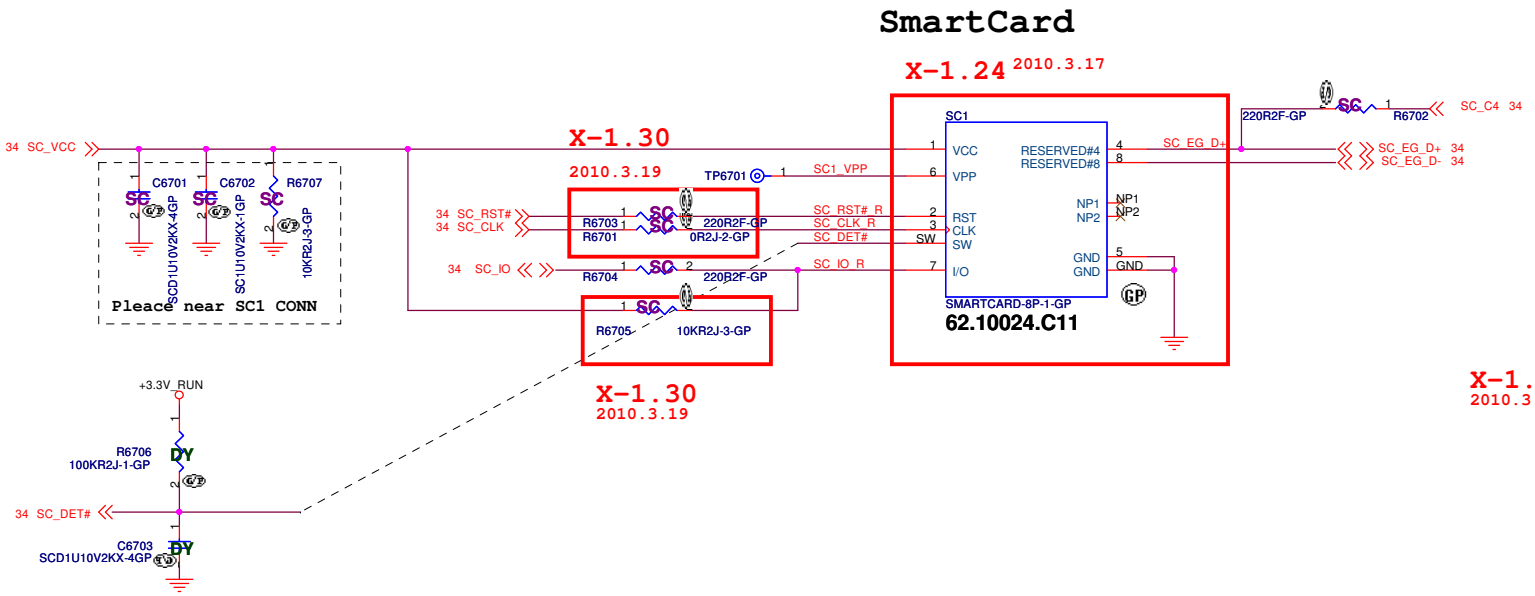
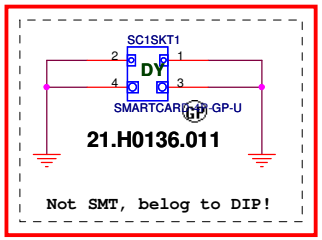
SSID = SmartCard

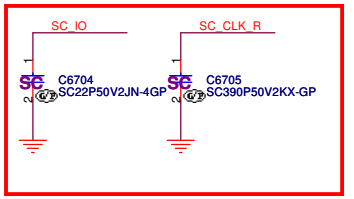


X-1.24 2010.3.17

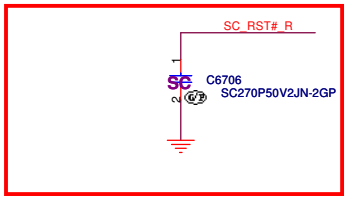
SmartCard Socket



X-1.21 2010.3.10



X-1.29 2010.3.18



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

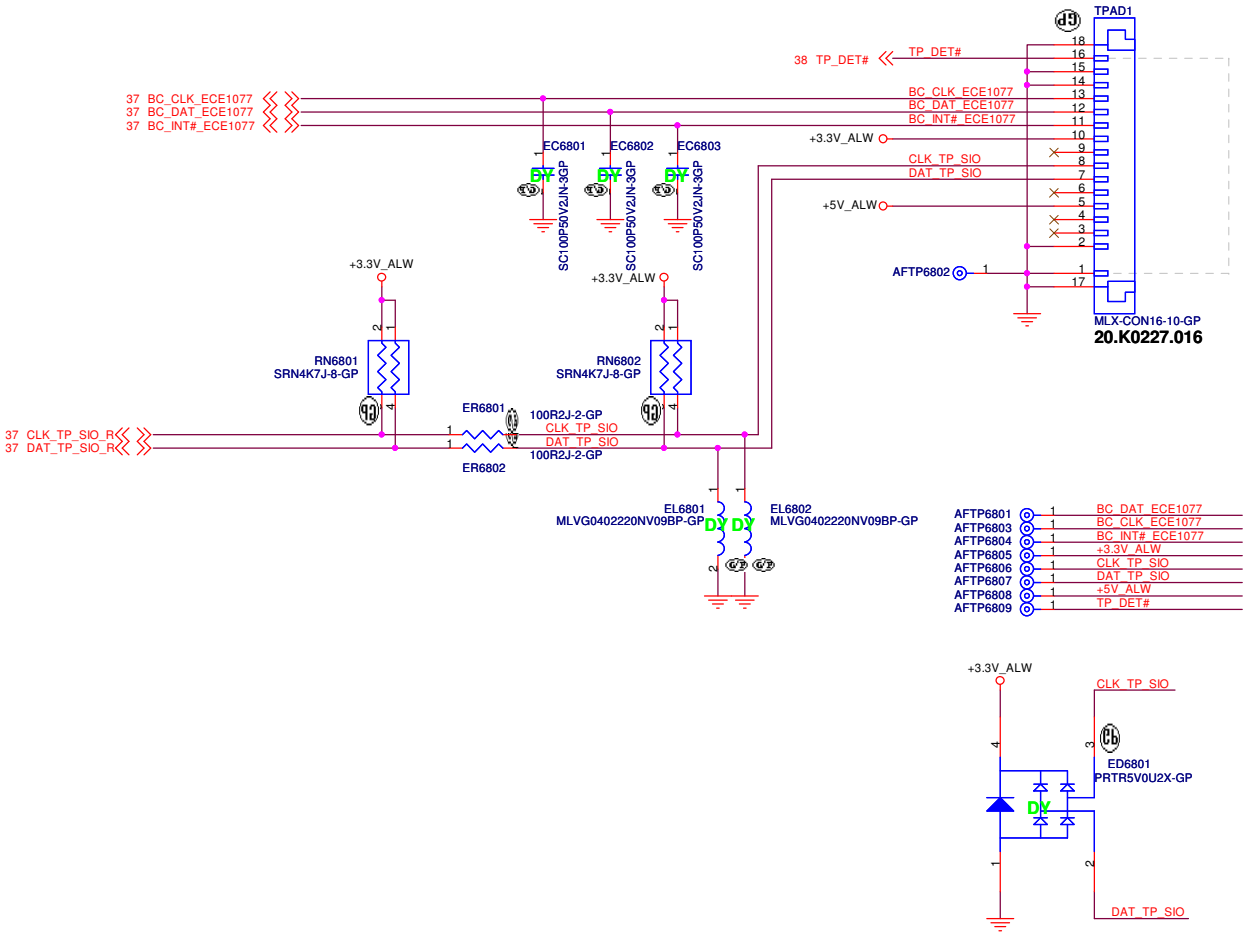
Title: Smart Card Socket

Size	Document Number	Rev
A3	Fonseca UMA	X02

Date: Friday, March 19, 2010 Sheet 67 of 82

SSID = Touch.Pad

TouchPad Connector



Touch PAD Module Side

16	TP_DET#
15	GND
14	GND
13	BC_CLK (ECE1077)
12	BC_DAT (ECE1077)
11	BC_INT# (ECE1077)
10	3.3V_ALW
09	3.3V_RUN (Internal NC)
08	PS2_CLK
07	PS2_DATA
06	5V_RUN (Backlight, No Use)
05	5V_ALW (Chip change to use 3V, NC)
04	PWM (Backlight, No Use)
03	GND (Backlight, No Use)
02	GND
01	Diag_loop

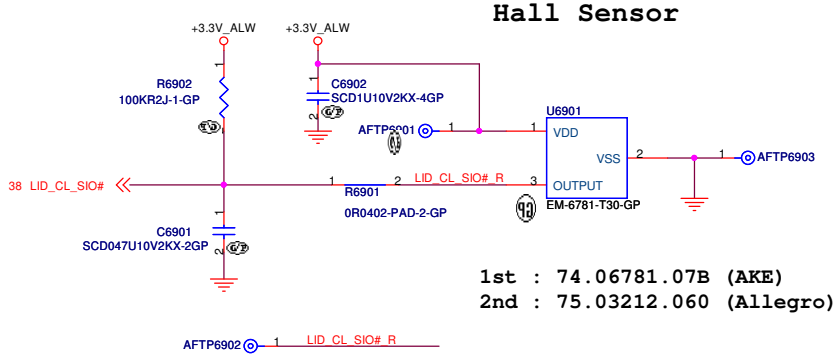
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Touch Pad Connector	
Size: A3	Document Number: Fonseca UMA	Rev: X02
Date: Thursday, March 18, 2010	Sheet 68 of 82	

SSID = User.interface

Hall Sensor



1st : 74.06781.07B (AKE)
2nd : 75.03212.060 (Allegro)

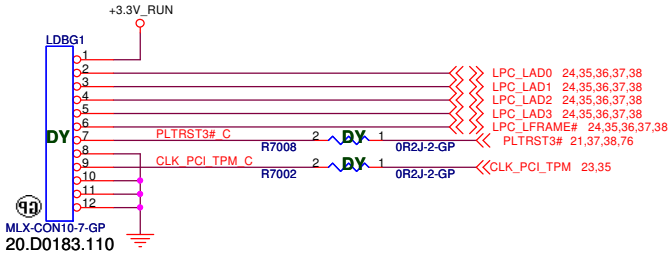
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Hall Sensor*		
Size: A3	Document Number: *Fonseca UMA*	Rev: *X02*
Date: Thursday, March 18, 2010	Sheet 69 of 82	

SSID = User.Interface

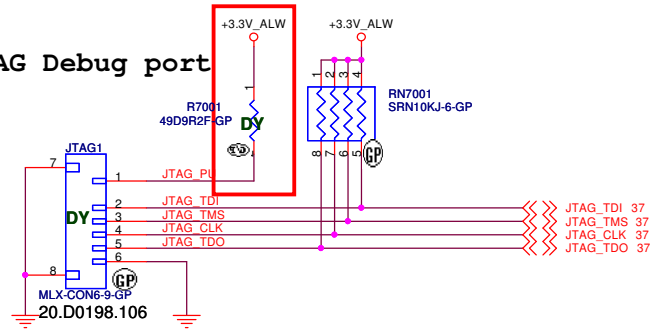
LPC Debug port

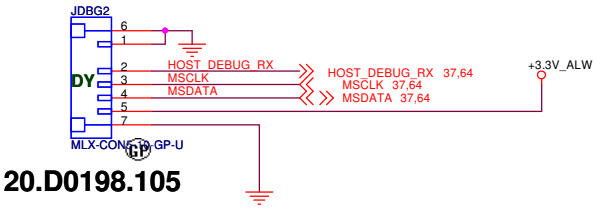


LDBG1, need pop R7008, R7002

X-1.22 2010.3.10

JTAG Debug port





20.D0198.105

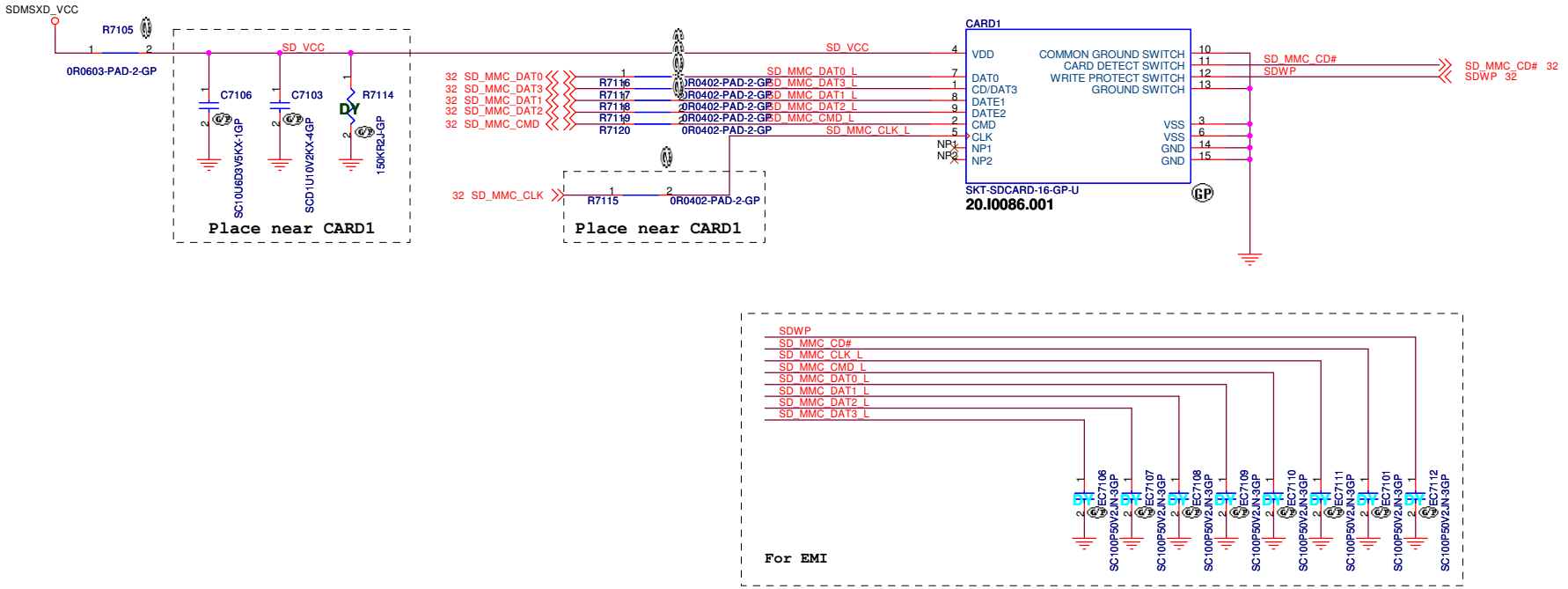
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
JTAG Debug		
Size: A3	Document Number: Fonseca UMA	Rev: X02
Date: Wednesday, March 17, 2010	Sheet 70 of 82	

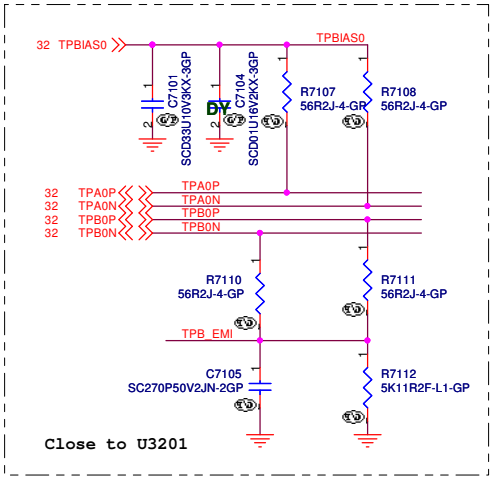
SSID = 1394

Flash Reader Socket

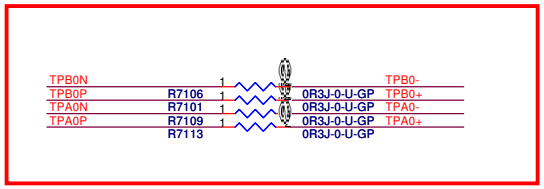


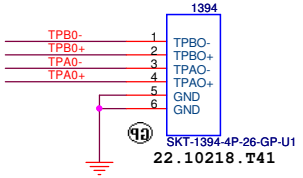
SSID = 1394

Shield GND separately for pairs of
TPA+ & TPA- and TPB+ & TPB-



X-1.10 2010.3.2





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

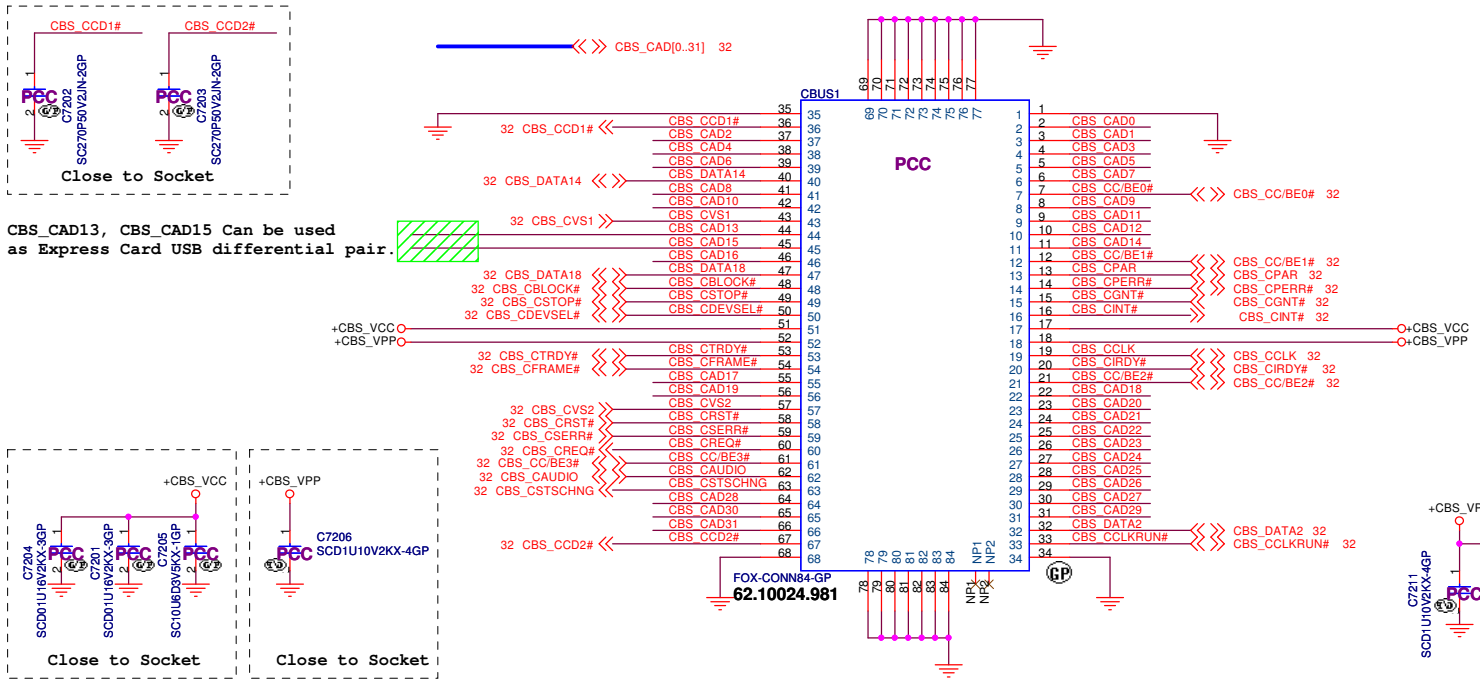
Title: 1394 Connector / Flash Socket

Size: A3 | Document Number: Fonseca UMA | Rev: X02

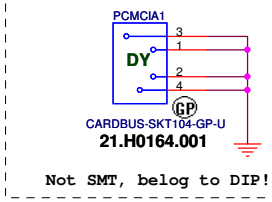
Date: Wednesday, March 17, 2010 | Sheet 71 of 82

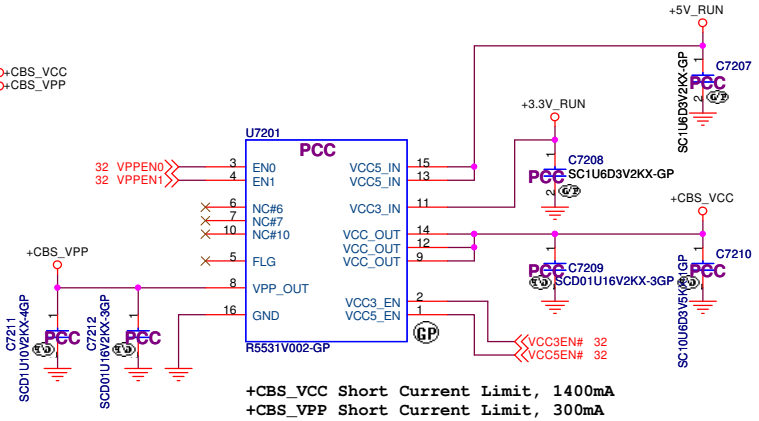
SSID = CARDBUS

Cardbus Connector



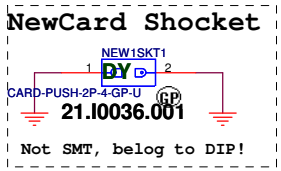
Cardbus Shocket

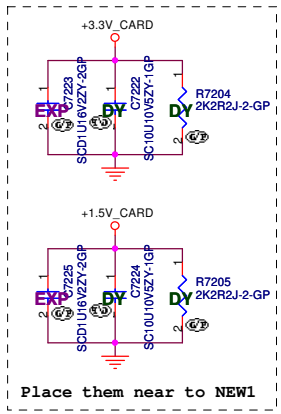




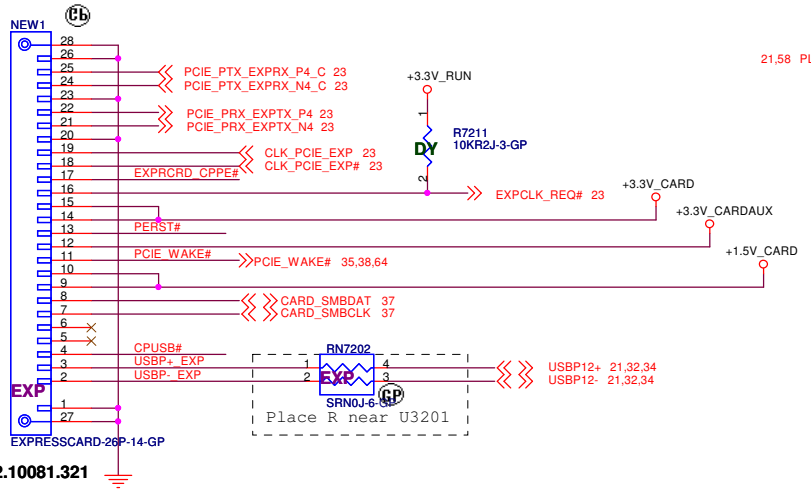
SSID = ExpressCard

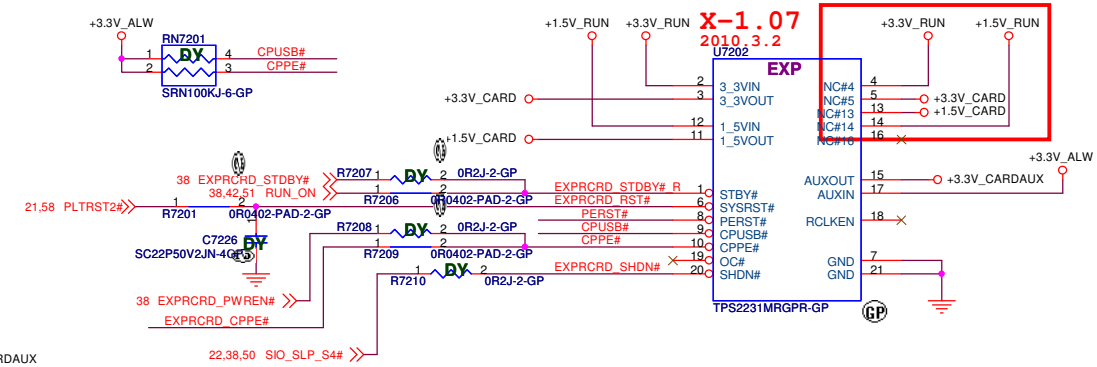
NewCard Shocket

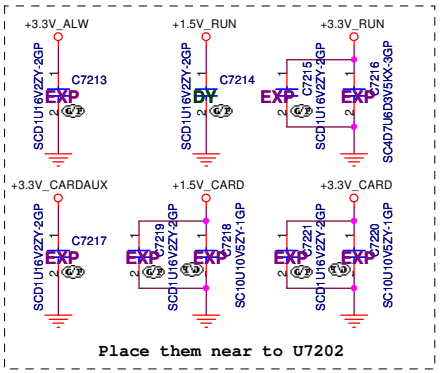




NewCard Connector







<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / ExpressCard

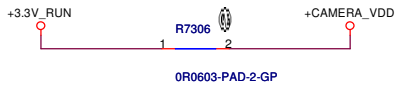
Size: A3 | Document Number: Fonseca UMA | Rev: X02

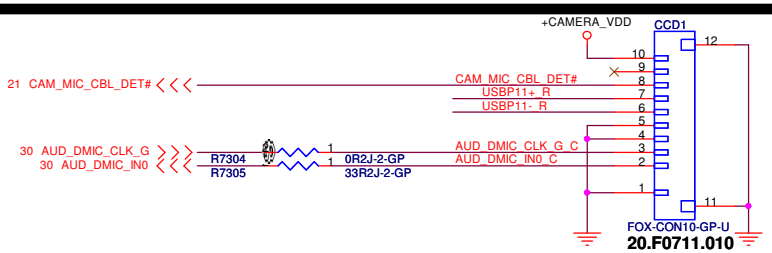
Date: Thursday, March 18, 2010 | Sheet 72 of 82

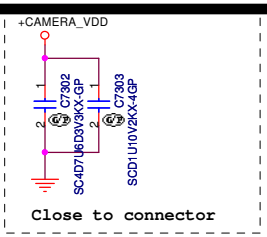
SSID = User.interface

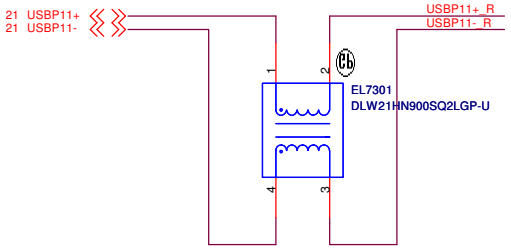
Camera Connector

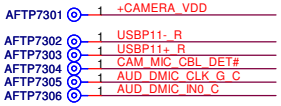
Camera Power CTRL





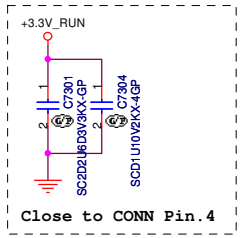


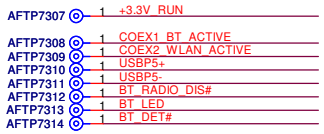


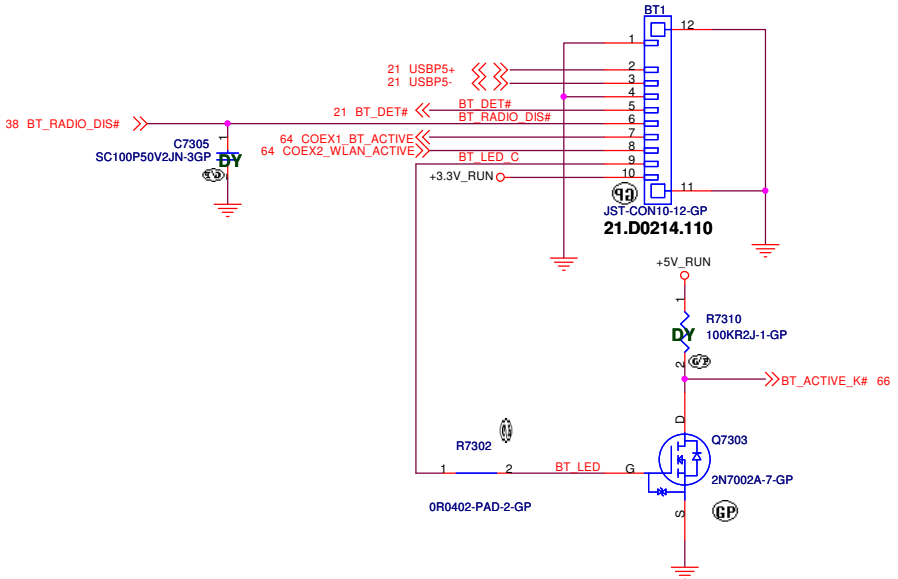


SSID = User.interface

Bluetooth Connector







MB BT CONN / BT Module CONN

PIN	Define	PIN	Define
1	GND	1	GND
2	USBP5+_R	12	USB_DP
3	USBP5-_R	11	USB_DN
4	GND	10	GND
5	BT_DET#	2	MOD_DET
6	BT_RADIO_DIS#	7	RADIO_DIS
7	COEX1_BT_ACTIVE	3	COEX1_BT_ACTIVE
8	COEX2_WLAN_ACTIVE	8	COEX2_WLAN_ACT
9	BT_LED	6	LINK_IND
10	+3.3V_RUN	9	3.3V
11	NC		
12	NC		

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth / Camera / DMIC

Size: A3 | Document Number: Fonseca UMA | Rev: X02

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SSID = Docking

DK1

JAE-CONN144D-3-GP-U

20.F1572.144

Dock eSATA

]----->Dock USB 1

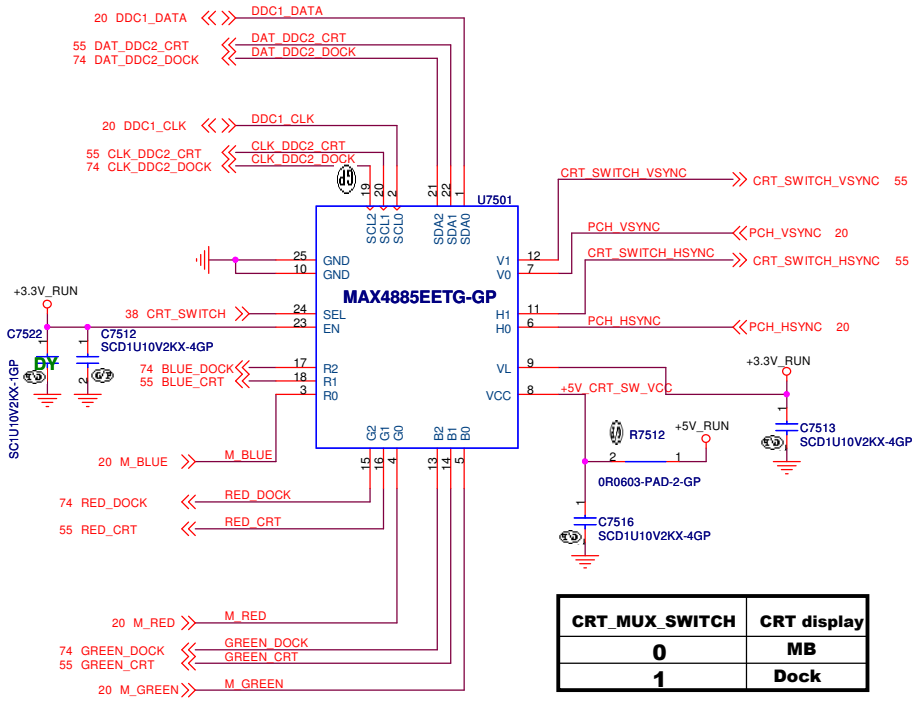
]----->Dock USB 2

Clost to DK1

<Core Design>

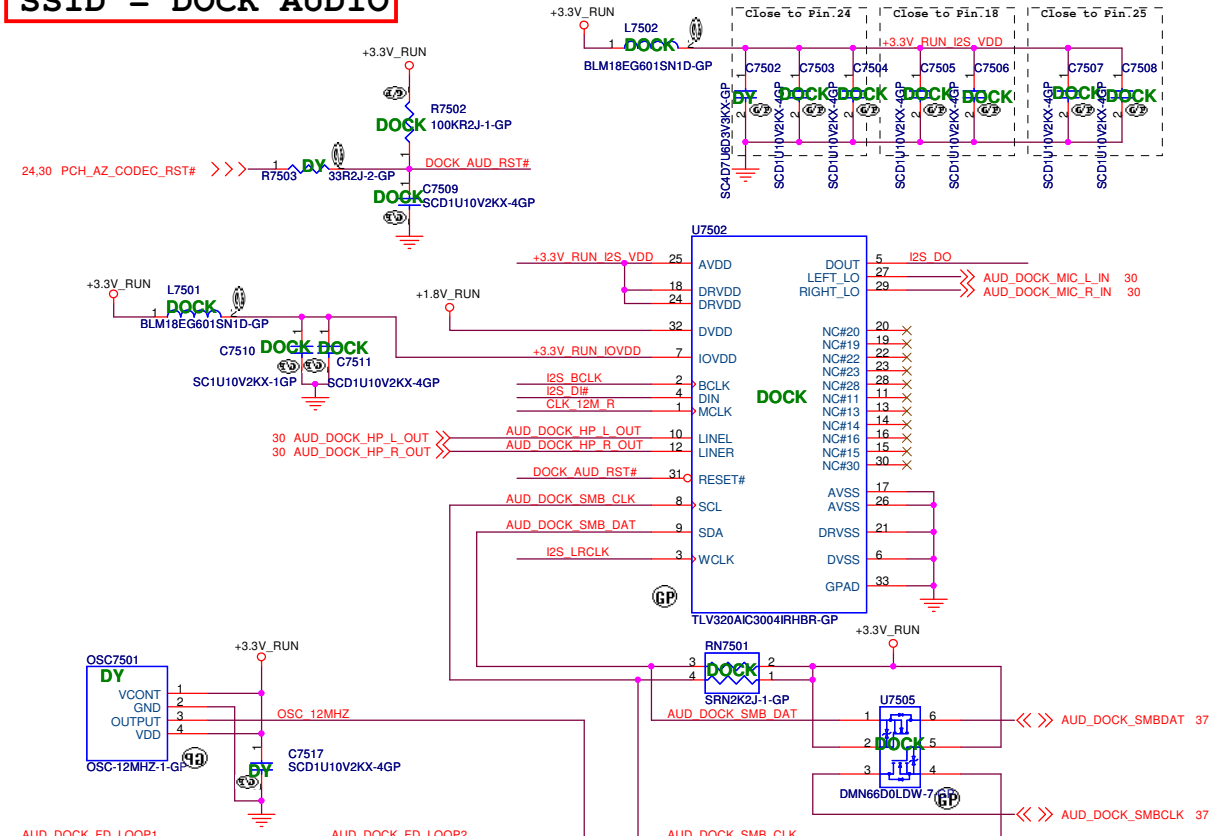
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Docking Connector
Size: Custom	Document Number: Fonseca UMA
Rev	X02
Date: Thursday, March 18, 2010	Sheet 74 of 82

SSID = DOCK CRT SWITCH



CRT_MUX_SWITCH	CRT display
0	MB
1	Dock

SSID = DOCK AUDIO



<Core Design>

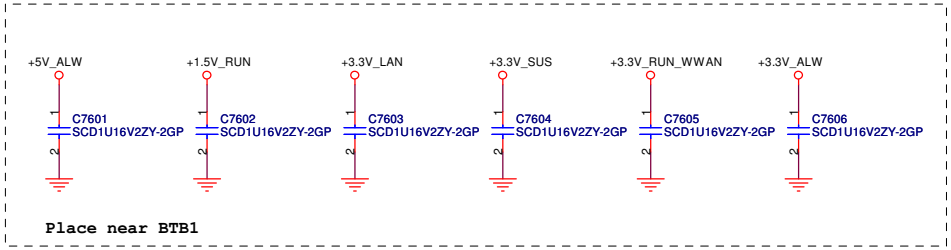
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Docking IC / SW

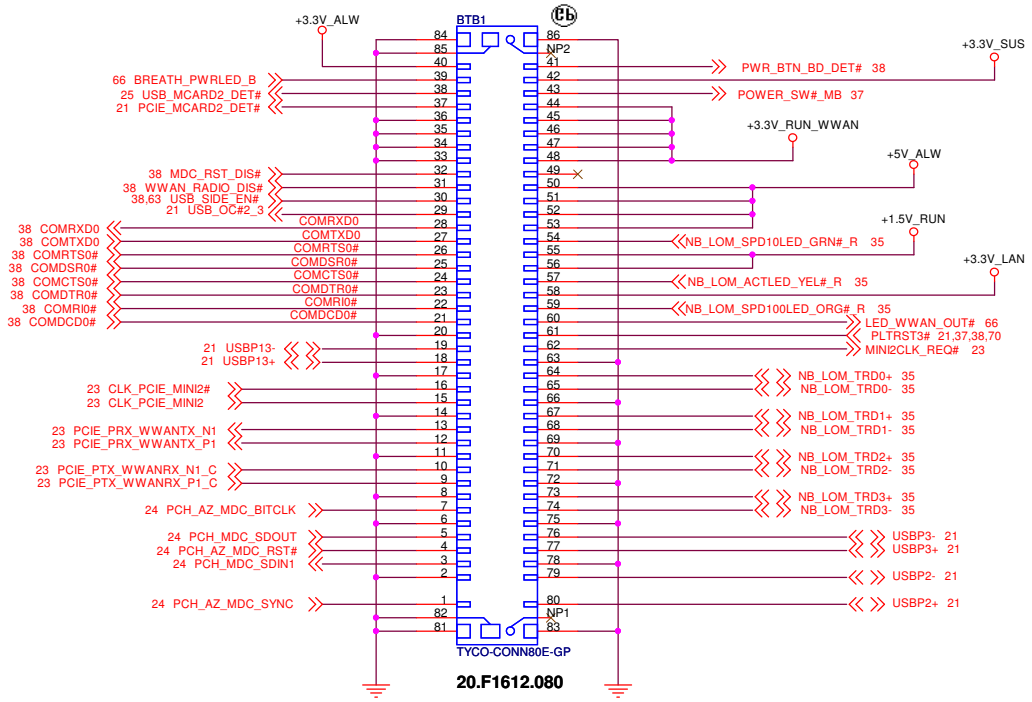
Size: A3 | Document Number: Fonseca UMA | Rev: X02

Date: Wednesday, March 17, 2010 | Sheet 75 of 82

SSID = User.Interface



IO Board Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

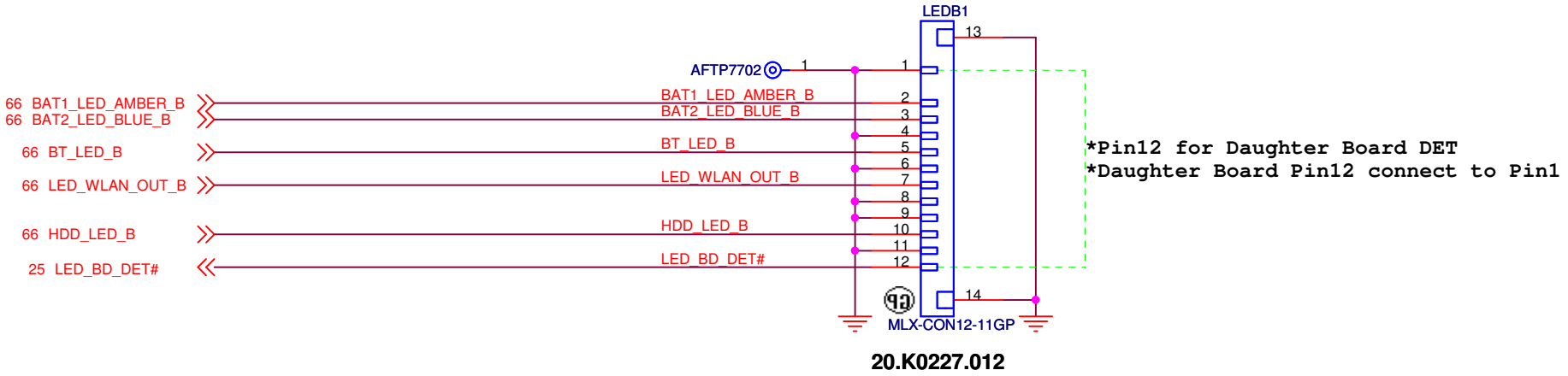
Title: IO Board CONN

Size: A3 | Document Number: Fonseca UMA | Rev: X02

Date: Wednesday, March 17, 2010 | Sheet 76 of 82

SSID = User.interface

LED BD Connector



20.K0227.012

AFTP7701 — BAT1_LED_AMBER_B
AFTP7703 — BAT2_LED_BLUE_B
AFTP7704 — BT_LED_B
AFTP7705 — LED_WLAN_OUT_B
AFTP7706 — HDD_LED_B
AFTP7707 — LED_BD_DET#

LED Location from left to right

HDD	BATTERY	WLAN	BLUE TOOTH

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Board Connector

Size	Document Number	Rev
A4	Fonseca UMA	X02

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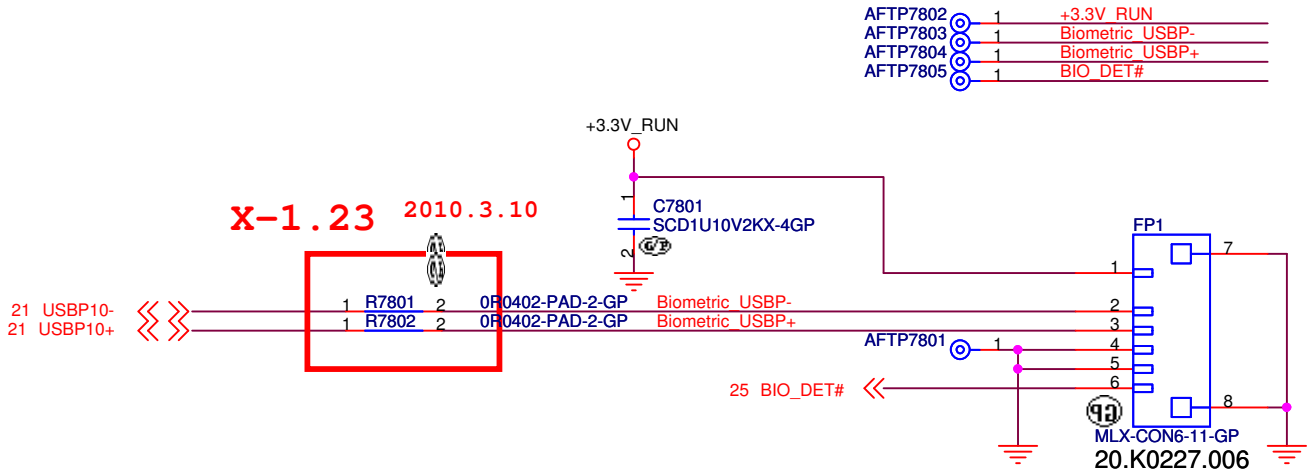
SSID = User.Interface



Biometric Connector

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Finger Printer Board CONN***

Size	Document Number	Rev
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SSID = Mechanical

Hole

ZZ.00PAD.J11

H1 HOLE298R166-GP
H2 HOLE298R166-GP
H3 HOLE298R166-GP
H4 HOLE298R166-GP
For CPU

ZZ.00PAD.I51

H6 HTE10BE10R32-D-55-GP
H7 HTE10BE10R32-D-55-GP
For Docking

ZZ.00PAD.J01

H8 HOLE256R126-GP
For IO Board

Hole

ZZ.00PAD.M01

H9 HOLET256B315R111-GP

ZZ.00PAD.I71

H11 HOLE355X355R126-GP
H12 HOLE355X355R126-GP
H13 HOLE355X355R126-GP
H14 HOLE355X355R126-GP
H15 HOLE355X355R126-GP
H16 HOLE355X355R126-GP

H17 HOLE
H27 HOLE

Hole

X-1.27
2010.3.17

ZZ.00PAD.S31

H18 HOLE78X42R54X34-S-GP
H19 HOLE78X42R54X34-S-GP

ZZ.00PAD.I61

H20 HOLE300X166R111-GP
H21 HOLE300X166R111-GP

ZZ.00PAD.I81

H24 HOLE197R91-GP
H25 HOLE197R91-GP

H10 HT65585X925R29-S-GP
ZZ.00PAD.E01

BOSS1
BOSS1 STF217R128H83-GP
34.4Y702.001
For Heatsink

H22 HT65X75B62X56R28-2P-S-GP
H23 HOLE197R99-1-GP
H26 HTE54585R28-D-42-GP

Spring

34.4F822.002

SPR1 SPRING-51-GP
SPR2 SPRING-51-GP
SPR3 SPRING-51-GP

34.45T31.001

SPR4 SPRING-24-GP-U
SPR5 SPRING-24-GP-U

34.45T31.001

SPR6 SPRING-24-GP-U
SPR7 SPRING-24-GP-U

Unused Parts

+3.3V_RUN U7402E TSAHC14PW-GP
+3.3V_RUN U7402F TSAHC14PW-GP
+5V_CRT_RUN U5501C SSAHCT125PWR-GP
+5V_CRT_RUN U5501D SSAHCT125PWR-GP

RF Cap.

+5V_ALW EC7902 SCD1U25V2ZY-1GP
+5V_ALW EC7903 SC33P50V2JN-3GP

+3.3V_RUN EC7905 SC33P50V2JN-3GP
+3.3V_RUN +1.05V_RUN EC7906 SC33P50V2JN-3GP

+5V_ALW EC7907 SC33P50V2JN-3GP
+5V_ALW EC7908 SC33P50V2JN-3GP

RF Cap.

+3.3V_ALW EC7909 SC33P50V2JN-3GP
+1.5V_SUS EC7910 SC33P50V2JN-3GP
+1.5V_SUS EC7911 SC33P50V2JN-3GP
+5V_RUN EC7912 SCD1U25V2ZY-1GP
+5V_RUN EC7913 SC33P50V2JN-3GP
+5V_RUN EC7914 SC33P50V2JN-3GP
+5V_RUN EC7915 SC33P50V2JN-3GP
+3.3V_RUN EC7916 SC33P50V2JN-3GP

RF Cap.

+3.3V_RUN EC7917 SC33P50V2JN-3GP
+3.3V_RUN EC7918 SC33P50V2JN-3GP
+3.3V_RUN +1.05V_RUN EC7920 SC33P50V2JN-3GP
+1.05V_RUN EC7921 SC33P50V2JN-3GP
+1.5V_SUS EC7922 SC33P50V2JN-3GP
+1.5V_SUS EC7923 SC33P50V2JN-3GP
+3.3V_RUN EC7919 SC33P50V2JN-3GP

RF Cap.

+5V_ALW EC7924 SC33P50V2JN-3GP
+5V_ALW EC7925 SC33P50V2JN-3GP
+1.05V_RUN EC7926 SC33P50V2JN-3GP
+1.05V_RUN EC7927 SC33P50V2JN-3GP
+3.3V_RUN EC7928 SC33P50V2JN-3GP
+3.3V_RUN EC7929 SC33P50V2JN-3GP
+PWR_SRC EC7930 SCD1U50V3KX-GP
+PWR_SRC EC7931 SC68P50V2JN-2GP

RF Cap.

+5V_RUN EC7932 SC33P50V2JN-3GP
+3.3V_RUN EC7933 SC33P50V2JN-3GP
+3.3V_RUN EC7934 SC33P50V2JN-3GP
+3.3V_RUN EC7935 SC33P50V2JN-3GP
+5V_RUN EC7936 SC33P50V2JN-3GP
+5V_RUN EC7937 SC33P50V2JN-3GP
+PWR_SRC EC7939 SCD1U50V3KX-GP
+PWR_SRC EC7940 SCD1U50V3KX-GP

EMI Cap.

+5V_ALW EC7901 SCD1U50V3KX-GP
+3.3V_RUN EC7904 SCD1U50V3KX-GP
+PWR_SRC EC7938 SCD1U50V3KX-GP
+3.3V_RUN EC7941 SC33P50V2JN-3GP
+PWR_SRC_3V EC7942 SCD1U25V2ZY-1GP

EMI Cap.

<Core Design>

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DATE	NO	PAGE	ACTION	reference	Issue Description	OWNER
20100302	X-1.01	47	change	PTC4701 --->DY PTC4702 --->POP	change cap place location for factory request.	EE
	X-1.02	58	DY	XDP1,XDP2,C5802,C5803,R5803,R5804,R5806,R5808	change to DY part number for layout used.	EE
	X-1.03	64	STUFF	C6410,R6419	C6410 --> soft start R6419 --> quick discharge	EE
	X-1.04	65	STUFF	C6501,R6502,R6503,Q6501	C6501 --> soft start R6502,R6503,Q6501 --> quick discharge	EE
	X-1.05	42	Change	C4208	change to 470P for soft start used	EE
	X-1.06	51	ADD	PC5108	reserve location	POWER-EE
	X-1.07	72	ADD	U7202	add pin4,5,13,14 for second source	EE
	X-1.08	37	Change	R3703	change board ID to -1	EE
	X-1.09	37,54	ADD	R3741,Q5404,R5428,R5429,C5412,U5402,C5410,C5411	add power switch to control lcd power	EE
	X-1.10	71	remove	L7504,L7101	remove co-layout part for PSE request	EMC
20100310	X-1.11	54	change	R5415	change part number to 63.10133.15L	EE
	X-1.12	58	change	TP5801~TP5815	change test pad to DY part for layout	EE
	X-1.13	7	remove	RN701,RN703,RN704,RN705	remove 0 ohm part for layout	EE
	X-1.14	23	change	RN2312,RN2313	change RN2312 ,RN2313 to short pad for layout	EE
	X-1.15	23	remove	RN2307,RN2308,RN2301	remove 0 ohm part for layout	EE
	X-1.16	25	remove	RN2501	remove 0 ohm part for layout	EE
	X-1.17	32	change	RN3201	change RN3210 to short pad for layout	EE
	X-1.18	40	STUFF	C4002		EE
	X-1.19	64	remove	EL6401	remove EL6401 for PSE request because it co-layout with resister.	PSE
	X-1.20	55	ADD	AFTP5501	add test pad for I/O test used	factory
	X-1.21	67	STUFF	C6704,C6705		EE
	X-1.22	70	DY	R7001	not use debug port	EE
	X-1.23	78	change	remove EL7801 change R7801,R7802 to short pad	remove EL7801 for PSE request because it co-layout with resister.	PSE
20100317	X-1.24	67	change	SC1 SC1SKT1	change connector type	ME
	X-1.25	63	remove	EL6301 EL6302	remove co-layout 0 ohm pad	PSE
	X-1.26	64	change	SW1	change connector type	PSE
	X-1.27	79	change	H18 H19	change hole type	ME
20100318	X-1.28	9	DY	R913 Q901 C901 R903		EE
	X-1.29	67	ADD	C6706		EE
20100319	X-1.30	67	change	C6704 C6705 R6705	change resister and capacitance value	EE

Core Design

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Title: *Change List (1/1)*

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