

Fonseca 14.1" DIS Schematics Document

rPGA988A Mobile Arrandale

Intel Ibex Peak-M

2009-11-02

REV : X01

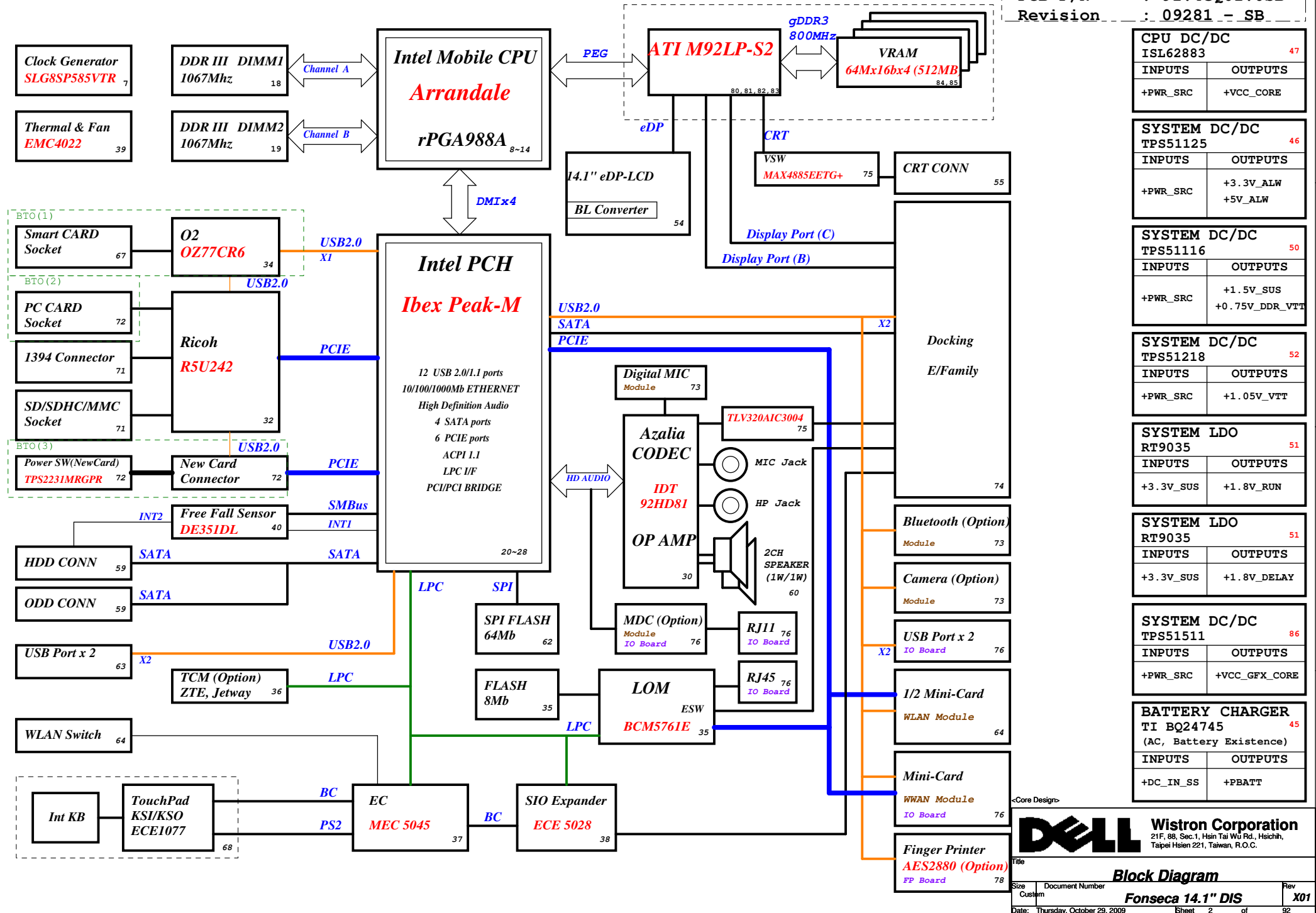
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B_TPM:Use Lom TPM
C_TPM:Use China TPM

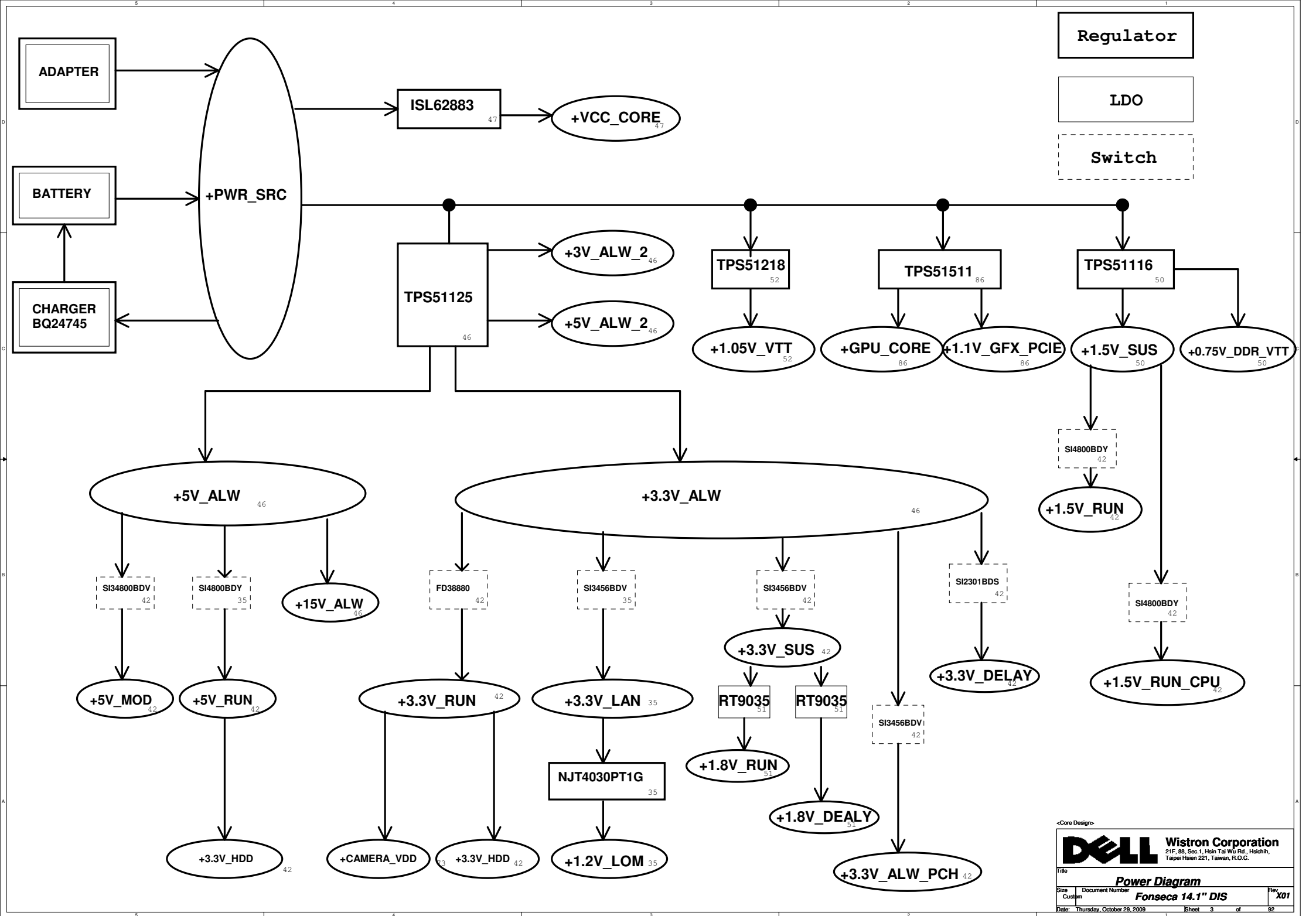
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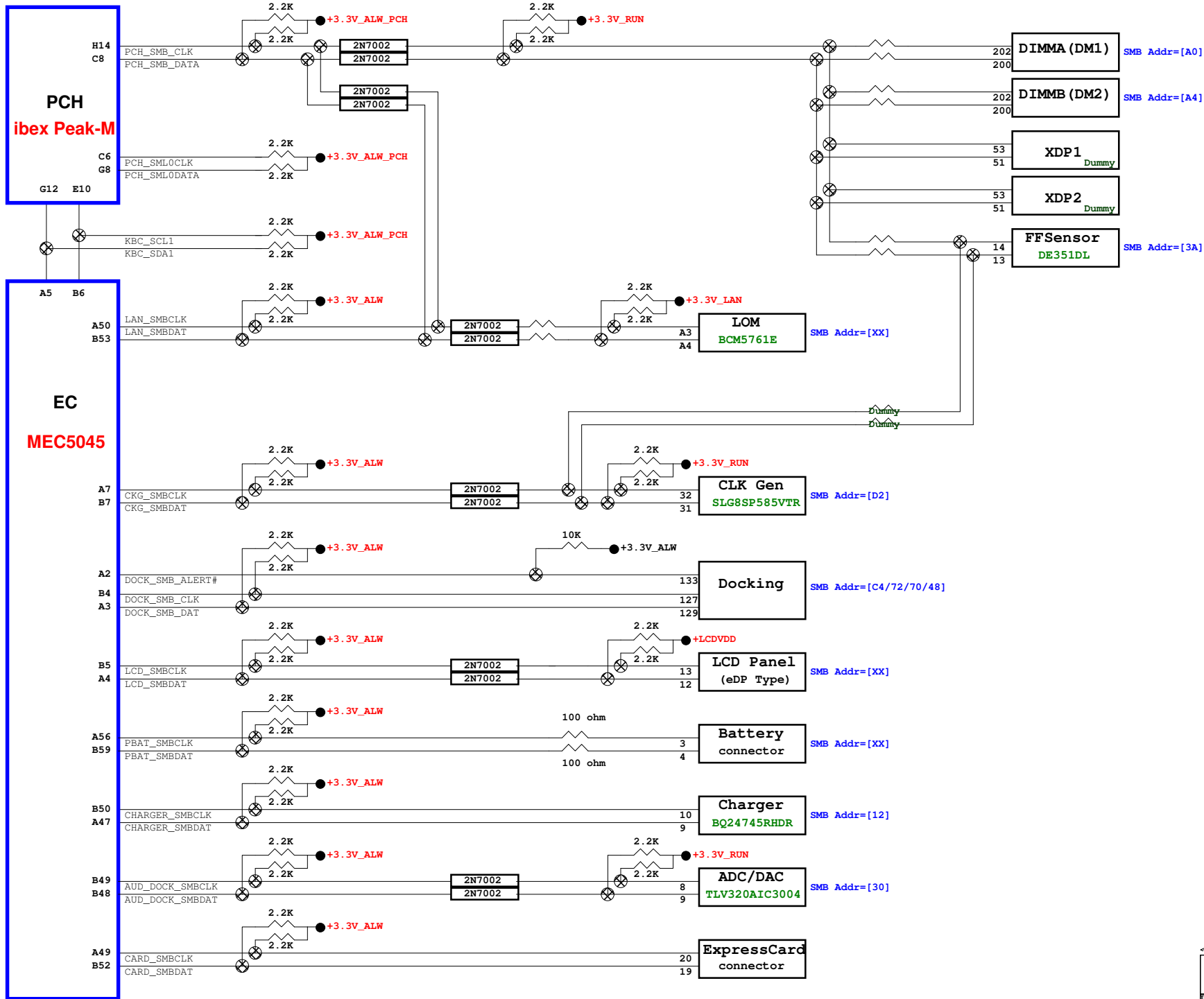
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Title			
Cover Page			
Size Custom	Document Number Fonseca 14.1" DIS		Rev X01
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Fonseca 14" DIS Block Diagram

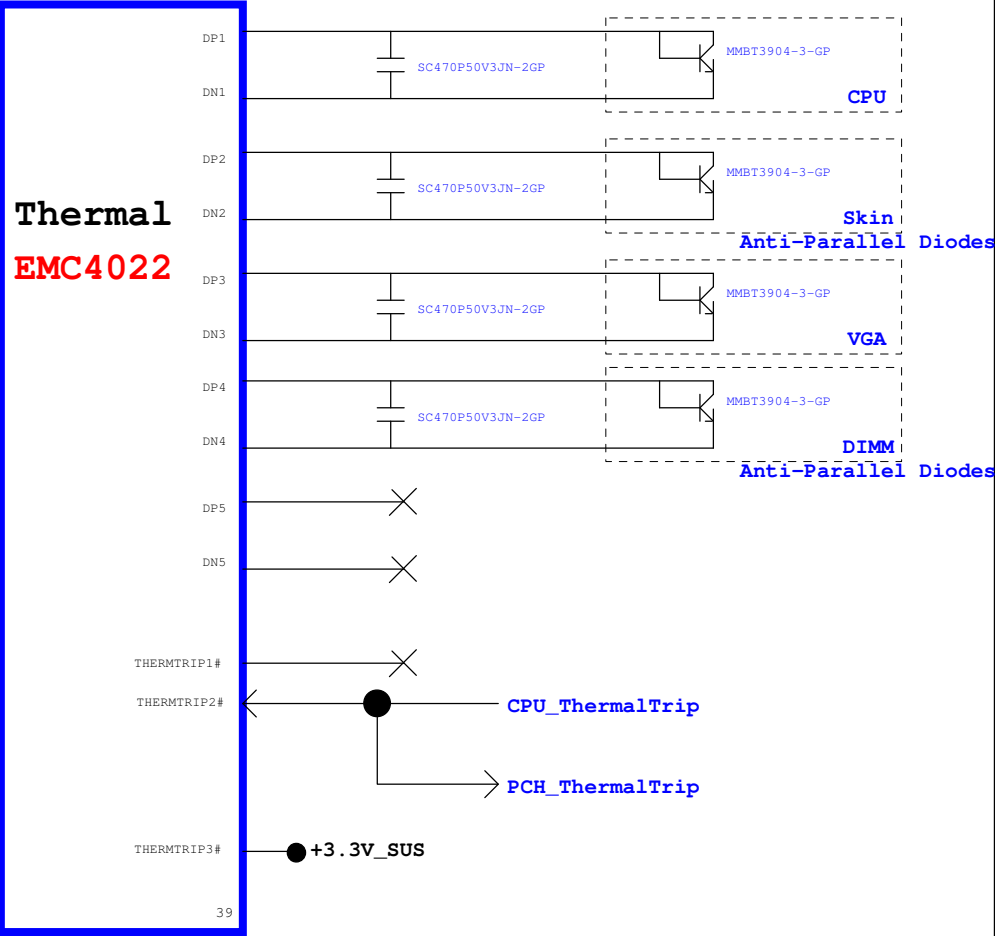
Project name: DF3-14D
Project code: 91.4GQ01.001
PCB P/N : 91.4GQ01.0SB
Revision : 09281 - SB



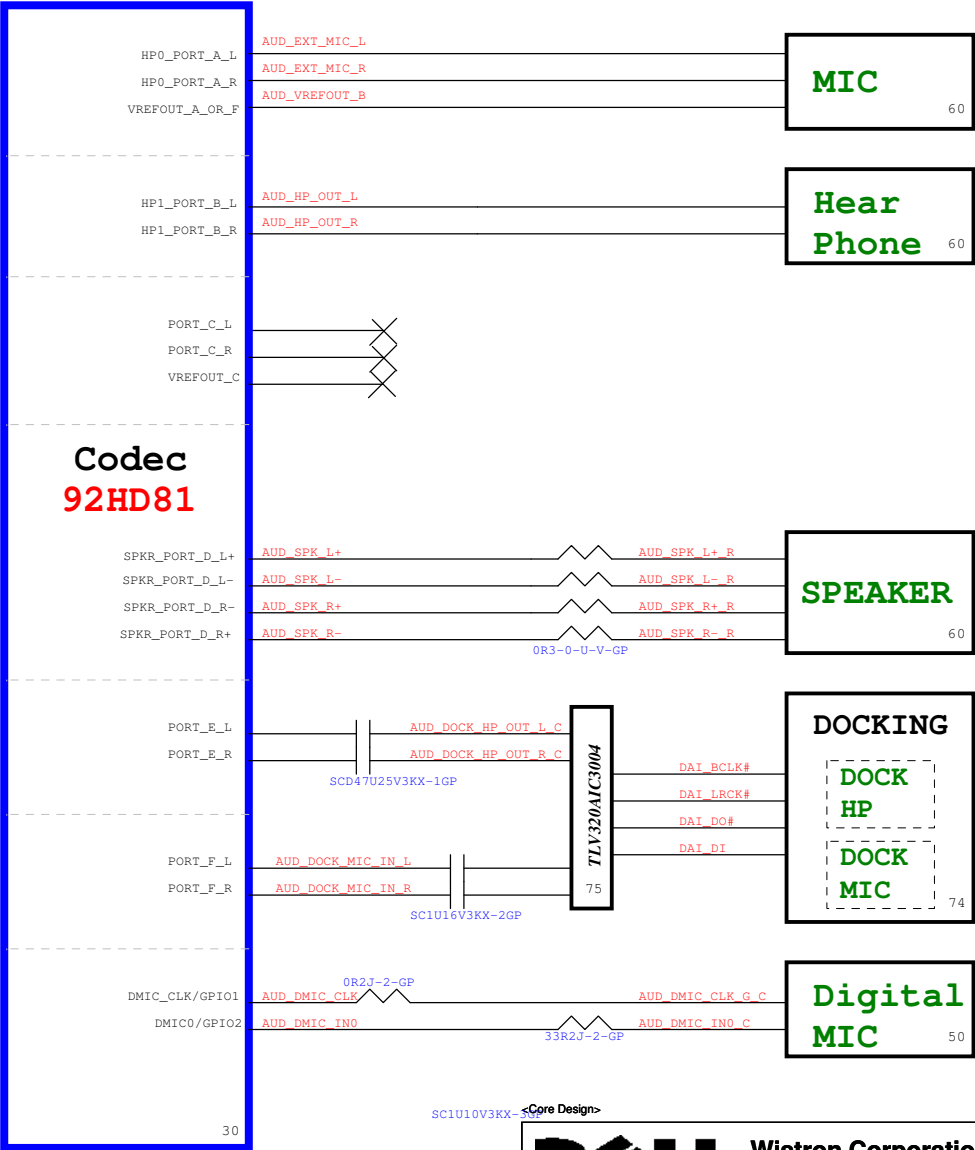




Thermal Block Diagram



Audio Block Diagram



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PCH Strapping

Calpella Schematic Checklist Rev: 1.6

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ ~ 10-kΩ weak pull-up resistor.
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ ; do not stuff resistor
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled Note: CRB uses a 330-k resistor.
GNT0#, GNT1#	Default (SPI): Leave both GNT0# and GNT1# floating. No pull up required Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	Enable Intel Anti-Theft Technology: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Intel Anti-Theft Technology: Left floating, no pull-down required.
NV_ALE	Enable Intel Anti-Theft Technology: Connect to +NVRAM_VCCQ with 8.2-kΩ weak pull-up resistor [CRB has it pulled up with 1-kΩ no-stuff resistor] Disable Intel Anti-Theft Technology: Leave floating (internal pull-down).
NV_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HDA_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1): Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note: This is an unmuxed signal. This signal has a weak internal pull-down of 20KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1K pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	Default = Do not connect (floating). Internal pull-up. High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev: 1.6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1

PCIE Routing

LANE1	WWAN
LANE2	WLAN
LANE3	PCMCIA
LANE4	Express Card
LANE5	None
LANE6	10M/100M/1G LAN
LANE7	Not available for HM55
LANE8	Not available for HM55

USB Routing

USB	
Pair	Device
0	USB0 @ MB
1	USB1 @ MB
2	USB2 @ IO Board
3	USB3 @ IO Board
4	WLAN
5	Bluetooth
6	Not available for HM55
7	Not available for HM55
8	DOCKING PORT1
9	DOCKING PORT2
10	Finger Printer
11	Camera
12	PCCard / SmartCard
13	WWAN

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Title

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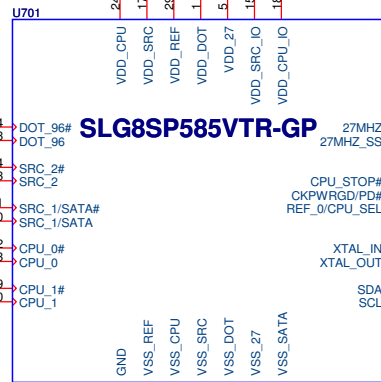
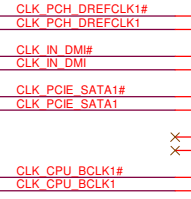
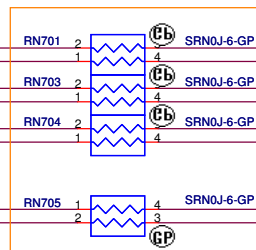
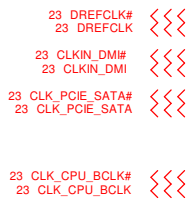
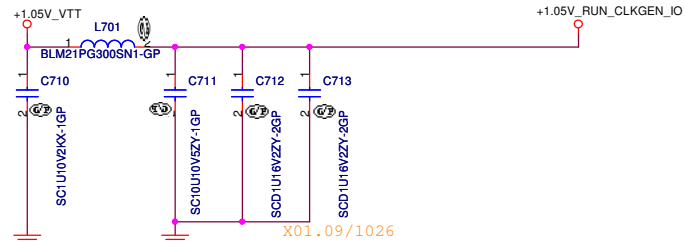
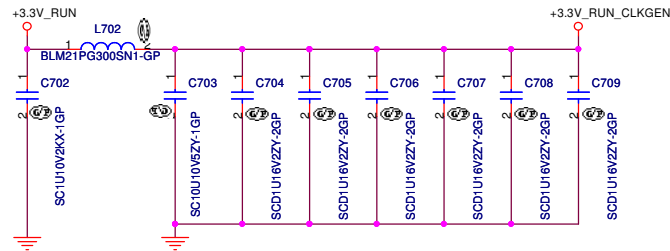
Fonseca 14.1" DIS

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X01

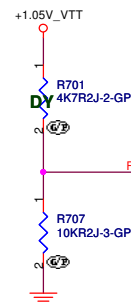
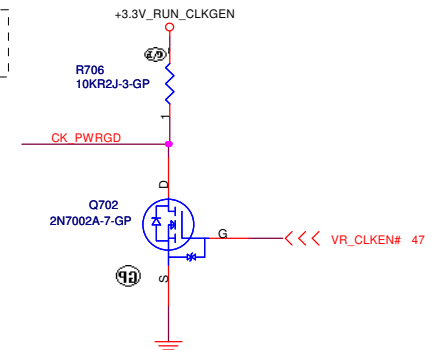
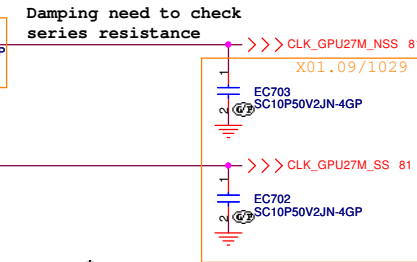
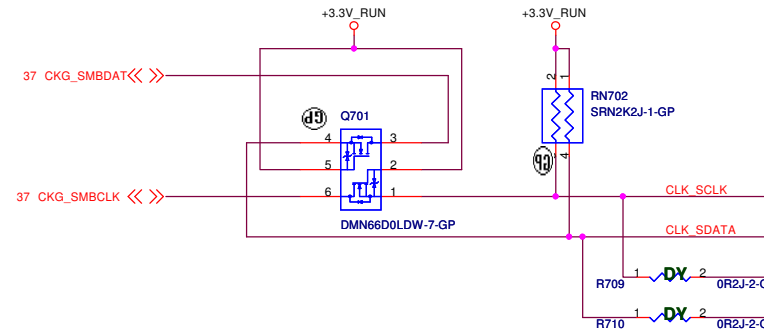
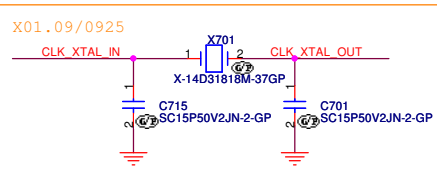
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SSID = CLOCK



Main Source: 71.08585.003 (SLG8SP585VTR)
2nd Source: 71.93197.003 (ICS9LRS3197AKLFT)
3rd Source: 71.00875.D03 (RIM875N-632-VB-GRT)



FSC	0	1
SPEED	133MHz (Default)	100MHz

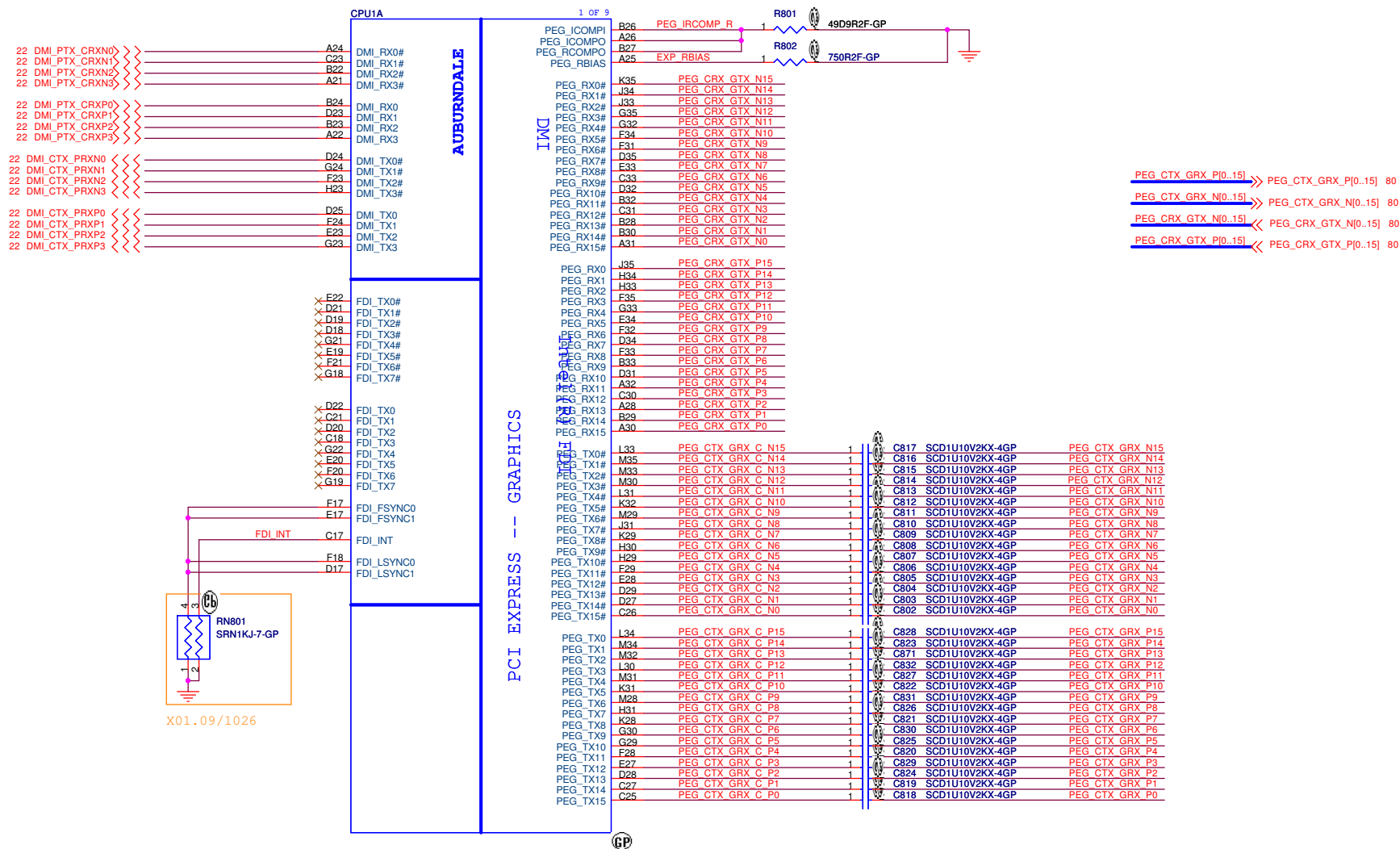
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Title: **Clock Generator - SLG8SP585**

Size A3 Document Number: **Fonseca 14.1" DIS** Rev: **X01**

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SSID = CPU⁵

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Title

CPU - PCIE/DMI/FDI (1/7)

Size

Document Number

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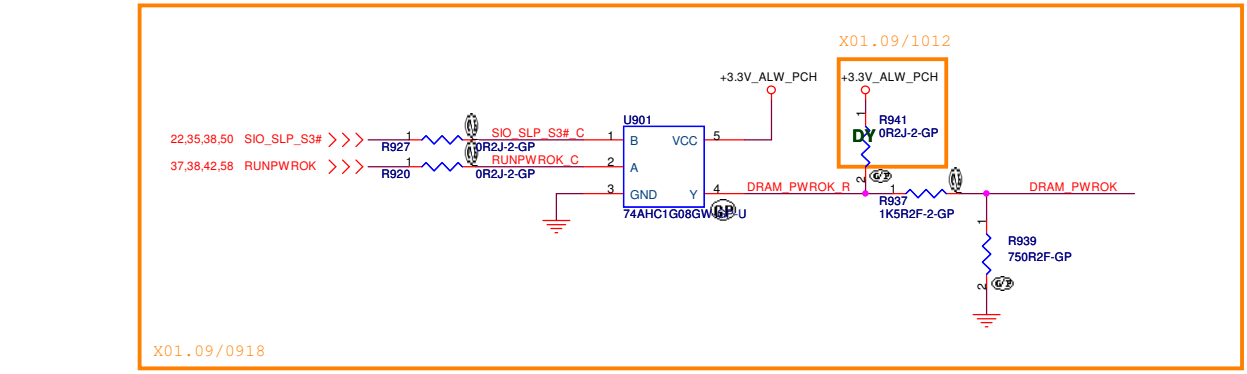
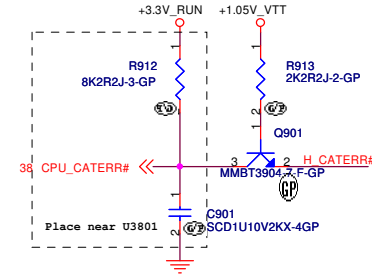
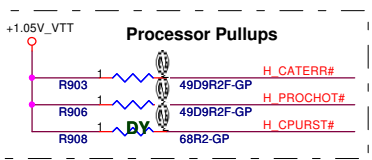
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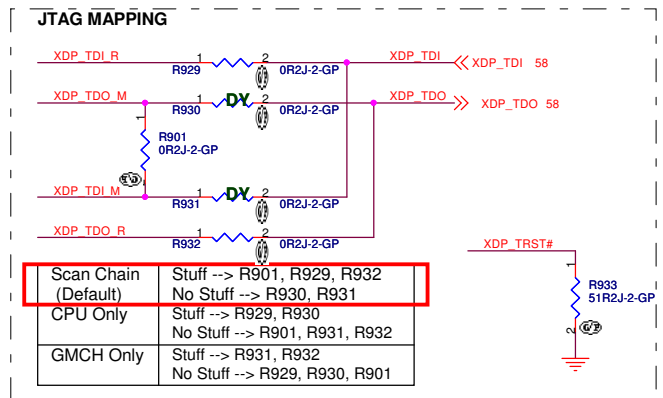
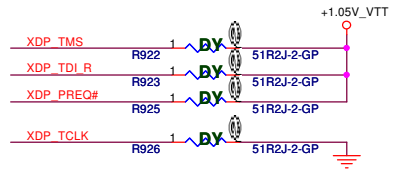
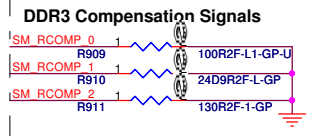
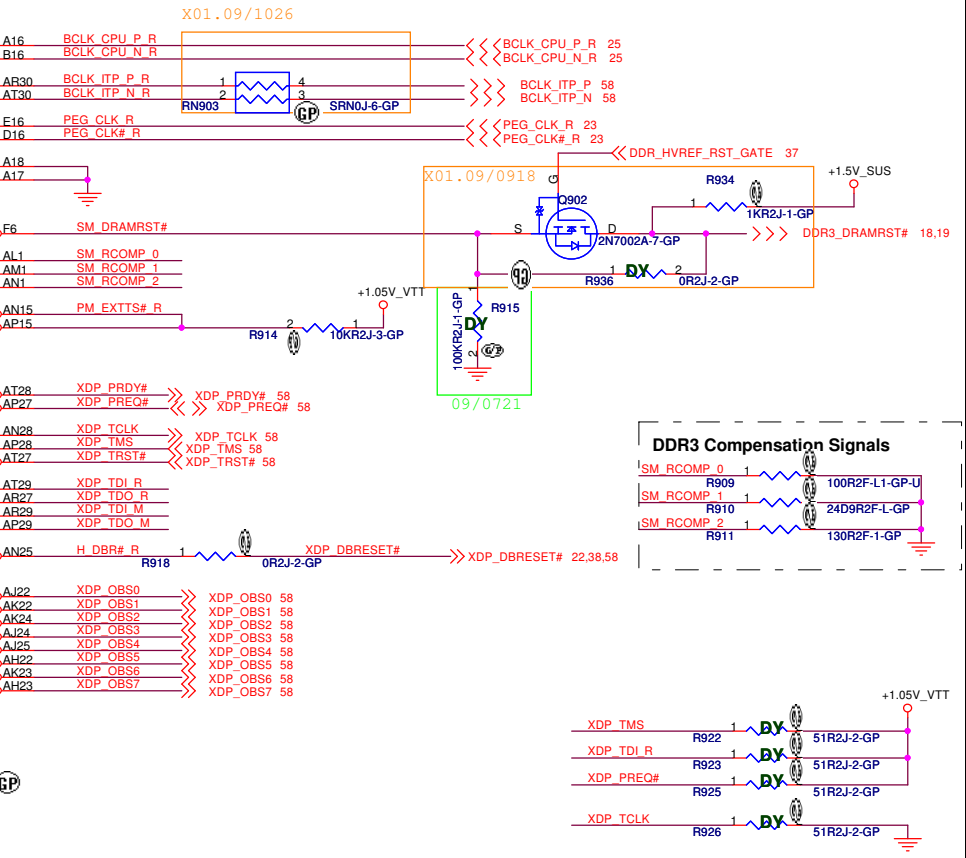
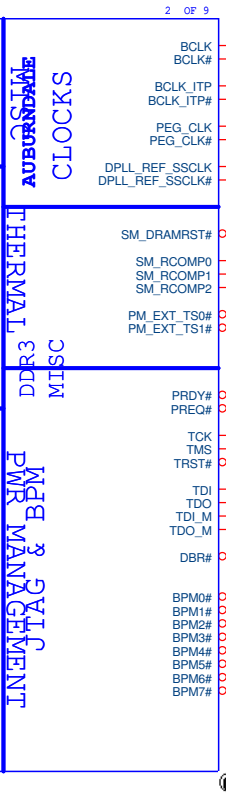
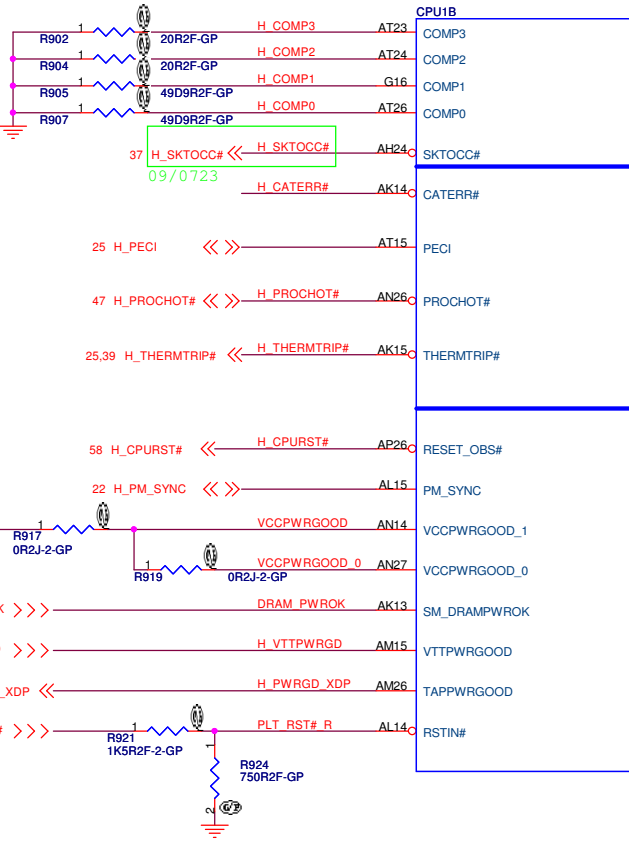
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SSID = CPU



Processor Compensation Signals



SSID = CPU

18 M_A_DQ[63..0] <<>>

M_A DQ0	A10	SA_DQ0
M_A DQ1	C10	SA_DQ1
M_A DQ2	G7	SA_DQ2
M_A DQ3	A7	SA_DQ3
M_A DQ4	B10	SA_DQ4
M_A DQ5	D10	SA_DQ5
M_A DQ6	E10	SA_DQ6
M_A DQ7	A8	SA_DQ7
M_A DQ8	D8	SA_DQ8
M_A DQ9	F10	SA_DQ9
M_A DQ10	E9	SA_DQ10
M_A DQ11	F7	SA_DQ11
M_A DQ12	E9	SA_DQ12
M_A DQ13	B7	SA_DQ13
M_A DQ14	E7	SA_DQ14
M_A DQ15	C6	SA_DQ15
M_A DQ16	H10	SA_DQ16
M_A DQ17	G8	SA_DQ17
M_A DQ18	K7	SA_DQ18
M_A DQ19	J8	SA_DQ19
M_A DQ20	G7	SA_DQ20
M_A DQ21	G10	SA_DQ21
M_A DQ22	I7	SA_DQ22
M_A DQ23	J10	SA_DQ23
M_A DQ24	L7	SA_DQ24
M_A DQ25	M6	SA_DQ25
M_A DQ26	M8	SA_DQ26
M_A DQ27	L9	SA_DQ27
M_A DQ28	L6	SA_DQ28
M_A DQ29	K8	SA_DQ29
M_A DQ30	N8	SA_DQ30
M_A DQ31	P9	SA_DQ31
M_A DQ32	AH5	SA_DQ32
M_A DQ33	AF5	SA_DQ33
M_A DQ34	AK6	SA_DQ34
M_A DQ35	AK7	SA_DQ35
M_A DQ36	AF6	SA_DQ36
M_A DQ37	AG5	SA_DQ37
M_A DQ38	AJ7	SA_DQ38
M_A DQ39	AJ6	SA_DQ39
M_A DQ40	AJ10	SA_DQ40
M_A DQ41	AJ9	SA_DQ41
M_A DQ42	AL10	SA_DQ42
M_A DQ43	AK12	SA_DQ43
M_A DQ44	AK8	SA_DQ44
M_A DQ45	AL7	SA_DQ45
M_A DQ46	AK11	SA_DQ46
M_A DQ47	AL8	SA_DQ47
M_A DQ48	AN8	SA_DQ48
M_A DQ49	AM10	SA_DQ49
M_A DQ50	AR11	SA_DQ50
M_A DQ51	AL11	SA_DQ51
M_A DQ52	AM9	SA_DQ52
M_A DQ53	AN9	SA_DQ53
M_A DQ54	AT11	SA_DQ54
M_A DQ55	AP12	SA_DQ55
M_A DQ56	AM12	SA_DQ56
M_A DQ57	AM12	SA_DQ57
M_A DQ58	AM13	SA_DQ58
M_A DQ59	AT14	SA_DQ59
M_A DQ60	AT12	SA_DQ60
M_A DQ61	AL13	SA_DQ61
M_A DQ62	AR14	SA_DQ62
M_A DQ63	AP14	SA_DQ63

18 M_A_BS0 <<>> AC3
18 M_A_BS1 <<>> AB2
18 M_A_BS2 <<>> U7

18 M_A_CAS# <<>> AE1C
18 M_A_RAS# <<>> AB3
18 M_A_WE# <<>> AE9

AUBURNDALE

DDR SYSTEM MEMORY A

SA_CK0 AA6
SA_CK0# AA7
SA_CKE0 P7

SA_CK1 Y6
SA_CK1# Y5
SA_CKE1 P6

SA_CS0# AE2
SA_CS1# AE8

SA_ODT0 AD8
SA_ODT1 AF9

SA_DM0 B9 M_A DM0
SA_DM1 D7 M_A DM1
SA_DM2 H7 M_A DM2
SA_DM3 LM7 M_A DM3
SA_DM4 AG6 M_A DM4
SA_DM5 AM7 M_A DM5
SA_DM6 AN10 M_A DM6
SA_DM7 AN13 M_A DM7

SA_DQS0# C9 M_A DQS#0
SA_DQS1# F8 M_A DQS#1
SA_DQS2# J9 M_A DQS#2
SA_DQS3# N9 M_A DQS#3
SA_DQS4# AH7 M_A DQS#4
SA_DQS5# AK9 M_A DQS#5
SA_DQS6# AP11 M_A DQS#6
SA_DQS7# AT13 M_A DQS#7

SA_DQS0 C8 M_A DQS0
SA_DQS1 F9 M_A DQS1
SA_DQS2 H9 M_A DQS2
SA_DQS3 M9 M_A DQS3
SA_DQS4 AH8 M_A DQS4
SA_DQS5 AK10 M_A DQS5
SA_DQS6 AN11 M_A DQS6
SA_DQS7 AR13 M_A DQS7

SA_MA0 Y3 M_A A0
SA_MA1 W1 M_A A1
SA_MA2 AA8 M_A A2
SA_MA3 AA3 M_A A3
SA_MA4 V1 M_A A4
SA_MA5 AA9 M_A A5
SA_MA6 V8 M_A A6
SA_MA7 T1 M_A A7
SA_MA8 Y9 M_A A8
SA_MA9 UB M_A A9
SA_MA10 AD4 M_A A10
SA_MA11 T2 M_A A11
SA_MA12 U3 M_A A12
SA_MA13 AG8 M_A A13
SA_MA14 T3 M_A A14
SA_MA15 V9 M_A A15



19 M_B_DQ[63..0] <<>>

M_B DQ0	B5	SB_DQ0
M_B DQ1	A5	SB_DQ1
M_B DQ2	C3	SB_DQ2
M_B DQ3	B3	SB_DQ3
M_B DQ4	E4	SB_DQ4
M_B DQ5	A6	SB_DQ5
M_B DQ6	A4	SB_DQ6
M_B DQ7	C4	SB_DQ7
M_B DQ8	D1	SB_DQ8
M_B DQ9	D2	SB_DQ9
M_B DQ10	F2	SB_DQ10
M_B DQ11	F1	SB_DQ11
M_B DQ12	C2	SB_DQ12
M_B DQ13	F5	SB_DQ13
M_B DQ14	F3	SB_DQ14
M_B DQ15	G4	SB_DQ15
M_B DQ16	H6	SB_DQ16
M_B DQ17	G2	SB_DQ17
M_B DQ18	J6	SB_DQ18
M_B DQ19	J3	SB_DQ19
M_B DQ20	G1	SB_DQ20
M_B DQ21	G5	SB_DQ21
M_B DQ22	J2	SB_DQ22
M_B DQ23	J1	SB_DQ23
M_B DQ24	J5	SB_DQ24
M_B DQ25	L3	SB_DQ25
M_B DQ26	L1	SB_DQ26
M_B DQ27	M1	SB_DQ27
M_B DQ28	K5	SB_DQ28
M_B DQ29	K4	SB_DQ29
M_B DQ30	M4	SB_DQ30
M_B DQ31	N5	SB_DQ31
M_B DQ32	AF3	SB_DQ32
M_B DQ33	AG1	SB_DQ33
M_B DQ34	AJ3	SB_DQ34
M_B DQ35	AK1	SB_DQ35
M_B DQ36	AG4	SB_DQ36
M_B DQ37	AG3	SB_DQ37
M_B DQ38	AJ4	SB_DQ38
M_B DQ39	AH4	SB_DQ39
M_B DQ40	AK3	SB_DQ40
M_B DQ41	AK4	SB_DQ41
M_B DQ42	AM6	SB_DQ42
M_B DQ43	AN2	SB_DQ43
M_B DQ44	AK5	SB_DQ44
M_B DQ45	AK2	SB_DQ45
M_B DQ46	AM4	SB_DQ46
M_B DQ47	AM3	SB_DQ47
M_B DQ48	AP3	SB_DQ48
M_B DQ49	AN5	SB_DQ49
M_B DQ50	AT4	SB_DQ50
M_B DQ51	AN6	SB_DQ51
M_B DQ52	AN4	SB_DQ52
M_B DQ53	AN3	SB_DQ53
M_B DQ54	AT5	SB_DQ54
M_B DQ55	AT6	SB_DQ55
M_B DQ56	AN7	SB_DQ56
M_B DQ57	AP6	SB_DQ57
M_B DQ58	AP8	SB_DQ58
M_B DQ59	AT9	SB_DQ59
M_B DQ60	AT7	SB_DQ60
M_B DQ61	AP9	SB_DQ61
M_B DQ62	AR10	SB_DQ62
M_B DQ63	AT10	SB_DQ63

19 M_B_BS0 <<>> AB1
19 M_B_BS1 <<>> W5
19 M_B_BS2 <<>> R7

19 M_B_CAS# <<>> AC5
19 M_B_RAS# <<>> Y7
19 M_B_WE# <<>> AC6

DDR SYSTEM MEMORY - B

CPU1D

SB_CK0 W8
SB_CK0# W9
SB_CKE0 M3

SB_CK1 V7
SB_CK1# V6
SB_CKE1 M2

SB_CS0# AB8
SB_CS1# AD6

SB_ODT0 AC7
SB_ODT1 AD1

SB_DM0 D4 M_B DM0
SB_DM1 E1 M_B DM1
SB_DM2 H3 M_B DM2
SB_DM3 AL1 M_B DM3
SB_DM4 AL2 M_B DM4
SB_DM5 AR4 M_B DM5
SB_DM6 AT8 M_B DM6
SB_DM7 M_B DM7

SB_DQS0# D5 M_B DQS#0
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SB_DQS7# AR8 M_B DQS#7

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SB_DQS5 AL5 M_B DQS5
SB_DQS6 AP5 M_B DQS6
SB_DQS7 AR7 M_B DQS7

SB_MA0 U5 M_B A0
SB_MA1 V2 M_B A1
SB_MA2 T5 M_B A2
SB_MA3 V3 M_B A3
SB_MA4 R1 M_B A4
SB_MA5 T8 M_B A5
SB_MA6 R2 M_B A6
SB_MA7 UB M_B A7
SB_MA8 R4 M_B A8
SB_MA9 R5 M_B A9
SB_MA10 AR5 M_B A10
SB_MA11 P3 M_B A11
SB_MA12 R3 M_B A12
SB_MA13 AE7 M_B A13
SB_MA14 P5 M_B A14
SB_MA15 N1 M_B A15

M_CLK_DDR2 19
M_CLK_DDR#2 19
M_CKE2 19

M_CLK_DDR3 19
M_CLK_DDR#3 19
M_CKE3 19

M_CS#2 19
M_CS#3 19

M_ODT2 19
M_ODT3 19

M_B_DM[7..0] 19
M_B_DQS[7..0] 19

M_B_DQS[7..0] 19
M_B_A[15..0] 19

<Core Design> GP



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Title

CPU - DDR (3/7)

Size A3

Document Number

Fonseca 14.1" DIS

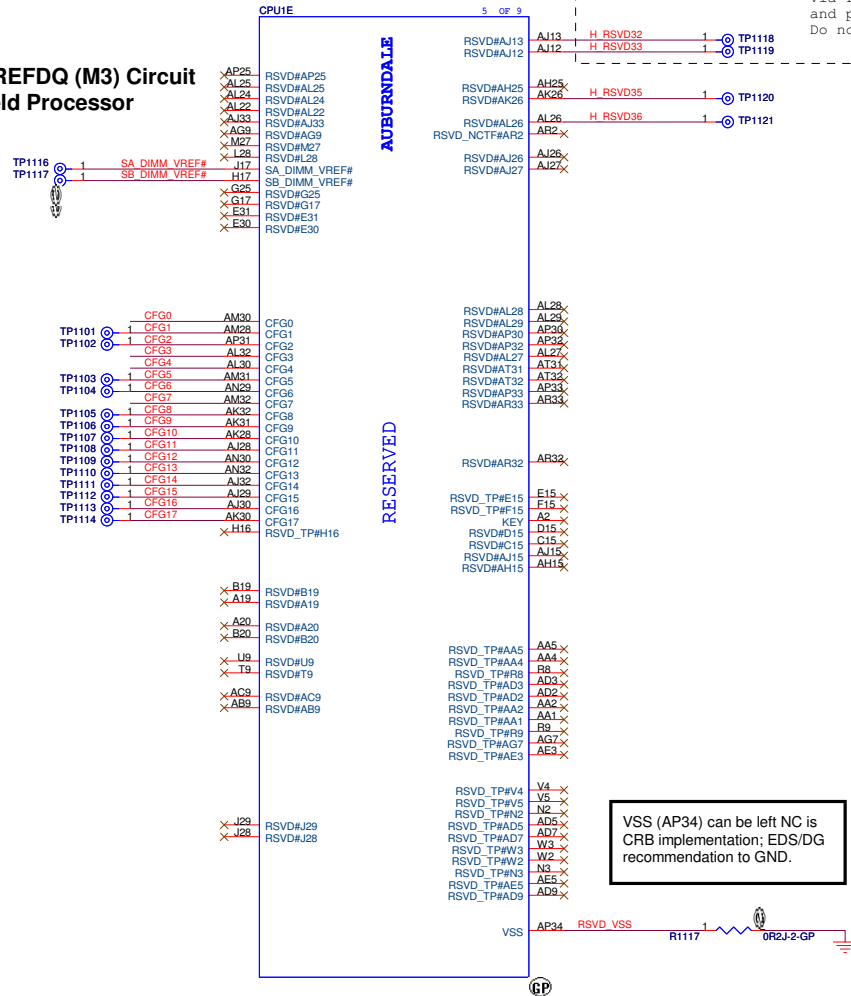
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SSID = CPU

SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor

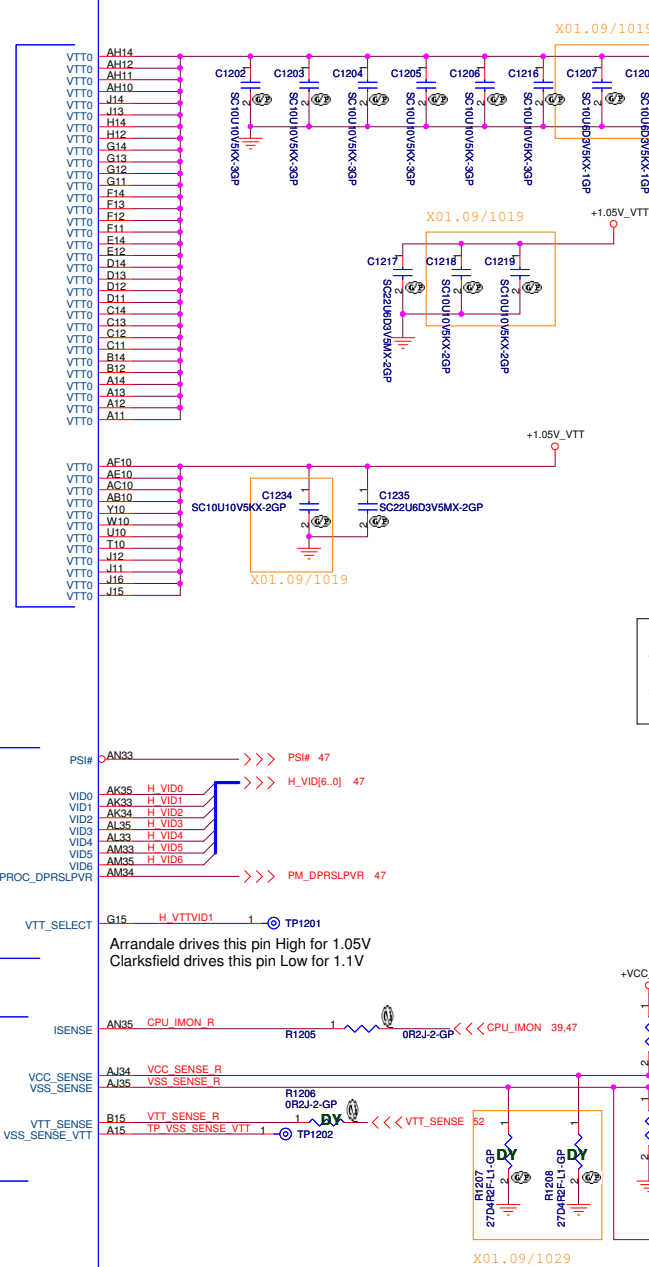
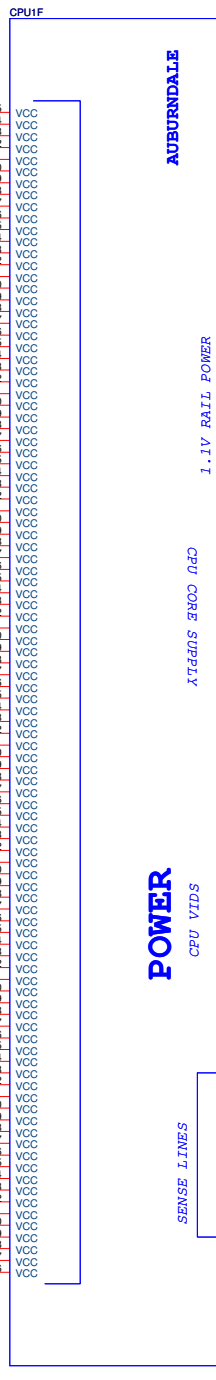
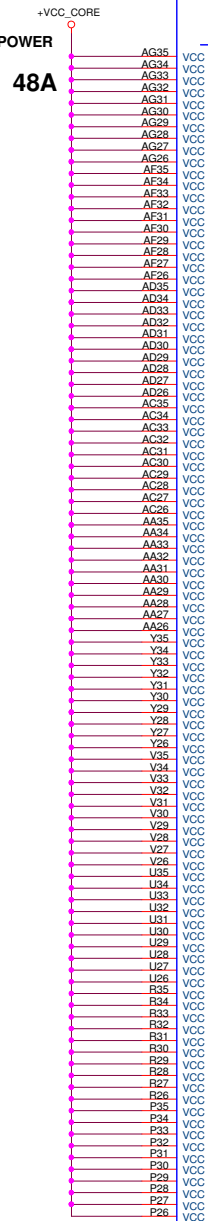
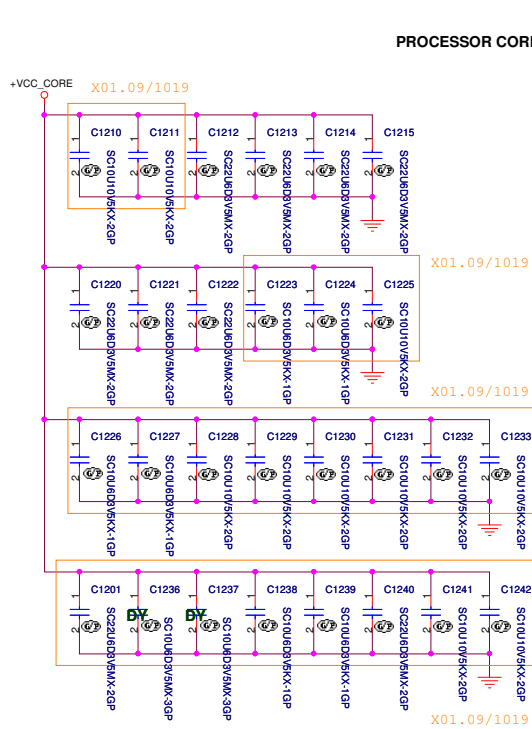


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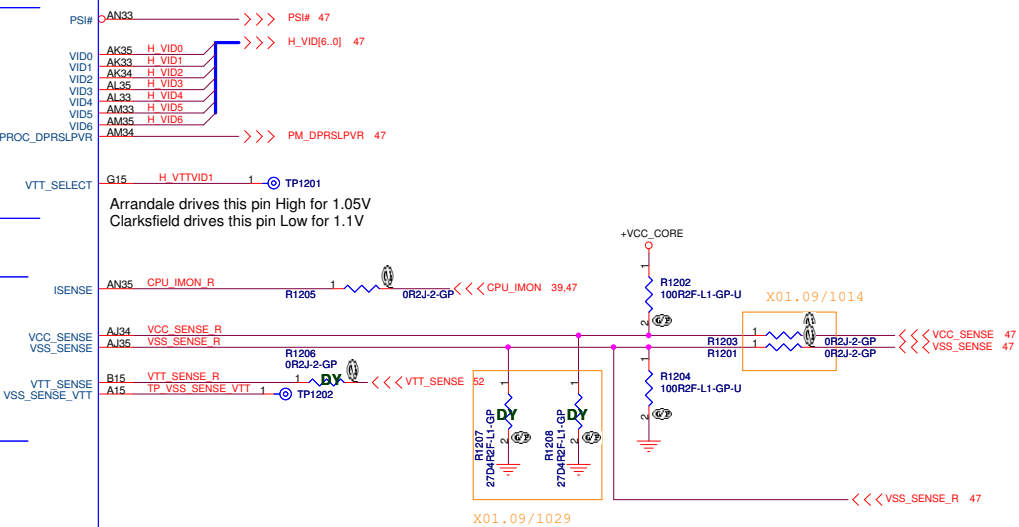
Title		CPU - Reserve (4/7)	
Size	Custom	Document Number	Fonseca 14.1" DIS
Date	Thursday, October 29, 2009	Sheet	11 of 92
Rev	X01		

SSID = CPU



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that
The VTT Rail values are
Arrandale for VTT=1.05V
Clarksfield for VTT=1.1V

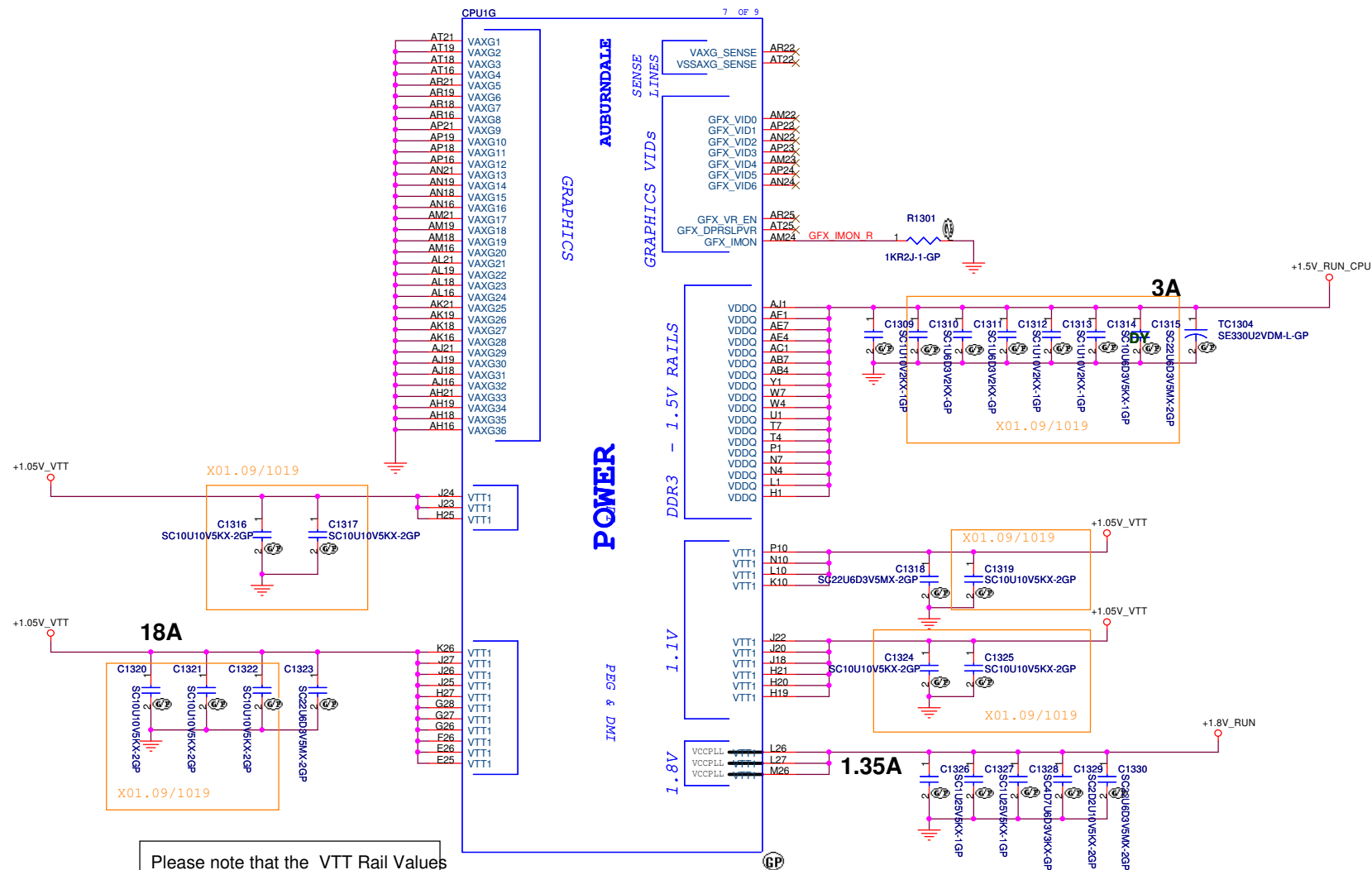


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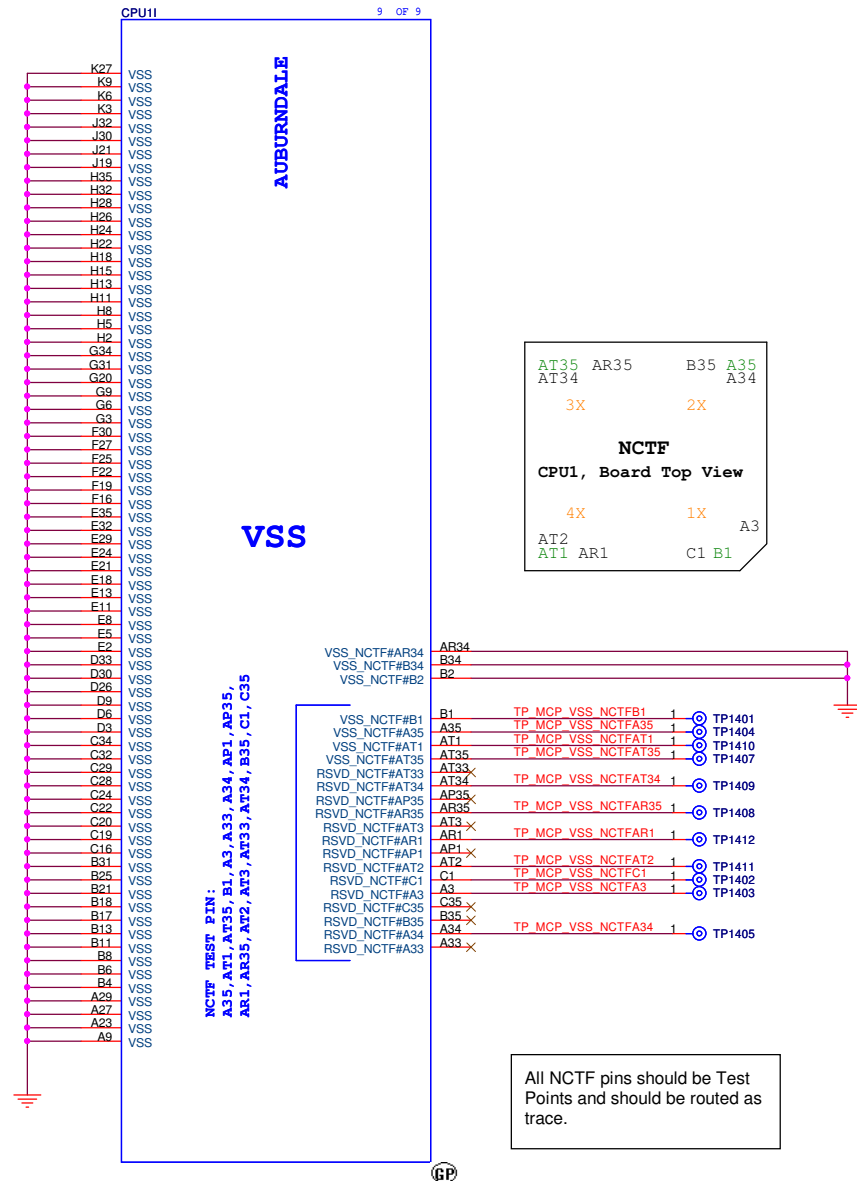
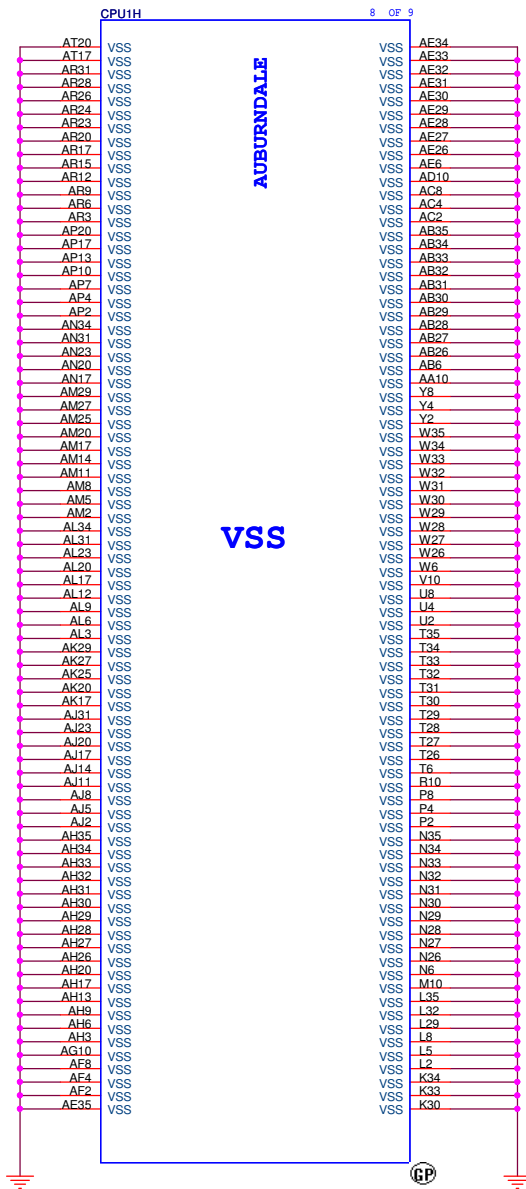
Title			
CPU - VCC_CORE (5/7)			
Size	Document Number	Rev	
Custom	Fonseca 14.1" DIS	X0	
Date: Thursday, October 29, 2009	Sheet 12	of 92	

SSID = CPU



Please note that the VTT Rail Values
Arrandale for VTT=1.05V
Clarksfield for VTT=1.1V

SSID = CPU



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<Core Design>



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Title

Size

Custom

Document Number

Rev

Reserve

Fonseca 14.1" DIS

X01

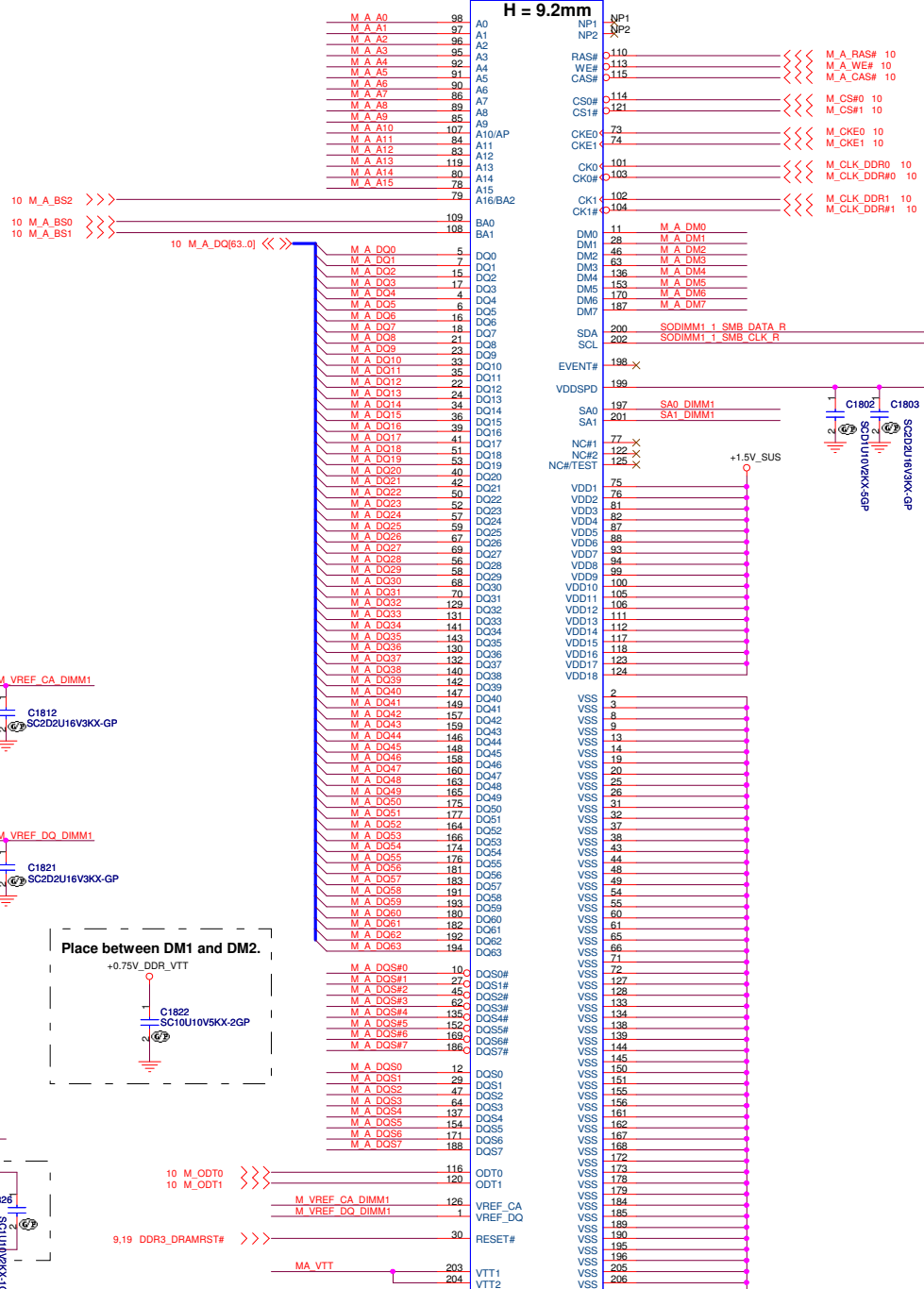
Date: Thursday, October 29, 2009

Sheet 16 of 92

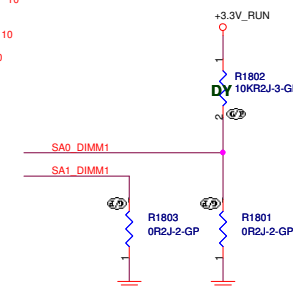
(Blank)

SSID = Memory

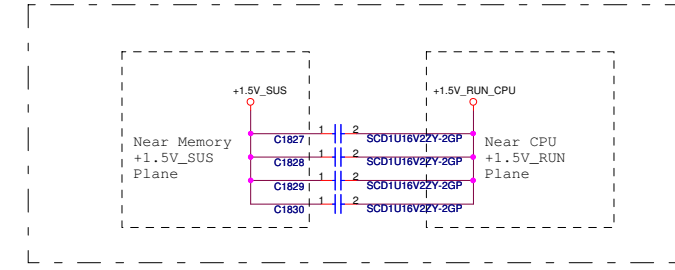
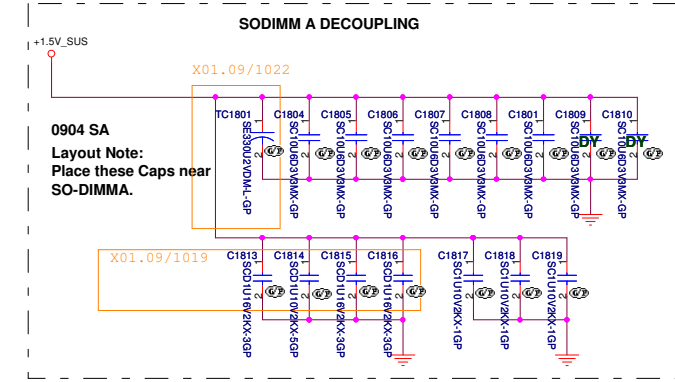
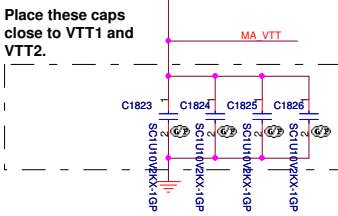
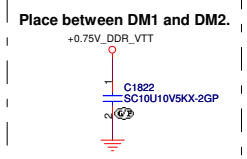
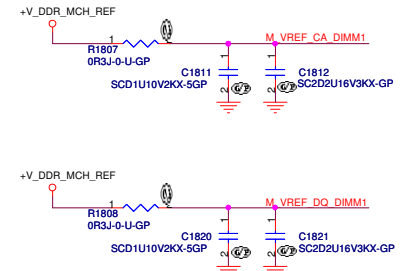
SO-DIMMA H = 9.2mm



M_A_DM[7..0] 10
 M_A_DQS[7..0] 10
 M_A_DQS[7..0] 10
 M_A_A[15..0] 10



Note:
 If SA0 DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30
 If SA0 DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32



62.10017.N61 DDR3-204P-42-GP

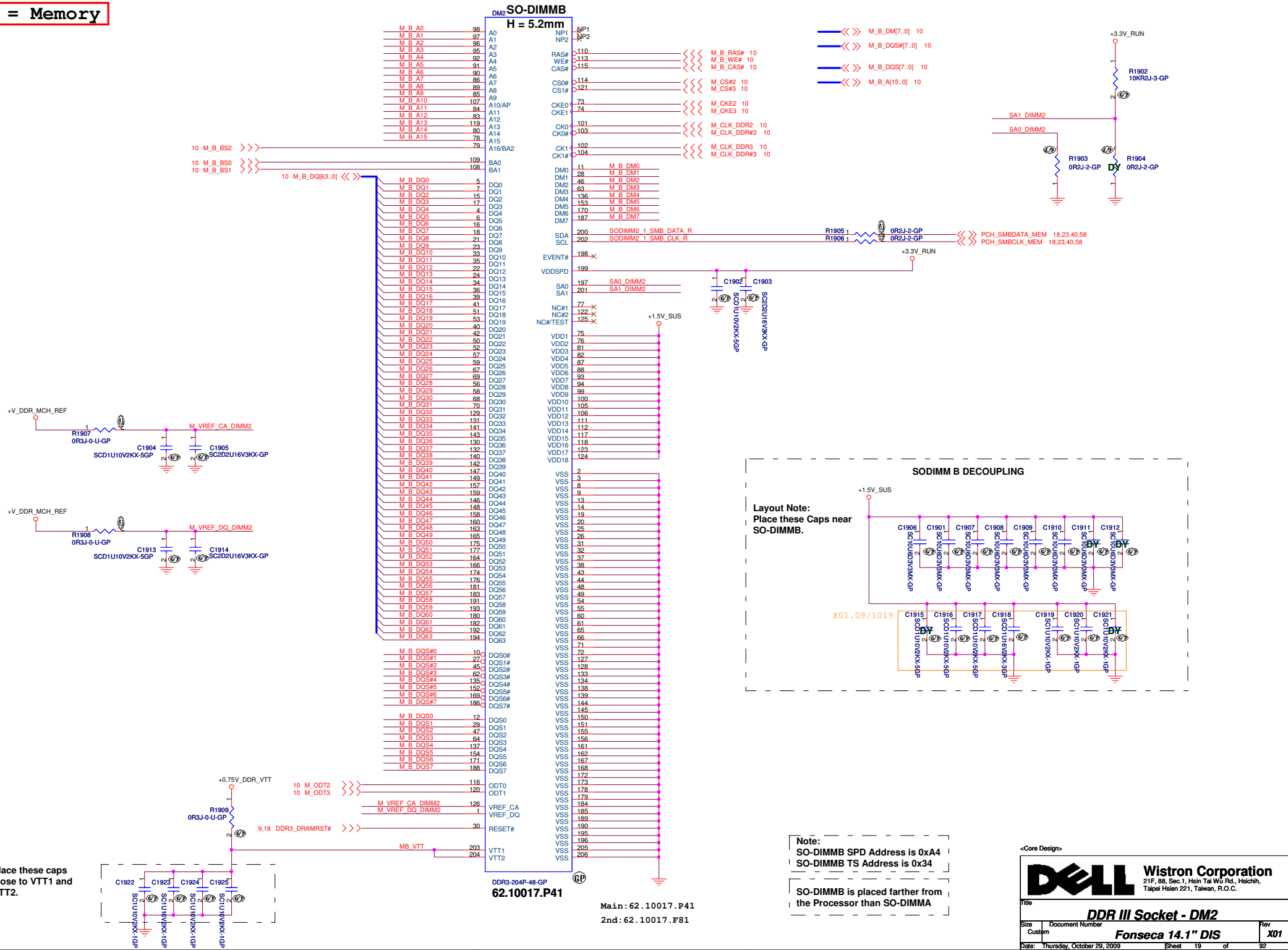
Main: 62.10017.N61
 2nd: 62.10017.F91

Dell Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

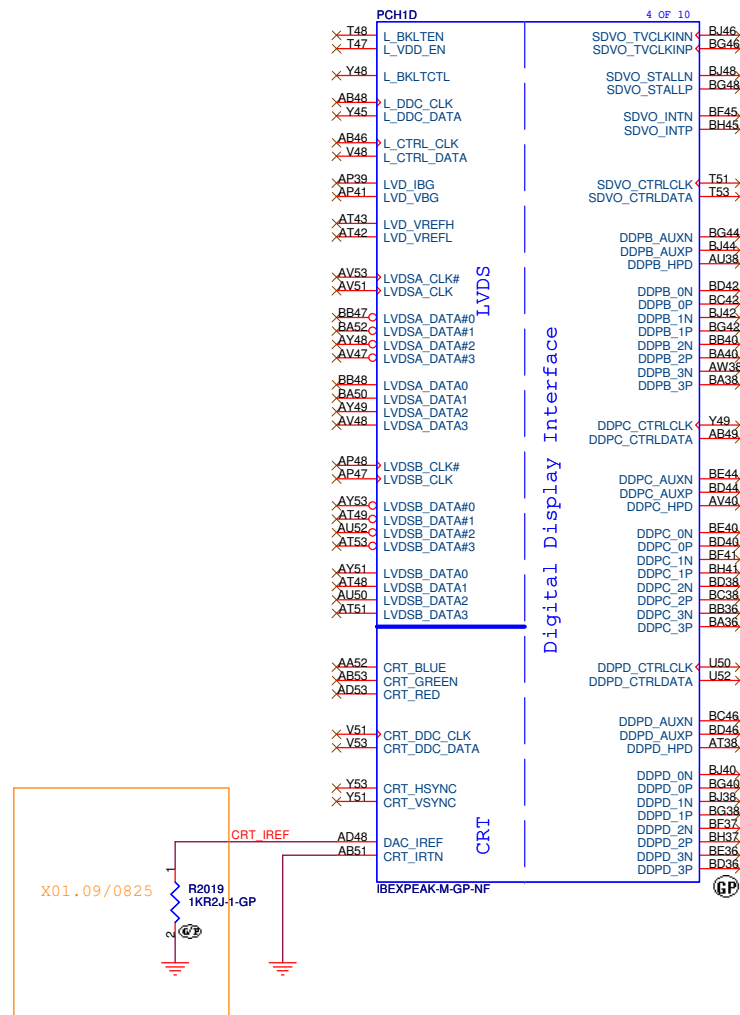
Title: **DDR III Socket - DM1**
 Size: Custom
 Date: Thursday, October 29, 2009
 Sheet: 18 of 92

Rev: X01
 Fonseca 14.1" DIS

SSID = Memory



SSID = PCH

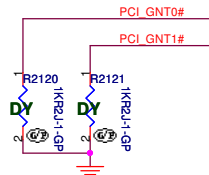
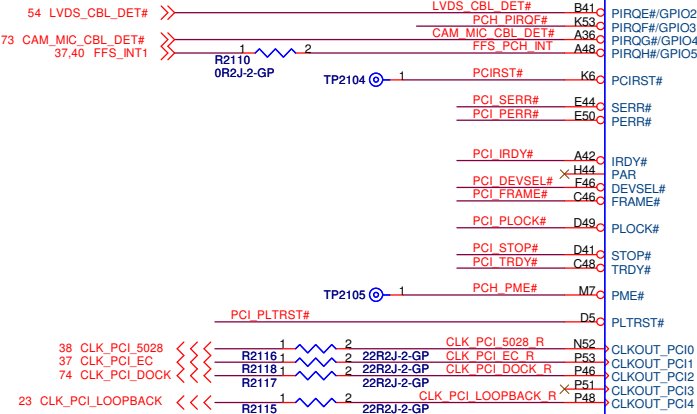
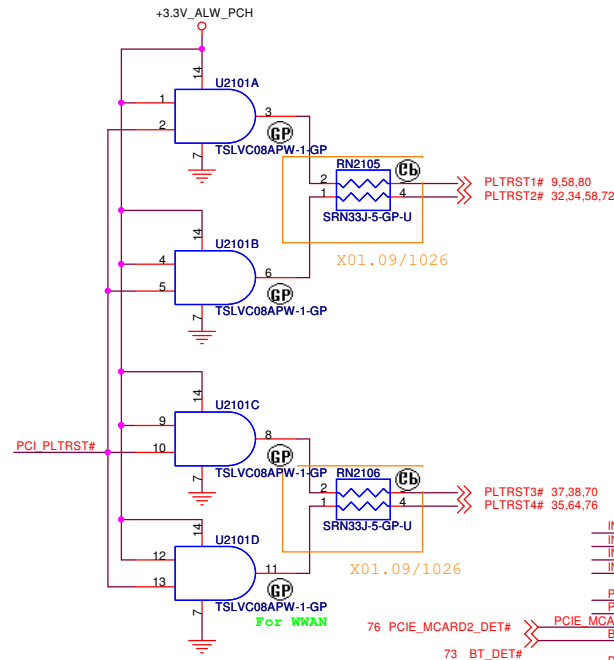
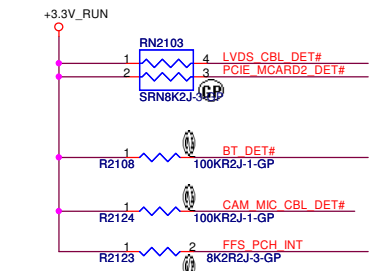
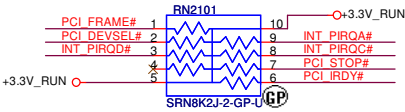
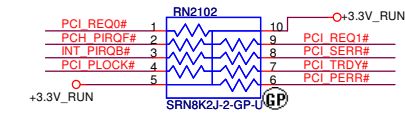


<Core Design>



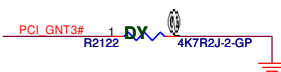
Title				PCH - LVDS/CRT/DDI (1/9)		Rev X01
Size A3	Document Number			Fonseca 14.1" DIS		
Date: Thursday, October 29, 2009			Sheet	20	of	92

SSID = PCH

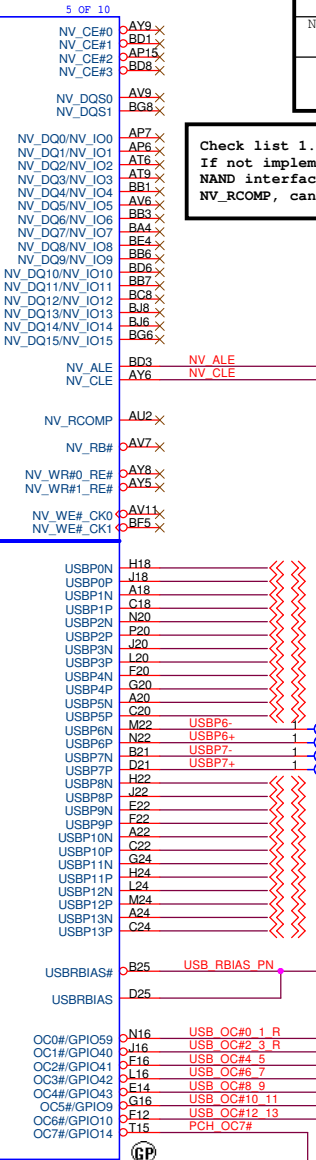
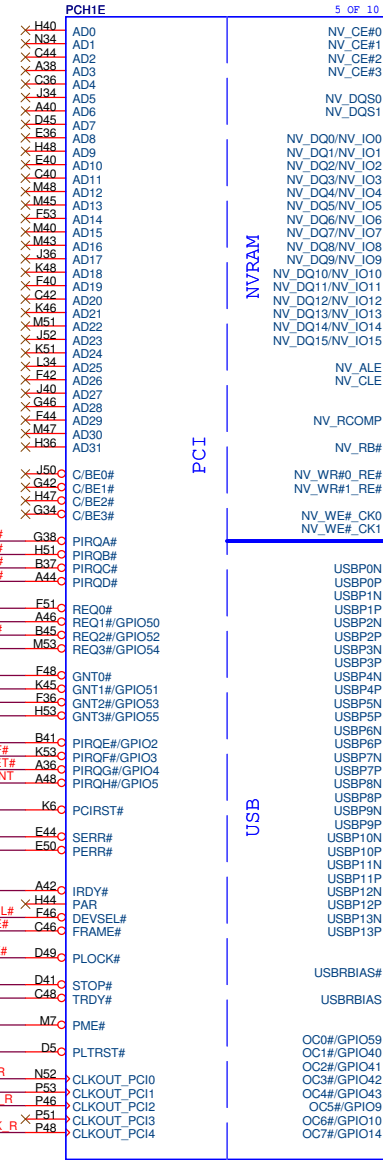


BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI(Default)

PCT_GNT[3:0]#: Internal pull high during Strap



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

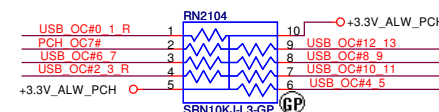
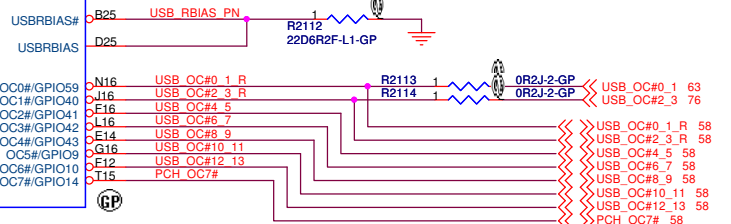


DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.
DMI termination voltage Weak internal pull-up Do not pull low	

Check list 1.6
If not implemented, the dual channel
NAND interface signals, including
NV_RCOMP, can be left as No Connect

Danbury Technology:
Disabled when Low.
Enable when High.

USB	
Pair	Device
0	USB0 @ MB (Charger)
1	USB1 @ MB
2	USB2 @ IO Board
3	USB3 @ IO Board
4	WLAN
5	Bluetooth
6	Not available for HM55
7	Not available for HM55
8	DOCK1
9	DOCK2
10	Finger Printer
11	Camera
12	PCCard/SmartCard/ExpCard
13	WWAN



<Core Design>



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Title

PCH - PCI/USB/NVRAM (2/9)

Size

Size	Document Number
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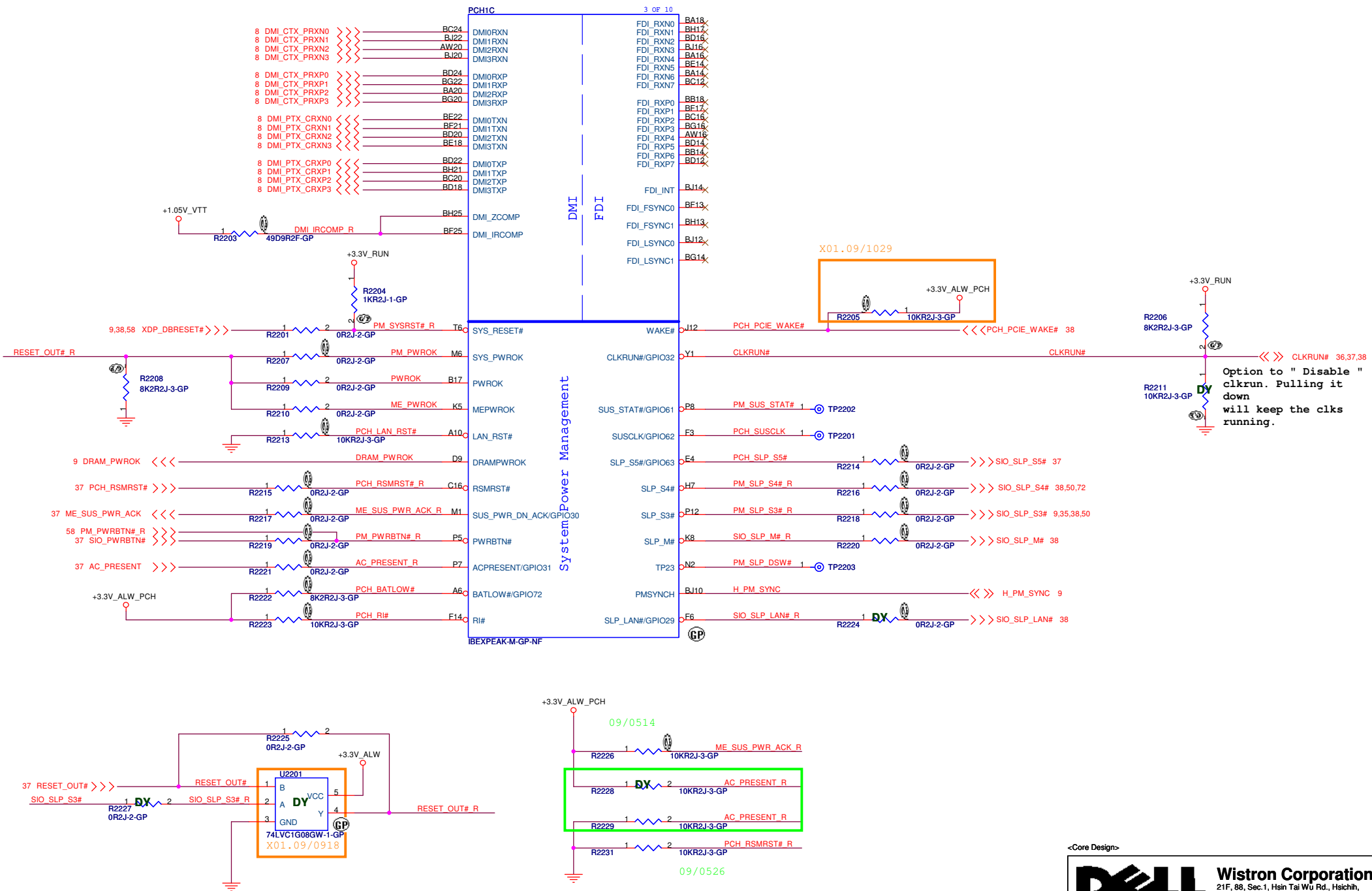
OF, COB/NVTAM

A3

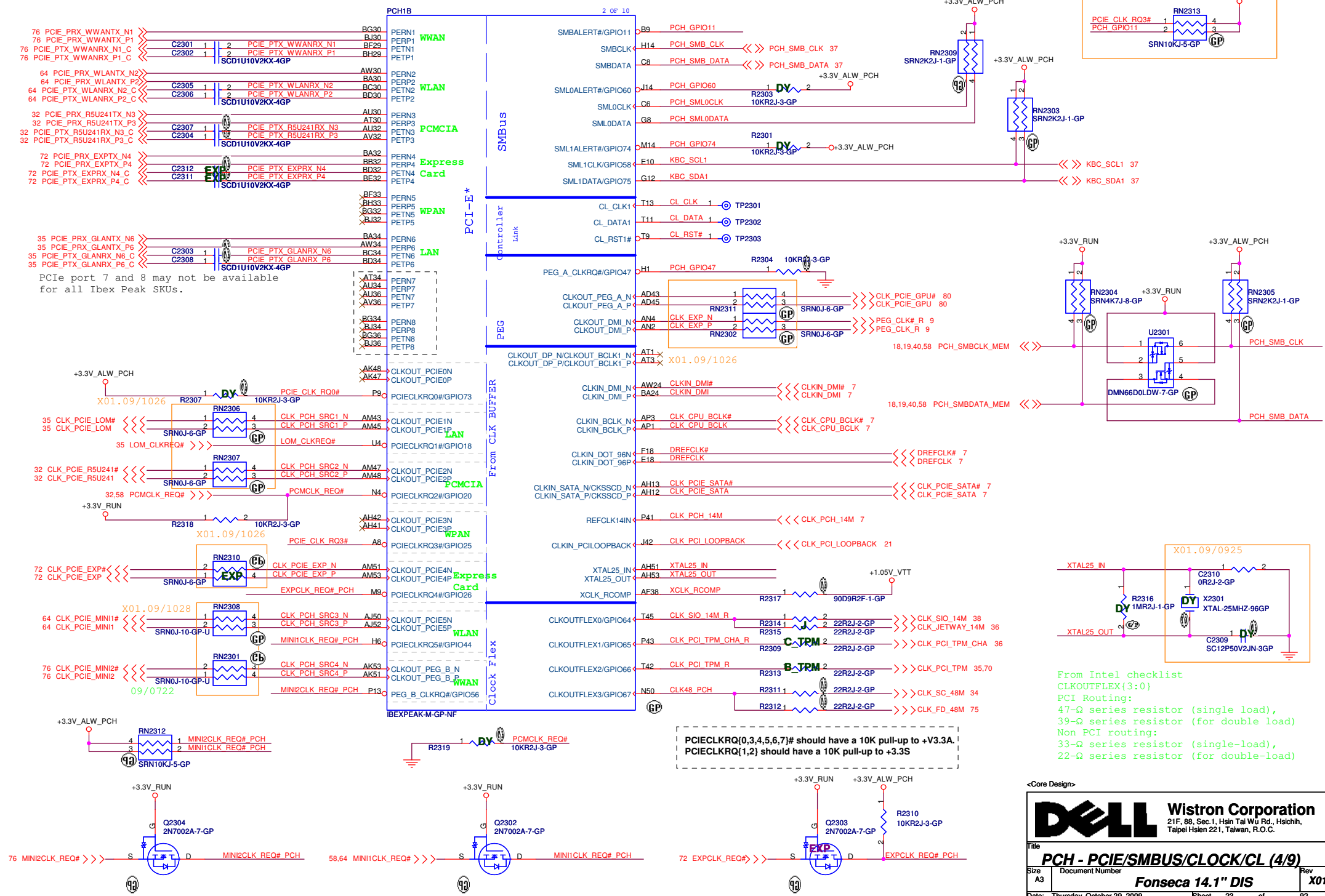
14 1" DIS

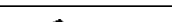
14.1 DIS

SSID = PCH

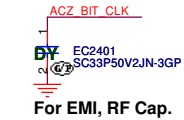
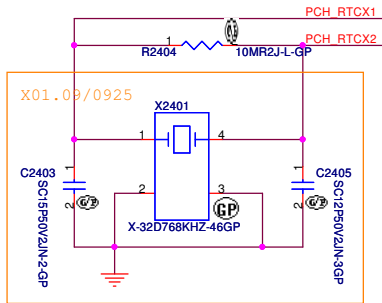


SSID = PCH

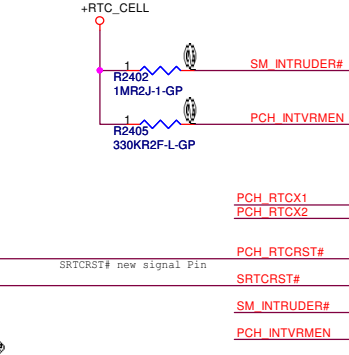
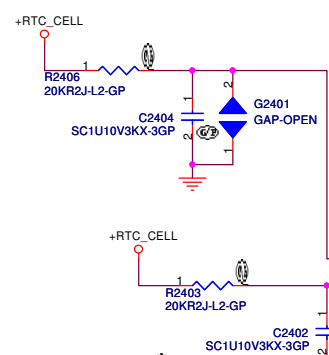


<Core Design>			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
PCH - PCIE/SMBUS/CLOCK/CL (4/9)			
Size	Document Number		Rev
A3		Fonseca 14.1" DIS	X01
Date:	Thursday, October 29, 2009	Sheet	23 of 92

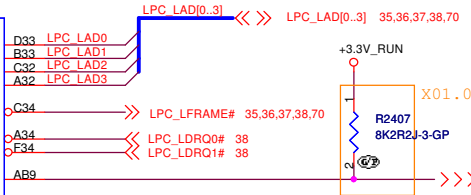
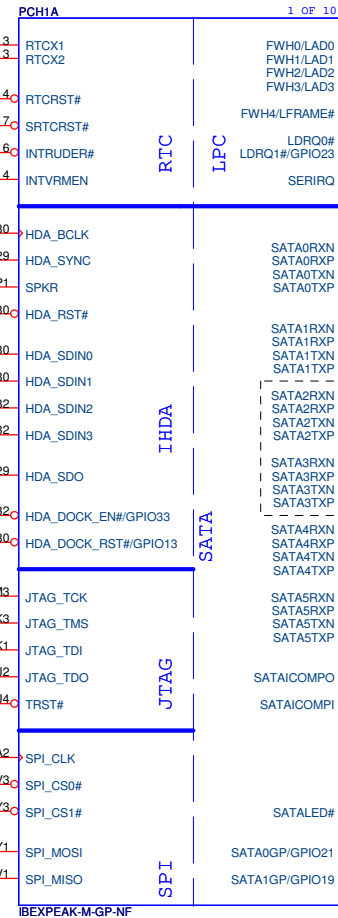
SSID = PCH



76 PCH_AZ_MDC_BITCLK
30 PCH_AZ_CODEC_BITCLK
76 PCH_AZ_MDC_SYNC
30 PCH_AZ_CODEC_SYNC
76 PCH_AZ_MDC_RST#
30,75 PCH_AZ_CODEC_RST#
76 PCH_MDC_SDOUT
30 PCH_CODEC_SDOUT



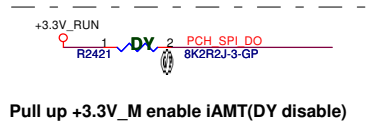
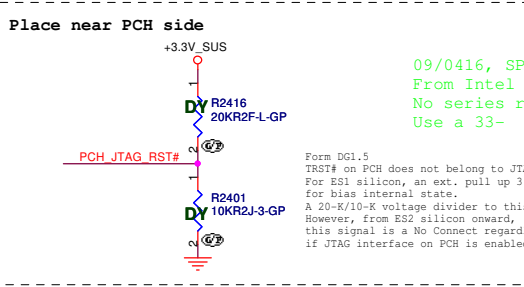
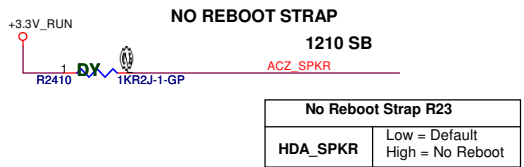
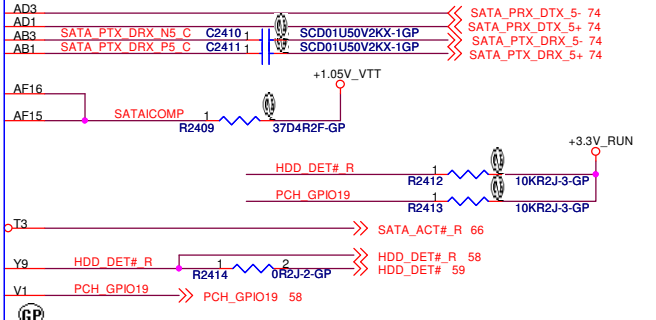
INTVRMEN- Integrated SUS
1.1V VRM Enable
High - Enable internal VRs



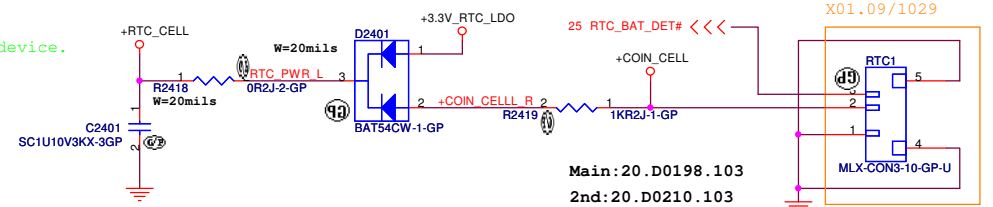
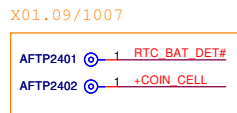
HDD
SATA_PRX_HTX0- 59
SATA_PRX_HTX0+ 59
SATA_PRX_HTX0- 59
SATA_PRX_HTX0+ 59
SATA_PRX_OTX1- 59
SATA_PRX_OTX1+ 59
SATA_PRX_OTX1- 59
SATA_PRX_OTX1+ 59
SATA_PRX_OTX1- 59
SATA_PRX_OTX1+ 59

SATA port 2 and 3 may not be available
for all Ibex Peak SKUs.

DOCKING eSATA



09/0416, SPI_MISO
From Intel qchecklist,
No series resistor required if routing length is 1.5"-6.5" if using 1 SPI device.
Use a 33- series resistors close to them PCH if using 2 SPI devices.



integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

<Core Design>

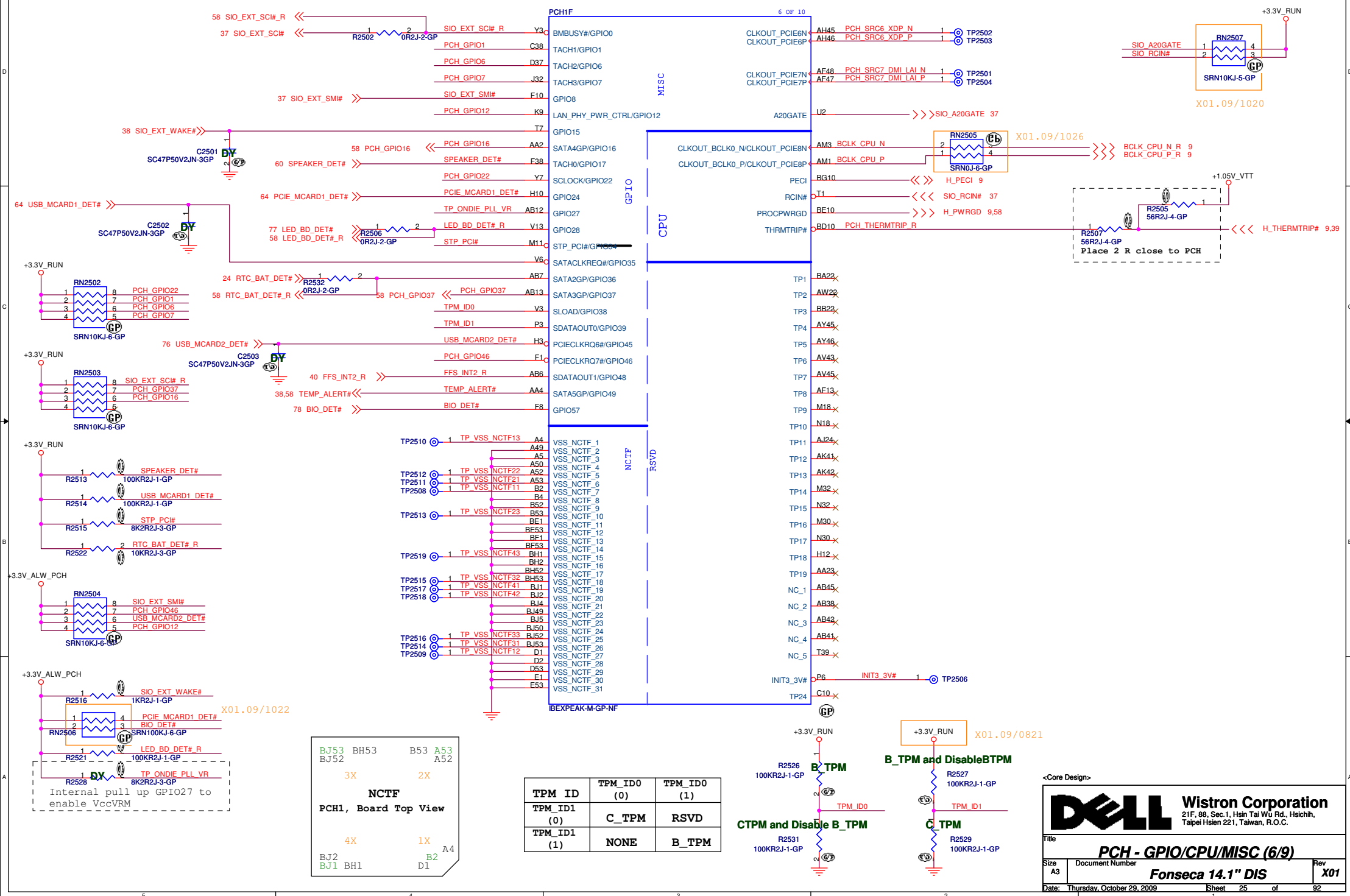
DELL Wistron Corporation
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Title: **PCH - SPI/RTC/LPC/SATA/IHDA (5/9)**

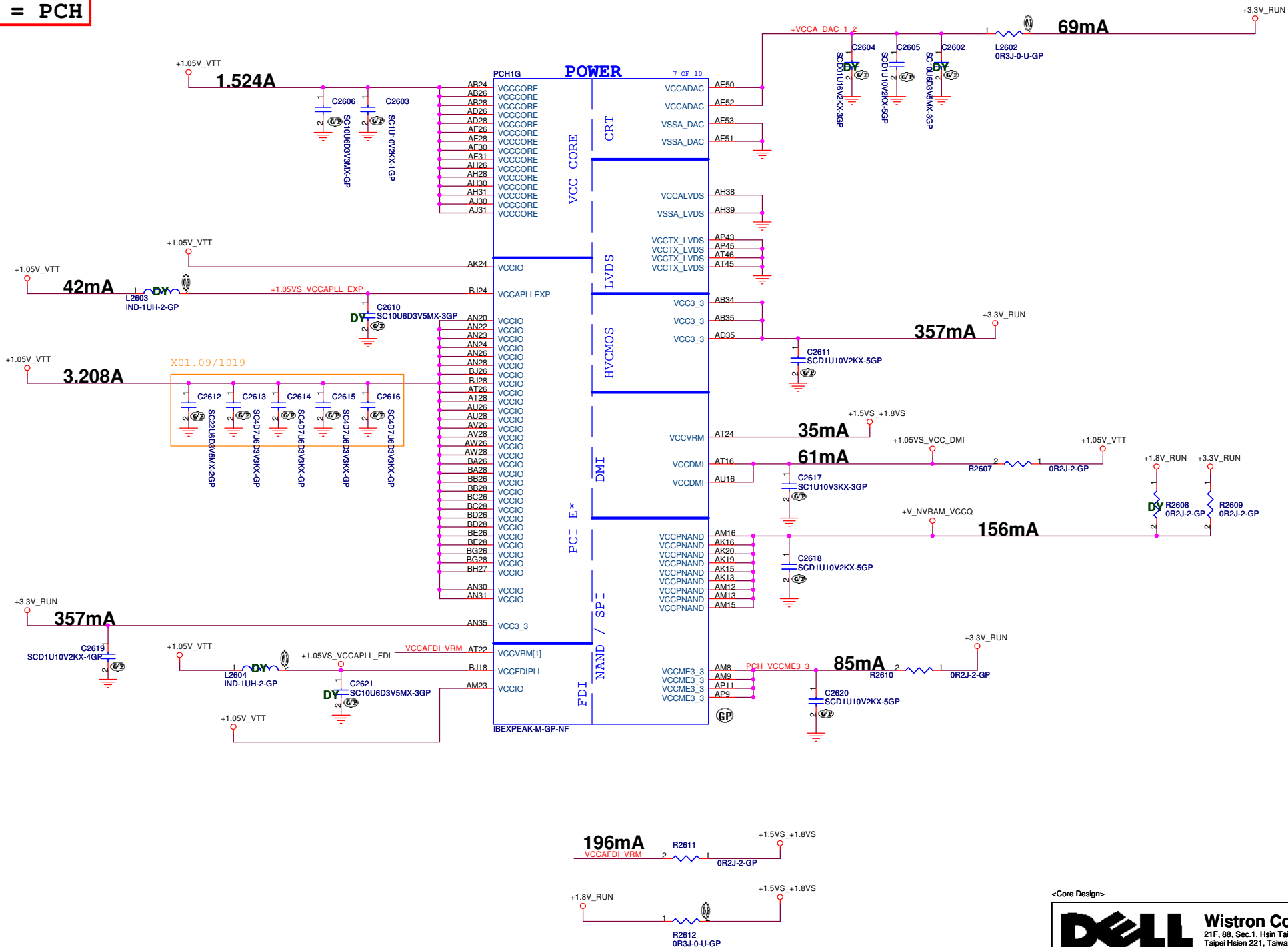
Size: A3 Document Number: **Fonseca 14.1" DIS** Rev: **X01**

Date: Thursday, October 29, 2009 Sheet 24 of 92

SSID = PCH



SSID = PCH



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Title

PCH (7/9)

Size
A3

Document Number

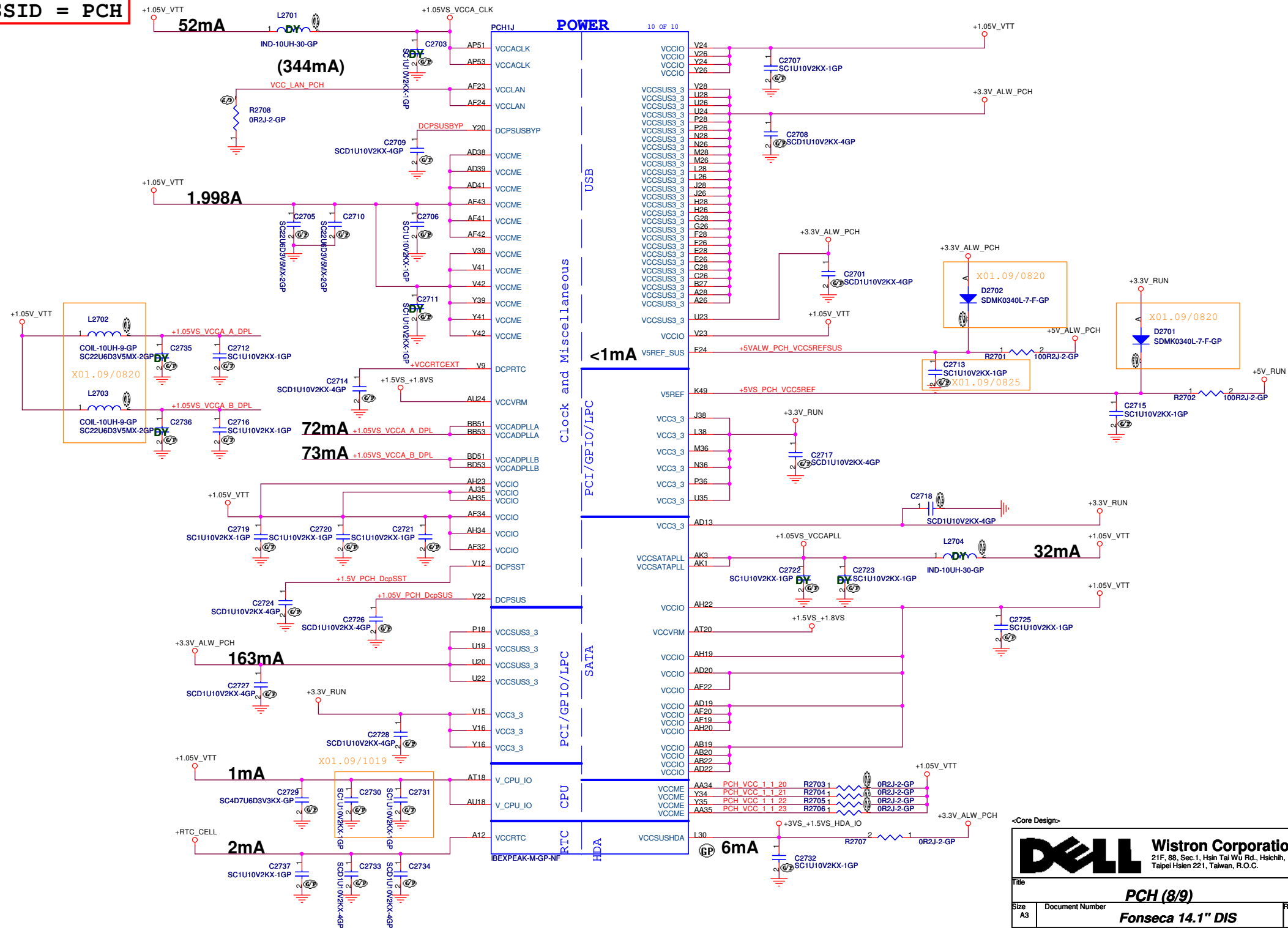
Fonseca 14.1" DIS

Rev
X01

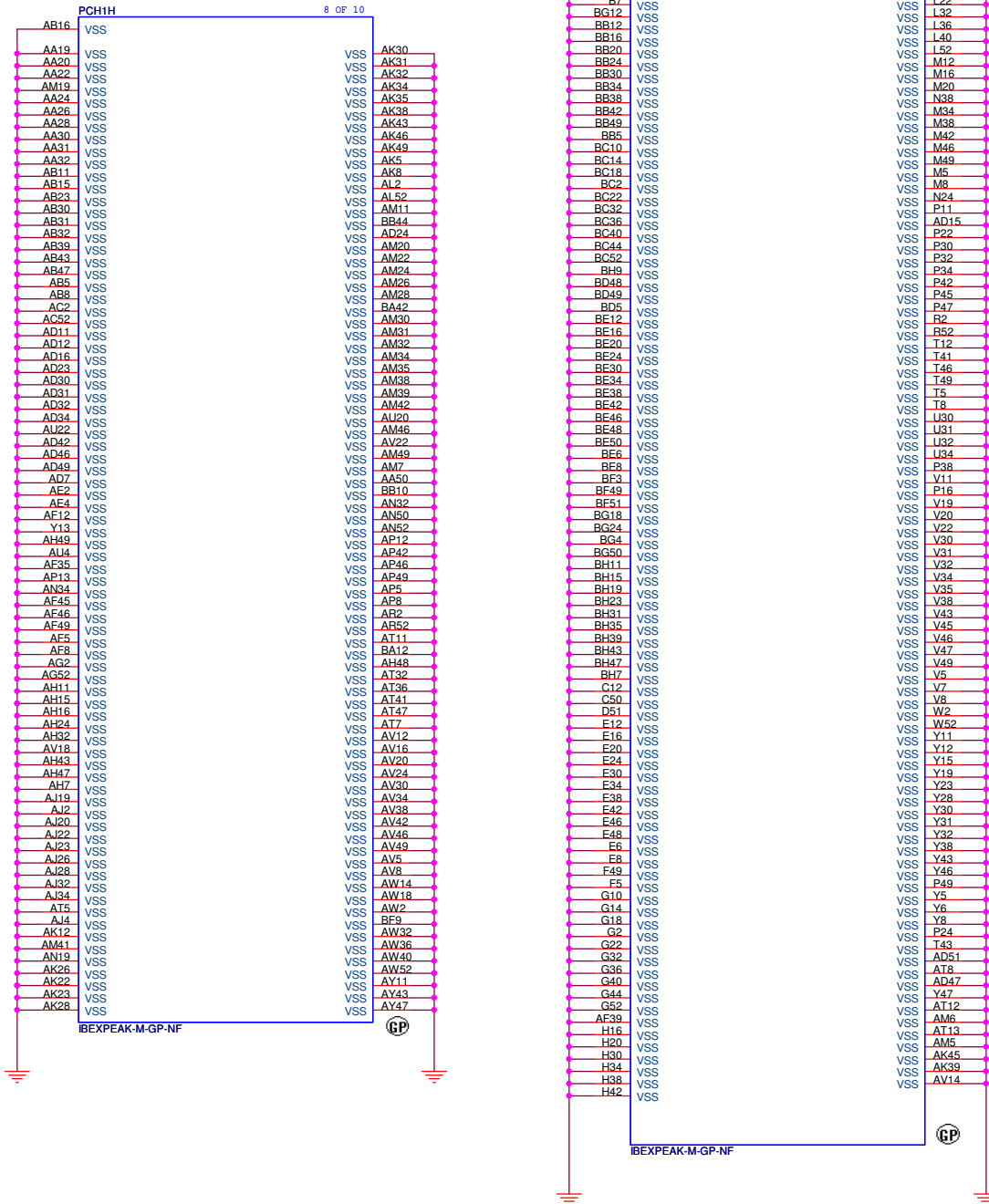
Date: Thursday, October 29, 2009

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SSID = PCH



SSID = PCH



<Core Design>

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Title: **PCH (9/9)**

Size: A3	Document Number: Fonseca 14.1" DIS	Rev: X01
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Date: Thursday, October 29, 2009 Sheet 28 of 92

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Custom

Document Number

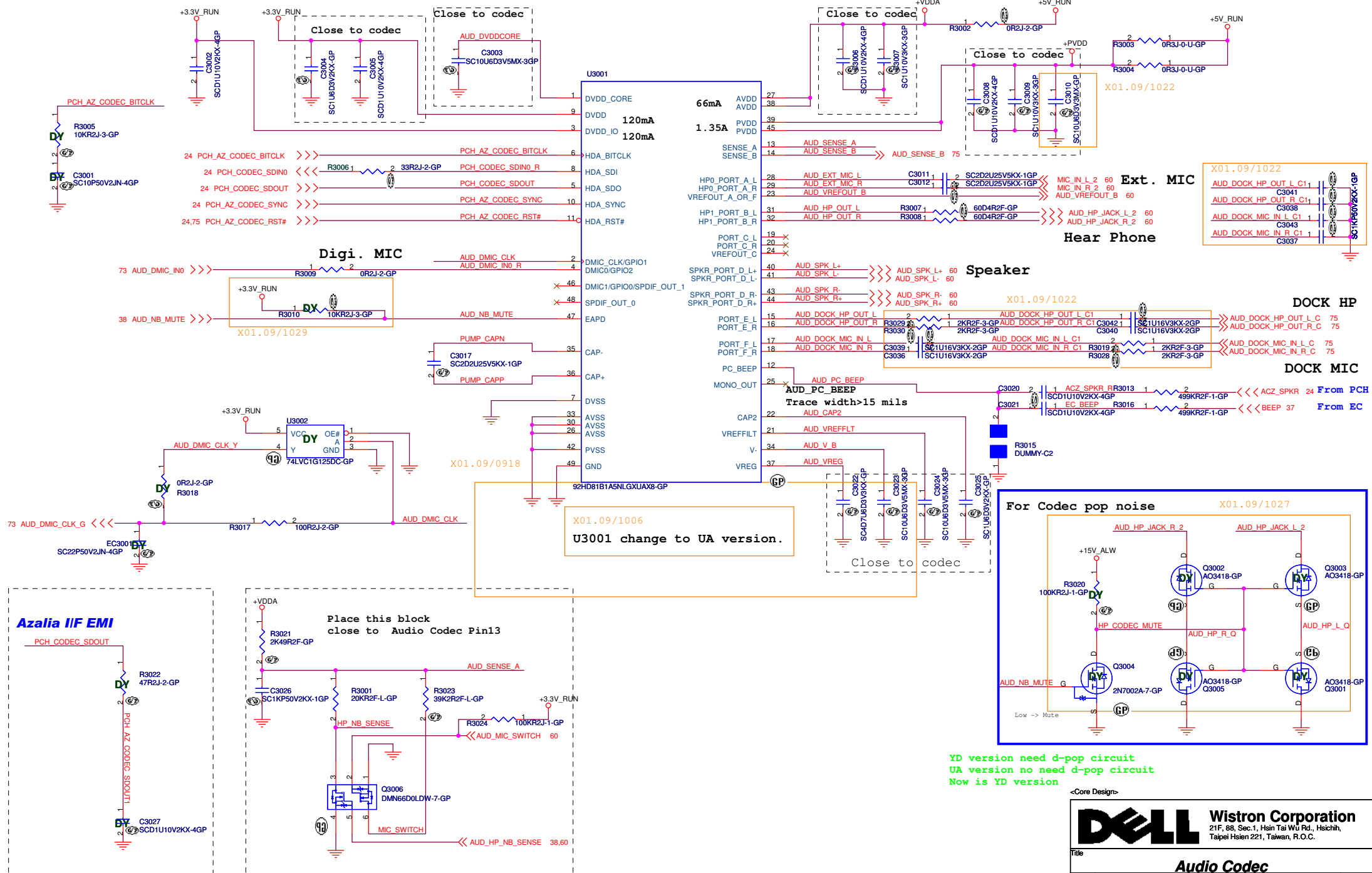
Rev

Reserve
Fonseca 14.1" DIS
X01

Date: Thursday, October 29, 2009

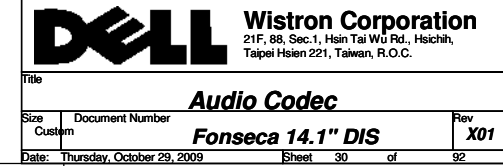
Sheet 29 of 92

SSID = AUDIO



```
YD version need d-pop circuit
UA version no need d-pop circuit
Now is YD version
```

<Core Design>



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<Core Design>



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Title

Size

Custom

Document Number

Rev

Reserve

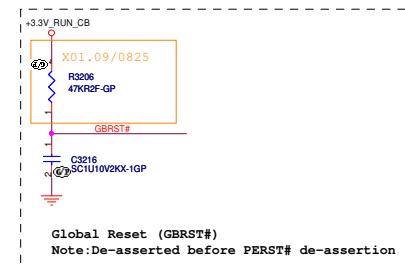
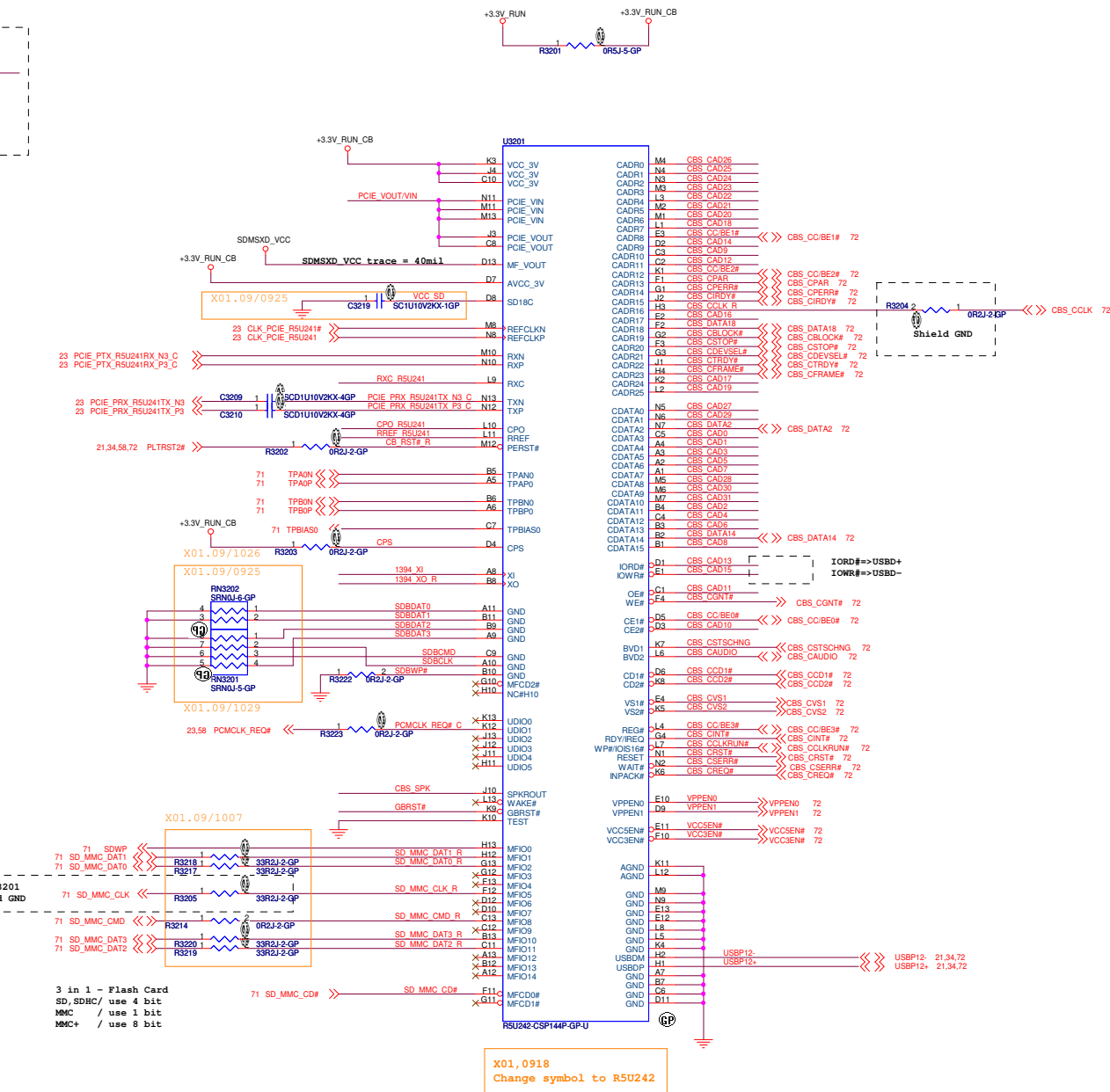
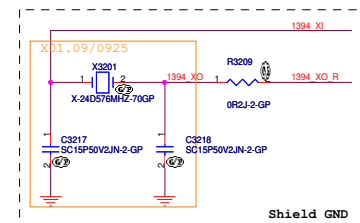
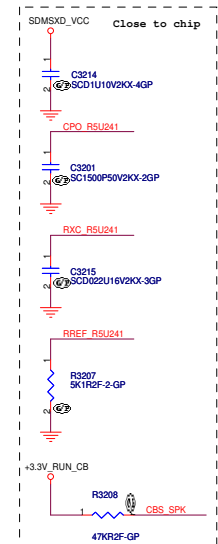
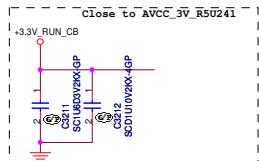
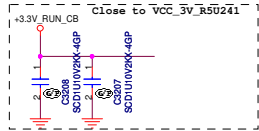
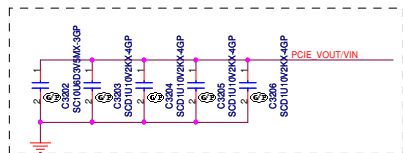
Fonseca 14.1" DIS

X01

Date: Thursday, October 29, 2009

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SSID = 1394



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<Core Design>



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Title

Size

Custom

Document Number

Rev

Reserve

Fonseca 14.1" DIS

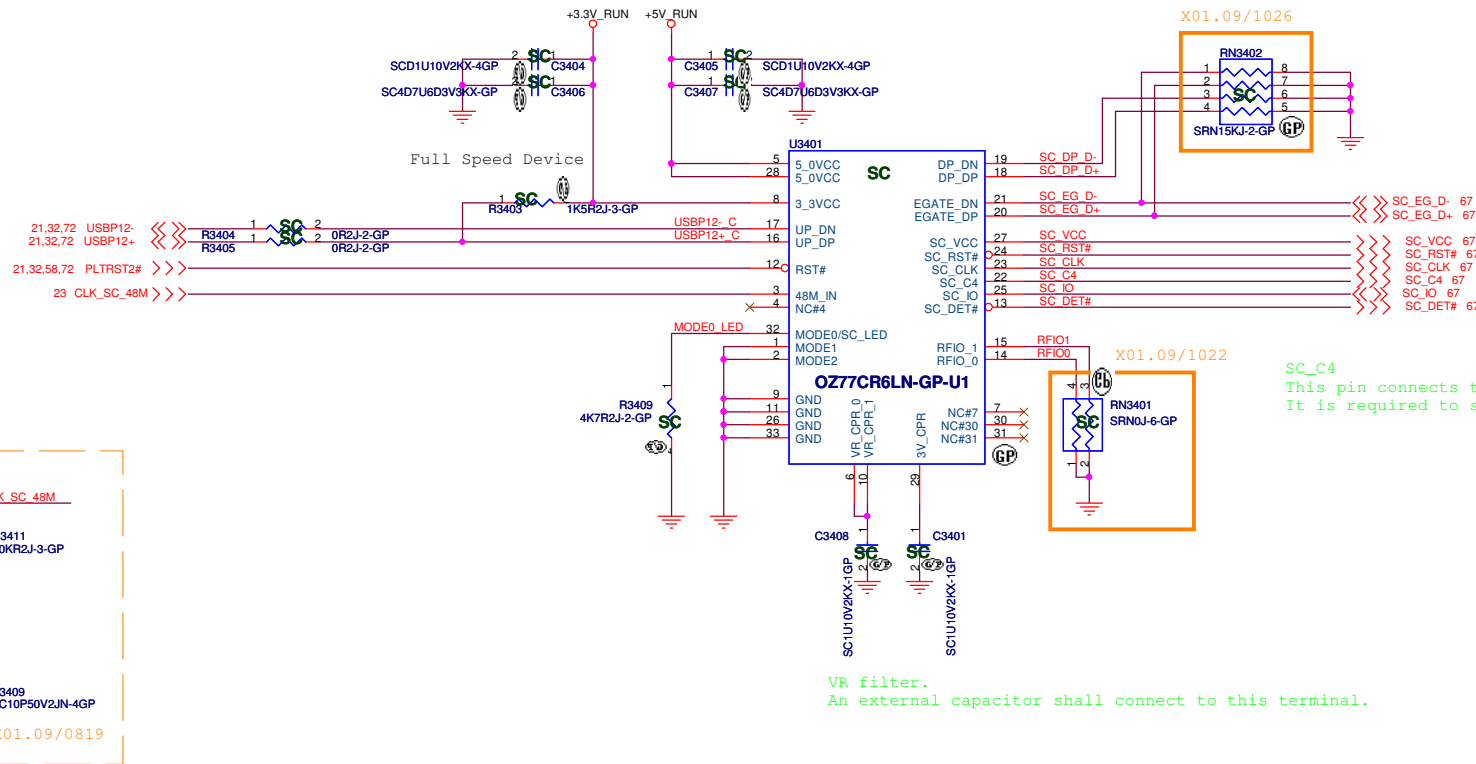
X01

Date: Thursday, October 29, 2009

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SSID = SmartCard

SmartCard Chip



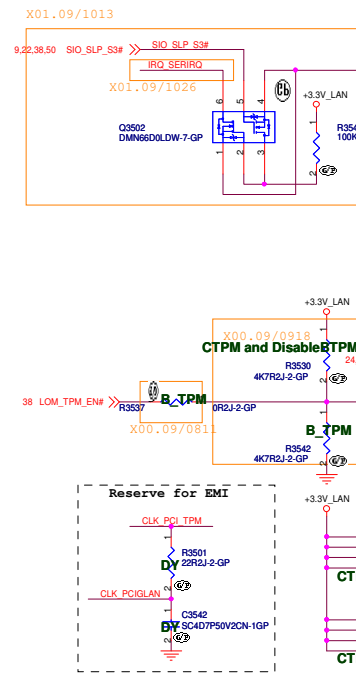
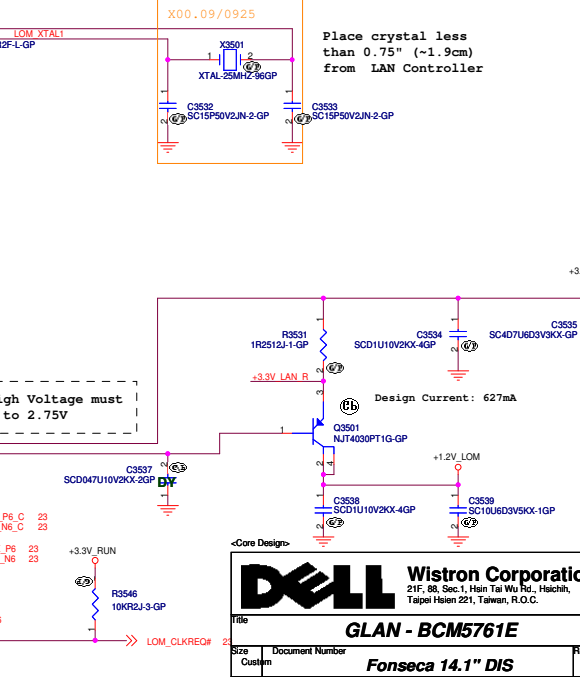
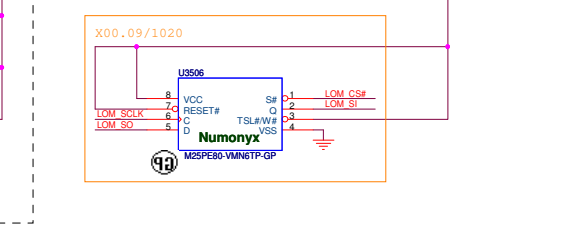
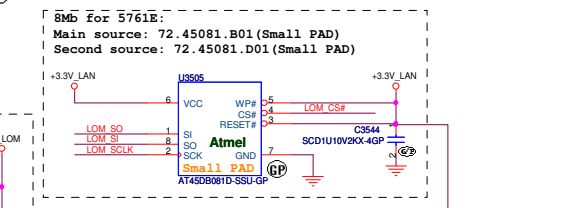
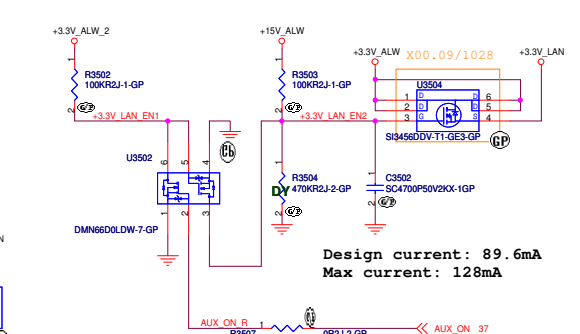
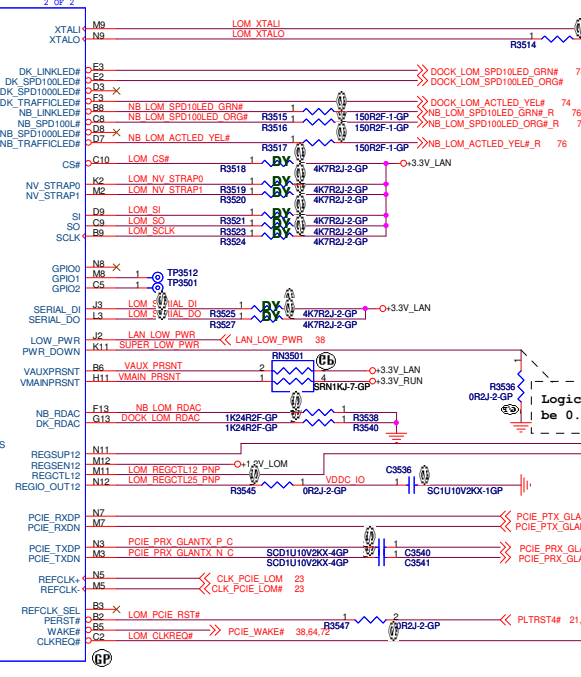
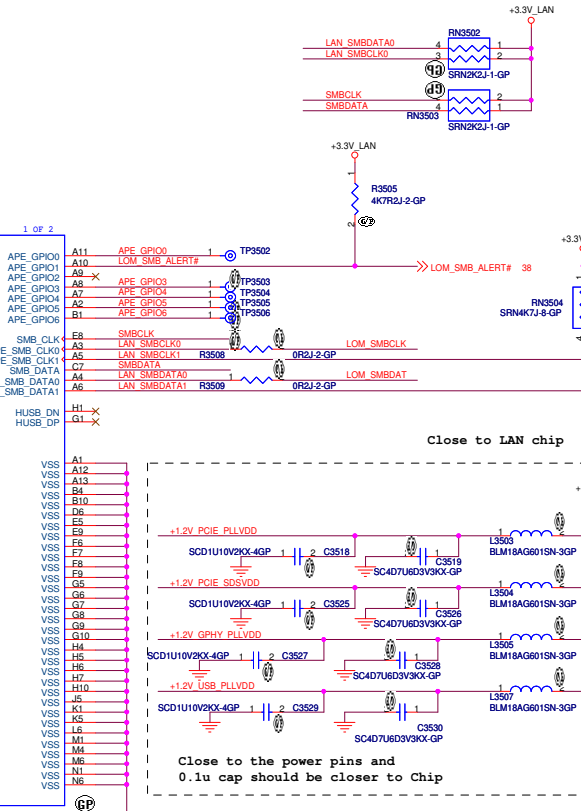
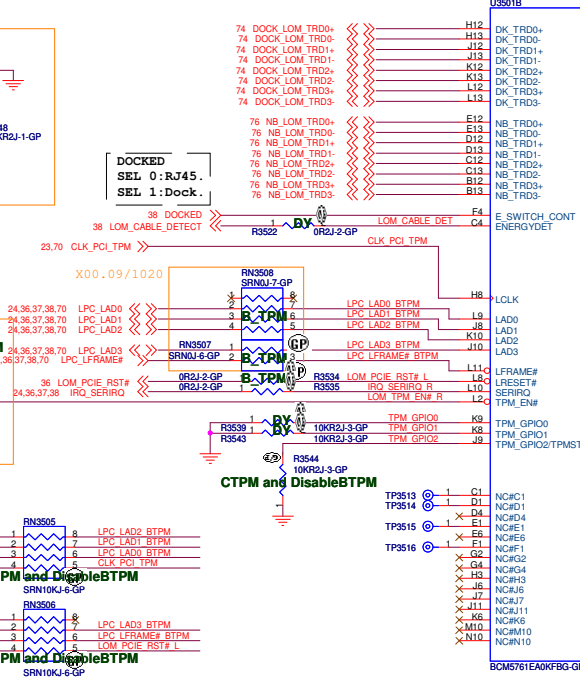
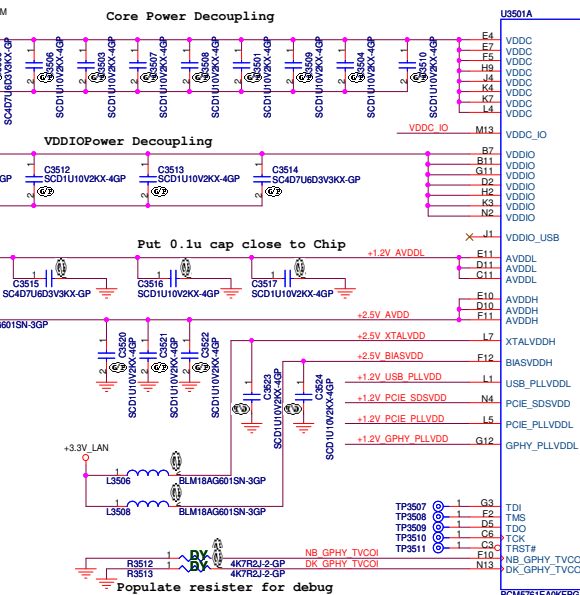
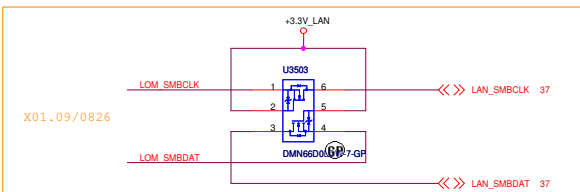
MODE0 / SC_LED	This terminal is an output indicating Smart Card activity; capable to drive an external LED device. The SC_LED terminal drives a low logic level during Smart Card data read/write activity, and is capable to source 12mA of IOL current to drive an external LED circuit. When RST# is asserted, this terminal is sampled to select the downstream port configuration for DP_DP and DP_DN (Internal Port 1). When sampled low (4.7k), the downstream port device is removable. ~~When sampled high, the downstream port is a non-removable device.~~ Includes internal input pull-up resistor.
MODE1	Test Pin. This terminal shall be externally connected to GND.
MODE2	Test Pin. This terminal shall be externally connected to GND.

RFIO_0	Contactless Smart Card Interface Signal 0 and 1. This signal provides detection and data communication with an external RF device.
RFIO_1	If contactless is disabled, then this terminal shall be pulled down to GND through a pull-down resistor, or directly connected to GND.

SSID = LOM

SYMBOL: 71.05761.00U

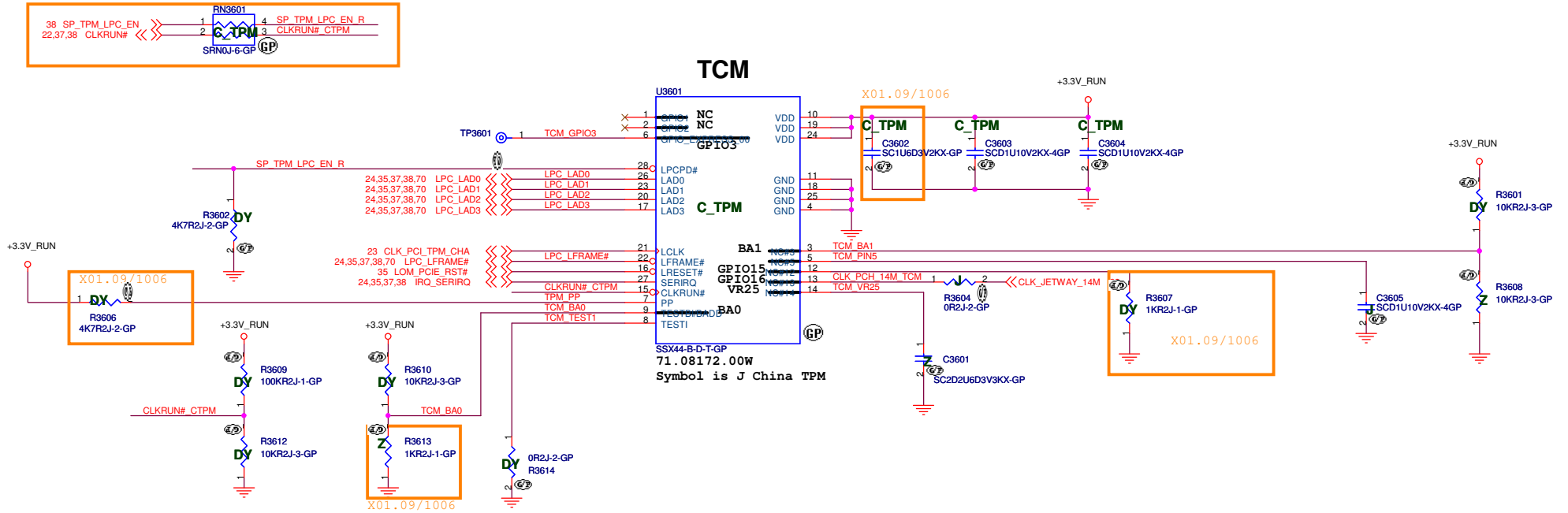
Product : P802H /
71.05761.M02 (Rev:B0)



SSID = TCM

Symbol : Jetway, but linked to ZTE
Product : 71.08172.00W (ZTE)

X01.09/1020



Base Address	BA1 PIN3	BA0 PIN9
EE/EF	0	0
7E/7F	0	1
2E/2F	1	0
4E/4F	1	1

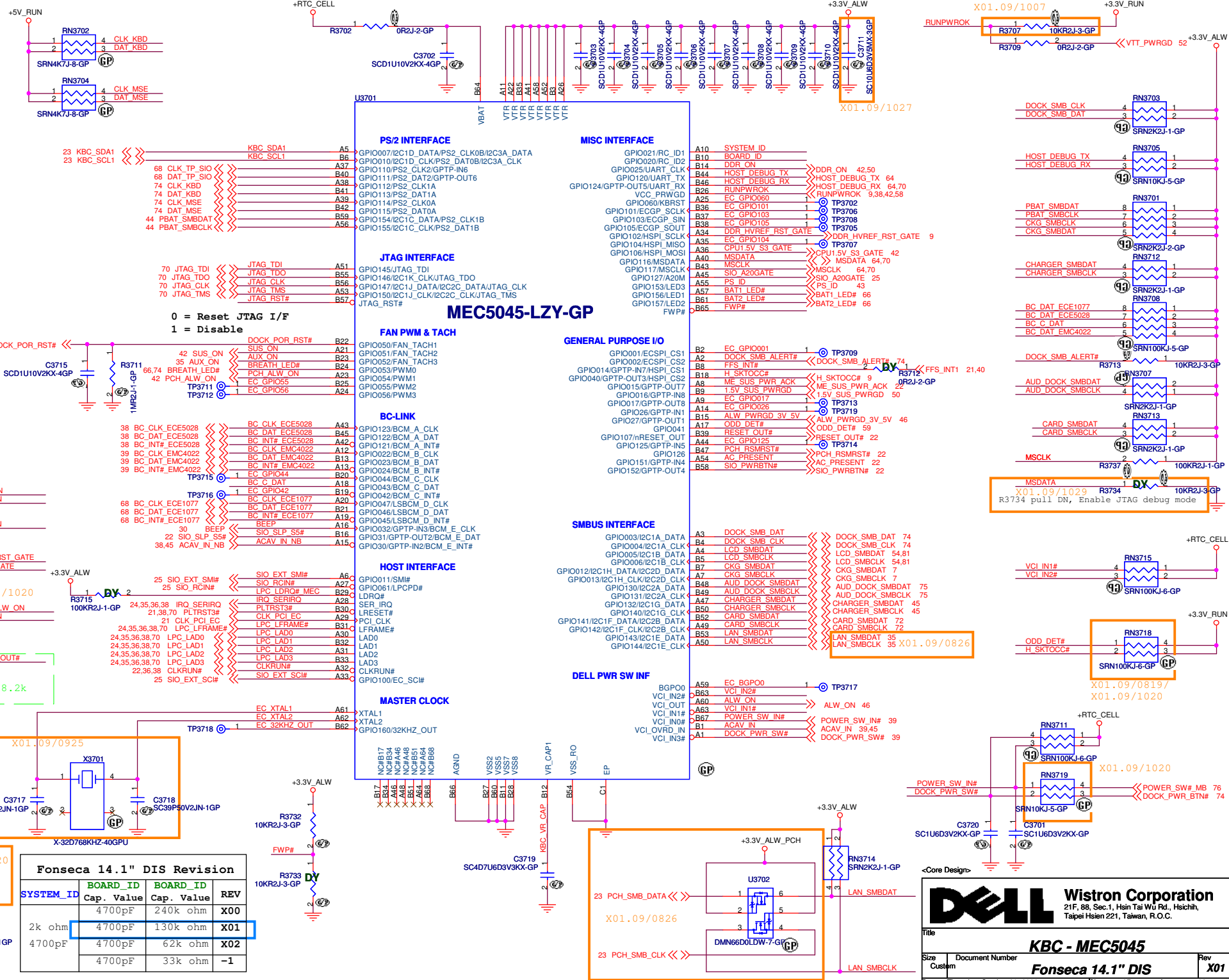
Default EE/EF as Any recommended

	1(default)	0
PIN12	FLASH	SRAM

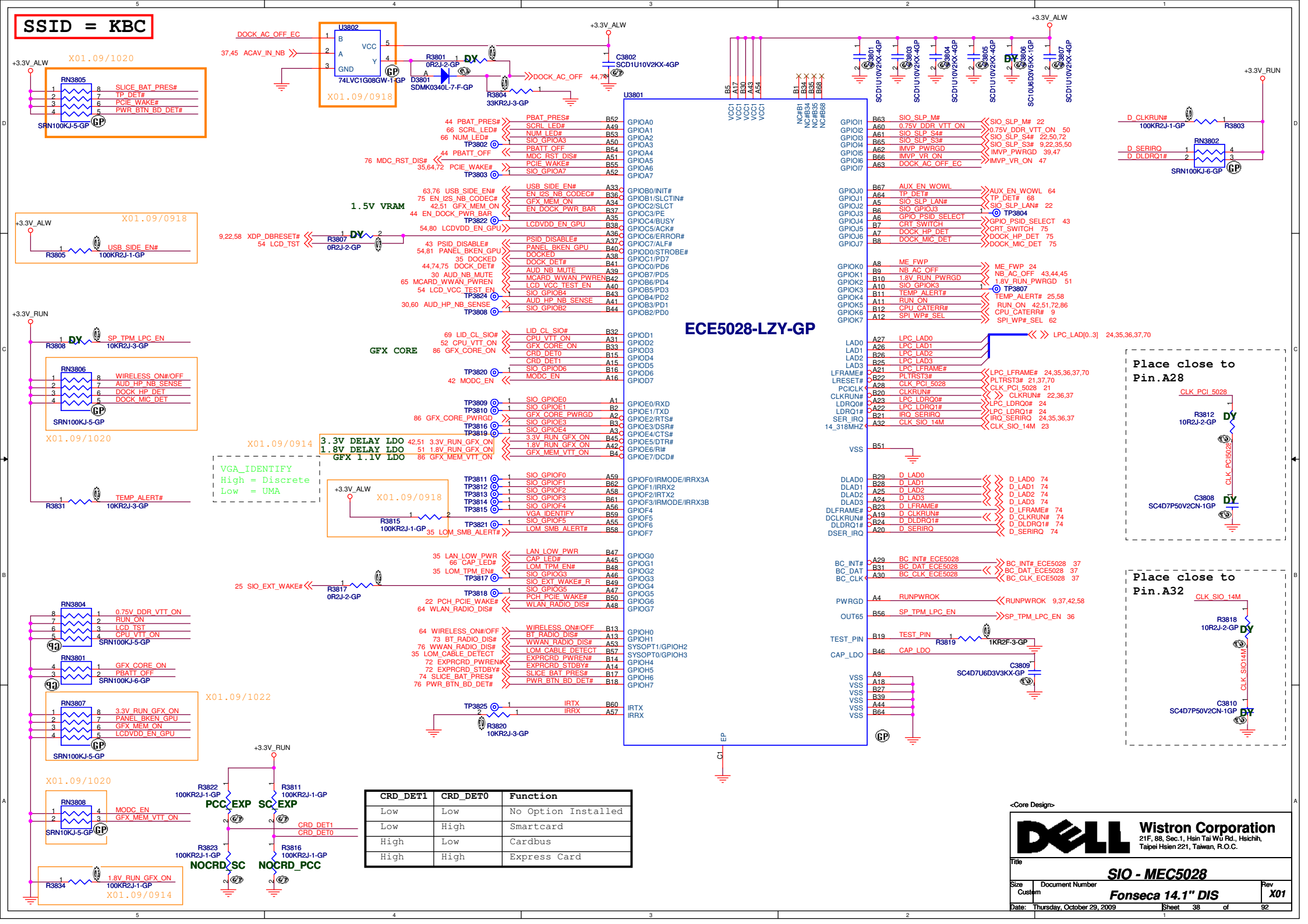
J has internal PU with PIN12.

<Core Design>

SSID = KBC



SSID = KBC



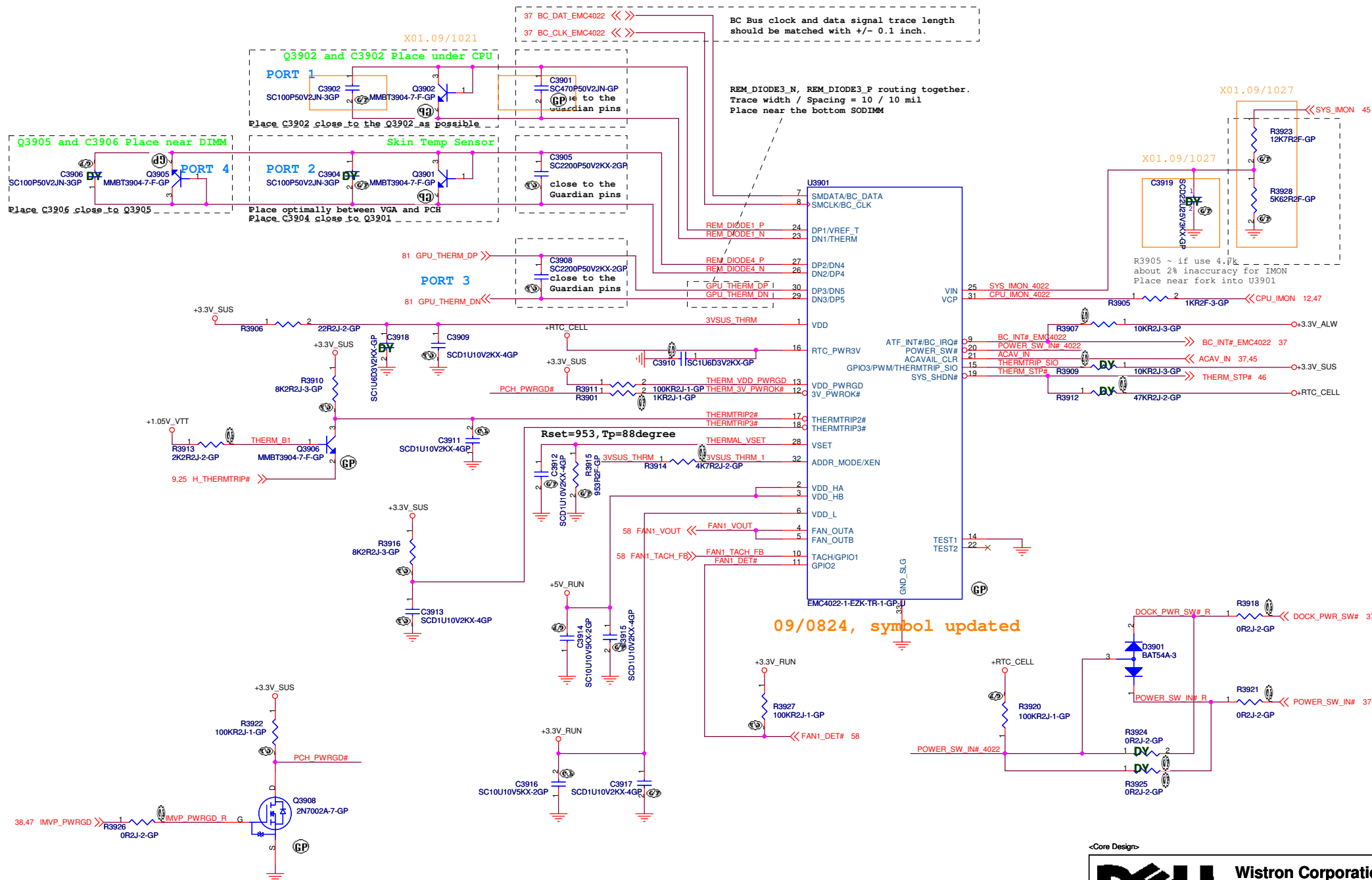
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **SIO - MEC5028**

Size: Custom Document Number: **Fonseca 14.1" DIS** Rev: **X01**

Date: Thursday, October 29, 2009 Sheet 38 of 92

SSID = Thermal



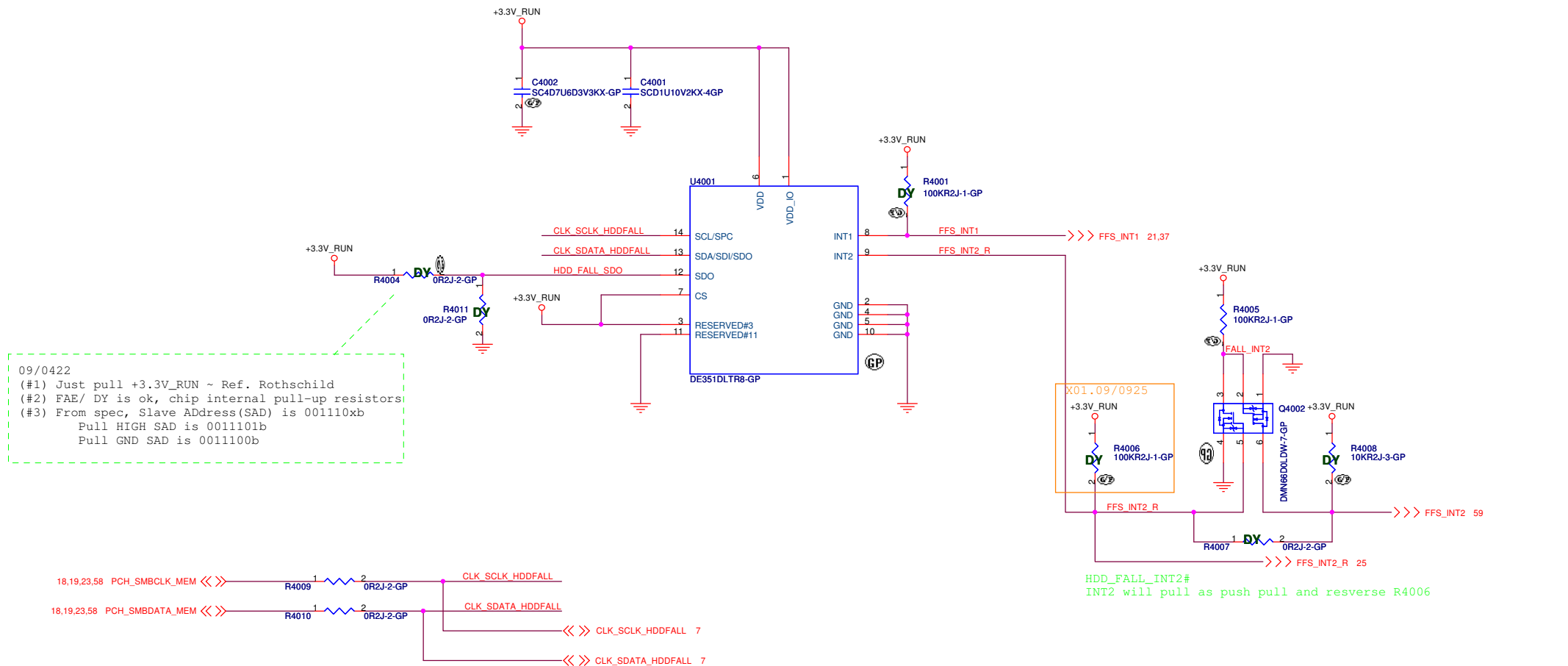
<Core Design>



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<i>Thermal, Fan controller</i>			
Size	Document Number	Rev	
Custom	<i>Fonseca 14.1" DIS</i>	X01	
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Free Fall Sensor



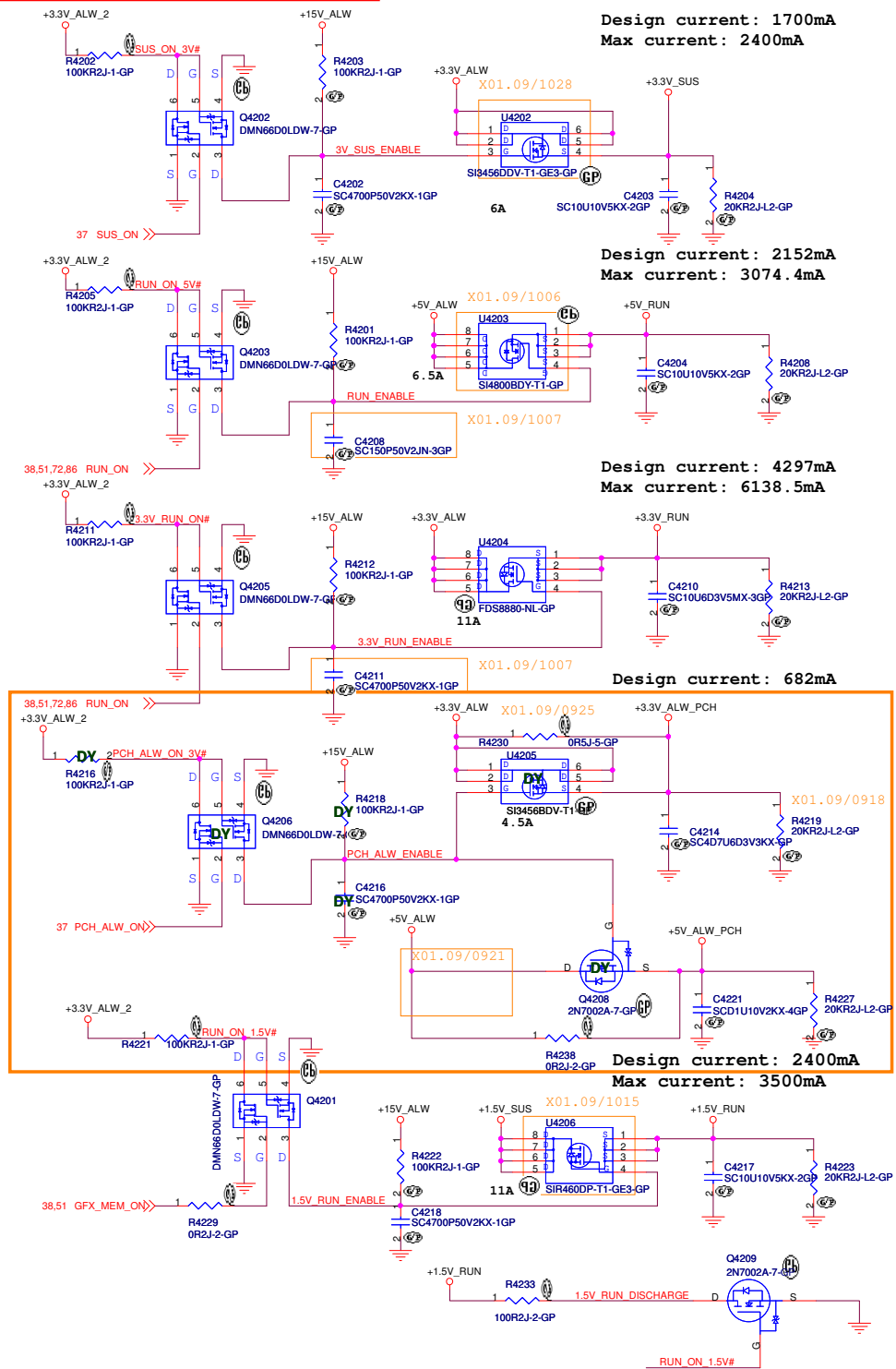
Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

SSID = Reset.Suspend

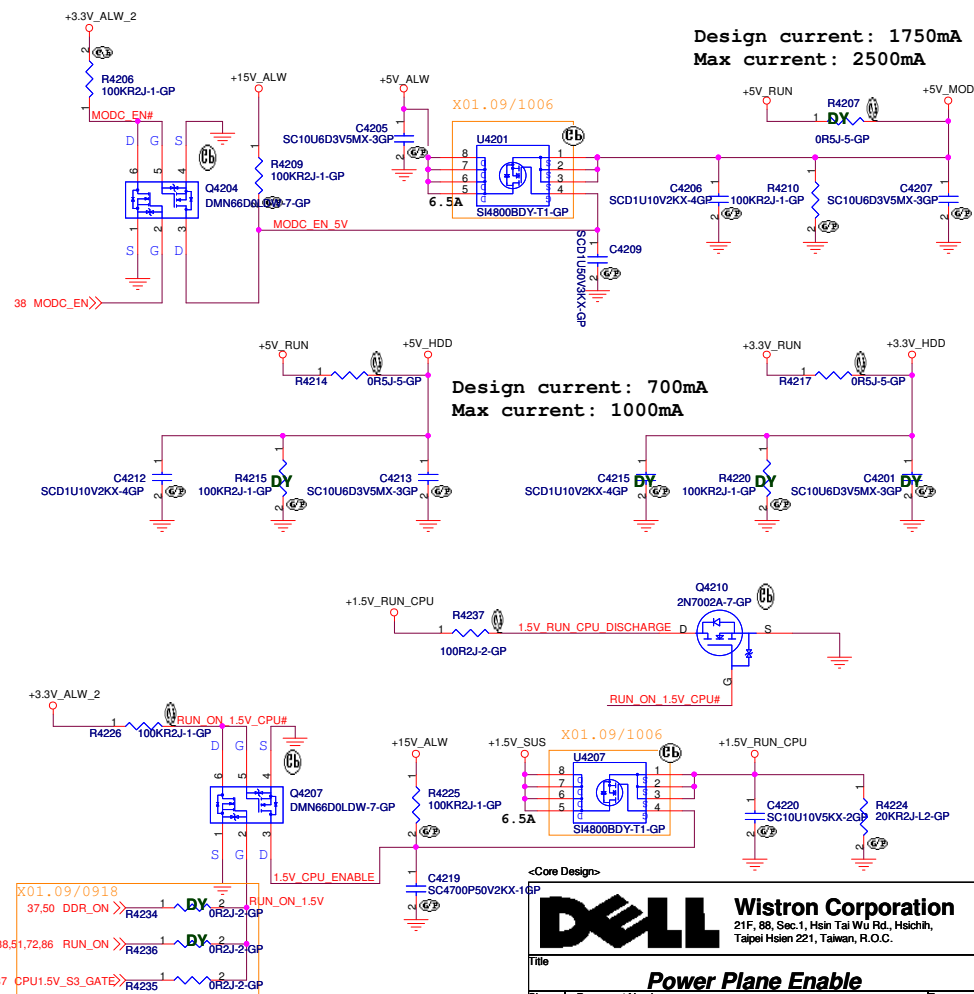
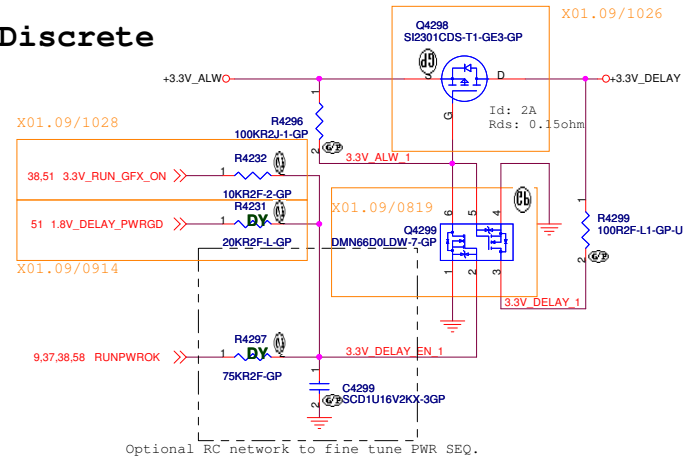
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Power On Logic			
Size A3	Document Number		Rev X01
Date: Thursday, October 29, 2009		Sheet 41 of 92	

```
SSID = Reset.Suspend
```



For Discrete



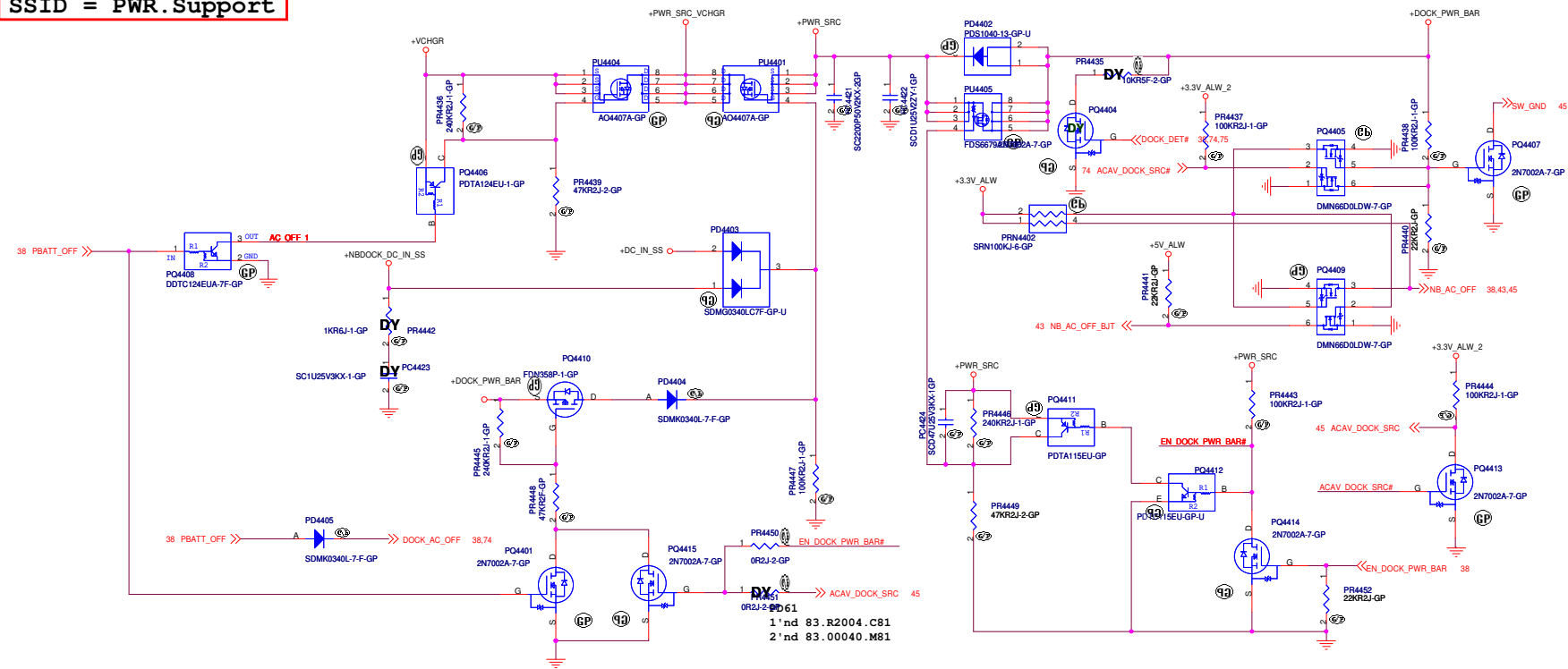
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Power Plane Enable

Fonseca 14.1" DIS

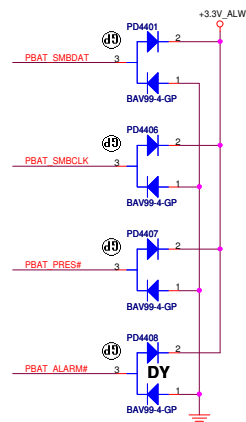
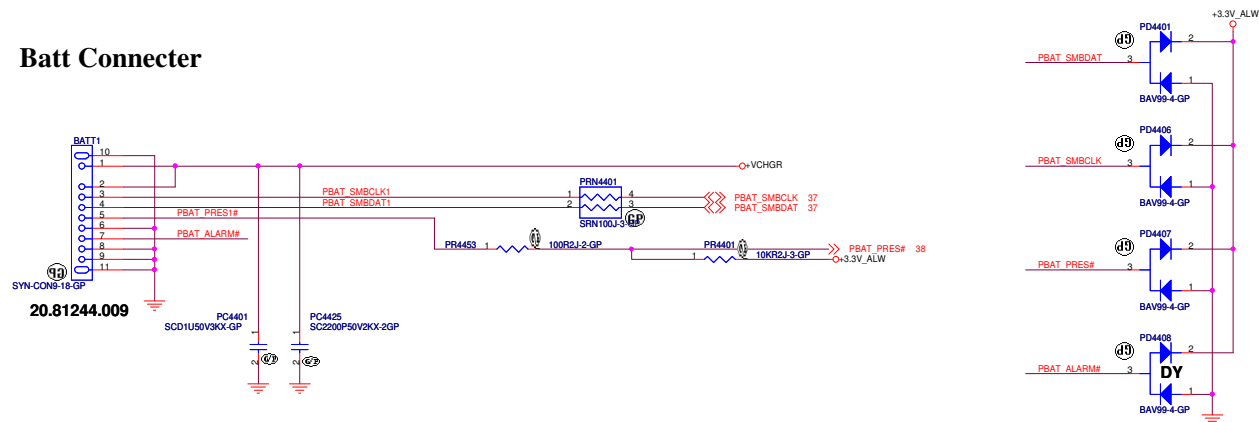
X01


```
SSID = PWR.Support
```

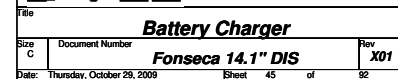


SSID = RBATT

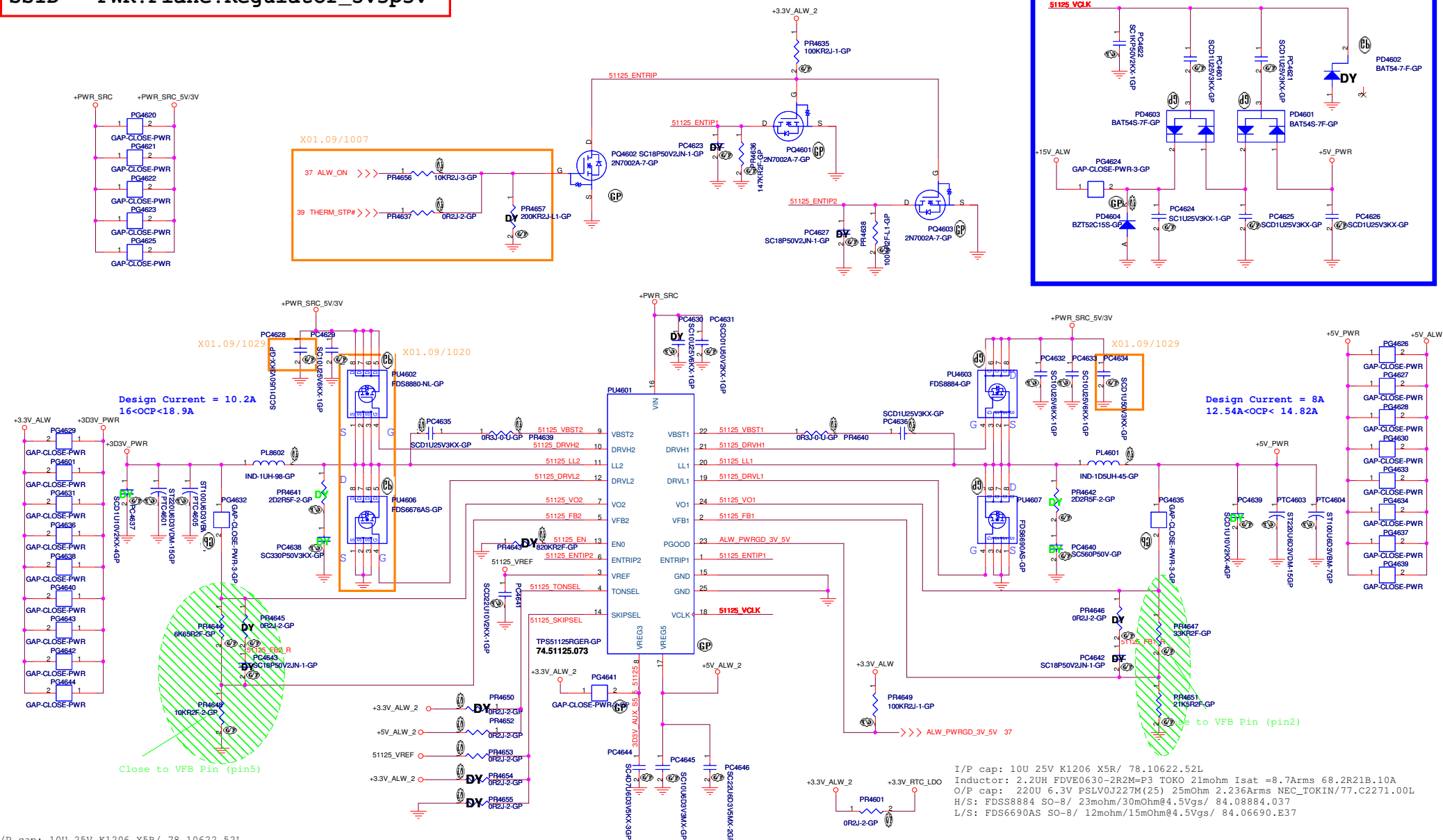
Batt Connector



<Core Design>



SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH FDVE0630-3R3M=P3 TOKO 31mohm Isat =6.9Arms 68.3R31A.10E
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

<Core Design>

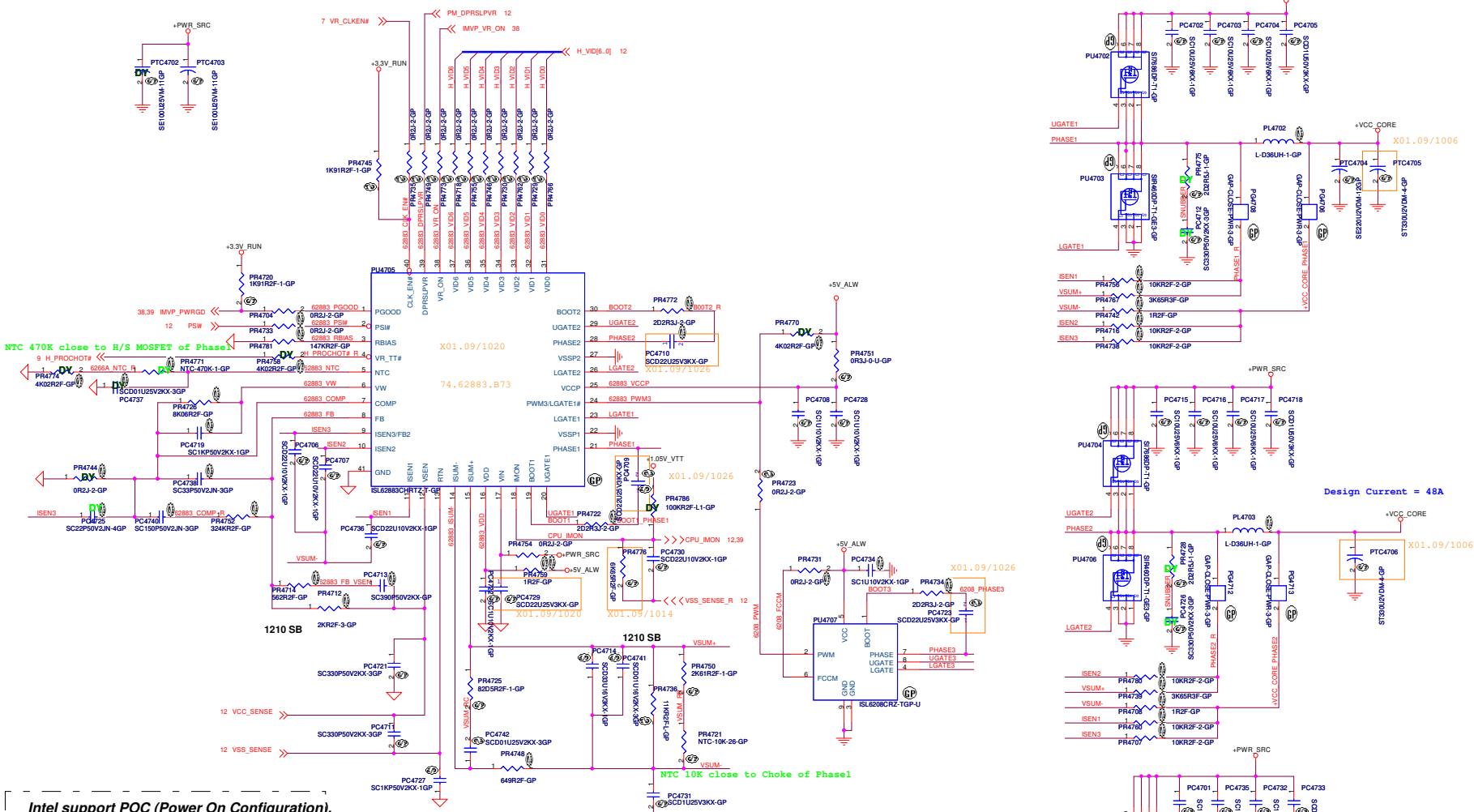
**Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

File
DCDC 5V/3D3V (TPS51125)

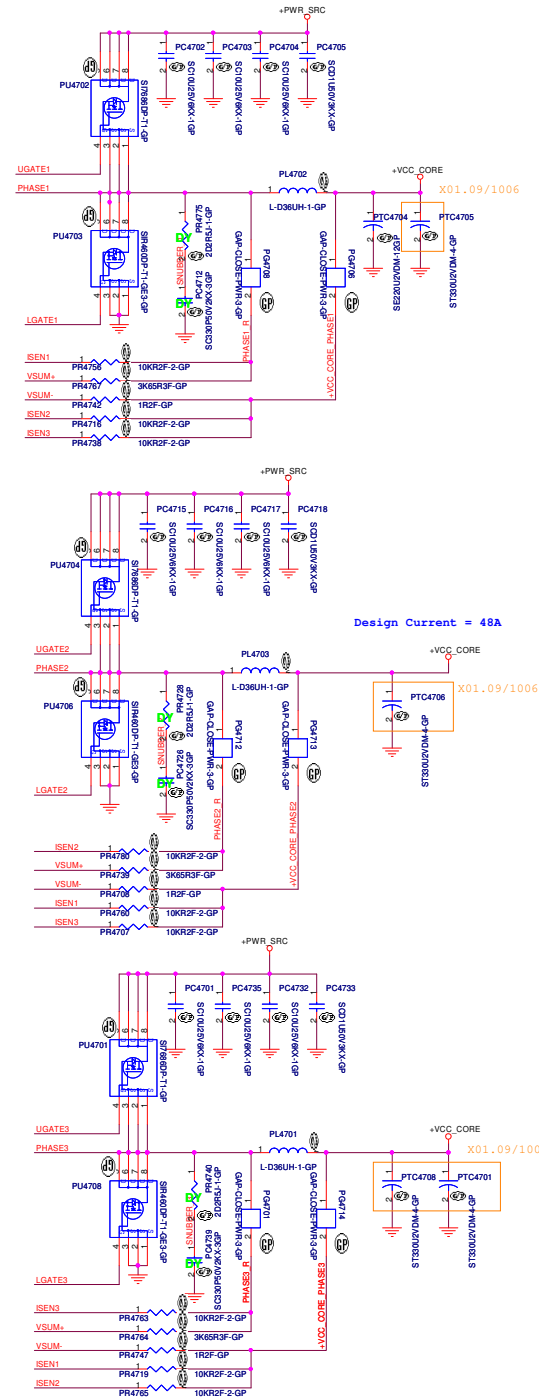
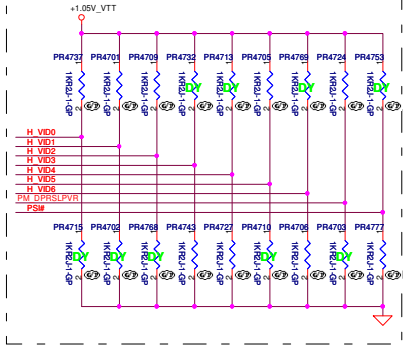
Size
Customer Document Number
Fonseca 14.1" DIS

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Rev
X01



Intel support POC (Power On Configuration).



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<Core Design>



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Title

Reserve

Size A3	Document Number Fonseca 14.1" DIS	Rev X01
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

DC to DC 1.05V

Size
A3

Document Number

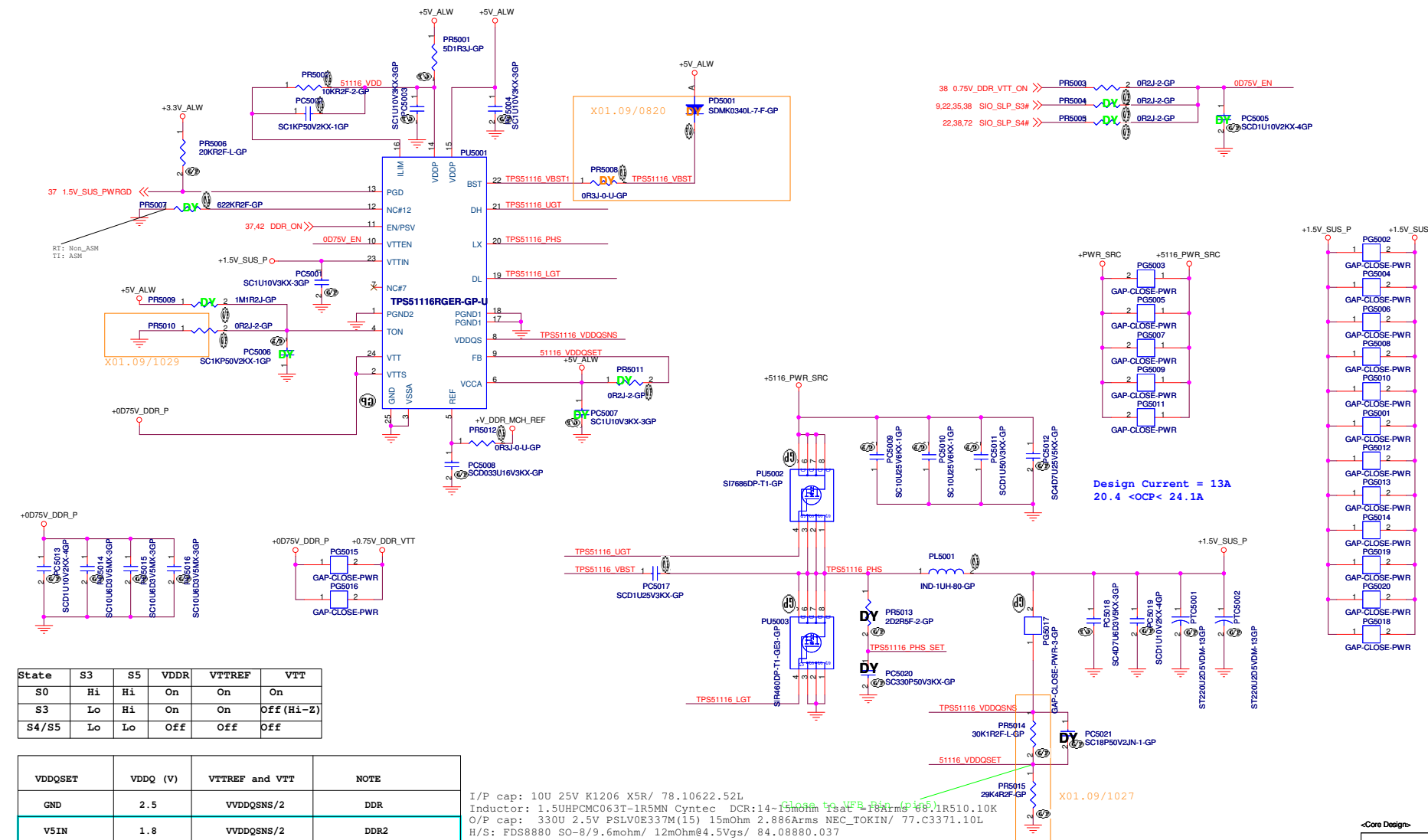
Date: Thursday, October 29, 2009

Fonseca 14.1" DIS

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Rev
X01

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC063T-1R5MN Cyntec DCR:14-15mohm Isat =18Amps P=88.1R510.10K
O/P cap: 330U 2.5V PSLV0E337M(15) 15mohm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: FDS8880 SO-8/9.6mohm/ 12mohm@4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mohm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq->400KHz

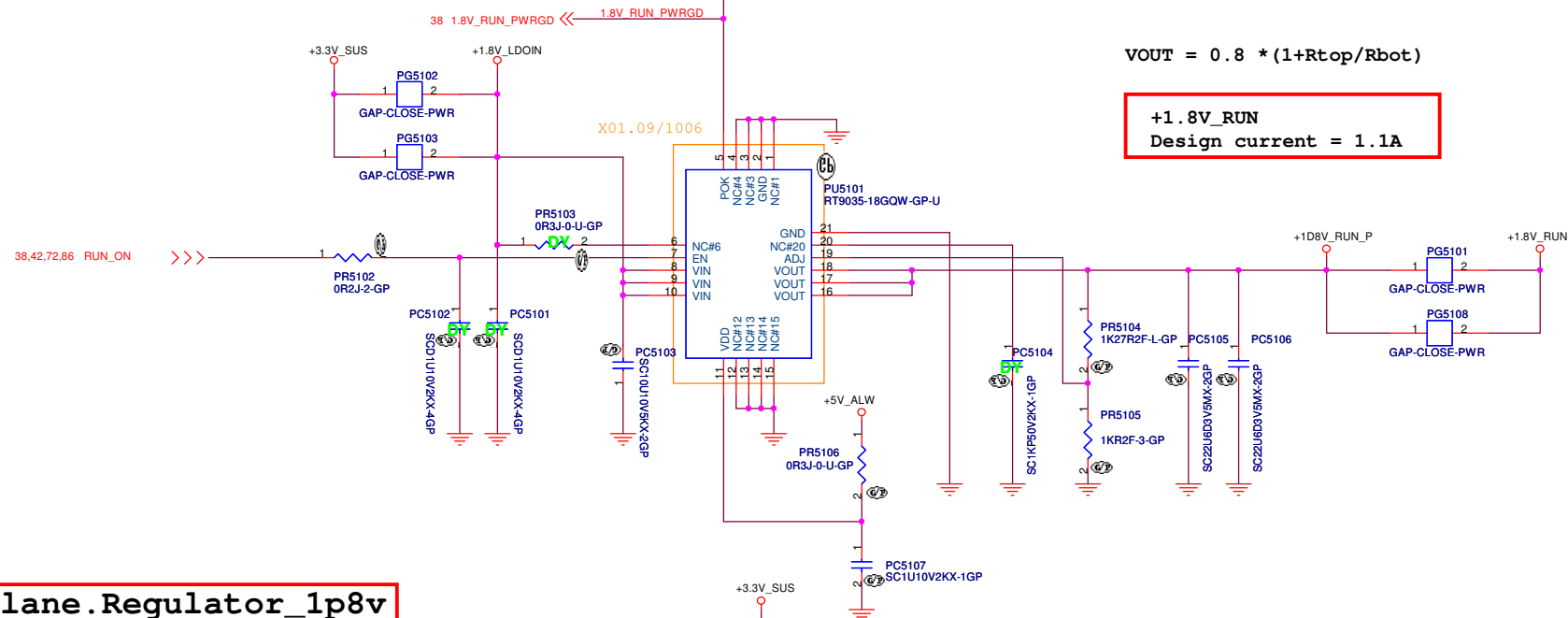
<Core Design>



Title			DC to DC 1.5V / 0.75V
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Custom	Fonseca 14.1" DIS		
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```
SSID = PWR.Plane.Regulator_1p8v
```

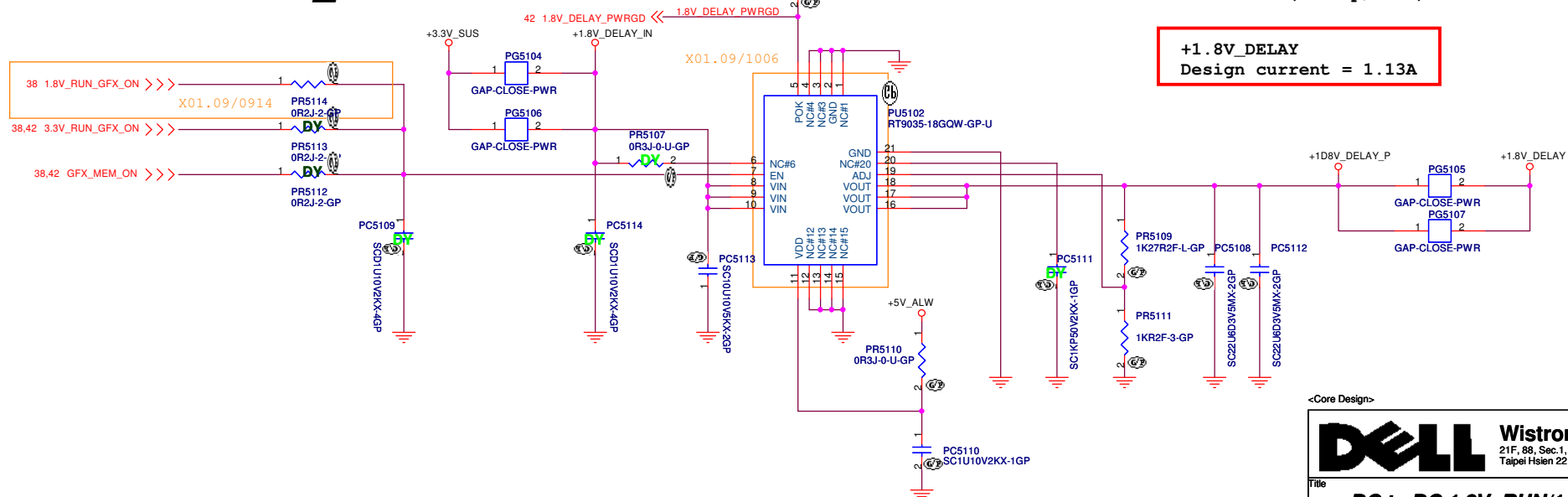
LDO for +1.8V_RUN


$$V_{OUT} = 0.8 * (1 + R_{top}/R_{bot})$$

+1.8V_RUN
Design current = 1.1A

```
SSID = PWR.Plane.Regulator_1p8v
```

LDO for +1.8V_DELAY


$$V_{OUT} = 0.8 * (1 + R_{top}/R_{bot})$$

+1.8V_DELAY
Design current = 1.13A

<Core Design>



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Title	Author	Year	Journal	Volume	Page
...	...	...	...	...	...

DC to DC 1.8V RUN/1.8V DELAY

Size

Document Number

Fonseca 14.1" DISRev
X01

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<Core Design>



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Title

CPU GFXCORE

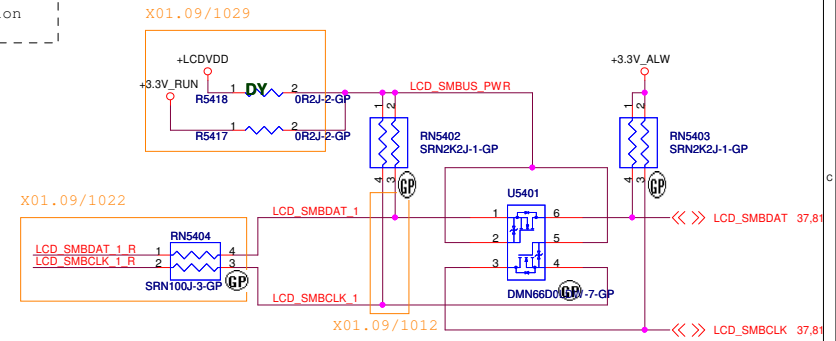
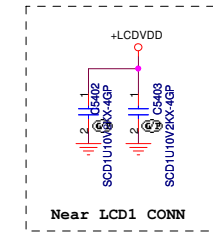
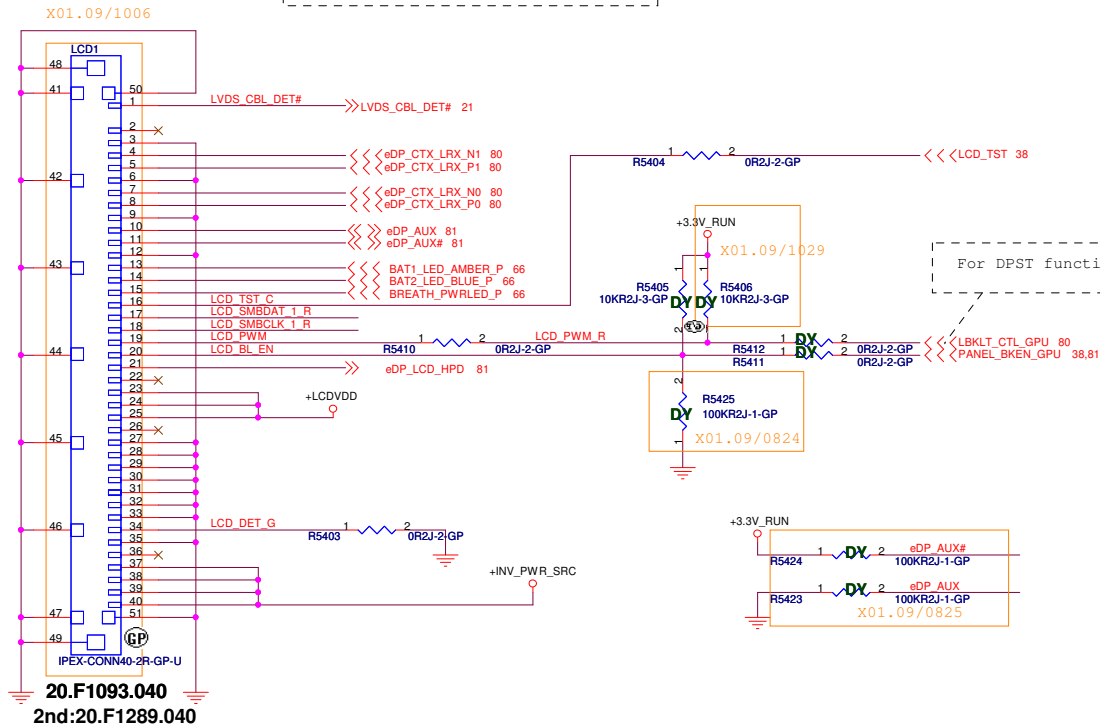
Size	Document Number	Rev
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SSID = VIDEO

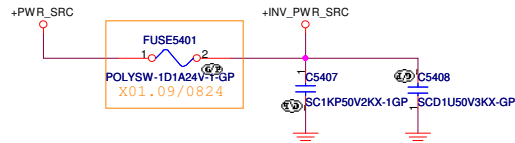
LED Location from left to right

HDD BATTERY

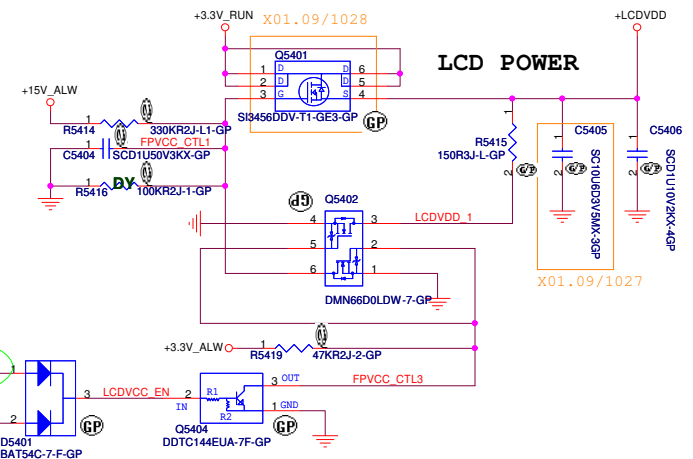
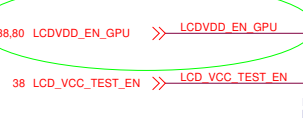


SSID = Inverter

LED BACKLIGHT CONVERTER POWER



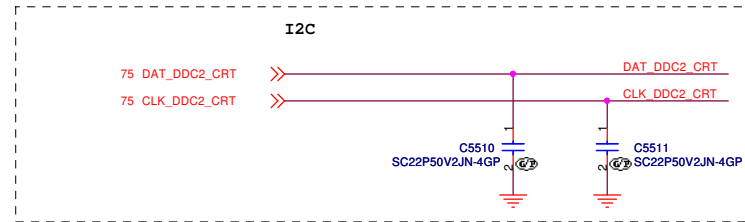
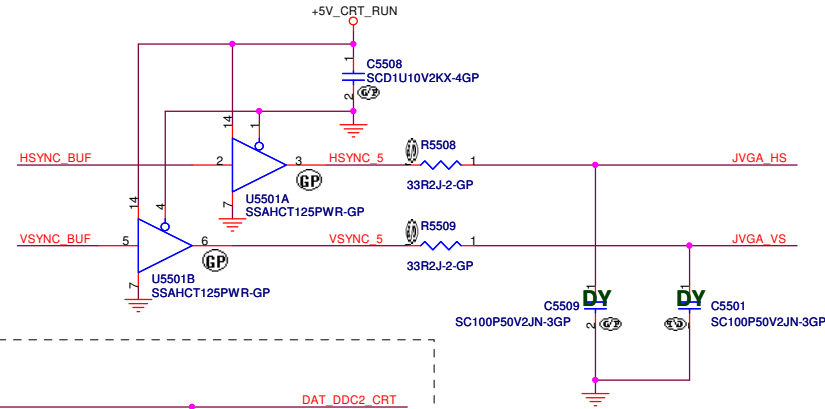
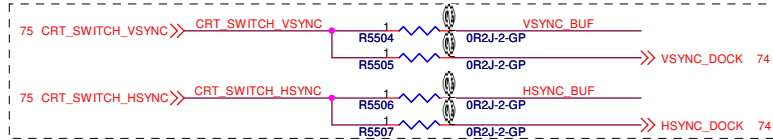
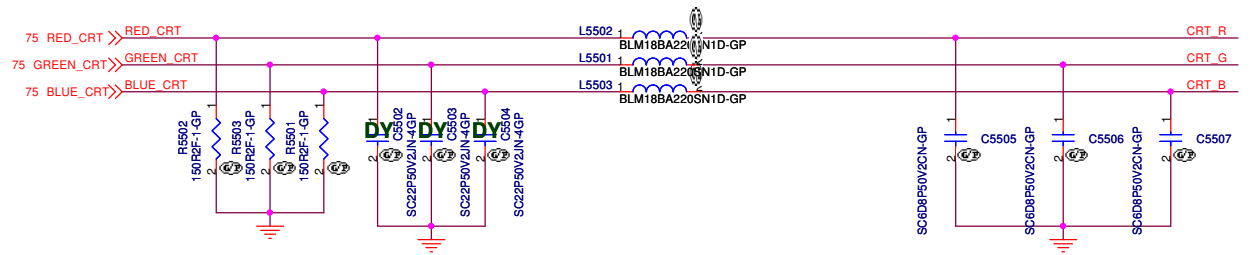
Need confirm



<Core Design>

DELL		Wistron Corporation	
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Title			
LCD			
Size	Document Number	Rev	
Custom	Fonseca 14.1" DIS	X01	
Date:	Monday, November 02, 2009	Sheet	54 of 92

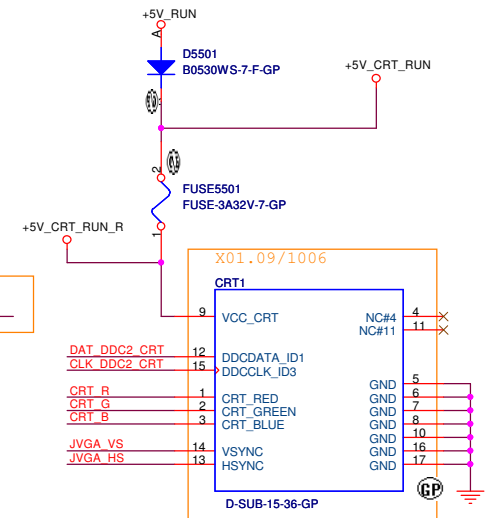
SSID = VIDEO



MAX4885E has internal ESD protection and internal level shift

X01.09/1007
AFTP5501 1 +5V_CRT_RUN_R

Layout Note:
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



20.20431.015

CRT Connector

<Core Design>

DELL		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CRT			
Size	Document Number	Rev	
A3	Fonseca 14.1" DIS	X01	
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<Core Design>

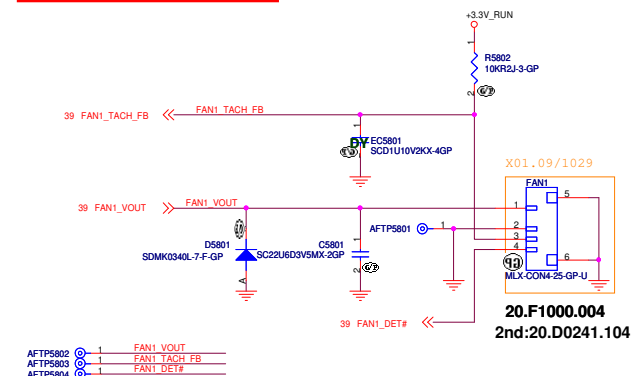
		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserve			
Size A3	Document Number		Rev X01
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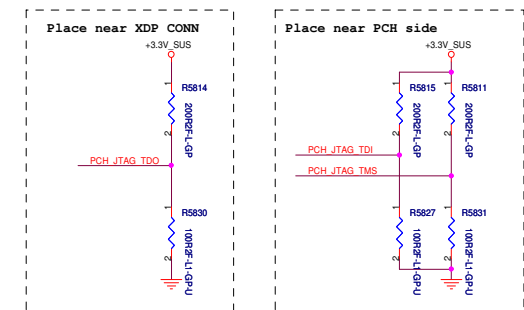
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		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserve			
Size A3	Document Number		Rev X01
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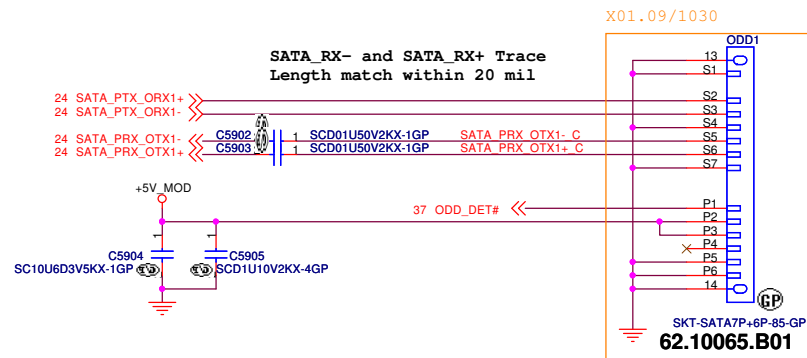
SSID = Thermal



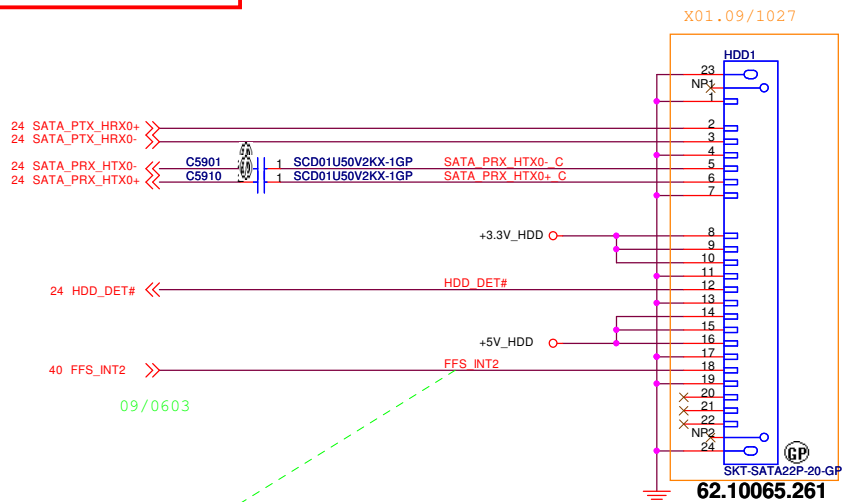
A 33 ohm series resistor should be placed within 1 inch (or 25.4 mm) of the PCH to source terminate the interface.



SSID = SATA SATA ODD Connector



SSID = SATA SATA HDD Connector



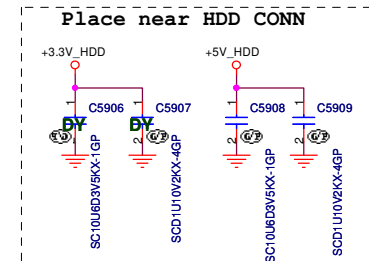
FFS_INT2
#1) It is active High when Free Fall is detected,
allowing Pin.11 to be pulled high.
Pin.11 driven low on power up and then
held low unless free fall.

Main: 62.10065.261
2nd: 62.10065.511

SATA HDD Interface comment

--- GND
RX+
RX-
--- GND
TX-
TX+
--- GND

----- 3.3V
----- 3.3V
----- 3.3V
--- GND
--- GND / Dell Detected Pin
--- GND
----- 5V
----- 5V
----- 5V
--- GND
Staggered spinup/activity (in supporting drives)
--- GND
----- 12V
----- 12V
----- 12V

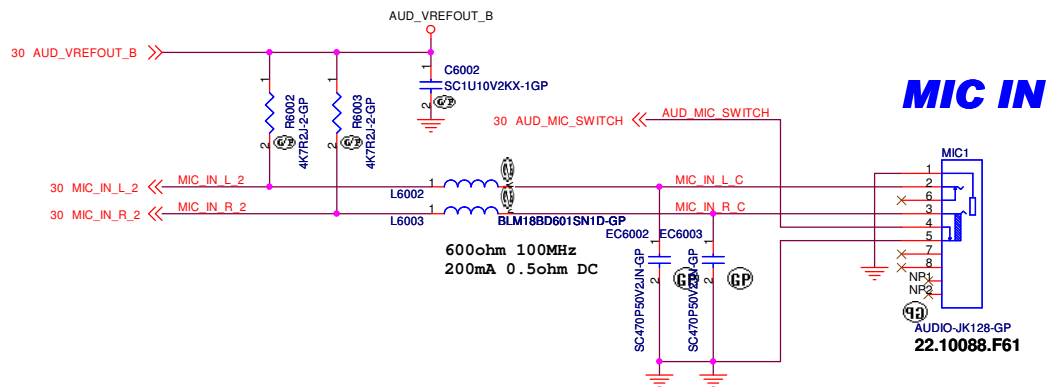


<Core Design>

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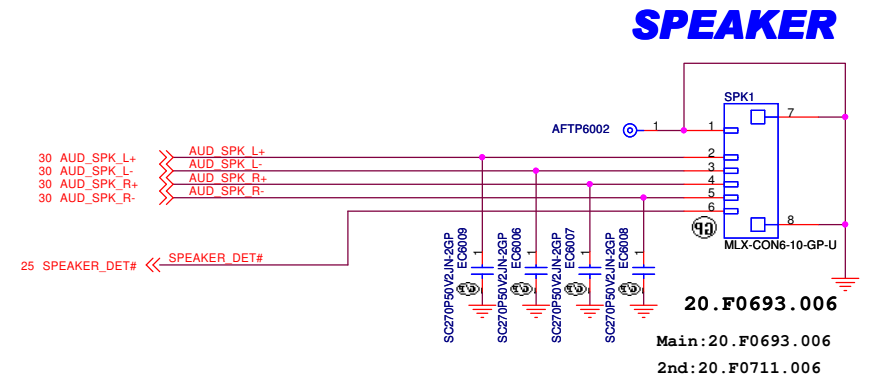
Title			
HDD / ODD Connector			
Size	Document Number		Rev
A3	Fonseca 14.1" DIS		X01
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SSID = AUDIO



MIC IN

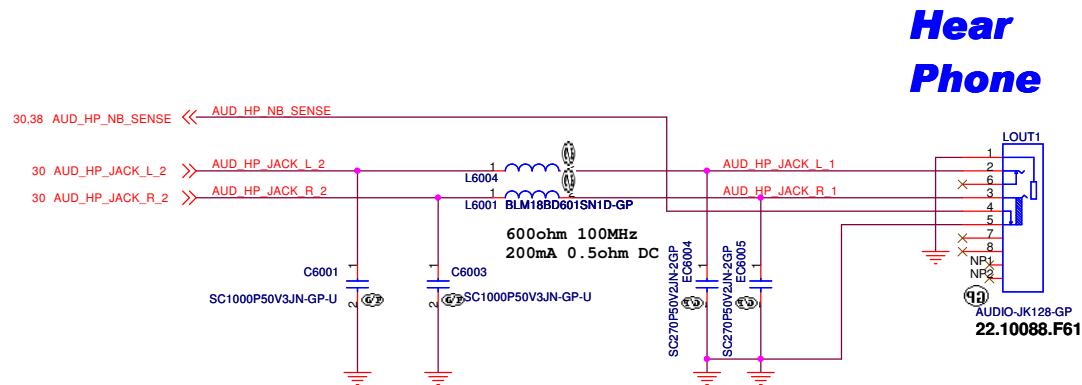
SSID = AUDIO



SPEAKER

AFTP6003 1 AUD_SPK_L+
AFTP6004 1 AUD_SPK_L-
AFTP6005 1 AUD_SPK_R+
AFTP6001 1 AUD_SPK_R-
AFTP6006 1 SPEAKER_DET#

SSID = AUDIO



Hear
Phone

<Core Design>

SSID = LOM

(Blank)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN

Size
C

Document Number
Fonseca 14.1" DIS

Rev
X01

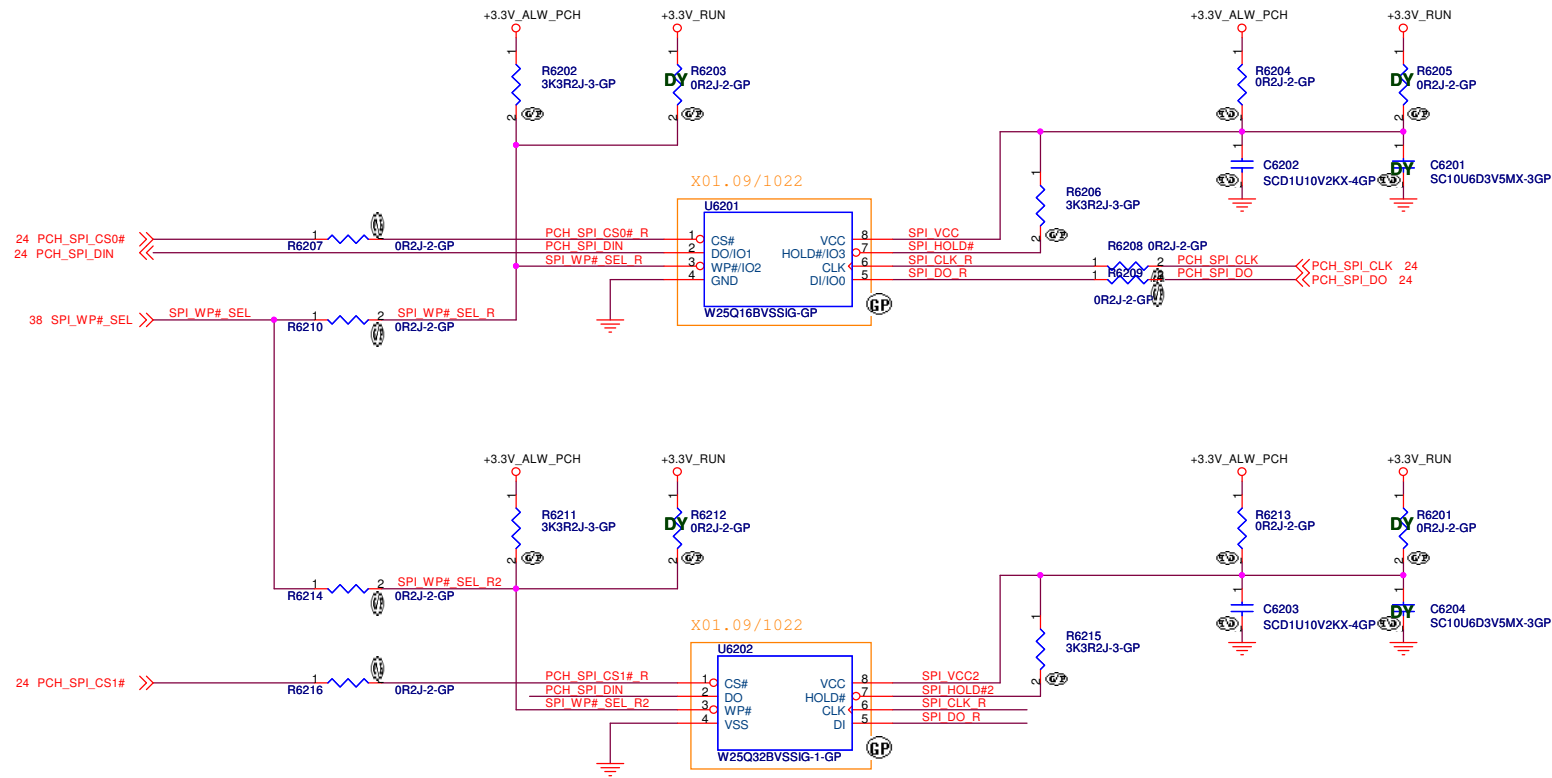
Date: **Thursday, October 29, 2009**

Sheet **61** of **92**

SSID = Flash.ROM

09/0416, Pin.2
From Intel checklist,
SPI_CS0#/CS1#
No series resistor required
if routing length is 1.5"-6.5"
(with 1 or 2 SPI device)

09/0416, Pin.6
Intel checklist
No series resistor required if routing length is 1.5"-6.5"
(with 1 or 2 SPI device)



- #1 source: 72.25Q16.001 (2MB, Winbond)
 - #2 source: 72.25165.A01 (2MB, MXIC)
 - #3 source: 72.25016.D01 (2MB, SST)
 - #4 source: 72.02516.A01 (2MB, Numonyx)
-
- #1 source: 72.25Q32.A01 (4MB, Winbond)
 - #2 source: 72.25325.A01 (4MB, MXIC)
 - #3 source: 72.25032.A01/72.25032.D01 (4MB, SST)
 - #4 source: 72.25P32.B01 (4MB, Numonyx)
-
- #1 source: 72.25Q64.001 (8MB, Winbond)
 - #2 source: 72.25644.001 (8MB, MXIC)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

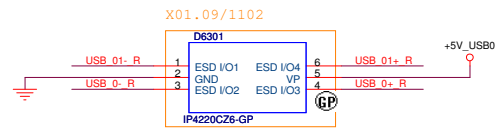
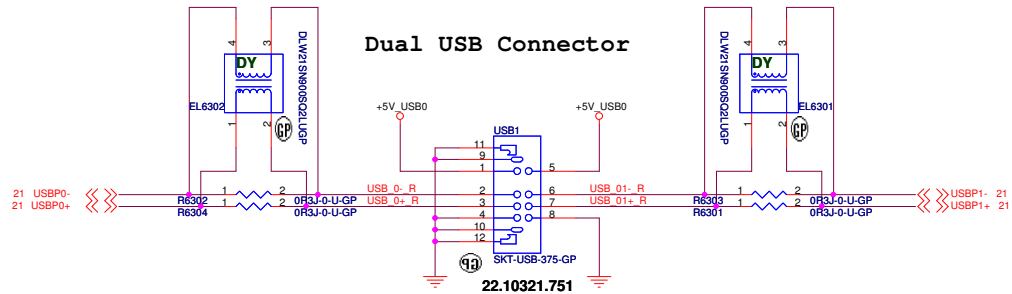
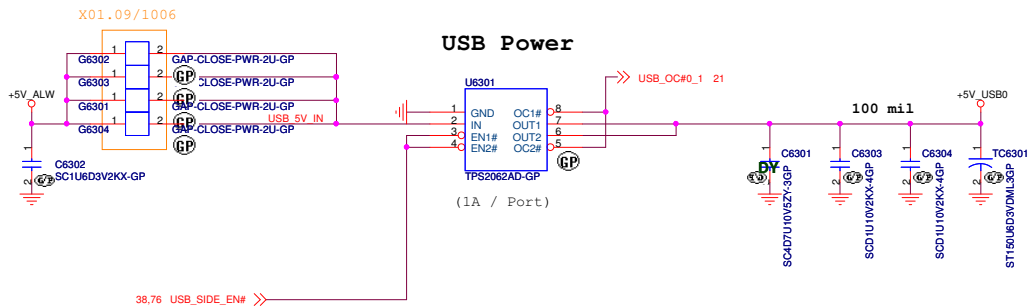
Title: **Flash / EEPROM**

Size: A3	Document Number: Fonseca 14.1" DIS	Rev: X01
Date: Friday, October 30, 2009	Sheet: 62	of: 92

SSID = USB

S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

09/0429



<Core Design>

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Taipai Hsien 221, Taiwan, R.O.C.

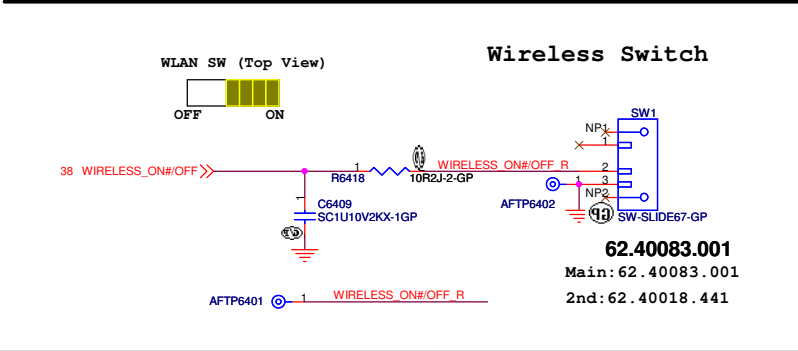
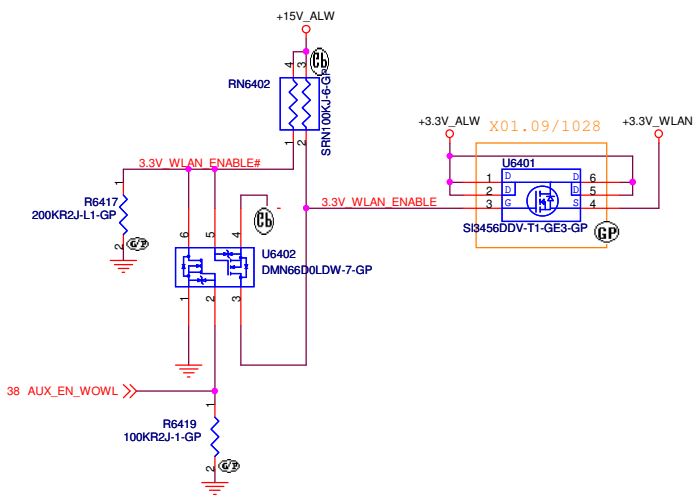
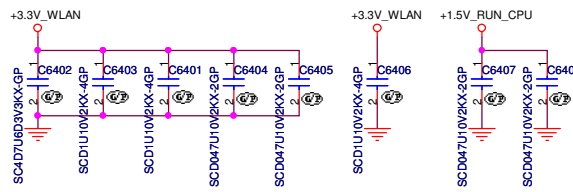
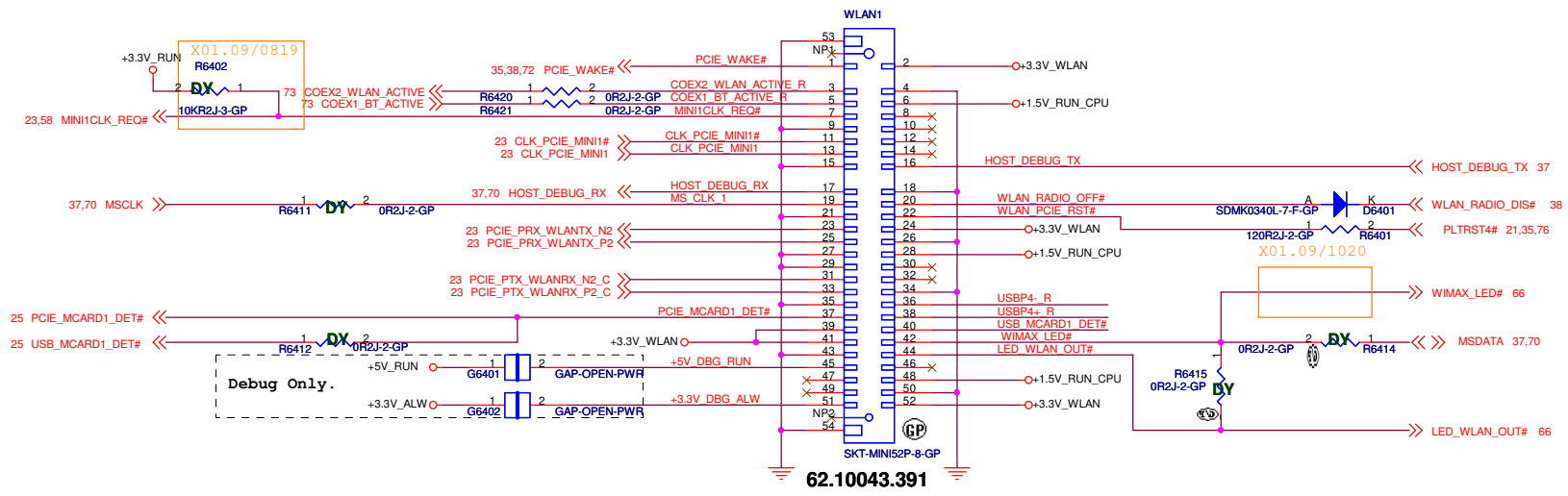
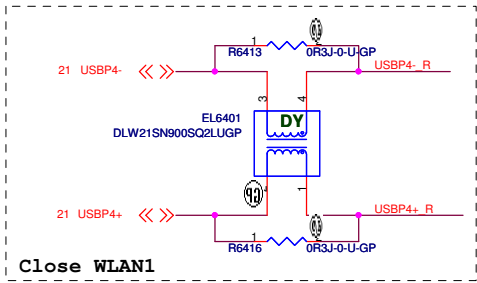
Title: **USB**

Size: Custom Document Number: **Fonseca 14.1" DIS** Rev: **X01**

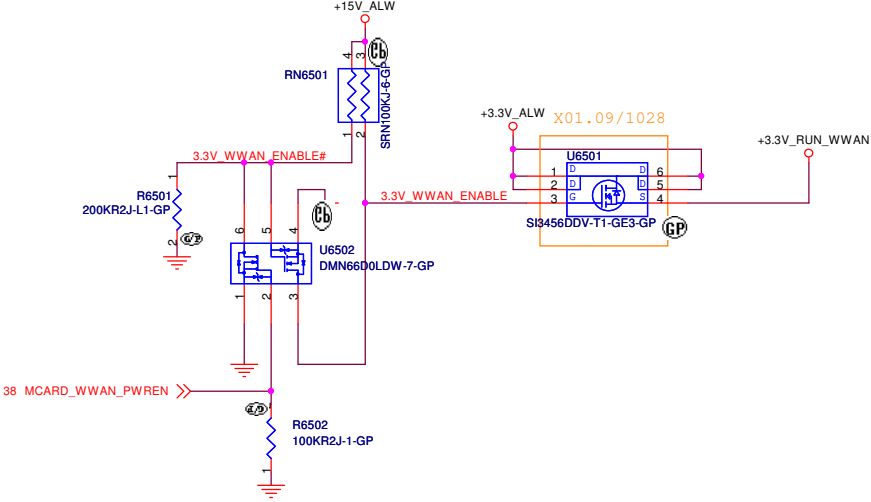
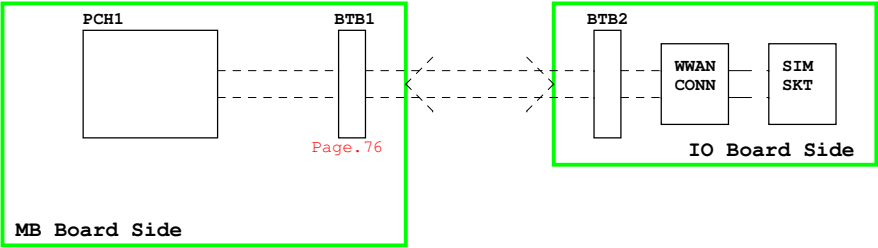
Date: Monday, November 02, 2009 Sheet 63 of 92

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

DEBUG PINS



SSID = Wireless

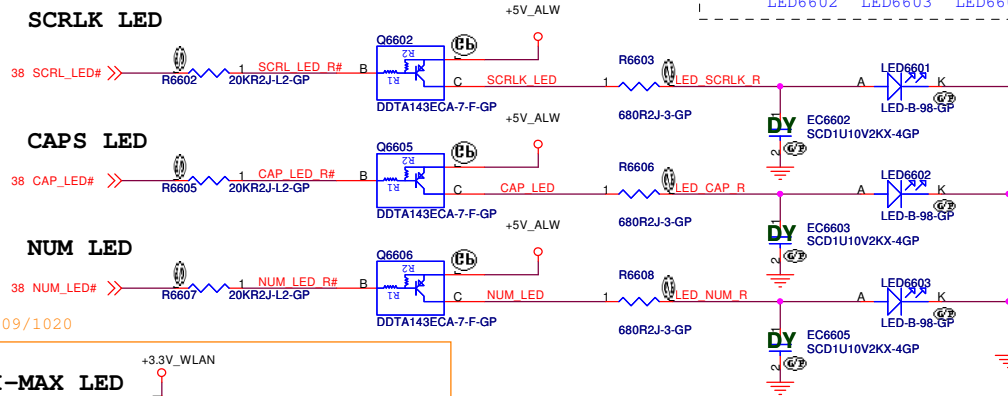


SSID = User.interface

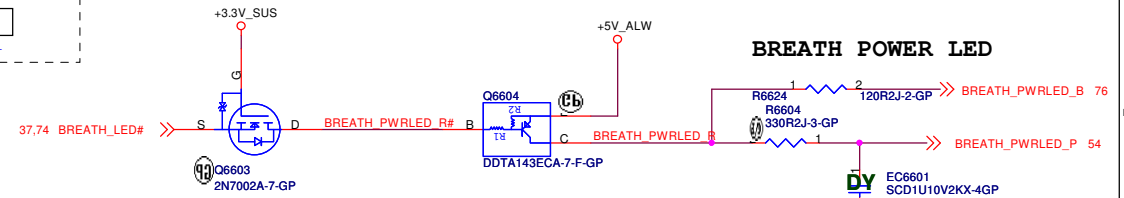
LED Location from left to right
(MB, Top View)

CAPS NUM SCRLK
LED6602 LED6603 LED6601

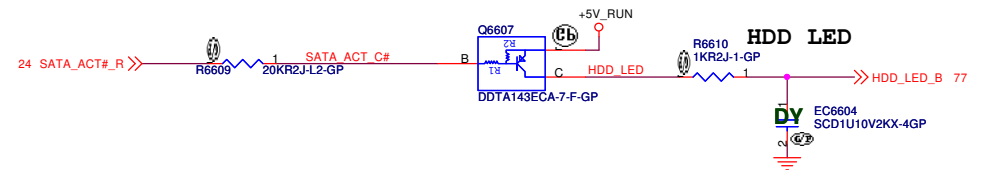
SCRLK LED



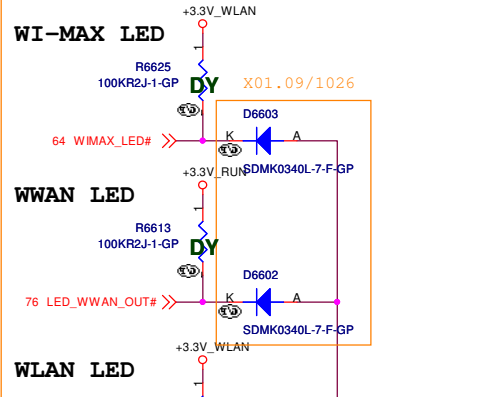
BREATH POWER LED



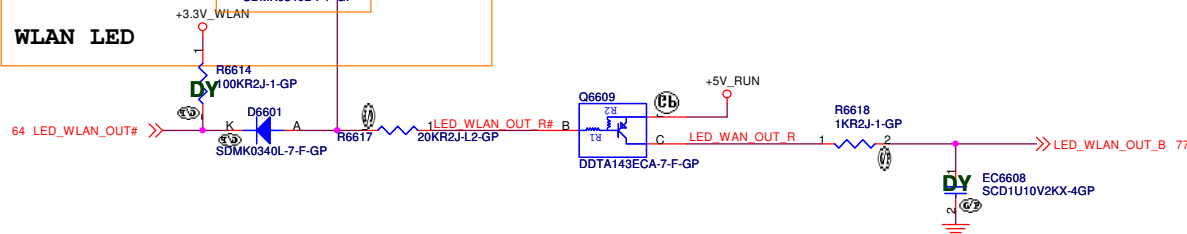
HDD LED



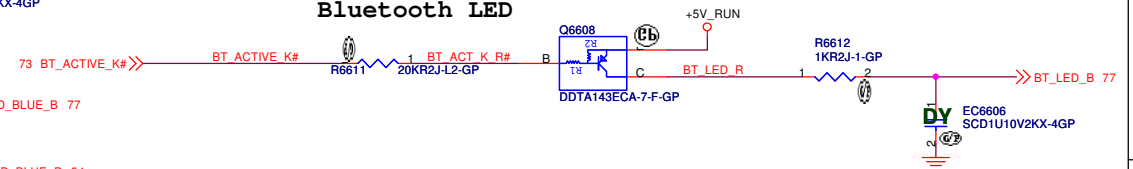
WI-MAX LED



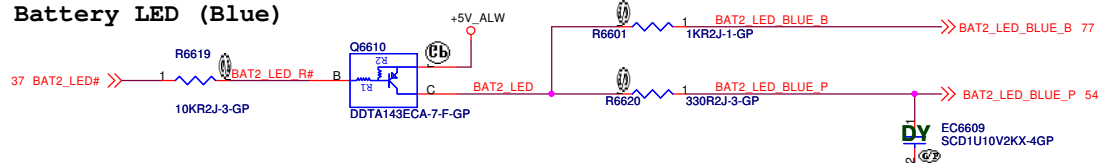
WLAN LED



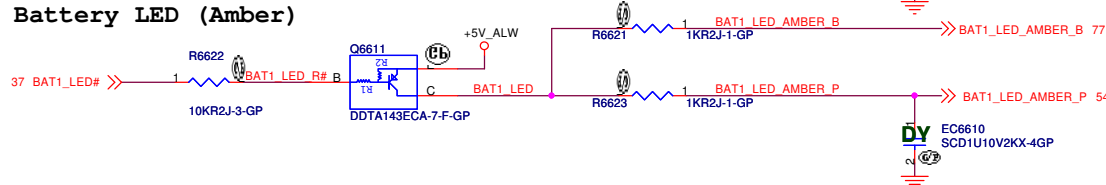
Bluetooth LED



Battery LED (Blue)



Battery LED (Amber)

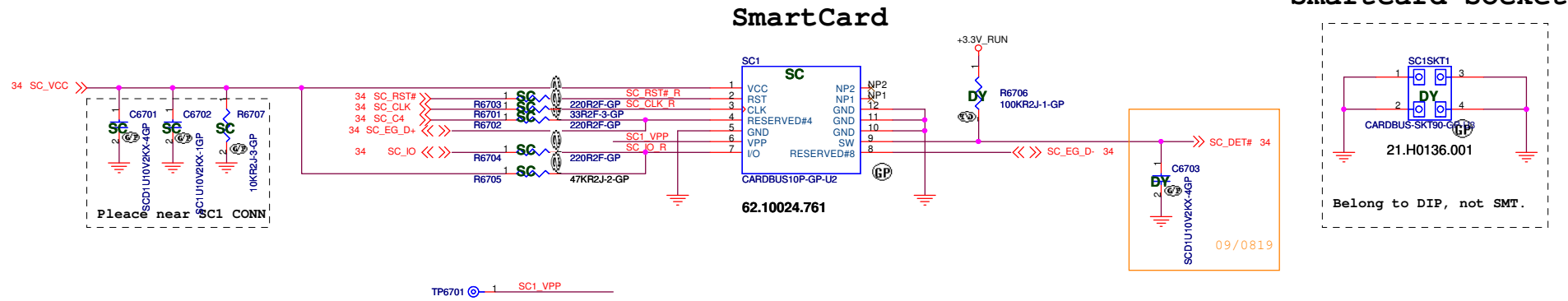


<Core Design>

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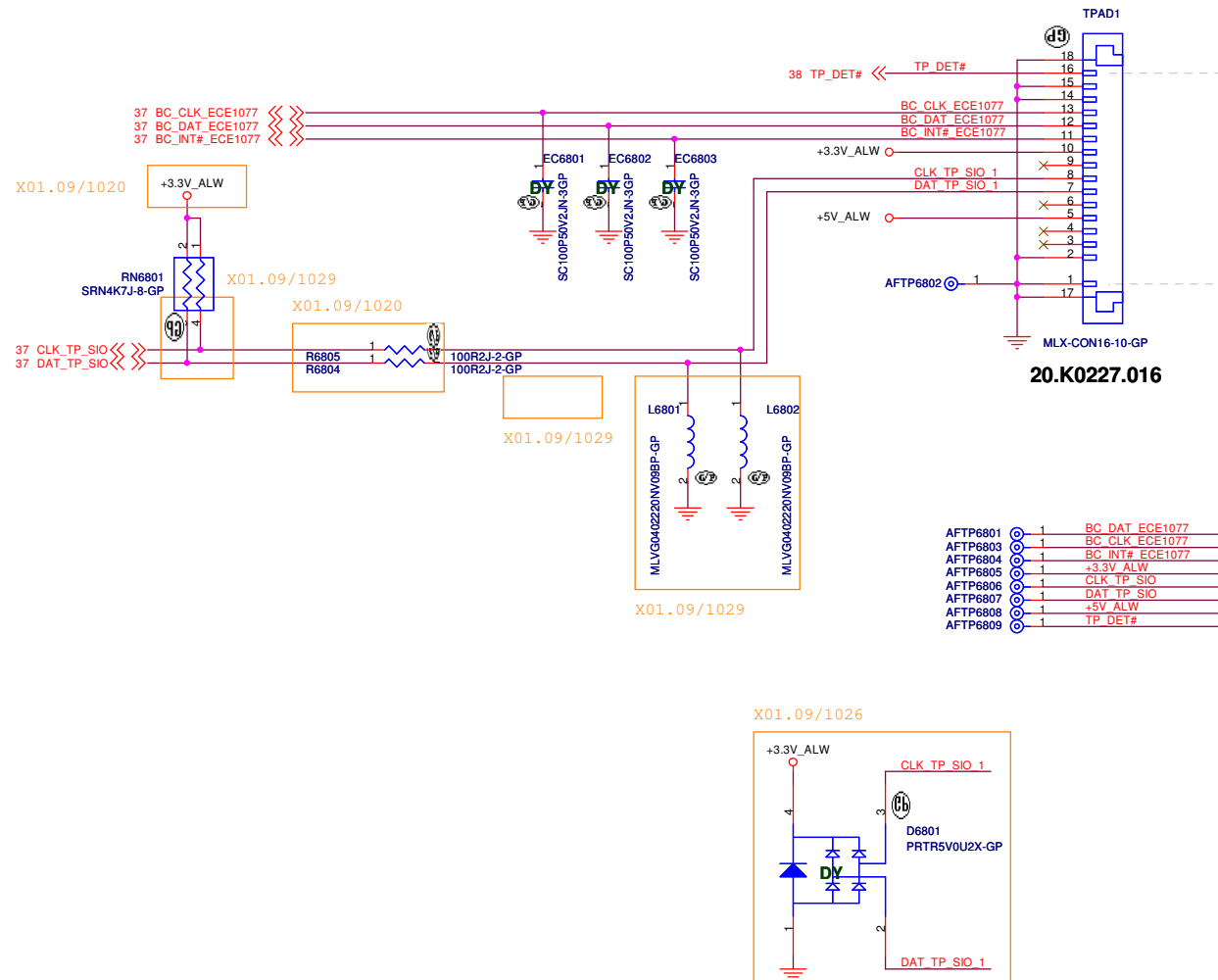
Title			LED	
Size	Document Number	Fonseca 14.1" DIS		Rev
A3				X01
Date:	Thursday, October 29, 2009	Sheet	66	of 92

SSID = SmartCard



SSID = Touch.Pad

TouchPad Connector



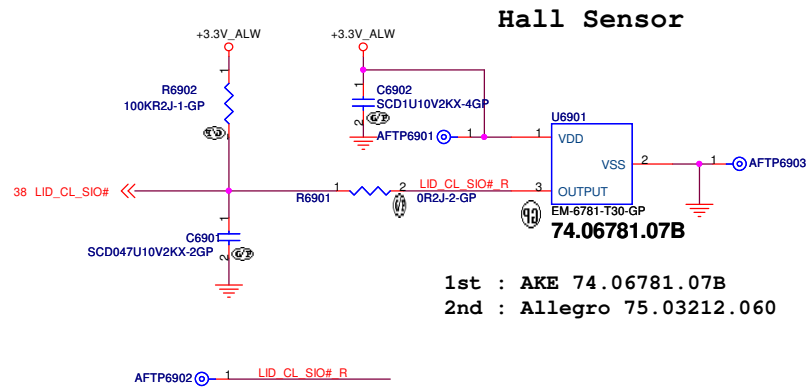
Touch PAD Module Side

- | | |
|----|----------------------------|
| 16 | TP_DET# |
| 15 | GND |
| 14 | GND |
| 13 | BC_CLK (ECE1077) |
| 12 | BC_DAT (ECE1077) |
| 11 | BC_INT# (ECE1077) |
| 10 | 3.3V_ALW |
| 09 | 3.3V_RUN (Internal NC) |
| 08 | PS2_CLK |
| 07 | PS2_DATA |
| 06 | 5V_RUN (Backlight, No Use) |
| 05 | 5V_ALW |
| 04 | PWM (Backlight, No Use) |
| 03 | GND (Backlight, No Use) |
| 02 | GND |
| 01 | Diag_loop |

- | | | |
|----------|---|-----------------|
| AFTP6801 | 1 | BC_DAT ECE1077 |
| AFTP6803 | 1 | BC_CLK ECE1077 |
| AFTP6804 | 1 | BC_INT# ECE1077 |
| AFTP6805 | 1 | +3.3V_ALW |
| AFTP6806 | 1 | CLK_TP_SIO |
| AFTP6807 | 1 | DAT_TP_SIO |
| AFTP6808 | 1 | +5V_ALW |
| AFTP6809 | 1 | TP_DET# |

<Core Design>

```
SSID = User.interface
```



1st : AKE 74.06781.07B
2nd : Allegro 75.03212.060



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	Title
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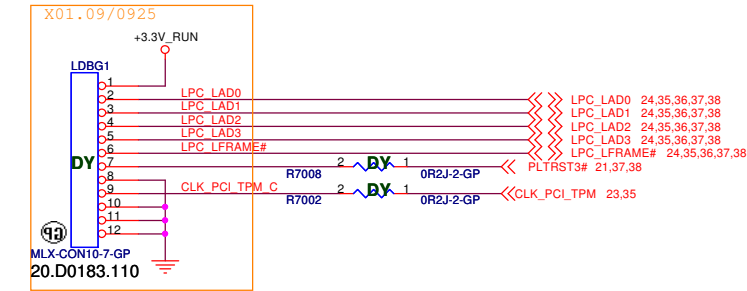
Hall Sensor

Size A3	Document Number
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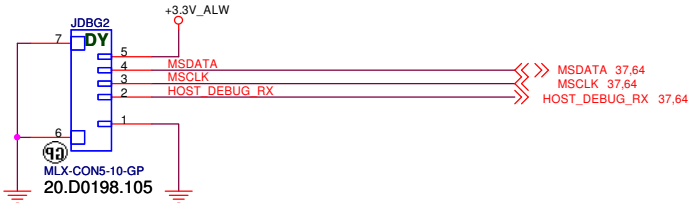
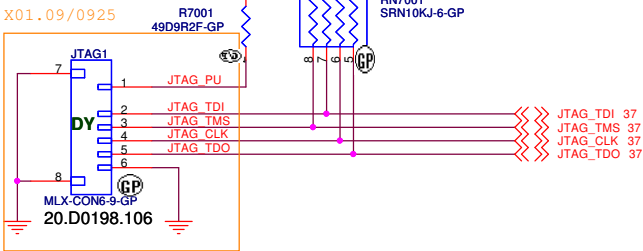
Fonseca 14.1" DIS

Rev
X01

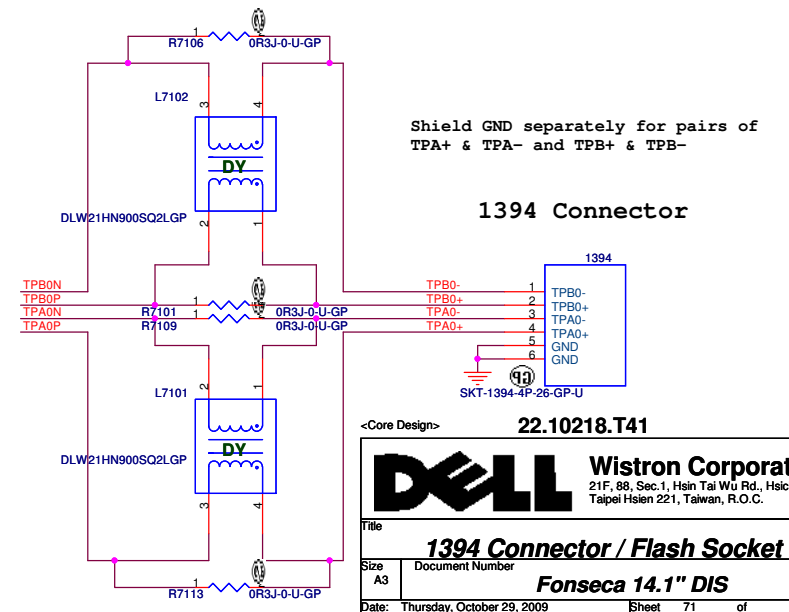
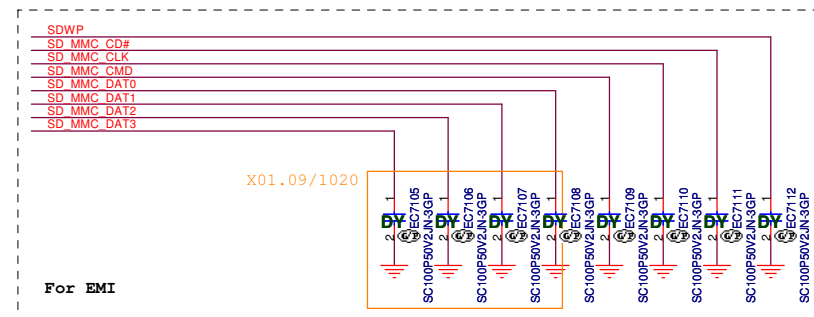
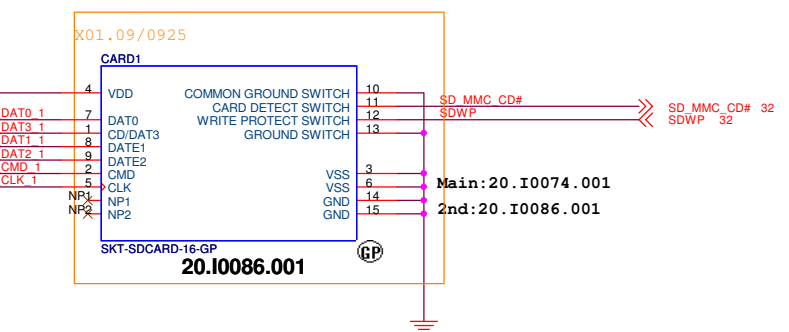
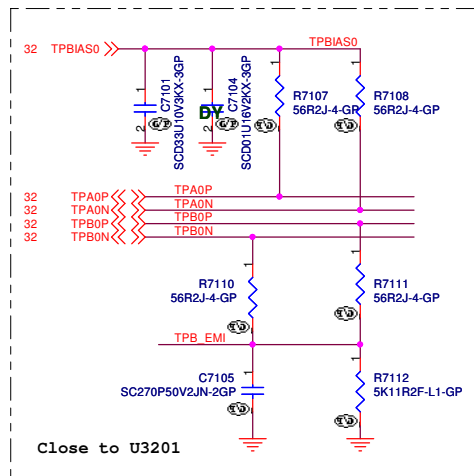
LPC Debug port



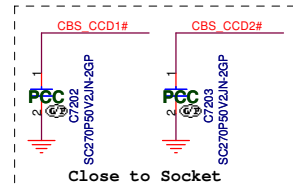
JTAG Debug port



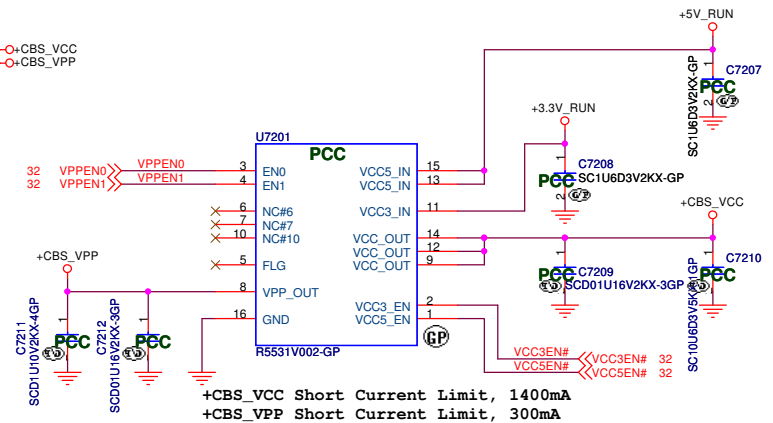
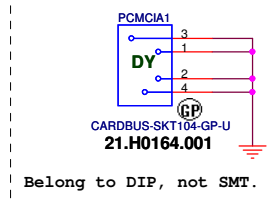
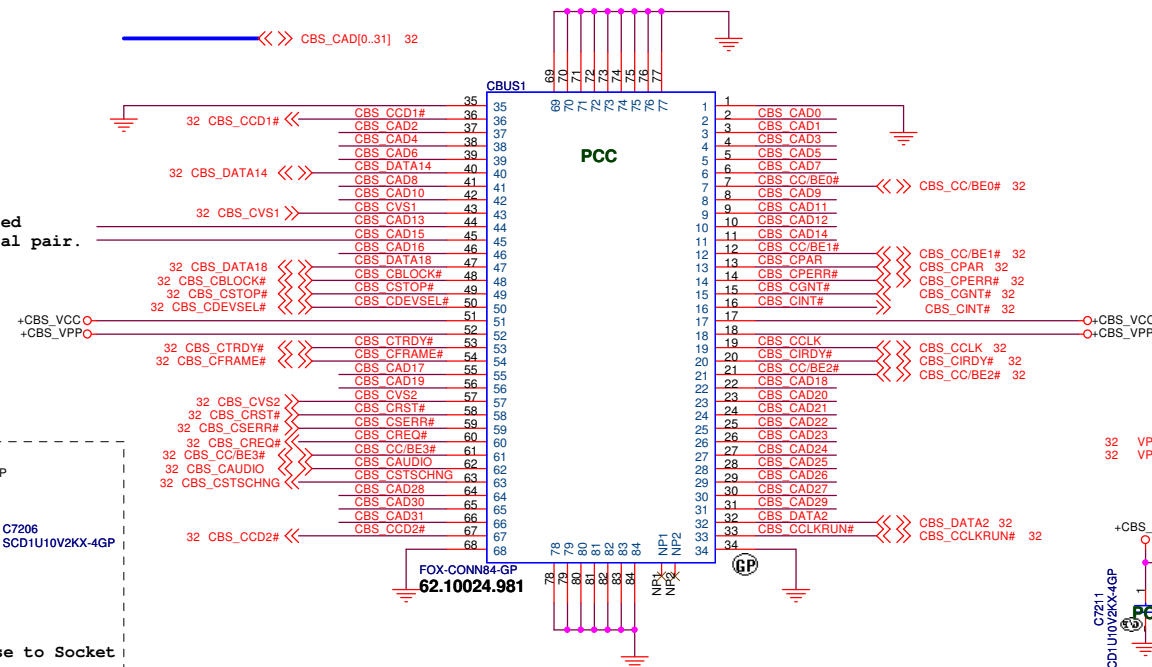
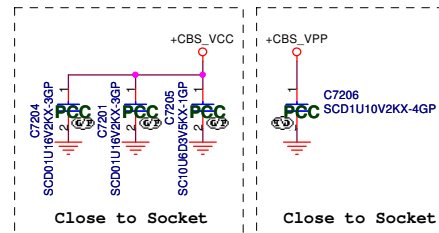
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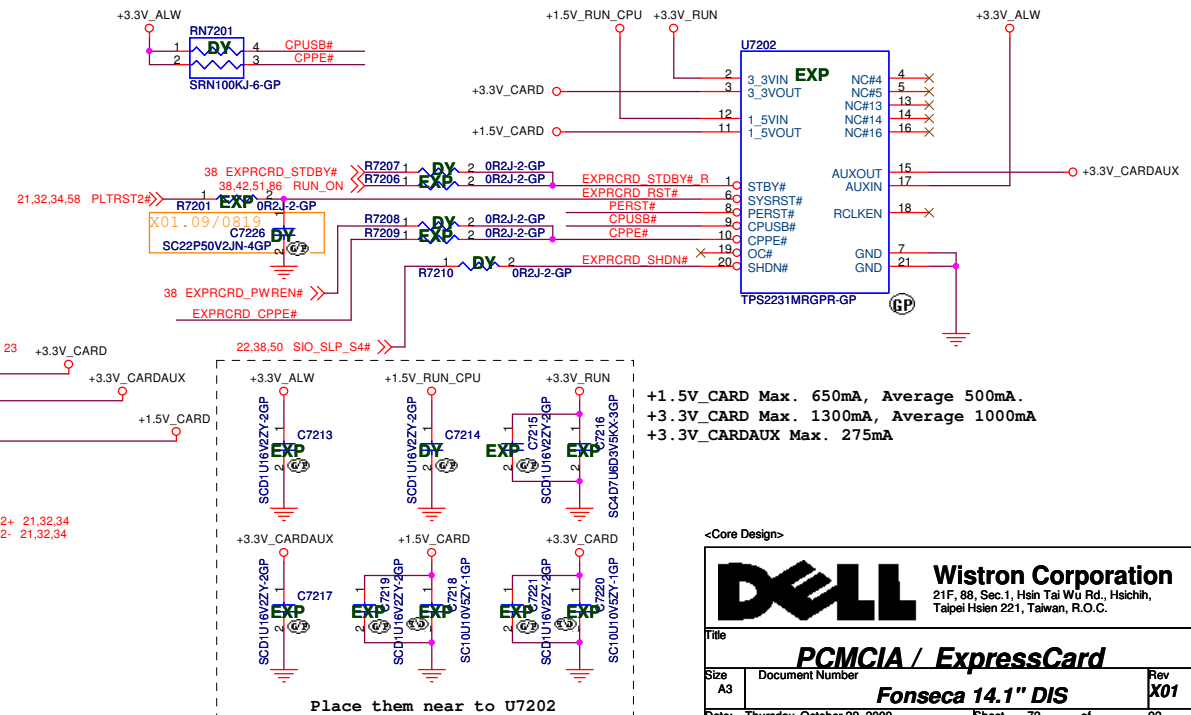
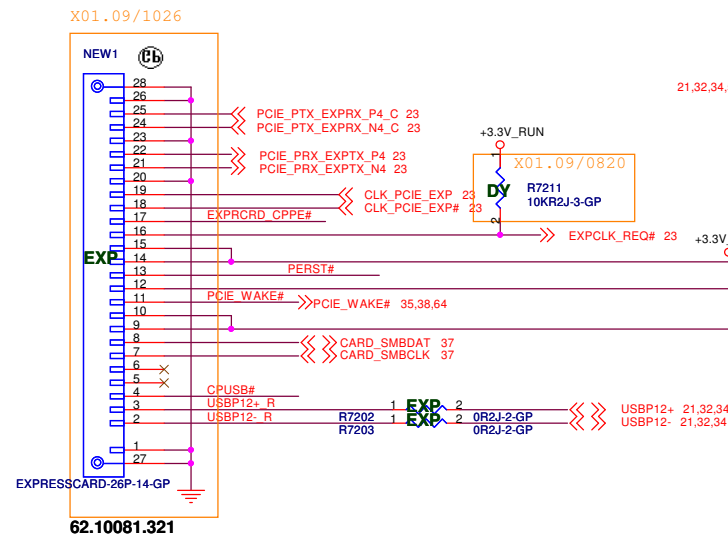
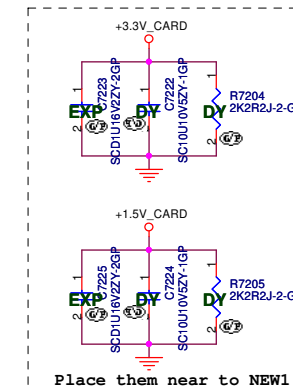
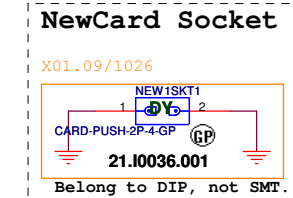
SSID = CARDBUS



CBS_CAD13, CBS_CAD15 Can be used
as Express Card USB differential pair.



```
SSID = ExpressCard
```



```
| +1.5V_CARD Max. 650mA, Average 500mA.  
| +3.3V_CARD Max. 1300mA, Average 1000mA  
| +3.3V_CARDAUX Max. 275mA
```

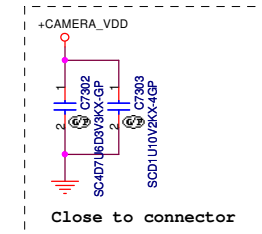
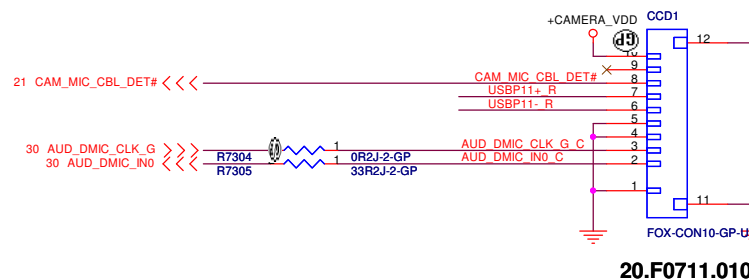
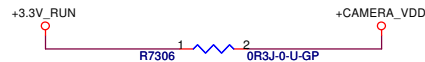
<Core Design>

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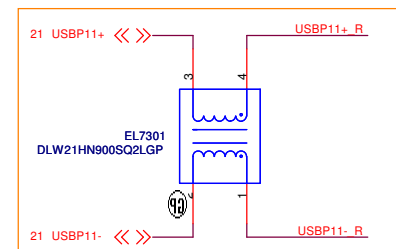
Title **PCMCIA / ExpressCard**

Size A3	Document Number Fonseca 14.1" DIS	Rev X01
Date: Thursday, October 29, 2009	Sheet 72 of 92	

User.interface

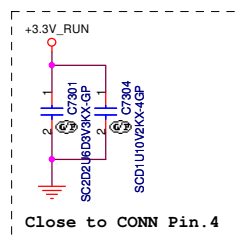


X01.09/1029



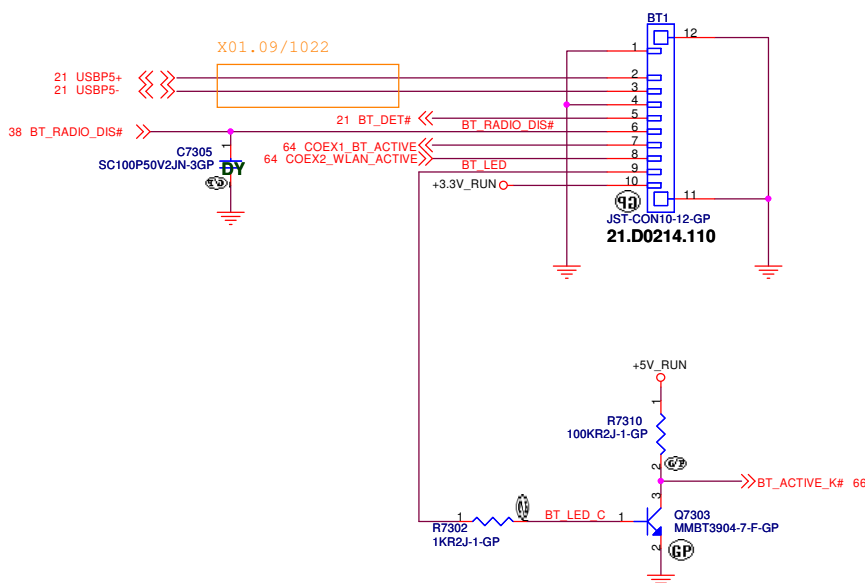
AFTP7301 1 +CAMERA_VDD
AFTP7302 1 USBP11+_R
AFTP7303 1 USBP11+_R
AFTP7304 1 CAM_MIC_CBL_DET#
AFTP7305 1 AUD_DMIC_CLK_G_C
AFTP7306 1 AUD_DMIC_IN0_C

User.interface



AFTP7307 1 +3.3V_RUN
AFTP7308 1 COEX1_BT_ACTIVE
AFTP7309 1 COEX2_WLAN_ACTIVE
AFTP7310 1 USBP5+_R
AFTP7311 1 BT_RADIO_DIS#
AFTP7312 1 BT_LED
AFTP7313 1 BT_DET#

Bluetooth Connector



MB BT CONN

PIN	Define	PIN	Define
1	GND	1	GND
2	USBP5+_R	12	USB_DP
3	USBP5-_R	11	USB_DN
4	GND	10	GND
5	BT_DET#	2	MOD_DET
6	BT_RADIO_DIS#	7	RADIO_DIS
7	COEX1_BT_ACTIVE	3	COEX1_BT_ACTIVE
8	COEX2_WLAN_ACTIVE	8	COEX2_WLAN_ACT
9	BT_LED	6	LINK_IND
10	+3.3V_RUN	9	3.3V

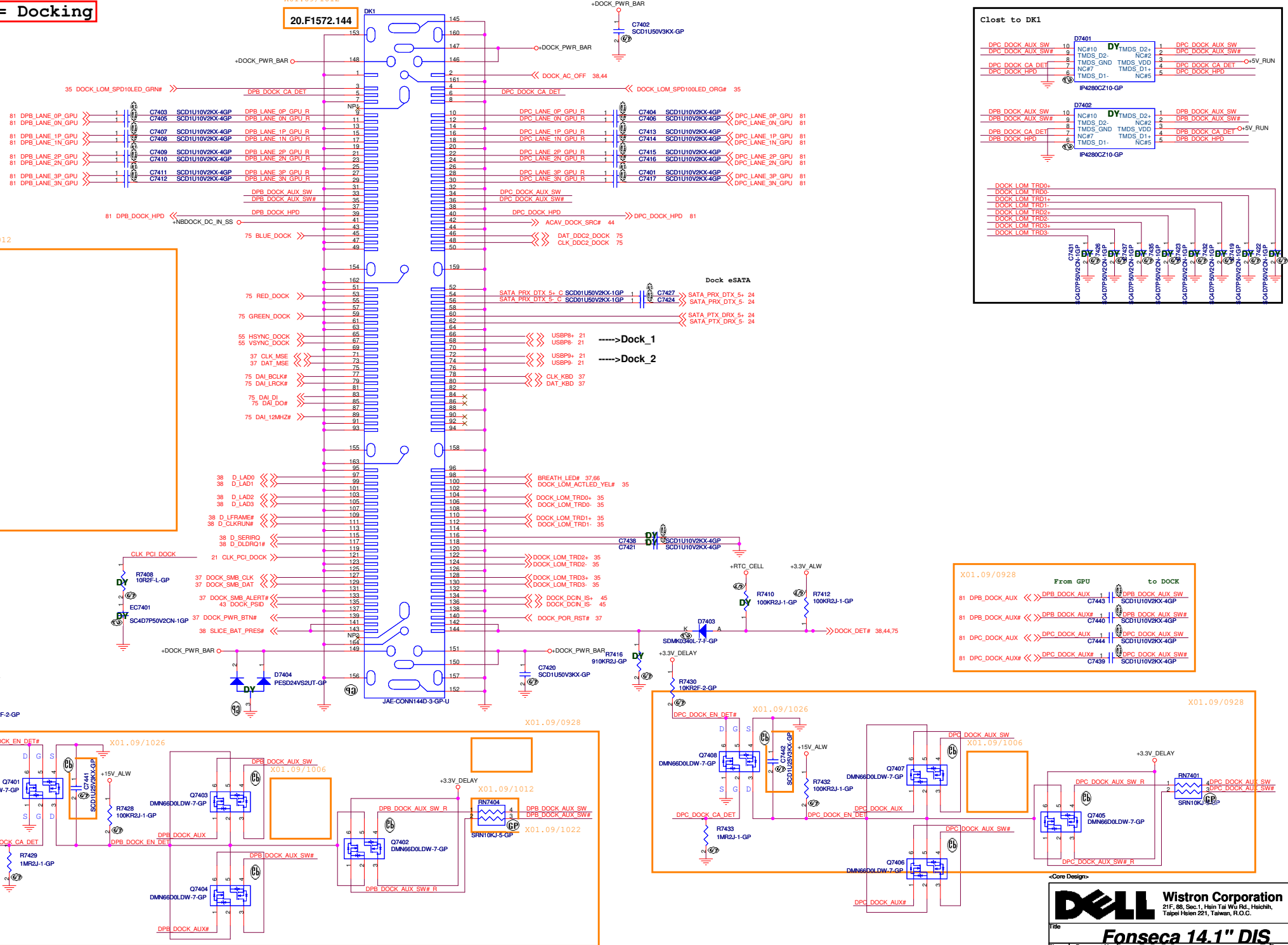
<Core Design>



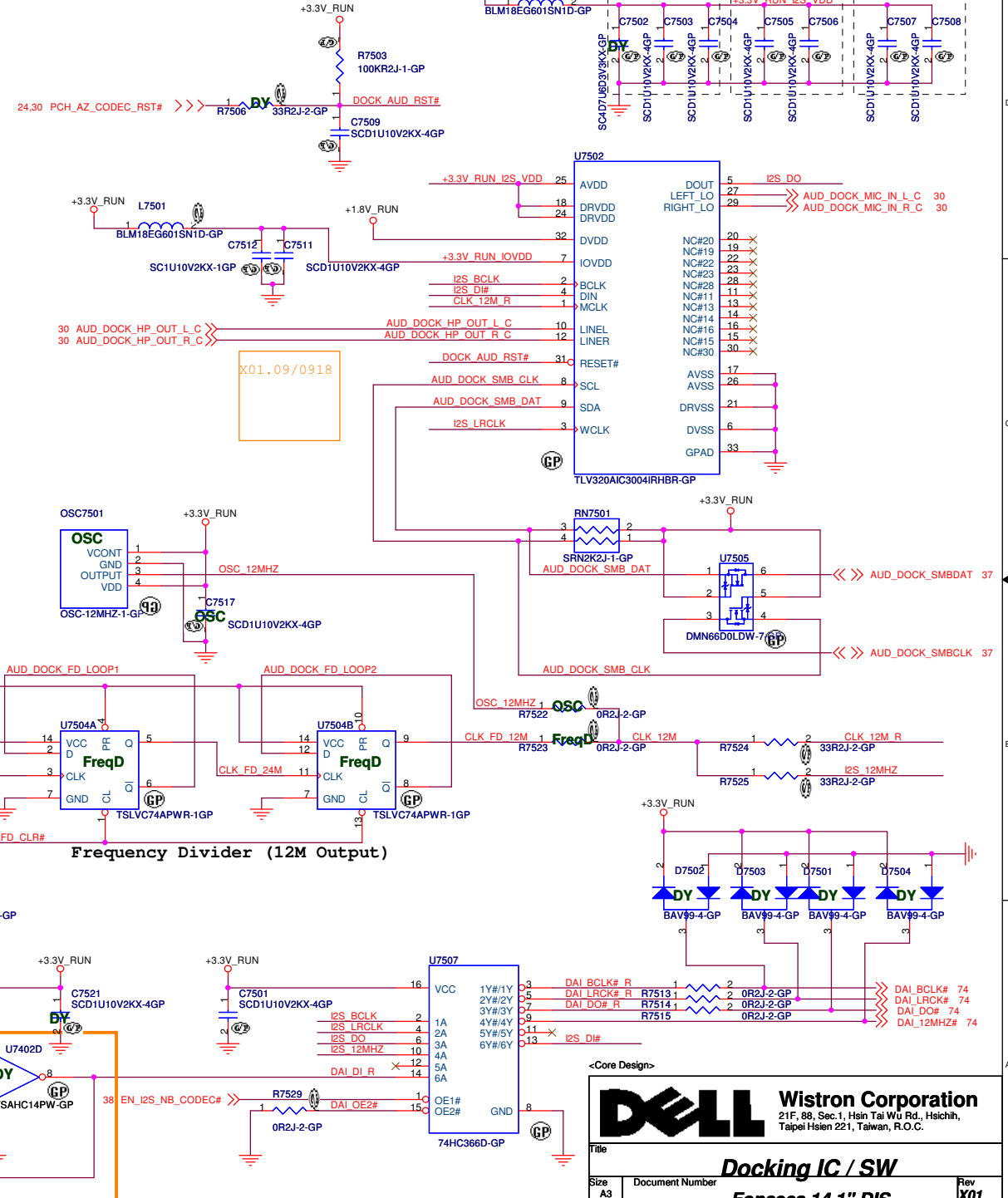
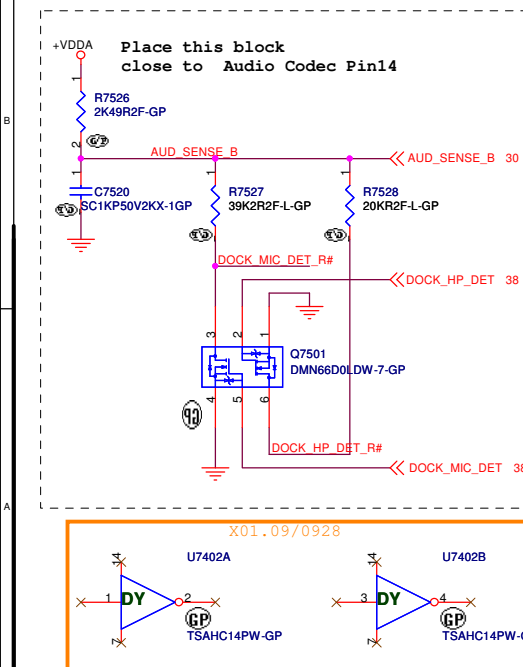
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Title	Bluetooth / Camera / DMIC		
Size A3	Document Number	Rev X01	
Date: Thursday, October 29, 2009	Sheet 73	of 92	

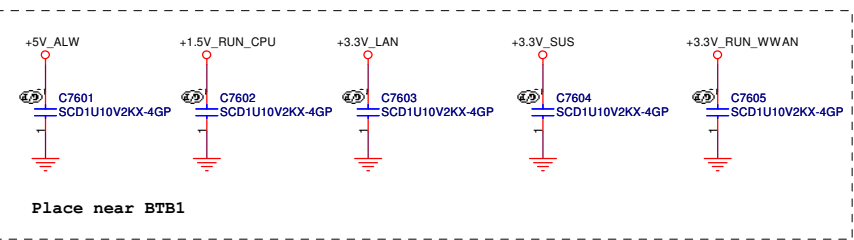
SSID = Docking



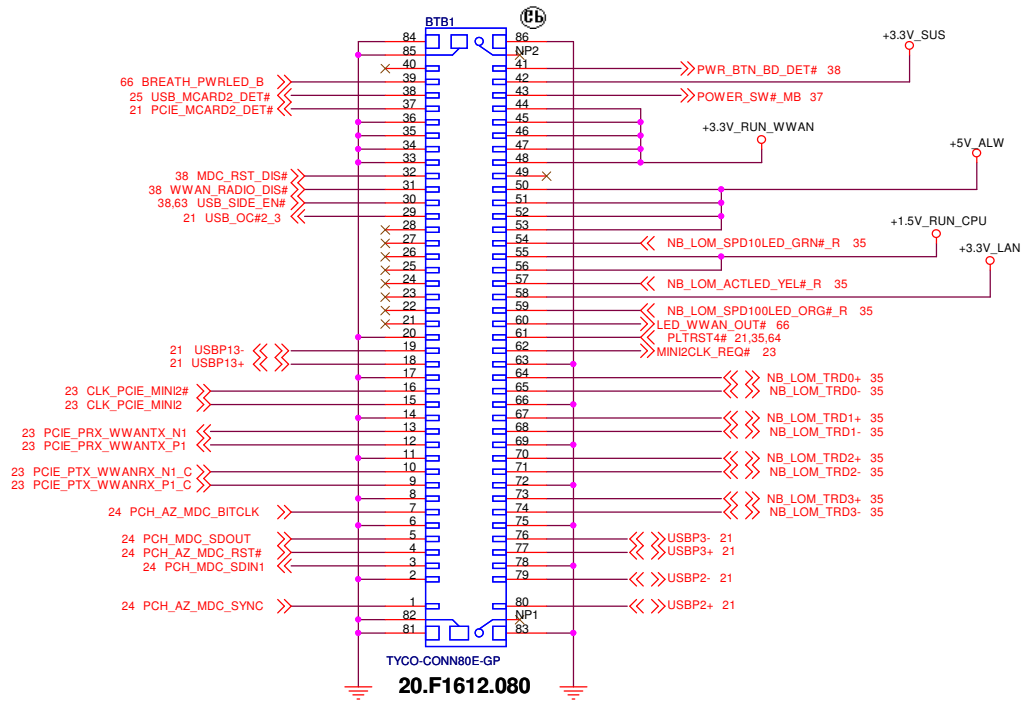
SSID = DOCK AUDIO



SSID = User.Interface

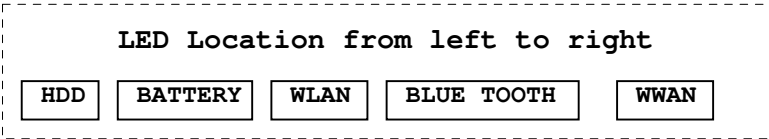
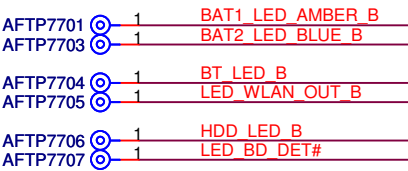
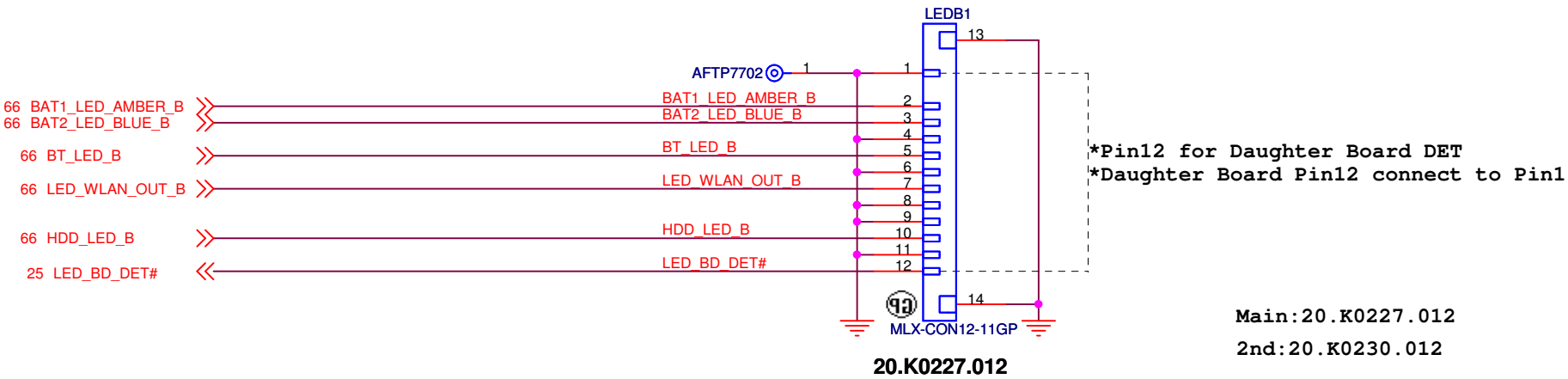


IO Board Connector



SSID = User.interface

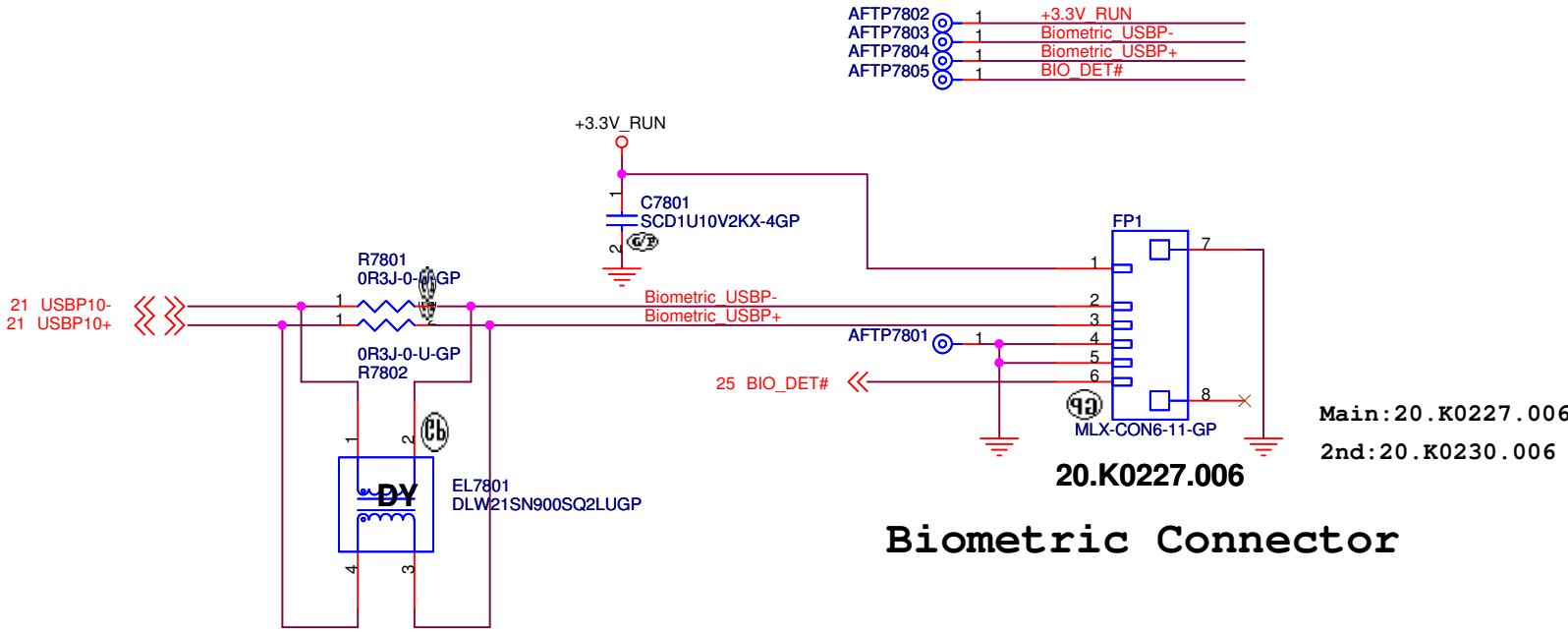
LED BD Connector



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LED Board Connector			
Size A4	Document Number Fonseca 14.1" DIS		Rev X01
Date: Thursday, October 29, 2009		Sheet 77 of 92	

SSID = User.Interface



Biometric Connector

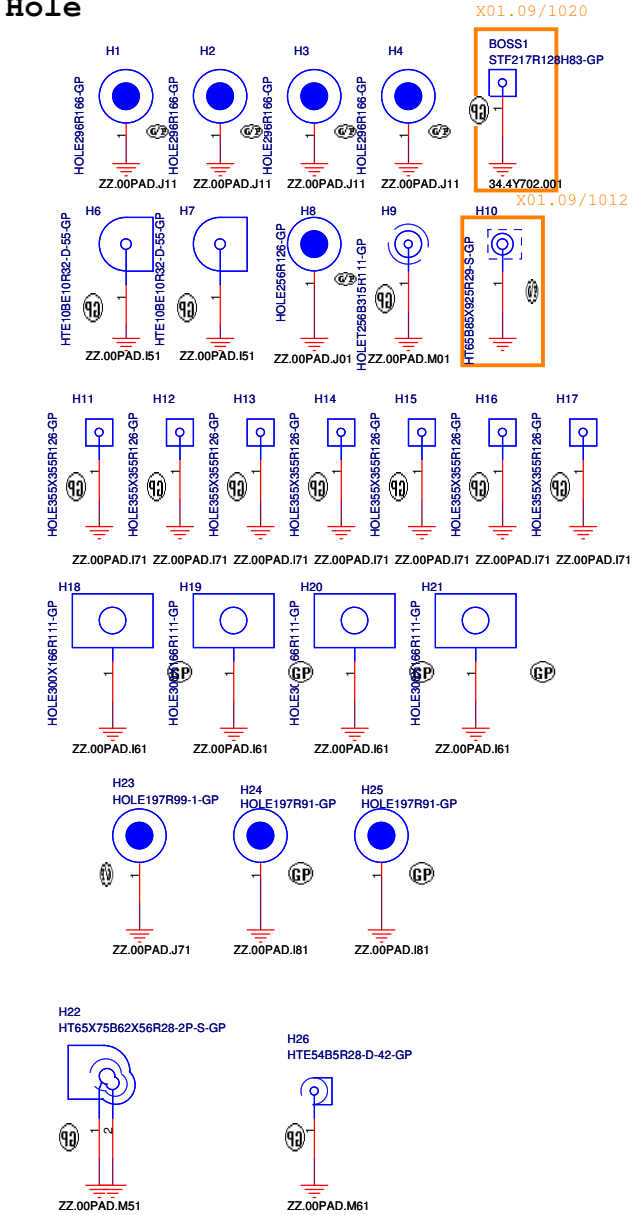
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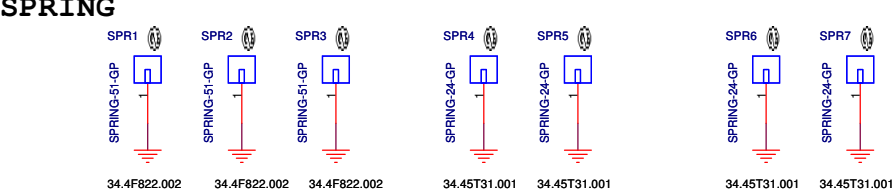
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Finger Printer Board CONN		
Size A4	Document Number	Rev X01
Date: Thursday, October 29, 2009		Sheet 78 of 92

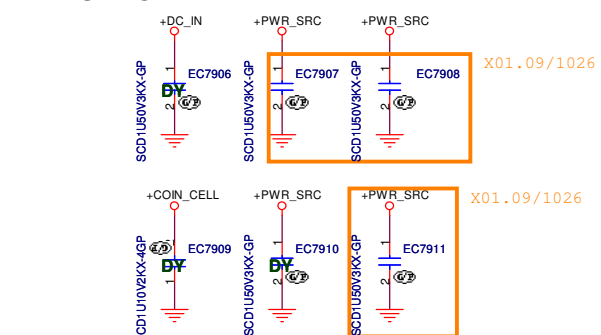
Hole



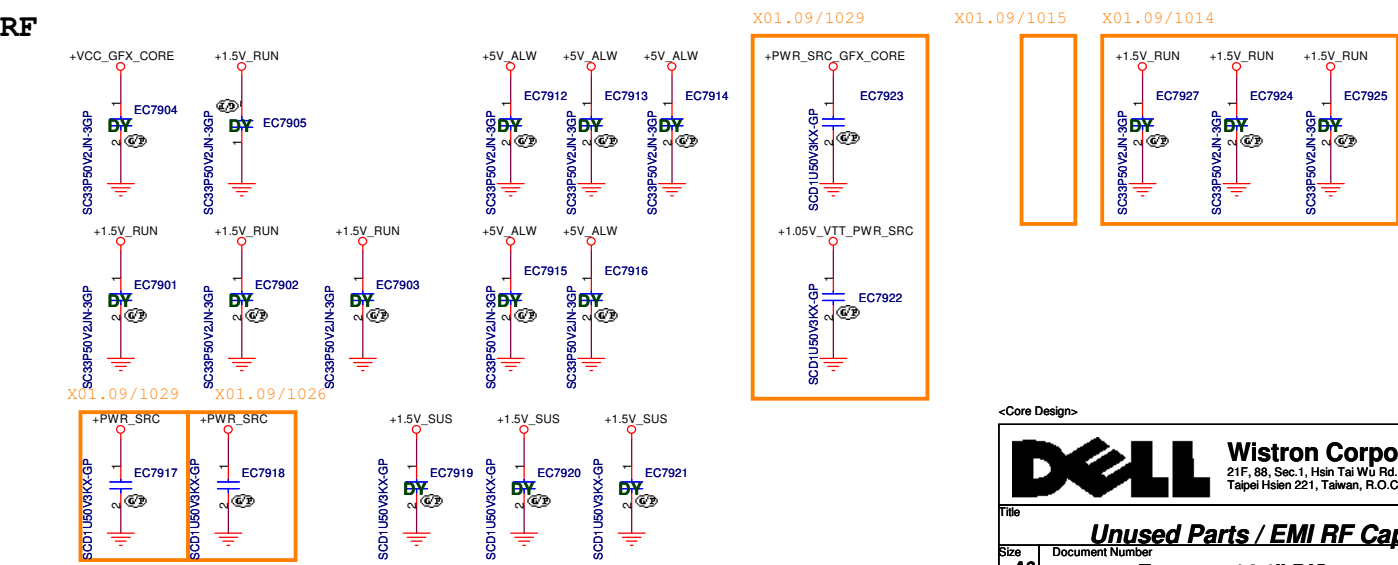
SPRING



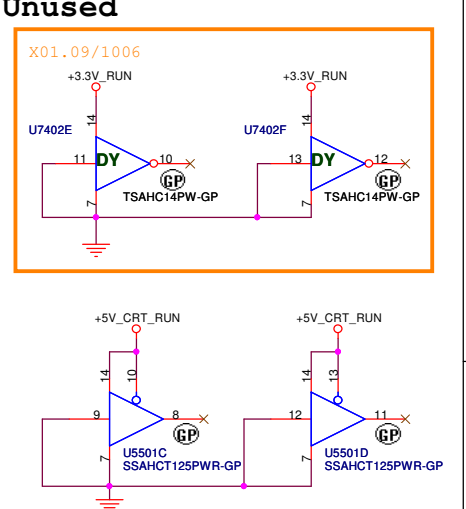
EMI CAPS



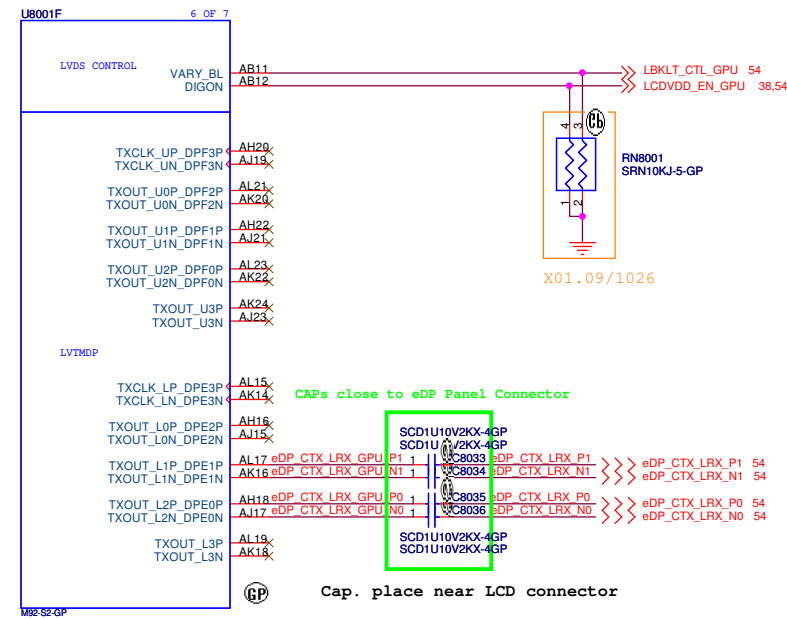
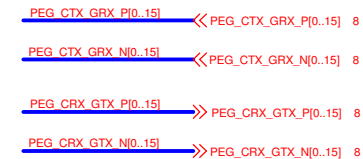
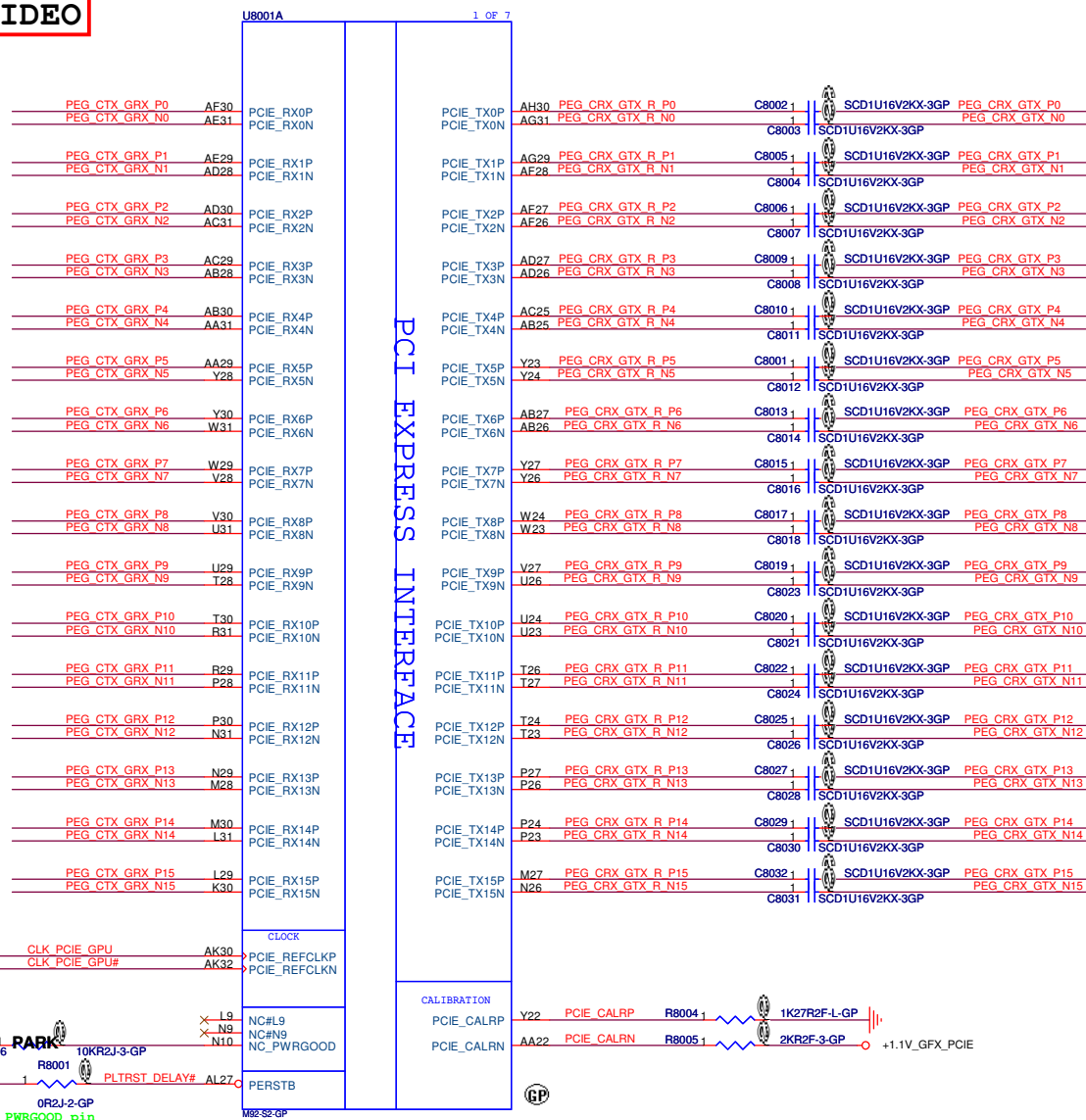
RF



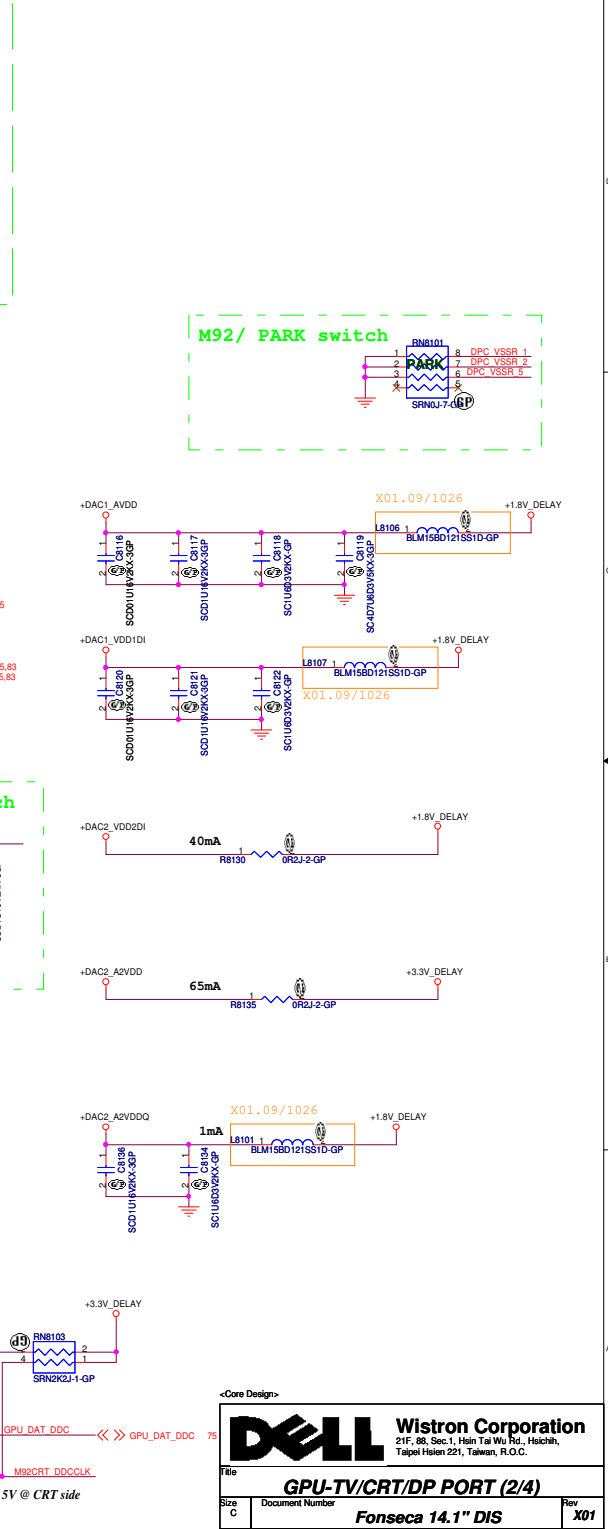
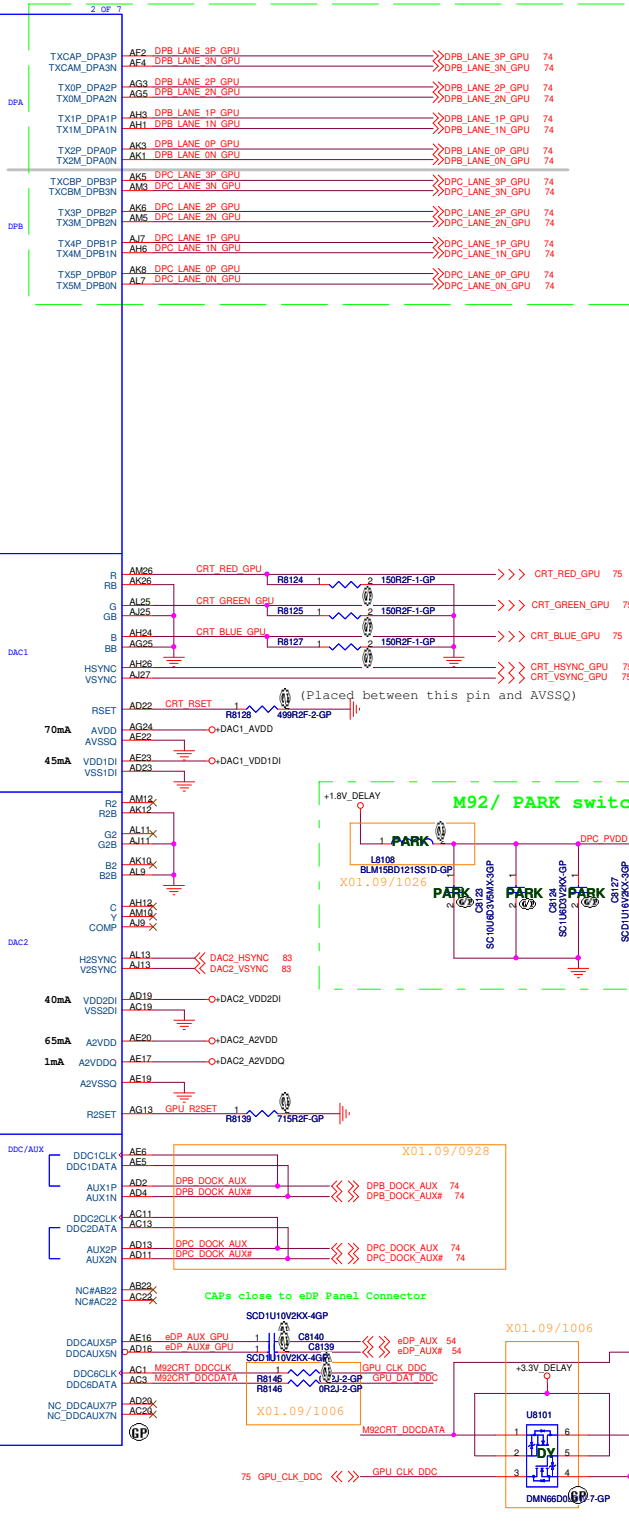
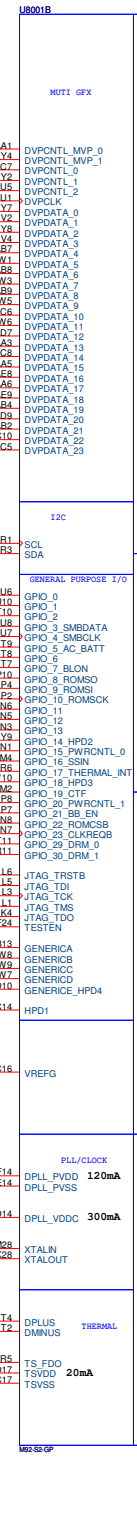
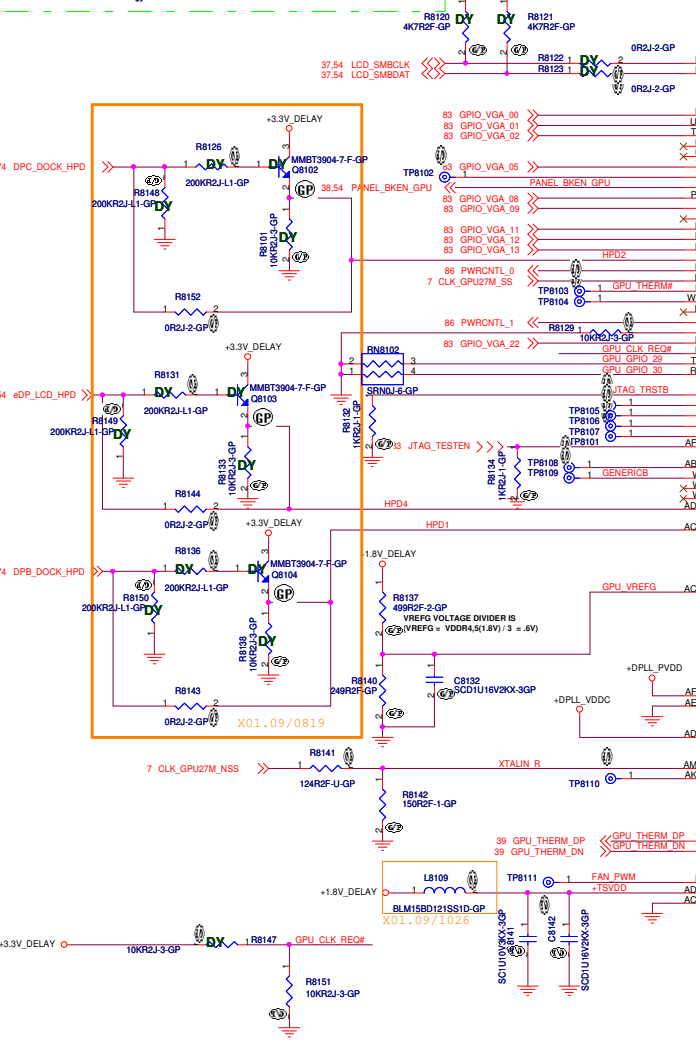
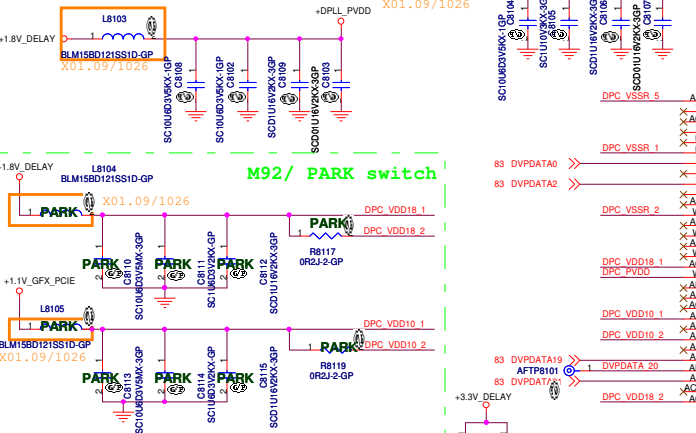
Unused



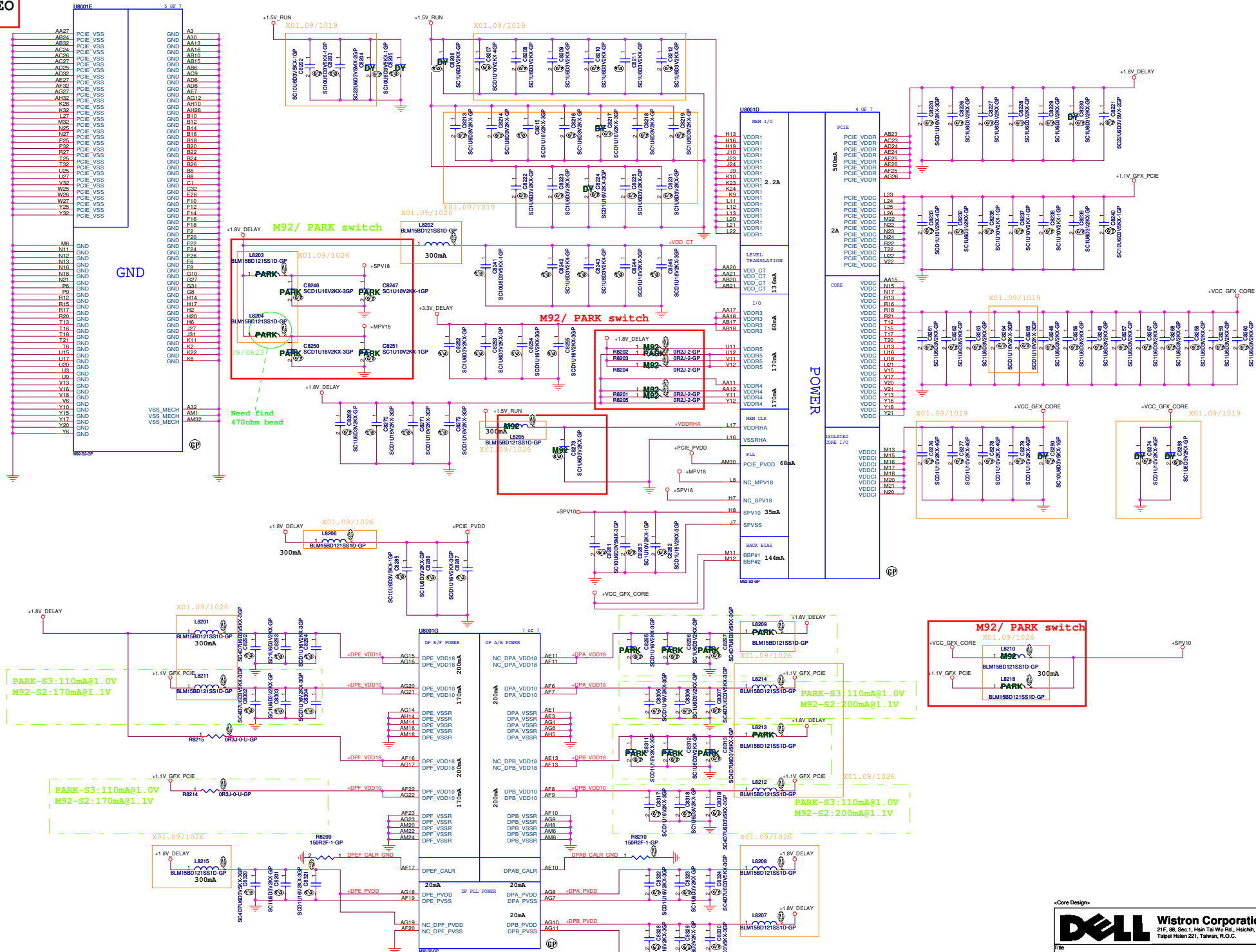
SSID = VIDEO



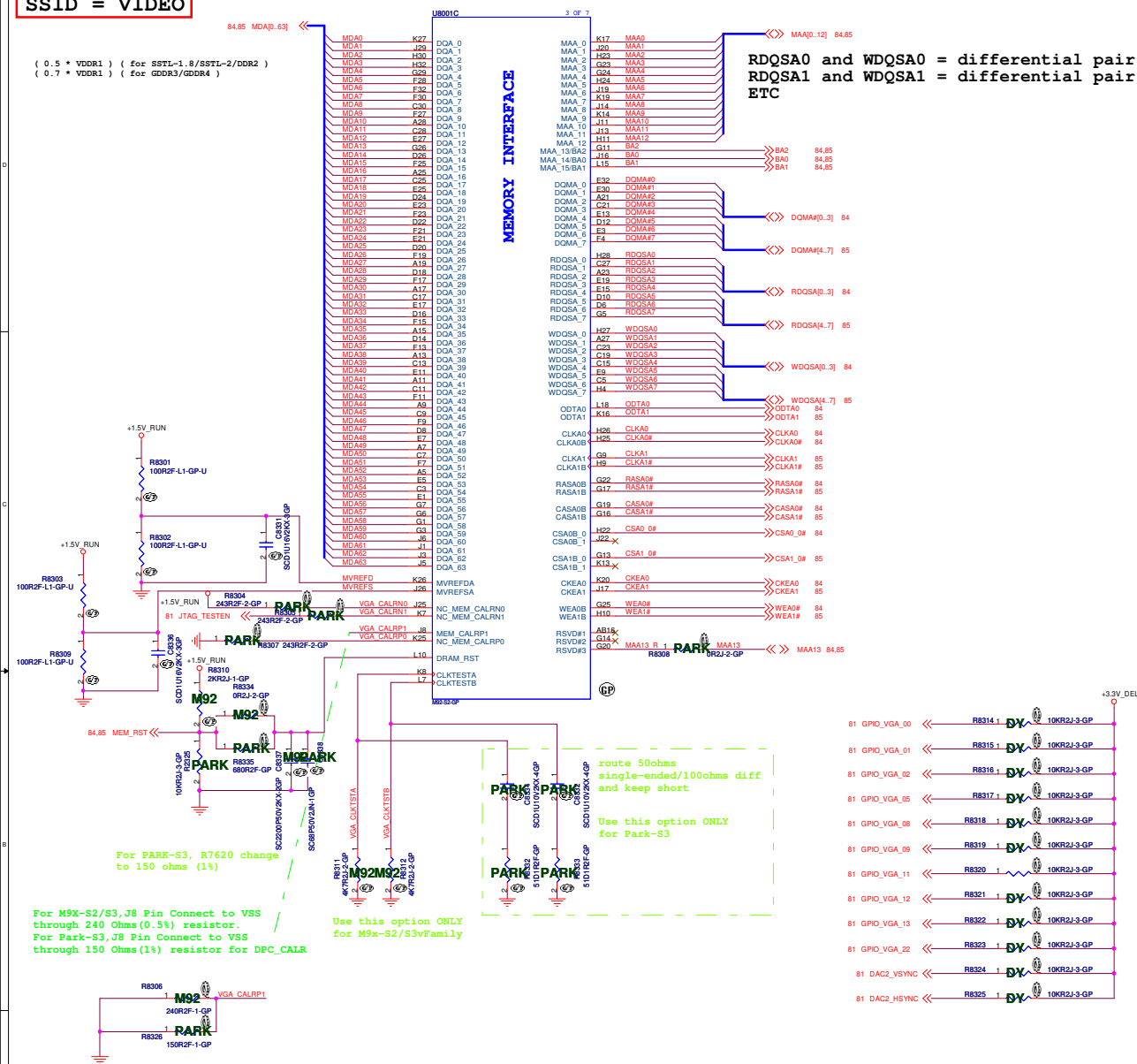
SSID = VIDEO



SSID = VIDEO



SSID = VIDEO

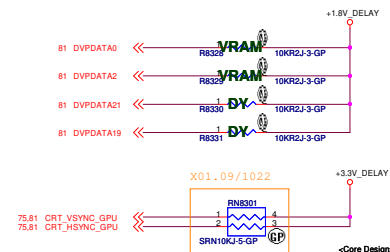


ATI RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE
GPI03, H2SYNC, V2SYNC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO{13,12,11}	Manufacturer	Part Number	GPIO{13,12,11}
V	128MB	x000	M25P05A	0100
	256MB	x001	M25P10A	0101
	64MB	x010	M25P20	0101
	32MB	x	M25P40	0101
	512MB	x	M25P80	0101
	1GB	x		
	2GB	x		
	4GB	x		
		ST Microelectronics		
		Chingis (formerly PMC)	Pm25LV512A Pm25LV010A	0100 0101

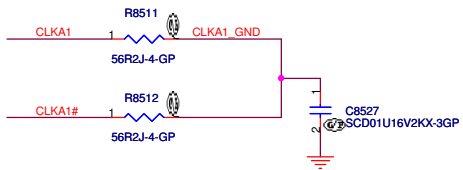
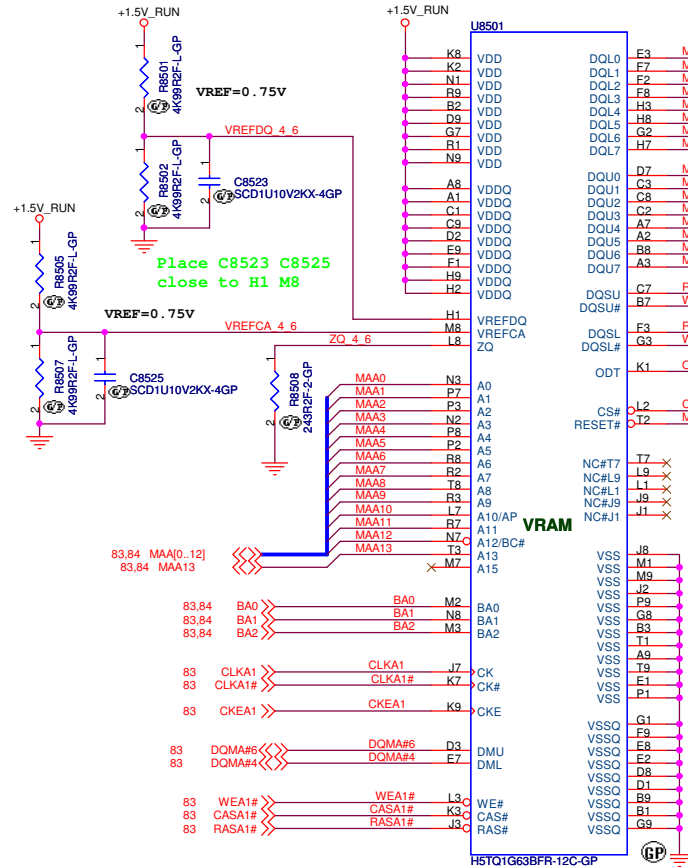
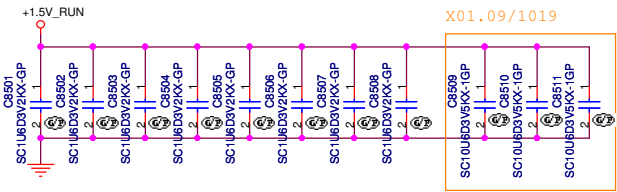
STRAPS	PIN	DESCRIPTION
TX_FWRS_ENB (Internal PD)	GPIO0	V Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	V Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	V0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_FM_EN	GPIO8	V0 = Disable CLKREQ# power management capability 1 = Enable CLKREQ# power management capability
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1 = Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (1 if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI V
GPIO_VGA_05 (Internal PD)		GPIO_5_AC_BATT is an optional input which allows the system to request a fast power reduction by setting GPIO_5_AC_BATT to low (0 V).The resulting state transition may disturb the display momentarily.Power reductions that are less time critical should use the standard software methods only in order to prevent display disturbances. V

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVDPATA(19,21,2,0) (Internal PD)	MEMORY TYPE, MAKE AND SIZE INFO V0000 - gDDR3 64Mx16 Hynix 0001 - gDDR3 64Mx16 Samsung 0010 - gDDR3 128Mx16 Hynix 0011 - gDDR3 128Mx16 Samsung

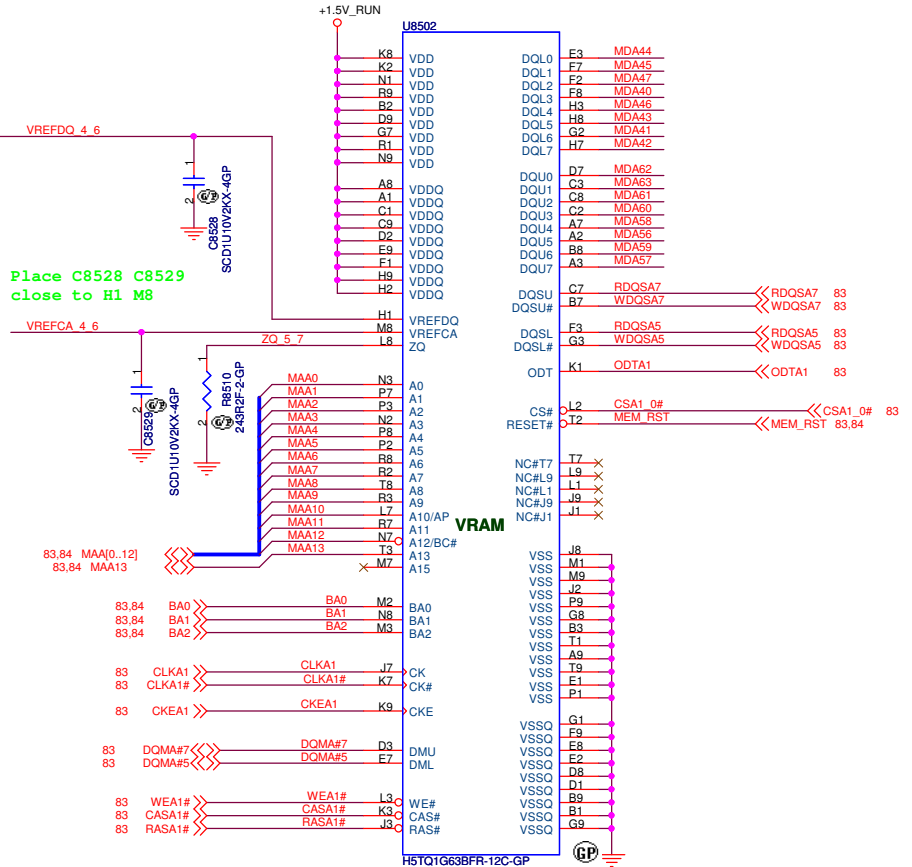
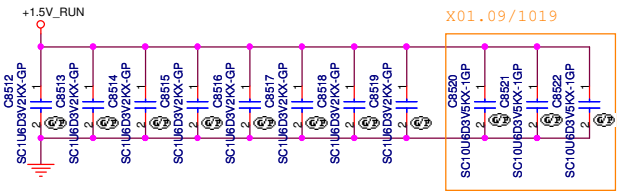


SSID = VIDEO

Place blow decoupling caps close VDD pin.



Place blow decoupling caps close VDD pin.



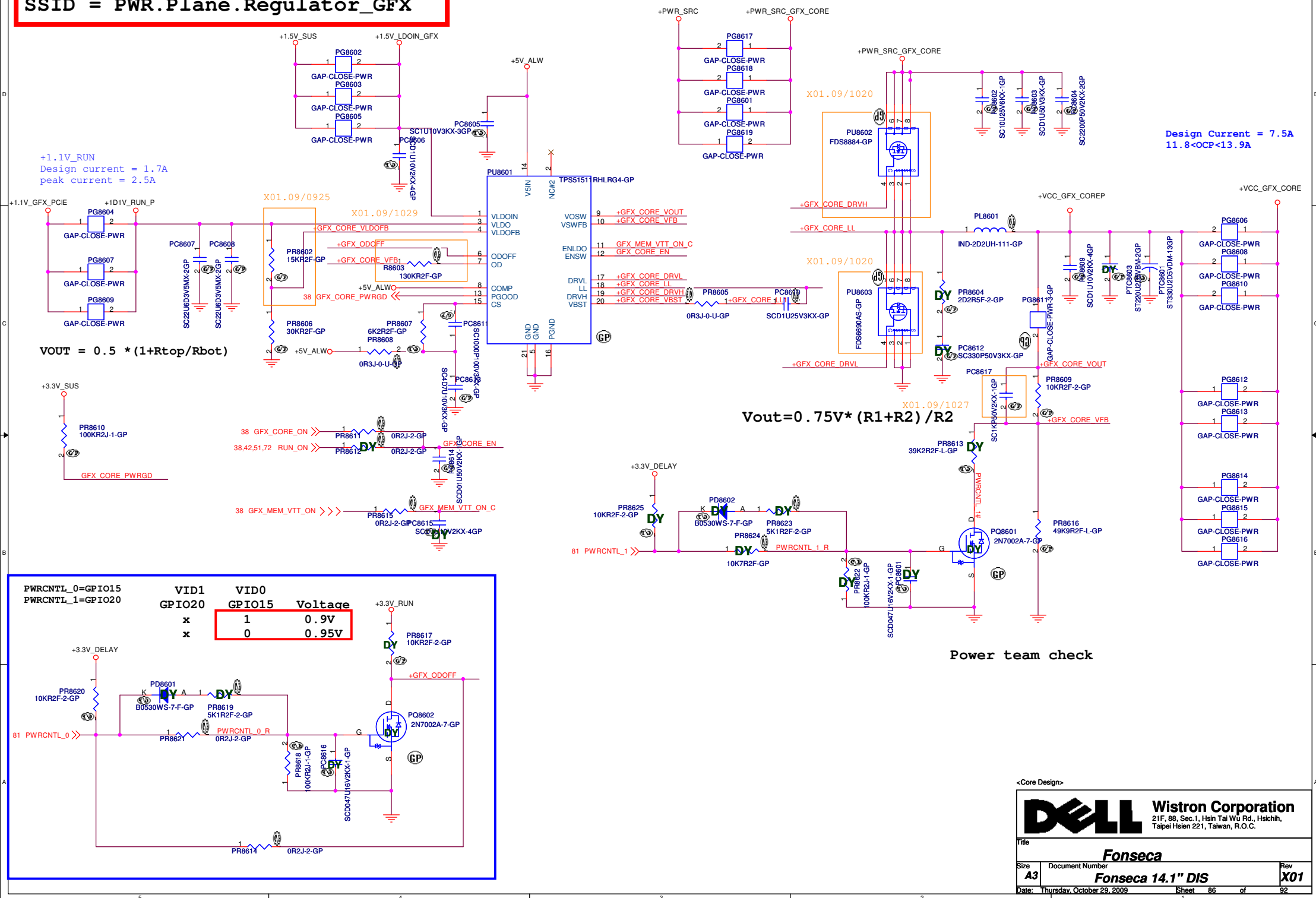
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Title: **VRAM (2/2)**

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SSID = PWR.Plane.Regulator_GFX



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VERSION	DATE	NO	PAGE	Modified List	Issue Description	OWNER
X01	08/19	1	34	Add R3411 C3409 and DY	AC terminal	EE
		2	35	Remove R3541 and pop R3537	BTPM enable control pin	EE
		3	37,38	Remove R3827 and add R3739 for H_SKTOCC# circuit	CPU_DETECT#	EE
		4	42	Change Q4299 Q4208 P/N	Use same MOS&BJT with other part	EE
		5	81	Add R8143 R8144 and R8152 for co-layout and DY HPD circuit	Hot plug detect co-layout 0 ohm	EE
		6	54,64,72	Rename F1 to FUSE5401;Rename R2323 to R6402 Rename R2320 to R7211;Rename C7802 to C7226	For schematic standard rule	EE
		7	47	Update PU4705 symbol	Update PU4705 symbol	POWER
	08/20	8	27,50	Change L2702,L2703,D2701,D2702,PD5001 P/N	Change coil for intel requirment;Change diode for PSL vender	EE
		9	37	Remove R3738	Just for JTAG debug, remove R3738 pull high	EE
		10	67	Add 0.1uF C6703 for SC_DET#	Add 0.1uF for SC_DET#	EE
		11	35	Remove U3506	Remove U3506 for height limit co-layout circuit	EE
		12	37	Change R3703 to 130K	Board Version (X01)	EE
		13	47	DY PR5007	TPS51116 already built-in BST circuit	POWER
		14	81	Remove C8133,C8135,C8137 and C8138	Already have decouple cap at end side	EE
	08/21	15	74	Change R7418,R7419,R7420 and R7421 to 100K	Follow ATI design guide	EE
		16	25	Change R2527 pull high to +3.3V_RUN	Core power rail	EE
	08/24	17	54	Add R5425 and DY	Some panel backlight float	EE
		18	39	Update U3901 symbol	EMC4022 change pinout	EE
		19	54	Change FUSE5401 P/N	Change fuse to Poly fuse type	EE
	08/25	20	27	Change C2713 from 0.1uF to 1uF	Follow calpella design guide update	EE
		21	20	Change R2019 tolerance from +/-0.5% to +/-5%	Follow calpella design guide update	EE
		22	32	Change R3206 to 47K	Fine tune GBRST# timing	EE
		23	54	DY R5423 and R5424	eDP no need them	EE
	08/26	24	4,35,37	Modify SMBus Diagram for LAN change KBC I2C1E group link to PCH1 and U3701 pull high +3.3V_ALW_PCH. change LAN SMBus from U3503 link to U3701.	Modify LAN SMBus for avoid leakage from +3.3V_LAN to +3.3V_ALW_PCH	EE
	08/27	25	74	Add port B,C DOCK_AUX_SW pull high circuit ; remove DDC pull high resistor ; DY DPx DOCK_AUX resistor	Pull high DDC will disable AUX function modify DDC pull high resistor after switch;DY DPx AUX resistor due to DOCK already had	EE
	09/21		42	Remove R4228.	+3.3V_ALW_PCH is now connect directly to +3.3V_ALW.	EE
			54	Add R5426, R5427.	Add 100 ohm resistors to LCD SMBus clk and data.	
	09/25		7,37,24,35,32,23	X701 use 82.30005.901; C715 and C701 change to 78.15034.1FL. X3701 use 82.30001.841; C3717 and C3718 change to 78.39034.1FL. X2401 change to 82.30001.861; C2403 change to 78.15034.1FL, C2405 change to 78.12034.1FL. X3501 change to 82.30020.791; C3533, C3532 change to 78.15034.1FL. X3201 use 82.30023.611; C3217, C3218 change to 78.15034.1FL. X2301 change to 82.30020.791; C2309 change to 78.12034.1FL.	Tuning crystal capacitors.	EE
			86	Change PR8602 from 14KQ to 15KQ.	Tuning voltage level.	EE
			32	Add RN3201, RN3202. R3221 change to C3219.	Modification for R5U242 implementation.	EE
			40	R4006 dummy.	Free fall sensor INT2 is puph-pull.	EE
			42	R4230 change to 0805.	Incase current passing the resistor is too great.	EE

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X01	09/25		58	XDP1, R5808 dummy.	Dummy all XDP related components.	EE
			70	JTAG1, LDBG1 dummy.	Dummy circuit for debug use.	EE
			71	Change CARD1 to 20.I0086.001.	Changing flash reader socket.	EE
	09/28		74,81	Add in DVI/DP switching circuit.	ATI version circuit.	EE
			75,79	U7402 A,B,C,D,E,F all dummy.		EE
	10/06		75	U7501, power changes to +3.3V_DELAY.	Power saving concern.	EE
			30	U3001 change to version UA.	Update to newer version of CODEC.	EE
			81	R8145 and R8146 populate. U8101 dummy.	Remove 2N7002 circuit.	EE
			74	Delete RN7402 and RN7403.	Related circuit already built into docking.	EE
			36	R3605 delete, R3606 dummy, R3607 dummy, change C3602 into 1uF, change R3613 into 1Kohm.	TCM circuit modification.	EE
			71	Add R7115, R7116, R7117, R7118, R7119.		EE
			42,45,47,51,54,55,63	U4201, U4203, U4207 change symbol. PU5101, PU5102 change symbol. PU4505, PU4506 change symbol. PTC4701, PTC4705, PTC4706, PTC4708 change symbol. LCD1 change symbol. G6301, G6302, G6303, G6304 change symbol. CRT1 change symbol.	Update to new OrCAD symbols.	EE
	10/07		32	R3218, R3217, R3205, R3220, R3219 change to 33 ohm.		
			24,55	Add AFTP2401, AFTP2402, AFTP5501.	Add extra test points.	
			42,37	C4208 change to 150pF. C4211 change to 4700pF. R3707 change to 10k ohm.	Tuning S3 power sequence.	
			46	Add PR4656, 10k ohm. Add PR4657, 200k ohm, dummy.	Solve thermal shut down issue.	
	10/12		9	R941 connect to +3.3V_ALW_PCH instead of +3.3V_SUS.	Simplify layout.	
			74	Change DK1 to 20.F1572.144.	Introducing new connector.	
			79	Change H10 to ZZ.00PAD.E01.	Hole change.	
			74	RN7404 rotate. RN3201 swap nets. RN5402 swap nets.	Layout request.	
			79	Add EC7922 and EC7923, dummy.	RF team request.	
			66	WWAN LED circuit, dummy.	Combine WWAN LED with WLAN LED.	
			74	Delete some display port pull up and pull down resistors.		
	10/13		35	Add Lan chip SER-IRQ anti-leakage related circuit.	Prevent leakage of +3.3V_RUN.	
	10/14		12	R1203 change to 0 ohm. PR4776 change to 6.65k ohm.	Power team request.	
			79	Add EC7924, EC7925 EC7926, EC7927.	RF team request.	
	10/15		42	U4206 change to 84.00460.037.		
			79	Delete EC7926.		

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VERSION	DATE	NO	PAGE	Modified List	Issue Description	OWNER
X01	10/19		18,19, 13,12, 26,27, 82,84, 85	Modify C1813, C1815, C1816, C1915, C1918, C1921, C1310, C1311, C1314, C1315, C1207, C1208, C1218, C1219, C1234, C1316, C1317, C1319, C1320, C1321, C1322, C1324, C1325, C2612, C2613, C2614, C2615, C2616, C8202, C8204, C8207, C8208, C8209, C8210, C8212, C8213, C8214, C8216, C8217, C8218, C8219, C8222, C8223, C8224, C8225, C8231, C8401, C8409, C8410, C8411, C8420, C8421, C8422, C8509, C8510, C8511, C8520, C8521, C8522, C1201, C1210, C1211, C1223, C1224, C1225, C1226, C1227, C1228, C1229, C1230, C1231, C1232, C1233, C1236, C1237, C1238, C1239, C1240, C1241, C1242, C8264, C8265, C8274, C8276, C8277, C8278, C8279, C8280, C8288		EE
			86	PU8602 change to 84.08884.037. PU8603 change to 84.06690.E37. PU4705 change to 74.62883.B73. PU4602 change to 84.08880.037. PU4606 change to 84.06676.A37.	Power team suggestion.	EE
	10/20		25,37, 38	R2520, R2523 combined to form RN2506. R2503, R2504 combined to form RN2507. R3723, R3701 combined to form RN3717. R3729, R3739 combined to form RN3718. R3725, R3727 combined to form RN3719. R3802, R3806, RN3803 combined to form RN3805. R3809, R3810, R3813, R3814 combined to form RN3806. R3826, R3832, R3824, R3825 combined to form RN3807. R3821, R3833 combined to form RN3808.	Combine resistors into RN. To save part counts.	EE
			47,12	PC4729 change to 78.22422.2BL. Add R1207, R1208.	Power team suggestion.	EE
			79	Replace H5 by BOSS1, using 34.4Y702.001. Replace CPU1 by 62.10053.561 in part manager.	ME suggestion.	EE
			35	Add U3506, 72.25P80.D01 as alternative source of EEPROM.		EE
			66,64	Delete Q6601, R6616, EC6607, R6615, R6422. Add D6603, R6625. Dummy R6625, R6613.	Combine WWAN, WLAN and WI-MAX LED into one.	EE
			68	Add R6804, R6805, R6806, R6807. Dummy R6806, R6807.	Touch pad circuit modification.	EE
			11	R1105 change to 63.33234.1DL.		EE
	10/21		71	EC7105, EC7106, EC7107, EC7108 dummy.		EE
			35	R3526, R3528, R3529 combined into RN3508. R3532, R3533 combined into RN3507.		EE
	10/22		39	C3901 change to 78.47134.1FL.C3902 undummy.	Thermal shut down tuning.	EE
			18	TC1801 change to 79.33719.L01.	Sourcer suggestion.	EE
			30	C3010 change to 78.10610.5BL.	Factory request, create spacing.	EE
			73	R7307 and R7309 delete.	USB1.1 does not need resistors in USB pair.	EE
			74	C7441 and C7442 change to 25V capacitors.		EE
			62	U6201 change to 2MB. U6202 change to 4MB.		EE
	10/23		23,8, 21,34, 36,54, 83,80	R2302, R2308 combined into RN2313. R833, R832 combined into RN801. R2107 and R2109 combined into RN2106. R2102, R2104 combined into RN2105. R3401, R3410 combined into RN3401. R3402, R3406, R3407, R3408 combined into RN3402. R3603, R3611 combined into RN3601. R5426, R5427 combined into RN5404. R8336, R8337 combined into RN8301. R8002, R8003 combined into RN8001.		EE
			30	Delete R3011, R3012, C3018, C3019, C3015, C3016, C3029, C3014, C3031, C3030, R3014, R3025, R3026, R3027, C3034, C3035, C3032, C3033. Add R3029, R3030, C3042, C3040, C3039, C3036, C3041, C3038, C3043, C3037.		EE

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X01	10/23		74, 25, 38	RN7404, RN2506, RN3807 swap nets.	Swap nets for better layout.	EE
	10/26		54, 35, 42, 64, 65	Change Q5401, U3504, U4202, U6401, U6501 into 84.03456.E3D.	Original part, 84.03456.C3D obsoleted.	EE
			68, 34, 80, 8, 21	RN6801, RN3402, RN8001, RN801, RN2105, RN2106 swap nets.	Layout purpose modification.	EE
			79, 46	Pop EC7911, EC7918, EC7907, EC7908. PC4628 change to 0.1u.	EMI request.	EE
			35	SERIRQ leakage solving circuit, connect to IRQ_SERIRQ instead of IRQ_SERIRQ_R.	Limit output current of IRQ_SERIRQ by tuning resitstor.	EE
			66	WWAN LED circuit change.		EE
			71	R7114 change to 0 ohm resistor.		EE
			74	C7441 and C7442 change to X7R.		EE
			30	R3010 remove.	AUD_NB_MUTE is push-pull.	EE
	10/27		81, 82, 42	L8101, L8102, L8103, L8104, L8105, L8106, L8107, L8108, L8109, L8201, L8202, L8203, L8204, L8205, L8206, L8207, L8208, L8209, L8210, L8211, L8212, L8213, L8214, L8215, L8218 change to 68.00084.F81. Q4298 change to 84.02301.G31.	Original material obsoleted.	EE
			7, 9, 23, 25, 32	RN701, RN703, RN704, RN705, RN903, RN2301, RN2302, RN2306, RN2307, RN2308, RN2310, RN2311, RN2505, RN3202 change to 66.R0036.04L. RN3201 change to 66.R0036.08L.		EE
			68	Add L6801, L6802, D6801.	Add ESD protection circuit.	EE
			72	Change NEW1 to 62.10081.321. Change NEW1SKT1 to 21.I0036.001.	Change connectors.	EE
			47	PC4709, PC4710, PC4723 change to 78.22422.2BL.	Original part out of stock.	EE
			39, 50, 86	Add C3919, PC8617. Change R3923 to 64.12725.6DL. Change R3928 to 64.56215.6DL. Change PR5014 to 64.30125.6DL. Change PR5015 to 64.29425.6DL.	Power team change.	Power
			37, 71	Change C3711, C5405 to 78.10610.51L. Change C7102 to 78.10610.5BL.	Capacitor with higher precision.	EE
			59	HDD connector change to 62.10065.261. ODD connector change to 62.10065.791.		EE
	10/28		30	R3020, Q3002, Q3003, Q3004, Q3005, Q3001 dummy.		EE
			54, 35, 42, 64, 65	Q5401, U3504, U4202, U6401, U6501 change to 84.03456.D3D.	Original material obsoleted.	EE
			23	RN2301, RN2308 change to 66.R003A.04L.	Layout spacing not big enough.	EE
			75	C7521 dummy.		EE
			73	Remove R7301, R7307. Change EL7301 into 68.00201.141.	RF team suggestion.	EE

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X01	10/28	30		Add R3010 back to schematics.	Still to verify if this pin is indeed push-pull.	EE
		42		R4232 change to 64.10025.6DL.	Change sequence timing.	EE
	10/29	46		PC4628, PC4634 change to 78.10424.2BL. PC4634 remain dummy.	RF, EMI suggestion.	EE
		22		R2205 change to 10k ohm resistor. R2407 change to 8.2k ohm resistor.		EE
		7,79,		EC702, EC703 change to 78.10034.1FL. EC7917 pop. PC4634 pop. EC7922, EC7923 pop.	RF team suggestion.	EE
		86		R8603 change to 130k.	+VCC_GFX_CORE 2 steps: 0.95V and 0.9V modification.	Power
		58,24		Change FAN1 to 20.F1000.004. Change RTC1 to 20.F1000.003.	Connectors change.	EE
		12		R1207, R1208 dummy.		EE
		30		R3010 dummy.		EE
		68		C6801, C6802 delete. L6801, L6802 pop. L6802 connect to CLK_TP_SIO_1. L6801 connect to DAT_TP_SIO_1. RN6801 now connects to CLK_TP_SIO and DAT_TP_SIO.		EE
		37		R3734 dummy.		EE
		50		PR5010 connects ground.		EE
		54		Source of LCD_SMBUS_PWR change to +3.3V_RUN. R5406 dummy.		EE
		73,32		EL7301, RN3201 swap nets.	Layout purpose.	EE
	10/30	59		Change ODD1 to 62.10065.B01.	Connector change.	EE
	11/02	63		D6301 pop.	ESD protection.	EE

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