Fonseca 14.1" DIS Schematics Document

rPGA988A Mobile Arrandale

Intel Ibex Peak-M

2010-03-22

REV : -1

DY : Nopop Component
B_TPM:Use Lom TPM
C_TPM:Use China TPM

<Core Design>

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Title: *Cover Page*

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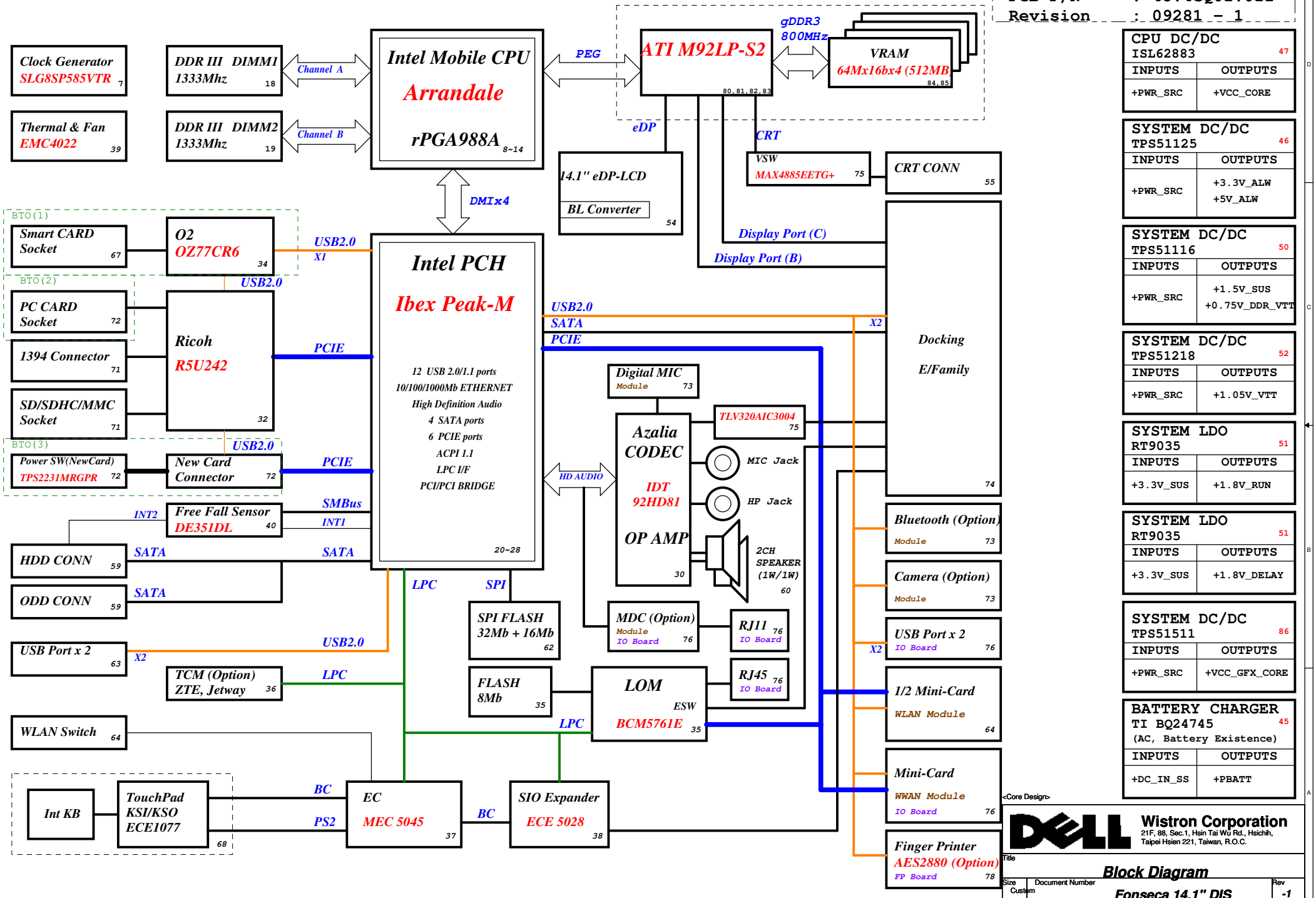
Fonseca 14" DIS Block Diagram

Project name: DF3-14D
Project code: 91.4GQ01.001
PCB P/N : 48.4GQ01.011
Revision : 09281 - 1



CPU DC/DC 47
ISL62883

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC 46
TPS51125

INPUTS	OUTPUTS
+PWR_SRC	+3.3V_ALW +5V_ALW

SYSTEM DC/DC 50
TPS51116

INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT

SYSTEM DC/DC 52
TPS51218

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM LDO 51
RT9035

INPUTS	OUTPUTS
+3.3V_SUS	+1.8V_RUN

SYSTEM LDO 51
RT9035

INPUTS	OUTPUTS
+3.3V_SUS	+1.8V_DELAY

SYSTEM DC/DC 86
TPS51511

INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

BATTERY CHARGER 45
TI BQ24745
(AC, Battery Existence)

INPUTS	OUTPUTS
+DC_IN_SS	+PBATT

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Title: Block Diagram
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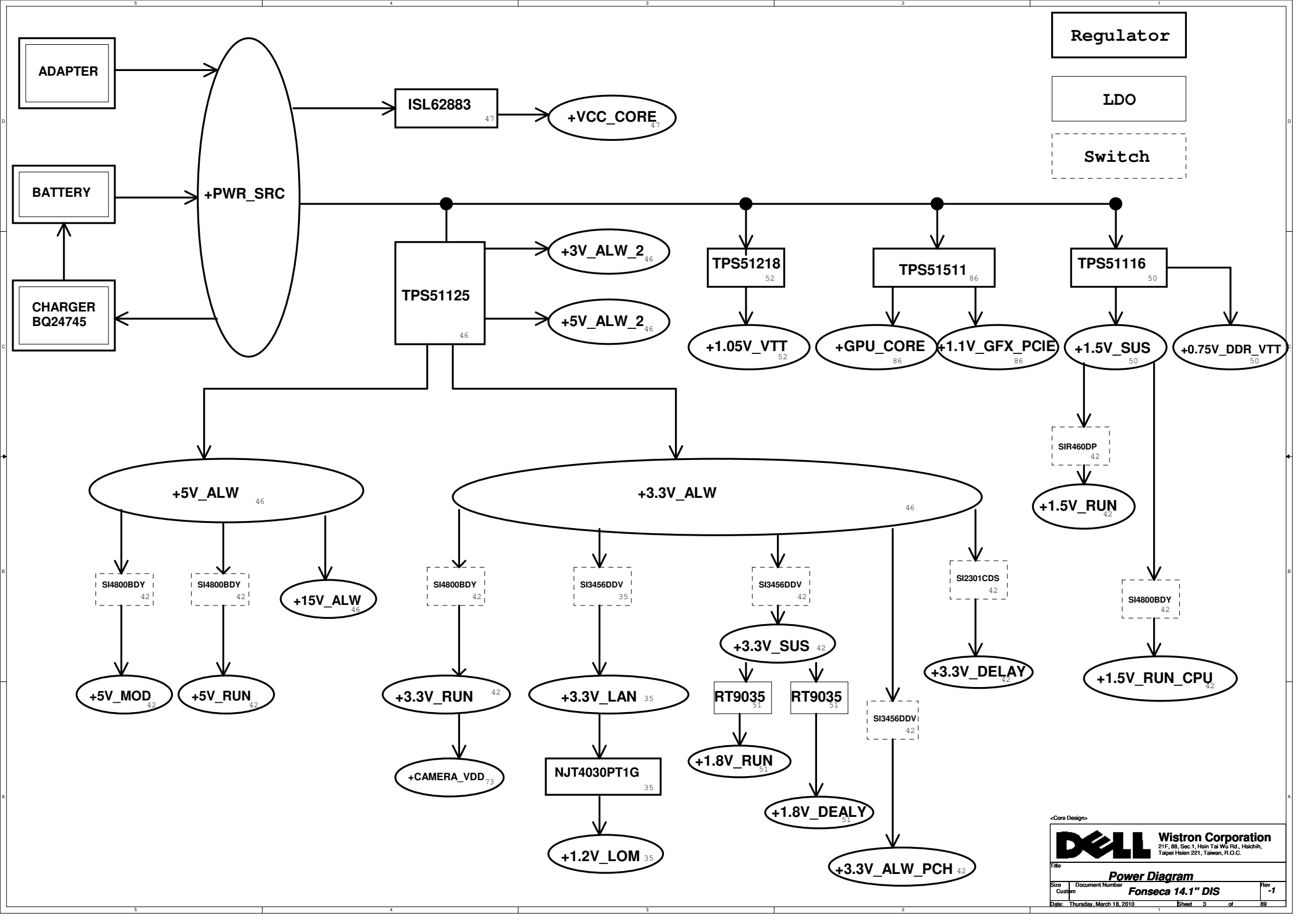

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Title: *Power Diagram*

Size: Custom | Document Number: *Fonseca 14.1" DIS* | Rev: -1

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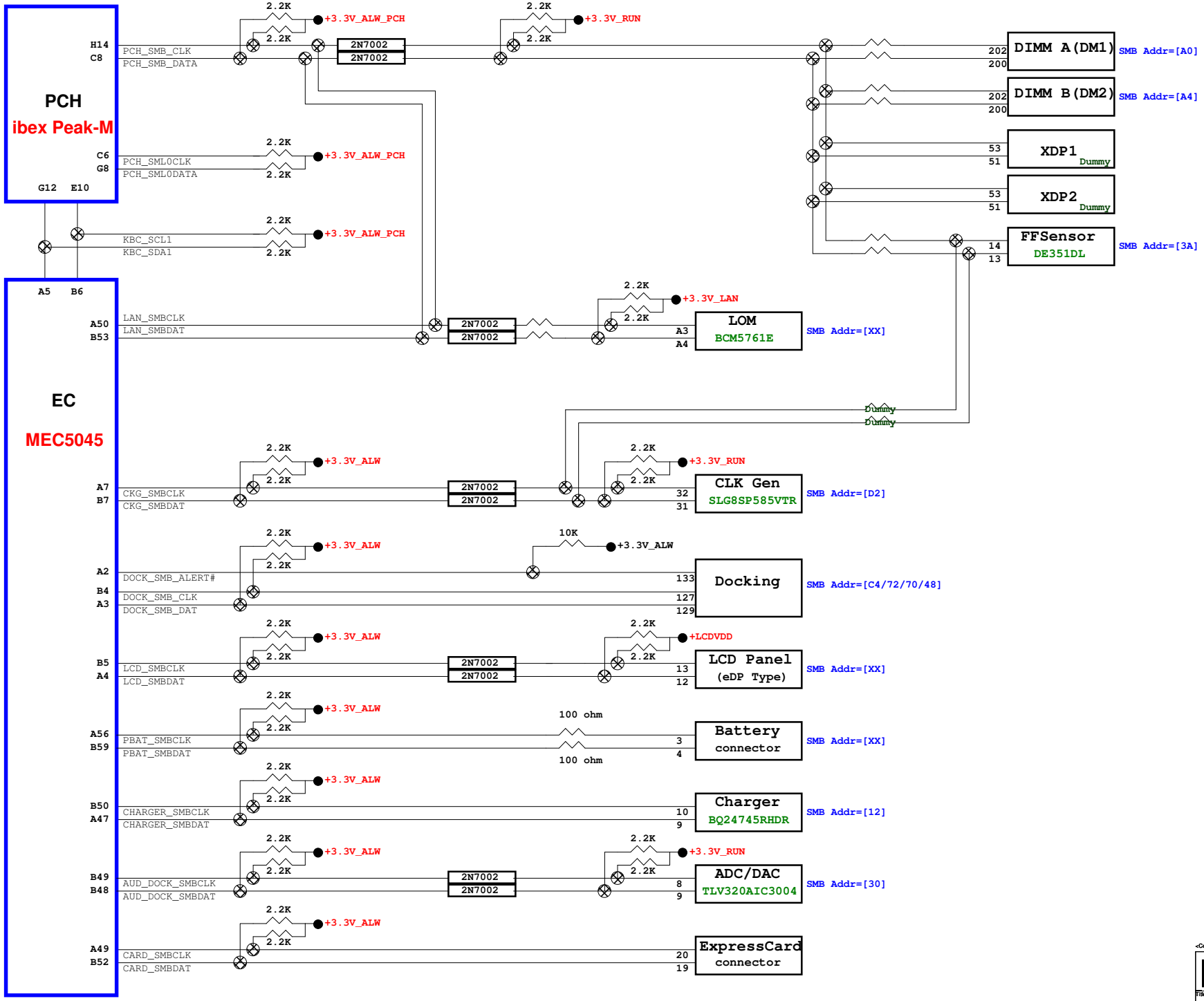

<Core Design>

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Title: SMBus Diagram

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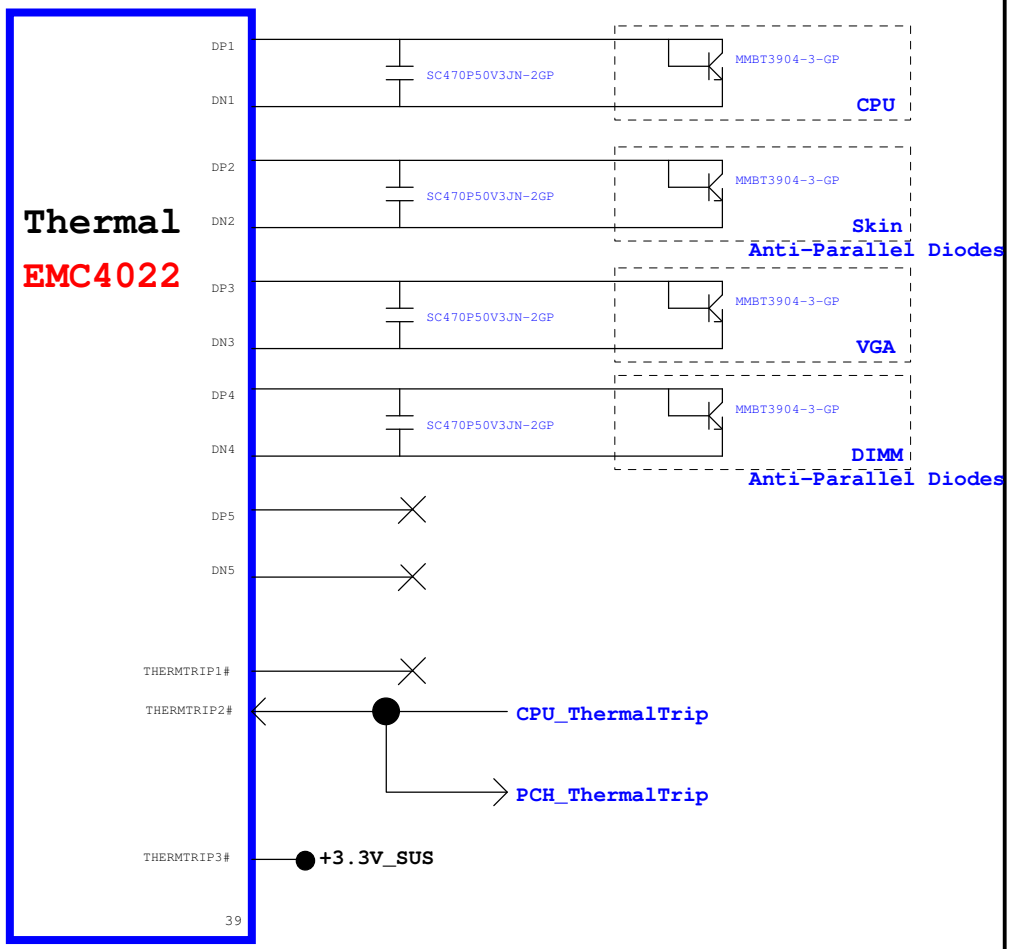
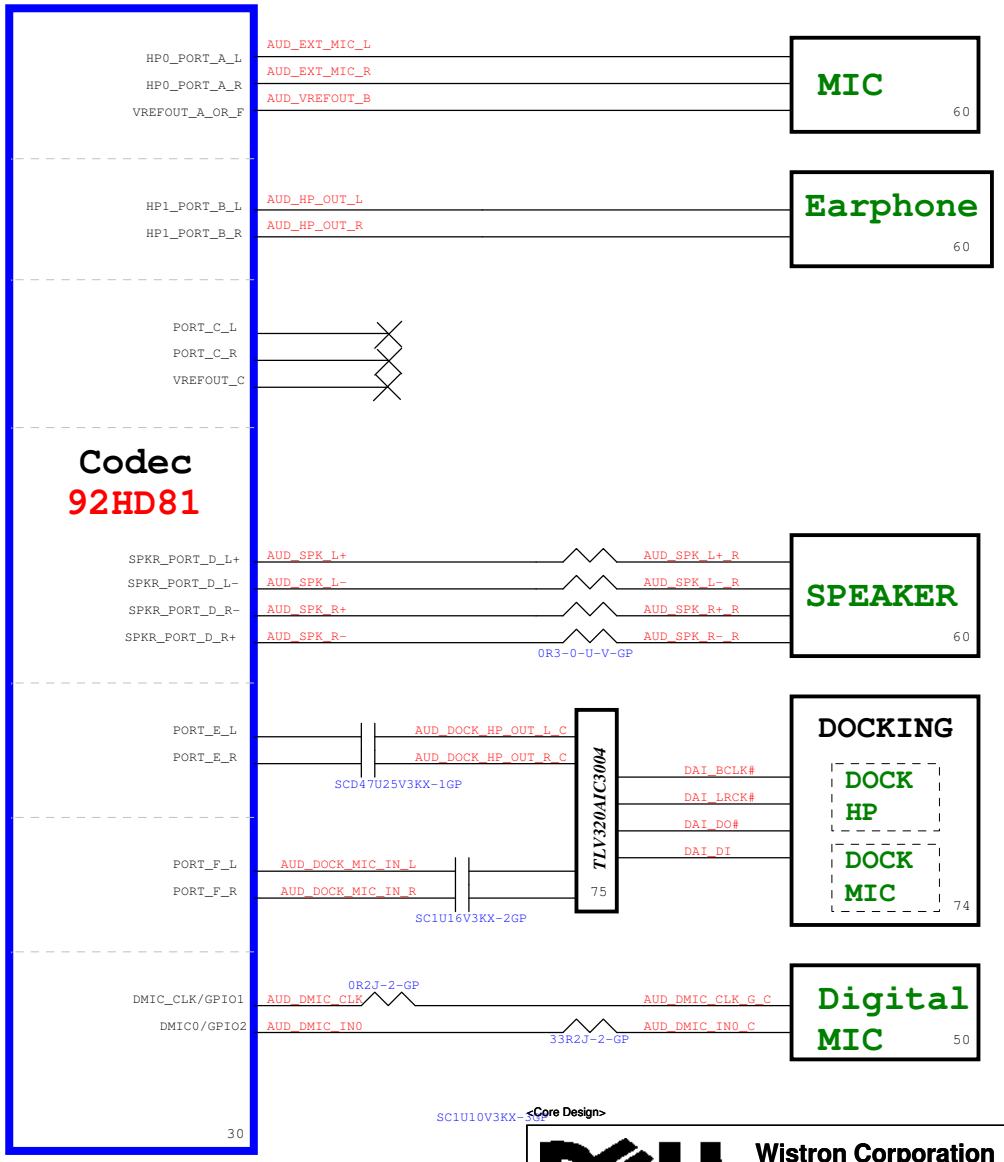
Thermal Block Diagram



Audio Block Diagram



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Title: AUDIO/THERMAL Diagram

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PCH Strapping

Calpella Schematic Checklist Rev: 1.6

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ ~ 10-kΩ weak pull-up resistor.
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** **Note:** Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ ; do not stuff resistor
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled** **Note:** CRB uses a 330-k resistor.
GNT0#, GNT1#	**Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default –** Internal pull-up. **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	**Enable Intel Anti-Theft Technology:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Intel Anti-Theft Technology:** Left floating, no pull-down required.
NV_ALE	**Enable Intel Anti-Theft Technology:** Connect to +NVRAM_VCCQ with 8.2-kΩ weak pull-up resistor [CRB has it pulled up with 1-kΩ no-stuff resistor] **Disable Intel Anti-Theft Technology:** Leave floating (internal pull-down).
NV_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HDA_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. **High (1):** Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. **Note:** CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) – Intel ME Crypto Transport Layer Security TLS) cipher suite with no confidentiality. High (1) – Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note: This is an unmuxed signal. This signal has a weak internal pull-down of 20KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1K pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	**Default =** Do not connect (floating). Internal pull-up. High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev: 1.6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**

PCIE Routing

LANE1	WWAN
LANE2	WLAN
LANE3	PCMCIA
LANE4	Express Card
LANE5	None
LANE6	10M/100M/1G LAN
LANE7	**Not available for HM55**
LANE8	**Not available for HM55**

USB Routing

USB	
Pair	**Device**
0	**USB0 @ MB**
1	**USB1 @ MB**
2	**USB2 @ IO Board**
3	**USB3 @ IO Board**
4	**WLAN**
5	**Bluetooth**
6	**Not available for HM55**
7	**Not available for HM55**
8	**DOCKING PORT1**
9	**DOCKING PORT2**
10	**Finger Printer**
11	**Camera**
12	**PCCard/ SmartCard/ ExpCard**
13	**WWAN**

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Title: ***Table of Content***

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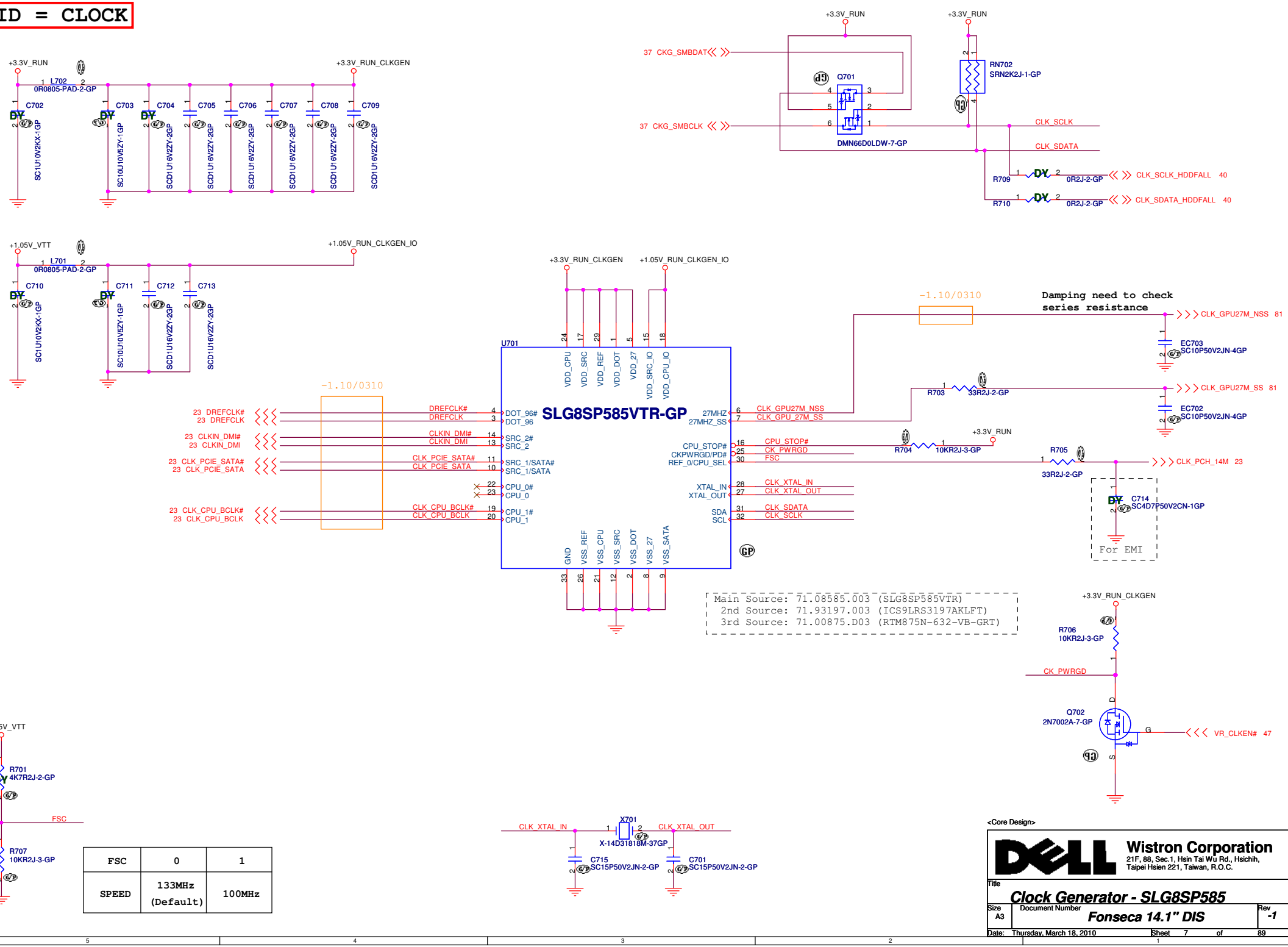
SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz

<Core Design>

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Title: Clock Generator - SLG8SP585

Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

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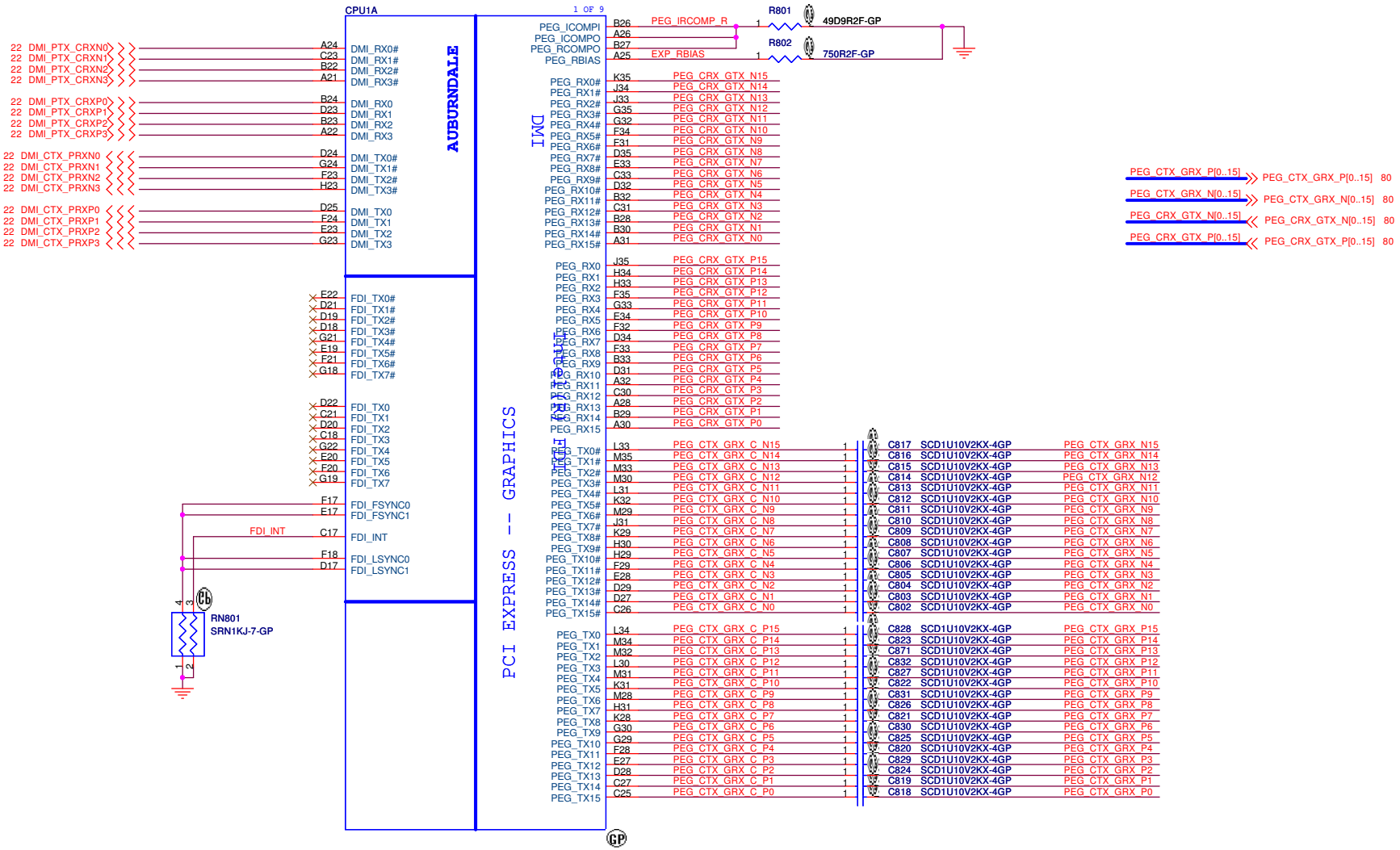
SSID = CPU



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Title: CPU - PCIE/DMI/FDI (1/7)

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SSID = CPU

Processor Pullups

+1.05V_VTT

R903 1 DY 49D9R2F-GP H_CATERR#
R906 1 DY 49D9R2F-GP H_PROCHOT#
R908 1 DY 68R2-GP H_CPURST#

+3.3V_RUN +1.05V_VTT

R912 8K2R2J-3-GP
R913 2K2R2J-2-GP DY
Q901 MMBT3904-F-GP DY
38 CPU_CATERR# H_CATERR#
C901 SCD1U10V2KX-4GP DY
Place near U3801

-1.10/0318

Processor Compensation Signals

CPU1B 2 OF 9

R902 1 20R2F-GP H_COMP3 AT23 COMP3
R904 1 20R2F-GP H_COMP2 AT24 COMP2
R905 1 49D9R2F-GP H_COMP1 G16 COMP1
R907 1 49D9R2F-GP H_COMP0 AT26 COMP0

37 H_SKTOCC# H_SKTOCC# AH24 SKTOCC#
H_CATERR# AK14 CATERR#
25 H_PECI AT15 PECI
47 H_PROCHOT# H_PROCHOT# AN26 PROCHOT#
25,39 H_THERMTRIP# H_THERMTRIP# AK15 THERMTRIP#
58 H_CPURST# H_CPURST# AP26 RESET_OBS#
H_PM_SYNC AL15 PM_SYNC
25,58 H_PWRGD R917 0R0402-PAD-2-GP VCCPWRGOOD AN14 VCCPWRGOOD_1
R919 0R0402-PAD-2-GP VCCPWRGOOD_0 AN27 VCCPWRGOOD_0
22 DRAM_PWROK DRAM_PWROK AK13 SM_DRAMPWROK
52 H_VTTPWRGD H_VTTPWRGD AM15 VTTPWRGOOD
58 H_PWRGD_XDP H_PWRGD_XDP AM26 TAPPWRGOOD
21,58,80 PLTRST1# R921 1K5R2F-2-GP PLT_RST#_R AL14 RSTIN#
R924 750R2F-GP

CLOCKS
DDR3 MISC
THERMAL, PWR MANAGEMENT, JTAG & BPM

BCLK A16 BCLK_CPU_P_R → BCLK_CPU_P_R 25
BCLK# B16 BCLK_CPU_N_R → BCLK_CPU_N_R 25
BCLK_ITP AR30 BCLK_ITP_P_R → RN903 SRN0J-6-GP → BCLK_ITP_P 58
BCLK_ITP# AT30 BCLK_ITP_N_R → BCLK_ITP_N 58
PEG_CLK E16 PEG_CLK_R → PEG_CLK_R 23
PEG_CLK# D16 PEG_CLK#_R → PEG_CLK#_R 23
DPLL_REF_SSCLK A18
DPLL_REF_SSCLK# A17

SM_DRAMRST# F6 SM_DRAMRST# → DDR3_DRAMRST# 18,19
SM_RCOMP0 AL1 SM_RCOMP_0
SM_RCOMP1 AM1 SM_RCOMP_1
SM_RCOMP2 AN1 SM_RCOMP_2
PM_EXT_TS0# AN15
PM_EXT_TS1# AP15 PM_EXTTS#_R
R914 2 1 10KR2J-3-GP +1.05V_VTT
R915 100KR2J-1-GP DY

DDR_HVREF_RST_GATE 37
C903 SCD047U10V2KX-2GP
+1.5V_SUS
Q902 2N7002A-7-GP
R934 1KR2J-1-GP
R936 0R2J-2-GP DY
C902 SC470P50V2JN-GP

PRDY# AT28 XDP_PRDY# → XDP_PRDY# 58
PREQ# AP27 XDP_PREQ# → XDP_PREQ# 58
TCK AN28 XDP_TCLK → XDP_TCLK 58
TMS AP28 XDP_TMS → XDP_TMS 58
TRST# AT27 XDP_TRST# → XDP_TRST# 58
TDI AT29 XDP_TDI_R
TDO AR27 XDP_TDO_R
TDI_M AP29 XDP_TDI_M
TDO_M AP29 XDP_TDO_M
DBR# AN25 H_DBR#_R R918 0R0402-PAD-2-GP → XDP_DBRESET# 22,38,58

BPM0# AJ22 XDP_OBS0 → XDP_OBS0 58
BPM1# AK22 XDP_OBS1 → XDP_OBS1 58
BPM2# AK24 XDP_OBS2 → XDP_OBS2 58
BPM3# AJ24 XDP_OBS3 → XDP_OBS3 58
BPM4# AJ25 XDP_OBS4 → XDP_OBS4 58
BPM5# AH22 XDP_OBS5 → XDP_OBS5 58
BPM6# AK23 XDP_OBS6 → XDP_OBS6 58
BPM7# AH23 XDP_OBS7 → XDP_OBS7 58

DDR3 Compensation Signals

SM_RCOMP_0 R909 100R2F-L1-GP-U
SM_RCOMP_1 R910 24D9R2F-L-GP
SM_RCOMP_2 R911 130R2F-1-GP

+1.05V_VTT
XDP_TMS R922 51R2J-2-GP DY
XDP_TDI_R R923 51R2J-2-GP DY
XDP_PREQ# R925 51R2J-2-GP DY
XDP_TCLK R926 51R2J-2-GP DY

22,35,38,50 SIO_SLP_S3# R927 0R0402-PAD-2-GP SIO_SLP_S3#_C
37,38,58 RUNPWROK R920 0R0402-PAD-2-GP RUNPWROK_C
U901 74LVC1G08GW-1-GP (B, A, GND, VCC, Y)
+3.3V_ALW_PCH
R941 0R2J-2-GP DY
DRAM_PWROK_R
R937 1K5R2F-2-GP
DRAM_PWROK
R939 750R2F-GP

JTAG MAPPING

XDP_TDI_R R929 0R0402-PAD-2-GP XDP_TDI → XDP_TDI 58
XDP_TDO_M R930 0R2J-2-GP DY
R901 0R0402-PAD-2-GP
XDP_TDO → XDP_TDO 58
XDP_TDI_M R931 0R2J-2-GP DY
XDP_TDO_R R932 0R0402-PAD-2-GP
XDP_TRST# R933 51R2J-2-GP

Scan Chain (Default)	Stuff --> R901, R929, R932 No Stuff --> R930, R931
CPU Only	Stuff --> R929, R930 No Stuff --> R901, R931, R932
GMCH Only	Stuff --> R931, R932 No Stuff --> R929, R930, R901

<Core Design>

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Title: CPU Thermal/Clock/PM (2/7)
Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1
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SSID = CPU

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AUBURNDALE

DDR SYSTEM MEMORY A

18 M_A_DQ[63..0]

M_A_DQ0 A10 SA_DQ0
M_A_DQ1 C10 SA_DQ1
M_A_DQ2 C7 SA_DQ2
M_A_DQ3 A7 SA_DQ3
M_A_DQ4 B10 SA_DQ4
M_A_DQ5 D10 SA_DQ5
M_A_DQ6 E10 SA_DQ6
M_A_DQ7 A8 SA_DQ7
M_A_DQ8 D8 SA_DQ8
M_A_DQ9 F10 SA_DQ9
M_A_DQ10 E6 SA_DQ10
M_A_DQ11 F7 SA_DQ11
M_A_DQ12 E9 SA_DQ12
M_A_DQ13 B7 SA_DQ13
M_A_DQ14 E7 SA_DQ14
M_A_DQ15 C6 SA_DQ15
M_A_DQ16 H10 SA_DQ16
M_A_DQ17 G8 SA_DQ17
M_A_DQ18 K7 SA_DQ18
M_A_DQ19 J8 SA_DQ19
M_A_DQ20 G7 SA_DQ20
M_A_DQ21 G10 SA_DQ21
M_A_DQ22 J7 SA_DQ22
M_A_DQ23 J10 SA_DQ23
M_A_DQ24 L7 SA_DQ24
M_A_DQ25 M6 SA_DQ25
M_A_DQ26 M8 SA_DQ26
M_A_DQ27 L9 SA_DQ27
M_A_DQ28 L6 SA_DQ28
M_A_DQ29 K8 SA_DQ29
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M_A_DQ41 AJ9 SA_DQ41
M_A_DQ42 AL10 SA_DQ42
M_A_DQ43 AK12 SA_DQ43
M_A_DQ44 AK8 SA_DQ44
M_A_DQ45 AL7 SA_DQ45
M_A_DQ46 AK11 SA_DQ46
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M_A_DQ59 AT14 SA_DQ59
M_A_DQ60 AT12 SA_DQ60
M_A_DQ61 AL13 SA_DQ61
M_A_DQ62 AR14 SA_DQ62
M_A_DQ63 AP14 SA_DQ63

18 M_A_BS0 AC3 SA_BS0
18 M_A_BS1 AB2 SA_BS1
18 M_A_BS2 U7 SA_BS2

18 M_A_CAS# AE1 SA_CAS#
18 M_A_RAS# AB3 SA_RAS#
18 M_A_WE# AE9 SA_WE#

SA_CK0 AA6 M_CLK_DDR0 18
SA_CK0# AA7 M_CLK_DDR#0 18
SA_CKE0 P7 M_CKE0 18

SA_CK1 Y6 M_CLK_DDR1 18
SA_CK1# Y5 M_CLK_DDR#1 18
SA_CKE1 P6 M_CKE1 18

SA_CS0# AE2 M_CS#0 18
SA_CS1# AE8 M_CS#1 18

SA_ODT0 AD8 M_ODT0 18
SA_ODT1 AF9 M_ODT1 18

SA_DM0 B9 M_A_DM0
SA_DM1 D7 M_A_DM1
SA_DM2 H7 M_A_DM2
SA_DM3 M7 M_A_DM3
SA_DM4 AG6 M_A_DM4
SA_DM5 AM7 M_A_DM5
SA_DM6 AN10 M_A_DM6
SA_DM7 AN13 M_A_DM7

M_A_DM[7..0] 18
M_A_DQS#[7..0] 18
M_A_DQS[7..0] 18
M_A_A[15..0] 18

SA_DQS0# C9 M_A_DQS#0
SA_DQS1# F8 M_A_DQS#1
SA_DQS2# J9 M_A_DQS#2
SA_DQS3# N9 M_A_DQS#3
SA_DQS4# AH7 M_A_DQS#4
SA_DQS5# AK9 M_A_DQS#5
SA_DQS6# AP11 M_A_DQS#6
SA_DQS7# AT13 M_A_DQS#7

SA_DQS0 C8 M_A_DQS0
SA_DQS1 F9 M_A_DQS1
SA_DQS2 H9 M_A_DQS2
SA_DQS3 M9 M_A_DQS3
SA_DQS4 AH8 M_A_DQS4
SA_DQS5 AK10 M_A_DQS5
SA_DQS6 AN11 M_A_DQS6
SA_DQS7 AR13 M_A_DQS7

SA_MA0 Y3 M_A_A0
SA_MA1 W1 M_A_A1
SA_MA2 AA8 M_A_A2
SA_MA3 AA3 M_A_A3
SA_MA4 V1 M_A_A4
SA_MA5 AA9 M_A_A5
SA_MA6 V8 M_A_A6
SA_MA7 T1 M_A_A7
SA_MA8 Y9 M_A_A8
SA_MA9 U6 M_A_A9
SA_MA10 AD4 M_A_A10
SA_MA11 T2 M_A_A11
SA_MA12 U3 M_A_A12
SA_MA13 AG8 M_A_A13
SA_MA14 T3 M_A_A14
SA_MA15 V9 M_A_A15

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AUBURNDALE

DDR SYSTEM MEMORY - B

19 M_B_DQ[63..0]

M_B_DQ0 B5 SB_DQ0
M_B_DQ1 A5 SB_DQ1
M_B_DQ2 C3 SB_DQ2
M_B_DQ3 B3 SB_DQ3
M_B_DQ4 E4 SB_DQ4
M_B_DQ5 A6 SB_DQ5
M_B_DQ6 A4 SB_DQ6
M_B_DQ7 C4 SB_DQ7
M_B_DQ8 D1 SB_DQ8
M_B_DQ9 D2 SB_DQ9
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M_B_DQ15 G4 SB_DQ15
M_B_DQ16 H6 SB_DQ16
M_B_DQ17 G2 SB_DQ17
M_B_DQ18 J6 SB_DQ18
M_B_DQ19 J3 SB_DQ19
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M_B_DQ39 AH4 SB_DQ39
M_B_DQ40 AK3 SB_DQ40
M_B_DQ41 AK4 SB_DQ41
M_B_DQ42 AM6 SB_DQ42
M_B_DQ43 AN2 SB_DQ43
M_B_DQ44 AK5 SB_DQ44
M_B_DQ45 AK2 SB_DQ45
M_B_DQ46 AM4 SB_DQ46
M_B_DQ47 AM3 SB_DQ47
M_B_DQ48 AP3 SB_DQ48
M_B_DQ49 AN5 SB_DQ49
M_B_DQ50 AT4 SB_DQ50
M_B_DQ51 AN6 SB_DQ51
M_B_DQ52 AN4 SB_DQ52
M_B_DQ53 AN3 SB_DQ53
M_B_DQ54 AT5 SB_DQ54
M_B_DQ55 AT6 SB_DQ55
M_B_DQ56 AN7 SB_DQ56
M_B_DQ57 AP6 SB_DQ57
M_B_DQ58 AP8 SB_DQ58
M_B_DQ59 AT9 SB_DQ59
M_B_DQ60 AT7 SB_DQ60
M_B_DQ61 AP9 SB_DQ61
M_B_DQ62 AR10 SB_DQ62
M_B_DQ63 AT10 SB_DQ63

19 M_B_BS0 AB1 SB_BS0
19 M_B_BS1 W5 SB_BS1
19 M_B_BS2 R7 SB_BS2

19 M_B_CAS# AC5 SB_CAS#
19 M_B_RAS# Y7 SB_RAS#
19 M_B_WE# AC6 SB_WE#

SB_CK0 W8 M_CLK_DDR2 19
SB_CK0# W9 M_CLK_DDR#2 19
SB_CKE0 M3 M_CKE2 19

SB_CK1 V7 M_CLK_DDR3 19
SB_CK1# V6 M_CLK_DDR#3 19
SB_CKE1 M2 M_CKE3 19

SB_CS0# AB8 M_CS#2 19
SB_CS1# AD6 M_CS#3 19

SB_ODT0 AC7 M_ODT2 19
SB_ODT1 AD1 M_ODT3 19

SB_DM0 D4 M_B_DM0
SB_DM1 E1 M_B_DM1
SB_DM2 H3 M_B_DM2
SB_DM3 K1 M_B_DM3
SB_DM4 AH1 M_B_DM4
SB_DM5 AL2 M_B_DM5
SB_DM6 AR4 M_B_DM6
SB_DM7 AT8 M_B_DM7

M_B_DM[7..0] 19
M_B_DQS#[7..0] 19
M_B_DQS[7..0] 19
M_B_A[15..0] 19

SB_DQS0# D5 M_B_DQS#0
SB_DQS1# F4 M_B_DQS#1
SB_DQS2# J4 M_B_DQS#2
SB_DQS3# L4 M_B_DQS#3
SB_DQS4# AH2 M_B_DQS#4
SB_DQS5# AL4 M_B_DQS#5
SB_DQS6# AR5 M_B_DQS#6
SB_DQS7# AR8 M_B_DQS#7

SB_DQS0 C5 M_B_DQS0
SB_DQS1 E3 M_B_DQS1
SB_DQS2 H4 M_B_DQS2
SB_DQS3 M5 M_B_DQS3
SB_DQS4 AG2 M_B_DQS4
SB_DQS5 AL5 M_B_DQS5
SB_DQS6 AP5 M_B_DQS6
SB_DQS7 AR7 M_B_DQS7

SB_MA0 U5 M_B_A0
SB_MA1 V2 M_B_A1
SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
SB_MA4 R1 M_B_A4
SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
SB_MA7 R6 M_B_A7
SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AF7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU - DDR (3/7)

Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

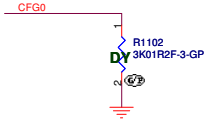
Date: Friday, March 19, 2010 | Sheet 10 of 89

SSID = CPU

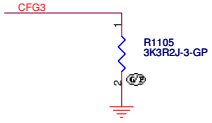
SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor

CPU Piin AJ13 and AJ12:
Core voltage sense line.
Via from PGA pad to the back of the MB and provide test point.
Do not route any additional trace.

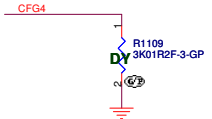
VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



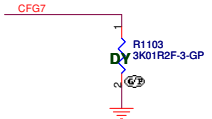
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled For Clarksfield



CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU - Reserve (4/7)

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Friday, March 19, 2010 | Sheet 11 of 89

SSID = CPU

PROCESSOR CORE POWER

48A

+VCC_CORE

CPU1F

6 OF 9

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that
The VTT Rail values are
Arrandale for VTT=1.05V
Clarksfield for VTT=1.1V

Arrandale drives this pin High for 1.05V
Clarksfield drives this pin Low for 1.1V

<Core Design>

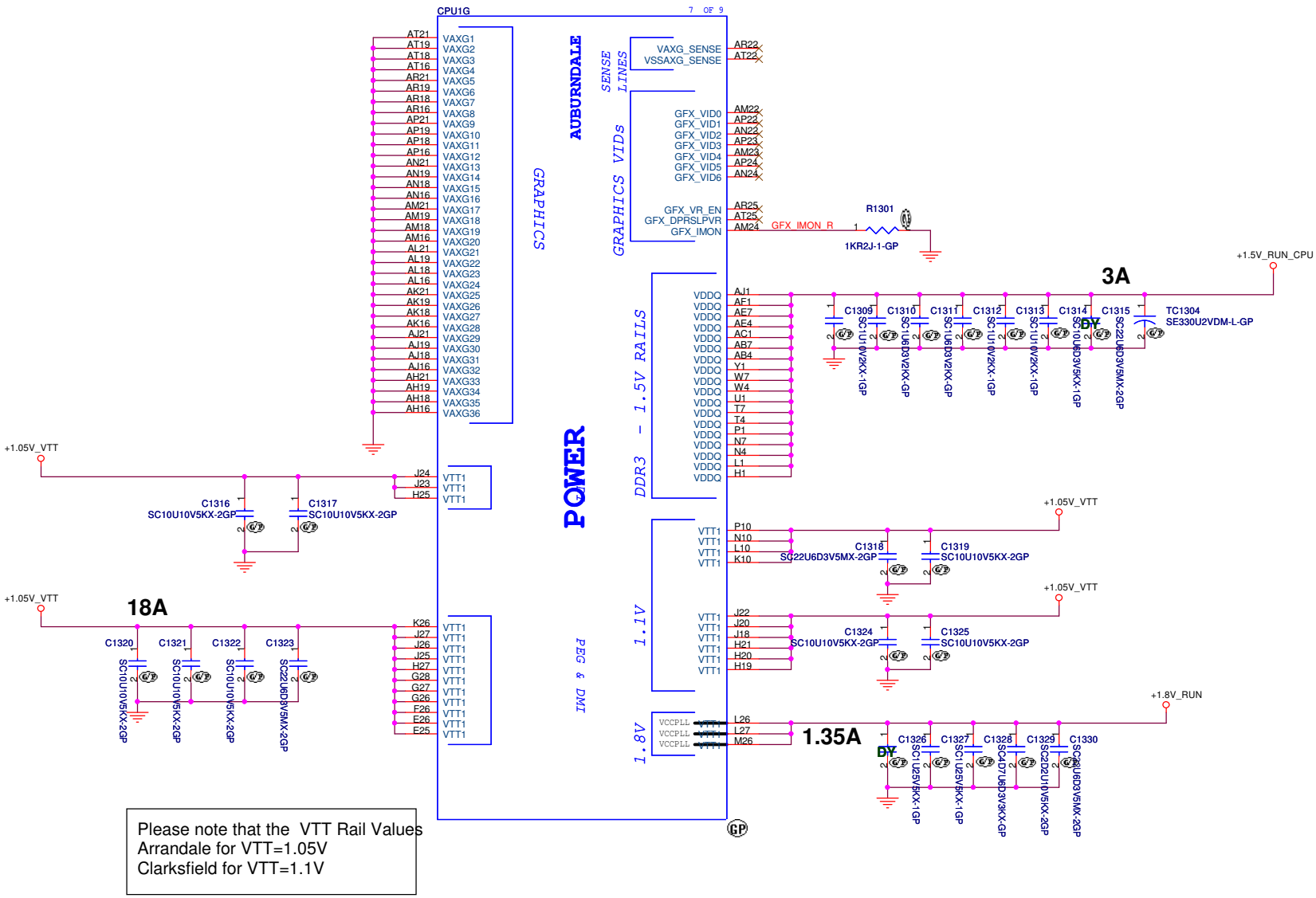
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU - VCC_CORE (5/7)

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Friday, March 19, 2010 | Sheet 12 of 89

SSID = CPU



<Core Design>

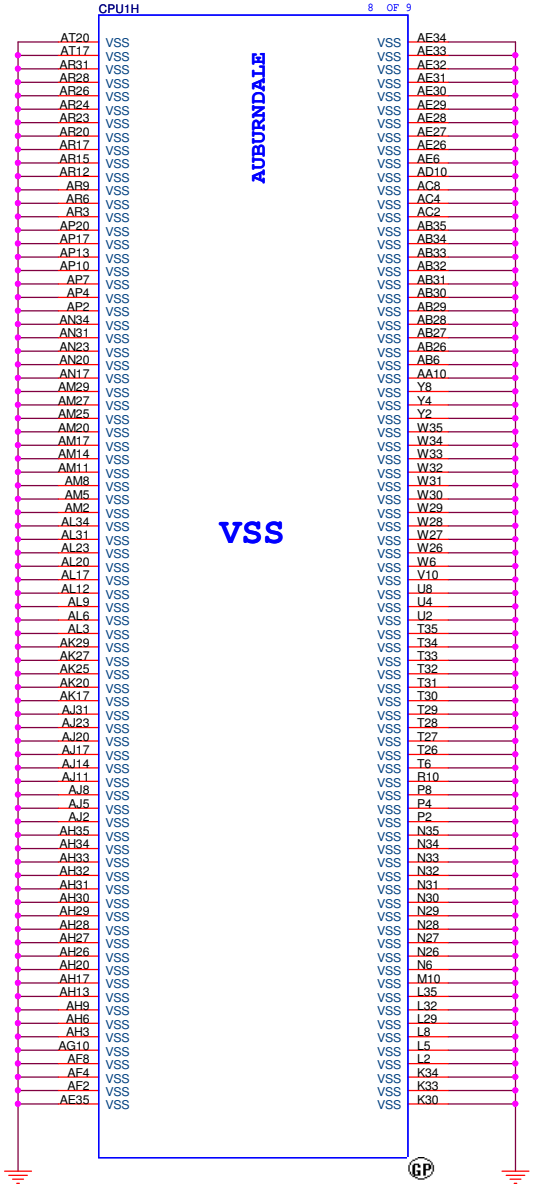
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

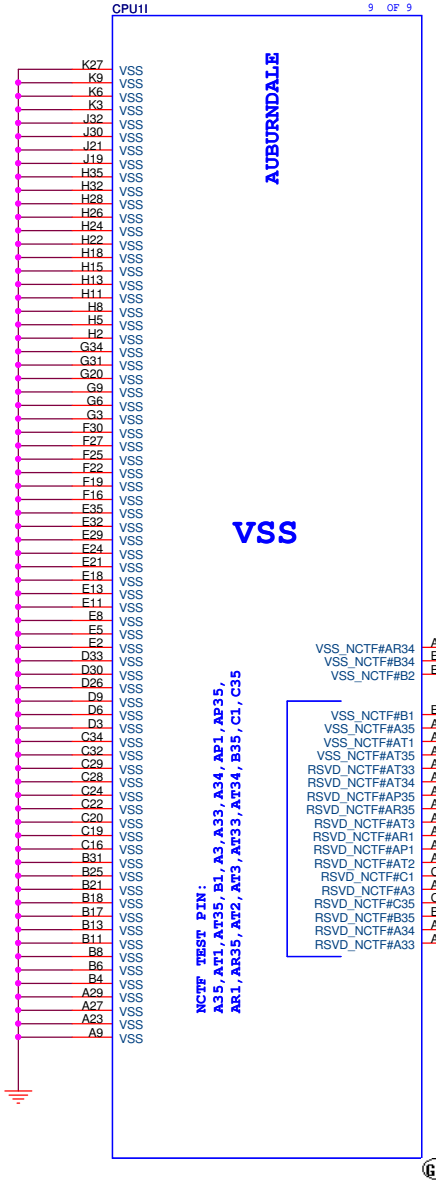
Title: CPU - GFXCORE (6/7)

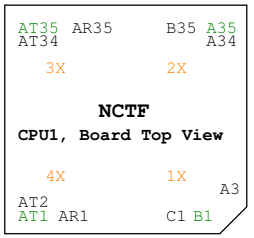
Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

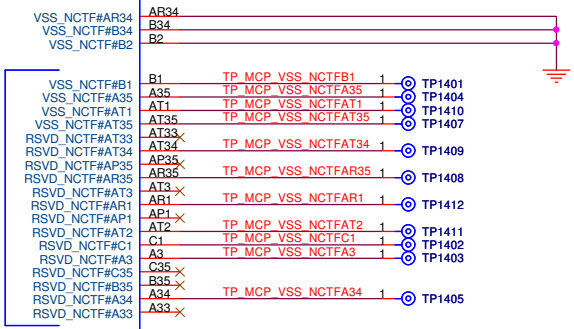
Date: Friday, March 19, 2010 | Sheet 13 of 89

SSID = CPU









All NCTF pins should be Test Points and should be routed as trace.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU - VSS (7/7)***

Size	Document Number	Rev
A3	***Fonseca 14.1" DIS***	-1

Date: Friday, March 19, 2010 Sheet 14 of 89

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserve

Size	Document Number	Rev
Custom	*Fonseca 14.1" DIS*	*-1*

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserve

Size	Document Number	Rev
Custom	***Fonseca 14.1" DIS***	*-1*

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserve

Size	Document Number	Rev
Custom	***Fonseca 14.1" DIS***	*-1*

SSID = Memory

SO-DIMMA
H = 9.2mm

DM1

DDR3-204P-42-GP

62.10017.N61

Main:62.10017.N61
2nd:62.10017.F91

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM A DECOUPLING

0904 SA

Layout Note:
Place these Caps near SO-DIMMA.

Place between DM1 and DM2.

Place these caps close to VTT1 and VTT2.

Near Memory +1.5V_SUS Plane

Near CPU +1.5V_RUN Plane

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR III Socket - DM1

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 18 of 89

SSID = Memory

SO-DIMMB
H = 5.2mm

DDR3-204P-48-GP
62.10017.P41

Main:62.10017.P41
2nd:62.10017.F81

SODIMM B DECOUPLING

Layout Note:
Place these Caps near SO-DIMMB.

Place these caps close to VTT1 and VTT2.

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR III Socket - DM2

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

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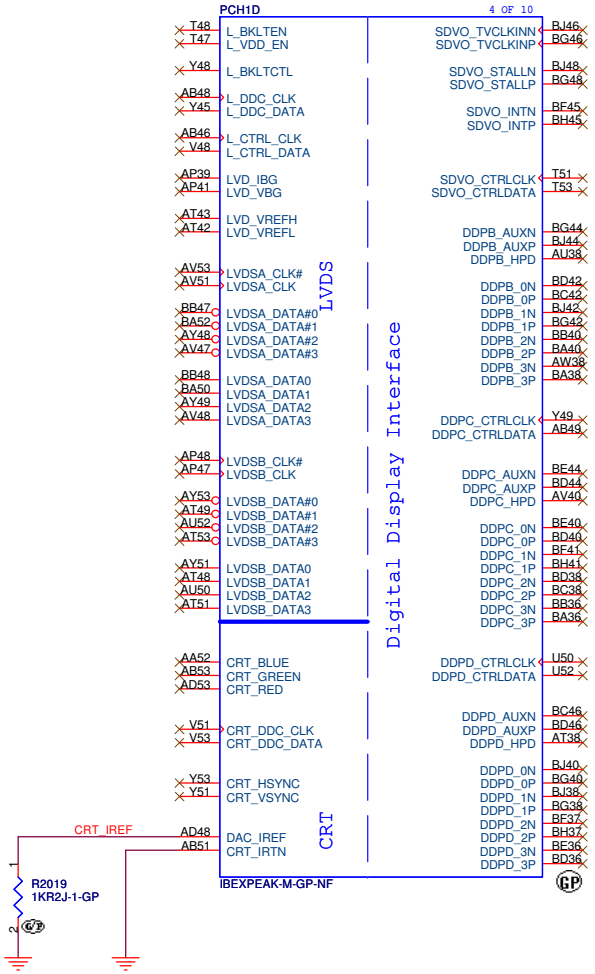
SSID = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - LVDS/CRT/DDI (1/9)

Size	Document Number	Rev
A3	Fonseca 14.1" DIS	-1

Date: Thursday, March 18, 2010 Sheet 20 of 89

SSID = PCH

DMI Termination Voltage

NV_CLE	Set to Vss when low. Set to Vcc when high.

DMI termination voltage
Weak internal pull-up
Do not pull low

Check list 1.6
If not implemented, the dual channel NAND interface signals, including NV_RCOMP, can be left as No Connect

Danbury Technology:
Disabled when Low.
Enable when High.

USB

Pair	Device
0	USB0 @ MB (Charger)
1	USB1 @ MB
2	USB2 @ IO Board
3	USB3 @ IO Board
4	WLAN
5	Bluetooth
6	Not available for HM55
7	Not available for HM55
8	DOCK1
9	DOCK2
10	Finger Printer
11	Camera
12	PCCard/SmartCard/ExpCard
13	WWAN

BOOT BIOS Strap

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI(Default)

PCI_GNT[3:0]#: Internal pull high during Strap

A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

<Core Design>

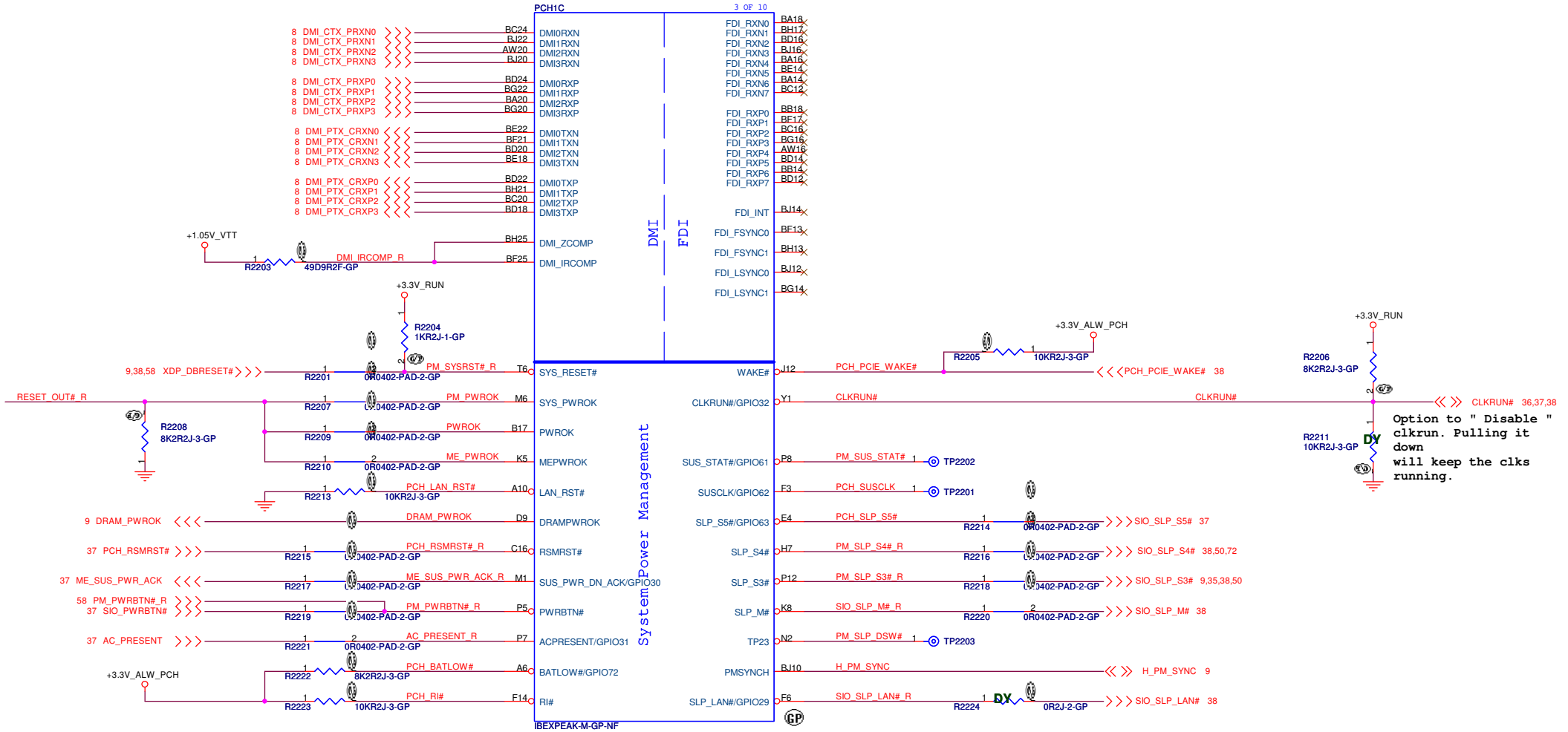
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - PCI/USB/NVRAM (2/9)

Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 21 of 89

SSID = PCH



<Core Design>

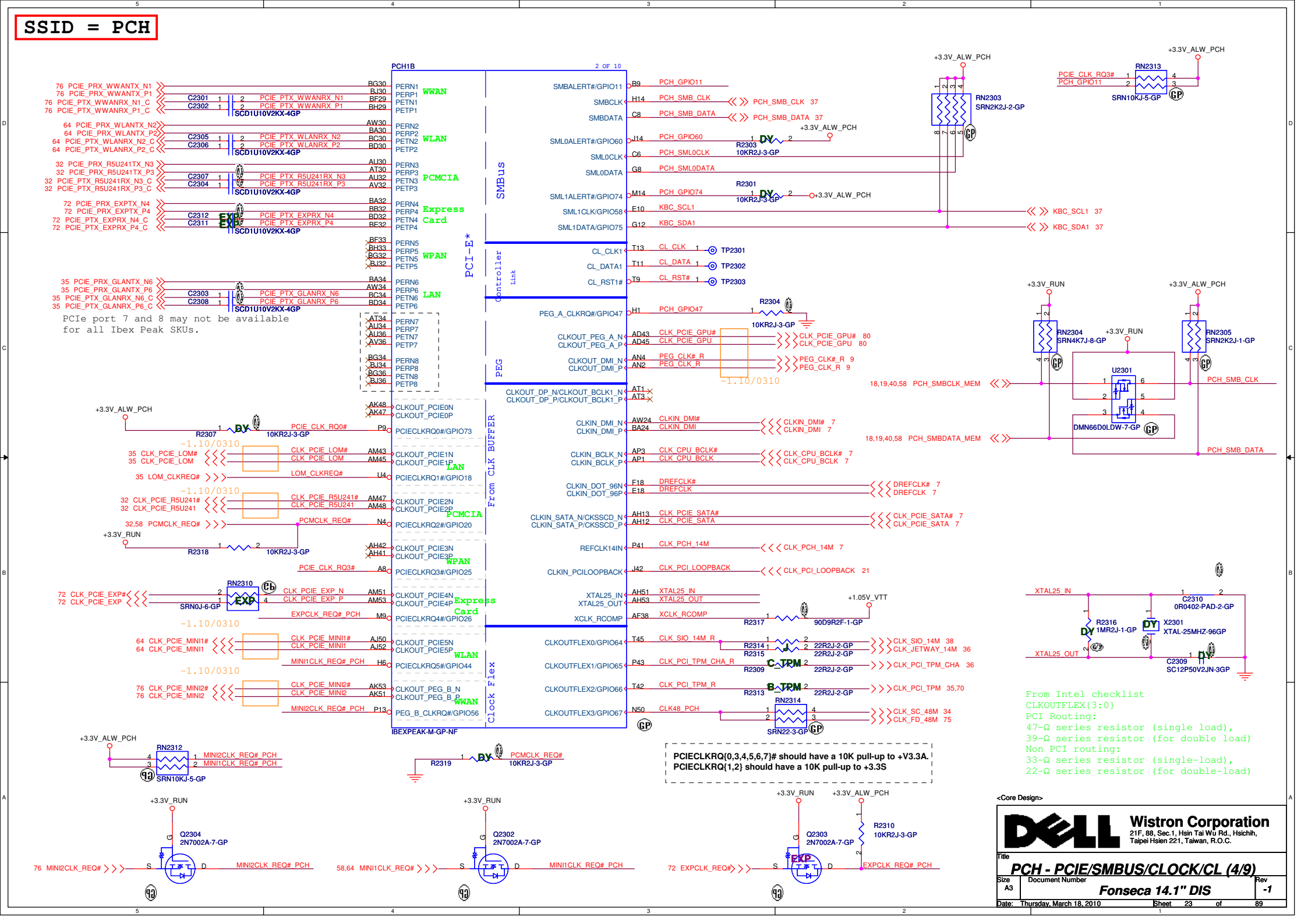
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - DMI/FDI/PM (3/9)

Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 22 of 89

SSID = PCH



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Core Design>
Title: PCH - PCIE/SMBUS/CLOCK/CL (4/9)
Size: A3
Document Number: Fonseca 14.1" DIS
Rev: -1
Date: Thursday, March 18, 2010
Sheet 23 of 89

SSID = PCH

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

PCH1A

1 OF 10

IBEXPEAK-M-GP-NF

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN

LPC: LPC_LAD[0..3], LPC_LFRAME#, LPC_LDRQ0#, LPC_LDRQ1#, SERIRQ

IHDA: HDA_BCLK, HDA_SYNC, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO

SATA: HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO13

JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#

SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

SRTCRST# new signal Pin

HDD

ODD

SATA port 2 and 3 may not be available for all Ibex Peak SKUs.

DOCKING eSATA

NO REBOOT STRAP
1210 SB

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

Place near PCH side

Form DG1.5
TRST# on PCH does not belong to JTAG interface.
For ES1 silicon, an ext. pull up 3.3-V Sus is required for bias internal state.
A 20-K/10-K voltage divider to this signal to 1.1 V.
However, from ES2 silicon onward, this signal is a No Connect regardless if JTAG interface on PCH is enabled or not.

09/0416, SPI_MISO
From Intel checklist,
No series resistor required if routing length is 1.5"-6.5" if using 1 SPI device.
Use a 33- series resistors close to them PCH if using 2 SPI devices.

-1.10/0308

Pull up +3.3V_M enable iAMT(DY disable)

integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

Main:20.F1000.003
2nd:20.D0210.103

20.F1000.003

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - SPI/RTC/LPC/SATA/IHDA (5/9)

Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 24 of 89

SSID = PCH

PCH1F

6 OF 10

BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
GPIO24
GPIO27
GPIO28
STP_PCI#/GPIO34
SATACLKREQ#/GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57

MISC
GPIO
CPU
NCTF
RSVD

CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
A20GATE
CLKOUT_BCLK0_N/CLKOUT_PCIE8N
CLKOUT_BCLK0_P/CLKOUT_PCIE8P
PECI
RCIN#
PROCPWRGD
THRMTRIP#
TP1 … TP24
NC_1 … NC_5
INIT3_3V#

VSS_NCTF_1 … VSS_NCTF_31

IBEXPEAK-M-GP-NF

58 SIO_EXT_SCI#_R
37 SIO_EXT_SCI#
R2502 0R0402-PAD-2-GP
37 SIO_EXT_SMI#
38 SIO_EXT_WAKE#
C2501 DY SC47P50V2JN-3GP
58 PCH_GPIO16
60 SPEAKER_DET#
64 USB_MCARD1_DET#
C2502 DY SC47P50V2JN-3GP
64 PCIE_MCARD1_DET#
77 LED_BD_DET#
58 LED_BD_DET#_R
R2506 0R0402-PAD-2-GP
24 RTC_BAT_DET#
R2532 0R0402-PAD-2-GP
58 RTC_BAT_DET#_R
58 PCH_GPIO37
76 USB_MCARD2_DET#
C2503 DY SC47P50V2JN-3GP
40 FFS_INT2_R
38,58 TEMP_ALERT#
78 BIO_DET#

+3.3V_RUN
RN2502 SRN10KJ-6-GP
PCH_GPIO22
PCH_GPIO1
PCH_GPIO6
PCH_GPIO7

+3.3V_RUN
RN2503 SRN10KJ-6-GP
SIO_EXT_SCI#_R
PCH_GPIO37
PCH_GPIO16

+3.3V_RUN
R2513 100KR2J-1-GP SPEAKER_DET#
R2514 100KR2J-1-GP USB_MCARD1_DET#
R2515 8K2R2J-3-GP STP_PCI#
R2522 10KR2J-3-GP RTC_BAT_DET#_R

+3.3V_ALW_PCH
RN2504 SRN10KJ-6-GP
SIO_EXT_SMI#
PCH_GPIO46
USB_MCARD2_DET#
PCH_GPIO12

+3.3V_ALW_PCH
R2516 1KR2J-1-GP SIO_EXT_WAKE#
RN2506 SRN100KJ-6-GP PCIE_MCARD1_DET#
BIO_DET#
R2521 100KR2J-1-GP LED_BD_DET#_R
R2528 DY 8K2R2J-3-GP TP_ONDIE_PLL_VR
Internal pull up GPIO27 to enable VccVRM

TP2510 TP_VSS_NCTF13
TP2512 TP_VSS_NCTF22
TP2511 TP_VSS_NCTF21
TP2508 TP_VSS_NCTF11
TP2513 TP_VSS_NCTF23
TP2519 TP_VSS_NCTF43
TP2515 TP_VSS_NCTF32
TP2517 TP_VSS_NCTF41
TP2518 TP_VSS_NCTF42
TP2516 TP_VSS_NCTF33
TP2514 TP_VSS_NCTF31
TP2509 TP_VSS_NCTF12

BJ53 BH53 BJ52 — 3X
B53 A53 A52 — 2X
NCTF
PCH1, Board Top View
4X
1X
BJ2 BJ1 BH1
B2 D1
A4

TPM_ID	TPM_ID0 (0)	TPM_ID0 (1)
TPM_ID1 (0)	C_TPM	RSVD
TPM_ID1 (1)	NONE	B_TPM

AH45 PCH_SRC6_XDP_N — TP2502
AH46 PCH_SRC6_XDP_P — TP2503
AF48 PCH_SRC7_DMI_LAI_N — TP2501
AF47 PCH_SRC7_DMI_LAI_P — TP2504
U2 A20GATE → SIO_A20GATE 37
-1.10/0310
AM3 BCLK_CPU_N_R → BCLK_CPU_N_R 9
AM1 BCLK_CPU_P_R → BCLK_CPU_P_R 9
BG10 PECI → H_PECI 9
T1 RCIN# → SIO_RCIN# 37
BE10 PROCPWRGD → H_PWRGD 9,58
BD10 THRMTRIP# — PCH_THERMTRIP_R
+1.05V_VTT
RN2508 SRN56J-4-GP
H_THERMTRIP# 9,39
Place close to PCH

+3.3V_RUN
RN2507 SRN10KJ-5-GP
SIO_A20GATE
SIO_RCIN#

P6 INIT3_3V# — TP2506
C10

+3.3V_RUN
R2526 100KR2J-1-GP B_TPM
TPM_ID0
CTPM and Disable B_TPM
R2531 100KR2J-1-GP

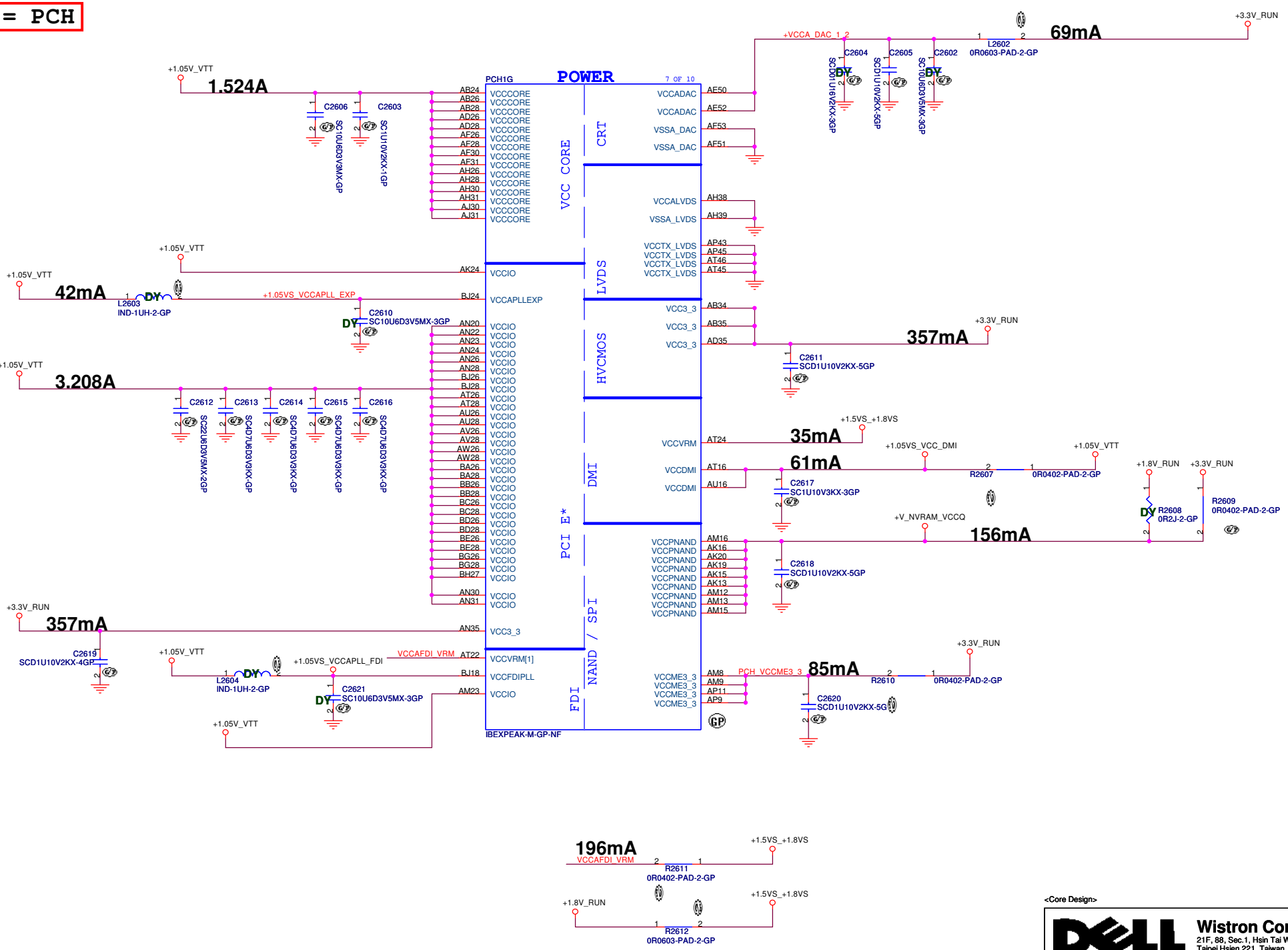
+3.3V_RUN
B_TPM and DisableBTPM
R2527 100KR2J-1-GP
TPM_ID1
C_TPM
R2529 100KR2J-1-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - GPIO/CPU/MISC (6/9)
Size: A3
Document Number: Fonseca 14.1" DIS
Rev: -1
Date: Thursday, March 18, 2010
Sheet 25 of 89

SSID = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (7/9)

Size	Document Number	Rev
A3	Fonseca 14.1" DIS	-1

Date: Thursday, March 18, 2010 Sheet 26 of 89

SSID = PCH

PCH1J

POWER

10 OF 10

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

CPU

RTC

HDA

IBEXPEAK-M-GP-NF

52mA

(344mA)

1.998A

72mA

73mA

163mA

1mA

2mA

<1mA

32mA

6mA

<Core Design>

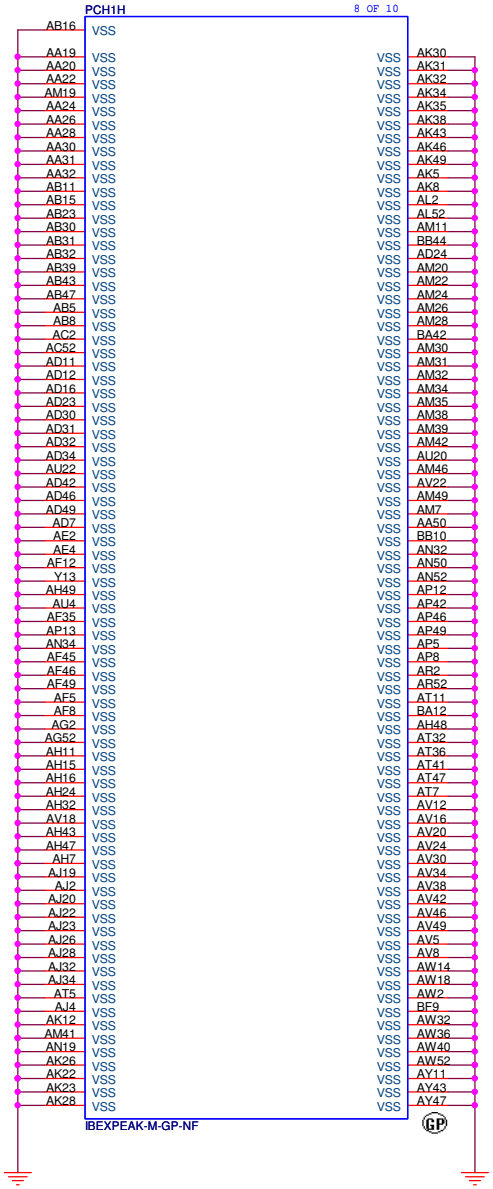
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

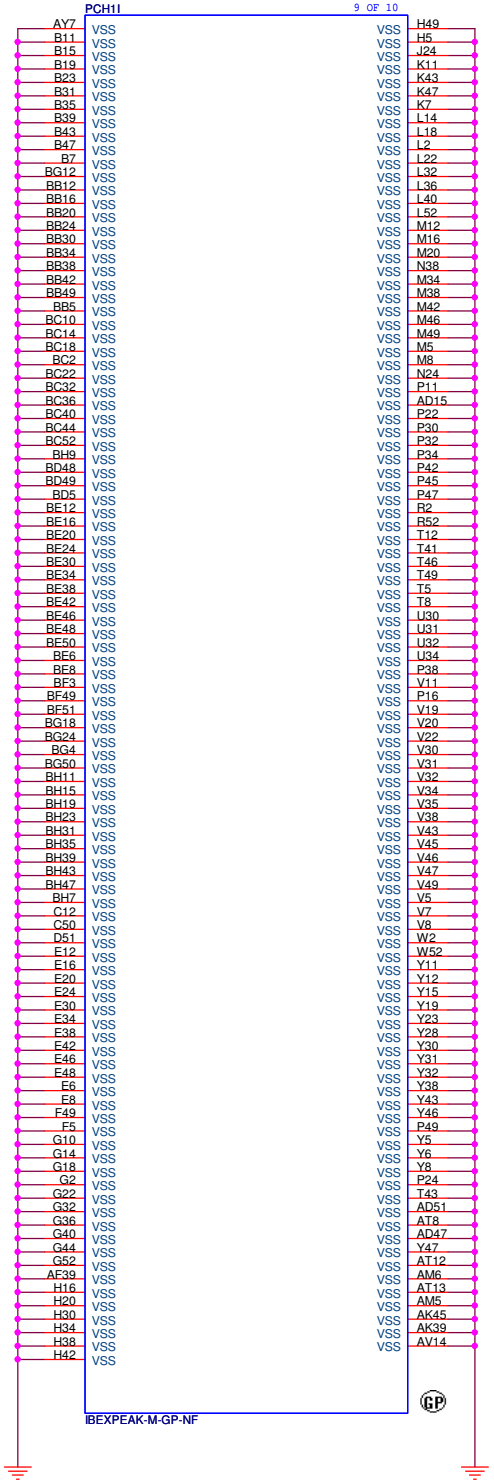
Title: PCH (8/9)

Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 27 of 89

SSID = PCH





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (9/9)	
Size: A3	Document Number: Fonseca 14.1" DIS	Rev: -1
Date: Thursday, March 18, 2010	Sheet 28 of 89	

(Blank)

<Core Design>

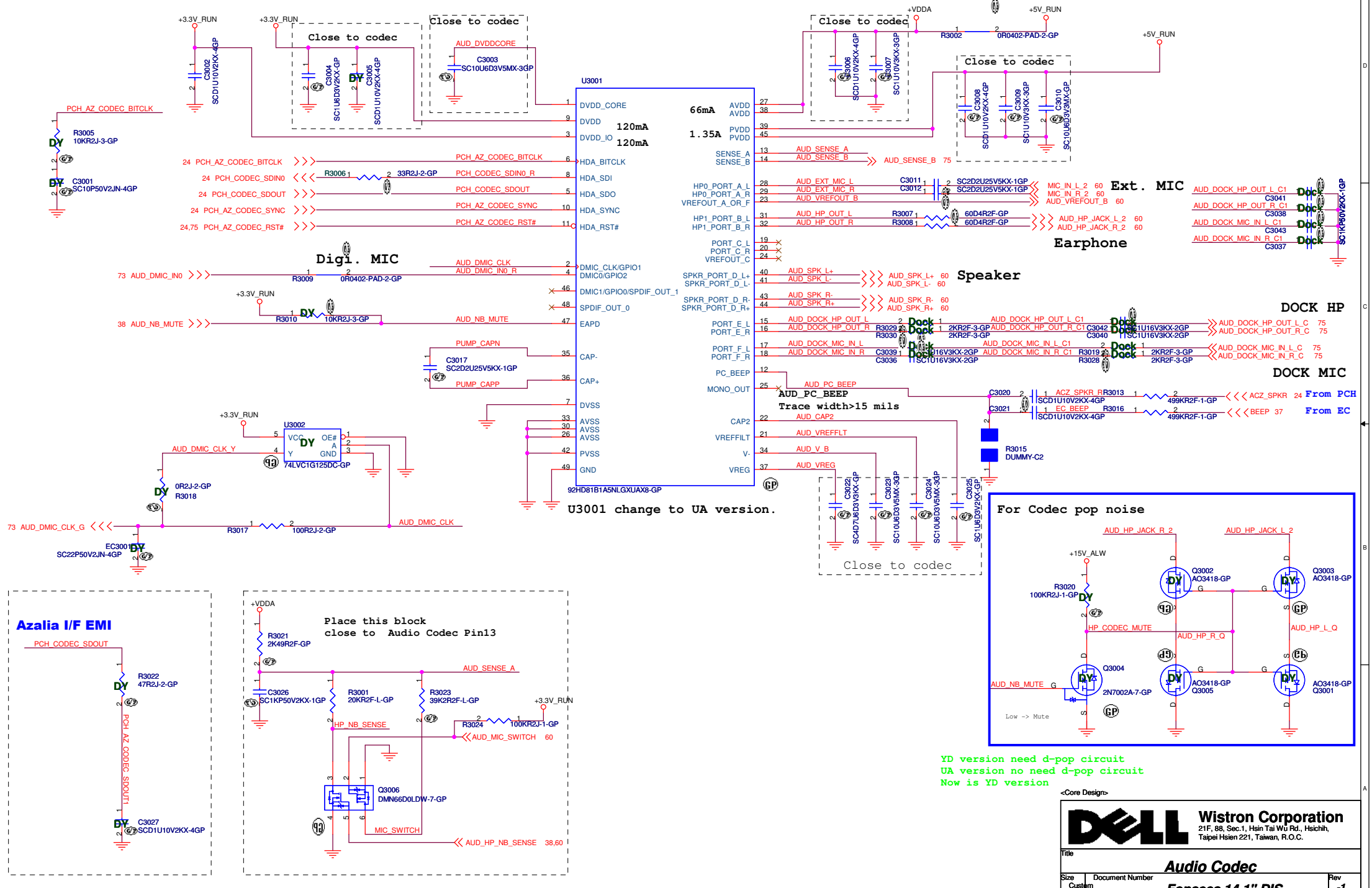
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: Custom | Document Number: *Fonseca 14.1" DIS* | Rev: *-1*

Date: Thursday, March 18, 2010 | Sheet 29 of 89

SSID = AUDIO


U3001
92HD81B1A5NLGXUAX8-GP
U3001 change to UA version.
Close to codec
Digi. MIC
Ext. MIC
Earphone
Speaker
DOCK HP
DOCK MIC
For Codec pop noise
Azalia I/F EMI
Place this block close to Audio Codec Pin13
YD version need d-pop circuit
UA version no need d-pop circuit
Now is YD version
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec
Fonseca 14.1" DIS
Thursday, March 18, 2010

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

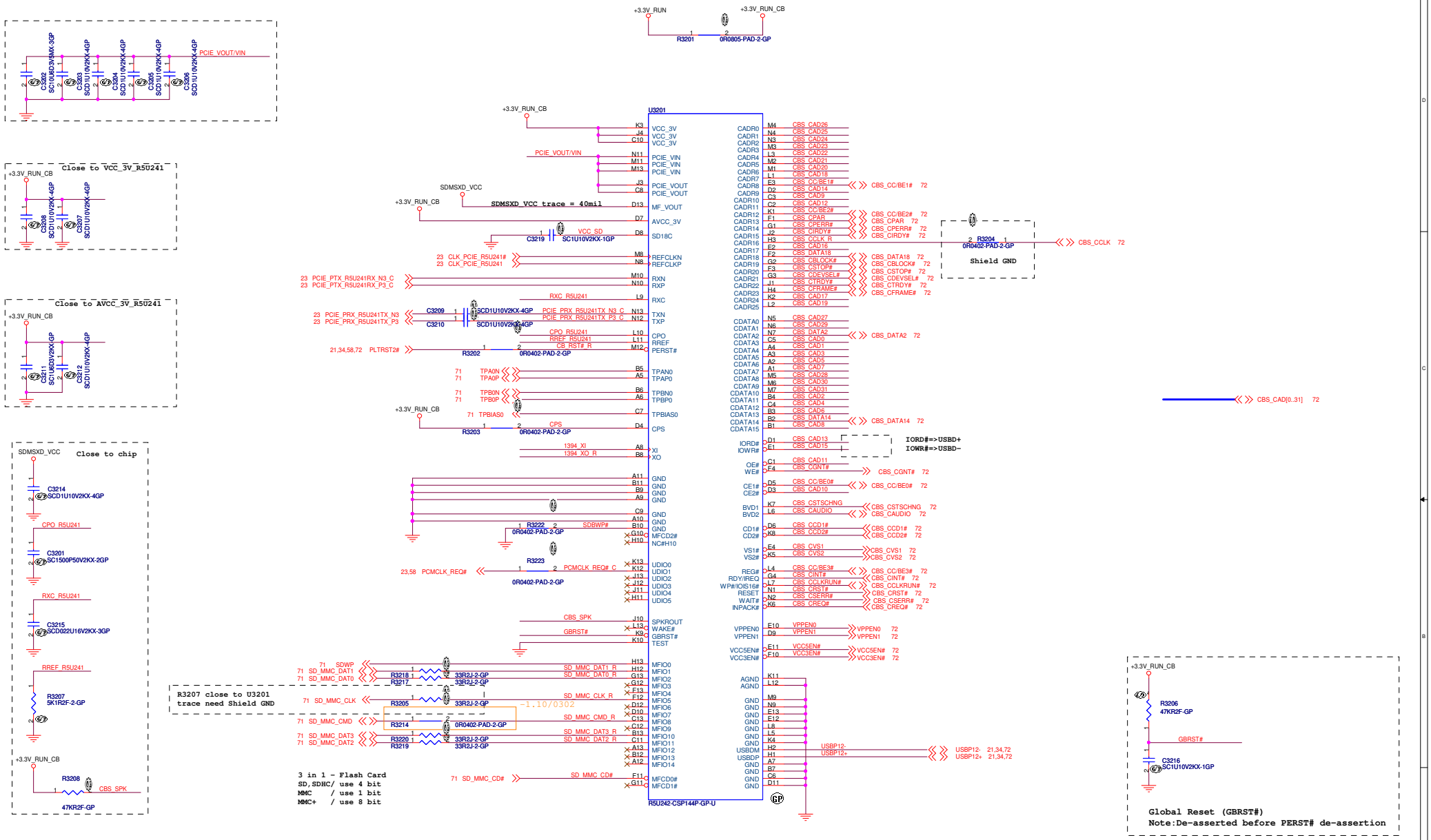
Title

Reserve

Size	Document Number	Rev
Custom	***Fonseca 14.1" DIS***	*-1*

Date:	Thursday, March 18, 2010	Sheet	31	of	89

SSID = 1394



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash Reader / 1394 / PCMCIA

Size	Document Number	Rev
C	Fonseca 14.1" DIS	-1

Date: Thursday, March 18, 2010 Sheet 32 of 89

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

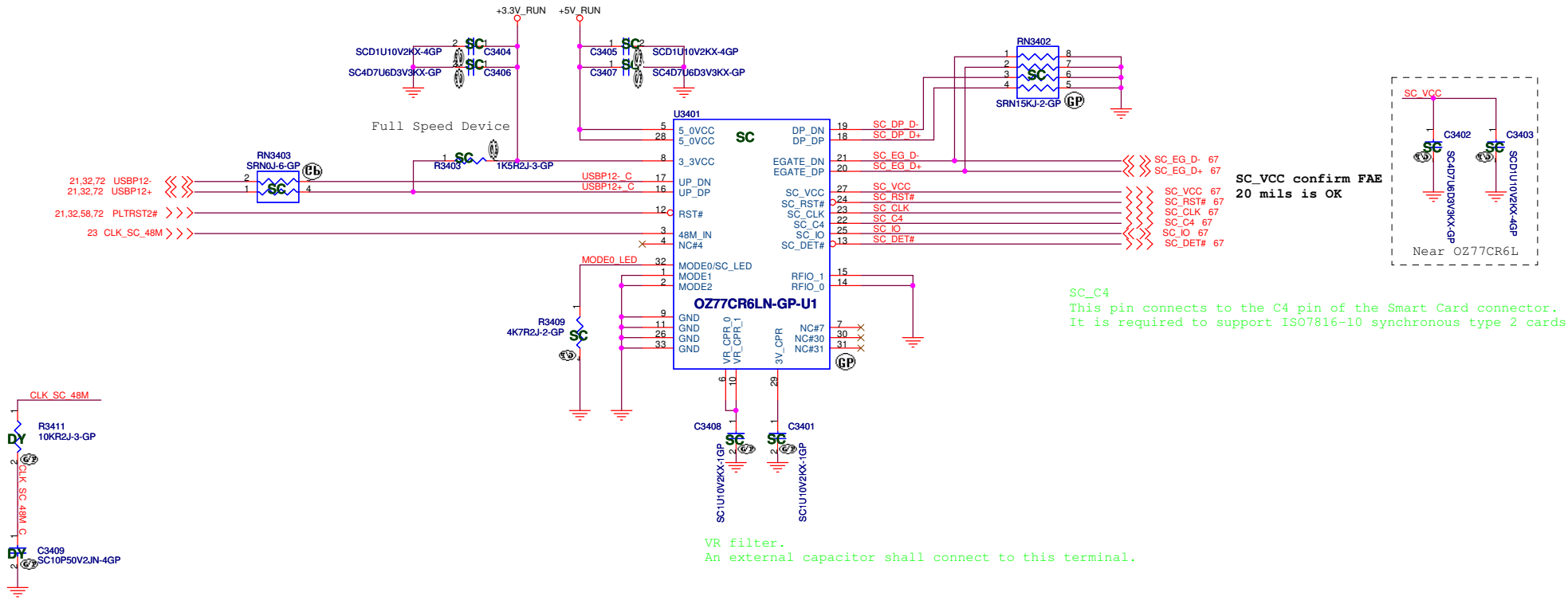
Reserve

Size	Document Number	Rev
Custom	***Fonseca 14.1" DIS***	*-1*

Date:	Thursday, March 18, 2010	Sheet	33	of	89

SSID = SmartCard

SmartCard Chip



MODE0 / SC_LED	This terminal is an output indicating Smart Card activity; capable to drive an external LED device. The SC_LED terminal drives a low logic level during Smart Card data read/write activity, and is capable to source 12mA of IOL current to drive an external LED circuit. When RST# is asserted, this terminal is sampled to select the downstream port configuration for DP_DP and DP_DN (Internal Port 1). When sampled low (4.7k), the downstream port device is removable. When sampled high, the downstream port is a non-removable device. Includes internal input pull-up resistor.
MODE1	Test Pin. This terminal shall be externally connected to GND.
MODE2	Test Pin. This terminal shall be externally connected to GND.

RFIO_0 **RFIO_1**	Contactless Smart Card Interface Signal 0 and 1. This signal provides detection and data communication with an external RF device. If contactless is disabled, then this terminal shall be pulled down to GND through a pull-down resistor, or directly connected to GND.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Smart Card (OZ77CR6LN)

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 34 of 89

SSID = LOM

SYMBOL: 71.05761.00U

Product : P802H /
71.05761.M02(Rev:B0)

Core Power Decoupling

VDDIOPower Decoupling

Put 0.1u cap close to Chip

Close to LAN chip

Close to the power pins and
0.1u cap should be closer to Chip

Populate resister for debug

8Mb for 5761E:
Main source: 72.45081.B01(Small PAD)
Second source: 72.45081.D01(Small PAD)

Atmel
Small PAD
AT45DB081D-SSU-GP

Numonyx
M25PE80-VMN6TP-GP

72.25P80.D01

Design current: 89.6mA
Max current: 128mA

Place crystal less
than 0.75" (~1.9cm)
from LAN Controller

Design Current: 627mA

DOCKED
SEL 0:RJ45.
SEL 1:Dock.

CTPM and DisableBTPM

B_TPM

Reserve for EMI

Logic High Voltage must
LE 0.7V to 2.75V

09/0529

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

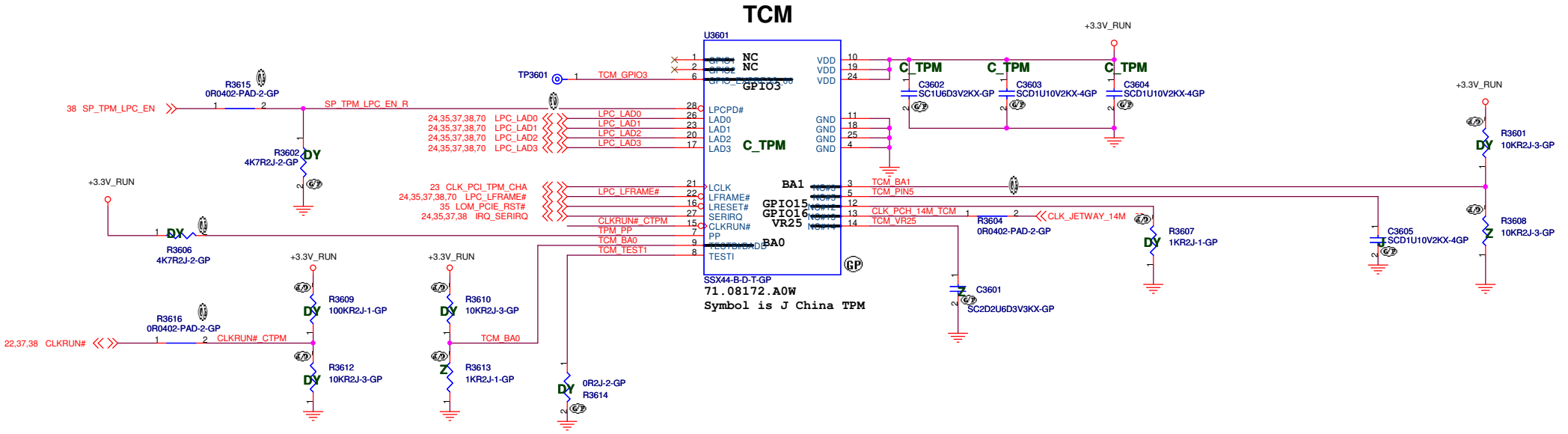
Title: GLAN - BCM5761E

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 35 of 89

SSID = TCM

Symbol : Jetway, but linked to ZTE
Product : 71.08172.00W (ZTE)



Z

Base Address	BA1 PIN3	BA0 PIN9
EE/EF	0	0
7E/7F	0	1
2E/2F	1	0
4E/4F	1	1

Default EE/EF as Amy recommended

J

	1(default)	0
PIN12	FLASH	SRAM

J has internal PU with PIN12.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TCM

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 36 of 89

SSID = KBC

MEC5045-LZY-GP

U3701

PS/2 INTERFACE
GPIO0007/I2C1D_DATA/PS2_CLK0B/I2C3A_DATA
GPIO0010/I2C1D_CLK/PS2_DAT0B/I2C3A_CLK
GPIO110/PS2_CLK2/GPTP-IN6
GPIO111/PS2_DAT2/GPTP-OUT6
GPIO112/PS2_CLK1A
GPIO113/PS2_DAT1A
GPIO114/PS2_CLK0A
GPIO115/PS2_DAT0A
GPIO154/I2C1C_DATA/PS2_CLK1B
GPIO155/I2C1C_CLK/PS2_DAT1B

JTAG INTERFACE
GPIO145/JTAG_TDI
GPIO146/I2C1K_CLK/JTAG_TDO
GPIO147/I2C1J_DATA/I2C2C_DATA/JTAG_CLK
GPIO150/I2C1J_CLK/I2C2C_CLK/JTAG_TMS
JTAG_RST#

0 = Reset JTAG I/F
1 = Disable

FAN PWM & TACH
GPIO050/FAN_TACH1
GPIO051/FAN_TACH2
GPIO052/FAN_TACH3
GPIO053/PWM0
GPIO054/PWM1
GPIO055/PWM2
GPIO056/PWM3

BC-LINK
GPIO123/BCM_A_CLK
GPIO122/BCM_A_DAT
GPIO121/BCM_A_INT#
GPIO022/BCM_B_CLK
GPIO023/BCM_B_DAT
GPIO024/BCM_B_INT#
GPIO044/BCM_C_CLK
GPIO043/BCM_C_DAT
GPIO042/BCM_C_INT#
GPIO047/LSBCM_D_CLK
GPIO046/LSBCM_D_DAT
GPIO045/LSBCM_D_INT#
GPIO032/GPTP-IN3/BCM_E_CLK
GPIO031/GPTP-OUT2/BCM_E_DAT
GPIO30/GPTP-IN2/BCM_E_INT#

HOST INTERFACE
GPIO011/SMI#
GPIO061/LPCPD#
LDRQ#
SER_IRQ
LRESET#
PCI_CLK
LFRAME#
LAD0
LAD1
LAD2
LAD3
CLKRUN#
GPIO100/EC_SCI#

MASTER CLOCK
XTAL1
XTAL2
GPIO160/32KHZ_OUT

MISC INTERFACE
GPIO021/RC_ID1
GPIO020/RC_ID2
GPIO025/UART_CLK
GPIO120/UART_TX
GPIO124/GPTP-OUT5/UART_RX
VCC_PRWGD
GPIO060/KBRST
GPIO101/ECGP_SCLK
GPIO103/ECGP_SIN
GPIO105/ECGP_SOUT
GPIO102/HSPI_SCLK
GPIO104/HSPI_MISO
GPIO106/HSPI_MOSI
GPIO116/MSDATA
GPIO117/MSCLK
GPIO127/A20M
GPIO153/LED3
GPIO156/LED1
GPIO157/LED2
FWP#
SYSTEM_ID
BOARD_ID
DDR_ON
HOST_DEBUG_TX
HOST_DEBUG_RX
RUNPWROK
EN_INVPWR
EC_GPIO101
EC_GPIO103
EC_GPIO105
DDR_HVREF_RST_GATE
EC_GPIO104
CPU1.5V_S3_GATE
MSDATA
MSCLK
SIO_A20GATE
PS_ID
BAT1_LED#
BAT2_LED#
FWP#

GENERAL PURPOSE I/O
GPIO001/ECSPI_CS1
GPIO002/ECSPI_CS2
GPIO014/GPTP-IN7/HSPI_CS1
GPIO040/GPTP-OUT3/HSPI_CS2
GPIO015/GPTP-OUT7
GPIO016/GPTP-IN8
GPIO017/GPTP-OUT8
GPIO26/GPTP-IN1
GPIO27/GPTP-OUT1
GPIO041
GPIO107/nRESET_OUT
GPIO125/GPTP-IN5
GPIO126
GPIO151/GPTP-IN4
GPIO152/GPTP-OUT4
EC_GPIO001
DOCK_SMB_ALERT#
FFS_INT1
H_SKTOCC#
ME_SUS_PWR_ACK
1.5V_SUS_PWRGD
EC_GPIO017
EC_GPIO026
ALW_PWRGD_3V_5V
ODD_DET#
RESET_OUT#
EC_GPIO125
PCH_RSMRST#
AC_PRESENT
SIO_PWRBTN#

SMBUS INTERFACE
GPIO003/I2C1A_DATA
GPIO004/I2C1A_CLK
GPIO005/I2C1B_DATA
GPIO006/I2C1B_CLK
GPIO012/I2C1H_DATA/I2C2D_DATA
GPIO013/I2C1H_CLK/I2C2D_CLK
GPIO130/I2C2A_DATA
GPIO131/I2C2A_CLK
GPIO132/I2C1G_DATA
GPIO140/I2C1G_CLK
GPIO141/I2C1F_DATA/I2C2B_DATA
GPIO142/I2C1F_CLK/I2C2B_CLK
GPIO143/I2C1E_DATA
GPIO144/I2C1E_CLK
DOCK_SMB_DAT
DOCK_SMB_CLK
LCD_SMBDAT
LCD_SMBCLK
CKG_SMBDAT
CKG_SMBCLK
AUD_DOCK_SMBDAT
AUD_DOCK_SMBCLK
CHARGER_SMBDAT
CHARGER_SMBCLK
CARD_SMBDAT
CARD_SMBCLK
LAN_SMBDAT
LAN_SMBCLK

DELL PWR SW INF
BGPO0
VCI_IN2#
VCI_OUT
VCI_IN1#
VCI_IN0#
VCI_OVRD_IN
VCI_IN3#
EC_BGPO0
VCI_IN2#
ALW_ON
VCI_IN1#
POWER_SW_IN#
ACAV_IN
DOCK_PWR_SW#

Fonseca 14.1" DIS Revision

SYSTEM_ID	BOARD_ID Cap. Value	BOARD_ID Cap. Value	REV
2k ohm / 4700pF	4700pF	240k ohm	X00
	4700pF	130k ohm	X01
	4700pF	62k ohm	X02
	4700pF	33k ohm	-1

Place close to Pin58

09/0703
PCH side, pull down 8.2k

R3734 pull DN, Enable JTAG debug mode

-1.10/0301
-1.10/0302

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC - MEC5045
Size: Custom
Document Number: Fonseca 14.1" DIS
Rev: -1
Date: Thursday, March 18, 2010
Sheet 37 of 89

SSID = KBC

U3801 ECE5028-LZY-GP

CRD_DET1	CRD_DET0	Function
Low	Low	No Option Installed
Low	High	Smartcard
High	Low	Cardbus
High	High	Express Card

Place close to Pin.A28

Place close to Pin.A32

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SIO - MEC5028

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 38 of 89

SSID = Thermal

BC Bus clock and data signal trace length should be matched with +/- 0.1 inch.

REM_DIODE3_N, REM_DIODE3_P routing together.
Trace width / Spacing = 10 / 10 mil
Place near the bottom SODIMM

Q3902 and C3902 Place under CPU
PORT 1
Place C3902 close to the Q3902 as possible

Q3905 and C3906 Place near DIMM
PORT 4
Place C3906 close to Q3905

Skin Temp Sensor
PORT 2
Place optimally between VGA and PCH
Place C3904 close to Q3901

PORT 3

close to the Guardian pins

R3905 ~ if use 4.7k about 2% inaccuracy for IMON
Place near fork into U3901

Rset=953, Tp=88degree

09/0824, symbol updated

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

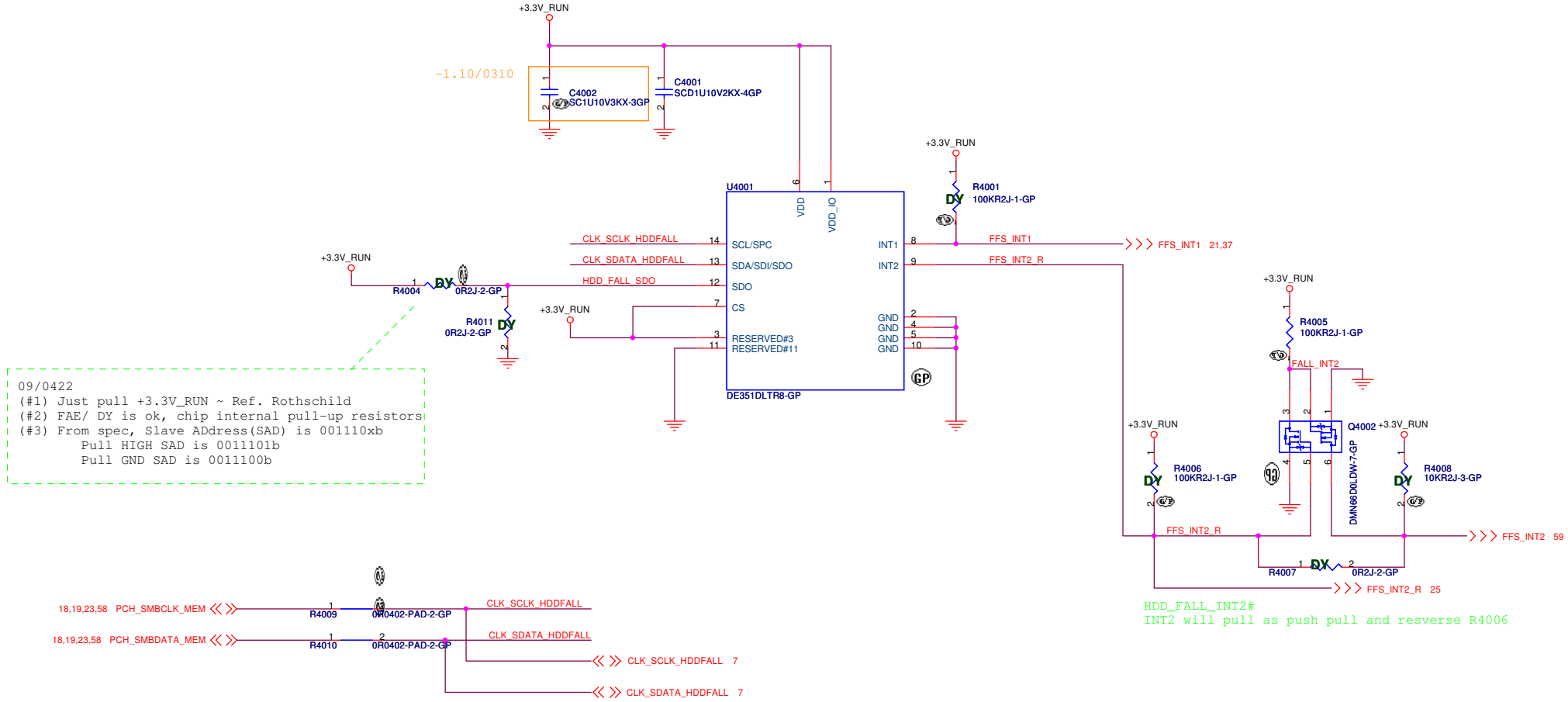
Title: Thermal, Fan controller

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 39 of 89

SSID = User.Interface

Free Fall Sensor



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor
Size: A3
Document Number: Fonseca 14.1" DIS
Rev: -1
Date: Thursday, March 18, 2010
Sheet 40 of 89

SSID = Reset.Suspend

<Core Design>

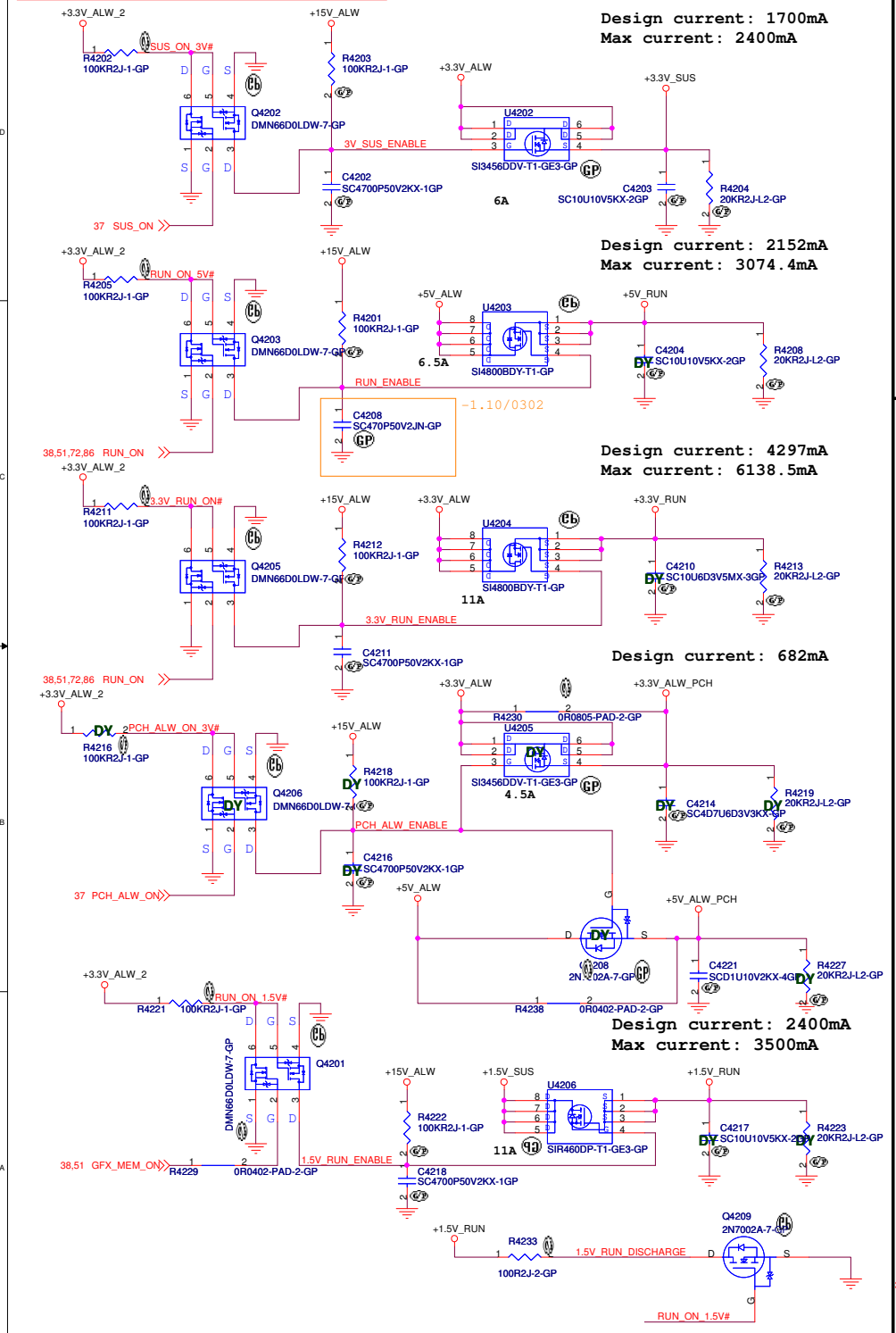
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power On Logic

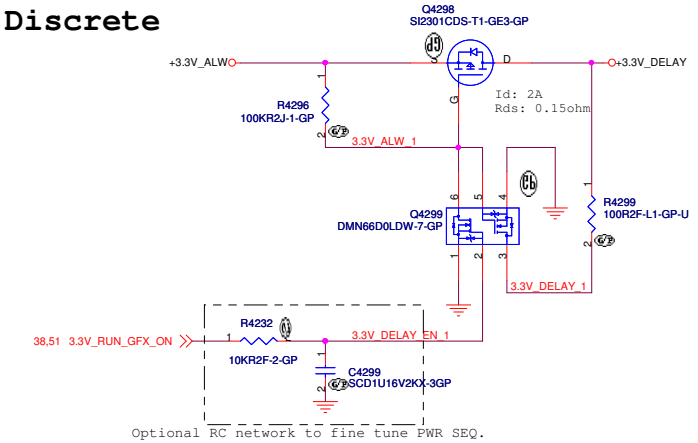
Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

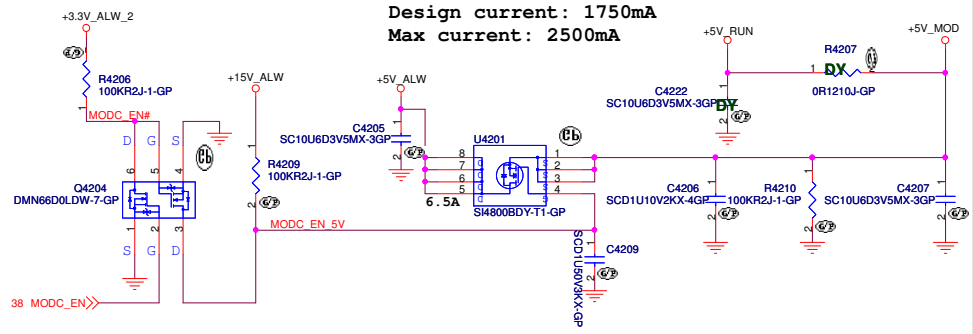
Date: Thursday, March 18, 2010 | Sheet 41 of 89

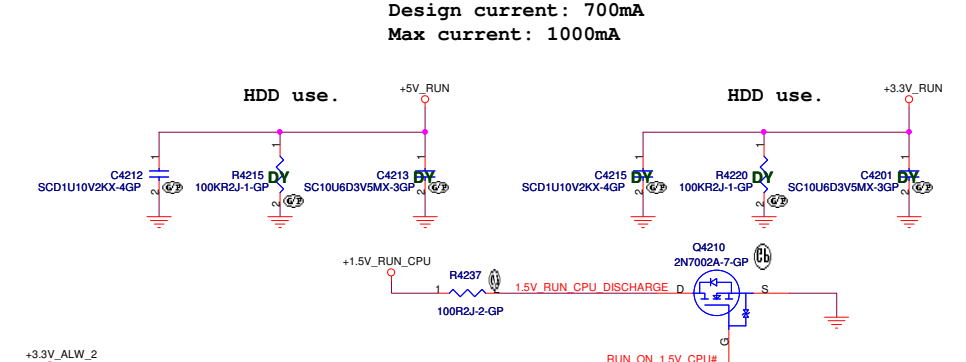
SSID = Reset.Suspend

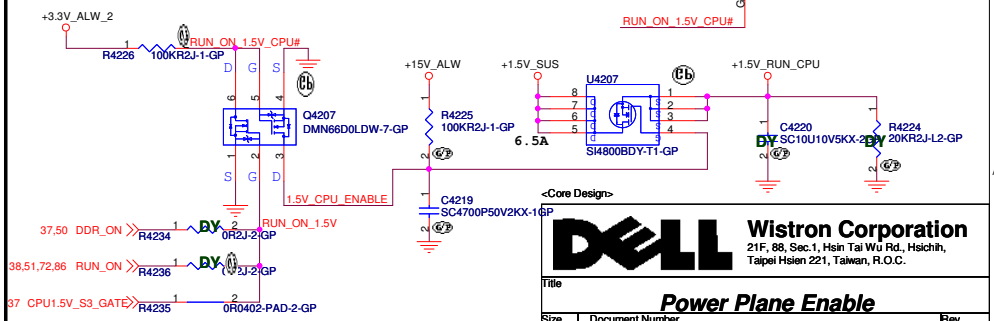


For Discrete









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Plane Enable***

Size	Document Number	Rev
Custom	***Fonseca 14.1" DIS***	-1

Date: Thursday, March 18, 2010 Sheet 42 of 89

SSID = PWR.Support

Adapter In

DC_IN CONN	
PIN 3,4	DC_IN+
PIN 4,5	DC_IN-
PIN 1	ID
PIN 6,7,8,9	GND

PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL	BQ24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMP	FBO
7	DAC	NC	CE
8	IINP	ICM	VICM
11	VDD	VDDSMB	VDDSMB
14	BATSEL	NC	NC
15	FBSA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSON	CSON
18	CSIP	CSOP	CSOP
20	DLO	LGATE	LGATE
21	LDO	VDDP	VDDP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGSTE
25	BST	BOOT	BOOT
26	VCC	VCC	ICOUT

"NC" means no-connect

TABLE
MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL	TI
R411	8.45K 1%	DUMMY	DUMMY
C98	0.01uF	0.1uF	0.1uF
C459	0.1uF 10V	DUMMY	200P 10V
C5	1uF 10V	DUMMY	1uF 10V
R16	365K 1%	215K 1%	309K 1%
R434	0 5%	10 5%	0 5%
R414	0 5%	10 5%	0 5%
C473	DUMMY	0.22uF	0.1uF
C457	DUMMY	0.22uF	0.1uF
C442	0.01uF	DUMMY	DUMMY
C453	0.1uF 10V	DUMMY	DUMMY
C36	220pF 50V	DUMMY	DUMMY
D23	RB751V-40	DUMMY	RB751V-40
C58	3.3nF	DUMMY	DUMMY
R64	1 1%	0 5%	0 5%
R394	100 5%	0 5%	0 5%
R110	0 5%	8.45K 1%	8.45K 1%
R401	10K 5%	2.2K 5%	4.7K 5%
C441	0.01uF	0.01uF	DUMMY
C449	0.01uF	0.01uF	DUMMY
R397	1K 5%	DUMMY	DUMMY
Q41	ISS355	DUMMY	DUMMY
C16	1uF 10V	1uF 10V	DUMMY
R30	33 1%	33 1%	DUMMY
R408	DUMMY	DUMMY	0 5%
R400	DUMMY	DUMMY	200K 5%
R403	DUMMY	DUMMY	7.5K 5%
C450	DUMMY	DUMMY	51P 10V
C444	DUMMY	DUMMY	2000P 10V
C448	DUMMY	DUMMY	130P 10V
C446	DUMMY	DUMMY	0.1uF
C483	DUMMY	DUMMY	0.1uF
R438	10K 1%	10K 1%	DUMMY
R412	DUMMY	DUMMY	10k 5%
R440	15.8K 1%	15.8K 1%	DUMMY
R407	DUMMY	10K 5%	DUMMY
R9	0 5%	10 5%	0 5%
C482	DUMMY	DUMMY	DUMMY
C12	DUMMY	DUMMY	DUMMY
R435	0 5%	10 5%	0 5%

MAX 8731A/ISL88731

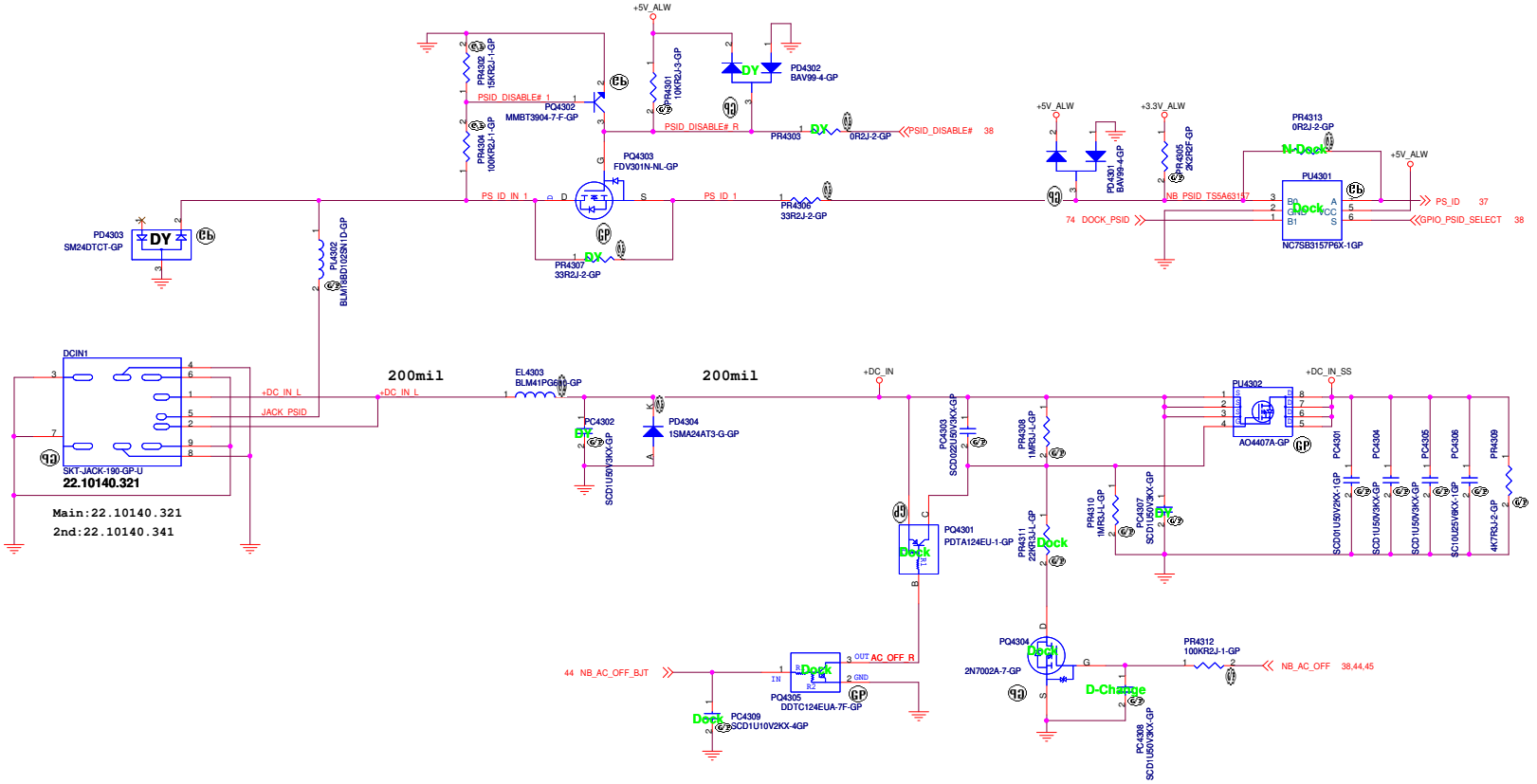
Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	13.0K	105	24.9K
90	4.43	51.1K	17.8K	348	33.2K

*R504 is populated if ADAPT_TRIP_SEL is used
to program for the next lower adapter.

BQ247451

Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	12.4K	205	24.3K
90	4.43	51.1K	16.9K	499	32.4K

*R504 is populated if ADAPT_TRIP_SEL is used
to program for the next lower adapter.



<Core Design>

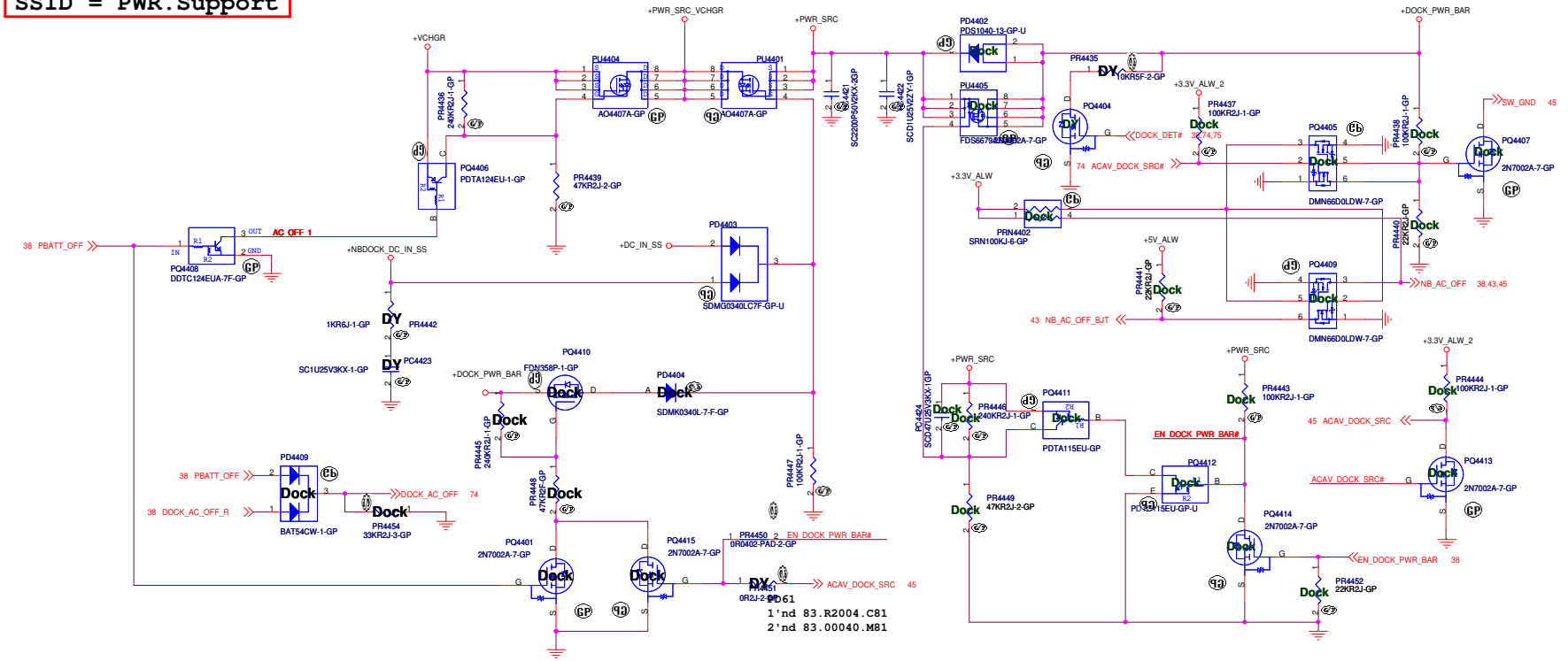
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC IN Jack

Size: C | Document Number: Fonseca 14.1" DIS | Rev: -1

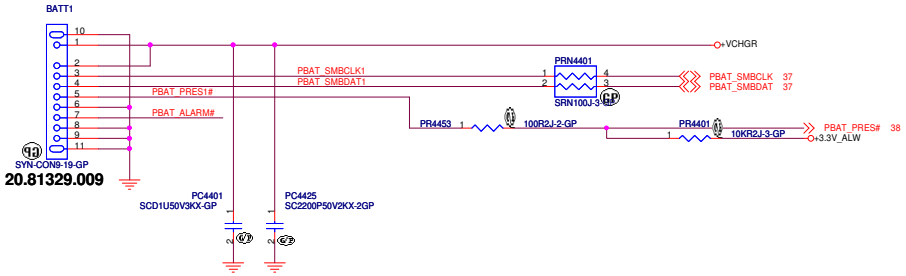
Date: Thursday, March 18, 2010 | Sheet 43 of 89

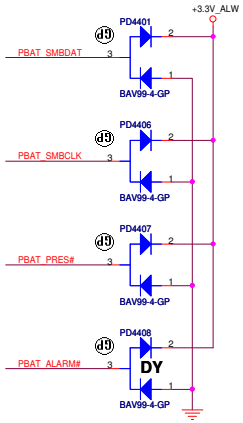
SSID = PWR.Support



SSID = RBATT

Batt Connecter





<Core Design>

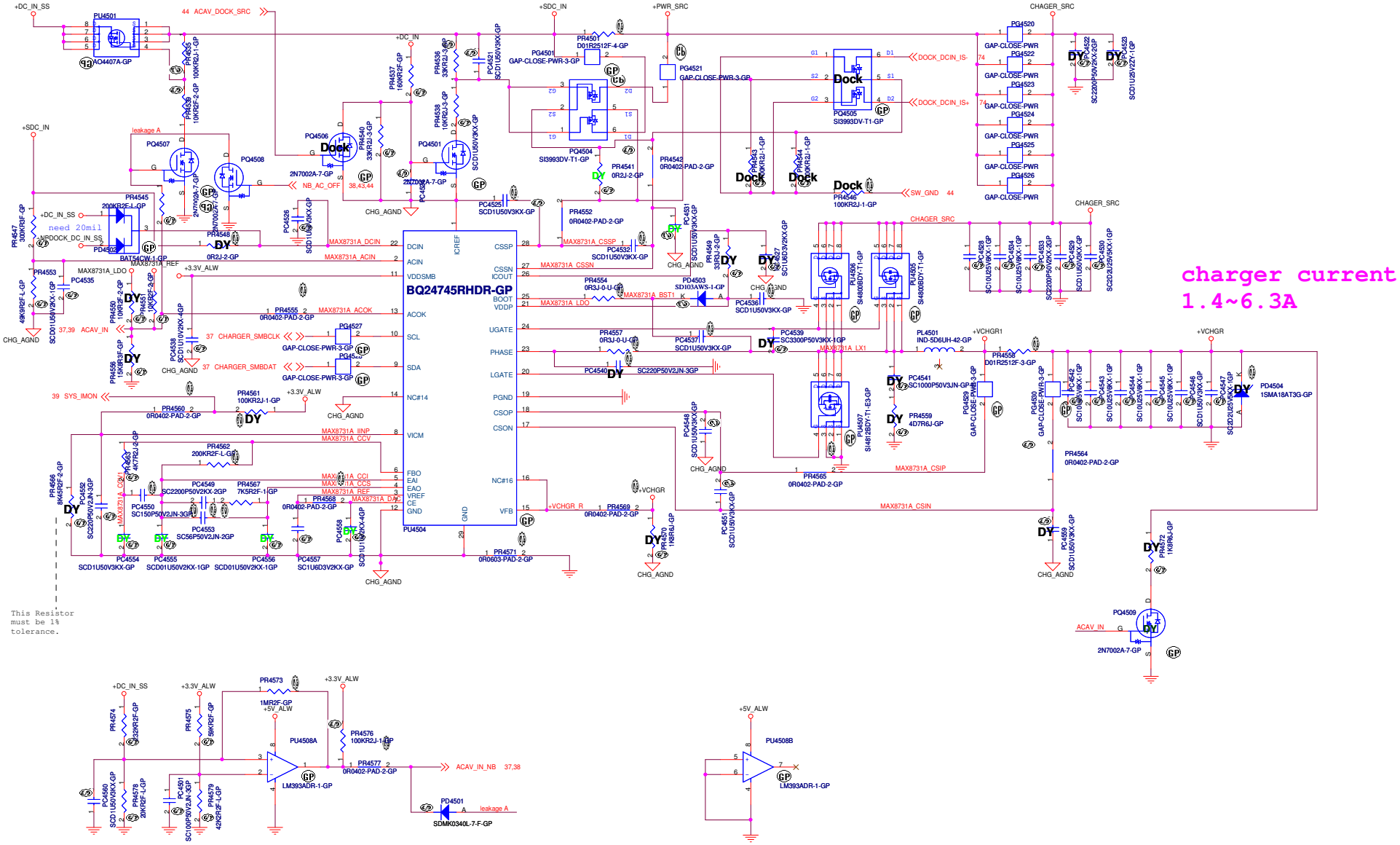
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DOCK DCIN/BATT Connector

Size: C | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 44 of 89

SSID = Charger



<Core Design>

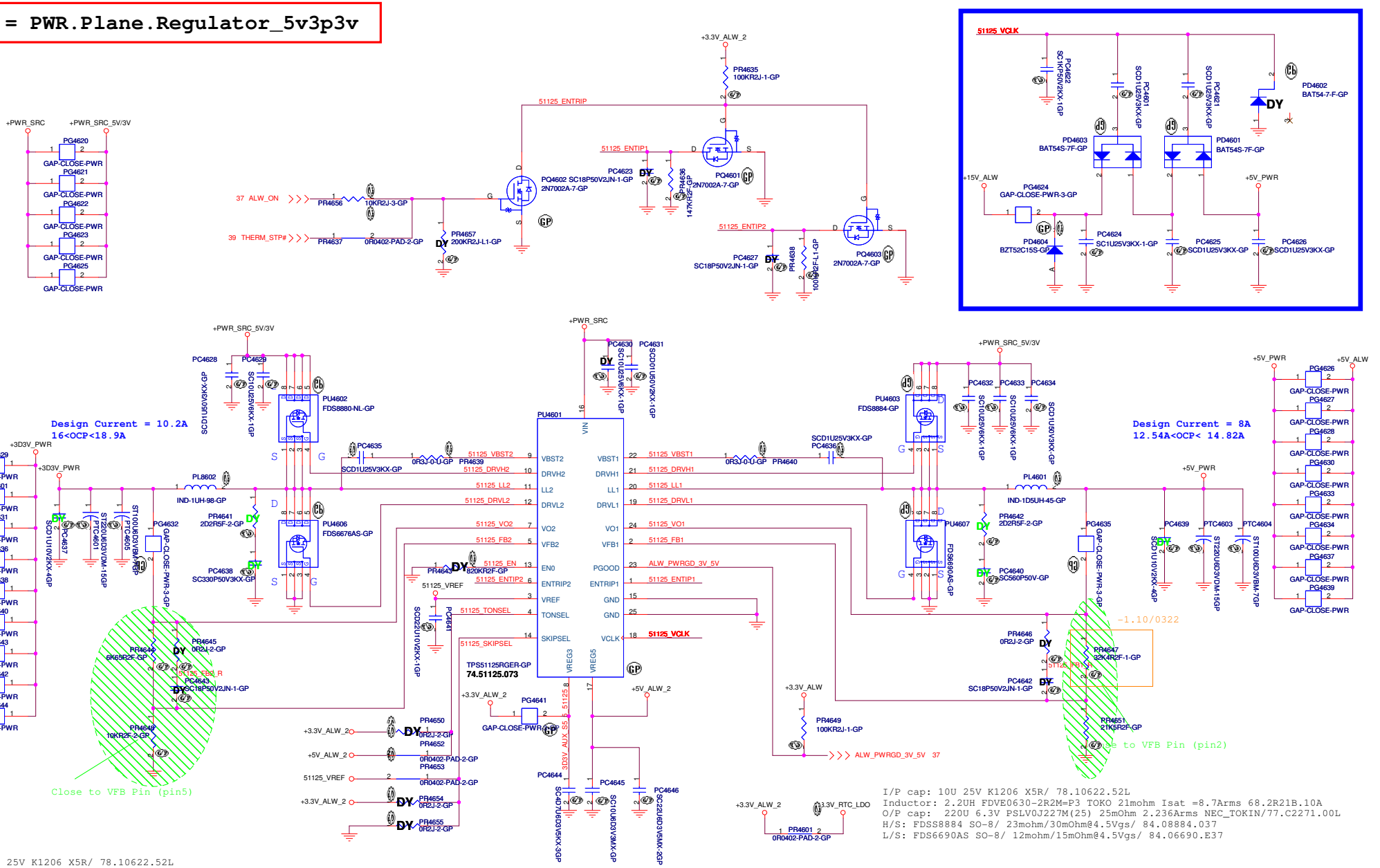
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Battery Charger**

Size	Document Number	Rev
C	Fonseca 14.1" DIS	-1

Date: Thursday, March 18, 2010 Sheet 45 of 89

SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH FDV0630-3R3M=P3 TOKO 31mohm Isat =6.9Arms 68.3R31A.10E
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE0630-2R2M=P3 TOKO 21mohm Isat =8.7Arms 68.2R21B.10A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 5V/3D3V (TPS51125)
Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1
Date: Monday, March 22, 2010 | Sheet 46 of 89

SSID = CPU.Regulator

~1.10/0305

NTC 470K close to H/S MOSFET of Phase1

X01.09/1020

74.62883.B73

1210 SB

1210 SB

NTC 10K close to Choke of Phase1

Design Current = 48A

Intel support POC (Power On Configuration).

<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *ISL62883_CPU_CORE_1*		
Size: A2	Document Number: *Fonseca 14.1" DIS*	Rev: *-1*
Date: Thursday, March 18, 2010	Sheet 47 of 89	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: A3 | Document Number: *Fonseca 14.1" DIS* | Rev: *-1*

Date: Thursday, March 18, 2010 | Sheet 48 of 89

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<Core Design>

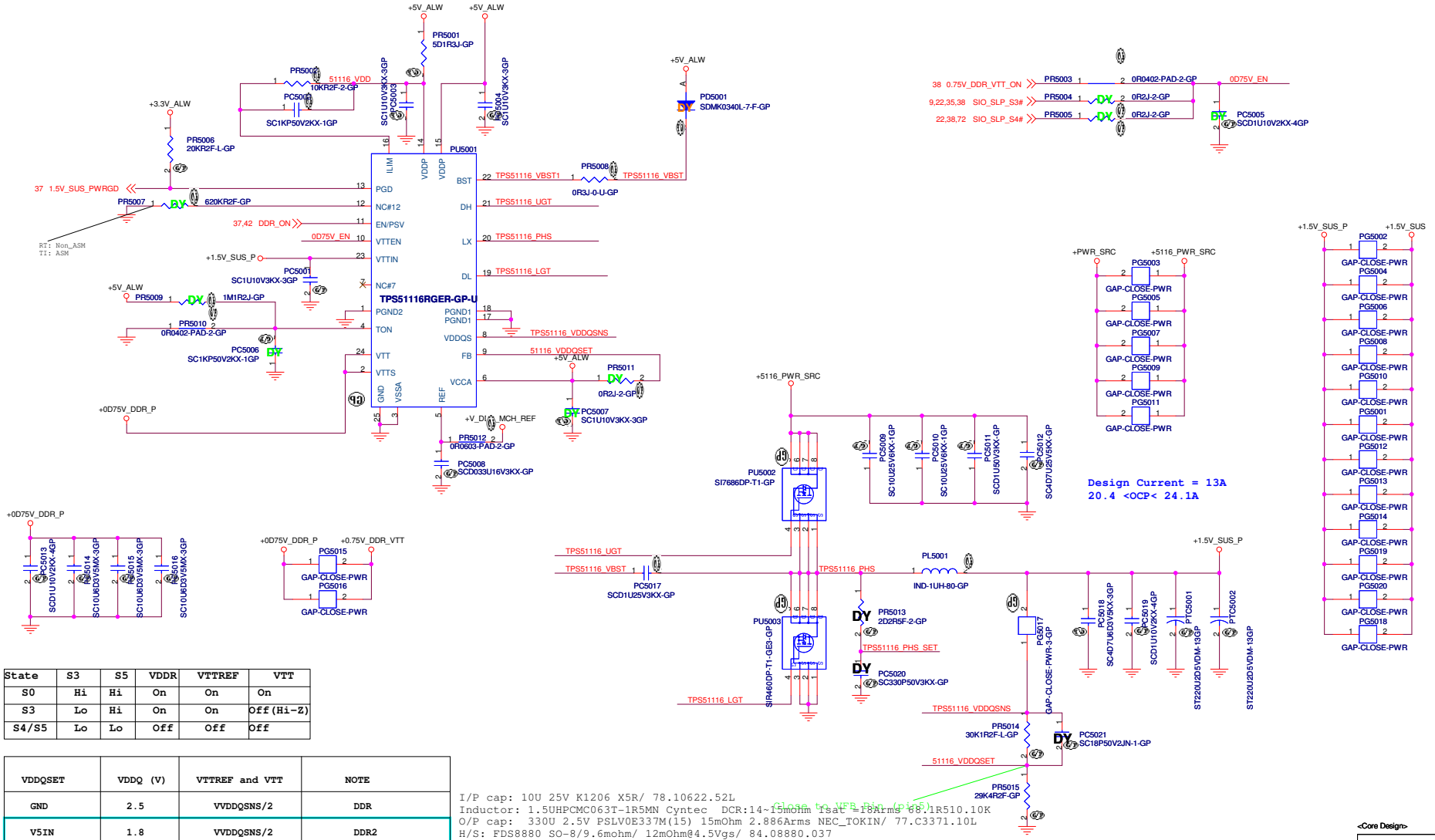
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.05V

Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 49 of 89

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC063T-1R5MN Cyntec DCR:14~15mohm Isat = 18Arms 68.1R510.10K
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->400KHz

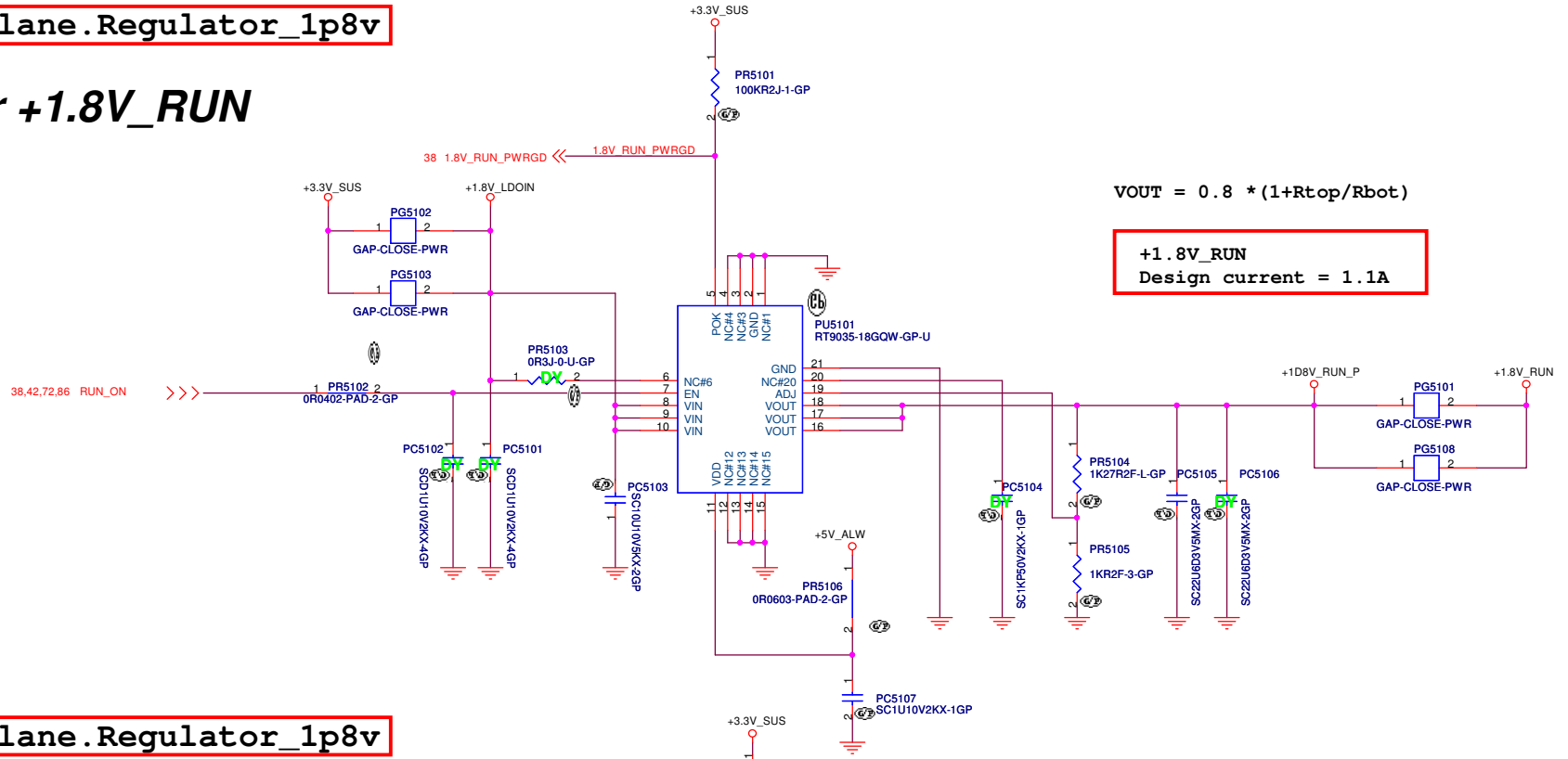
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.5V / 0.75V
Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1
Date: Thursday, March 18, 2010 | Sheet 50 of 89

SSID = PWR.Plane.Regulator_1p8v

LDO for +1.8V_RUN

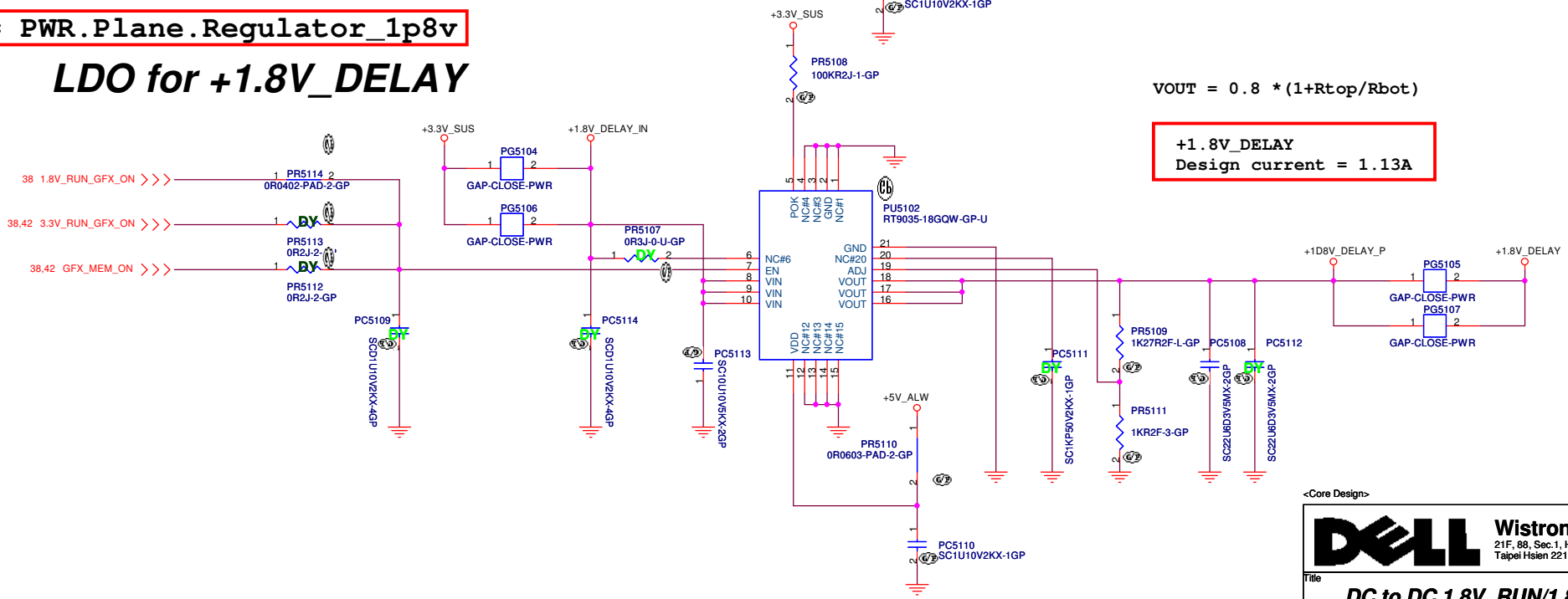


VOUT = 0.8 *(1+Rtop/Rbot)

+1.8V_RUN
Design current = 1.1A

SSID = PWR.Plane.Regulator_1p8v

LDO for +1.8V_DELAY



VOUT = 0.8 *(1+Rtop/Rbot)

+1.8V_DELAY
Design current = 1.13A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

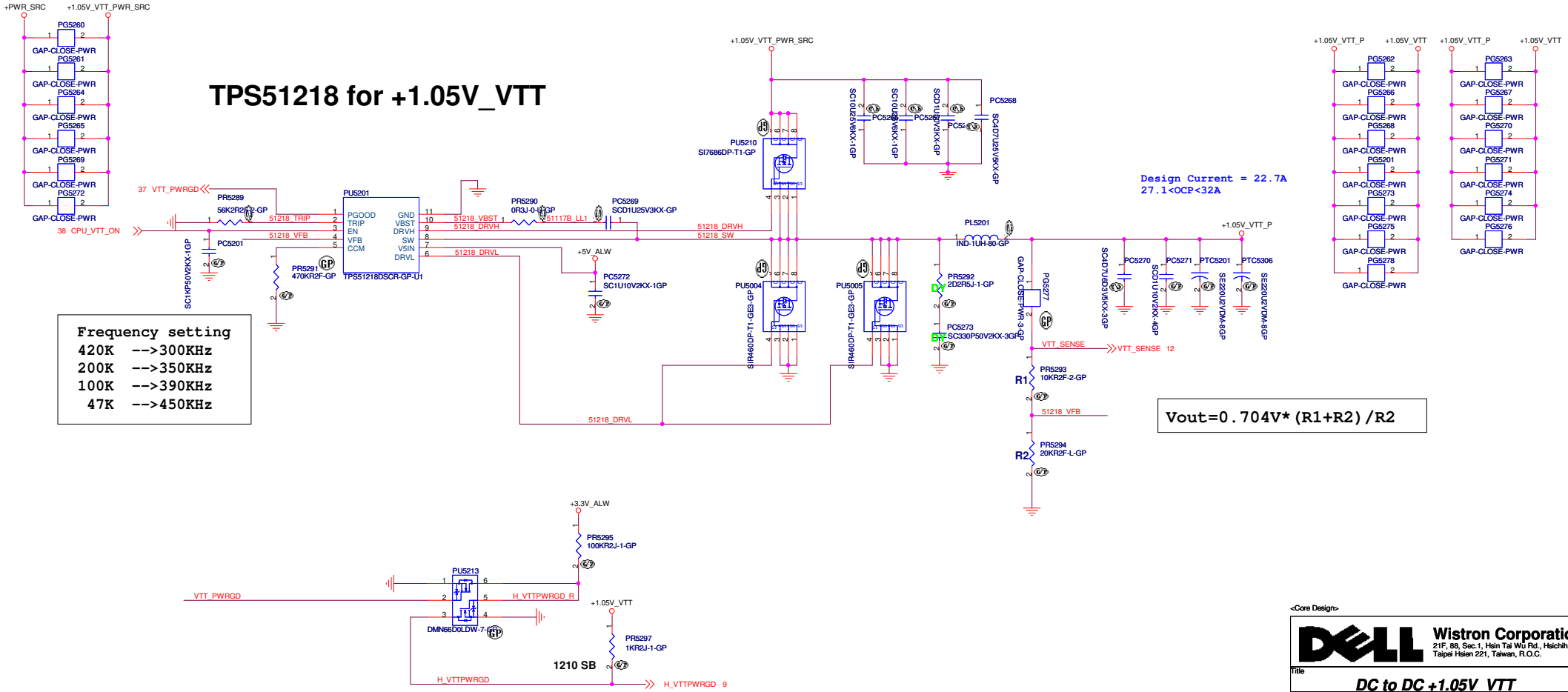
Title: DC to DC 1.8V_RUN/1.8V_DELAY

Size	Document Number	Rev
A3	Fonseca 14.1" DIS	-1

Date: Thursday, March 18, 2010 Sheet 51 of 89

SSID = PWR.Plane.Regulator_1p05v

TPS51218 for +1.05V_VTT



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC to DC +1.05V_VTT	
Size: Custom	Document Number: Fonseca 14.1" DIS	Rev: -1
Date: Thursday, March 18, 2010	Sheet 52 of 89	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

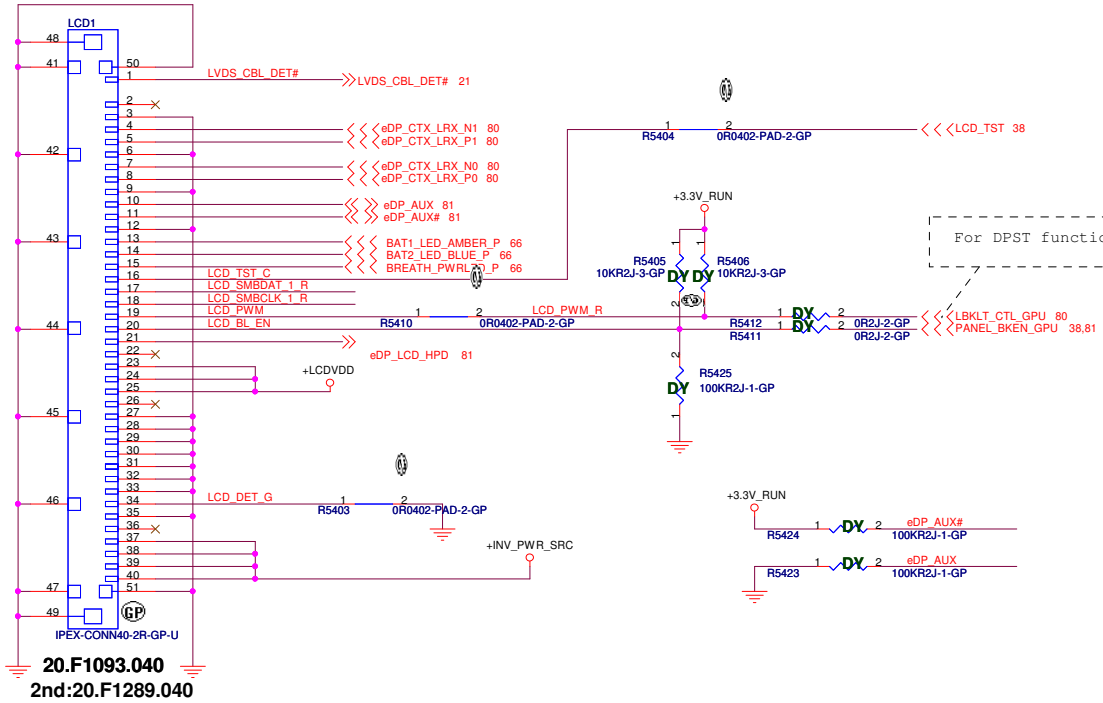
CPU GFXCORE

Size	Document Number	Rev
Custom	Fonseca 14.1" DIS	-1

SSID = VIDEO

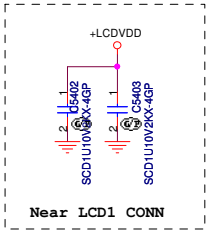
LED Location from left to right

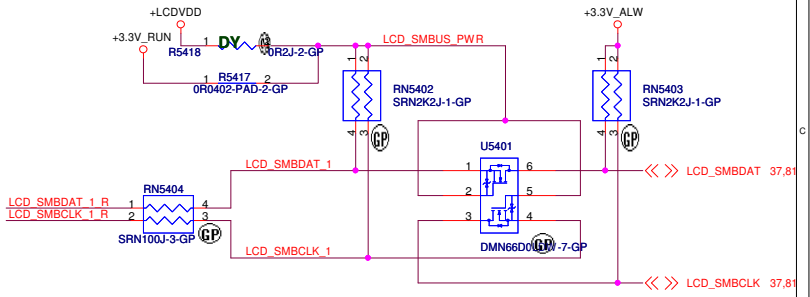
HDD | BATTERY



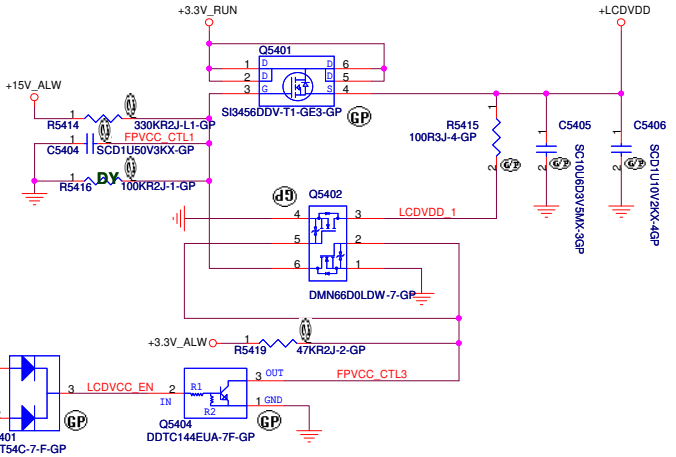
20.F1093.040

2nd:20.F1289.040



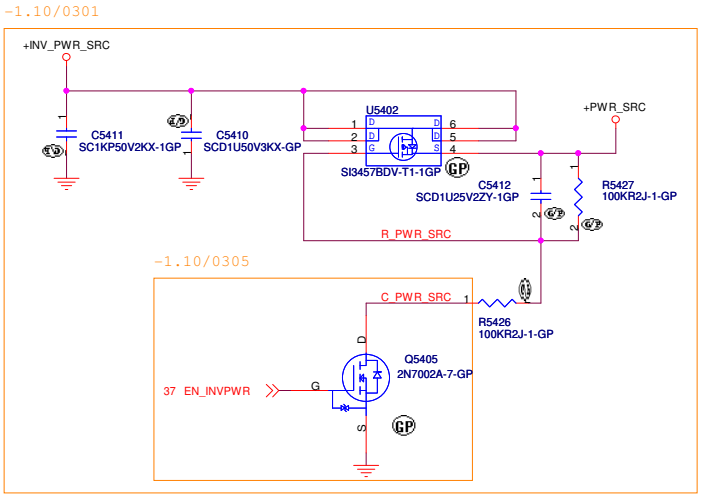


LCD POWER



SSID = Inverter

LED BACKLIGHT CONVERTER POWER



<Core Design>

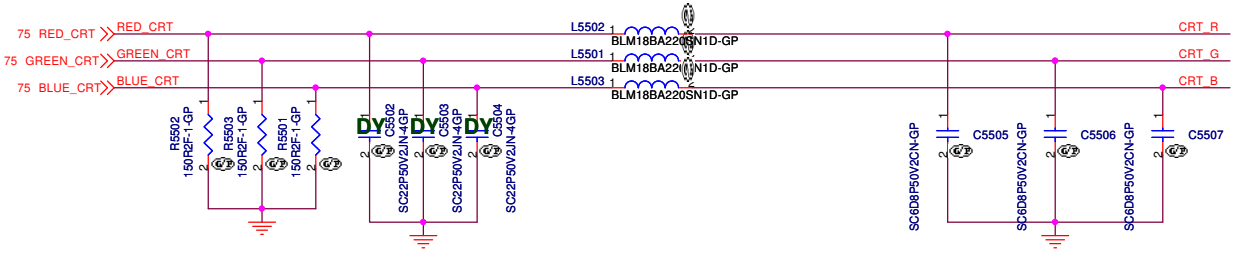
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

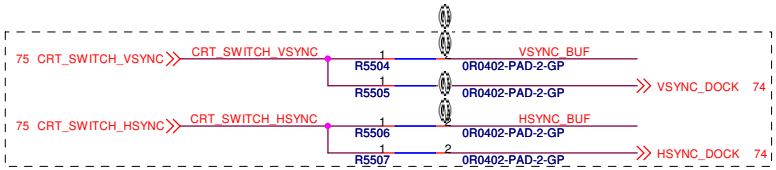
Title: LCD

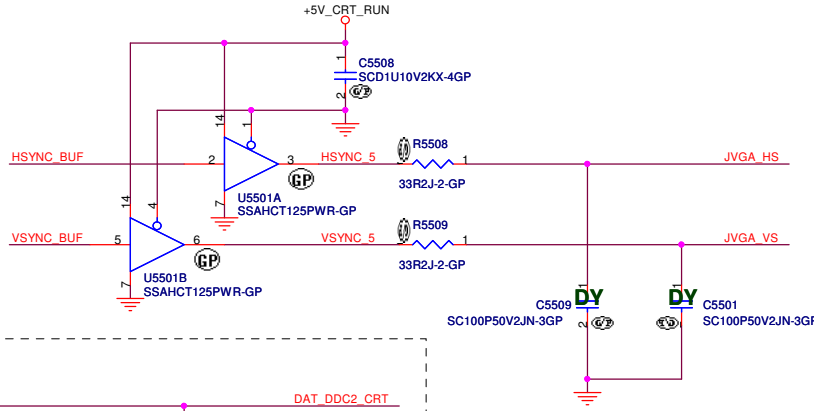
Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 54 of 89

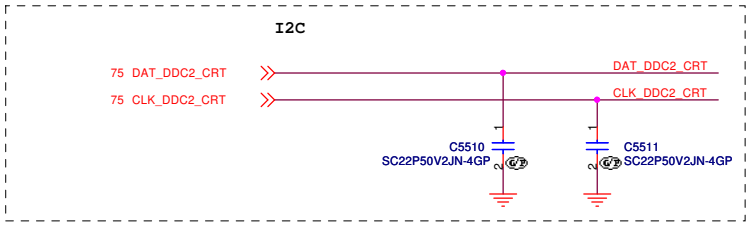
SSID = VIDEO



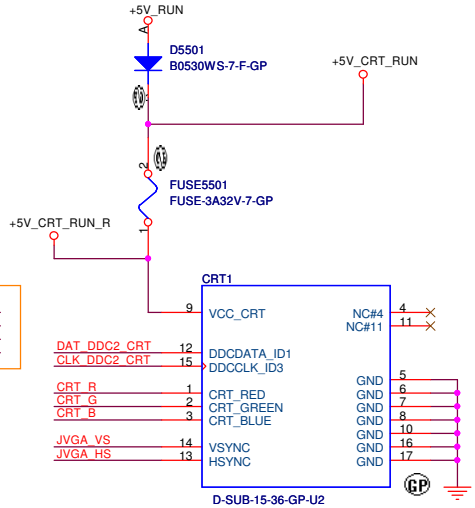




Layout Note:
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



MAX4885E has internal ESD protection and internal level shift



-1.10/0310

AFTP5501 +5V_CRT_RUN_R
AFTP5502 CRT_R
AFTP5503 CRT_G
AFTP5504 CRT_B

20.20431.015

CRT Connector

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT

Size	Document Number	Rev
A3	Fonseca 14.1" DIS	-1

Date: Thursday, March 18, 2010 Sheet 55 of 89

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: A3 | Document Number: *Fonseca 14.1" DIS* | Rev: *-1*

Date: Thursday, March 18, 2010 | Sheet 56 of 89

(Blank)

<Core Design>

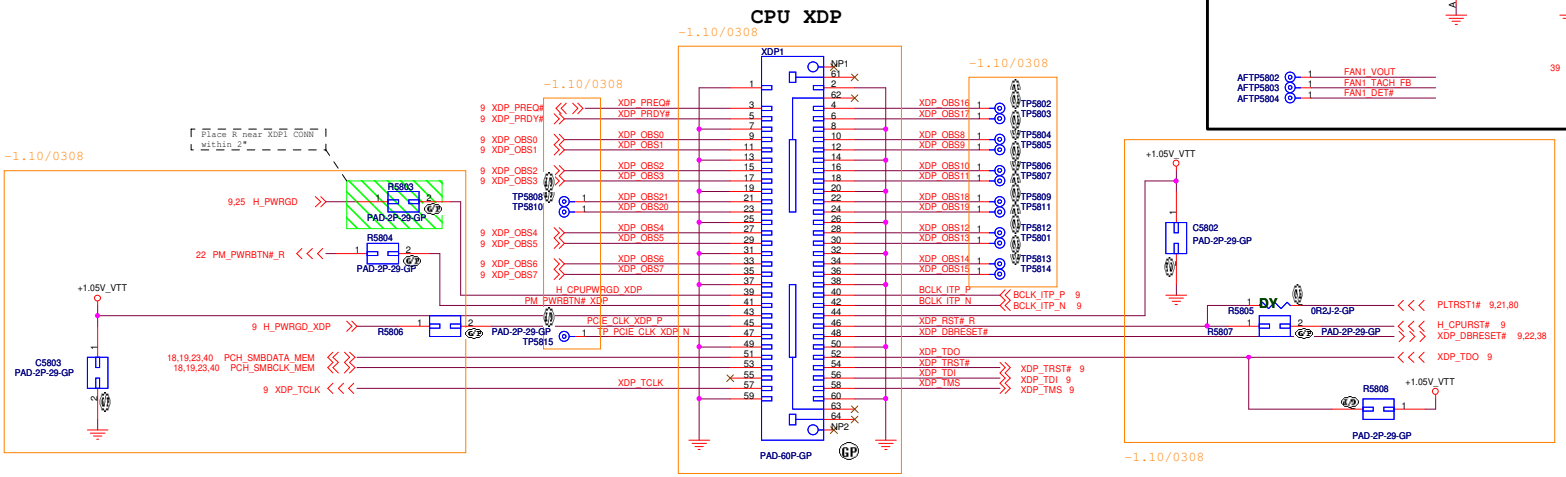
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

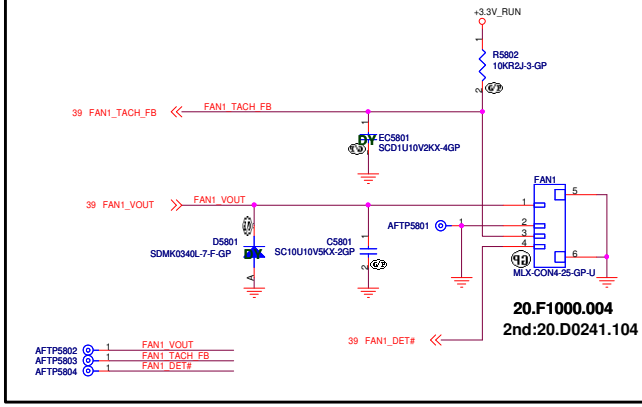
Size: A3 | Document Number: *Fonseca 14.1" DIS* | Rev: *-1*

Date: Thursday, March 18, 2010 | Sheet 57 of 89

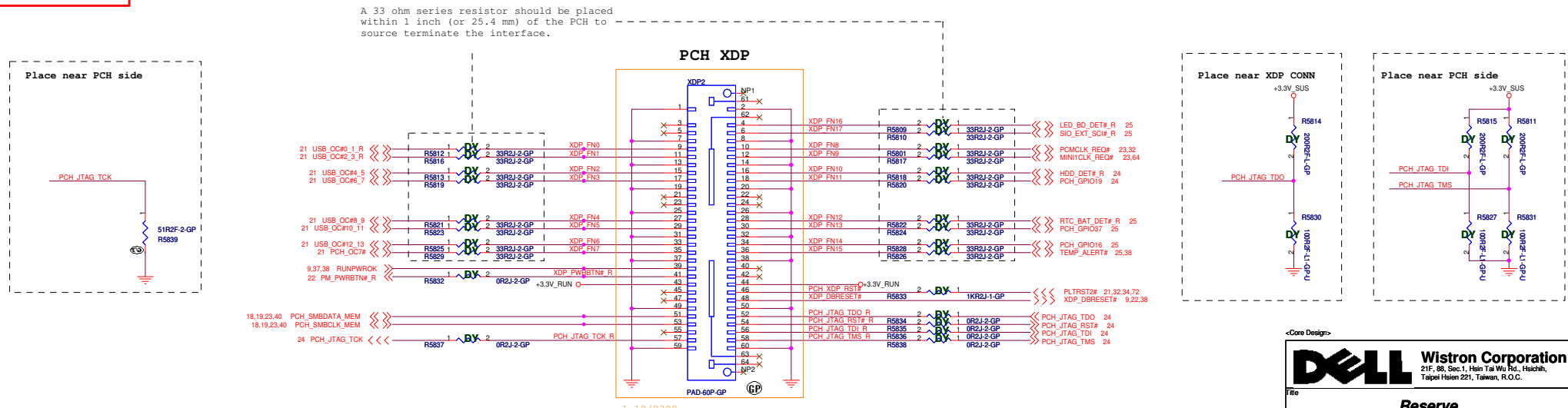
SSID = CPU



SSID = Thermal



SSID = PCH



<Core Design>

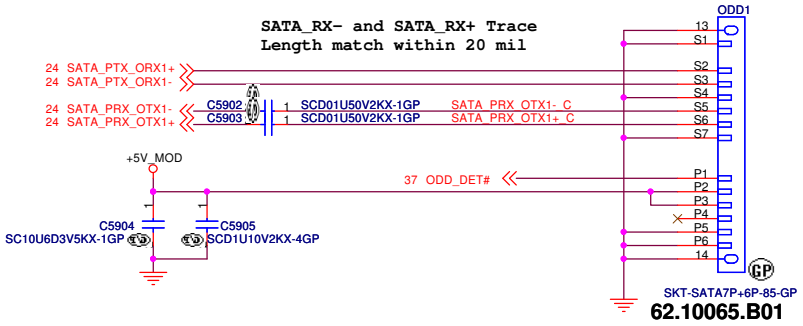
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserve

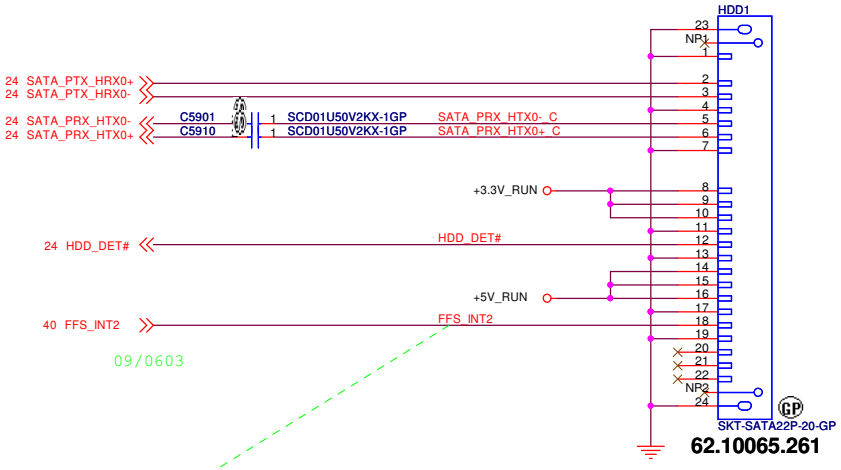
Size	Document Number	Rev
C	Fonseca 14.1" DIS	-1

Date: Thursday, March 18, 2010 Sheet 58 of 89

SSID = SATA SATA ODD Connector



SSID = SATA SATA HDD Connector

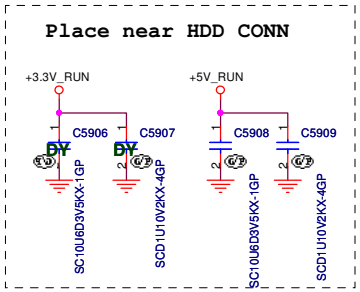


FFS_INT2
#1) It is active High when Free Fall is detected,
allowing Pin.11 to be pulled high.
Pin.11 driven low on power up and then
held low unless free fall.

Main:62.10065.261

2nd:62.10065.511

```
SATA HDD Interface comment
*******************************
--- GND
RX+
RX-
--- GND
TX-
TX+
--- GND
*******************************
------------ 3.3V
------------ 3.3V
------------ 3.3V
--- GND
--- GND / Dell Detected Pin
--- GND
------------ 5V
------------ 5V
------------ 5V
--- GND
Staggered spinup/activity (in supporting drives)
--- GND
------------ 12V
------------ 12V
------------ 12V
*******************************
```



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

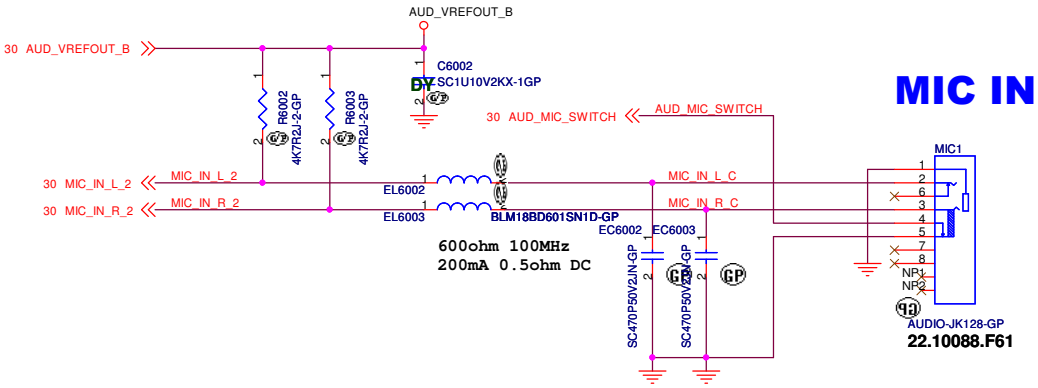
Title: HDD / ODD Connector

Size	Document Number	Rev
A3	Fonseca 14.1" DIS	-1

Date: Thursday, March 18, 2010 Sheet 59 of 89

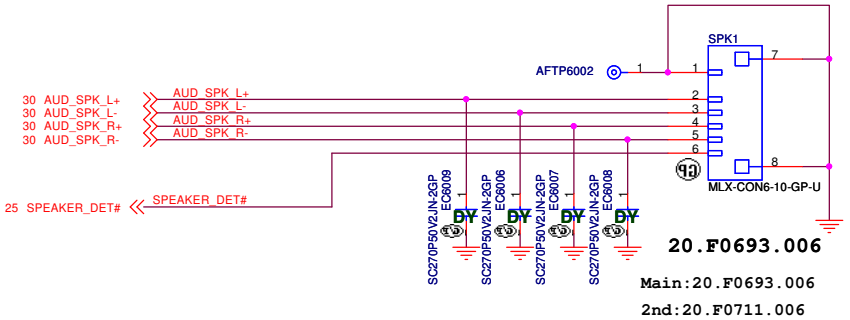
SSID = AUDIO

MIC IN



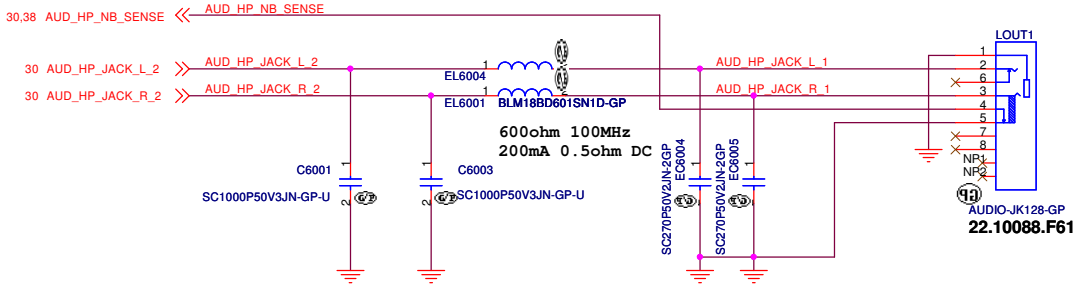
SSID = AUDIO

SPEAKER



SSID = AUDIO

Earphone



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack / Speaker Connector

Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 60 of 89

SSID = LOM

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN

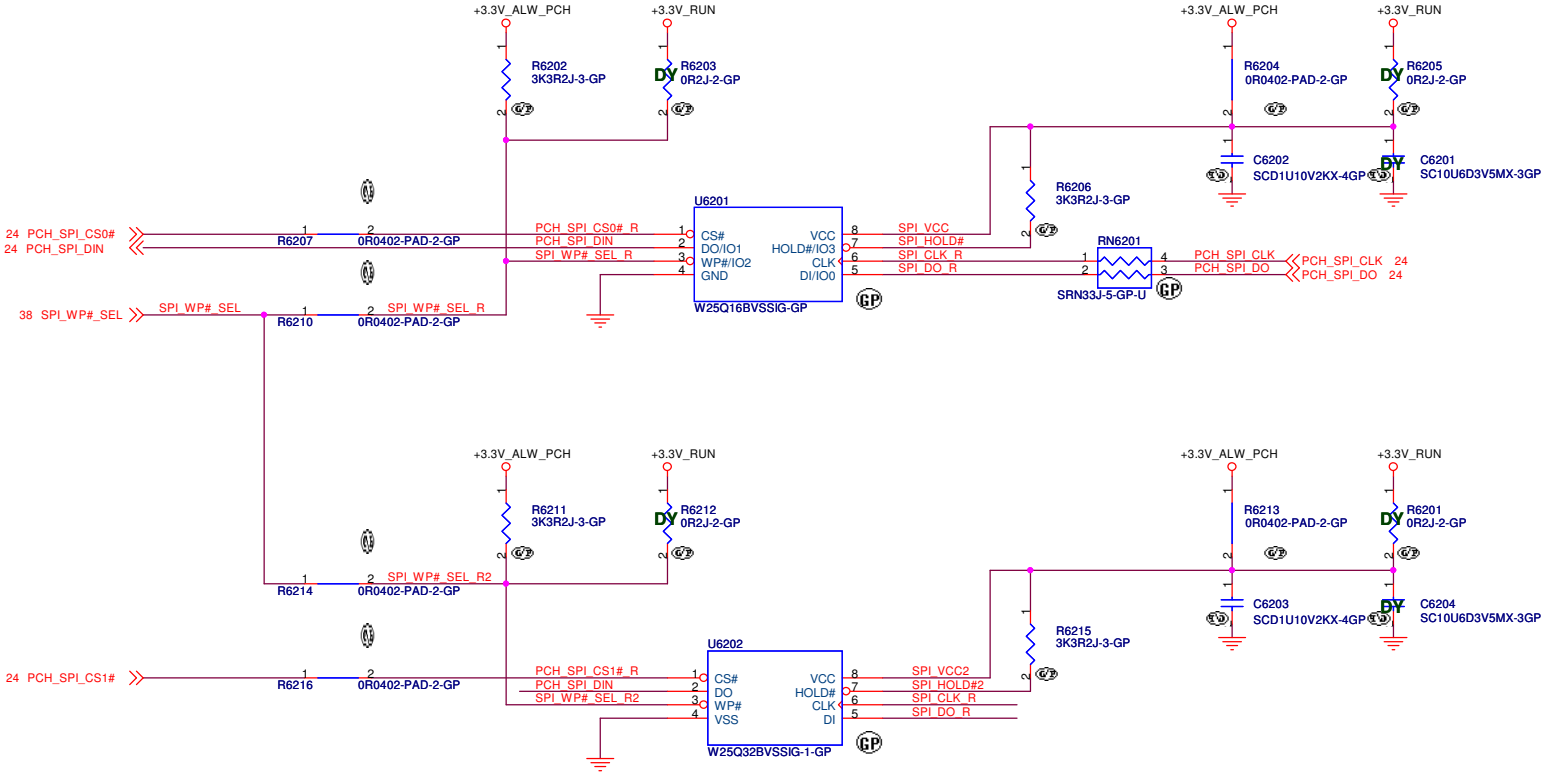
Size: C | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 61 of 89

SSID = Flash.ROM

09/0416, Pin.2
From Intel checklist,
SPI_CS0#/CS1#
No series resistor required
if routing length is 1.5"-6.5"
(with 1 or 2 SPI device)

09/0416, Pin.6
Intel checklist
No series resistor required if routing length is 1.5"-6.5"
(with 1 or 2 SPI device)



-1.10/0305

#1 source: 72.25Q16.001 (2MB, Winbond)
#2 source: 72.25165.B01 (2MB, MXIC)
#3 source: 72.02516.A01 (2MB, Numonyx)

#1 source: 72.25Q32.A01 (4MB, Winbond)
#2 source: 72.25325.A01 (4MB, MXIC)
#3 source: 72.25P32.B01 (4MB, Numonyx)

#1 source: 72.25Q64.001 (8MB, Winbond)
#2 source: 72.25644.001 (8MB, MXIC)

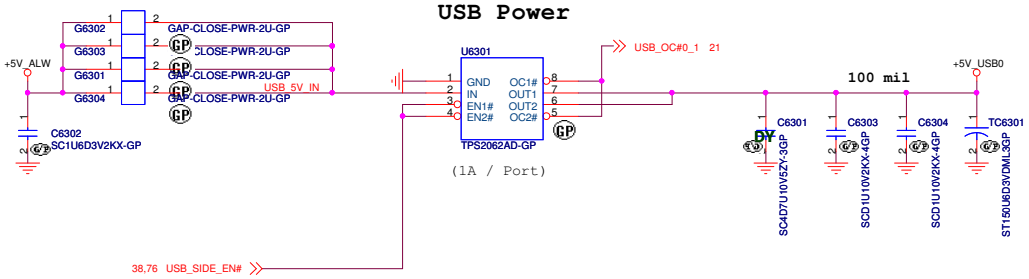
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

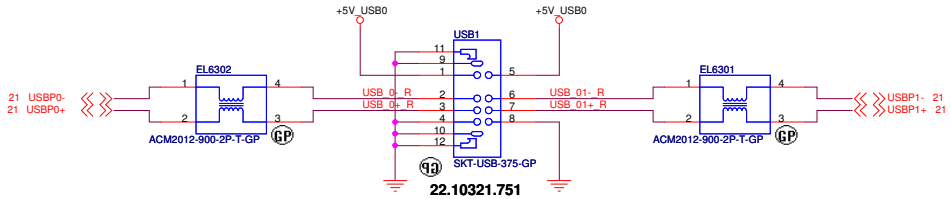
Title: Flash / EEPROM
Size: A3
Document Number: Fonseca 14.1" DIS
Rev: -1
Date: Thursday, March 18, 2010
Sheet 62 of 89

SSID = USB

USB Power



Dual USB Connector

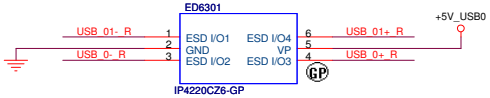


22.10321.751

Main source: 22.10321.751

Second source: 22.10321.F61

S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D



09/0429

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

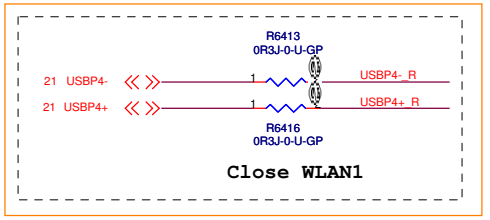
Date: Thursday, March 18, 2010 | Sheet 63 of 89

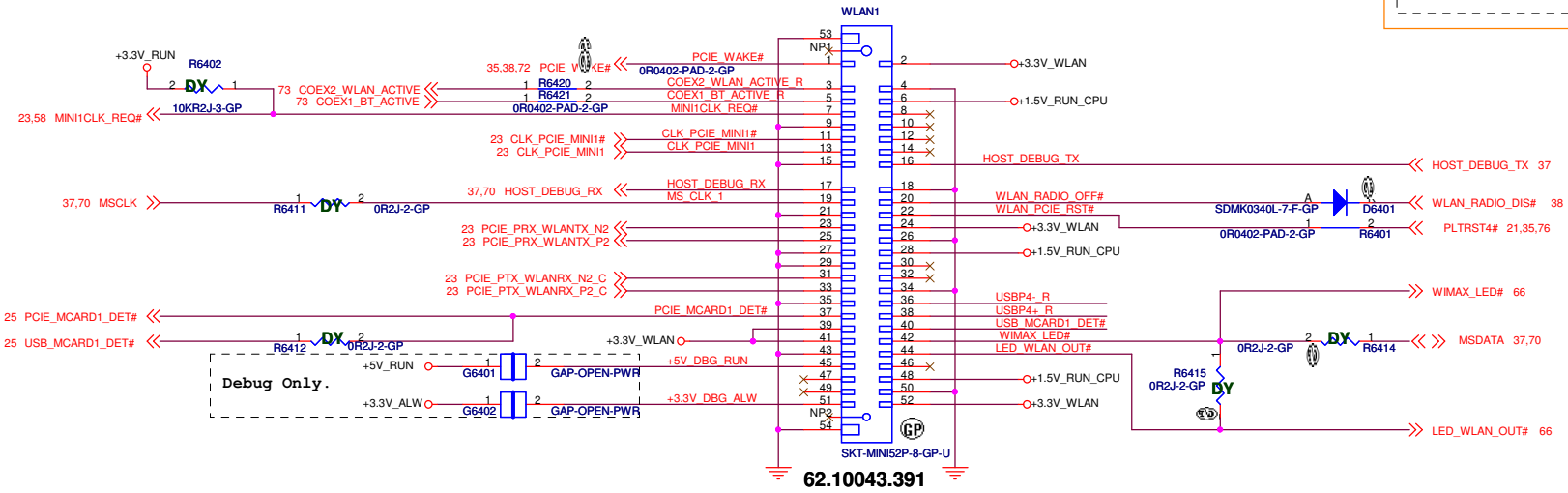
SSID = Wireless

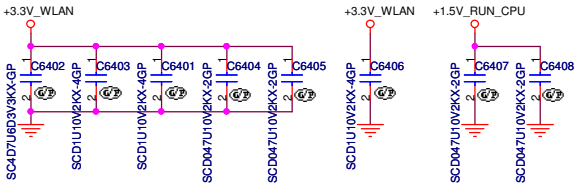
JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

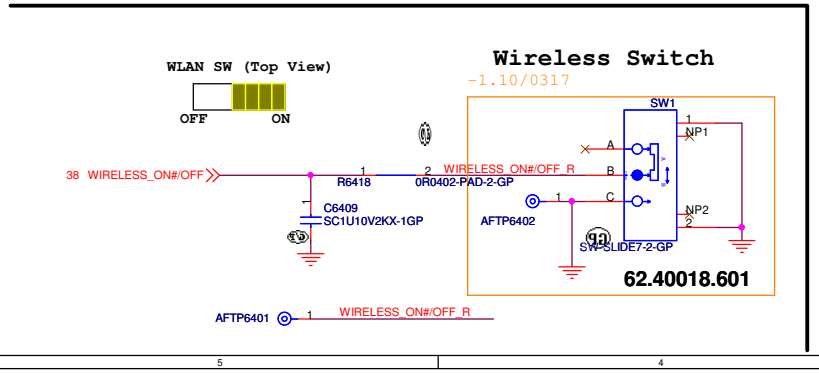
DEBUG PINS

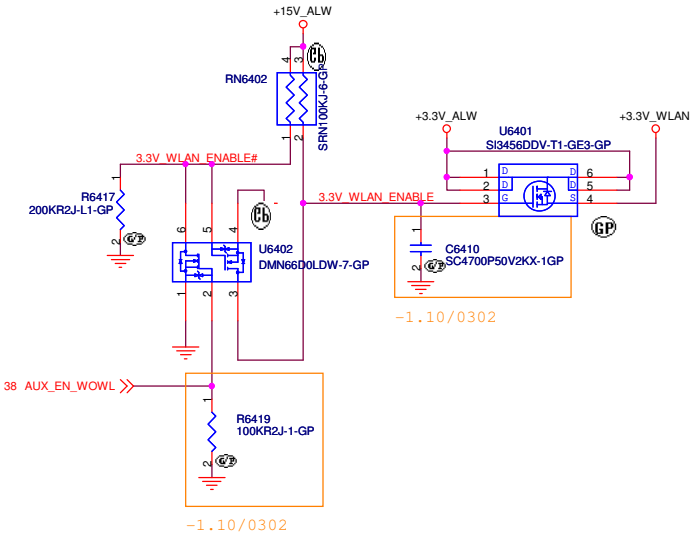
-1.10/0318











<Core Design>

Wistron Corporation
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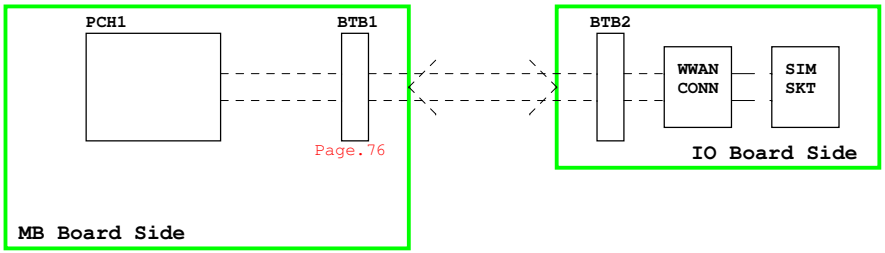
Taipei Hsien 221, Taiwan, R.O.C.

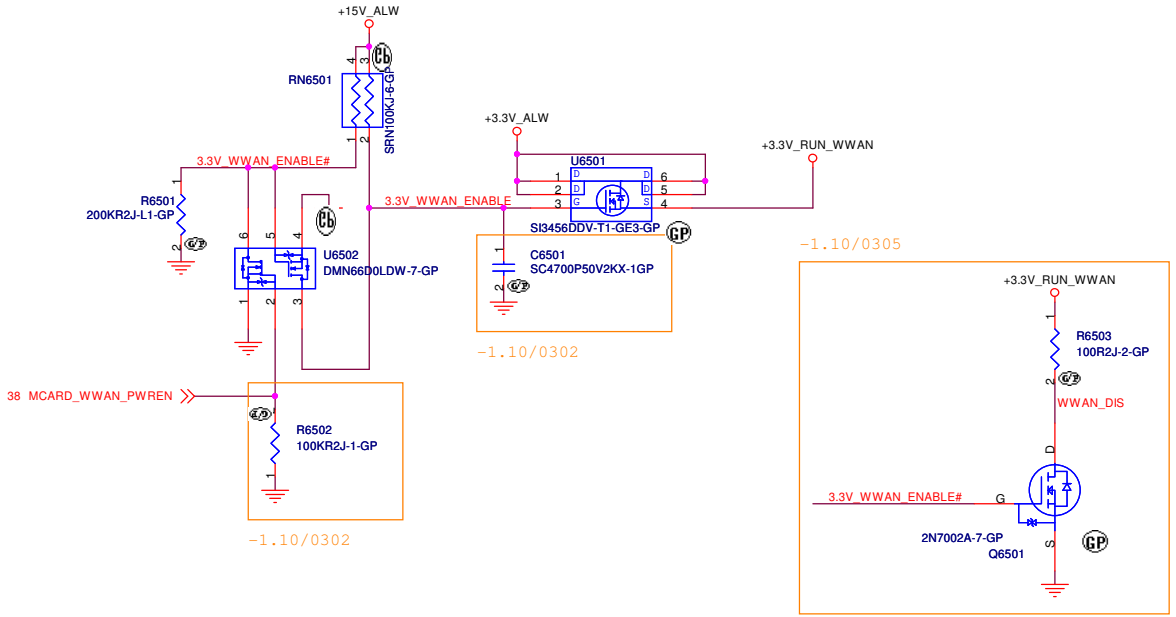
Title: WLAN / Serial Out Connector

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 64 of 89

SSID = Wireless





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	WWAN	
Size A3	Document Number: Fonseca 14.1" DIS	Rev -1
Date: Thursday, March 18, 2010	Sheet 65 of 89	

SSID = User.interface

LED Location from left to right
(MB, Top View)

NUM	CAPS	SCRLK
LED6603	LED6602	LED6601

SCRLK LED

38 SCRL_LED# → R6602 20KR2J-L2-GP → SCRL_LED_R# → Q6602 DDTA143ECA-7-F-GP (+5V_ALW) → SCRLK_LED → R6603 680R2J-3-GP → LED_SCRLK_R → LED6601 LED-B-98-GP

EC6602 SCD1U10V2KX-4GP

CAPS LED

38 CAP_LED# / 38 NUM_LED# → RN6603 SRN20KJ-GP-U → CAP_LED_R# → Q6605 DDTA143ECA-7-F-GP (+5V_ALW) → CAP_LED → R6606 680R2J-3-GP → LED_CAP_R → LED6602 LED-B-98-GP

EC6603 SCD1U10V2KX-4GP

NUM LED

NUM_LED_R# → Q6606 DDTA143ECA-7-F-GP (+5V_ALW) → NUM_LED → R6608 680R2J-3-GP → LED_NUM_R → LED6603 LED-B-98-GP

EC6605 SCD1U10V2KX-4GP

BREATH POWER LED

37,74 BREATH_LED# → Q6603 2N7002A-7-GP (+3.3V_SUS) → BREATH_PWRLED_R# → Q6604 DDTA143ECA-7-F-GP (+5V_ALW) → BREATH_PWRLED_B → R6624 120R2J-2-GP → BREATH_PWRLED_B 76

R6604 330R2J-3-GP → BREATH_PWRLED_P 54

EC6601 SCD1U10V2KX-4GP

HDD LED

24 SATA_ACT#_R → R6609 20KR2J-L2-GP → SATA_ACT_C# → Q6607 DDTA143ECA-7-F-GP (+5V_RUN) → HDD_LED → R6610 1KR2J-1-GP → HDD_LED_B 77

EC6604 SCD1U10V2KX-4GP

WI-MAX LED

+3.3V_WLAN → R6625 100KR2J-1-GP → 64 WIMAX_LED#

WWAN LED

+3.3V_RUN → R6613 100KR2J-1-GP → 76 LED_WWAN_OUT#

D6602 BAT54A-3-GP

WLAN LED

+3.3V_WLAN → R6614 100KR2J-1-GP → D6601 SDMK0340L-7-F-GP → 64 LED_WLAN_OUT#

R6617 → LED_WLAN_OUT_R# → Q6609 DDTA143ECA-7-F-GP (+5V_RUN) → LED_WAN_OUT_R → R6618 1KR2J-1-GP → LED_WLAN_OUT_B 77

EC6608 SCD1U10V2KX-4GP

Bluetooth LED

73 BT_ACTIVE_K# → BT_ACTIVE_K# → R6611 20KR2J-L2-GP → BT_ACT_K_R# → Q6608 DDTA143ECA-7-F-GP (+5V_RUN) → BT_LED_R → R6612 1KR2J-1-GP → BT_LED_B 77

EC6606 SCD1U10V2KX-4GP

Battery LED (Blue)

37 BAT2_LED# / 37 BAT1_LED# → RN6601 SRN10KJ-5-GP → BAT2_LED_R# → Q6610 DDTA143ECA-7-F-GP (+5V_ALW) → BAT2_LED

R6601 1KR2J-1-GP → BAT2_LED_BLUE_B → BAT2_LED_BLUE_B 77

R6620 330R2J-3-GP → BAT2_LED_BLUE_P → BAT2_LED_BLUE_P 54

EC6609 SCD1U10V2KX-4GP

Battery LED (Amber)

BAT1_LED_R# → Q6611 DDTA143ECA-7-F-GP (+5V_ALW) → BAT1_LED → RN6602 SRN1KJ-7-GP → BAT1_LED_AMBER_B → BAT1_LED_AMBER_B 77

BAT1_LED_AMBER_P → BAT1_LED_AMBER_P 54

EC6610 SCD1U10V2KX-4GP

<Core Design>

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Title		
LED		
Size: A3	Document Number: Fonseca 14.1" DIS	Rev: -1
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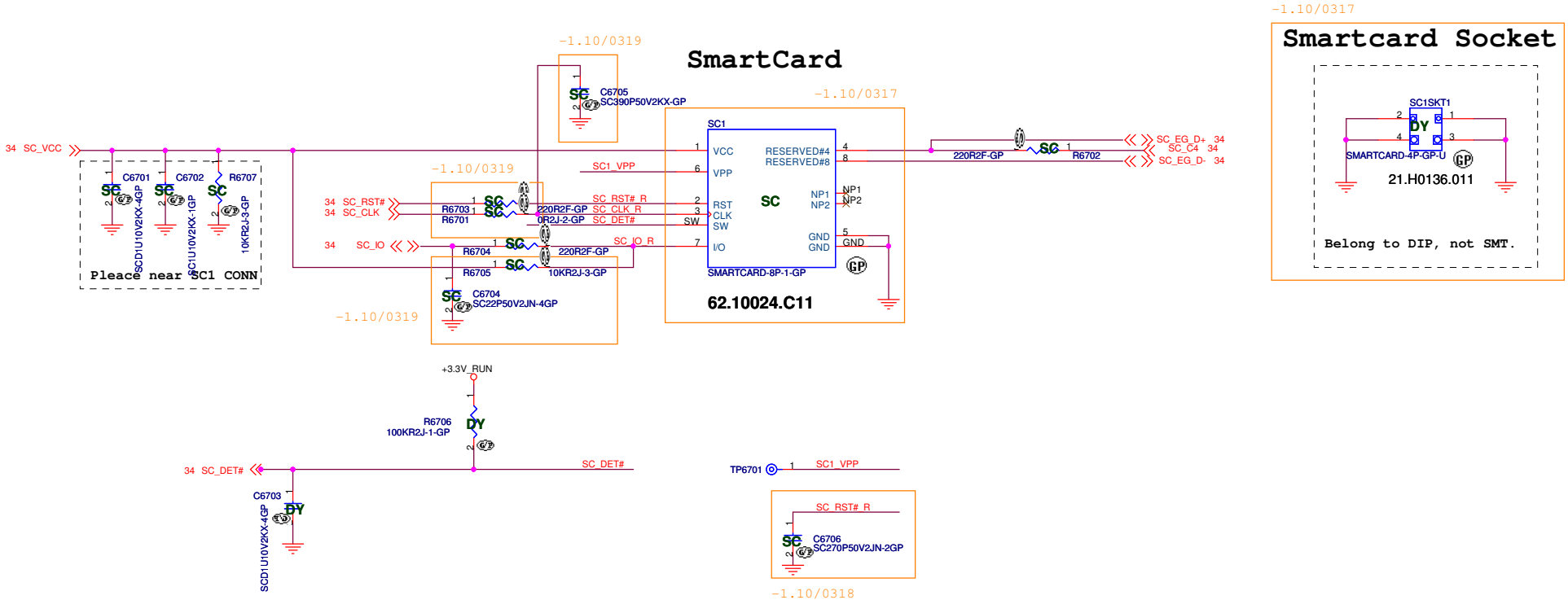
SSID = SmartCard



-1.10/0317

Smartcard Socket

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

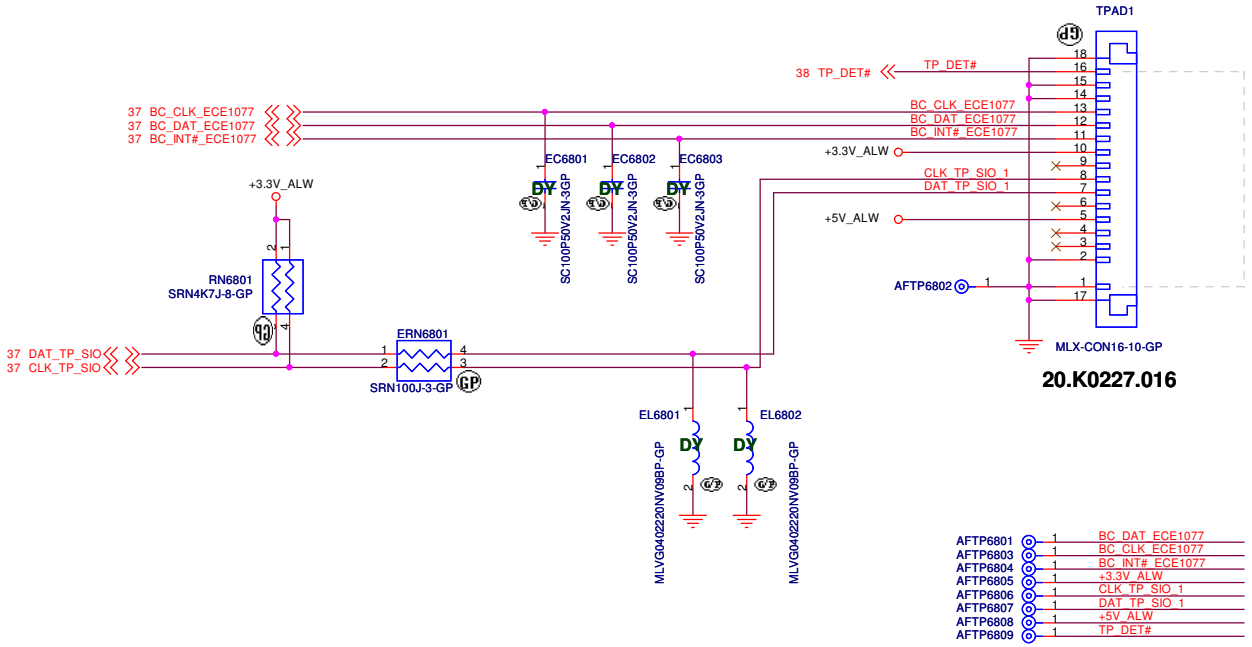
Title: Smart Card Socket

Size	Document Number	Rev
Custom	Fonseca 14.1" DIS	-1

Date: Monday, March 22, 2010 Sheet 67 of 89

SSID = Touch.Pad

TouchPad Connector



Touch PAD Module Side
16 TP_DET#
15 GND
14 GND
13 BC_CLK (ECE1077)
12 BC_DAT (ECE1077)
11 BC_INT# (ECE1077)
10 3.3V_ALW
09 3.3V_RUN (Internal NC)
08 PS2_CLK
07 PS2_DATA
06 5V_RUN (Backlight, No Use)
05 5V_ALW
04 PWM (Backlight, No Use)
03 GND (Backlight, No Use)
02 GND
01 Diag_loop

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

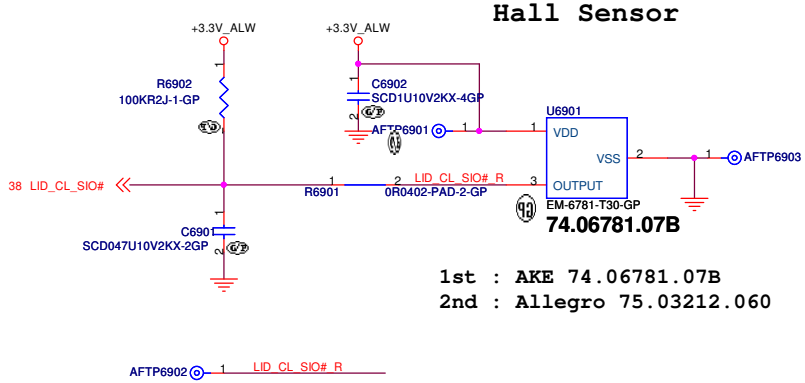
Title: Touch Pad Connector

Size	Document Number	Rev
A3	Fonseca 14.1" DIS	-1

Date: Thursday, March 18, 2010 Sheet 68 of 89

SSID = User.interface

Hall Sensor



1st : AKE 74.06781.07B
2nd : Allegro 75.03212.060

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

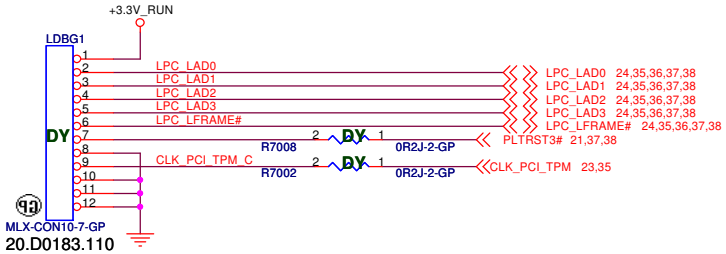
Title: *Hall Sensor*

Size: A3 | Document Number: *Fonseca 14.1" DIS* | Rev: -1

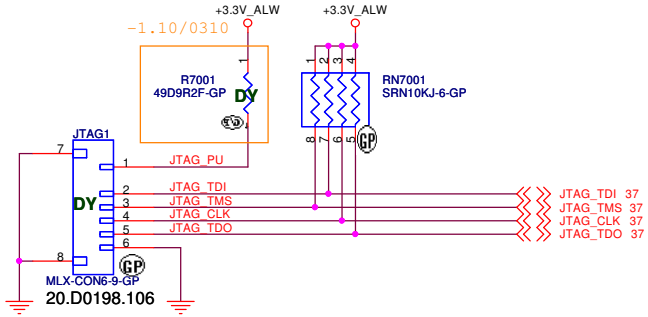
Date: Thursday, March 18, 2010 | Sheet 69 of 89

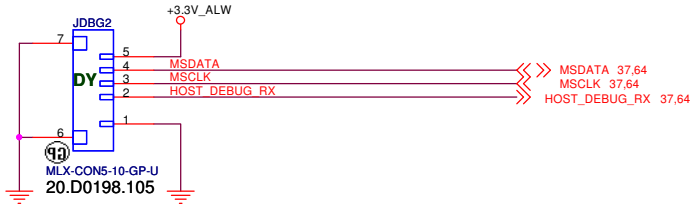
SSID = User.Interface

LPC Debug port



JTAG Debug port





<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: JTAG Debug

Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

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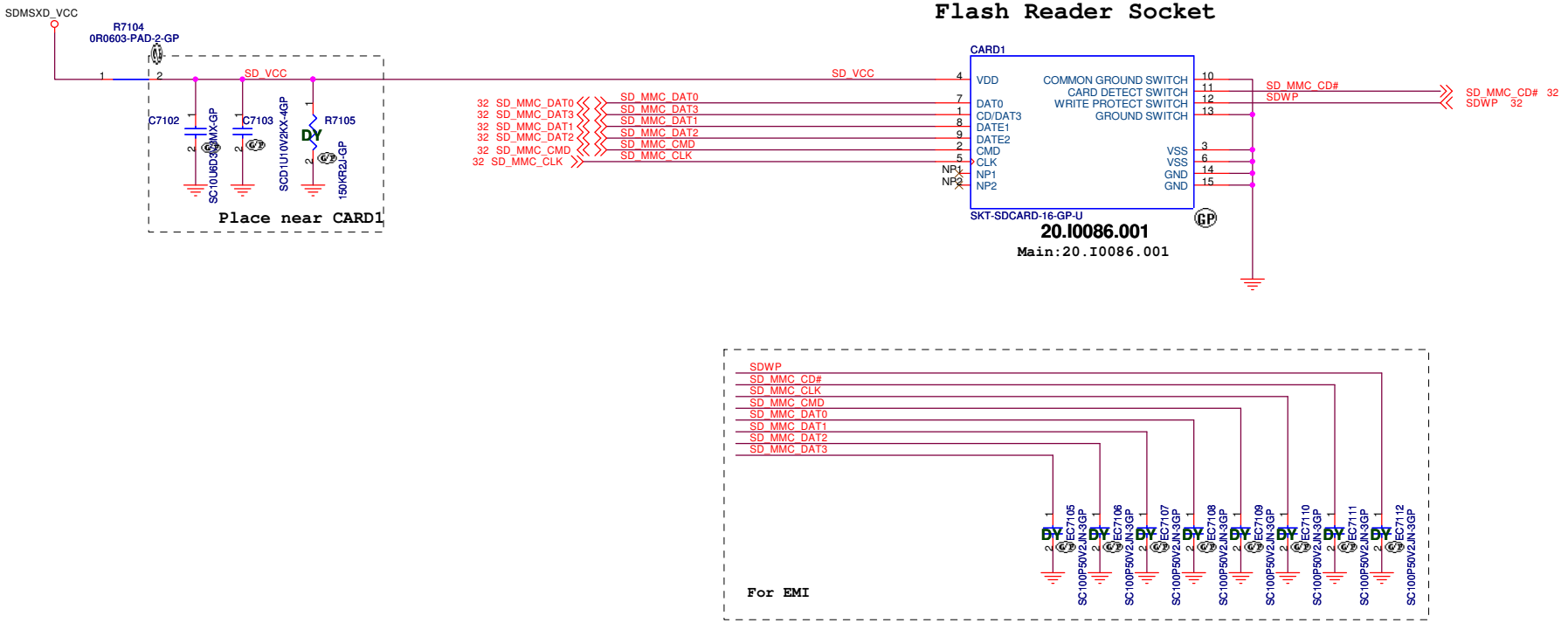
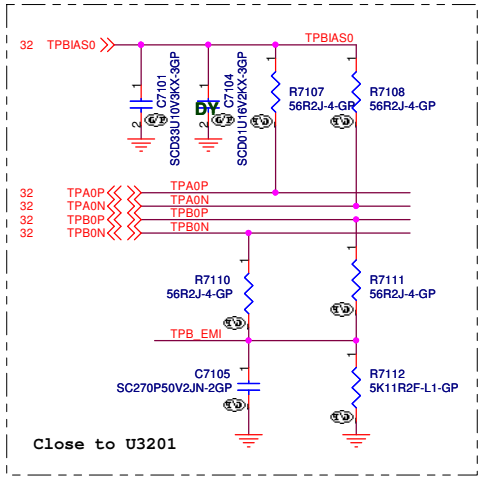
SSID = 1394

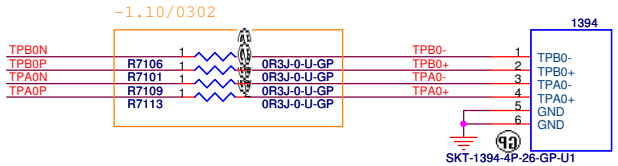


SSID = 1394



Shield GND separately for pairs of
TPA+ & TPA- and TPB+ & TPB-

1394 Connector



<Core Design> 22.10218.T41

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Taipei Hsien 221, Taiwan, R.O.C.

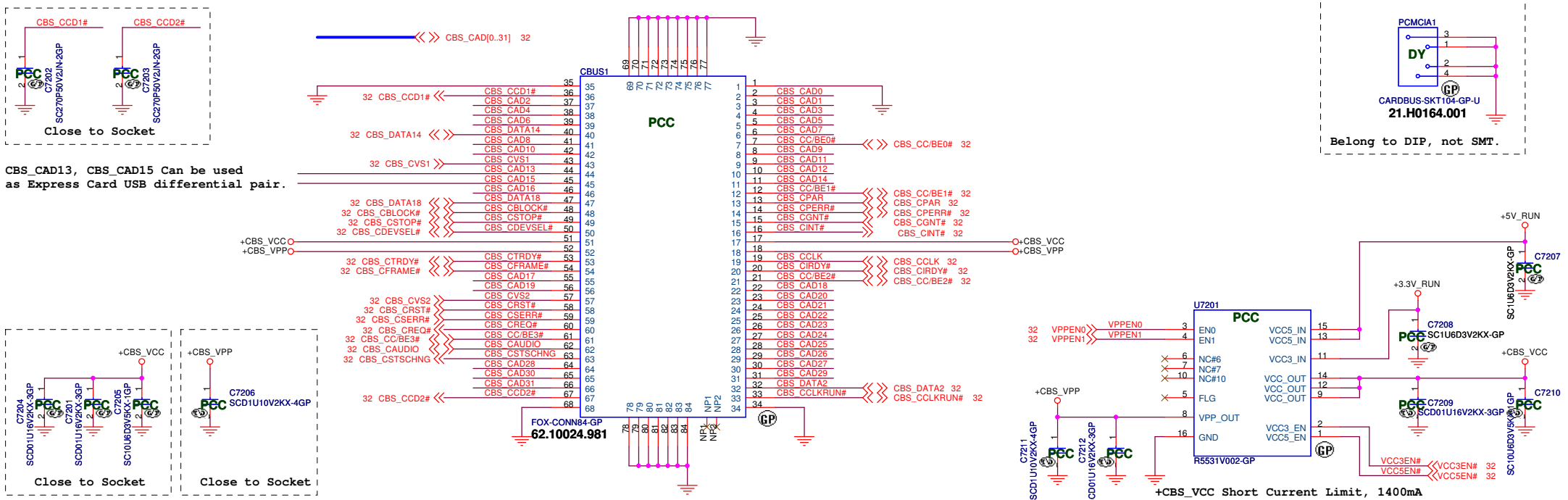
Title: 1394 Connector / Flash Socket

Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 71 of 89

SSID = CARDBUS

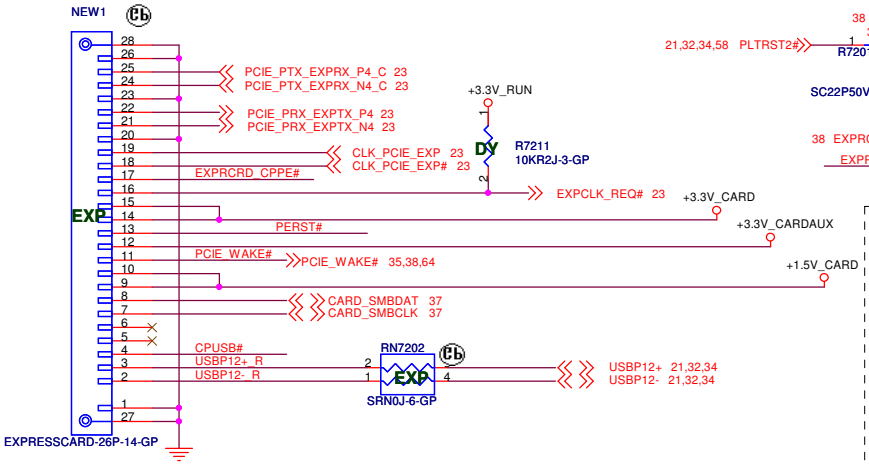
Cardbus Connector



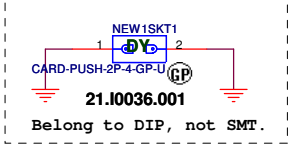
Cardbus Socket

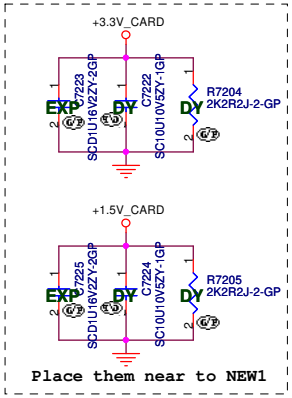
SSID = ExpressCard

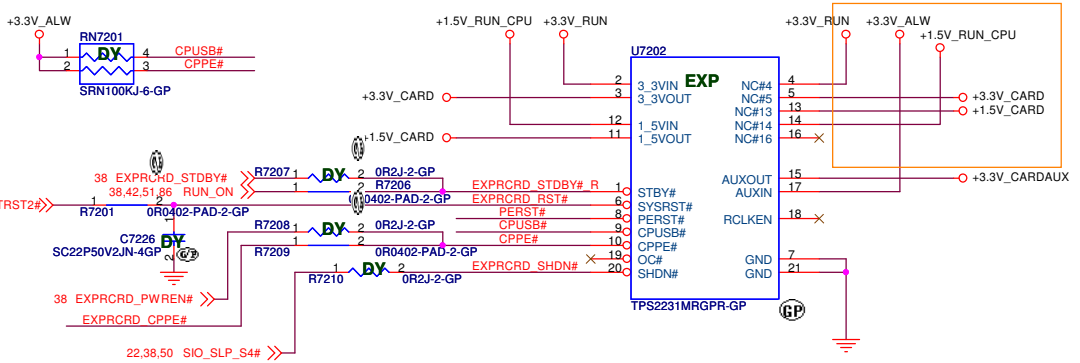
NewCard Connector

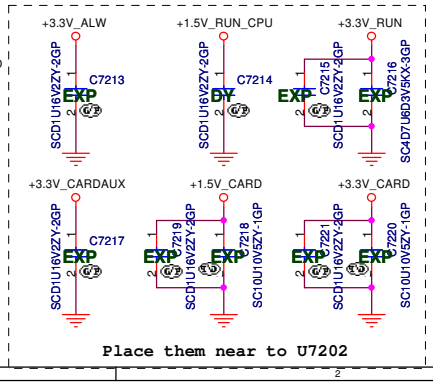


NewCard Socket









+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / ExpressCard

Size	Document Number	Rev
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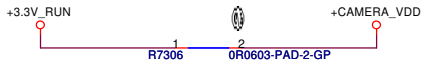
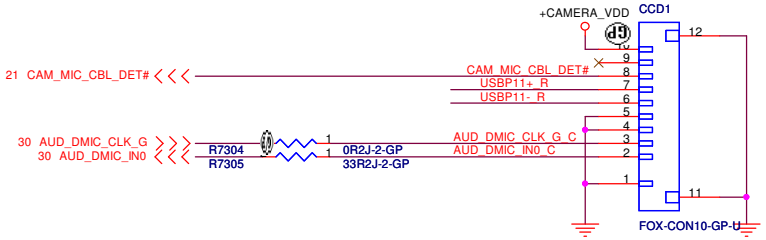
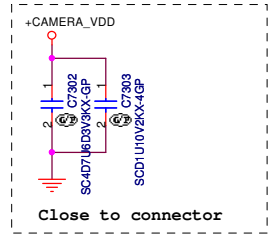
User.interface

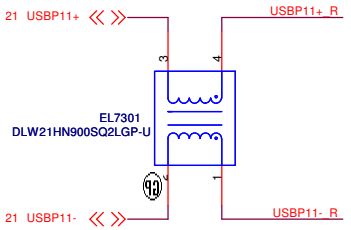
Camera Connector

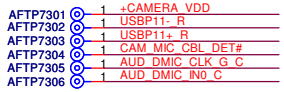




20.F0711.010

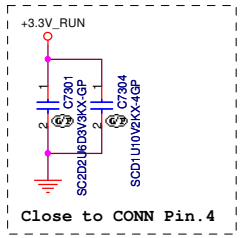


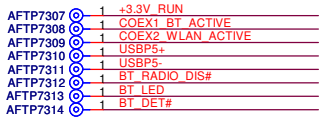


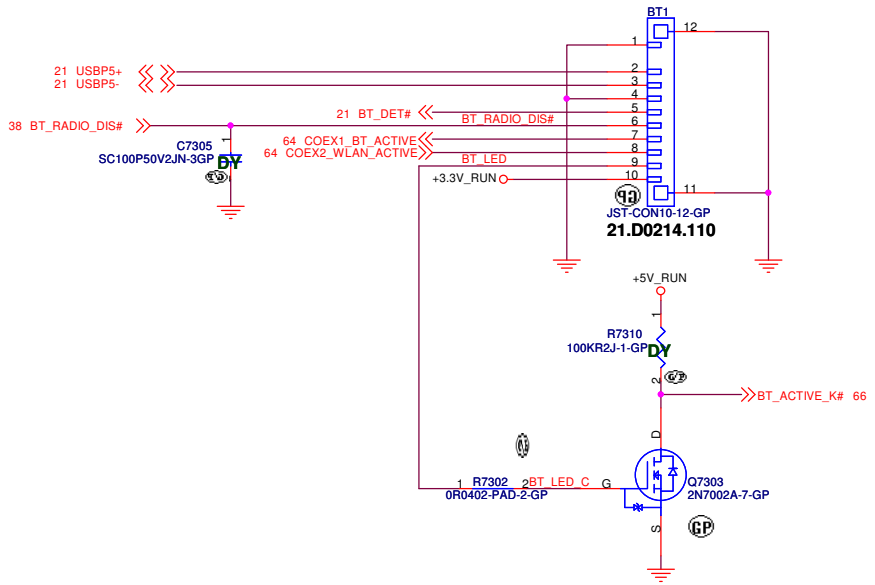


User.interface

Bluetooth Connector







MB BT CONN / BT Module CONN

MB BT CONN PIN	MB BT CONN Define	BT Module CONN PIN	BT Module CONN Define
1	GND	1	GND
2	USBP5+_R	12	USB_DP
3	USBP5-_R	11	USB_DN
4	GND	10	GND
5	BT_DET#	2	MOD_DET
6	BT_RADIO_DIS#	7	RADIO_DIS
7	COEX1_BT_ACTIVE	3	COEX1_BT_ACTIVE
8	COEX2_WLAN_ACTIVE	8	COEX2_WLAN_ACT
9	BT_LED	6	LINK_IND
10	+3.3V_RUN	9	3.3V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth / Camera / DMIC

Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

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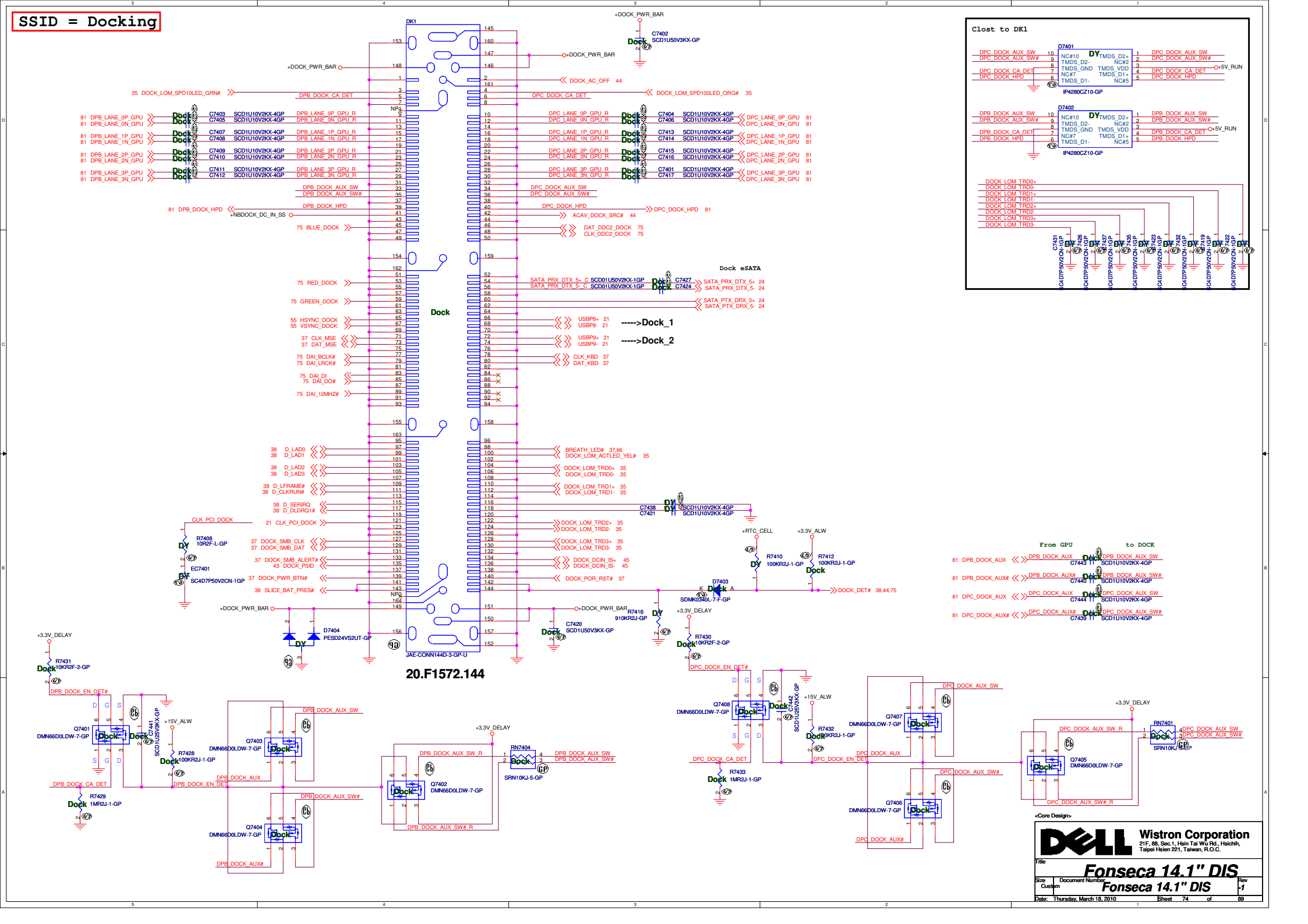
SSID = Docking



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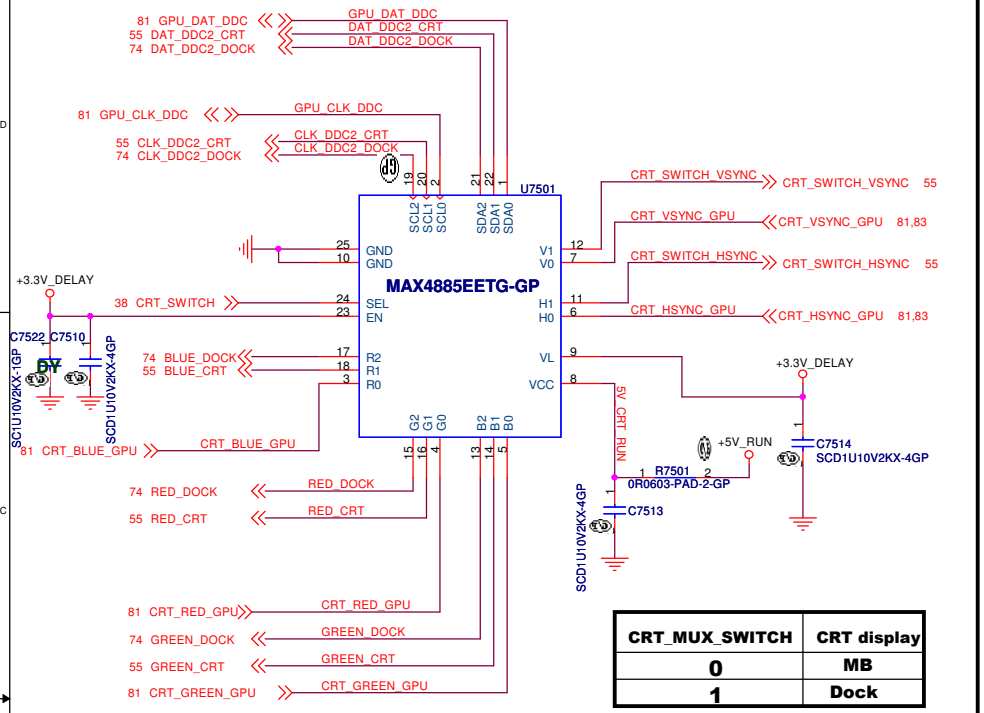
Title: Fonseca 14.1" DIS

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

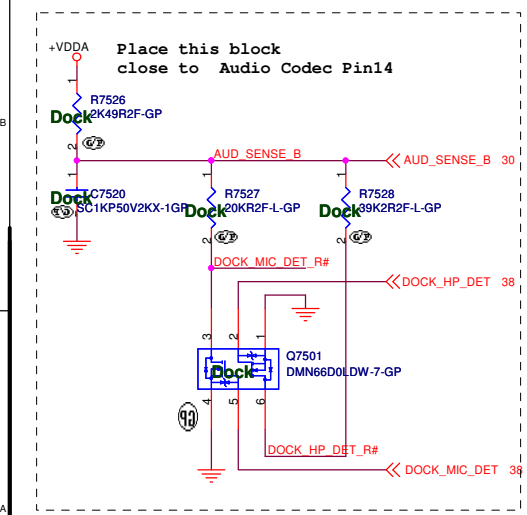
Date: Thursday, March 18, 2010 | Sheet 74 of 89

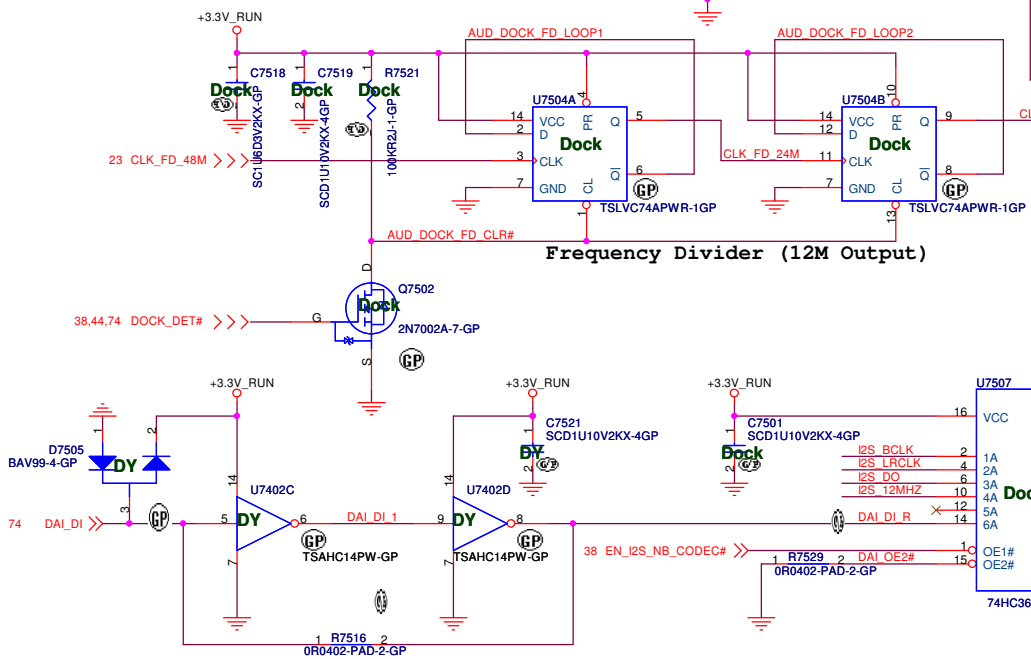
SSID = DOCK CRT SWITCH

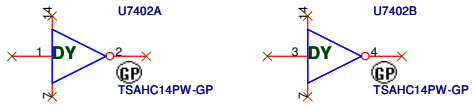


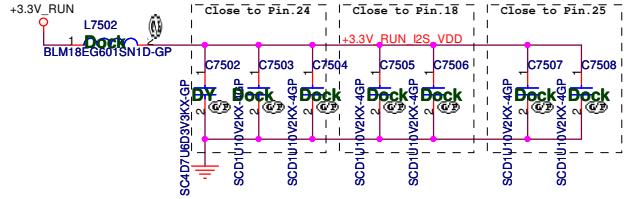
CRT_MUX_SWITCH	CRT display
0	MB
1	Dock

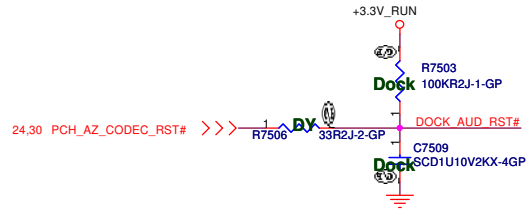
SSID = DOCK AUDIO

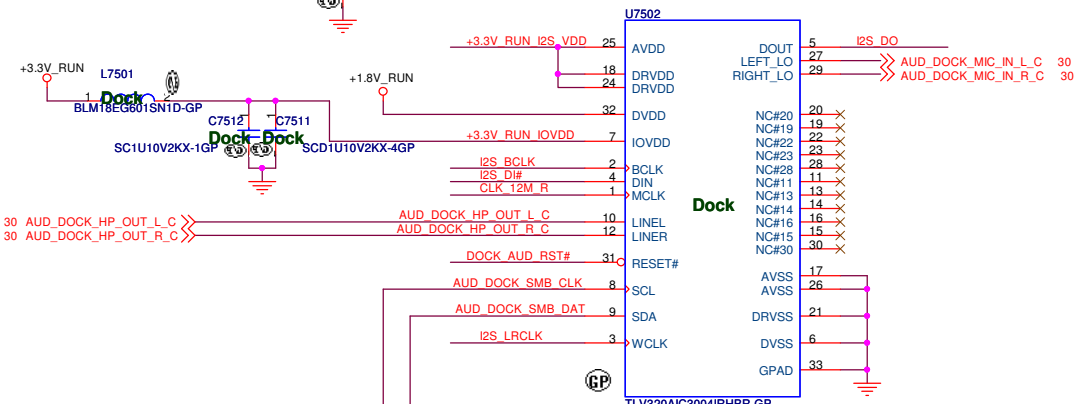


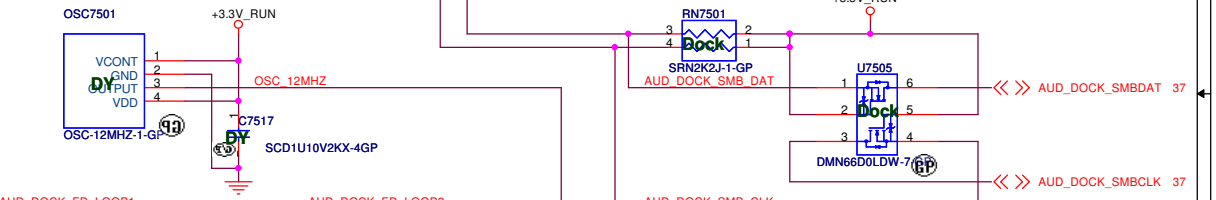












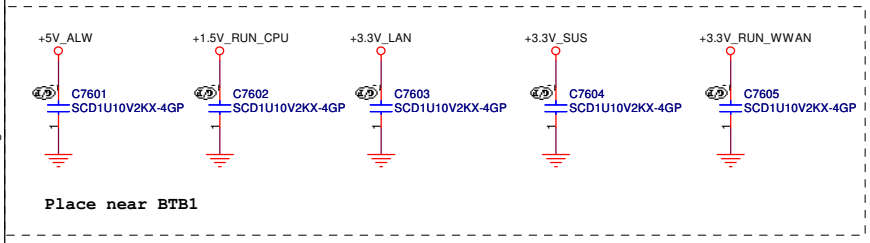
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Docking IC / SW

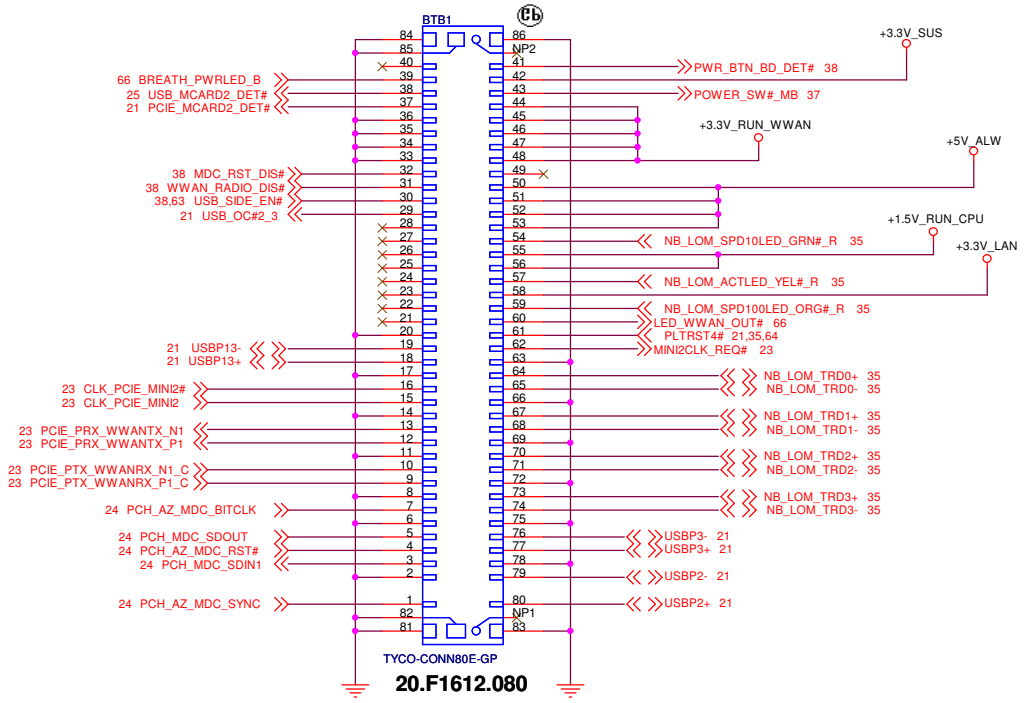
Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 75 of 89

SSID = User.Interface



IO Board Connector



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

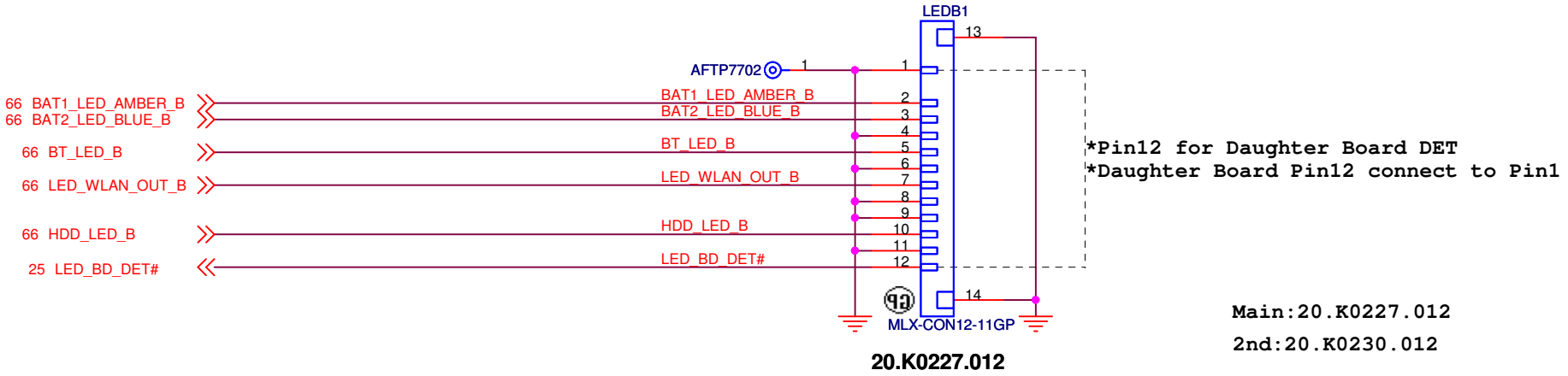
Title: IO Board CONN

Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 76 of 89

SSID = User.interface

LED BD Connector



*Pin12 for Daughter Board DET
*Daughter Board Pin12 connect to Pin1

Main:20.K0227.012
2nd:20.K0230.012

AFTP7701 — BAT1_LED_AMBER_B
AFTP7703 — BAT2_LED_BLUE_B
AFTP7704 — BT_LED_B
AFTP7705 — LED_WLAN_OUT_B
AFTP7706 — HDD_LED_B
AFTP7707 — LED_BD_DET#

LED Location from left to right

HDD	BATTERY	WLAN	BLUE TOOTH

<Core Design>

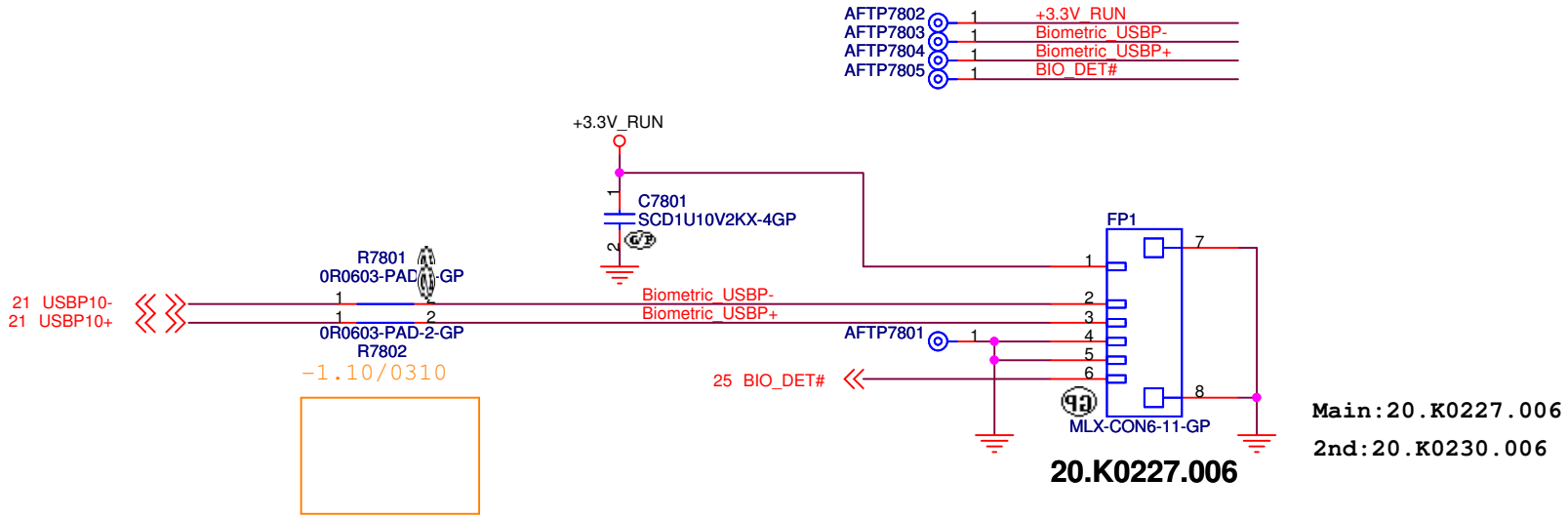
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Board Connector

Size	Document Number	Rev
A4	Fonseca 14.1" DIS	-1

Date: Thursday, March 18, 2010 Sheet 77 of 89

SSID = User.Interface



Biometric Connector

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Finger Printer Board CONN

Size	Document Number	Rev
A4	Fonseca 14.1" DIS	-1

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Hole

H1 HOLE296R166-GP ZZ.00PAD.J11
H2 HOLE296R166-GP ZZ.00PAD.J11
H3 HOLE296R166-GP ZZ.00PAD.J11
H4 HOLE296R166-GP ZZ.00PAD.J11
BOSS1 STF217R128H83-GP 34.4Y702.001

H6 HTE108E10R32-D-55-GP ZZ.00PAD.I51
H7 HTE108E10R32-D-55-GP ZZ.00PAD.I51
H8 HOLE256R126-GP ZZ.00PAD.J01
H9 HOLET256B315R111-GP ZZ.00PAD.M01
H10 HT65B685X925R29-S-GP

H11 HOLE355X355R126-GP ZZ.00PAD.I71
H12 HOLE355X355R126-GP ZZ.00PAD.I71
H13 HOLE355X355R126-GP ZZ.00PAD.I71
H14 HOLE355X355R126-GP ZZ.00PAD.I71
H15 HOLE355X355R126-GP ZZ.00PAD.I71
H16 HOLE355X355R126-GP ZZ.00PAD.I71
H17 HOLE

H27 HOLE

-1.10/0317

H18 HOLE78X42R54X34-S-GP ZZ.00PAD.S31
H19 HOLE78X42R54X34-S-GP ZZ.00PAD.S31
H20 HOLE300X166R111-GP ZZ.00PAD.I61
H21 HOLE300X166R111-GP ZZ.00PAD.I61

H23 HOLE197R99-1-GP ZZ.00PAD.J71
H24 HOLE197R91-GP ZZ.00PAD.I81
H25 HOLE197R91-GP ZZ.00PAD.I81

H22 HT65X75B62X56R28-2P-S-GP ZZ.00PAD.M51
H26 HTE54B5R28-D-42-GP ZZ.00PAD.M61

SSID = Mechanical

SPRING

SPR1 SPRING-51-GP 34.4F822.002
SPR2 SPRING-51-GP 34.4F822.002
SPR3 SPRING-51-GP 34.4F822.002
SPR4 SPRING-24-GP-U 34.45T31.001
SPR5 SPRING-24-GP-U 34.45T31.001
SPR6 SPRING-24-GP-U 34.45T31.001
SPR7 SPRING-24-GP-U 34.45T31.001

EMI CAPS

+DC_IN EC7906 SCD1U50V3KX-GP
+PWR_SRC EC7907 SCD1U50V3KX-GP
+PWR_SRC EC7908 SCD1U50V3KX-GP
+COIN_CELL EC7909 SCD1U10V2KX-4GP
+PWR_SRC EC7910 SCD1U50V3KX-GP
+PWR_SRC EC7911 SCD1U50V3KX-GP

RF

+VCC_GFX_CORE EC7904 SC33P50V2JN-3GP
+1.5V_RUN EC7905 SC33P50V2JN-3GP
+1.5V_RUN EC7901 SC33P50V2JN-3GP
+1.5V_RUN EC7902 SC33P50V2JN-3GP
+1.5V_RUN EC7903 SC33P50V2JN-3GP
+PWR_SRC EC7917 SCD1U50V3KX-GP
+PWR_SRC EC7918 SCD1U50V3KX-GP
+1.5V_SUS EC7919 SCD1U50V3KX-GP
+1.5V_SUS EC7920 SCD1U50V3KX-GP
+1.5V_SUS EC7921 SCD1U50V3KX-GP
+5V_ALW EC7912 SC33P50V2JN-3GP
+5V_ALW EC7913 SC33P50V2JN-3GP
+5V_ALW EC7914 SC33P50V2JN-3GP
+5V_ALW EC7915 SC33P50V2JN-3GP
+5V_ALW EC7916 SC33P50V2JN-3GP
+PWR_SRC_GFX_CORE EC7923 SCD1U50V3KX-GP
+1.05V_VTT_PWR_SRC EC7922 SCD1U50V3KX-GP
+1.5V_RUN EC7927 SC33P50V2JN-3GP
+1.5V_RUN EC7924 SC33P50V2JN-3GP
+1.5V_RUN EC7925 SC33P50V2JN-3GP

Unused

+3.3V_RUN U7402E TSAHC14PW-GP
+3.3V_RUN U7402F TSAHC14PW-GP
+5V_CRT_RUN U5501C SSAHCT125PWR-GP
+5V_CRT_RUN U5501D SSAHCT125PWR-GP

<Core Design>

Wistron Corporation
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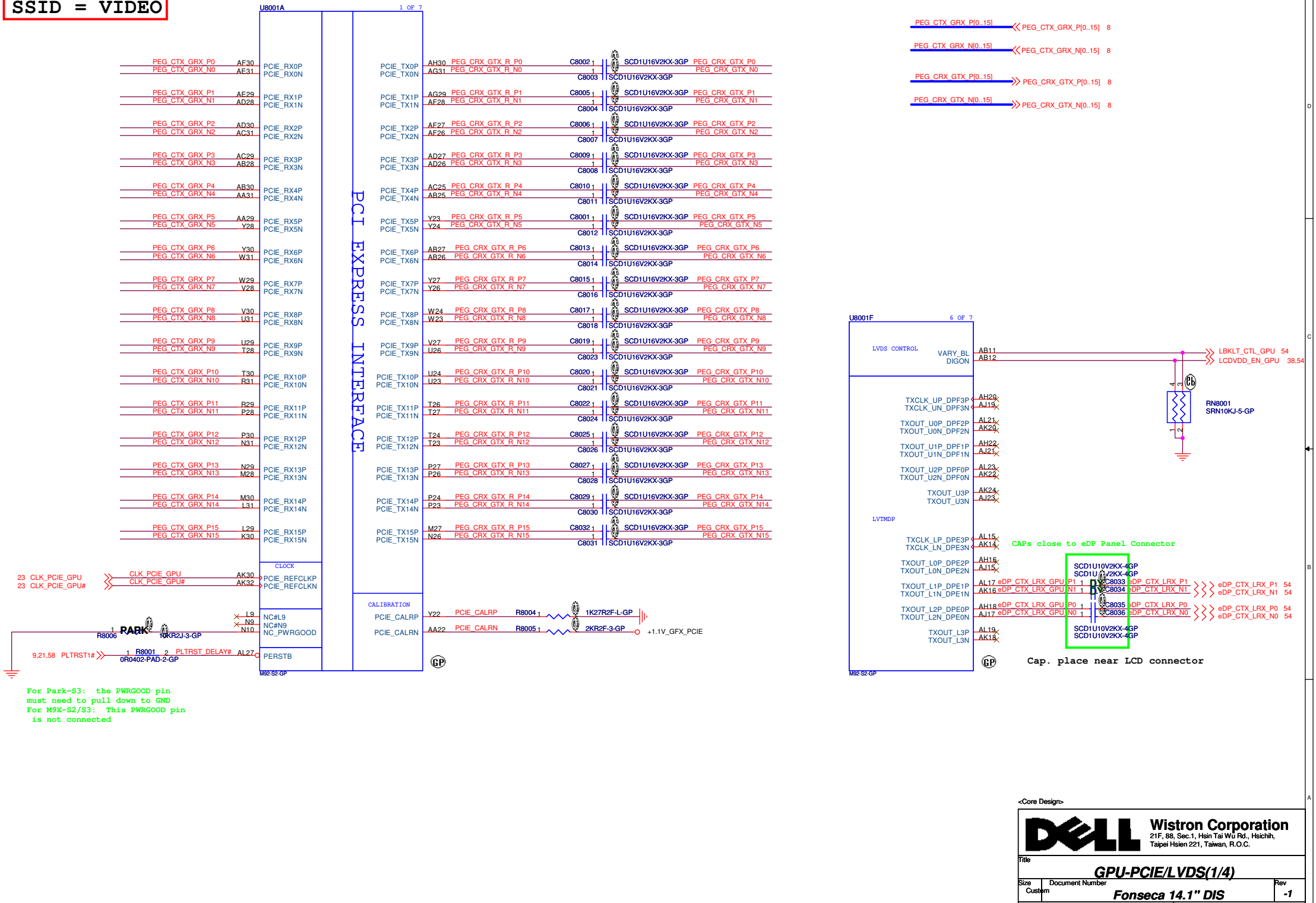
Taipei Hsien 221, Taiwan, R.O.C.

Title: Unused Parts / EMI RF Cap.
Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1
Date: Thursday, March 18, 2010 | Sheet 79 of 89

SSID = VIDEO



For Park-S3: the PWRGOOD pin must need to pull down to GND
For M9X-S2/S3: This PWRGOOD pin is not connected

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-PCIE/LVDS(1/4)

Size: Custom | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 80 of 89

SSID = VIDEO

M92/ PARK switch

M92/ PARK switch

M92/ PARK switch

M92/ PARK switch

<Core Design>

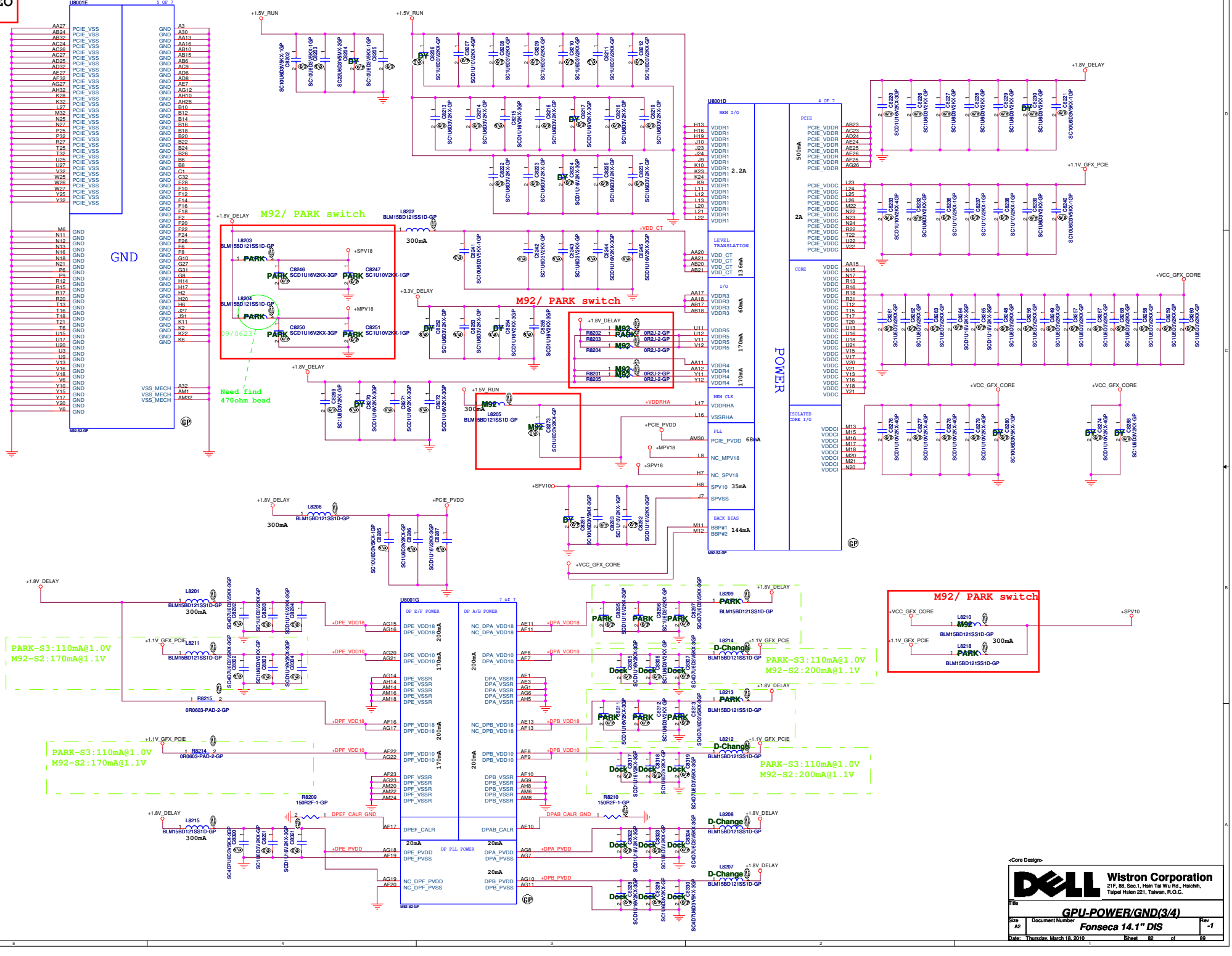
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-TV/CRT/DP PORT (2/4)

Size	Document Number	Rev
C	Fonseca 14.1" DIS	-1

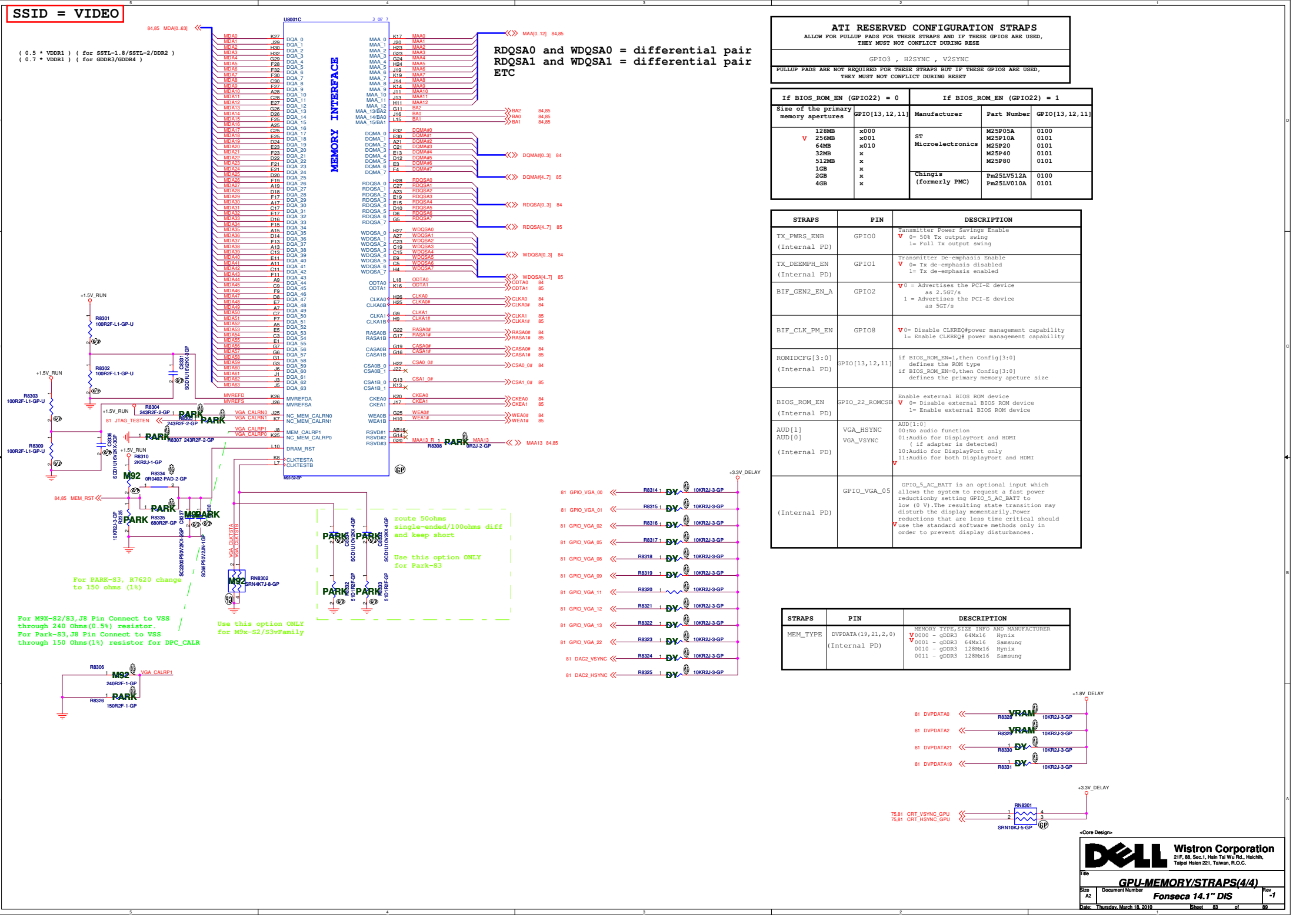
Date: Thursday, March 18, 2010 Sheet 81 of 89

SSID = VIDEO


U8001E
5 OF 7
GND
M92/ PARK switch
M92/ PARK switch
09/0623
Need find
470ohm bead
U8001D
4 OF 7
POWER
U8001G
7 OF 7
PARK-S3:110mA@1.0V
M92-S2:170mA@1.1V
PARK-S3:110mA@1.0V
M92-S2:200mA@1.1V
M92/ PARK switch
PARK-S3:110mA@1.0V
M92-S2:170mA@1.1V
PARK-S3:110mA@1.0V
M92-S2:200mA@1.1V
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GPU-POWER/GND(3/4)
Fonseca 14.1" DIS
Rev -1
Thursday, March 18, 2010
Sheet 82 of 89

SSID = VIDEO

(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)



ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO3 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
V 256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x			
2GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
4GB	x		Pm25LV010A	0101

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Tansmitter Power Savings Enable V 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable V 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	V 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	V 0= Disable CLKREQ#power management capability 1= Enable CLKREQ# power management capability
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI V
(Internal PD)	GPIO_VGA_05	GPIO_5_AC_BATT is an optional input which allows the system to request a fast power reductionby setting GPIO_5_AC_BATT to low (0 V).The resulting state transition may disturb the display momentarily.Power reductions that are less time critical should V use the standard software methods only in order to prevent display disturbances.

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(19,21,2,0) (Internal PD)	MEMORY TYPE,SIZE INFO AND MANUFACTURER V 0000 - gDDR3 64Mx16 Hynix V 0001 - gDDR3 64Mx16 Samsung 0010 - gDDR3 128Mx16 Hynix 0011 - gDDR3 128Mx16 Samsung

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Title: GPU-MEMORY/STRAPS(4/4)

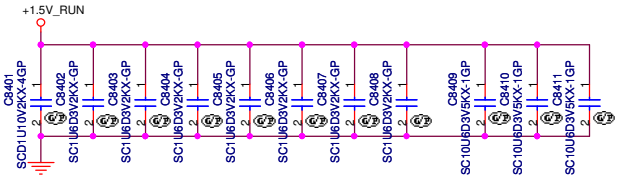
Size: A2 | Document Number: Fonseca 14.1" DIS | Rev: -1

Date: Thursday, March 18, 2010 | Sheet 83 of 89

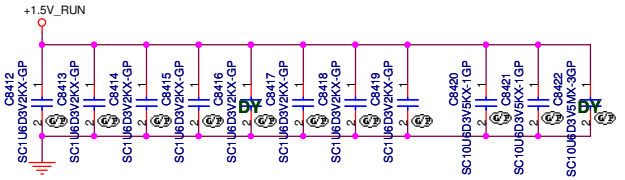
SSID = VIDEO

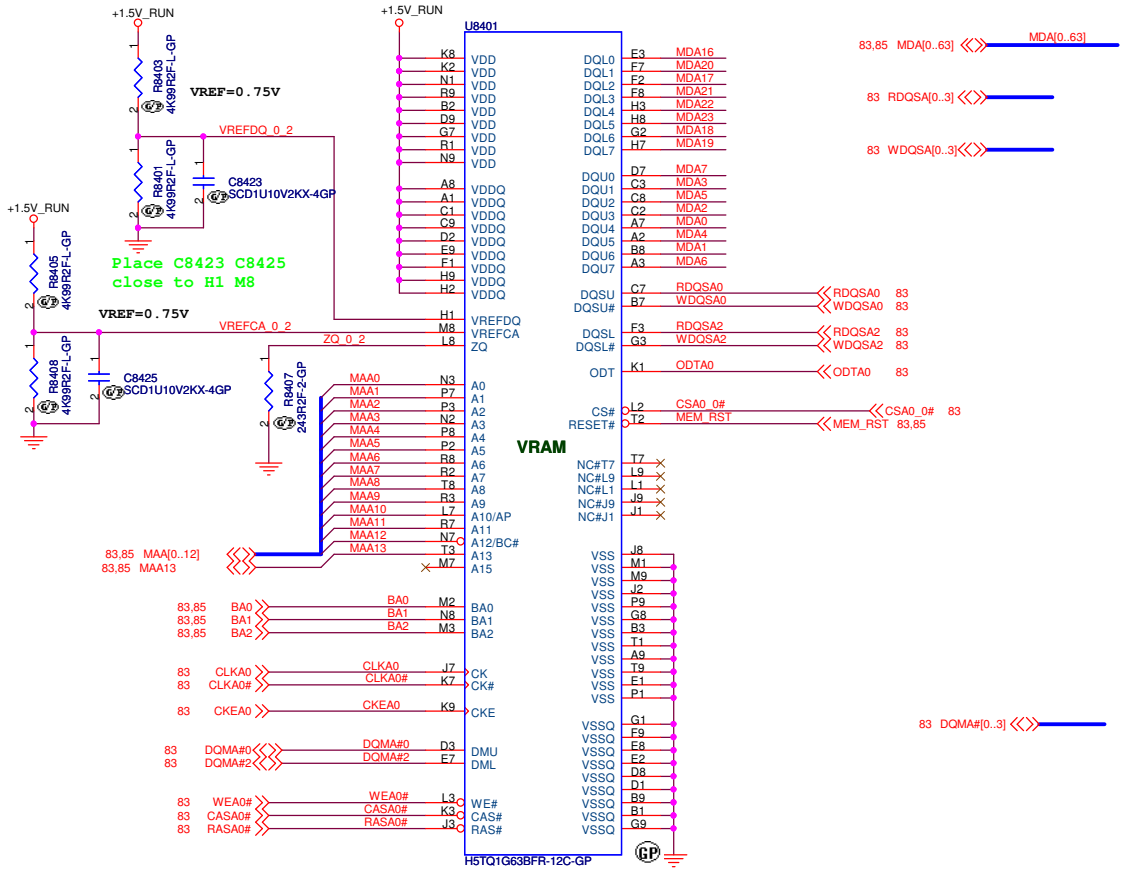
DIVIDER RESISTORS	DDR2/3	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

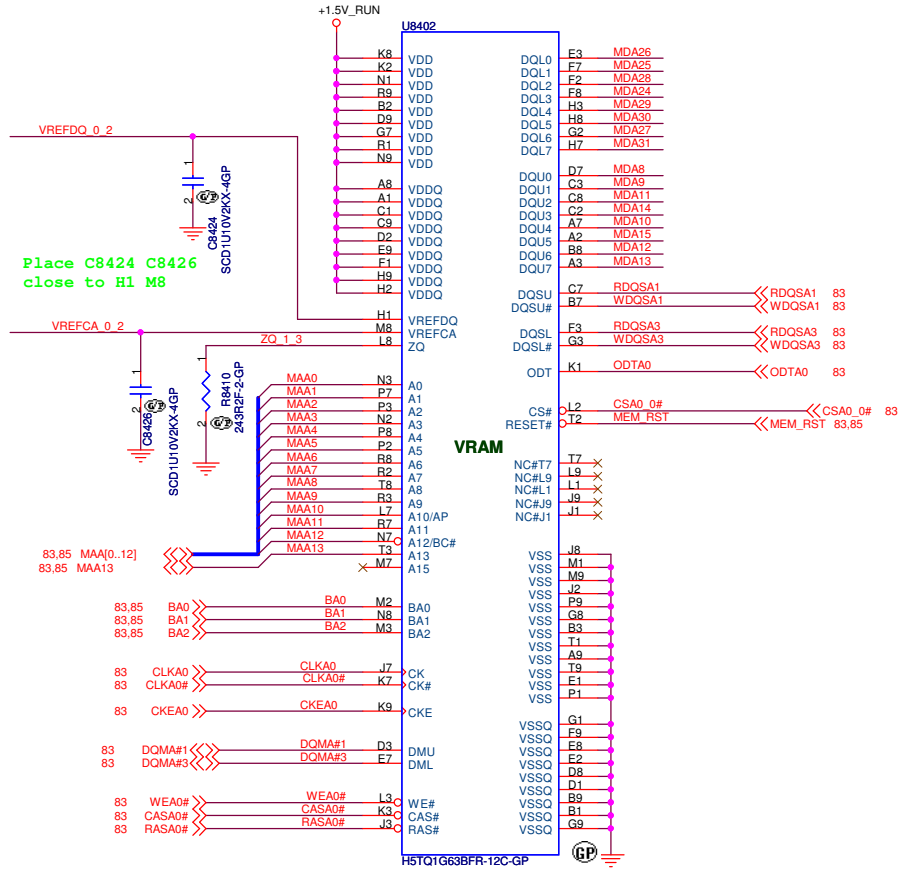
Place blow decouping caps close VDD pin.

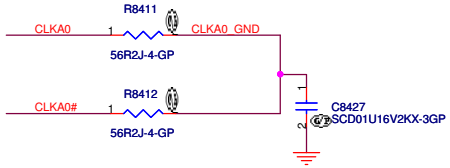


Place blow decouping caps close VDD pin.









<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

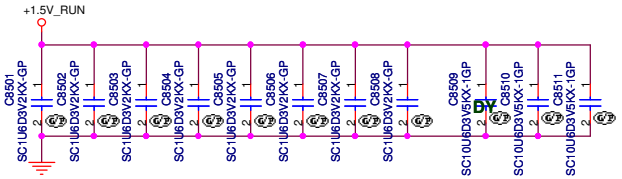
Title: VRAM (1/2)

Size	Document Number	Rev
Custom	Fonseca 14.1" DIS	-1

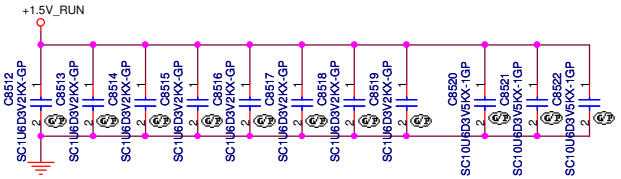
Date: Thursday, March 18, 2010 Sheet 84 of 89

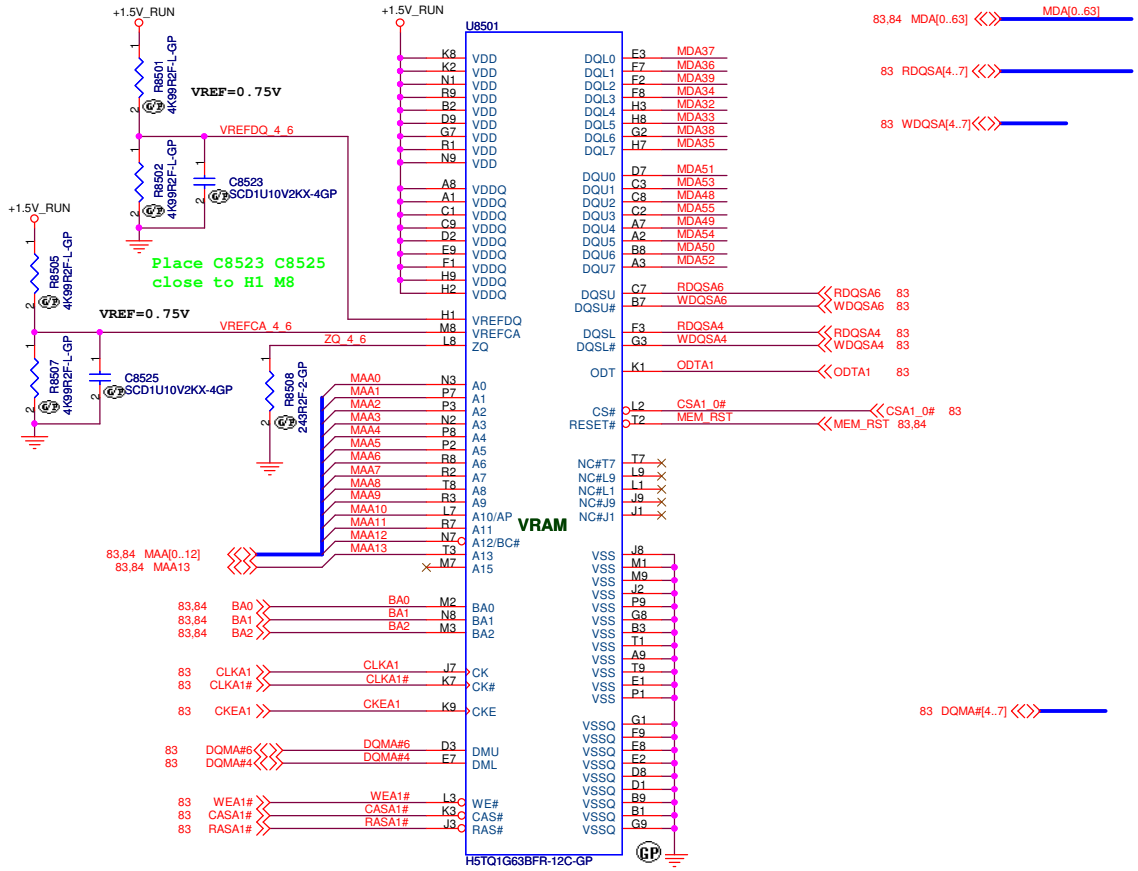
SSID = VIDEO

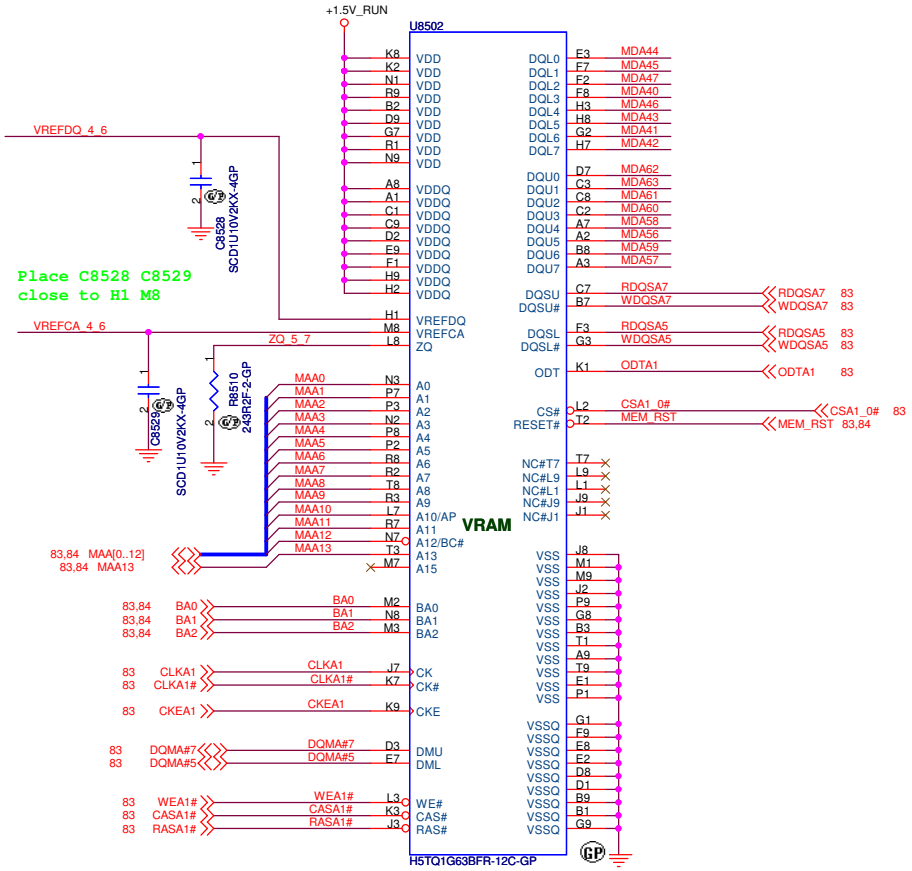
Place blow decouping caps close VDD pin.

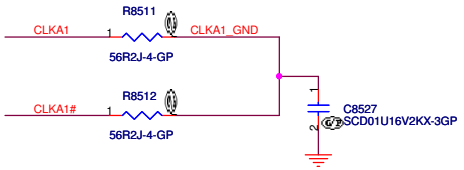


Place blow decouping caps close VDD pin.









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM (2/2)

Size	Document Number	Rev
Custom	Fonseca 14.1" DIS	-1

Date: Thursday, March 18, 2010 Sheet 85 of 89

SSID = PWR.Plane.Regulator_GFX

+1.1V_RUN
Design current = 1.7A
peak current = 2.5A

-1.10/0302

VOUT = 0.5 *(1+Rtop/Rbot)

Design Current = 7.5A
11.8<OCP<13.9A

Vout=0.75V*(R1+R2)/R2

Power team check

PWRCNTL_0=GPIO15
PWRCNTL_1=GPIO20

VID1 GPIO20	VID0 GPIO15	Voltage
x	1	0.9V
x	0	0.95V

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Fonseca
Size: A3 | Document Number: Fonseca 14.1" DIS | Rev: -1
Date: Thursday, March 18, 2010 | Sheet 86 of 89

(Blank)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Fonseca 14.1" DIS*

Size: Custom | Document Number: *DC to DC 1.5V/1.1V* | Rev: *-1*

Date: Thursday, March 18, 2010 | Sheet 87 of 89

VERSION	DATE	NO	PAGE	Modified List	Issue Description	OWNER
-1	02/24	1	54	Delete FUSE5401, C5407, C5408. Add C5410, C5411, C5412, U5402, R5427, R5426, Q5405.		EE
	03/01	2	37,54	Rename net "EC_GPIO060" into "EN_INVPWR". Delete TP3702. Add R3741, 63.10434.1DL.	To solve panel white screen issue on pulling off ADP and apply it on again within 2 seconds.	EE
	03/02	3	64	Add C6410, pop R6419.	Solve +3.3V_ALW drop issue.	EE
		4	65	Add C6501, pop R6502.	Solve +3.3V_ALW drop issue.	EE
		5	86	Add PC8618.	Solve +1.5V_SUS drop issue.	EE
		6	42	Change C4208 to 470pF.	Solve +5V_ALW drop issue.	EE
		7	32	R3214 change to short pad.		EE
		8	65	Add R6503, Q6501.	+3.3V_RUN_WWAN discharge circuit.	EE
		9	71	Delete L7101, L7102.		EE
		10	37	R3703 change to 33k ohm.	Change board ID.	EE
	03/03	11	72	Add extra power pins to U7202.	Add Ricoh as express card power switch second source.	EE
	03/05	12	47	PTC4702 pop. PTC4703 dummy.	Add Ricoh as express card power switch second source.	EE
		13	54	Change Q5405 to 84.2N702.E31.		EE
		14	65	Name net "WWAN_DIS".		EE
	03/08	15	58	XDP1, XDP2, R5803, R5804, R5806, C5803, C5802, R5808, R5807, TP5808, TP5810, TP5815, TP5802, TP5803, TP5804, TP5805, TP5806, TP5807, TP5809, TP5811, TP5812, TP5801, TP5813, TP5814 change symbols.	Change the symbols so that when SMT, solder paste will not be applied onto the locations.	EE
		16	24	Delete AFTP2401, AFTP2402.		EE
	03/10	17	7,23, 25	Delete RN701, RN703, RN704, RN705, R708, RN2311, RN2302, RN2306, RN2307, RN2308, RN2301, RN2505.		EE
		18	40	C4002 pop.		EE
		19	55	Add AFTP5502, AFTP5503, AFTP5504.	Factory request.	EE
		20	67	C6705, C6704 set as SC.	Smart Card use only.	EE
		21	70	R7001 dummy.		EE
		22	78	Delete EL7801.	Common mode choke longer needed.	EE
	03/17	23	67	Change Smart Card socket into 21.H0136.011, Smart Card connector into 62.10024.C11.		EE
		24	68	Change SW1 into 62.40018.601.		EE
		25	79	Change H18 and H19 into ZZ.00PAD.S31.		EE

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VERSION	DATE	NO	PAGE	Modified List	Issue Description	OWNER
-1	03/18	26	9	Dummy R903, R913, Q901, C901.	CPU_CATERR# continously pull high.	EE
		27	67	Add C6706, 78.27134.1FL.	Eliminate ripple.	EE
		28	64	Remove EL6401.		EE
	03/19	29	67	Change R6705 into 63.10334.1DL, C6704 into 78.22034.1FL, C6705 into 78.39124.2FL, R6701 change to 63.R0034.1DL.	Smart card VCC ripple eliminate.	EE
	03/22	30	46	Change PR4647 into 64.32425.6DL.	Raise +5V_ALW voltage level.	EE

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