

COMPAL CONFIDENTIAL

MODEL NAME : JAZ00

PCB NO : LA-4291P

BOM P/N : 46155331L01

MINICOOPER

**uFCBGA Mobile Penryn SFF ULV
Intel Cantiga GS(High Performance) + ICH9M SFF**

12-07-2007

REV : 0.1(X00)

@ : Nopop Component

1@ : TAA board Used only

2@ : Without TAA board Used only

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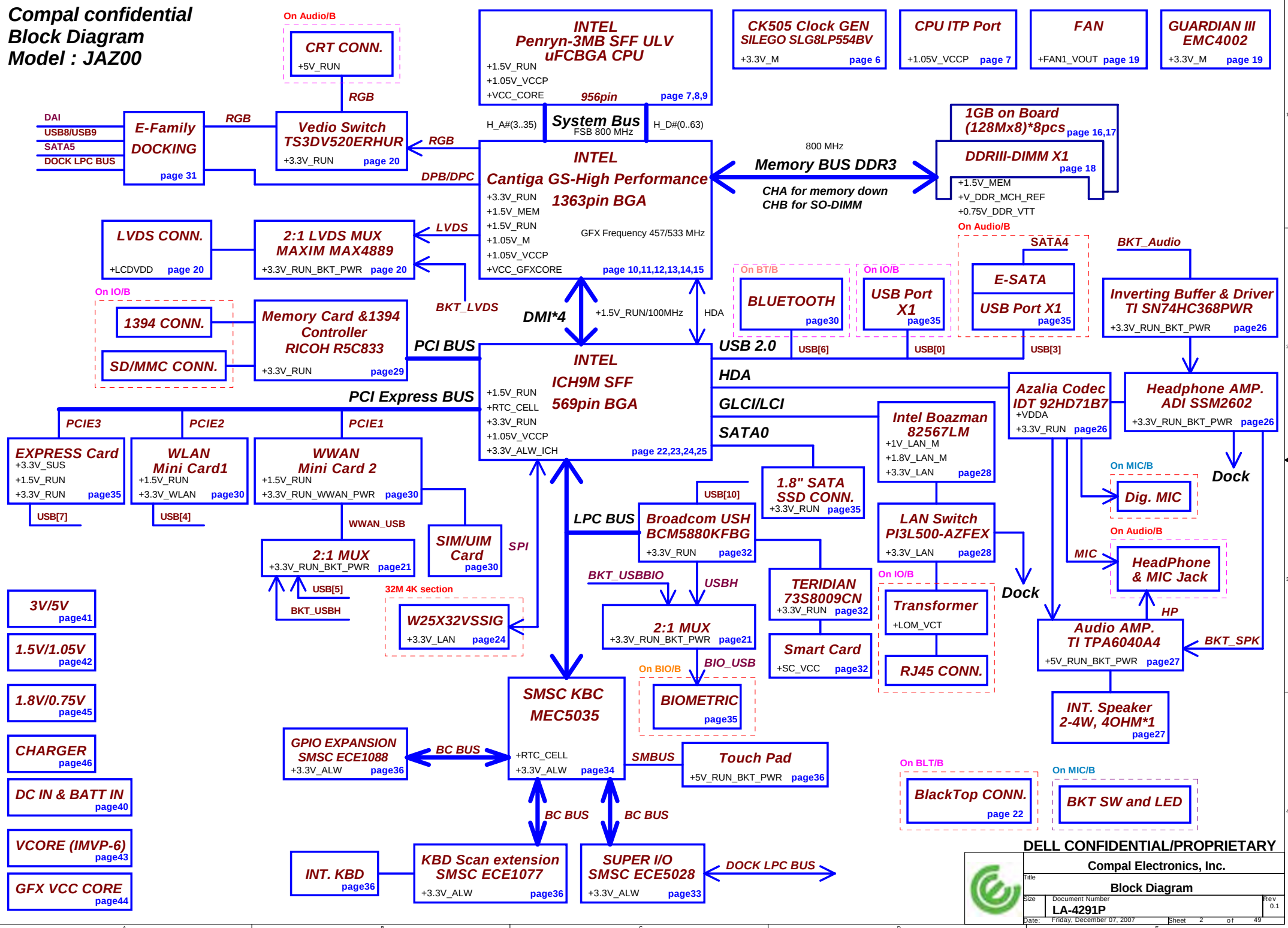


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Cover sheet			
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Compal confidential
Block Diagram
Model : JAZ00



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
0	JUSB (Ext Right Side)
1	NONE
2	NONE
3	JESATA (Ext Left Side)
4	WLAN
5	WWAN
6	BT
7	Express card
8	DOCKING
9	DOCKING
10	USH->BIO
11	NONE

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO +1.5V_ALW_HDA	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_GFXCORE +VCC_CORE +1.05V_VCCP	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)	+3.3V_RUN_BKT_PWR +5V_RUN_BKT_PWR +3.3V_RUN_WWAN_PWR +INV_PWR_SRC +LCDVDD	+3.3V_BKT_PWR
S0	ON	ON	ON	ON	ON	ON	OFF
S3	ON	ON	OFF	ON	OFF	OFF	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BLT mode	ON	OFF	OFF	OFF	OFF	ON	ON

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-2 WWAN
Lane 2	MINI CARD-1 WLAN
Lane 3	None
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	Giga LAN

PCI TABLE

PCI DEVICE	IDSEL	REQ#/IGNT#	PIRQ
R5C833	AD17	REQ#1 / GNT#1	PIRQ[C..D]

SATA	DESTINATION
SATA0	SSD
SATA1	None
SATA4	ESATA
SATA5	DOCKING

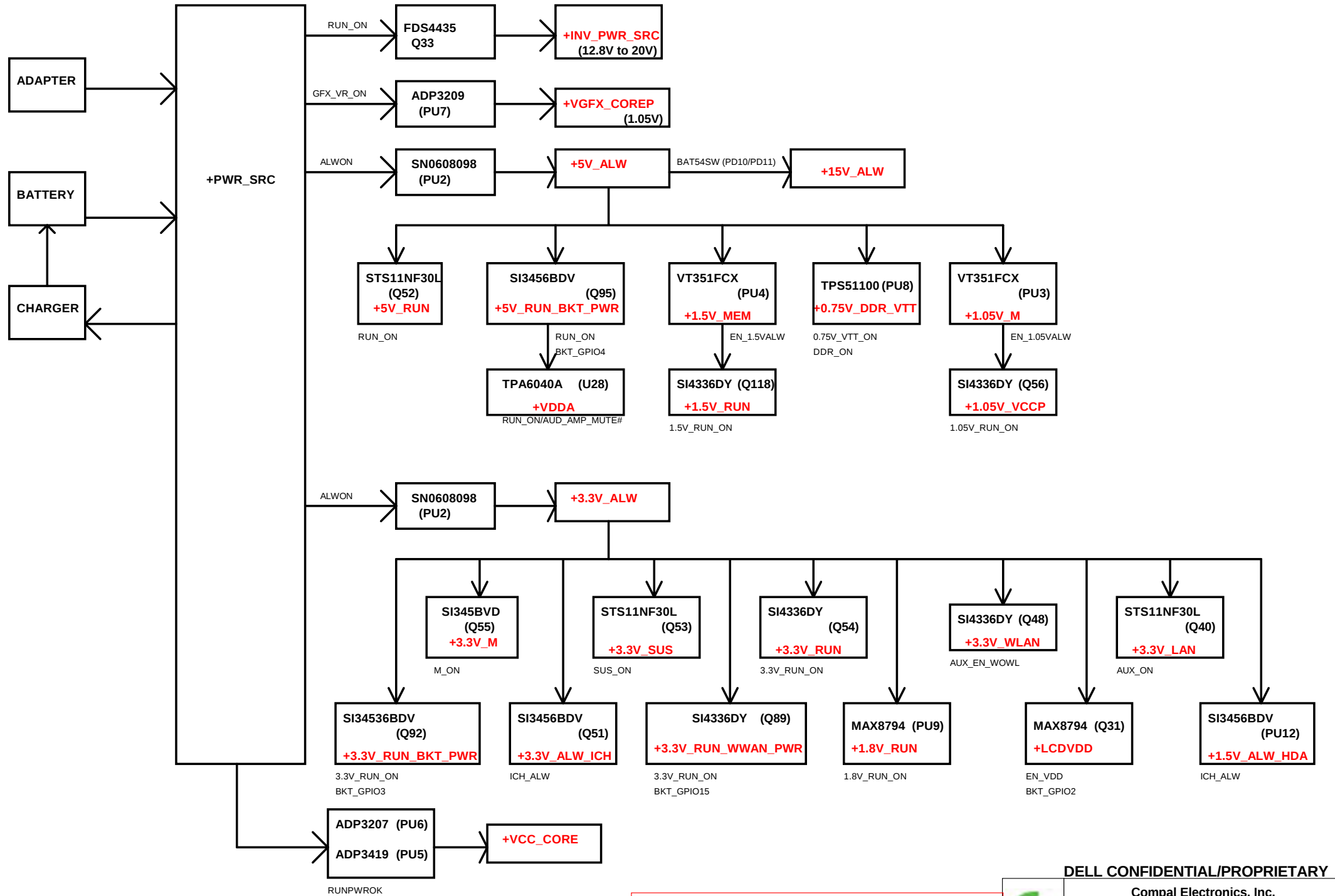
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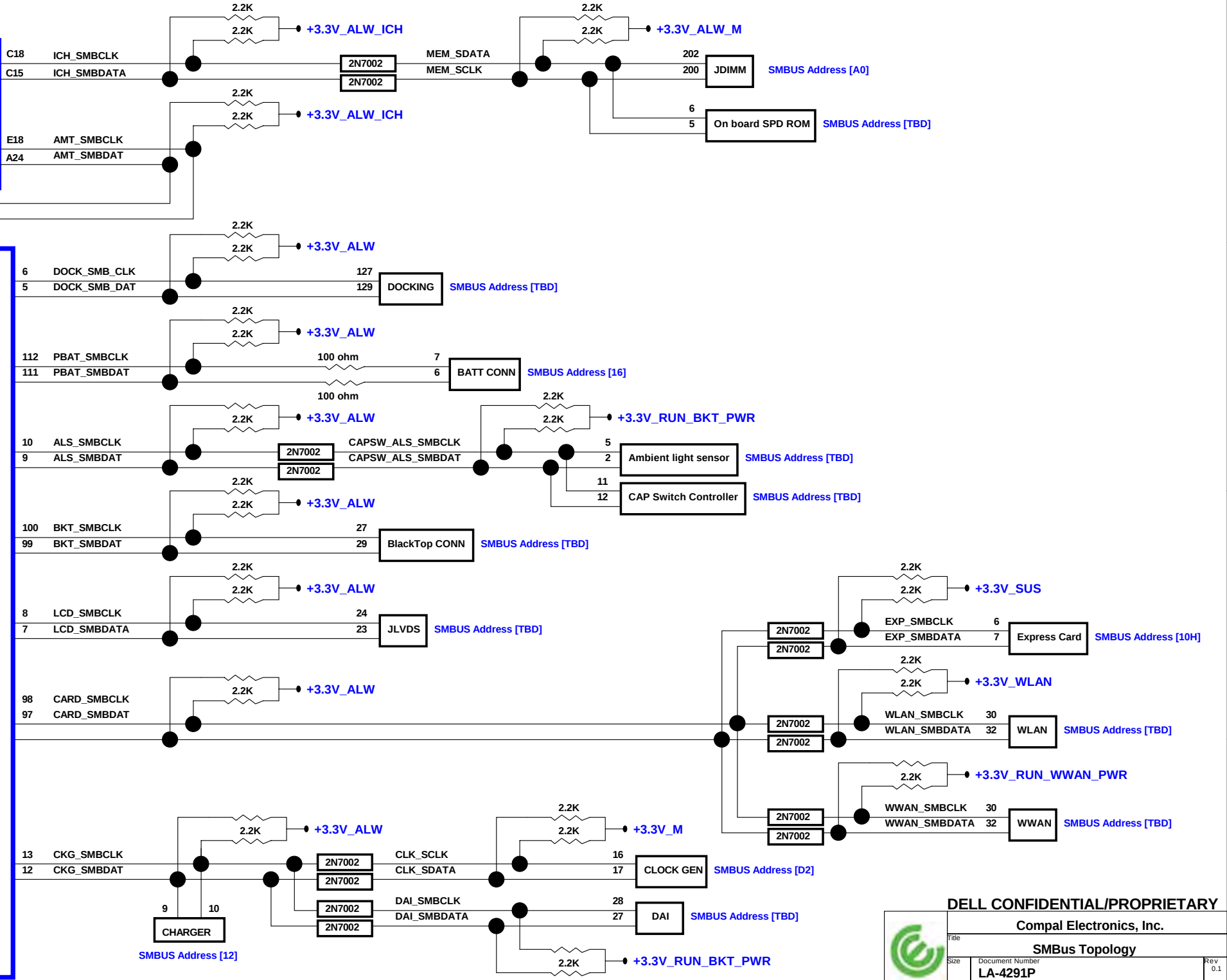
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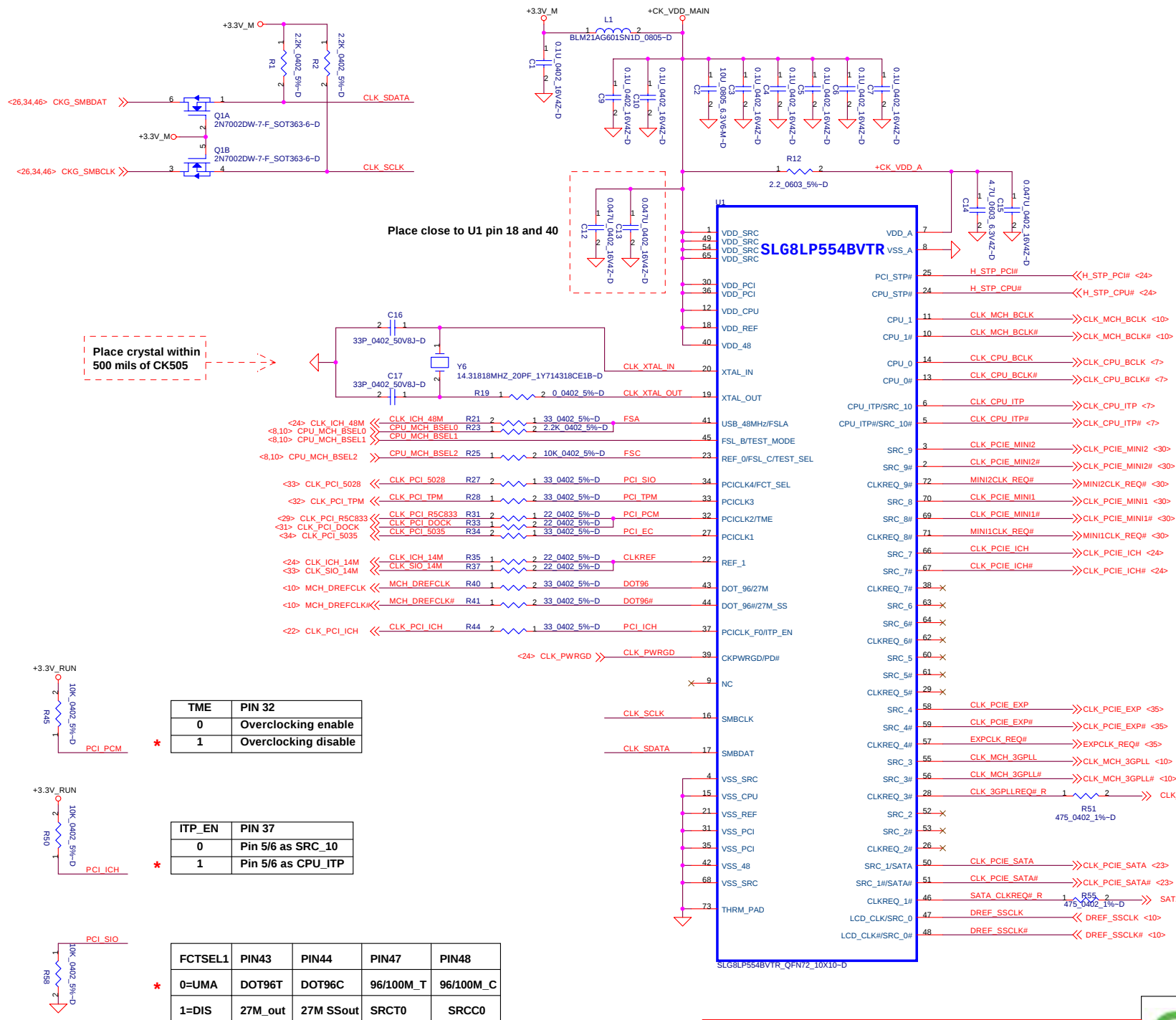




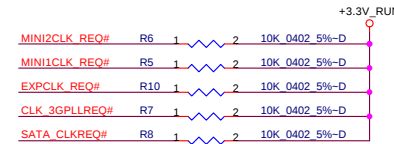
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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3



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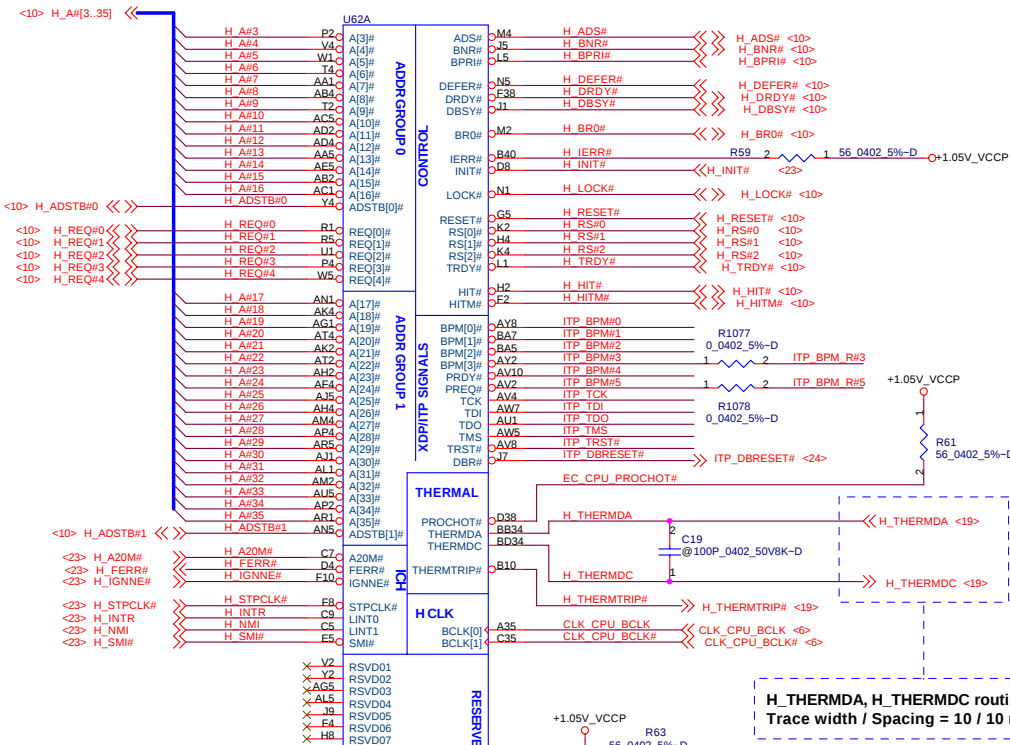
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Clock GEN. with internal terminations

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Place close to J1TP within 100 mil

<6> CLK_CPU_ITP

<6> CLK_CPU_ITP#

H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

Place close to CPU within 200 mil

Place close to CPU within 200ps = 1000 mil

Place close to J1TP within 1ns = 5000 mil

Place close to J1TP within 200ps = 1000 mil

Layout Note: for ITP700Flex debug port with a XDP based Run Control Tools

ITP_BPM#[0..5], TCK, and TMS routings
must be a maximum of 1.5ns = 7500 mil

ITP_BPM#[0..5], and TCK to FBO routings
must be length matched to within 50ps = 250 mil

Place R70 close to J1TP pin 5
TCK to FBO routing should refer to debug port design guide
H_RESET# should be routed from GMCH with split to ITP conn. Refer to DG page #56

Depop J1TP, C18, R68, R70, R64, R67, R69
when JIP connector is depopulated



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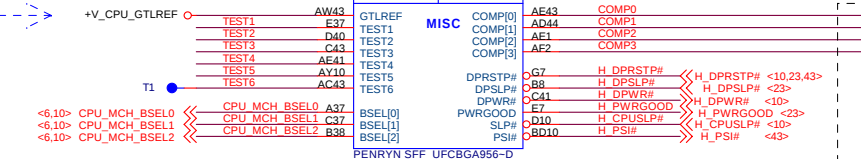
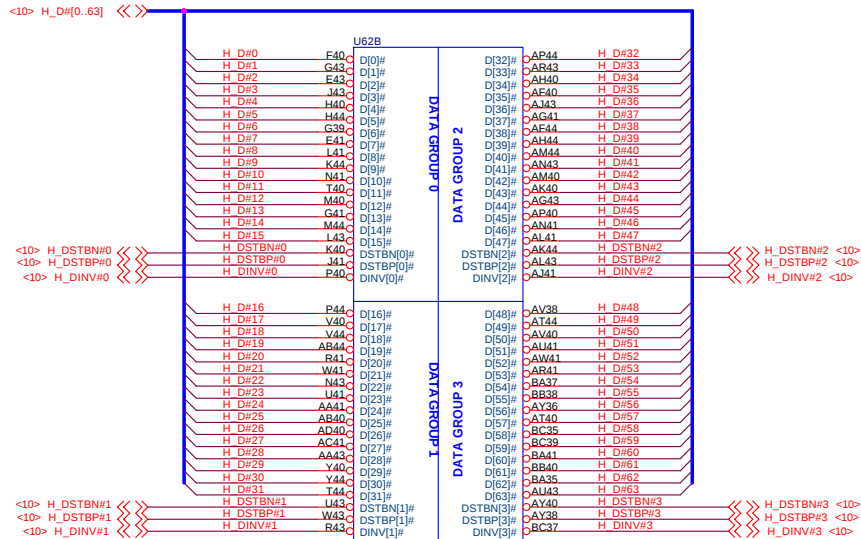
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Penryn SFF ULV Processor(1/3)

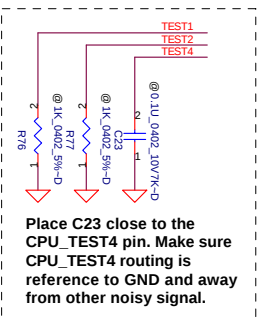
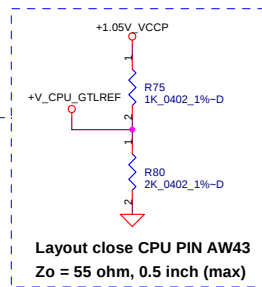
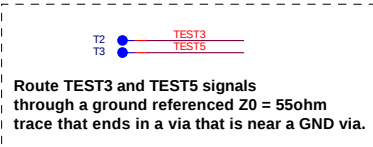
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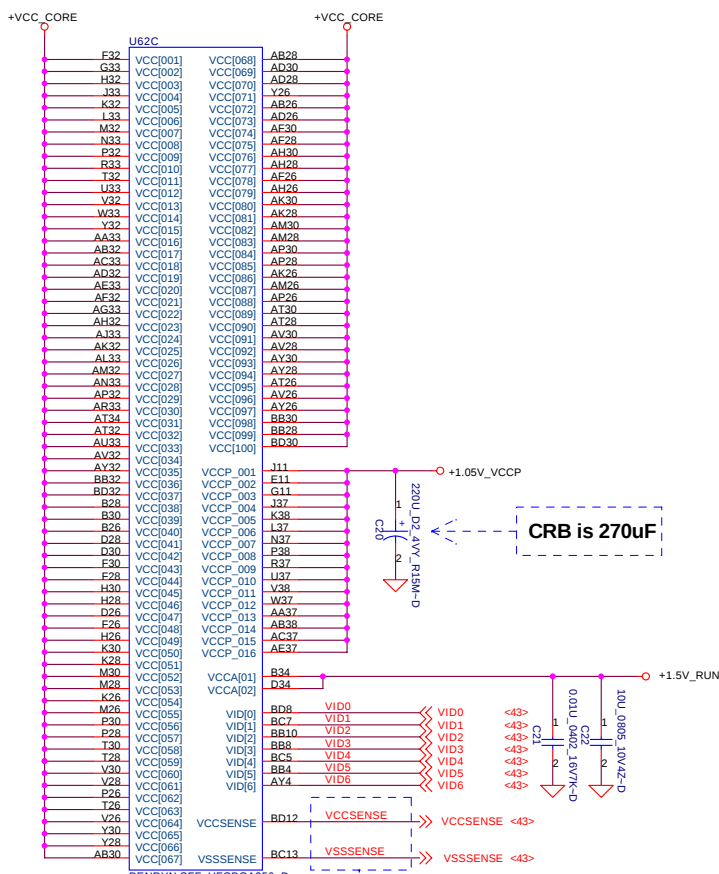
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FSB	BCLK	BSEL2	BSEL1	BSEL0
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

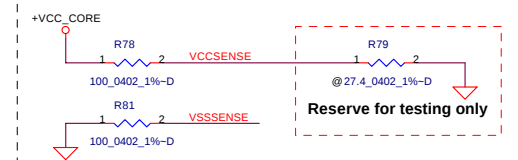


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP0, COMP2 trace should be 27.4 ohm. COMP1, COMP3 should be 55ohm.



Length match within 25 mils, Z0=27.4 ohm

Place R78 and R81 close to CPU within 1000 mil



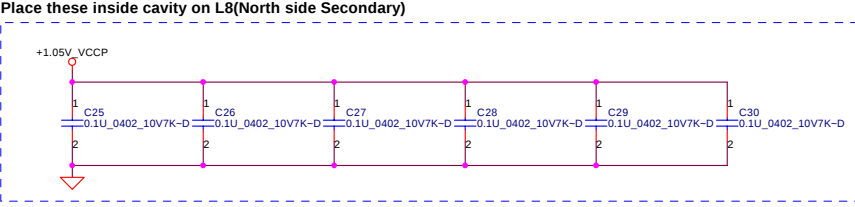
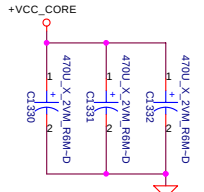
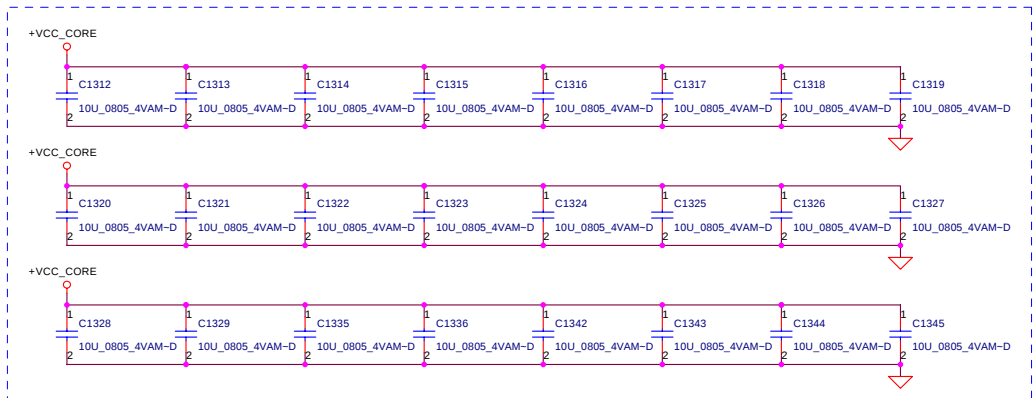
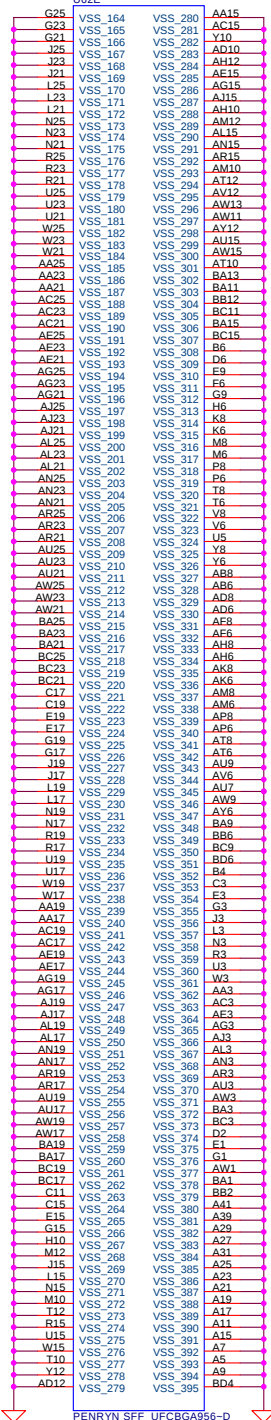
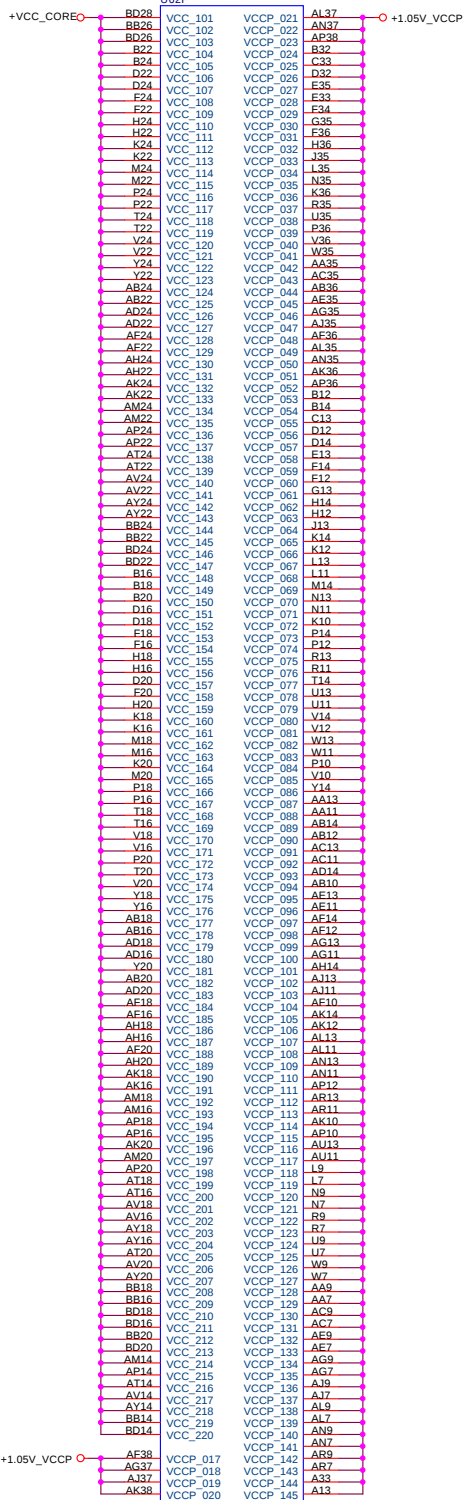
Route VCCSENSE and VSSSENSE trace at 27.4 ohms with 7 mil spacing

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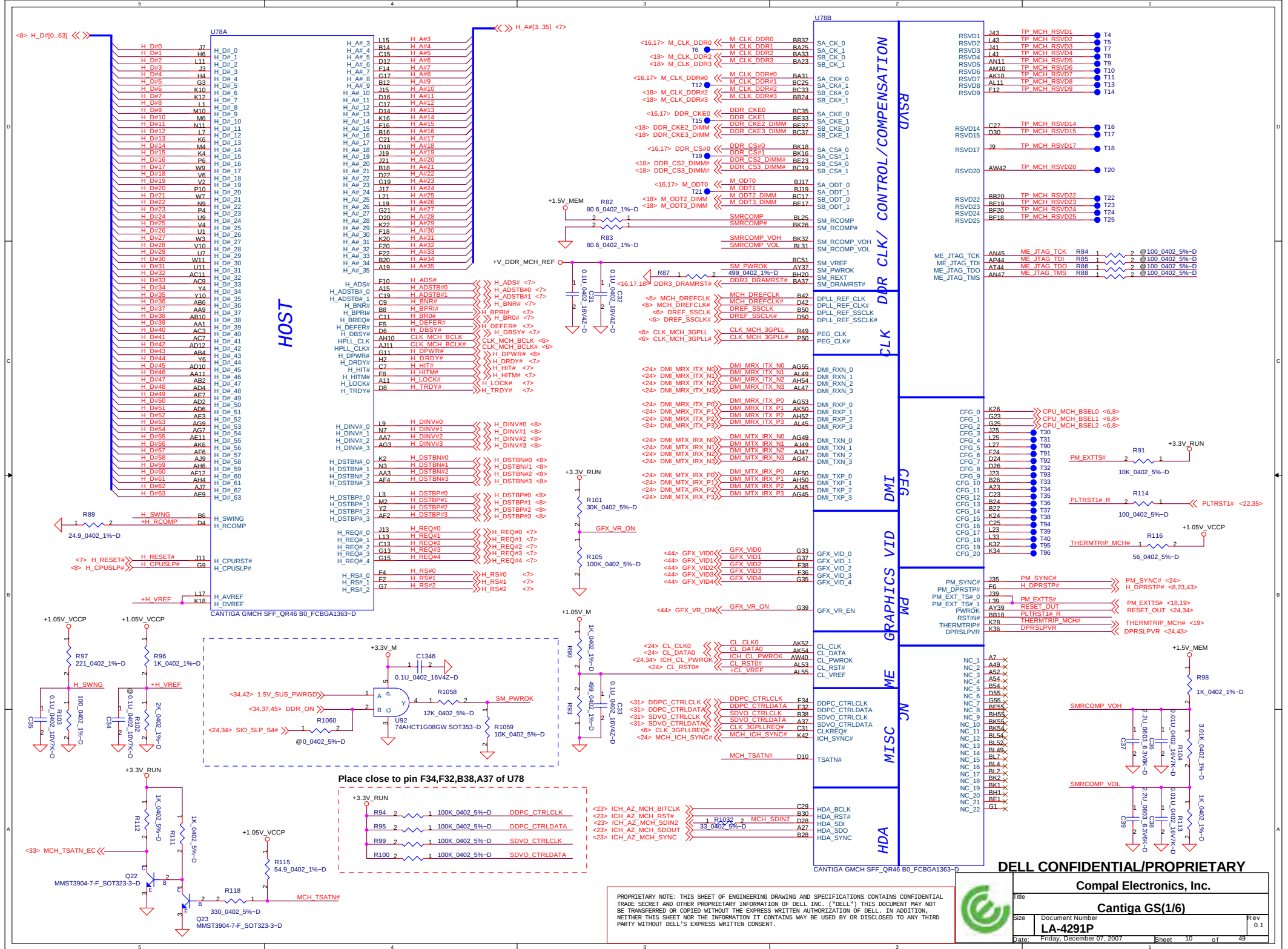
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Penryn SFF ULV Processor(3/3)

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D

C

B

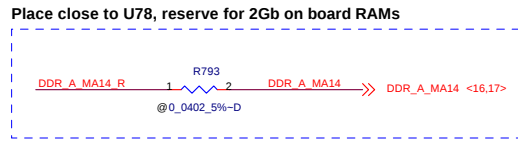
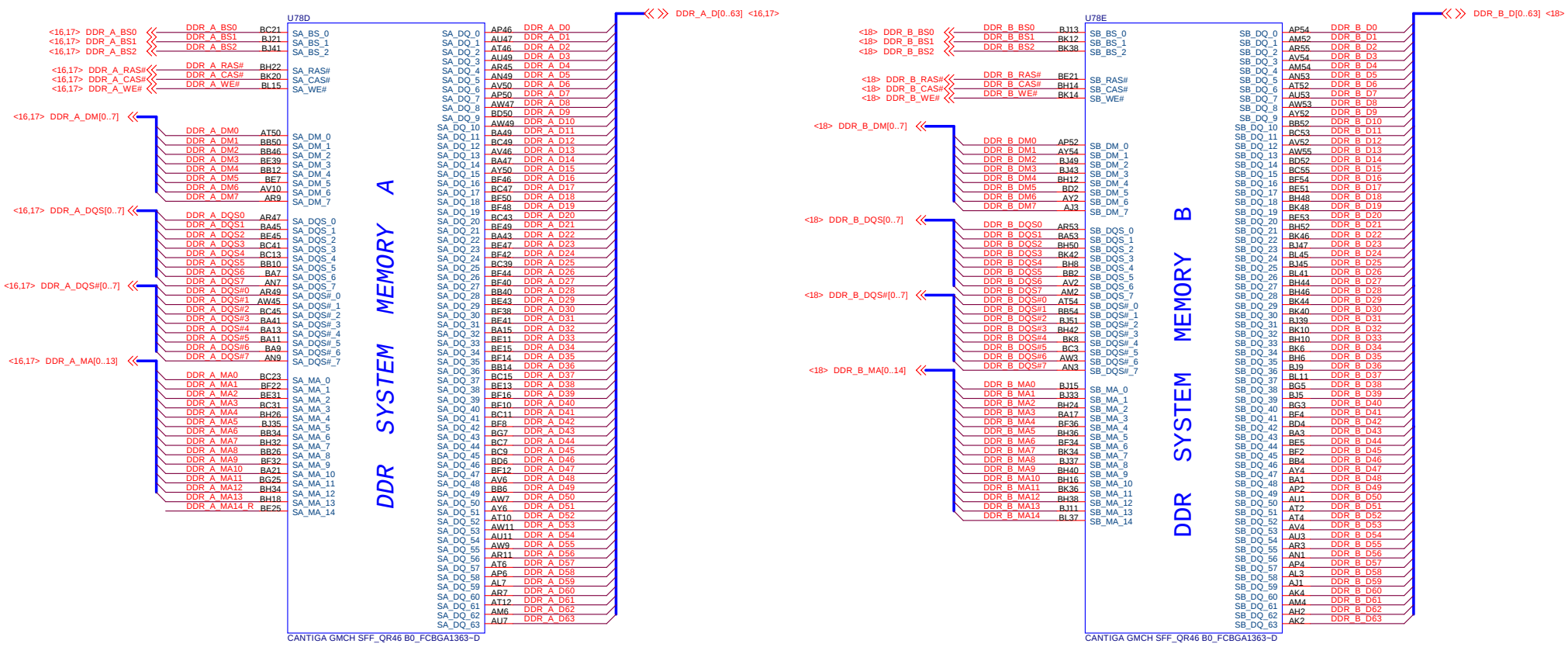
A

D

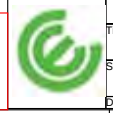
C

B

A



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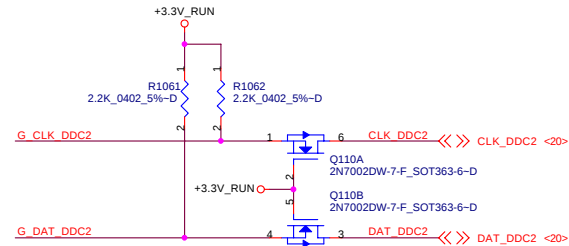


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Cantiga GS(2/6)

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CFG[5:16] have internal pullup CFG[19:20] have internal pulldown

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CRB 270uF

118.8mA Max.

64.8mA Max.

64.8mA Max.

24mA Max.

139.2mA Max.

CRT

PLL

A PEG A LVDS

A SM

SM CK

HV

PEG

DMI

LVDS

TV/CRT HDA TV

POWER

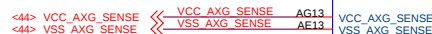
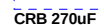
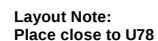
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Cantiga GS(4/6)

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U78I

BA55	VSS_1	VSS_100	C43
AU55	VSS_2	VSS_101	A43
AN55	VSS_3	VSS_102	BD42
AJ55	VSS_4	VSS_103	H42
AE55	VSS_5	VSS_104	BG41
AA55	VSS_6	VSS_105	AY41
IJ55	VSS_7	VSS_106	AU41
BD54	VSS_8	VSS_107	AM41
BG53	VSS_9	VSS_108	AU41
AJ53	VSS_10	VSS_109	AG41
AE53	VSS_11	VSS_110	AE41
AA53	VSS_12	VSS_111	AA41
IJ53	VSS_13	VSS_112	RA41
N53	VSS_14	VSS_113	MA41
J53	VSS_15	VSS_114	E41
GS5	VSS_16	VSS_115	BD40
E53	VSS_17	VSS_116	AU40
K52	VSS_18	VSS_117	AR40
BG51	VSS_19	VSS_118	AN40
AW51	VSS_20	VSS_119	W40
AU51	VSS_21	VSS_120	IA40
AR51	VSS_22	VSS_121	TA40
AN51	VSS_23	VSS_122	R40
AE51	VSS_24	VSS_123	K40
AA51	VSS_25	VSS_124	H40
IJ51	VSS_26	VSS_125	BL39
BD50	VSS_27	VSS_126	BG39
BG49	VSS_28	VSS_127	BA39
AJ49	VSS_29	VSS_128	E39
AE49	VSS_30	VSS_129	C39
AA49	VSS_31	VSS_130	A39
IJ49	VSS_32	VSS_131	BD38
N49	VSS_33	VSS_132	AU38
J49	VSS_34	VSS_133	H38
GS4	VSS_35	VSS_134	BG37
E49	VSS_36	VSS_135	AU37
K48	VSS_37	VSS_136	M37
BG47	VSS_38	VSS_137	E37
AW47	VSS_39	VSS_138	BD36
AU47	VSS_40	VSS_139	AW36
AR47	VSS_41	VSS_140	H36
AN47	VSS_42	VSS_141	BL35
AE47	VSS_43	VSS_142	BG35
AA47	VSS_44	VSS_143	AY35
IJ47	VSS_45	VSS_144	AU35
BD46	VSS_46	VSS_145	AL35
BG45	VSS_47	VSS_146	AG35
AJ45	VSS_48	VSS_147	AE35
AE45	VSS_49	VSS_148	AA35
AA45	VSS_50	VSS_149	Y35
IJ45	VSS_51	VSS_150	M35
N45	VSS_52	VSS_151	E35
J45	VSS_53	VSS_152	A35
GS4	VSS_54	VSS_153	BD34
E45	VSS_55	VSS_154	AU34
K44	VSS_56	VSS_155	AN34
BG43	VSS_57	VSS_156	H34
AW43	VSS_58	VSS_157	BL33
AU43	VSS_59	VSS_158	BG33
AR43	VSS_60	VSS_159	AY33
AN43	VSS_61	VSS_160	E33
AE43	VSS_62	VSS_161	BD32
AA43	VSS_63	VSS_162	AU32
IJ43	VSS_64	VSS_163	AN32
BD42	VSS_65	VSS_164	AG32
BG41	VSS_66	VSS_165	AC32
AJ41	VSS_67	VSS_166	Y32
AE41	VSS_68	VSS_167	H32
AA41	VSS_69	VSS_168	B32
IJ41	VSS_70	VSS_169	BL31
N41	VSS_71	VSS_170	BG31
J41	VSS_72	VSS_171	AY31
GS4	VSS_73	VSS_172	U31
E41	VSS_74	VSS_173	M31
K40	VSS_75	VSS_174	E31
BG39	VSS_76	VSS_175	N30
AW39	VSS_77	VSS_176	H30
AU39	VSS_78	VSS_177	AN29
AR39	VSS_79	VSS_178	AJ29
AN39	VSS_80	VSS_179	M29
AE39	VSS_81	VSS_180	A29
AA39	VSS_82	VSS_181	AW28
IJ39	VSS_83	VSS_182	AN28
BD38	VSS_84	VSS_183	AD28
BG37	VSS_85	VSS_184	AC28
AJ37	VSS_86	VSS_185	Y28
AE37	VSS_87	VSS_186	W28
AA37	VSS_88	VSS_187	H28
IJ37	VSS_89	VSS_188	F28
N37	VSS_90	VSS_189	AN27
J37	VSS_91	VSS_190	AJ27
GS3	VSS_92	VSS_191	M27
E37	VSS_93	VSS_192	BE26
K36	VSS_94	VSS_193	BD26
BG35	VSS_95	VSS_194	N26
AW35	VSS_96	VSS_195	H26
AU35	VSS_97	VSS_196	AY25
AR35	VSS_98	VSS_197	AU25
AN35	VSS_99	VSS_198	

CANTIGA GMCH SFF_QR46 B0_FCBGA1363-D

U78J

AN25	VSS_199	VSS_300	AM8
AG25	VSS_200	VSS_301	AK8
AE25	VSS_201	VSS_302	AH8
AA25	VSS_202	VSS_303	AE8
IJ25	VSS_203	VSS_304	AD8
N25	VSS_204	VSS_305	AB8
J25	VSS_205	VSS_306	Y8
GS24	VSS_206	VSS_307	V8
E25	VSS_207	VSS_308	P8
BD24	VSS_208	VSS_309	M8
AN24	VSS_209	VSS_310	K8
AL24	VSS_210	VSS_311	H8
H24	VSS_211	VSS_312	B17
BG23	VSS_212	VSS_313	E7
AY23	VSS_213	VSS_314	BF6
BD22	VSS_214	VSS_315	BC5
BB22	VSS_215	VSS_316	BA5
AN22	VSS_216	VSS_317	AW5
Y22	VSS_217	VSS_318	AU5
W22	VSS_218	VSS_319	AR5
H22	VSS_219	VSS_320	AN5
BL21	VSS_220	VSS_321	AL5
BG21	VSS_221	VSS_322	AJ5
AY21	VSS_222	VSS_323	AG5
AN21	VSS_223	VSS_324	AE5
AG21	VSS_224	VSS_325	AC5
AE21	VSS_225	VSS_326	AA5
M21	VSS_226	VSS_327	W5
E21	VSS_227	VSS_328	U5
A21	VSS_228	VSS_329	N5
BD20	VSS_229	VSS_330	L5
H20	VSS_230	VSS_331	J5
BG19	VSS_231	VSS_332	G5
AY19	VSS_232	VSS_333	C5
BL19	VSS_233	VSS_334	BH4
BD18	VSS_234	VSS_335	BE3
N18	VSS_235	VSS_336	U3
E18	VSS_236	VSS_337	E3
BL17	VSS_237	VSS_338	BC1
BG17	VSS_238	VSS_339	AW1
AY17	VSS_239	VSS_340	AR1
M17	VSS_240	VSS_341	AL1
E17	VSS_241	VSS_342	AG1
A17	VSS_242	VSS_343	AC1
BD16	VSS_243	VSS_344	W1
AN16	VSS_244	VSS_345	N1
AG16	VSS_245	VSS_346	J1
AE16	VSS_246	VSS_347	AU43
Y16	VSS_247	VSS_348	BB42
W16	VSS_248	VSS_349	AW38
M16	VSS_249	VSS_350	BA35
H16	VSS_250	VSS_351	L29
BG15	VSS_251	VSS_352	N28
AY15	VSS_252	VSS_353	N22
AN15	VSS_253	VSS_354	N20
AD15	VSS_254	VSS_355	N14
AC15	VSS_255	VSS_356	AL13
BL15	VSS_256	VSS_357	B10
M15	VSS_257	VSS_358	AN13
E15	VSS_258		
BD14	VSS_259	VSS_359	N42
BL14	VSS_260	VSS_360	N40
BL13	VSS_261	VSS_361	N38
BG13	VSS_262	VSS_362	M39
AY13	VSS_263		
AU13	VSS_264	VSS_NCTF_1	A138
AP13	VSS_265	VSS_NCTF_2	AH38
AC13	VSS_266	VSS_NCTF_3	AD38
AA13	VSS_267	VSS_NCTF_4	AC38
W13	VSS_268	VSS_NCTF_5	T35
U13	VSS_269	VSS_NCTF_6	R35
M13	VSS_270	VSS_NCTF_7	AT32
E13	VSS_271	VSS_NCTF_8	AR32
BD12	VSS_272	VSS_NCTF_9	U32
AV12	VSS_273	VSS_NCTF_10	R32
AP12	VSS_274	VSS_NCTF_11	T28
AM12	VSS_275	VSS_NCTF_12	I28
AK12	VSS_276	VSS_NCTF_13	AT25
AR12	VSS_277	VSS_NCTF_14	AR25
V12	VSS_278	VSS_NCTF_15	T24
P12	VSS_279	VSS_NCTF_16	R24
H12	VSS_280	VSS_NCTF_17	AN19
BG11	VSS_281	VSS_NCTF_18	AJ19
AG11	VSS_282	VSS_NCTF_19	AA19
E11	VSS_283	VSS_NCTF_20	Y19
BD10	VSS_284	VSS_NCTF_21	T19
F28	VSS_285	VSS_NCTF_22	R19
AP10	VSS_286	VSS_NCTF_23	AN18
H10	VSS_287		
BG9	VSS_288	VSS_SCB_1	BL55
E9	VSS_289	VSS_SCB_2	BL1
A9	VSS_290	VSS_SCB_3	A55
BD8	VSS_291	VSS_SCB_4	D1
B8	VSS_292	VSS_SCB_5	B55
AY8	VSS_293	VSS_SCB_6	B2
AV8	VSS_294	VSS_SCB_7	A4
AT8	VSS_295		
AP8	VSS_296		
	VSS_297		
	VSS_298		
	VSS_299		

CANTIGA GMCH SFF_QR46 B0_FCBGA1363-D

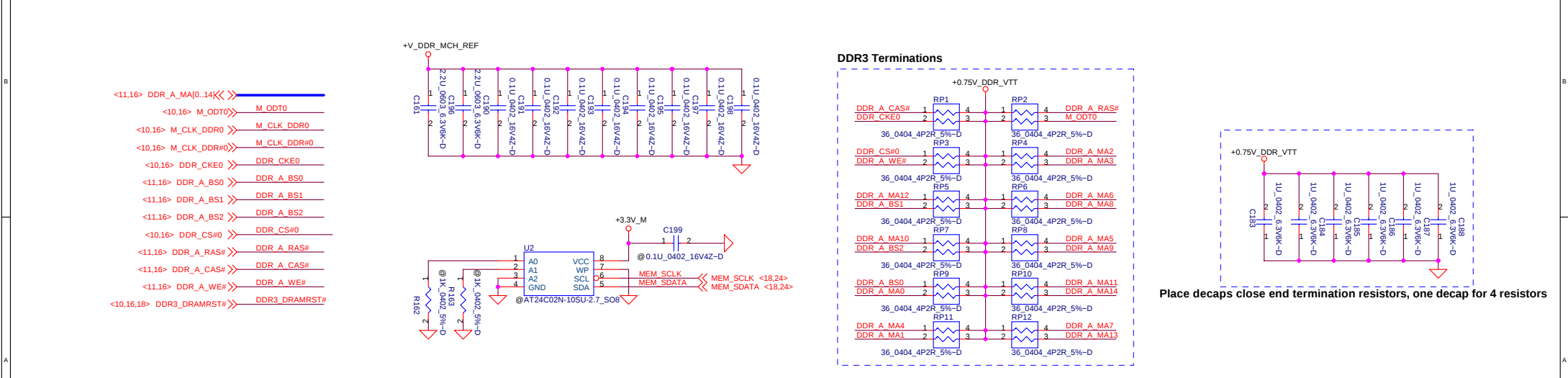
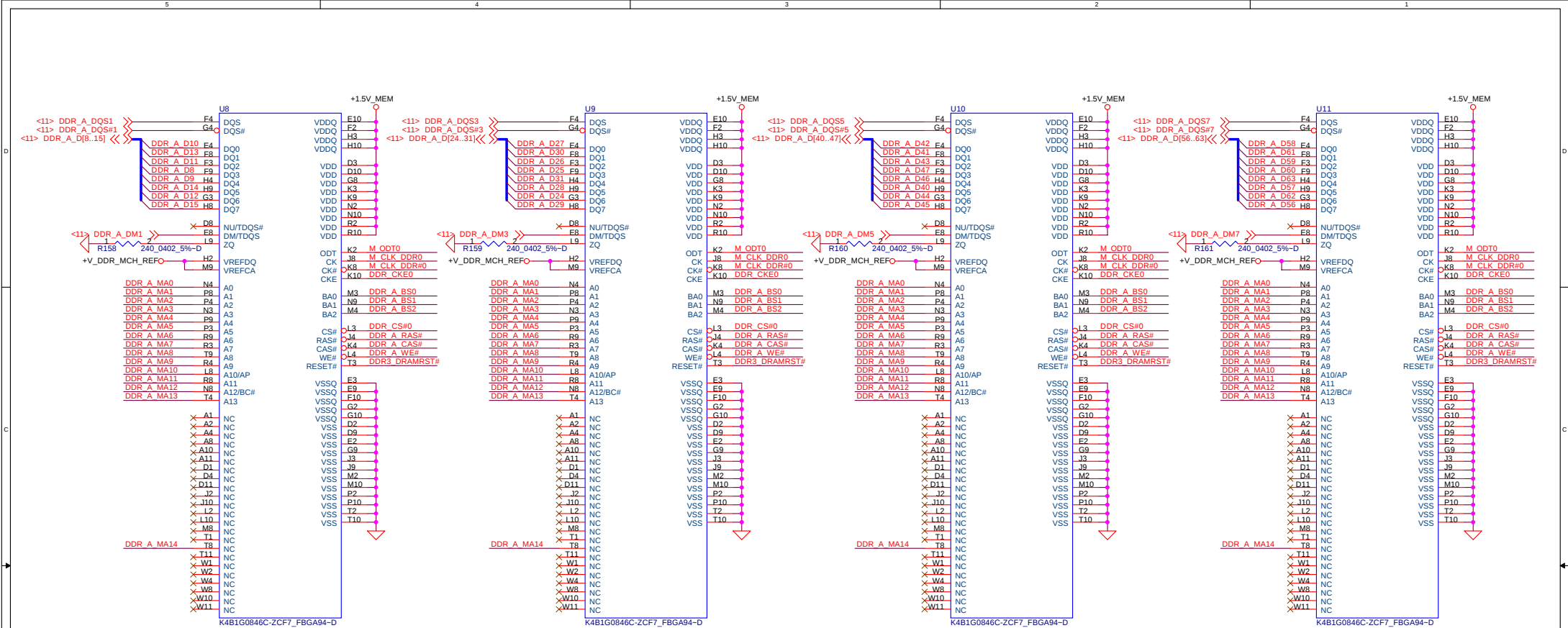
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Cantiga GS(6/6)

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Size		0.1
Document Number		
LA-4291P		
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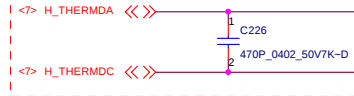
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Place Q29 under CPU



C225 close to Guardian and C224 close to Q29

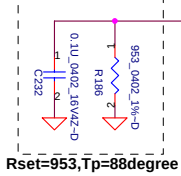
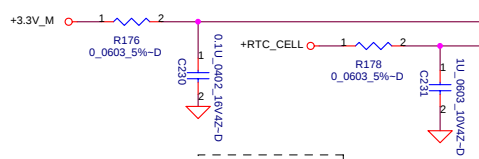
Place C226 close to Guardian pin as possible



Place Q28 close to SO-DIMM



C229 close to Guardian and C223 close to Q28



Rset=953, Tp=88degree

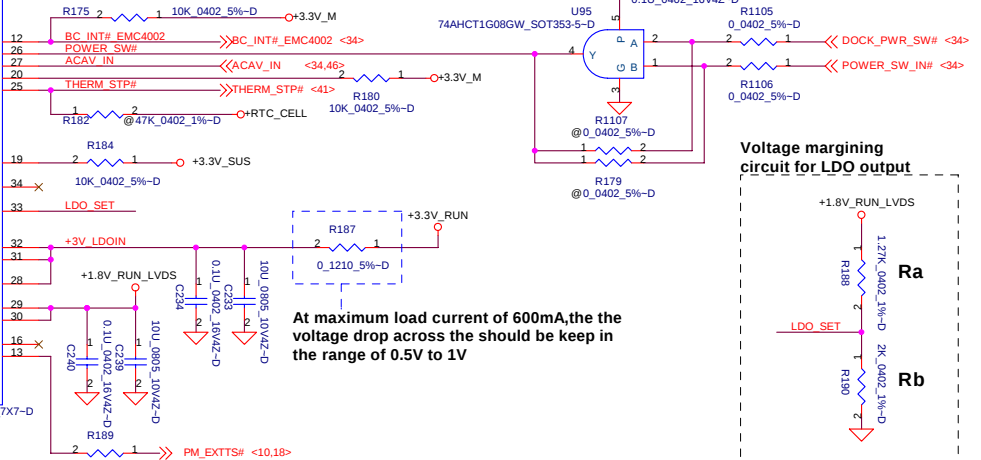
Pull-up Resistor on ADDR_MODE/XEN	For Remote1 mode	SMBus Address
<= 4.7K +/- 5%	2N3904	2F(r/w)
10K	2N3904	2F(r/w)
18K	Thermistor	2F(r/w)
>= 33K	Thermistor	2F(r/w)

Must confirm we can get C version to solve leakage issue
Backdrive from RTC PWR to 3VSUS
B Version need external solution , check Roush I schematic

Diode circuit at DP4/DN4 is used for skin temp sensor (placed Q28 optimally between CPU, MCH and MEM)

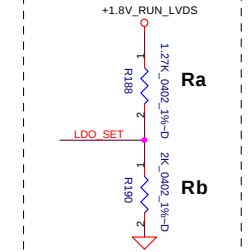
C222 close to Guardian and C228 close to Q30

THERMISTOR OPTION:
Single-ended routing to thermistor is permissible (ground return). Place R173 and C227 near EMC4002



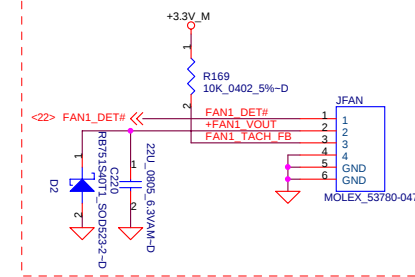
At maximum load current of 600mA, the voltage drop across the should be keep in the range of 0.5V to 1V

Voltage margining circuit for LDO output



Adjustable from 1.2V to 2.5V
 $R_a = ((LDO_OUT/1.1)-1) \times R_b$

FAN control and Tachometer



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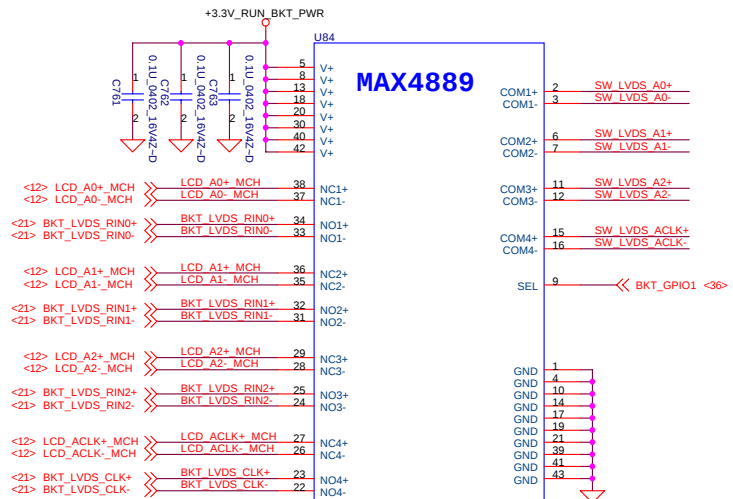
Thermal Sensor and FAN

LA-4291P

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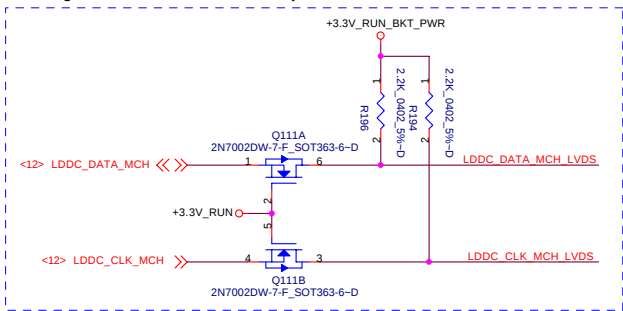
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SEL Logic 1 Work from BKT

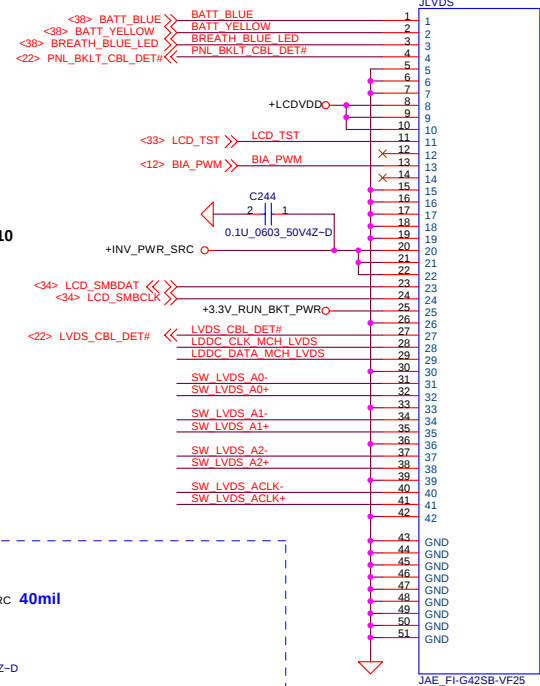
SEL	NC to COM	NO to COM
0	ON	OFF
1	OFF	ON

EDID signals drive low when BlackTop mode

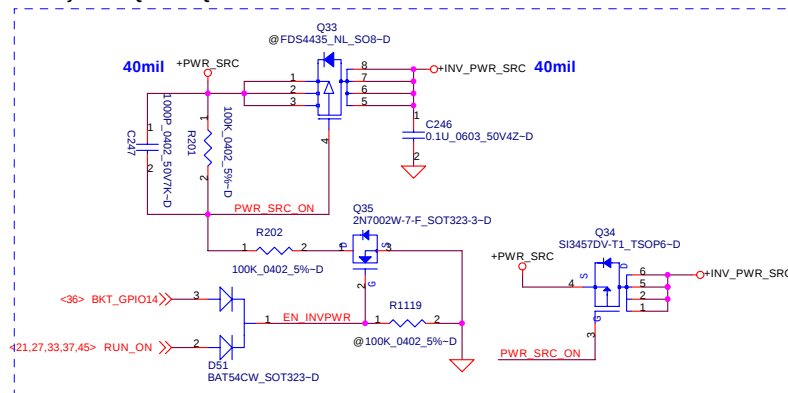


Place close to JLVDS.8,9,10

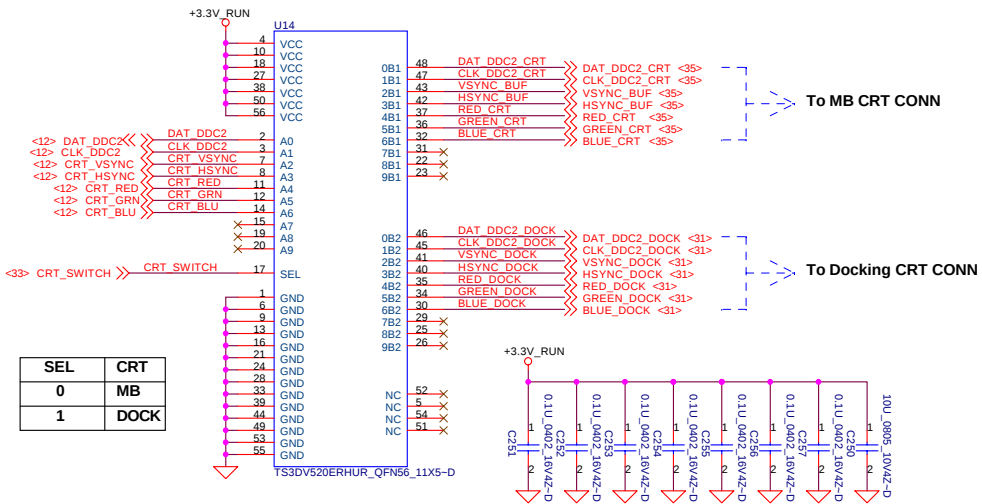
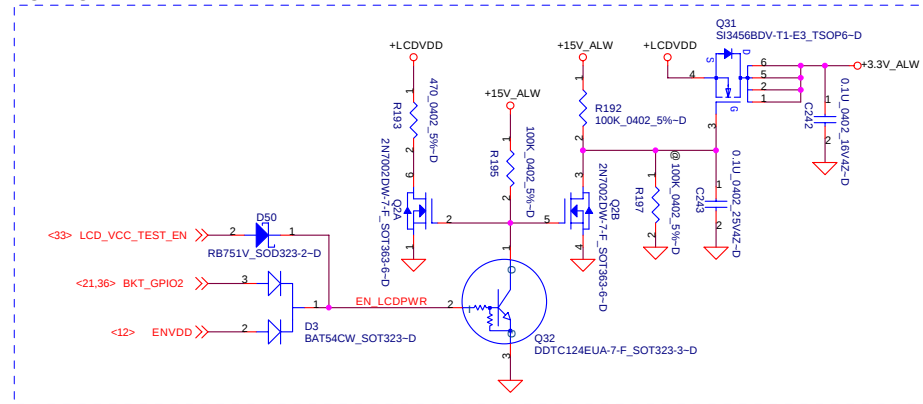
Place close to JLVDS.25



Dual layout for Q33 and Q34



LCD POWER



SEL	CRT
0	MB
1	DOCK

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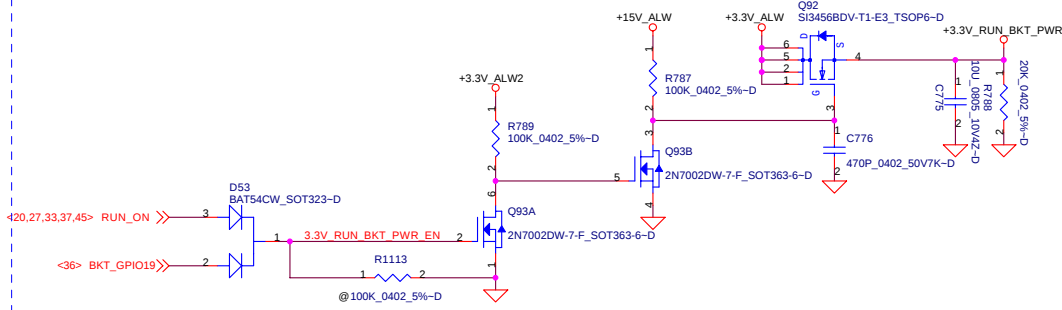
CRT SWITCH, LVDS MUX, LVDS CONN

LA-4291P

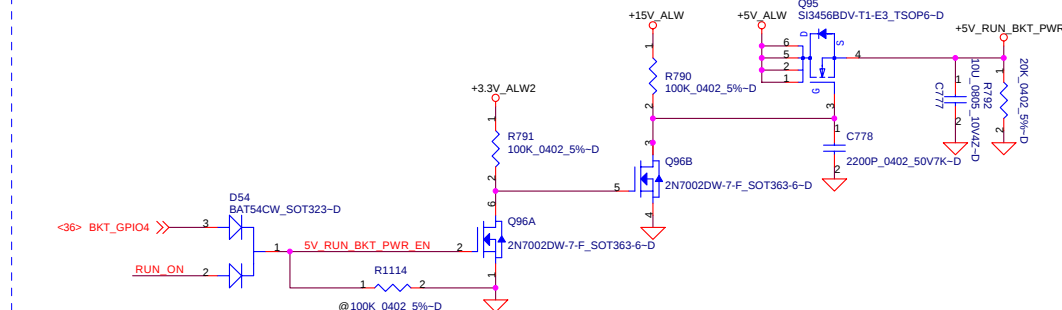
Date: Friday, December 07, 2007 Sheet 20 of 49

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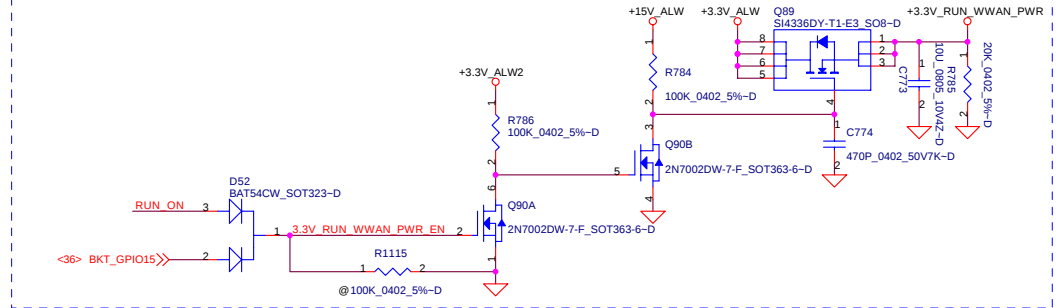
+3.3V_RUN_BKT_PWR Source



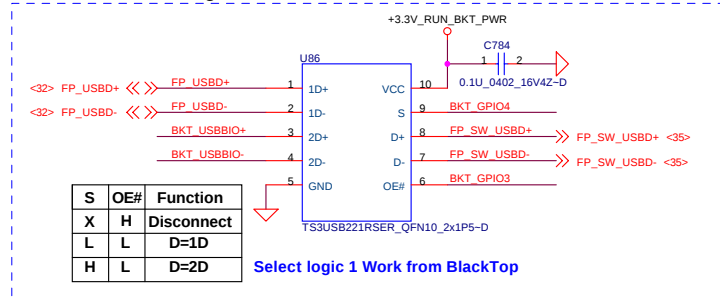
+5V_RUN_BKT_PWR Source, for Touch Pad and Audio Amplifier



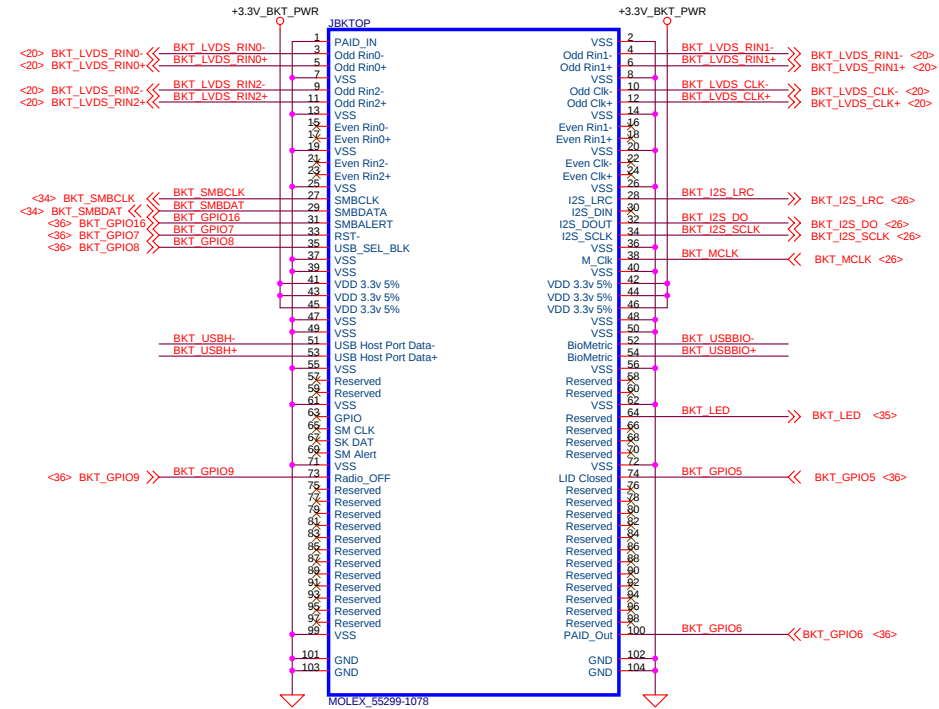
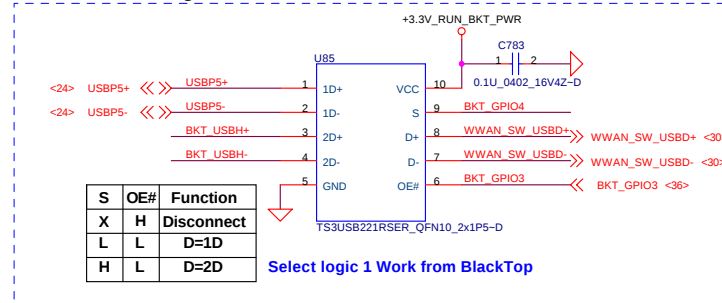
+3.3V_RUN_WWAN_PWR Source, for WWAN



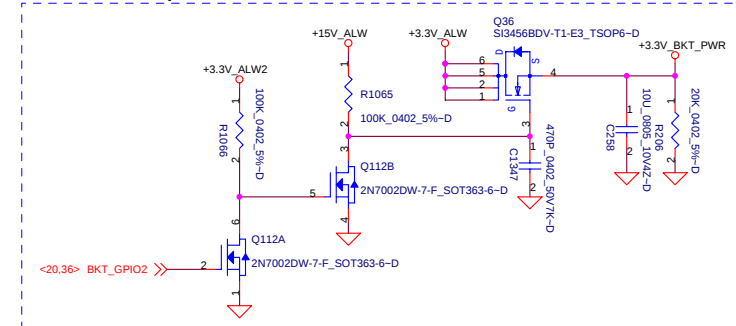
For Biometric USB signals isolation



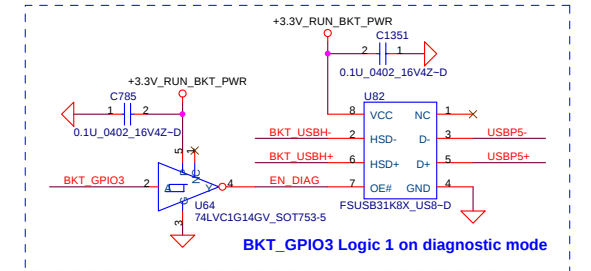
For WWAN USB signals isolation



Enable BlackTop POWER



Add BlackTop to ICH9M interface by USB signals when diagnostic mode



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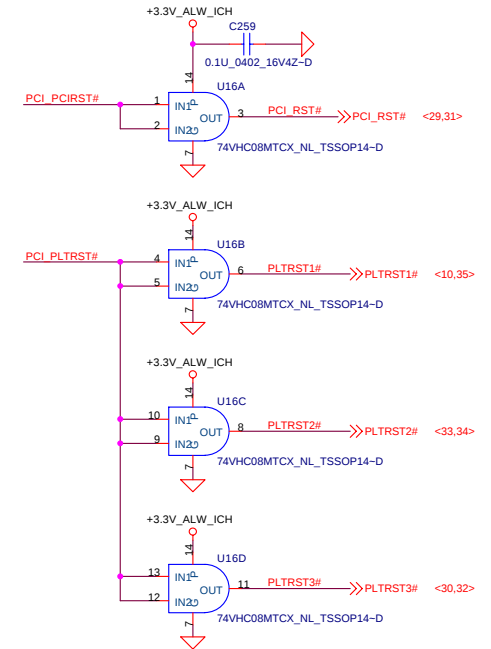
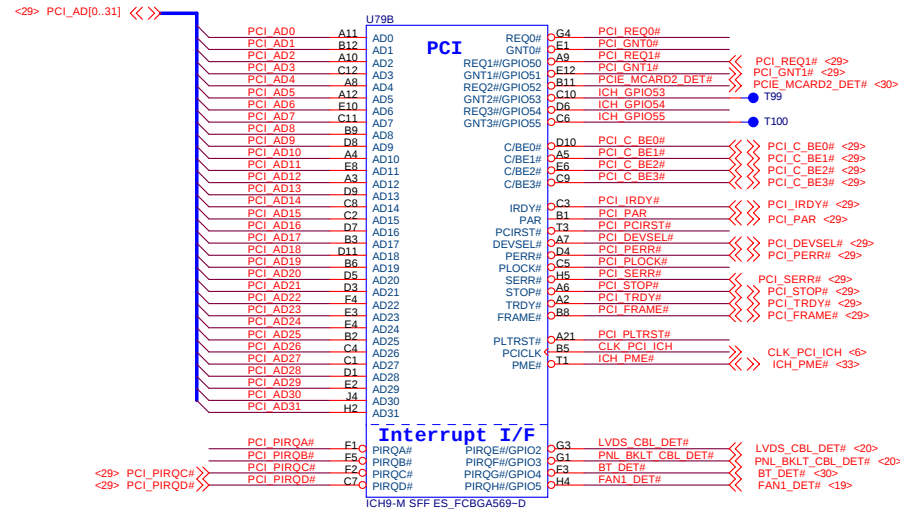
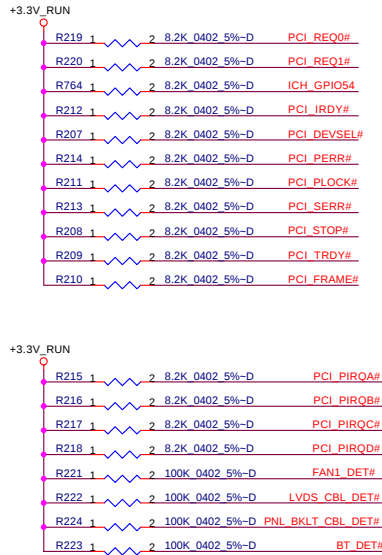
Compal Electronics, Inc.

BlackTop POWER and CONN

LA-4291P

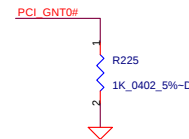
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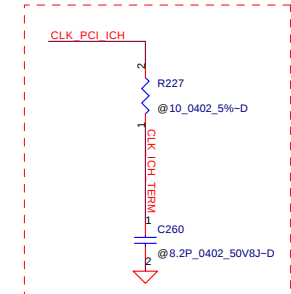


There is a weak integrated pull-up resistor on SPI_CS#1 pin

Boot BIOS Strap		
PCI_GNT0#	SPI_CS1#	Boot BIOS Destination
0	1	SPI
1	0	PCI
1	1	LPC



Place closely pin U79.B5

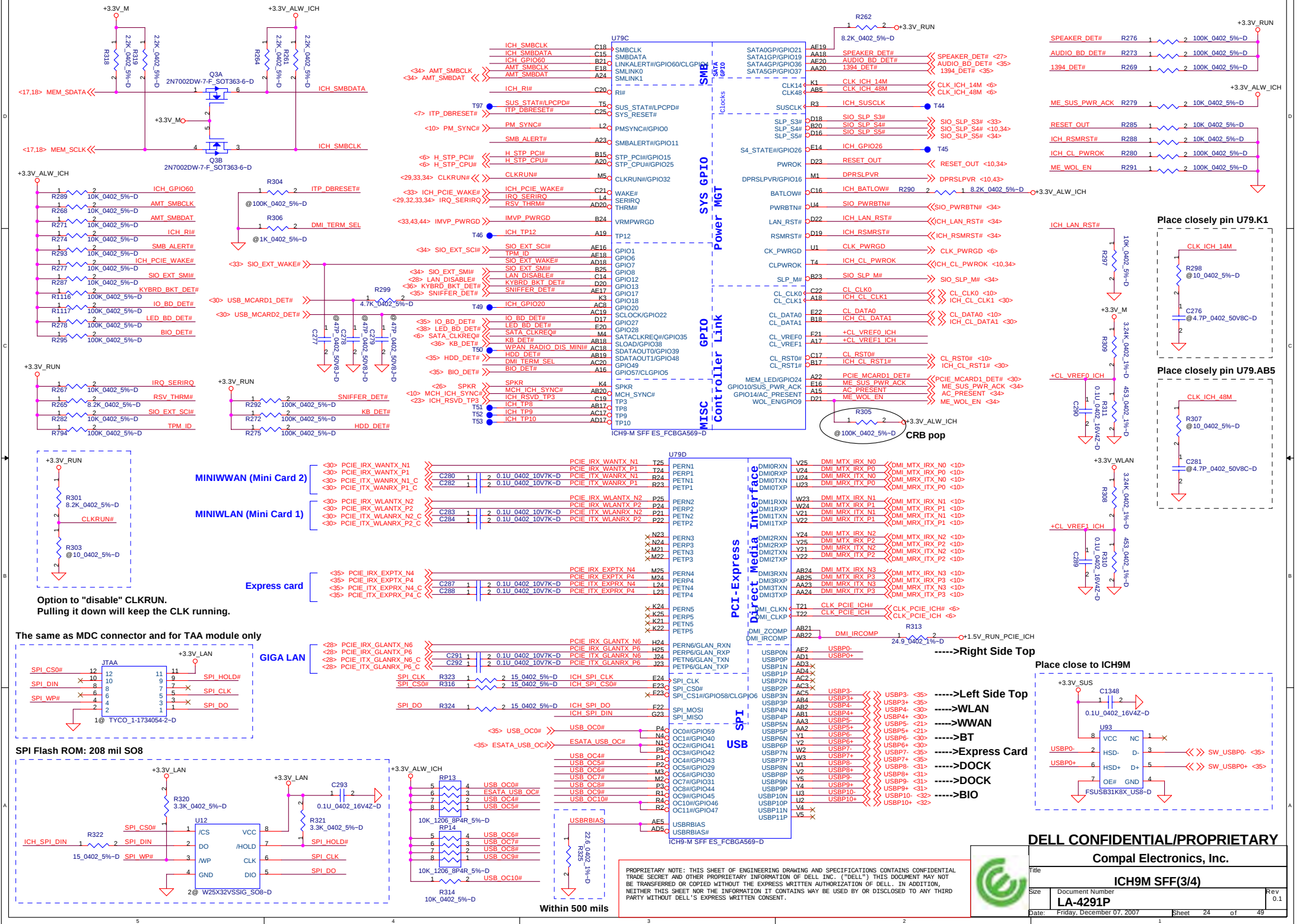


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Title		ICH9M SFF(1/4)	
Size	Document Number	LA-4291P	
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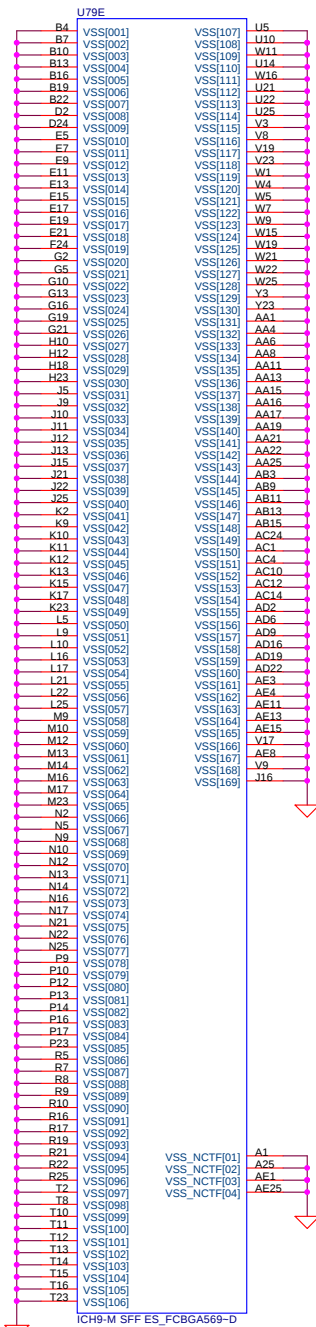
ICH9M SFF(3/4)

LA-4291P

Rev 0.1

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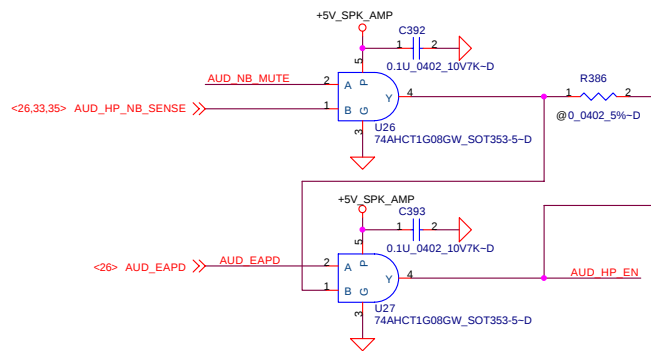
Compal Electronics, Inc.

Codec 92HD71B and I2C D/A A/D converters

size	Document Number LA 4301B	Rev 0.1
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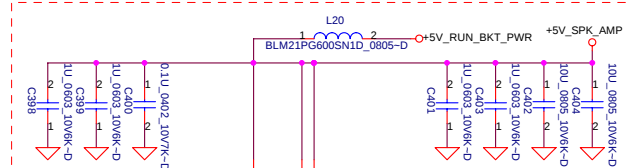
Date: Friday, December 07, 2007 Sheet 26 of 49

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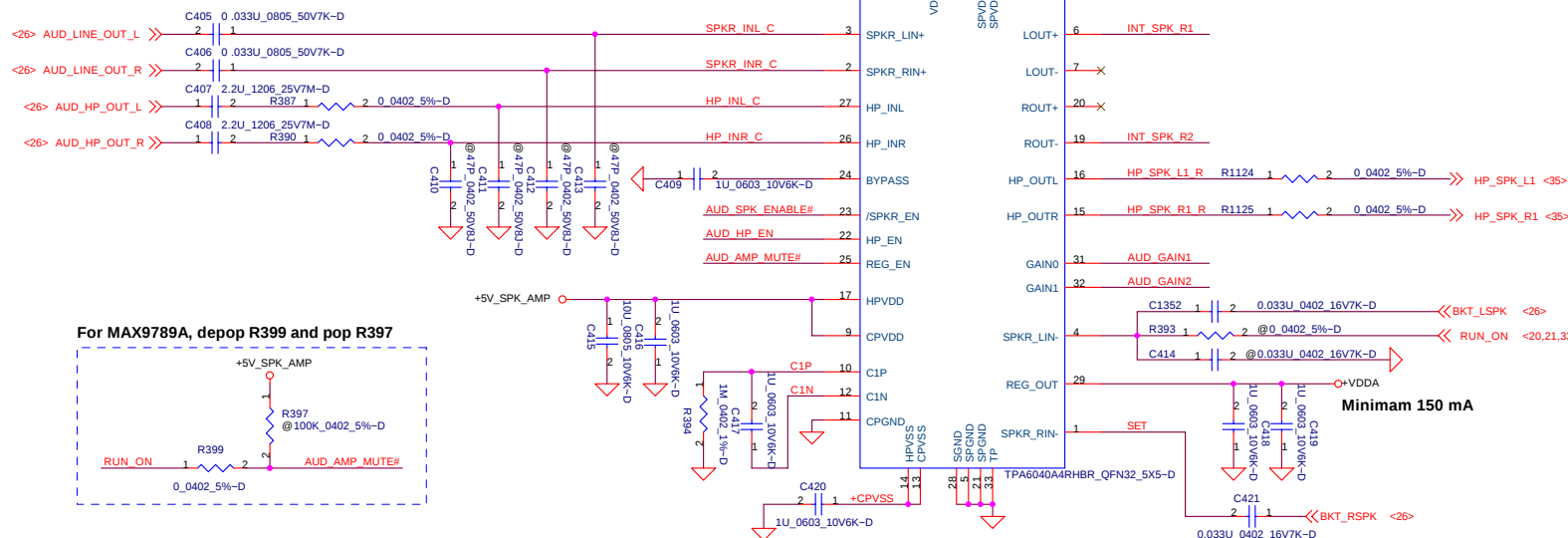
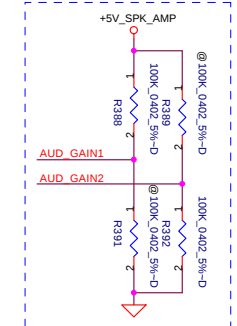


Place close to Audio Chip

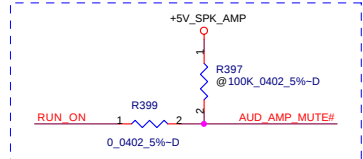
W=40mils



Gain Setting for TPA6040A4

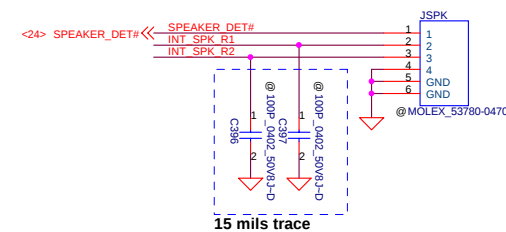


For MAX9789A, depop R399 and pop R397



GAIN1	GAIN2	AV(inv)	INPUT IMPEDANCE
0	0	6dB	82K ohm
0	1	10dB	66K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	26K ohm

Minimam 150 mA



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Audio amplifier and speaker CONN

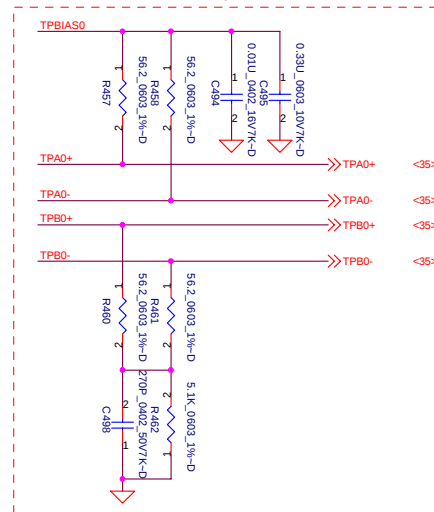
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UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-down	Pull-down	Enable SD,MMC Card

Media I/F	SD Card	MMC Card
MDIO00	SDCD#	MMCCD#
MDIO01		
MDIO02		
MDIO03	SDWP#	
MDIO04	SDPWR0	MMCPWR
MDIO05	SDPWR1	
MDIO06	SDLED#	MMCLEd#
MDIO07	SDEXTCK	
MDIO08	SDCCMD	MMCCMD
MDIO09	SDCCLK	MMCCCLK
MDIO10	SDCDAT0	MMCDAT0
MDIO11	SDCDAT1	MMCDAT1
MDIO12	SDCDAT2	MMCDAT2
MDIO13	SDCDAT3	MMCDAT3
MDIO14		MMCDAT4
MDIO15		MMCDAT5
MDIO16		MMCDAT6
MDIO17		MMCDAT7
MDIO18		
MDIO19		

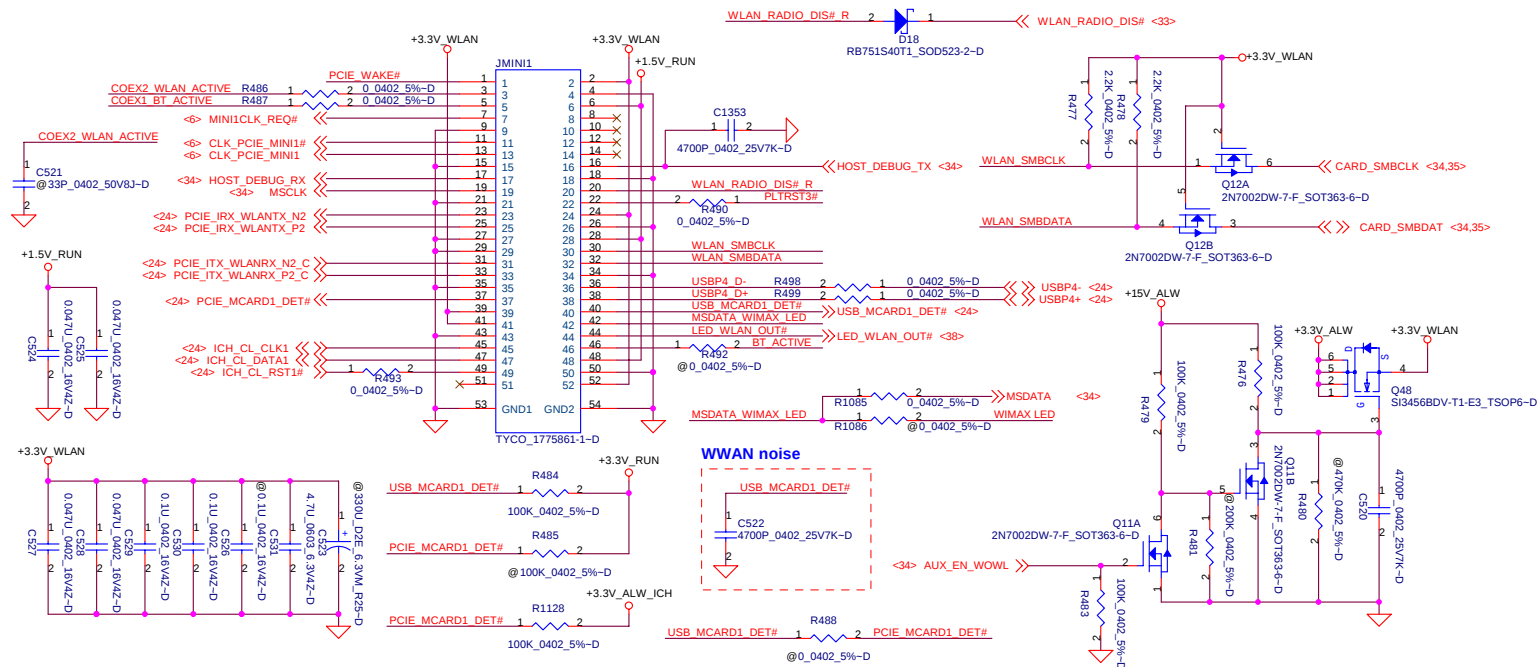


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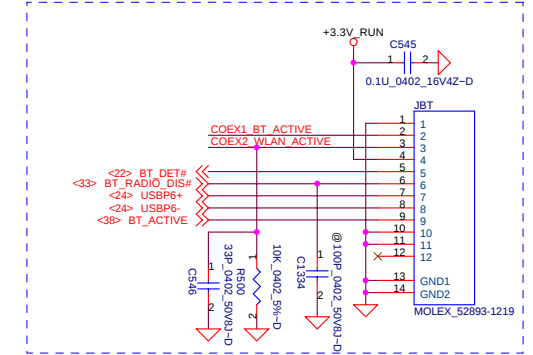


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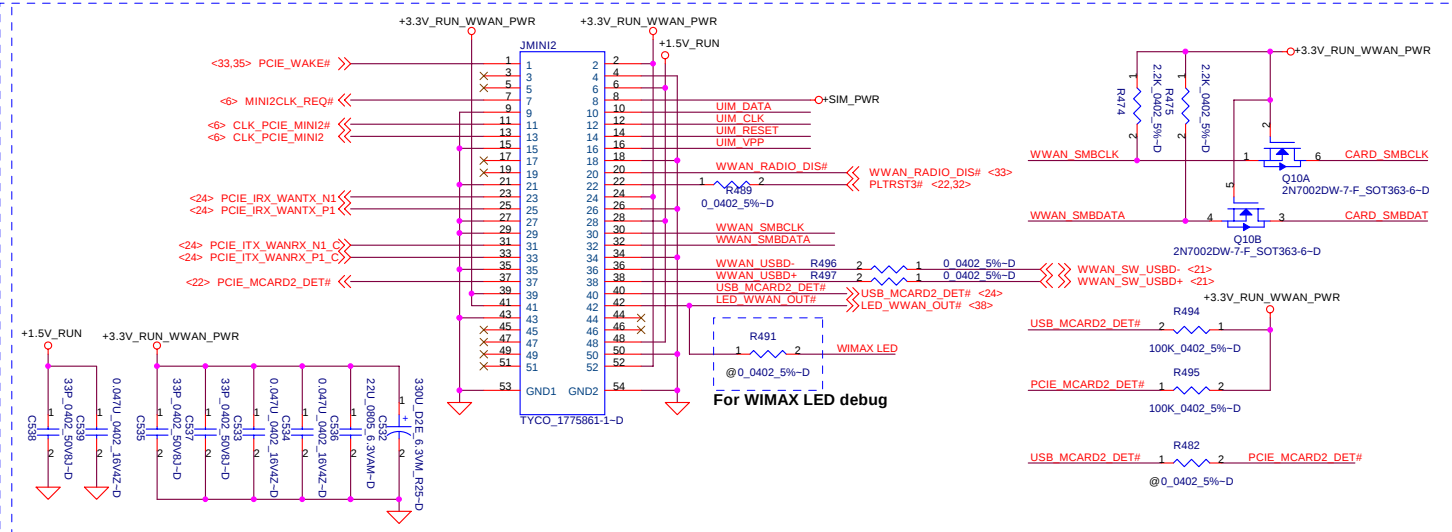
Mini Card 1---WLAN



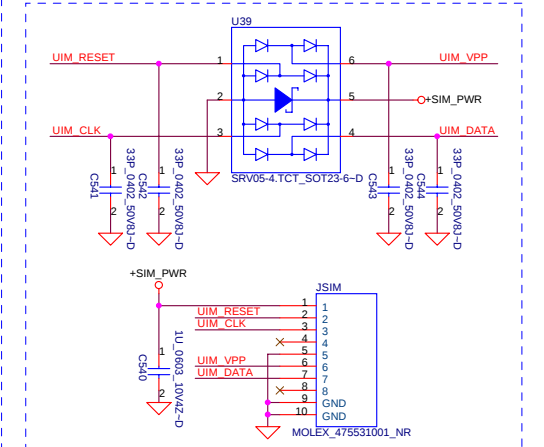
BlueTooth



Mini Card 2---WWAN



SIM Card



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Mini WLAN/WWAN, SIM card and BT

LA-4291P

Friday, December 07, 2007

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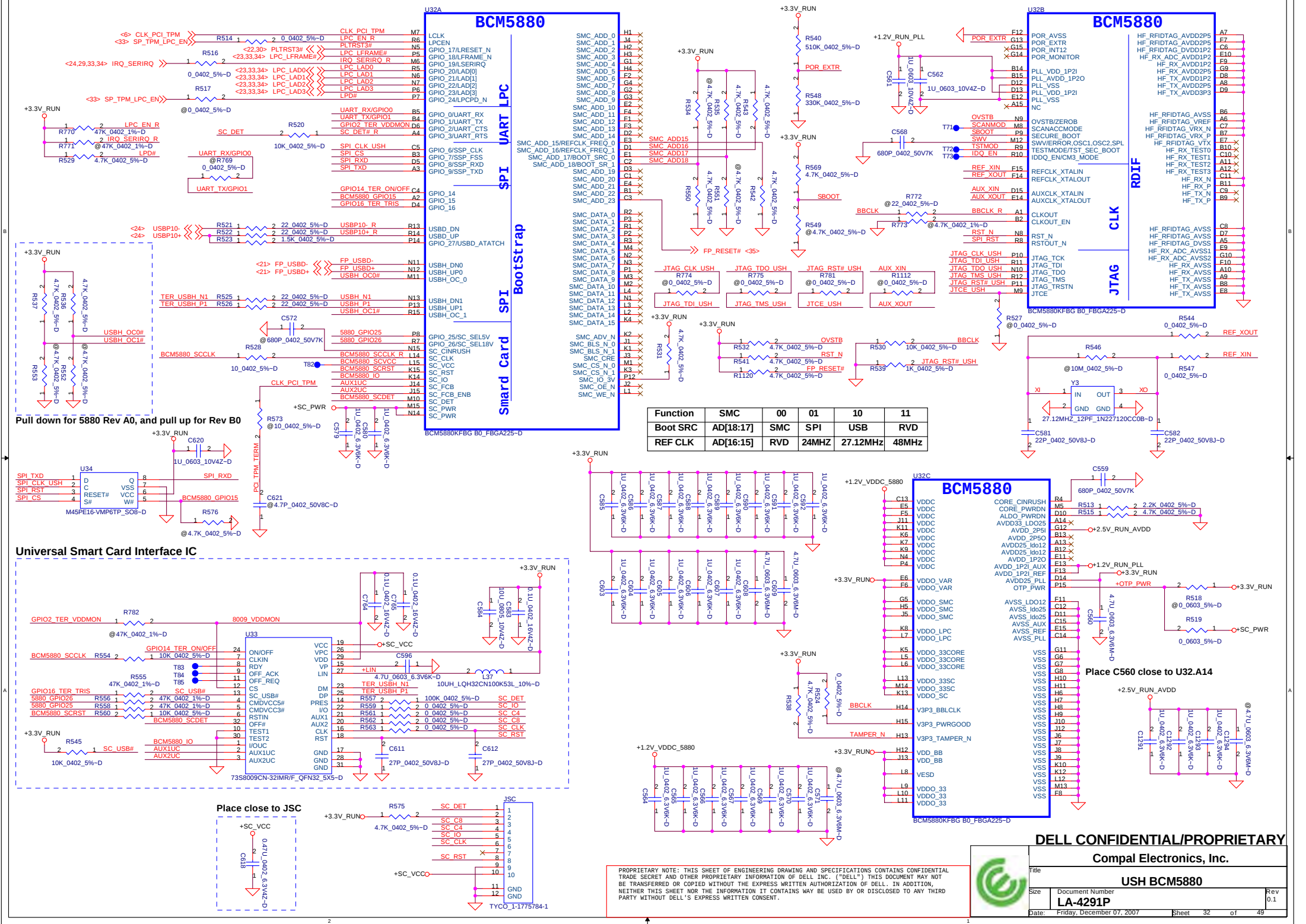
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RCLAMP0524P.TCT-D									
DPB_LANE_P0_C	1		10	DPB_LANE_P0_C					
DPB_LANE_N0_C	2		9	DPB_LANE_N0_C					
DPB_LANE_P1_C	4		7	DPB_LANE_P1_C					
DPB_LANE_N1_C	5		6	DPB_LANE_N1_C					
	3								
	8								
RCLAMP0524P.TCT-D									
DPB_LANE_P2_C	1		10	DPB_LANE_P2_C					
DPB_LANE_N2_C	2		9	DPB_LANE_N2_C					
DPB_LANE_P3_C	4		7	DPB_LANE_P3_C					
DPB_LANE_N3_C	5		6	DPB_LANE_N3_C					
	3								
	8								
RCLAMP0524P.TCT-D									
SDVO_CTRLCLK	1		10	SDVO_CTRLCLK					
SDVO_CTRLDATA	2		9	SDVO_CTRLDATA					
DPB_DOCK_HPD	4		7	DPB_DOCK_HPD					
DPB_CA_DET	5		6	DPB_CA_DET					
	3								
	8								
RCLAMP0524P.TCT-D									
DPC_LANE_P0_C	1		10	DPC_LANE_P0_C					
DPC_LANE_N0_C	2		9	DPC_LANE_N0_C					
DPC_LANE_P1_C	4		7	DPC_LANE_P1_C					
DPC_LANE_N1_C	5		6	DPC_LANE_N1_C					
	3								
	8								
RCLAMP0524P.TCT-D									
DPC_LANE_P2_C	1		10	DPC_LANE_P2_C					
DPC_LANE_N2_C	2		9	DPC_LANE_N2_C					
DPC_LANE_P3_C	4		7	DPC_LANE_P3_C					
DPC_LANE_N3_C	5		6	DPC_LANE_N3_C					
	3								
	8								
RCLAMP0524P.TCT-D									
DDPC_CTRLCLK	1		10	DDPC_CTRLCLK					
DDPC_CTRLDATA	2		9	DDPC_CTRLDATA					
DPC_DOCK_HPD	4		7	DPC_DOCK_HPD					
DPC_CA_DET	5		6	DPC_CA_DET					
	3								
	8								
RCLAMP0524P.TCT-D									



The diagram shows the electrical connection for the DPC Dock HPD signal. A diode (Q49, BSS138_SOT23-D) is connected between the DPC_DOCK_HP# pin (pin 2) and the +3.3V_RUN supply. The signal path includes a 7.5K_0402_5%-D resistor (R502) and a 100K_0402_5%-D resistor (R503) to ground. The signal is labeled DPC_DOCK_HP# <12>.

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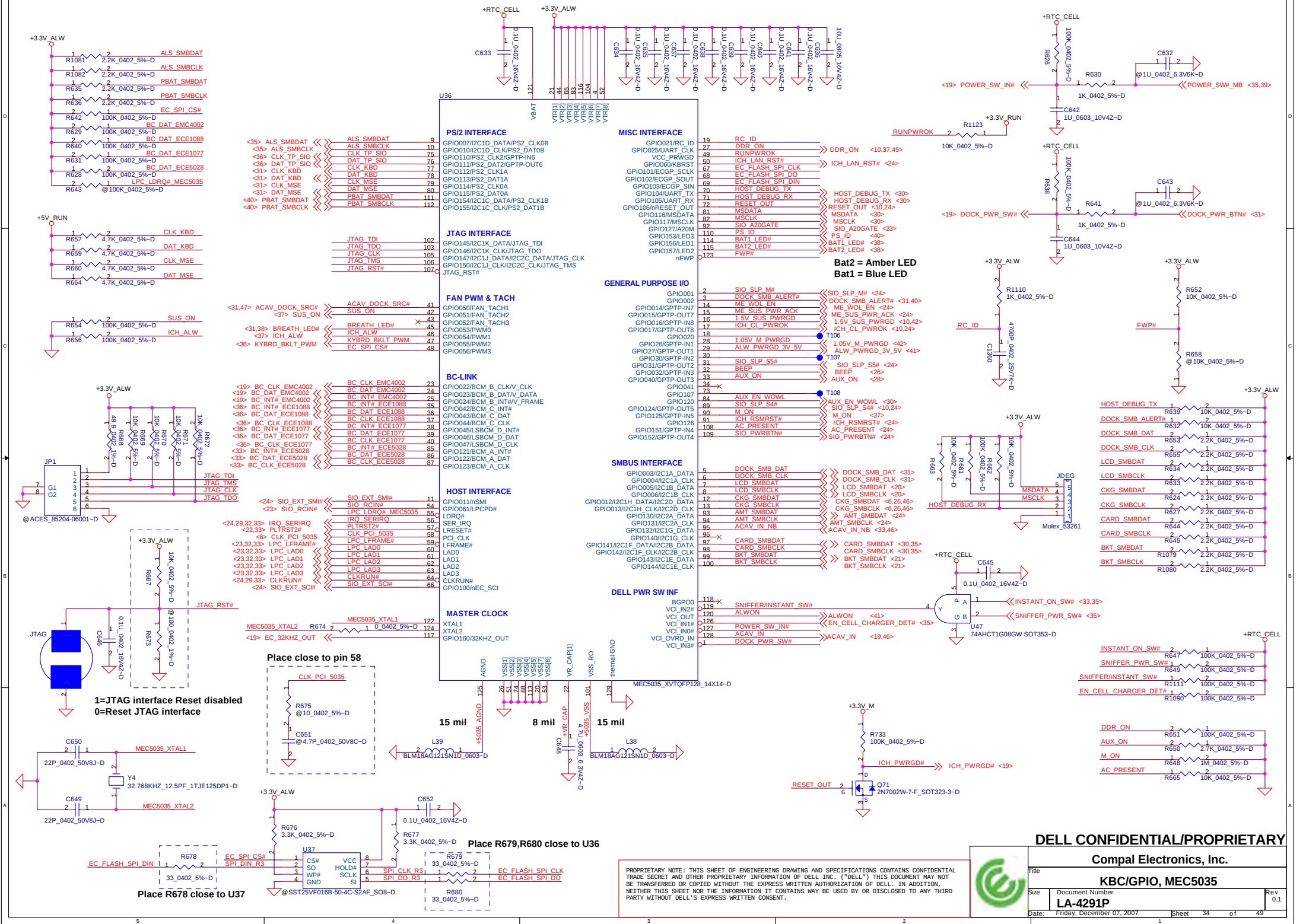
USH BCM5880

LA-4291P

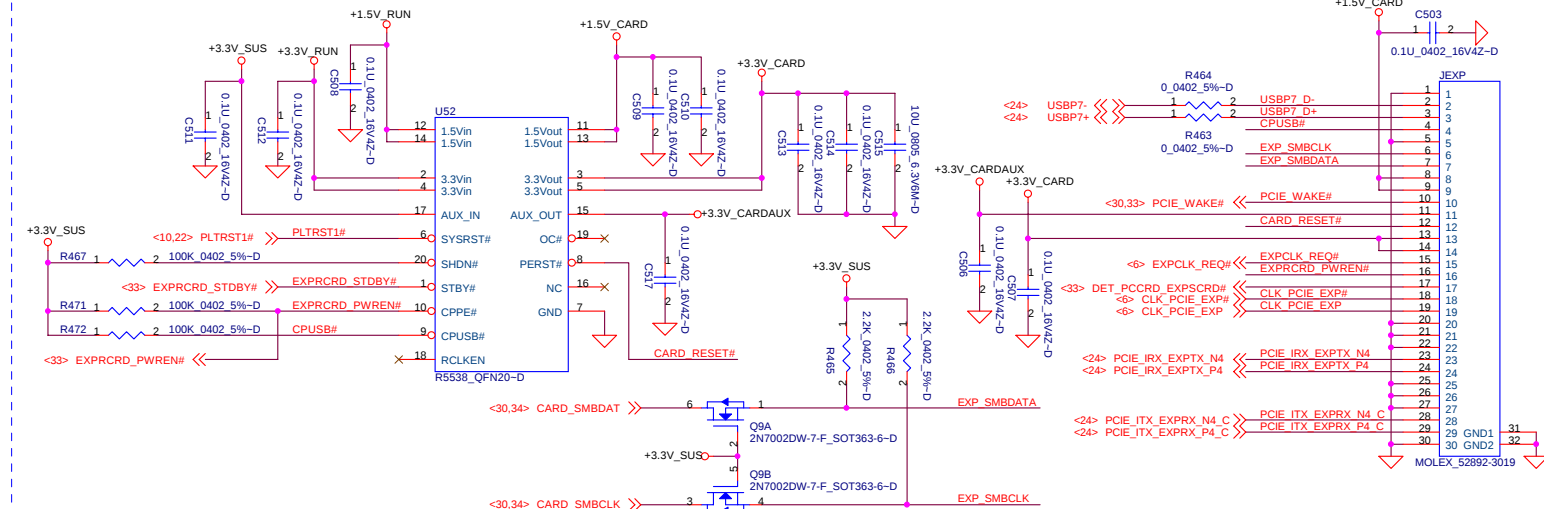
Friday, December 07, 2007

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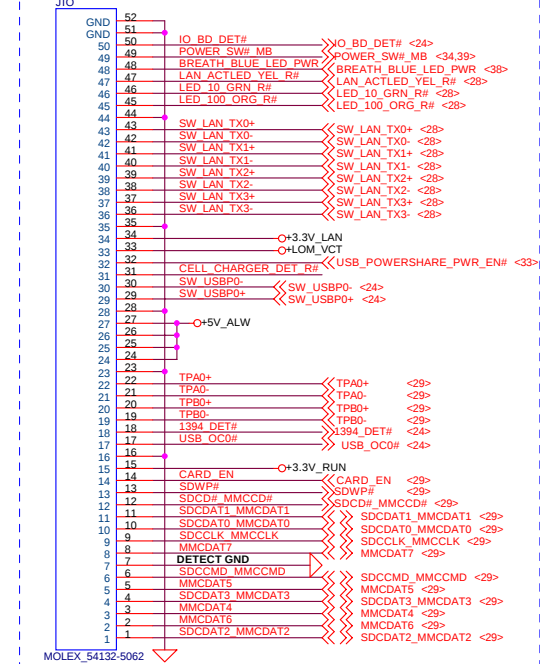




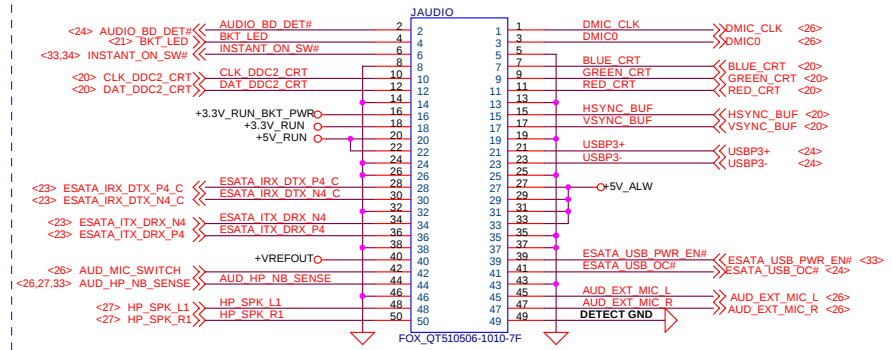
Express Card



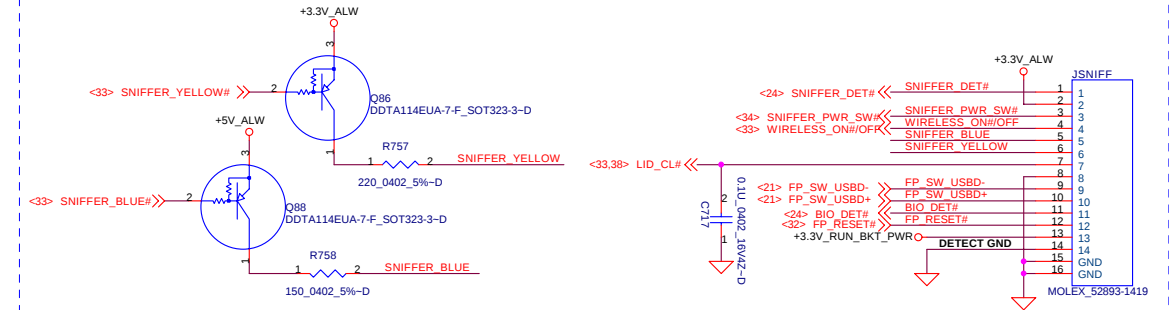
I/O/B connector, Right side



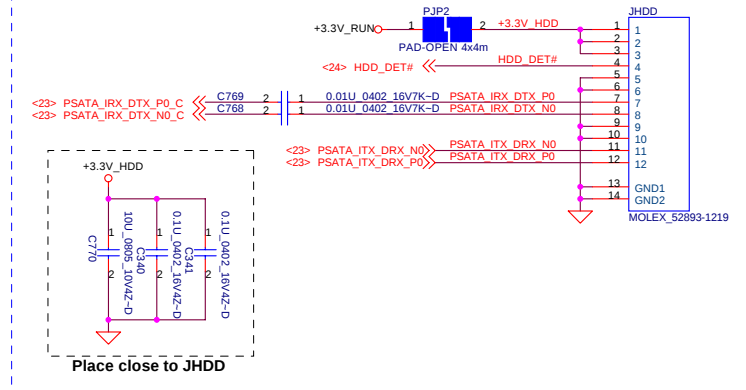
AUDIO/B BTB connector, Left side



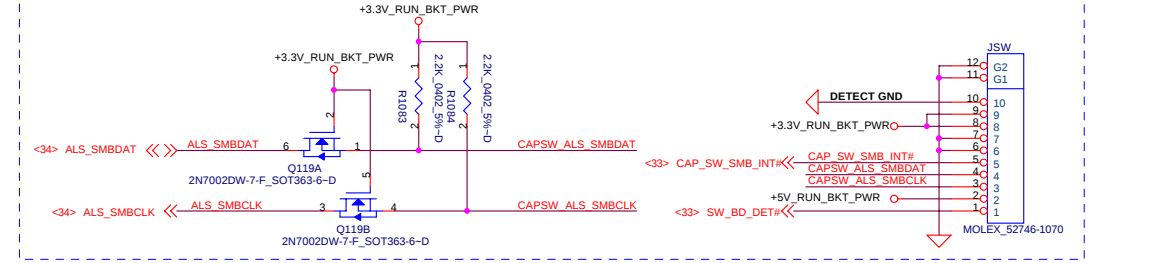
SNIFLER connector and LED



1.8" Micro SATA HDD connector



CAP Switch and ALS connector



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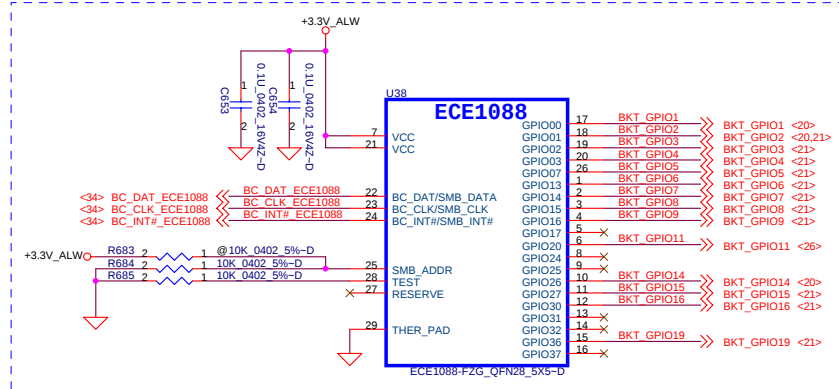
Compal Electronics, Inc.



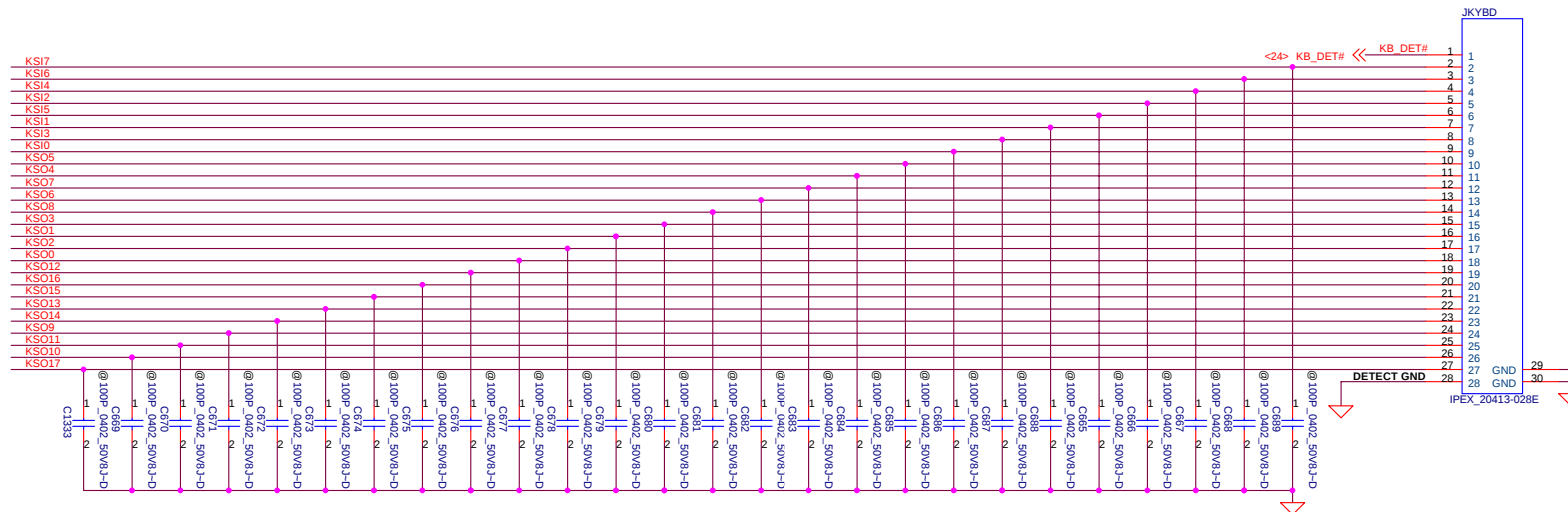
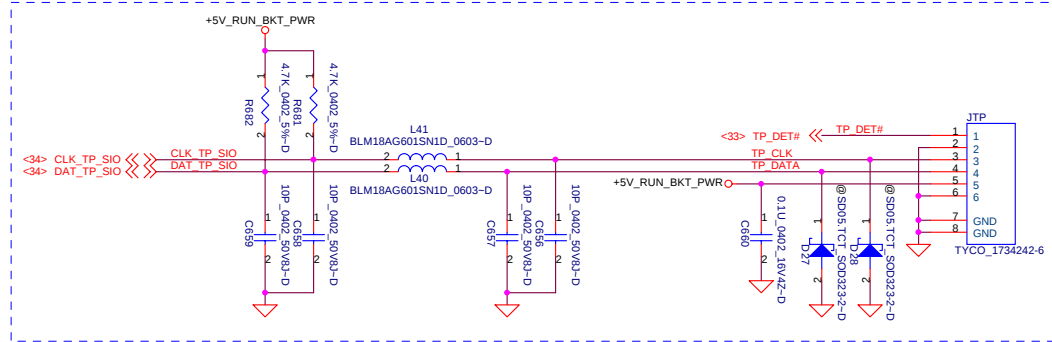
Express Card, HDD, Sniffer, IO CONN
LA-4291P

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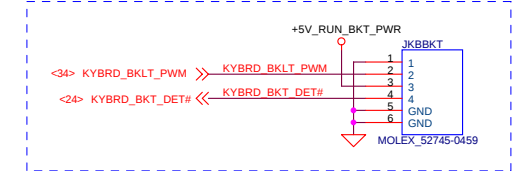
GPIO Expander for BlackTop



Touch Pad connector



Keyboard Backlight connector



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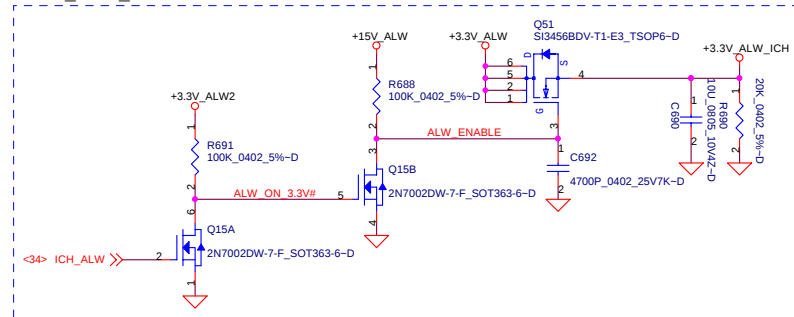
Compal Electronics, Inc.



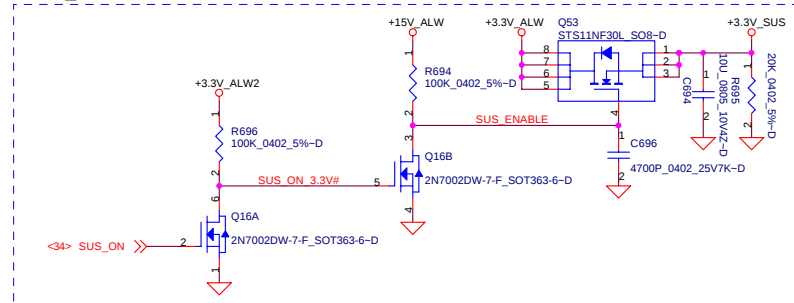
Title: Keyboard, TouchPad and GPIO expander
Size: Document Number
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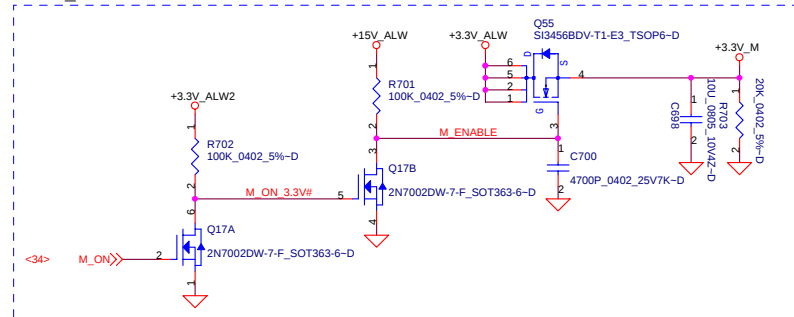
+3.3V_ALW_ICH Source



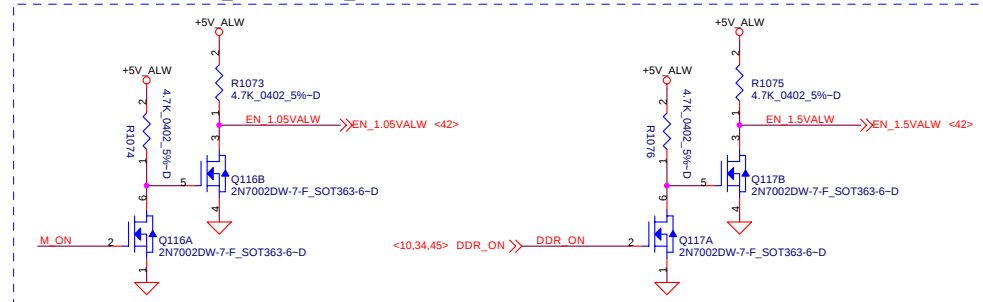
+3.3V_SUS Source



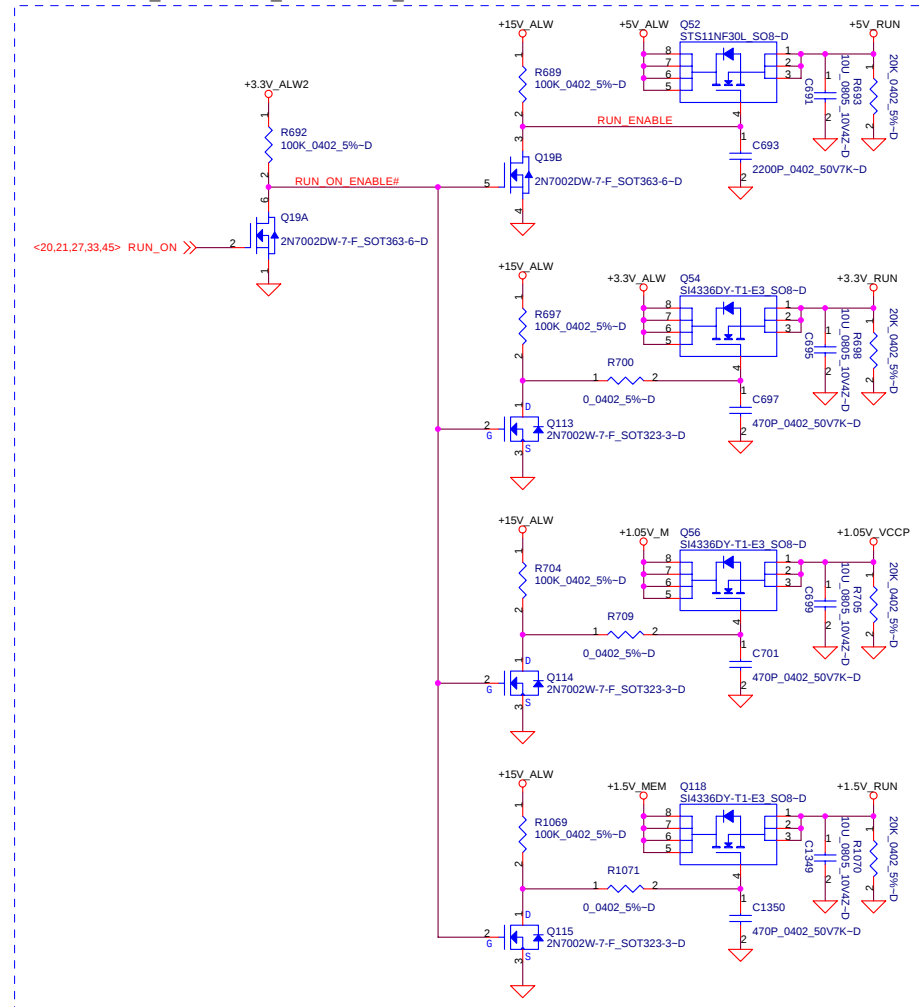
+3.3V_M Source



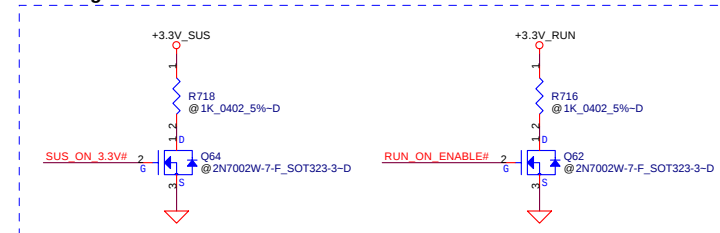
Level shifter for +1.05V_M and +1.5V_MEM PWM IC



+5V_RUN/+3.3V_RUN/+1.05V_VCCP/+1.5V_RUN Source



Discharg Circuit



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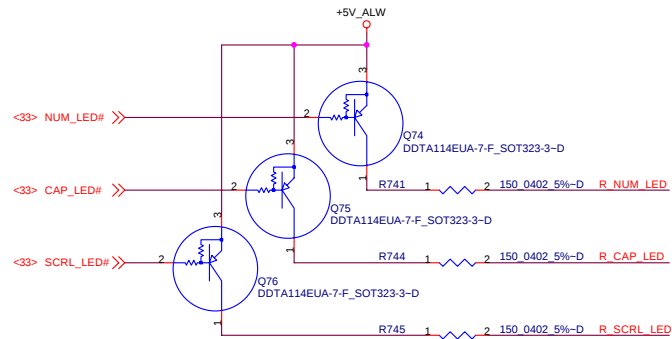
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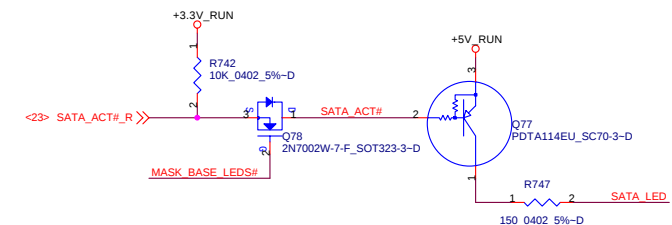
POWER CONTROL

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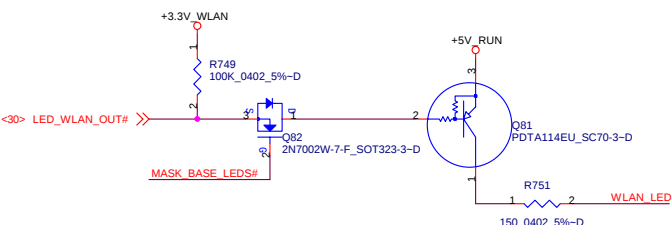
Keyboard Status, Num Lock/Caps Lock/Scroll Lock LEDs



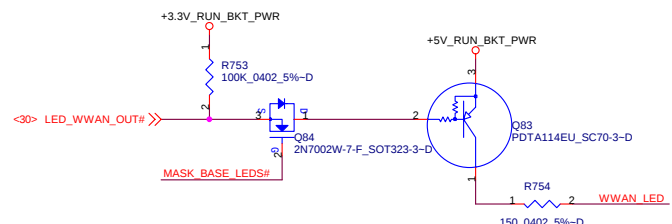
HDD LED



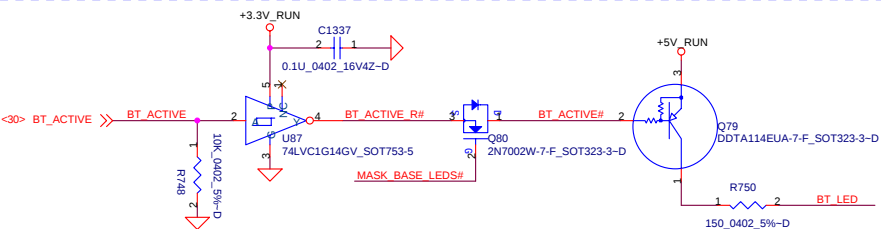
WLAN LED



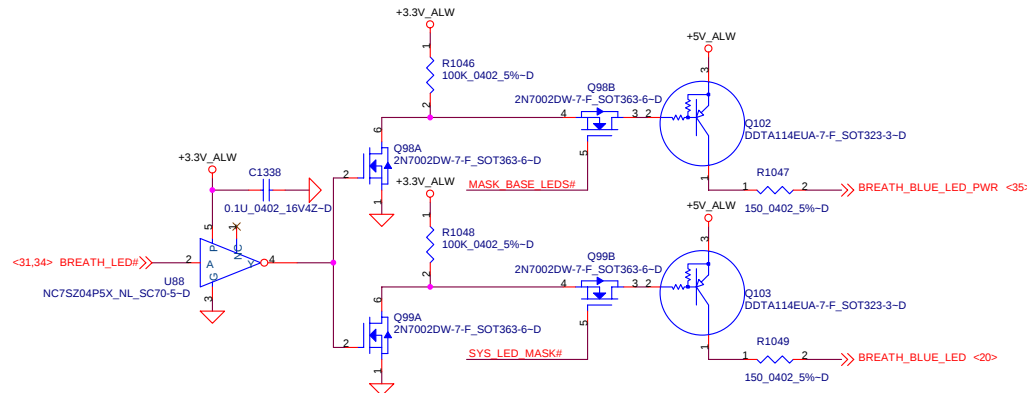
WWAN LED



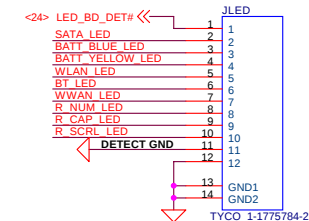
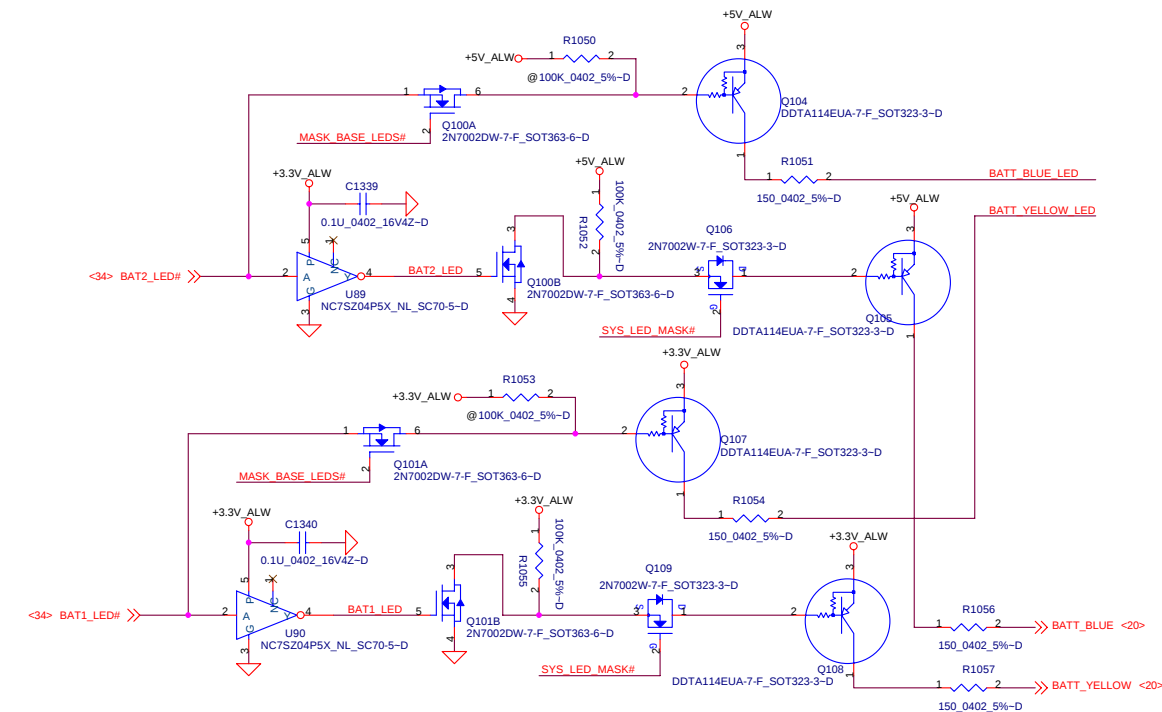
BLUETOOTH LED



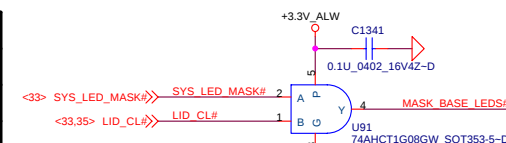
POWER/SUSPEND breathing LED



BATTERY LED



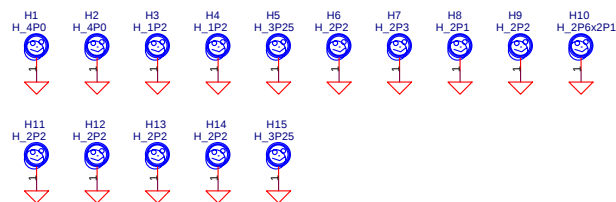
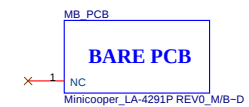
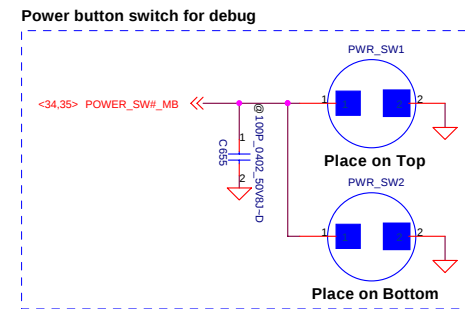
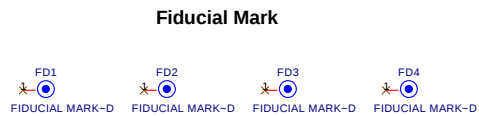
LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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System LEDs Control	
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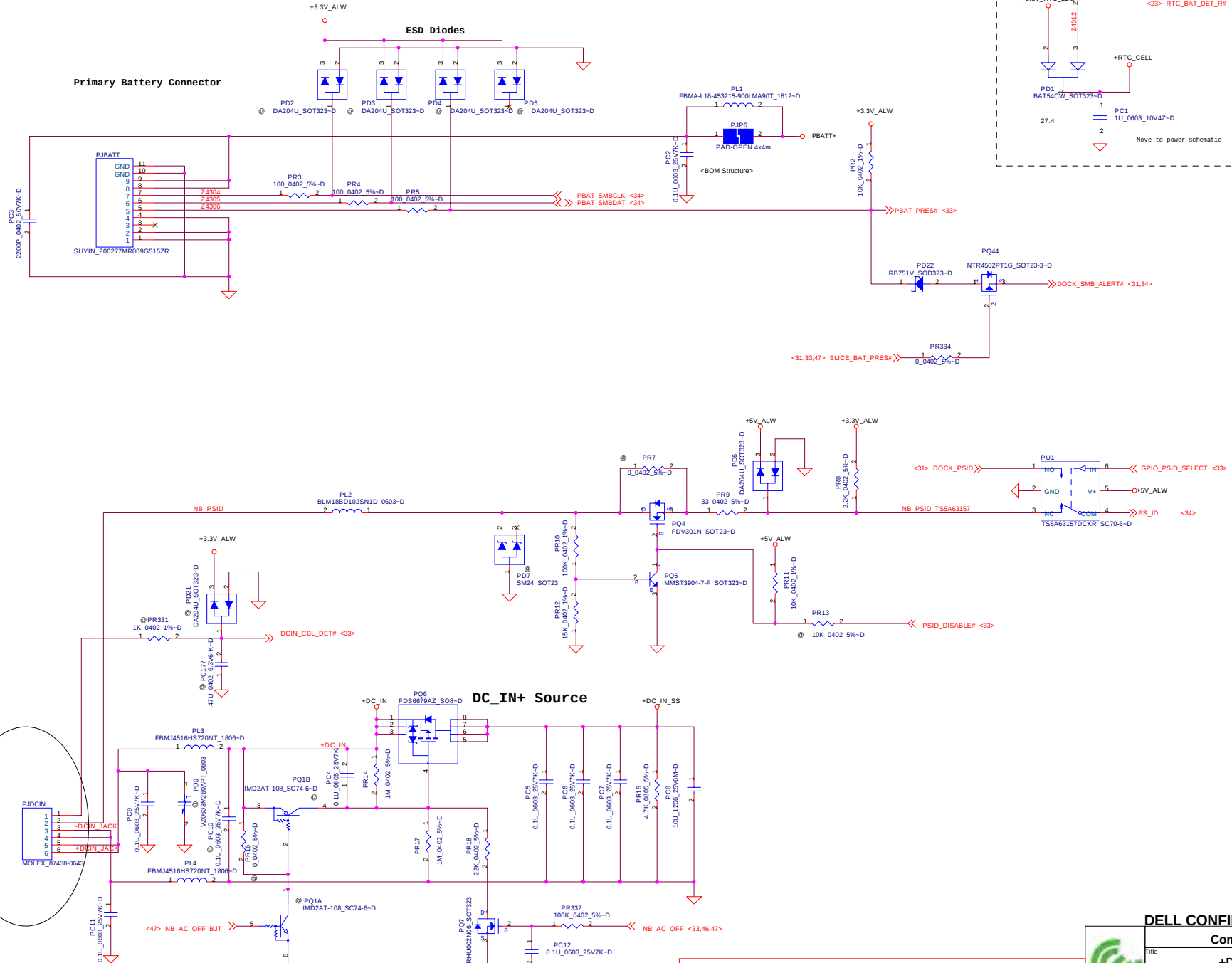
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Primary Battery Connector

ESD Diodes

COIN RTC Battery



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+DCIN

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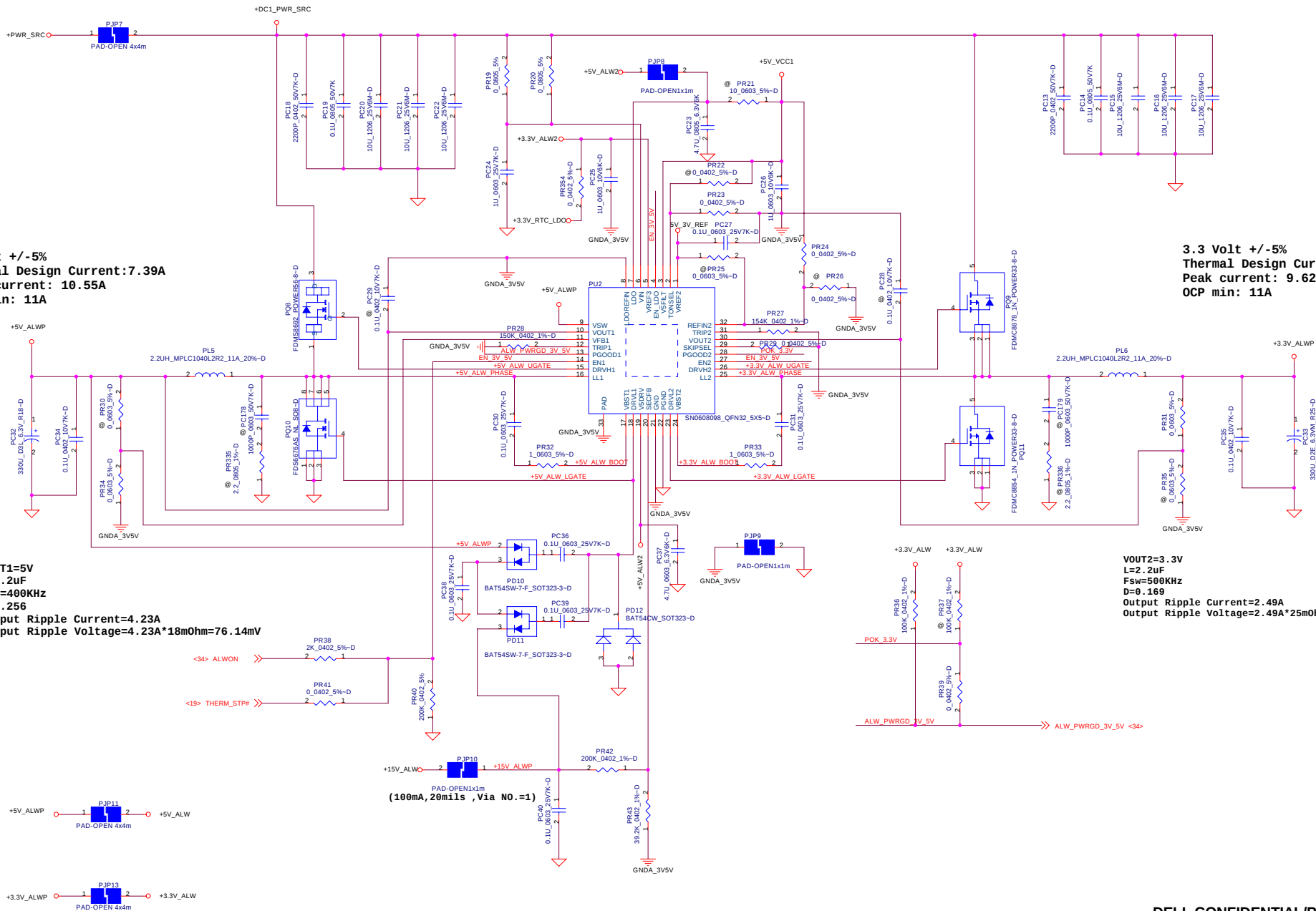
+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP

5 Volt +/-5%
Thermal Design Current:7.39A
Peck current: 10.55A
OCP min: 11A

3.3 Volt +/-5%
Thermal Design Current: 6.73A
Peak current: 9.62A
OCP min: 11A

VOUT1=5V
L=2.2uF
Fsw=400KHz
D=0.256
Output Ripple Current=4.23A
Output Ripple Voltage=4.23A*18mOhm=76.14mV

VOUT2=3.3V
L=2.2uF
Fsw=500KHz
D=0.169
Output Ripple Current=2.49A
Output Ripple Voltage=2.49A*25mOhm=62.25mV



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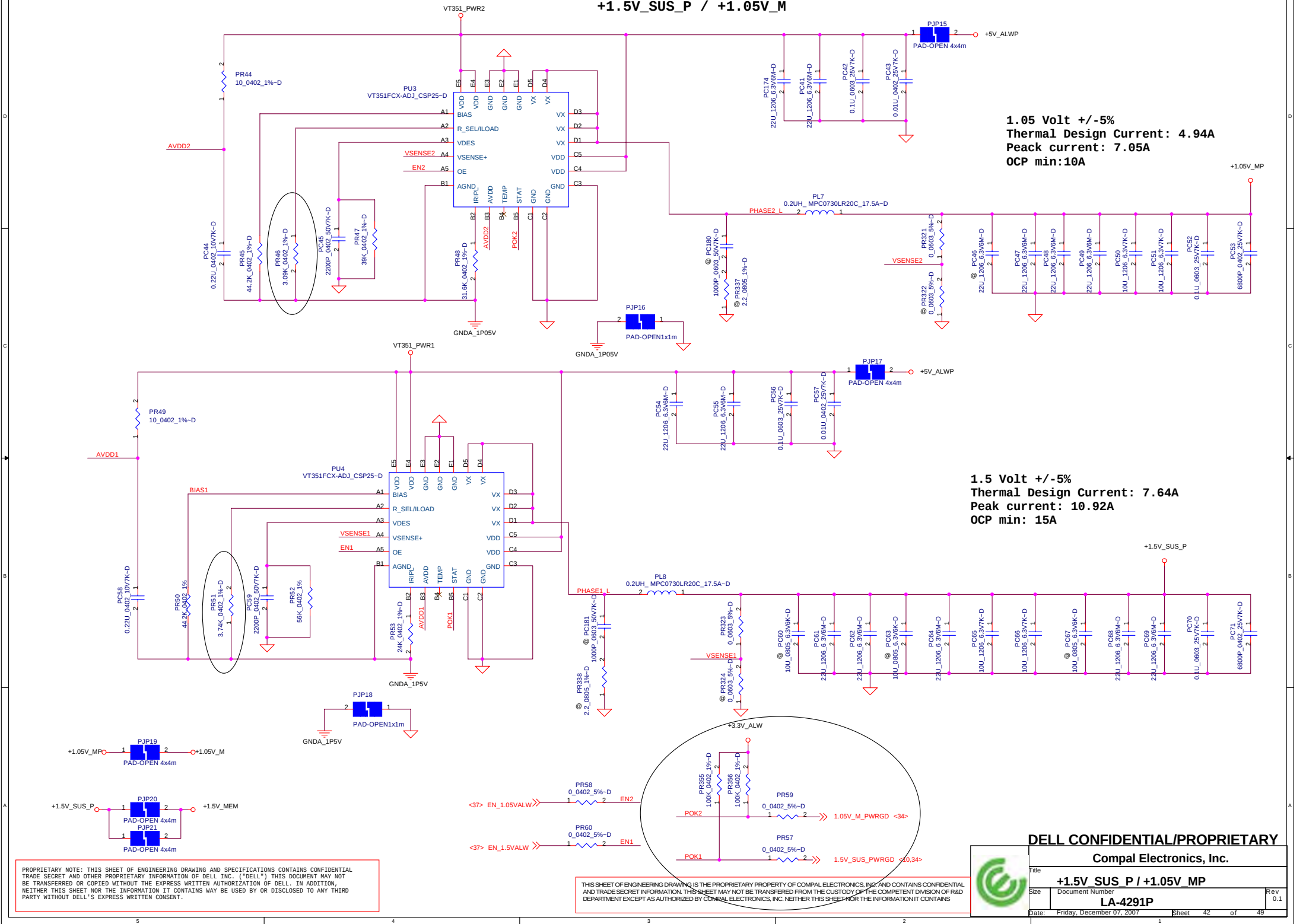
DC/DC +3V/+5V

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+1.5V_SUS_P / +1.05V_M



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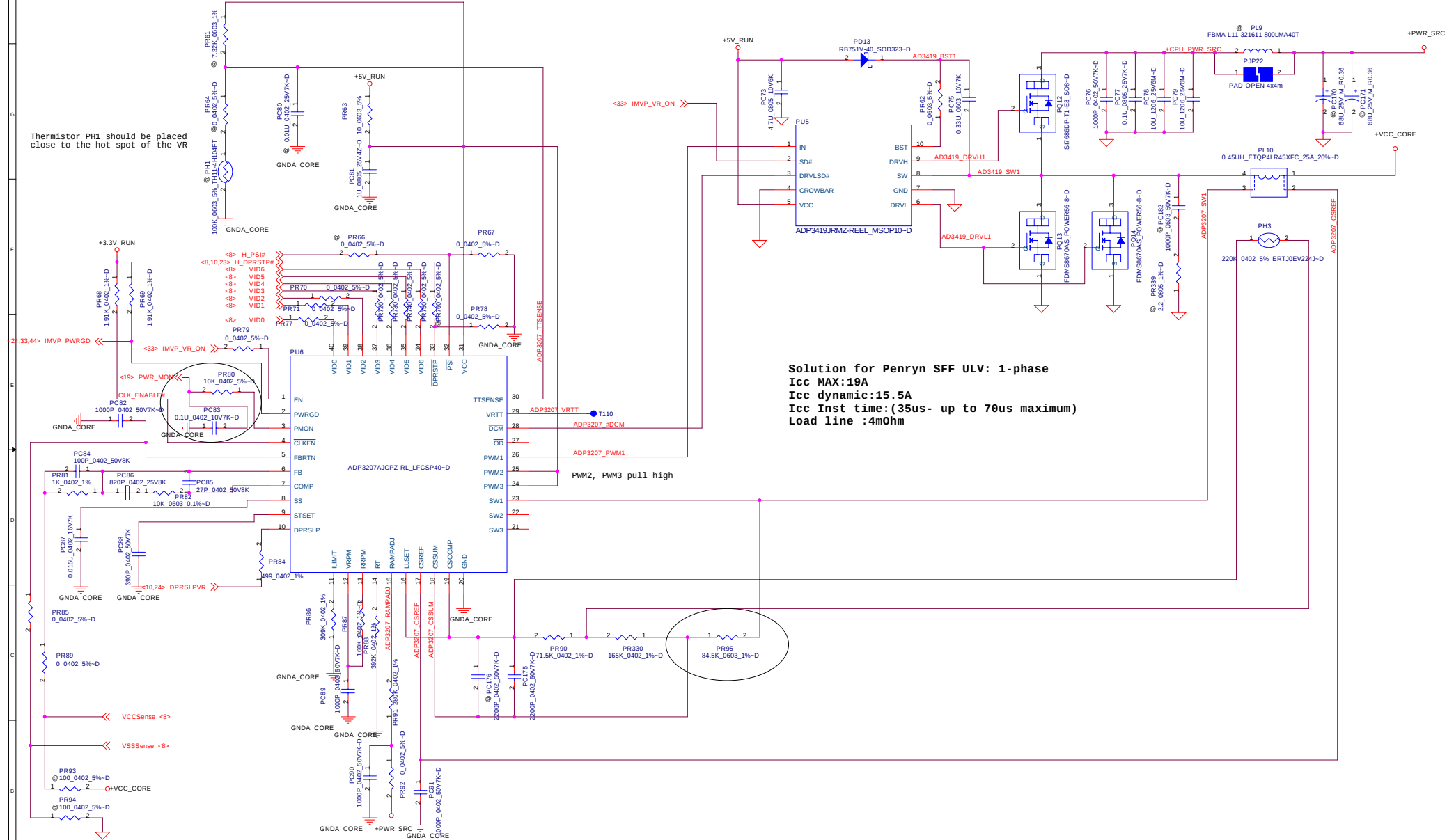
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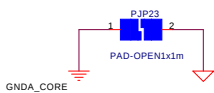
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Thermistor PH1 should be placed close to the hot spot of the VR



Solution for Penryn SFF ULV: 1-phase
Icc MAX:19A
Icc dynamic:15.5A
Icc Inst time:(35us- up to 70us maximum)
Load line :4m0hm

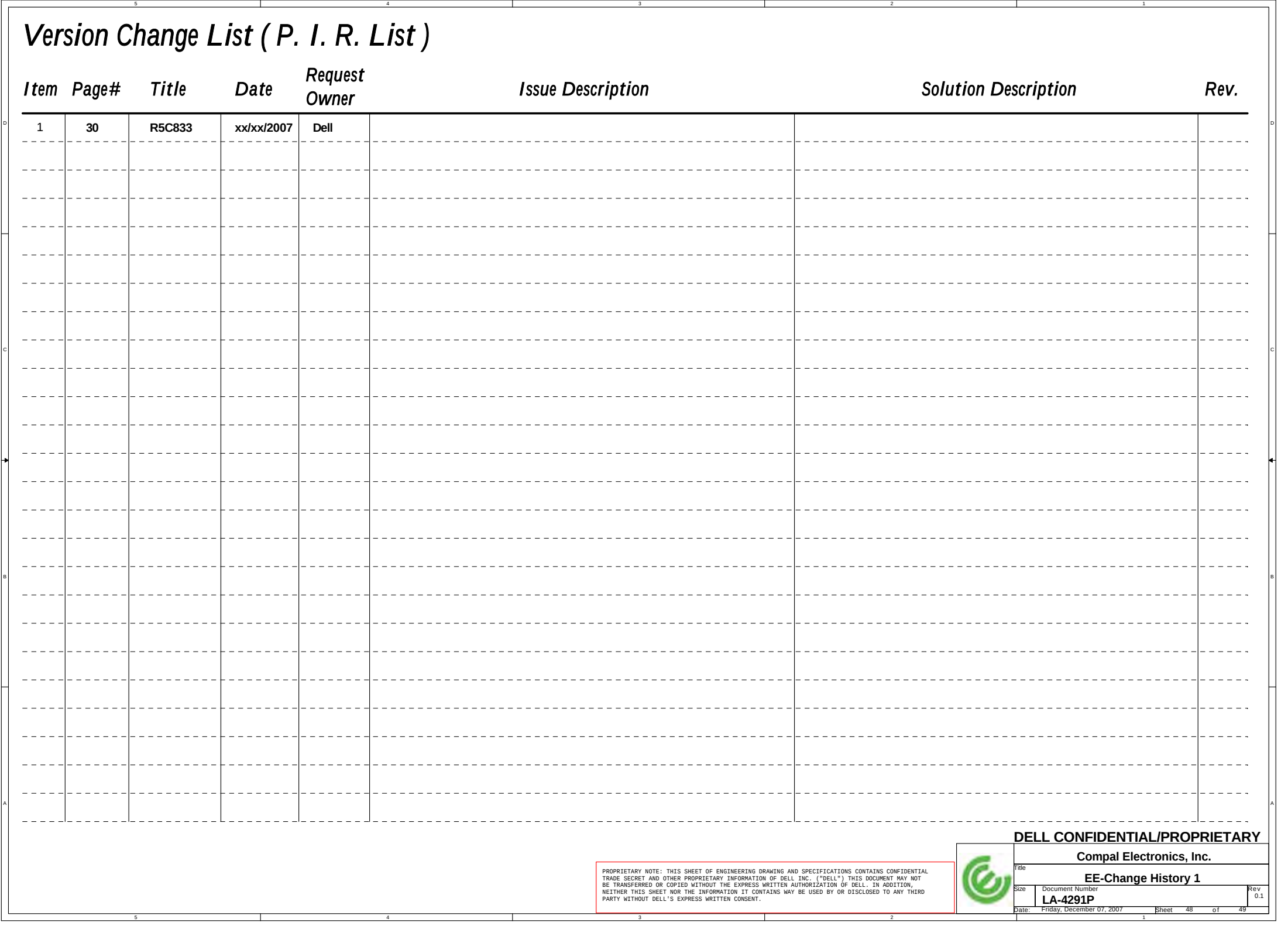
NOTE: (Connection VCCORE output Cap GND)
 De-populate PR93 and PR94 when CPU is present



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