COMPAL CONFIDENTIAL

MODEL NAME : ***IBQ00***

PCB NO : ***LA-3302P (DAA00000K0L)***

BOM P/N : ***45144731L01***

M08 (DIS) Briscoe

uFCPGA Mobile Merom
Intel Crestline + ICH8M

2007-03-07

REV : 0.4 (X03)

@ : Nopop Component
1@ : Populate for G72MV
2@ : Populate for G86MV
45144731L01 pop for G86MV
45144XXXXX pop for G72MV

MB PCB

Part Number	Description
DAA00000K0L	PCB ZGX LA-3302P REV0 M/B DIS

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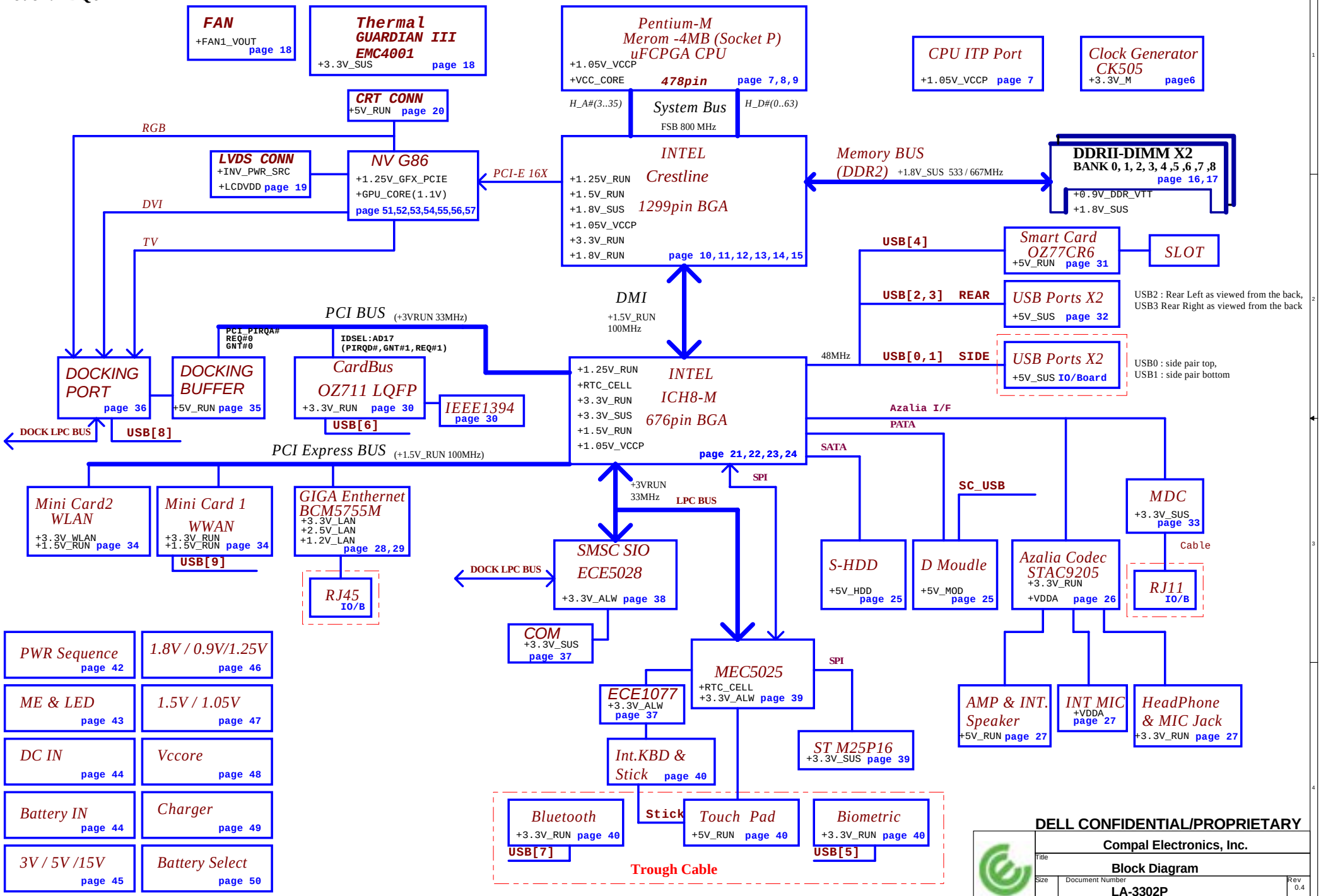
Title: Cover Sheet

Size | Document Number: LA-3302P | Rev: 0.4

Date: Wednesday, March 07, 2007 | Sheet 1 of 66

Block Diagram
Compal confidential
Model : IBQ01



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Title: Block Diagram		
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW +3.3V_RTC_LDO	+5V_SUS +3.3V_SUS +1.8V_SUS	+5V_RUN +3.3V_RUN +2.5V_RUN +1.8V_RUN +1.5V_RUN +VCC_+1P2V_GPU_CORE +0.9V_DDR_VTT +GPU_CORE +VCC_CORE +1.05V_VCCP	+3.3V_M +1.25V_M +1.05V_M	+1.25V_M +3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
OZ711	AD17	REQ#1 / GNT#1	PIRQD
Docking	AD24	REQ#0 / GNT#0	PIRQA

	USB PORT#	DESTINATION
ICH8-M	0	Side Top
	1	Side Bottom
	2	Rear Left
	3	Rear Right
	4	Smart Card
	5	Biometric
	6	Card Bus
	7	Bluetooth
	8	Docking
	9	WWAN
ECE 5028	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	GIGA LAN

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Title: Index and Config.
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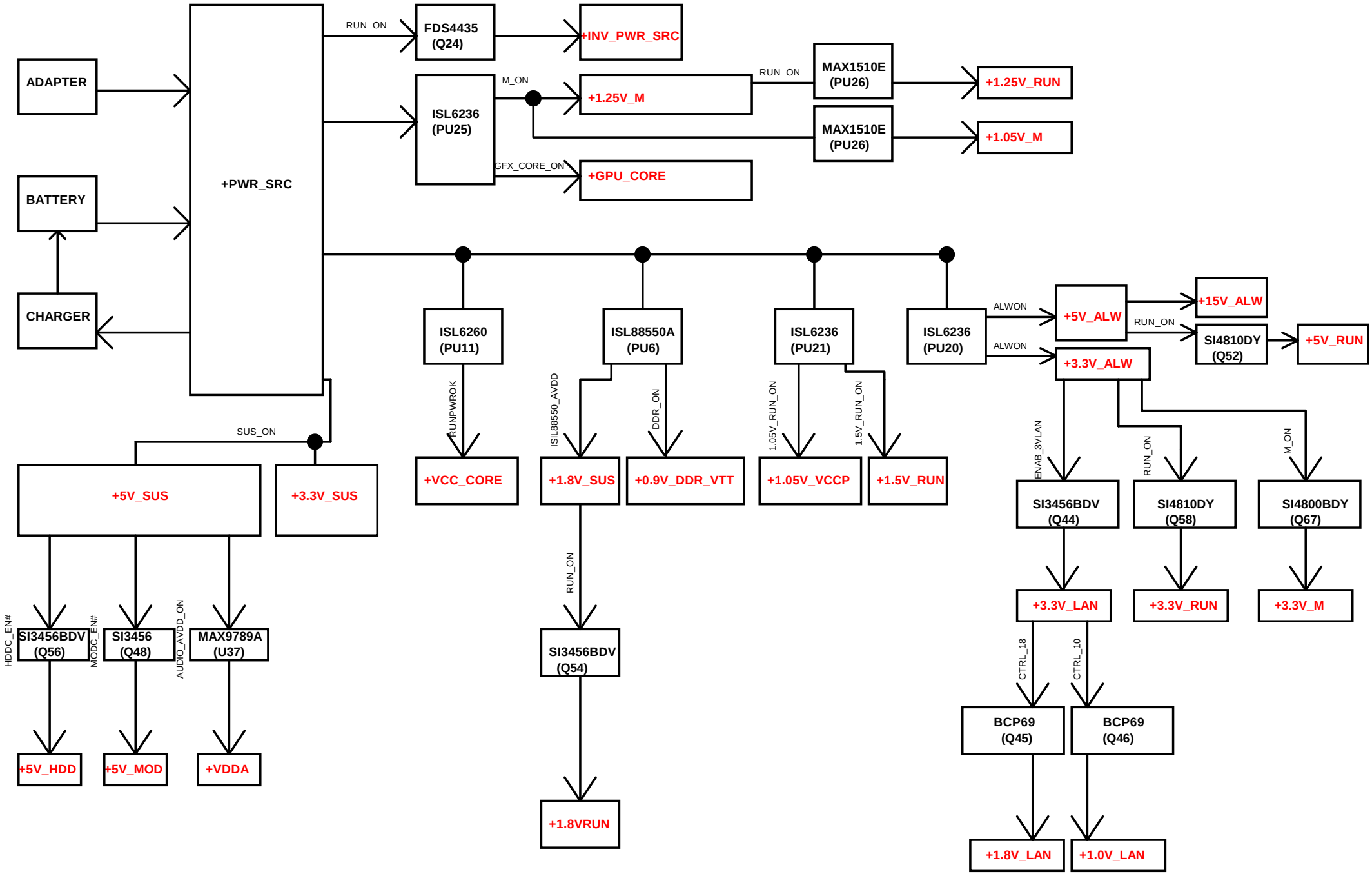

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Title: Power Rail

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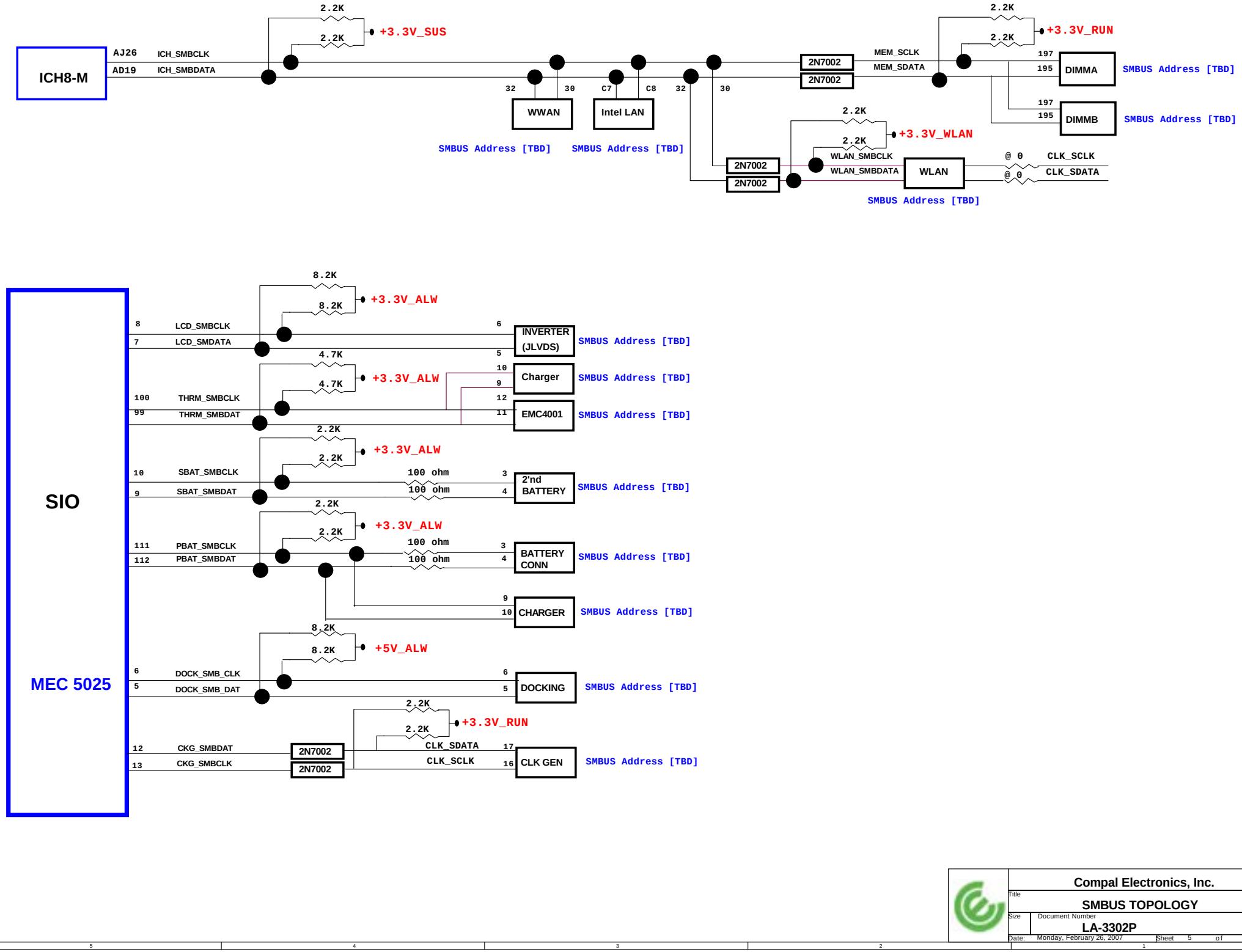
Date: Monday, February 26, 2007 | Sheet 4 of 66



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Title: SMBUS TOPOLOGY

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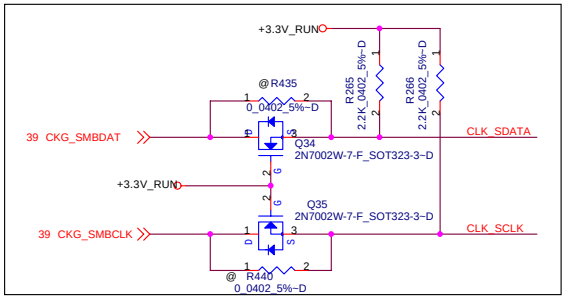
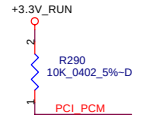
Date: Monday, February 26, 2007 | Sheet 5 of 66

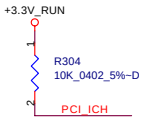


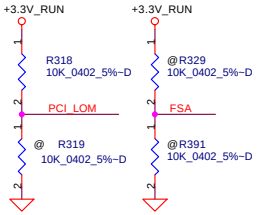
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
* 0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1	200	100	33.3

Table : ICS954305AK

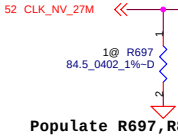
CPU_BSEL	CPU_BSEL2(FSC)	CPU_BSEL1(FSB)
133	0	0
166	0	1







0=UMA
1=Disc. GRFX down



Populate R697,R833 for G72MV
Populate R286 for G86MV.
R833,R286 place overlap

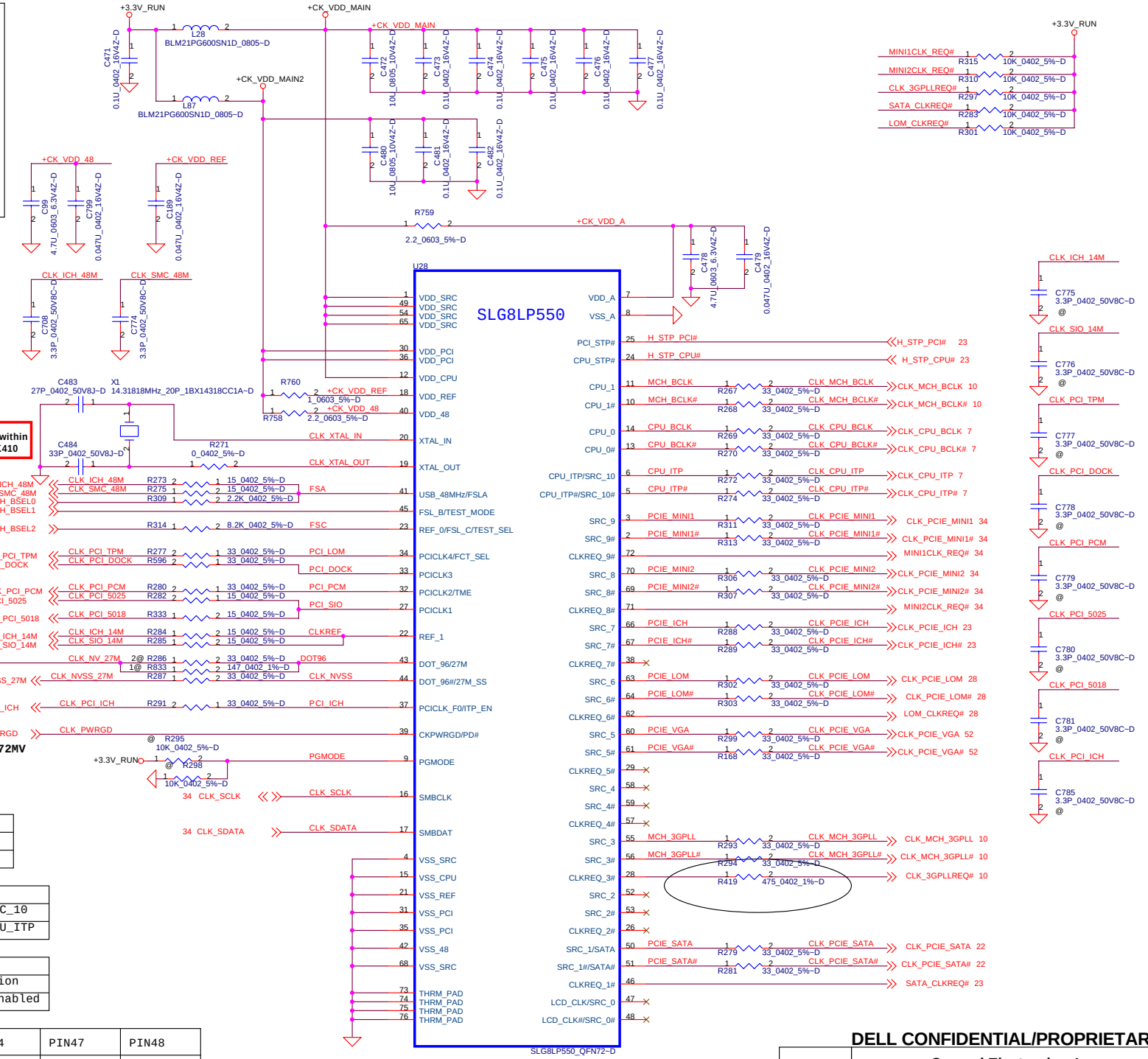
PGMODE	PIN 9
0	VTT_PWRGD#/PD
1	CKPWRGD/PD#

ITP_EN	PIN 37
0	Pin 5/6 as SRC_10
* 1	Pin 5/6 as CPU_ITP

TME	PIN 32
0	Normal Operation
* 1	Trusted Mode Enabled

FCTSEL1	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
* 1=DIS	27M_out	27M SSout	SRCT0	SRCC0

Place crystal within 500 mils of CK410



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Title: Clock Generator

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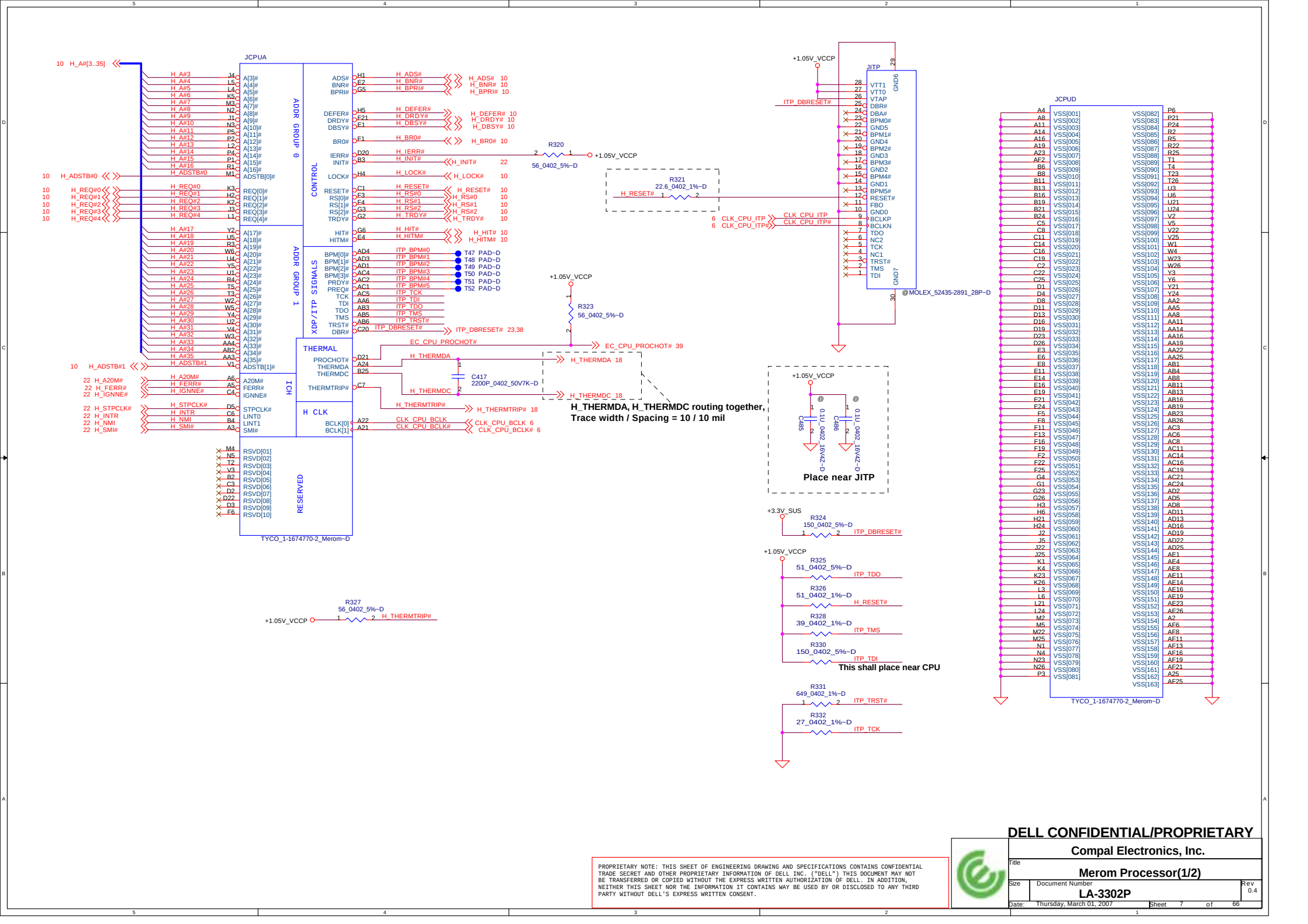
JCPUA
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
ICH
H_CLK
RESERVED
TYCO_1-1674770-2_Merom-D
JITP
@MOLEX_52435-2891_28P-D
JCPUD
TYCO_1-1674770-2_Merom-D
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil
Place near JITP
This shall place near CPU
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Compal Electronics, Inc.
Merom Processor(1/2)
LA-3302P
Thursday, March 01, 2007
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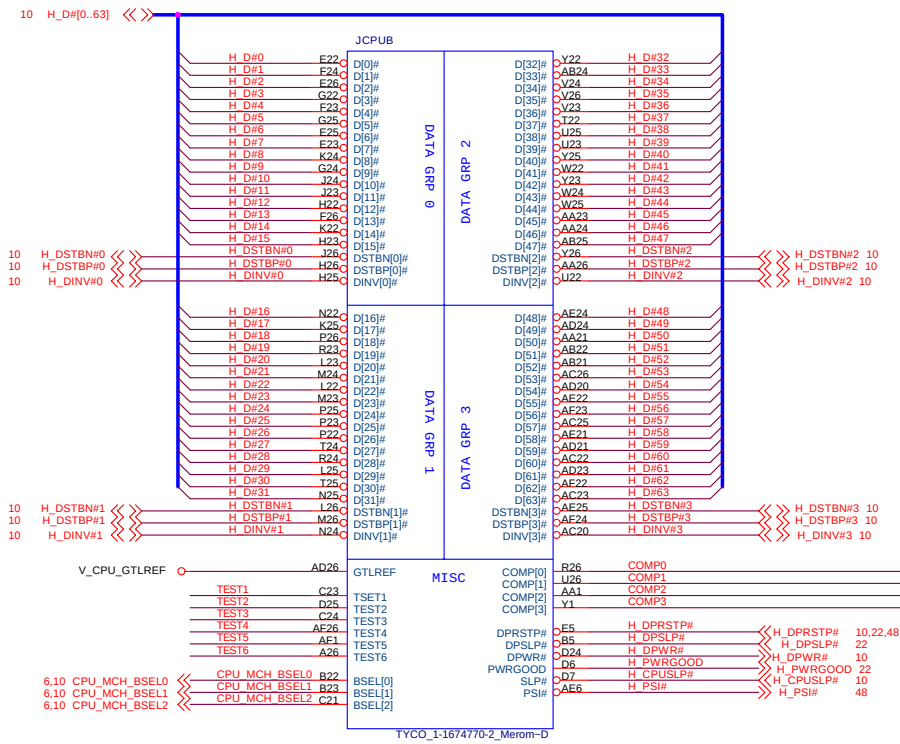
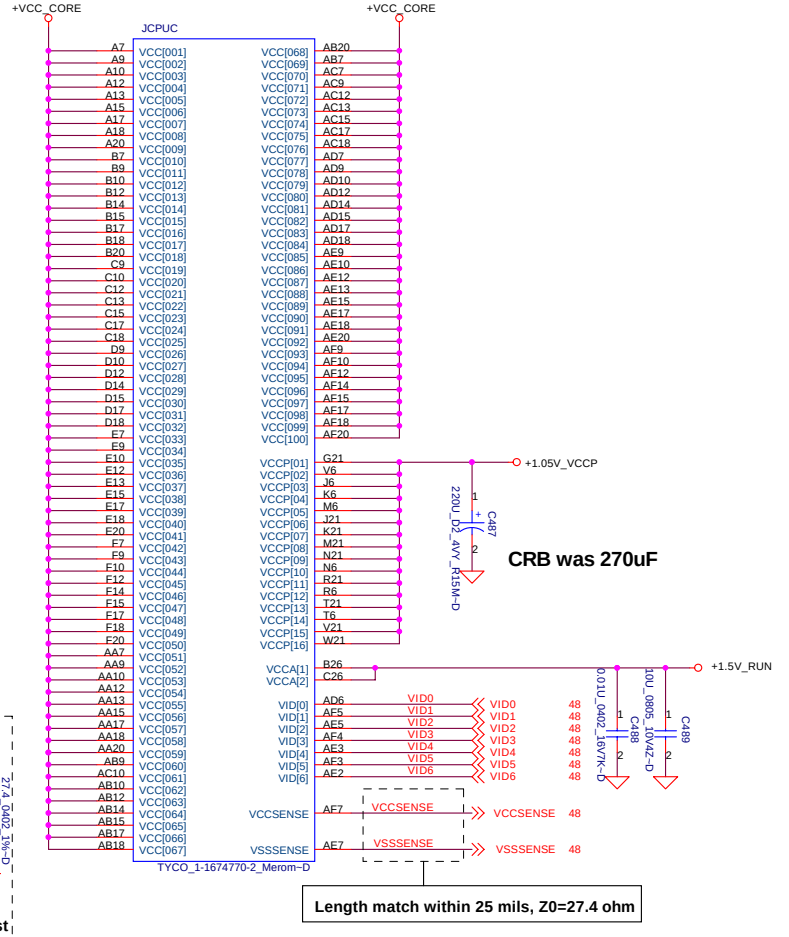
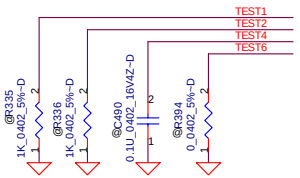


Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP0, COMP2 trace should be 27.4 ohm. COMP1, COMP3 should be 55 ohm.



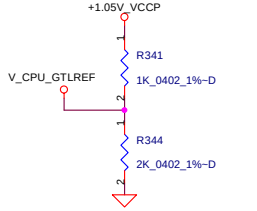
Length match within 25 mils, Z0=27.4 ohm



Place C490 close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

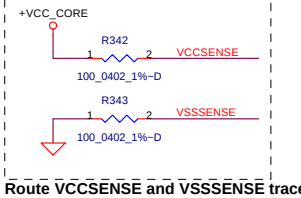
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0



Layout close CPU PIN AD26
55 ohm, 0.5 inch (max)

Place R342 and R343 near CPU



Route VCCSENSE and VSSSENSE trace at 27.4 ohms, 7 mils spacing and 1 inch (max)

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Title: Merom Processor(2/2)

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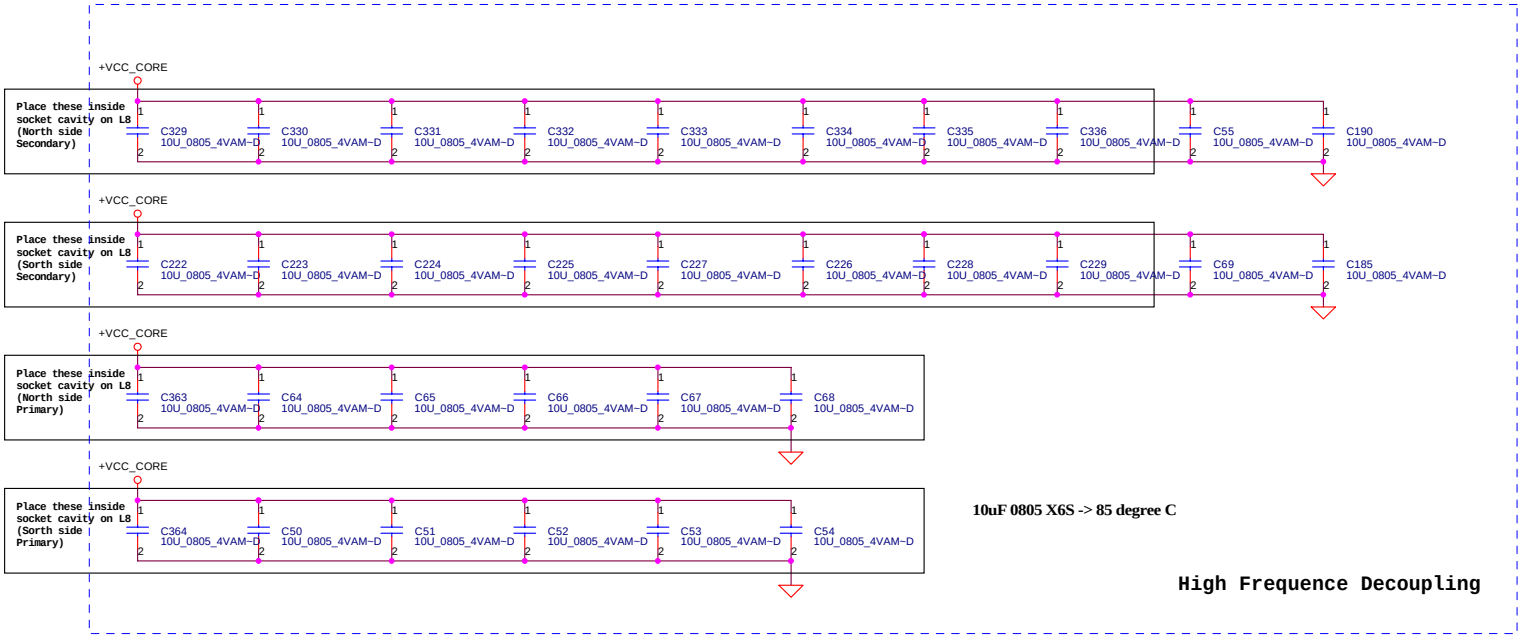
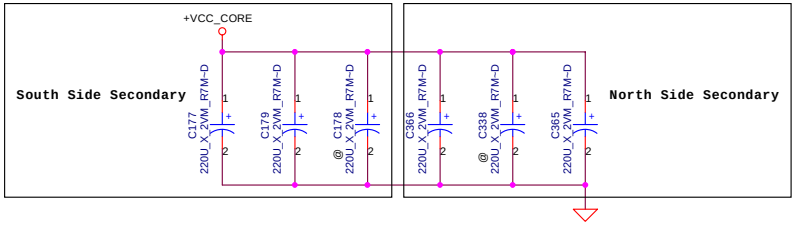
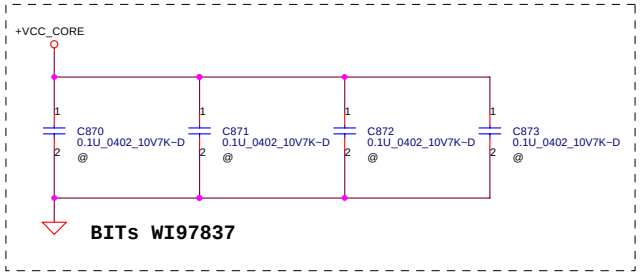
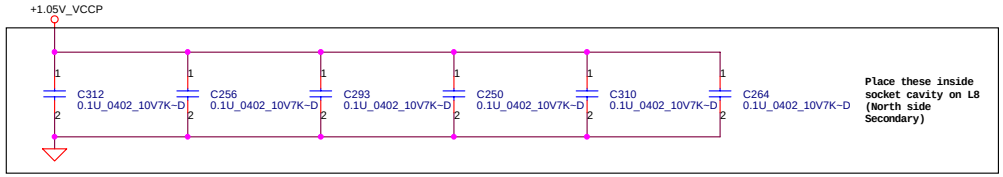


Near VCORE regulator.



ESR <= 1.5m ohm
Capacitor > 1980uF





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Title	CPU Bypass
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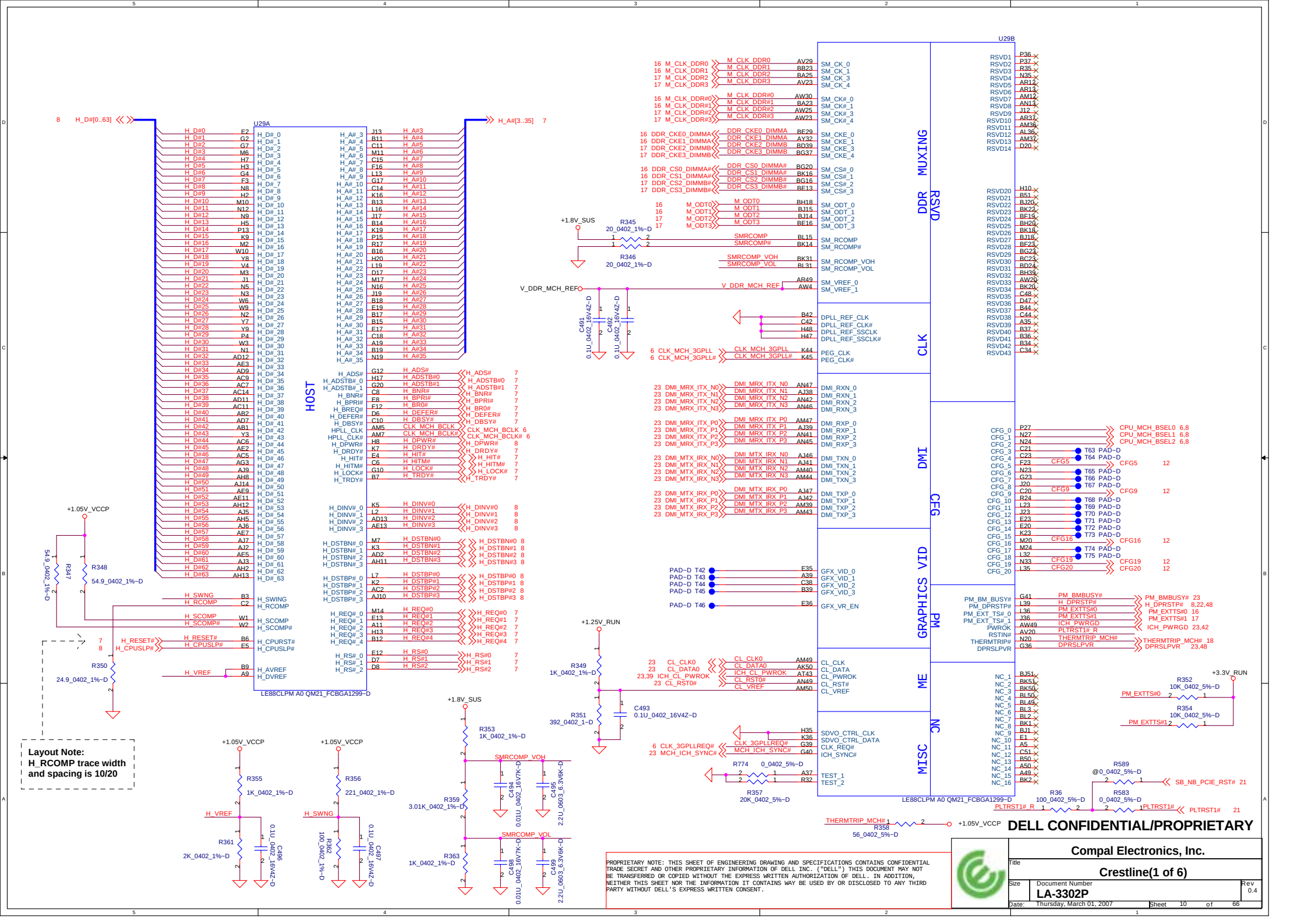
U29A
HOST
LE88CLPM A0 QM21_FCBGA1299~D
U29B
DDR MUXING
DDR RSVD
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
LE88CLPM A0 QM21_FCBGA1299~D
Layout Note:
H_RCOMP trace width
and spacing is 10/20
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Title
Crestline(1 of 6)
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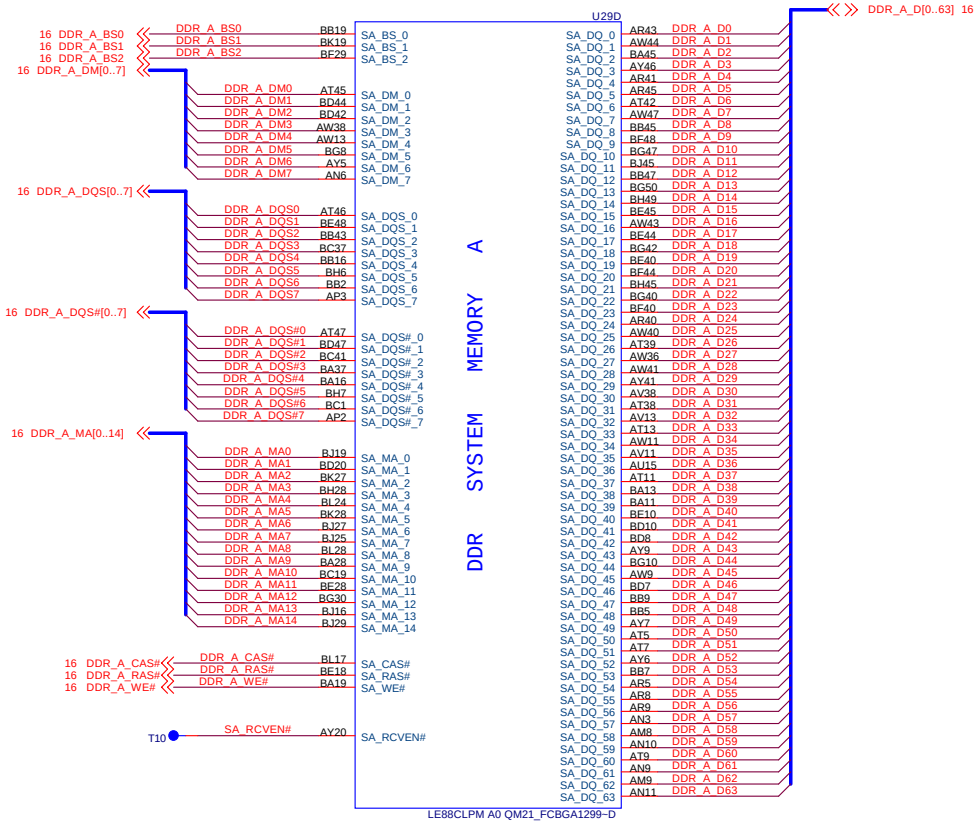

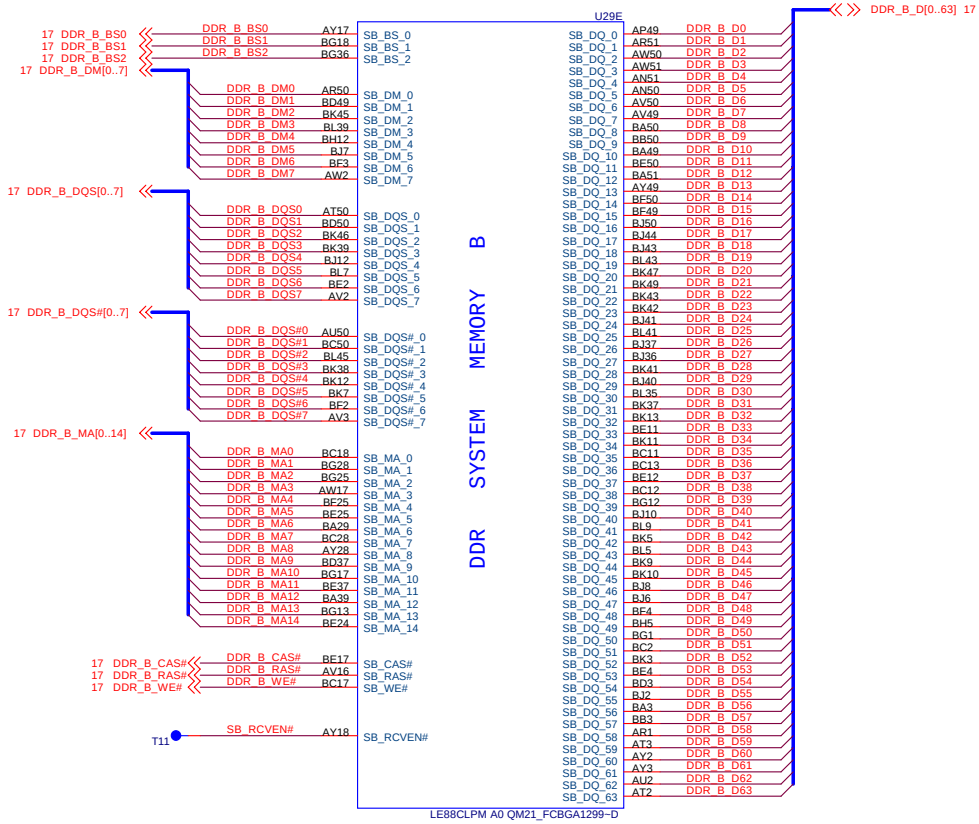

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Title: Crestline(2 of 6)

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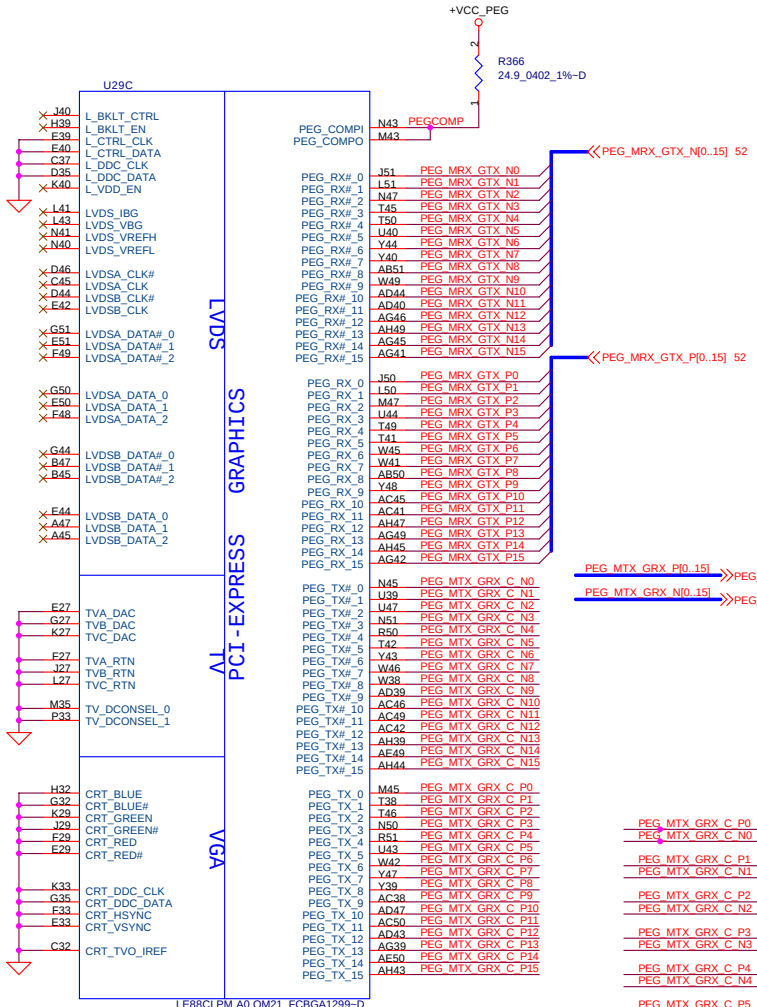
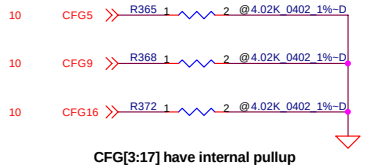
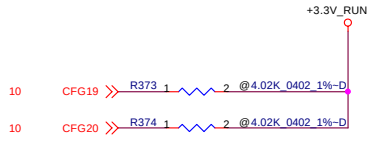


Strap Pin Table

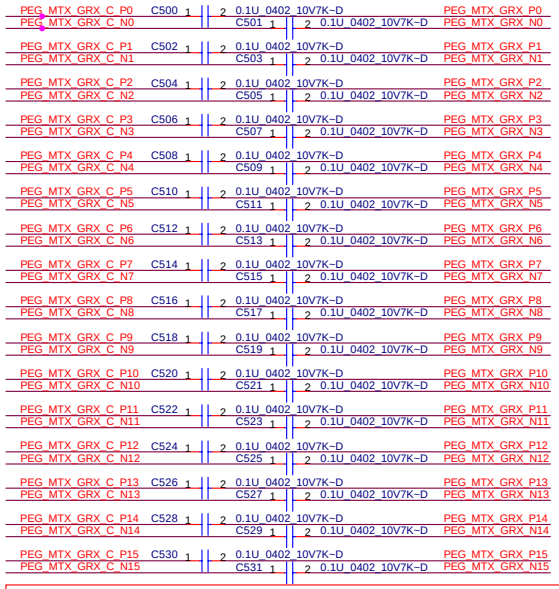
CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation (Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA		Low=No SDVO Device Present (default) High=SDVO Device Present



CFG[3:17] have internal pullup



CFG[18:19] have internal pulldown



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Title: Crestline(3 of 6)

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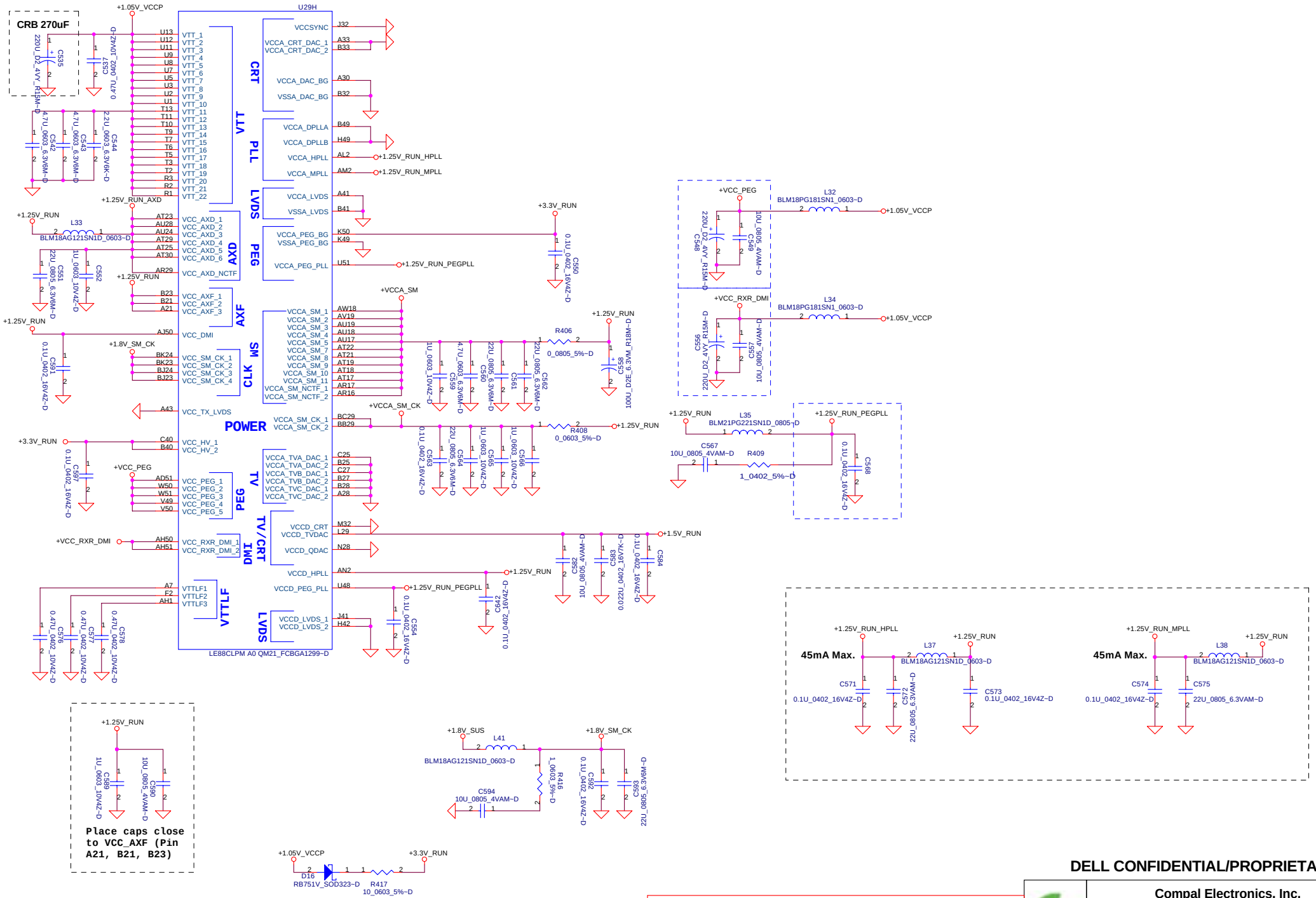

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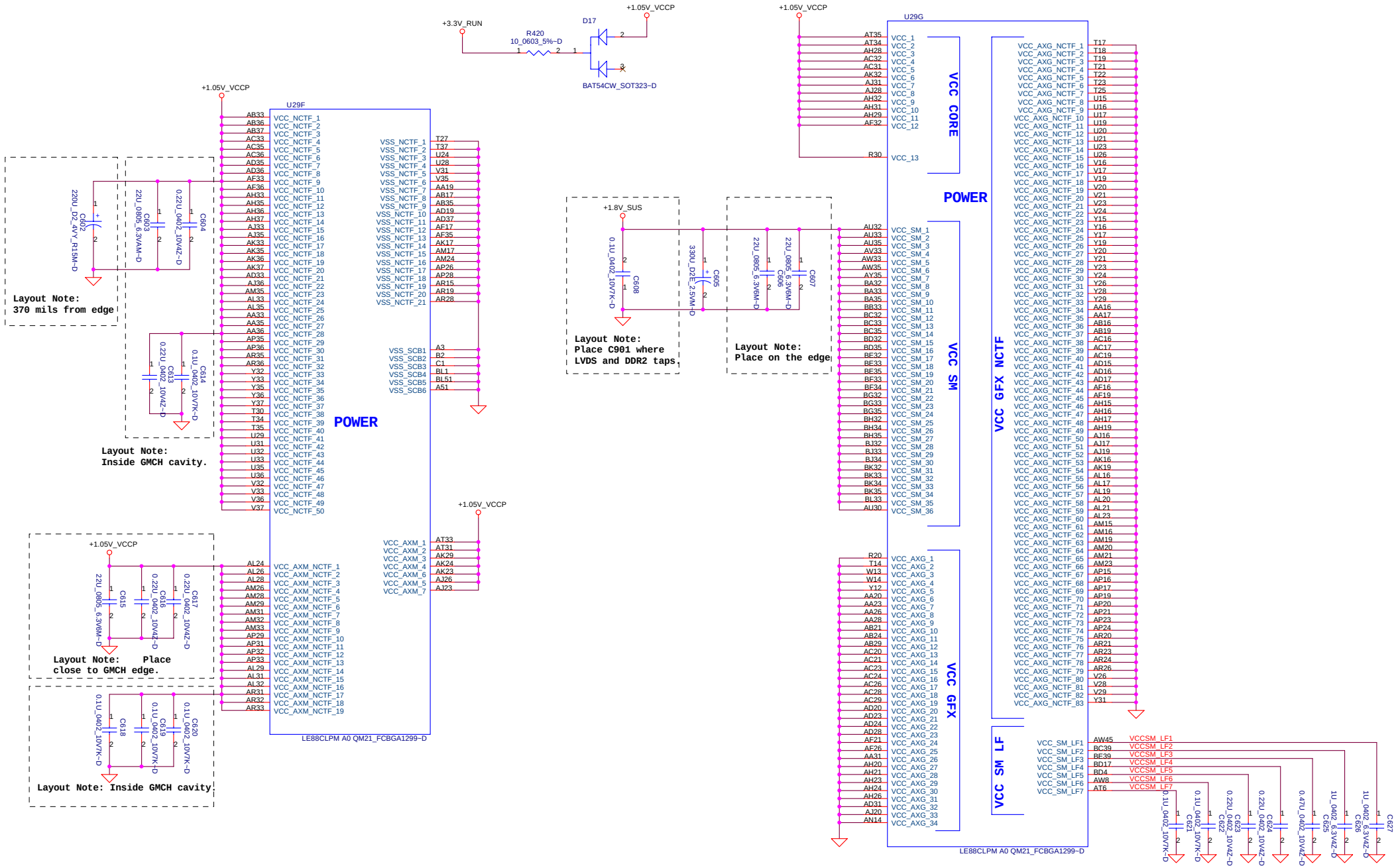

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Title: Crestline(5 of 6)

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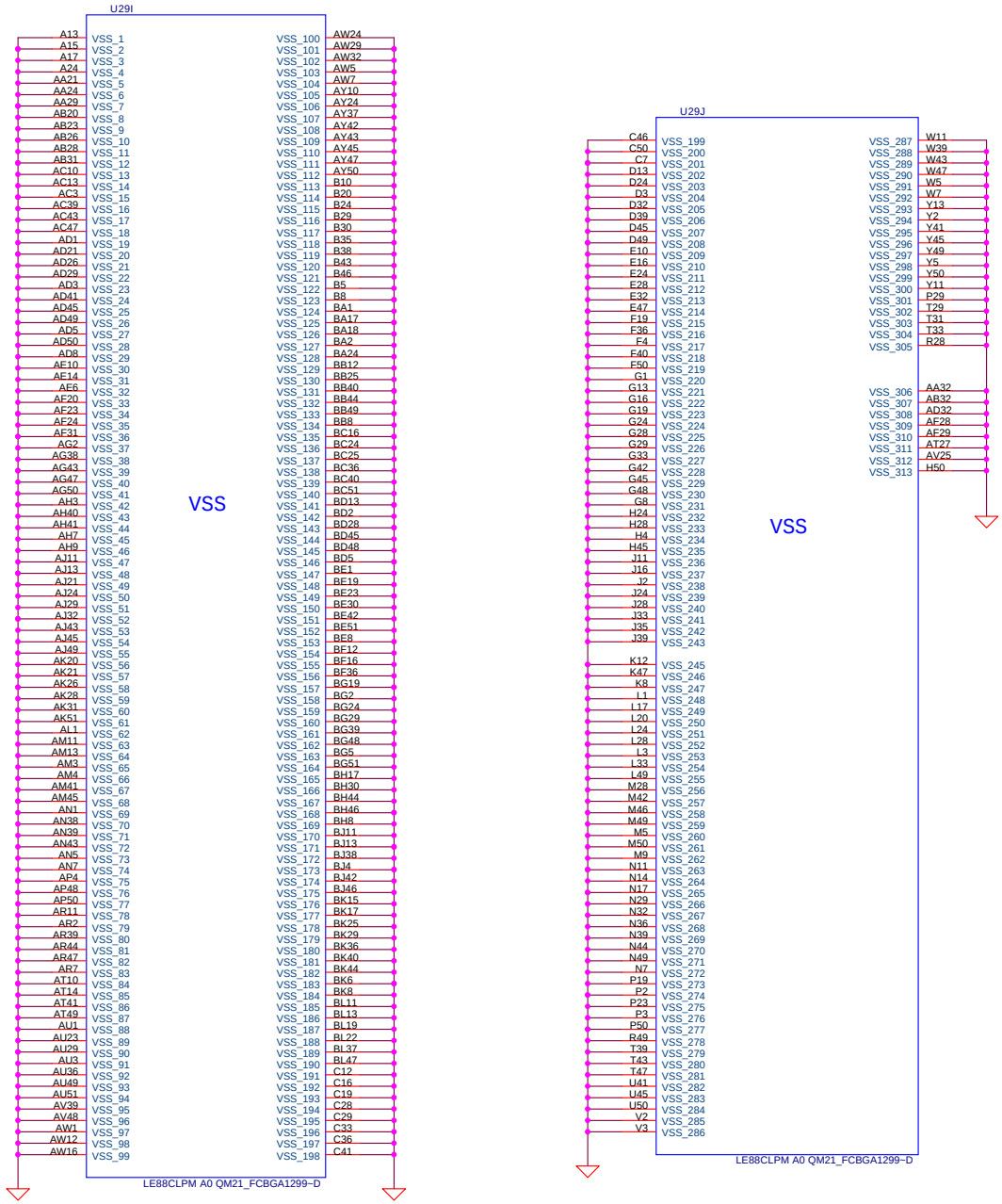

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Title: Crestline(6 of 6)

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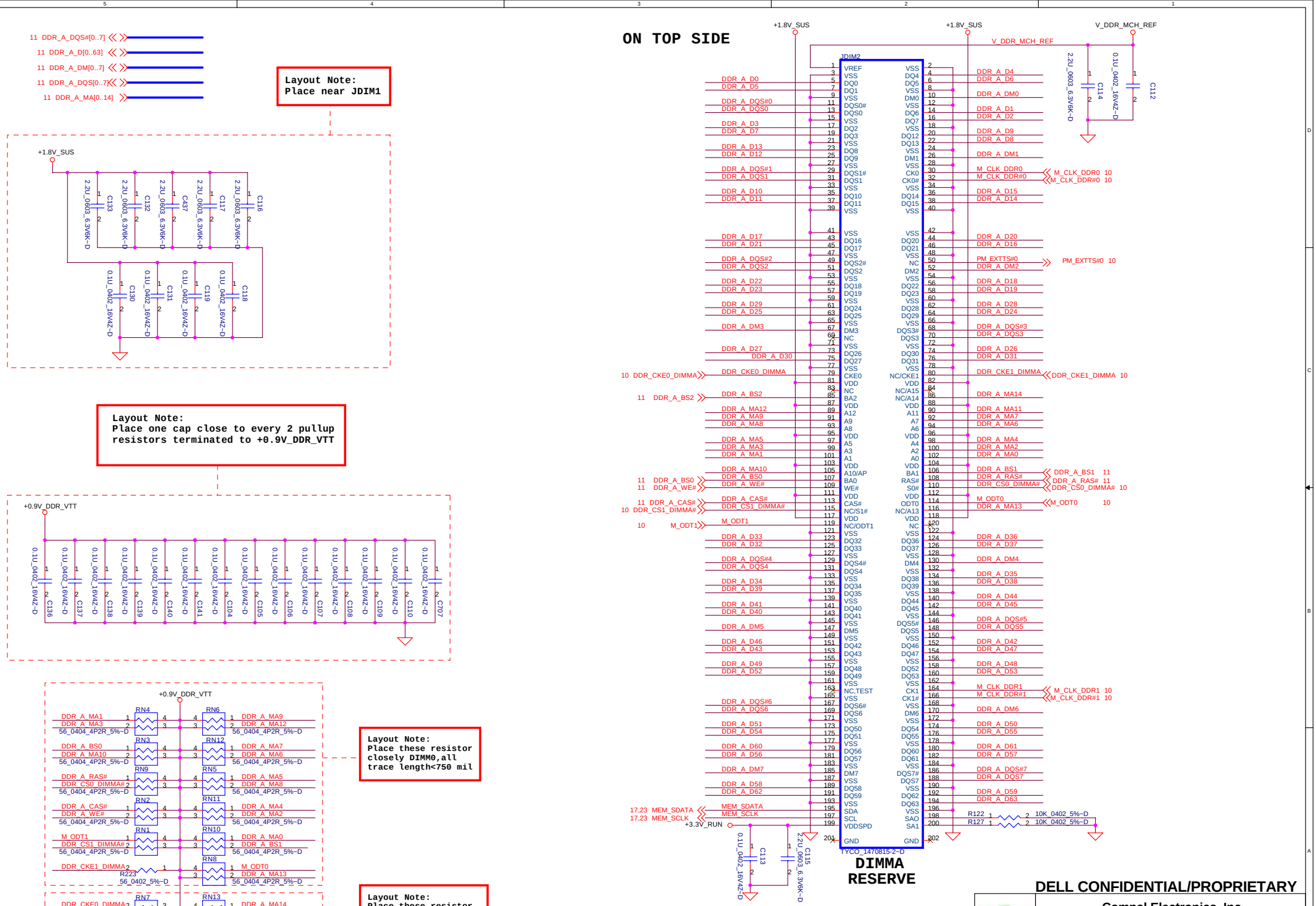
ON TOP SIDE
11 DDR_A_DQS#[0..7]
11 DDR_A_D[0..63]
11 DDR_A_DM[0..7]
11 DDR_A_DQS[0..7]
11 DDR_A_MA[0..14]
Layout Note:
Place near JDIM1
+1.8V_SUS
C133 C132 C437 C117 C116
C130 C131 C119 C118
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
+0.9V_DDR_VTT
C136 C137 C138 C139 C140 C141 C104 C105 C106 C107 C108 C109 C110 C707
+0.9V_DDR_VTT
RN4 RN6 RN3 RN12 RN9 RN5 RN2 RN11 RN1 RN10 RN8 RN7 RN13
56_0404_4P2R_5%~D
R223 56_0402_5%~D
Layout Note:
Place these resistor
closely DIMM0,all
trace length<750 mil
Layout Note:
Place these resistor
closely DIMM0,all
trace length
Max=1.3"
+1.8V_SUS
+1.8V_SUS
V_DDR_MCH_REF
V_DDR_MCH_REF
C114 C112
JDIM2
TYCO_1470815-2~D
DIMMA
RESERVE
10 DDR_CKE0_DIMMA
11 DDR_A_BS2
11 DDR_A_BS0
11 DDR_A_WE#
11 DDR_A_CAS#
10 DDR_CS1_DIMMA#
10 M_ODT1
17,23 MEM_SDATA
17,23 MEM_SCLK
+3.3V_RUN
C113 C115
M_CLK_DDR0 10
M_CLK_DDR#0 10
PM_EXTTS#0 10
DDR_CKE1_DIMMA 10
DDR_A_BS1 11
DDR_A_RAS# 11
DDR_CS0_DIMMA# 10
M_ODT0 10
M_CLK_DDR1 10
M_CLK_DDR#1 10
R122 10K_0402_5%~D
R127 10K_0402_5%~D
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Rev
0.4
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ON BOTTOM SIDE

11 DDR_B_DQS#[0..7]
11 DDR_B_D[0..63]
11 DDR_B_DM[0..7]
11 DDR_B_DQS[0..7]
11 DDR_B_MA[0..14]

Layout Note:
Place near JDIM2

+1.8V_SUS

2.2U_0603_6.3V6K-D: C439, C440, C412, C438, C411

0.1U_0402_16V4Z-D: C434, C433, C413, C414

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT

+0.9V_DDR_VTT

0.1U_0402_16V4Z-D: C456, C455, C454, C453, C452, C451, C450, C410, C409, C408, C407, C406, C405

+0.9V_DDR_VTT

RN23: DDR_B_MA1, DDR_B_MA3 — RN21: DDR_B_MA9, DDR_B_MA12
RN24: DDR_B_BS0, DDR_B_MA10 — RN14: DDR_B_MA14, DDR_B_MA11
RN17: DDR_B_MA0, DDR_B_BS1 — RN22: DDR_B_MA5, DDR_B_MA8
RN18: DDR_B_RAS#, DDR_CS2_DIMMB# — RN15: DDR_B_MA7, DDR_B_MA6
RN25: DDR_B_CAS#, DDR_B_WE# — RN16: DDR_B_MA4, DDR_B_MA2
RN19: DDR_CKE3_DIMMB — R312 — M_ODT2, DDR_B_MA13
56_0404_4P2R_5%-D; 56_0402_5%-D

Layout Note:
Place these resistor closely DIMM0,all trace length<750 mil

RN26: DDR_CS3_DIMMB#, M_ODT3 — RN20: DDR_B_BS2, DDR_CKE2_DIMMB
56_0404_4P2R_5%-D

Layout Note:
Place these resistor closely DIMM0,all trace length Max=1.3"

+1.8V_SUS (x2)
V_DDR_MCH_REF
2.2U_0603_6.3V6K-D: C447
0.1U_0402_16V4Z-D: C436

JDIM1 — TYCO_1565917-4-D

DDR_B_D1, DDR_B_D0, DDR_B_DQS#0, DDR_B_DQS0, DDR_B_D6, DDR_B_D7, DDR_B_D8, DDR_B_D9, DDR_B_DQS#1, DDR_B_DQS1, DDR_B_D14, DDR_B_D15, DDR_B_D16, DDR_B_D21, DDR_B_DQS#2, DDR_B_DQS2, DDR_B_D19, DDR_B_D18, DDR_B_D24, DDR_B_D25, DDR_B_DM3, DDR_B_D26, DDR_B_D27, 10 DDR_CKE2_DIMMB, 11 DDR_B_BS2, DDR_B_MA12, DDR_B_MA9, DDR_B_MA8, DDR_B_MA5, DDR_B_MA3, DDR_B_MA1, DDR_B_MA10, 11 DDR_B_BS0, 11 DDR_B_WE#, 11 DDR_B_CAS#, 10 DDR_CS3_DIMMB#, 10 M_ODT3, DDR_B_D32, DDR_B_D36, DDR_B_DQS#4, DDR_B_DQS4, DDR_B_D35, DDR_B_D34, DDR_B_D40, DDR_B_D41, DDR_B_DM5, DDR_B_D46, DDR_B_D42, DDR_B_D53, DDR_B_D49, DDR_B_DQS#6, DDR_B_DQS6, DDR_B_D55, DDR_B_D50, DDR_B_D56, DDR_B_D60, DDR_B_DM7, DDR_B_D58, DDR_B_D59, 16,23 MEM_SDATA, 16,23 MEM_SCLK, +3.3V_RUN

DDR_B_D5, DDR_B_D4, DDR_B_DM0, DDR_B_D2, DDR_B_D3, DDR_B_D13, DDR_B_D12, DDR_B_DM1, M_CLK_DDR2 10, M_CLK_DDR#2 10, DDR_B_D10, DDR_B_D11, DDR_B_D20, DDR_B_D17, PM_EXTTS#1 10, DDR_B_DM2, DDR_B_D22, DDR_B_D23, DDR_B_D28, DDR_B_D29, DDR_B_DQS#3, DDR_B_DQS3, DDR_B_D30, DDR_B_D31, DDR_CKE3_DIMMB 10, DDR_B_MA14, DDR_B_MA11, DDR_B_MA7, DDR_B_MA6, DDR_B_MA4, DDR_B_MA2, DDR_B_MA0, DDR_B_BS1 11, DDR_B_RAS# 11, DDR_CS2_DIMMB# 10, M_ODT2 10, DDR_B_MA13, DDR_B_D33, DDR_B_D37, DDR_B_DM4, DDR_B_D38, DDR_B_D39, DDR_B_D44, DDR_B_D45, DDR_B_DQS#5, DDR_B_DQS5, DDR_B_D43, DDR_B_D47, DDR_B_D52, DDR_B_D48, M_CLK_DDR3 10, M_CLK_DDR#3 10, DDR_B_DM6, DDR_B_D54, DDR_B_D51, DDR_B_D57, DDR_B_D61, DDR_B_DQS#7, DDR_B_DQS7, DDR_B_D62, DDR_B_D63

+3.3V_RUN
R243 10K_0402_5%-D
R241 10K_0402_5%-D
0.1U_0402_16V4Z-D: C431
2.2U_0603_6.3V6K-D: C429

DIMMB STANDARD

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT2

Size | Document Number: LA-3302P | Rev: 0.4

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FAN1 Control and Tachometer

$$VSET = \frac{R438}{R436+R438} \times 3.3V = 0.865V$$

$$VSET = \left(\frac{Tp-70}{21}\right) \Rightarrow Tp = 88.2\ C$$

+3.3V_SUS
R423 8.2K_0402_5%~D
+1.05V_VCCP
R425 2.2K_0402_5%~D
THERMATRIP1#
Q38 MMST3904-7-F_SOT323-3~D
C628 0.1U_0402_16V4Z~D
7 H_THERMTRIP#

+3.3V_SUS
R426 8.2K_0402_5%~D
+1.05V_VCCP
R427 2.2K_0402_5%~D
THERMATRIP2#
Q39 MMST3904-7-F_SOT323-3~D
C632 0.1U_0402_16V4Z~D
10 THERMTRIP_MCH#

+3.3V_RUN
R424 10K_0402_5%~D
FAN1_TACH 39
R414 0_0402_5%~D
+FAN1_VOUT
FAN1_TACH_FB
JFAN1 MOLEX_53398-0371~D
@ D19 RB751S40T1_SOD523-2~D
C630 22U_0805_6.3VAM~D

+5V_SUS
R771 2.21K_0603_1%~D
VCP2
C750 2200P_0402_50V7K~D
R772 10K_0603_1%_TSM1A103F34D3RZ~D
Q102 2N7002W-7-F_SOT323-3~D
+3.3V_SUS
R773 10K_0402_5%~D
5V_CAL_SIO#
This thermistor circuit is located near Top side DDR connector.

Discrete
VGA_THERMDP 53
C706 470P_0402_50V7K~D
VGA_THERMDN 53
Place Capacitor close to Guardian Chip

PWR_MON 48

Place C649 close to the Guardian pins as possible.
REM_DIODE3_N, REM_DIODE3_P routing together. Trace width / Spacing = 10 / 10 mil
C649 2200P_0402_50V7K~D
Q41 MMST3904-7-F_SOT323-3~D
C650 2200P_0402_50V7K~D @
Q41 Place near the bottom SODIMM
Place C650 close to Q41

Place under CPU
@C633 2200P_0402_50V7K~D
Q40 MMST3904-7-F_SOT323-3~D
2200P_0402_50V7K~D C634
Place C633 close to the Q40 as possible
Place C636 close to the Guardian pins as possible
Place C634 close to the Guardian pins as possible

U31
39,49 THRM_SMBDAT
39,49 THRM_SMBCLK
SMDATA
SMBCLK
REM_DIODE1_P
REM_DIODE1_N
DP1
DN1
DP2
DN2
7 H_THERMDA
C636 470P_0402_50V7K~D
7 H_THERMDC
R428 49.9_0603_1%~D
+3.3V_SUS
+3VSUS_THRM
3V_SUS
+RTC_CELL
RTC_PWR3V
C637 0.1U_0402_16V4Z~D
C638 0.1U_0402_16V4Z~D
42 SUSPWROK
R429 1K_0402_5%~D
VSUS_PWRGD
42 ICH_PWRGD#
R432 1K_0402_5%~D
3V_PWROK#
THERMATRIP1#
THERMTRIP1#
THERMATRIP2#
THERMTRIP2#
THERMATRIP3#
THERMTRIP3#
VSET
XEN
VSS
+FAN1_VOUT
FAN_OUT
FAN_OUT
FAN_DAC1
R437 1K_0402_5%~D
33 MDC_RST_DIS#
MDC_RST_DIS#
SIO_GFX_PWR
5V_CAL_SIO#
GPIO1
GPIO2
GPIO3
GPIO4
27 AUDIO_AVDD_ON
AUDIO_AVDD_ON
GPIO5
GPIO6/FAN_DAC2
PAD_GND
EMC4001_QFN48~D
VCP1
VCP2
VCP2
DP3
DN3
REM_DIODE3_P
REM_DIODE3_N
DP4
DN4
REM_DIODE4_P
REM_DIODE4_N
DP5
DN5
VGA_THERMDP
VGA_THERMDN
ATF_INT#
ATF_INT# 38
POWER_SW#
POWER_SW# 39,40
ACAVAIL_CLR
ACAV_IN 39,49,50
THERMTRIP_SIO
SYS_SHDN#
LDO_SHDN#/ADDR
LDO_POK
LDO_SET
LDO_OUT
LDO_OUT
LDO_IN
LDO_IN
VDD_3V
VDD_5V
VDD_5V

Diode circuit at DP4/DN4 is used for skin temp sensor (placed optimally between CPU, MCH and GPU).
C418 2200P_0402_50V7K~D
Q19 MMST3904-7-F_SOT323-3~D
C904 2200P_0402_50V7K~D @
C418 close to Guardian and C904 close to diode Q19.

R96 10K_0402_5%~D
+3.3V_SUS
R430 10K_0402_5%~D
+3.3V_ALW
THERM_STP# 45
R434 7.5K_0402_5%~D
+3.3V_SUS
@R431 10K_0402_5%~D
+RTC_CELL
2.5V_RUN_PWRGD 42
LDO_SET
+2.5V_RUN
C640 10U_0603_10V4Z~D
C641 0.1U_0402_16V4Z~D @
+3V_LDOIN
R439 0_1210_5%~D
+3.3V_RUN
C643 10U_0603_10V4Z~D
C644 0.1U_0402_16V4Z~D
+3.3V_RUN
C645 10U_0805_10V4Z~D
C646 0.1U_0402_16V4Z~D
+5V_RUN
C647 10U_0805_10V4Z~D
C648 0.1U_0402_16V4Z~D

+3.3V_SUS
@ R196 MDC_RST_DIS# 10K_0402_5%~D
@ R194 SIO_GFX_PWR 10K_0402_5%~D
C639 0.1U_0402_16V4Z~D
R436 332K_0402_1%~D
C100 2200P_0402_50V7K~D
R438 118K_0402_1%~D

SMBUS ADDRESS : 2F

+3.3V_RUN
R186 8.2K_0402_5%~D
+3.3V_SUS
R187 2.2K_0402_5%~D 2@
R433 8.2K_0402_5%~D
THERMATRIP3#
THERM_B3
Q76 MMST3904-7-F_SOT323-3~D 2@
C203 0.1U_0402_16V4Z~D 2@
52 THERMTRIP_VGA#

+2.5V_RUN
@ R485 31.6K_0402_1%~D
Ra
LDO_SET
R441 1K_0402_1%~D
Rb
Voltage margining circuit for LDO output. For Vmargin, stuff Ra=31.6K and Rb=30K. Rb=1K for production

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Compal Electronics, Inc.
Title: FAN & Thermal Sensor
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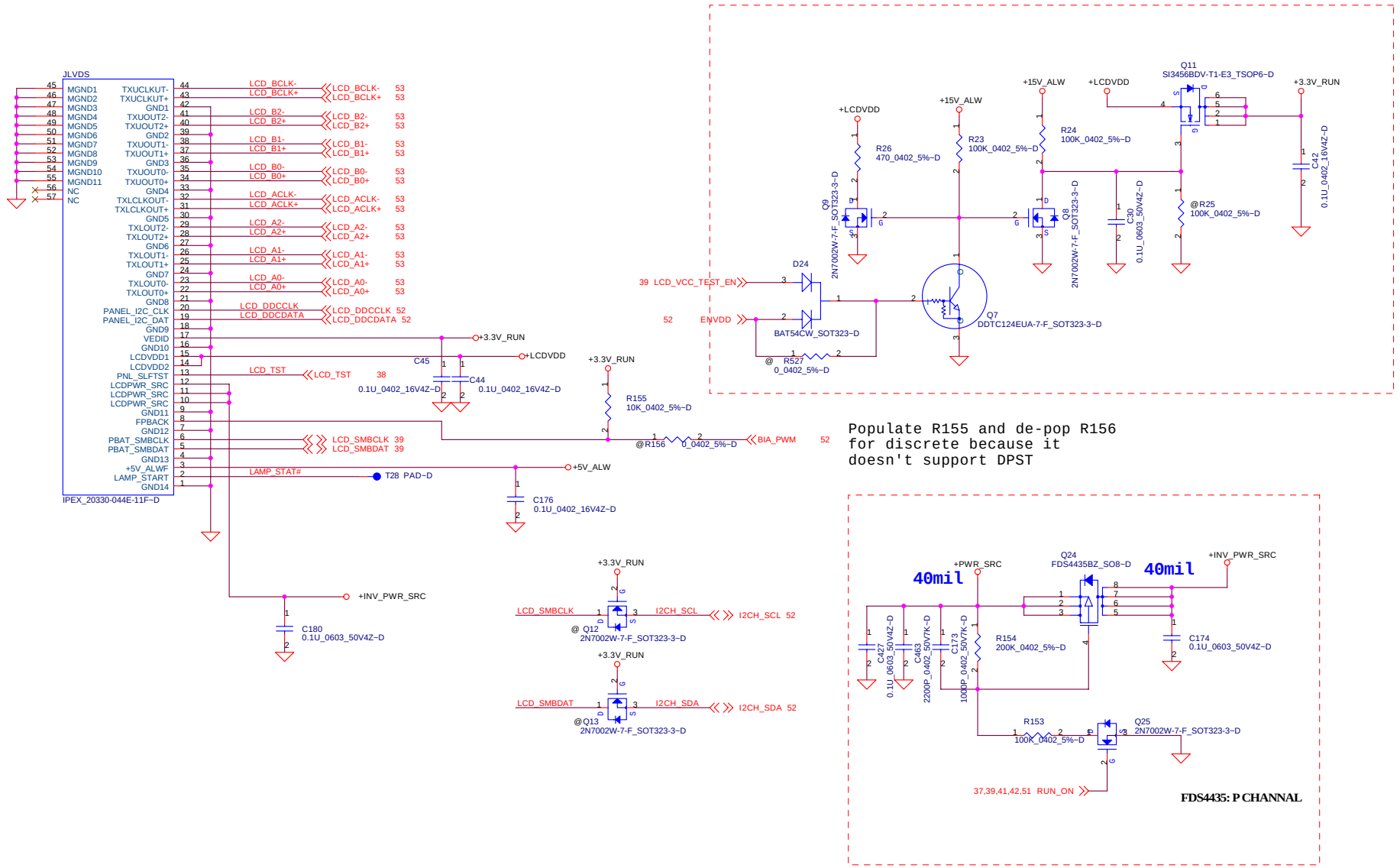

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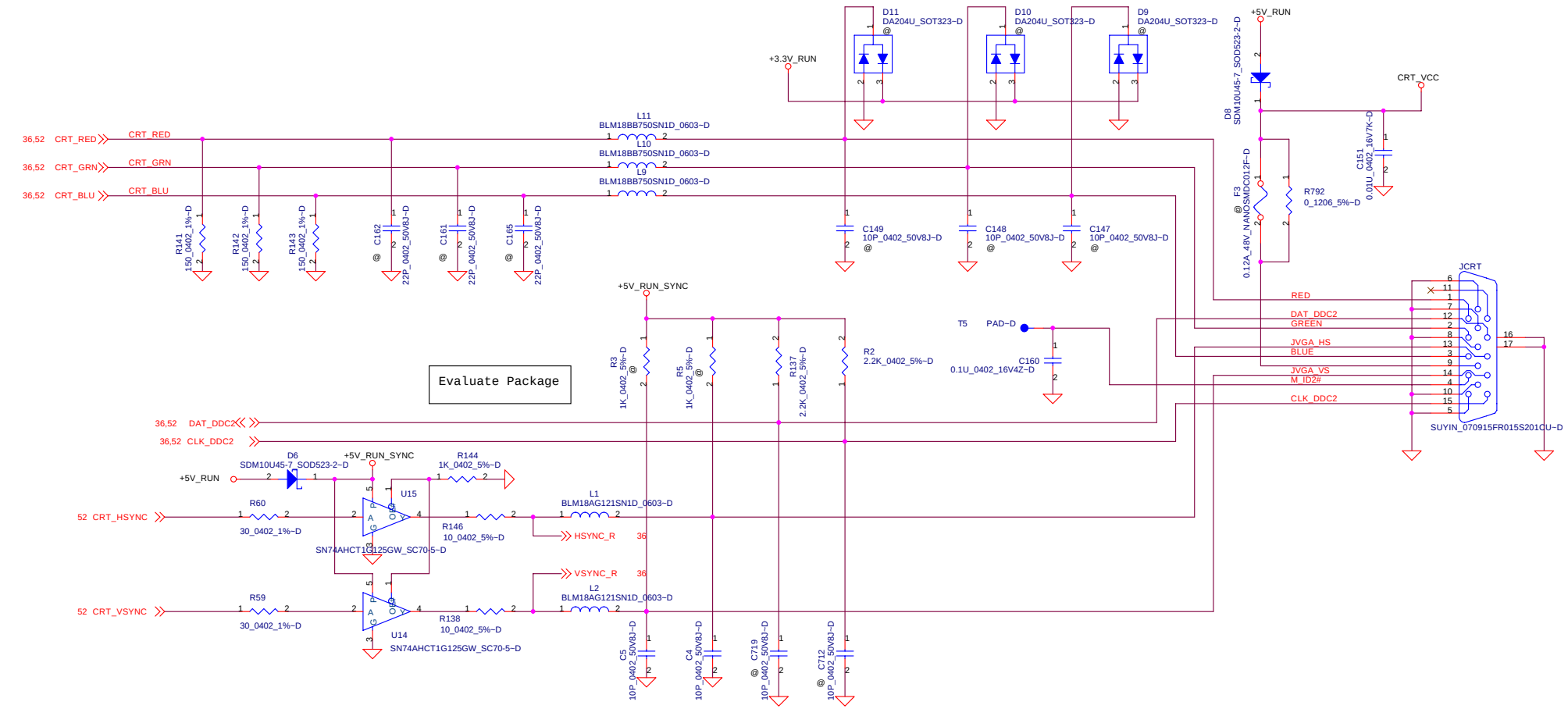
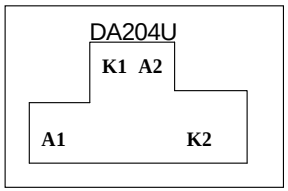
Compal Electronics, Inc.

Title: Internal LVDS

Size | Document Number: LA-3302P | Rev: 0.4

Date: Thursday, March 01, 2007 | Sheet 19 of 66





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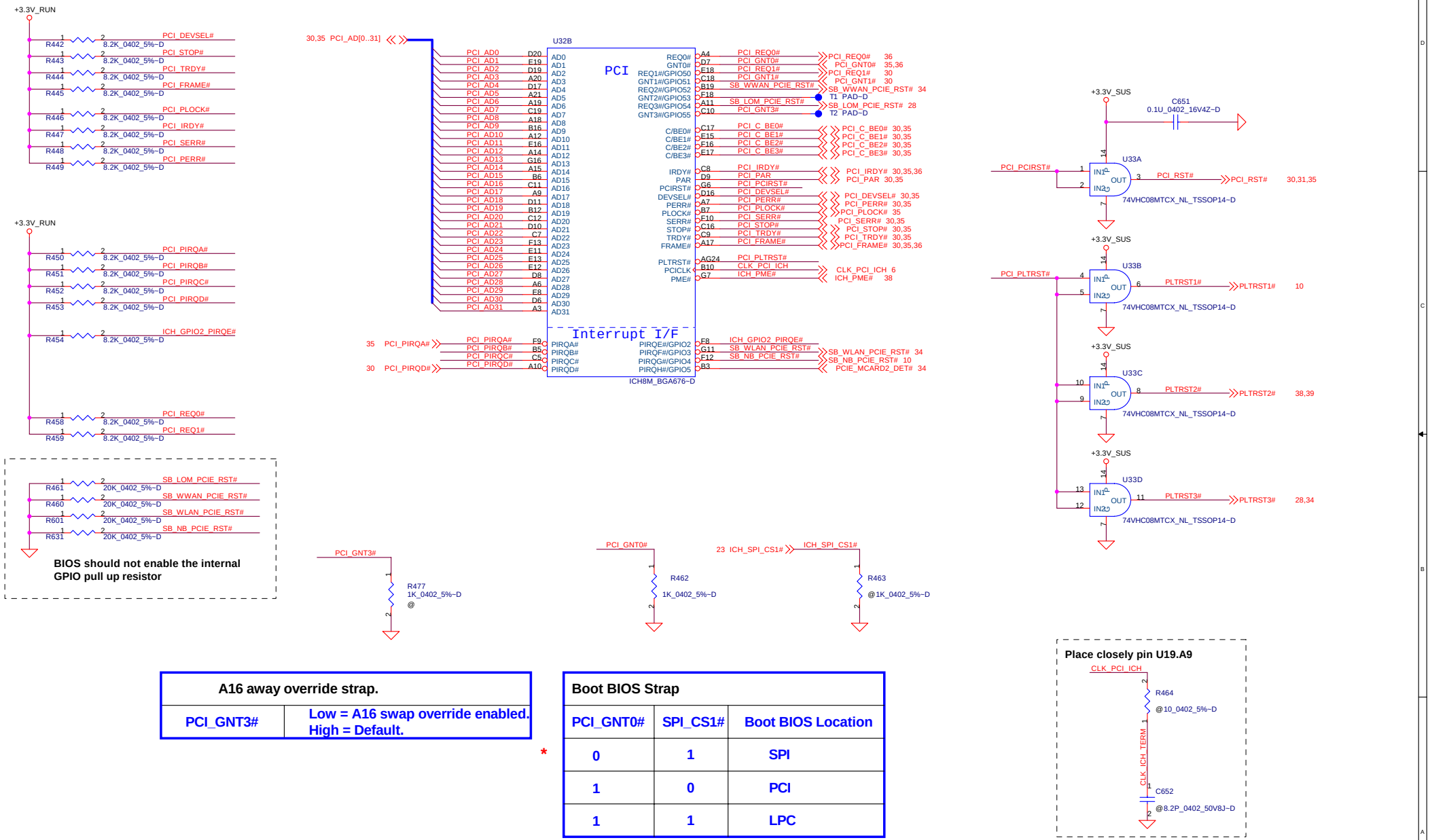
Compal Electronics, Inc.

Title: CRT

Size: | Document Number: LA-3302P | Rev: 0.4

Date: Thursday, March 01, 2007 | Sheet 20 of 66



A16 away override strap.	
PCI_GNT3#	Low = A16 swap override enabled. High = Default.

*

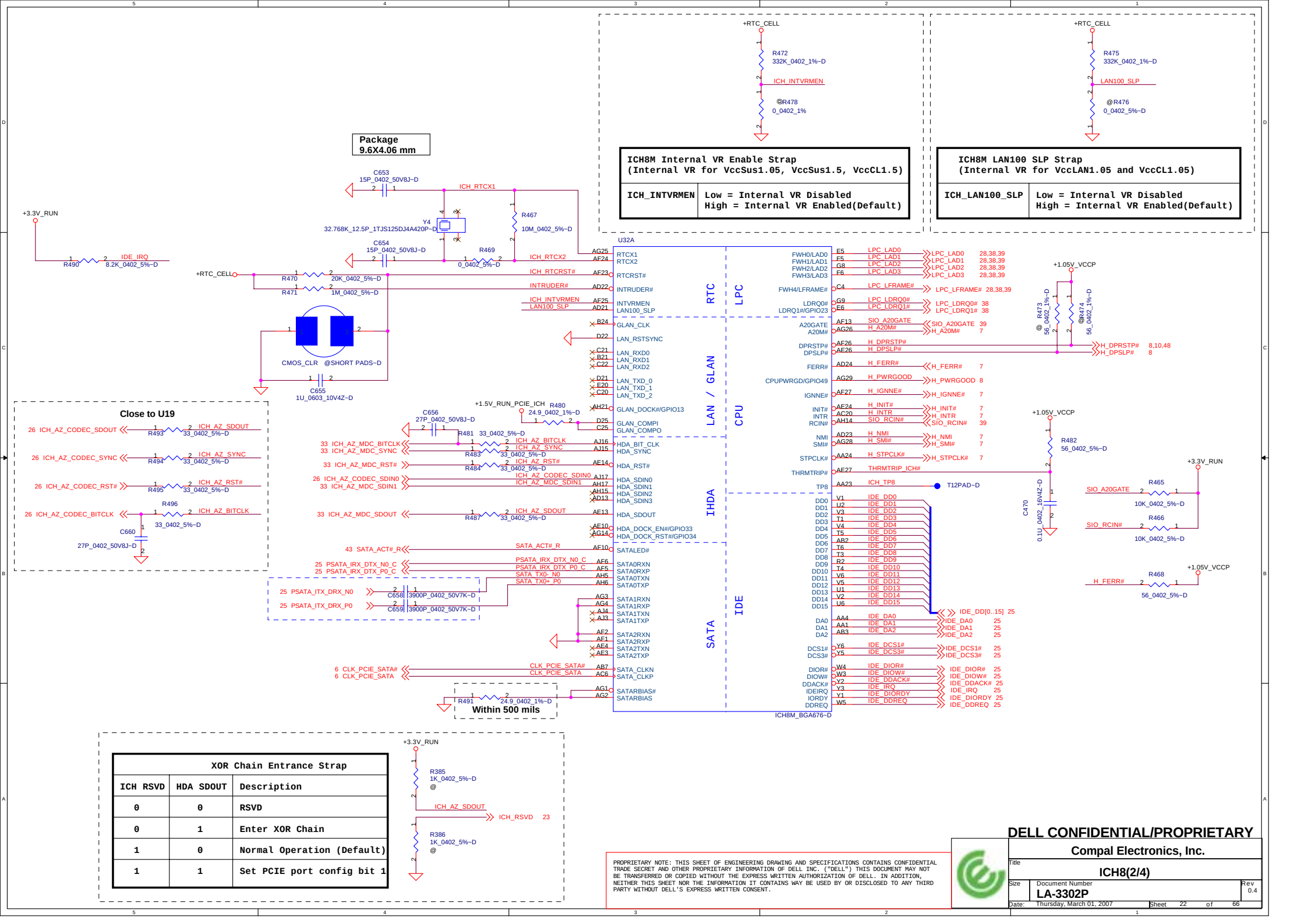
Boot BIOS Strap		
PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC

Compal Electronics, Inc.

Title: ICH8(1/4)

Size | Document Number: LA-3302P | Rev: 0.4

Date: Thursday, March 01, 2007 | Sheet 21 of 66


Package
9.6X4.06 mm
ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)
ICH_INTVRMEN
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
ICH_LAN100_SLP
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
Close to U19
Within 500 mils
XOR Chain Entrance Strap
ICH RSVD
HDA SDOUT
Description
0
0
RSVD
0
1
Enter XOR Chain
1
0
Normal Operation (Default)
1
1
Set PCIE port config bit 1
U32A
RTC
LPC
LAN / GLAN
CPU
IHDA
IDE
SATA
ICH8M_BGA676-D
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Compal Electronics, Inc.
ICH8(2/4)
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Thursday, March 01, 2007
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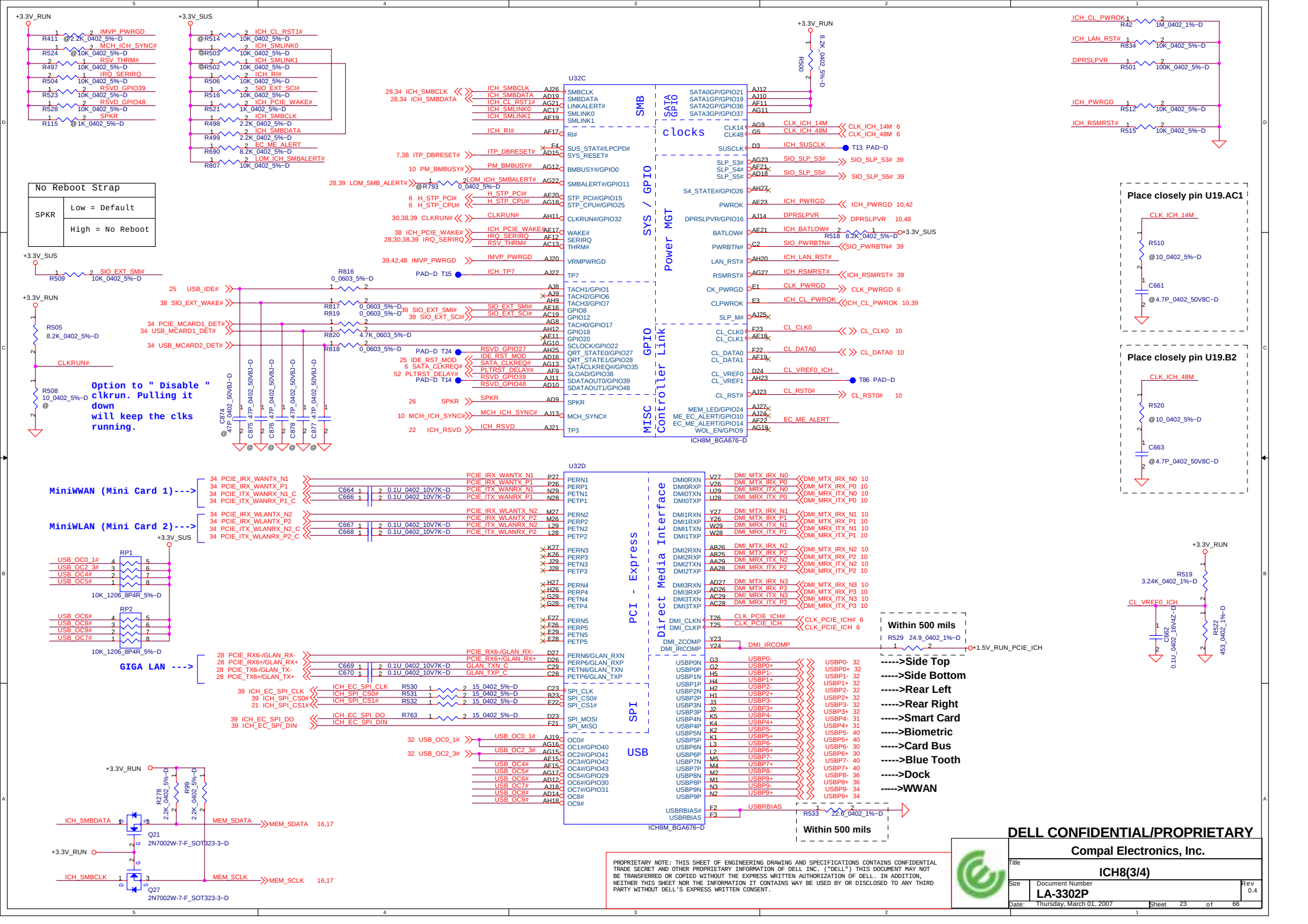
No Reboot Strap
SPKR
Low = Default
High = No Reboot
Option to " Disable " clkrun. Pulling it down will keep the clks running.
U32C
ICH8M_BGA676-D
U32D
ICH8M_BGA676-D
MiniWWAN (Mini Card 1)--->
MiniWLAN (Mini Card 2)--->
GIGA LAN --->
Place closely pin U19.AC1
Place closely pin U19.B2
Within 500 mils
Within 500 mils
----->Side Top
----->Side Bottom
----->Rear Left
----->Rear Right
----->Smart Card
----->Biometric
----->Card Bus
----->Blue Tooth
----->Dock
----->WWAN
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Compal Electronics, Inc.
ICH8(3/4)
LA-3302P
Thursday, March 01, 2007
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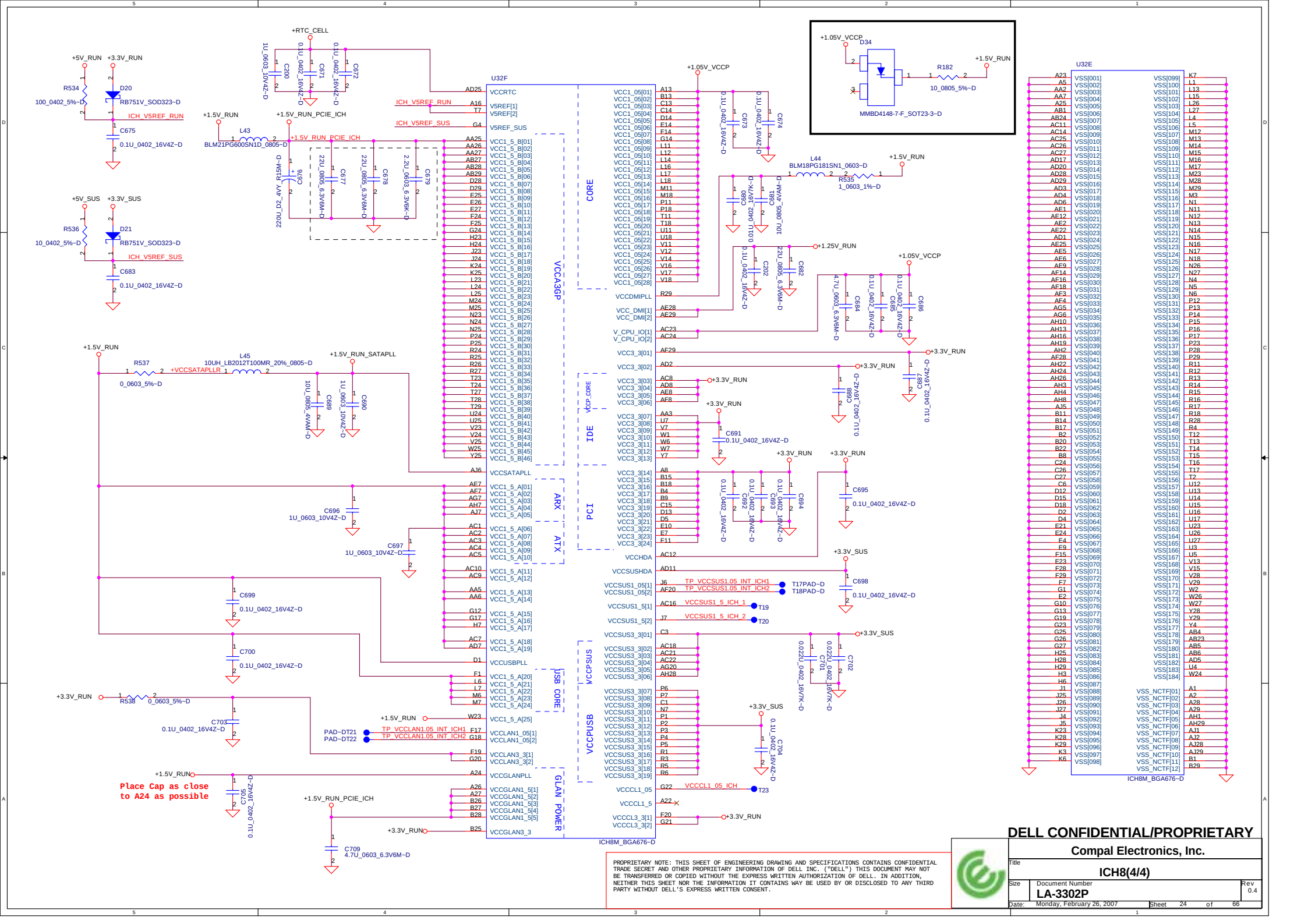

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Compal Electronics, Inc.

Title	ICH8(4/4)	
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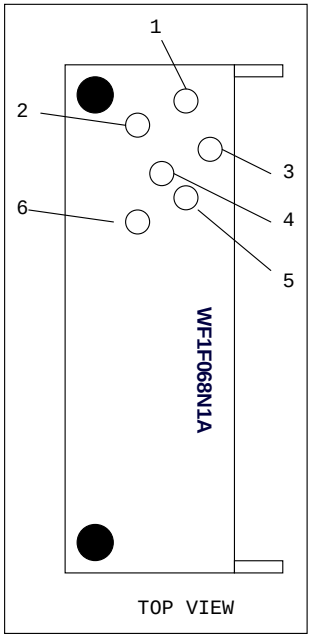

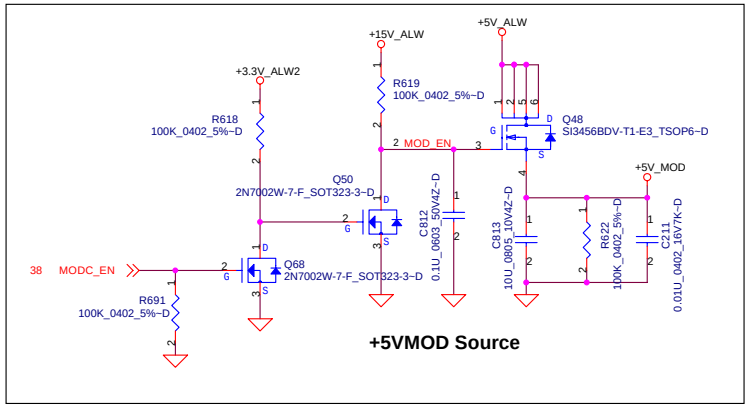

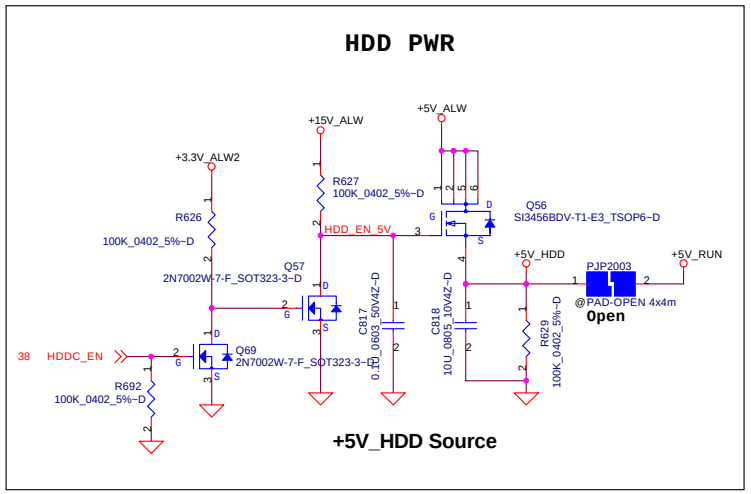

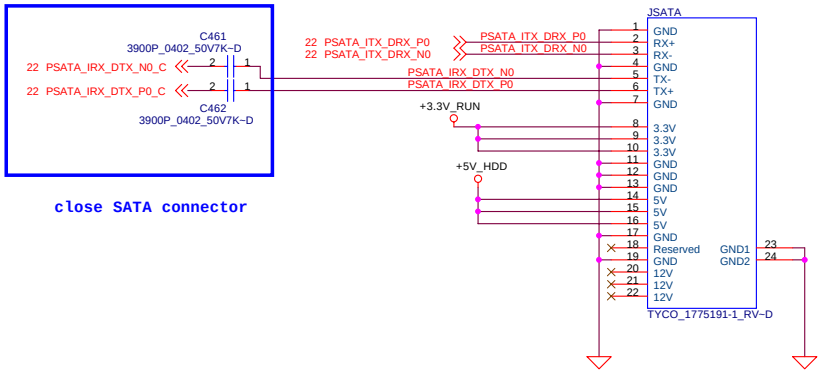

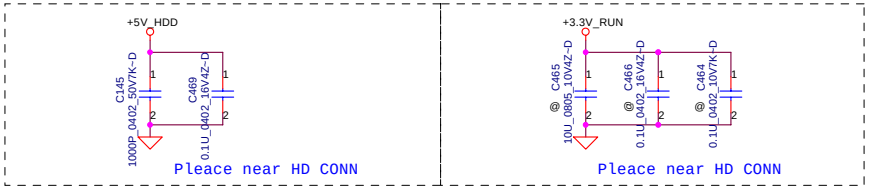

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: DVD MODULE

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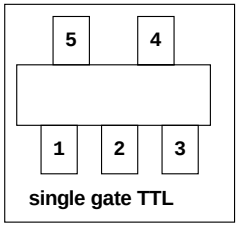
Date: Thursday, March 01, 2007 | Sheet 25 of 66



+VDDA

C710 0.1U_0402_16V4Z~D

23 SPKR
39 BEEP

U34 74AHCT1G86GW_SOT353-5~D

R540 20K_0402_5%~D

BEEP1 BEEP2

C711 0.1U_0402_10V6K~D

AUD_PC_BEEP

R541 10K_0402_5%~D

TRACE>15 mil

U34 place as close to CODEC as possible

+3.3V_RUN

R821 100K_0402_5%~D

W=30 mil

+3.3V_RUN

C714 0.1U_0402_16V4Z~D

C759 1000P_0402_50V7K~D

C715 1U_0603_10V4Z~D

C716 0.1U_0402_16V4Z~D

C172 @ 10U_0805_10V4Z~D

U35

DVDD_CORE
DVDD_CORE
DVDD_CORE/VPP
DVDD_IO

+VDDA

C726 1U_0603_10V4Z~D

C717 0.1U_0402_16V4Z~D

C718 @ 10U_0805_10V4Z~D

AVDD1
AVDD2

SENSE_A
SENSE_B

AUD_SENSE_A
AUD_SENSE_B

22 ICH_AZ_CODEC_BITCLK → ICH_AZ_CODEC_BITCLK → HDA_BIT_CLK

22 ICH_AZ_CODEC_SDIN0 → R544 33_0402_5%~D → ICH_AC_SDIN0_R → HDA_SDI_CODEC

22 ICH_AZ_CODEC_SDOUT → ICH_AZ_CODEC_SDOUT → HDA_SDO

22 ICH_AZ_CODEC_SYNC → HDA_SYNC

22 ICH_AZ_CODEC_RST# → HDA_RST#

PORT_A_L → AUD_HP_OUT_L 27
PORT_A_R → AUD_HP_OUT_R 27
VREFOUT_A

PORT_B_L → AUD_EXT_MIC_L 27
PORT_B_R → AUD_EXT_MIC_R 27
VREFOUT_B → VREFOUT

PORT_C_L
PORT_C_R → AUD_INT_MIC_IN 27
VREFOUT_C

PORT_D_L → AUD_LINE_OUT_L → AUD_LINE_OUT_L 27
PORT_D_R → AUD_LINE_OUT_R → AUD_LINE_OUT_R 27

PORT_E_L
PORT_E_R
VREFOUT_E/GPIO4 → DOCK_HP_MUTE# → DOCK_HP_MUTE# 38

PORT_F_L
PORT_F_R
VREFOUT_F/GPIO3 → AUD_SPDIF_SHDN 38

CD_L
CD_GND
CD_R

PC_BEEP → AUD_PC_BEEP

MONO_OUT

CAP2
VREFFILT

NC1
NC2
NC3

DMIC_CLK
VOL_UP/DMIC0/GPIO1
VOL_DN/DMIC1/GPIO2

27 AUD_EAPD → AUD_EAPD → SPDIF_ IN//GPIO0/EAPD

36 AUD_SPDIF_OUT → AUD_SPDIF_OUT → SPDIF _OUT

R823 10K_0402_5%~D

DVSS
AVSS1
AVSS2
Thermal PAD GND

QFN 7x7 & LQFP 9x9 colay footprint.

STAC9205X5NBEB1XR_QFN48_COMON~D

STAC9205

C724 10U_0805_10V4Z~D

C725 10U_0805_10V4Z~D

+VDDA

R542 5.11K_0402_1%~D

AUD_SENSE_A

R710 39.2K_0402_1%~D

R711 20K_0402_1%~D

C713 1000P_0402_50V7K~D

27,38 AUD_HP_NB_SENSE → AUD_HP_NB_SENSE

Q74 2N7002W-7-F_SOT323~D

Q75 2N7002W-7-F_SOT323~D

AUD_MIC_SWITCH 27

+VDDA

R543 10K_0402_5%~D

AUD_SENSE_B

DOCK_HP_MUTE#

R546 10K_0402_5%~D

AUD_SPDIF_SHDN

R547 10K_0402_5%~D

ICH_AZ_CODEC_BITCLK

R545 10_0402_5%~D

Close to Pin 6

C721 10P_0402_50V8J~D

ICH_AZ_CODEC_SDOUT

R479 47_0402_5%~D @

Close to Pin 5

C782 0.1U_0402_16V4Z~D @

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Azalia (HD) Codec

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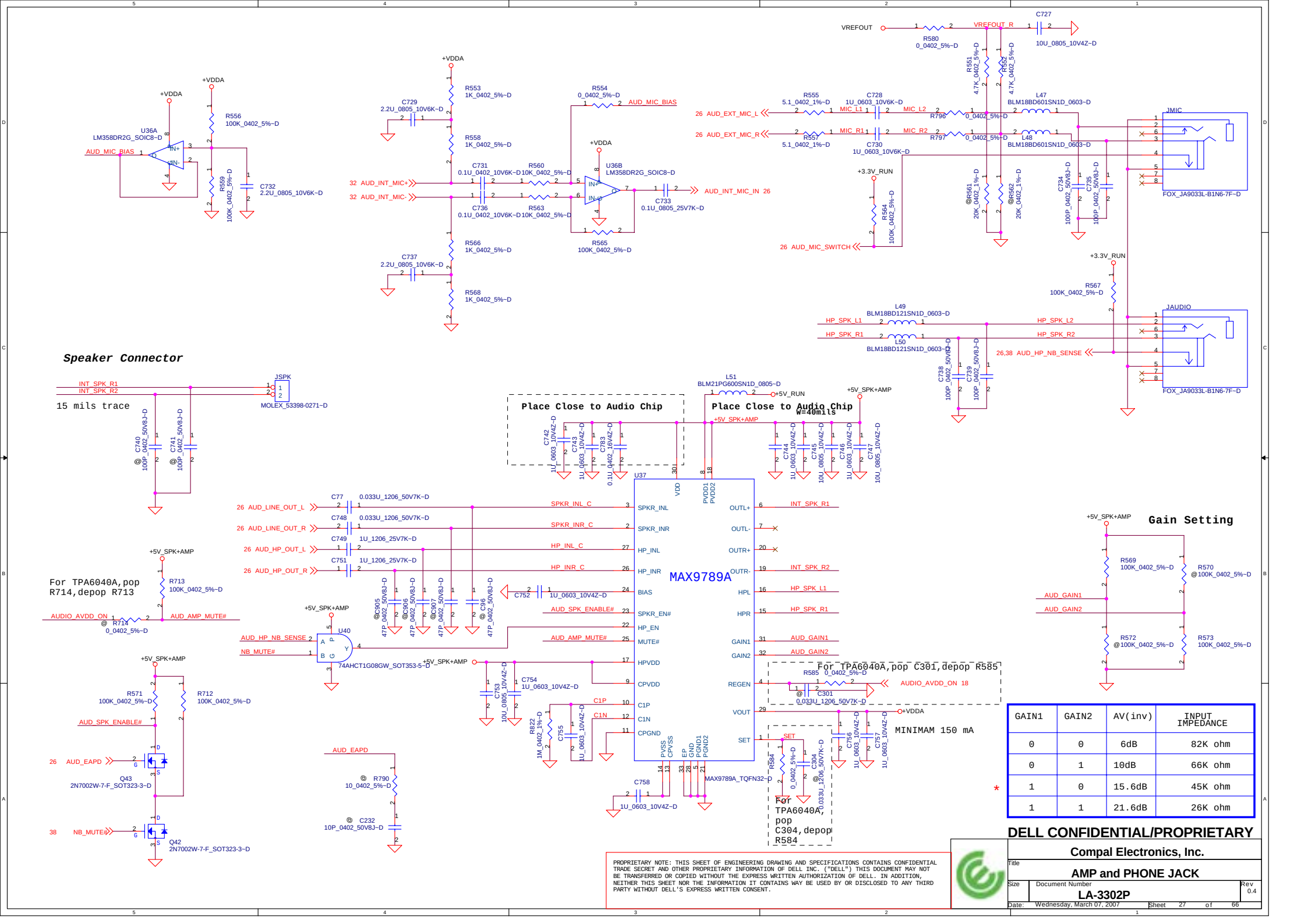
Speaker Connector
MAX9789A
MAX9789A_TQFN32-D
Place Close to Audio Chip
Place Close to Audio Chip W=40mils
15 mils trace
For TPA6040A,pop R714,depop R713
For TPA6040A,pop C301,depop R585
For TPA6040A,pop C304,depop R584
Gain Setting
MINIMAM 150 mA
GAIN1 GAIN2 AV(inv) INPUT IMPEDANCE
0 0 6dB 82K ohm
0 1 10dB 66K ohm
1 0 15.6dB 45K ohm
1 1 21.6dB 26K ohm
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Compal Electronics, Inc.
AMP and PHONE JACK
LA-3302P
Rev 0.4
Wednesday, March 07, 2007
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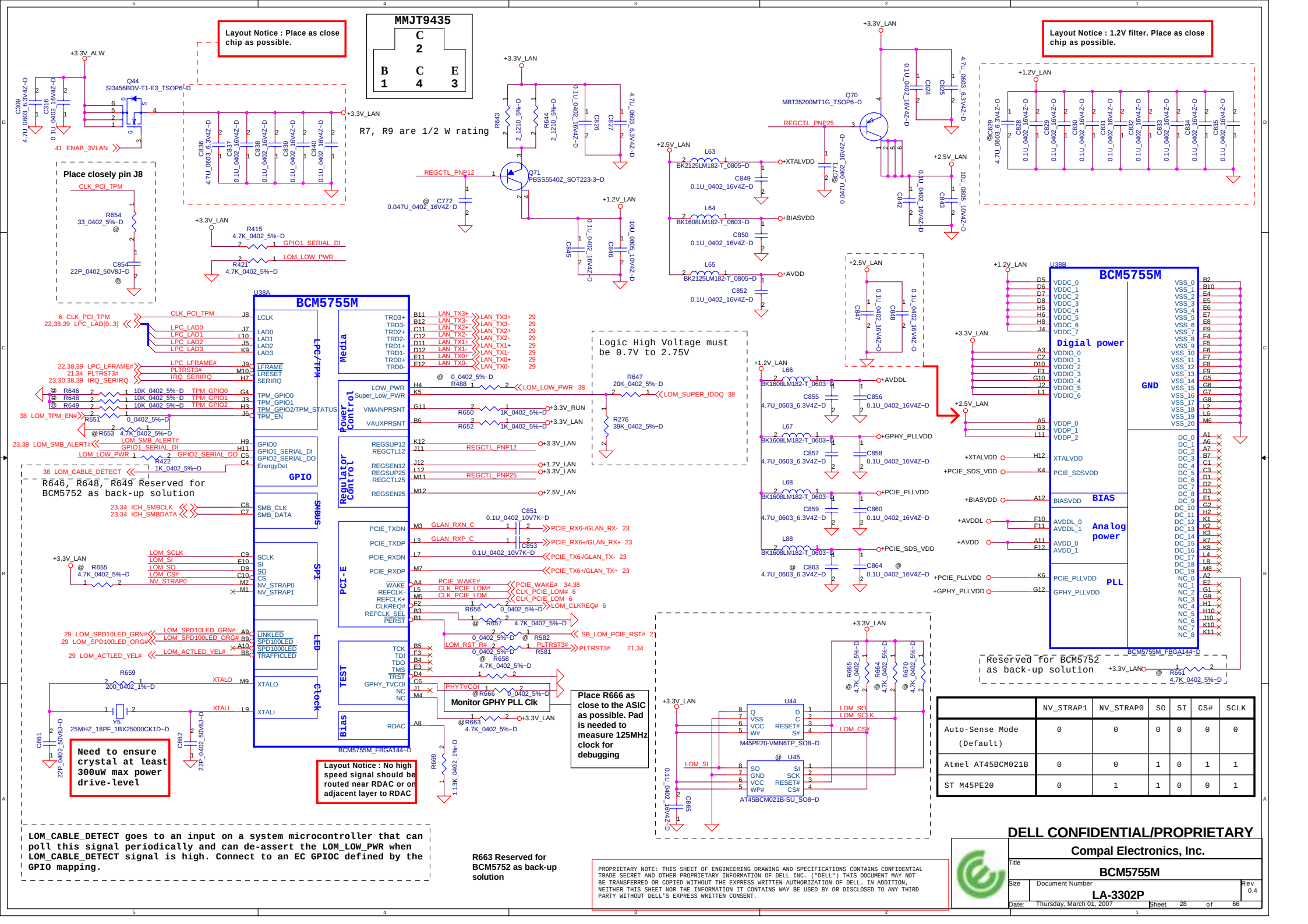
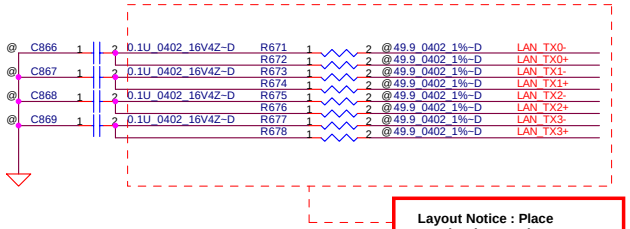
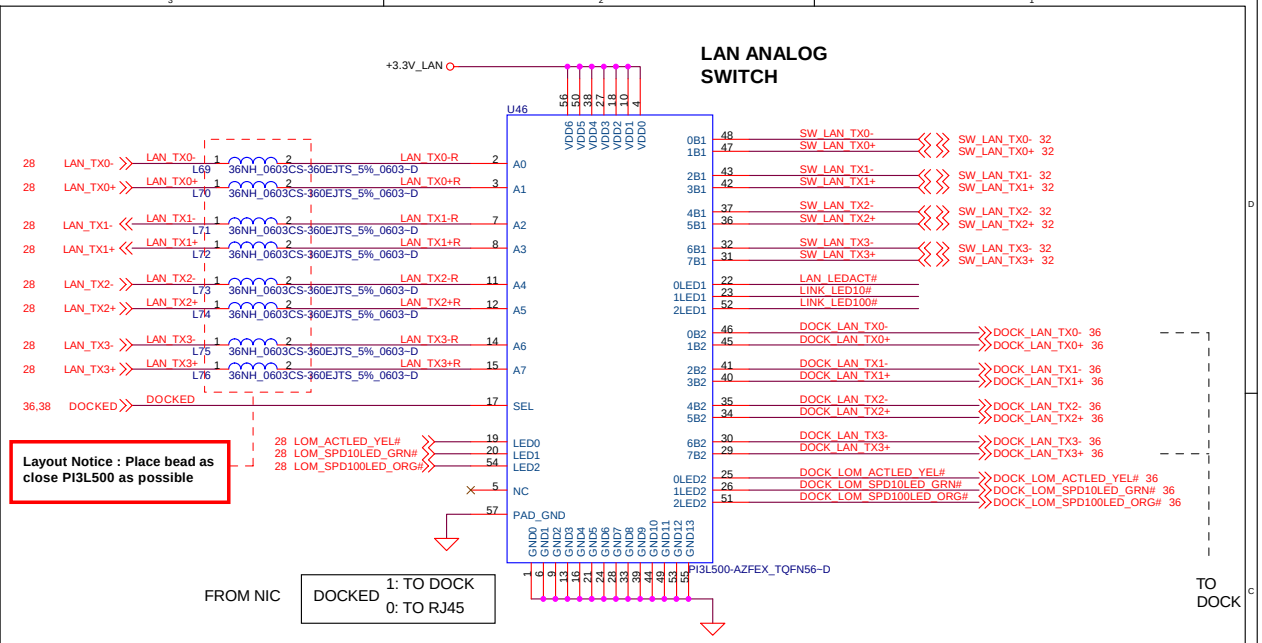


	NV_STRAP1	NV_STRAP0	SO	SI	CS#	SCLK
Auto-Sense Mode (Default)	0	0	0	0	0	0
Atmel AT45BCM021B	0	0	1	0	1	1
ST M45PE20	0	1	1	0	0	1

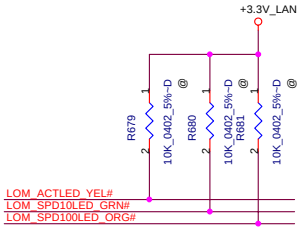


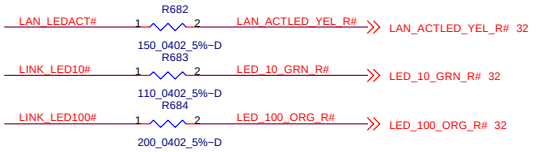
Layout Notice : Place termination as close as ASIC as possible

The resistors need at least 1/16W



Layout Notice : Place bead as close PI3L500 as possible





Compal Electronics, Inc.

Title: LAN TRANSFOMER

Size: | Document Number: LA-3302P | Rev: 0.4

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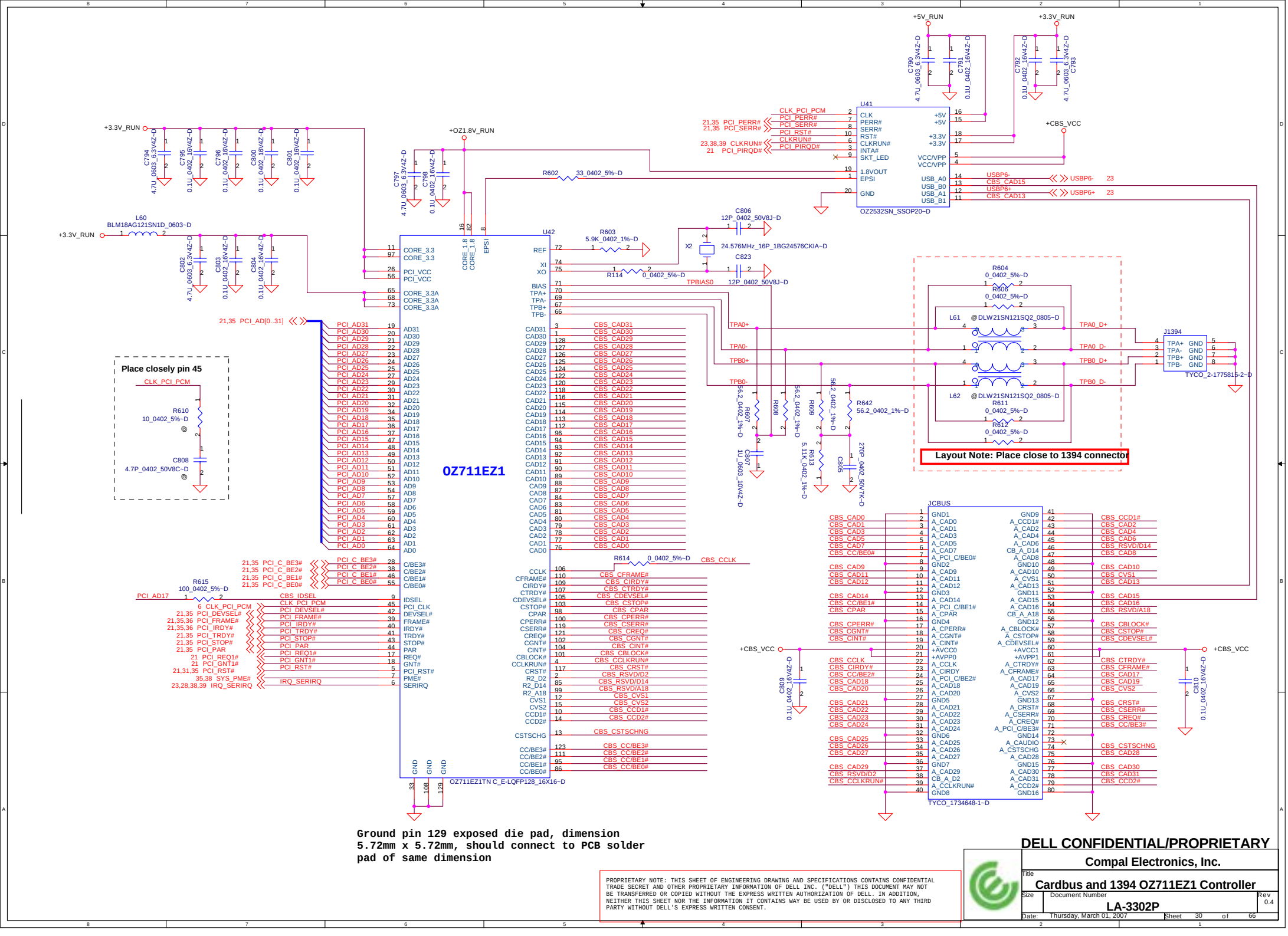

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Compal Electronics, Inc.

Title: Cardbus and 1394 OZ711EZ1 Controller

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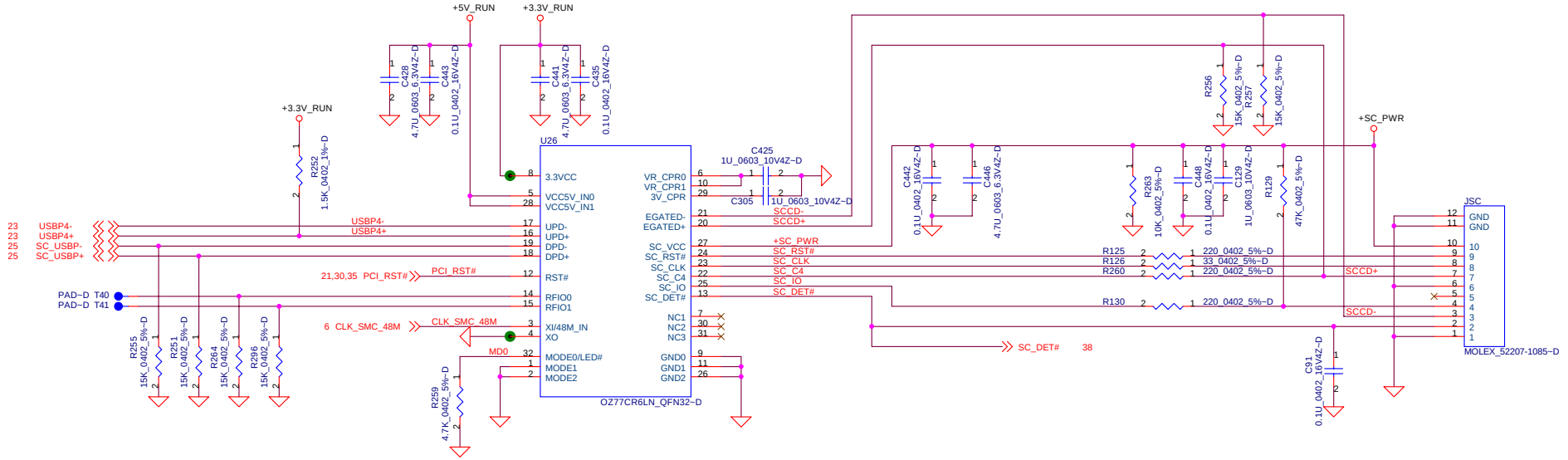
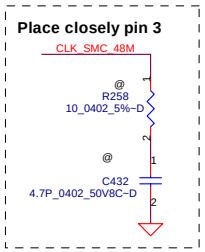
USB SMARTCARD READER.
TYPE A (5V), B (3V), AB (5V/3V)
& USB SMARTCARDS ARE SUPPORTED.





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Compal Electronics, Inc.		
Title: Smart Card OZ77CR6		
Size	Document Number: LA-3302P	Rev: 0.4
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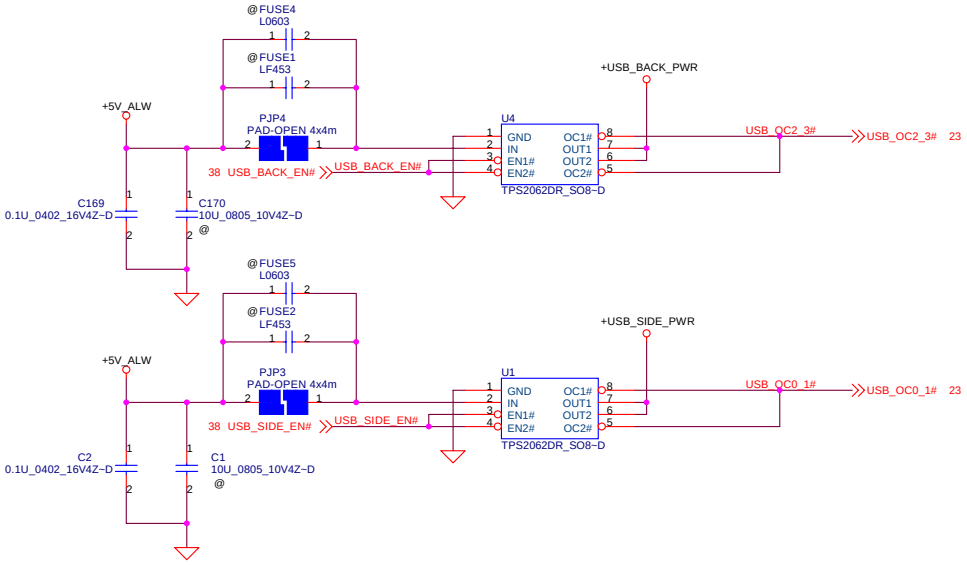

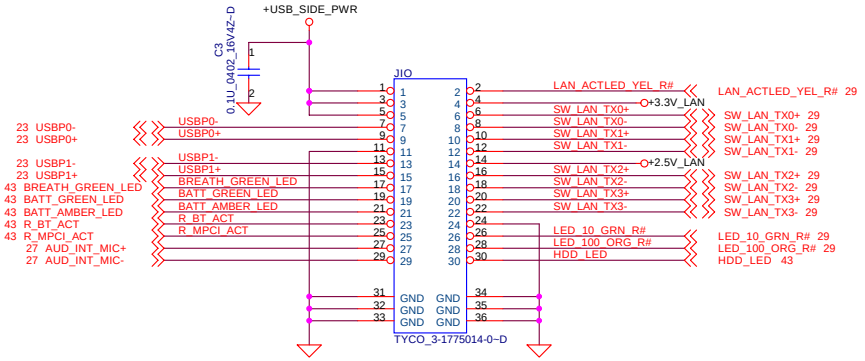

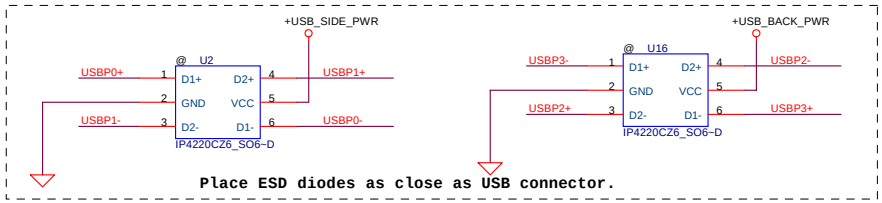

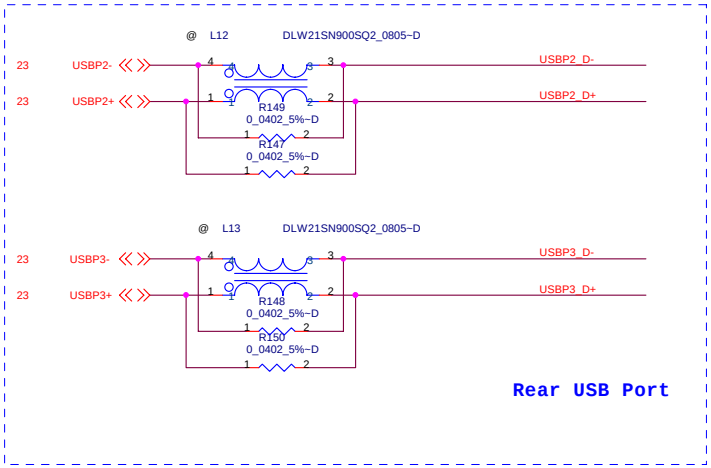

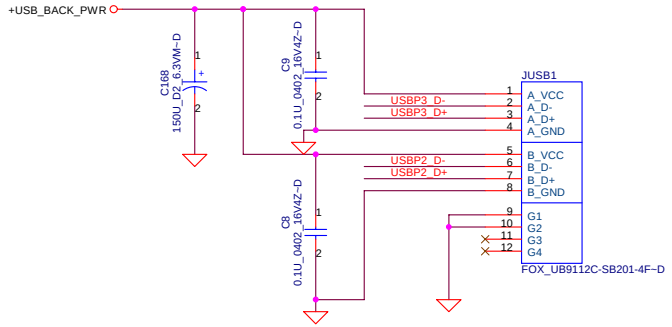

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Compal Electronics, Inc.

Title: USB 2.0 Port

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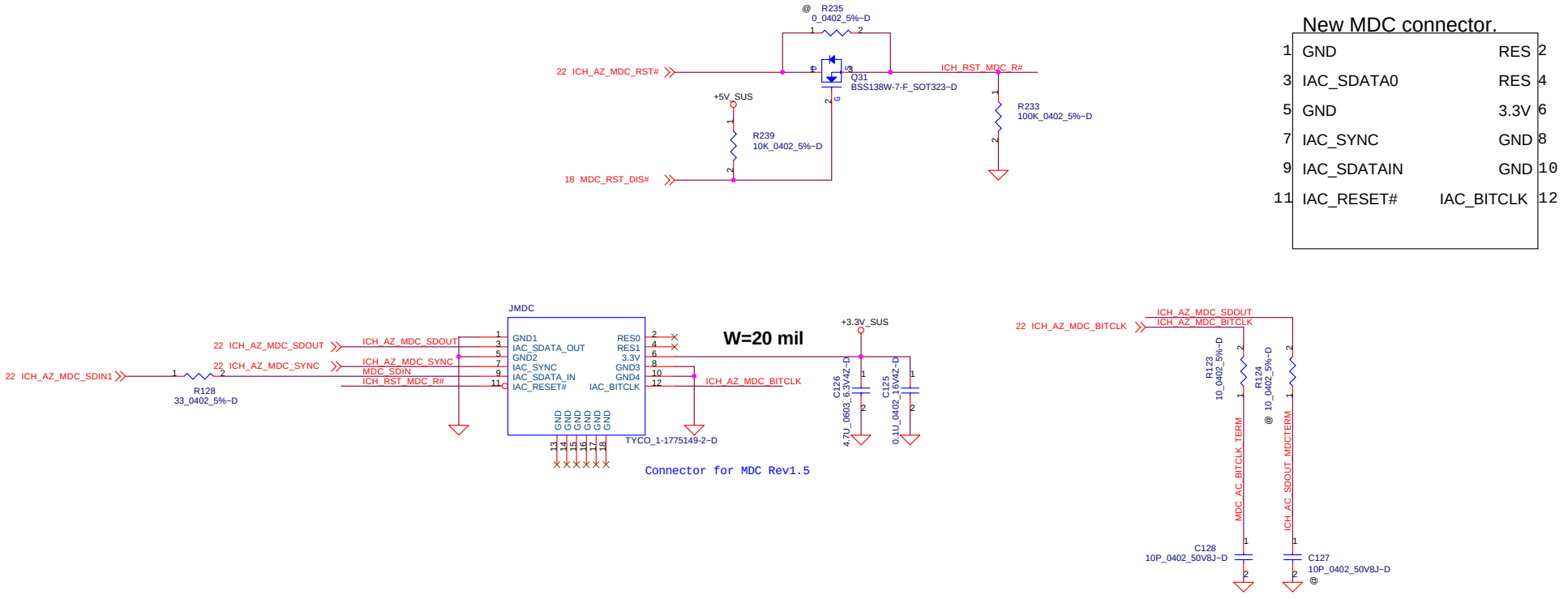
Date: Thursday, March 01, 2007 | Sheet 32 of 66



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Compal Electronics, Inc.

Title: BT PORT and MDC

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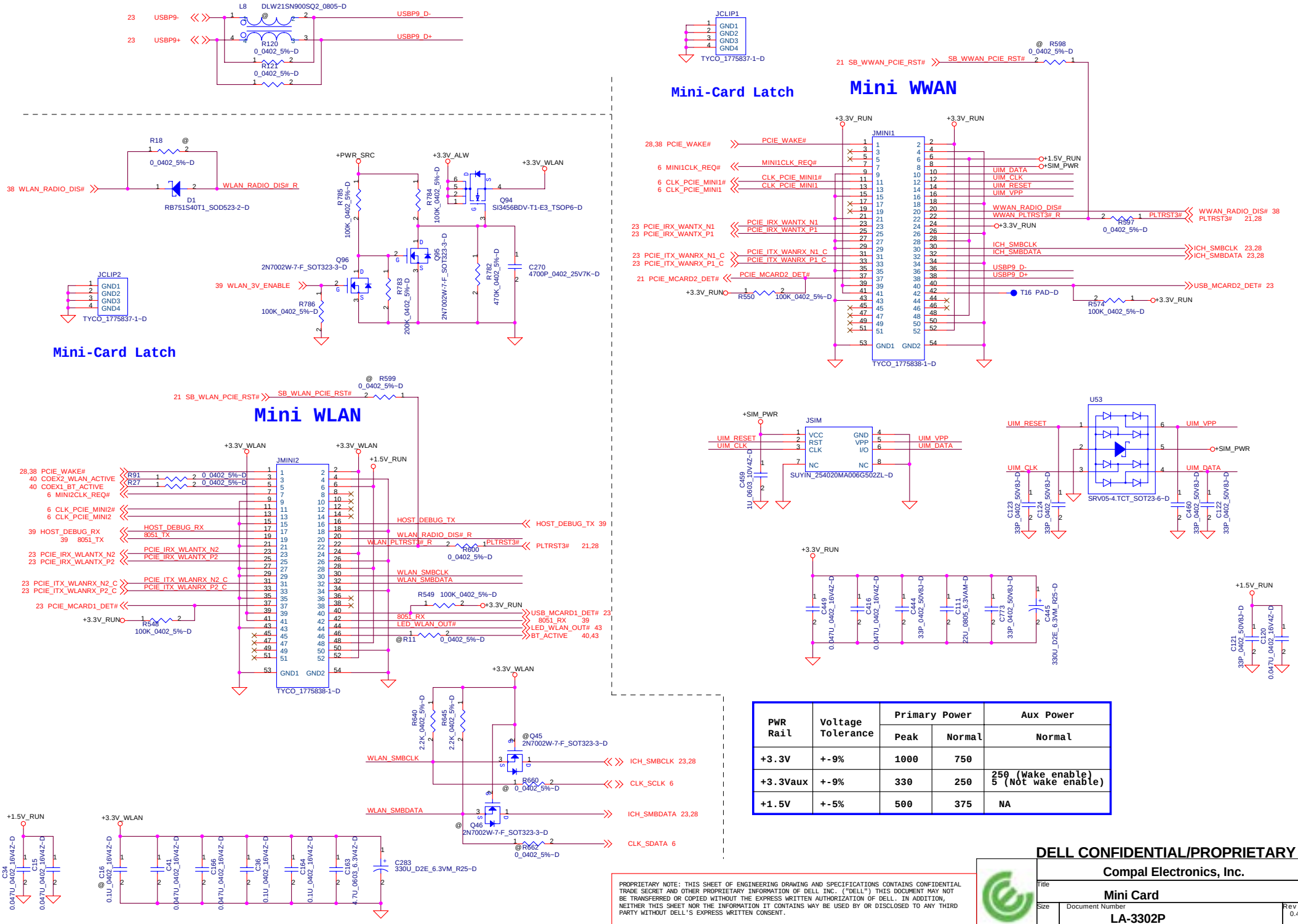
Date: Thursday, March 01, 2007 | Sheet 33 of 66



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

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Compal Electronics, Inc.

Title: Mini Card

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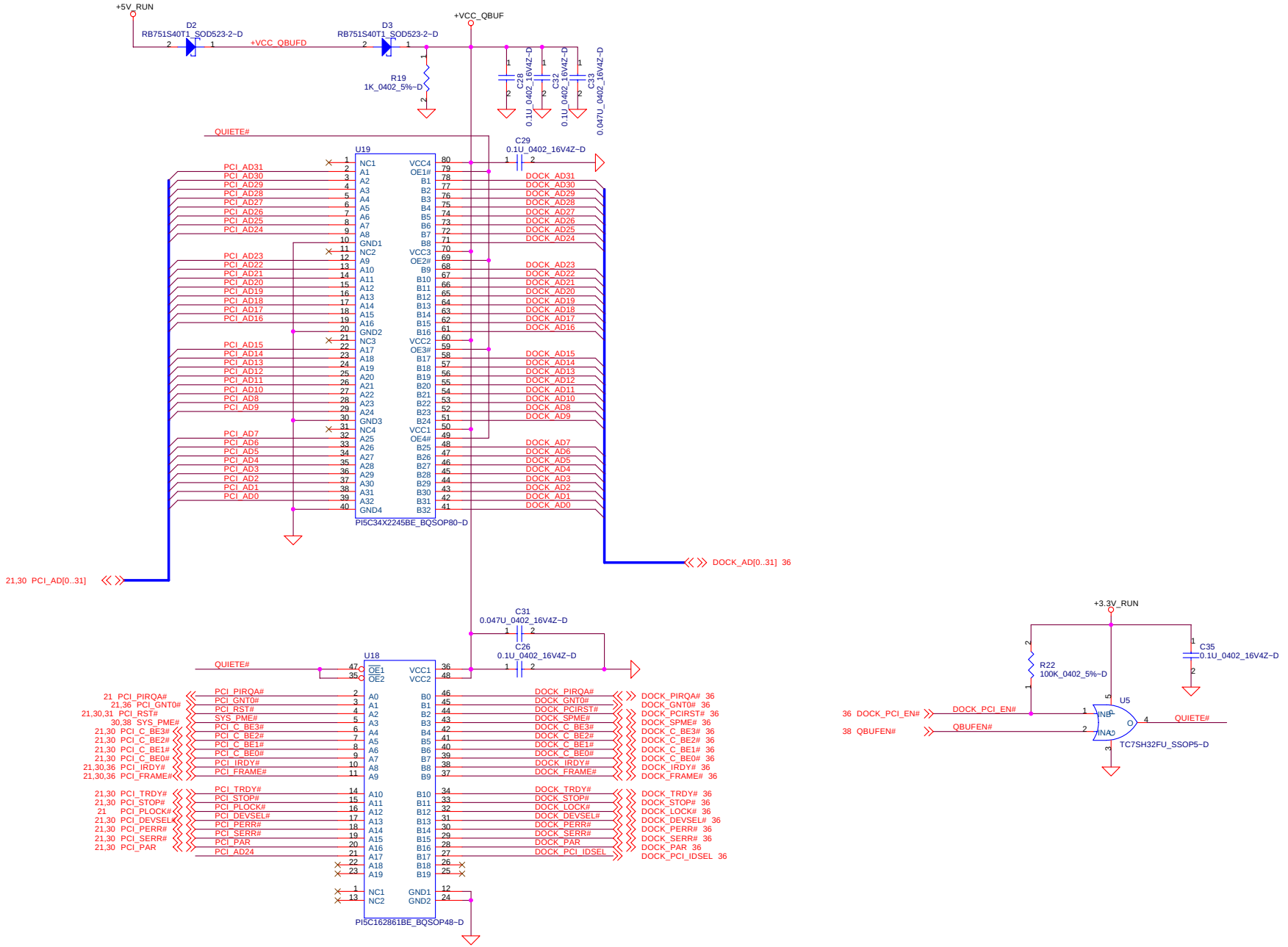
Date: Thursday, March 01, 2007 | Sheet 34 of 66



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Compal Electronics, Inc.

Title: **DOCKING BUFFER**

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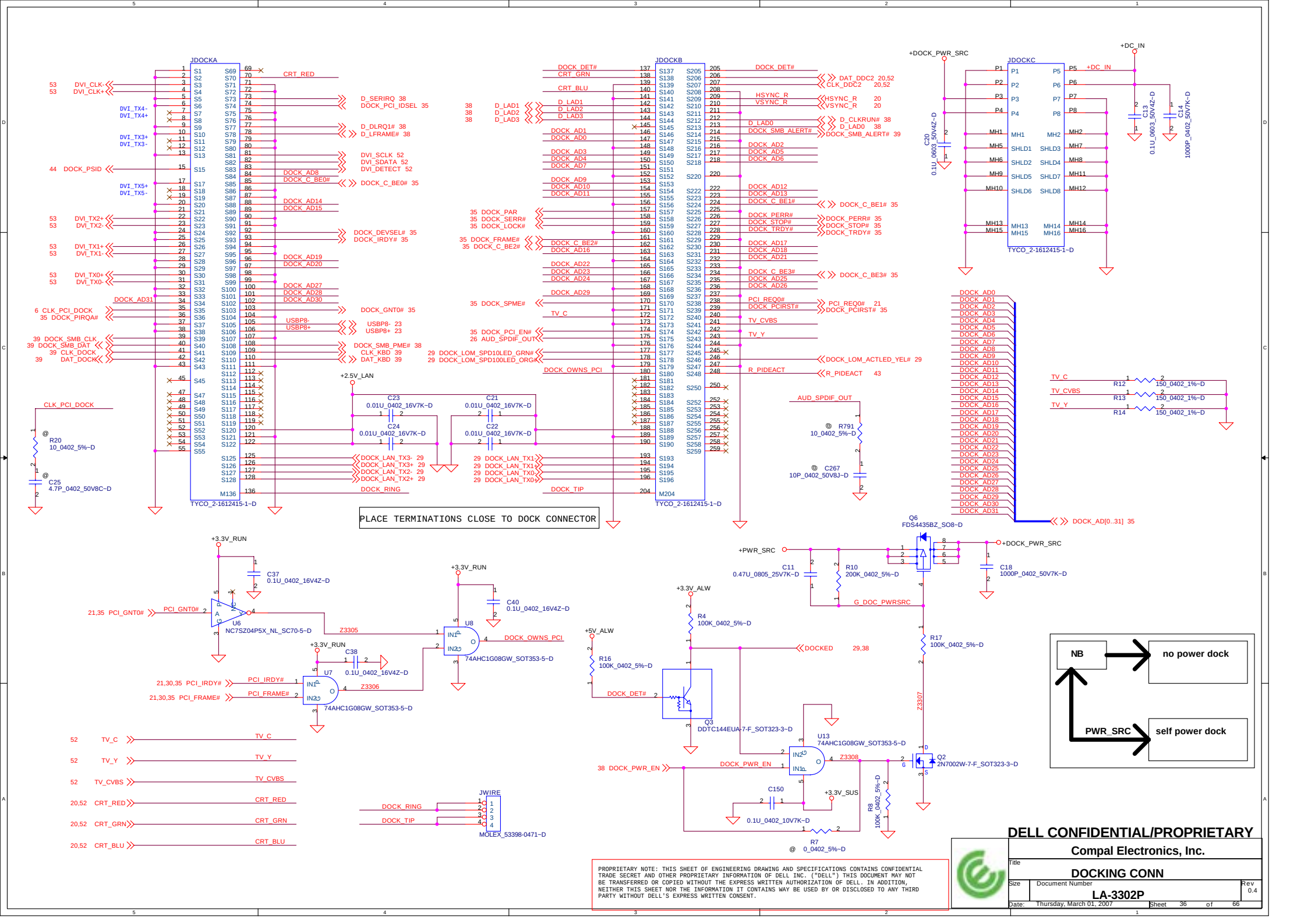

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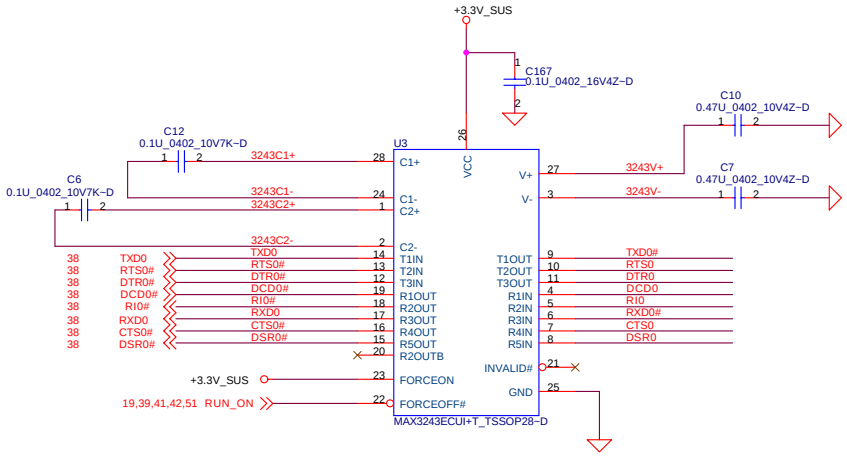

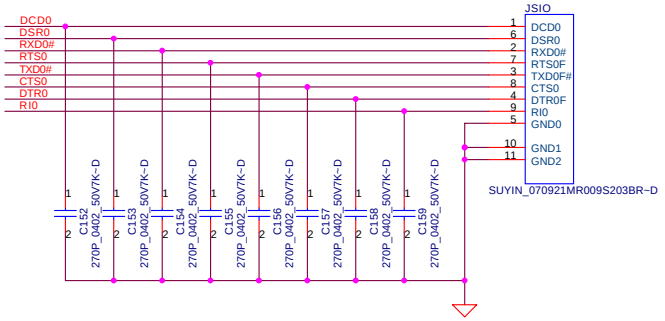

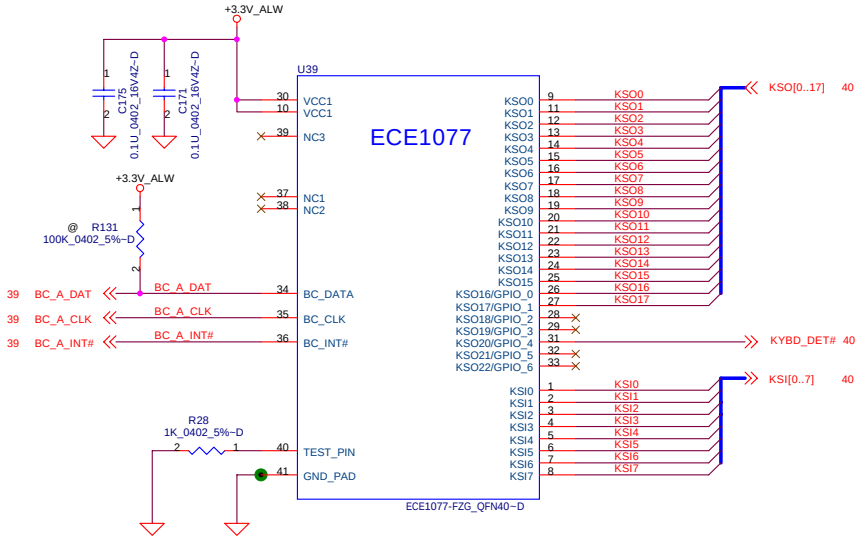

Compal Electronics, Inc.

Title: Serial & FIR

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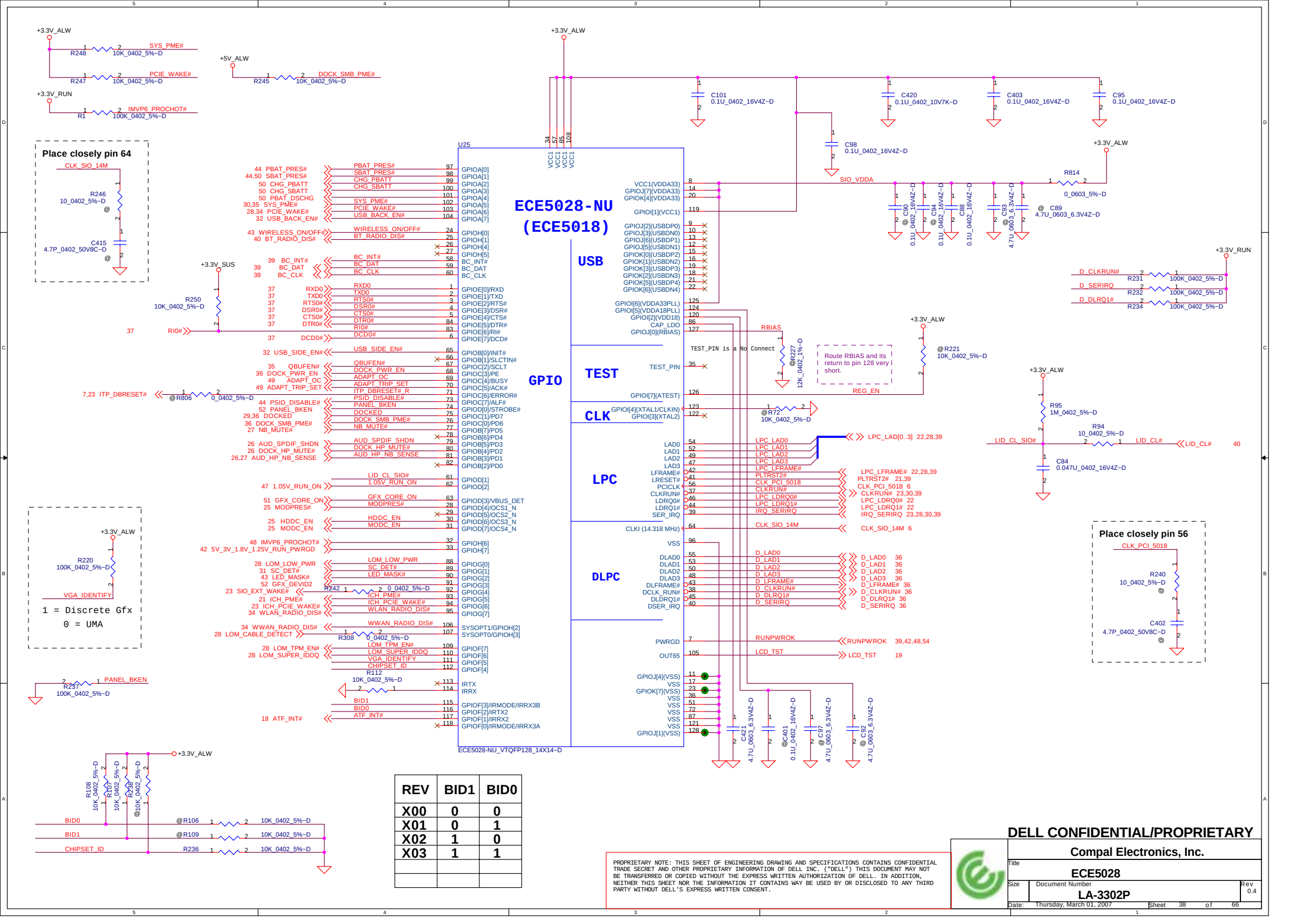

REV	BID1	BID0
X00	0	0
X01	0	1
X02	1	0
X03	1	1

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Compal Electronics, Inc.

Title: ECE5028

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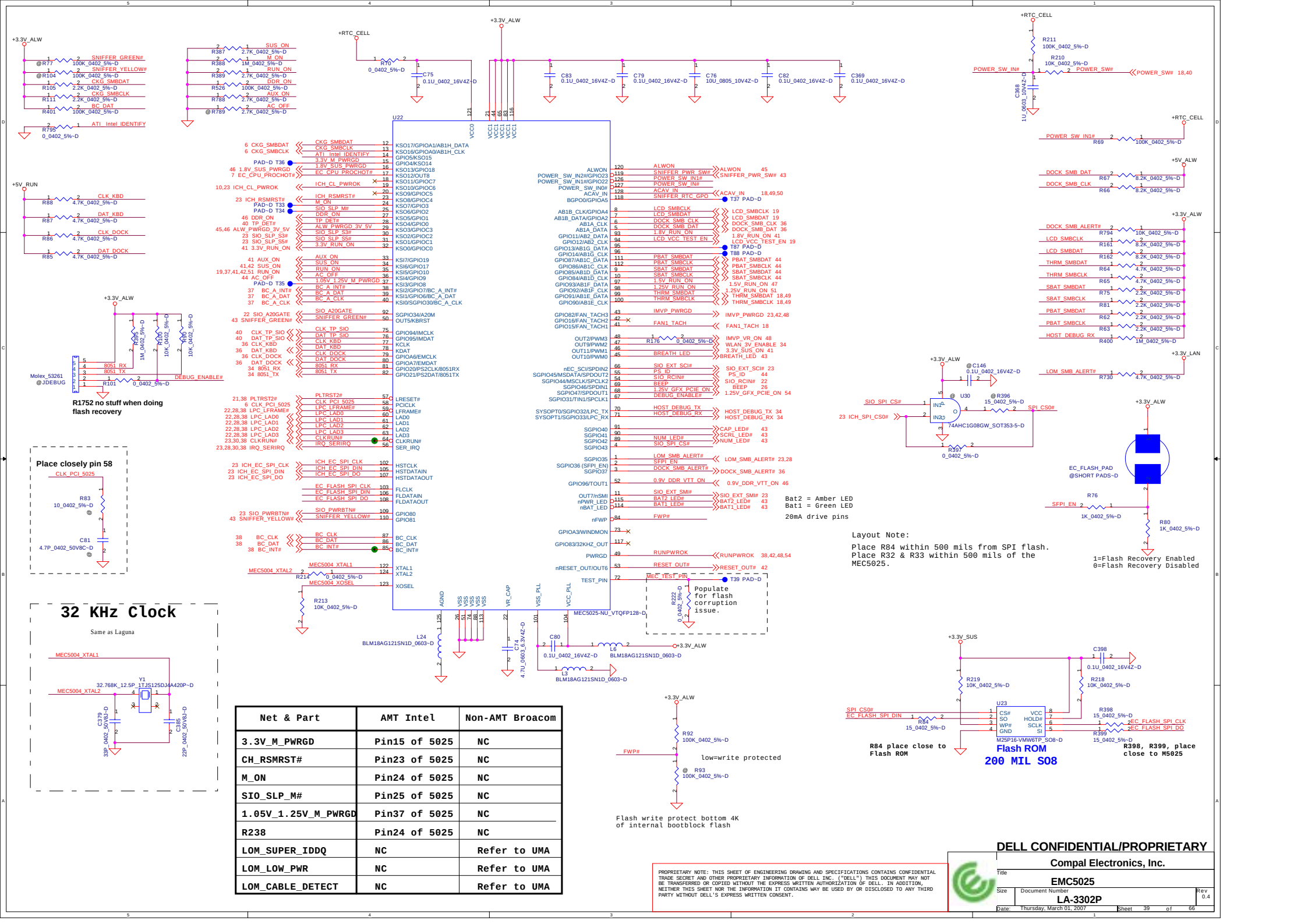

Net & Part	AMT Intel	Non-AMT Broacom
3.3V_M_PWRGD	Pin15 of 5025	NC
CH_RSMRST#	Pin23 of 5025	NC
M_ON	Pin24 of 5025	NC
SIO_SLP_M#	Pin25 of 5025	NC
1.05V_1.25V_M_PWRGD	Pin37 of 5025	NC
R238	Pin24 of 5025	NC
LOM_SUPER_IDDQ	NC	Refer to UMA
LOM_LOW_PWR	NC	Refer to UMA
LOM_CABLE_DETECT	NC	Refer to UMA

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Compal Electronics, Inc.

Title: EMC5025

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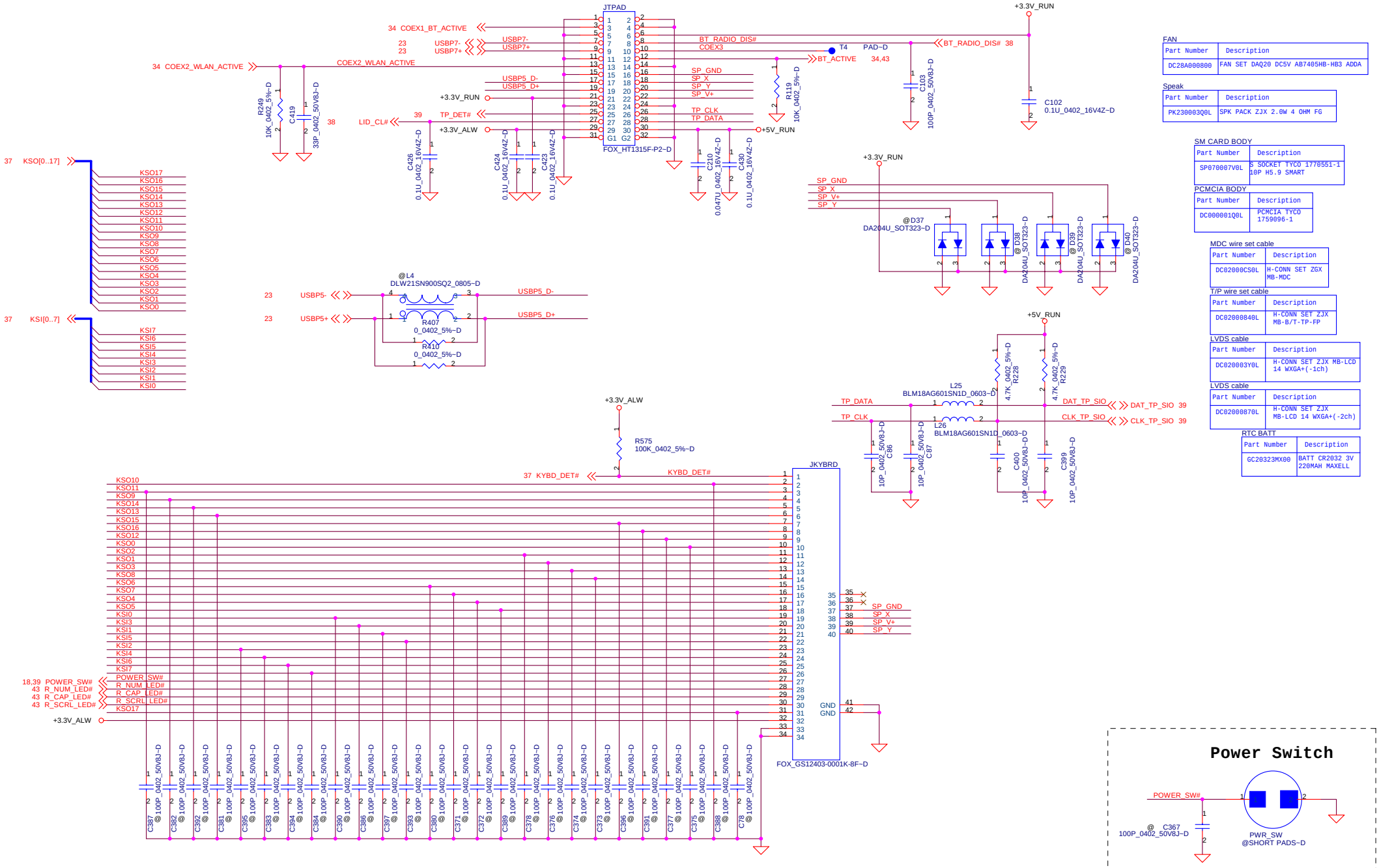
Touch PAD



FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

SM CARD BODY

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

PCMCIA BODY

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

MDC wire set cable

Part Number	Description
DC02000C50L	H-CONN SET ZGX MB-MDC

T/P wire set cable

Part Number	Description
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP

LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+(-1ch)

LVDS cable

Part Number	Description
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+(-2ch)

RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

Power Switch

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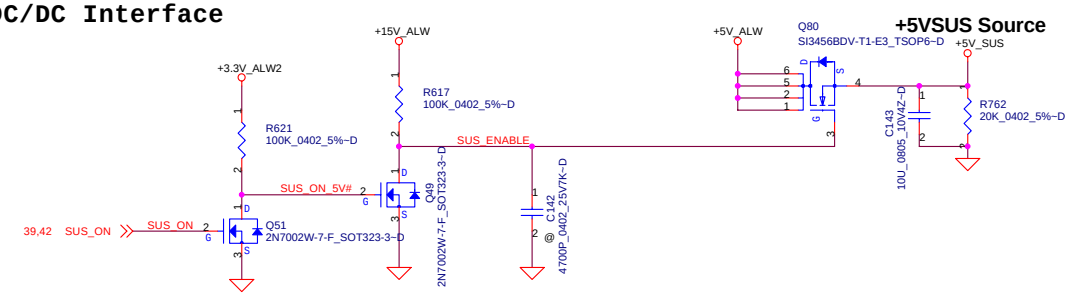
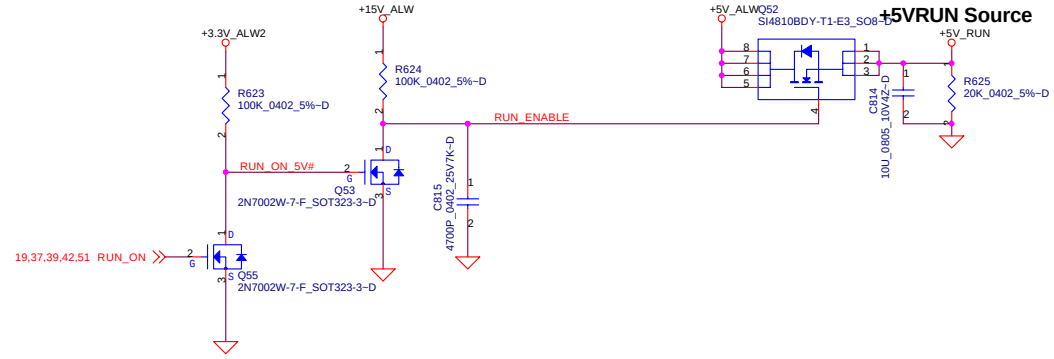
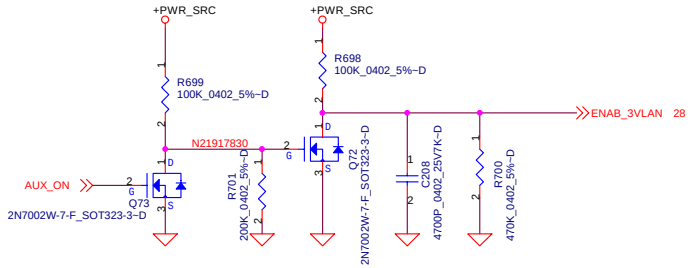
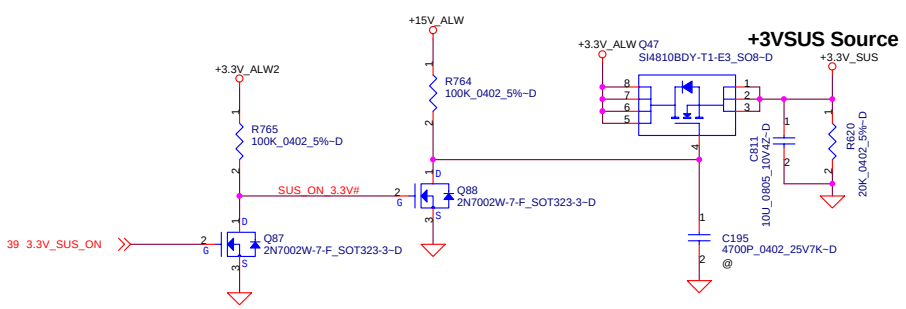
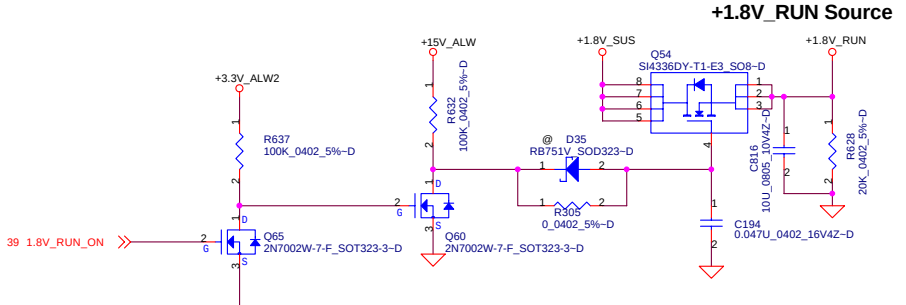
DC/DC Interface

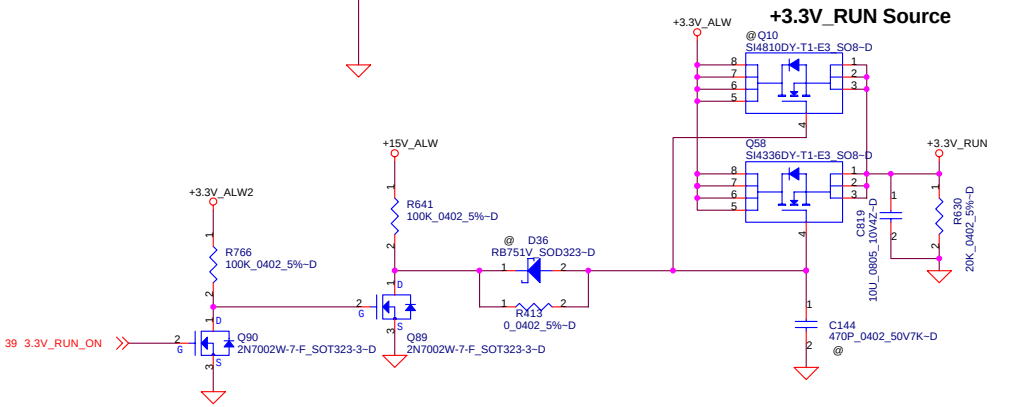


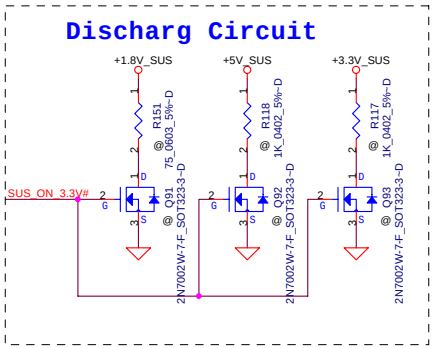


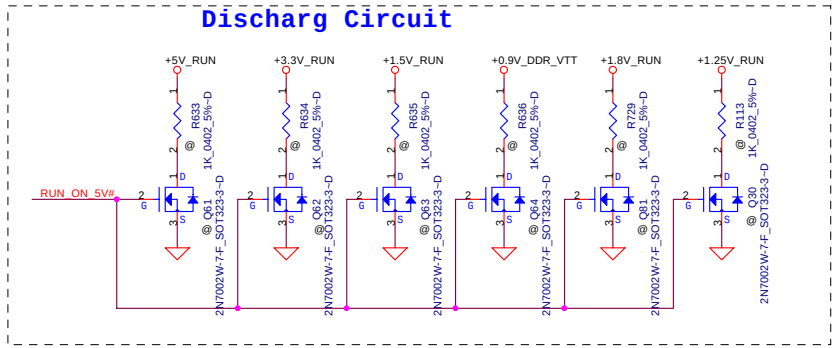












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Compal Electronics, Inc.	
Title	POWER CONTROL
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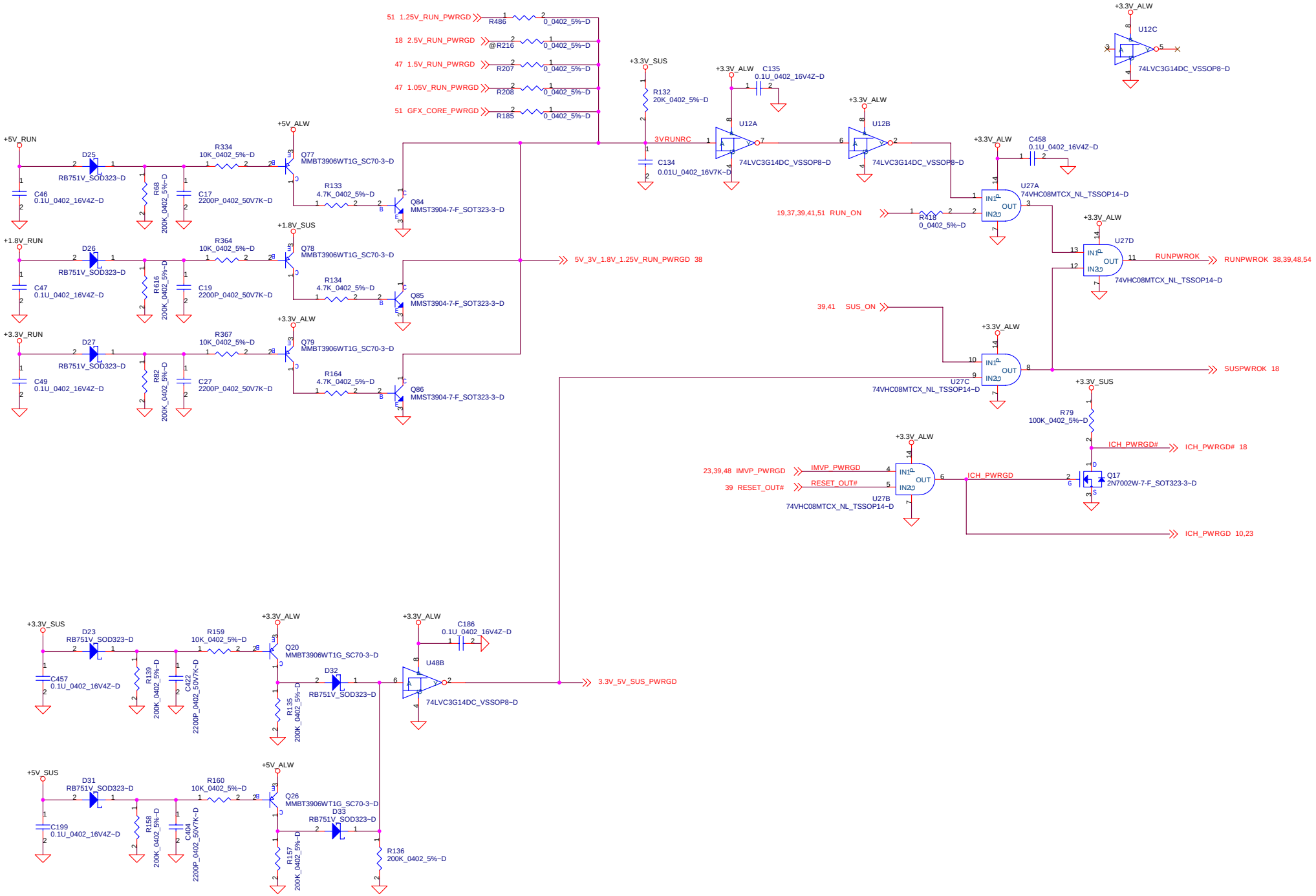

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Compal Electronics, Inc.

Title: Power Good

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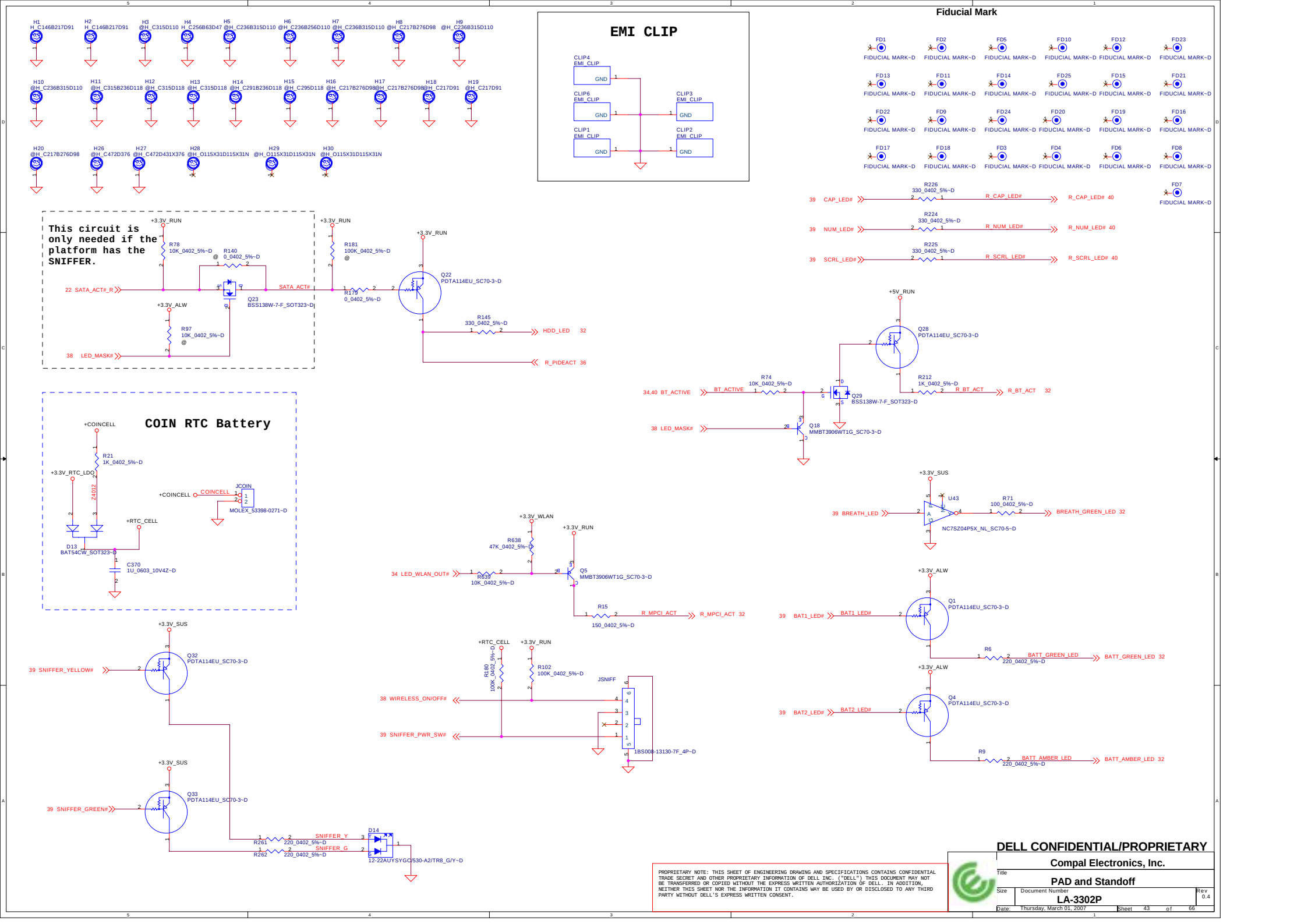
H1 H_C146B217D91
H2 H_C146B217D91
H3 @H_C315D110
H4 H_C256B63D47
H5 @H_C236B315D110
H6 @H_C236B256D110
H7 @H_C236B315D110
H8 @H_C217B276D98
H9 @H_C236B315D110
H10 @H_C236B315D110
H11 @H_C315B236D118
H12 @H_C315D118
H13 @H_C315D118
H14 @H_C291B236D118
H15 @H_C295D118
H16 @H_C217B276D98
H17 @H_C217B276D98
H18 @H_C217D91
H19 @H_C217D91
H20 @H_C217B276D98
H26 @H_C472D376
H27 @H_C472D431X376
H28 @H_O115X31D115X31N
H29 @H_O115X31D115X31N
H30 @H_O115X31D115X31N
EMI CLIP
CLIP4 EMI_CLIP
CLIP6 EMI_CLIP
CLIP3 EMI_CLIP
CLIP1 EMI_CLIP
CLIP2 EMI_CLIP
GND
Fiducial Mark
FD1 FD2 FD5 FD10 FD12 FD23
FD13 FD11 FD14 FD25 FD15 FD21
FD22 FD9 FD24 FD20 FD19 FD16
FD17 FD18 FD3 FD4 FD6 FD8
FD7
FIDUCIAL MARK~D
This circuit is only needed if the platform has the SNIFFER.
+3.3V_RUN
R78 10K_0402_5%~D
R140 @ 0_0402_5%~D
22 SATA_ACT#_R
SATA_ACT#
Q23 BSS138W-7-F_SOT323~D
+3.3V_ALW
R97 10K_0402_5%~D @
38 LED_MASK#
R181 100K_0402_5%~D @
R179 0_0402_5%~D
Q22 PDTA114EU_SC70-3~D
R145 330_0402_5%~D
HDD_LED 32
R_PIDEACT 36
R226 330_0402_5%~D
39 CAP_LED#
R_CAP_LED#
R_CAP_LED# 40
R224 330_0402_5%~D
39 NUM_LED#
R_NUM_LED#
R_NUM_LED# 40
R225 330_0402_5%~D
39 SCRL_LED#
R_SCRL_LED#
R_SCRL_LED# 40
COIN RTC Battery
+COINCELL
R21 1K_0402_5%~D
+3.3V_RTC_LDO
Z4012
JCOIN
MOLEX_53398-0271~D
+RTC_CELL
D13 BAT54CW_SOT323~D
C370 1U_0603_10V4Z~D
+5V_RUN
Q28 PDTA114EU_SC70-3~D
R74 10K_0402_5%~D
34,40 BT_ACTIVE
Q29 BSS138W-7-F_SOT323~D
R212 1K_0402_5%~D
R_BT_ACT
R_BT_ACT 32
Q18 MMBT3906WT1G_SC70-3~D
+3.3V_WLAN
R638 47K_0402_5%~D
34 LED_WLAN_OUT#
R639 10K_0402_5%~D
Q5 MMBT3906WT1G_SC70-3~D
R15 150_0402_5%~D
R_MPCI_ACT
R_MPCI_ACT 32
+3.3V_SUS
U43 NC7SZ04P5X_NL_SC70-5~D
39 BREATH_LED
R71 100_0402_5%~D
BREATH_GREEN_LED 32
+3.3V_ALW
Q1 PDTA114EU_SC70-3~D
39 BAT1_LED#
R6 220_0402_5%~D
BATT_GREEN_LED
BATT_GREEN_LED 32
Q4 PDTA114EU_SC70-3~D
39 BAT2_LED#
R9 220_0402_5%~D
BATT_AMBER_LED
BATT_AMBER_LED 32
Q32 PDTA114EU_SC70-3~D
39 SNIFFER_YELLOW#
Q33 PDTA114EU_SC70-3~D
39 SNIFFER_GREEN#
R261 220_0402_5%~D
SNIFFER_Y
R262 220_0402_5%~D
SNIFFER_G
D14 12-22AUYSYGC/S30-A2/TR8_G/Y~D
+RTC_CELL
+3.3V_RUN
R180 100K_0402_5%~D
R102 100K_0402_5%~D
JSNIFF
38 WIRELESS_ON/OFF#
39 SNIFFER_PWR_SW#
1BS008-13130-7F_4P~D
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Compal Electronics, Inc.
Title
PAD and Standoff
Size
Document Number
LA-3302P
Rev 0.4
Date: Thursday, March 01, 2007
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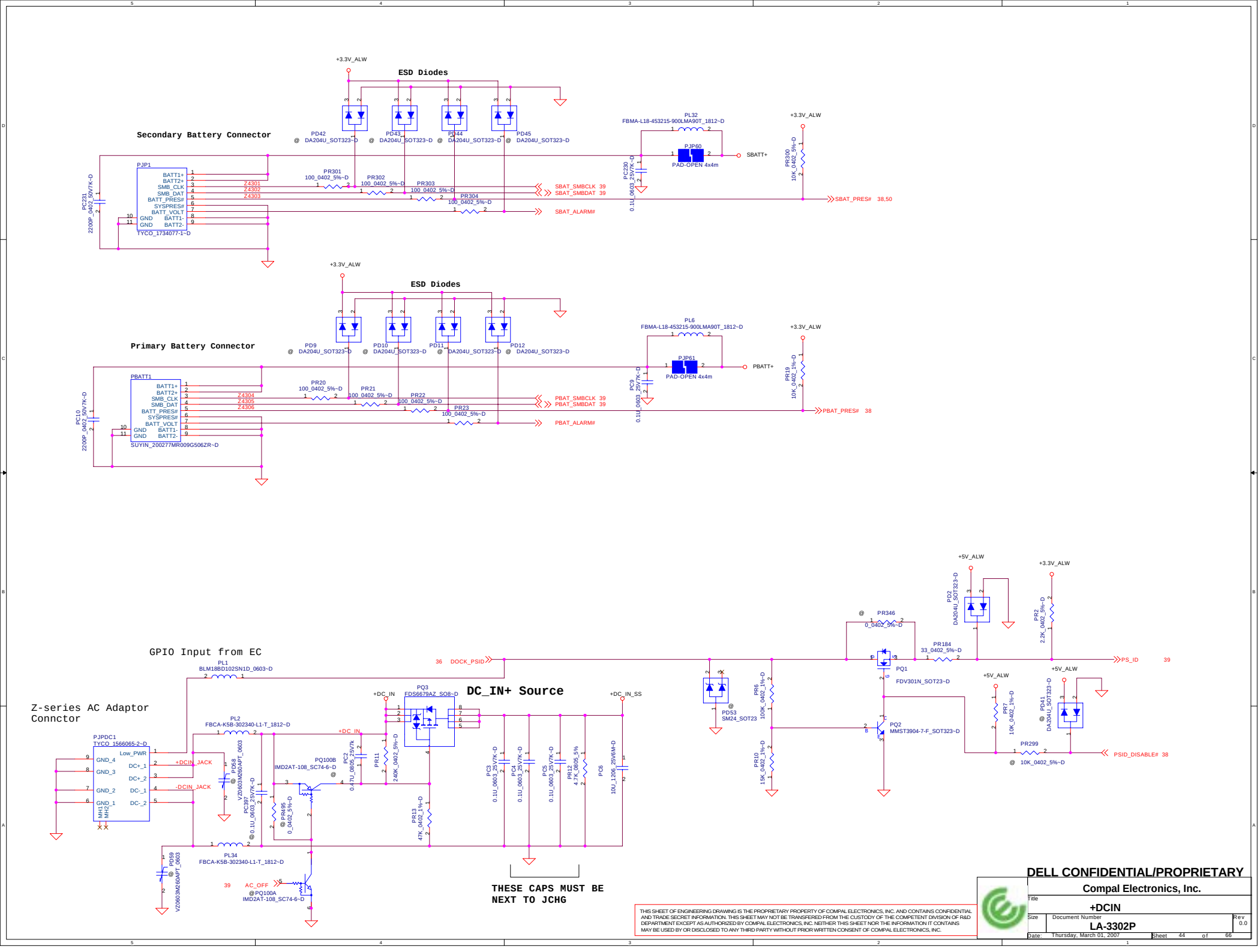

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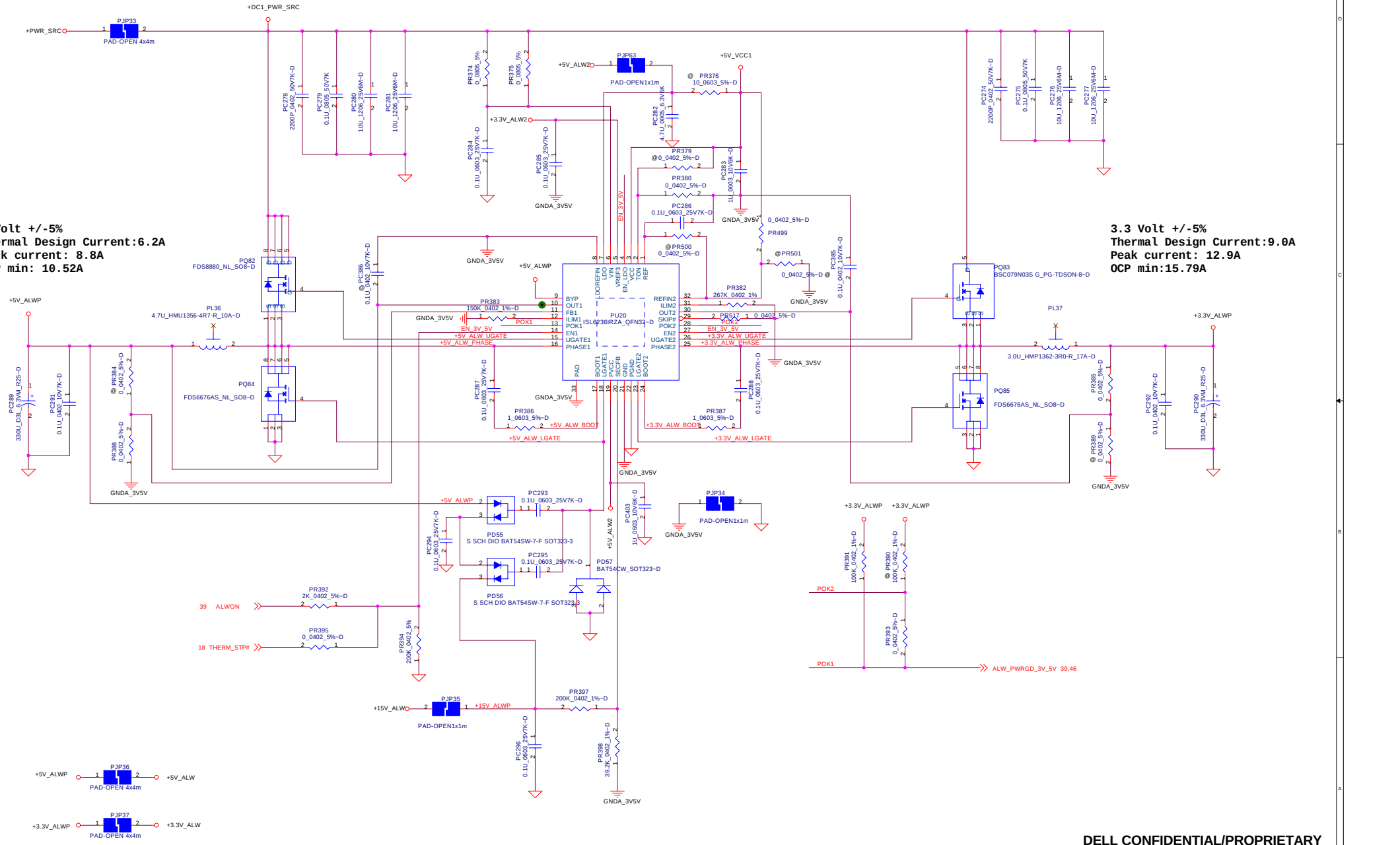
Compal Electronics, Inc.

Title	+DCIN	
Size	Document Number LA-3302P	Rev 0.0
Date: Thursday, March 01, 2007	Sheet 44 of 66	

+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP

5 Volt +/-5%
Thermal Design Current:6.2A
Peck current: 8.8A
OCP min: 10.52A

3.3 Volt +/-5%
Thermal Design Current:9.0A
Peak current: 12.9A
OCP min:15.79A

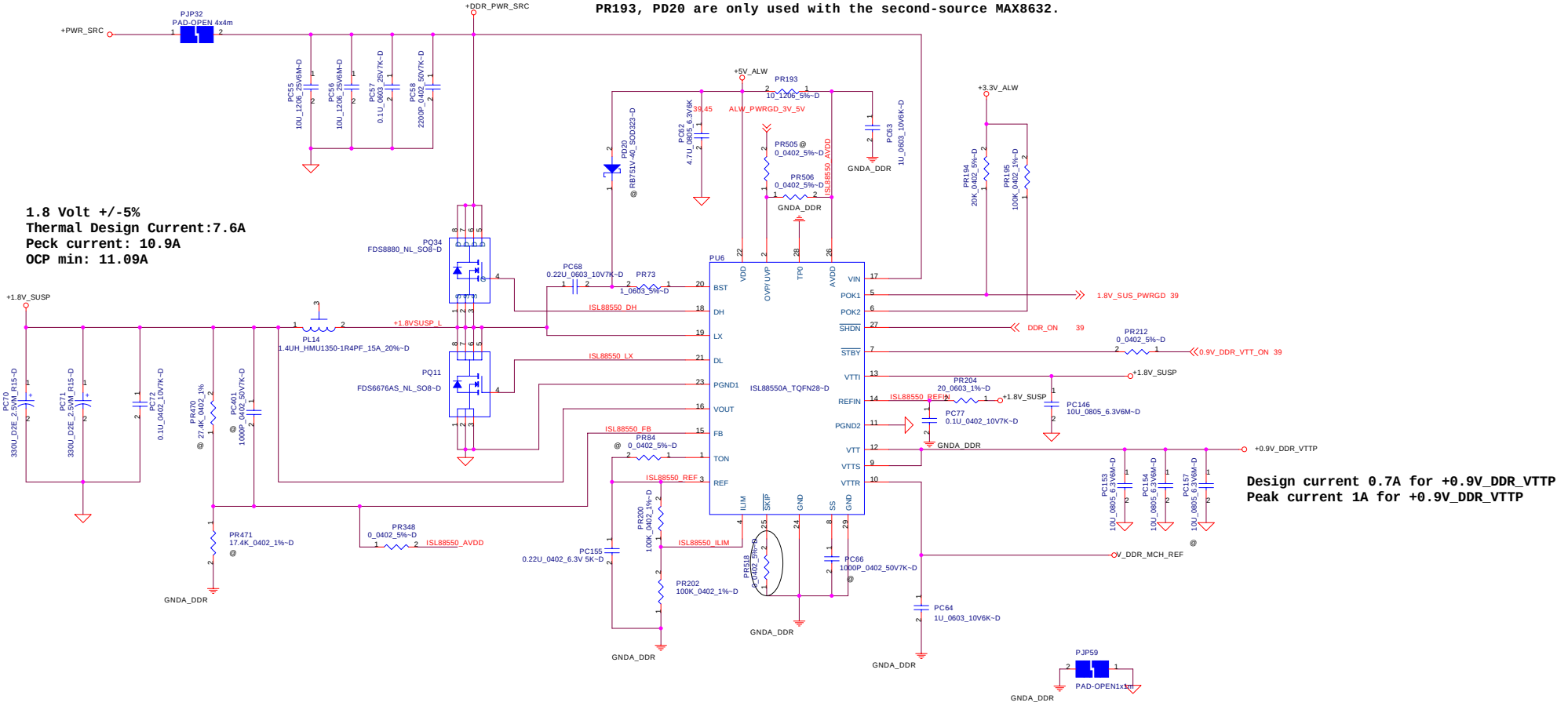


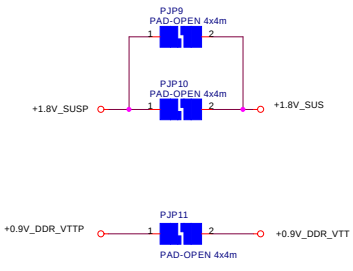
Compal Electronics, Inc.		
Title: DC/DC +3V/ +5V		
Size	Document Number: LA-3302P	Rev: 0.0
Date: Thursday, March 01, 2007	Sheet 45 of 66	

+1.8VSUSP/ +0.9V_DDR_VTT

DDR2 Termination

PR193, PD20 are only used with the second-source MAX8632.





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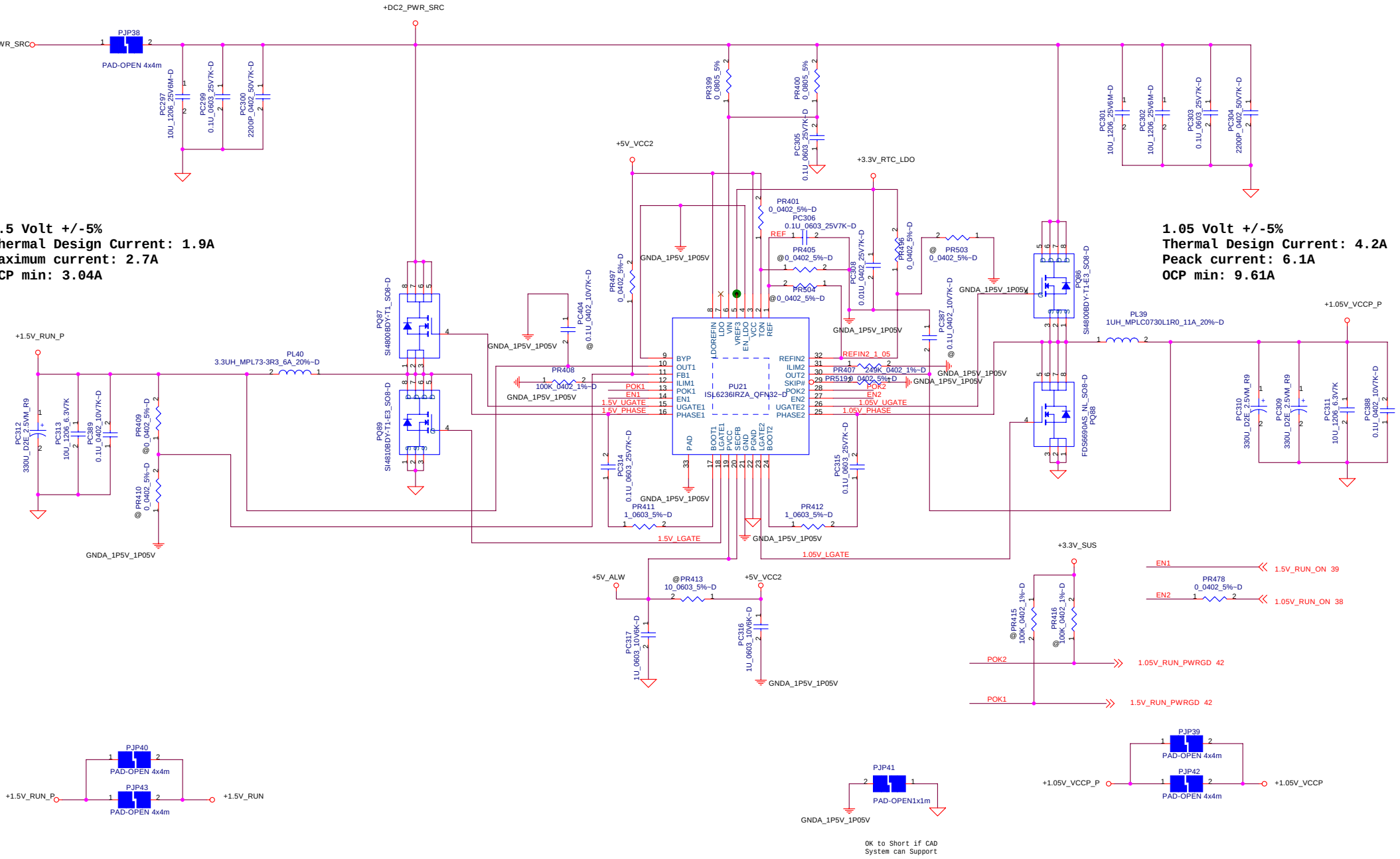
Compal Electronics, Inc.

Title	+1.8VSUSP/ +0.9V_DDR_VT	
Size	Document Number LA-3302P	Rev 0.0
Date: Thursday, March 01, 2007	Sheet 46 of 66	

+1.5V_RUN / +1.05V_VCCP / +3.3V_ALW / +3.3V_RTC_LDO

1.5 Volt +/-5%
Thermal Design Current: 1.9A
Maximum current: 2.7A
OCP min: 3.04A

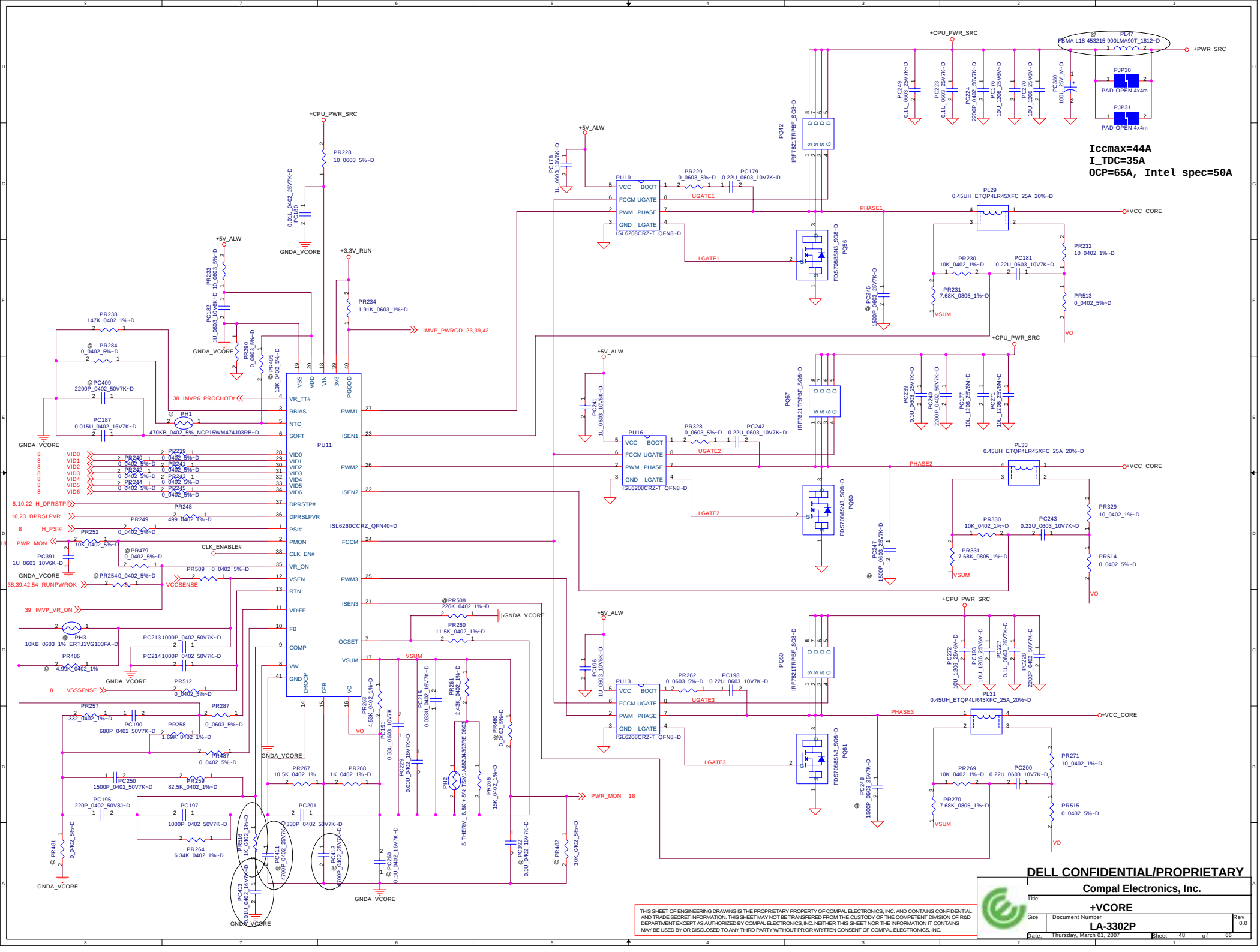
1.05 Volt +/-5%
Thermal Design Current: 4.2A
Peack current: 6.1A
OCP min: 9.61A



OK to Short if CAD System can Support

Compal Electronics, Inc.

Title	+1.5V_RUN / +1.05V_VCCP	
Size	Document Number LA-3302P	Rev 0.0
Date: Thursday, March 01, 2007	Sheet 47 of 66	


Iccmax=44A
I_TDC=35A
OCP=65A, Intel spec=50A
+CPU_PWR_SRC
+PWR_SRC
+5V_ALW
+3.3V_RUN
+VCC_CORE
GNDA_VCORE
PU11
ISL6260CCRZ_QFN40~D
PU10
PU16
PU13
ISL6208CRZ-T_QFN8~D
PQ42
PQ56
PQ57
PQ60
PQ61
PQ50
IRF7821TRPBF_SO8~D
FDS7088SN3_SO8~D
PL29
PL33
PL31
0.45UH_ETQP4LR45XFC_25A_20%~D
PJP30
PJP31
PAD-OPEN 4x4m
IMVP_PWRGD 23,39,42
38 IMVP6_PROCHOT#
39 IMVP_VR_ON
38,39,42,54 RUNPWROK
8,10,22 H_DPRSTP#
10,23 DPRSLPVR
8 H_PSI#
18 PWR_MON
CLK_ENABLE#
8 VSSSENSE
VCCSENSE
VSUM
VO
PHASE1
PHASE2
PHASE3
UGATE1
UGATE2
UGATE3
LGATE1
LGATE2
LGATE3
VID0
VID1
VID2
VID3
VID4
VID5
VID6
PWM1
PWM2
PWM3
ISEN1
ISEN2
ISEN3
OCSET
DROOP
DFB
PGOOD
VR_TT#
RBIAS
NTC
SOFT
DPRSTP#
DPRSLPVR
PSI#
PMON
CLK_EN#
VR_ON
VSEN
RTN
VDIFF
FB
COMP
VW
GND
VSS
VDD
VIN
3V3
PR228 10_0603_5%~D
PR233 10_0603_5%~D
PR234 1.91K_0603_1%~D
PR238 147K_0402_1%~D
PR284 0_0402_5%~D
PC409 2200P_0402_50V7K~D
PC187 0.015U_0402_16V7K~D
470KB_0402_5%_NCP15WM474J03RB~D
PR290 0_0603_5%~D
PR485 13K_0402_5%~D
PC180 0.01U_0402_25V7K~D
PC182 1U_0603_10V6K~D
PR229 0_0603_5%~D
PC179 0.22U_0603_10V7K~D
PC178 1U_0603_10V6K~D
PR230 10K_0402_1%~D
PC181 0.22U_0603_10V7K~D
PR231 7.68K_0805_1%~D
PR232 10_0402_1%~D
PR513 0_0402_5%~D
PC246 1500P_0603_25V7K~D
PR328 0_0603_5%~D
PC242 0.22U_0603_10V7K~D
PC241 1U_0603_10V6K~D
PR330 10K_0402_1%~D
PC243 0.22U_0603_10V7K~D
PR331 7.68K_0805_1%~D
PR329 10_0402_1%~D
PR514 0_0402_5%~D
PC247 1500P_0603_25V7K~D
PR262 0_0603_5%~D
PC198 0.22U_0603_10V7K~D
PC196 1U_0603_10V6K~D
PR269 10K_0402_1%~D
PC200 0.22U_0603_10V7K~D
PR270 7.68K_0805_1%~D
PR271 10_0402_1%~D
PR515 0_0402_5%~D
PC248 1500P_0603_25V7K~D
PC149 0.1U_0603_25V7K~D
PC223 0.1U_0603_25V7K~D
PC224 2200P_0402_50V7K~D
PC176 10U_1206_25V6M~D
PC270 10U_1206_25V6M~D
PC380 100U_25V_M~D
PC239 0.1U_0603_25V7K~D
PC240 2200P_0402_50V7K~D
PC177 10U_1206_25V6M~D
PC271 10U_1206_25V6M~D
PC272 10U_1206_25V6M~D
PC198 10U_1206_25V6M~D
PC227 0.1U_0603_25V7K~D
PC228 2200P_0402_50V7K~D
PR239 0_0402_5%~D
PR240 0_0402_5%~D
PR241 0_0402_5%~D
PR242 0_0402_5%~D
PR243 0_0402_5%~D
PR244 0_0402_5%~D
PR245 0_0402_5%~D
PR248
PR249 499_0402_1%~D
PR252 0_0402_5%~D
PC391 1U_0603_10V6K~D
PR479 0_0402_5%~D
PR509 0_0402_5%~D
PR254 0_0402_5%~D
PH3 10KB_0603_1%_ERTJ1VG103FA~D
PR486 4.99K_0402_1%
PC213 1000P_0402_50V7K~D
PC214 1000P_0402_50V7K~D
PR512 0_0402_5%~D
PR257 332_0402_1%~D
PR287
PC190 680P_0402_50V7K~D
PR258 1.69K_0402_1%~D
PR487 0_0402_5%~D
PC250 1500P_0402_50V7K~D
PR259 82.5K_0402_1%~D
PC195 220P_0402_50V8J~D
PC197 1000P_0402_50V7K~D
PR264 6.34K_0402_1%~D
PR481 0_0402_5%~D
PR508 226K_0402_1%~D
PR260 11.5K_0402_1%~D
PR283 4.58K_0402_1%~D
PC191 0.33U_0603_10V7K
PC215 0.033U_0402_16V7K~D
PR261 2.43K_0402_1%~D
PR480 0_0402_5%~D
PR267 10.5K_0402_1%
PR268 1K_0402_1%~D
PC229 0.01U_0402_16V7K~D
PH2 8.8K +5% TSM1A682J4302RE 0603
PR260 15K_0402_1%~D
PC201 330P_0402_50V7K~D
PR516 1K_0402_1%~D
PC411 4700P_0402_25V7K~D
PC412 2700P_0402_25V7K~D
PC413 0.01U_0402_16V7K~D
PC260 0.1U_0402_16V7K~D
PC392 0.1U_0402_16V7K~D
PR482 30K_0402_5%~D
PWR_MON 18
GNDA_VCORE
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Compal Electronics, Inc.
+VCORE
LA-3302P
Rev 0.0
Thursday, March 01, 2007
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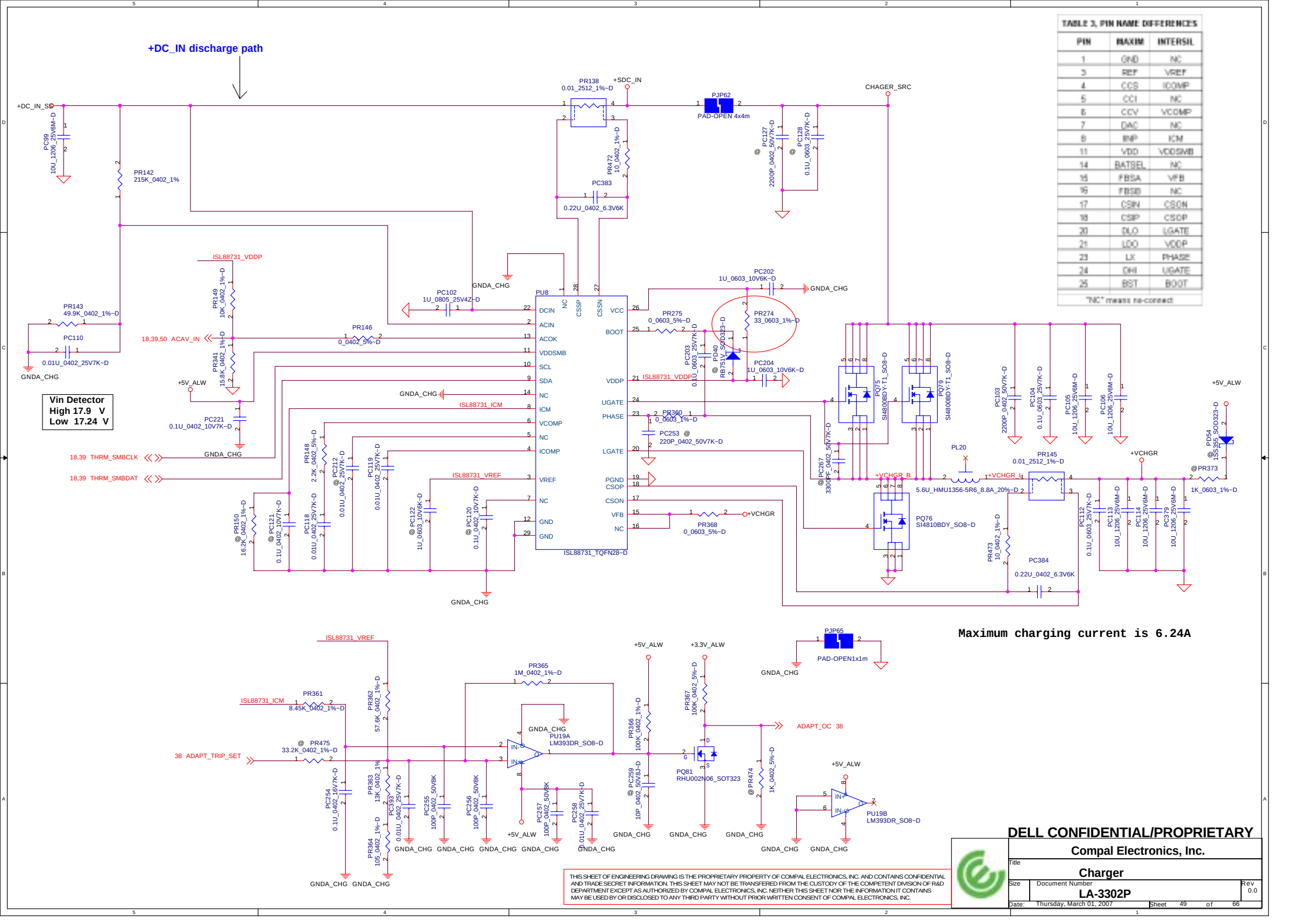
+DC_IN discharge path
TABLE 3, PIN NAME DIFFERENCES
PIN | MAXIM | INTERSIL
1 GND NC
3 REF VREF
4 CCS ICOMP
5 CC1 NC
6 CCV VCOMP
7 DAC NC
8 BNP ICM
11 VDD VDDSMB
14 RATSEL NC
15 FBSA VFB
16 FBSB NC
17 CSN CSON
18 CSP CSOP
20 DLO LGATE
21 LDO VDDP
23 LX PHASE
24 DHI UGATE
25 BST BOOT
"NC" means no-connect
Vin Detector
High 17.9 V
Low 17.24 V
Maximum charging current is 6.24A
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Compal Electronics, Inc.
Charger
LA-3302P
Rev 0.0
Thursday, March 01, 2007
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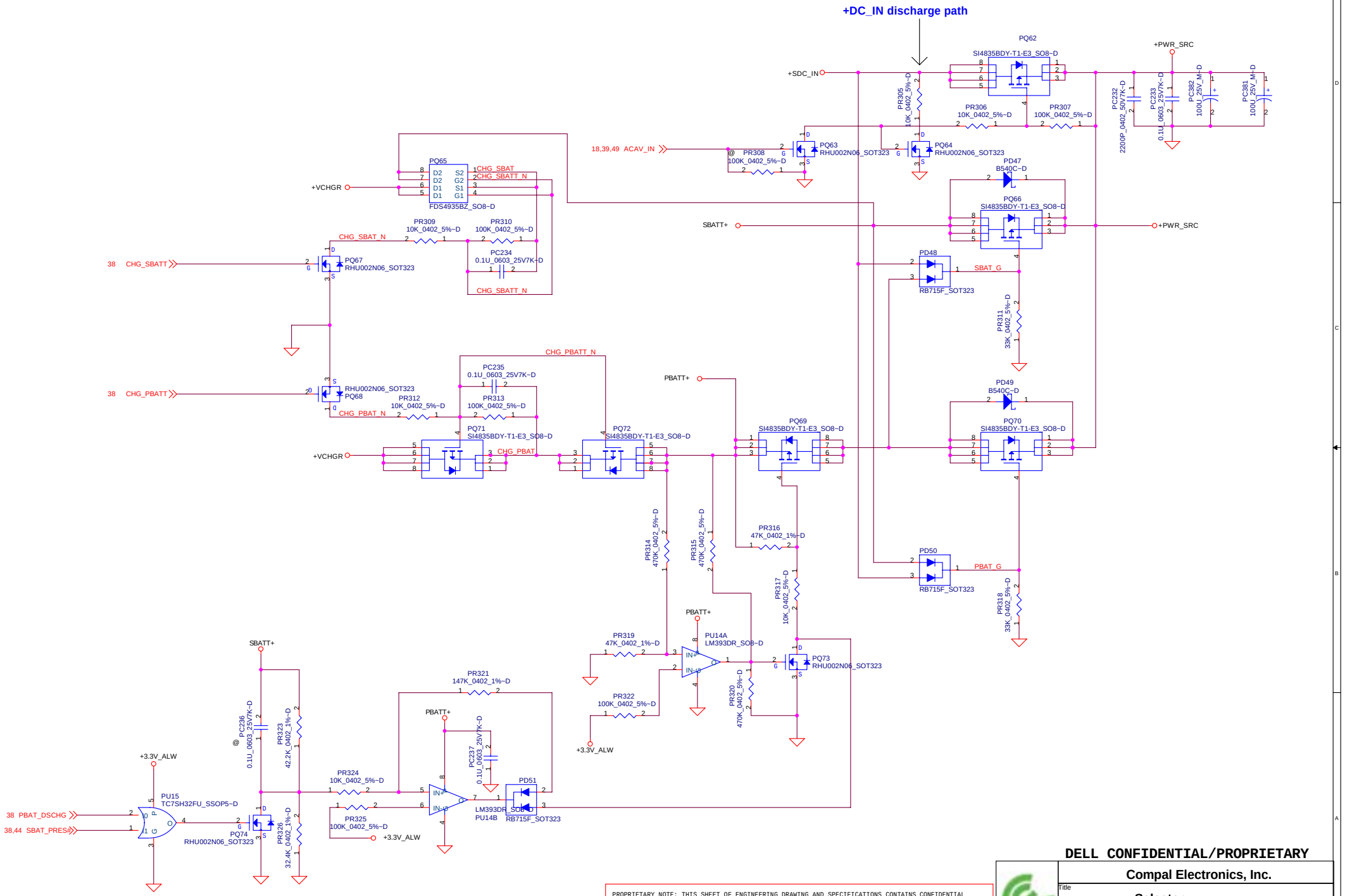

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Title: Selector

Size | Document Number: LA-3302P | Rev: 0.0

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GPU_COREP/ +1.25V_RUN

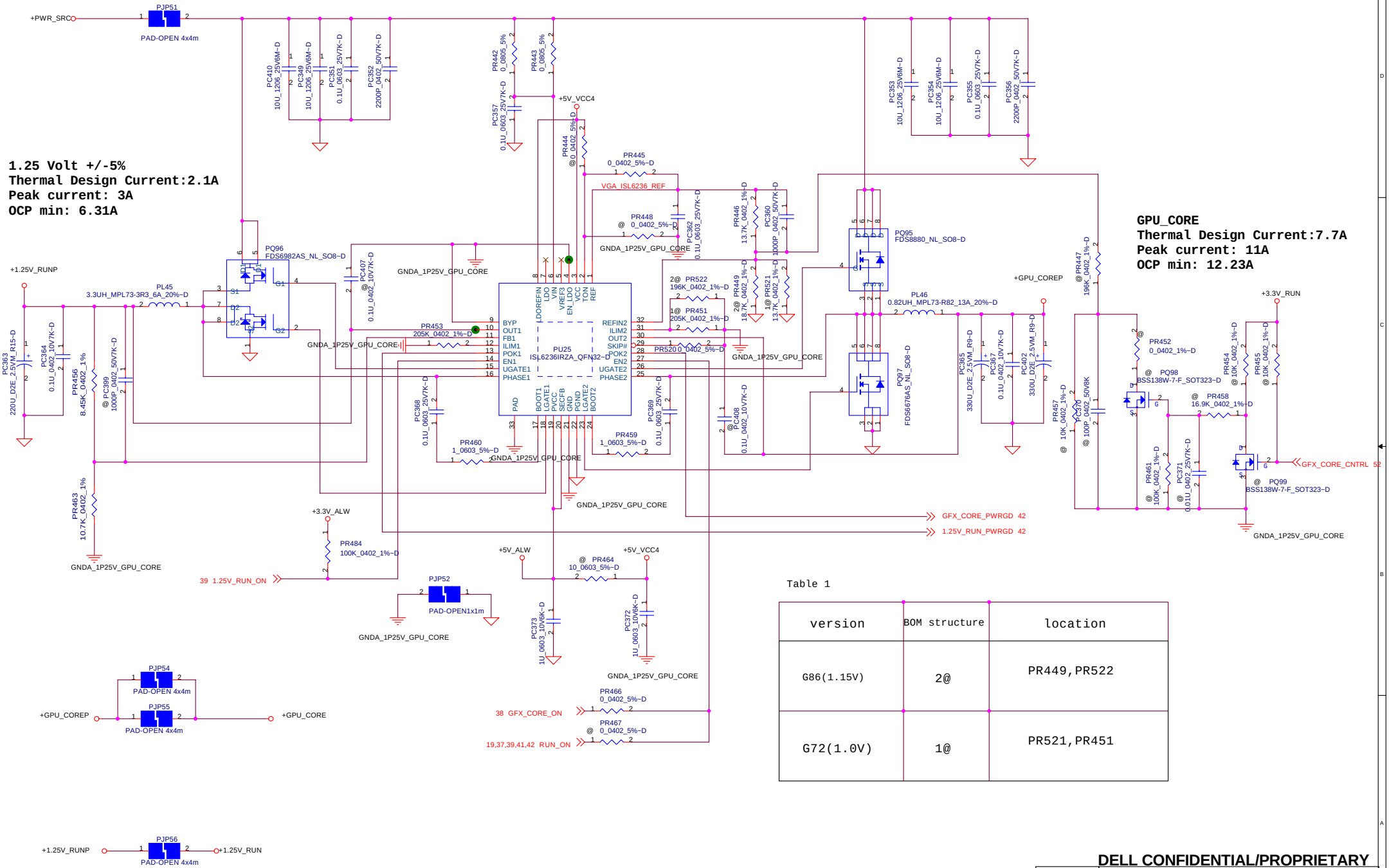

Table 1

version	BOM structure	location
G86(1.15V)	2@	PR449,PR522
G72(1.0V)	1@	PR521,PR451

Compal Electronics, Inc.

Title: PWR_NVG72 +VDD_CORE

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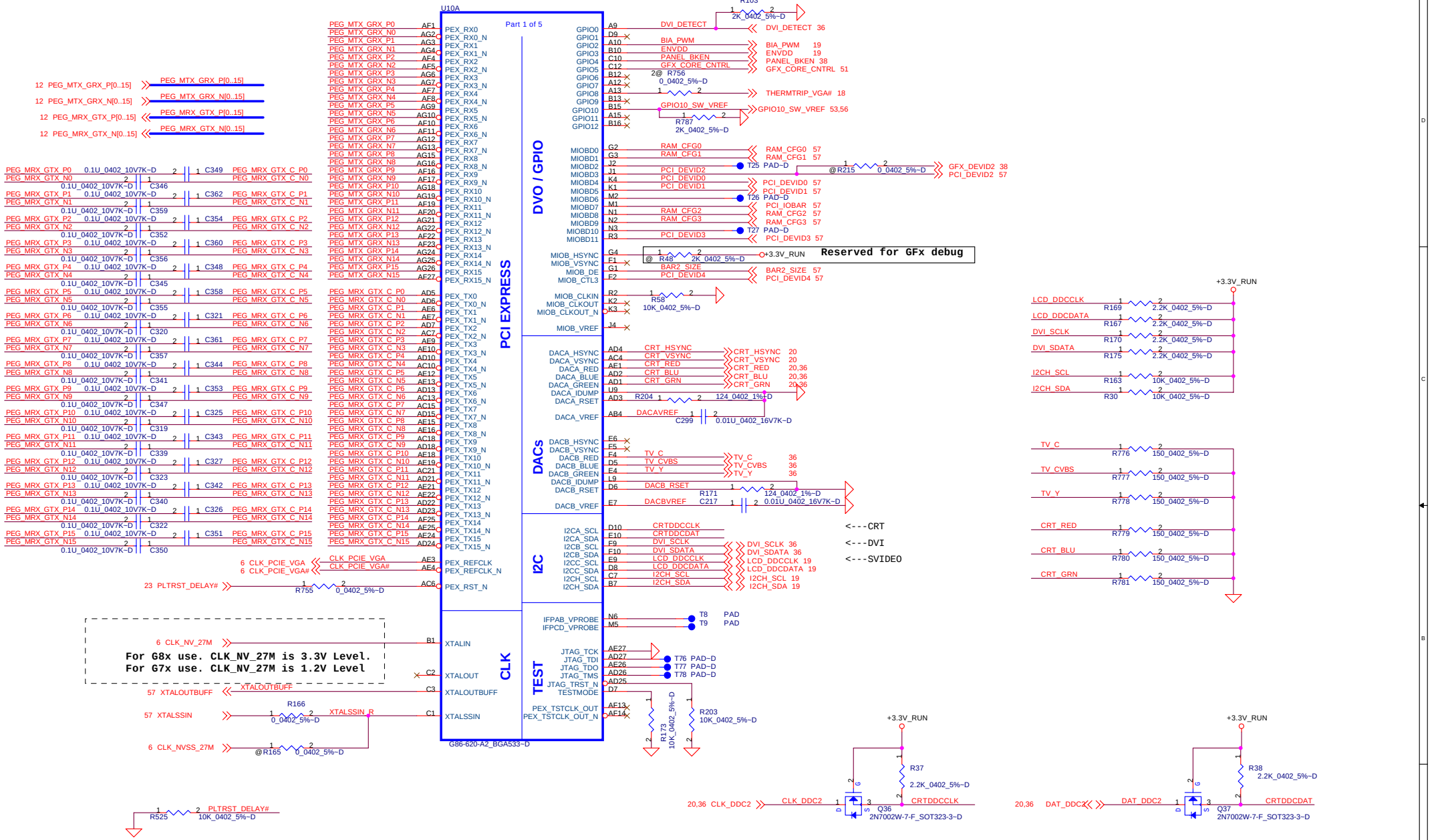
Date: Thursday, March 01, 2007 | Sheet 51 of 66



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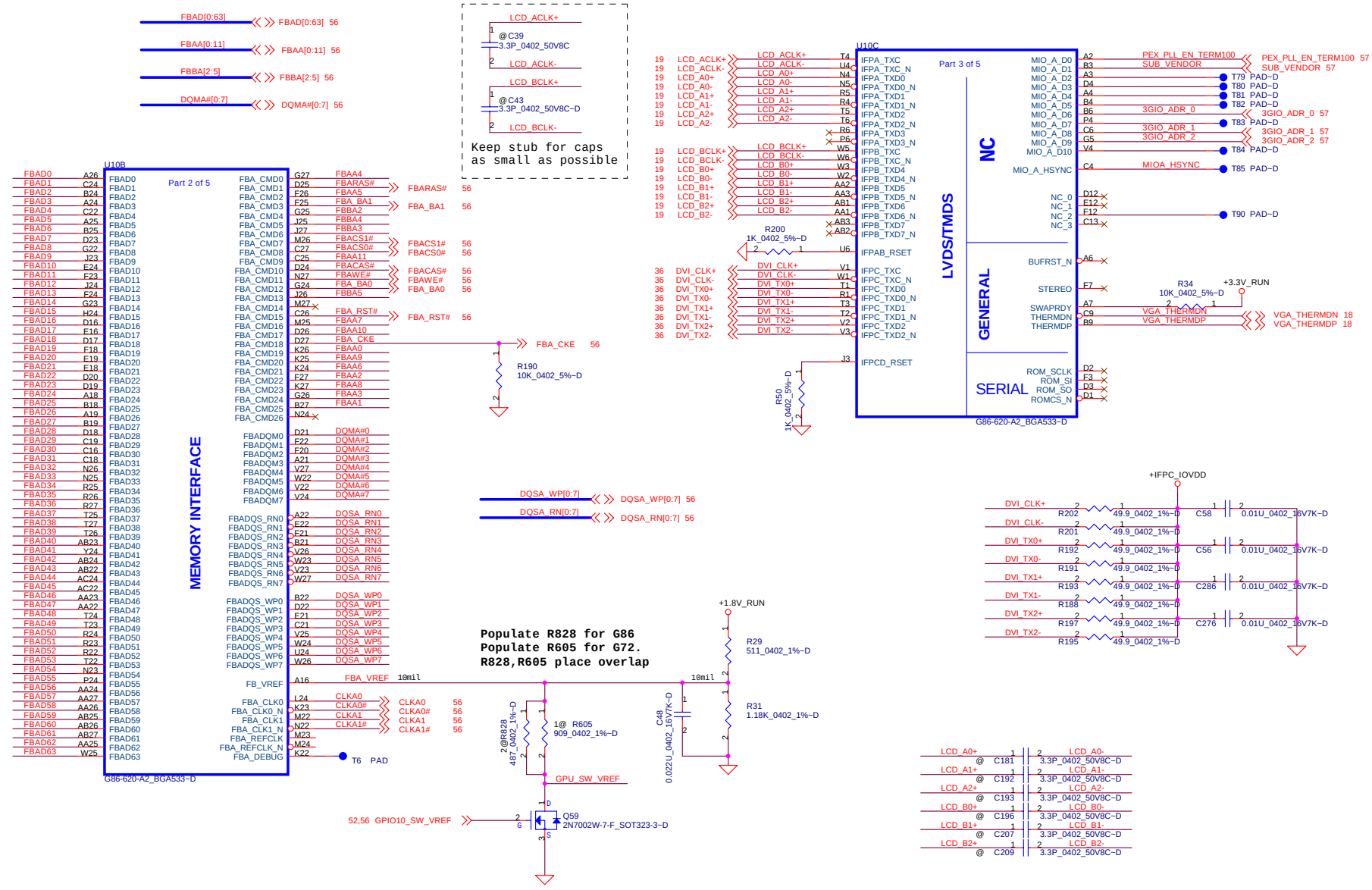
Compal Electronics, Inc.

Title: NVG86 PCIE,GPIO,CLK

Size: | Document Number: LA-3302P | Rev: 0.4

Date: Thursday, March 01, 2007 | Sheet 52 of 66



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Compal Electronics, Inc.	
Title	NVG86 Memory Interface
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+2.5V_RUN for G7x
+1.25V_GFX_PCIE for G8x.

Populate C251, C255 for G86 and G72 solution per Nvidia

For G8x use. NC for G7x

Populate R825 for G72MV
Populate R35 for G86MV.
R825,R35 place overlap

+2.5V_RUN for G7x
+1.8V_RUN for G8x.

+2.5V_RUN for G7x
+1.8V_RUN for G8x.

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Compal Electronics, Inc.	
Title	NVG86 Power
Size	Document Number: LA-3302P
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Date:	Thursday, March 01, 2007
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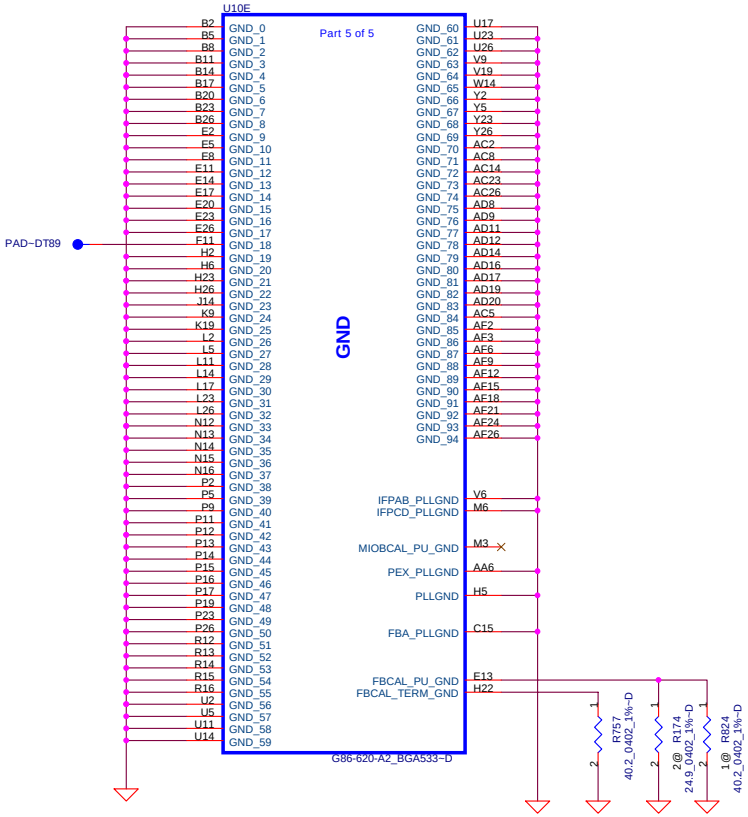

Populate R824 for G72MV
Populate R174 for G86.

R174,R824 place overlap

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Compal Electronics, Inc.	
Title	NVG86 Ground
Size	Document Number: LA-3302P
Rev	0.4
Date: Thursday, March 01, 2007	Sheet 55 of 66

VREF=VDDQ x Rb/(Ra+Rb)
VREF=0.7 x VDDQ for G86 trun on, 0.4x VDDQ when trun off
VREF=0.7 x VDDQ for G72MV trun on, 0.5x VDDQ when trun off

R829,R830 for G86
R402,R403 for G72MV.
R829,R402 and R830,R403 place overlap

R831,R832 for G86
R404,R405 for G72MV.
R831,R404 and R832,R405 place overlap

Populate R827 for G86
Populate R172 for G72MV.

R172,R827 place overlap
and close to U49

Change to 220ohm/100MHz

Populate R826 for G86
Populate R177 for G72MV.

R177,R826 place overlap
and close to U50

Place below decoupling caps close U11 VDD Pins

Place below decoupling caps close U14 VDD Pins

Place below decoupling caps close U11 VDDQ Pins

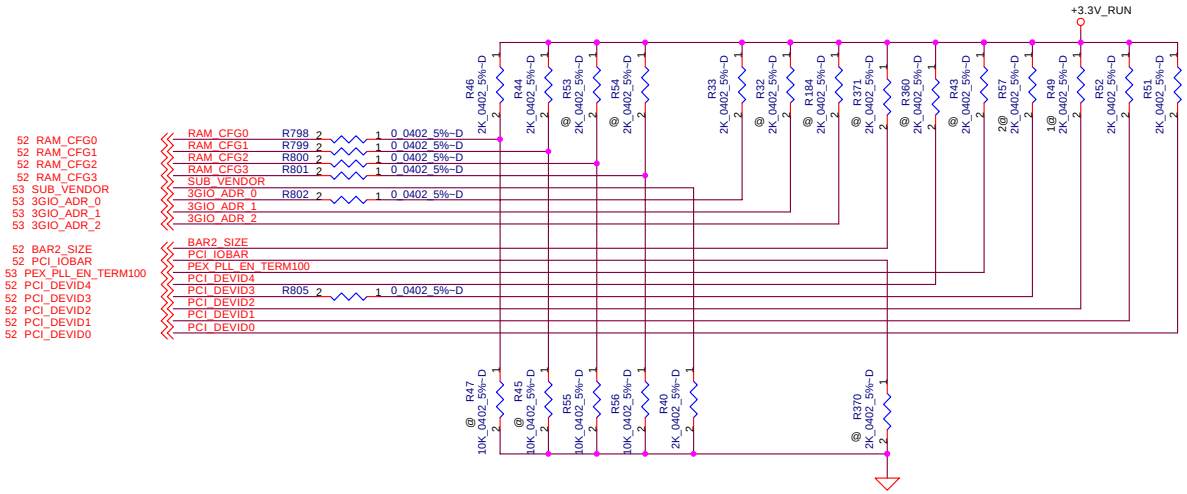
Place below decoupling caps close U14 VDDQ Pins

Compal Electronics, Inc.

Title: NVG86 External DDR

Size: | Document Number: LA-3302P | Rev: 0.4

Date: Thursday, March 01, 2007 | Sheet 56 of 66

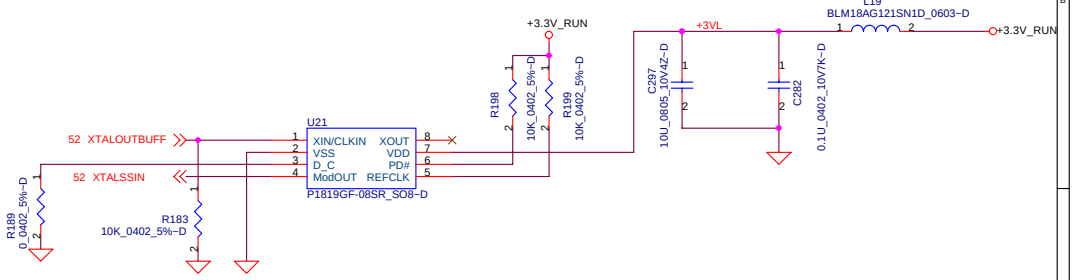


G72MV STRAPS

STRAPS	PIN	DESCRIPTION		Value
ROM_TYPE[1:0]	MIOBD10 MIOB_VSYNC	Parallel=00, SERIAL AT25F=01 DEFAULT, Serial SST45VF=10, LPC=11		01
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)		0
PEX_PLL_TERM	MIOAD0			0
RAM_CFG[3:0]	MIOBD0 MIOBD1 MIOBD8 MIOBD9	For GDDR1	8Mx32 DDR monolithic (64bit) 300MHz, 1.8V	0001
			8Mx32 DDR monolithic (32bit) 300MHz, 1.8V	1001
			8Mx32 DDR (Samsung K4D55323QF-GC) 300MHz, 1.8V	0010
			4Mx32 DDR generic (64bit) 1.8V I/O	0100
			4Mx32 DDR generic (32bit) 1.8V I/O	1100
		For GDDR3	Infineon 16Mx32 500MHz, 1.8V	0001
			Hynix 16Mx32 500MHz, 1.8V	0010
			Samsung 16Mx32 500MHz, 1.8V	0011 *

Device ID strapping

	DEVID3	DEVID2	DEVID1	DEVID0
G72GLM	1	1	0	0
G72M	1	0	0	0
G72MV	0	1	1	1
G86MV	1	0	1	1



	S0
-1.75% (DOWN)	0
±0.875% (CENTER)	1

S0 Internal pull up

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Compal Electronics, Inc.

Title: NVG86 Spread Spectrum & Strapping

Size: | Document Number: LA-3302P | Rev: 0.4

Date: Thursday, March 01, 2007 | Sheet 57 of 66

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	38	HW	08/2/2006	Compal	BID change to X01	Pop R108, depop R106	X01
2	18	HW	08/10/2006	Compal	Change SOT23 package to SOT323 package	Change Q102, Q59 to SOT323 package	X01
3	7	HW	08/21/2006	Compal	BITS issue WI86517 (S5 state back driver issue)	Change R324 pin1 connect from +3.3V_ALW to +3.3V_SUS	X01
4	41	HW	08/21/2006	Compal	Bits issue WI84312 (Derating issue)	Change R151 from 30 ohm to 75 ohm	X01
5	23	HW	08/21/2006	Compal	Bits issue WI86509	Populate R761 and change value from 100k to 10k. Change R761 pin1 connect from +3.3V_ALW to +3.3V_SUS	X01
6	39	HW	08/21/2006	Compal	Bits issue WI86511	Add R401 (100K) for signal BC_DAT pull up to +3.3V_ALW	X01
7	37	HW	08/21/2006	Compal	Bits issue WI86512	Change R131 to no-stuff and from 4.7k to 100k per SMSC	X01
8	23	HW	08/21/2006	Compal	Bits issue WI86516	R509 PU for SIO_EXT_SMI# change from +3.3V_ALW to +3.3V_SUS to prevent backdrive through the ICH in S4/S5	X01
9	38,39	HW	08/21/2006	Compal	Bits issue WI86518	Swap PSID GPIO from ECE5018 pin 71 with MEC5025 ITP_DBRESET# pin 55	X01
10	38,39	HW	08/21/2006	Compal	Bits issue WI86532	Swap BEEP (ECE5018 GPIOB[6]) with PLTRST_DELAY# (MEC5025 SGPIO46)	X01
11	18	HW	08/21/2006	Compal	Bits issue WI86752	Change pull-up rail for R773 from +5V_SUS to +3.3V_SUS	X01
12	21	HW	08/30/2006	Compal	Bits issue WI86530	Move SB_NB_PCIE_RST# to GPIO4/PIRQG# pinF12 per M08 design	X01
13	21	HW	09/7/2006	Compal	Bits issue WI86529	Move SB_WLAN_PCIE_RST# to GPIO3/PIRQF# U32 pin G11 per M08 direction, add test point T1 on pin F18	X01
14	39	HW	09/7/2006	Compal	Bits issue WI86376. Due to increase in number of payloads the BIOS is carrying	Change U23 from (ST M25P80 8M bit) to (MXIC MX25L1605AM2C 16M bit)	X01
15	54	HW	09/7/2006	Compal	Bits issue WI87262. Add depopulated soft start capacitor	Add C85 (470PF_0402) across R244	X01
16	43	HW	09/11/2006	Compal	Bits issue WI90535	Change Q5 to MMBT3906WT1G, R15 to 150 ohm. Add R638 on LED_WLAN_OUT# pull up to +3.3V_WLAN. Add R639 (10K ohm) in series on LED_WLAN_OUT#	X01
17	7	HW	09/14/2006	Compal	Briscoe ESD/EMI Improvement Requests on PT	Remove ITP port and just keep ITP test point	X01
18	34	HW	09/14/2006	Compal	Bits issue WI90713	No stuff C16	X01
19	43	HW	09/14/2006	Compal	Bits issue WI90712	Remove R73, R178, C192, and C193	X01
20	43	HW	09/14/2006	Compal	Bits issue WI90705	Add SMBus isolation circuit for WLAN, R640,R645,R660,R662,Q45,Q46	X01
21	34	HW	09/14/2006	Compal	Bits issue WI90696	JMINI1 connect to +3.3V_RUN. Removed C427	X01
22	12	HW	09/14/2006	Compal	Shunt caps on LVDS for improving WWAN	Add C181,C192,C193,C196,C207,C209 cross LVDS signals	X01
23	27	HW	09/14/2006	Compal	Bits issue WI90516	Remove C759 from mic amp bias circuit	X01
24	26	HW	09/14/2006	Compal	Bits issue WI90487	Populate R541to cut BEEP level in half	X01

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25	18,52	HW	09/14/2006	Compal	Bits issue WI90207	Connect THERMTRIP_VGA# from U10 pinB13 to U10 pin A13. Populate R186 for THERMTRIP_VGA# pull up	X01
26	43	HW	09/14/2006	Compal	Bits issue WI89637	Populate EMI Clips Clip1, Clip2, Clip3, Clip4, Clip6	X01
27	23	HW	09/14/2006	Compal	Bits issue WI89409	No stuff R516, add R690 (8.2K ohm) for pull up ICH8 pin AF22 to +3.3V_SUS	X01
28	25	HW	09/14/2006	Compal	Bits issue WI89407	Add Q68, Q69, R691, R692 for HDDC_EN and MODC_EN circuits	X01
29	41	HW	09/14/2006	Compal	Bits issue WI89394	Change connect R765 pin1, R623 pin1, R621 pin1, R766 pin1, R637 pin1, R300 pin1 from +5V_ALW to +5V_ALW2	X01
30	37,39	HW	09/14/2006	Compal	Bits issue WI89379	Change R387,R389 from 1M to 2.7K. Add R778,R779 for AUX_ON,AC_OFF	X01
31	39	HW	09/15/2006	Compal	Bits issue WI92249	Change R730 from 100K to 4.7K ohm	X01
32	57	HW	09/15/2006	Compal	Bits issue WI92188. The MIO_A_D0 signal has an internal pull-down in the GPU	Remove R39	X01
33	53,55	HW	09/18/2006	Compal	Bits issue WI92289	U10 (NV86) pin F11,F12 connect to test point T89,T90 for testing and debug	X01
34	23	HW	09/18/2006	Compal	Bits issue WI92296	PLTRST_DELAY# move from ECE5018 GPOB[6] to ICH8 GPIO38	X01
35	34	HW	09/18/2006	Compal	Bits issue WI92287,WI90716	R660 and R662 connected to CLK_SCLK and CLK_SDATA.	X01
36	57,37, 22,33, 28,19, 20	HW	09/18/2006	Compal	EMI solutions	Populate SSCG U21,R189,R198,R199,L19,C297,C282,R166. depopR165. Populate RS232 C152,153,154,155,156, 157,158,159. Resume ICH_AZ_MDC_BITCLK C656,R123,C128. Add R790,R791,C232, C267. Change L63,L65 from 0603size to 0805size. Add C309,C316 for LOM. Add C427,C463 for LVDS. Add fuse F3, R792 for CRT. Populate C660, R545 (10 ohm),C721 (10P)	X01
37	23,36	HW	09/18/2006	Compal	Bits issue WI92298	Move SIO_EXT_SCI# from to ICH8 GPIO11/SMBALERT# pin AG22 to GPO12 pin AC19. Remove D22 and R761 and net DOCK_DET#	X01
38	23	HW	09/18/2006	Compal	Bits issue WI92299	ICH8 Pin AG22 tie to LOM_ICH_SMBALERT#. Add R793 (0 ohm) series on LOM_ICH_SMBALERT# and LOM_SMB_ALERT#. Change R730 pull up rail from +3.3V_ALW to +3.3V_LAN. Add R807 pull up to +3.3V_SUS for LOM_ICH_SMBALERT#	X01
39	39	HW	09/18/2006	Compal	Bits issue WI92301	Move ALW_PWRGD_3V_5V from MEC5025 pin 18 to MEC5025 pin 29. Remove 3.3V_5V_SUS_PWRGD from MEC5025 pin 29	X01
40	38,39	HW	09/18/2006	Compal	Bits issue WI92305	Swap DOCK_SMB_PME and DOCK_SMB_ALERT# from MEC5025 pin3 and ECE5028 pin76	X01
41	39,42	HW	09/18/2006	Compal	Bits issue WI92308	Removed 3.3V_LAN_PWRGD from MEC5025 KSO15/GPIO5. Remove U52,Q83,D29,R89,R98,R381,C784,C182,C183,C184	X01
42	39	HW	09/18/2006	Compal	Bits issue WI92312	Add R795 (10K ohm) pull down for MEC5025 pin 14	X01
43	29	HW	09/19/2006	Compal	EMI issue	Populate R671~R678 and C866~C869. Change L69~L76 from 24NH to 36NH inductor	X01
44	27	HW	09/19/2006	Compal	Bits issue WI90510	Add R796,R797 (0ohm) between L47/L48 and C728/C730	X01
45	57	HW	09/20/2006	Compal	EMI request	Add R798~R803 for strap damping	X01

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46	18	HW	09/20/2006	Compal	Bits issue WI92860	Depop Q39 and R427	X01
47	28	HW	09/20/2006	Compal	Bits issue WI92858	Change R669 to from 1.15K to 1.13K. Depop C771 & C772. Change C861 and C862 to 22pF	X01
48	38	HW	09/20/2006	Compal	Bits issue WI92857	Add no-stuff series 0-ohm for ITP_DBRESET# on ECE5028	X01
49	33	HW	09/21/2006	Compal	Bits issue WI93157	Remove R586 and make JMDC pin2 NC	X01
50	34	HW	09/21/2006	Compal	Bits issue WI93158	Depop Q45, Q46	X01
51	6	HW	09/25/2006	Compal	Bits issue WI93403	C484 change to 33pF, C861/C862 change to 22pF	X01
52	29	HW	09/26/2006	Compal	Bits issue DF86424	No Populate C866-C869/R671-R678	X01
53	40	HW	09/26/2006	Compal	EMI request	Add D37-D40 for stick point signals	X01
54	32	HW	09/27/2006	Compal	Bits issue DF94094	Add FUSE4,FUSE5	X01
55	9	HW	09/28/2006	Compal	Bits issue WI94923	C329,C330 chagne back to 10 0805 X6S	X01
56	18	HW	10/05/2006	Compal	Bits issue WI94892	Populate R771, C750, R772, Q102, R773	X01
57	30	HW	10/05/2006	Compal	Bits issue WI95910	Change R603 from 6.2k to 5.9k. Change C805 from 820pF to 270pF	X01
58	38,23 27,6	HW	10/05/2006	Compal	Bits issue WI95932	No stuff R227, R221, C89, C93, C97, c401, C92, r72, C90, C94. No stuff C775-C781, C785. No stuff R514 (no iAMT). Populate R515.	X01
59	36	HW	10/14/2006	Dell	Bits issue WI97539	Added signal DOCK_DET# to JDOCKBpin137, pin205 and Q3pin2	X02
60	9	HW	10/17/2006	Dell	Bits issue WI97837	Add 0.1 uf (0402) caps on +Vcc_Core to Gnd. Four total, bottom of board. (C870 ~ C873)	X02
61	23	HW	10/18/2006	Dell	Bits issue WI98222 (Change for ASF2.0 due to ICH8M errata)	1. No stuff R502, R503 2. Connect the pad of R503.2 to the pad of R498.2 3. Connect the pad of R502.1 to the pad of R499.2	X02
62	38	HW	10/24/2006	Dell	Board ID Changed to X02	Populated R106, R107. Depopulated R108, R109.	X02
62	38	HW	10/24/2006	Dell	Bits issue WI98660	The DevID for G86 on Briscoe needs to be updated to 1011	X02
63	23	HW	11/16/2006	Dell	Bits issue WI104573	Add R816,C874 for USB_IDE#. R817,C875 for SIO_EXT_WAKE#. R819,C876 for PCIE_MCARD1_DET#. R820,C878 for USB_MCARD1_DET#. R818,C877 for USB_MCARD2_DET#. Remove net RSVD_GPIO6 and R513	X02
64	6,23,34	HW	11/16/2006	Dell	Bits issue WI103311	Change R309 from 8.2K to 2.2K. No stuff R820. No stuff R550	X02
65	39	HW	11/18/2006	Dell	Bits issue WI103986	Change C379 from 22pF to 33pF per KDS X'tal report	X02
66	25,41	HW	11/20/2006	Compal	Bits issue WI105207	Change net name from +5V_ALW2 to +3.3V_ALW2 at R618.1, R626.1, R623.1, R621.1, R766.1, R765.1, R637.1, R300.	X03

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67	28	HW	11/21/2006	Dell	Bits issue WI105200	Change L64,L66,L67,L68 from BLM18AG601SN1D to BK1608LM182. Change R668 to L88 BK1608LM182.Change L63, L65 from BLM21AG601SN1D to BK2125LM182.	X02
68	6,54,57	HW	11/21/2006	Dell	Bits issue WI105712	Depop R697,change R286 to 0 ohm.Pop L53,depop L16.Pop L27,C314,C315.Depop L20,L21,pop L54,L55.Depop L17.	X02
69	38,39	HW	11/21/2006	Dell	Bits issue WI105754	Change R794 pin1 from +5V_ALW to +3.3V_ALW. Change R245 pin1 from +3.3V_ALW to +5V_ALW	X02
70	26	HW	11/21/2006	Dell	Bits issue WI105758. Updates for potential Back Drive	Add 100kohm resistor R721 between U35 pin 40 and +3.3V_RUN and 1000pF cap C759	X02
71	21,23,34	HW	12/1/2006	Dell	Bits issue WI106999	Please populate R820 with a 4.7k-ohm resistor. Move signal PCIE_MCARD2_DET# from ICH8m GPIO20 pinAE11 to PIRQH#/GPIO5 pinB3. Delete R457 and net ICH_GPIO5_PIRQH#. Populate R550	X02
72	41	HW	12/1/2006	Dell	Bits issue WI107466. +2.5V_LAN in-rush current test fai.	Populate C208	X02
73	6	HW	12/5/2006	Dell	Bits issue WI107881	Change R286 from 0 ohm to 33 ohms	X02
74	27	HW	12/6/2006	Dell	Bits issue WI107896	Change R554 from 10K to 0 ohm	X02
75	36,38	HW	12/6/2006	Dell	Bits issue WI108259. Per M08 GPIO map rev A15 Change list	Change net DOCK_SMB_PME to DOCK_SMB_PME#	X02
76	9	HW	12/6/2006	Dell	Bits issue WI108223	Change C177,C179,C178,C366,C338,C365 to EEFSX0D221E7 220uF	X02
77	52	HW	12/12/2006	Dell	Bits issue WI109622. Per NB8M PUN document	Change R35 from 60.4 ohm to 40.2 ohm	X02
78	55	HW	12/13/2006	Dell	Bits issue WI109627	Change R174 from 40.2 ohm to 30 ohm	X02
79	39	HW	12/14/2006	Dell	Bits issue WI110179	Add EC_FLASH_PAD pin1 connect to +3.3V_ALW,pin2 connect to R76 pin1 and R80 pin1	X02
80	27	HW	12/15/2006	Dell	Bits issue WI110158	Add R822 (1M_0402) from Pin 10 (C1P) pin of MAX9789A to ground	X02
81	26	HW	12/18/2006	Dell	Bits issue WI110749	Add R823 (10K_0402) to ground on pin 47 of STAC9205 (U37)	X02
82	29	HW	12/20/2006	Dell	Bits issue WI111288	Change R683 from 150ohms to 110 ohms, R684from 150ohms to 200ohms	X02
83	12,23 28	HW	12/25/2006	Dell	Change AC Coupling Cap SPEC for PCIE	Change C500~C531,C664,C666~C670,C851,C853 from 0.1uF Y5V to 0.1uF X7R	X02
84	54,55	HW	1/5/2007	Dell	Bits issue WI113179	Change R174 to 24.9 ohm for G86, Add R824 40.2 ohm for G72. Change R35 to 45.3 ohm G86, add R825 60.4 ohm for G72MV	X03
85	56	HW	1/5/2007	Dell	Bits issue WI113180	Add R826,R827 243 ohm for G86	X03
86	53,56	HW	1/5/2007	Dell	Bits issue WI113227	Add R828,R829,R830,R831,R832 487 ohm for G86	X03
87	38	HW	1/5/2007	Dell	Chagne Board ID to X03	Populate R108, de-pop R106	X03
88	6	HW	1/8/2007	Dell	Bits issue WI113588	Change U10 value to G86-620-A2. Add R833=147 ohm with R697 use 1@ for G72. R286=33 ohm use 2@ for G86. Change R48 note to "Reserved for GFx debug".	X03

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89	38	HW	1/26/2007	Dell	Bits issue WI115658. M08 GPIO map rev A16 change	Change ECE5028 GPIOF4 from BID2 to CHIPSET_ID.	X03
90	23	HW	2/12/2007	Dell	Bits issue WI121957	Add R834 (1M_0402_1%) for ICH_LAN_RST#	X03
91	27	HW	2/12/2007	Dell	Bits issue WI121438	Change R565 from 10K to 100k ohm	X03
92	41	HW	2/12/2007	Dell	Bits issue DF116813	Depop C194, changed C815 from 4700pF to 2200pF	X03
93	54	HW	2/14/2007	Dell	Modify pop option symbol for G72M/G86M power bead	L53,L27,L55,L54, with 2@, L16,L17,L21, L20, with 1@	X03
94	57	HW	2/14/2007	Dell	Modify NV strap table	Change GDDR3 table from 500 MHz to 700 MHz	X03
95	18	HW	2/26/2007	Dell	Bits issue WI124164	populate C640 = 10uF for G72MV. Add 1@ for C640	X03
96	54 57	HW	2/26/2007	Dell	Bits issue WI124408	Add note "Populate C251, C255 for G86 and G72 solution per Nvidia". Add 2@ for C314, C315, R805 and R57. Add 1@ for R49.	X03
97	54	HW	2/27/2007	Dell	Bits issue WI123608	Change C233 from X5R to X7R	X03
98	23	HW	2/27/2007	Dell	Bits issue WI125173. Per Intel's latest recommendation	Change R834 from 1M to 10K	X03
99	54	HW	2/28/2007	Dell	Bits issue WI123608	Change C233 back to X5R	X03
100	18 52	HW	2/28/2007	Dell	Bits issue WI124613. Need to connect THERMTRIP_VGA to the thermal sensor for G86	Add 2@ for R756, R187, Q76, C203	X03
101	18	HW	3/1/2007	Dell	Bits issue WI125873. Populate circuit for THERMTRIP_MCH#	Populate R427 and Q39	X03
102	27	HW	3/7/2007	Dell	Bits issue WI127300	Change U40 from 74AHC1G08 to 74AHCT1G08	X03

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1	48/50	PWR	9/14	Elick	change the AL CAP to 2000hr	change PC380 from SF10004M08L to SF000000S8L. change PC381 from SF10004M08L to SF000000S8L. change PC382 from SF10004M08L to SF000000S8L.	0.1
2	45	PWR	9/14	DELL	change to correct parts for 15ALW	change PD55 from SCSB717F08L to SCS00001U8L. change PD56 from SCSB717F08L to SCS00001U8L.	0.1
3	48	PWR	9/14	DELL	change to PSL of DELL	change PH2 from SL20000030L to SL200000F8L	0.1
4	44	PWR	9/14	DELL	change to PSL of DELL	change PL1 from SM01001680L to SM010008U0L.	0.1
5	44	PWR	9/14	DELL	change to PSL of DELL	change PL2 from SM01001418L to SM010009C8L. change PL34 from SM01001418L to SM010009C8L.	0.1
6	46	PWR	9/14	DELL	BITS-WI89364 The 0.9V_DDR_VTT_PWRGD net is not used at the MEC5025. The 0.9V_DDR_VTT_PWRGD net should be no connect at the MEC5025 pin 73.	remove PR437, PR438, PR441, PQ93 and PQ94.	0.1
7	45	PWR	9/14	DELL	BITS-WI91011 change to correct current limits	Change PR383 from 124K(SD03412438L) to 150K(SD03415038L). Change PR382 from 187K(SD03418738L) to 226K(SD03422638L).	0.1
8	47	PWR	9/14	DELL	BITS-WI91278 following DELL rule	Depopulate PR415 and PR416 resistors.	0.1
9	49	PWR	9/14	DELL	BITS-WI91289 be compliant with the reference schematic.	Change PR274 from 4.7 ohm(SD000006T8L) to 33 ohm(SD014330A8L). Populate PR373 and PD54.	0.1
10	51	PWR	9/14	DELL	BITS-WI91295 Implement changes to 1.25V_RUN and GPU Core regulators	Add PC410 10uF, 1206, 25V at the input rail (+PWR_SRC) of the 1.25V_RUN regulator. Change PR460 from 0 ohm(SD01300008L) to 1 ohm(SD013100B8L). Change PR459 from 0 ohm (SD01300008L) to 1 ohm(SD013100B8L). Change PR449 ground connection from AGND to PGND.	0.1
11	47	PWR	9/14	DELL	BITS-WI91372 following DELL rule	Change PR408 from 75K(SD03475028L) to 82.5K(SD00000278L).	0.1
12	44	PWR	9/14	DELL	BITS-WI91682 DC IN schematic changes.	Change PL1 from SM01001680L to SM010008U0L. Change PQ100 from SI2301BDS(SB923010020) to PQ100A depopulated IMD2A(SB000009N8L). Change PQ101 from SI2301BDS(SB923010020) to PQ100B depopulated IMD2A(SB000009N8L). Change PR12 from 10K,0603(SD01310028L) to 4.7K,0805(SD00247018L).	0.1
13	45	PWR	9/14	DELL	BITS-WI90985 following DELL rule	Change PC285 pin 2 pad connection from PGND to AGND.	0.1
14	45	PWR	9/14	DELL	BITS-WI90988 Change PQ83 from FDS8880 to BSC079N03SG PPAK	Change PQ83 from SB000004U8L to SB000004D8L.	0.1
15	51	PWR	9/15	DELL	BITS-WI92173 correct the current limit on GPU CORE regulator	Change PR451 from 140K(SD03414038L) to 182K(SD03418238L)	0.1

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16	51	PWR	9/15	DELL	BITS-WI92161 correct the current limit on 1.25V_RUN regulator.	Change PR453 from 140K(SD03414038L) to 205K (SD03420538L)	0.1
17	46	PWR	9/15	DELL	BITS-WI91932 correct the current limit on 1.8V output	Change PR202 from 61.9K(SD03461928L) to 100K (SD03410038L)	0.1
18	46	PWR	9/18	DELL	BITS-WI92459 follow BITS of DELL	change PR193 to be populate. change PR506 to be populate. change PR505 to be depopulate.	0.1
19	48	PWR	9/18	DELL	BITS-WI92462 improve transients at load dump. and reduce jittering.	Add depopulate PR516(SD03410018L) and depopulate PC413(SE076103K8L) between pin 9 of PU11 and AGND. Add depopulated PC411(SE075472K8L),4700pF between pin 14 of PU11 and AGND . Add depopulated PC412(SE075472K8L),4700pF between pin 15 of PU11 and AGND	0.1
20	51	PWR	9/18	DELL	BITS-WI87245 PWRGD signals are reversed coming from the wrong side of the IC.	Change the node name at pin 13 of PU25 from GFX_CORE_PWRGD to 1.25V_RUN_PWRGD. Change the node name at pin 28 of PU25 from 1.25V_RUN_PWRGD to GFX_CORE_PWRGD . Remove +3.3V_RUN node connected to pin 2 of PR462. Remove +3.3V_ALW node connected to pin 1 of PR483. Remove +3.3V_ALW node connected to pin 1 of PR450. Remove totally PR462 pad, PR483, PR450.	0.1
21	51	PWR	9/20	Elick	change GPU_CORE voltage	change PR446 from 10k to 13.7k(SD03413728L)	0.1
22	44	PWR	9/21	DELL	BITS-WI91682 change PL1 from BK1608HM to BLM18BD102SN1D.	change PL1 from SM010008U0L to SM010007C8L.	0.1
23	48/50	PWR	9/21	DELL	BITS-WI87563 change populate PC380 from 25CE100AX to 25CE100LS change PC381 from 25CE100AX to 25CE100LS change PC382 from 25CE100AX to 25CE100LS	change populate PC380 from SF000000S8L to SF000000T8L. change PC381 from SF000000S8L to SF000000T8L. change PC382 from SF000000S8L to SF000000T8L.	0.1
24	49	PWR	9/29	DELL	match Maxim's response time of ICM input to comparator.	change PR361 from 0 Ohm (SD02800008L) to 8.45K (SD00000068L). change PC254 from 0.01uF 25V (SE068103K8L) to 0.1uF 16V (SE076104K8L).	0.1
25	49	PWR	9/29	DELL	ICM is voltage source and does not need this component.	depopulate PR150.	0.1
26	49	PWR	9/29	DELL	Increase BW from 20kHz to 25kHz while maintaining 80degrees phase margin.	change PR148 from 4.7K (SD03447018L) to 10K (SD03410028L).	0.1
27	49	PWR	9/29	DELL	following DELL rule	depopulate PD54 and PR373	0.1
28	48	PWR	10/27	DELL	Add bead to connect +PWR_SRC to +CPU_PWR_SRC	Add PL47(SM01002078L) to parallel PJP30.	0.2

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29	45,46, 47,51	PWR	10/27	DELL	BITS-WI99895 This is to add an optional ultrasonic mode in case the regulators experience an audible noise.	Add PR517 0 ohm 0402(SD02800008L) between pin 29 of PU20 and AGND . Add PR519 0 ohm 0402(SD02800008L) between pin 29 of PU21 and AGND . Add PR520 0 ohm 0402(SD02800008L) between pin 29 of PU25 and AGND . Add PR518 0 ohm 0402(SD02800008L) between pin 26 of PU6 and AGND .	0.2
30	49	PWR	10/27	DELL	BITS: WI102600 Change PR148 from 10K_0402_1% to 2.2K_0402_5%	change PR148 from 10k 0402 1%(SD03410028L) to 2.2k 0402 5%(SD02822018L)	0.3
31	45	PWR	11/20	DELL	BITS-WI105406 Add node name +3.3V_ALW2 for the trace connected to the pin 5 (VREF3) of PU20. Populate PC285 with 0.1uF cap.	Add node name +3.3V_ALW2 between pin5 of PU20 and PC285. Populate PC285.	0.3
32	49	PWR	12/06	DELL	BITS-WI106278 make sure that PC113, PC114 and PC379 are X5R/X7R caps, need to stuff PC379.	change PC379 is populated.	0.3
33	48	PWR	12/06	DELL	BITS-WI108229 Change PC187 from 10nF to 15nF. Change PR258 from 2.21K to 1.69K. Populate PR516 with 1K resistor. Populate C413 with 0.01uF.	change PR187 from 10nF(SE076103K8L) to 15nF(SE076153K8L). change PR258 from 2.21K(SD03422118L) to 1.69K(SD00000JB8L). populate PC413. populate PR516.	0.3
34	51	PWR	01/04	ELICK	EMI CLK issue	Add PL3 to parallel PJP54. add PC414 to connect between GPU_CORE to GND. add PC415 to connect between GPU_CORE to GND.	0.3
35	49	PWR	01/25	ELICK	change to new part number for PSL	change PR138 from SD021100D8L to SD021100D3L(S RES 1W .01 +-1% 2512 FOR M08 PROJECTS) change PR145 from SD021100D8L to SD021100D3L(S RES 1W .01 +-1% 2512 FOR M08 PROJECTS)	0.4
36	44	PWR	01/26	ELICK	change bead to 9A 1812 in DC-IN.	change PL2 from SM010009C8L(TAIYO FBMJ4516HS720NT 1806) to SM01000BI0L(KC FBCA-K5B-302340-L1-T 1812). change PL32 from SM010009C8L(TAIYO FBMJ4516HS720NT 1806) to SM01000BI0L(KC FBCA-K5B-302340-L1-T 1812).	0.4
37	45/47/51	PWR	02/05	DELL	BITS-WI119950 Increase current limits for 3.3V, 1.5V and GPU_CORE regulators.	change PR382 from 226K to 267k (SD02822018L). Change PR408 from 82.5K to 100K(SD03410038L). Change PR451 from 182K to 205K(SD03420538L) .	0.4
38	49	PWR	02/06	DELL	additional 1206 resistor on +VCHGR for Maxim solution.	add an unpopulation PR522 (1.8K 1206 1%(SD00000JN8L))between +VCHGR to PGND.	0.4
39	49	PWR	02/12	DELL	delete 1206 resistor on +VCHGR not to implement for Maxim solution.	delete an unpopulate PR520 (1.8K 1206 1%(SD00000JN8L))between +VCHGR to PGND.	0.4

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40	51	PWR	02/26	DELL	BITS-WI123151 GPU Core Voltage for G86MV is staying at 1.15V all the time	Nostuff: PR447, PR457, PC370, PR452, PQ98, PR461, PC371, PR458, PQ99, PR454, PR455. Change 2@PR449 from 20.5K to 18.7K 0402 1%(SD03418728L) Add 2@PR522 = 196K, 0402. <-- This would be a 2@ resistor added in parallel to the existing PR451	0.4