

COMPAL CONFIDENTIAL

MODEL NAME : *HAL00*
PCB NO : *LA-2791*
COMPAL P/N : *45135631L01*

Travis (UMA) Schematics Document
uFCPGA Mobile Yonah
Intel Calistoga + ICH7M

2006 - 01 - 20

REV : 1.0 (DELL: A00)

MB PCB

Part Number	Description
DAA0000040L	PCB ZJX LA-2791 REV0 N/B UMA

BOM NO. *45135631L01*
PCB P/N: *DA800002L1L*

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Title

Cover Sheet

Size

Document Number

LA-2791

Date: Tuesday, February 07, 2006

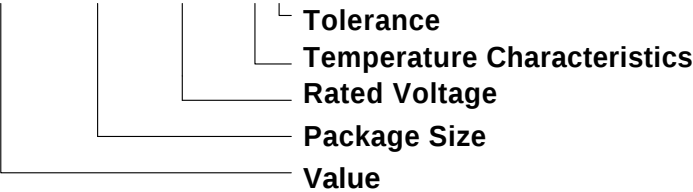
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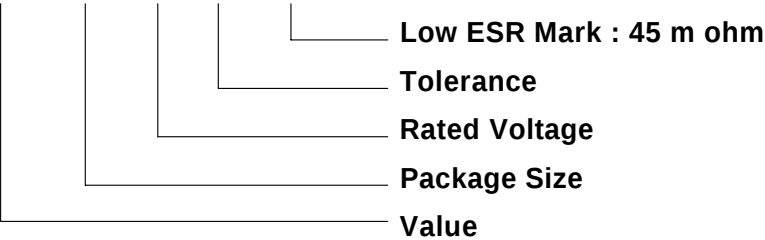
Ceramic Capacitors :

0.1U_0402_6.3VXX



Tantalum or Polymer Capacitors :

10U_D2_10VX_R45



Capacitor Spec Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NPO	C0G	X6S	BJ	CH	CJ	CK	SH	SJ

H	I	J	K
UJ	UK	SL	X5S

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+0.05PF	+0.1PF	+0.25PF	+0.5PF	+1PF	+2%	+3%	+5%

K	M	N	P	Q	V	X	Z	
+10%	+20%	+30%	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	

NOTE1:

@XX : Depop component

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PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	1	C

PM TABLE

power plane State	+5V_ALW +3.3V_ALW	+3.3V_SRC +15V_SUS +5V_SUS +3.3V_SUS +1.8V_SUS	+5V_RUN +3.3V_RUN +3.3V_RUN_R +1.8V_RUN +0.9V_DDR_VTT +1.5V_RUN +VCC_CORE +1.05V_VCCP +2.5V_RUN
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

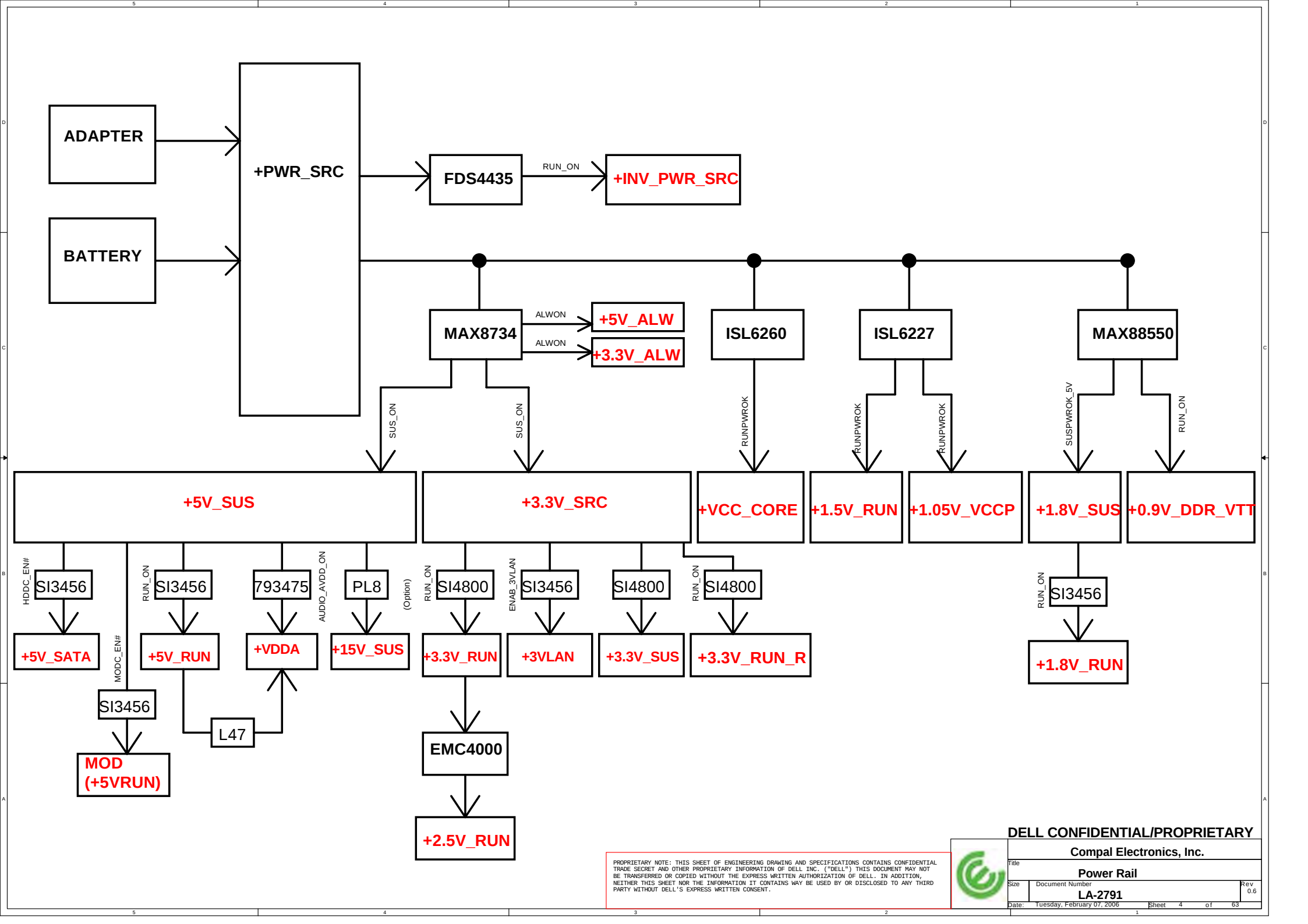
USB TABLE

USB PORT#	DESTINATION
0	Mini 2(WLAN)
1	USB Hub (5018)
2	D Moudle
3,4	SIDE
5,6	REAR
7	Docking

USB HUB	DESTINATION
1	PC Card Bay
2	Mini 1(WWAN)
3	Smart Card --> BIO
4	Blue tooth

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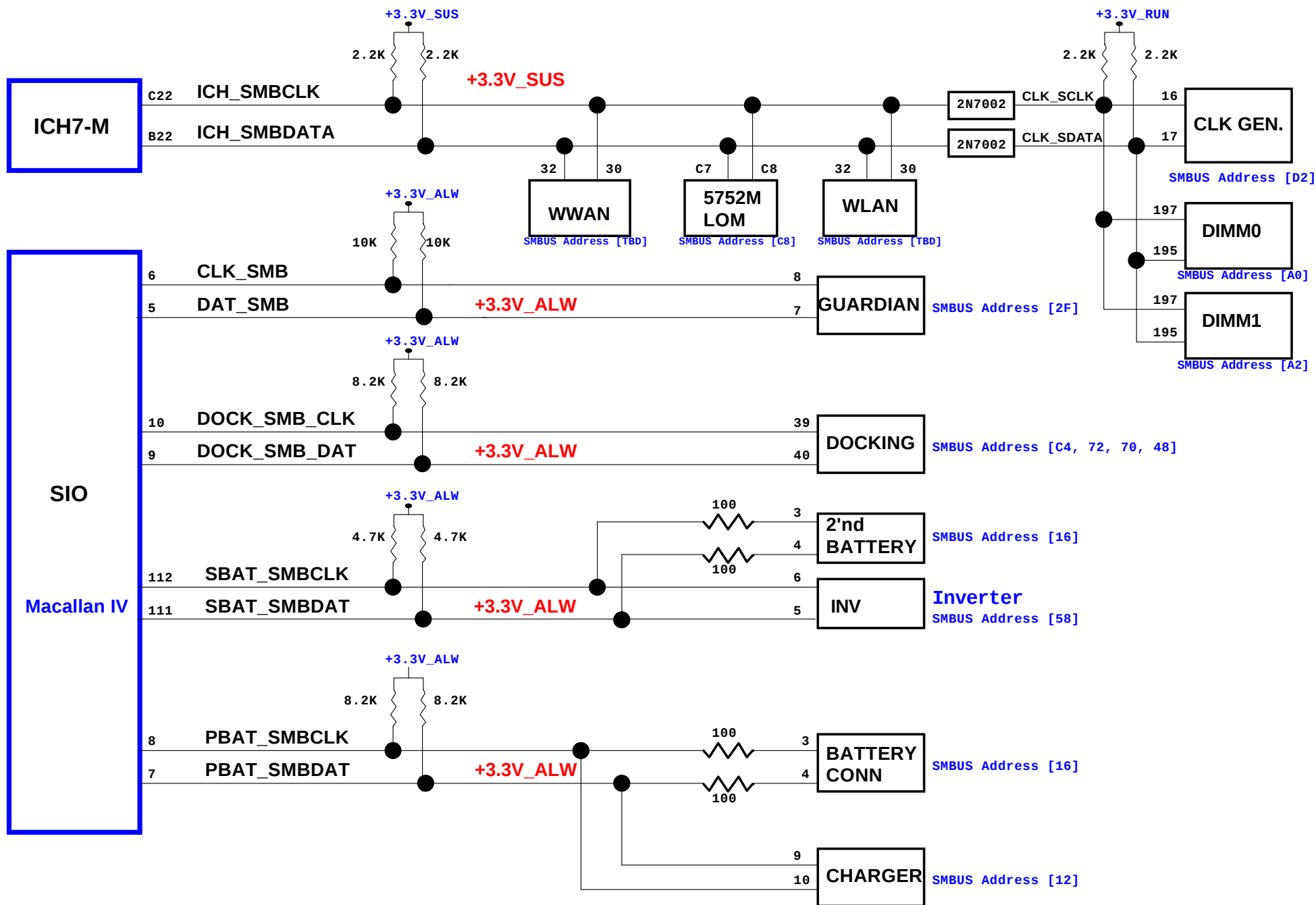
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Title			Power Rail	
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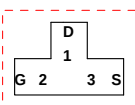


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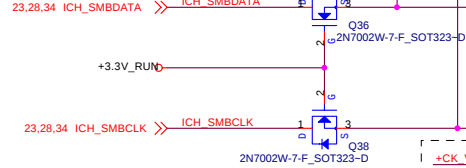
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SMBUS TOPOLOGY

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2N7002



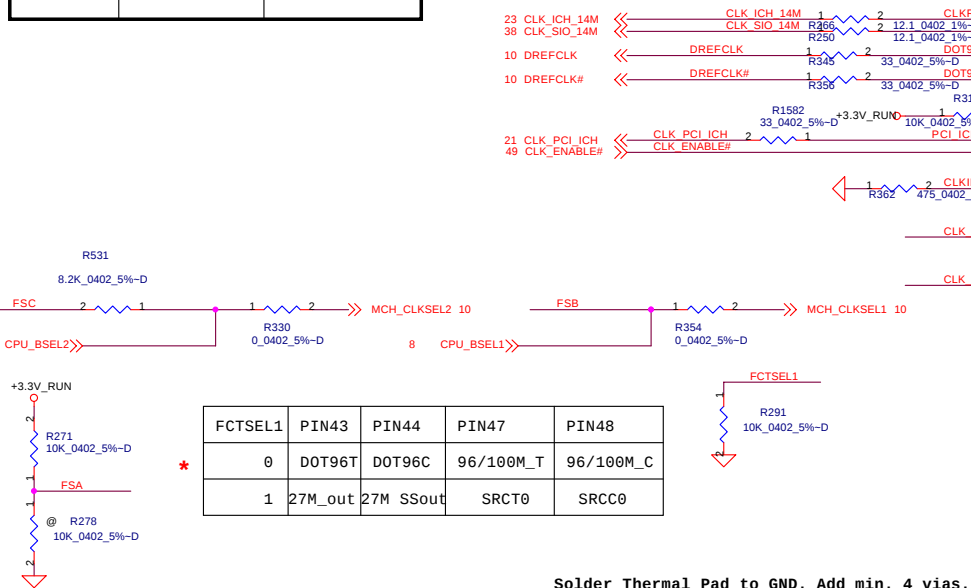
FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1	Reserve		

Table : ICS954305AK

CPU_BSEL	CPU_BSEL2(FSC)	CPU_BSEL1(FSB)
133	0	0
166	0	1

NOTE: Place Decoupling as close as physically possible to the VDD pins

Place crystal within 500 mils of CK410



FCTSEL1	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27M_out	27M SSout	SRCT0	SRCC0

Solder Thermal Pad to GND. Add min. 4 vias.

Place near each pin
W>40 mil

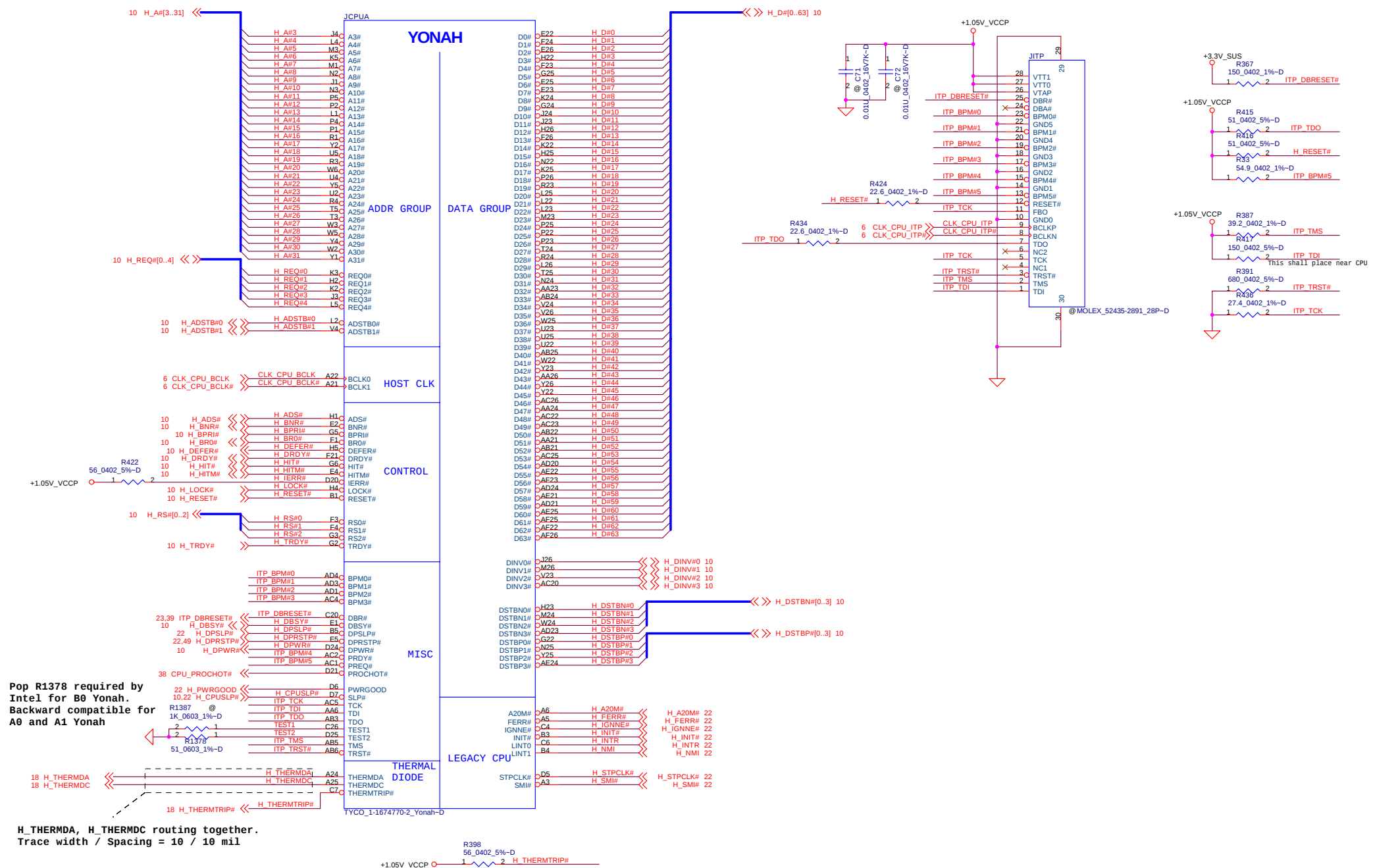
Place near CK410+

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Clock Generator			
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Pop R1378 required by Intel for B0 Yonah. Backward compatible for A0 and A1 Yonah

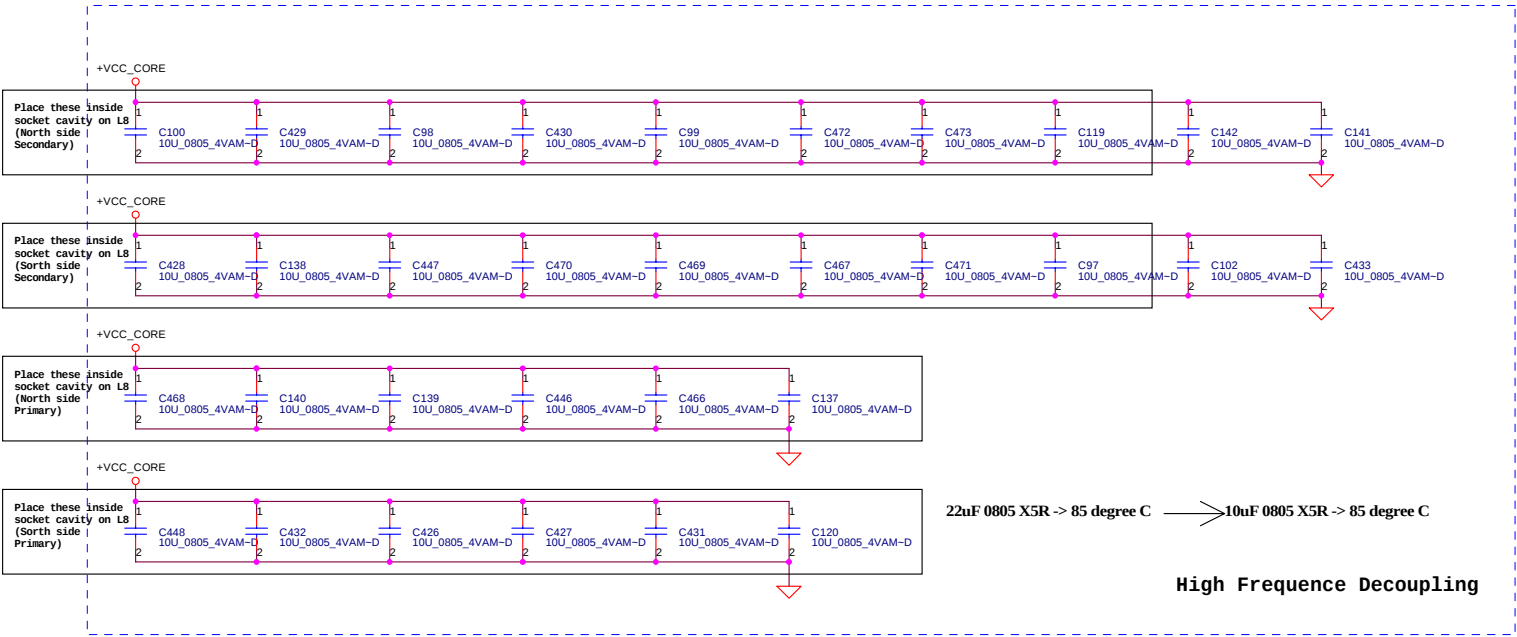
H_THERMDA, H_THERMDC routing together. Trace width / Spacing = 10 / 10 mil

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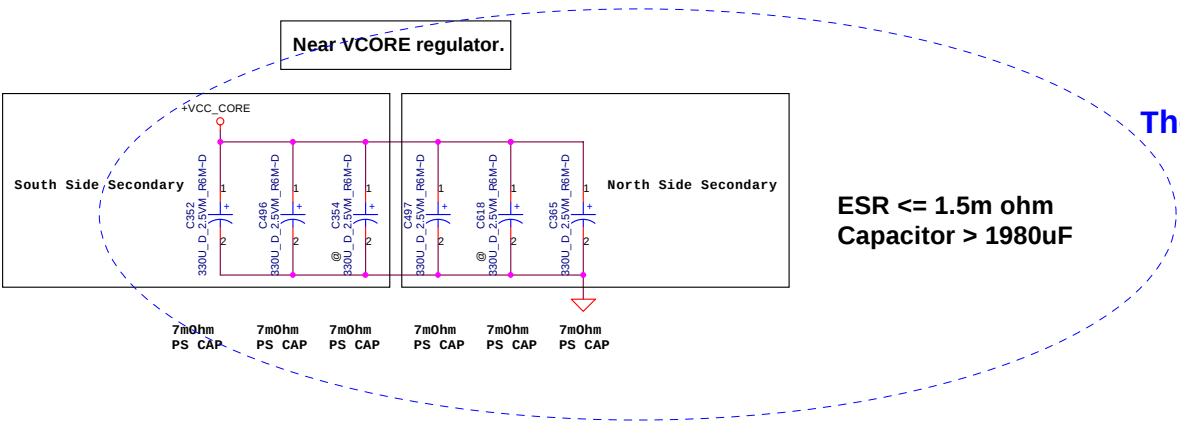


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Yonah in mFCPGA479		
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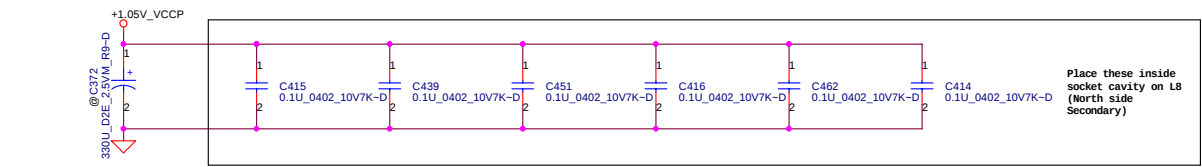


22uF 0805 X5R -> 85 degree C → 10uF 0805 X5R -> 85 degree C
High Frequency Decoupling



The caps need change to ESR=6m ohms

ESR <= 1.5m ohm
Capacitor > 1980uF



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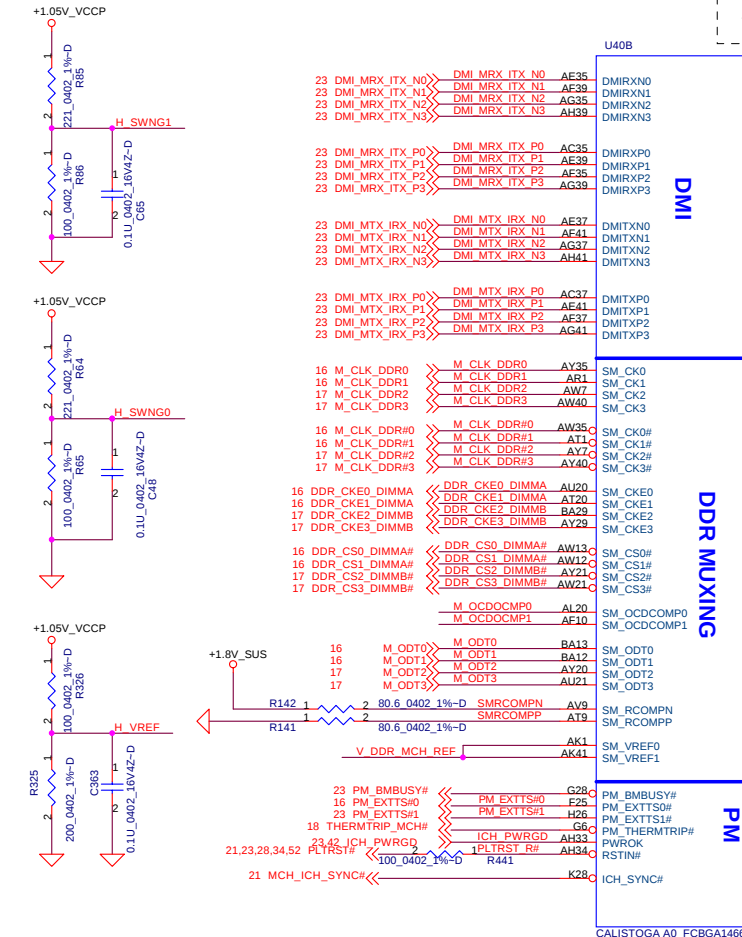
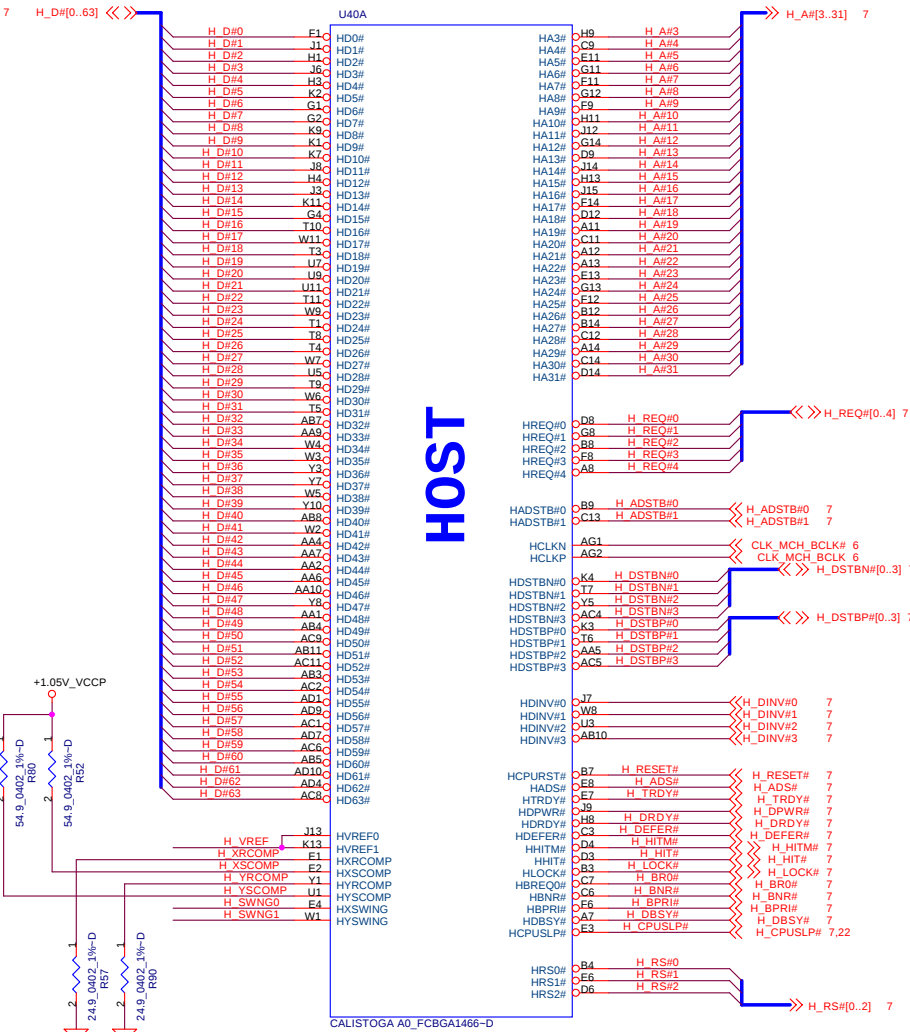
CPU Bypass

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Description at page12

Note :
CF63:17 has
internal pullup,
CF618:19 has
internal pulldown



Layout Note:
H_XRCOMP & H_YRCOMP trace width
and spacing is 10/20

Stuff R435 & R437 for A1 Calistoga

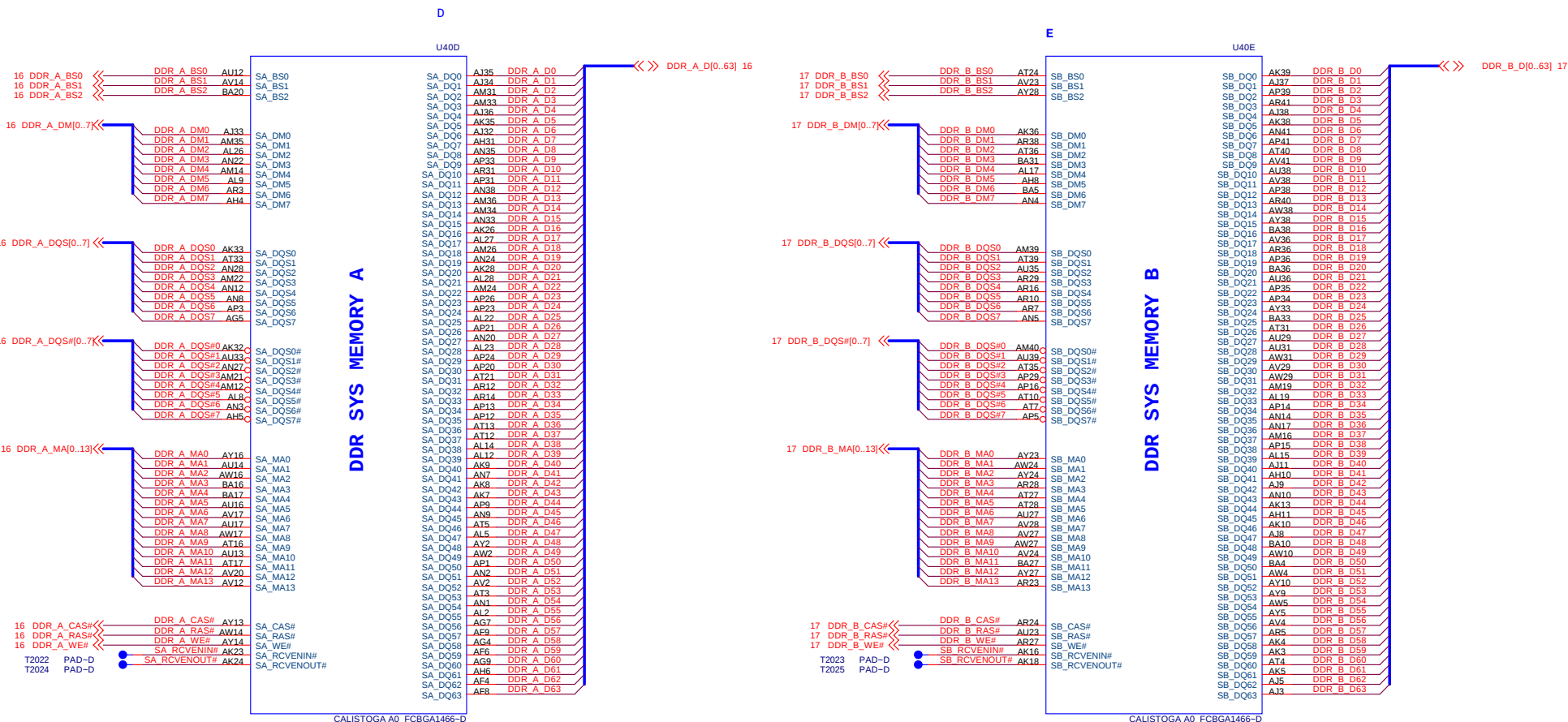
Layout Note:
Route as short
as possible

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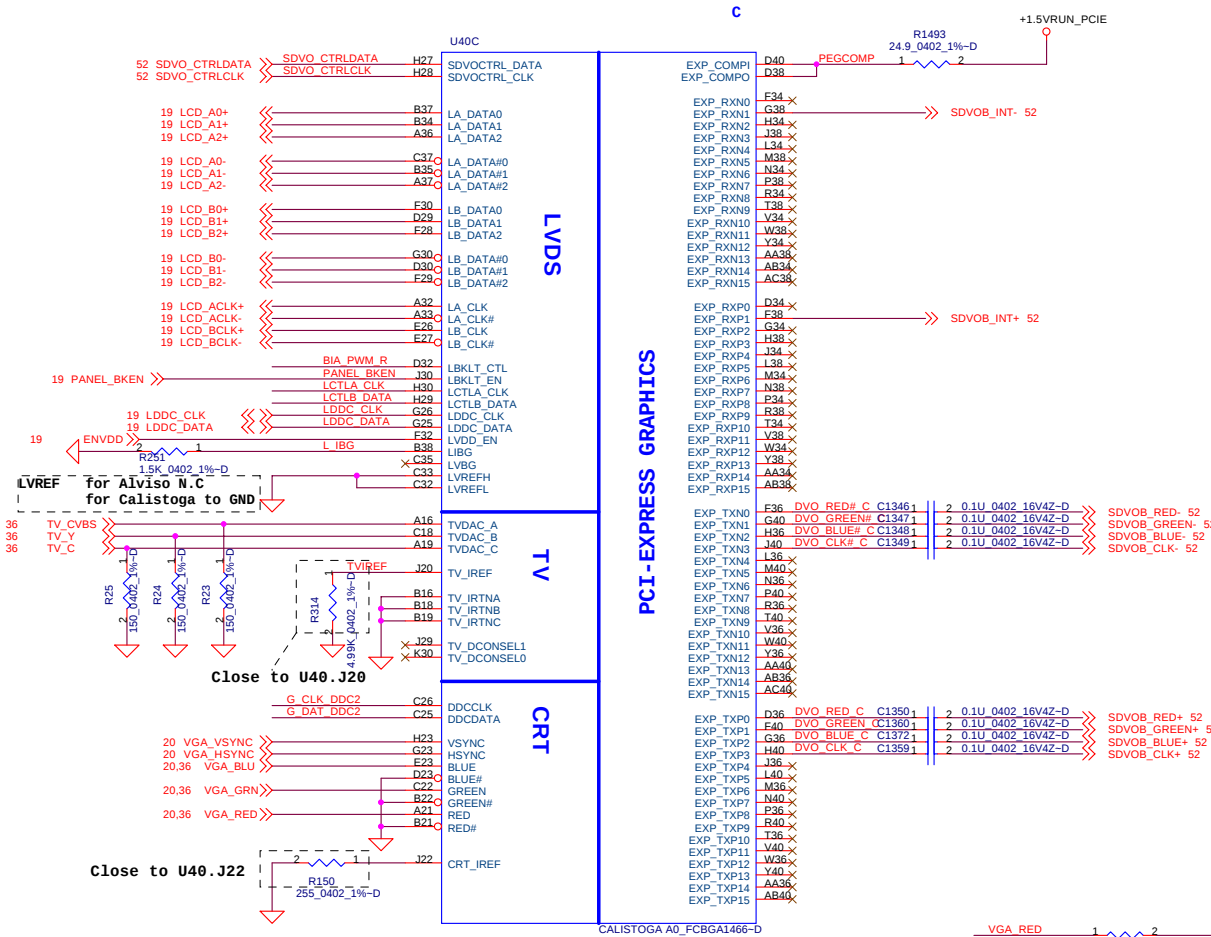
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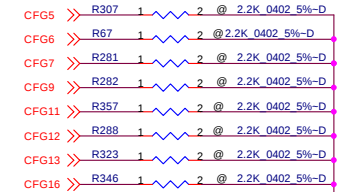
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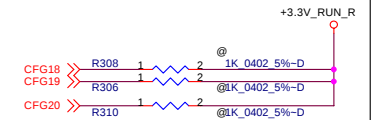


Strap Pin Table

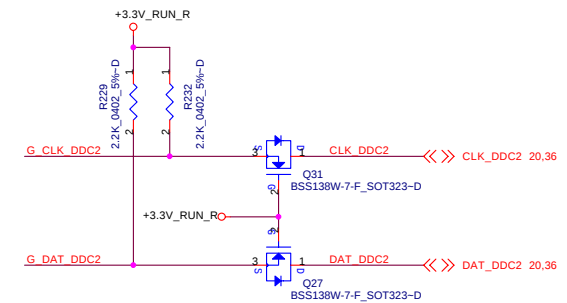
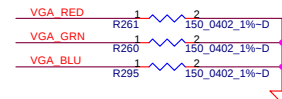
CFG5	Low = DMI x 2 High = Moby Dick *	10
CFG6	Low = Moby Dick High = Calistoga *	10
CFG7	Low = DT/Transportable CPU High = Mobile CPU *	10
CFG9	Low = Reverse Lane High = Normal Operation *	10
CFG11		10
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All 2 Mode Enabled 11 = Normal Operation *	10
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *	10
CFG18 (VCC Select)	Low = 1.05V (Default) *	10
CFG19 (DMI Lane Reversal)	Low = Normal * Operation (Default): Lane number in Order High = Reverse Lane	10
SDVO_CTRLDATA	Low = No SDVO Device Present (Default) * High = SDVO Device Present	10
CFG20 (PCIE/SDVO select)	Low = Only PCIE or SDVO is operational. (Default) * High = PCIE/SDVO are operating simu.	10



CFG[3:17] have internal pullup



CFG[18:20] have internal pulldown



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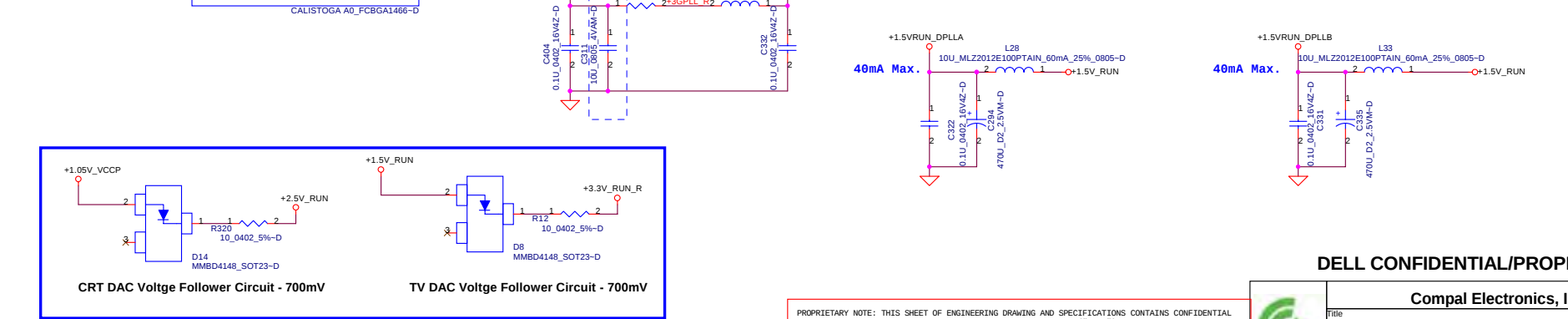
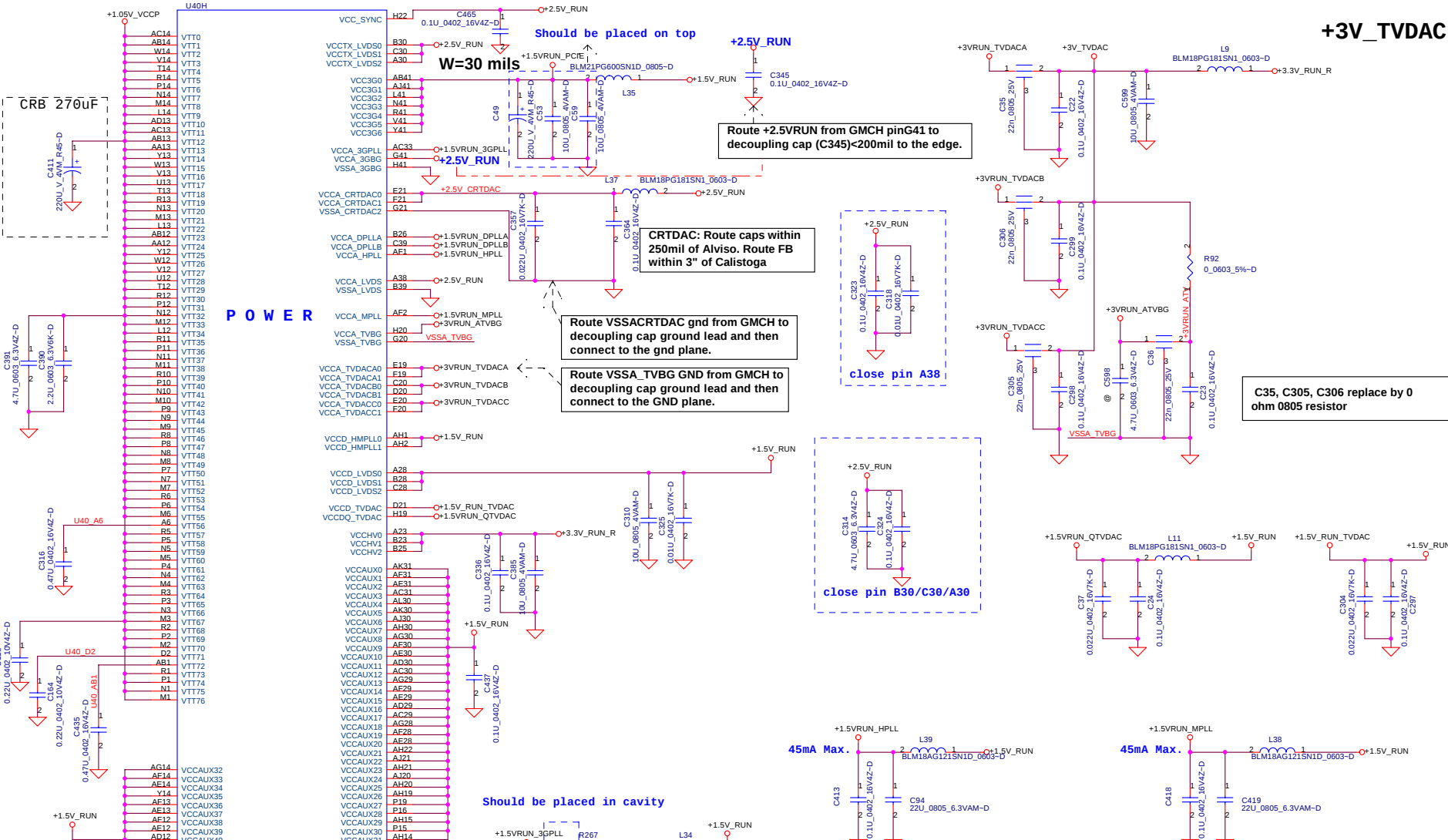
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+3V_TVDAC

POWER

Route +2.5VRUN from GMCH pinG41 to decoupling cap (C345)<200mil to the edge.

CRTDAC: Route caps within 250mil of Alvisto. Route FB within 3" of Calistoga

Route VSSACRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

Route VSSA_TVDBG GND from GMCH to decoupling cap ground lead and then connect to the GND plane.

C35, C305, C306 replace by 0 ohm 0805 resistor

close pin B30/C30/A30

close pin B30/C30/A30

Should be placed in cavity

45mA Max.

45mA Max.

40mA Max.

40mA Max.

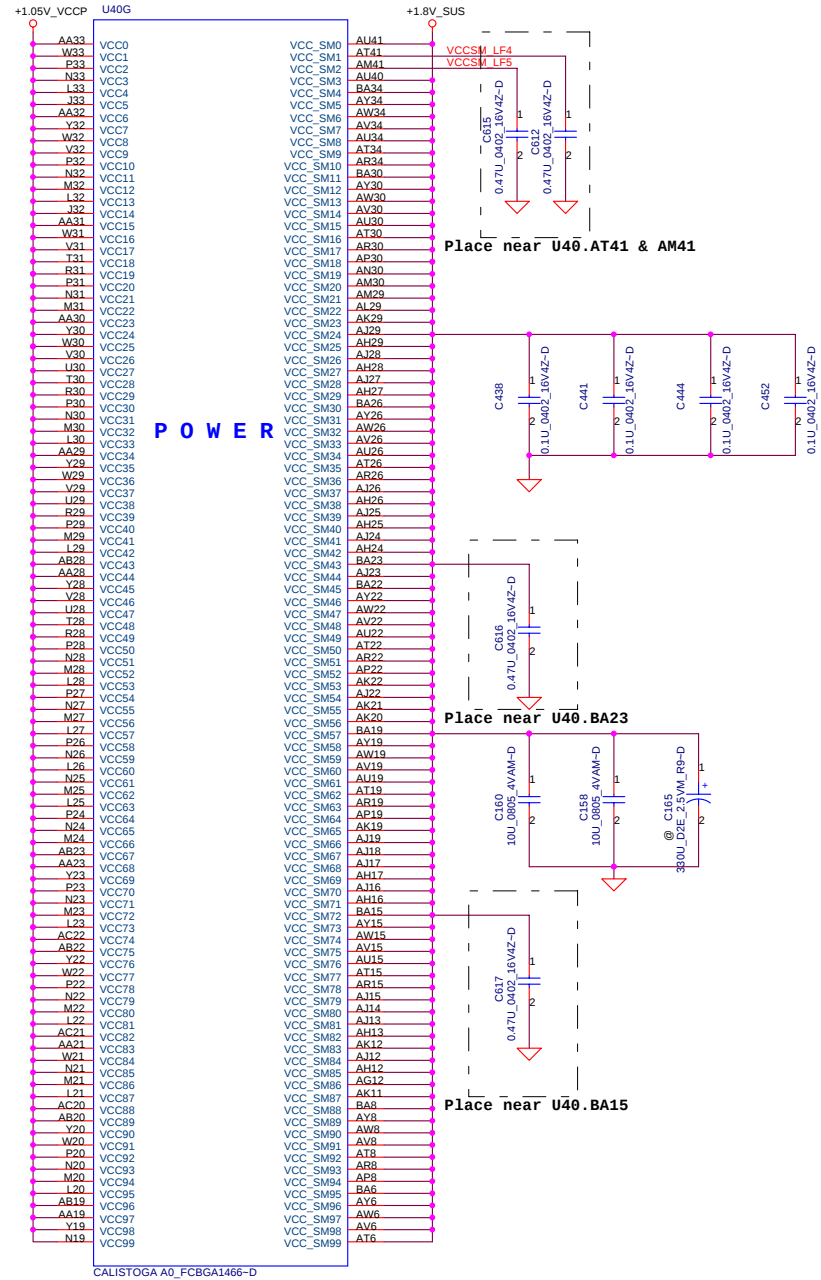
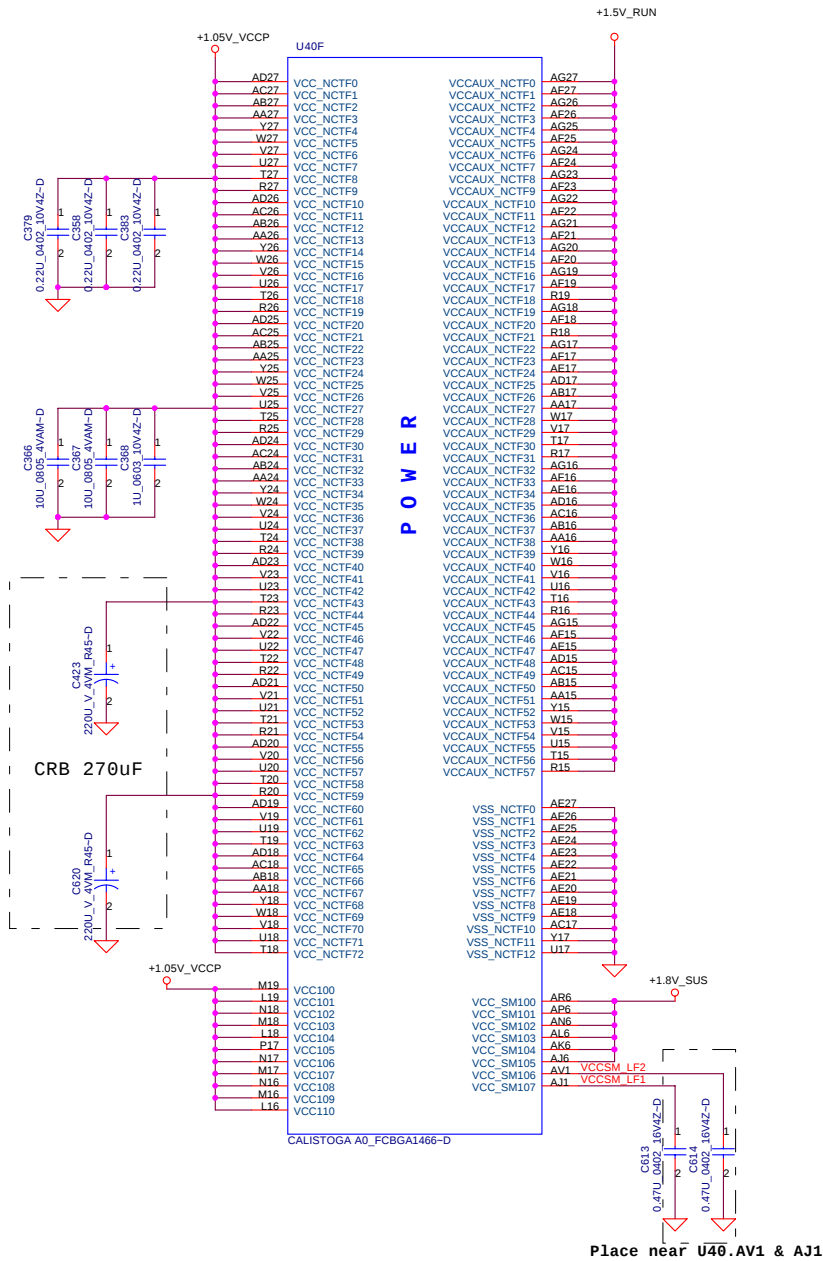
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U401		
AC41	VSS0	AE34
AA41	VSS1	AC34
WA1	VSS2	C34
T41	VSS3	AW23
P41	VSS4	AV33
M41	VSS5	AR33
F41	VSS6	AE33
AV40	VSS7	AB33
AP40	VSS8	Y33
AN40	VSS9	V33
AK40	VSS10	R33
AJ40	VSS11	M33
AH40	VSS12	H33
AG40	VSS13	G33
AE40	VSS14	F33
AE40	VSS15	E33
B40	VSS16	B33
AY39	VSS17	AH32
AW39	VSS18	AG32
AV39	VSS19	AF32
AR39	VSS20	AE32
AN39	VSS21	AC32
AJ39	VSS22	AB32
AC39	VSS23	G32
AB39	VSS24	B32
AA39	VSS25	AY31
Y39	VSS26	AV31
W39	VSS27	AN31
V39	VSS28	AJ31
T39	VSS29	AG31
R39	VSS30	AB31
P39	VSS31	Y31
N39	VSS32	AB30
M39	VSS33	E30
L39	VSS34	AT29
J39	VSS35	AN29
H39	VSS36	AB29
G39	VSS37	T29
F39	VSS38	N29
D39	VSS39	K29
AT38	VSS40	Q29
AM38	VSS41	E29
AH38	VSS42	C29
AG38	VSS43	B29
AE38	VSS44	A29
AE38	VSS45	BA28
C38	VSS46	AW28
AK37	VSS47	AU28
AH37	VSS48	AP28
AB37	VSS49	AM28
AA37	VSS50	AD28
Y37	VSS51	AC28
W37	VSS52	W28
V37	VSS53	J28
T37	VSS54	E28
R37	VSS55	AP27
P37	VSS56	AM27
N37	VSS57	J27
M37	VSS58	G27
L37	VSS59	F27
J37	VSS60	B27
H37	VSS61	C27
G37	VSS62	AN26
F37	VSS63	M26
D37	VSS64	K26
AY36	VSS65	F26
AW36	VSS66	D26
AV36	VSS67	AK25
AN36	VSS68	P25
AH36	VSS69	K25
AG36	VSS70	H25
AE36	VSS71	E25
AE36	VSS72	D25
AC36	VSS73	A25
C36	VSS74	BA24
B36	VSS75	AU24
BA35	VSS76	AW23
AV35	VSS77	AT23
AR35	VSS78	AN23
AH35	VSS79	AM23
AB35	VSS80	AH23
AA35	VSS81	AC23
Y35	VSS82	W23
W35	VSS83	K23
V35	VSS84	J23
T35	VSS85	E23
R35	VSS86	F23
P35	VSS87	G23
N35	VSS88	AA22
M35	VSS89	K22
L35	VSS90	G22
J35	VSS91	F22
H35	VSS92	E22
G35	VSS93	D22
F35	VSS94	A22
D35	VSS95	BA21
AN34	VSS96	AV21
AK34	VSS97	AR21
AG34	VSS98	
AF34	VSS99	

CALISTOGA A0_FCBGA1466-D

U403		
AN21	VSS200	AG10
AL21	VSS201	AC10
AB21	VSS202	W10
Y21	VSS203	VSS282
P21	VSS204	VSS283
K21	VSS205	VSS284
H21	VSS206	VSS285
C21	VSS207	AW9
AW20	VSS208	AG9
AR20	VSS209	AH9
AM20	VSS210	AB9
AA20	VSS211	Y9
K20	VSS212	R9
B20	VSS213	G9
A20	VSS214	E9
AN19	VSS215	AG
AC19	VSS216	AG8
W19	VSS217	A8
K19	VSS218	AA8
G19	VSS219	VSS296
C19	VSS220	VSS297
AH18	VSS221	VSS298
P18	VSS222	VSS299
H18	VSS223	VSS300
D18	VSS224	VSS301
A18	VSS225	AV7
AY17	VSS226	AP7
AR17	VSS227	AL7
AP17	VSS228	VSS303
AM17	VSS229	VSS304
AK17	VSS230	VSS305
AV16	VSS231	VSS306
AN16	VSS232	VSS307
AL16	VSS233	AC7
J16	VSS234	G7
F16	VSS235	D7
C16	VSS236	AG6
AN15	VSS237	AD6
AM15	VSS238	VSS312
AK15	VSS239	VSS313
N15	VSS240	VSS314
M15	VSS241	Y6
L15	VSS242	U6
B15	VSS243	N6
A15	VSS244	K6
BA14	VSS245	VSS317
AT14	VSS246	VSS318
AK14	VSS247	VSS319
AD14	VSS248	VSS320
AA14	VSS249	VSS321
U14	VSS250	VSS322
K14	VSS251	VSS323
E14	VSS252	VSS324
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		VSS355
		VSS356
		VSS357
		VSS358
		VSS359
		VSS360

CALISTOGA A0_FCBGA1466-D

POWER

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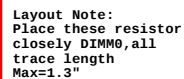
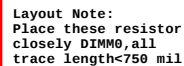
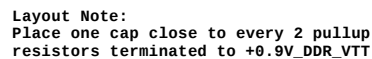
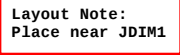
Compal Electronics, Inc.

Calistoga(6 of 6)

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[illegible]

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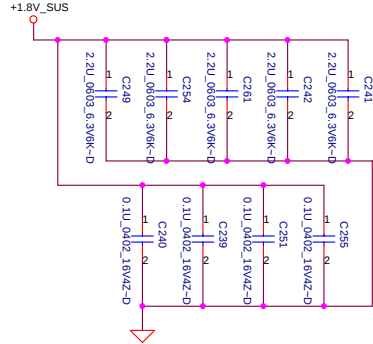


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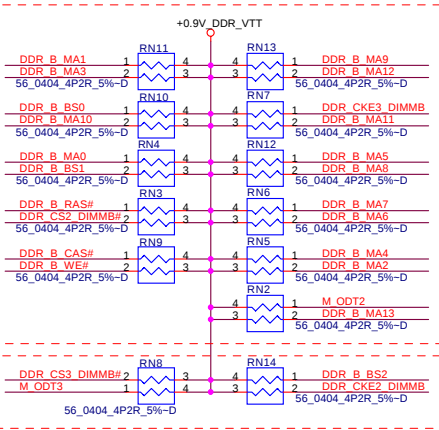
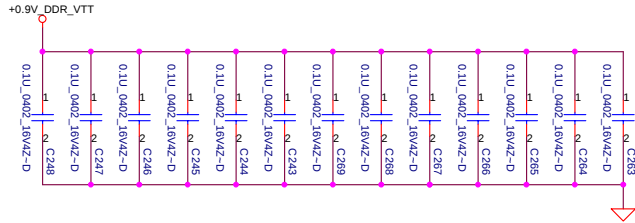
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11 DDR_B_DQS#[0..7] <<>>
 11 DDR_B_DQ[0..63] <<>>
 11 DDR_B_DM[0..7] <<>>
 11 DDR_B_DQS[0..7]<<>>
 11 DDR_B_MA[0..13] <<>>

Layout Note:
Place near JDIM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor closely DIMM0, all trace length<750 mil

Layout Note:
Place these resistor closely DIMM0, all trace length Max=1.3"

ON BOTTOM SIDE



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DDRRII-SODIMM SLOT2		
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FAN1 and Tachometer

R479 place on bottom side next to SoDIMM connector

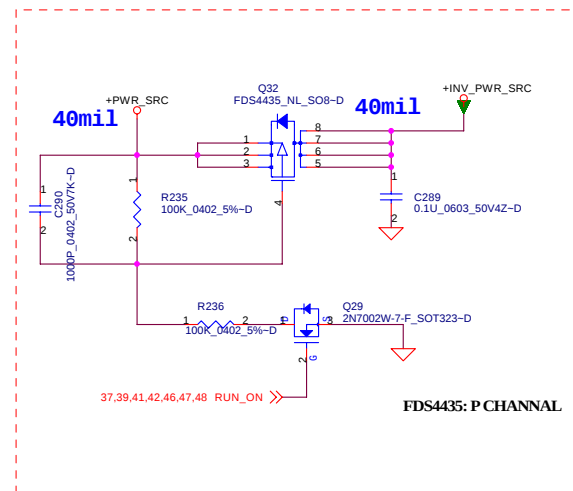
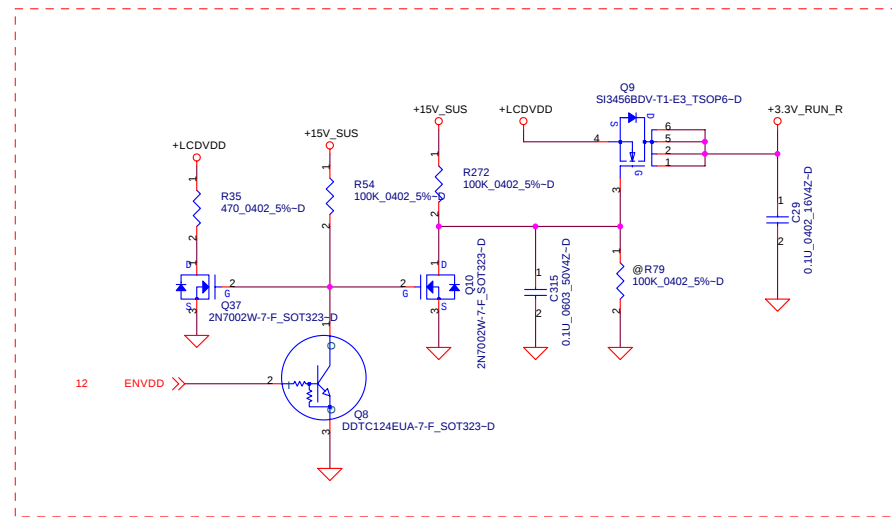
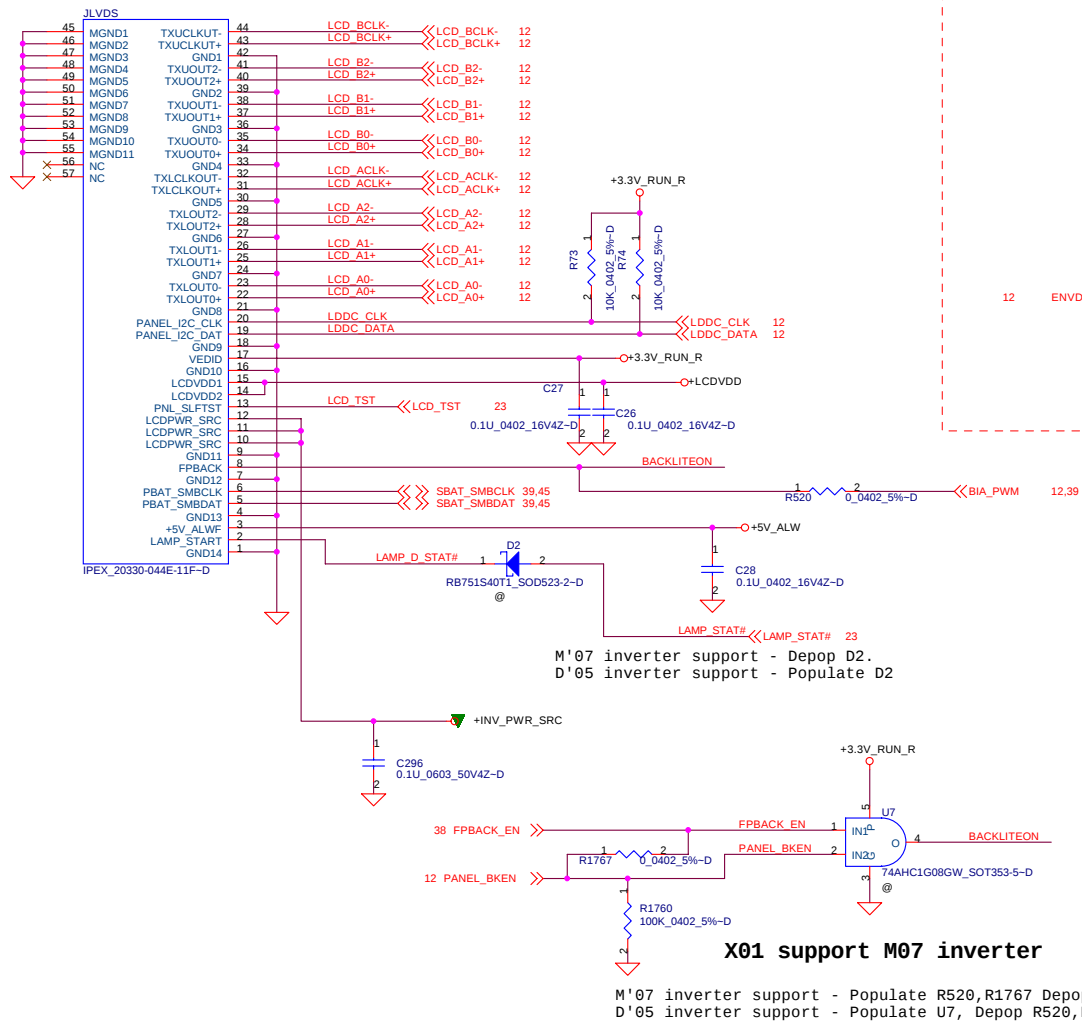
DP2, DN2 routing together. Trace width / Spacing = 10 / 10 mil



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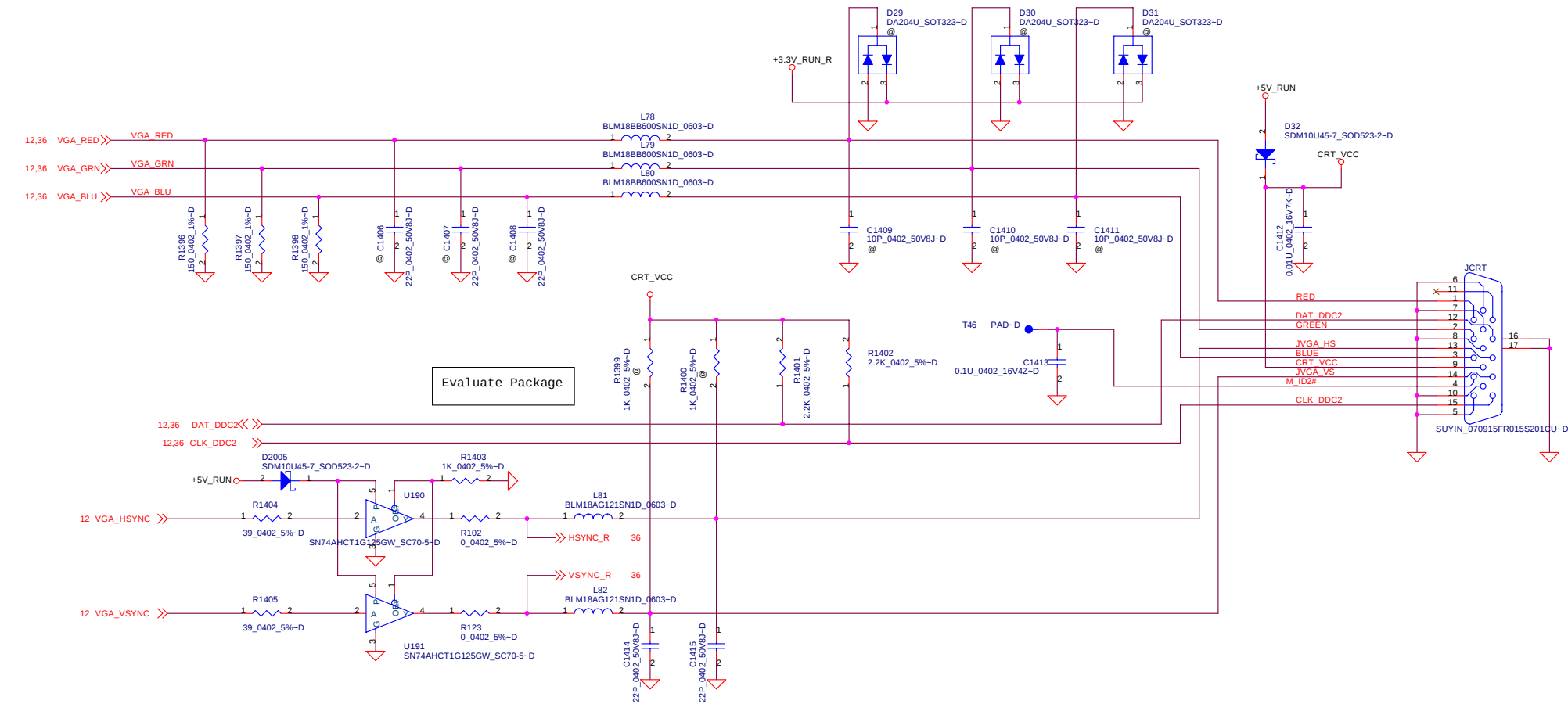
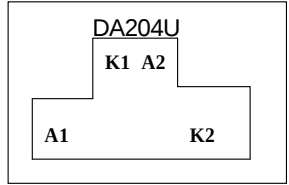
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Compal Electronics, Inc.

Title			Internal LVDS	
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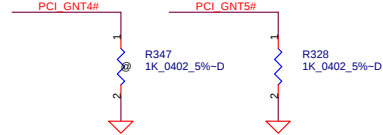
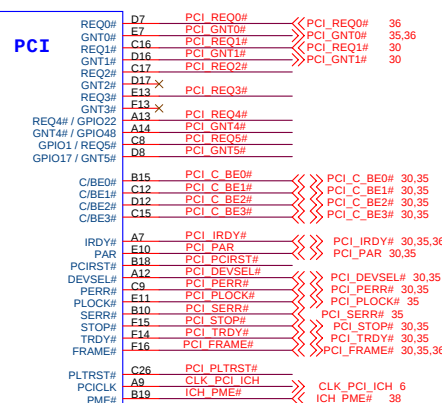
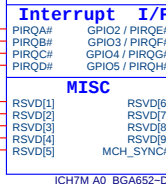
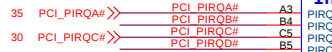
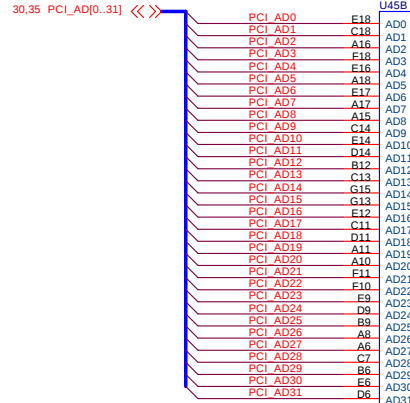
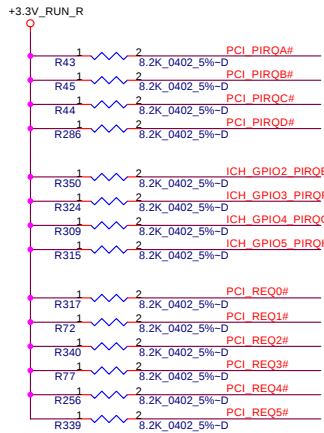
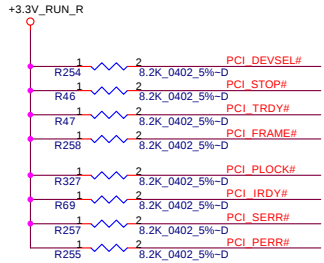
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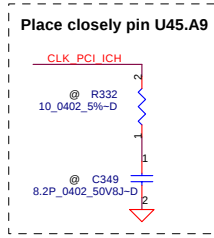
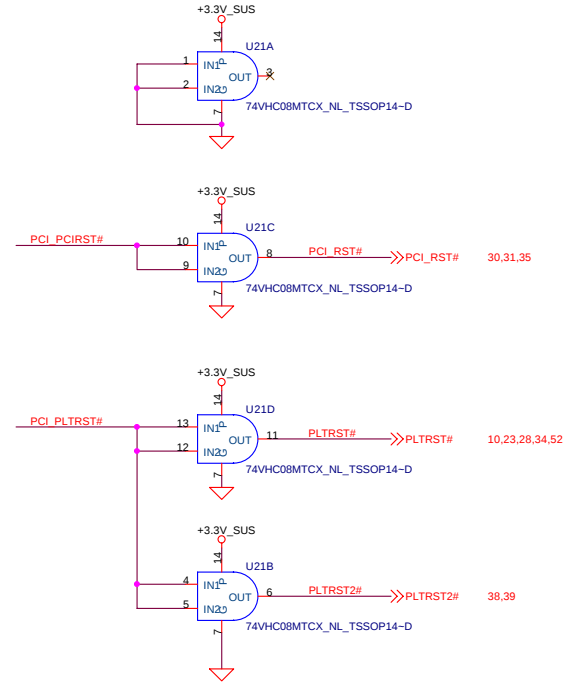
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	GNT5# R328	GNT4# R347
LPC (11)	unstuff	unstuff
PCI (10)	unstuff	stuff
SPI (01)	stuff	unstuff



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Title: **ICH7(1/4)**

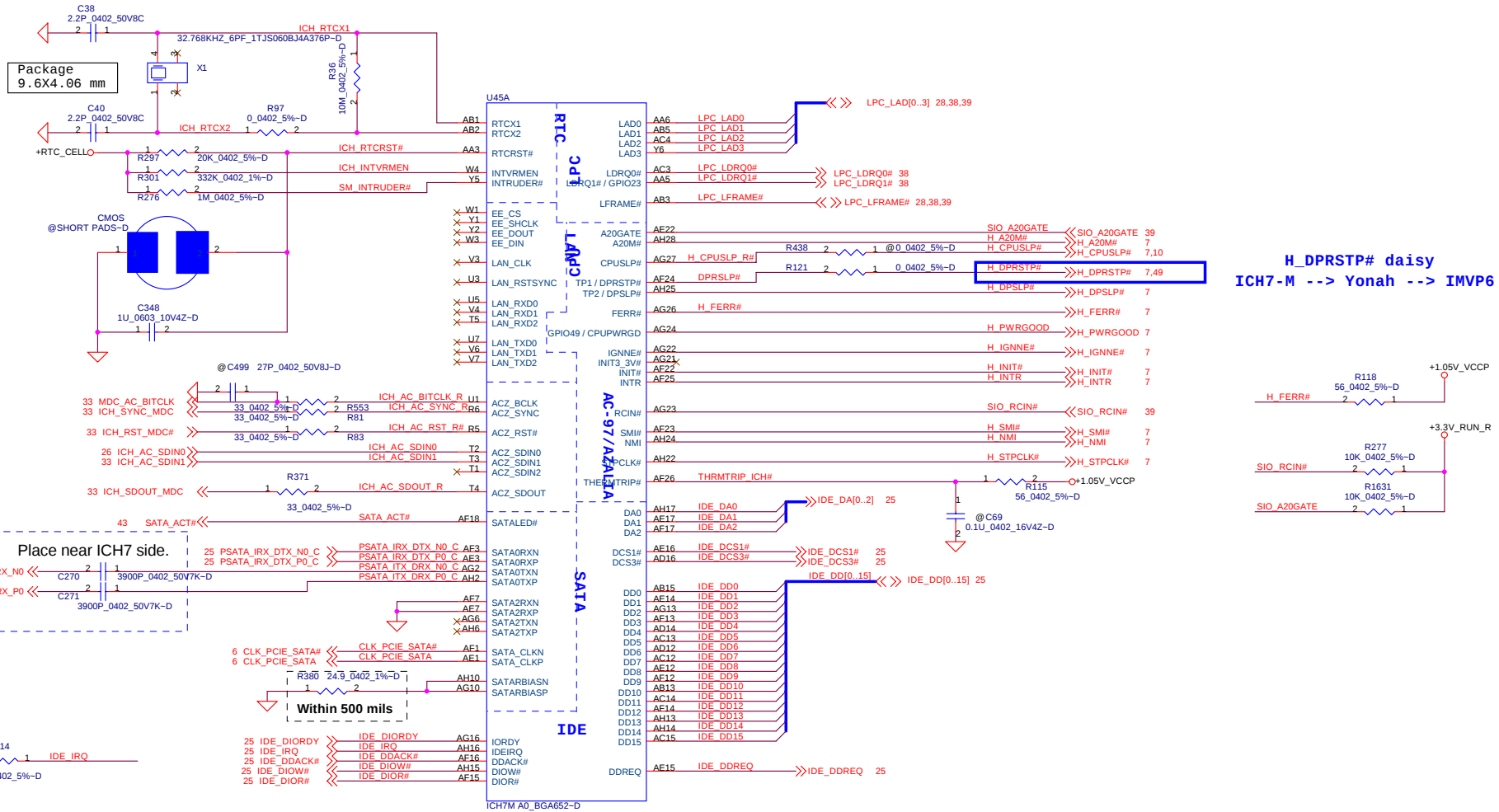
Size: **LA-2791**

Date: Tuesday, February 07, 2006

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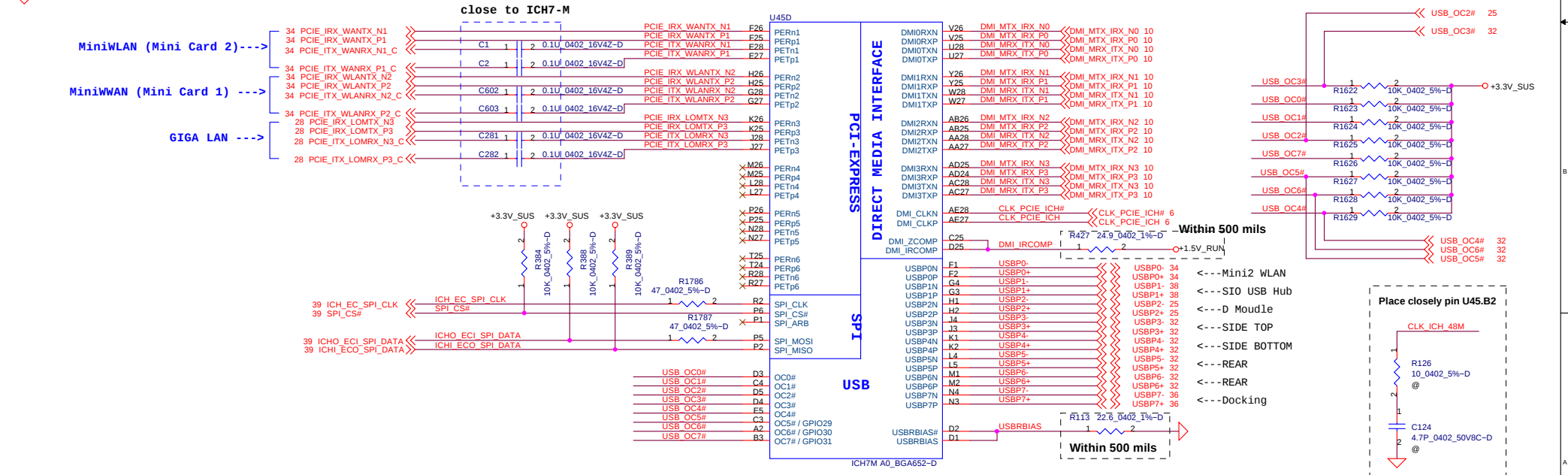
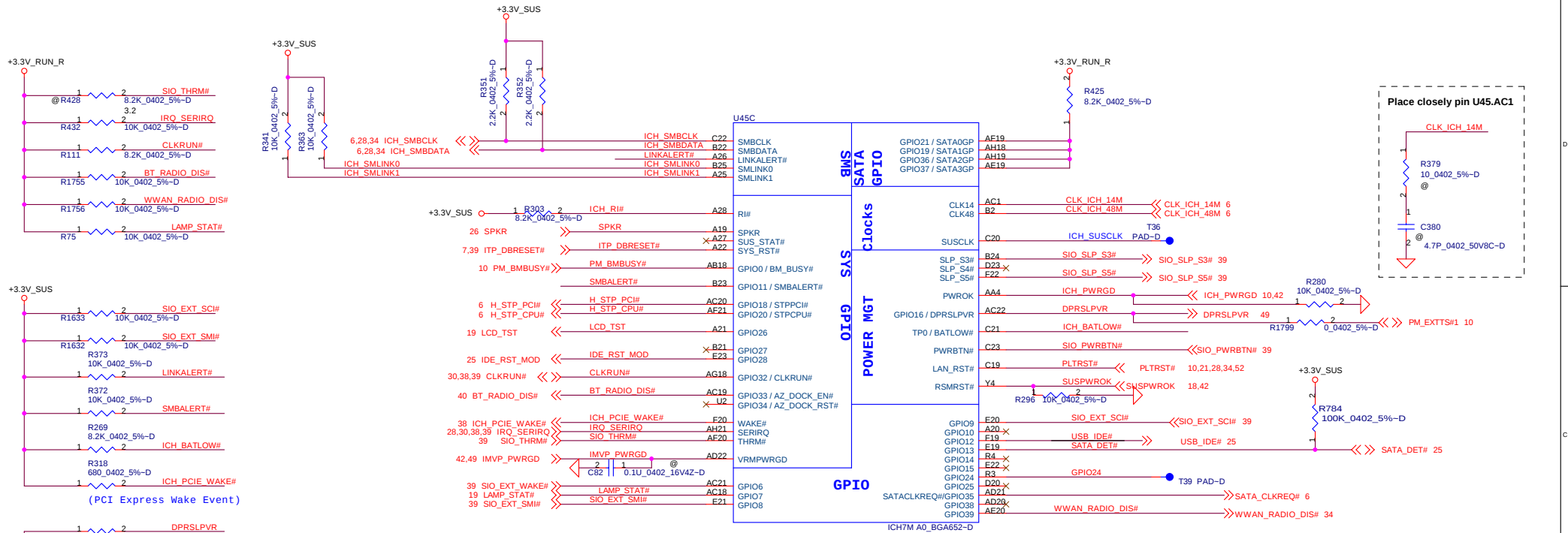


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Title		ICH7(2/4)	
Size	Document Number	Rev	
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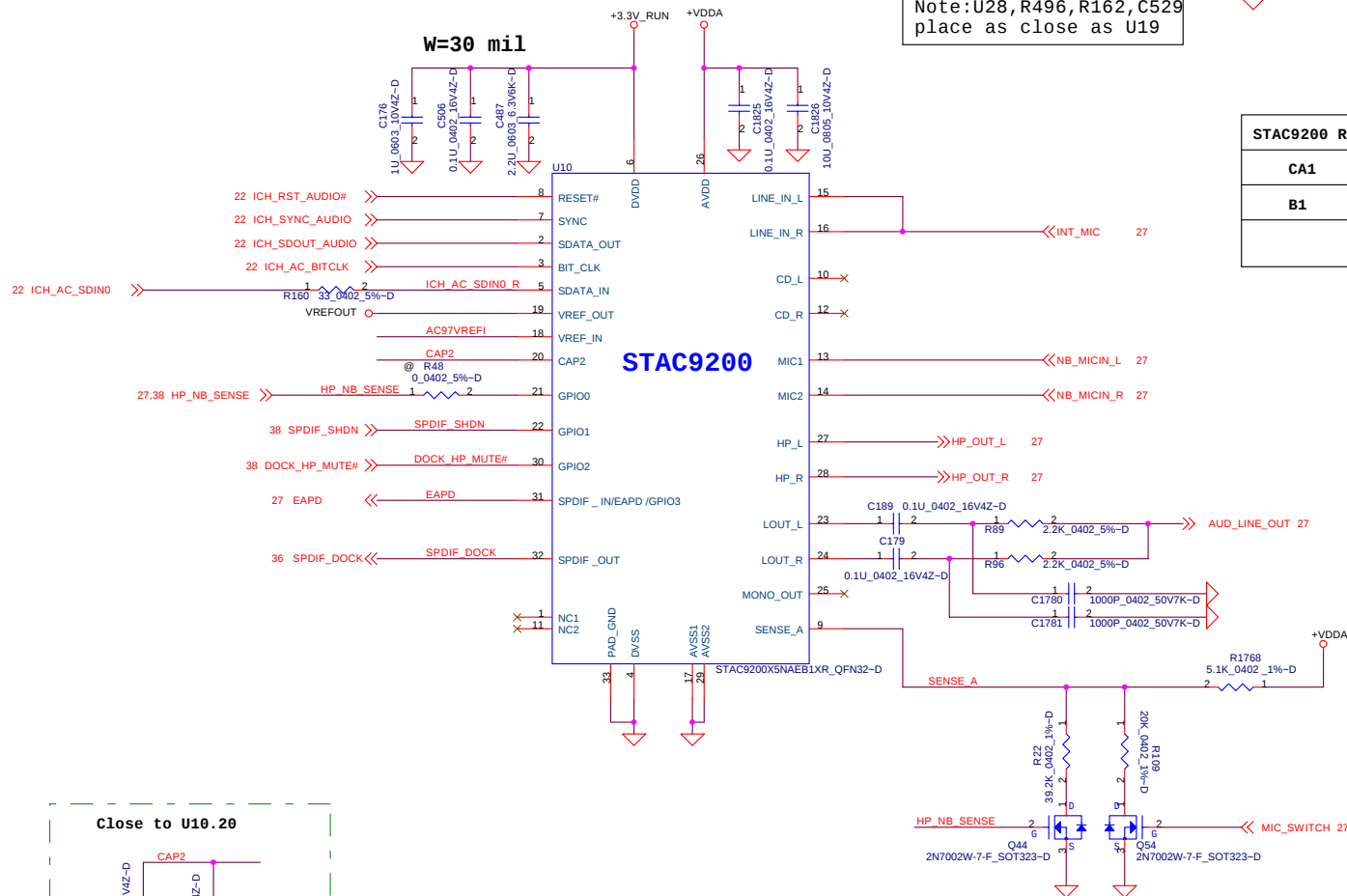
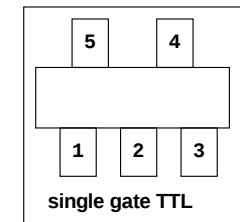
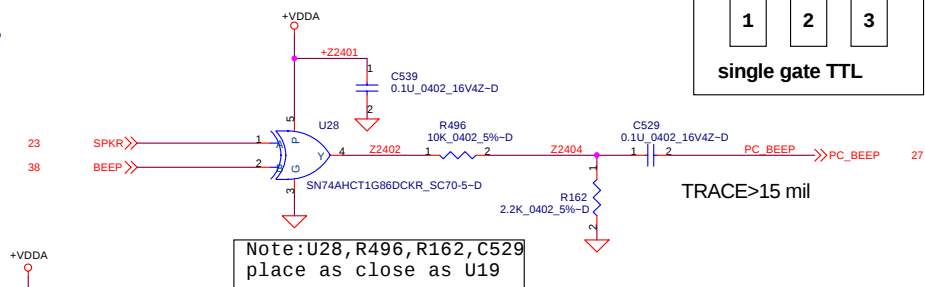
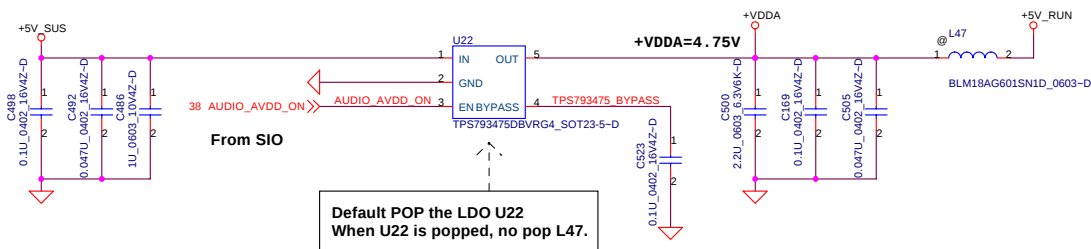
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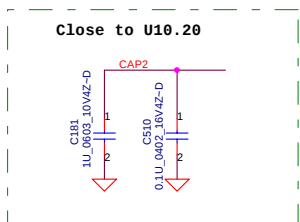
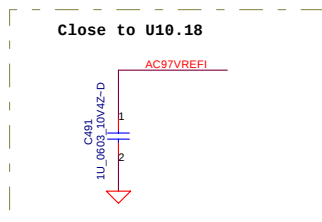
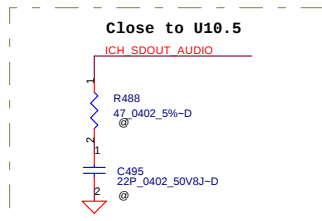
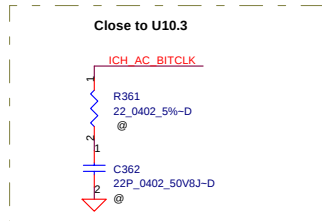
ICH7(3/4)

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STAC9200 Rev.	R22	R109
CA1	5.11K	10K
B1	39.2K	20K



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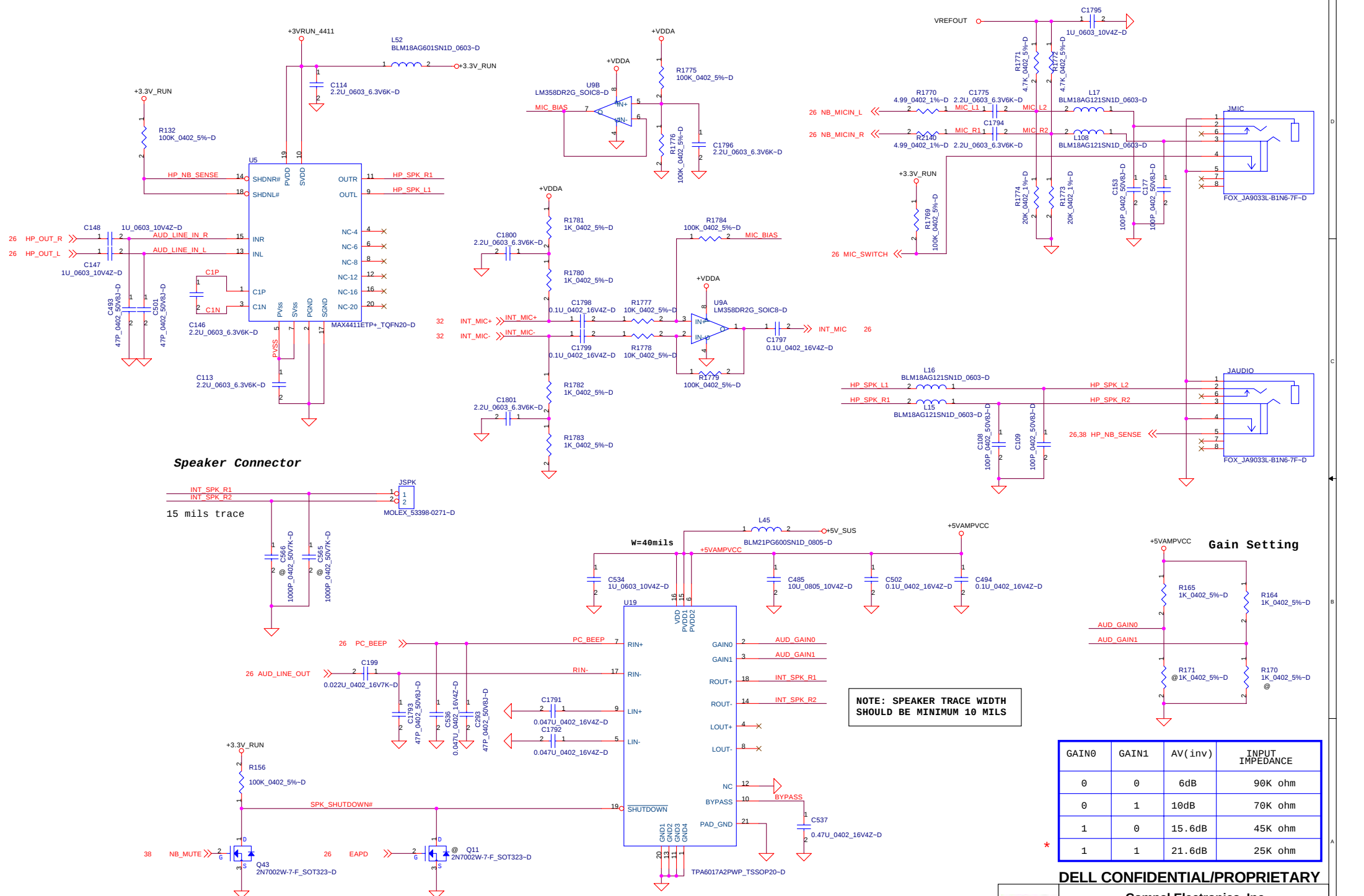
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Azalia (HD) Codec

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Speaker Connector

15 mils trace

NOTE: SPEAKER TRACE WIDTH SHOULD BE MINIMUM 10 MILS

Gain Setting

GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm

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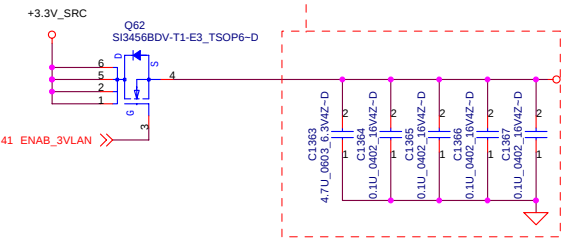
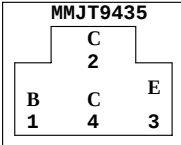
AMP and PHONE JACK

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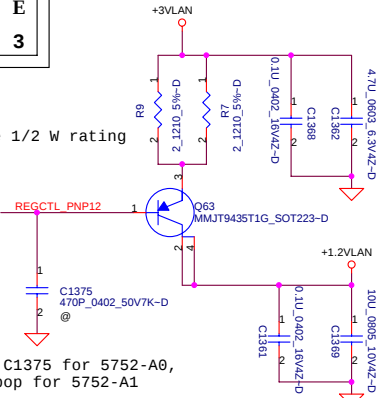
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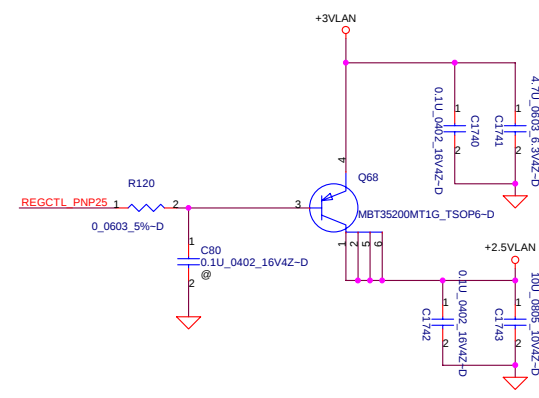
Layout Notice : Place as close chip as possible.



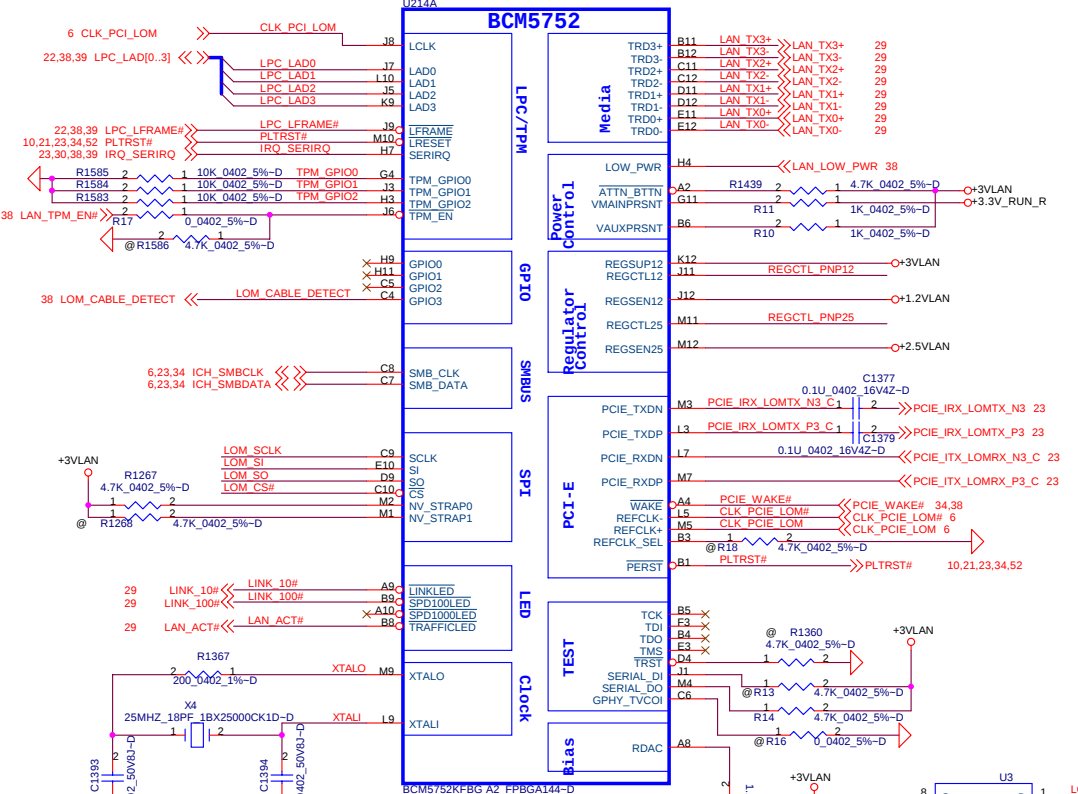
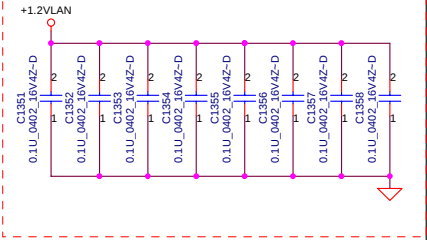
R7, R9 are 1/2 W rating



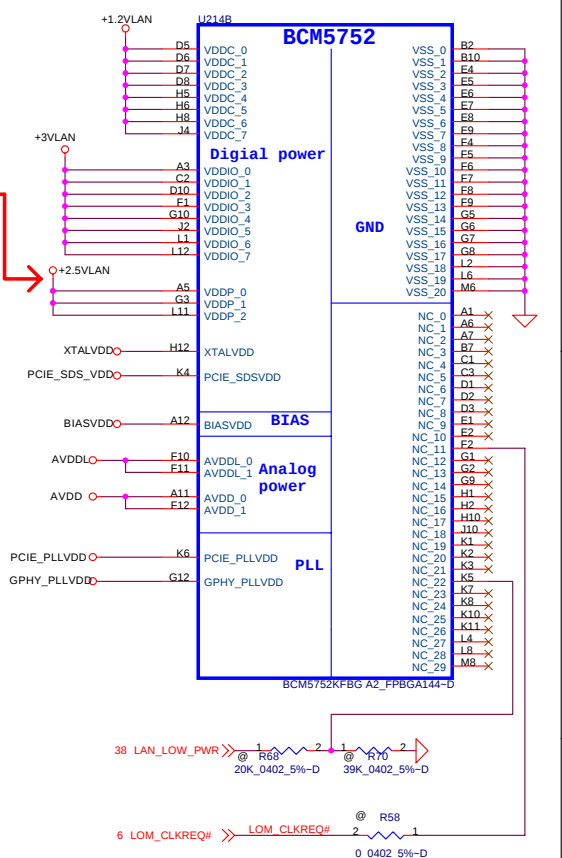
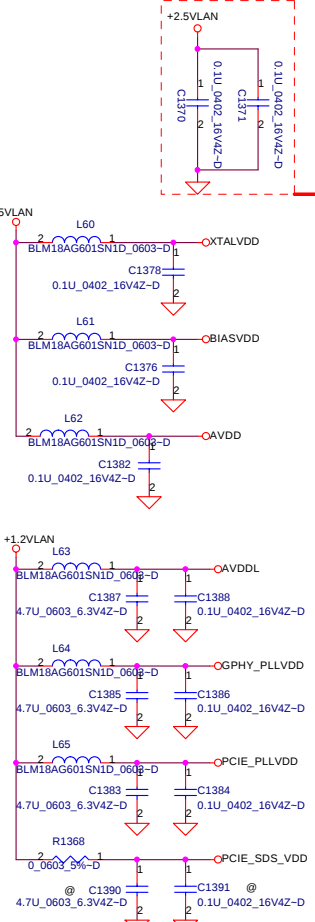
Pop C1375 for 5752-A0,
De-pop for 5752-A1



Layout Notice : 1.2V filter. Place as close chip as possible.



Place closely pin J8

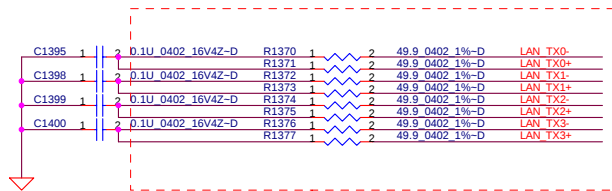


Layout Notice : No high speed signal should be routed near RDAC or on adjacent layer to RDAC

	NV_STRAP1	NV_STRAP0	SO	SI	CS#	SCLK
Atmel AT45BCM021B	0	0	1	0	1	1
ST M45PE20	0	1	1	0	0	1

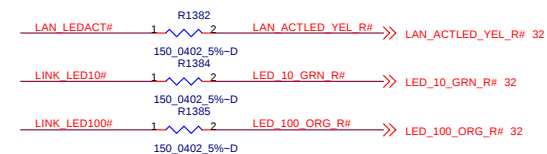
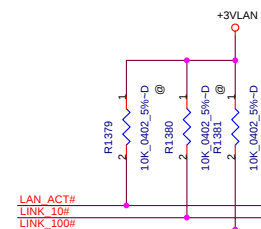
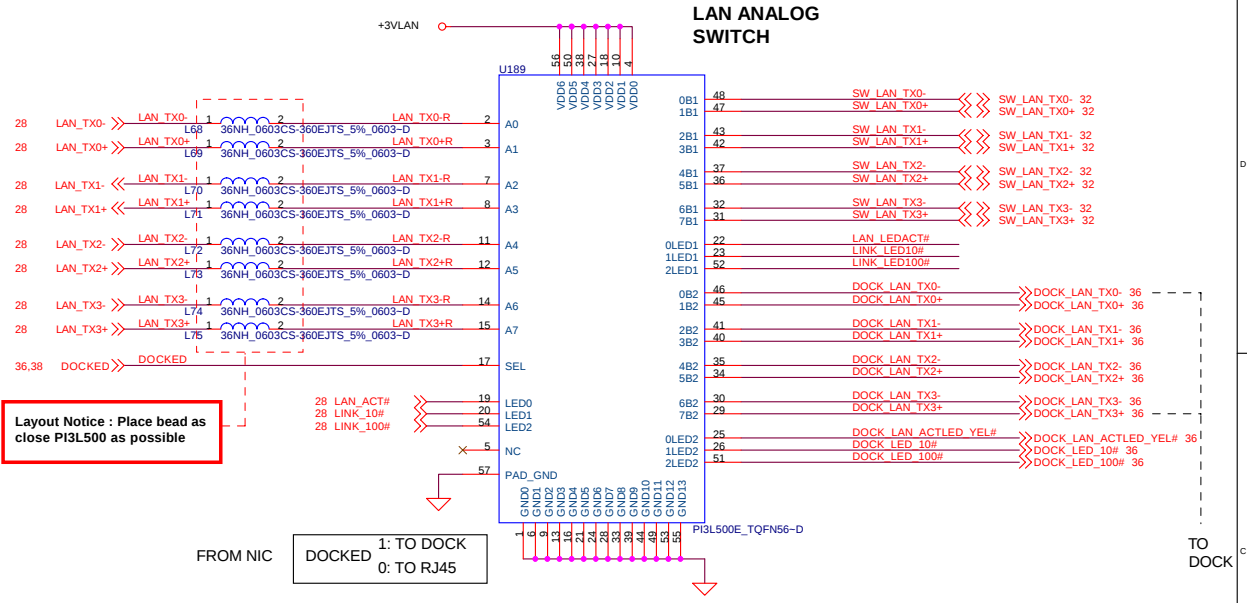
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Layout Notice : Place termination as close as ASIC as possible

The resistors need at least 1/16W

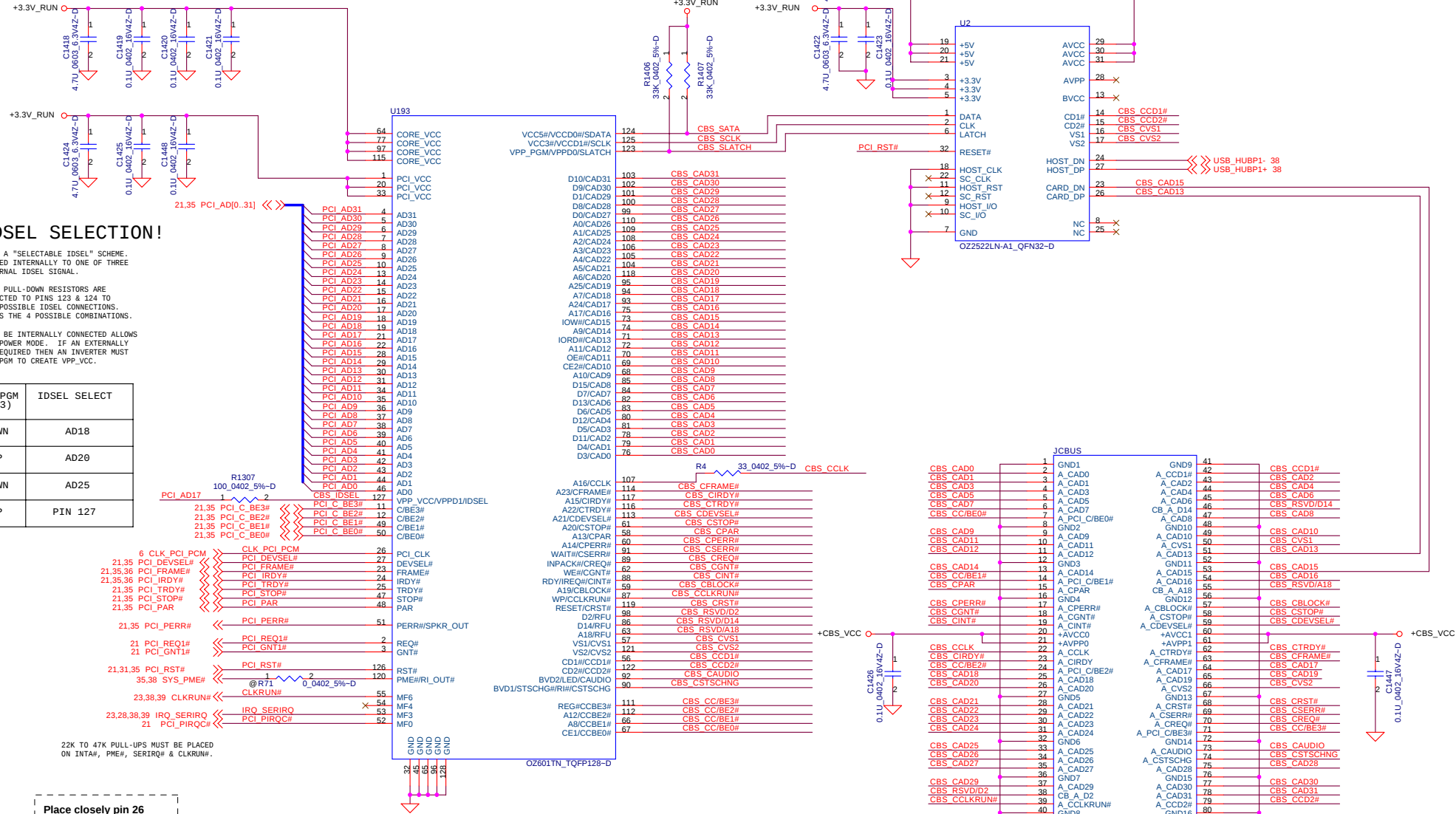


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NOTE:
THIS PAGE SHOWS THE OZ601B CONFIGURED WITH
EXTERNAL IDSEL AND WITHOUT 12V VPP SUPPORT.

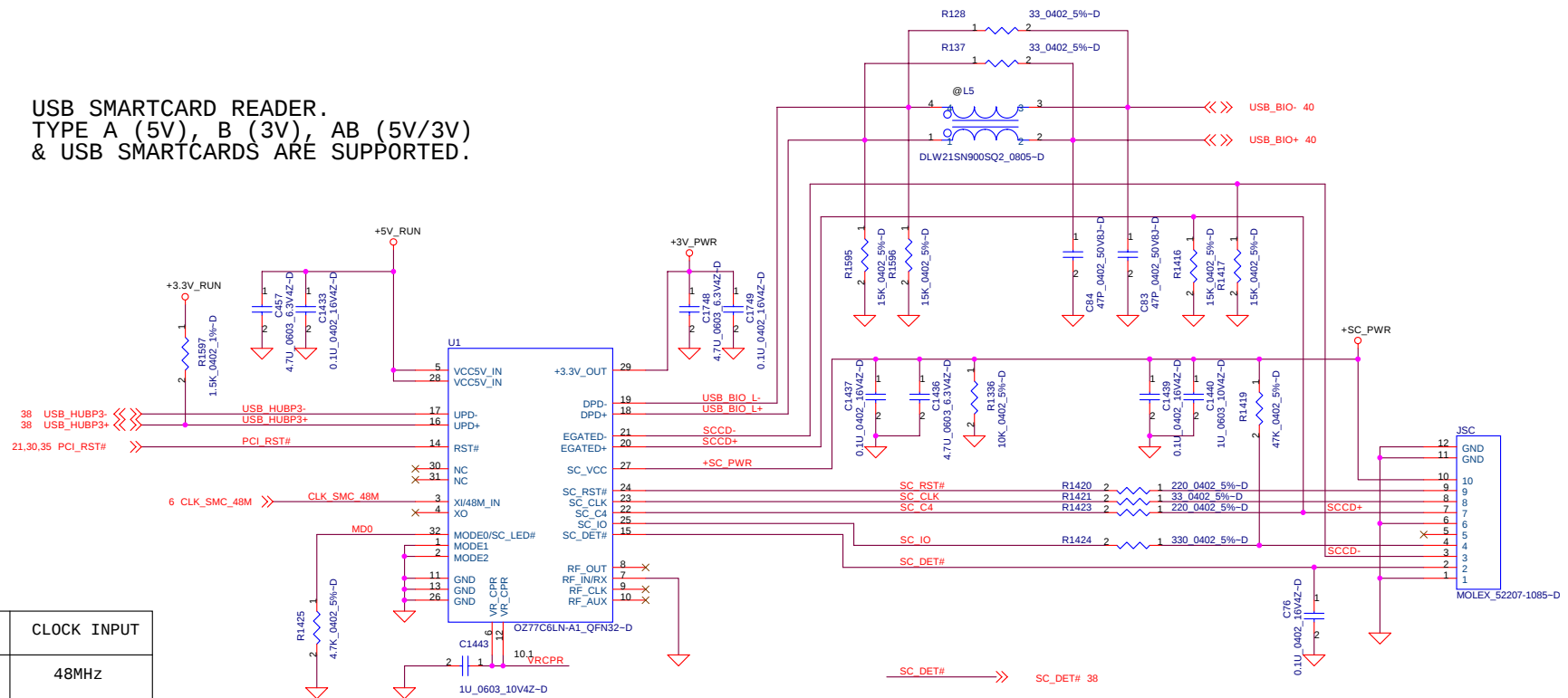
IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)



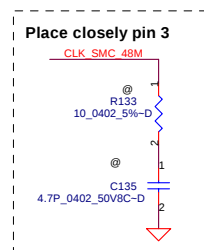
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Card Bus OZ601			
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USB SMARTCARD READER.
TYPE A (5V), B (3V), AB (5V/3V)
& USB SMARTCARDS ARE SUPPORTED.



MODE1	CLOCK INPUT
LOW	48MHZ
HIGH	6MHz Crystal



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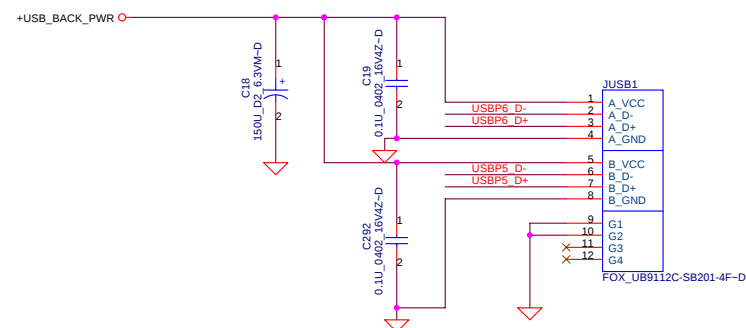
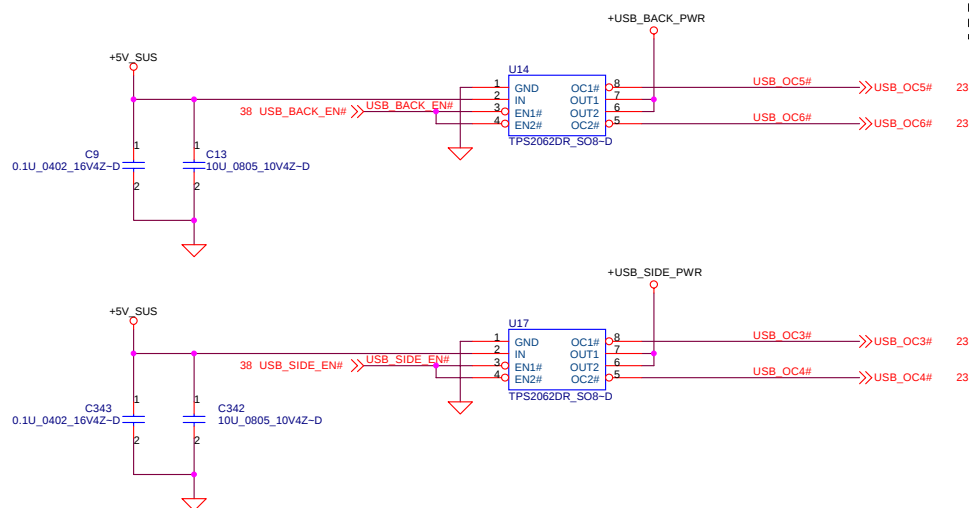
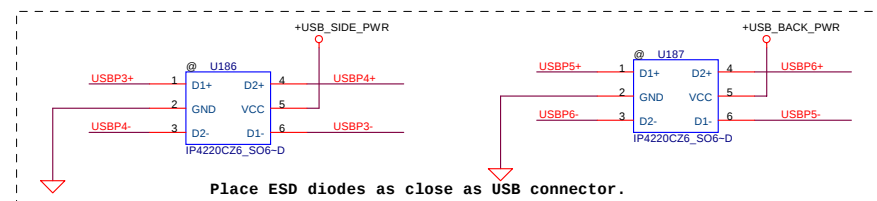
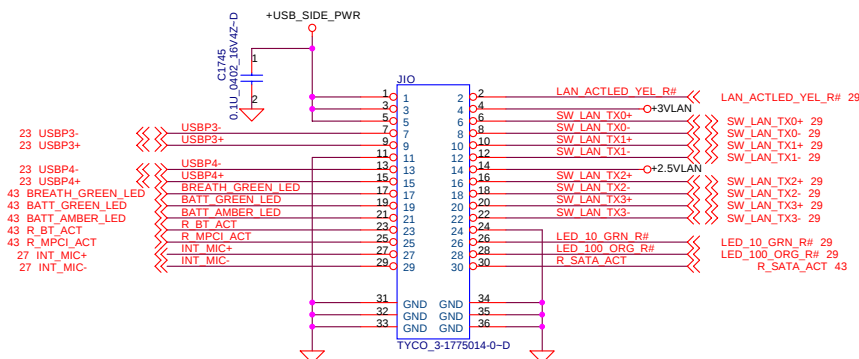
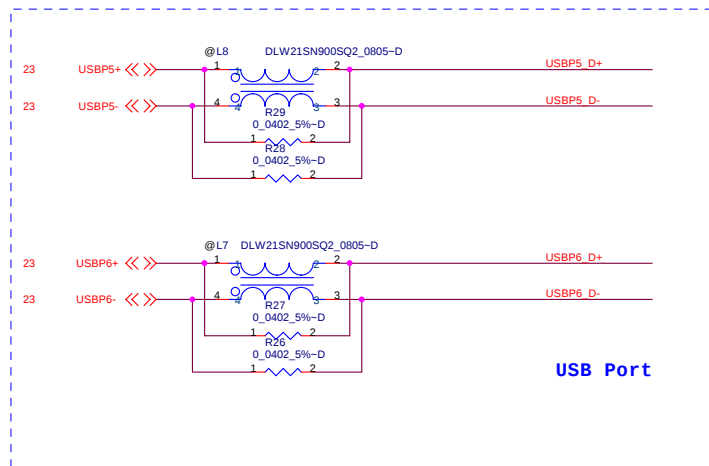
Smart Card OZ77C6

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Rear USB Ports

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Compal Electronics, Inc.

USB 2.0 Port

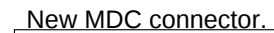
LA-2791

Rev 0.6

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1	GND	RES	2
3	IAC_SDATA0	RES	4
5	GND	3.3V	6
7	IAC_SYNC	GND	8
9	IAC_SDATAIN	GND	10
11	IAC_RESET#	IAC_BITCLK	12



Compal Electronics, Inc.

BT PORT and MDC

LA-2791

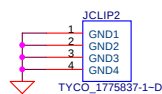
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Date: Tuesday, February 07, 2006 Sheet 33 of 63

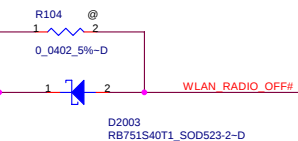
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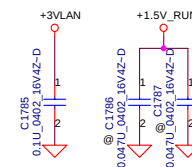
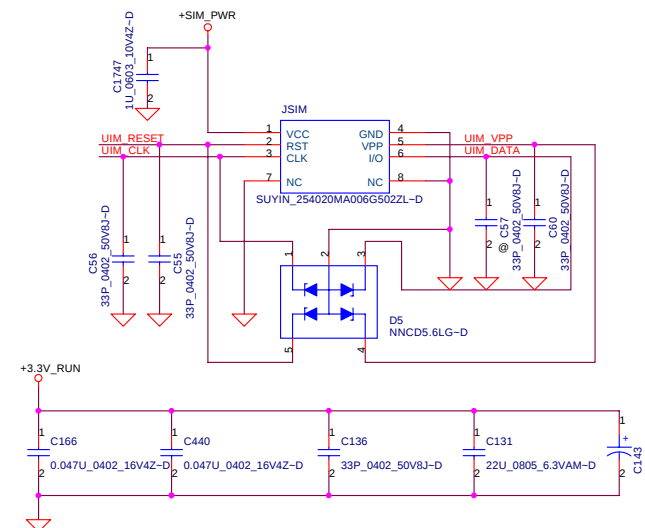
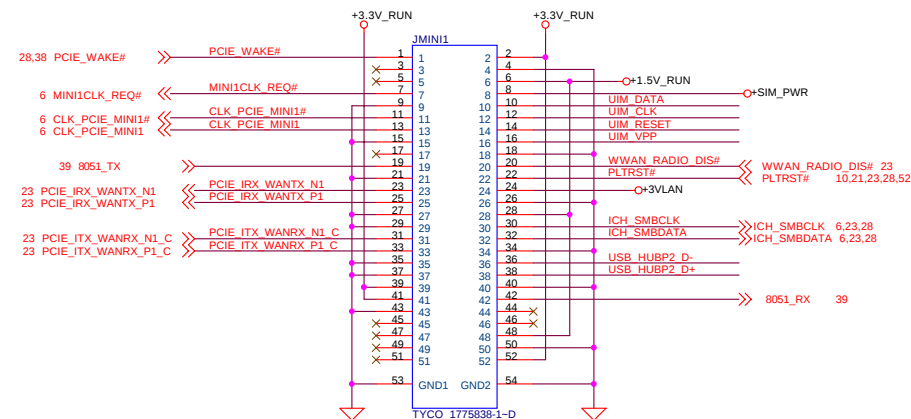
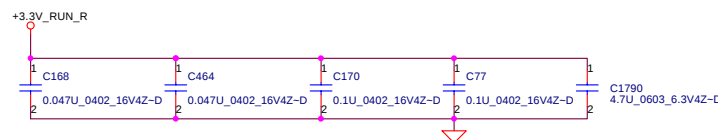
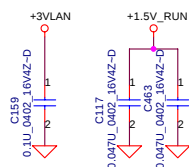
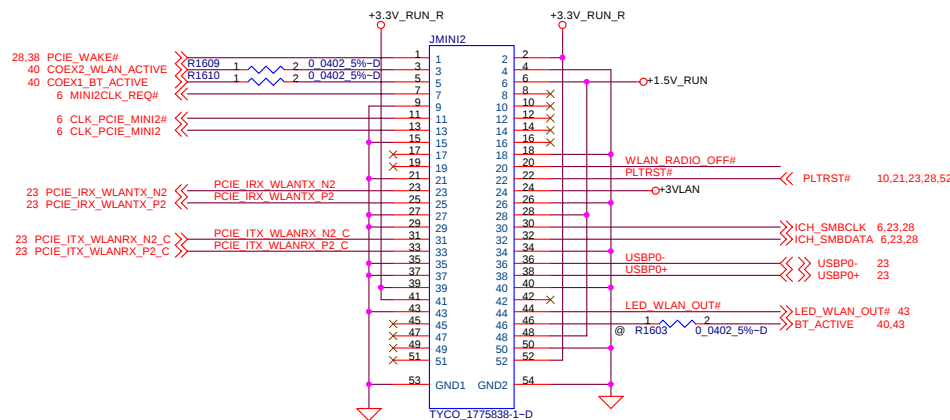
Mini-Card Latch



Mini-Card Latch



Mini Card Wire less LAN



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+ -9%	1000	750	
+3.3Vaux	+ -9%	330	250	250 (wake enable) 5 (Not wake enable)
+1.5V	+ -5%	500	375	NA

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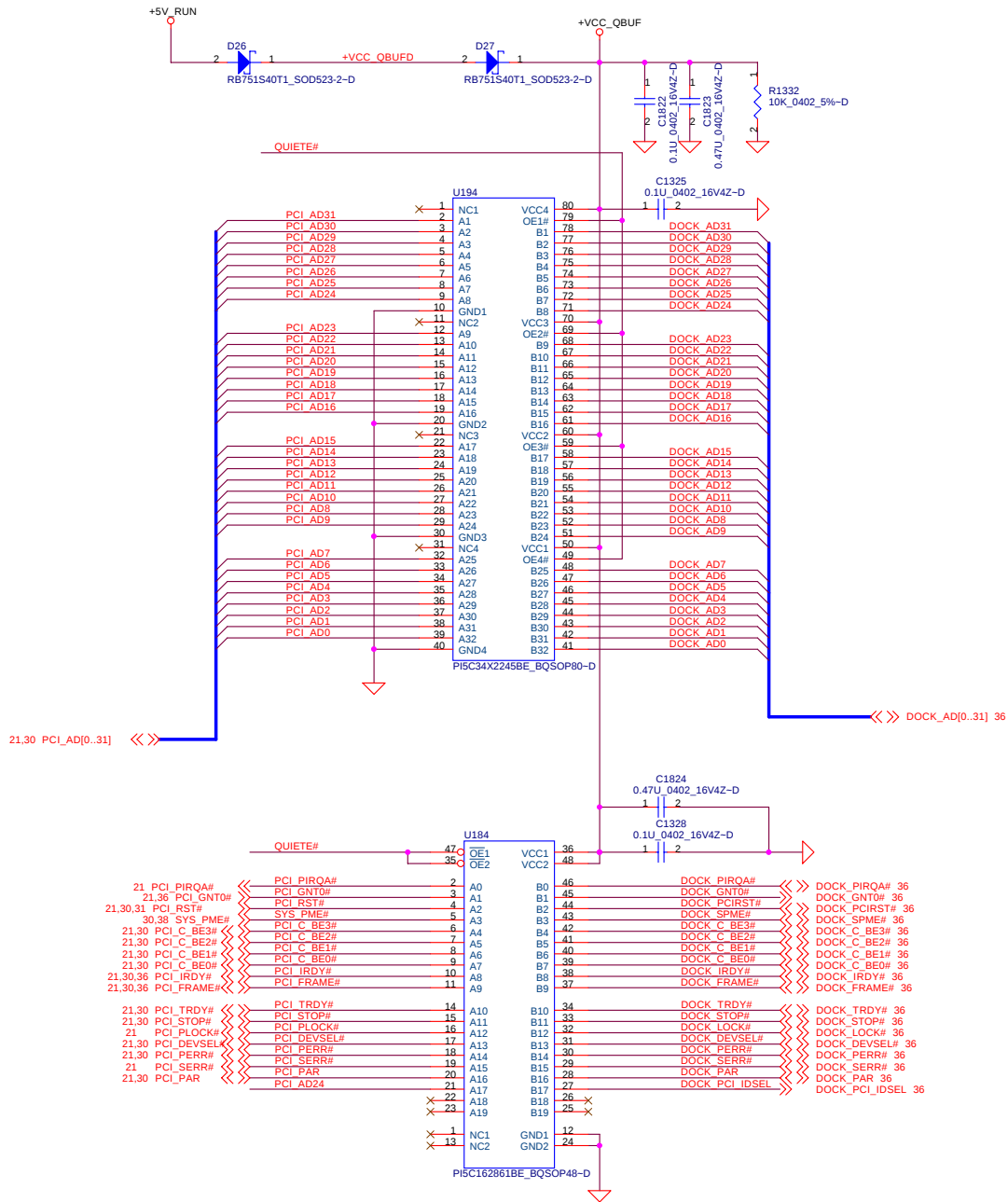
Mini Card

LA-2791

Size Document Number
LA-2791
Date: Tuesday, February 07, 2006

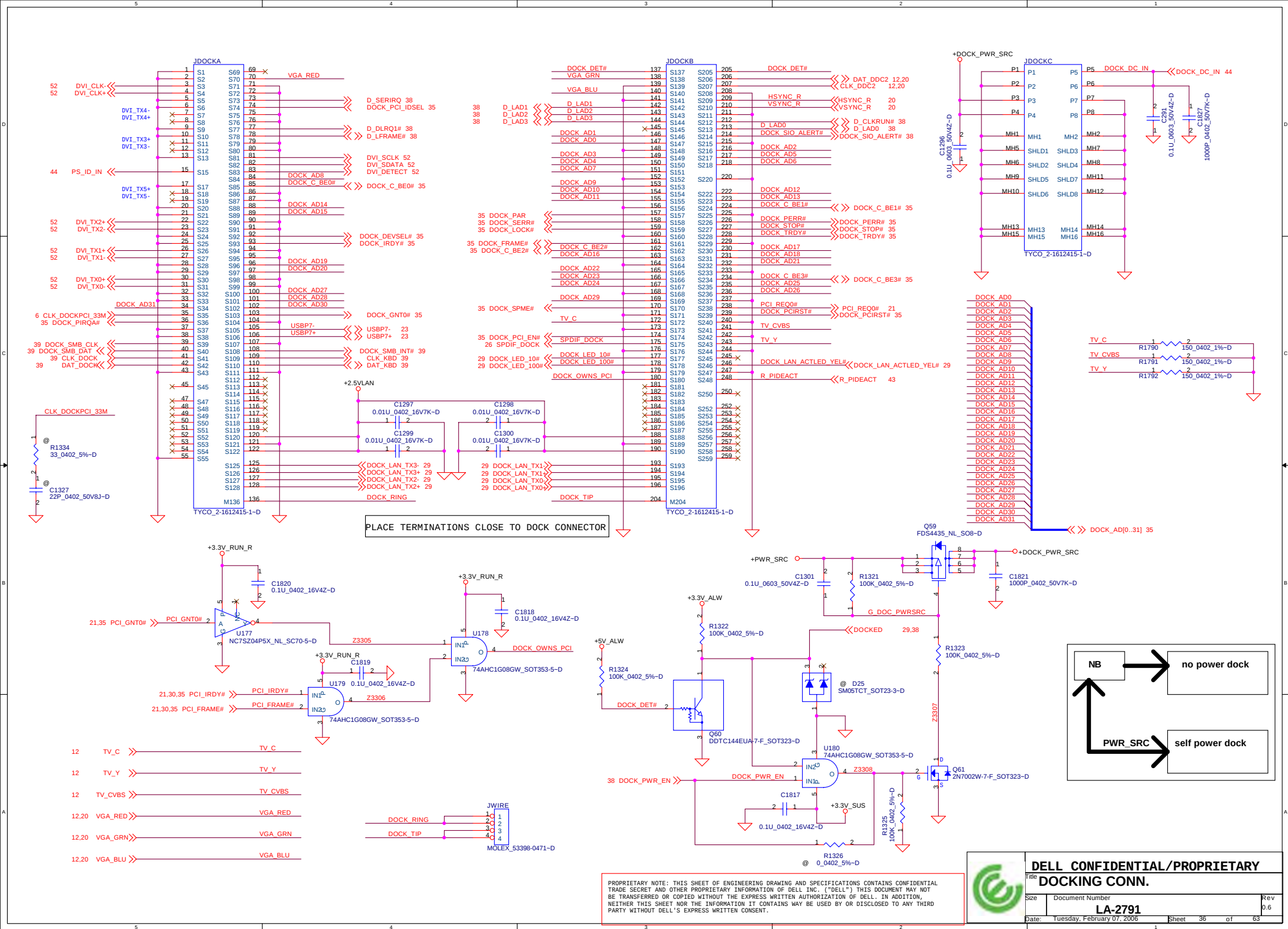
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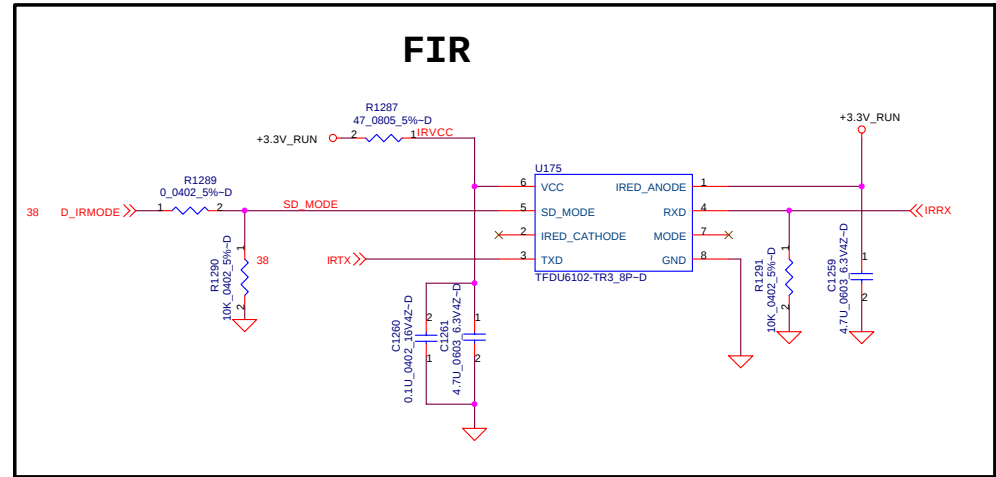
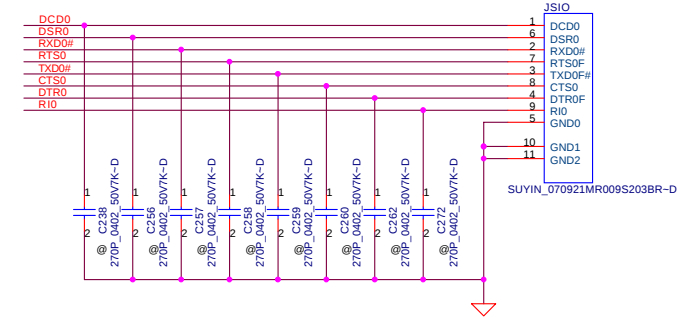
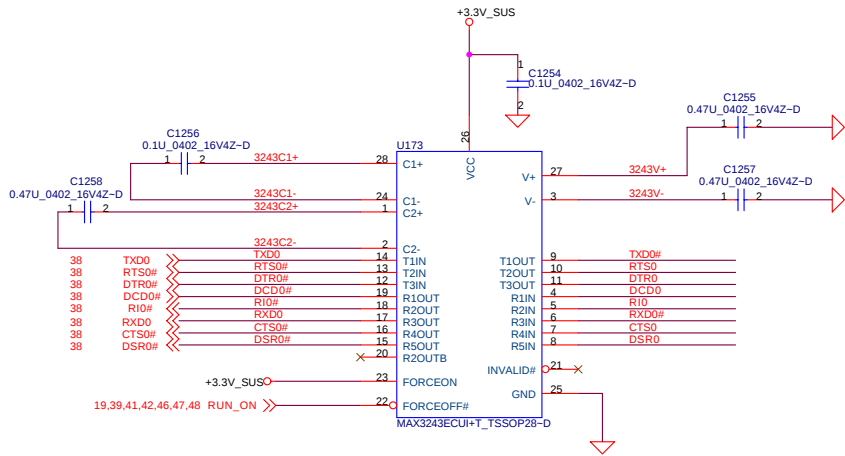
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		Title	
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Size	Document Number	Rev	
		0.6	
Date:	Tuesday, February 07, 2006	Sheet	35 of 63

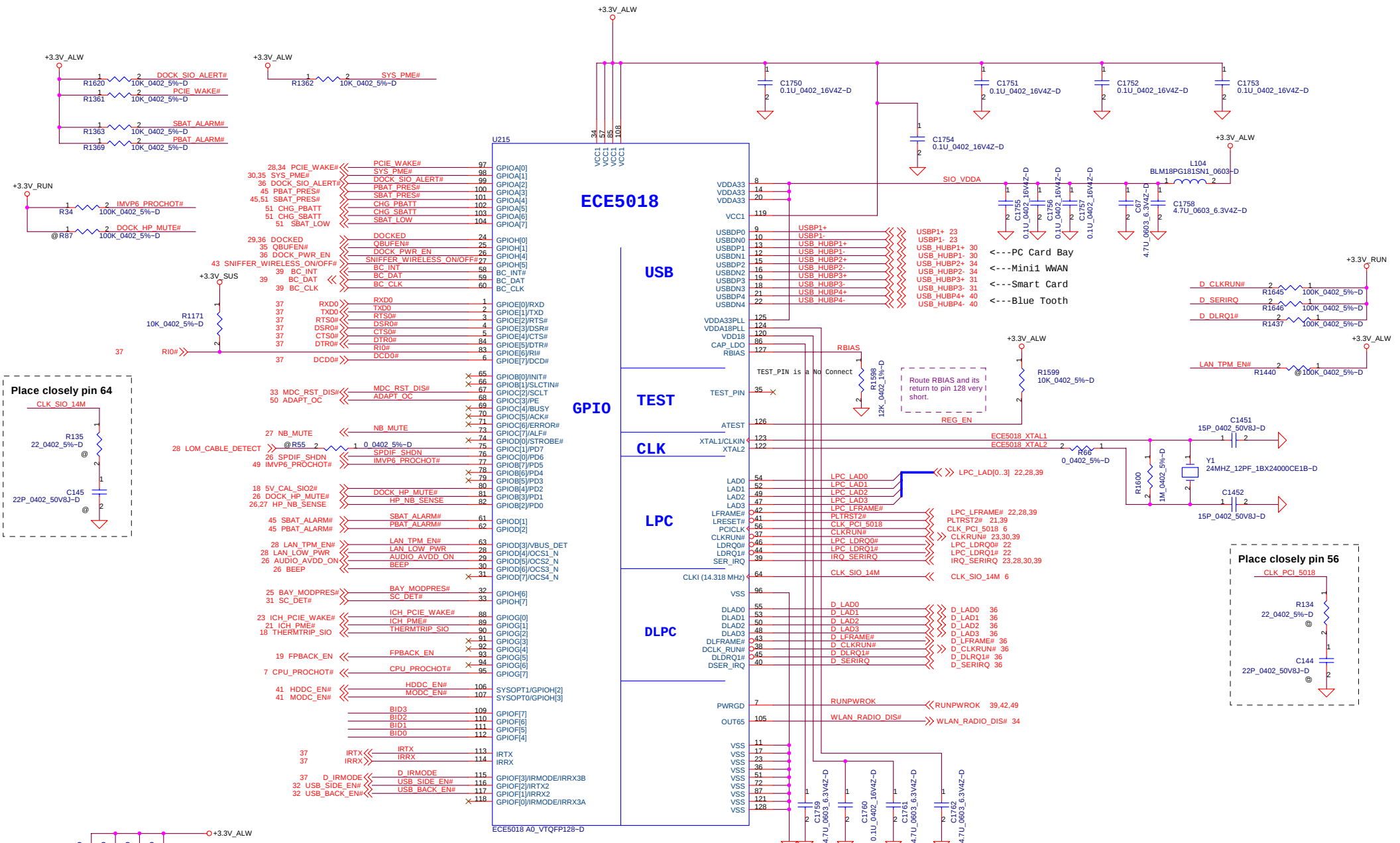




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Size	Document Number
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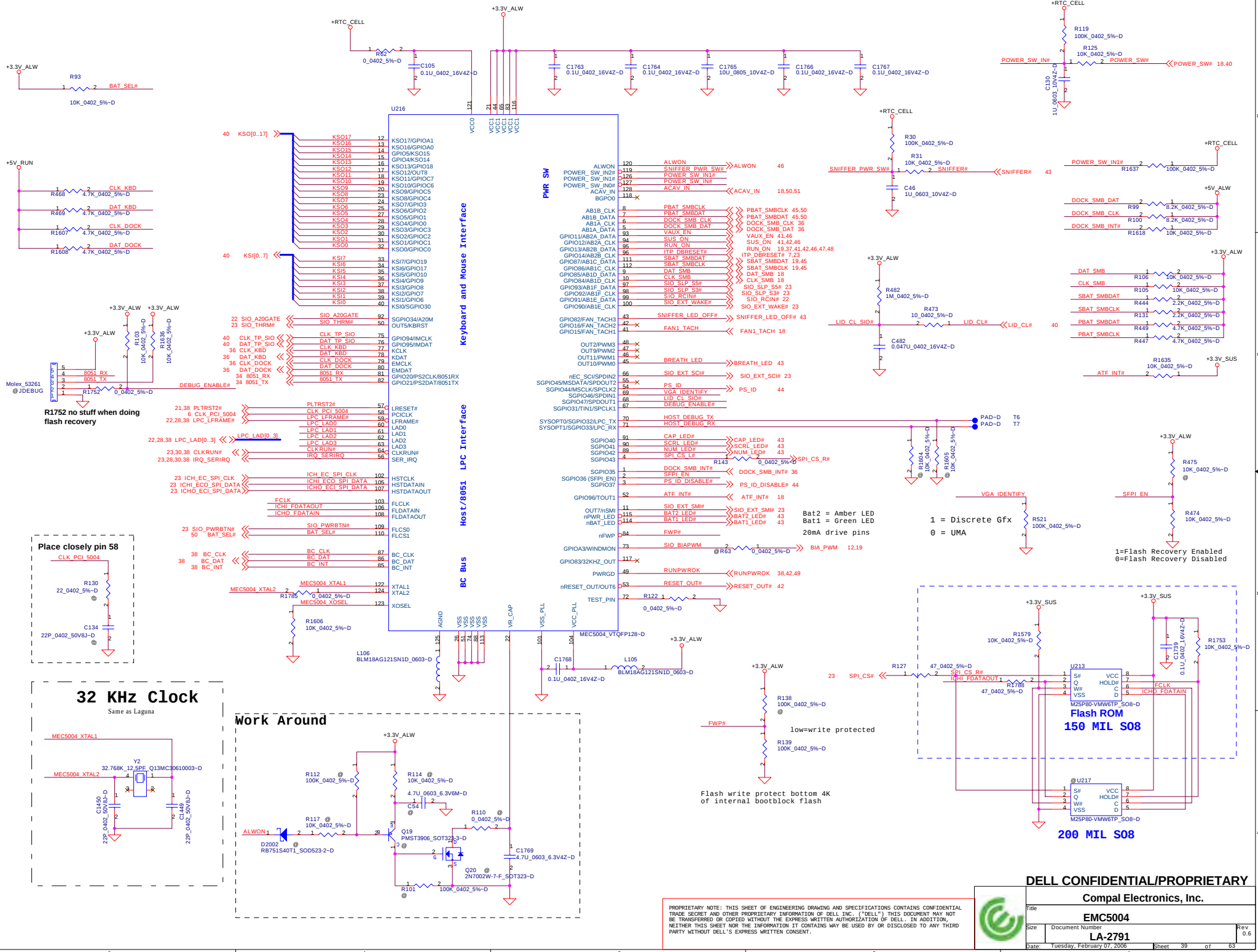
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0	1	0	1	X03

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ECE5018		
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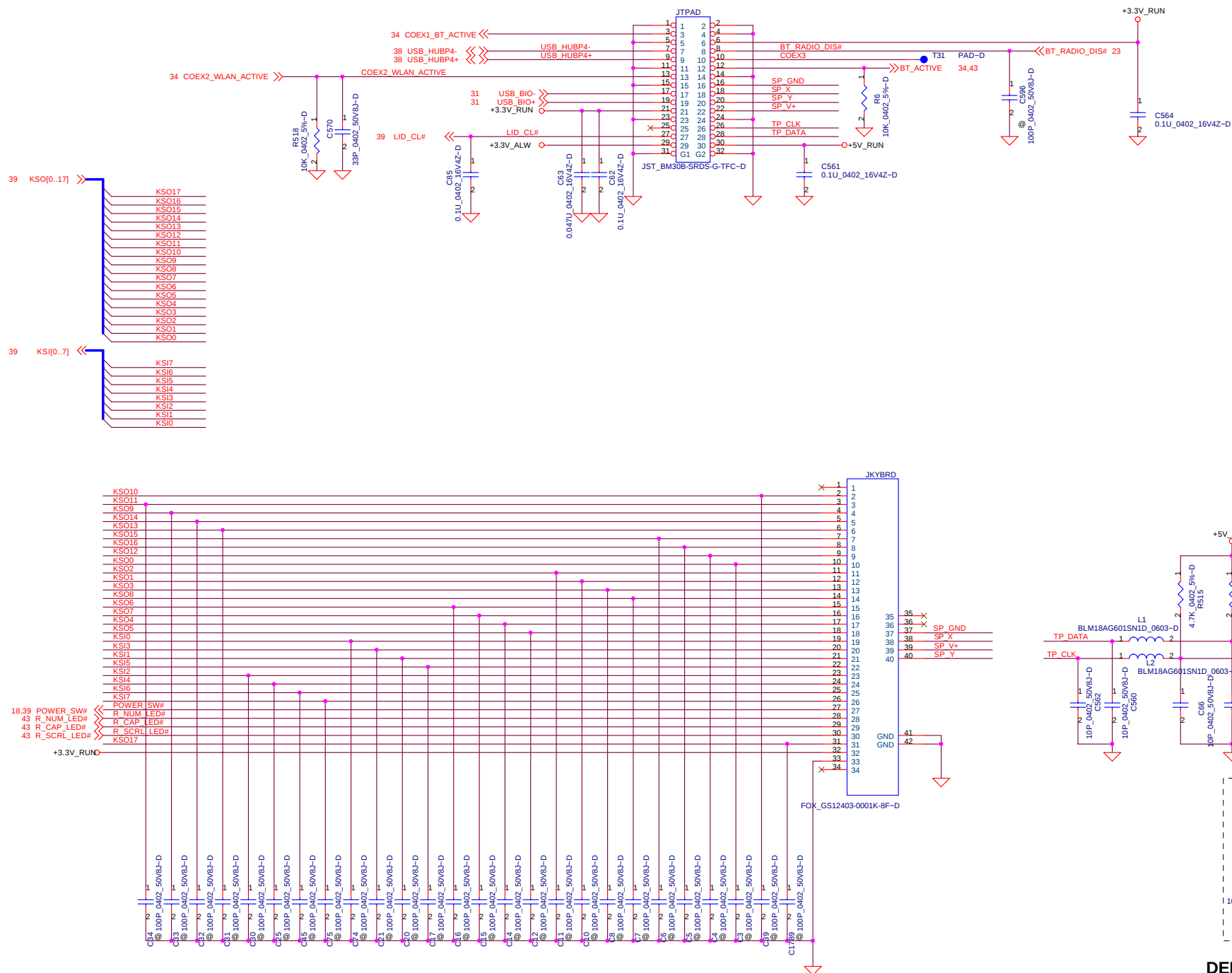
Compal Electronics, Inc.

EMC5004

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Touch PAD



FAN	
Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

PCMCIA BODY	
Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

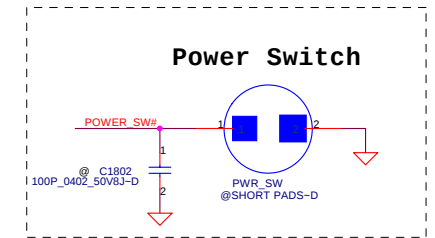
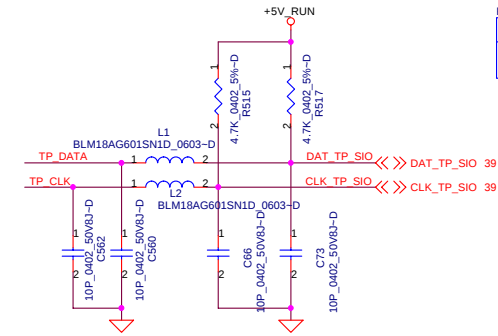
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Part Number	Description
DC020003Z0L	H-CONN SET ZJX MB-MDC

Part Number	Description
DC020004T0L	H-CONN SET ZJX MB-TP

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL



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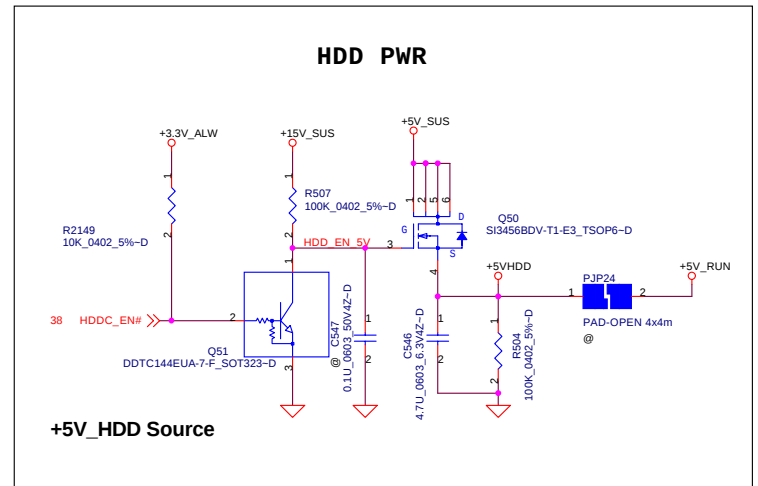
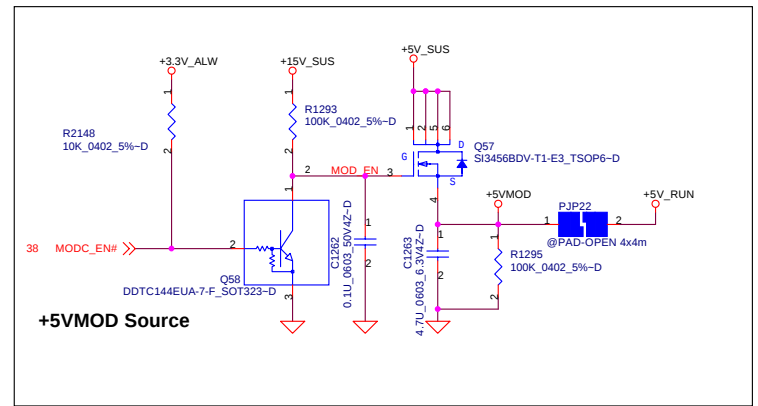
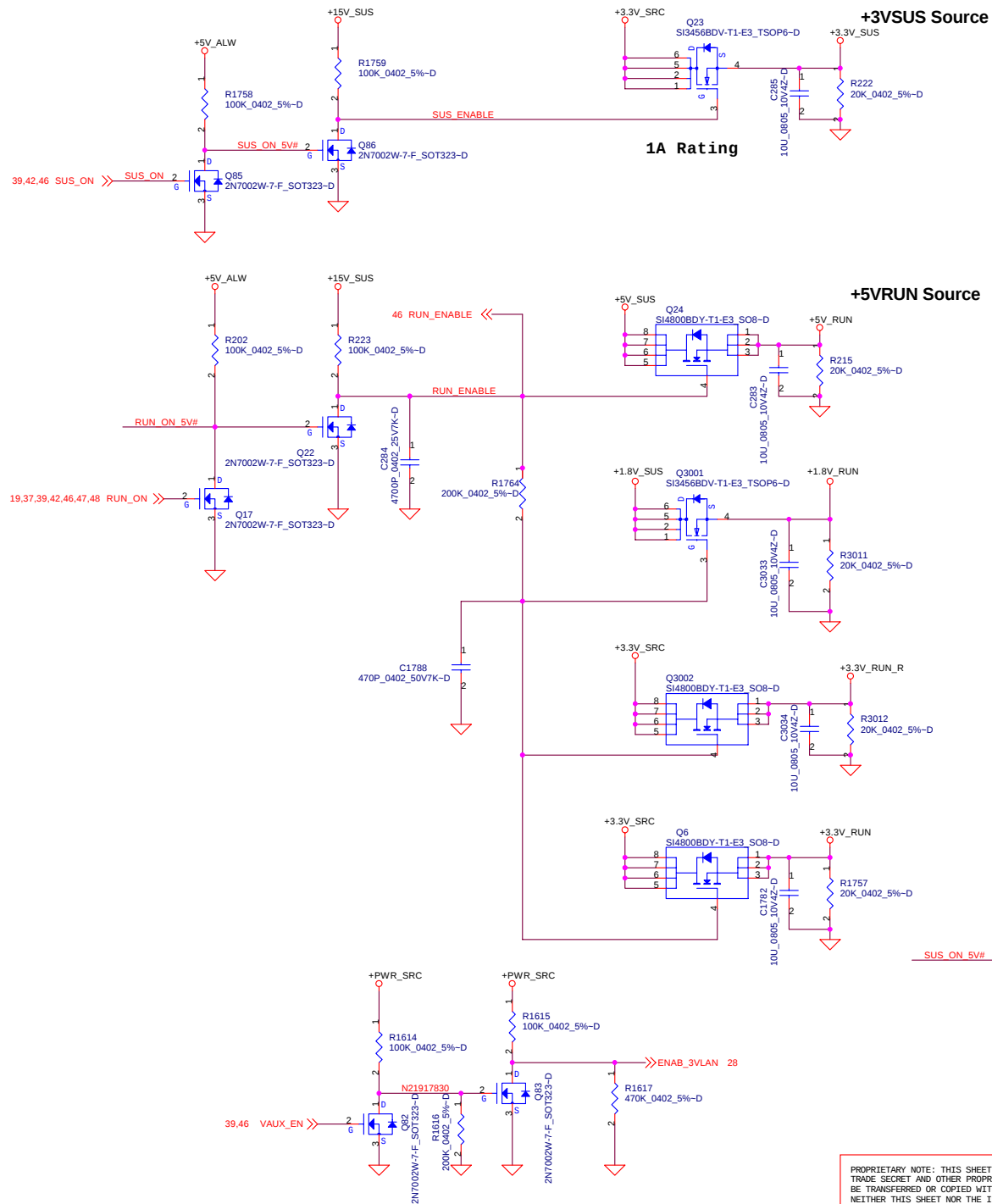
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Date: Tuesday, February 07, 2006

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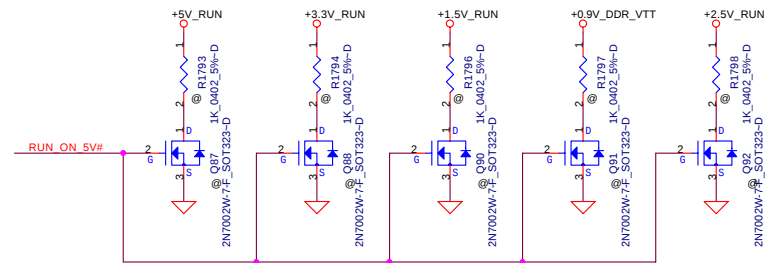
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DC/DC Interface



Discharg Circuit



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POWER CONTROL

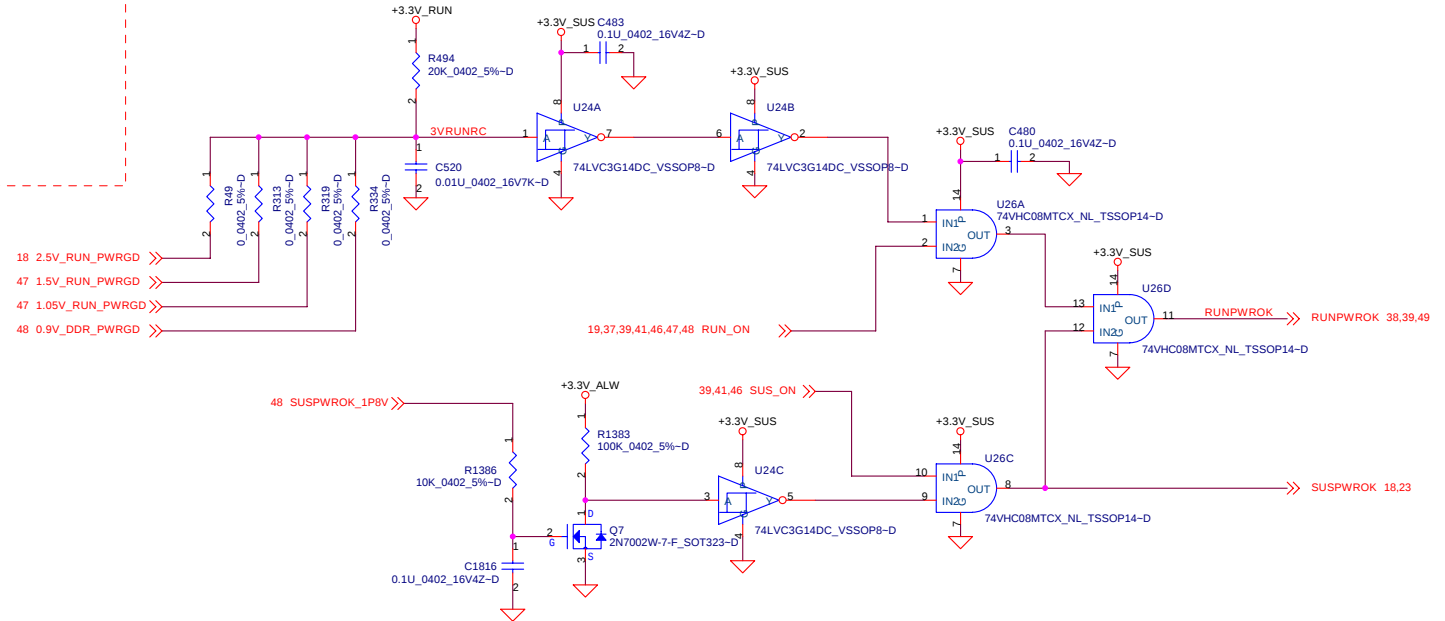
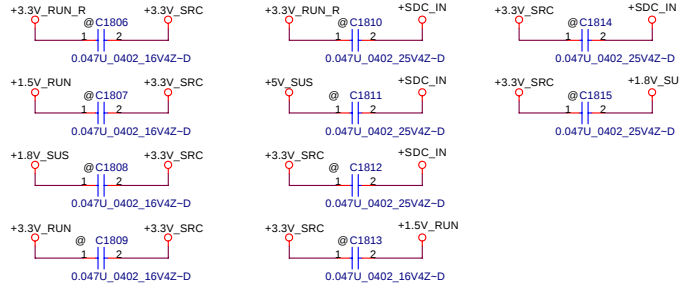
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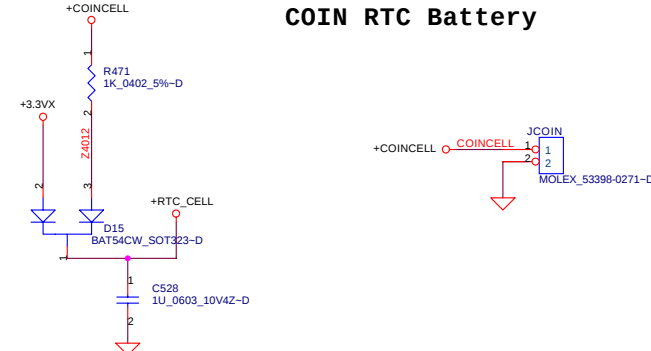
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For EMI



COIN RTC Battery



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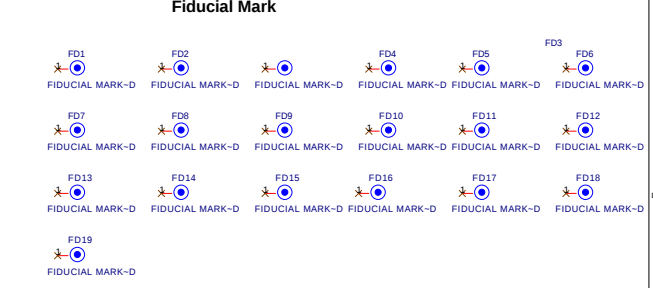
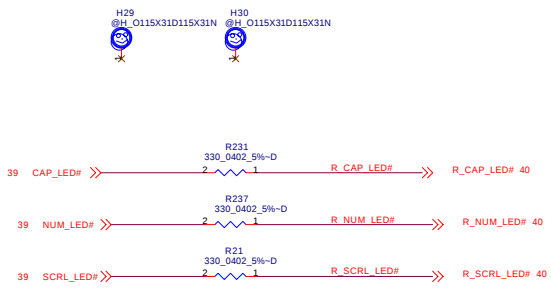
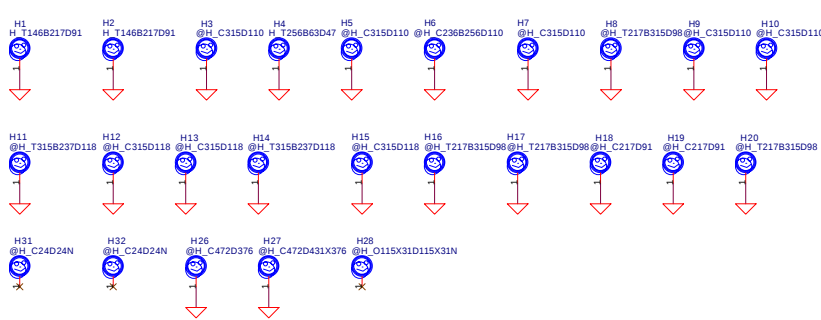
Power Good

LA-2791

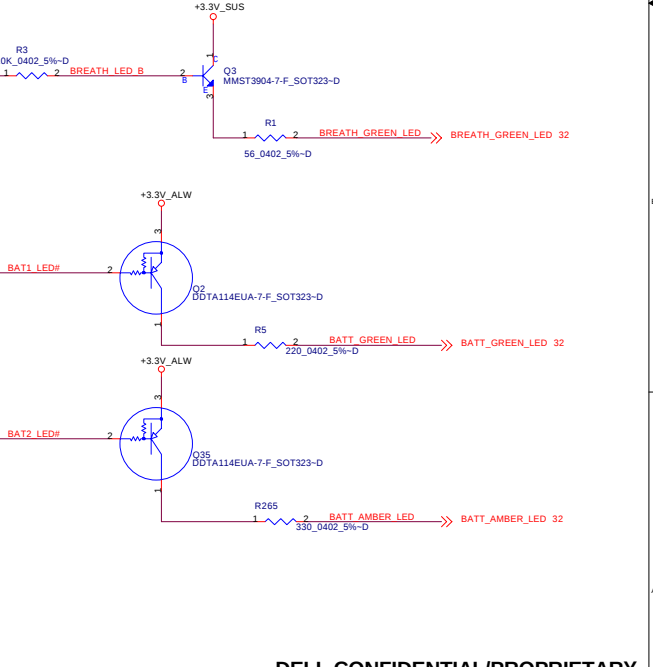
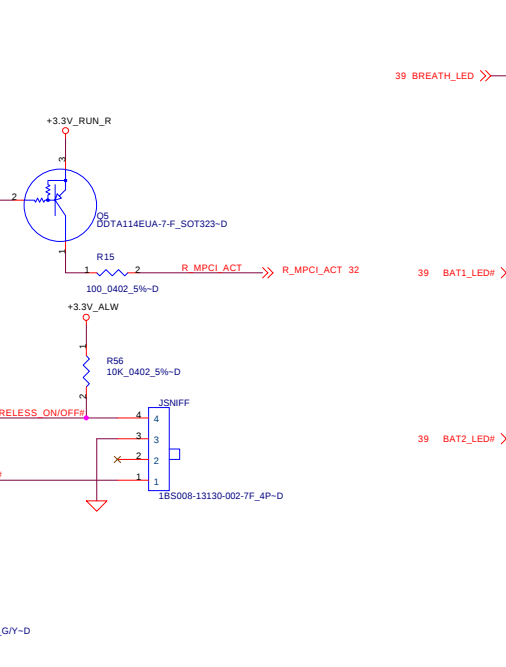
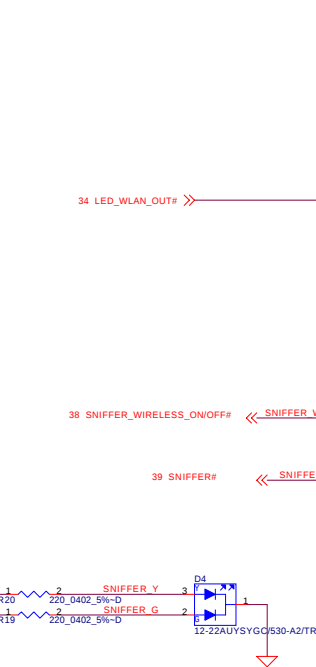
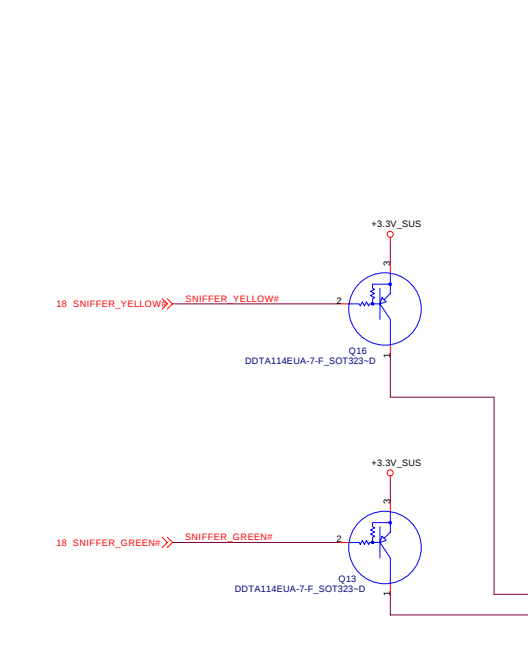
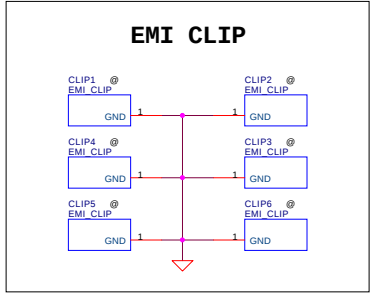
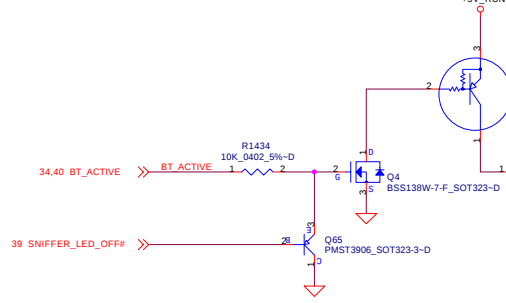
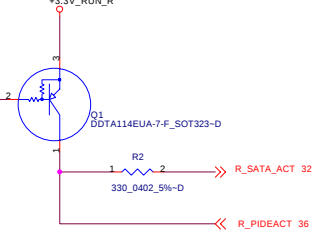
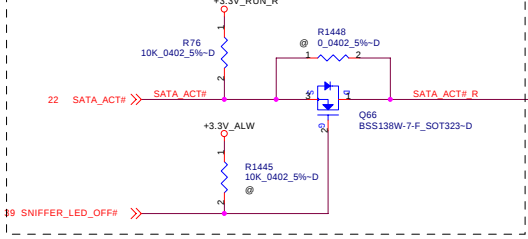
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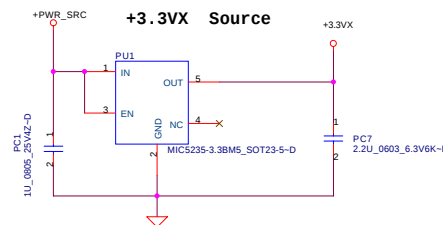
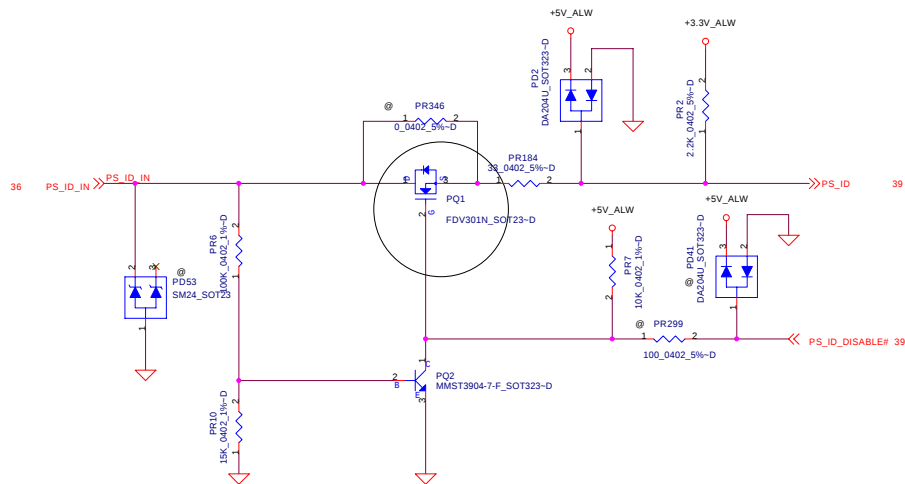




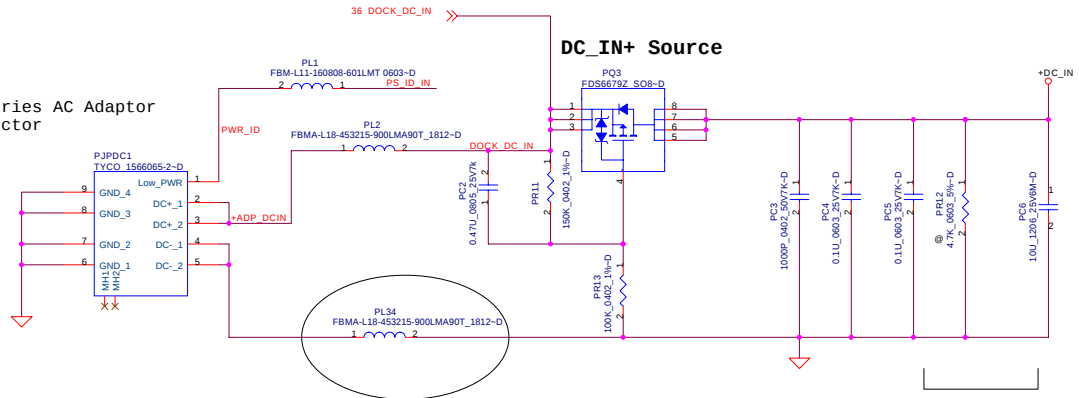
Disable HDD LED



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Z-series AC Adaptor
Connctor



THESE CAPS MUST BE
NEXT TO JCHG

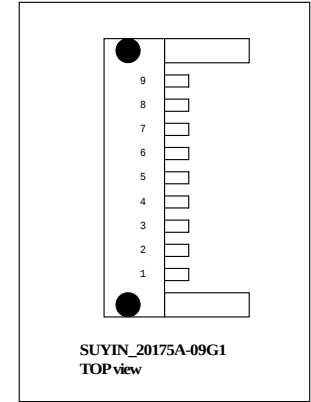
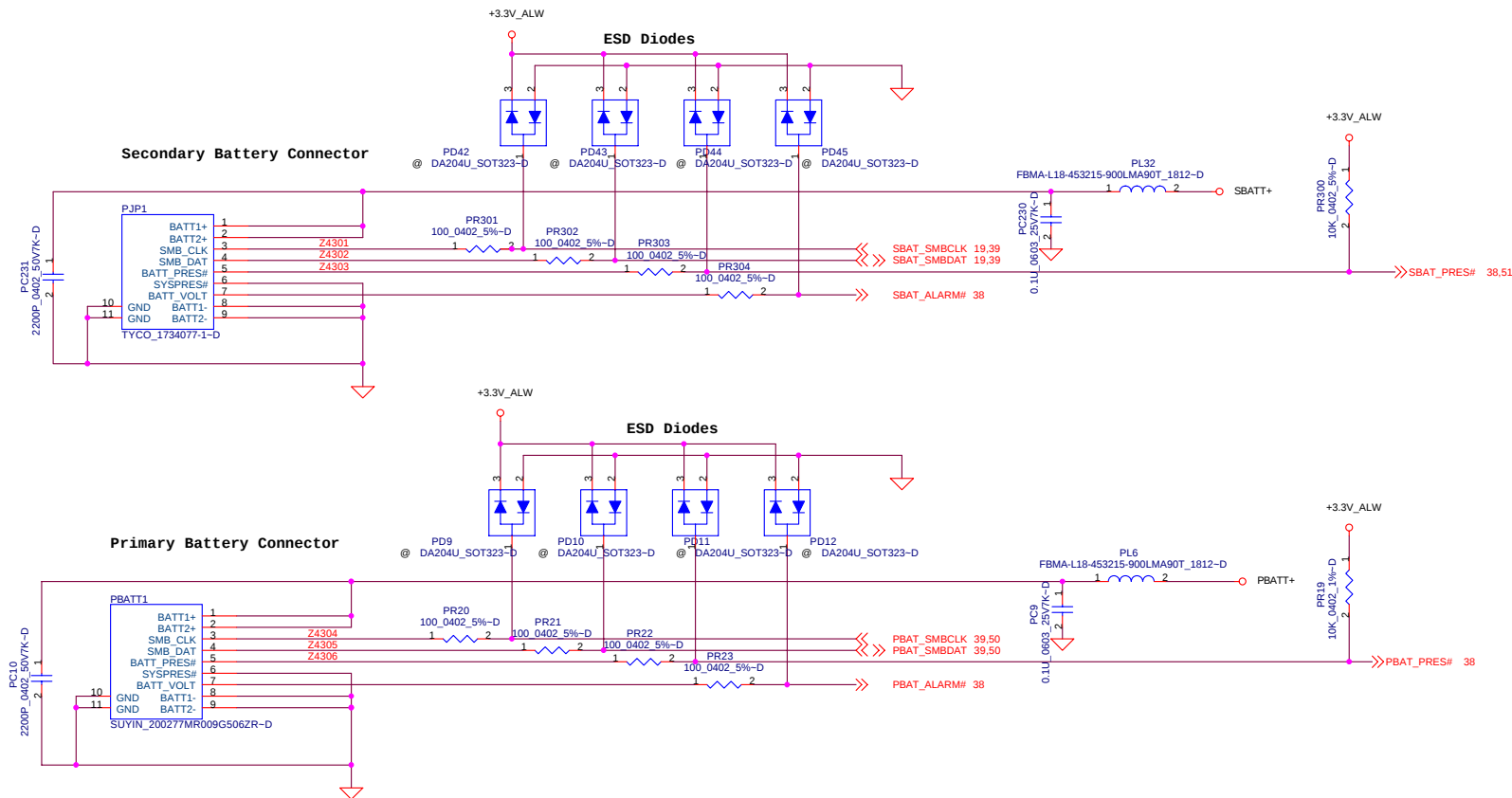
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+DCIN

Size Document Number
LA-2792
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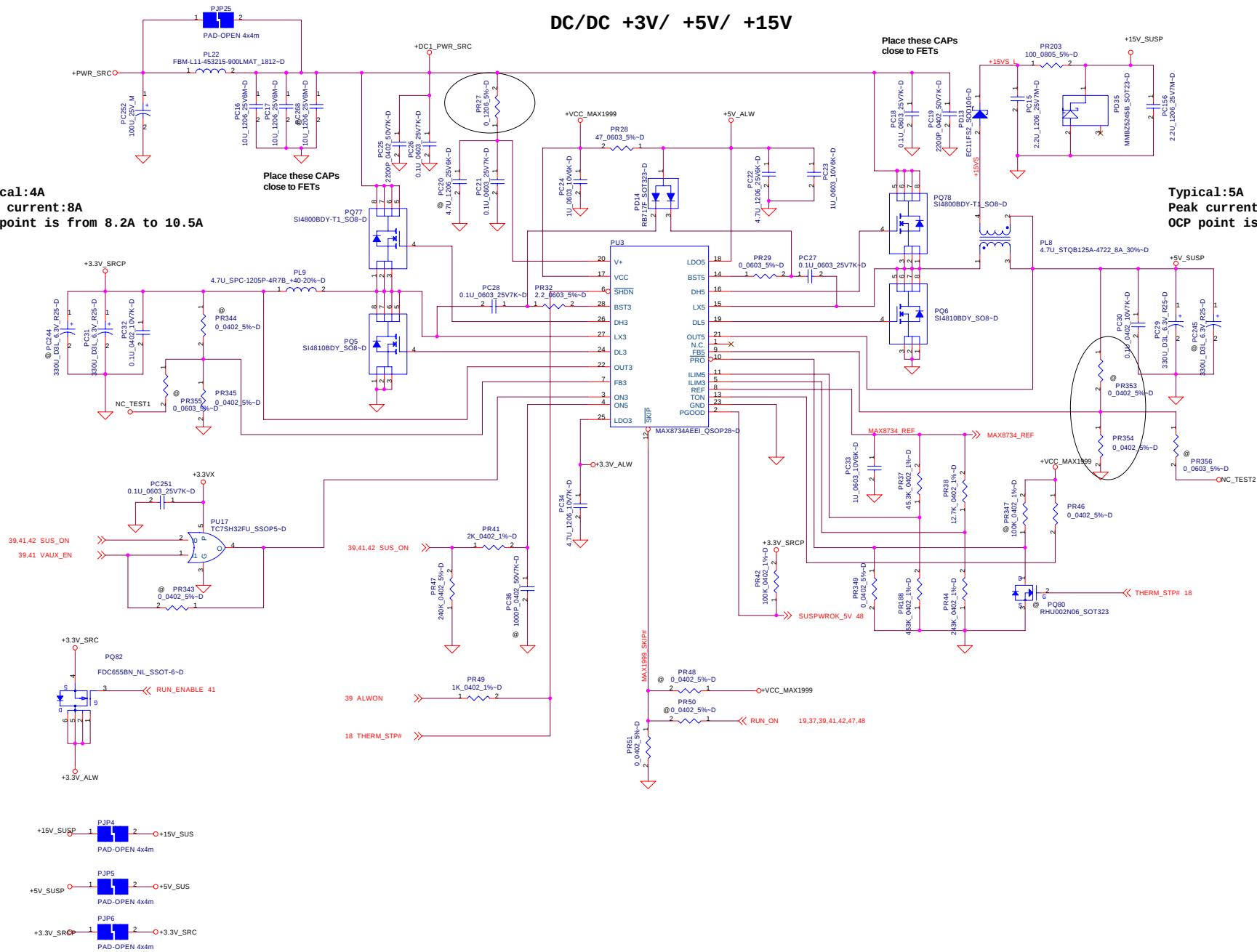


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Compal Electronics, Inc.			
Title Battery Conn.			
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DC/DC +3V/ +5V/ +15V

Typical:4A
Peak current:8A
OCP point is from 8.2A to 10.5A

Typical:5A
Peak current:7A
OCP point is from 8A to 11.2A



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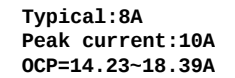
+3.3V/+5V/+15V

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+1.5VRUNP / +VCCP_1P05VP



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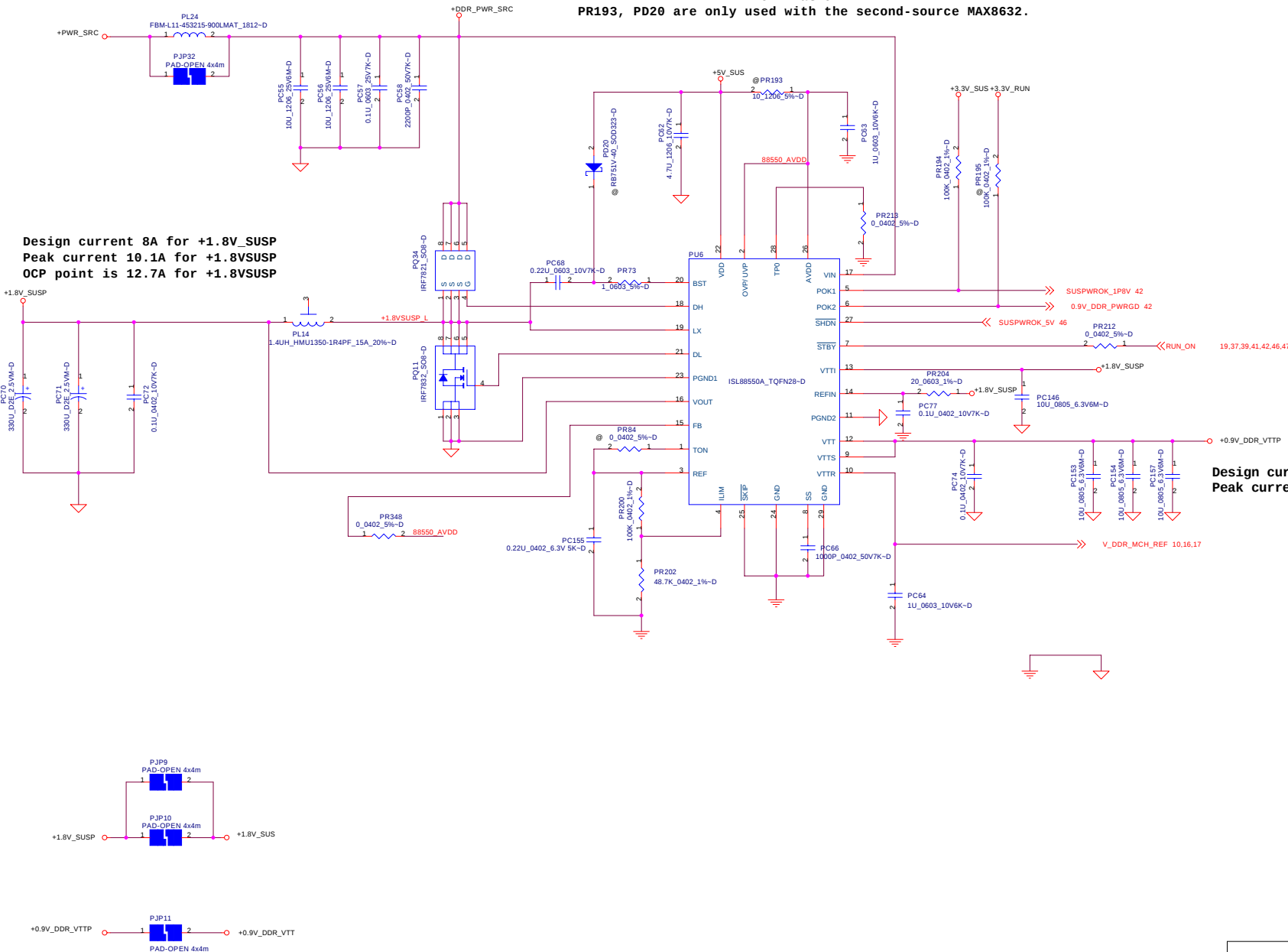
+1.5VSUSP /+VCCP_1P05VP

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+1.8VSUSP/ +0.9V_DDR_VTT **DDR2 Termination** **PR193, PD20 are only used with the second-source MAX8632.**

Design current 8A for +1.8V_SUSP
 Peak current 10.1A for +1.8VSUSP
 OCP point is 12.7A for +1.8VSUSP

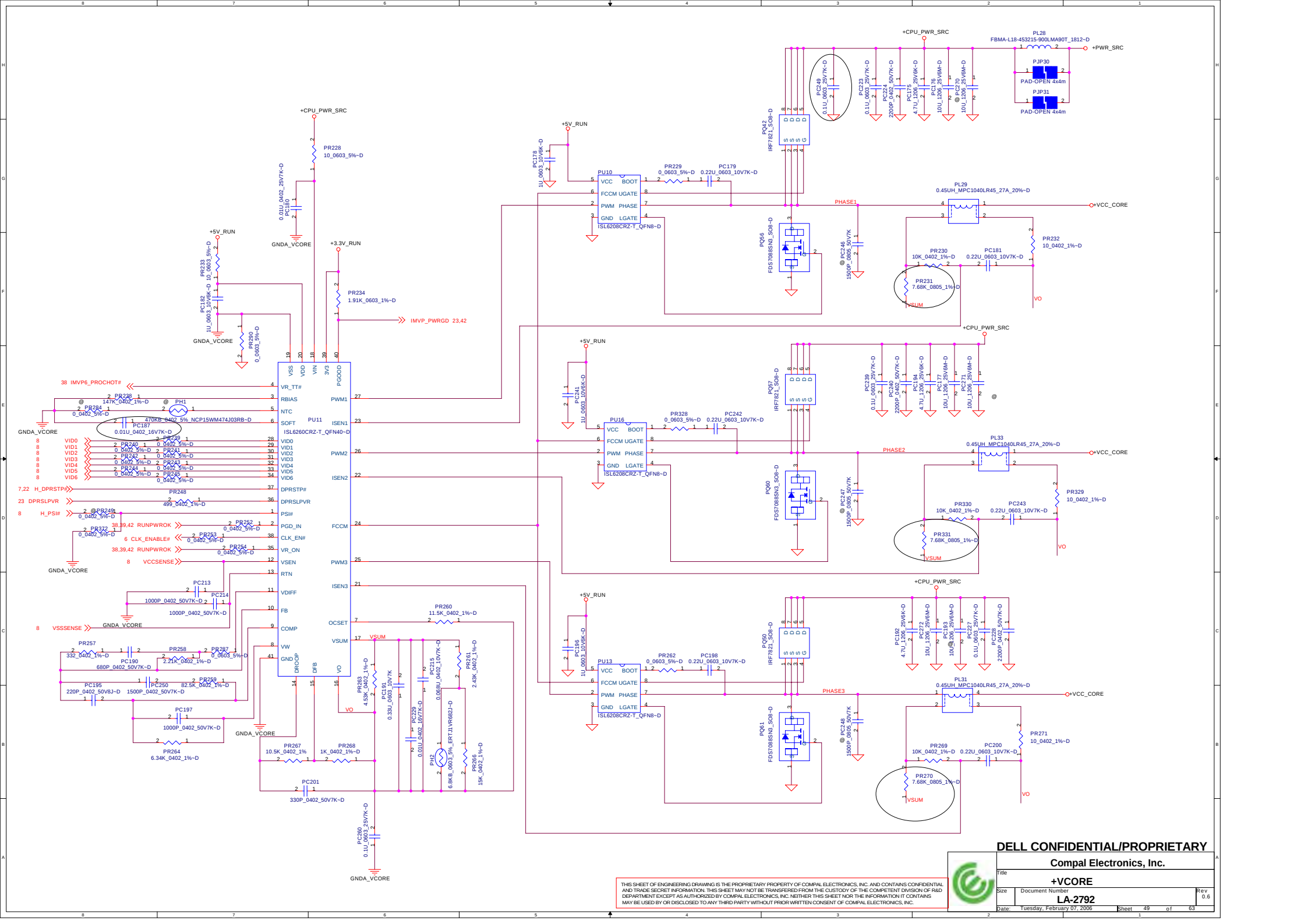
Design current 1.05A for +0.9V_DDR_VTTP
 Peak current 1.5A for +0.9V_DDR_VTTP



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Title		
+1.8VSUSP/ +0.9V_DDR_VT		
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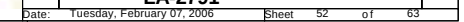
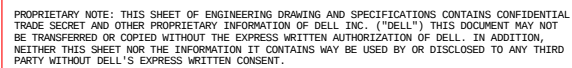
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	31	H/W	05/27	Roger	Smart card pin definition not match the cage pin define	Change JSC pin connection, pin1 connect to GND, pin2 connect to SC_DET# ~ pin10 connect to +SC_PWR	0.2
2	12, 36	H/W	05/27	Roger	Fix TV out issue	Depop R23, R24, R25. And add R1790, R1791, R1792 75 ohms	0.2
3	40	H/W	05/27	Roger	Remove power switch to save placement spacing	Remove SW1. Reseve R1793 pad for power switch	0.2
4	20	H/W	05/27	Roger	Docking CRT HSYNC, VSYNC connect to the out put side of buffer	DOCK_HSYNC connect from U190 pin4 to docking connector pin 209, DOCK_VSYNC connect from U191 pin4 to docking connector pin 210	0.2
5	32	H/W	05/27	Roger	Improve RJ45 center tap driving	Connect +2.5VLAN to J10 pin 14 for RJ45 center tap	0.2
6	39	H/W	05/27	Roger	SPI ROM pass through mode connect error	Change FDATAIN to ICHO_FDATAIN and connect from U216 pin 106 to U213 pin5. Chagne FDATAOUT to ICHI_FDATAOUT and connect from U216 pin 108 to R1788 pin1	0.2
7	39	H/W	05/27	Roger	Flash Recovery strapping issue	Change R474, R475 from 100K to 10K	0.2
8	ALL	H/W	05/30	Brike	To fix MEC5004 VCC1 power lading	Change net from +3VALW to +3VSRC	0.2
9	43	H/W	05/30	Brike	None	Delete H21 and change H4 footprint from H_C176D122to H_C176D102	0.2
10	39	H/W	06/01	Will	For delay MEC5004 internal 1.8V reg.	Modified C1769 from 4.7UF to 22UF.	0.2
11	23	H/W	06/01	Will	To improve rise time of serial D0 from SPI ROM.	Modified R389 from 10K to 1K..	0.2
12	41	H/W	06/01	Will	None	Add pullup to HDDC_EN# and MODC_EN#.	0.2
13	36	H/W	06/01	Will	Fix Docking TV out issue.	Modified R1790, R1791, R1792 from 75 ohms to 1500hm.	0.2
14	39	H/W	06/01	Will	None	Change power on SPI ROM (pins 3 and 8) from +3VALW to +3VSUS.	0.2
15	38	H/W	06/01	Will	For GPIO control.	Use ECE5018 GPIOC2 (pin 67), pin name MDC_RST_DIS#. Reserve this pin for MDC disable circuit.	0.2
16	12	H/W	06/01	Lester	None	Remove R34, R242, R37, R247, Q7, and Q33 to connect LDDC_CLK, LDDC_DATA directly to LVDS connector.	0.2
17	13	H/W	06/01	Lester	Intel Checklist recommends a 1 nH ferrite which calculates to 200 ohm.	Change L34 to BLM18PG181SN1_0603.	0.2
18	06	H/W	06/01	Lester	Add resistor for cystal drive current limiting	Add R32 0 ohm resistor	0.2
19	39	H/W	06/01	Will	Correct SPI connection for SMSC recomment	ICH7M.P5 connect to MEC 5004.107, MEC5004.108 connect to SPI ROM.5. ICH7M.P2 connect to MEC 5004.105, MEC5004.106 connect to SPI ROM.2	0.2
20	38	H/W	06/02	Roger	SMSC recomment add VBUS_DET pull up resistor	Add R1440 100K for LAN_TPM_EN# (VBUS_DET)	0.2
21	33	H/W	06/02	Roger	Add MDC disable circuit	Add R1441, R1442, R1443, Q64. ECE5018 pin 67 program MDC_RST_DIS#	0.2
22	34	H/W	06/06	Roger	None	Change U8 NNCD6.8RL-A to D5 NNCD5.6LG	0.2
23	3	H/W	06/06	Roger	None	Fixed USB table	0.2
24	3	H/W	06/13	Roger	None	Add PJP22, PJP24 for +5VMOD and +5VHDD. Delete R506	0.3

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25	13	H/W	06/14	Roger	Follow Intel CRB	D14 pin2 connect to +VCCP, pin1 connect to R320 pin1, R320 pin2 connect to +2.5VRUN. D18 pin2 connect to +1.5VRUN, pin2 connect to R12 pin1, R12 pin2 connect to +3VRUN_R	0.3
26	27	H/W	06/14	Roger	U10 (STAC9200) pin21 (GPIO0) is analog power plane	Change R156 pull up from +3VSUS to +VDDA	0.3
27	7	H/W	06/14	Roger	Change ITP debug to XDP debug definition for Yonah CPU	Change R387, R417, R391, R436, R416, R415 to 56 ohms. Add R33 56 ohms. Change R424 to 1K ohms.	0.3
28	39	H/W	06/14	Roger	For easier flash EC code	Add short pad and change R475 to 1K ohms	0.3
29	40	H/W	06/14	Roger	For easier power switch	Change R1793 to a pad like CMOS pad	0.3
30	34	H/W	06/14	Roger	ME change mini card stand off to Latch	Remove H22,H23,H24,H25. Add JCLIP1,JCLIP2	0.3
31	42	H/W	06/14	Roger	EMI request add caps for the splite power plane that PCI bus routed	Add C1806,C1807,C1808,C1809,C1810,C1811	0.3
32	41	H/W	06/16	Roger	Reserve discharg circuit for +5VRUN,+3VRUN,+1.8VRUN,+1.5VRUN,+0.9V_DDR_VTT,+2.5VRUN power rails	Add R1793,R1794,R1795,R1796,R1797,R1798,Q87,Q88,Q89,Q90,Q91,Q92	0.3
33	28	H/W	06/21	Gautam	Reserve ST M45PE20 for LOM EEPROM	Add U3 (ST M45PE20) co-layout with U188 (AT45BCM021B)	0.3
34	42	H/W	06/23	Gary	EMI request add caps for the splite power plane that PCI bus routed	Add C1812-C1814 0.047uF 0402. Change C1810-C1813 from 0603 to 0402 package	0.3
35	38	H/W	06/23	Roger	+3VRUN leakage at AC mode in S5	Change R1362 pull up from +3VSRC to +3VRUN	0.3
36	All	H/W	06/24	Roger	Follow Dell USB assignment recommendation	Update USB table, block diagram and connection	0.3
37	39	H/W	06/24	Will	4.7uF cap for VR_Cap pin of REV B 5504	Change C1769 for 22uF 0805 size to 4.7uF 0603 size	0.3
38	All	H/W	06/24	Joey	Change +3V/+5V design to follow Dell recommendation	Change +3VSRC to +3VALW except for LOM	0.3
39	28	H/W	06/24	Gautam	IEEE testing the voltage level are closer to the higher end of IEEE range	Change R1364 from 1.15K to 1.18K 0402 1%	0.3
40	7	H/W	06/24	Lester	Required by Intel for B0 Yonah.	Add R1378 (51_0603_1%) for TEST2 pulldown	0.3
41	39	H/W	06/24	Lester	Required by Intel for B0 Yonah.	Populate R1752 and add note "No stuff when doing flash recovery"	0.3
42	33	H/W	06/28	Rossana	MDC signal by pass caps not require	Delete C93, C82, C73	0.3
43	31, 40	H/W	06/28	Rossana	Reseved USB port of 0277C6 for Biometrics reader	Change JTPAD from 10 pins to 20 pins. Add USB_BI0+/- on U1 pin18,19 connect to JTPAD pin9,11	0.3
44	30	H/W	06/28	Rossana	Request by Dell	Remove C1783, C1784	0.3
45	34	H/W	06/28	Rossana	Request by Dell	Remove L18, R149, and R144 - direct connect USB to Wireless LAN card	0.3
46	34	H/W	06/28	Rossana	Request by Dell	Add R1603 connect to JMINI2 pin46, outgoing signal BT_ACTIVE	0.3
47	34	H/W	06/28	Rossana	Gerber Gate List issue	Add series 0-ohms R1609, R1610 for pins 3 and 5 of JMINI2	0.3

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48	34	H/W	06/28	Rossana	Gerber Gate List issue	Change C159 and C1785 from 10uF to 0.1uF	0.3
49	34	H/W	06/28	Rossana	Gerber Gate List issue	Add T1 test point for JMINI1 pin 42	0.3
50	36	H/W	06/28	Rossana	Gerber Gate List issue	Add C1817~1820 for U180,U178,U179,U177	0.3
51	39	H/W	06/28	Rossana	Gerber Gate List issue	Change R30 pull up from +3VSRC to +3VALW	0.3
52	43	H/W	06/28	Rossana	Change sniffer switch type, the active direction swap	WIRELESS_ON/OFF# connection from pin1 to pin 4 of JSNIFF, pin3 connect to GND, pin2 NC, pin 1 connect to SNIFFER#	0.3
53	36	H/W	06/28	Rossana	Gerber Gate List issue	Add C1821 1000pF for +DOCK_PWR_SRC, add C1827 1000pF for DOCK_DC_IN	0.3
54	35	H/W	06/28	Rossana	Gerber Gate List issue	Add C1822 0.1uF_0402 and C1823,C1824 .47uF_0402 for QBUF power	0.3
55	26, 27	H/W	06/28	Rossana	Gerber Gate List issue	Follow Dell "Travis_Audio_0628" reference circuit design	0.3
56	39	H/W	06/29	Scott	Gerber Gate List issue	Change L4 form MURATA BLM11A121S to BLM18PG181SN1	0.3
57	24	H/W	06/30	Scott	Gerber Gate List issue	Remove C375, C37 for ICH_V5REF_RUN, remove C420 for ICH_V5REF_SUS	0.3
58	24	H/W	06/30	Scott	Gerber Gate List issue	Add R37 0.5 ohm 0603 resistor connect to L42 pin1	0.3
59	24	H/W	06/30	Scott	Gerber Gate List issue	Populate C347 and C442	0.3
60	24	H/W	06/30	Scott	Gerber Gate List issue	Change C450 for 220uF to 330uF poly cap	0.3
61	40	H/W	06/30	Roger	Match Dell JTPAD pinout definition	Match Dell JTPAD pinout definition, add C62, C63 for BIO power rail bypass	0.3
62	26, 27	H/W	06/30	Rossana	Gerber Gate List issue	R162 change from 8.2K to 2.2K, remove D33, D34, Change C1800, C1801 from 1uF to 2.2uF, change C534 from 0.1uF to 1uF, del C533.	0.3
63	26	H/W	06/30	Rossana	Gerber Gate List issue	HP_NB_SENSE move from GPIO2 to GPIO0 of U10, add series resistor 0 ohm for this signal	0.3
64	7	H/W	07/07	Roger	Support A1 Yanah CPU	De-pop R513, R514 for A1 yanah CPU	0.3
65	7	H/W	08/01	Roger	Gerber Gate List issue item 6	Change Change R417 to 150 ohm, R415 to 51 ohm, R387 to 39.2 ohm, R436 to 27.4 ohm, R391 to 680 ohm, R424 to 22.6 ohm	0.4
66	38	H/W	08/01	Roger	Gerber Gate List issue item 8	Change R110 from 68 ohm to 75 ohm for H_PROCHOT# pull up	0.4
67	43	H/W	08/01	Roger	Gerber Gate List issue item 9	Change the voltage rail on sniffer LED pull-ups (at Q13 and Q16) from +3VALW to +3VSUS	0.4
68	7	H/W	08/01	Roger	None	Remove unnecessary capacitor C1805	0.4
69	40	H/W	08/01	Roger	Hall switch design on touch pad moudle	Depop U46 and C54	0.4
70	38	H/W	08/01	Roger	Gerber Gate List issue item 19	Move NB_MUTE from U215 pin 107 to pin73	0.4
71	16, 17	H/W	08/01	Roger	Gerber Gate List issue item 20, 21	Remove R178, pop R177	0.4
72	10, 23	H/W	08/01	Roger	Gerber Gate List issue item 22, 23	Depop R253, populate R1799	0.4

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73	42	H/W	08/02	Roger	Gerber Gate List issue item3	Connect 2.5V_RUN_PWRGD net to LD0_POK pin. Add depop R49	0.4
74	18	H/W	08/02	Roger	Gerber Gate List issue item11	Add R1800 31.6K ohm resistor for Vmargin circuit.	0.4
75	23	H/W	08/02	Roger	Gerber Gate List issue item5	Change R389 from 1K to 10K	0.4
76	33, 40	H/W	08/04	Steven	Combine the BT and TP in 30 PIN connector.	Delete JBT and move components to JTAP.	0.4
77	42	H/W	08/04	Steven	Gerber Gate List issue item3	Add Depop resistor R3019.	0.4
78	22, 23	H/W	08/04	Steven	For intel NAPA platform check list 1.5 request.	Chnage R425 from 330hm pull-down to 8.2Kohm pull-up. And add pull-up resistor R3020 in SIO_RCIN#.	0.4
79	19	H/W	08/08	Roger	Follow Intel CRB circuit	Pull up LDDC_CLK, LDDC_DATA to +3VRUN_R by R73, R74	0.4
80	16	H/W	08/09	Roger	V_DDR_MCH_REF discharge issue	Add R51 (100K_0402) connect to V_DDR_MCH_REF	0.4
81	23	H/W	08/09	Roger	Leakage issue when system into S3	Change SIO_EXT_SMI#, SIO_EXT_SCI# pull up to +3VSUS	0.4
82	36	H/W	08/09	Roger	Refer Dell docking reference circuit	Remove R1320, R1319	0.4
83	12	H/W	08/09	Roger	Gerber Gate List issue item 28	Depop R357	0.4
84	28	H/W	08/10	Roger	Gerber Gate List issue item 30	Add R53 4.7K resistor for LOM_S0 pull down	0.4
85	28	H/W	08/10	Roger	Gerber Gate List issue item 33	Connect BCM5752 pin C4 to ECE5018 pin75 net name LOM_CABLE_DETECT. Series no stuff resistor R55	0.4
86	38	H/W	08/10	Roger	Gerber Gate List issue item 39	R1171 change pull up from +3VRUN to +3VSUS	0.4
87	38	H/W	08/10	Roger	Gerber Gate List issue item 42	Add a 4.7uF cap for ECE5018 VDDA33 coupling	0.4
88	39	H/W	08/10	Roger	Gerber Gate List issue item 43	Add a 0 Ohm 0402 resistor R62 in series with the RTC_CELL and EMC5004 pin 121	0.4
89	7	H/W	08/10	Roger	Follow Intel CRB circuit	R513, R514 pull up to +VCCP	0.4
90	39	H/W	08/10	Roger	Gerber Gate List issue item 46	Add resistor R63 (0_0402_5%) between the BIA_PWM signal and MEC5004 pin 73	0.4
91	39	H/W	08/10	Roger	Gerber Gate List issue item 47	Change ITP_DBRESET# connection from EMC5004 pin 55 to pin96	0.4
92	22	H/W	08/10	Roger	Gerber Gate List issue item 50	Add no stuff C69 (0.1U_0402_16V4Z) between THRMTRIP_ICH# and GND	0.4
93	41	H/W	08/10	Roger	None	Change R1795 pin 1 connect from +1.8VRUN to +1.8VSUS for discharge	0.4
94	23	H/W	08/10	Roger	Gerber Gate List issue item 51	Move pull-up R388 to pin 1 side of R1787	0.4
95	6	H/W	08/10	Roger	Gerber Gate List issue item 29	Add C70 (0.1U_0402_16V4Z) for +CK_VDD_MAIN decoupling. Remove R290, R343, R329 to save spacing	0.4
96	7	H/W	08/11	Roger	Gerber Gate List issue item 68	Remove R513 and R514 platform no longer use Yonah A00	0.4
97	42	H/W	08/11	Roger	Gerber Gate List issue item 65	Populate 0ohm for R49, R313, R319, R334	0.4

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98	41	H/W	08/11	Roger	Gerber Gate List issue item 67	Change R494 to 20K	0.4
99	7	H/W	08/11	Roger	Gerber Gate List issue item 69	Add no stuff C71 and C72 for +VCCP of J1TP	0.4
100	7	H/W	08/11	Roger	Gerber Gate List issue item 70	Change R416 and R33 from 56 ohm to 54.9 ohm	0.4
101	12	H/W	08/11	Roger	Gerber Gate List issue item 72	Delete R333 to follow reference schematics	0.4
102	28	H/W	08/11	Roger	Gerber Gate List issue item 34	Add R68 (20K_0402_5%) and R70 (39K_0402_1%) for LAN_LOW_PWR voltage divider connect to pin K5	0.4
103	26, 27, 38	H/W	08/12	Roger	Gerber Gate List issue item 75	DOCK_HP_MUTE# for GPIO2 of codec connect to ECE5018 pin 81. EAPD for GPIO3 of codec connect to additional Q11 gate	0.4
104	38	H/W	08/15	Roger	Gerber Gate List issue item 38	Chnge SYS_PME# pull up from +3VRUN to +3VALW. Add no stuff R71 in series	0.4
105	38	H/W	08/15	Roger	Gerber Gate List issue item 41	Remove HP_NB_SENSE from ECE5018 pin 106 to pin 82	0.4
106	23	H/W	08/15	Roger	Gerber Gate List issue item 188,189	Depop R428,Change value of R75 to 10k ohms	0.4
107	40	H/W	08/16	Roger	Gerber Gate List issue item 48	Change R1750 and R1751 to L1 and L2	0.4
108	28	H/W	08/16	Roger	Gerber Gate List issue item 213	Depop U188, R1366 and populate U3, R1267 for ST AT45BCM021B	0.4
109	39	H/W	08/16	Roger	Gerber Gate List issue item 217	Remove R166. Move R1635 for AFT_INT# move to page 39	0.4
110	39	H/W	08/16	Roger	Add pull up for open drain out put	Add R93 pull up to +3VALW for BAT_SEL#	0.4
110	38	H/W	08/16	Roger	Mute internal speaker when docking aduio jack plug in	Add pull down resistor for DOCK_HP_MUTE#	0.4
111	06	H/W	09/07	Roger	Follow Dell CoE schematics	Change C329, C333 from 33pF to 27pF	0.5
112	43	H/W	09/14	Roger	Blue tooth LED too bright	Change R8 from 3.3K to 1K ohms	0.4
113	41	H/W	09/14	Roger	+1.8VSUS discharge low issue	Populate Q89, R1795	0.4
114	39	H/W	09/14	Roger	LID_CL# can't assert low	Change R482 from 100K to 1M ohms	0.4
115	40	H/W	10/04	Brike	Delete U46, C54, SW1	None	0.5
116	34, 39	H/W	10/13	Brike	Connect 8051TX to WWAN Pin 19 and Connect 8051RX to WWAN Pin 42.	Modified.	0.5
117	22	H/W	10/15	Brike	Gerber Gate List issue item 60	Add R97 0-ohm tuning resistor between R36 pin2 and X1 pin1	0.5
118	41	H/W	10/17	Brike	Gerber Gate List issue item 66	Change R1795 to a 30 ohm 0603 resistor	0.5
119	39	H/W	10/18	Brike	MEC5004 per SMSC recommendations to add circuit for improving POR issue.	Add de-pop components R101, R110, R112, R114, R117, Q20, Q19, C54, D2002. And change C1769 to 22U.	0.5
120	38	H/W	10/18	Brike	change board ID to X02	Pop R95, R419 and De-pop R108, R405.	0.5
121	40	H/W	10/18	Brike	Gerber Gate List issue item 77. Add 10pF cap between GND and pin2 of L1/L2.	Add C66, C73.	0.5

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122	23	H/W	10/18	Brike	Gerber Gate List issue item 78. Pull up LAMP_STAT# to +3VRUN	Change R75 pull-up to +3.3V_RUN.	0.5
123	6	H/W	10/19	Brike	Gerber Gate List issue item 72. Inductor design follow M07 design on L40,L32 (Size:0805).	Change L32, L40 from 0603 to 0805.	0.5
124	23	H/W	10/19	Brike	Gerber Gate List issue item 79. SATA_DET# is pull up to +3.3V_SUS.	Change R784 pull up to +3.3V_SUS.	0.5
125	18	H/W	10/19	Brike	Gerber Gate List issue item 74.Make R1643 prior to bypass caps at +3VRUN.	Change R1643 prior to bypass caps " C152 and C517 " at +3VRUN power rail .	0.5
126	9	H/W	10/20	Brike	Gerber Gate List issue item 84	Change the 32 high frequency decoupling caps, 0805 X5R, from 22uF to 10uF. Depop C354 and C618.Change C352, C496, C497, and C365 from 330uF/7mOhm to 330uF/6m0hm SP caps.	0.5
127	34	H/W	10/20	Brike	Gerber Gate List issue item 82	Connect PLTRST# instead of PLTRST_DELAY# to WLAN and WWAN connectors.	0.5
128	23	H/W	10/20	Brike	IMVP_PWRGD glitch issue	Add C79 0.1uF cap on IMVP_PWRGD to filter the glitch	0.5
129	28	H/W	10/21	Brike	Q68 surge current	Add R102 (0603) and C80 0.1uF cap Q68 pin1 for reduce surge current	0.5
130	40, 43	H/W	10/21	Brike	BT & HDD LED is on when the SNIFFER is turned on.	Added a circuit (FET and Resistors) to keep the BT LED & HDD LED off when the SNIFFER is turned on	0.5
131	38	H/W	10/21	Brike	Gerber Gate List issue item 81	Depop R1440	0.5
132	34	H/W	10/22	Brike	Add Intel WoWLAN Support Circuit	Add pop components Q21 and R101, and un-pop componet R24.	0.5
133	18	H/W	10/24	Brike	Gerber Gate List issue item 89. Change OTP trip temperature to 88 deg C.	Change R249 to 332K and R262 to 118K.	0.5
134	39	H/W	10/24	Brike	Gerber Gate List issue item 90. Pop SMSC workround circuit for 11/7 build.	Pop R101, R110, R112, R114, R117, Q20, Q19, C54, D2002.	0.5
135	39	H/W	10/24	Brike	Gerber Gate List issue item 91. Add a 0 ohm pulldown resistor on TEST_PIN.	Add R122 00hm resister.	0.5
136	43	H/W	10/24	Brike	Gerber Gate List issue item 111. Remove one of the pull-ups on SNIFFER_LED_OFF#.	Remove Pull up resister R1447.	0.5
137	43	H/W	10/24	Brike	Gerber Gate List issue item 110.	More R76 to pin 1 of Q66 and populate it.	0.5
138	34	H/W	10/24	Brike	Add Intel WoWLAN Support Circuit	Replace Q21 and R101 to D2003	0.5
139	20	H/W	10/24	Brike	Gerber Gate List issue item 108. Add 39 ohm resistors at output of U190 and U191.	Add resister R102 and R123.	0.5
140	18	H/W	10/24	Brike	Gerber Gate List issue item 92. Add thermistor circuit to VCP2 (pin 40) of EMC4000. Please route to 5V_CAL_SIO2# (pin 80, GPIO B4 on ECE5018).	Add thermistor circuit R479, R480, R481, C79, Q21.	0.5
141	43	H/W	10/24	Brike	Gerber Gate List issue item 114. Modified SATA_ACT# LED sniffer disable circuit.	Modified the circuit and Add and D2004. Chnage Q1 to 3904, R1449/1448 change to 10K and 1K.	0.5
142	40	H/W	10/25	Brike	Gerber Gate List issue item 119. For fix the IMVP_PWRGOOD glitch issue.	Change delay circuit R1764 from 200K0hm, C1788 to 470PF to +1.8V_run and +3V_run.	0.5

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143	38	H/W	10/25	Brike	Gerber Gate List issue item 104. Modified the SATA_ACT# circuit.	Modified the circuit Pull up R1449 to +5V_SUS and R1445 to +5V_run. R2 move to Q1 pin 3, SNIFFER_LED change to GPIO82.	0.5
144	20	H/W	10/25	Brike	Gerber Gate List issue item 116. Add diode HSYNC and VSYNC buffers.	Add D2005 (RB751) in U190, U191 Pin 5.	0.5
145	40, 43	H/W	10/26	Brike	Modified HDD/BT disable circuit.	Move 40 BT Disable circuit to 43.	0.5
146	19	H/W	10/26	Brike	Add level shit circuit for BIA_PWM.	Delete R520 and Add U8.	0.5
147	23	H/W	11/03	Brike	the delay circuit on +3.3V should get rid of the glitch	Depop C82.	0.5
148	41	H/W	11/03	Brike	Populate the HDD power switch circuit	Pop Q51, R507, Q50 and Depop PJP24.	0.5
149	31	H/W	11/03	Brike	For passing EMVCo test.	Change R1424 from 220 to 3300hm.	0.5
150	43	H/W	11/03	Brike	SNIFFER_LED_OFF# is a push/pull signal.	De-pop R1445.	0.5
151	27	H/W	11/03	Brike	To improve audio quality	Change C199 to 0.022uF and pop R164, depop R170.	0.5
152	39	H/W	11/11	Brike	Change SMSC MEC5004 from version C to D.	Change U216 P/N to D version. Depop R117, R114, R110, R101, R104, D2002, Q19, Q20, C54. And chnage C1769 value from 22UF to 4.7UF.	0.5
153	39	H/W	11/11	Brike	Change DOCK_SMB_CLK and DOCK_SMB_DAT for consistent with other M07 platforms.	Change R99 and R100 resister from 100K to 8.2K Ohm. And R1618 change to 10K0hm.	0.5
154	43	H/W	11/11	Brike	For improve LED brightness issue.	Change R2 value from 560hm to 3300hm. And modified R15 from 1500hm to 1000hm.	0.5
155	28	H/W	11/12	Brike	For Q68 broken issue. Modified R120 value for protect base pin.	ChangeR120 from 00hm to 2K0hm.	0.5
156	20	H/W	11/12	Brike	For Dell request change D32, D2005 to RB500.	Change D32 and D2005 from RB751 to RB500	0.5
157	27	H/W	11/12	Brike	For improve Audio THD+n performance.	Change C113, C114 and C146 from 1UF to 2.2U.	0.5
158	27	H/W	11/27	Brike	For adjust Audio gain to 15.6DB.	Pop R170, De-pop R164.	0.5
159	42	H/W	12/06	Brike	For improving SUSPWOK turn on issue.	Modified Q7 to 2N7002.	0.6
160	52	H/W	12/06	Brike	For solving DVI eye diagram issue.	Change C3030, C3025 from 1uF to 10uF; R3006 to 2200hm; R3015, R3016, R3017, R3018 to 1000hm.	0.6
161	23, 38	H/W	12/06	Brike	For solving HD warn boot parking sound issue.	Change HDDC_EN#, MODC_EN# from ICH7 to ECE5018 Pin 106, 107 (GPIOH2/3), and Depop R2148, R2149.	0.6
162	7	H/W	12/06	Brike	Add a De-pop resister for CPU test 1 PIN.	Add De-pop resister R1387.	0.6
163	39	H/W	12/07	Brike	Add an damping resister for improving SPI_CS# overshoot issue.	Add 470hm resister R127.	0.6
164	39	H/W	12/07	Brike	For solving SBAT_SMBDAT rising time over spec issue.	Change R444 to 4.7K0hm resister.	0.6
165	6	H/W	12/12	Brike	For Gerber Gating list item 14 Depop pullup resistor on ICH_CLKREQ#.	Depop resister R1761.	0.6
166	38	H/W	12/12	Brike	For Gerber Gating list item 17 Update board ID to A00	Pop R405, depop R419.	0.6
167	31	H/W	12/12	Brike	For Gerber Gating list item 11 add 47pF capacitors to the USB_BIO+/- pins to fix bio sensor ESD issue.	Add 2 capaciotr C83, C84 in USB_BIO+/-.	0.6

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168	41	H/W	12/14	Brike	For GPIOH[3:2] need, chnage pullup resister power plane to always.	Change pullup resister R2148, R2149 for +3.3V_SUS to +3.3V_ALW.	0.6
169	41	H/W	12/15	Brike	For Gerber Gating list item 18. Change pullup resister to 10K.	Change pullup resister R2148, R2149 for 100K to 10K0hm.	0.6
170	18	H/W	12/15	Brike	For Gerber Gating list item 1. Remove pullup resister from 2.5V_RUN_PWRGD.	Remove R116.	0.6
171	39	H/W	12/19	Brike	For Gerber Gating list item 21. Add 0 ohm series resistor to SPI_CS# at MEC5004.	Add series resister R143 at MEC5004 side.	0.6
172	31	H/W	12/19	Brike	For improving USB BIO sensor EMI issue.	Add Pop L5, and depop resister R128, R137.	0.6
173	40	H/W	12/20	Steven	For DELL EMI request for add a 0.1uF capacitor in JTPAD.	Add 0.1uF capacitor C85.	0.6
174	28	H/W	12/30	Steven	For Q68 damage issue change form BCP69 to MBT35200 as ZRS solution.	Use MBT35200 to replace Q68. Modified.	0.6
175	7	H/W	12/31	Brike	Intel Design Guide 1.0 to change H_RESET pull-up resister to 510hm.	Change resister R416 to 510hm.	0.6
176	39	H/W	01/04	Brike	For enable MEC5004 BIOS write protect function.	Pop R139 and de-pop R138.	0.6
177	27	H/W	01/07	Benson	For adjust Audio gain to 21.6 DB.	DePop R170, pop R164.	0.6
178	28	H/W	01/09	Brike	For Q68 issue to reserve soft start circuit.	Change R120 to 00hm, and depop C80.	0.6
179	20	H/W	01/20	Brike	For fixing issue with projector using long cable.	Change R102,R123 from 39 ohm to 0 ohm	0.6
180	19	H/W	01/20	Brike	For stronger the VGS driving in Battery Mode	Change R235 from 200K ohm to 100K ohm	0.6
181	6	H/W	01/20	Brike	The Drive Level too high	Change R32 from 0 ohm to 470 ohm	0.6
182	22	H/W	01/20	Brike	The Negative Resistance too low	Change X1 spec from CL=20pF to 6 pF and C38,C40 from 12pF to 2.2pF	0.6
183	38	H/W	01/20	Brike	The Frequency too high & Drive Level too high	Change Y1 spec from CL=20pF to 12pF and C1451,C1452 from 22P to 15P	0.6
184	31	H/W	01/20	Steven	None	Depop L5 ,pop R128,R137 33 ohm	0.6
185	39	H/W	02/07	Steven	For solving primary battery hand issue.	Change R447, R449 to 4.7K0Hm; R444, R131 to 2.2K0hm.	0.6

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1	46	PWR	06/01	Saha	M4 input current more than MAX8734 LD03 output 100mA	Delete PU17 SN74AHC1G32DCKR OR GATE(SA00732018L), PR49 1K_0402_1%(SD03410018L) Add PR350 0_0402_5%(SD02800008L) connect LD03 to ON3 PU18 74AHCT1G08GW AND GATE(SA00000L30L) PR352 1K_0402_1%(SD03410018L) PR351 0_0402_5%(SD02800008L)	0.2
2	46	PWR	06/01	Saha	MAX8734 LD0 soft start issue.	Delete PR27 4.7_1210_5%(SD000007E8L) Un-pop PC20 4.7U_1206_25V6K(SE093106M8L)	0.2
3	46	PWR	06/01	Saha	PWR_SRC noise issue	Un-pop PC252 100U_25V_M(SF10004M008)	0.2
4	44/45	PWR	06/01	Saha	+3VALW change to +3VSRC	Rename net +3VALW to +3VSRC	0.2
5	47	PWR	06/01	Saha	VCCP high/low side MOSFET change from IR to Infineon No-stuff PC207 and PC208	PQ38 change from IR7821(SB57821008L) to BS0072N03S(SB00000418L) PQ40 change from IR7832(SB57832008L) to BS0072N03S(SB00000418L) Un-pop PC207 and PC208 10U_0805_6.3V5K(SE093106M8L)	0.2
6	47	PWR	06/01	Saha	VCCP_1P05VP OCP issue(5A)	PR224 change from 124K_0402_1%(SD03412438L) to 60.4K_0402_1%(SD03460428L)	0.2
7	47/48	PWR	06/01	Saha	Choke height issue.(5.6mm change to 5.0mm)	PL14 and PL27 change from 1.4U_HMU1356-1R4_15.5A H5.6mm(SH04814AM8L) to 1.4U_HMU1350-1R4_15A H5.0mm(SH000004H8L)	0.2
8	44	PWR	06/01	Saha	PSID materiel change by Dell	PQ1 change from BSS138_SOT23(SB50138008L) to FDV301_SOT23(SB50301008L)	0.2
9	50	PWR	06/01	Saha	New version MAX8731 PIN1 define GND	Un-pop PR337 0_0402_5%(SD02800008L),Pop PR336 0_0402_5%(SD02800008L)	0.2
10	50	PWR	06/02	Saha	Add RC filter at pin 23 of MAX8731	Add PR360 1_0603_1%(SD014100B8L) PC253 220P_0402_50V7K(SE074221K8L)	0.2
11	46/48	PWR	06/02	Saha	Add support for Reliability voltage margining tests	Add PR356, PR355 and PR359 0_0603_5%(SD01300008L) PR353 and PR354 0_0402_5%(SD02800008L)	0.2
12	48	PWR	06/16	Saha	Change output capactior rating voltage from 6.3V to 2.5V	PC70 and PC71 change from 330U_D3L_6.3V_R25(SGA00000N8L) to 330U_D2E_2.5VM_R15(SGA19331D0L)	0.3
13	49	PWR	06/22	Saha	Change VCORE DPRSLPVR input resistor value	PR248 change from 0_0402_5%(SD02800008L) to 499_0402_1%(SD03449900L)	0.3
14	50	PWR	06/22	Saha	Add power limit schematic	Depop PR361 80.6K_0402_1%, PR362 200K_0402_1%, PR363 121K_0402_1%, PR364 3.01K_0402_1%, PR365 499K_0402_1%, PR366 100K_0402_1%, PR367 100K_0402_1%, PC254 0.01U_0402_25V8K, PC255 100P_0402_50V8K, PC256 100P_0402_50V8K, PC257 100P_0402_50V8K, PC258 0.01U_0402_25V8K, PC259 10P_0402_50J8K, PQ81 RHU002N06_SOT323, PU19 LM393DR_S08	0.3
15	46	PWR	06/29	Saha	Discreate 3VALW and 3VSRC.	Add PU17 SN74AHC1G32DCKR OR GATE(SA00732018L), PR49 1K_0402_1%(SD03410018L) PQ82 FDC655BN_NL(SB000004P8L) Delete PR352 1K_0402_1%(SD03410018L) PR351 0_0402_5%(SD02800008L) PR350 0_0402_5%(SD02800008L) PU18 74AHCT1G08GW AND GATE(SA00000L30L)	0.3

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16	46	PWR	06/29	Saha	Add V+ input Resistor	Add PR27 0_1206_5%(SD00100000L)	0.3
17	45/51	PWR	06/29	Saha	Battery conn. and battery selector +3VSRC change to +3VALW	Rename +3VSRC to +3VALW	0.3
18	47	PWR	06/29	Saha	ISL6227 Issue change 1.05V/1.5VHigh/Low side MOSFET change 1.05V choke adjust OCP and ISEN value	VCC Change from +5VRUN to +5VSUS. EN1 and EN2 change from RUNPWR0K to RUN_ON. PR221 change from 20K_04-2_1%(SD03420028L) to 19.6K_0402_1%(SD00000358L) PQ8 change from FDS6994S(SB56994008L) to FDS8880(SB000004U8L) Add PQ83 FDS6670AS(SB000004T8L) PQ38 change from BS0072N03S(SB00000418L) to FDS8880(SB000004U8L) PQ40 change from BS0072N03S(SB00000418L) to FDS6670AS(SB000004T8L) PL27 change from 1.4U_HMU1350(SH000004H8L) to 1.5U_SIL104(SH04215A08L) Add PC261 0.01U_0402(SE068103K8) Add PC262 and PC263 2200P_0402(SE074222K8L) PR219 change from 825_0402_1%(SD03482508L) to 1.43K_0402_1%(SD03414318L) PR220 change from 825_0402_1%(SD03482508L) to 2.1K_0402_1%(SD03421018L) PR223 change from 69.8K_0402_1%(SD03469828L) to 124K_0402_1%(SD03412438L) PR224 change from 60.4K_0402_1%(SD03460428L) to 124K_0402_1%(SD03412438L)	0.3
19	49	PWR	06/29	Saha	ISL6260 Issue	Delete PR338, PR339 and PR340 2.7_0603_5% Change PC246, PC247, PC248 to 1500P_0805-----Unpop Change PH1 from ERTJ1VR103J(SL20000020L) to NCP15WM474J03RB(SL20000098L) PR284 change from 15.8K_0402_1%(SD03415828L) to 0_0402_5%(SD02800008L) Add PC260 0.1U_0603(SE042104K8L)	0.3
20	50	PWR	06/29	Saha	Change +VCHGR output CAP from 1206 to 1210	PC113 and PC114 change from 10U_1206(SE142106M8L) to 10U_1210(SE056106K8L)	0.3
21	47	PWR	08/12	Saha	Add VSEN capacitor	Add PC265 and PC264 100P_0402_50V8K(SE071101K8L)	0.4
22	47	PWR	08/12	Saha	Delete PG00D pull high resistor	Delete PR283 100K_0402_1%(SD03410038L) De-pop PR195 100K_0402_1%(SD03410038L)	0.4
23	48	PWR	08/12	Saha	Delete reliability test resistor	Delete PR283 110K_0603_1%, PR359 0_0603_1%, and PR82 59.6K_0603_1%	0.4
24	49	PWR	08/12	Saha	Adjust VCORE load line	PR267 change from 7.87K_0402_1%(SD03478718L) to 9.09K_0402_1%(SD034909100) PR231, PR331, and PR270 change from 7.68K_0402_1%(SD00000238L) to 7.68K_0805_1%(SD00000B08L)	0.4
25	49	PWR	08/12	Saha	Delete H_PROCHOT# resistor	Delete PR235 0_0402_5%(SD02800008L)	0.4
26	50	PWR	10/17	Saha	Add RC filter in FBSA/B PIN	Add PR368 and PR369 100_0402_5%(SD02810008L) Add PC266 and PC267 0.01U_0603_50V7K(SE025103K8L) Un-pop PR371 and PR370 0_0402_5%	0.5
27	46	PWR	10/17	Saha	EMI request: change BST3 resestor	Change PR32 from 0_0603_5%(SD01300008L) to 2.2_0603_5%(SD013220B8L)	0.5
28	46	PWR	10/17	Saha	change 3V out put CAP height	change PC31 from 330U_6.3V_R25 H1.9(SGA00001C8L) to 330U_6.3V_R25 H2.8(SGA0000089L)	0.5

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29	50	PWR	10/17	Saha	Populate UL circuit	Populate PR361-PR367, PC254-259, PU19, PQ81. Change PR361 from 80.6k to 0. Change PR362 from 200k to 301k. Change PR363 from 121k to 59k. Change PR364 from 3.01k to 27.4k. Change PR365k from 499k to 4.32Meg.	0.5
30	49	PWR	10/20	Saha	Change VCC_CORE OCP, SOFT, and DPRSTP# value	PR260 change from 20K_0402_1%(SD03420028L) to 11.5K_0402_1%(SD03411520L) PC187 change from 0.022U_0402_16V7K(SE076223K8L) to 0.01U_0402_16V7K(SE076103K8L) Add PR372 0_0402_5%(SD02800008L) Delete PR246 0_0402_5%(SD02800008L) Un-pop PR249 0_0402_5%(SD02800008L)	0.5
31	48	PWR	10/20	Saha	Change PU6 BST resistor	PR73 change from 0_0603_5%(SD01300008L) to 1_0603_5%(SD013100B8L)	0.5
32	44	PWR	10/20	Saha	Change PQ2 from RUH002N06 to 3904	PQ2 change from RHU002N06(SB50206008L) to MMST3904(SB000002R0L)	0.5
33	49	PWR	11/12	Saha	Adjust CPU Load Line	PR267 change from 9.09K_0402_1%(SD03490918L) to 10.5K_0402_1%(SD03410528L) PR261 change from 3.57K_0402_1%(SD03435718L) to 2.47K_0402_1%(SD03424318L) Add PC252 100U_25V_(6.3X7.7)(SF10004M08L) Add PC215 0.068U_10VX7R_0402 (SE102683K8L)	0.5
34	50	PWR	12/6	Saha	Deeply discharged battery problem.	Add PD54 1SS355_sod323(SC1SS35500L) Add PR373 1K_0603_1%(SD01410018L)	0.5
35	50	PWR	12/6	Saha	Follow Coe A09 schematic	Add PC267 3300PF_0402_50V7K(SE074332K8L) Depop PC266 0.01U_0603_50V7K(SE025103K8L)	0.5
36	47	PWR	12/15	Saha	Follow GGL 1214 item19.	Depop PR12	0.6
37	49 50 46	PWR	1/7	Saha	For acoustical issue	Add PC270-PC273 and PC268 10U_1206_25V6M(SE142106M8L)	0.6

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