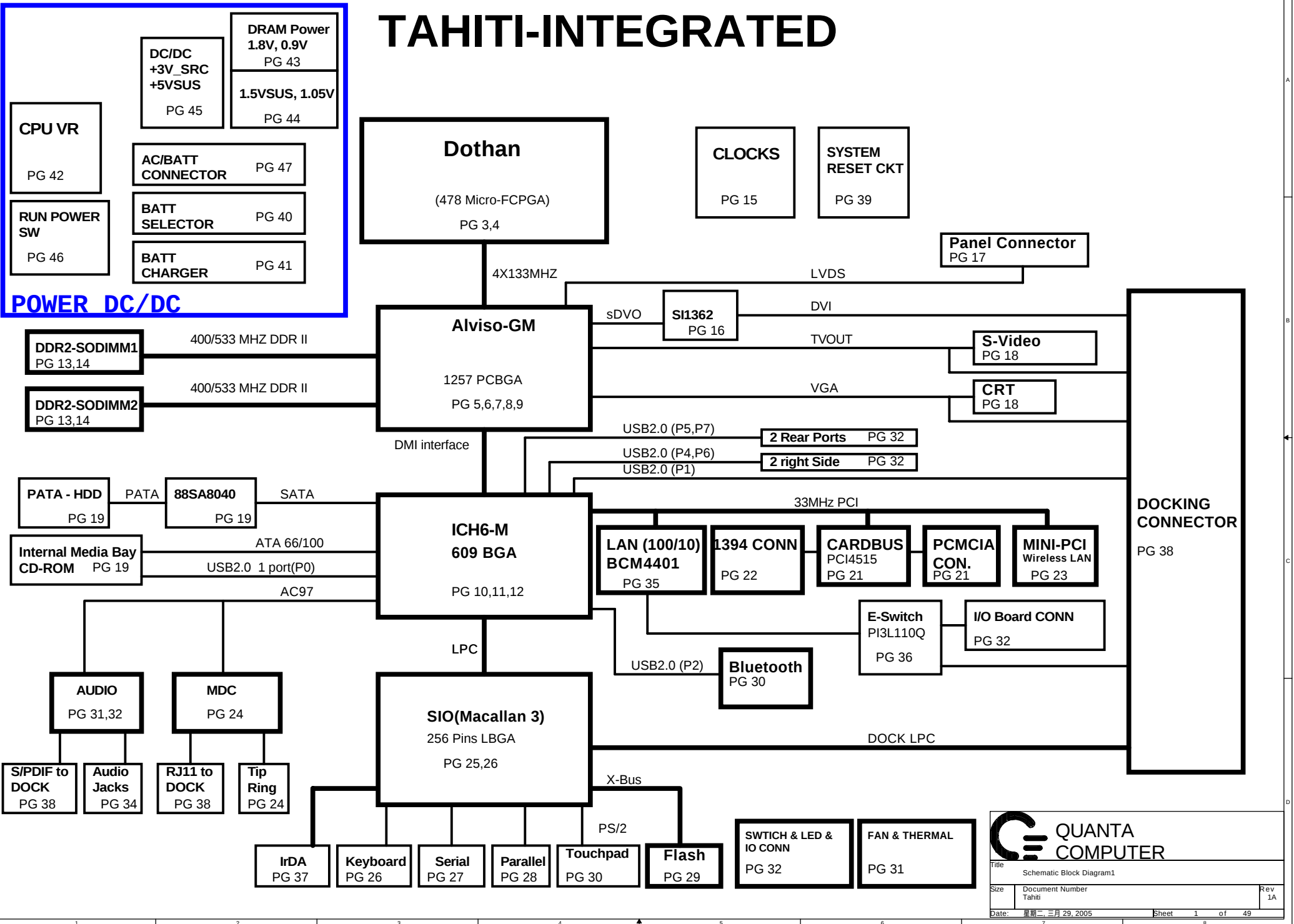
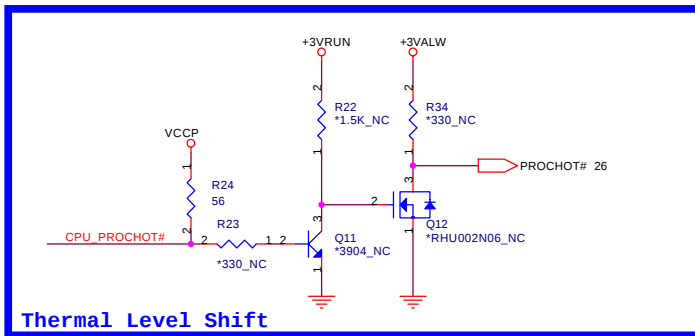
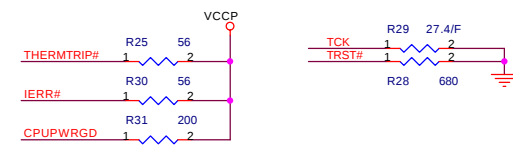
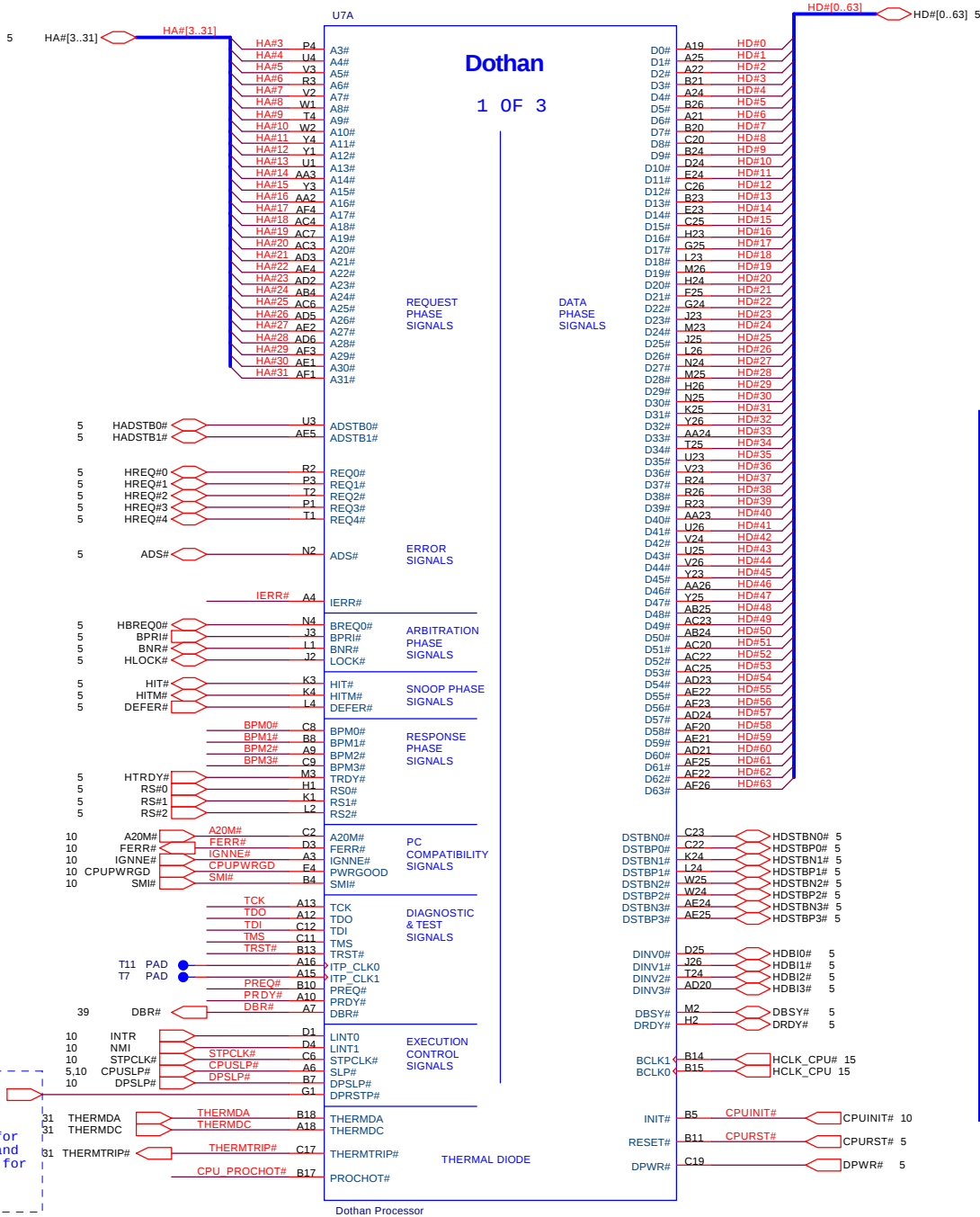


TAHITI-INTEGRATED



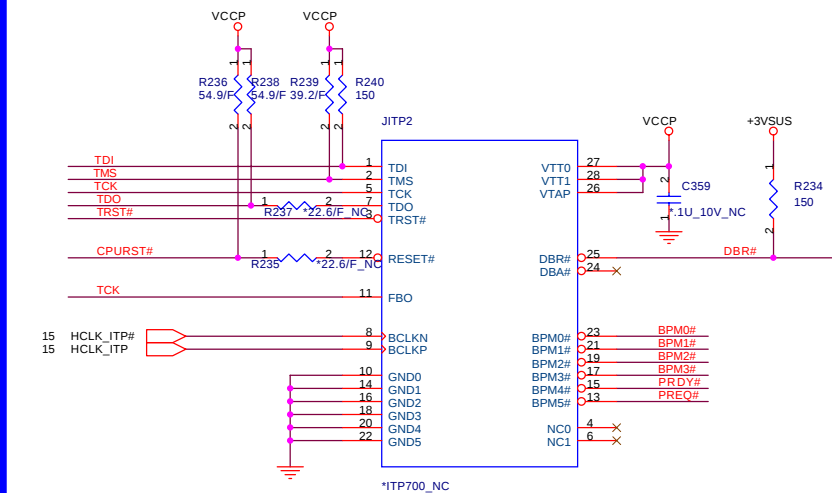
INDEX		
Pg#	Description	DNI LIST
1	Schematic Block Diagram 1	
2	Front Page	
3-4	Dothan	
5-9	Alviso	
10-12	ICH6	
13-14	DDRII SO-DIMM(200P)	
15	Clock Generator	
16	SI1362	
17	LCD Conn. & SSP	
18	CRT & TV Conn.	
19	SATA & IDE Conn.	
20	PAD & Screw Hole	
21	TI PIC4510	
22	CB/1394 CONN	
23	Mini PCI Conn.	
24	MDC Conn.	
25-26	SIO (LPC47N354)	
27	Parallel Port	
28	Serial Port	
29	Flash ROM	
30	Touch Pad CONN.& Bluetooth CONN	
31	Switch Board Conn. & LED & IO Board	
32	FAN & Thermal	
33-34	Audio CODEC (STAC9751) & Phone Jack	
35-36	LAN Interface	
37	FIR	
38	MISCELLANEA	
39	Docking Conn.	
40	SYSTEM RESET/POWER GOOD	
41-42	Battery Selector & Charger	
43	CPU Power	
44	1.8VSUS/0.9V	
45	1.5V/1.05V	
46	D/D Power	
47	RUN Power Switch	
48	RUN POWER SW	

Power & Ground			
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (20V)	
PBATT+		MAIN BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~20V)	
VHORE		CPU CORE POWER (1.25/1.15V)	RUNPWROK
1.05V		AGTL+ POWER (1.05V) I/O	RUNPWROK
+3VRUN		SLP_S3# CTRLD POWER	RUN_ON
+3VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VALW		8051 POWER (5V)	
+5VRUN		SLP_S3# CTRLD POWER	RUN_ON
+5VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VHDD		HDD POWER (5V)	HDDC_EN#
+5VMOD		MODULE POWER (5V)	MODC_EN#
STRB#/5V		EXTERNAL FDD POWER (5V)	FDD/LPT#
+5VRUN		FAN POWER (5V)	FAN_OFF/ON#
VDDA		AUDIO ANALOG POWER (5V)	RUN_ON
1_8VSUS		RESUME WELL IN ICH	
1_8VRUN		SLP_S3# CTRLD POWER	
+3VALW		8051 POWER (3V)	
V1_5RUN		ALVISO POWER Non-CPU I/O	
 GND	ALL PAGES	DIGITAL GROUND	
		COMBO CONN GND	



ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	VTT	Within 2.0" of the CPU

Note: Populate All NC component when ITP connector is populated.



QUANTA COMPUTER

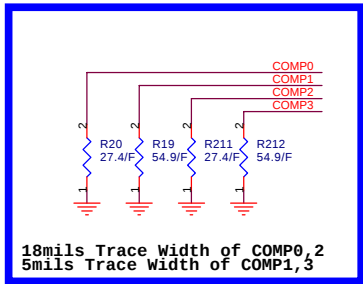
Title: Dothan Processor (HOST)

Size: Document Number Tahiti(DM3L)

Date: 星期三, 三月 29, 2005

Sheet: 3 of 49

Rev: 1A



VCCP

R16 1K/F

R15 2K/F

Z0 = 55 ohm, 25 mils
spacing for switching
signals

COMP0 P25
COMP1 P26
COMP2 AB2
COMP3 AB1

GTLREF0 AD26

TEST1 C5
TEST2 F23

NC1 B2

RSVD2 C3
RSVD3 AF7
RSVD4 AC1
RSVD5 E26

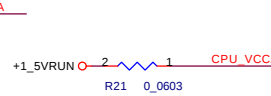
VCCA3 AC26
VCCA2 N1
VCCA0 B1

VHCCORE

D6 VCC00
D8 VCC01
D18 VCC02
D20 VCC03
D22 VCC04
E5 VCC05
E7 VCC06
E9 VCC07
E17 VCC08
E19 VCC09
E21 VCC10
E6 VCC11
F8 VCC12
F18 VCC13
F20 VCC14
F22 VCC15
G5 VCC16
G21 VCC17
H6 VCC18
H22 VCC19
J5 VCC20
K22 VCC21
J6 VCC22
V6 VCC23
V22 VCC24
W5 VCC25
W21 VCC26
Y6 VCC27
Y22 VCC28
AA5 VCC29
AA7 VCC30
AA9 VCC31
AA11 VCC32
AA13 VCC33
AA15 VCC34
AA17 VCC35
AA19 VCC36
AA21 VCC37
AB6 VCC38
AB8 VCC39
AB10 VCC40
AB12 VCC41
AB14 VCC42
AB16 VCC43
AB18 VCC44
AB20 VCC45
AB22 VCC46
AC9 VCC47
AC11 VCC48
AC13 VCC49
AC15 VCC50
AC17 VCC51
AC19 VCC52
AC21 VCC53
AD8 VCC54
AD10 VCC55
AD12 VCC56
AD14 VCC57
AD16 VCC58
AD18 VCC59
AE9 VCC60
AE11 VCC61
AE13 VCC62
AE15 VCC63
AE17 VCC64
AE19 VCC65
AE21 VCC66
AE23 VCC67
AE25 VCC68
AE27 VCC69
AE29 VCC70
AE31 VCC71

Dothan
2 OF 3

POWER, GROUND, RESERVED
SIGNALS



VHCCORE

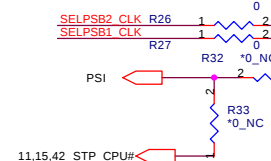
D6 VCC00
D8 VCC01
D18 VCC02
D20 VCC03
D22 VCC04
E5 VCC05
E7 VCC06
E9 VCC07
E17 VCC08
E19 VCC09
E21 VCC10
E6 VCC11
F8 VCC12
F18 VCC13
F20 VCC14
F22 VCC15
G5 VCC16
G21 VCC17
H6 VCC18
H22 VCC19
J5 VCC20
K22 VCC21
J6 VCC22
V6 VCC23
V22 VCC24
W5 VCC25
W21 VCC26
Y6 VCC27
Y22 VCC28
AA5 VCC29
AA7 VCC30
AA9 VCC31
AA11 VCC32
AA13 VCC33
AA15 VCC34
AA17 VCC35
AA19 VCC36
AA21 VCC37
AB6 VCC38
AB8 VCC39
AB10 VCC40
AB12 VCC41
AB14 VCC42
AB16 VCC43
AB18 VCC44
AB20 VCC45
AB22 VCC46
AC9 VCC47
AC11 VCC48
AC13 VCC49
AC15 VCC50
AC17 VCC51
AC19 VCC52
AC21 VCC53
AD8 VCC54
AD10 VCC55
AD12 VCC56
AD14 VCC57
AD16 VCC58
AD18 VCC59
AE9 VCC60
AE11 VCC61
AE13 VCC62
AE15 VCC63
AE17 VCC64
AE19 VCC65
AE21 VCC66
AE23 VCC67
AE25 VCC68
AE27 VCC69
AE29 VCC70
AE31 VCC71

Dothan Processor

VSS00 A2
VSS01 A5
VSS02 A8
VSS03 A11
VSS04 A14
VSS05 A17
VSS06 A20
VSS07 A23
VSS08 A26
VSS09 B3
VSS10 B6
VSS11 B9
VSS12 B12
VSS13 B16
VSS14 B19
VSS15 B22
VSS16 B25
VSS17 C1
VSS18 C4
VSS19 C7
VSS20 C10
VSS21 C13
VSS22 C15
VSS23 C18
VSS24 C21
VSS25 C24
VSS26 D2
VSS27 D5
VSS28 D7
VSS29 D9
VSS30 D11
VSS31 D13
VSS32 D15
VSS33 D17
VSS34 D19
VSS35 D21
VSS36 D23
VSS37 D26
VSS38 E3
VSS39 E6
VSS40 E8
VSS41 E10
VSS42 E12
VSS43 E14
VSS44 E16
VSS45 E18
VSS46 E20
VSS47 E22
VSS48 E25
VSS49 F1
VSS50 F4
VSS51 F6
VSS52 F7
VSS53 F9
VSS54 F11
VSS55 F13
VSS56 F15
VSS57 F17
VSS58 F19
VSS59 F21
VSS60 F24
VSS61 G2
VSS62 G6
VSS63 G22
VSS64 G23
VSS65 G26
VSS66 H3
VSS67 H5
VSS68 H21
VSS69 H25
VSS70 J1
VSS71 J4
VSS72 J6
VSS73 J22
VSS74 J24
VSS75 K2
VSS76 K5
VSS77 K21
VSS78 K23
VSS79 K26
VSS80 L3
VSS81 L6
VSS82 L22
VSS83 L25
VSS84 M1
VSS85 M4
VSS86 M5
VSS87 M21
VSS88 M24
VSS89 N3
VSS90 N6
VSS91 N22
VSS92 N23
VSS93 N26
VSS94 P2
VSS95 P5
VSS96 P21
VSS97 P24
VSS98 R1
VSS99 R4

6.15 SELPSB2_CLK
6.15 SELPSB1_CLK

Differential Probe
Test Using



NO PSI (Power Saving
Indicator)

	DothanA	DothanB
R26	NC	Install

VCCP

U7C

Dothan
3 OF 3

POWER, GROUND AND NC

VID

D10 VCCP0
D12 VCCP1
D14 VCCP2
D16 VCCP3
D18 VCCP4
D20 VCCP5
D22 VCCP6
D24 VCCP7
D26 VCCP8
D28 VCCP9
D30 VCCP10
D32 VCCP11
D34 VCCP12
D36 VCCP13
D38 VCCP14
D40 VCCP15
D42 VCCP16
D44 VCCP17
D46 VCCP18
D48 VCCP19
D50 VCCP20
D52 VCCP21
D54 VCCP22
D56 VCCP23
D58 VCCP24
D60 VCCQ0
D62 VCCQ1

VID0 E2
VID1 F2
VID2 G3
VID3 H4
VID4 I4
VID5 J4

VCCSENSE AE7
VSSSENSE AF6

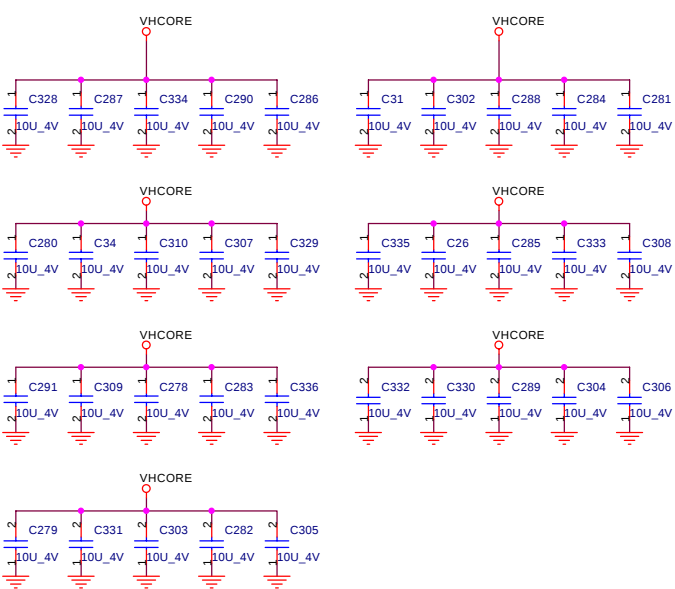
BSEL0 C16
BSEL1 C14

PSI F1

VSS100 R6
VSS101 R22
VSS102 R25
VSS103 T3
VSS104 T5
VSS105 T7
VSS106 T9
VSS107 T26
VSS108 U2
VSS109 U22
VSS110 U24
VSS111 U26
VSS112 V1
VSS113 V4
VSS114 V5
VSS115 V21
VSS116 V25
VSS117 W3
VSS118 W6
VSS119 W22

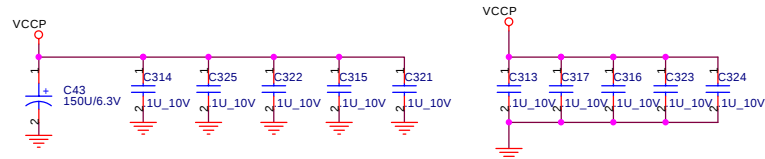
VSS120 W23
VSS121 W26
VSS122 Y2
VSS123 Y5
VSS124 Y24
VSS125 AA1
VSS126 AA2
VSS127 AA4
VSS128 AA6
VSS129 AA8
VSS130 AA10
VSS131 AA12
VSS132 AA14
VSS133 AA16
VSS134 AA18
VSS135 AA20
VSS136 AA25
VSS137 AB3
VSS138 AB5
VSS139 AB7
VSS140 AB9
VSS141 AB11
VSS142 AB13
VSS143 AB15
VSS144 AB17
VSS145 AB19
VSS146 AB21
VSS147 AB23
VSS148 AB26
VSS149 AC2
VSS150 AC5
VSS151 AC8
VSS152 AC10
VSS153 AC12
VSS154 AC14
VSS155 AC16
VSS156 AC18
VSS157 AC21
VSS158 AC24
VSS159 AD1
VSS160 AD4
VSS161 AD7
VSS162 AD9
VSS163 AD11
VSS164 AD13
VSS165 AD15
VSS166 AD17
VSS167 AD19
VSS168 AD22
VSS169 AD25
VSS170 AE3
VSS171 AE6
VSS172 AE8
VSS173 AE10
VSS174 AE12
VSS175 AE14
VSS176 AE16
VSS177 AE18
VSS178 AE20
VSS179 AE23
VSS180 AE26
VSS181 AE29
VSS182 AF5
VSS183 AF9
VSS184 AF11
VSS185 AF13
VSS186 AF15
VSS187 AF17
VSS188 AF19
VSS189 AF21
VSS190 AF24
VSS191

Dothan Processor

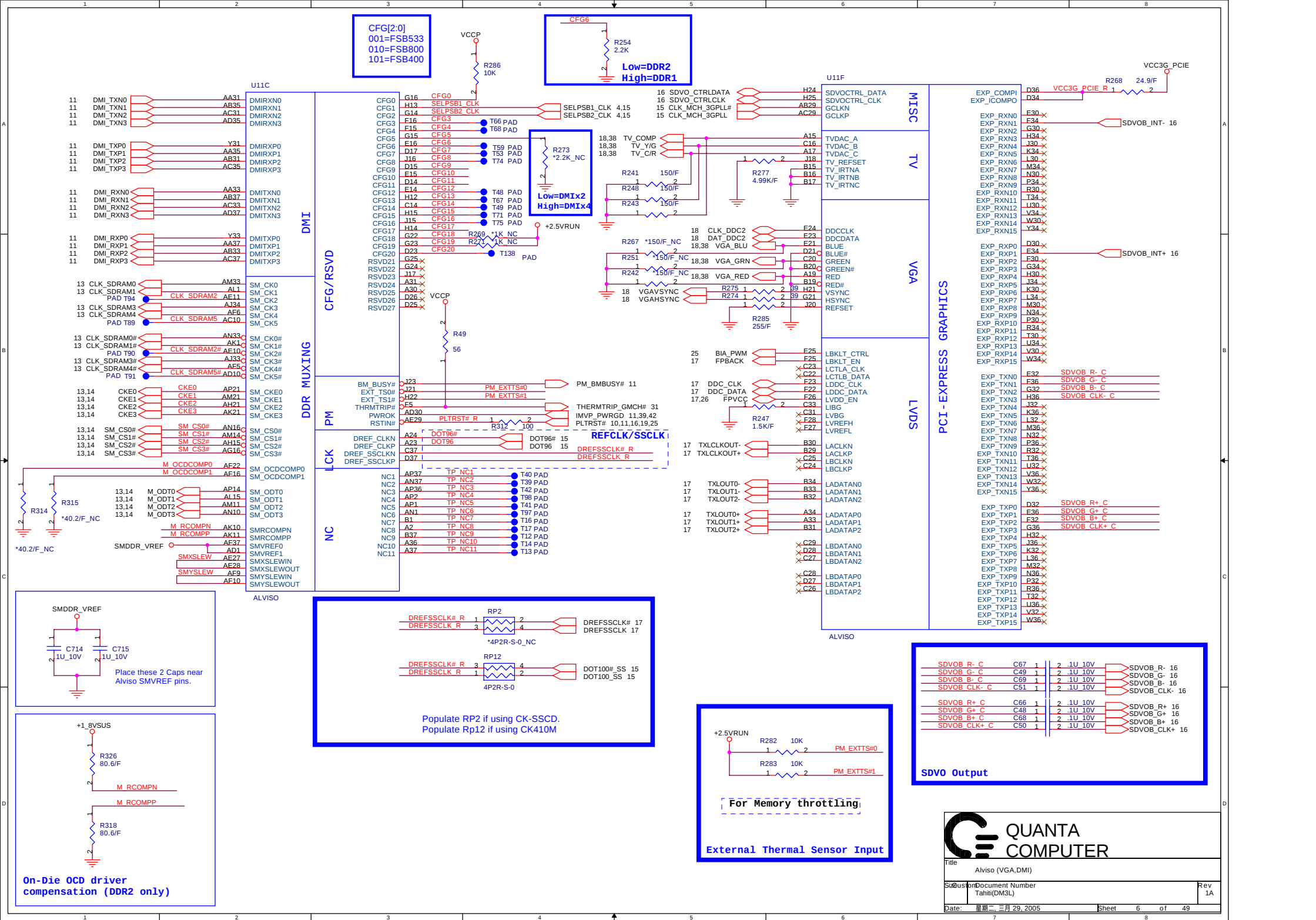


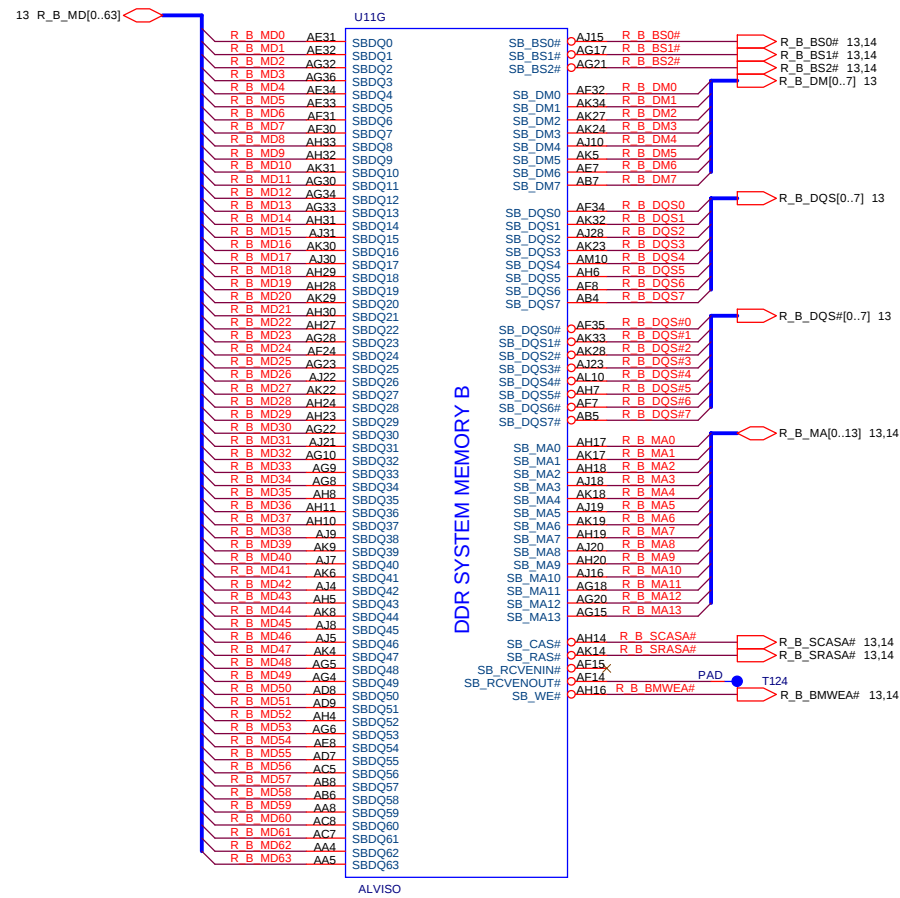
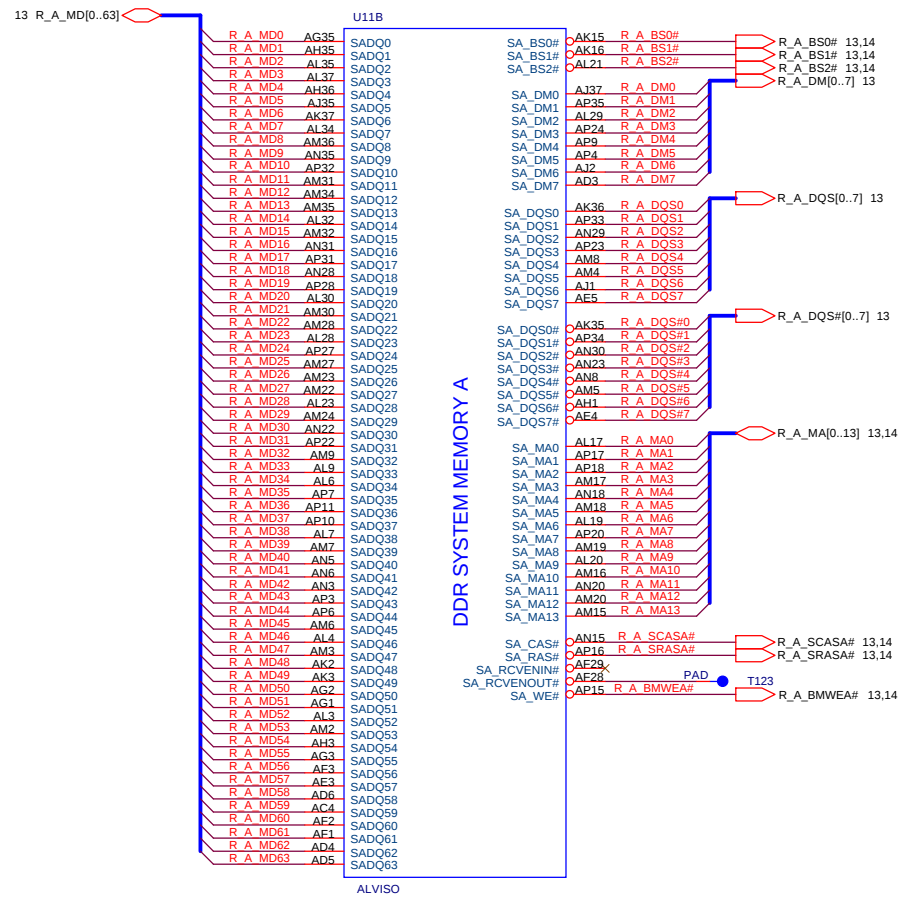
VHCCORE

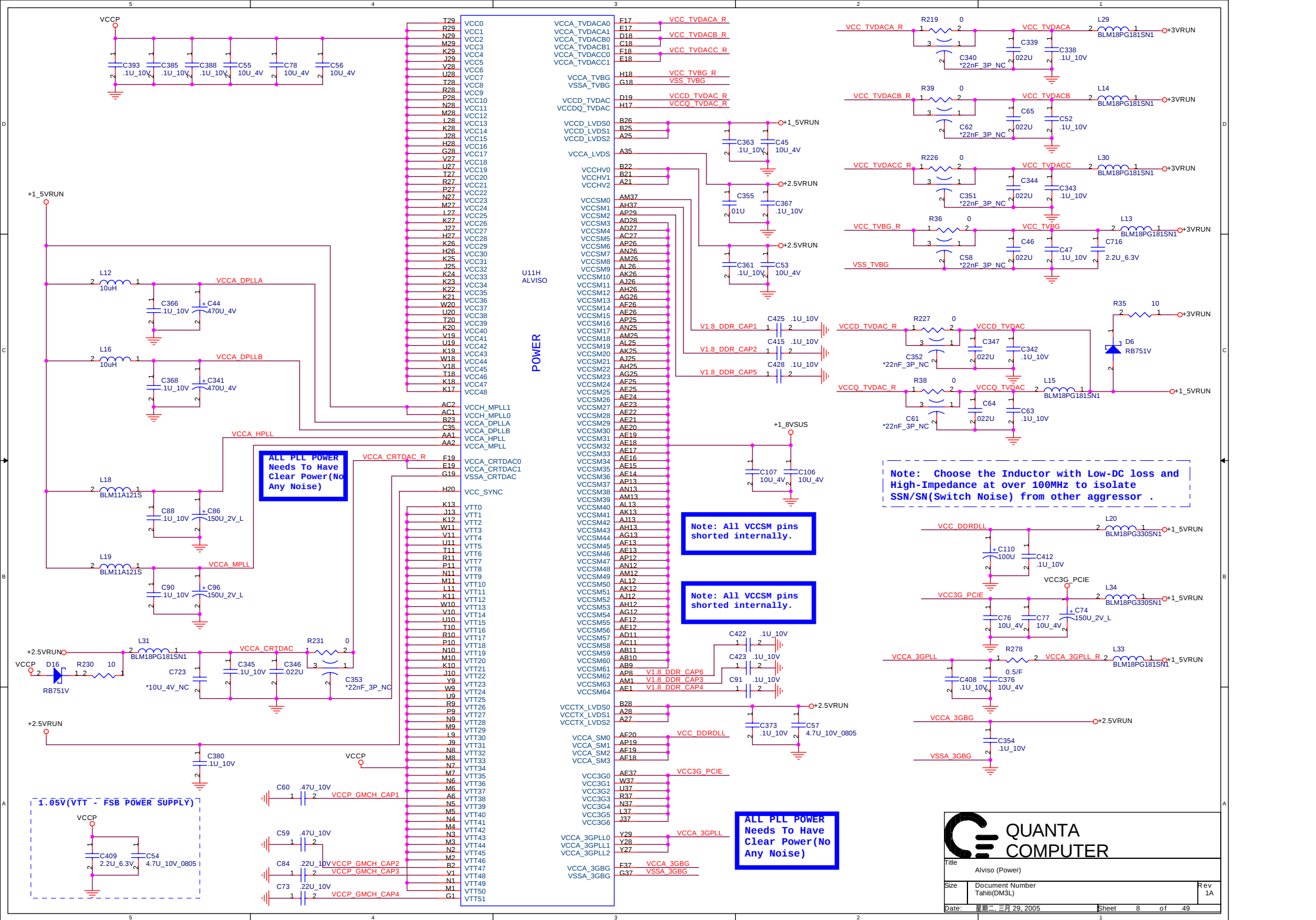
Total caps = 1670 uF > 1430 uF (Intel Recommendation)
ESR = 9m ohm/4 // 5m ohm/35 ----> = 0.1343m ohm



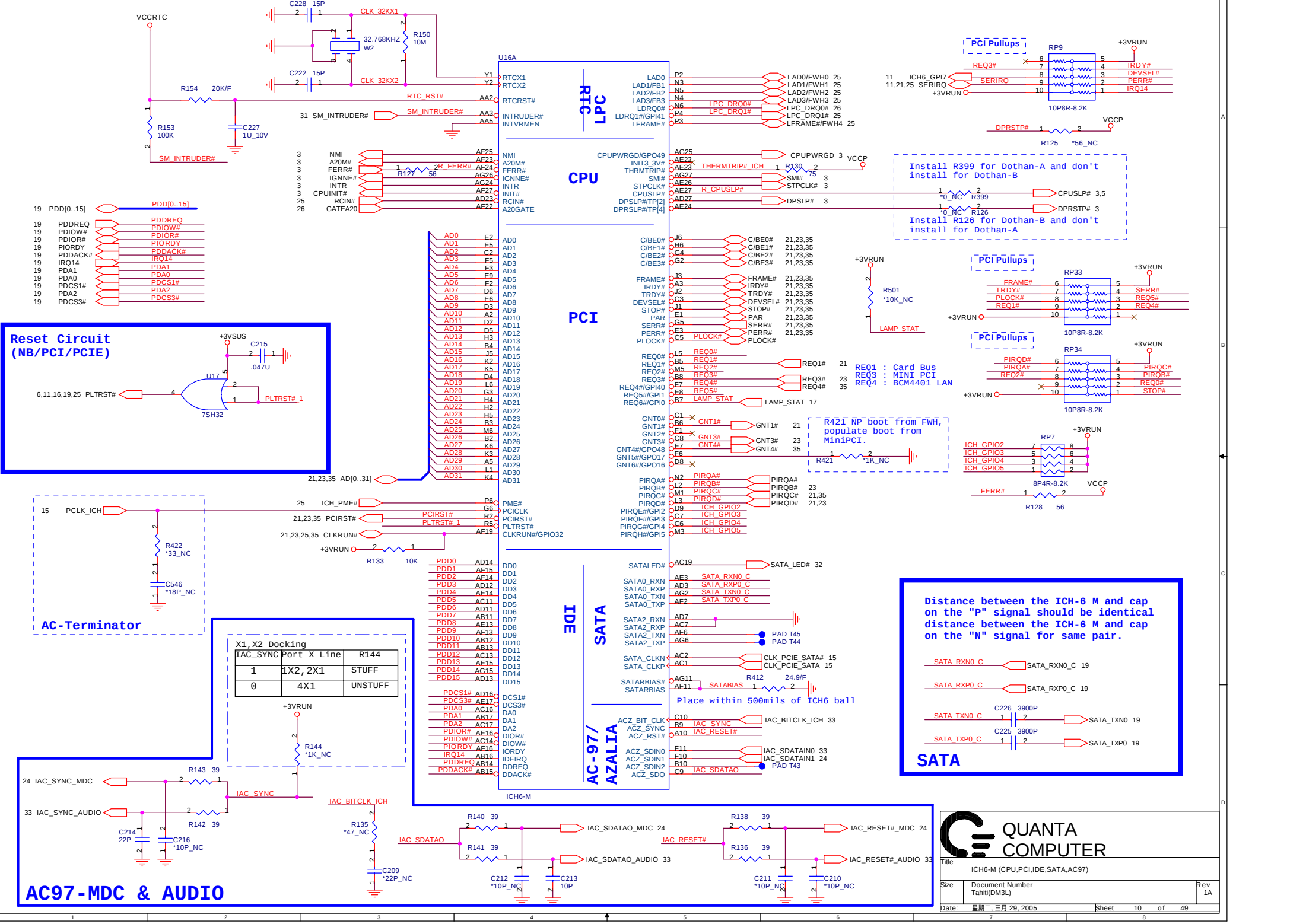
C, mF-----ESR, mW-----ESL, nH
1 x 150 mF-----42 mW (typ) / 2-----2.5 nH / 12
10 x 0.1 mF-----16 mW (typ) / 10-----0.6 nH / 10



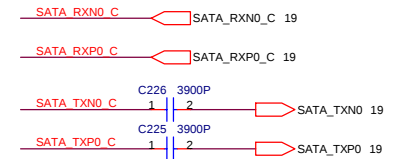






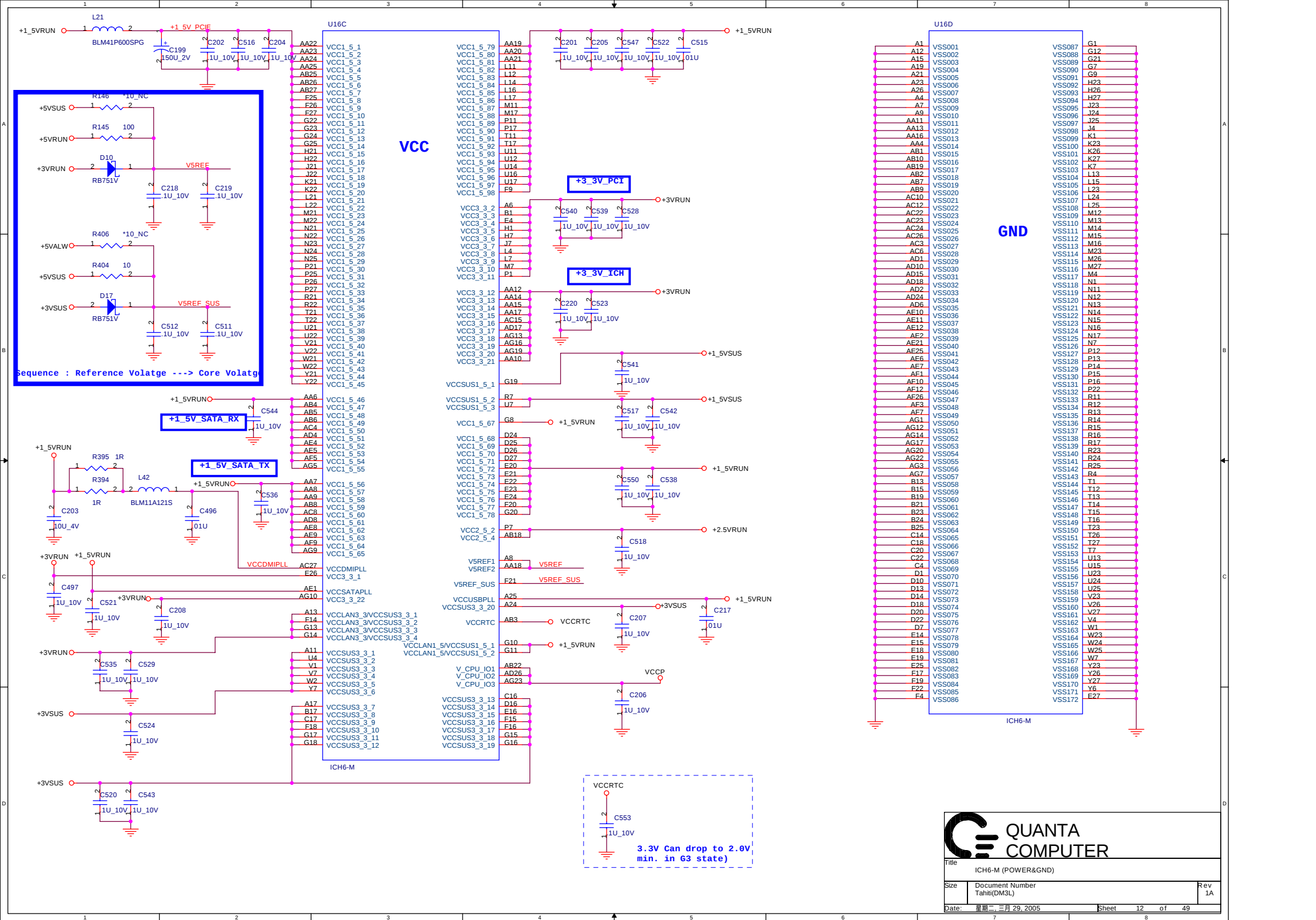


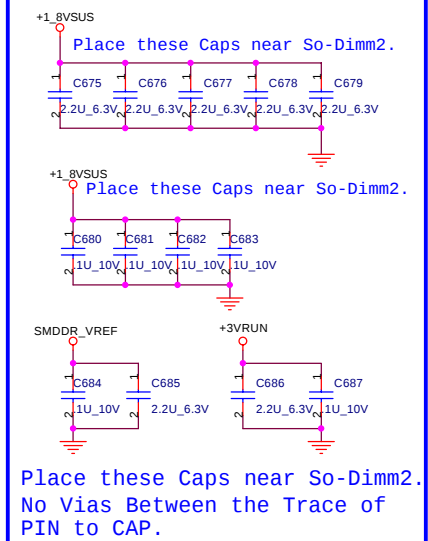
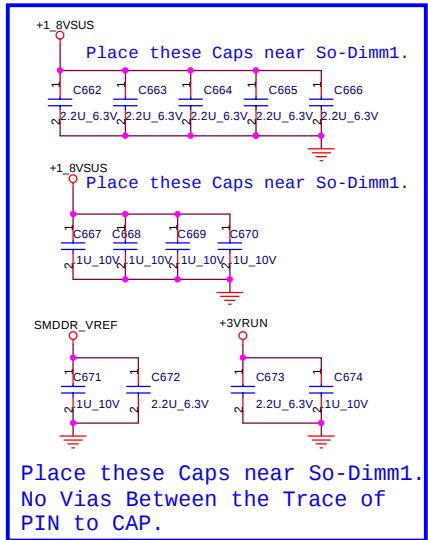
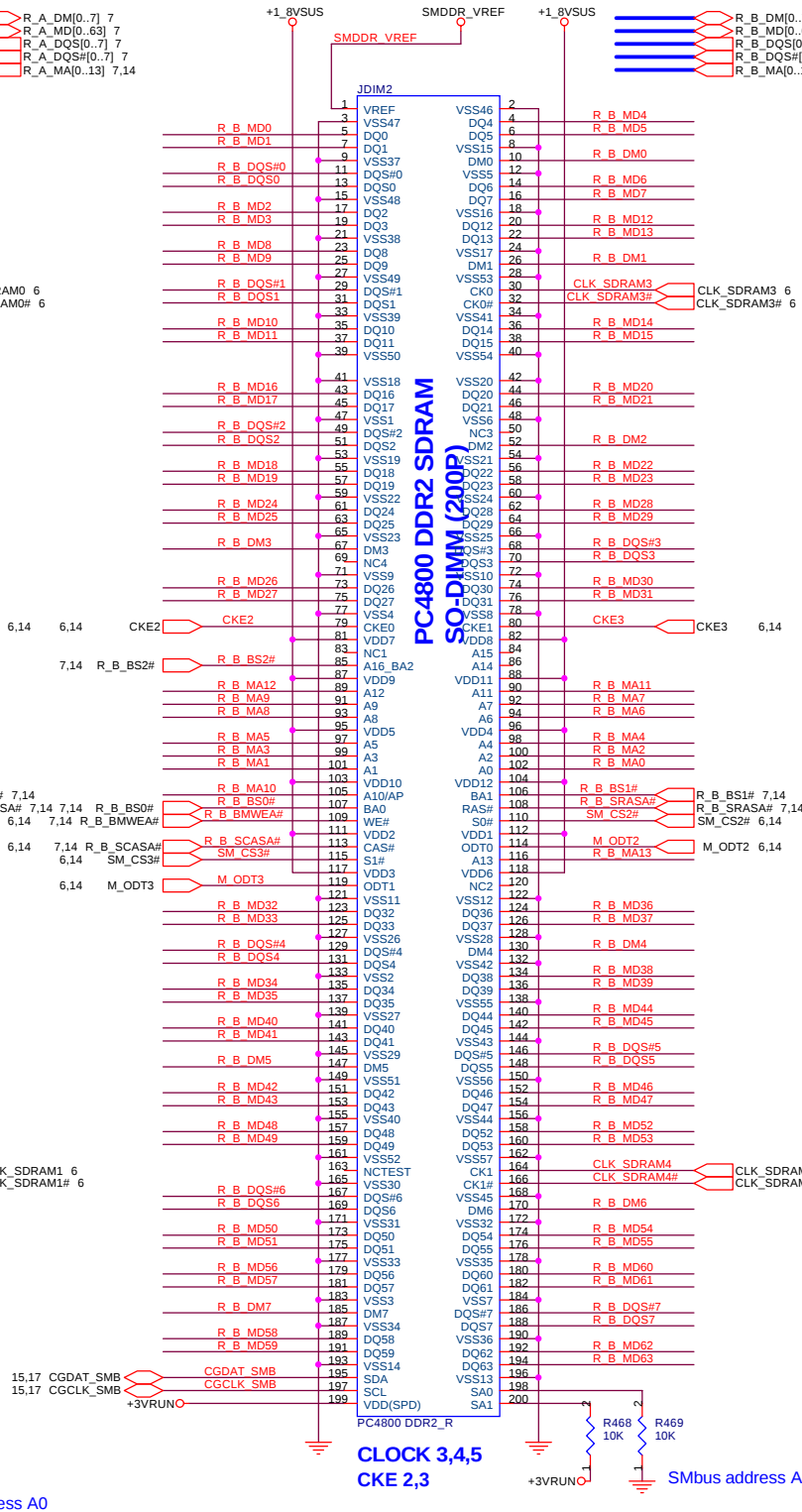
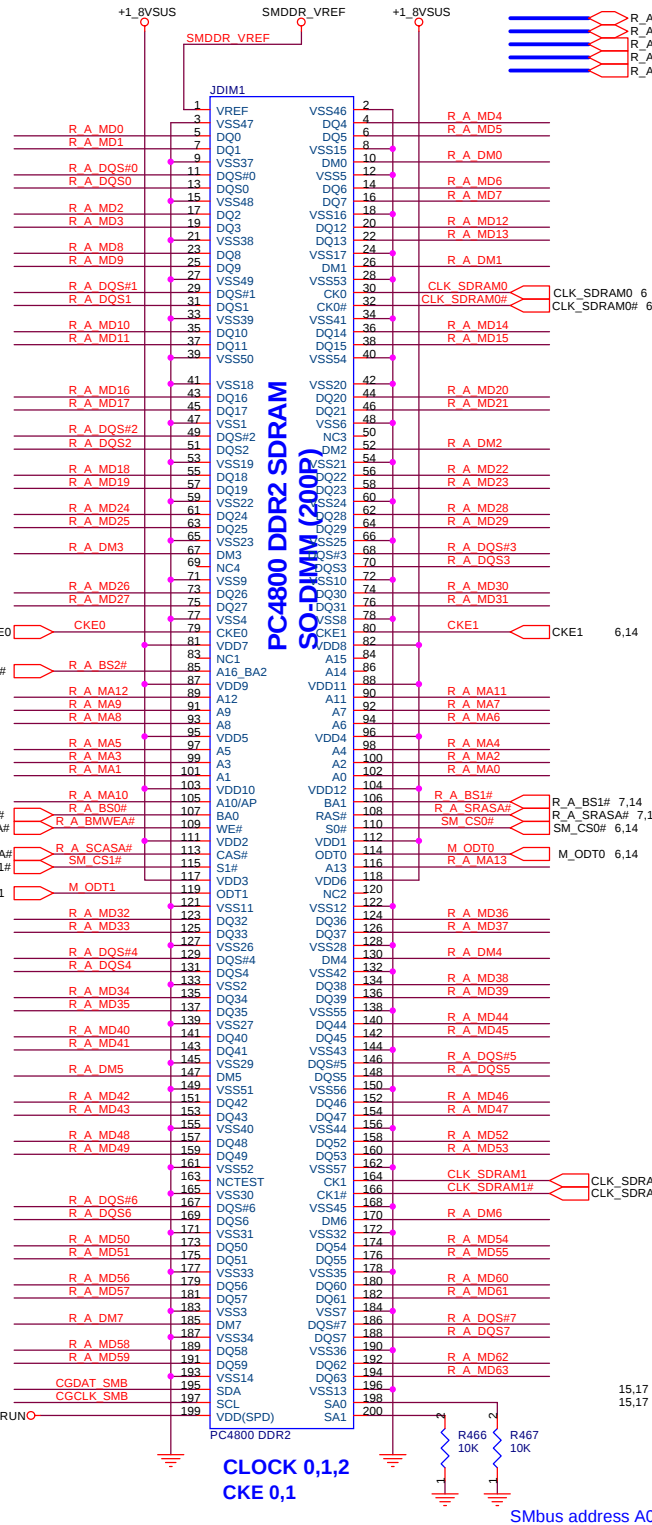
Distance between the ICH-6 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.



SATA

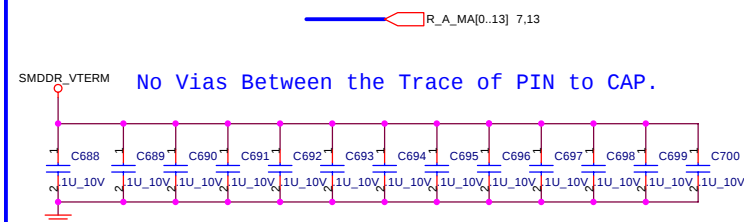




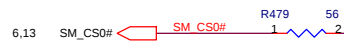
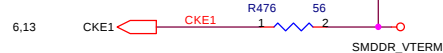
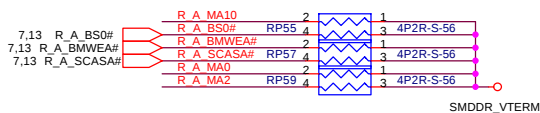
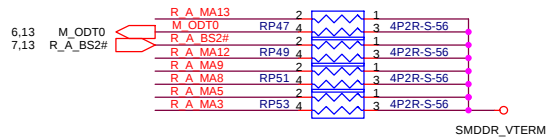
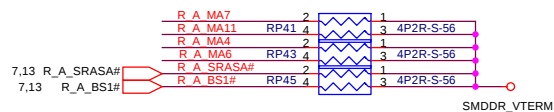


DDRII DUAL CHANNEL A,B.

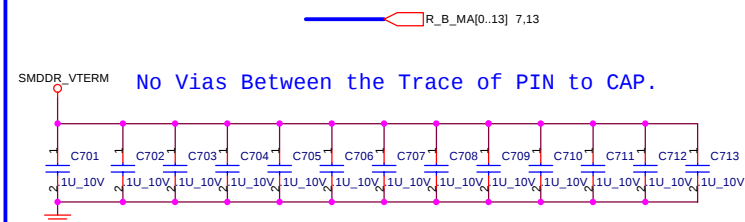
DDRII A CHANNEL



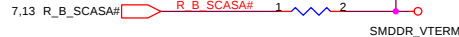
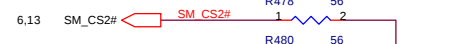
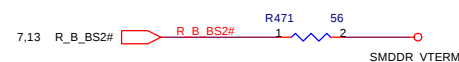
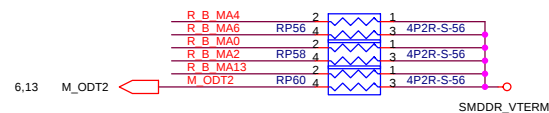
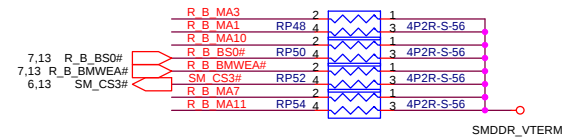
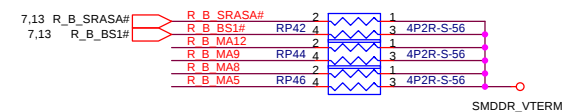
Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

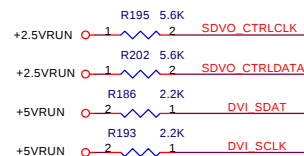


DDRII B CHANNEL

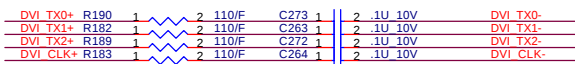
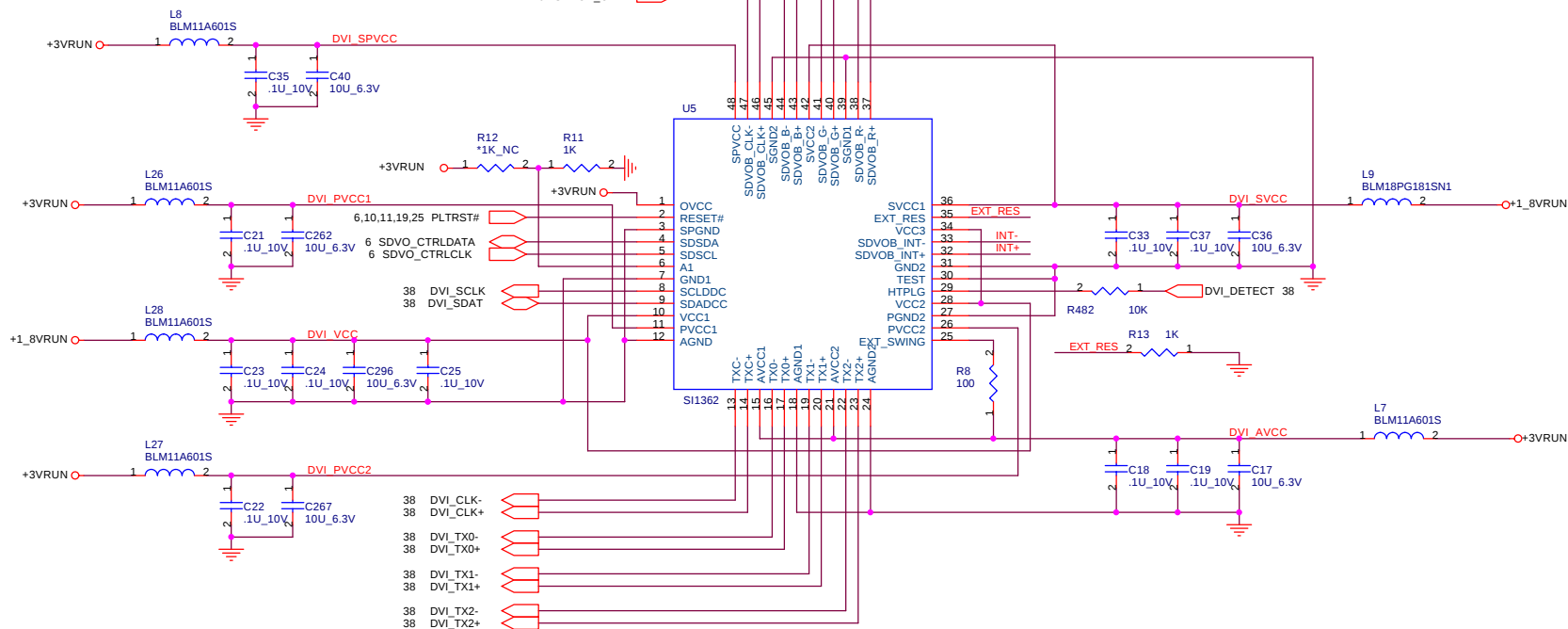
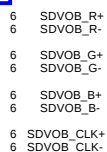
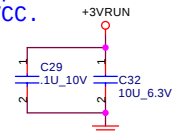


Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.



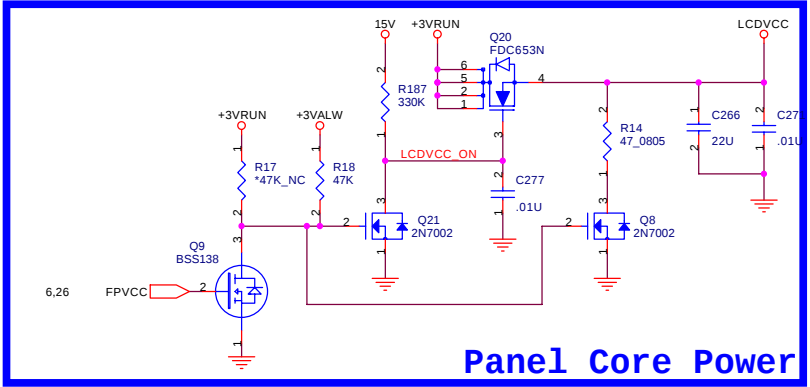


Placed this Bypass capacitor close to OVCC.



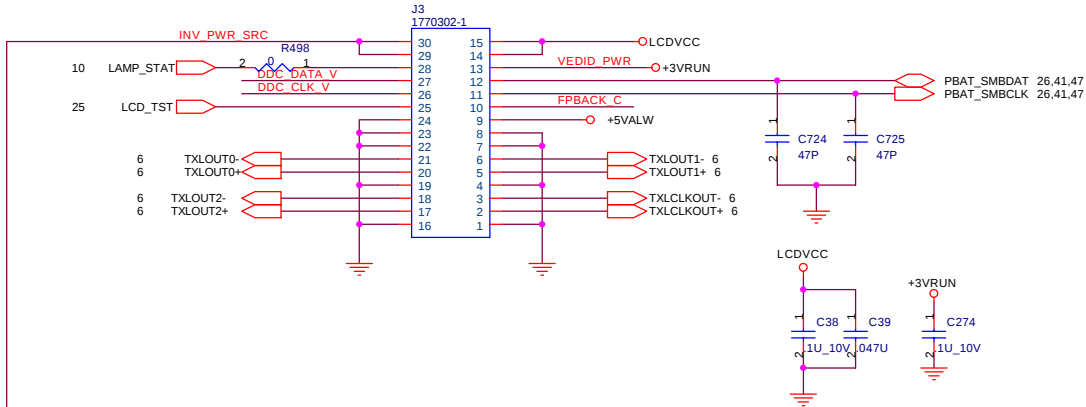
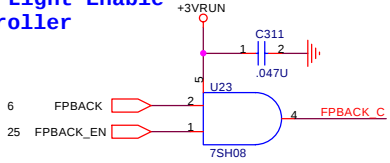
Put these 4 Resistors and 4 Capacitors close to the TX pin of SDVO device



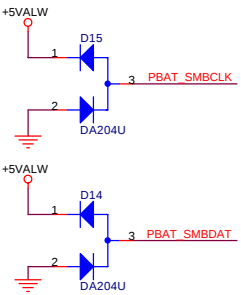


Panel Core Power

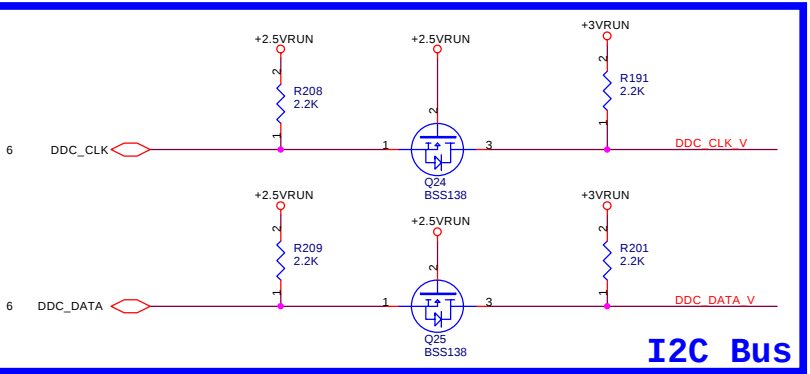
Back Light Enable controller



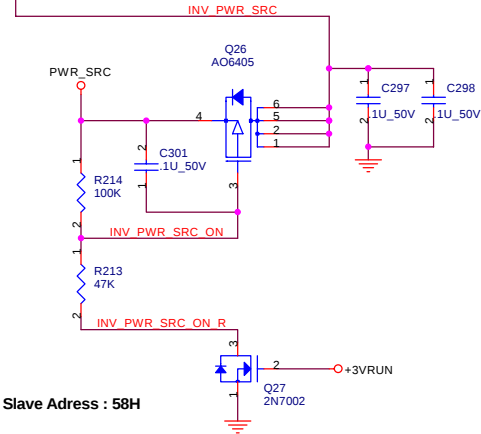
LCD CONN



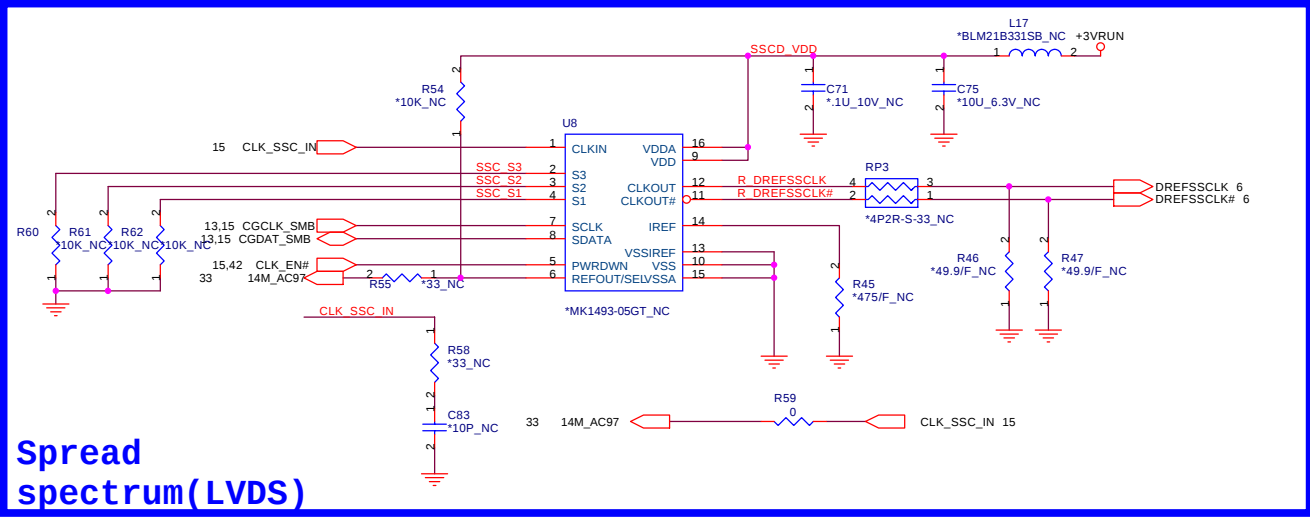
Diode Terminator/ ESD Protector



I2C Bus



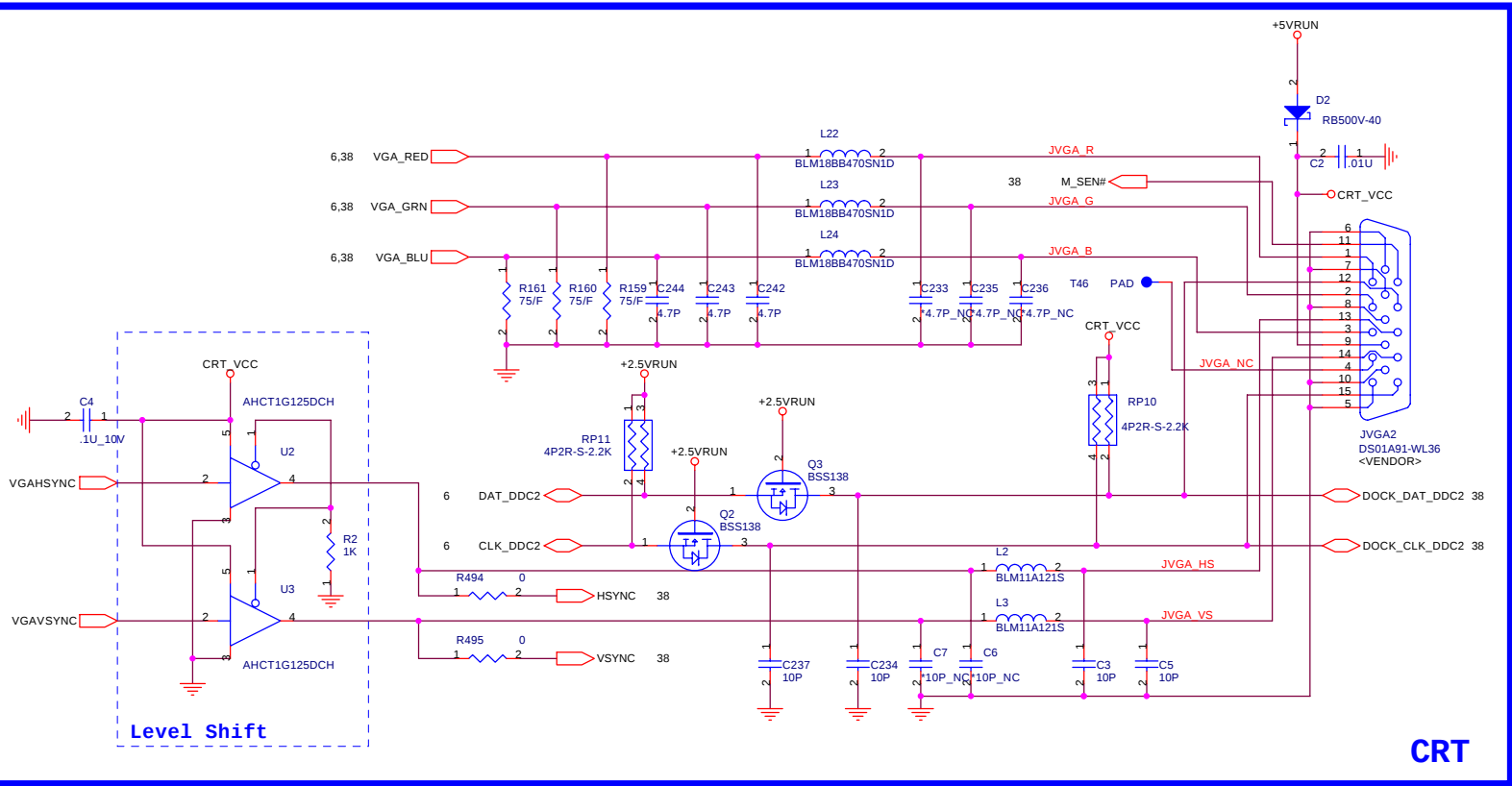
Slave Address : 58H



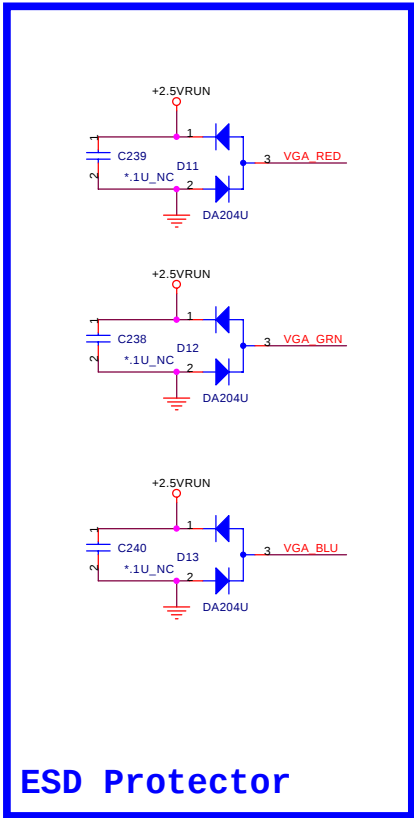
Spread spectrum(LVDS)



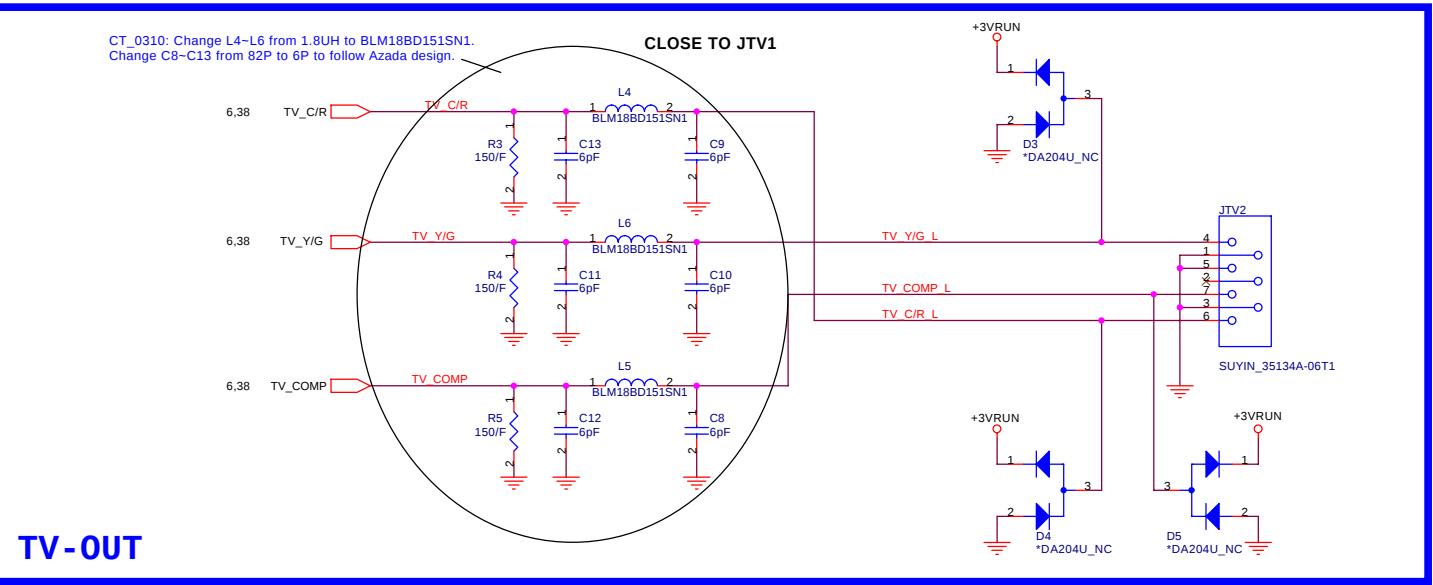
Title			LCD CONN&CK-SSCD
Size	Document Number	Rev	
	Tahiti(DM3L)	1A	
Date:	星期二, 三月 29, 2005	Sheet	17 of 49



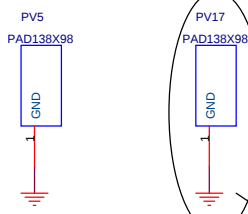
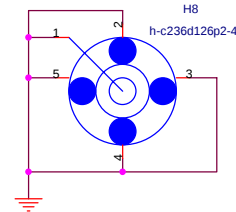
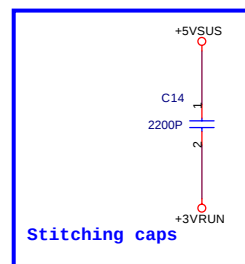
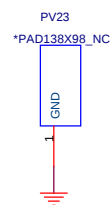
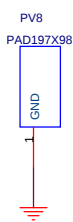
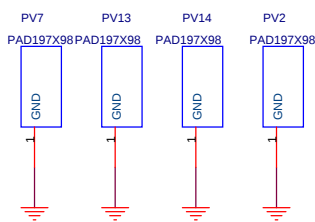
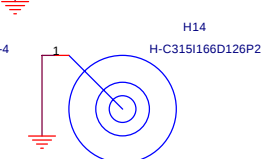
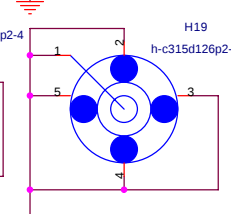
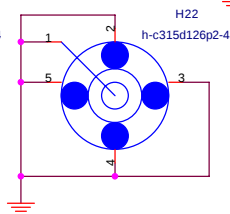
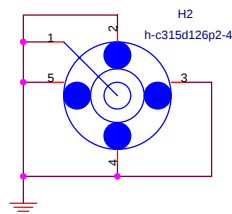
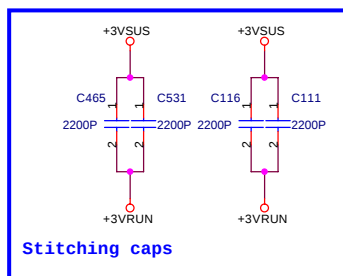
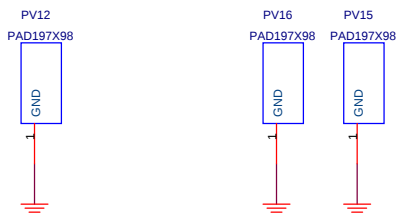
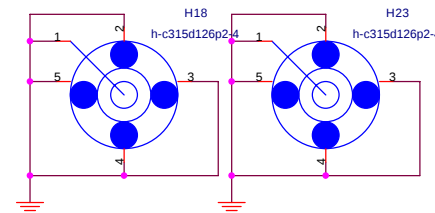
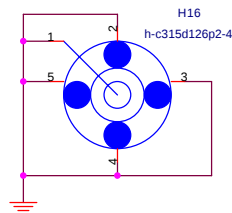
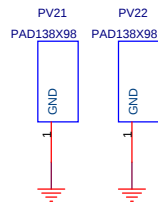
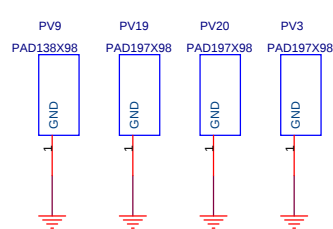
CRT



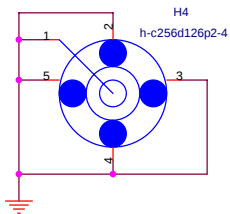
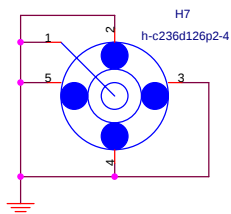
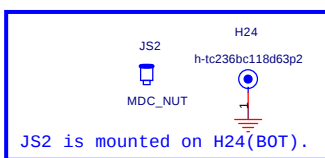
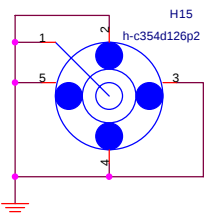
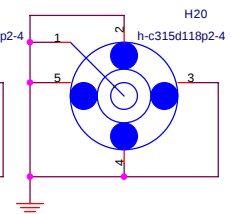
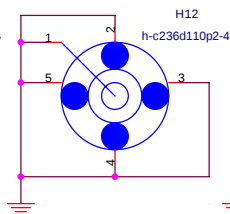
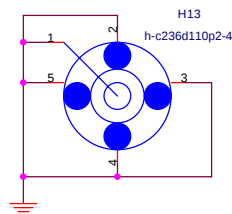
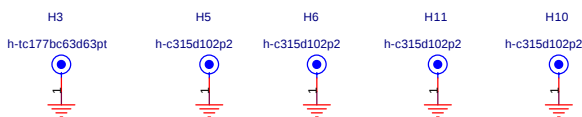
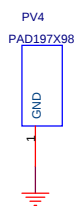
ESD Protector

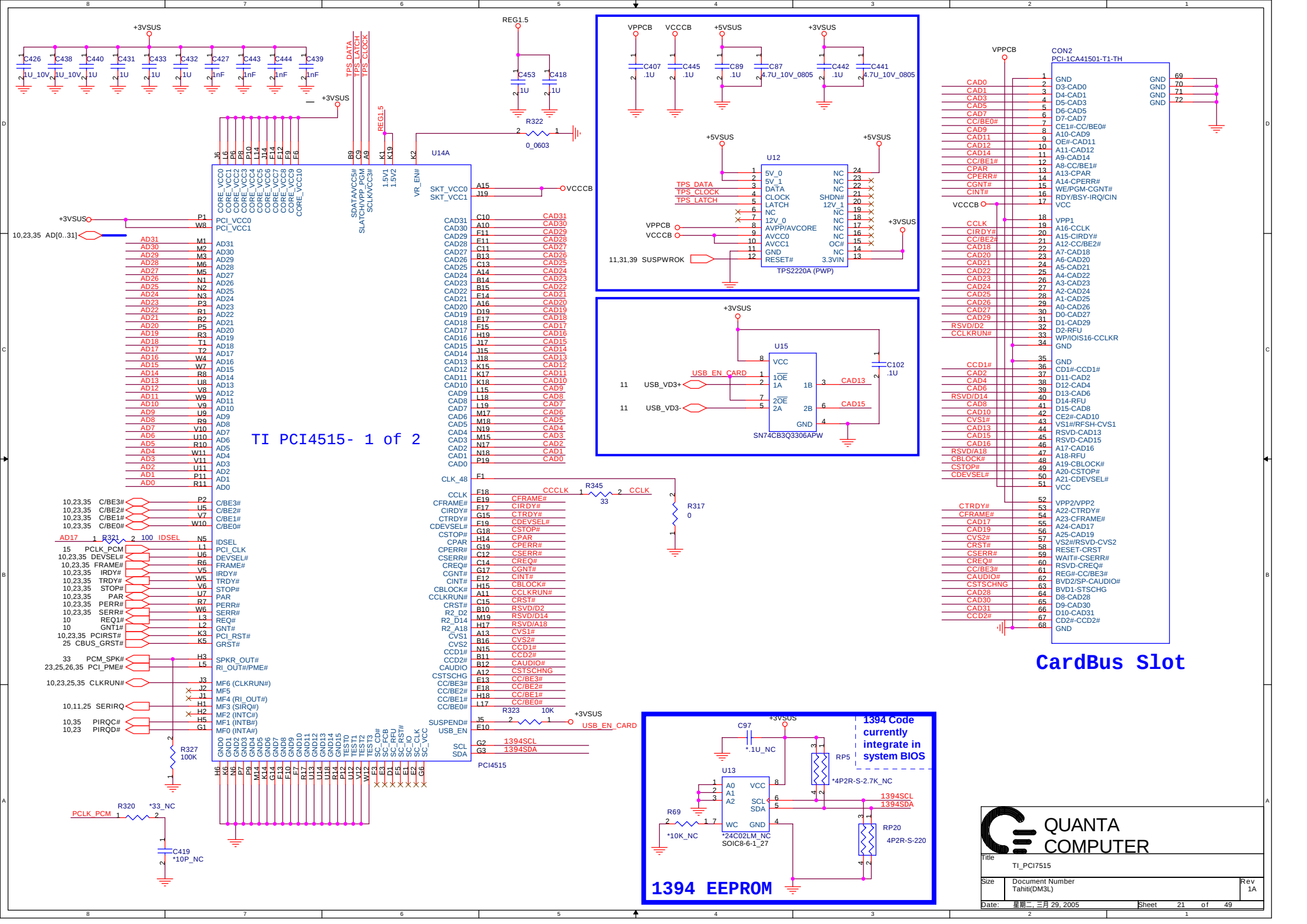


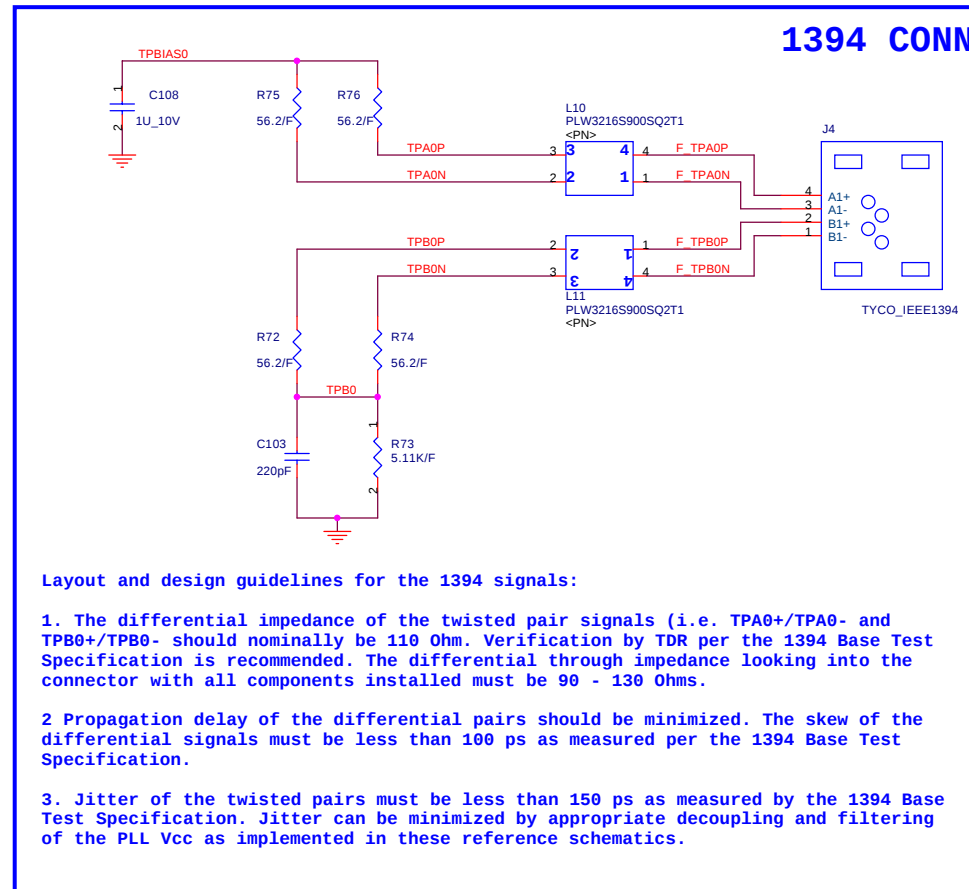
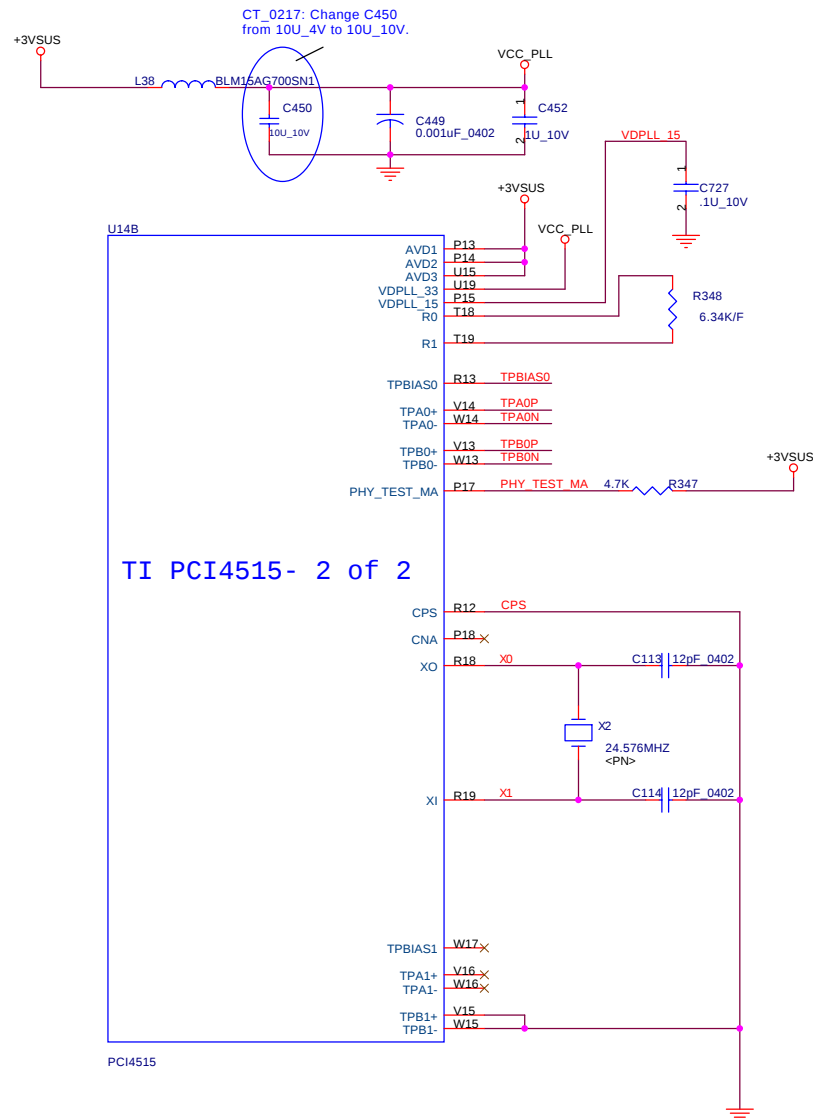
TV-OUT

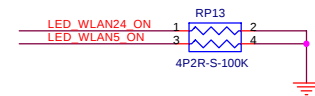
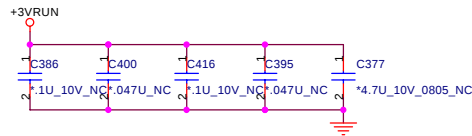
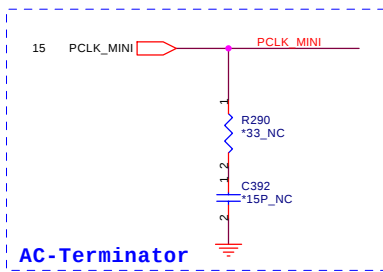


CT_0314:Change PV17 from PAD197x98 to PAD138x98 small size.

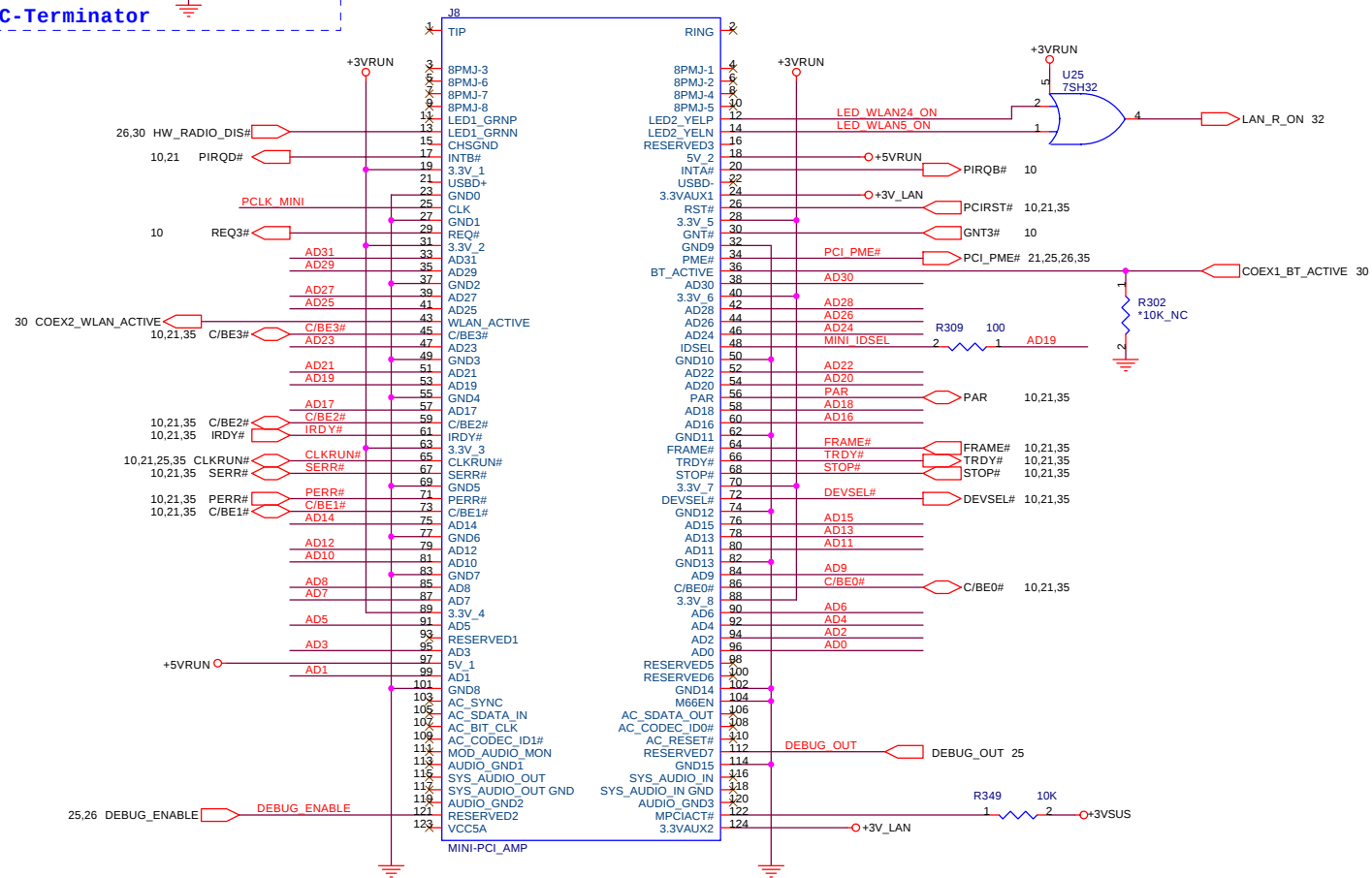


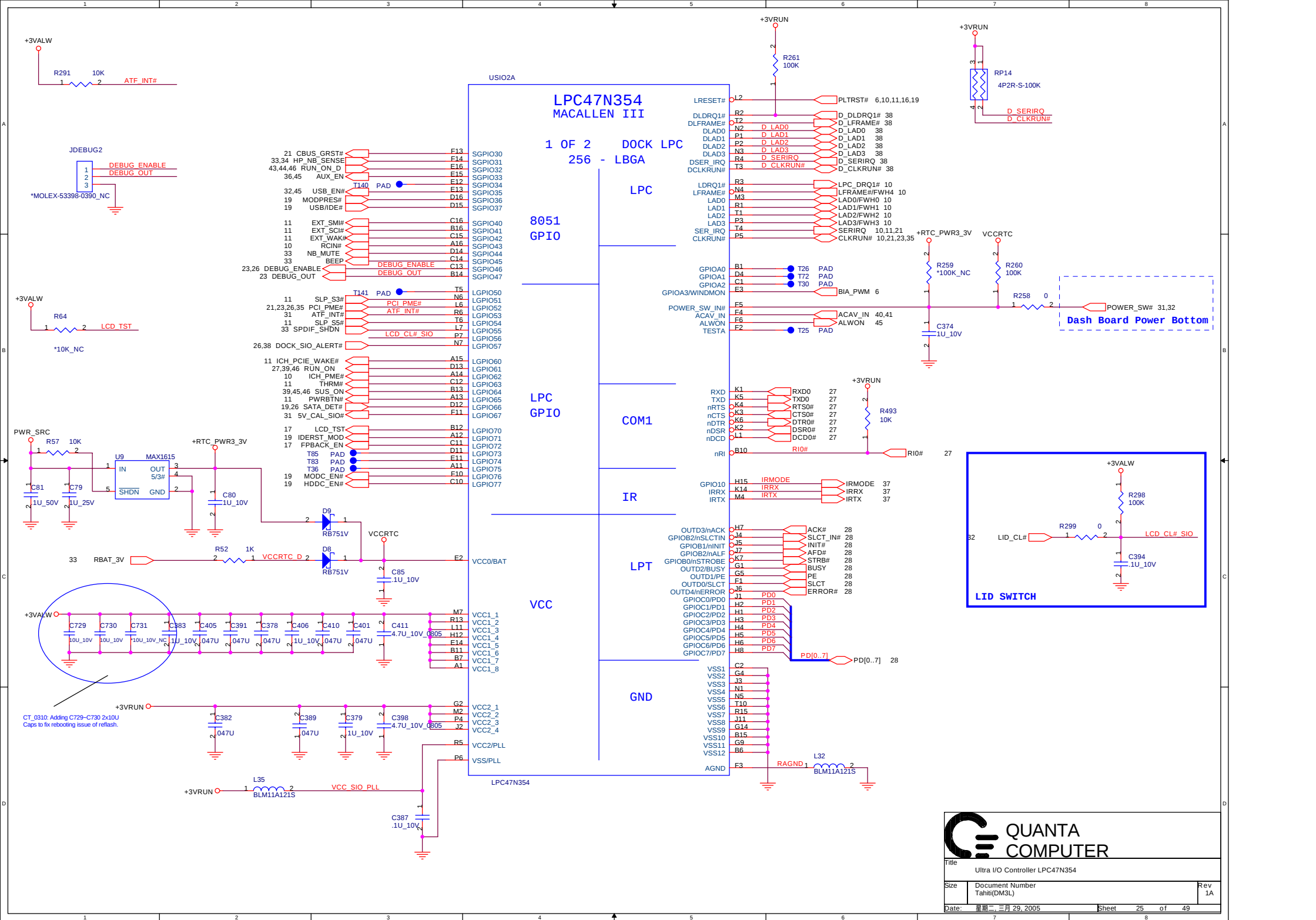


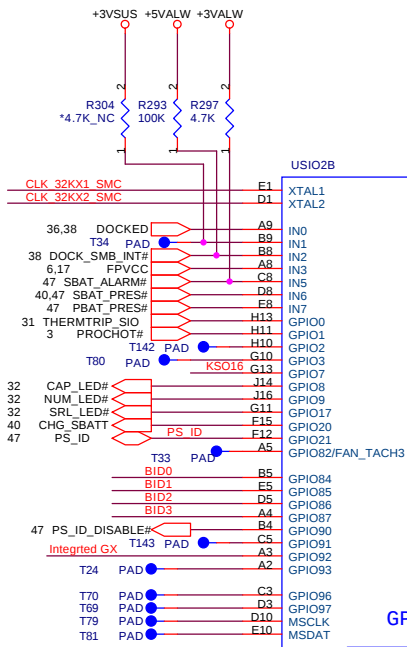
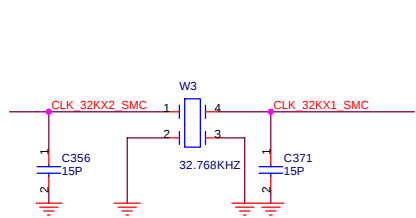




AD[0..31] 10,21,35







LPC47N354 MACALLEN III 2 OF 2 256 - LBGA

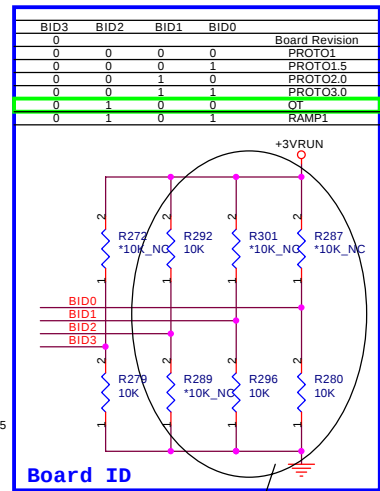
MISC

GPIO

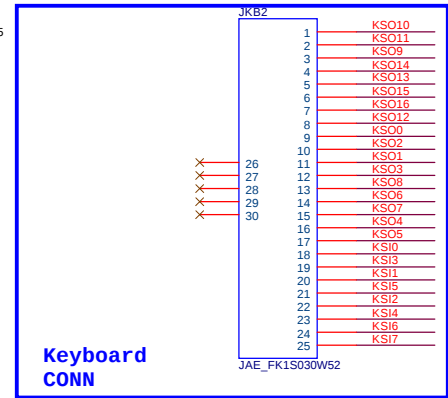
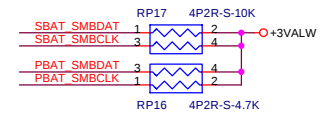
CLOCK

K/B

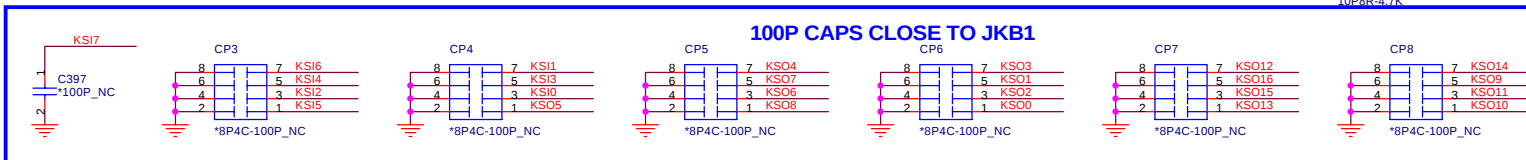
FLASH



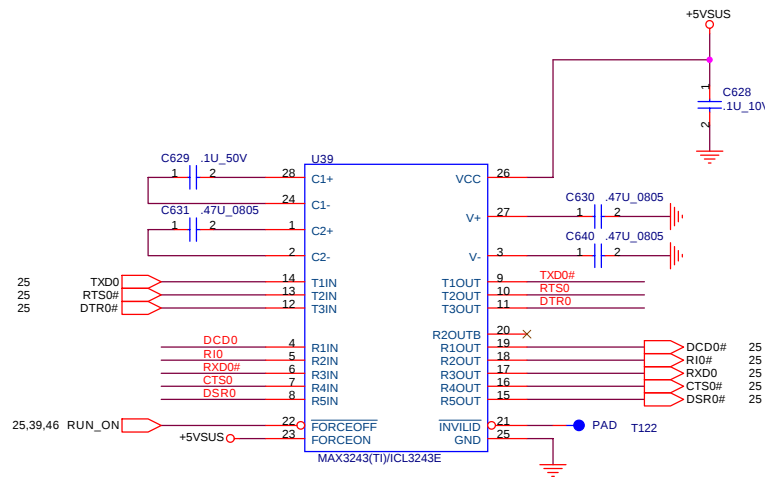
CT_0217: Pop R296, R280, R292 10K, Depop R301, R287, R289 10K.



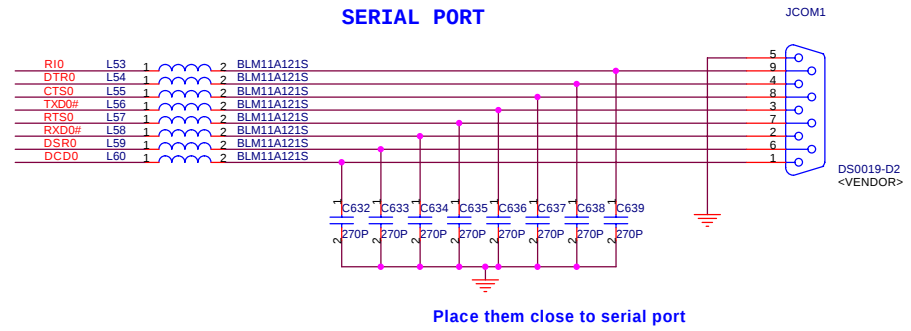
Keyboard CONN

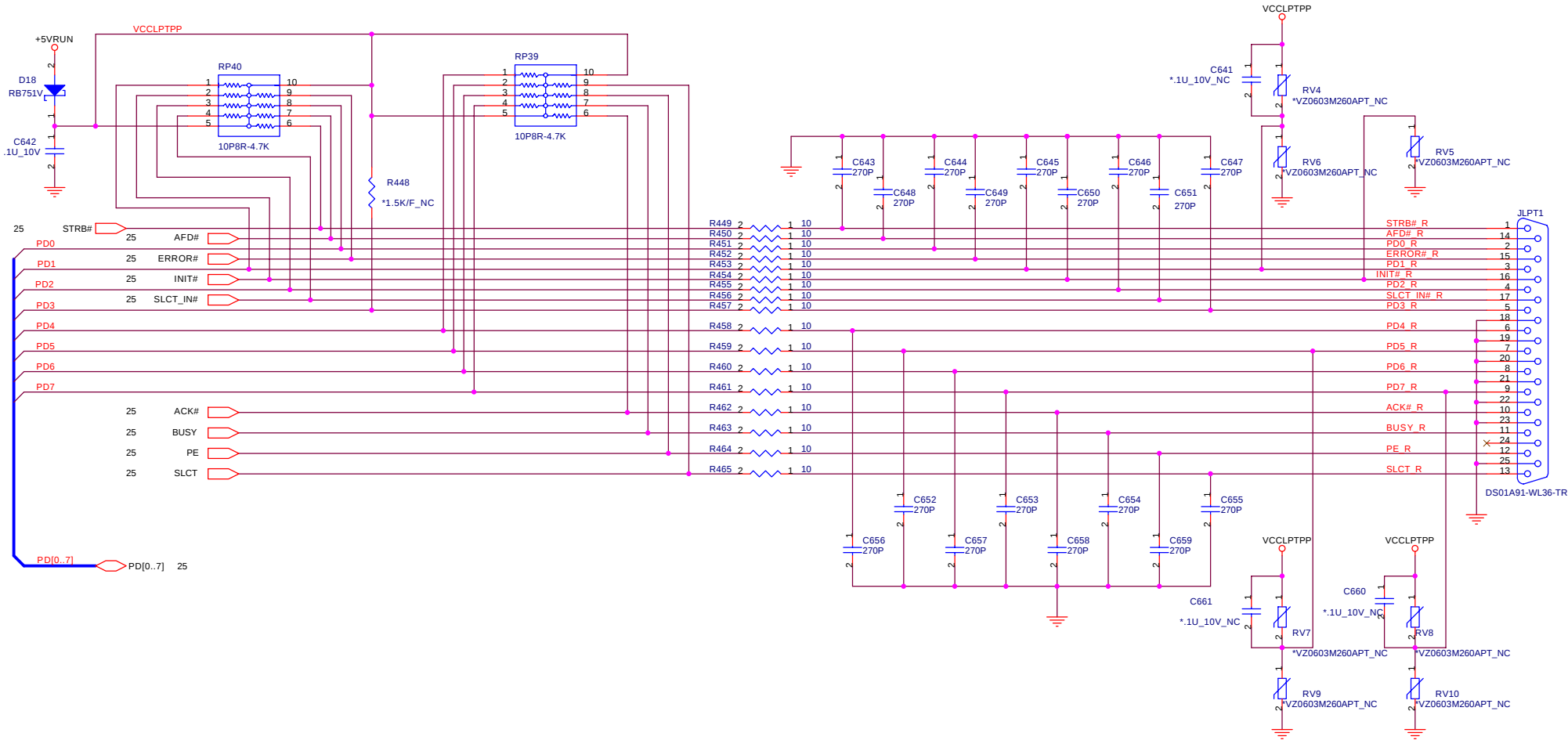


Title					Ultra I/O Controller LPC47N254(GPIO/KB/MISC/FLASH)				
Size		Document Number Tahiti(DM3L)				Rev 1A			
Date:		星期二, 三月 29, 2005				Sheet		26 of 49	



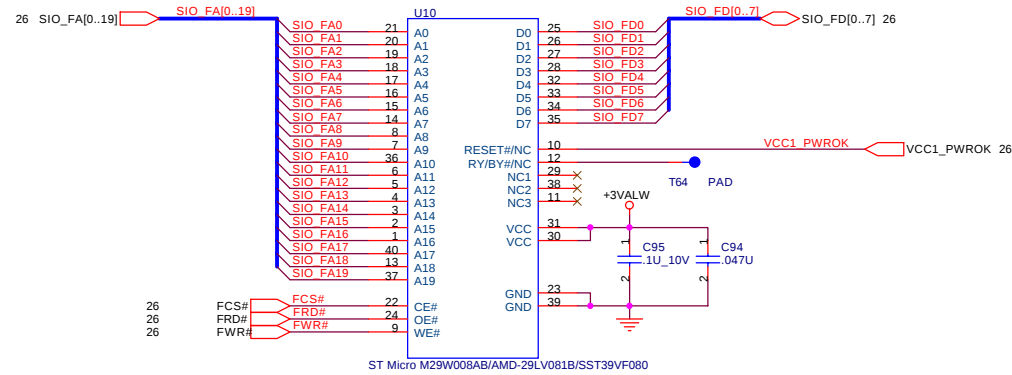
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out





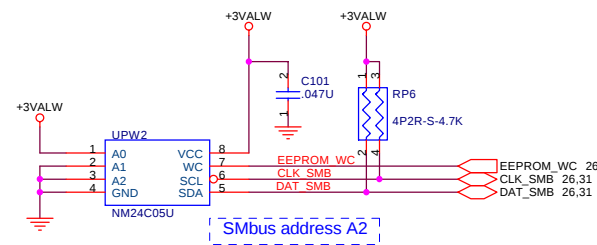
BIOS FLASH MEMORY

8Mbit (1M Byte), ISN'T PLCC TYPE



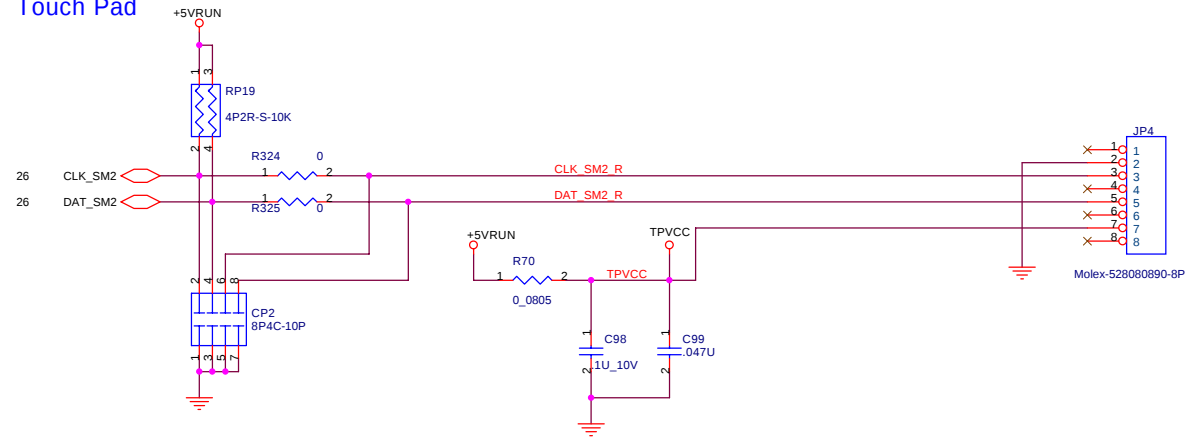
AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

- 1.AMD-29LV081B require MAX 500ns Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK

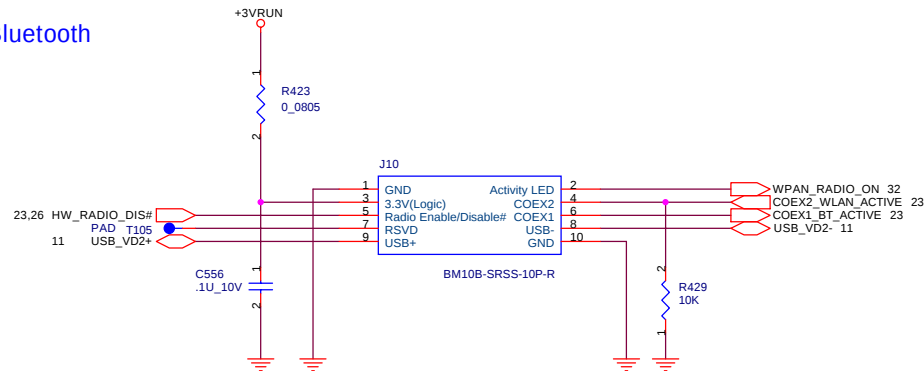


User Password

Touch Pad



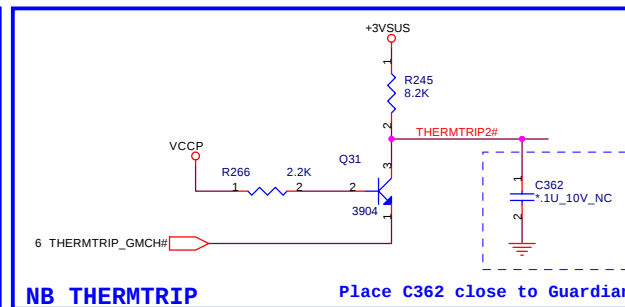
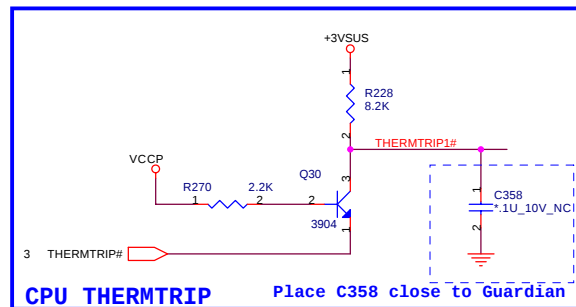
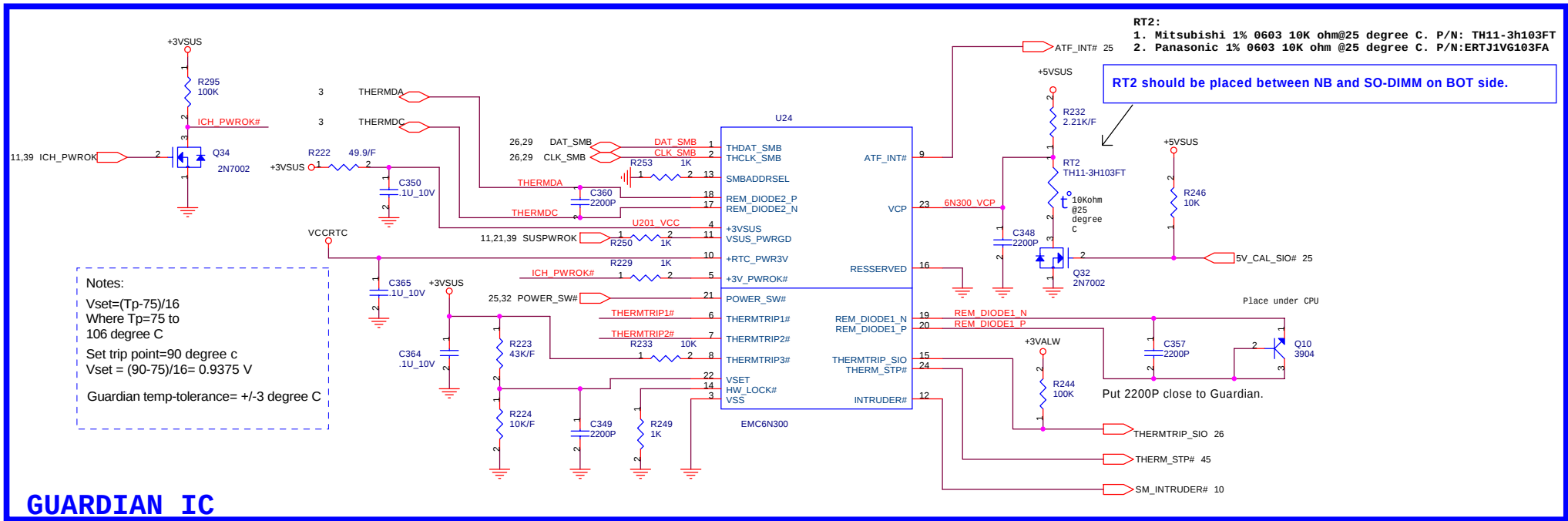
Bluetooth

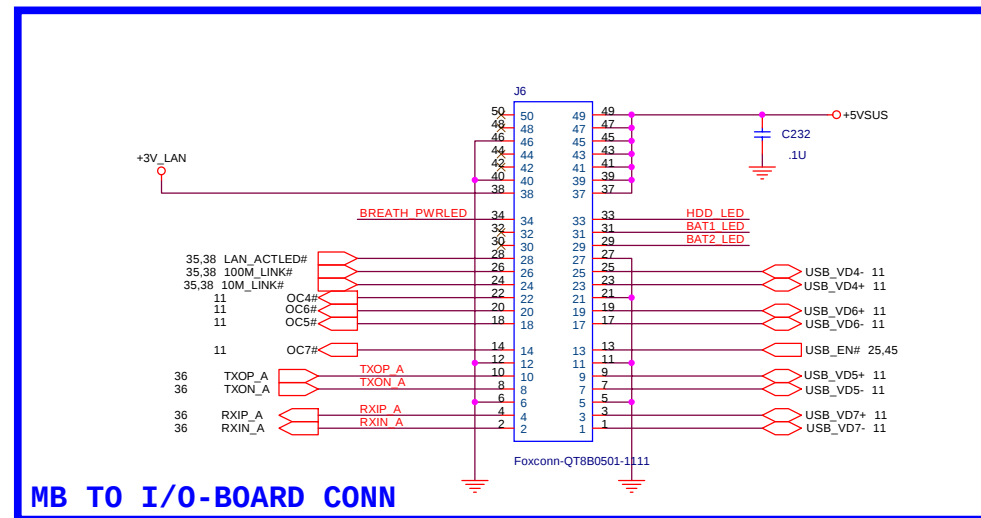
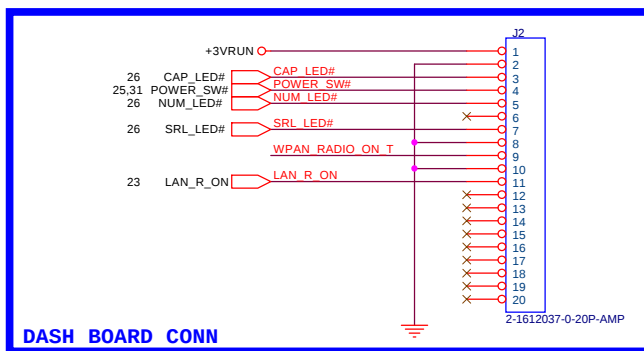
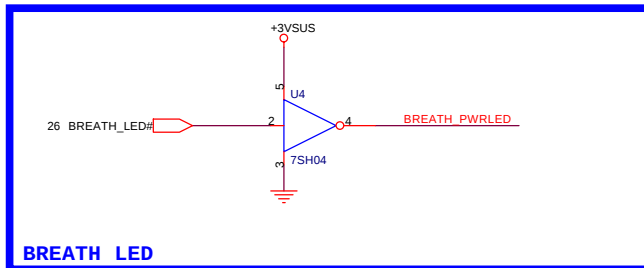
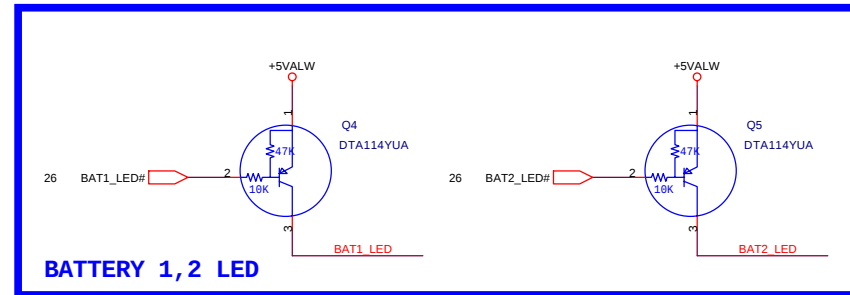
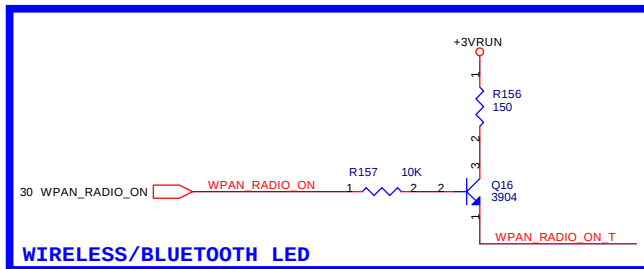
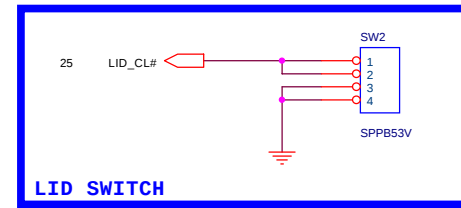
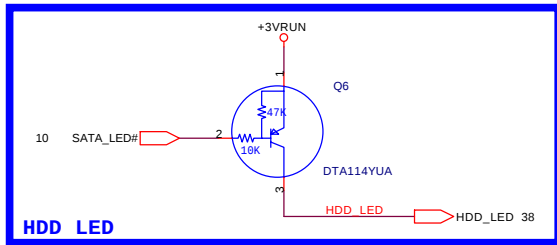


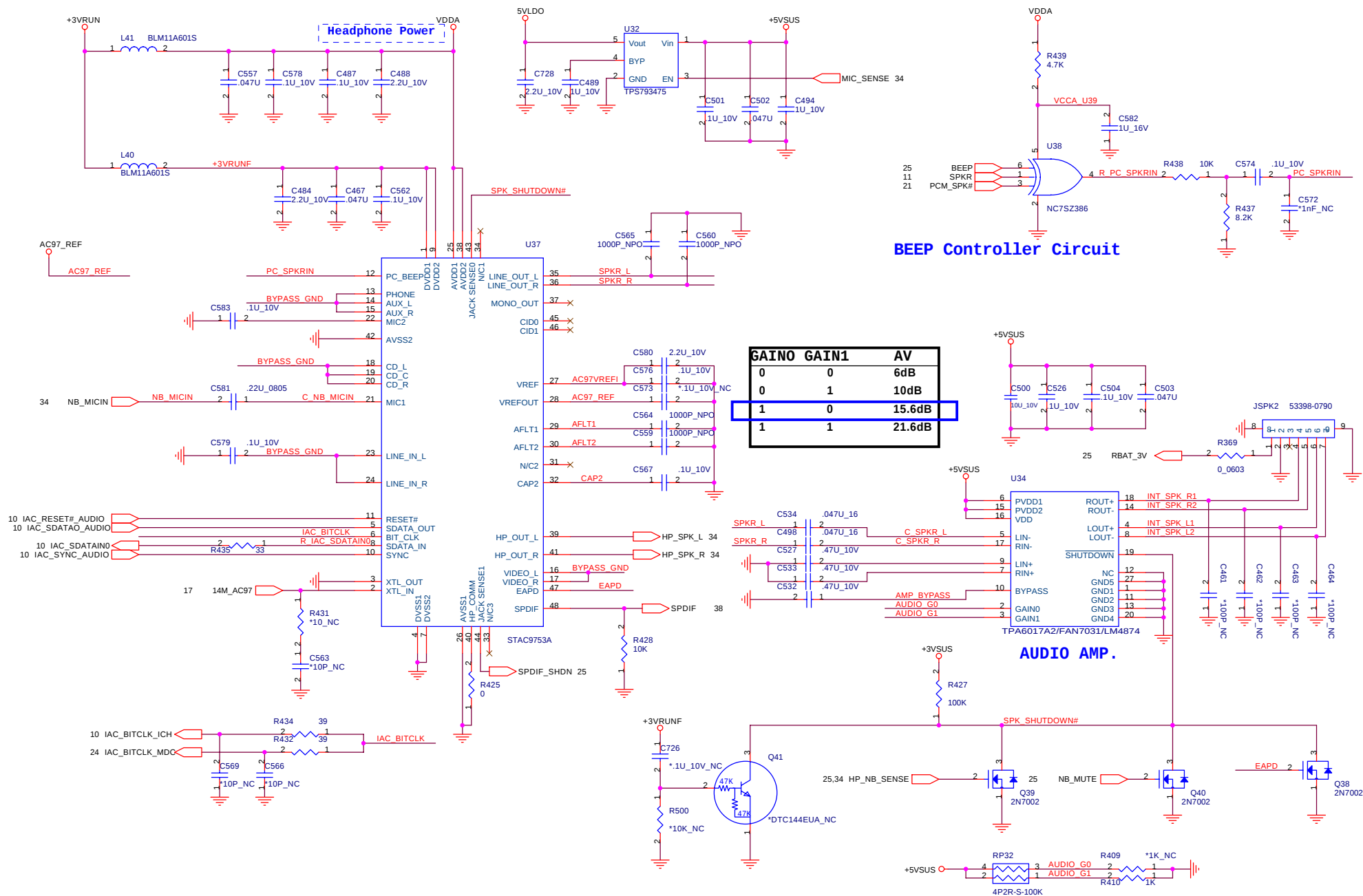
Title TOUCH PAD & BULE TOOTH

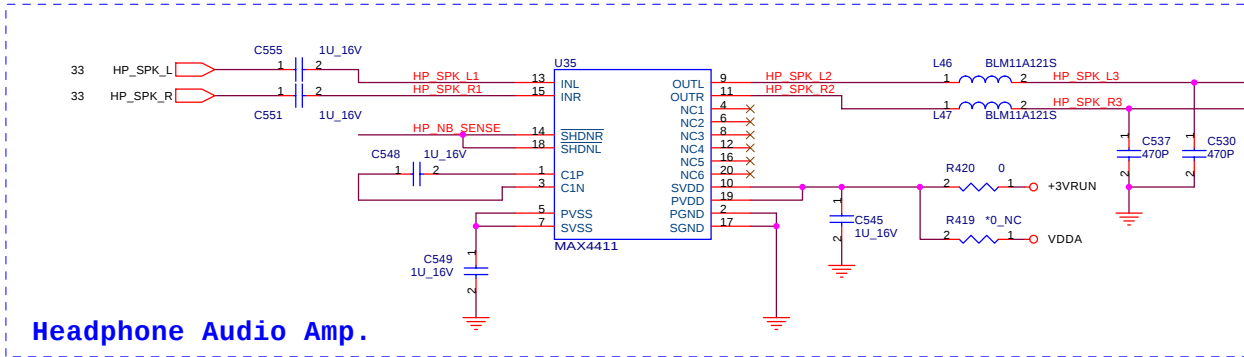
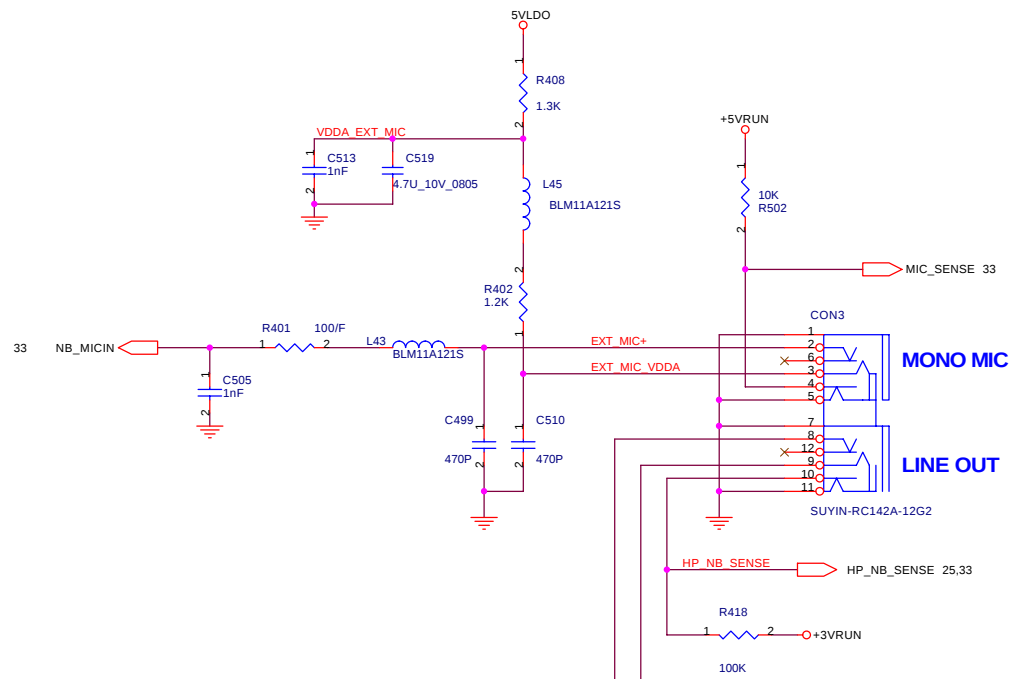
Size Document Number Tahiti(DM3L) Rev 1A

Date: 星期二, 三月 29, 2005 Sheet 30 of 49

[illegible]

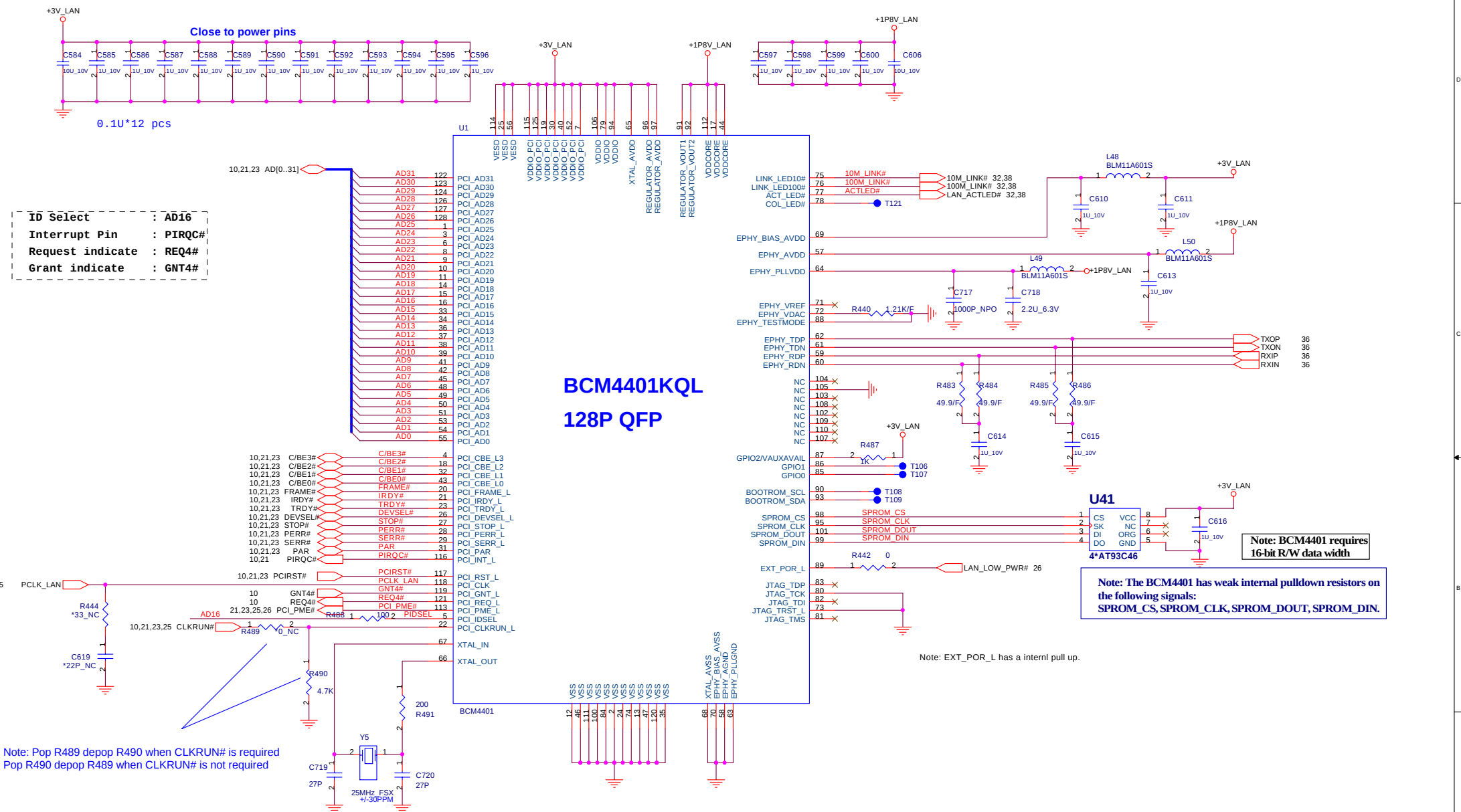






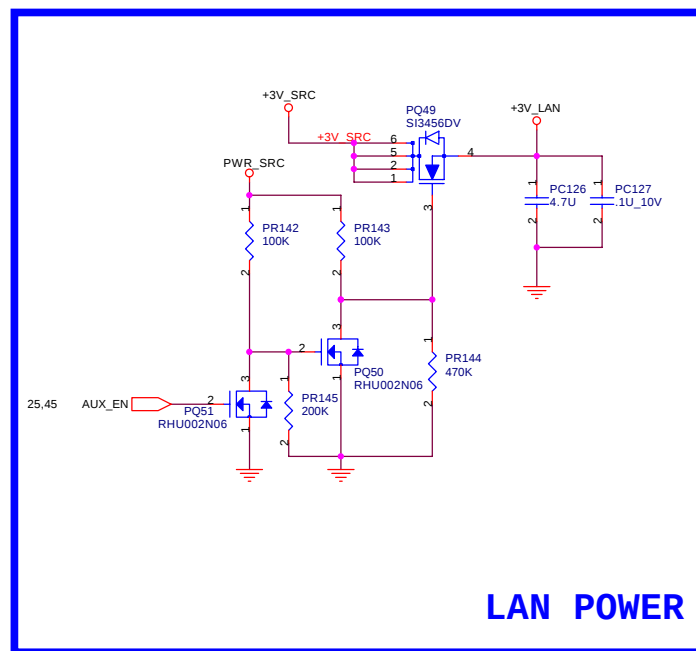
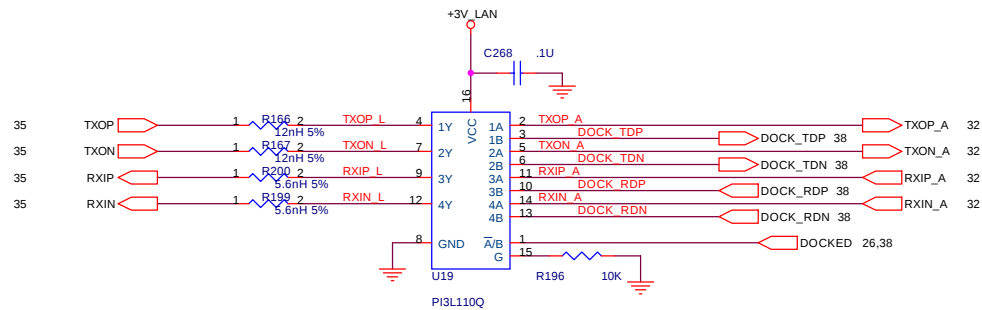
LAN - BCM4401KFB (10/100M)

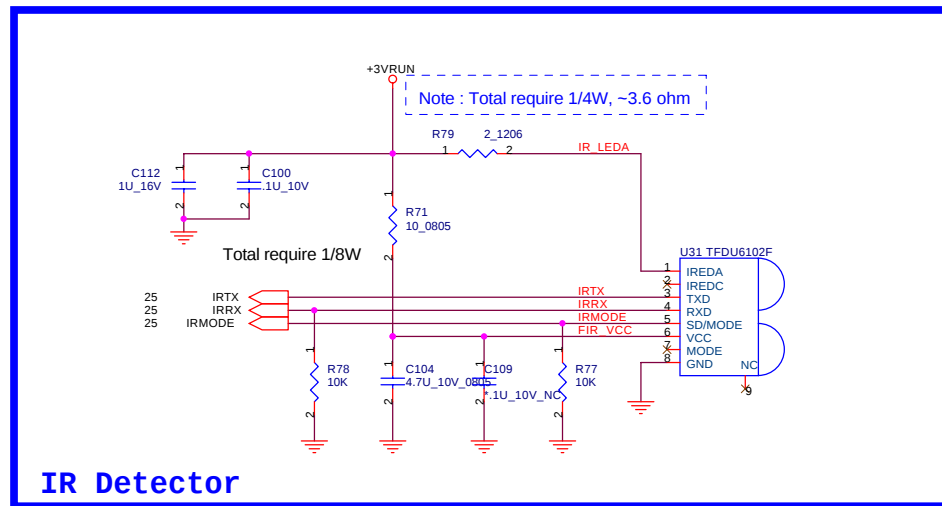
BCM4401 - -10/100

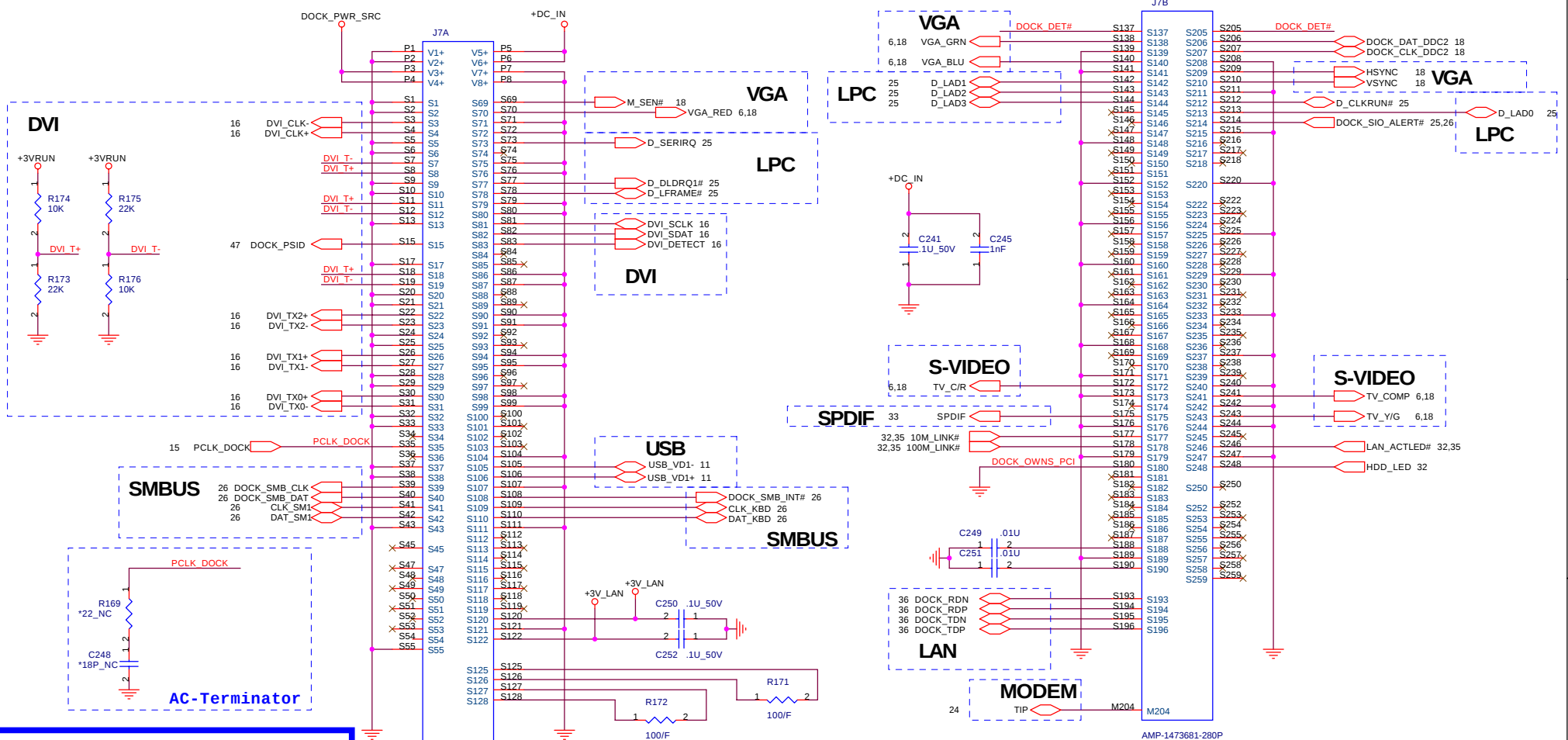


QUANTA
COMPUTER

Title				BCM4401 100/10 LAN			
Size		Document Number Tahiti(DM3L)					Rev 1A
Date:		星期三, 二月 29, 2005		Sheet		35	of 49







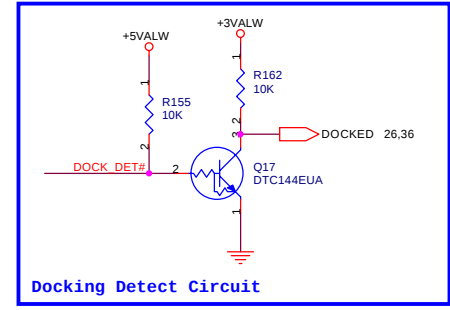
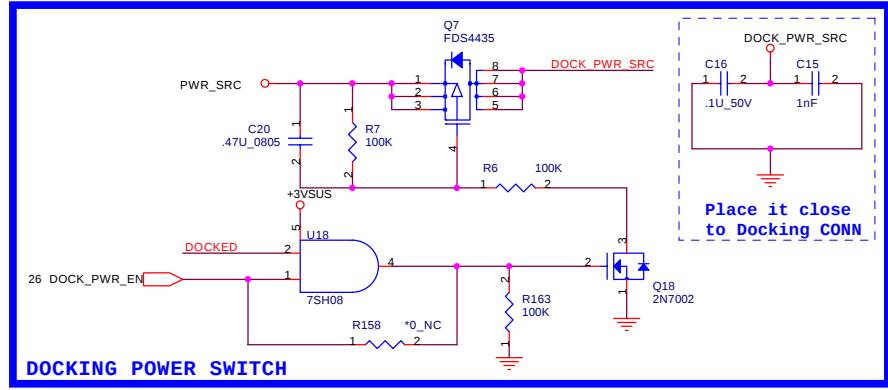
SMBUS ADDRESS :

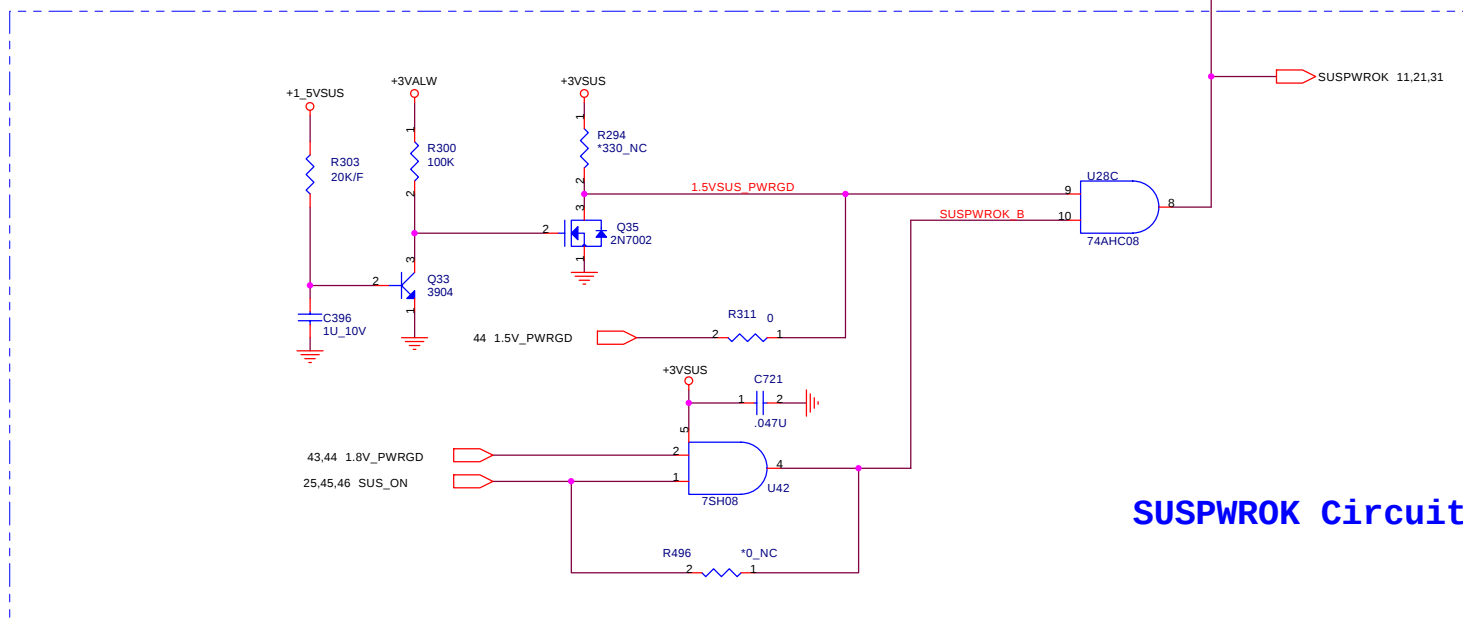
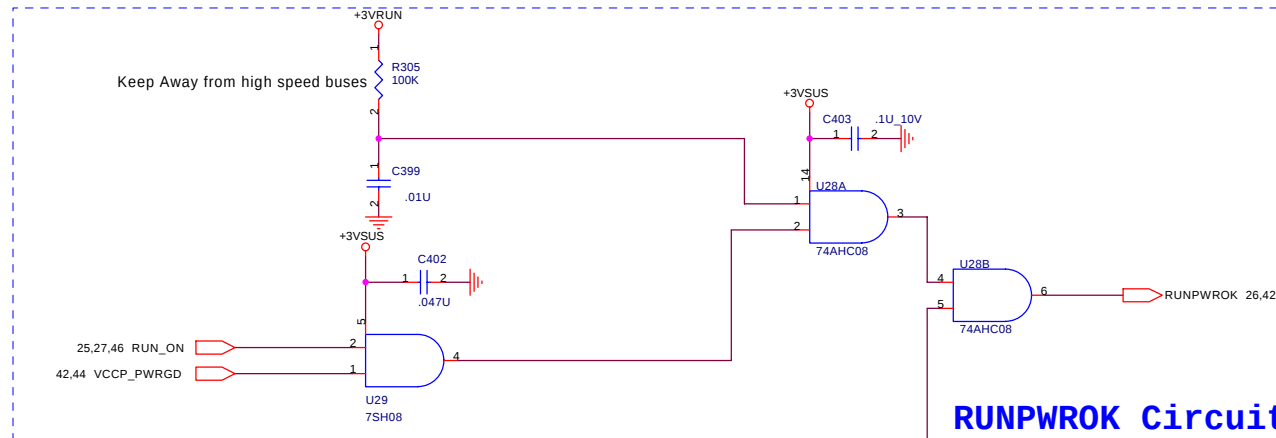
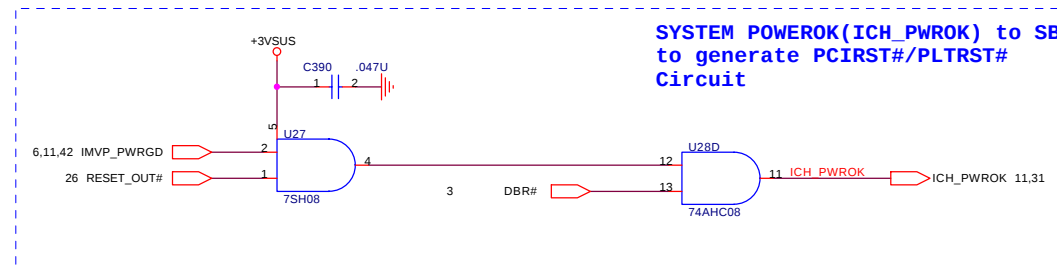
DOCK/APR Microprocessor -- 74H

DOCK USB/IDE Interface(FX2) -- 72H

DOCK Smbus Battery 16h Charger 12h IDE I/F 70h D-BAY

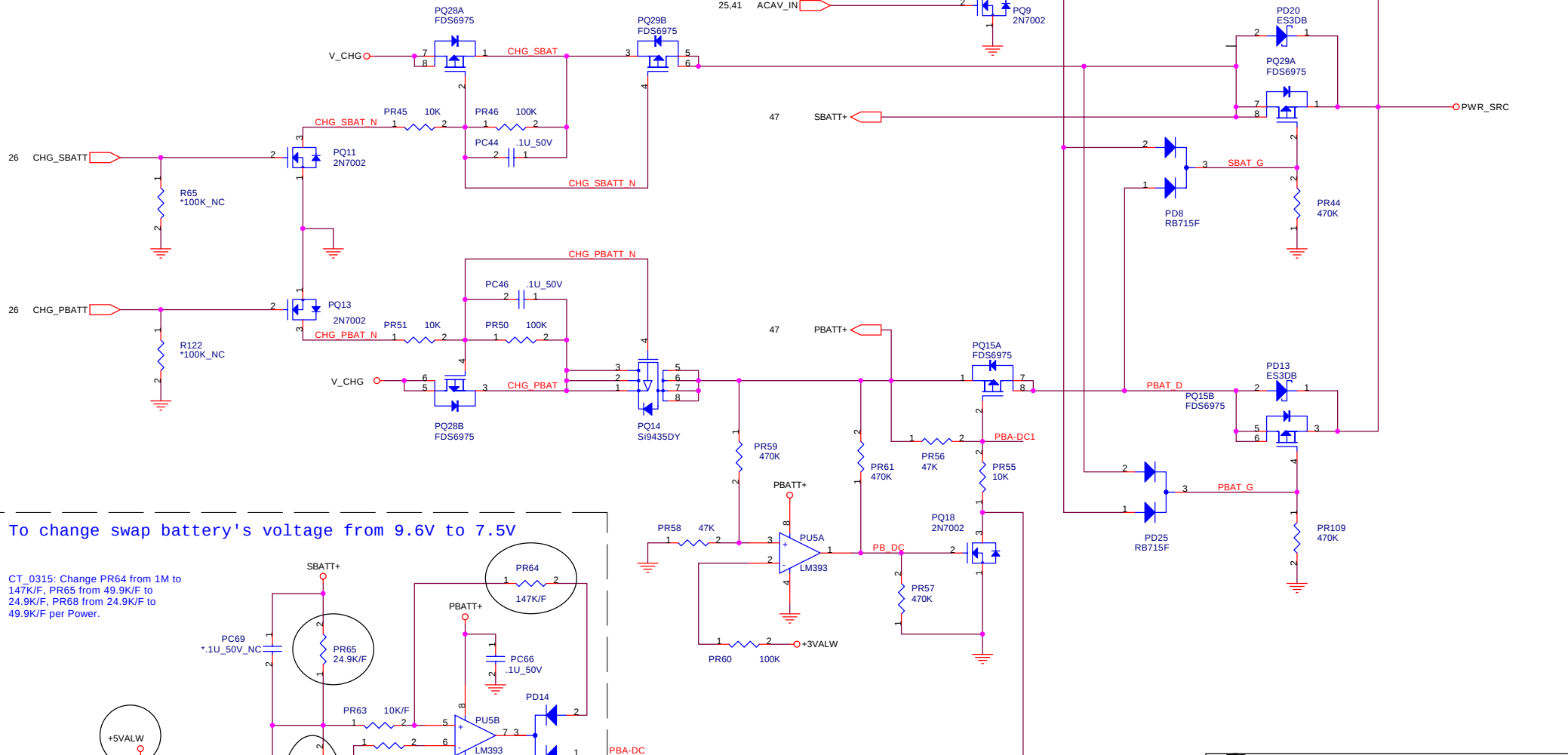
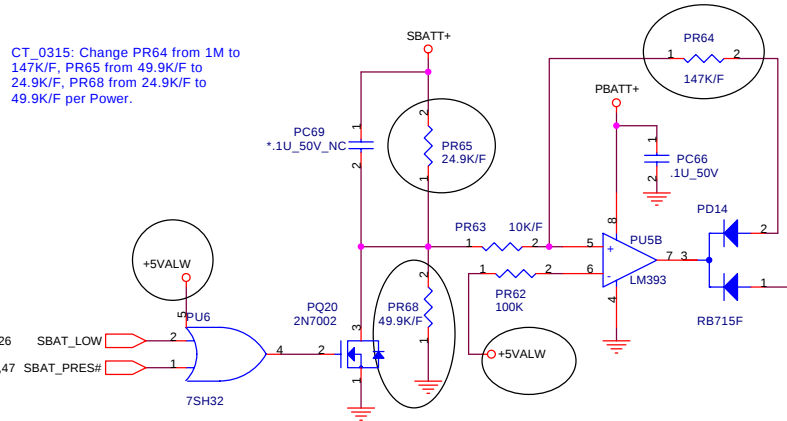
72h SIO 48h

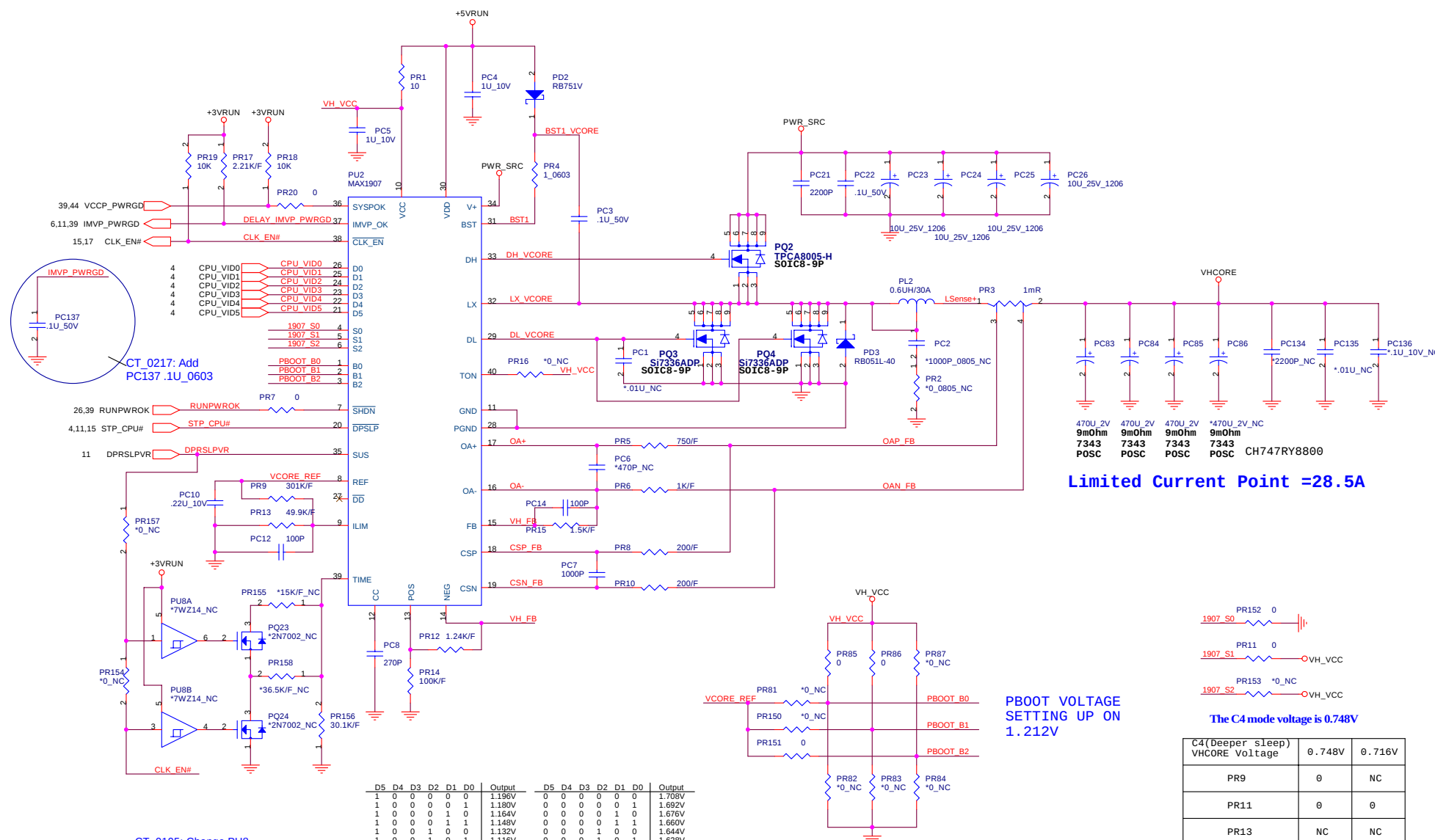




To change swap battery's voltage from 9.6V to 7.5V

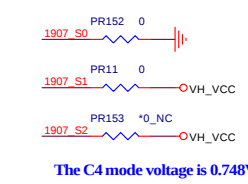
CT_0315: Change PR64 from 1M to 147K/F, PR65 from 49.9K/F to 24.9K/F, PR68 from 24.9K/F to 49.9K/F per Power.





Limited Current Point =28.5A

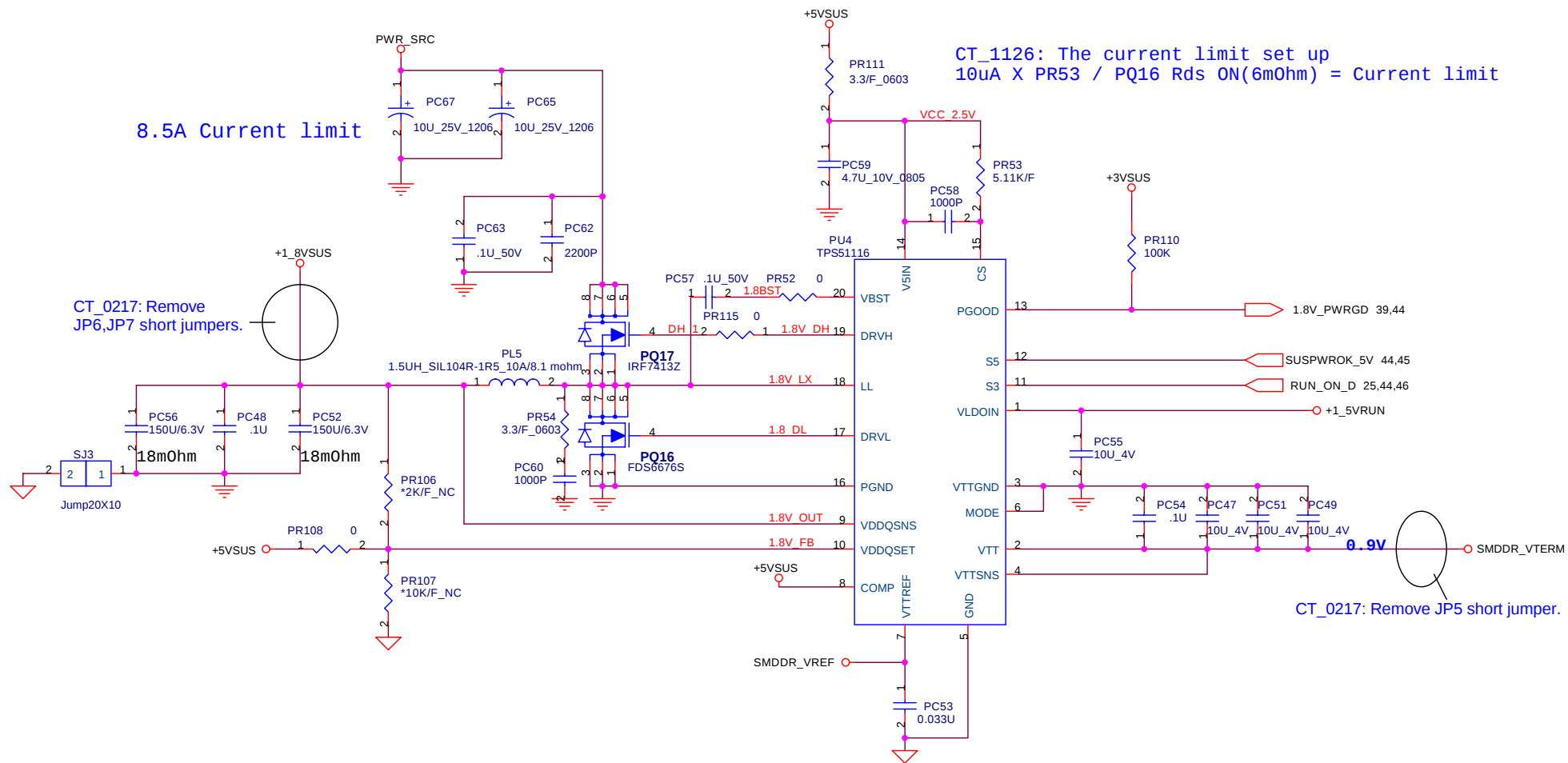
PBOOT VOLTAGE
SETTING UP ON
1.212V



The C4 mode voltage is 0.748V

C4(deeper sleep) VHCORE Voltage	0.748V	0.716V
PR9	0	NC
PR11	0	0
PR13	NC	NC

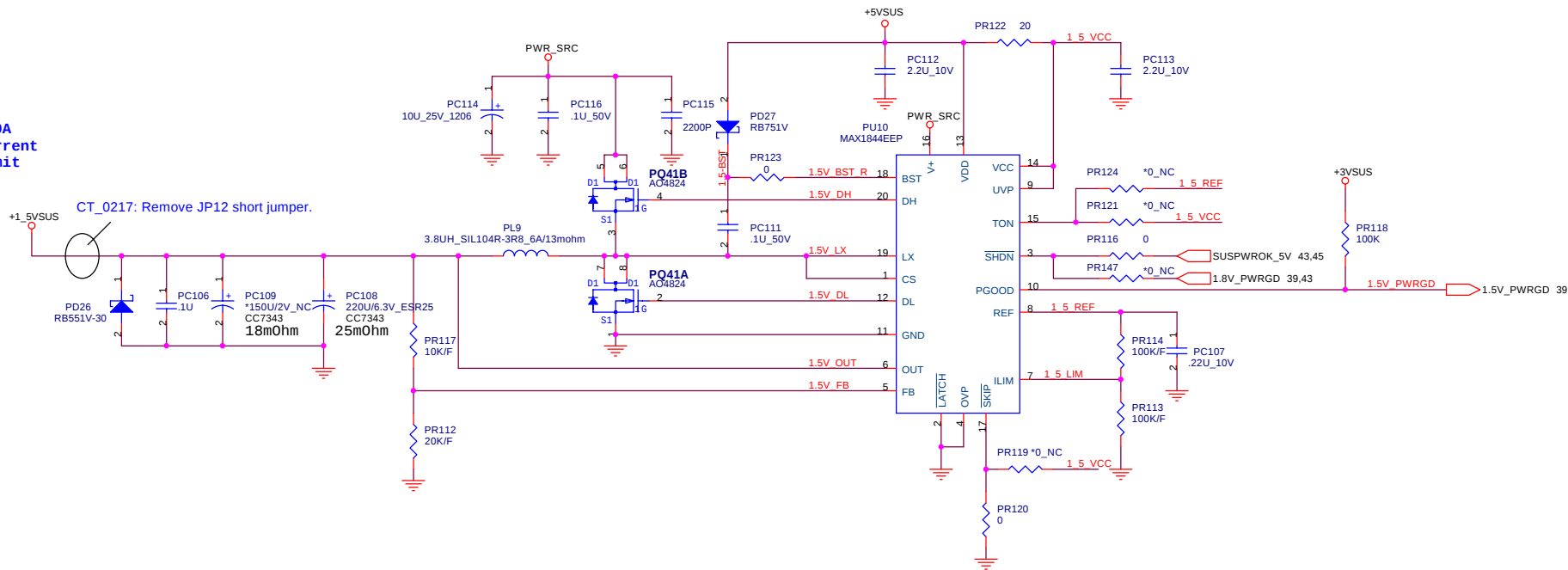
D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V



Title			
1.8V, 0.9V			
Size	Document Number		Rev
	Tahiti(DM3L)		1A
Date:	星期二, 三月 29, 2005	Sheet	43 of 49

5.0A
Current
Limit

CT_0217: Remove JP12 short jumper.



8.6A Current Limit

CT_0217: Remove
JP2,JP3 short jumpers.

