COMPAL CONFIDENTIAL

MODEL NAME : *VAW30*

PCB NO : *LA-9832P (DA8000XL000)*

BOM P/N : *4319M931L01*

GPIO MAP: X.X

Alpine 14"

Haswell ULT

2013-08-23(Gerber)

REV : 1.0

@ : Nopop Component

1@ : M/B SPI ROM

TAA@ : TAA/B SPI ROM

CONN@ : Connector Component

DIS@ : Discrete Pop Component

UMA@ : UMA Pop Component

EMI@ : EMI Component

ESD@ : ESD Component

RF@ : RF Component

XDP@ : XDP Component

eTP@ : TS eTP Component

NeTP@ : TS non - eTP Component

76_U3@ : USB 3.0 Redriver

: Short_Pad

Interleaved Memory

MB PCB

Part Number	Description
DAXXXXXXXXX	PCB 0LD LA-9832P REV1 M/B DIS

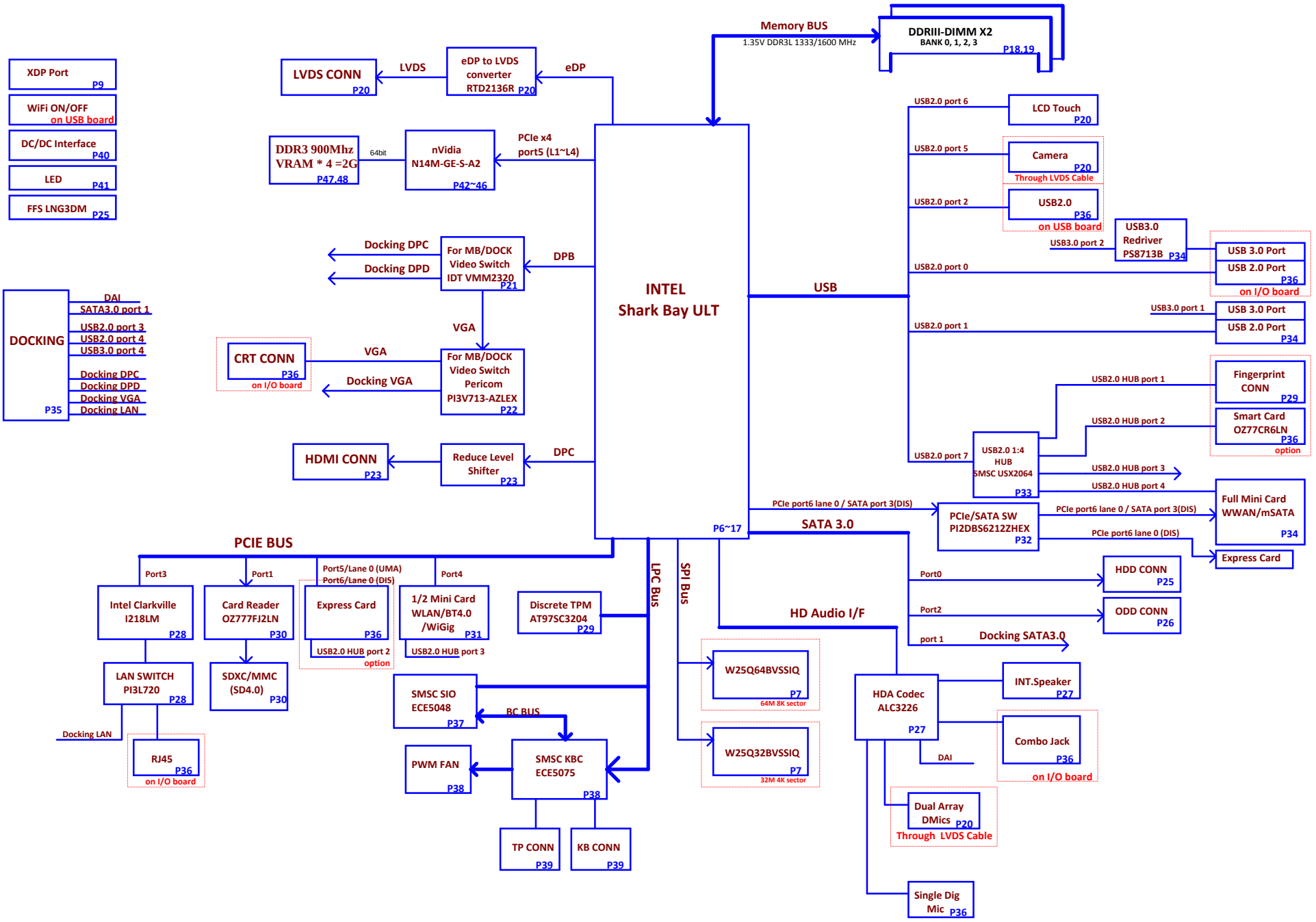
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Cover Sheet

Size | Document Number: LA-9832P | Rev: 0.5

Date: Thursday, August 15, 2013 | Sheet 1 of 64



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: Block Diagram		
Size	Document Number: LA-9832P	Rev: 0.5
Date: Thursday, June 13, 2013	Sheet 2 of 64	

POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

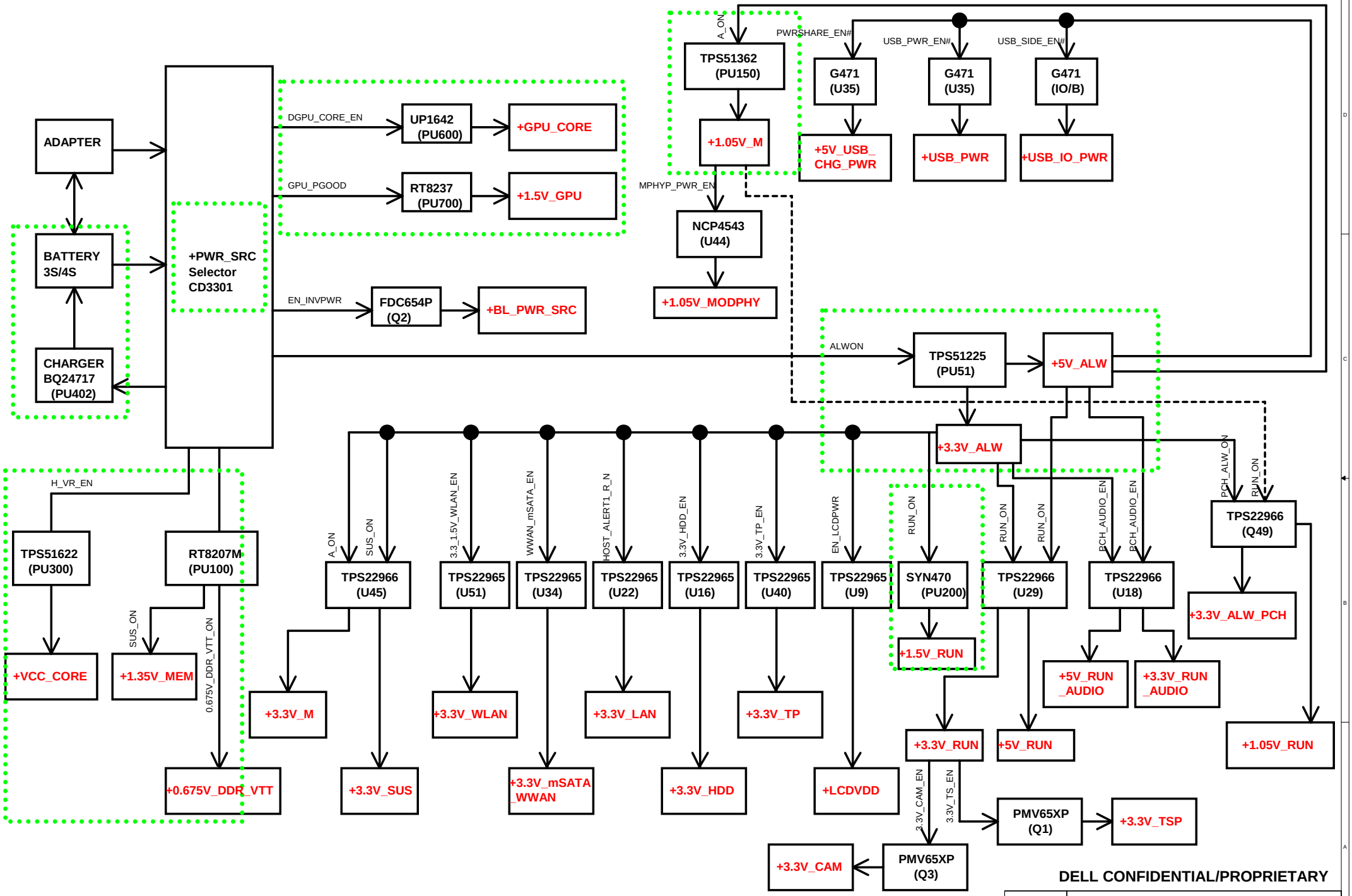
power plane / State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->MB-->LEFT
	USB3.0 2		USB3.0-->IOB-->Rear Right
PCIE 1	USB3.0 3		PCIE1-->MMI PCIE
PCIE 2	USB3.0 4		USB3.0-->Docking
PCIE 3			LOM
PCIE 4			WLAN (WiGi)
PCIE 5			GPU(DIS)/Express card(UMA)
PCIE 6		SATA 3	WWAN(mSATA)/Express card(PCIE)
		SATA 2	ODD
		SATA 1	HDD
		SATA 0	DOCK

	USB PORT#	DESTINATION
HSW ULT	0	IO (Right)
	1	JUSB1(Left)
	2	USB DB(Rear Left)
	3	DOCK
	4	Dock
	5	WebCAM
	6	Touch Screen
	7	USB HUB

Compal Electronics, Inc.
Title: Index and Config.
Size | Document Number: LA-9832P | Rev: 0.5
Date: Thursday, June 13, 2013 | Sheet 3 of 64



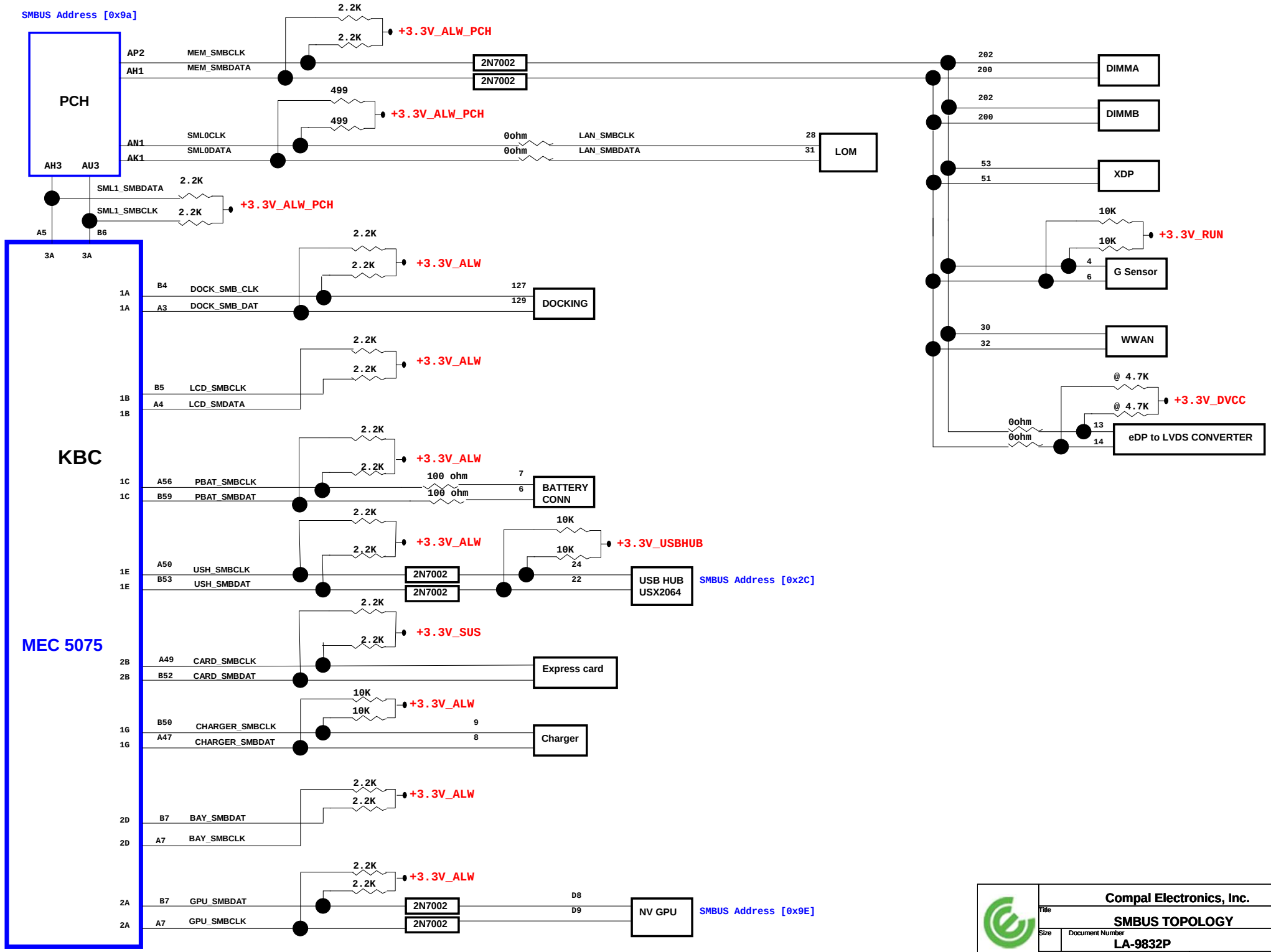
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Power Rail

Size | Document Number: LA-9832P | Rev: 0.5

Date: Thursday, June 13, 2013 | Sheet 4 of 64



Compal Electronics, Inc.	
Title	SMBUS TOPOLOGY
Size	Document Number: LA-9832P
Rev	0.5
Date:	Thursday, June 13, 2013
Sheet	5 of 64

+RTC_CELL

RC1 330K_0402_1%~D — PCH_INTVRMEN — @RC2 330K_0402_1%~D

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

+3.3V_ALW_PCH

@RC3 — PCH_AZ_SDOUT — 1K_0402_1%~D

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

+1.05V_M — RC16 0_0603_5%~D

+1.05V_M_JTAG — RC17 51_0402_1%~D — PCH_JTAG_TDI
RC18 51_0402_1%~D — PCH_JTAG_TDO
RC20 51_0402_1%~D — PCH_JTAG_TMS
@RC10 1K_0402_1%~D — PCH_JTAG_JTAGX
@RC22 51_0402_1%~D — PCH_JTAG_TCK

reference 479493 figure 7-1

HDA for Codec

27 PCH_AZ_CODEC_SDOUT — RC23 33_0402_5%~D — PCH_AZ_SDOUT
27 PCH_AZ_CODEC_SYNC — RC24 33_0402_5%~D — PCH_AZ_SYNC
27 PCH_AZ_CODEC_RST# — RC25 33_0402_5%~D — PCH_AZ_RST#
27 PCH_AZ_CODEC_BITCLK — RC26 33_0402_5%~D — PCH_AZ_BITCLK

@C3 22P_0402_50V8J_D — EMI

CC1 15P_0402_50V8J — PCH_RTCX1_R — RC4 @ 0_0402_5% — PCH_RTCX1
YC1 32.768KHZ_12.5PF_9H03200031
CC2 15P_0402_50V8J — PCH_RTCX2
RC5 10M_0402_5%~D

+RTC_CELL
RC7 1M_0402_5%~D
RC8 20K_0402_5%~D
RC6 20K_0402_5%~D

INTRUDER# — PCH_INTVRMEN — SRTCRST# — PCH_RTCRST#
9 PCH_RTCRST#

@ME1 SHORT PADS~D — CC3 1U_0402_6.3V6K~D
@CMOS1 SHORT PADS~D — CC4 1U_0402_6.3V6K~D
CMOS place near DIMM

27 PCH_AZ_CODEC_SDIN0
37 ME_FWP — RC9 1K_0402_1%~D — PCH_AZ_SDOUT

9 PCH_JTAG_TRST#
9 PCH_JTAG_TCK
9 PCH_JTAG_TDI
9 PCH_JTAG_TDO
9 PCH_JTAG_TMS
9 PCH_JTAG_JTAGX

UC1E — HASWELL_MCP_E

AW5	RTCX1	RTC	
AY5	RTCX2		
AU6	INTRUDER		
AV7	INTVRMEN		
AV6	SRTCRST		
AU7	RTCRST		
AW8	HDA_BCLK/I2S0_SCLK	AUDIO	
AV11	HDA_SYNC/I2S0_SFRM		
AU8	HDA_RST/I2S_MCLK		
AY10	HDA_SDI0/I2S0_RXD		
AU12	HDA_SDI1/I2S1_RXD		
AU11	HDA_SDO/I2S0_TXD		
AW10	HDA_DOCK_EN/I2S1_TXD		
AV10	HDA_DOCK_RST/I2S1_SFRM		
AY6	I2S1_SCLK		
AU62	PCH_TRST	JTAG	
AE62	PCH_TCK		
AD61	PCH_TDI		
AE61	PCH_TDO		
AD62	PCH_TMS		
AL11	RSVD		
AC4	RSVD		
AE63	JTAGX		
AV2	RSVD		

5 OF 19 — Rev1p2

SATA_RN0/PERN6_L3 — J5 — SATA_PRX_DKTX_N0_C 35
SATA_RP0/PERP6_L3 — H5 — SATA_PRX_DKTX_P0_C 35
SATA_TN0/PETN6_L3 — B15 — SATA_PTX_DKRX_N0_C 35
SATA_TP0/PETP6_L3 — A15 — SATA_PTX_DKRX_P0_C 35
DOCK

SATA_RN1/PERN6_L2 — J8 — SATA_PRX_DTX_N1_C 25
SATA_RP1/PERP6_L2 — H8 — SATA_PRX_DTX_P1_C 25
SATA_TN1/PETN6_L2 — A17 — SATA_PTX_DRX_N1_C 25
SATA_TP1/PETP6_L2 — B17 — SATA_PTX_DRX_P1_C 25
SATA HDD

SATA_RN2/PERN6_L1 — J6 — SATA_ODD_PRX_DTX_N2_C 26
SATA_RP2/PERP6_L1 — H6 — SATA_ODD_PRX_DTX_P2_C 26
SATA_TN2/PETN6_L1 — B14 — SATA_ODD_PTX_DRX_N2_C 26
SATA_TP2/PETP6_L1 — C15 — SATA_ODD_PTX_DRX_P2_C 26
ODD

SATA_RN3/PERN6_L0 — F5 — EXP_PRX_EXPTX_N6 — EXP_PRX_EXPTX_N6 32
SATA_RP3/PERP6_L0 — E5 — EXP_PRX_EXPTX_P6 — EXP_PRX_EXPTX_P6 32
SATA_TN3/PETN6_L0 — C17 — EXP_PTX_EXPRX_N6 — EXP_PTX_EXPRX_N6 32
SATA_TP3/PETP6_L0 — D17 — EXP_PTX_EXPRX_P6 — EXP_PTX_EXPRX_P6 32
Express card/mSATA

PCH Rx side need use strap pin to update PCIE +/-

SATA0GP/GPIO34 — V1 — MPCIE_RST# — MPCIE_RST# 31
SATA1GP/GPIO35 — U1 — HDD_DET# — HDD_DET# 25
SATA2GP/GPIO36 — V6 — PCH_GPIO36 — PCH_GPIO36 9
SATA3GP/GPIO37 — AC1 — MCARD_PCIE_MSATA# — MCARD_PCIE_MSATA# 37

SATA_IREF — A12 — SATA_IREF — 2 — @ — 1 — RC14 0_0402_5% — +PCH_ASATA3PLL
RSVD — L11
RSVD — K10
RSVD — C12
SATA_RCOMP — U3 — SATA_COMP
SATALED — SATA_ACT# — SATA_ACT# 41

+3.3V_RUN
HDD_DET# — RC11 100K_0402_5%~D
MPCIE_RST# — RC138 10K_0402_5%~D
MCARD_PCIE_MSATA# — RC12 10K_0402_5%~D

Shark_Bay_ULT_PDG 0.9:
the sampled value for the GPIO corresponding to the particular port during boot time.
SATA3GP/GPIO37-->SATAP3:
1:SATA
0:PCIe

SATA_IREF

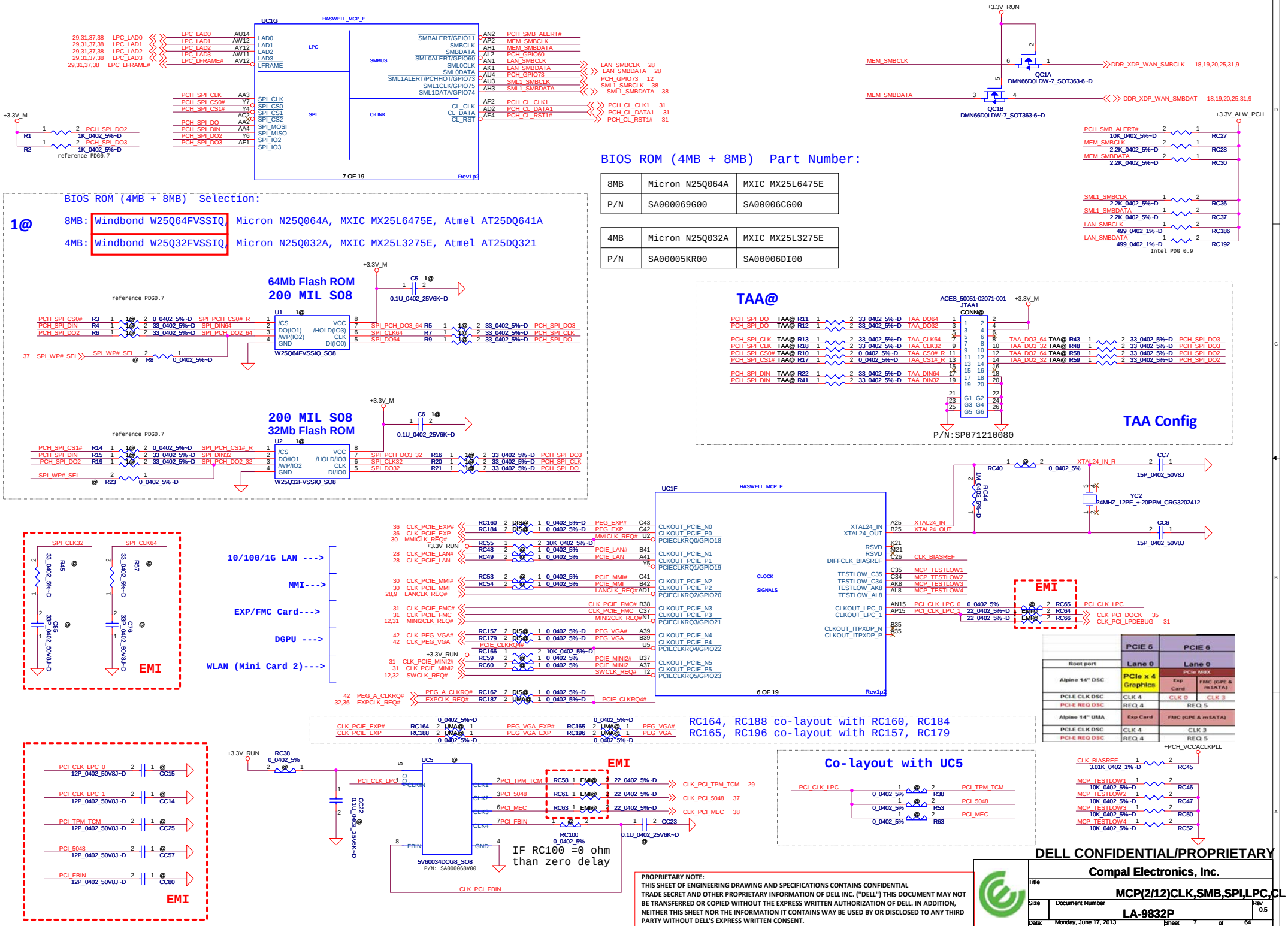
SATA_IREF min 4mil trace at break-out and 12-15mil trace with <0.2 ohms and length total <= 500mils. Requires 12 mils isolation from all High Speed IO and clocks.

SATA Impedance Compensation

+PCH_ASATA3PLL
SATA_COMP — RC19 3.01K_0402_1%~D
SATA_RCOMP min 4mil trace at break-out and 12-15mil trace with <0.2 ohms and length total <= 500mils. Requires 12 mils isolation from all High Speed IO and clocks.
reference FFRD sch 0.5

Compal Electronics, Inc.

Title: MCP(1/12) RTC,SATA,HDA,JTAG
Size: — Document Number: LA-9832P — Rev: 0.5
Date: Monday, June 17, 2013 — Sheet 6 of 64


BIOS ROM (4MB + 8MB) Selection:
1@
8MB: Windbond W25Q64FVSSIQ, Micron N25Q064A, MXIC MX25L6475E, Atmel AT25DQ641A
4MB: Windbond W25Q32FVSSIQ, Micron N25Q032A, MXIC MX25L3275E, Atmel AT25DQ321
64Mb Flash ROM
200 MIL SO8
200 MIL SO8
32Mb Flash ROM
W25Q64FVSSIQ_SO8
W25Q32FVSSIQ_SO8
BIOS ROM (4MB + 8MB) Part Number:
8MB | Micron N25Q064A | MXIC MX25L6475E
P/N | SA000069G00 | SA00006CG00
4MB | Micron N25Q032A | MXIC MX25L3275E
P/N | SA00005KR00 | SA00006DI00
TAA@
TAA Config
P/N:SP071210080
EMI
10/100/1G LAN --->
MMI--->
EXP/FMC Card--->
DGPU --->
WLAN (Mini Card 2)--->
RC164, RC188 co-layout with RC160, RC184
RC165, RC196 co-layout with RC157, RC179
Co-layout with UC5
IF RC100 =0 ohm than zero delay
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
MCP(2/12)CLK,SMB,SPI,LPC,CL
LA-9832P
Monday, June 17, 2013

DDR interleave routing

UC1C — HASWELL_MCP_E — DDR CHANNEL A — 3 OF 19 — Rev1p2

18 DDR_A_D[0..15]	DDR_A_D0	AH63	SA_DQ0	SA_CLK#0	AU37	M_CLK_DDR#0	M_CLK_DDR#0 18
	DDR_A_D1	AH62	SA_DQ1	SA_CLK0	AV37	M_CLK_DDR0	M_CLK_DDR0 18
	DDR_A_D2	AK63	SA_DQ2	SA_CLK#1	AW36	M_CLK_DDR#1	M_CLK_DDR#1 18
	DDR_A_D3	AK62	SA_DQ3	SA_CLK1	AY36	M_CLK_DDR1	M_CLK_DDR1 18
	DDR_A_D4	AH61	SA_DQ4				
	DDR_A_D5	AH60	SA_DQ5	SA_CKE0	AU43	DDR_CKE0_DIMMA	DDR_CKE0_DIMMA 18
	DDR_A_D6	AK61	SA_DQ6	SA_CKE1	AW43	DDR_CKE1_DIMMA	DDR_CKE1_DIMMA 18
	DDR_A_D7	AK60	SA_DQ7	SA_CKE2	AY42		
	DDR_A_D8	AM63	SA_DQ8	SA_CKE3	AY43		
	DDR_A_D9	AM62	SA_DQ9				
	DDR_A_D10	AP63	SA_DQ10	SA_CS#0	AP33	DDR_CS0_DIMMA#	DDR_CS0_DIMMA# 18
	DDR_A_D11	AP62	SA_DQ11	SA_CS#1	AR32	DDR_CS1_DIMMA#	DDR_CS1_DIMMA# 18
	DDR_A_D12	AM61	SA_DQ12				
	DDR_A_D13	AM60	SA_DQ13	SA_ODT0	AP32		
	DDR_A_D14	AP61	SA_DQ14				
	DDR_A_D15	AP60	SA_DQ15	SA_RAS	AY34	DDR_A_RAS#	DDR_A_RAS# 18
19 DDR_B_D[0..15]	DDR_B_D0	AR58	SA_DQ16	SA_WE	AW34	DDR_A_WE#	DDR_A_WE# 18
	DDR_B_D1	AR58	SA_DQ17	SA_CAS	AU34	DDR_A_CAS#	DDR_A_CAS# 18
	DDR_B_D2	AM57	SA_DQ18				
	DDR_B_D3	AK57	SA_DQ19	SA_BA0	AU35	DDR_A_BS0	DDR_A_BS0 18
	DDR_B_D4	AL58	SA_DQ20	SA_BA1	AV35	DDR_A_BS1	DDR_A_BS1 18
	DDR_B_D5	AK58	SA_DQ21	SA_BA2	AY41	DDR_A_BS2	DDR_A_BS2 18
	DDR_B_D6	AR57	SA_DQ22				DDR_A_MA[0..15] 18
	DDR_B_D7	AN57	SA_DQ23	SA_MA0	AU36	DDR_A_MA0	
	DDR_B_D8	AP55	SA_DQ24	SA_MA1	AY37	DDR_A_MA1	
	DDR_B_D9	AR55	SA_DQ25	SA_MA2	AR38	DDR_A_MA2	
	DDR_B_D10	AM54	SA_DQ26	SA_MA3	AP36	DDR_A_MA3	
	DDR_B_D11	AK54	SA_DQ27	SA_MA4	AU39	DDR_A_MA4	
	DDR_B_D12	AL55	SA_DQ28	SA_MA5	AR36	DDR_A_MA5	
	DDR_B_D13	AK55	SA_DQ29	SA_MA6	AV40	DDR_A_MA6	
	DDR_B_D14	AR54	SA_DQ30	SA_MA7	AW39	DDR_A_MA7	
	DDR_B_D15	AN54	SA_DQ31	SA_MA8	AY39	DDR_A_MA8	
18 DDR_A_D[16..31]	DDR_A_D16	AY58	SA_DQ32	SA_MA9	AU40	DDR_A_MA9	
	DDR_A_D17	AW58	SA_DQ33	SA_MA10	AP35	DDR_A_MA10	
	DDR_A_D18	AY56	SA_DQ34	SA_MA11	AW41	DDR_A_MA11	
	DDR_A_D19	AW56	SA_DQ35	SA_MA12	AU41	DDR_A_MA12	
	DDR_A_D20	AV58	SA_DQ36	SA_MA13	AR35	DDR_A_MA13	
	DDR_A_D21	AU58	SA_DQ37	SA_MA14	AV42	DDR_A_MA14	
	DDR_A_D22	AV56	SA_DQ38	SA_MA15	AU42	DDR_A_MA15	
	DDR_A_D23	AU56	SA_DQ39				
	DDR_A_D24	AY54	SA_DQ40	SA_DQSN0	AJ61	DDR_A_DQS#0	DDR_A_DQS#[0..1] 18
	DDR_A_D25	AW54	SA_DQ41	SA_DQSN1	AN62	DDR_A_DQS#1	DDR_B_DQS#[0..1] 19
	DDR_A_D26	AY52	SA_DQ42	SA_DQSN2	AM58	DDR_B_DQS#0	
	DDR_A_D27	AW52	SA_DQ43	SA_DQSN3	AM55	DDR_B_DQS#1	DDR_A_DQS#[2..3] 18
	DDR_A_D28	AV54	SA_DQ44	SA_DQSN4	AV57	DDR_A_DQS#2	
	DDR_A_D29	AU54	SA_DQ45	SA_DQSN5	AV53	DDR_A_DQS#3	DDR_B_DQS#[2..3] 19
	DDR_A_D30	AV52	SA_DQ46	SA_DQSN6	AL43	DDR_B_DQS#2	
	DDR_A_D31	AU52	SA_DQ47	SA_DQSN7	AL48	DDR_B_DQS#3	
19 DDR_B_D[16..31]	DDR_B_D16	AK40	SA_DQ48				
	DDR_B_D17	AK42	SA_DQ49	SA_DQSP0	AJ62	DDR_A_DQS0	DDR_A_DQS[0..1] 18
	DDR_B_D18	AM43	SA_DQ50	SA_DQSP1	AN61	DDR_A_DQS1	DDR_B_DQS[0..1] 19
	DDR_B_D19	AM45	SA_DQ51	SA_DQSP2	AN58	DDR_B_DQS0	
	DDR_B_D20	AK45	SA_DQ52	SA_DQSP3	AN55	DDR_B_DQS1	DDR_A_DQS[2..3] 18
	DDR_B_D21	AK43	SA_DQ53	SA_DQSP4	AW57	DDR_A_DQS2	
	DDR_B_D22	AM40	SA_DQ54	SA_DQSP5	AW53	DDR_A_DQS3	DDR_B_DQS[2..3] 19
	DDR_B_D23	AM42	SA_DQ55	SA_DQSP6	AL42	DDR_B_DQS2	
	DDR_B_D24	AM46	SA_DQ56	SA_DQSP7	AL49	DDR_B_DQS3	
	DDR_B_D25	AK46	SA_DQ57				
	DDR_B_D26	AM49	SA_DQ58	SM_VREF_CA	AP49		+SM_VREF_CA
	DDR_B_D27	AK49	SA_DQ59	SM_VREF_DQ0	AR51		+SM_VREF_DQ0
	DDR_B_D28	AM48	SA_DQ60	SM_VREF_DQ1	AP51		+SM_VREF_DQ1
	DDR_B_D29	AK48	SA_DQ61				
	DDR_B_D30	AM51	SA_DQ62				
	DDR_B_D31	AK51	SA_DQ63				

DDR interleave routing

UC1D — HASWELL_MCP_E — DDR CHANNEL B — 4 OF 19 — Rev1p2

18 DDR_A_D[32..47]	DDR_A_D32	AY31	SB_DQ0	SB_CK#0	AM38	M_CLK_DDR#2	M_CLK_DDR#2 19
	DDR_A_D33	AW31	SB_DQ1	SB_CK0	AN38	M_CLK_DDR2	M_CLK_DDR2 19
	DDR_A_D34	AY29	SB_DQ2	SB_CK#1	AK38	M_CLK_DDR#3	M_CLK_DDR#3 19
	DDR_A_D35	AW29	SB_DQ3	SB_CK1	AL38	M_CLK_DDR3	M_CLK_DDR3 19
	DDR_A_D36	AV31	SB_DQ4				
	DDR_A_D37	AU31	SB_DQ5	SB_CKE0	AY49	DDR_CKE2_DIMMB	DDR_CKE2_DIMMB 19
	DDR_A_D38	AV29	SB_DQ6	SB_CKE1	AU50	DDR_CKE3_DIMMB	DDR_CKE3_DIMMB 19
	DDR_A_D39	AU29	SB_DQ7	SB_CKE2	AW49		
	DDR_A_D40	AY27	SB_DQ8	SB_CKE3	AV50		
	DDR_A_D41	AW27	SB_DQ9				
	DDR_A_D42	AY25	SB_DQ10	SB_CS#0	AM32	DDR_CS2_DIMMB#	DDR_CS2_DIMMB# 19
	DDR_A_D43	AW25	SB_DQ11	SB_CS#1	AK32	DDR_CS3_DIMMB#	DDR_CS3_DIMMB# 19
	DDR_A_D44	AY27	SB_DQ12				
	DDR_A_D45	AU27	SB_DQ13	SB_ODT0	AL32		
	DDR_A_D46	AY25	SB_DQ14				
	DDR_A_D47	AU25	SB_DQ15	SB_RAS	AM35	DDR_B_RAS#	DDR_B_RAS# 19
19 DDR_B_D[32..47]	DDR_B_D32	AM29	SB_DQ16	SB_WE	AK35	DDR_B_WE#	DDR_B_WE# 19
	DDR_B_D33	AK29	SB_DQ17	SB_CAS	AM33	DDR_B_CAS#	DDR_B_CAS# 19
	DDR_B_D34	AL28	SB_DQ18				
	DDR_B_D35	AK28	SB_DQ19	SB_BA0	AL35	DDR_B_BS0	DDR_B_BS0 19
	DDR_B_D36	AR29	SB_DQ20	SB_BA1	AM36	DDR_B_BS1	DDR_B_BS1 19
	DDR_B_D37	AN29	SB_DQ21	SB_BA2	AU49	DDR_B_BS2	DDR_B_BS2 19
	DDR_B_D38	AR28	SB_DQ22				DDR_B_MA[0..15] 19
	DDR_B_D39	AP28	SB_DQ23	SB_MA0	AP40	DDR_B_MA0	
	DDR_B_D40	AN26	SB_DQ24	SB_MA1	AR40	DDR_B_MA1	
	DDR_B_D41	AR26	SB_DQ25	SB_MA2	AP42	DDR_B_MA2	
	DDR_B_D42	AR25	SB_DQ26	SB_MA3	AR42	DDR_B_MA3	
	DDR_B_D43	AP25	SB_DQ27	SB_MA4	AR45	DDR_B_MA4	
	DDR_B_D44	AK26	SB_DQ28	SB_MA5	AP45	DDR_B_MA5	
	DDR_B_D45	AM26	SB_DQ29	SB_MA6	AW46	DDR_B_MA6	
	DDR_B_D46	AK25	SB_DQ30	SB_MA7	AY46	DDR_B_MA7	
	DDR_B_D47	AL25	SB_DQ31	SB_MA8	AY47	DDR_B_MA8	
18 DDR_A_D[48..63]	DDR_A_D48	AY23	SB_DQ32	SB_MA9	AU46	DDR_B_MA9	
	DDR_A_D49	AW23	SB_DQ33	SB_MA10	AK36	DDR_B_MA10	
	DDR_A_D50	AY21	SB_DQ34	SB_MA11	AV47	DDR_B_MA11	
	DDR_A_D51	AW21	SB_DQ35	SB_MA12	AU47	DDR_B_MA12	
	DDR_A_D52	AV23	SB_DQ36	SB_MA13	AK33	DDR_B_MA13	
	DDR_A_D53	AU23	SB_DQ37	SB_MA14	AR46	DDR_B_MA14	
	DDR_A_D54	AV21	SB_DQ38	SB_MA15	AP46	DDR_B_MA15	
	DDR_A_D55	AU21	SB_DQ39				
	DDR_A_D56	AY19	SB_DQ40	SB_DQSN0	AW30	DDR_A_DQS#4	DDR_A_DQS#[4..5] 18
	DDR_A_D57	AW19	SB_DQ41	SB_DQSN1	AV26	DDR_A_DQS#5	DDR_B_DQS#[4..5] 19
	DDR_A_D58	AY17	SB_DQ42	SB_DQSN2	AN28	DDR_B_DQS#4	
	DDR_A_D59	AW17	SB_DQ43	SB_DQSN3	AN25	DDR_B_DQS#5	DDR_A_DQS#[6..7] 18
	DDR_A_D60	AV19	SB_DQ44	SB_DQSN4	AW22	DDR_A_DQS#6	
	DDR_A_D61	AU19	SB_DQ45	SB_DQSN5	AV18	DDR_A_DQS#7	DDR_B_DQS#[6..7] 19
	DDR_A_D62	AV17	SB_DQ46	SB_DQSN6	AN21	DDR_B_DQS#6	
	DDR_A_D63	AU17	SB_DQ47	SB_DQSN7	AN18	DDR_B_DQS#7	
19 DDR_B_D[48..63]	DDR_B_D48	AR21	SB_DQ48				
	DDR_B_D49	AR22	SB_DQ49	SB_DQSP0	AV30	DDR_A_DQS4	DDR_A_DQS[4..5] 18
	DDR_B_D50	AL21	SB_DQ50	SB_DQSP1	AW26	DDR_A_DQS5	DDR_B_DQS[4..5] 19
	DDR_B_D51	AM22	SB_DQ51	SB_DQSP2	AN28	DDR_B_DQS4	
	DDR_B_D52	AN22	SB_DQ52	SB_DQSP3	AM25	DDR_B_DQS5	DDR_A_DQS[6..7] 18
	DDR_B_D53	AP21	SB_DQ53	SB_DQSP4	AV22	DDR_A_DQS6	
	DDR_B_D54	AK21	SB_DQ54	SB_DQSP5	AW18	DDR_A_DQS7	DDR_B_DQS[6..7] 19
	DDR_B_D55	AK22	SB_DQ55	SB_DQSP6	AM21	DDR_B_DQS6	
	DDR_B_D56	AN20	SB_DQ56	SB_DQSP7	AM18	DDR_B_DQS7	
	DDR_B_D57	AR20	SB_DQ57				
	DDR_B_D58	AK18	SB_DQ58				
	DDR_B_D59	AL18	SB_DQ59				
	DDR_B_D60	AK20	SB_DQ60				
	DDR_B_D61	AM20	SB_DQ61				
	DDR_B_D62	AP18	SB_DQ62				
	DDR_B_D63	AP18	SB_DQ63				

Place near to SO-DIMM connector.

+1.35V_MEM

+SM_VREF_CA_DIMM — RC87 1.8K_0402_1% — RC68 1 2_0402_1% — +SM_VREF_CA

CC67 0.022U_0402_16V7K~D change 22nF

RC89 1.8K_0402_1%

RC83 24.9_0402_1%~D

+SM_VREF_DQ1_DIMM2 — RC130 1.8K_0402_1% — RC1261 2_0402_1% — +SM_VREF_DQ1

CC69 0.022U_0402_16V7K~D change 22nF

RC132 1.8K_0402_1%

RC128 24.9_0402_1%~D

+SM_VREF_DQ0_DIMM1 — RC217 1.8K_0402_1% — RC1731 2_0402_1% — +SM_VREF_DQ0

CC70 0.022U_0402_16V7K~D change 22nF

RC221 1.8K_0402_1%

RC195 24.9_0402_1%~D

Refer to Intel request PDG1.0 P148

Interleaved Memory

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Compal Electronics, Inc.

Title: MCP(3/12) DDR3

Size: | Document Number: LA-9832P | Rev: 0.5

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DeepSleep and Non-DeepSleep config:

Config	DSx	Non-DSx
Pop	RC86,R319,RC267	RC79,RC82,RC265
Depop	RC79,RC82,RC265	RC86,R319,RC267

DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

DDR3 COMPENSATION SIGNALS

200_0402_1%~D — JRC125 — SM_RCOMP0
121_0402_1% — JRC129 — SM_RCOMP1
100_0402_1%~D — JRC133 — SM_RCOMP2

CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

CAD Note:
Avoid stub in the PWRGD path while placing resistors RC115

PU/PD for JTAG signals

XDP_DBRESET# — RC116 — 1K_0402_1%~D — +3.3V_RUN
CPU_XDP_TMS — @RC118 — 51_0402_1%~D — +1.05V_RUN
CPU_XDP_TDI — @RC119 — 51_0402_1%~D
CPU_XDP_PRE0# — @RC120 — 51_0402_1%~D
CPU_XDP_TDO — RC122 — 51_0402_1%~D
CPU_XDP_TCLK — RC127 — 51_0402_1%~D
CPU_XDP_TRST# — @RC131 — 51_0402_1%~D

Place near JXDP1
Place near JXDP1.48
Place near JXDP1.47
RC5 need to close to JCPU1
reference Shark Bay ULT Validation Customer Debug Port Implementation Requirement Rev 1.0
reference CR8

EMI
For ESD concern,place RC209, RC208, RC194, RC204 near to CPU

Compal Electronics, Inc.
Title: MCP(4/12) PM, JTAG,MISC
Size: — Document Number: LA-9832P — Rev: 0.5
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Intel check list has updated correctly

DP HUB <-----

HDMI<-----

UC1A — HASWELL_MCP_E — 1 OF 19 — Rev1p2

UC1I — HASWELL_MCP_E — 9 OF 19 — Rev1p2

COMPENSATION PU FOR eDP

follow intel feedback

+VCCIOA_OUT

EDP_COMP 2 — 1 RC134 24.9_0402_1%~D

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

Intel WW18 Strapping option

Intel WW18 Strapping option

RP1 2.2K_0804_8P4R_5%

reference 0.55 design chane log WW23_2

reference PDG 0.9

Compal Electronics, Inc.

Title: MCP(5/12) DDI,EDP,GPIO

Size: | Document Number: LA-9832P | Rev: 0.5

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42 PEG_GTX_C_HRX_N[0..3] → PEG_GTX_C_HRX_N[0..3]
42 PEG_GTX_C_HRX_P[0..3] → PEG_GTX_C_HRX_P[0..3]
42 PEG_HTX_C_GRX_N[0..3] ← PEG_HTX_C_GRX_N[0..3]
42 PEG_HTX_C_GRX_P[0..3] ← PEG_HTX_C_GRX_P[0..3]

32 PEG_GTX_C_HRX_N0_M — PEG_GTX_C_HRX_N0_M — R101 1 UMA@ 2 0_0402_5%~D — PEG_GTX_C_HRX_N0_R
32 PEG_GTX_C_HRX_P0_M — PEG_GTX_C_HRX_P0_M — R100 1 UMA@ 2 0_0402_5%~D — PEG_GTX_C_HRX_P0_R
32 PEG_HTX_GRX_N0_M — PEG_HTX_GRX_N0_M — R102 1 UMA@ 2 0_0402_5%~D — PEG_HTX_GRX_N0
32 PEG_HTX_GRX_P0_M — PEG_HTX_GRX_P0_M — R104 1 UMA@ 2 0_0402_5%~D — PEG_HTX_GRX_P0

UC1K HASWELL_MCP_E

GPU -->
PEG_GTX_C_HRX_N0 R106 1 DIS@ 2 0_0402_5%~D PEG_GTX_C_HRX_N0_R F10 — PERN5_L0
PEG_GTX_C_HRX_P0 R105 1 DIS@ 2 0_0402_5%~D PEG_GTX_C_HRX_P0_R E10 — PERP5_L0
PEG_HTX_C_GRX_N0 CU16 1 2 DIS@ 0.1U_0402_10V7K~D PEG_HTX_GRX_N0 C23 — PETN5_L0
PEG_HTX_C_GRX_P0 CU17 1 2 DIS@ 0.1U_0402_10V7K~D PEG_HTX_GRX_P0 C22 — PETP5_L0
PEG_GTX_C_HRX_N1 F8 — PERN5_L1
PEG_GTX_C_HRX_P1 E8 — PERP5_L1
PEG_HTX_C_GRX_N1 CU18 1 2 DIS@ 0.1U_0402_10V7K~D PEG_HTX_GRX_N1 B23 — PETN5_L1
PEG_HTX_C_GRX_P1 CU19 1 2 DIS@ 0.1U_0402_10V7K~D PEG_HTX_GRX_P1 A23 — PETP5_L1
PEG_GTX_C_HRX_N2 H10 — PERN5_L2
PEG_GTX_C_HRX_P2 G10 — PERP5_L2
PEG_HTX_C_GRX_N2 CU20 1 2 DIS@ 0.1U_0402_10V7K~D PEG_HTX_GRX_N2 B21 — PETN5_L2
PEG_HTX_C_GRX_P2 CU21 1 2 DIS@ 0.1U_0402_10V7K~D PEG_HTX_GRX_P2 C21 — PETP5_L2
PEG_GTX_C_HRX_N3 E6 — PERN5_L3
PEG_GTX_C_HRX_P3 F6 — PERP5_L3
PEG_HTX_C_GRX_N3 CU22 1 2 DIS@ 0.1U_0402_10V7K~D PEG_HTX_GRX_N3 B22 — PETN5_L3
PEG_HTX_C_GRX_P3 CU23 1 2 DIS@ 0.1U_0402_10V7K~D PEG_HTX_GRX_P3 A21 — PETP5_L3

10/100/1G LAN --->
28 PCIE_PRX_GLANTX_N3 PCIE_PRX_GLANTX_N3 G11 — PERN3
28 PCIE_PRX_GLANTX_P3 PCIE_PRX_GLANTX_P3 F11 — PERP3
28 PCIE_PTX_GLANRX_N3 PCIE_PTX_GLANRX_N3 C29 — PETN3
28 PCIE_PTX_GLANRX_P3 PCIE_PTX_GLANRX_P3 B30 — PETP3

WLAN (Mini Card 2)--->
31 PCIE_PRX_WLANTX_N4 PCIE_PRX_WLANTX_N4 F13 — PERN4
31 PCIE_PRX_WLANTX_P4 PCIE_PRX_WLANTX_P4 G13 — PERP4
31 PCIE_PTX_WLANRX_N4 PCIE_PTX_WLANRX_N4 B29 — PETN4
31 PCIE_PTX_WLANRX_P4 PCIE_PTX_WLANRX_P4 A29 — PETP4

MMI PCIE <-----
30 PCIE_PRX_MMITX_N1 PCIE_PRX_MMITX_N1 G17 — PERN1/USB3RN3
30 PCIE_PRX_MMITX_P1 PCIE_PRX_MMITX_P1 F17 — PERP1/USB3RP3
30 PCIE_PTX_MMIRX_N1 PCIE_PTX_MMIRX_N1 C30 — PETN1/USB3TN3
30 PCIE_PTX_MMIRX_P1 PCIE_PTX_MMIRX_P1 C31 — PETP1/USB3TP3

E-Dock USB3.0<-----
35 USB3RN4 F15 — PERN2/USB3RN4
35 USB3RP4 G15 — PERP2/USB3RP4
35 USB3TN4 B31 — PETN2/USB3TN4
35 USB3TP4 A31 — PETP2/USB3TP4

reference CRB 3.01K 1%
+PCH_AUSB3PLL — RC161 1 2 3.01K_0402_1%~D PCH_PCIE_RCOMP A27 — PCIE_RCOMP
RC163 1 @ 2 0_0402_5% PCH_PCIE_IREF B27 — PCIE_IREF
E15 — RSVD
E12 — RSVD

PCIe | USB

USB2N0 AN8 USBP0- — USBP0- 36 — -----> Ext Port 1(I/O) RIGHT
USB2P0 AM8 USBP0+ — USBP0+ 36
USB2N1 AR7 USBP1- — USBP1- 34 — -----> Ext Port 2 (MB/Debug Port) LEFT
USB2P1 AT7 USBP1+ — USBP1+ 34
USB2N2 AR8 USBP2- — USBP2- 36 — -----> Ext Port 3 (USB/B) REAR
USB2P2 AP8 USBP2+ — USBP2+ 36
USB2N3 AR10 DOCK_USBP1- — DOCK_USBP1- 35 — -----> E-DOCK1
USB2P3 AT10 DOCK_USBP1+ — DOCK_USBP1+ 35
USB2N4 AM15 DOCK_USBP2- — DOCK_USBP2- 35 — -----> E-DOCK2
USB2P4 AL15 DOCK_USBP2+ — DOCK_USBP2+ 35
USB2N5 AM13 USBP5- — USBP5- 20 — -----> Camera
USB2P5 AN13 USBP5+ — USBP5+ 20
USB2N6 AP11 USBP6- — USBP6- 22 — -----> Touch Screen
USB2P6 AN11 USBP6+ — USBP6+ 22
USB2N7 AR13 USBP7- — USBP7- 33 — -----> HUB
USB2P7 AP13 USBP7+ — USBP7+ 33

USB3RN1 G20 USB3RN0 — USB3RN0 34
USB3RP1 H20 USB3RP0 — USB3RP0 34 — -----> Ext USB3 Port 1
USB3TN1 C33 USB3TN0 — USB3TN0 34
USB3TP1 B34 USB3TP0 — USB3TP0 34
USB3RN2 E18 USB3RN1 — USB3RN1 34
USB3RP2 F18 USB3RP1 — USB3RP1 34 — -----> Ext USB3 Port 2 IO/B
USB3TN2 B33 USB3TN1 — USB3TN1 34
USB3TP2 A33 USB3TP1 — USB3TP1 34

USBRBIAS AJ10 USBRBIAS
USBRBIAS AJ11
RSVD AN10
RSVD AM10

OC0/GPIO40 AL3 USB_OC0# — USB_OC0# 12,36
OC1/GPIO41 AT1 USB_OC1# — USB_OC1# 12,34
OC2/GPIO42 AH2 USB_OC2# — USB_OC2# 12,36
OC3/GPIO43 AV3 USB_OC3# — USB_OC3# 12

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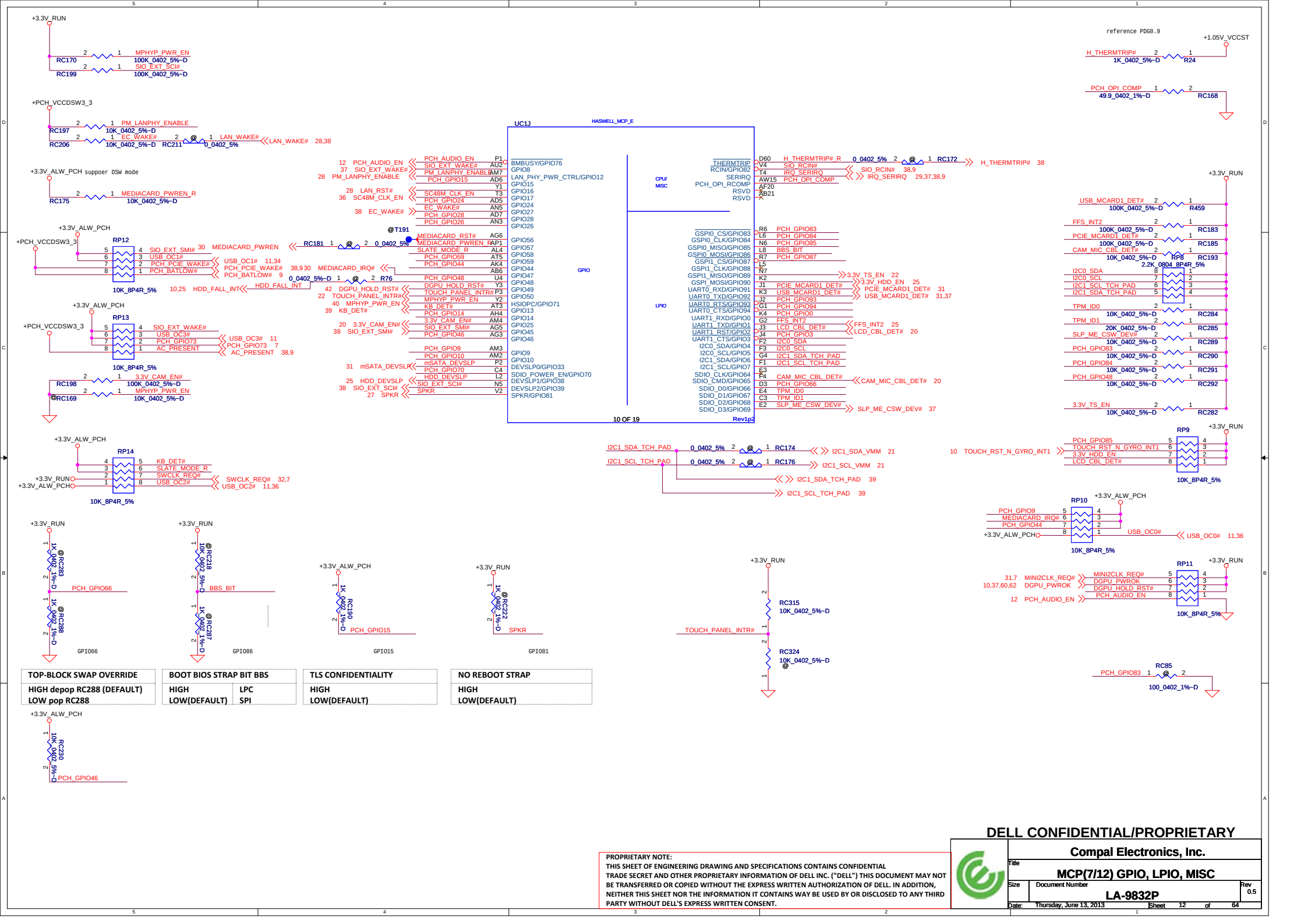
USBRBIAS — 1 RC159 22.6_0402_1%~D 2

CAD NOTE:
Route single-end 50-ohms and max 500-mils length.
Avoid routing next to clock pins or under stitching capacitors.
Recommended minimum spacing to other signal traces is 15 mils.

Compal Electronics, Inc.
Title: MCP(6/12) PCIE,USB
Size: | Document Number: LA-9832P | Rev: 0.5
Date: Thursday, June 13, 2013 | Sheet 11 of 64



TOP-BLOCK SWAP OVERRIDE	BOOT BIOS STRAP BIT BBS		TLS CONFIDENTIALITY	NO REBOOT STRAP
HIGH depop RC288 (DEFAULT)	HIGH	LPC	HIGH	HIGH
LOW pop RC288	LOW(DEFAULT)	SPI	LOW(DEFAULT)	LOW(DEFAULT)

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Compal Electronics, Inc.

Title: MCP(7/12) GPIO, LPIO, MISC

Size | Document Number: LA-9832P | Rev: 0.5

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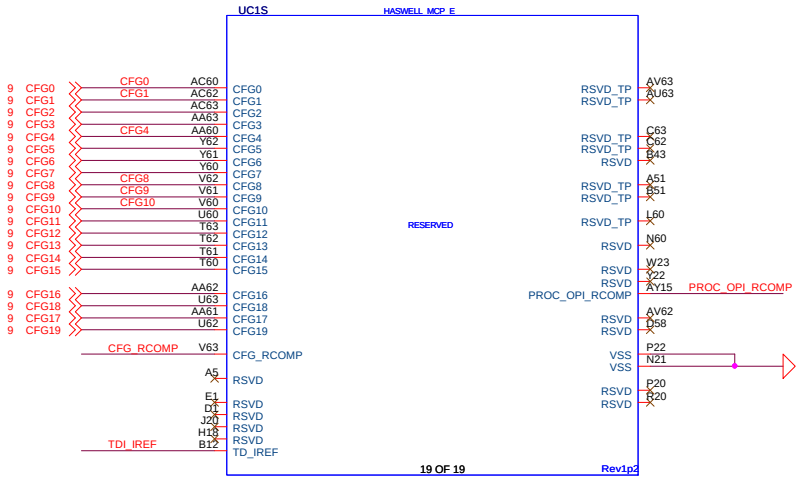
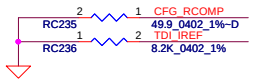
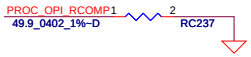
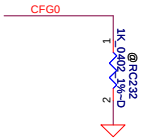
CFG STRAPS for CPU

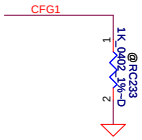




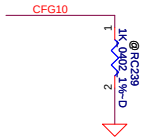


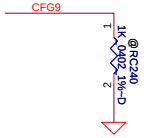


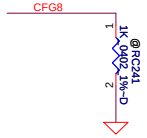
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

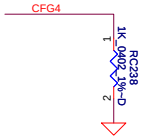


PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed









SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegardless of the locking of the unit

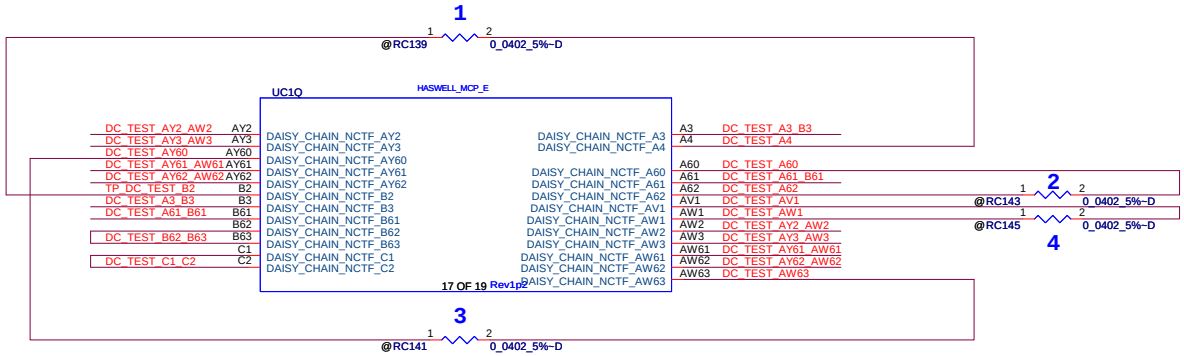
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Compal Electronics, Inc.

Title: MCP(8/12) CFG, RSVD

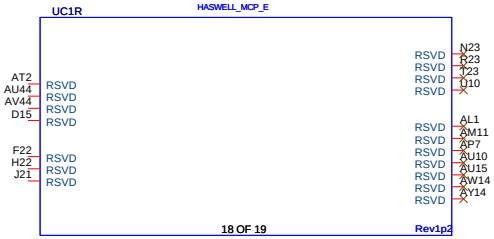
Size: | Document Number: LA-9832P | Rev: 0.5

Date: Thursday, June 13, 2013 | Sheet 13 of 64



Package Daisy Chain:

1. B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
2. A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
3. AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
4. AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1

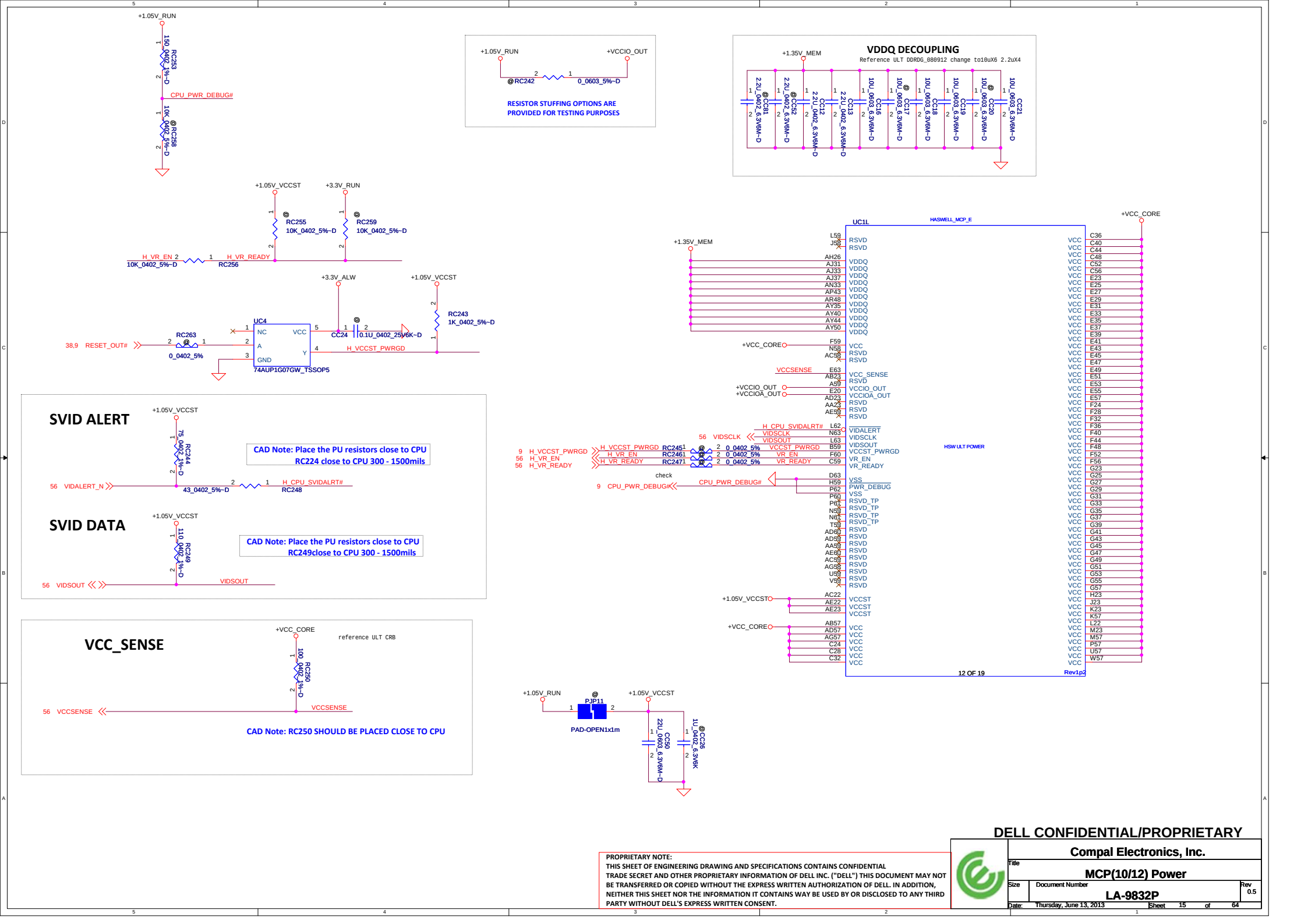


Compal Electronics, Inc.

Title: MCP(9/12) TP,RSVD

Size | Document Number: LA-9832P | Rev: 0.5

Date: Thursday, June 13, 2013 | Sheet 14 of 64



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Compal Electronics, Inc.

Title: MCP(10/12) Power

Size | Document Number: LA-9832P | Rev: 0.5

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CC29 place near K9;
CC27 place near L10
CC74 place near M9

CC42 place near B18

CC49 place near B11

CC56 place near AA21

CC66 place near AH13
CC61 CC62 place near J13

CC32 place near AH10

CC51 place near J18

CC58 place near A20

CC44 place near AH14

CC28 place near AC9

CC43 place near V8

CC63 close to Pin J17
CC64 close to Pin R21

DeepSleep and Non-DeepSleep config:

Config	DSx	Non-DSx
Pop	RC86,R319,RC267	RC79,RC82,RC265
Depop	RC79,RC82,RC265	RC86,R319,RC267

CC40 place near Y8

CC34 and CC33 place near J11; CC37 place near AE8

CC46 CC47 place near AE9

CC59 place near K14

CC45 place near U8

CC60 place near AG16

CC35,CC38, CC39 place near AG10

CC65 place near AG19

CC30 place near AH11

CC54 place near AD10

CC53 place near AB8

Table 6-3. Pre-Si I_{cc}max Estimates

Voltage Rail	Voltage (V)	S0 Iccmax Current (A)[3]	Sx Iccmax Current (A)[3]	Deep Sx Iccmax (A)[3]	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCHDA	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1[4]	1.05	0.109	0.014	0	0
DcpSus2[4]	1.05	0.025	0.001	0	0
DcpSus3[4]	1.05	0.010	0.003	0	0
DcpSus4[4]	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 µA See notes 1, 2

NOTES:

+1.5V_THERMAL use 20mil trace

close to UC1.J15

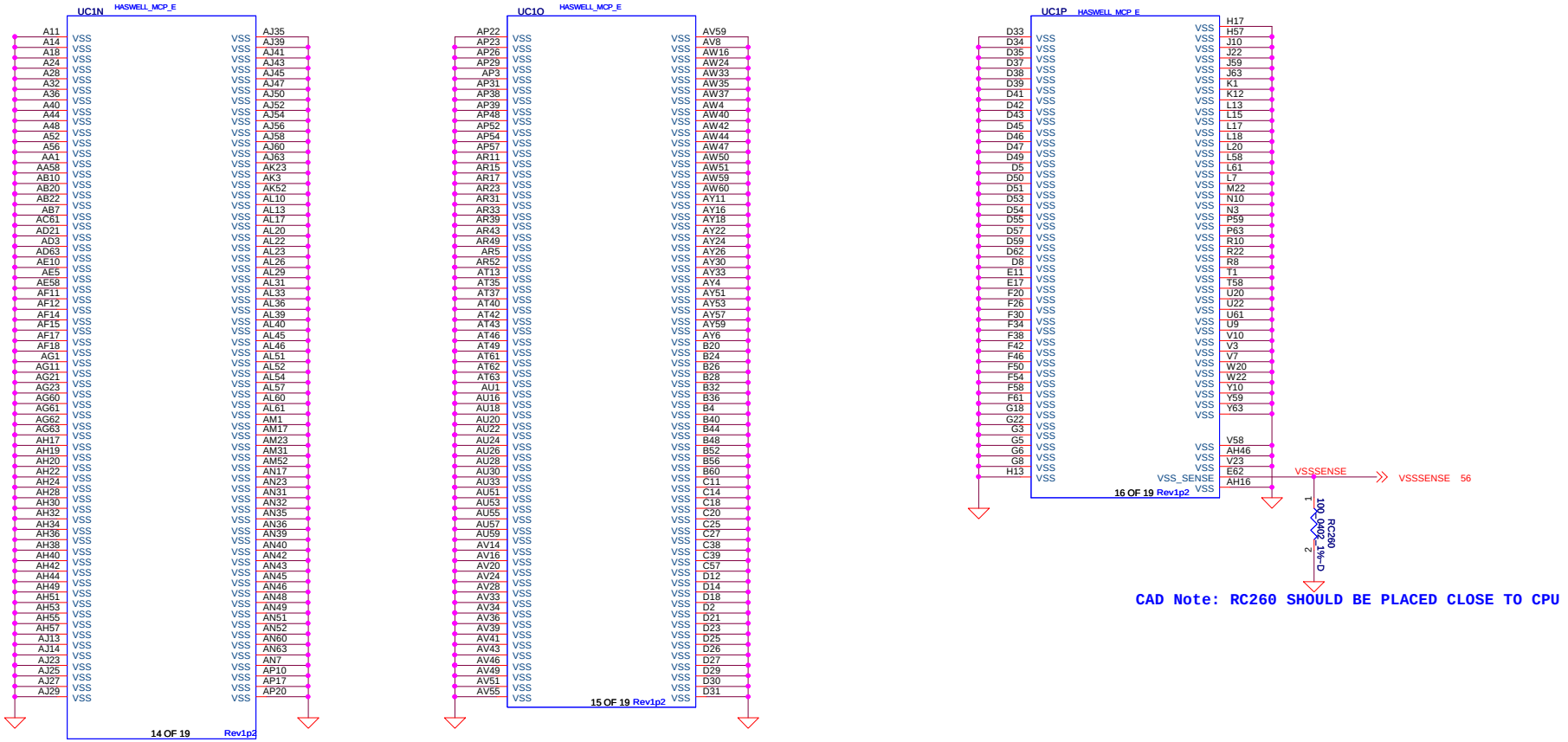
close to UC1

Compal Electronics, Inc.

Title: MCP(11/12) Power

Size: | Document Number: LA-9832P | Rev: 0.5

Date: Friday, August 30, 2013 | Sheet 16 of 64



Compal Electronics, Inc.

Title: MCP(12/12) VSS

Size | Document Number: LA-9832P | Rev: 0.5

Date: Thursday, June 13, 2013 | Sheet 17 of 64

JDIMM1 H=8mm

2-3A to 1 DIMMs/channel

Reverse Type

JDIMM1 CONN@ — CONCR_0706F0BE80F

P/N:SP07000VB00

All VREF traces should have 10 mil trace width

8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..15]

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM1.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

DDR3L SODIMM ODT GENERATION

QD1 BSS138-G_SOT23-3
R28 220K_0402_5%~D
R32 2M_0402_5%~D
R29 66.5_0402_1%
R30 66.5_0402_1%
R31 66.5_0402_1%
R33 66.5_0402_1%
M_ODT0
M_ODT1
M_ODT2 19
M_ODT3 19

U5 74AUP1G07GW_TSSOP5
R34 0_0402_5%~D
9 DDR_PG_CTRL
0.675V_DDR_VTT_ON

Interleaved Memory

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Compal Electronics, Inc.

Title: DDRIII DIMM1

Size: | Document Number: LA-9832P | Rev: 0.5

Date: Thursday, June 13, 2013 | Sheet 18 of 64

JDIMM2 H=4mm *2-3A to 1 DIMMs/channel*

Reverse Type

8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..15]

All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM2

Layout Note:
Place near JDIMM2.203,204

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

+SM_VREF_DQ1_DIMM2 — RD7 @ 0_0402_5%
+DIMM2_VREF_DQ — CD32 2.2U_0402_6.3V6M-D, CD33 0.1U_0402_25V6K-D

+1.35V_MEM — CD35 1U_0402_6.3V6K-D, CD36 1U_0402_6.3V6K-D, CD37 1U_0402_6.3V6K-D, CD38 1U_0402_6.3V6K-D, CD39 1U_0402_6.3V6K-D, CD40 1U_0402_6.3V6K-D, CD41 1U_0402_6.3V6K-D, CD42 1U_0402_6.3V6K-D

+1.35V_MEM — CD45 10U_0603_6.3V6M-D, CD46 10U_0603_6.3V6M-D @, CD47 10U_0603_6.3V6M-D @, CD48 10U_0603_6.3V6M-D, CD49 10U_0603_6.3V6M-D, CD50 10U_0603_6.3V6M-D, CD51 10U_0603_6.3V6M-D, CD52 10U_0603_6.3V6M-D, CD62 330U_D3_2.5V_R6M

+0.675V_DDR_VTT — CD54 0.1U_0402_25V6K-D, CD55 0.1U_0402_25V6K-D, CD56 0.1U_0402_25V6K-D, CD57 0.1U_0402_25V6K-D, CD58 10U_0603_6.3V6M-D, CD59 10U_0603_6.3V6M-D

+3.3V_RUN — 0_0402_5% @ RD10
+3.3V_RUN — CD60 0.1U_0402_25V6K-D, CD61 2.2U_0402_6.3V6M-D @, RD11 0_0402_5% @

+1.35V_MEM — CD34 0.1U_0402_25V6K-D @

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

+SM_VREF_CA_DIMMB — RD13 @ 0_0402_5% — +SM_VREF_CA_DIMM
CD43 2.2U_0402_6.3V6M-D, CD44 0.1U_0402_25V6K-D

JDIMM2 CONN@
CONCR_0706E0BE40F
P/N:SP07000QA00

		1	VREF_DQ	VSS	2		
	DDR_B_D23	3	VSS	DQ4	4	DDR_B_D22	
	DDR_B_D17	5	DQ0	DQ5	6	DDR_B_D16	
		7	DQ1	VSS	8		
		9	VSS	DQS0#	10	DDR_B_DQS#2	
		11	DM0	DQS0	12	DDR_B_DQS2	
	DDR_B_D21	13	VSS	VSS	14		
	DDR_B_D18	15	DQ2	DQ6	16	DDR_B_D19	
		17	DQ3	DQ7	18	DDR_B_D20	
	DDR_B_D3	19	VSS	VSS	20		
	DDR_B_D2	21	DQ8	DQ12	22	DDR_B_D4	
		23	DQ9	DQ13	24	DDR_B_D5	
	DDR_B_DQS#0	25	VSS	VSS	26		
	DDR_B_DQS0	27	DQS1#	DM1	28		
		29	DQS1	RESET#	30	DDR3_DRAMRST#	DDR3_DRAMRST# 18
		31	VSS	VSS	32		
	DDR_B_D0	33	DQ10	DQ14	34	DDR_B_D6	
	DDR_B_D1	35	DQ11	DQ15	36	DDR_B_D7	
		37	VSS	VSS	38		
	DDR_B_D12	39	DQ16	DQ20	40	DDR_B_D13	
	DDR_B_D8	41	DQ17	DQ21	42	DDR_B_D9	
		43	VSS	VSS	44		
	DDR_B_DQS#1	45	DQS2#	DM2	46		
	DDR_B_DQS1	47	DQS2	VSS	48		
		49	VSS	DQ22	50	DDR_B_D11	
	DDR_B_D14	51	DQ18	DQ23	52	DDR_B_D10	
	DDR_B_D15	53	DQ19	VSS	54		
		55	VSS	DQ28	56	DDR_B_D30	
	DDR_B_D31	57	DQ24	DQ29	58	DDR_B_D26	
	DDR_B_D25	59	DQ25	VSS	60		
		61	VSS	DQS3#	62	DDR_B_DQS#3	
		63	DM3	DQS3	64	DDR_B_DQS3	
		65	VSS	VSS	66		
	DDR_B_D27	67	DQ26	DQ30	68	DDR_B_D29	
	DDR_B_D24	69	DQ27	DQ31	70	DDR_B_D28	
		71	VSS	VSS	72		
8 DDR_CKE2_DIMMB	DDR_CKE2_DIMMB	73	CKE0	CKE1	74	DDR_CKE3_DIMMB	DDR_CKE3_DIMMB 8
		75	VDD	VDD	76		
		77	NC	A15	78	DDR_B_MA15	
8 DDR_B_BS2	DDR_B_BS2	79	BA2	A14	80	DDR_B_MA14	
		81	VDD	VDD	82		
	DDR_B_MA12	83	A12/BC#	A11	84	DDR_B_MA11	
	DDR_B_MA9	85	A9	A7	86	DDR_B_MA7	
		87	VDD	VDD	88		
	DDR_B_MA8	89	A8	A6	90	DDR_B_MA6	
	DDR_B_MA5	91	A5	A4	92	DDR_B_MA4	
		93	VDD	VDD	94		
	DDR_B_MA3	95	A3	A2	96	DDR_B_MA2	
	DDR_B_MA1	97	A1	A0	98	DDR_B_MA0	
		99	VDD	VDD	100		
8 M_CLK_DDR2	M_CLK_DDR2	101	CK0	CK1	102	M_CLK_DDR3	M_CLK_DDR3 8
8 M_CLK_DDR#2	M_CLK_DDR#2	103	CK0#	CK1#	104	M_CLK_DDR#3	M_CLK_DDR#3 8
		105	VDD	VDD	106		
	DDR_B_MA10	107	A10/AP	BA1	108	DDR_B_BS1	DDR_B_BS1 8
8 DDR_B_BS0	DDR_B_BS0	109	BA0	RAS#	110	DDR_B_RAS#	DDR_B_RAS# 8
		111	VDD	VDD	112		
	DDR_B_WE#	113	WE#	S0#	114	DDR_CS2_DIMMB#	DDR_CS2_DIMMB# 8
8 DDR_B_CAS#	DDR_B_CAS#	115	CAS#	ODT0	116	M_ODT2	M_ODT2 18
		117	VDD	VDD	118		
	DDR_B_MA13	119	A13	ODT1	120	M_ODT3	M_ODT3 18
8 DDR_CS3_DIMMB#	DDR_CS3_DIMMB#	121	S1#	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREF_CA	126		
		127	VSS	VSS	128		
	DDR_B_D32	129	DQ32	DQ36	130	DDR_B_D33	
	DDR_B_D35	131	DQ33	DQ37	132	DDR_B_D34	
		133	VSS	VSS	134		
	DDR_B_DQS#4	135	DQS4#	DM4	136		
	DDR_B_DQS4	137	DQS4	VSS	138		
		139	VSS	DQ38	140	DDR_B_D39	
	DDR_B_D36	141	DQ34	DQ39	142	DDR_B_D37	
	DDR_B_D38	143	DQ35	VSS	144		
		145	VSS	DQ44	146	DDR_B_D44	
	DDR_B_D40	147	DQ40	DQ45	148	DDR_B_D41	
	DDR_B_D45	149	DQ41	VSS	150		
		151	VSS	DQS5#	152	DDR_B_DQS#5	
		153	DM5	DQS5	154	DDR_B_DQS5	
		155	VSS	VSS	156		
	DDR_B_D43	157	DQ42	DQ46	158	DDR_B_D47	
	DDR_B_D42	159	DQ43	DQ47	160	DDR_B_D46	
		161	VSS	VSS	162		
	DDR_B_D52	163	DQ48	DQ52	164	DDR_B_D51	
	DDR_B_D49	165	DQ49	DQ53	166	DDR_B_D55	
		167	VSS	VSS	168		
	DDR_B_DQS#6	169	DQS6#	DM6	170		
	DDR_B_DQS6	171	DQS6	VSS	172		
		173	VSS	DQ54	174	DDR_B_D48	
	DDR_B_D50	175	DQ50	DQ55	176	DDR_B_D54	
	DDR_B_D53	177	DQ51	VSS	178		
		179	VSS	DQ60	180	DDR_B_D56	
	DDR_B_D63	181	DQ56	DQ61	182	DDR_B_D57	
	DDR_B_D62	183	DQ57	VSS	184		
		185	VSS	DQS7#	186	DDR_B_DQS#7	
		187	DM7	DQS7	188	DDR_B_DQS7	
		189	VSS	VSS	190		
	DDR_B_D58	191	DQ58	DQ62	192	DDR_B_D60	
	DDR_B_D59	193	DQ59	DQ63	194	DDR_B_D61	
		195	VSS	VSS	196		
		197	SA0	EVENT#	198		
		199	VDDSPD	SDA	200		DDR_XDP_WAN_SMBDAT 18,20,25,31,7,9
		201	SA1	SCL	202		DDR_XDP_WAN_SMBCLK 18,20,25,31,7,9
	+0.675V_DDR_VTT	203	VTT	VTT	204	+0.675V_DDR_VTT	
		205	BOSS1	BOSS2	206		

Interleaved Memory

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Compal Electronics, Inc.	
Title	DDRIII DIMM2
Size	Document Number: LA-9832P
Rev	0.5
Date:	Thursday, June 13, 2013
Sheet	19 of 64

Change to RTD2136R part number

RTD2136S

RTD2136R Operation Mode Table

Pin 47 / Pin 48	0	1
0	X	EP Mode
1	Internal ROM only	EEPROM

Panel backlight power control by EC

FDC654P: P CHANNAL

For Webcam

Connect to LVDS EDID.

Close to JLVDS1.36

Close to Pin 10

LVDS Conn.

EMI

ESD

LCD Power

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

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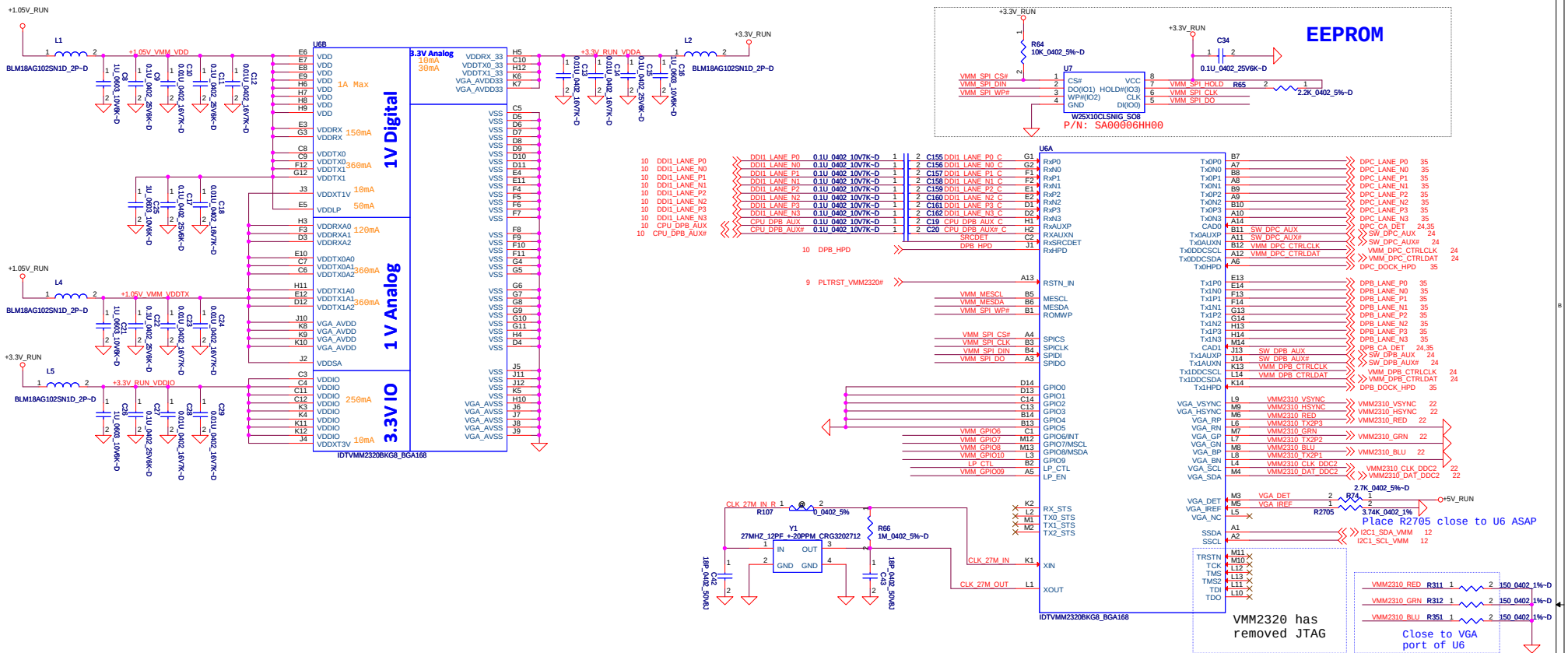
Compal Electronics, Inc.

Title: eDP to LVDS

Size | Document Number | Rev 0.5

Date: Thursday, June 13, 2013 | Sheet 20 of 64

P/N:SP010013I00



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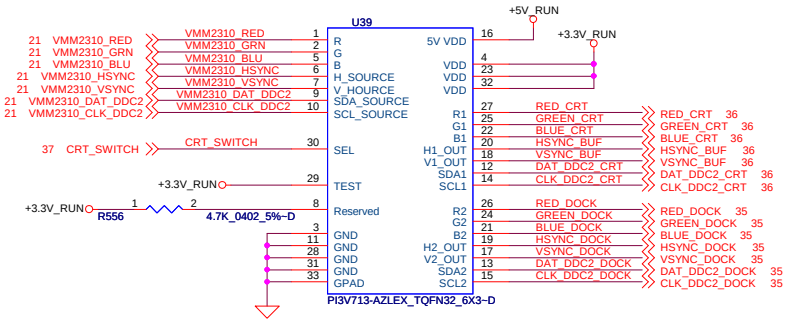
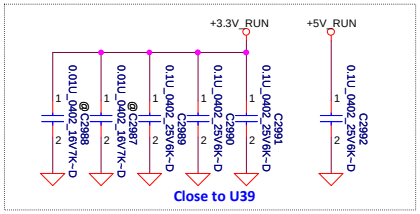
Compal Electronics, Inc.	
Title	IDT VMM2320 DP and VGA SW
Size	Document Number: LA-9832P
Rev	0.5
Date:	Monday, June 17, 2013
Sheet	21 of 64

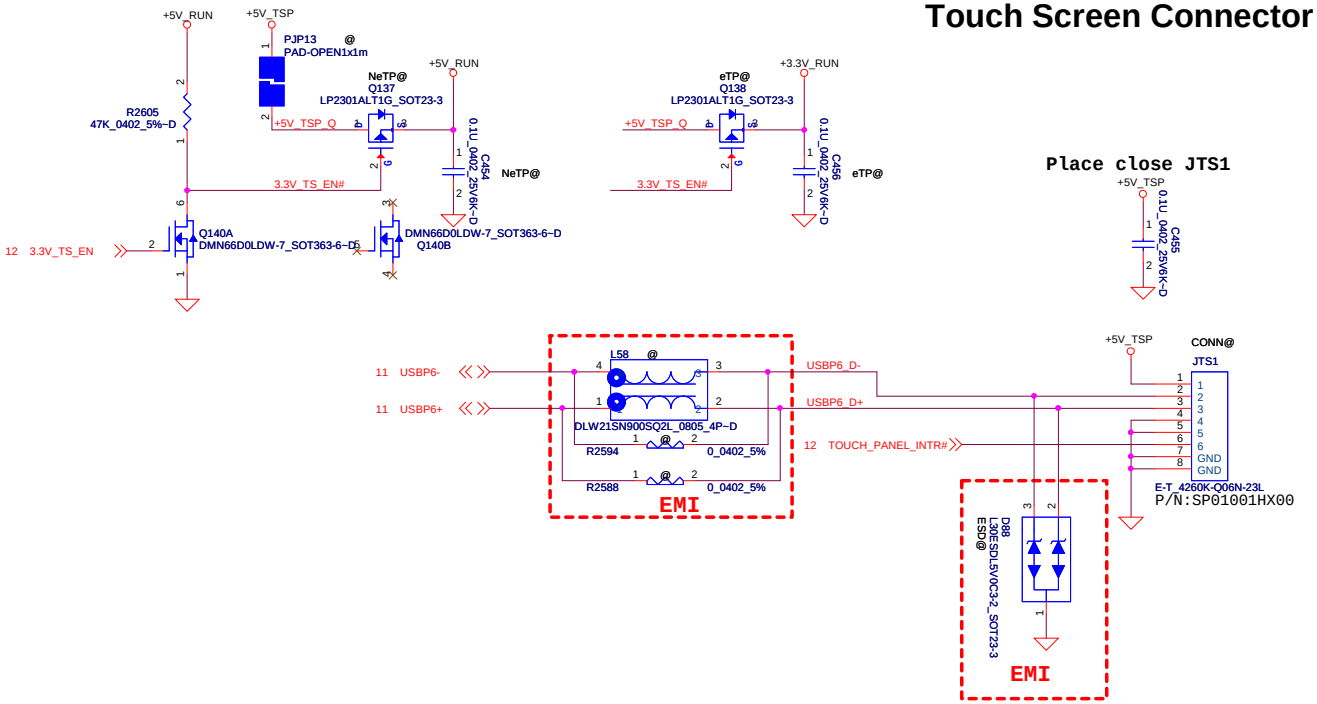
CRT SW for MB/DOCK

SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR





Touch Screen Connector



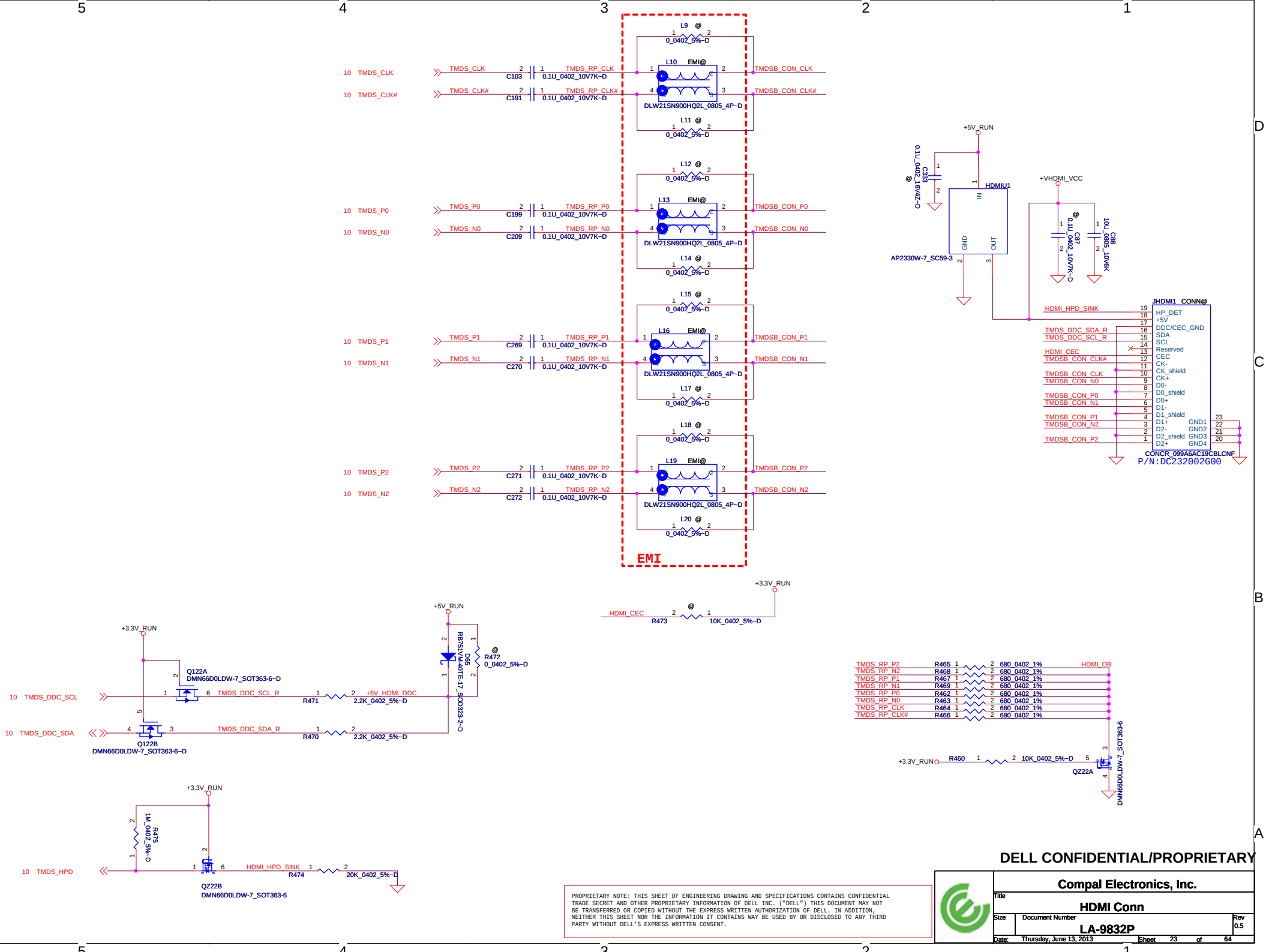
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **CRT switch/Conn and TS**

Size | Document Number | Rev 0.5

Date: Thursday, June 13, 2013 | Sheet 22 of 64



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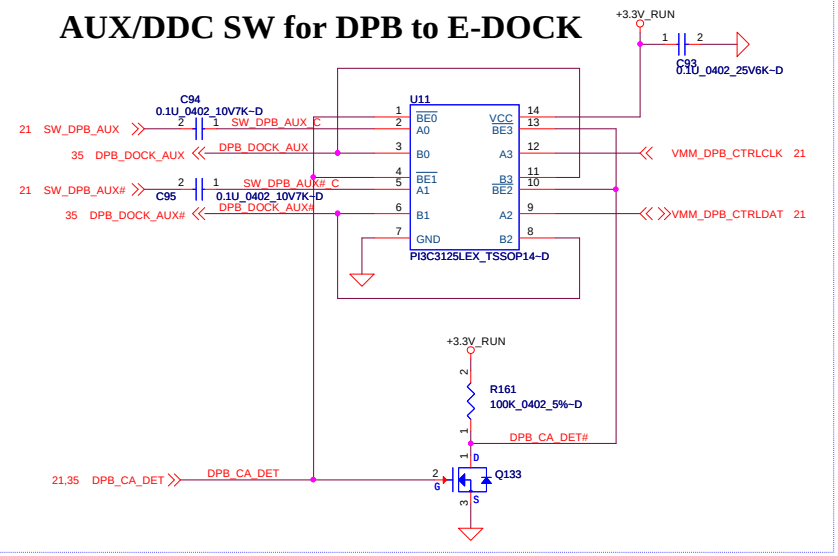
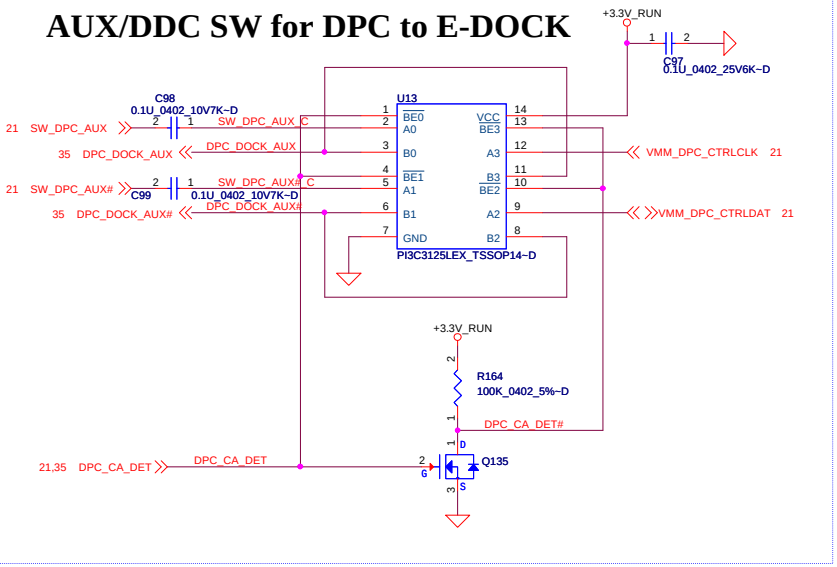
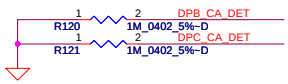
Compal Electronics, Inc.		
Title: HDMI Conn		
Size	Document Number: LA-9832P	Rev: 0.5
Date: Thursday, June 13, 2013	Sheet 23 of 64	

AUX/DDC SW for DPB to E-DOCK



AUX/DDC SW for DPC to E-DOCK





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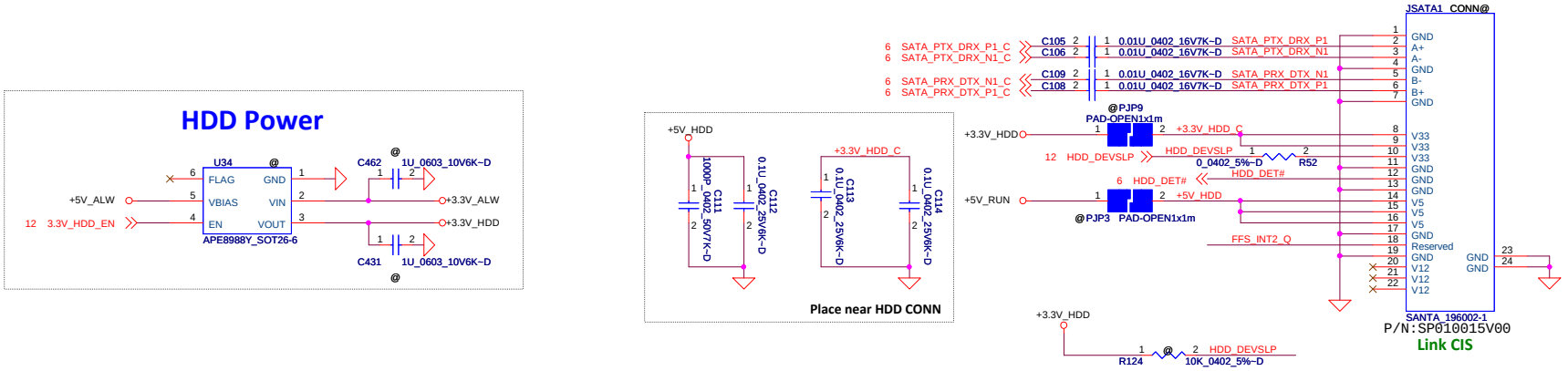
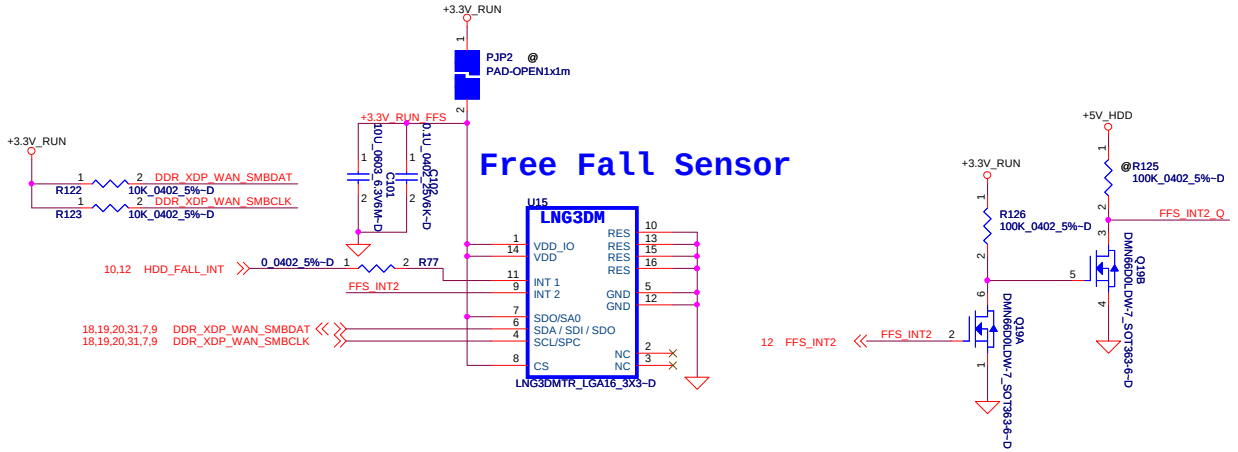
Compal Electronics, Inc.	
Title	DP SW_DP125
Size	Document Number: LA-9832P
Rev	0.5
Date:	Thursday, June 13, 2013
Sheet	24 of 64





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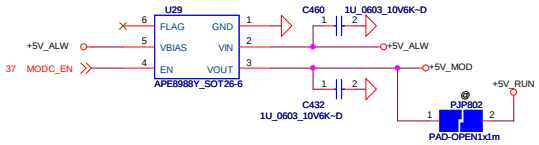
Compal Electronics, Inc.

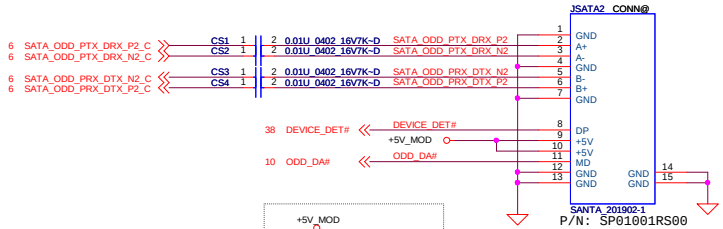
Title: HDD CONN

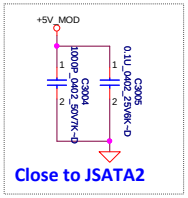
Size | Document Number: LA-9832P | Rev: 0.5

Date: Thursday, June 13, 2013 | Sheet 25 of 64

ODD power







Compal Electronics, Inc.

Title: ODD module

Size: | Document Number: LA-9832P | Rev: 0.5

Date: Thursday, June 13, 2013 | Sheet 26 of 64

Internal Speakers Header

40 mils trace keep 10 mil spacing

DVDD_IO should match with HDA Bus level

EMI

ESD

EMI Close to U17

Close to U17 pin5

Close to U17 pin6

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

Place R136 close to codec

Place R142 close to codec

Analog 5V

Analog 3.3V

2A: 80 mil width

SLEEVE/RING2 : keep 40mils trace
AUD_HP_OUT_R/AUD_HP_OUT_L : keep 15mils trace

Place C134 close to Codec

Place close to Codec

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

Place closely to Pin 13.

Add for solve pop noise and detect issue

Place closely to Pin 14

Realtek feedback
Prevent the Noise from Combo Jack while system entry into S3 / S4 /S (for Global Headset)

Pay attention to Audio no sound issue.

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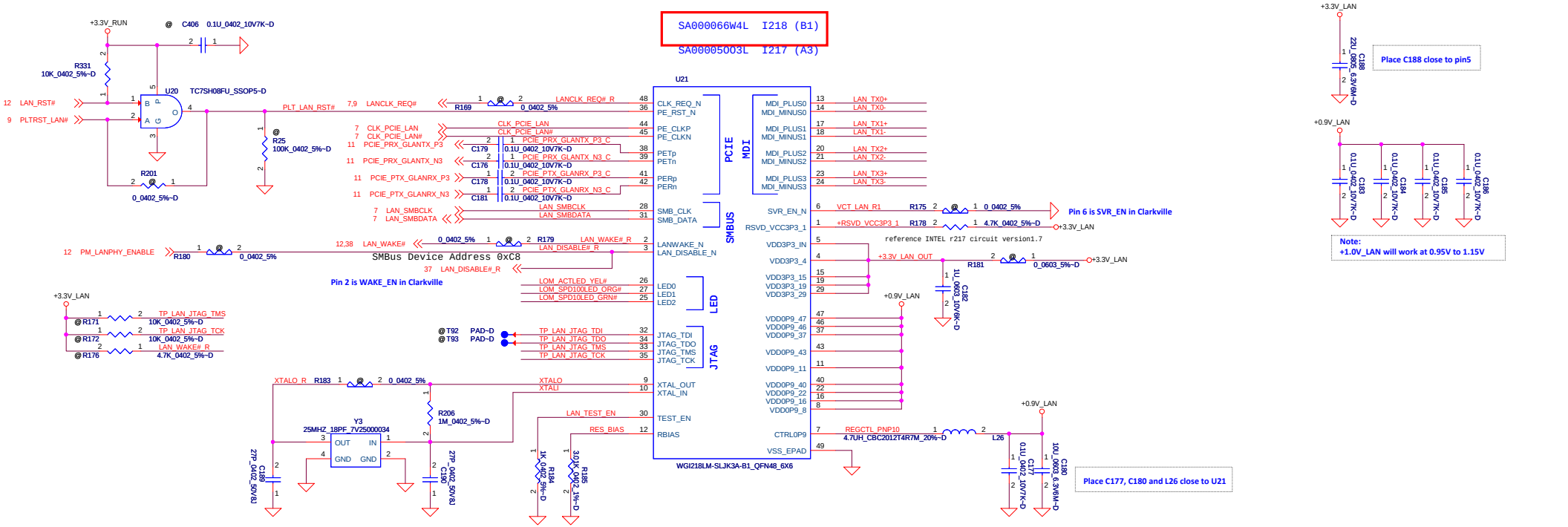
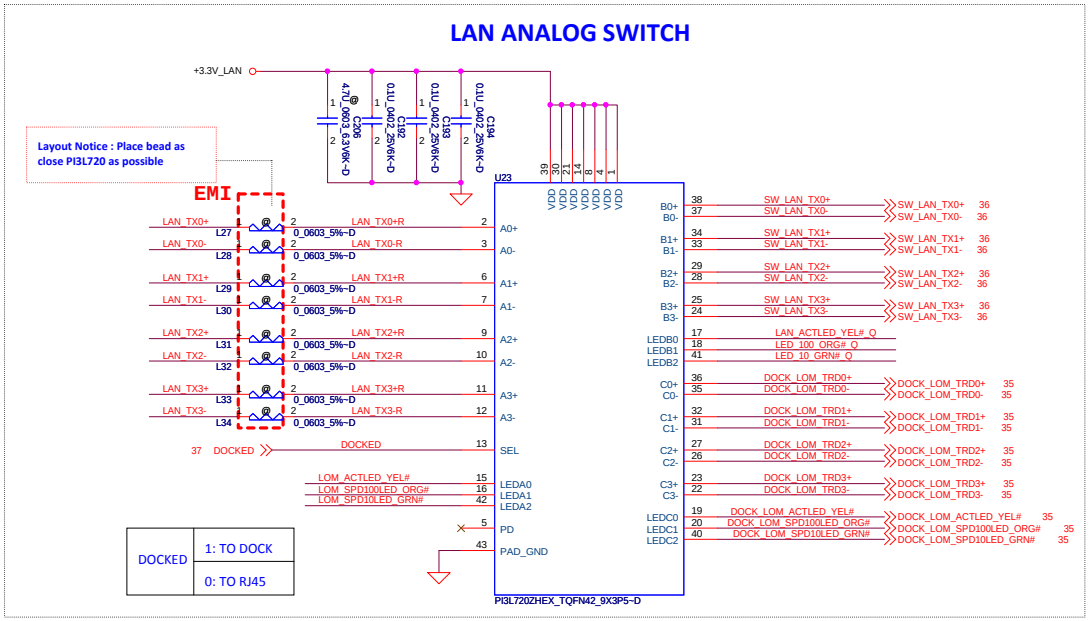
Compal Electronics, Inc.	
Title	Azalia (HD) Codec - ALC3226
Size	Document Number: LA-9832P
Rev	0.5
Date:	Friday, July 26, 2013
Sheet	27 of 64

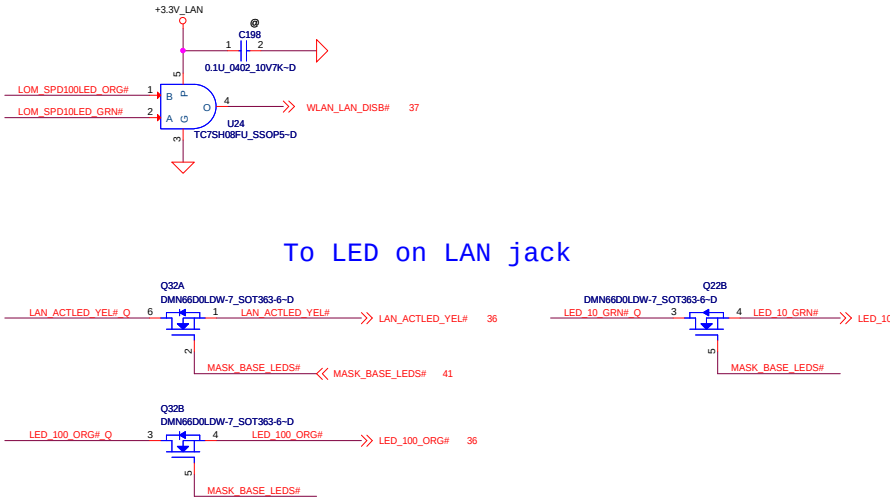
SA000066W4L I218 (B1)

SA00005003L I217 (A3)



LAN ANALOG SWITCH





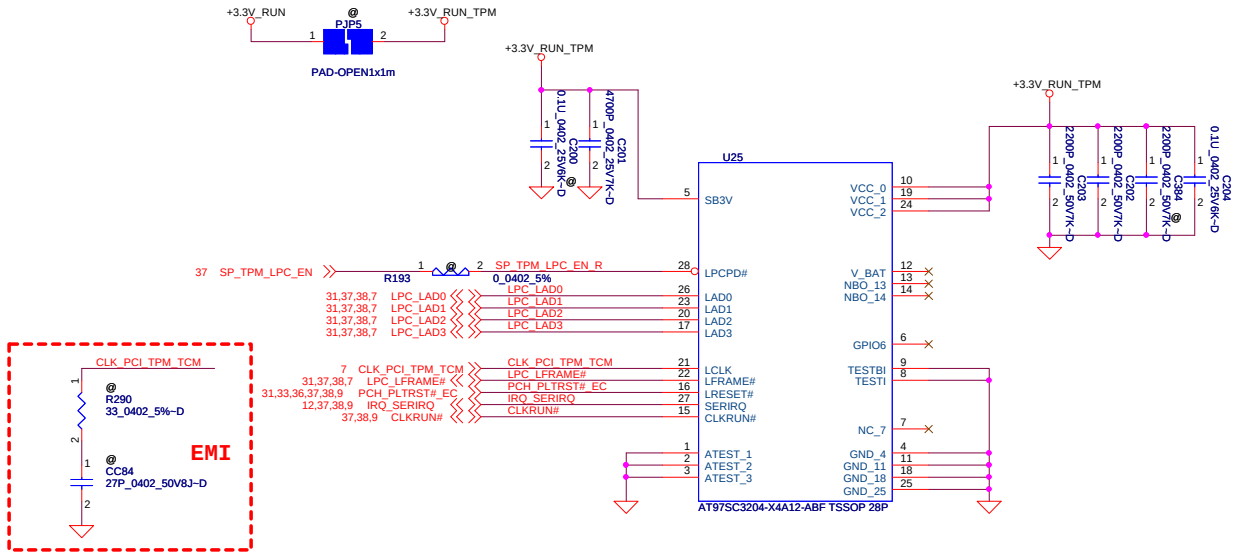
Compal Electronics, Inc.

Title: LAN Lewisville / LAN SW

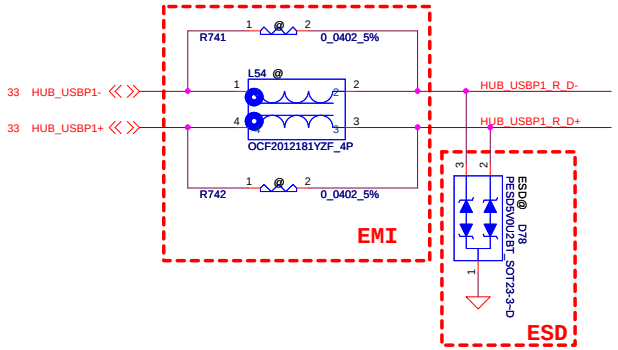
Size: | Document Number: LA-9832P | Rev: 0.5

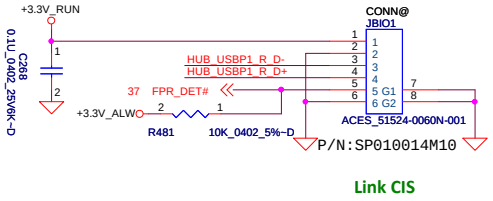
Date: Tuesday, August 13, 2013 | Sheet 28 of 64

ATMEL TPM



Finger print module





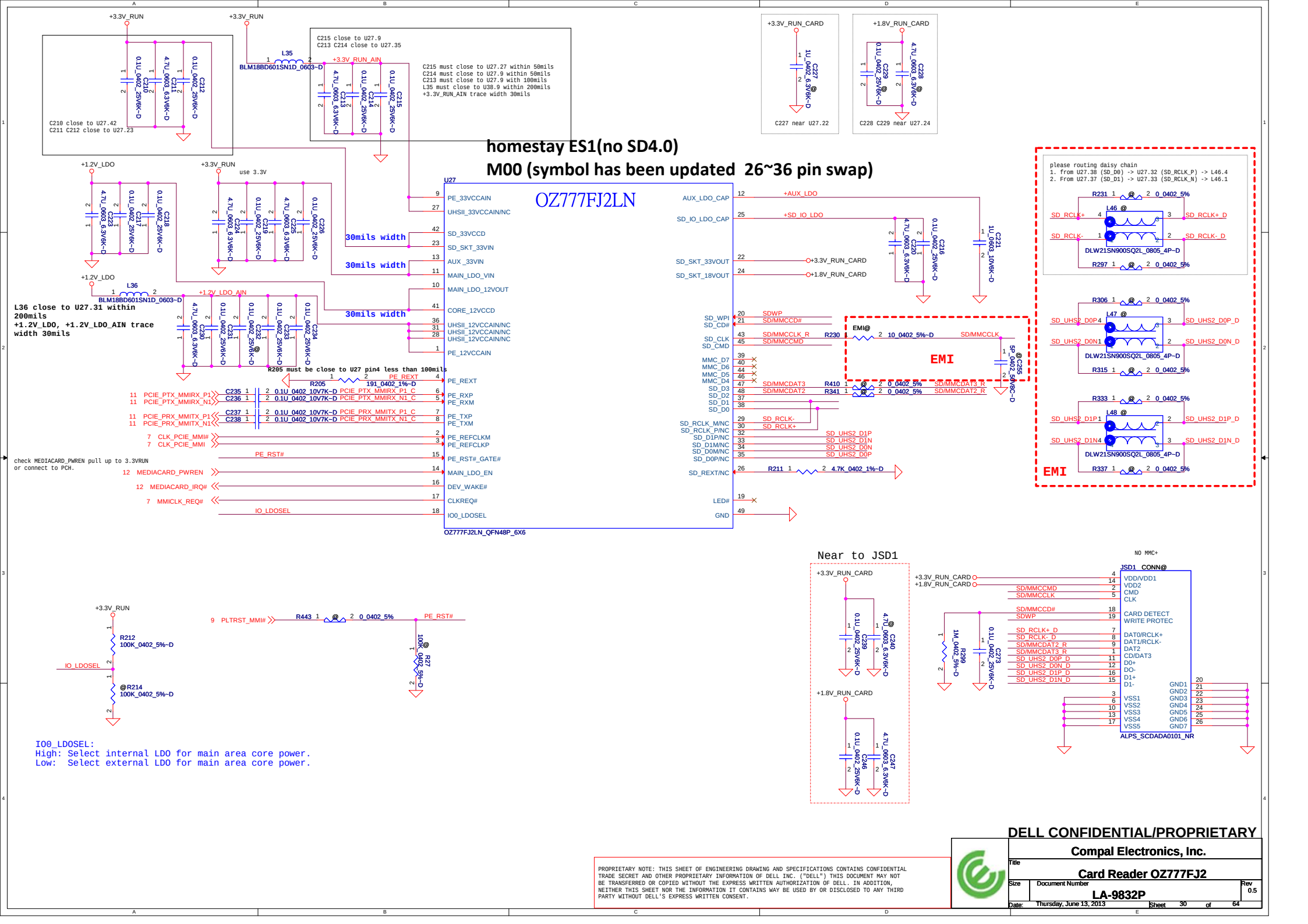
Link CIS

Compal Electronics, Inc.

Title: TPM/FP

Size | Document Number: LA-9832P | Rev: 0.5

Date: Thursday, June 13, 2013 | Sheet 29 of 64



Compal Electronics, Inc.

Title: Card Reader OZ777FJ2

Size | Document Number: LA-9832P | Rev: 0.5

Date: Thursday, June 13, 2013 | Sheet 30 of 64

HMC: Mini WLAN/WiGi/BT H=4

FMC: Mini WWAN/LTE H=8

EMI

L57 @
HUB_USBP4+_D
HUB_USBP4-_D
DLW21SN900SQ2L_0805_4P~D
HUB_USBP4+ 33
HUB_USBP4- 33
R483 @ 0_0402_5%
R482 @ 0_0402_5%

For 80 port Debug

29,31,33,36,37,38,9 PCH_PLTRST#_EC
7 CLK_PCI_LPDEBUG

For 80 port Debug

R238 @ 0_0402_5% LPC_LFRAME# → LPC_LFRAME# 29,37,38,7
R239 @ 0_0402_5% LPC_LAD3 → LPC_LAD3 29,37,38,7
R240 @ 0_0402_5% LPC_LAD2 → LPC_LAD2 29,37,38,7
R236 @ 0_0402_5% LPC_LAD1 → LPC_LAD1 29,37,38,7
R234 @ 0_0402_5% LPC_LAD0 → LPC_LAD0 29,37,38,7

For 80 port Debug

R228 @ 0_0402_5%~D +3.3V_ALW
R233 @ 0_0402_5% +3.3V_WLAN

uSIM Card Push-Push

JSIM1 CONN@
T-SOL_159-1000302602
P/N:SP070011M00
UIM_DATA
UIM_VPP
UIM_CLK
UIM_RESET
+SIM_PWR
C263 1U_0402_6.3V6K~D @

ESD

U28 @
SRV05-4.TCT_SOT23-6~D
UIM_RESET
UIM_VPP
+SIM_PWR
UIM_CLK
UIM_DATA
C264 33P_0402_50V8J~D @
C265 33P_0402_50V8J~D @
C266 33P_0402_50V8J~D @
C267 33P_0402_50V8J~D @

LED control circuit

Q22A DMN66D0LDW-7_SOT363-6~D
Q30A DMN66D0LDW-7_SOT363-6~D
Q30B DMN66D0LDW-7_SOT363-6~D
WLAN_LED# → WIRELESS_LED# 37,41
BT_LED#
LED_WWAN_OUT#
R229 100K_0402_5%~D
R227 100K_0402_5%~D
R226 100K_0402_5%~D @

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)

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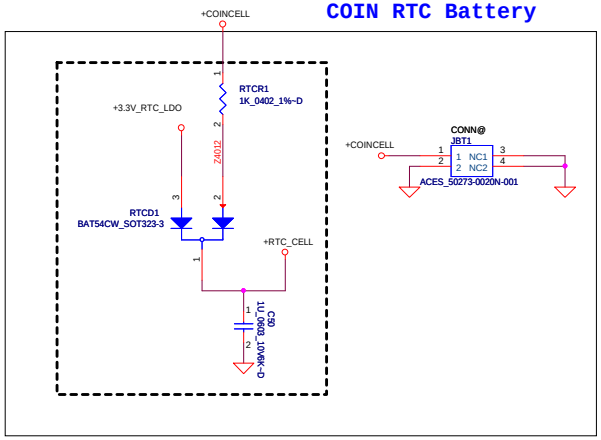
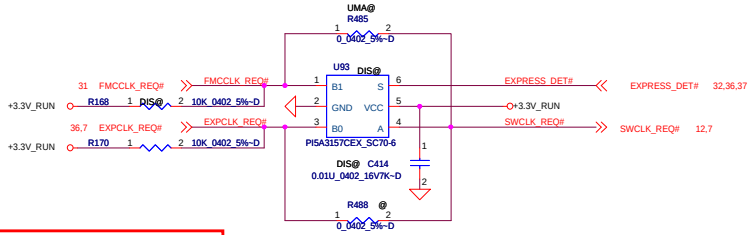
Compal Electronics, Inc.
Title: Mini Card/SIM Card
Size: Document Number: LA-9832P Rev: 0.5
Date: Thursday, June 13, 2013 Sheet 31 of 64

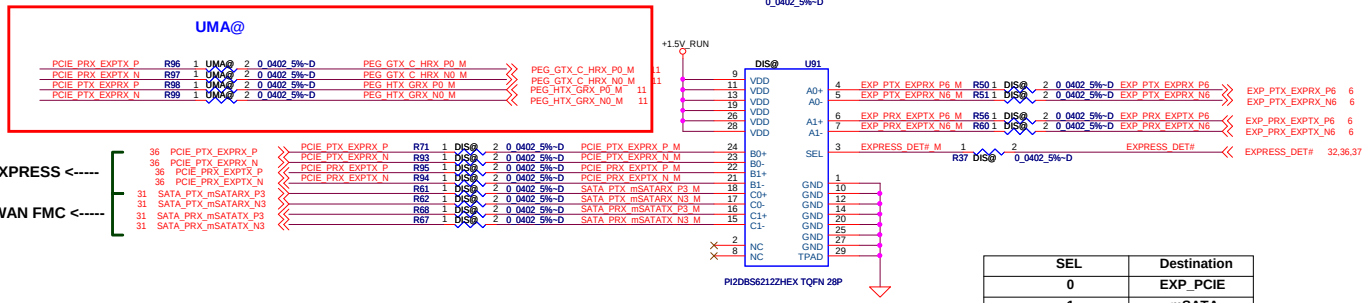
EXP/FMC PCIe clock/REQ Switch

COIN RTC Battery



B \ S	EXPRESS_DET#
EXPCLK_REQ#	0
FMCCLK_REQ#	1





SEL	Destination
0	EXP_PCIE
1	mSATA

Co-Layout with PI2DBS6212 PCIE/SATA SW

Compal Electronics, Inc.

Title: RTC Batt/PCIE_SATA SW

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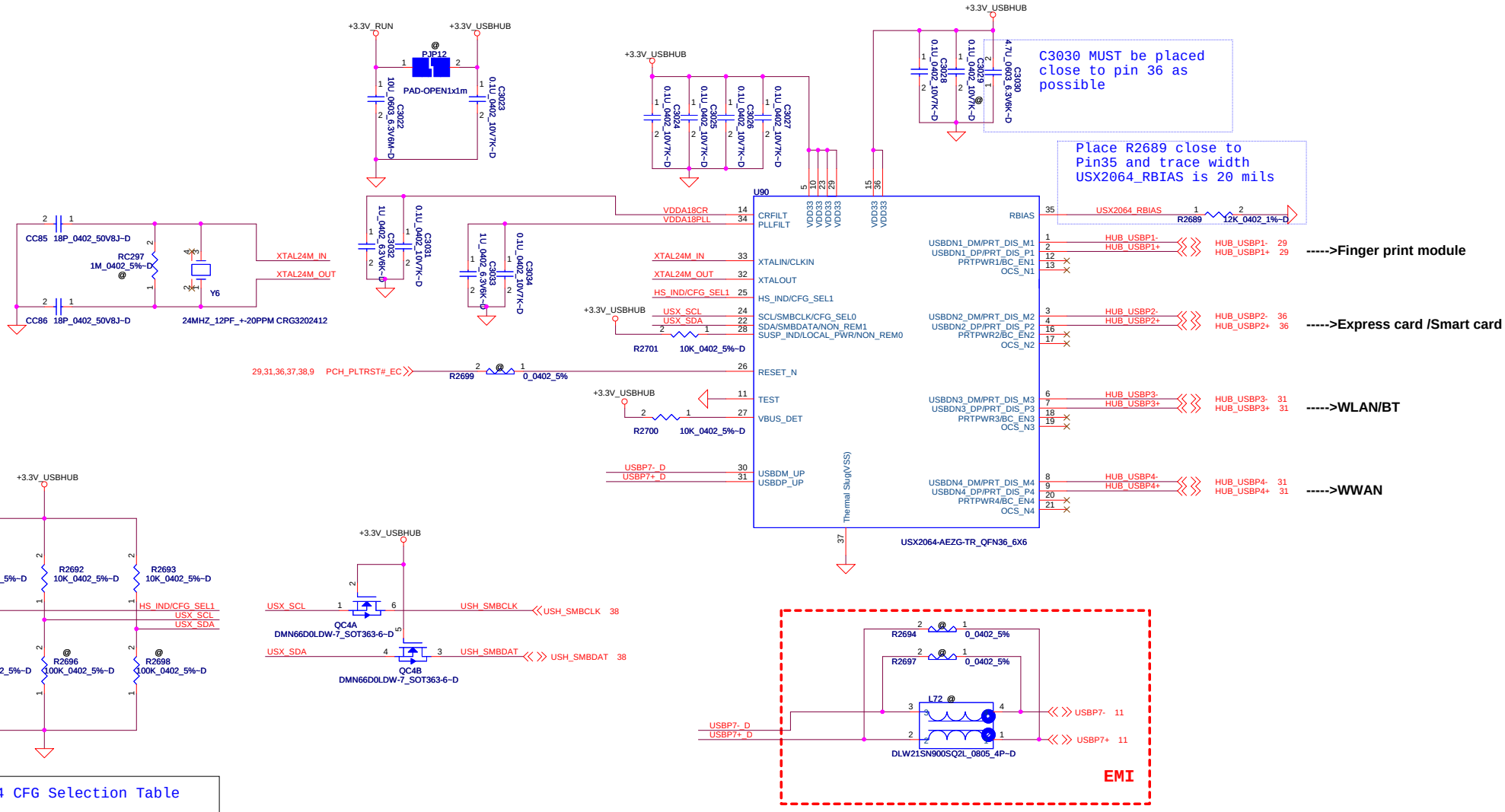
Date: Thursday, June 13, 2013 | Sheet 32 of 64



USX2064 CFG Selection Table		
CFG_SEL[0] / CFG_SEL[1]	0	1
0	Default	SMBus slave device
1	Bus-powered operation	I2C EEPROM

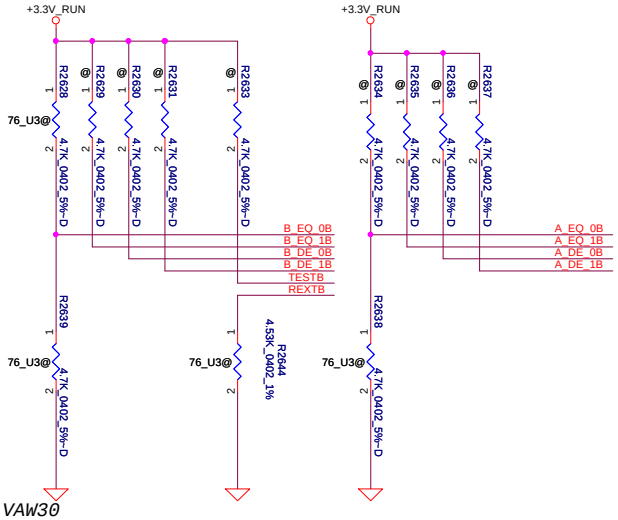
Compal Electronics, Inc.

Title: USB2.0 HUB-USX2064

Size | Document Number: LA-9832P | Rev: 0.5

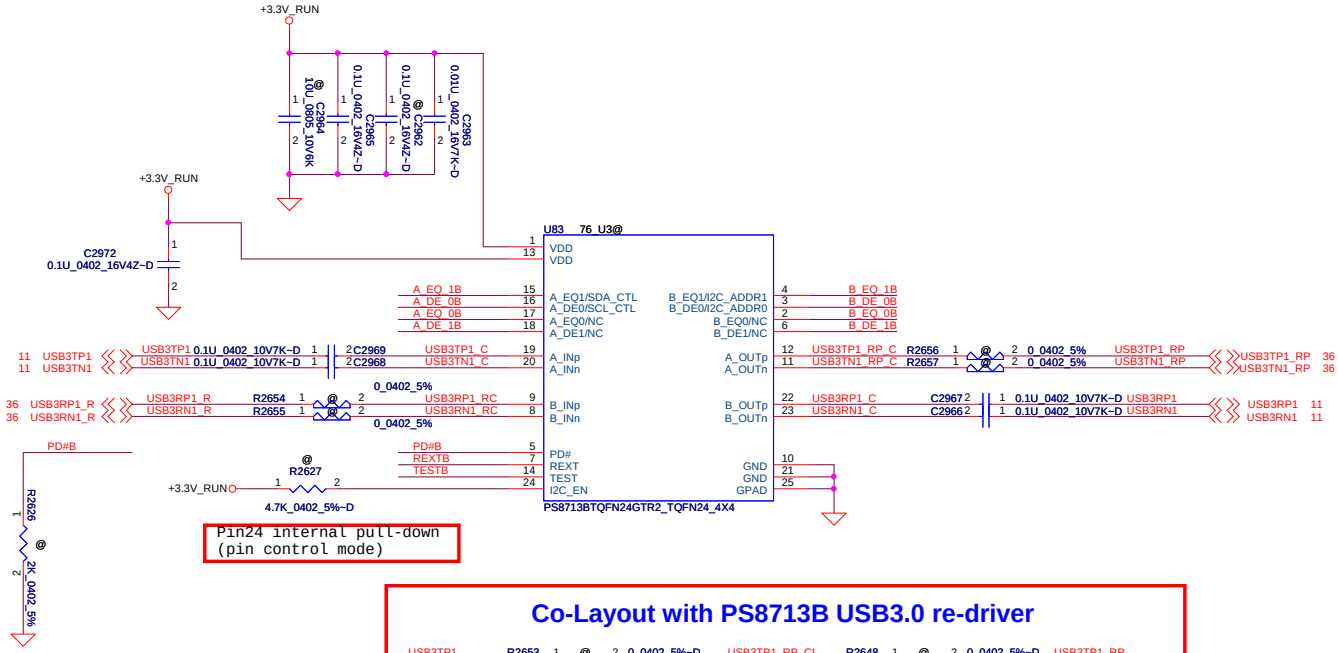
Date: Monday, June 17, 2013 | Sheet 33 of 64

USB 3.0 Re-driver for IOB



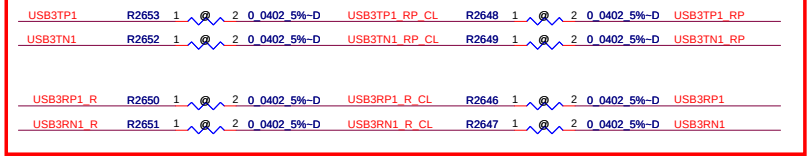
ONLY FOR VAW30

Pericom (Main) SA00006WV00	Parade (2nd) SA00005OR20
POP:R2638, R2639	POP:R2628
POP:R2644 (SD00000U200)	POP:R2644 (SD034453180)
A channel EQ 3db DE -3.5db B channel EQ 3db DE -3.5db	A channel EQ 9.5db DE 3.5db B channel EQ 13db DE 3.5db

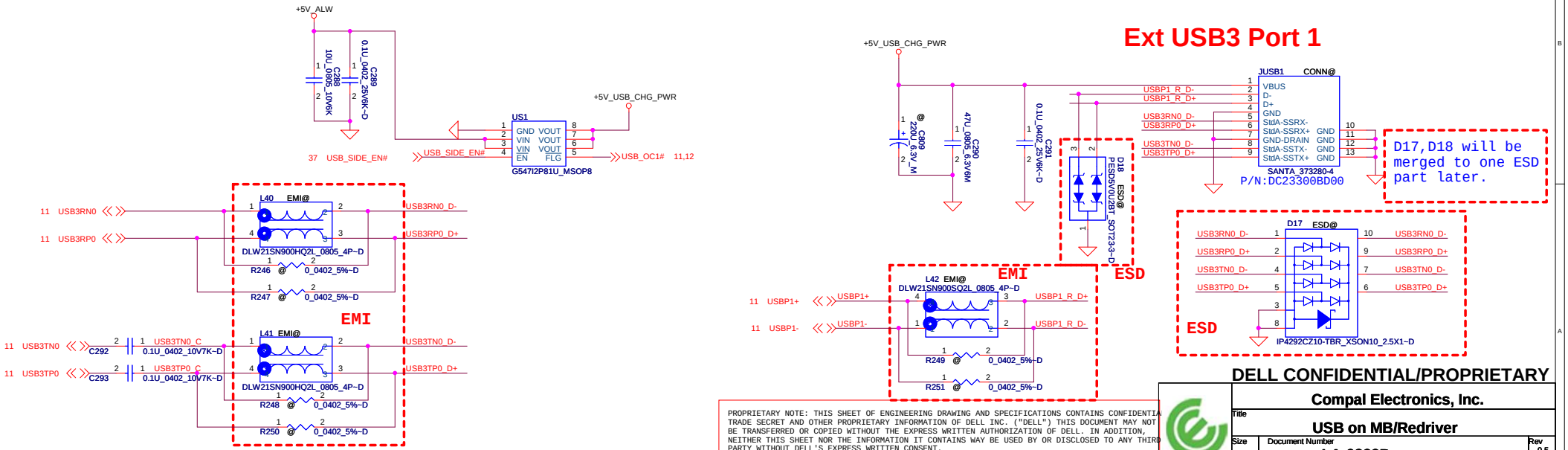


Pin24 internal pull-down
(pin control mode)

Co-Layout with PS8713B USB3.0 re-driver



Ext USB3 Port 1



Compal Electronics, Inc.

Title: USB on MB/Redriver

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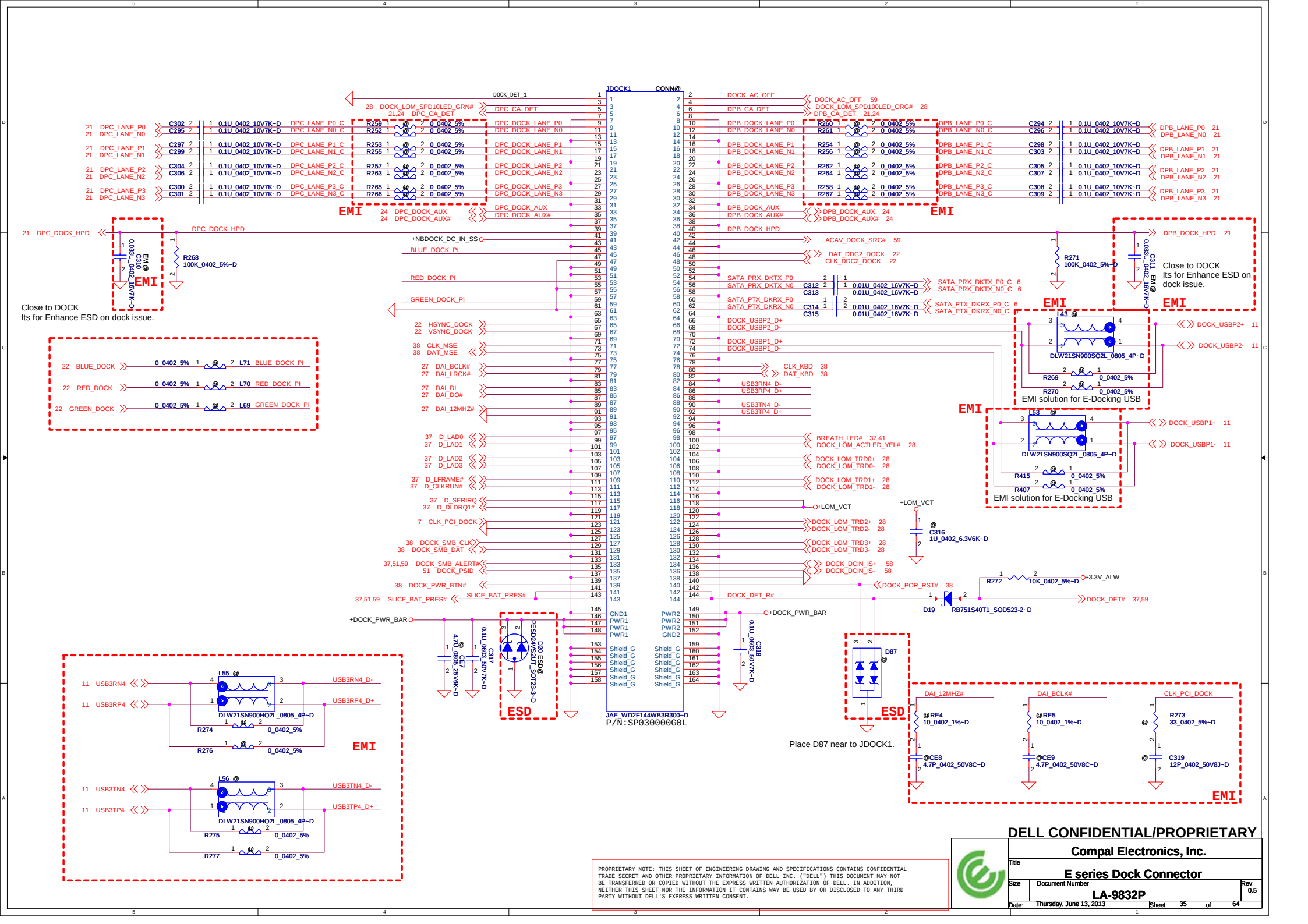
JDOCK1
CONN@
JAE_WD2F144WB3R300~D
P/N:SP030000G0L
EMI
ESD
Close to DOCK
Its for Enhance ESD on dock issue.
EMI solution for E-Docking USB
Place D87 near to JDOCK1.
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
E series Dock Connector
LA-9832P
Thursday, June 13, 2013
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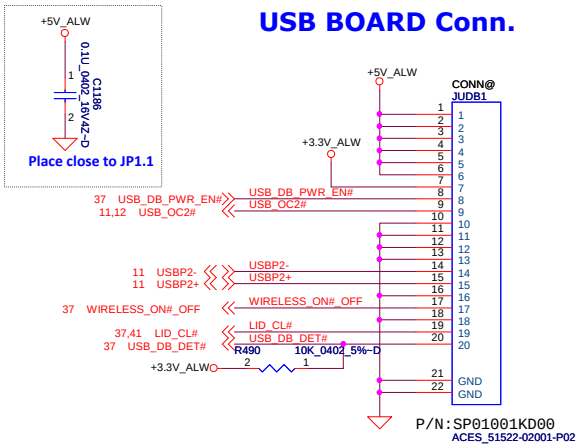
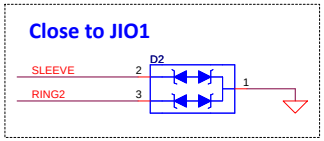
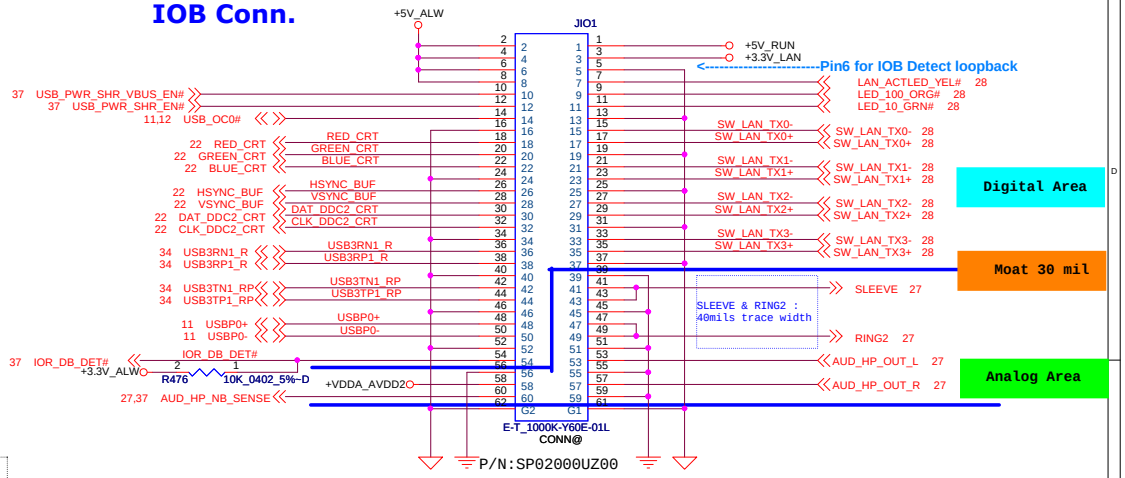
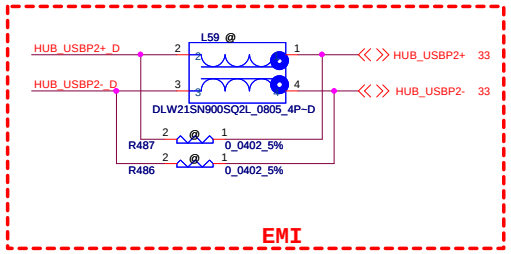
USB BOARD Conn.



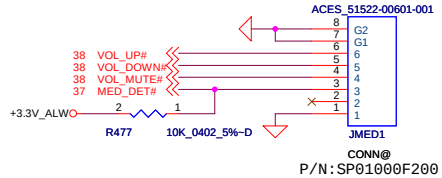


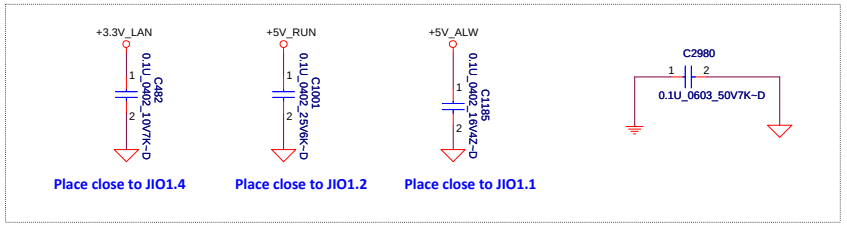
IOB Conn.



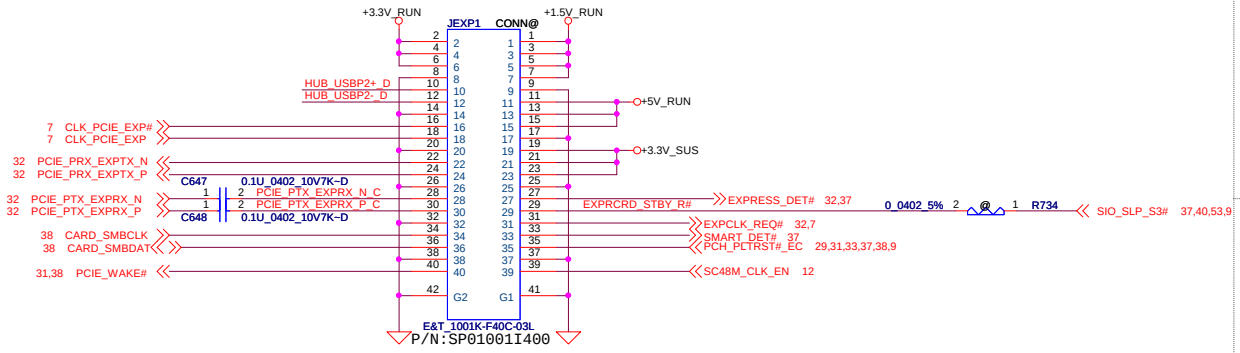


MEDIA BOARD Conn.

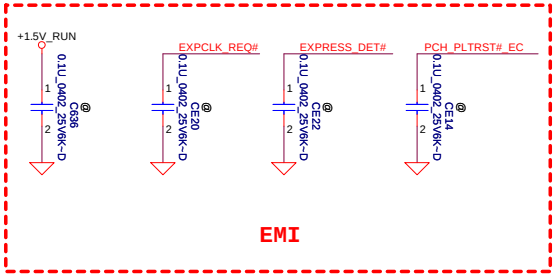


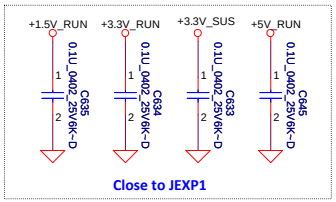


Express/Smart Card Conn.

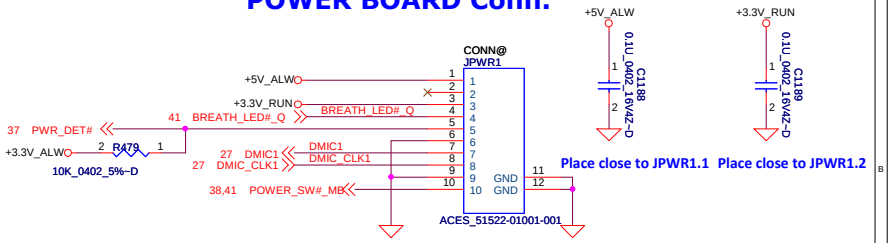


Link CIS

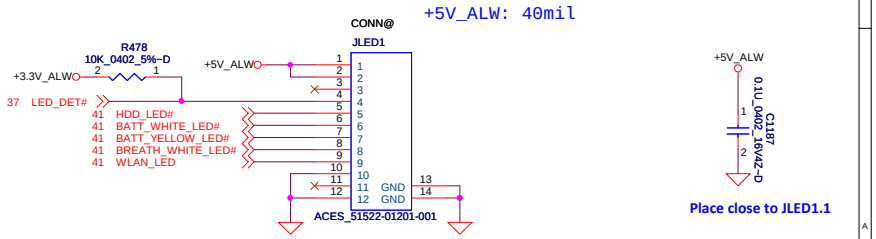




POWER BOARD Conn.



LED EXTERNAL BOARD Conn.



Compal Electronics, Inc.

Title: I/O Conn

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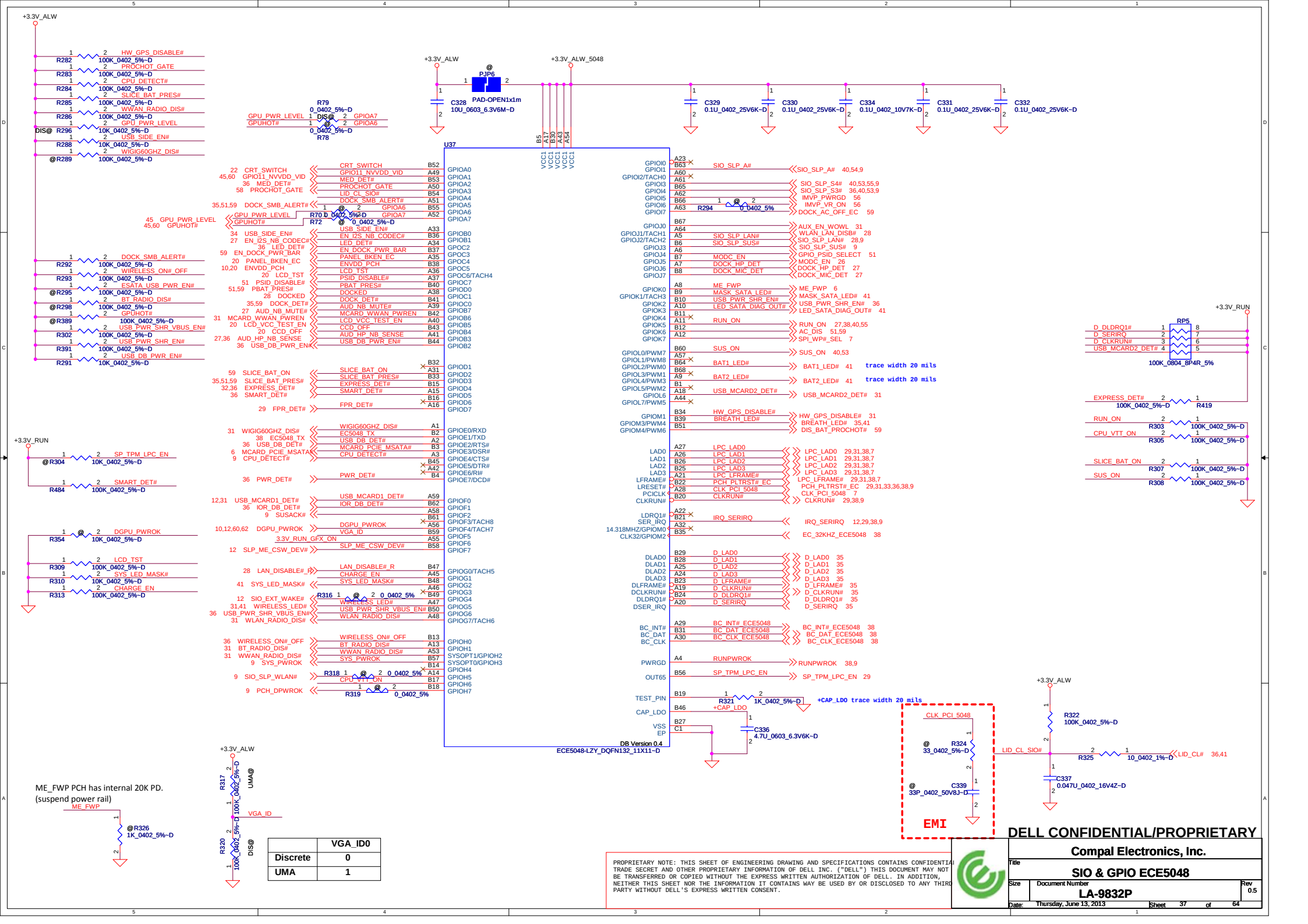
+3.3V_ALW
+3.3V_ALW_5048
+3.3V_RUN
U37
ECE5048-LZY_DQFN132_11X11~D
DB Version 0.4
PAD-OPEN1x1m
C328 10U_0603_6.3V6M~D
C329 0.1U_0402_25V6K~D
C330 0.1U_0402_25V6K~D
C334 0.1U_0402_10V7K~D
C331 0.1U_0402_25V6K~D
C332 0.1U_0402_25V6K~D
C336 4.7U_0603_6.3V6K~D
C337 0.047U_0402_16V4Z~D
C339 33P_0402_50V8J~D
R79 0_0402_5%~D
R78 0_0402_5%~D
R70 0_0402_5%~D
R72 0_0402_5%~D
R316 0_0402_5%
R318 0_0402_5%
R319 0_0402_5%
R321 1K_0402_5%~D
R322 100K_0402_5%~D
R324 33_0402_5%~D
R325 10_0402_1%~D
R317 100K_0402_5%~D
R320 100K_0402_5%~D
RP5 100K_0804_8P4R_5%
R282 100K_0402_5%~D
R283 100K_0402_5%~D
R284 100K_0402_5%~D
R285 100K_0402_5%~D
R286 100K_0402_5%~D
R296 10K_0402_5%~D
R288 10K_0402_5%~D
@R289 100K_0402_5%~D
R292 100K_0402_5%~D
R293 100K_0402_5%~D
@R295 100K_0402_5%~D
@R298 100K_0402_5%~D
@R389 100K_0402_5%~D
R302 100K_0402_5%~D
R391 100K_0402_5%~D
R291 10K_0402_5%~D
@R304 10K_0402_5%~D
R484 100K_0402_5%~D
R354 10K_0402_5%~D
R309 100K_0402_5%~D
R310 10K_0402_5%~D
R313 100K_0402_5%~D
@R326 1K_0402_5%~D
R303 100K_0402_5%~D
R305 100K_0402_5%~D
R307 100K_0402_5%~D
R308 100K_0402_5%~D
R419 100K_0402_5%~D
EMI
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
SIO & GPIO ECE5048
LA-9832P
Rev 0.5
Thursday, June 13, 2013
Sheet 37 of 64
ME_FWP PCH has internal 20K PD.
(suspend power rail)
VGA_ID
Discrete 0
UMA 1
+CAP_LDO trace width 20 mils
trace width 20 mils
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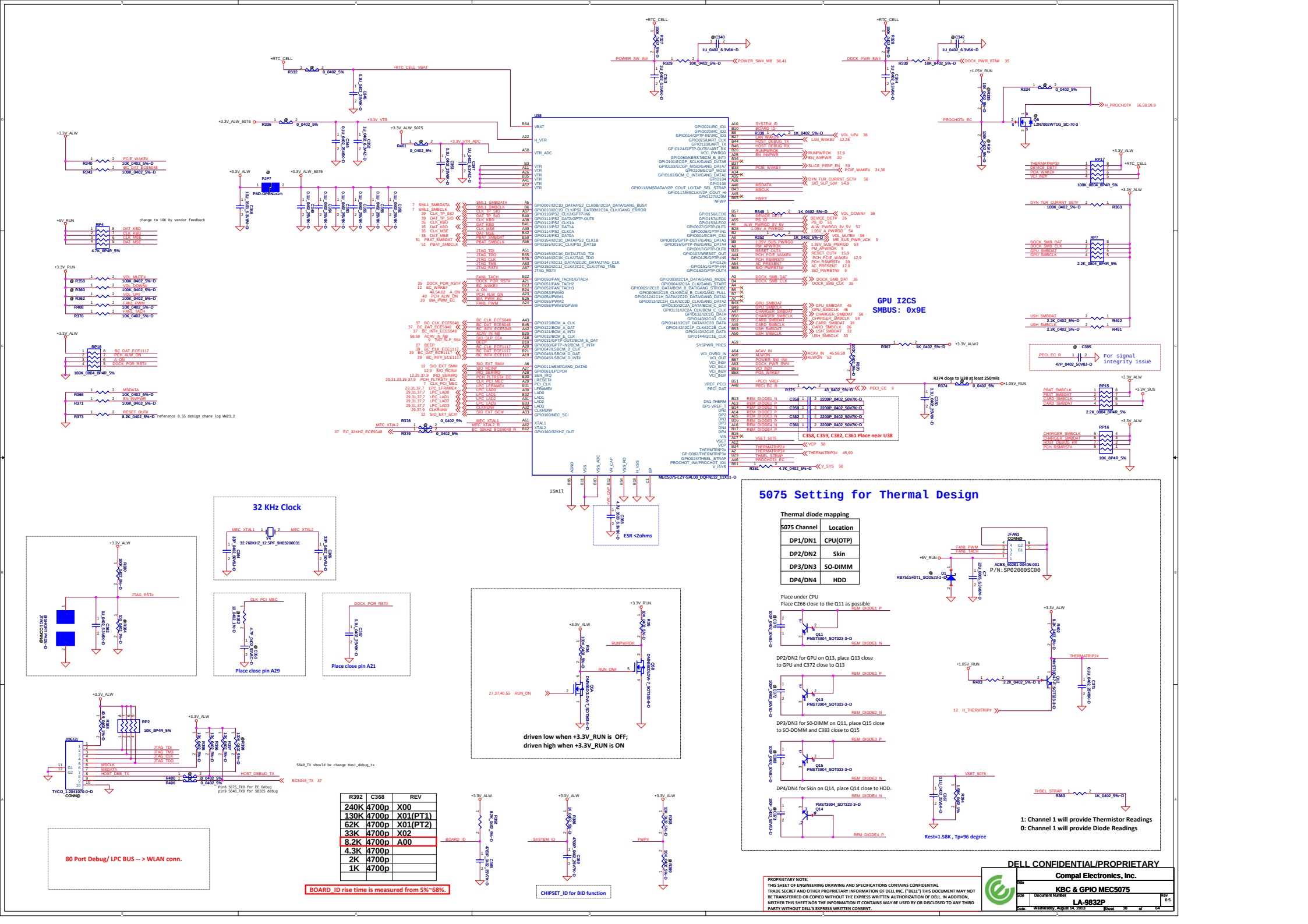
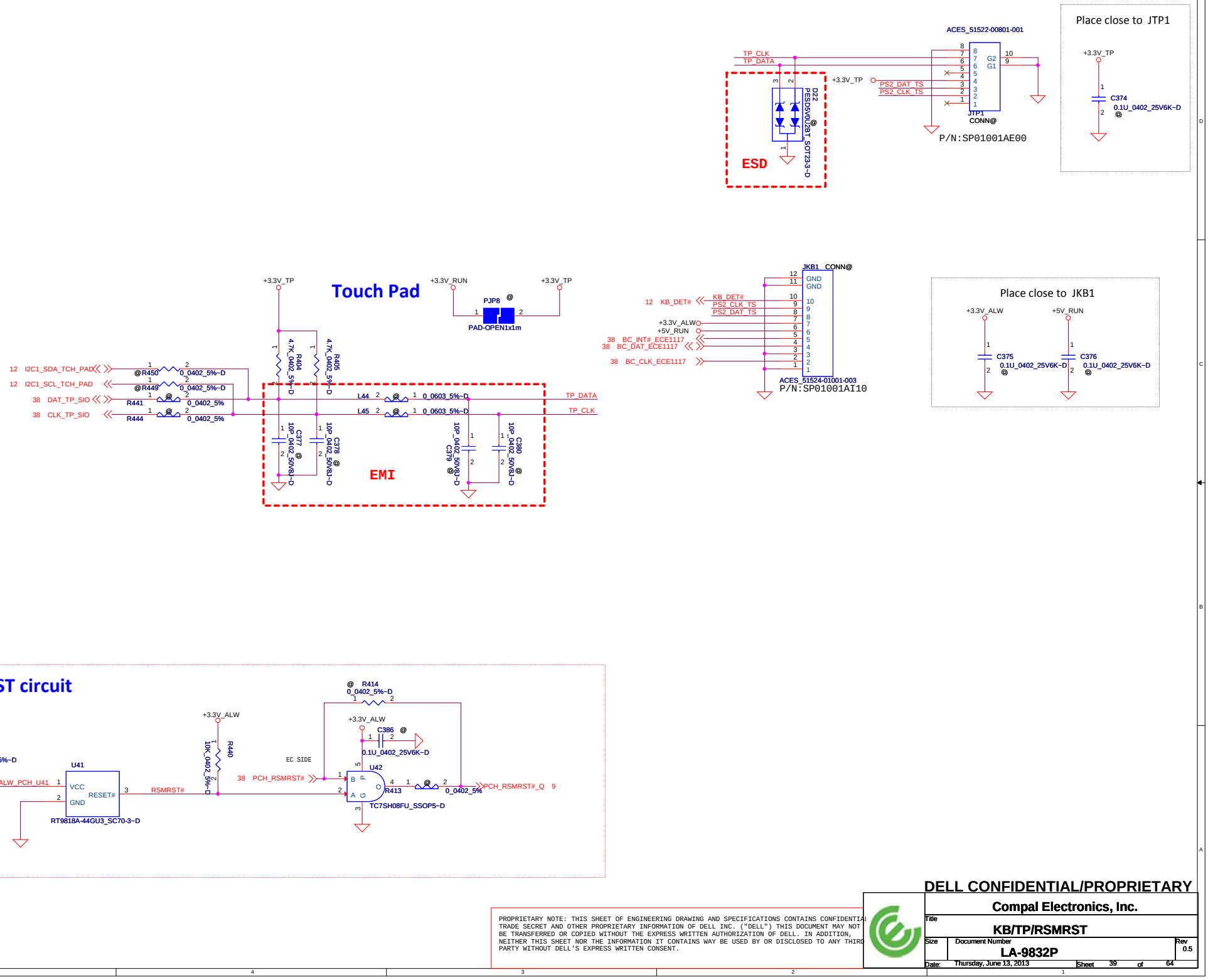

GPU I2CS
SMBUS: 0x9E
5075 Setting for Thermal Design
Thermal diode mapping
5075 Channel | Location
DP1/DN1 | CPU(OTP)
DP2/DN2 | Skin
DP3/DN3 | SO-DIMM
DP4/DN4 | HDD
Place under CPU
Place C266 close to the Q11 as possible
DP2/DN2 for GPU on Q13, place Q13 close to GPU and C372 close to Q13
DP3/DN3 for S0-DIMM on Q11, place Q15 close to SO-DOMM and C383 close to Q15
DP4/DN4 for Skin on Q14, place Q14 close to HDD.
Rest=1.58K , Tp=96 degree
1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings
C358, C359, C382, C361 Place near U38
ESR <2ohms
32 KHz Clock
32.768KHZ_12.5PF_9H03200031
Place close pin A29
Place close pin A21
driven low when +3.3V_RUN is OFF;
driven high when +3.3V_RUN is ON
80 Port Debug/ LPC BUS -- > WLAN conn.
BOARD_ID rise time is measured from 5%~68%.
CHIPSET_ID for BID function
R392 | C368 | REV
240K | 4700p | X00
130K | 4700p | X01(PT1)
62K | 4700p | X01(PT2)
33K | 4700p | X02
8.2K | 4700p | A00
4.3K | 4700p
2K | 4700p
1K | 4700p
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
KBC & GPIO MEC5075
LA-9832P
Wednesday, August 14, 2013


ACES_51522-00801-001
TP_CLK
TP_DATA
+3.3V_TP
PS2_DAT_TS
PS2_CLK_TS
JTP1
CONN@
P/N:SP01001AE00
D22
PESD5V0U2BT_SOT23-3-D
ESD
Place close to JTP1
C374
0.1U_0402_25V6K-D
Touch Pad
+3.3V_RUN
PJP8
PAD-OPEN1x1m
12 I2C1_SDA_TCH_PAD
12 I2C1_SCL_TCH_PAD
38 DAT_TP_SIO
38 CLK_TP_SIO
R450
R449
R441
R444
0_0402_5%-D
0_0402_5%
4.7K_0402_5%-D
R404
R405
L44
L45
0_0603_5%-D
TP_DATA
TP_CLK
C377
C378
C379
C380
10P_0402_50V8J-D
EMI
JKB1 CONN@
ACES_51524-01001-003
P/N:SP01001AI10
12 KB_DET#
38 BC_INT#_ECE1117
38 BC_DAT_ECE1117
38 BC_CLK_ECE1117
+3.3V_ALW
+5V_RUN
GND
Place close to JKB1
C375
C376
0.1U_0402_25V6K-D
RSMRST circuit
+5V_ALW
R411
33_0402_5%-D
U41
VCC
RESET#
GND
RT9818A-44GU3_SC70-3-D
+3.3V_ALW_PCH_U41
RSMRST#
C387
0.01U_0402_16V7K-D
R440
10K_0402_5%-D
EC SIDE
38 PCH_RSMRST#
R414
0_0402_5%-D
C386
0.1U_0402_25V6K-D
U42
R413
TC7SH08FU_SSOP5-D
PCH_RSMRST#_Q 9
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Title
KB/TP/RSMRST
Size
Document Number
LA-9832P
Rev
0.5
Date: Thursday, June 13, 2013
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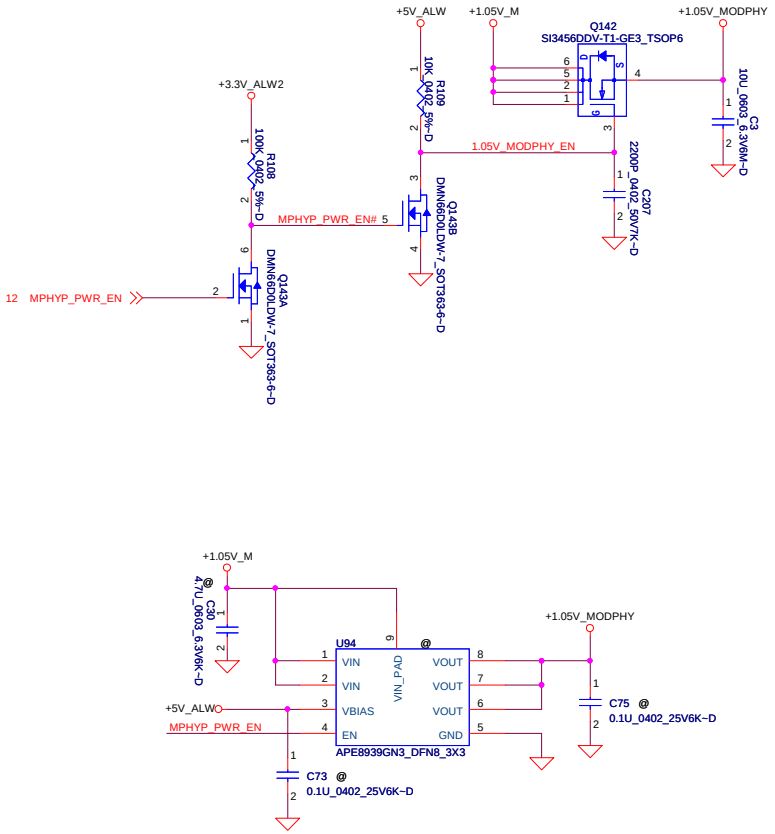
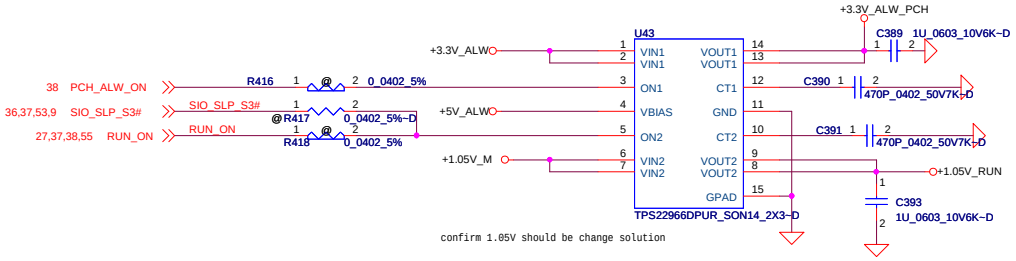
DC/DC Interface

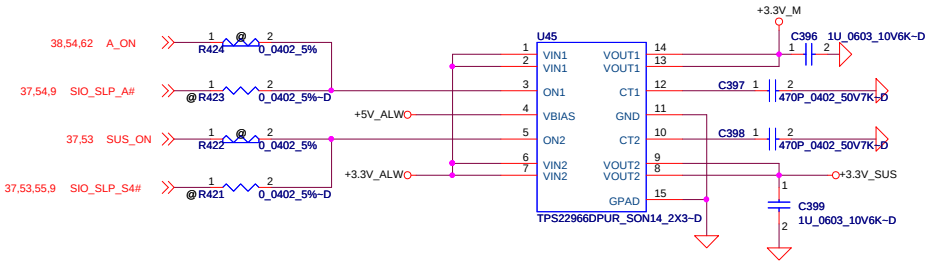
+1.05V_MODPHY source



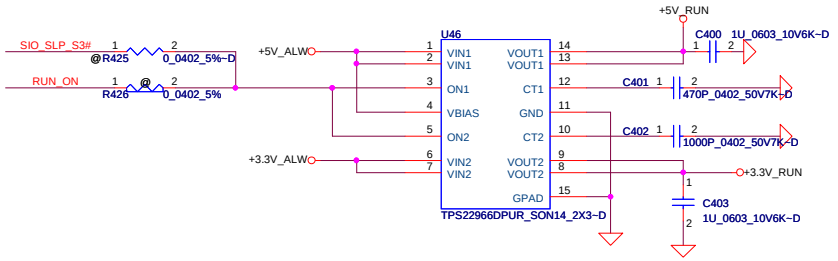
+3.3V_ALW_PCH/+1.05V_RUN source



+3.3V_SUS/+3.3V_M source



+3.3V_RUN/+5V_RUN source



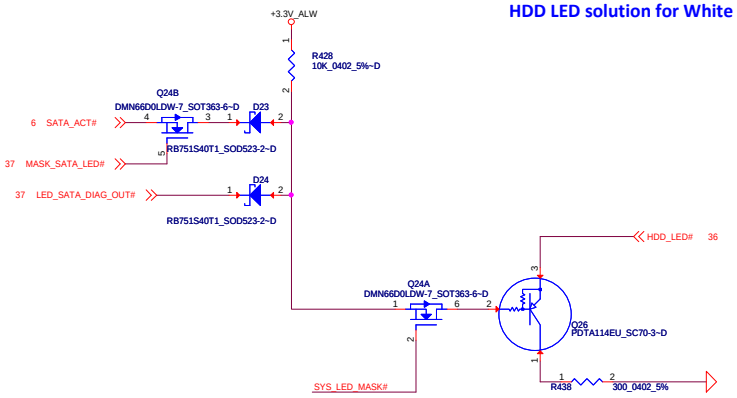
Compal Electronics, Inc.

Title: POWER CONTROL

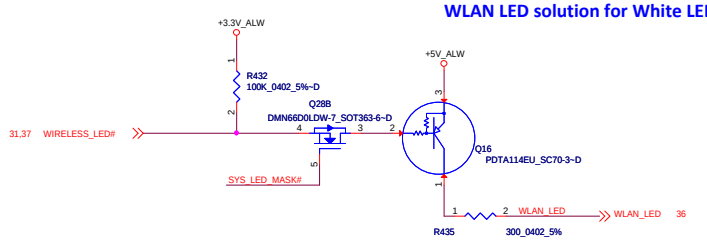
Size | Document Number: LA-9832P | Rev: 0.5

Date: Thursday, June 13, 2013 | Sheet 40 of 64

HDD LED solution for White LED



WLAN LED solution for White LED

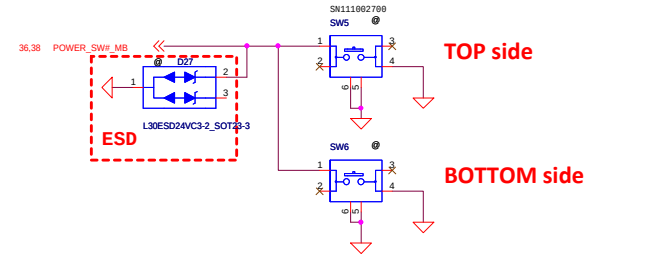


Battery LED

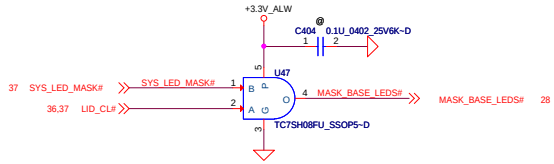
Breath LED

POWER & INSTANT ON SWITCH

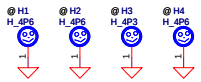
Need to change as ALW17 power switch.



Lid has beed moved to DB.



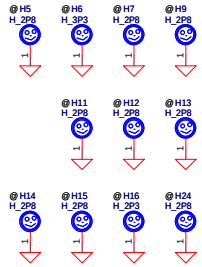
CPU stand-off hole :
Φ4.3mm X 1, Φ4.6mm X 3



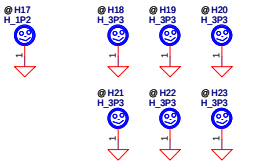
Screw hole Φ5.0mm X 1

Screw hole Φ3.3mmx2.8mm X 1

Screw hole Φ3.3mm X 1, Φ2.8mm X 14, Φ2.3mm X 1



Stand-off hole Φ3.3mm X 7,Φ1.2mm X 1



Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

LED Circuit Control Table

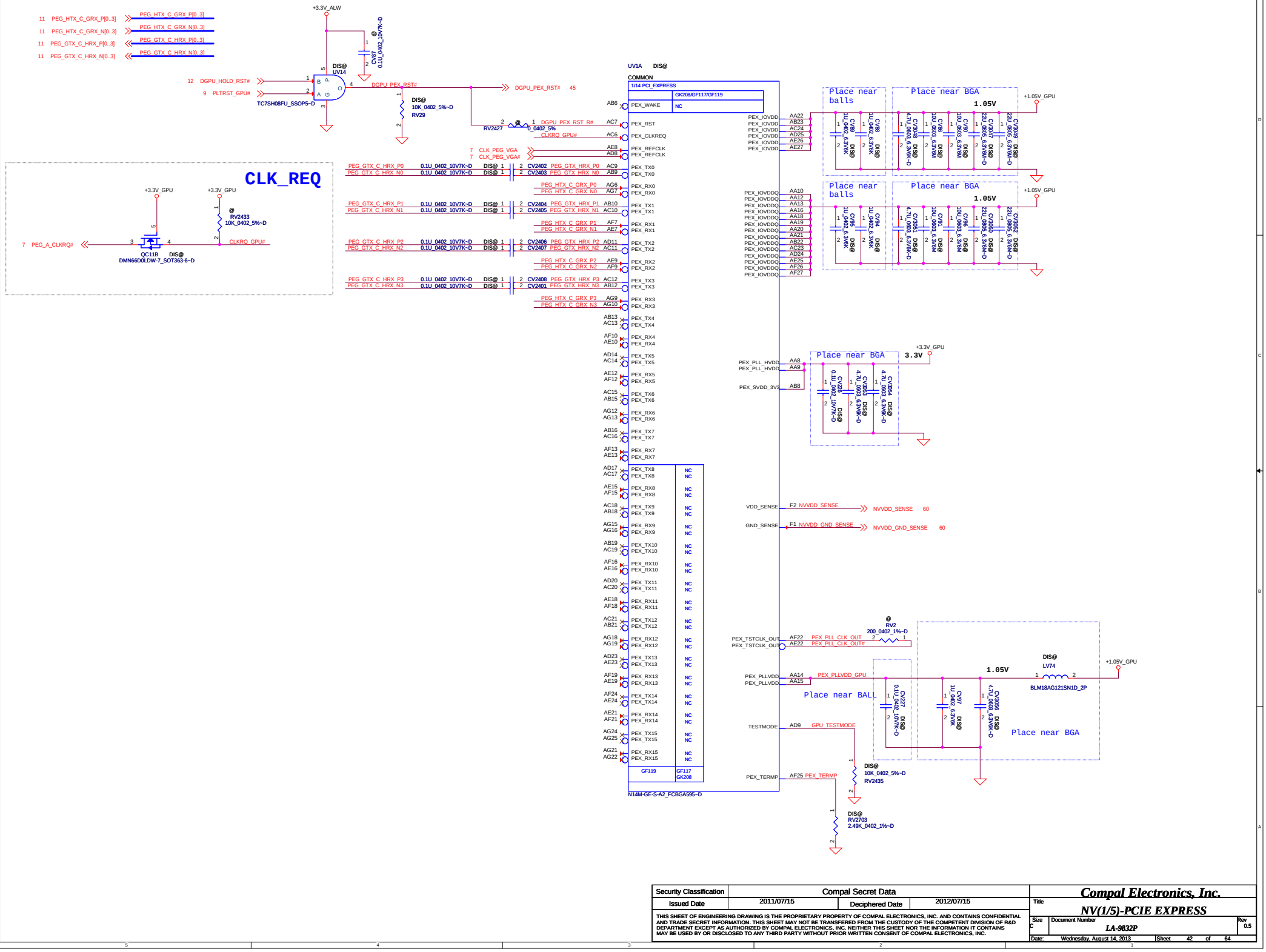
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Compal Electronics, Inc.

Title: PAD & ME & LED

Size: | Document Number: LA-9832P | Rev: 0.5

Date: Wednesday, August 14, 2013 | Sheet 41 of 64



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **NV(1/5)-PCIE EXPRESS**

Size	Document Number	Rev
C	LA-9832P	0.5

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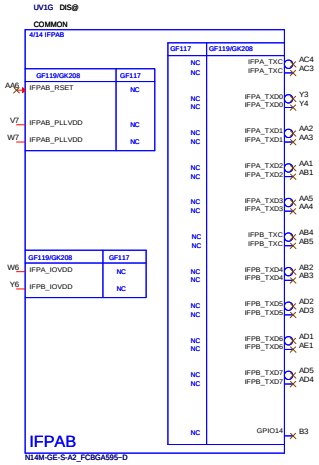
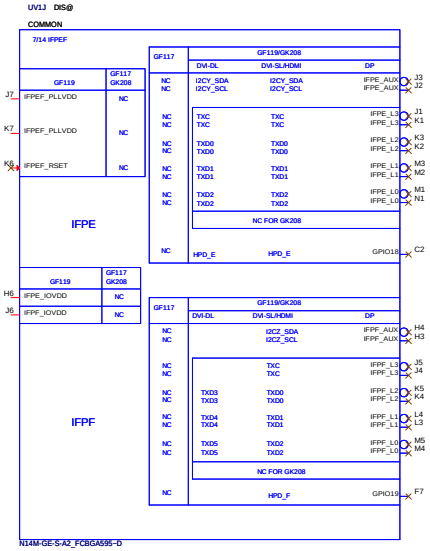
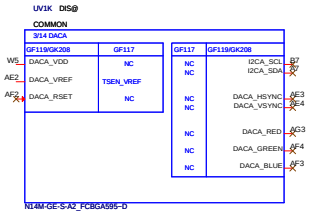
IFPA/B



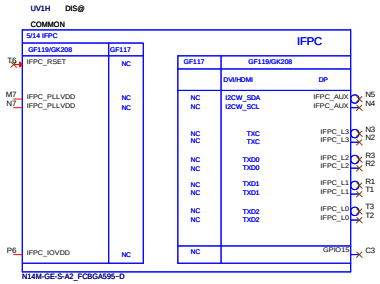
IFPE/F



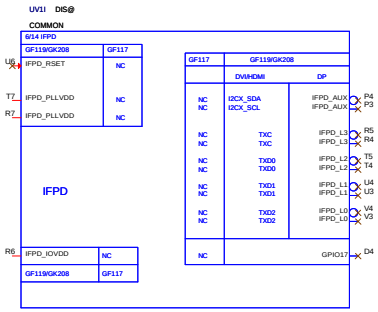
DAC_A



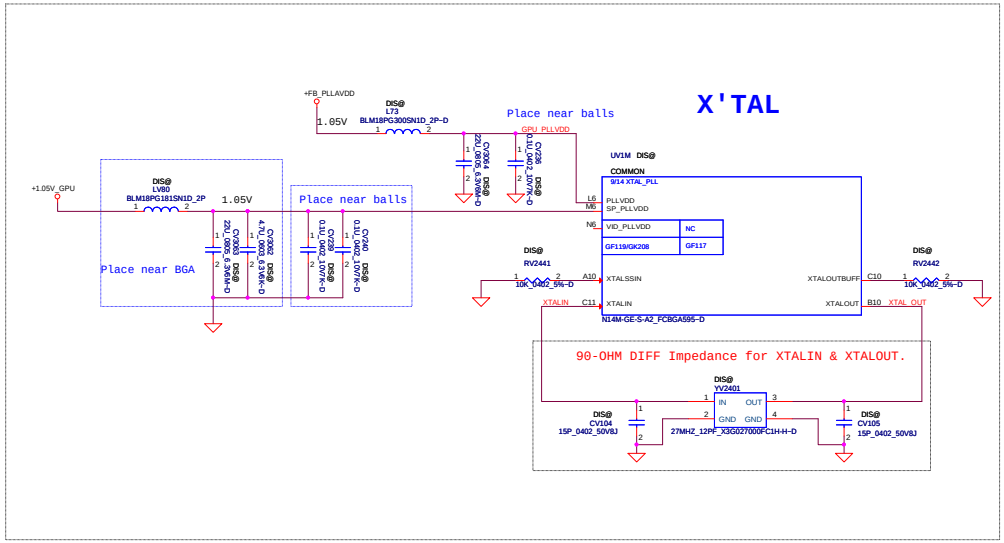
IFPC



IFPD

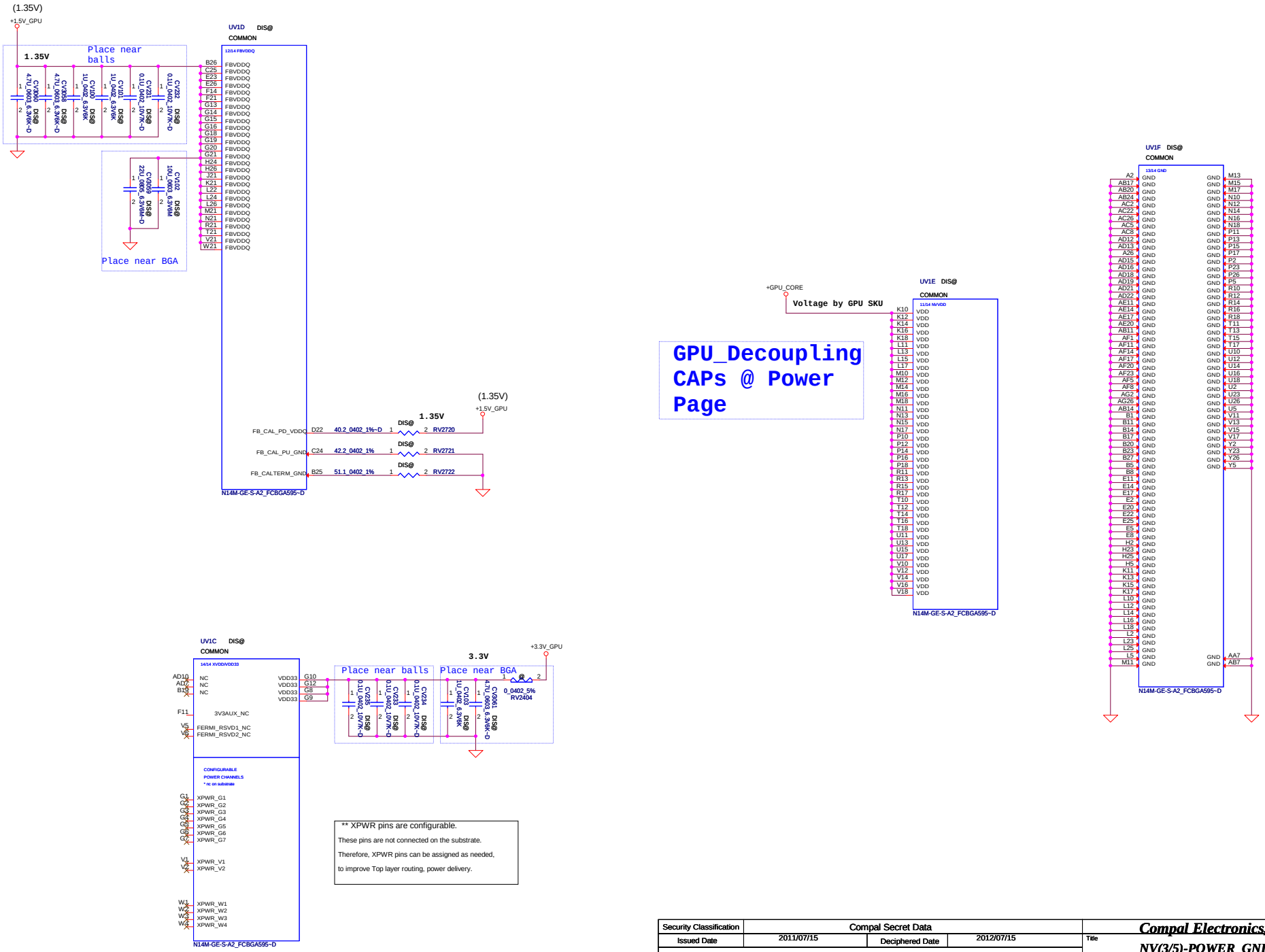


X'TAL



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.			
Title	NV(2/5)-IFP_ABCDEF_DAC_XTAL		
Size: Custom	Document Number: LA-9632P		Rev: 0.5
Date: Wednesday, August 14, 2013	Sheet 43 of 64		



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: NV(3/5)-POWER_GND

Size: C | Document Number: LA-9832P | Rev: 0.5

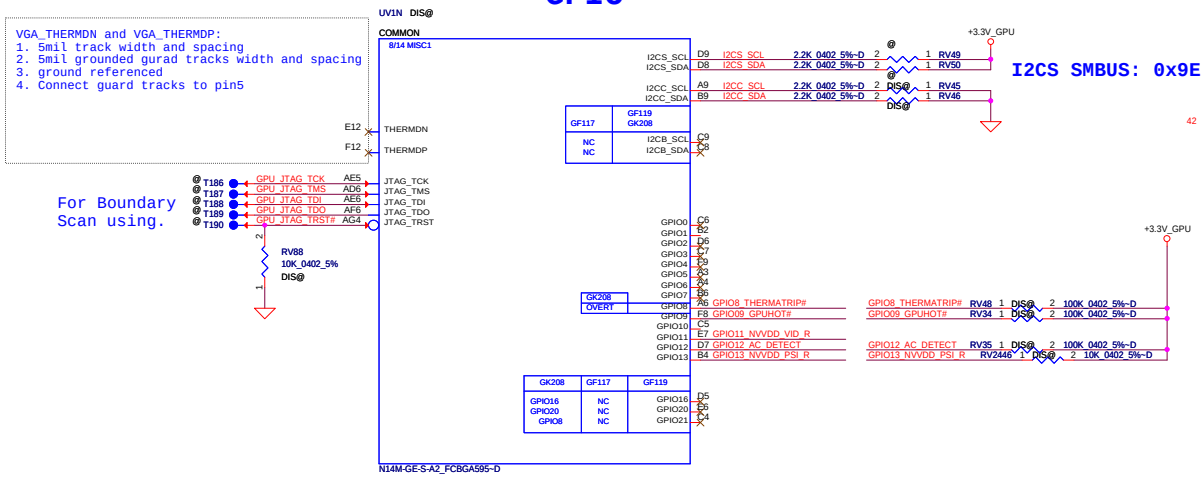
Date: Wednesday, August 14, 2013 | Sheet 44 of 64

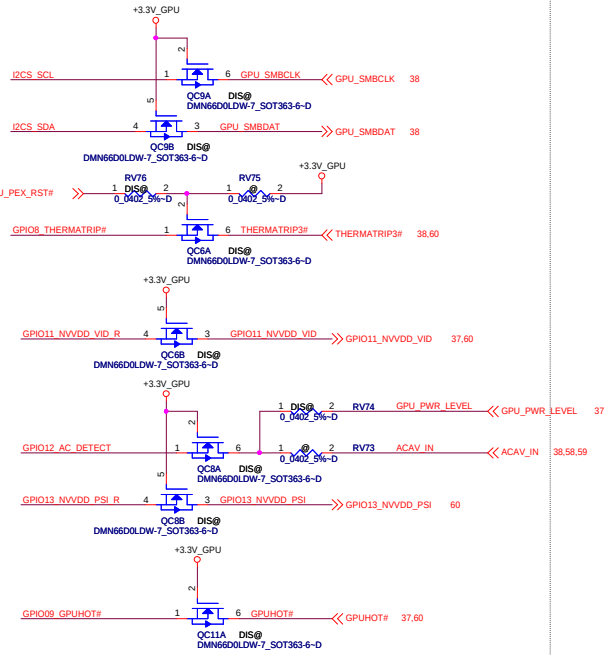
GPIO

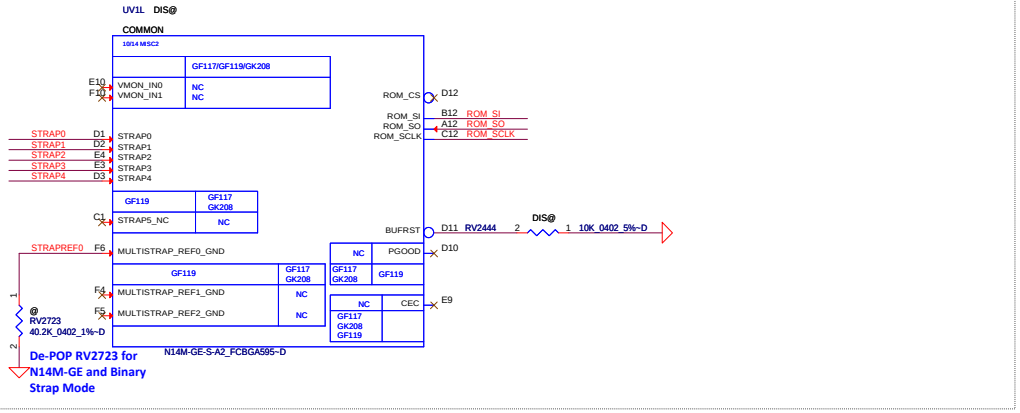
VGA_THERMDN and VGA_THERMDP:
1. 5mil track width and spacing
2. 5mil grounded gurad tracks width and spacing
3. ground referenced
4. Connect guard tracks to pin5

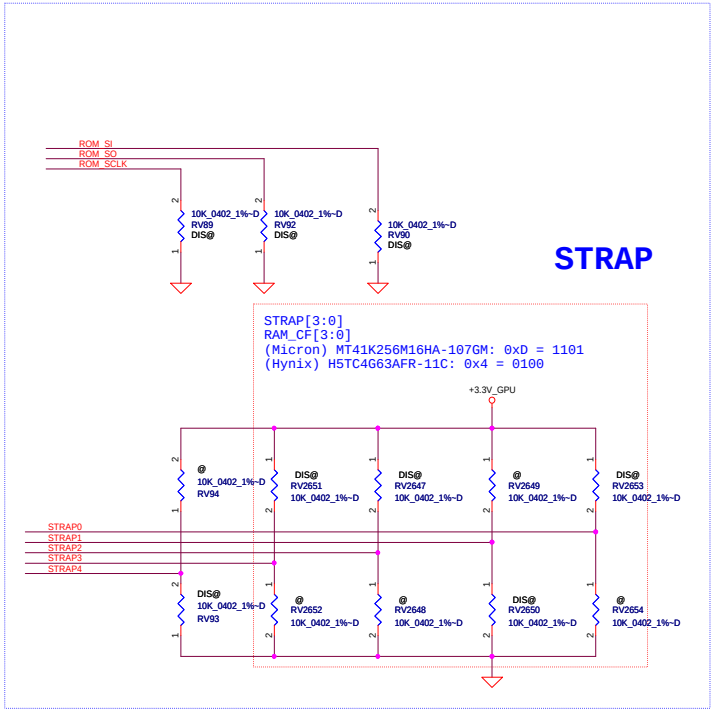
For Boundary Scan using.

I2CS SMBUS: 0x9E



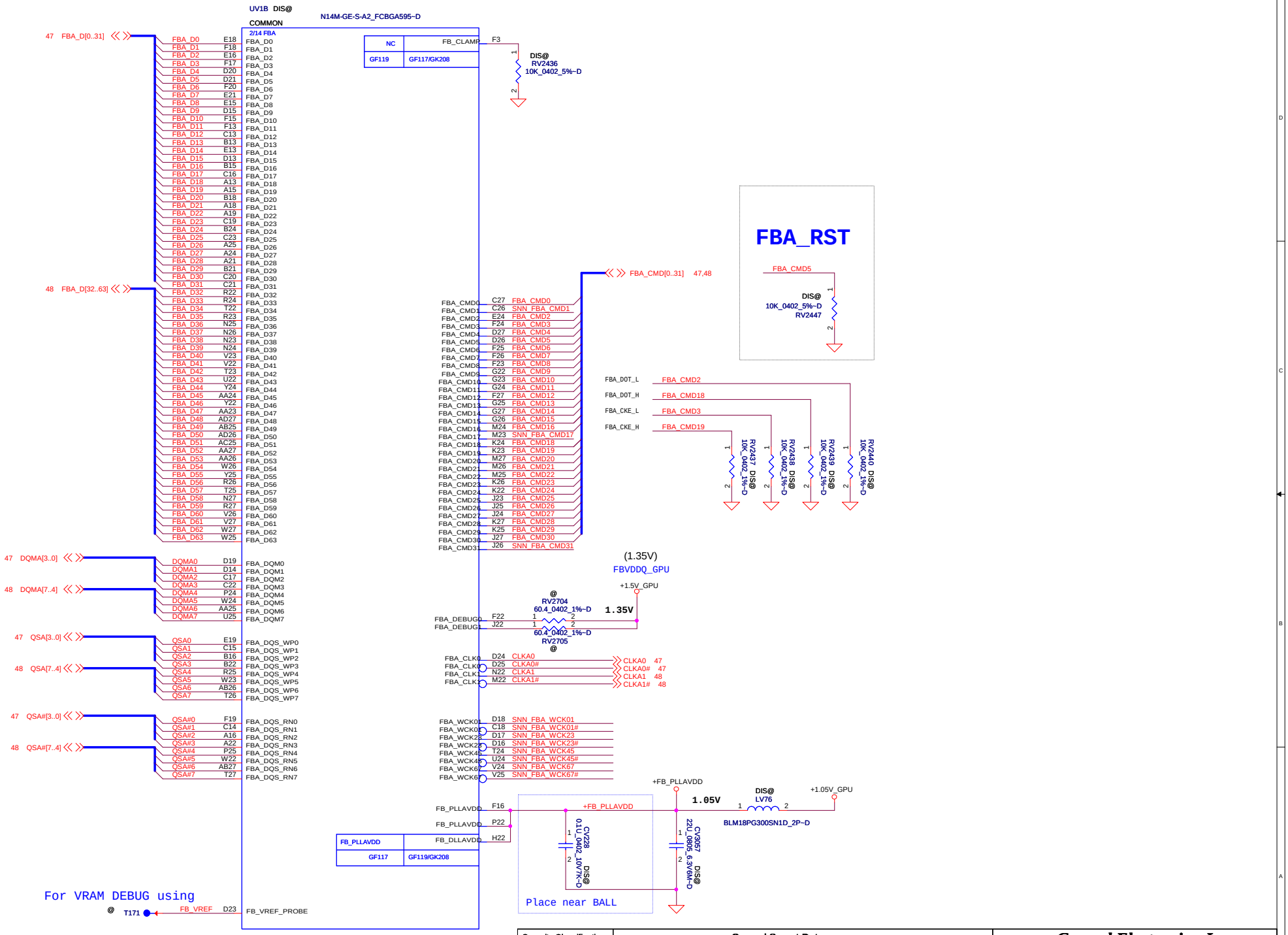






Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.			
Title	NV(4/5)-GPIO_BIOS_STRAP		
Size C	Document Number LA-9832P		Rev 0.5
Date: Wednesday, August 14, 2013	Sheet 45 of 64		



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **NV(5/5)-MEMORY FBA**

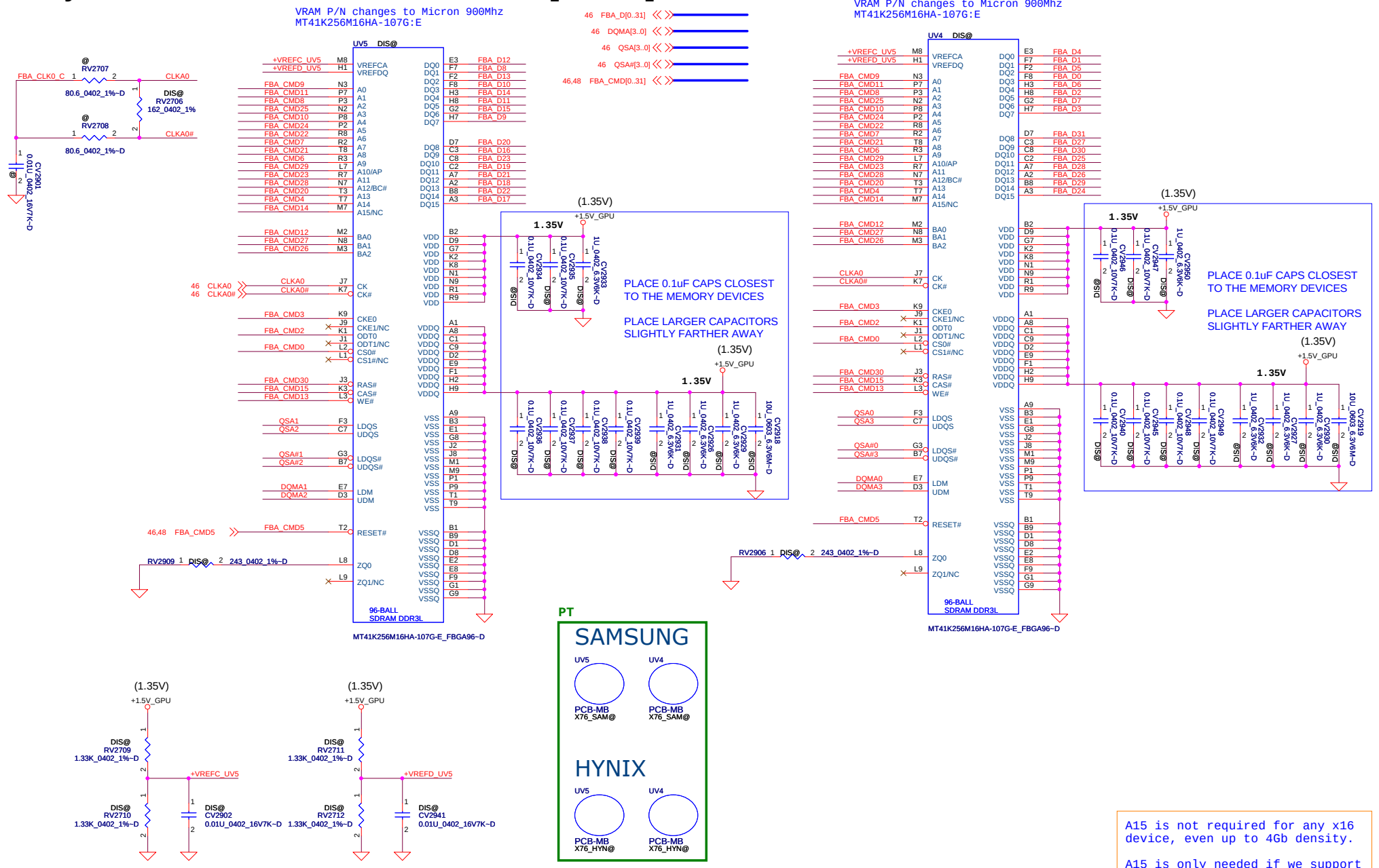
Size	Document Number	Rev
Custom	LA-9832P	0.5

Date: Wednesday, August 14, 2013 Sheet 46 of 64

Memory Partition A - Lower 32 bits [31..0]

VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E

VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E



PT

SAMSUNG

UV5 — PCB-MB X76_SAM@

UV4 — PCB-MB X76_SAM@

HYNIX

UV5 — PCB-MB X76_HYN@

UV4 — PCB-MB X76_HYN@

A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

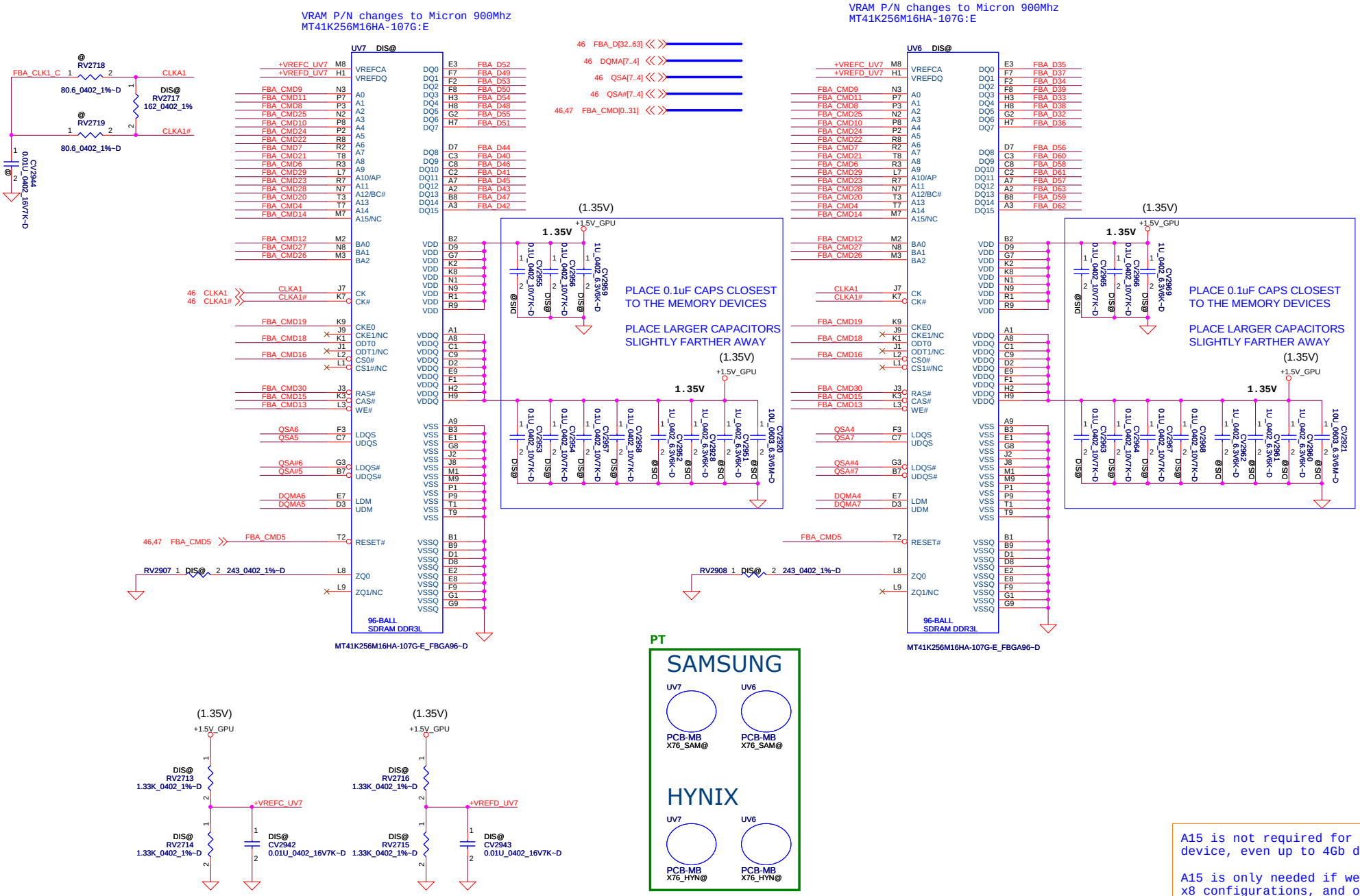
Compal Electronics, Inc.

Title: VRAM_DDR3_A Lower

Size: Custom | Document Number: LA-9832P | Rev: 0.5

Date: Thursday, June 13, 2013 | Sheet 47 of 64

Memory Partition A - Upper 32 bits [64..32]



A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

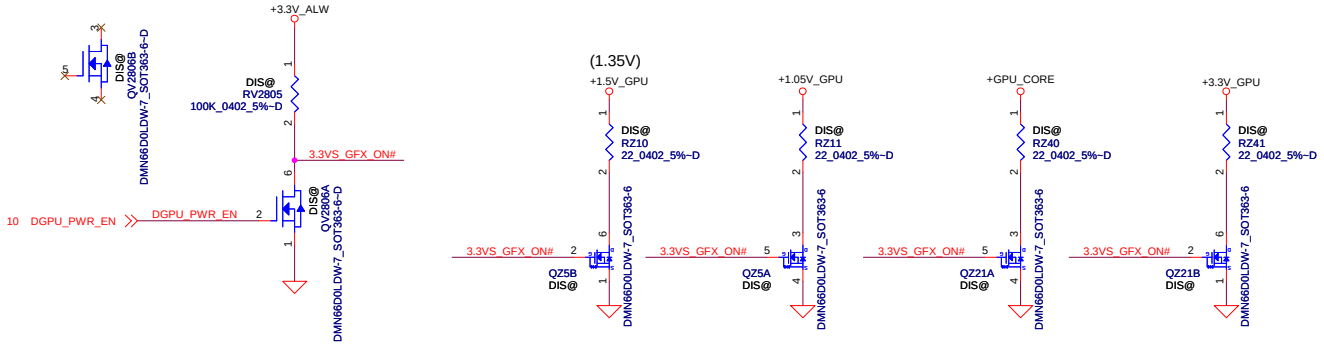
Compal Electronics, Inc.

Title: VRAM_DDR3_A Upper

Size	Document Number	Rev
Custom	LA-9832P	0.5

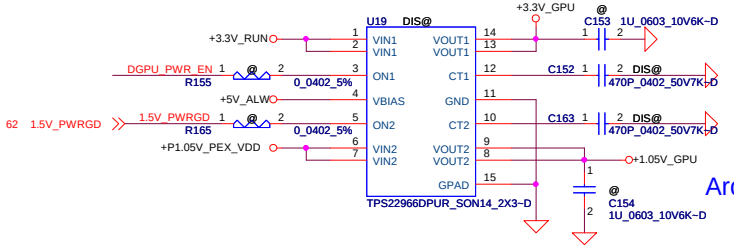
Date: Wednesday, August 14, 2013 Sheet 48 of 64

GPU Power Discharge Path



+3.3VRUN to +3.3V_RUN_GFX

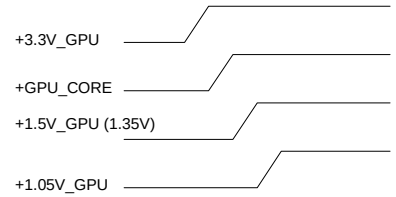
Around 1.4 A



Around 3 A

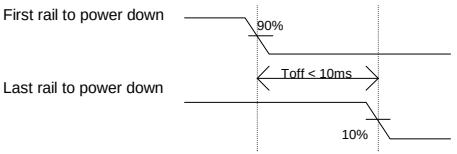
+1.05V_MP to +1.05V_PEX_VDD

GPU Power Up Power Rail Sequence

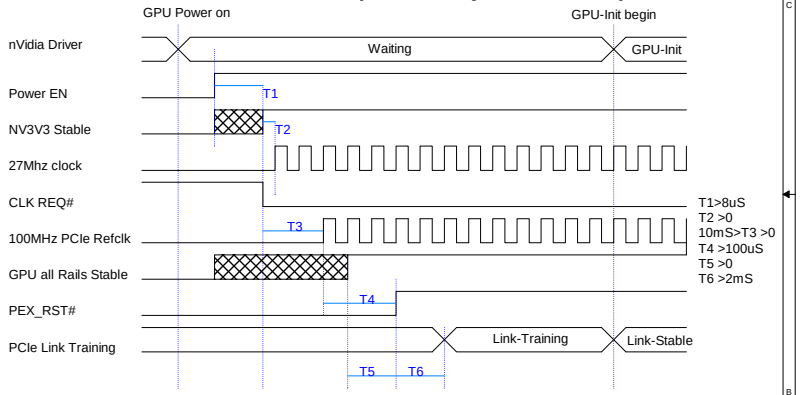


The ramp time for any rail must be more than 40us.

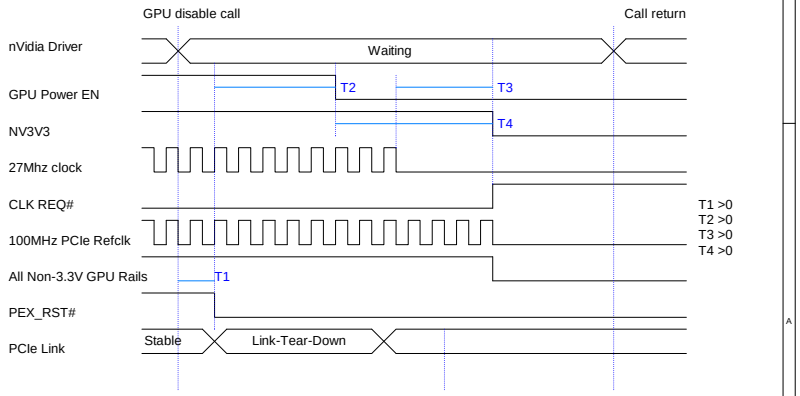
GPU Power Down Sequence



GPU Power Up Sub-system Sequence



GPU Power Down Sub-system Sequence



Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

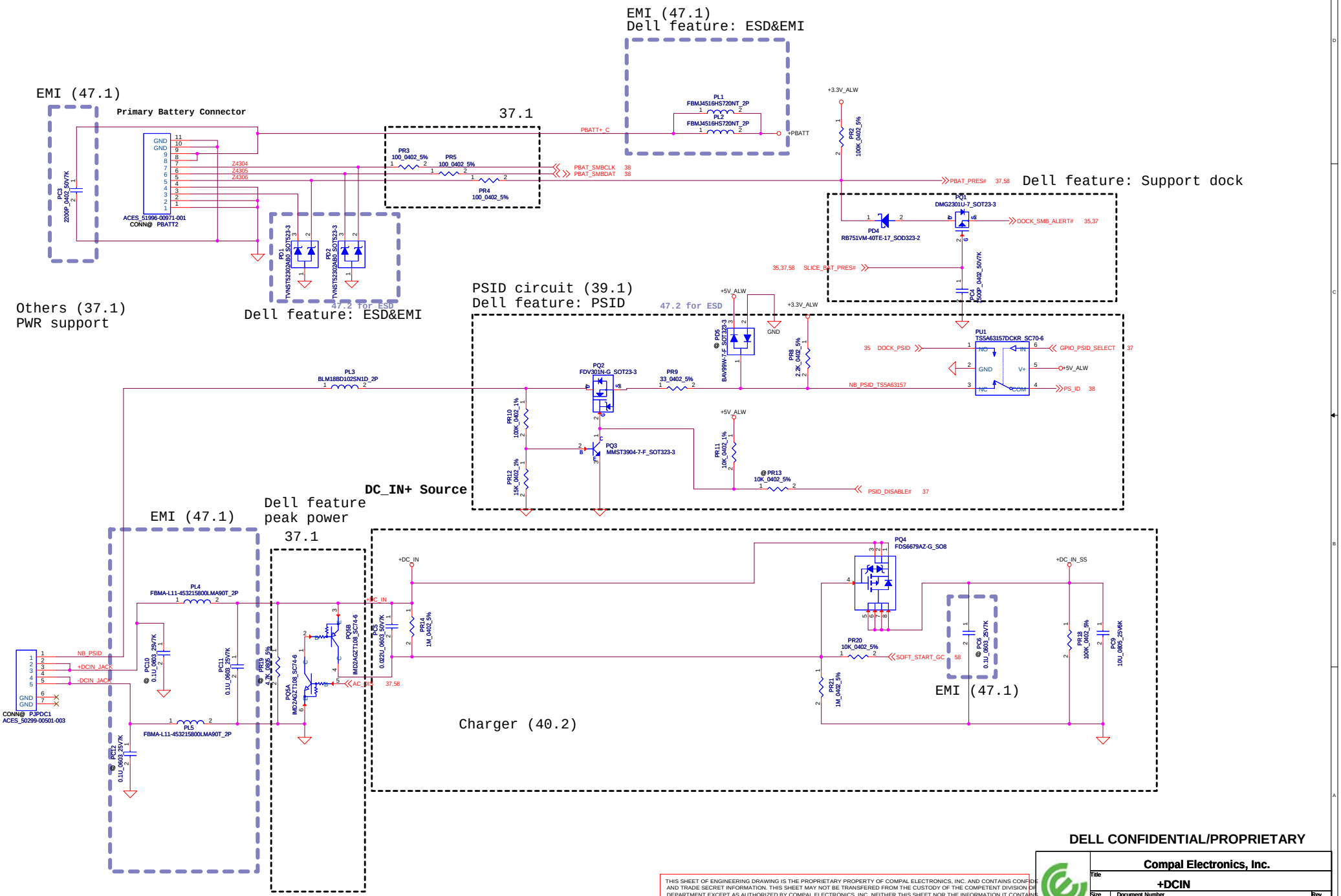
Title: **VGA_DC/DC Interface**

Size | Document Number | Rev 0.5

Date: Thursday, August 15, 2013 | Sheet 49 of 64

BLANK PAGE

	Compal Electronics, Inc.	
Title	BLANK PAGE	
Size	Document Number LA-9832P	Rev 0.5
Date: Thursday, June 13, 2013	Sheet 50 of 64	



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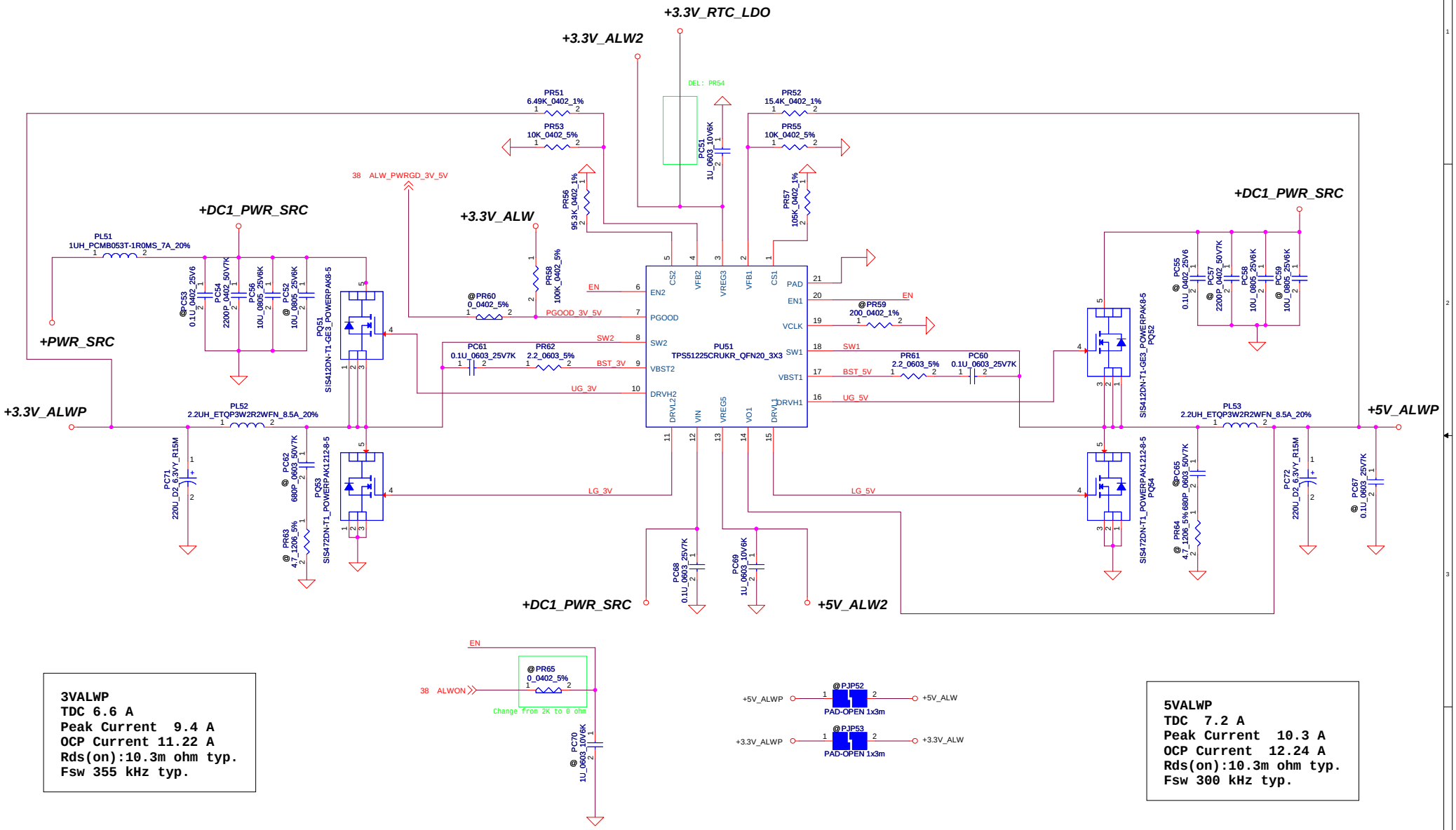
Compal Electronics, Inc.		
Title: +DCIN		
Size	Document Number: LA-XXXX	Rev: 0.1
Date: Wednesday, August 14, 2013	Sheet 51 of 64	



3VALWP
TDC 6.6 A
Peak Current 9.4 A
OCP Current 11.22 A
Rds(on):10.3m ohm typ.
Fsw 355 kHz typ.

5VALWP
TDC 7.2 A
Peak Current 10.3 A
OCP Current 12.24 A
Rds(on):10.3m ohm typ.
Fsw 300 kHz typ.

Compal Electronics, Inc.	
Title	PWR_+5V_ALW/3.3V_ALW
Size	Document Number: LA-XXXX
Rev	0.1
Date:	Wednesday, August 14, 2013
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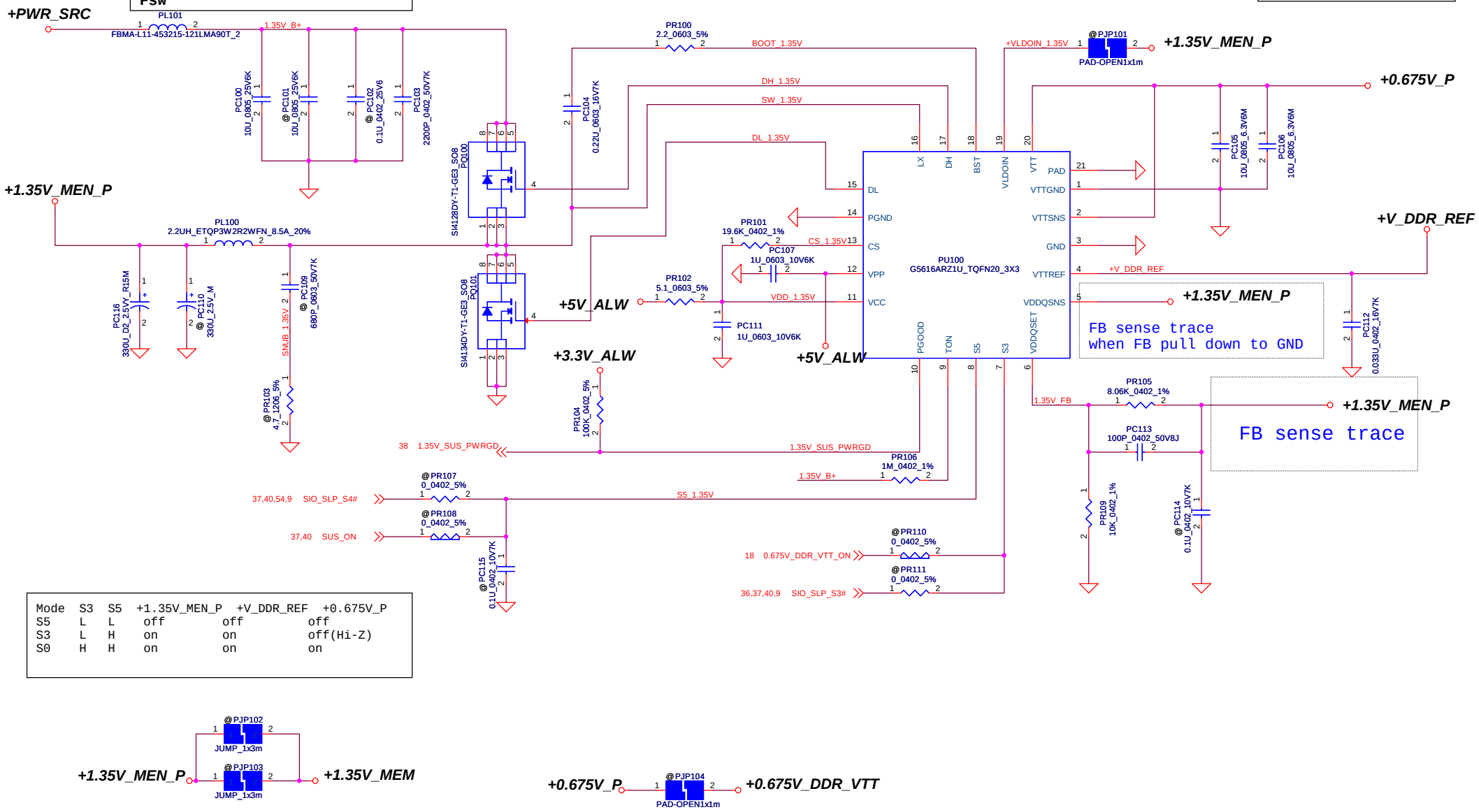
1.35Volt +/- 5%
TDC: 7.2 A
Peak Current: 10.3 A
OCP current: 12.24 A
Rds(on):14.5m ohm typ
Fsw

0.675Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.8925A



Mode	S3	S5	+1.35V_MEN_P	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off(Hi-Z)
S0	H	H	on	on	on

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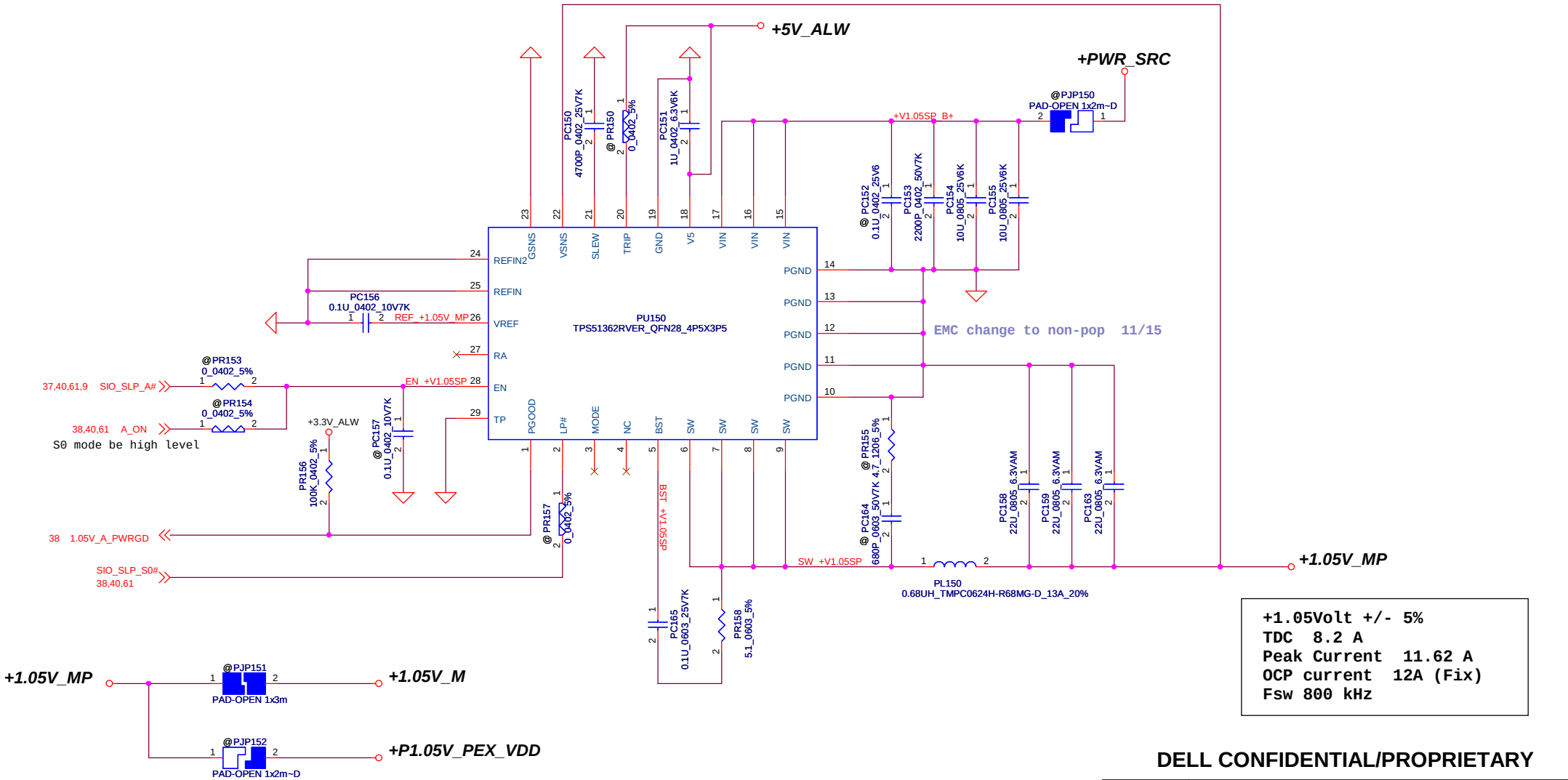
Compal Electronics, Inc.

Title: PWR_+1.35V_MEN/+0.675V_DDR

Size | Document Number: LA-XXXX | Rev: 0.1

Date: Wednesday, August 14, 2013 | Sheet 53 of 64



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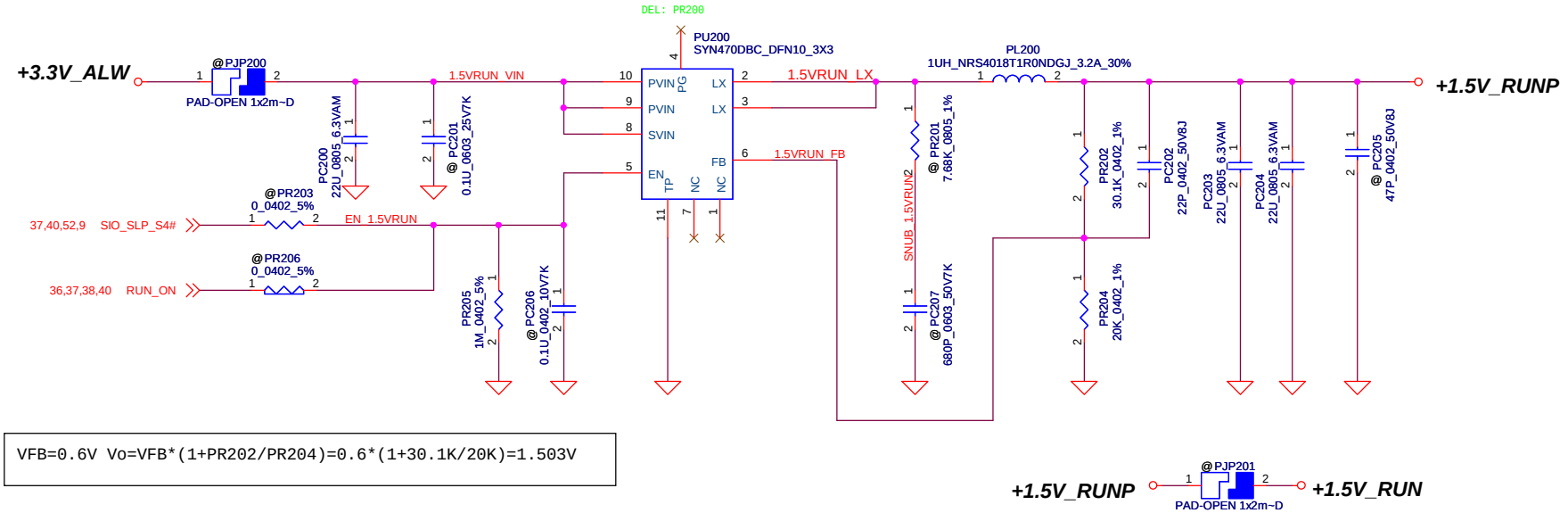
Compal Electronics, Inc.		
Title: PWR_+1.05VTTP		
Size	Document Number: LA-XXXX	Rev: 0.1
Date: Wednesday, August 14, 2013	Sheet 54 of 64	

1.5Volt
Frequency 1MHz
TDC 0.65A
Peak Current 0.93A
OCP current 3.5A (Fix)



VFB=0.6V Vo=VFB*(1+PR202/PR204)=0.6*(1+30.1K/20K)=1.503V

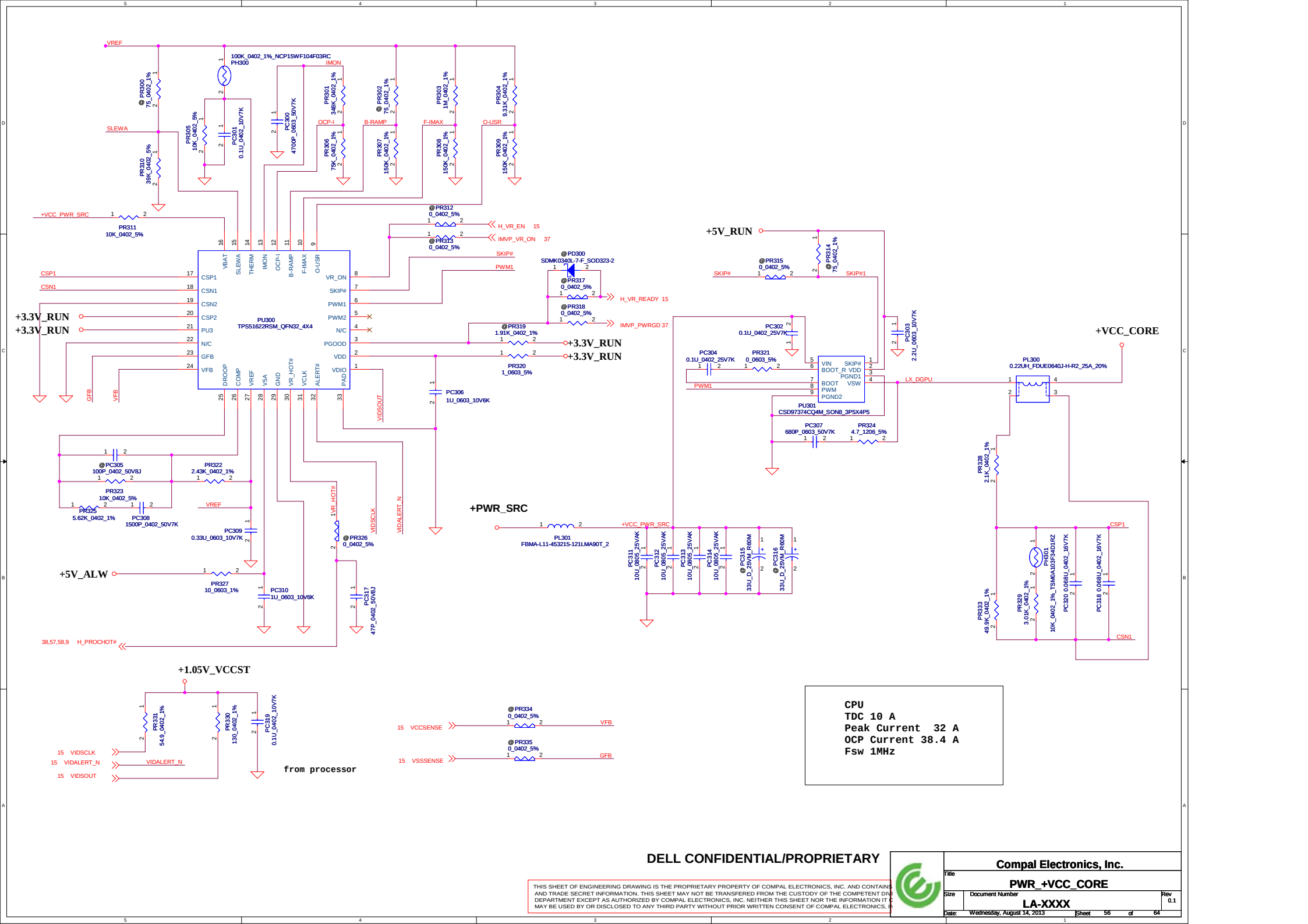
Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.

Title: PWR_1.5V_RUN

Size: B | Document Number | Rev: 1.0

Date: Wednesday, August 14, 2013 | Sheet 55 of 64

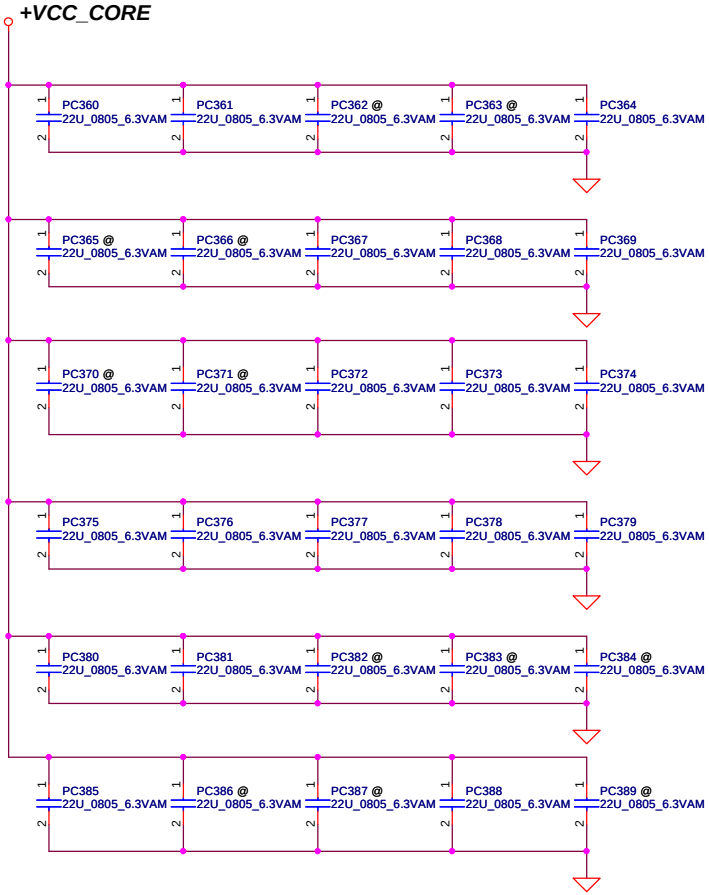


Compal Electronics, Inc.

Title: PWR_+VCC_CORE

Size: | Document Number: LA-XXXX | Rev: 0.1

Date: Wednesday, August 14, 2013 | Sheet 56 of 64



Compal Electronics, Inc.

Title: PWR_PROCESSOR DECOUPLING

Size: | Document Number: LA-XXXX | Rev: 0.1

Date: Wednesday, August 14, 2013 | Sheet 57 of 64

Charger controller (40.1)
Support Component (40.2)

Dell feature

E-dock power(41.2)
Dell feature

Adapter protection (39.7)
Dell feature: AC protect

E-dock power(41.2)
Dell feature: AC protect

	DYN_TUR_CURRENT_SET#
65W	High
90W	Low

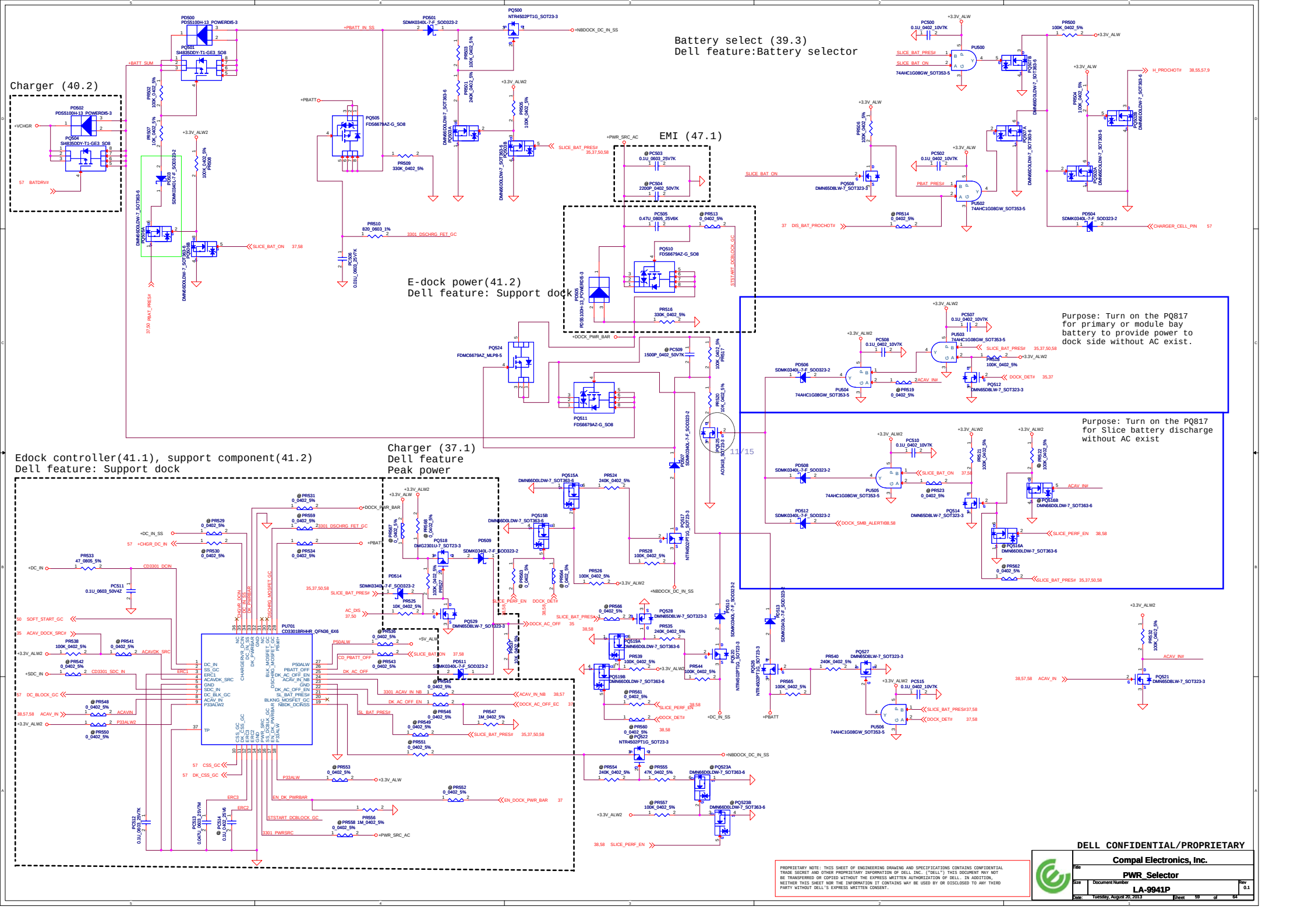
Adapter Protection Circuit for Turbo Mode

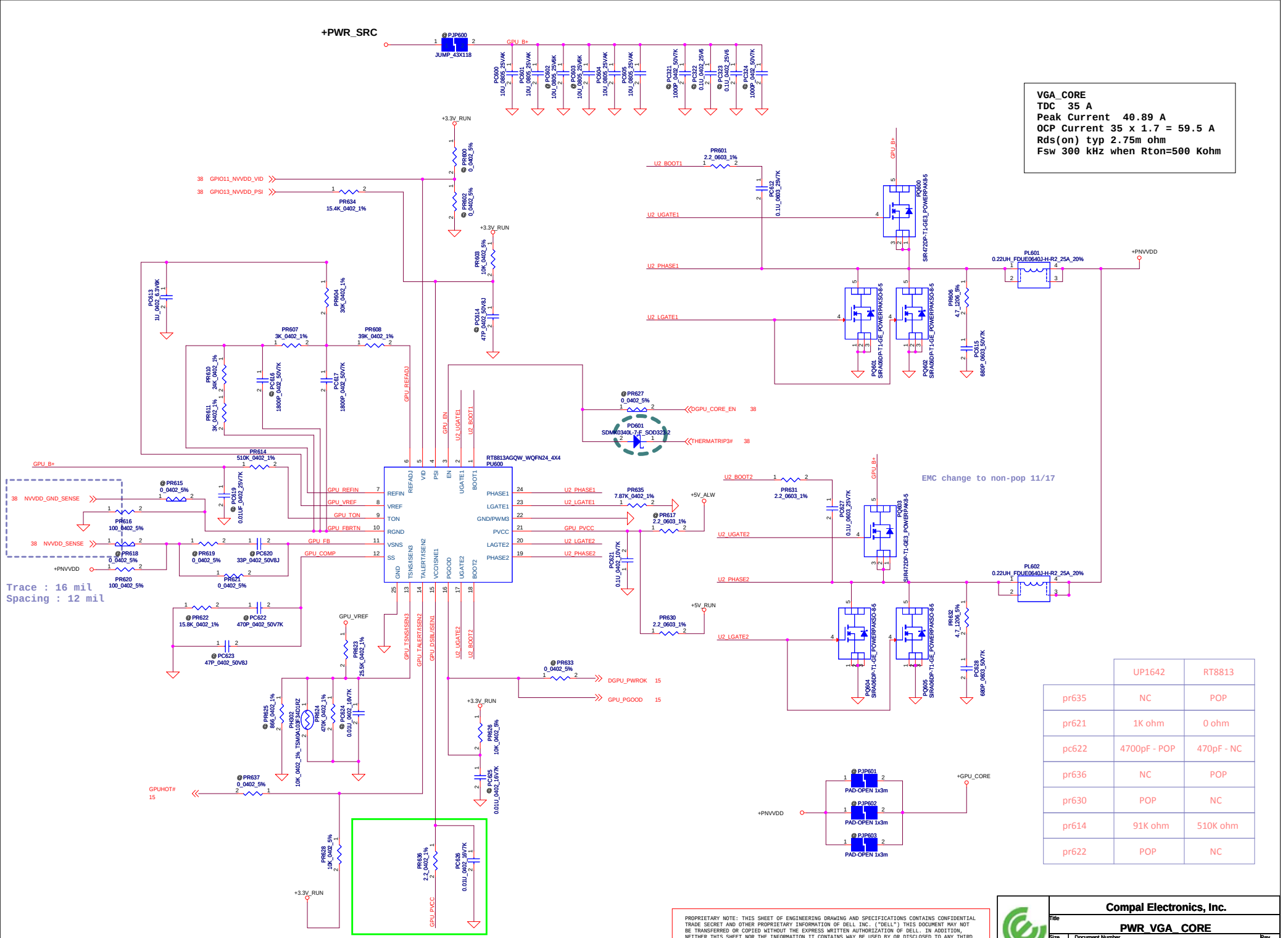
Compal Electronics, Inc.

Title: PWR_Chager

Size: | Document Number: LA-XXXX | Rev: 0.1

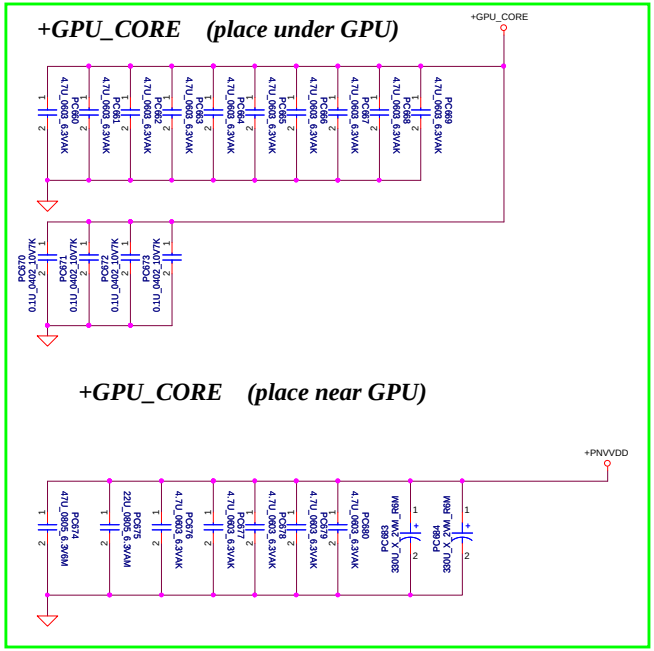
Date: Wednesday, August 14, 2013 | Sheet 58 of 64


Charger (40.2)
Battery select (39.3)
Dell feature:Battery selector
EMI (47.1)
E-dock power(41.2)
Dell feature: Support dock
Purpose: Turn on the PQ817 for primary or module bay battery to provide power to dock side without AC exist.
Purpose: Turn on the PQ817 for Slice battery discharge without AC exist
Edock controller(41.1), support component(41.2)
Dell feature: Support dock
Charger (37.1)
Dell feature
Peak power
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
PWR_Selector
LA-9941P
Tuesday, August 20, 2013



	UP1642	RT8813
pr635	NC	POP
pr621	1K ohm	0 ohm
pc622	4700pF - POP	470pF - NC
pr636	NC	POP
pr630	POP	NC
pr614	91K ohm	510K ohm
pr622	POP	NC

Compal Electronics, Inc.
Title: PWR_VGA_CORE
Size: Document Number: LA-XXXX
Rev: 0.1
Date: Wednesday, August 14, 2013
Sheet 60 of 64



Compal Electronics, Inc.

Title: PWR_GPU_ DECOUPLING

Size: | Document Number: LA-8821P | Rev: 0.1

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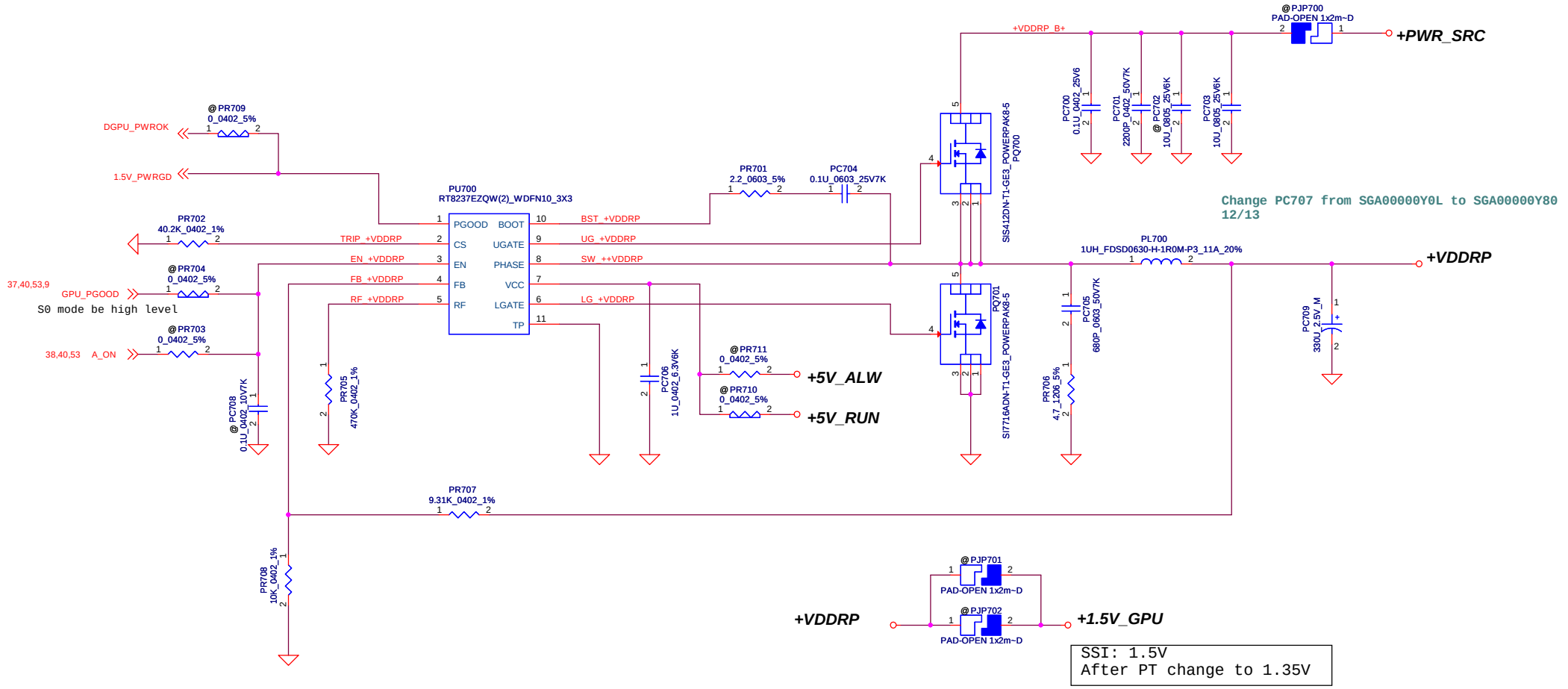

Compal Electronics, Inc.

Title	PWR_+1.5VDDR	
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VAW30 Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	58	Adapter Protection Circuit	2013/1/30	Power	PC432 220pF is not popular part	Change to 0402 size	X00
2	59	P59-PWR_Selector	2013/2/4	Power	Battery voltage leakage to docking if only battery	Add: PD513, PQ526, PR565, PR540, PQ527, PU506, PC515	X00
3	56	Vcore fine tune	2013/2/7	Power	Vcore fine tune	Modify: PR306, PR301, PR333, PR328, PR325, PR322, PL300	X00
4	57	Vcorecapacitor reduce	2013/2/7	Power	Vcore output capacitor reduce	NC: PC371 ,PC386, PC370 ,PC382,PC383	X00
5	58	Charger	2013/2/18	Power	Reserve H_PROCHOT# delay time fine tune by soft ware	Add "MODULE_BATT_PRES#" and PR454(Cancel 3/19)	X00
6	59	P59-PWR_Selector	2013/2/26	Power	Adjust divider resistor for MOSFET	Change from 240K to 100K: PR503, PR528, PR544, PR565	X00
7	59	P59-PWR_Selector	2013/2/26	Power	Adjust divider resistor for MOSFET	Change from 47K to 240K: PR501, PR524, PR535, PR540	X00
8	59	P59-PWR_Selector	2013/2/26	Power	SUT will unexpected shut down if un-docking during S0/S3	Add: PQ528, PR566	X00
9	51	"PBAT_PRES#" ESD fail	2013/3/4	Power	ESD PD1 fail, even connect 3.3V to VBUS pin	Change PD1 to PD1, PD2(TVNST52302AB0)	X00
10	59	P59-PWR_Selector	2013/3/6	Power	SB903380020 FDN338P derating fail	PQ500, PQ517,PQ520,PQ522,PQ526 change to SB000007900, PQ1change to SB00000PJ00	X00
11	51	PC5 down size	2013/3/12	Power	PC5 down size	Change PC5 from 0805 to 0603 size	X00
12	51,59	AC_DIS# net change	2013/3/12	Power	AC_DIS# should high enable, not low enable	AC_DIS# change to AC_DIS	X00
13		EMC open issue	2013/3/18	Power	Add parts for EMI	PR606,PC615, PR632, PC628, PR706, PC705, PR324, PC307	X00
14	60, 62	PU600, PU601 VCC	2013/3/19	Power	DIS S3 power consumption voer 200mW	Add PR630 PR711, PR710 for reserve +5V_RUN	X00
15	61	Change DGPU output cap	2013/3/19	Power	For thermal issue change DGPU power output cap.-14"	Change PC683,PC684	X00
16	62	GPU DDR change to 1.35V	2013/3/19	Power	Change VDDR output voltage from 1.5V to 1.35V	Change PR707 from 11.5K to 9.1K	X00
17	54	+1.05V dynamic load test	2013/3/19	Power	+1.05V dynamic load over spec	Change PL150 from 1uH to 0.68uH	X00
18	58	Change output chock	2013/3/20	Power	Same as 14" for height limit	Charger output choke change to 2.2uH	X00
19	60	0 ohm resistor	2013/3/21	Power	0 ohm 1% vender is not correct in ISPD	Change PR621 0ohm from 1% to 5%	X00
20	54	1.05V dynamic over spec	2013/3/21	Power	1.05V dynamic over spec	Change PL150 from 1uH to 0.68uH	X00
21	59	Modify for Peak power	2013/3/21	Power	Modify schematic	PQ529, PQ518, PR527 and PR567	X00
22	NA	Reserve	Reserve	Power	Reserve	Reserve	X01
23	60	DGPU core output ripple	2013/5/10	Power	Output ripple with a low frequence ripple	+PWR_SRC do not include feedback via	X01
24	60	DGPU core output ripple	2013/5/10	Power	Output ripple with a low frequence ripple	+PWR_SRC do not include feedback via	X01
25	59	14" 組裝問題	2013/5/10	Power	PD512 太靠邊板	Move location	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	56	14" Vcore find tune	2013/5/29	Power	14" Vcore find tune for LL and DIMON	PR328=2.4K->2.1K; PR333=30K->49.9K; PR301=390K->348K	X02
2	NA	Reserve	Reserve	Power	Reserve	Reserve	X02
3	58	EMI solution	2013/5/31	EMI	EMI: 200~225MHz boardband	Populate bead 120 ohm on PJP100 and PL301, populate 0.1uF on pc302 and pc700, 2200pF on pc701.	X02
4	58	EMI solution	2013/5/31	EMI	EMI: 200~225MHz boardband	PC419 add parallel PC441:2200pF and PC440: 0.1uF	X02
5	62	Thermal de-ratgin issue	2013/6/10	Power	MLCC are exceeded thermal derating criteria	Change to X6S/X7R: PC600, PC601, PC604, PC605, PC674, PC302, PC304,PC311,PC312,PC313,PC314	X02
6	59	Change part number	2013/6/6	Power	Part number ~N0 is for other customer	PC505 SE043474KN0 change to SE043474K80	X02
7	NA	14" NPI report(4/19)	2013/6/6	Power	Co-lay need select 1 conponent	Del NC: PJP300, PL600, PJP1, PC66, PC707, PJP51,PJP400	X02
8		Selector	2013/5/30	Power	For 3V/5V volgate level, change VDS rating from 30V to 20V	PQ1, PQ518 change to 20V rating DMG2301U-7_SOT23-3	X02
9	62	14" DGPU DDR	2013/6/7	Power	Output capacitor PC709 not in PSL	Change to NCC: SF000003100	X02
XB							
1		Thermal de-ratgin issue	2013/7/10	Power	According QAD test result change MLCC back to X5R	PC674, PC302, PC304,PC311,PC312,PC313,PC314	X03
2		Change 0 ohm to short pad	2013/7/10	Power	Reduce part count	Except: PR321 and PR621	X03
3		Thermal de-ratgin issue	2013/7/10	Power	MLCC are exceeded thermal derating criteria	VAW30 change to X6S/X7R: PC302, PC304, PC311, PC312, PC313, PC314	X03

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	USB3.0 Re-driver	13'0814	EE	Pull-up and Pull-down resister	R2628, R2638, R2639, R2644	1.0
2	41	POWER BOTTON	13'0814	EE	Un-pop power botton.	SW5 and SW6	1.0
3	38	Board ID	13'0814	EE	Change board ID to REV. A00.	Change R392 to 8.2K ohm.	1.0
4	41	LED bright	13'0814	ME	change LED resister to 300 ohm	R438, R436, R435, R433 and R429	1.0
5	38	AUDIO test fail	13'0814	EE	Audio resistor change from 9.1 ohm to 18 ohm	R162 and R166	1.0
6	42~46	GPU chip PN	13'0814	EE	Update P/N of GPU chip	Change P/N of UV1 to SA00006CB1L.	1.0
7	28	LAN chip P/N	13'0814	EE	Type change to T & R	Change P/N of U21 to SA000066W4L.	1.0
8	1	change R3 PN of PCB	13'0815	EE	change R3 PN of PCB	Change from DA8000WJ000 to DA8000WJ011	1.0
9	16	BT issue	13'0822	EE	Un-pop 0.47uF between “+PCH_VCCDSW3_3” and “+PCH_VCCDSW”	C413	1.0
10	36	EMI Request	13'0822	EMI	Add D2 on “Sleeve” & “Ring2” and connect to DGND		1.0