COMPAL CONFIDENTIAL

MODEL NAME : *QAL80*

PCB NO : *LA-7781P (DA60000OP10)*

BOM P/N : *4319EK31L01*

GPIO MAP: E4_VC_GPIO_map_rev_1.1

Dalmore 14 UMA

@ *Ivy Bridge + Panther POINT*

2012-02-24

REV : 1.0 (A00)

@ : Nopop Component

CONN@ : Connector Component

MB Type	BOM P/N	
ATG TPM	L51	1@ 5@
ATG Non-TPM	L52	2@ 5@
TPM	L01	1@
Non-TPM	L02	2@

MB PCB

Part Number	Description
DA60000OP10	PCB 0LD LA-7781P REV1 M/B UMA

DELL CONFIDENTIAL/PROPRIETARY

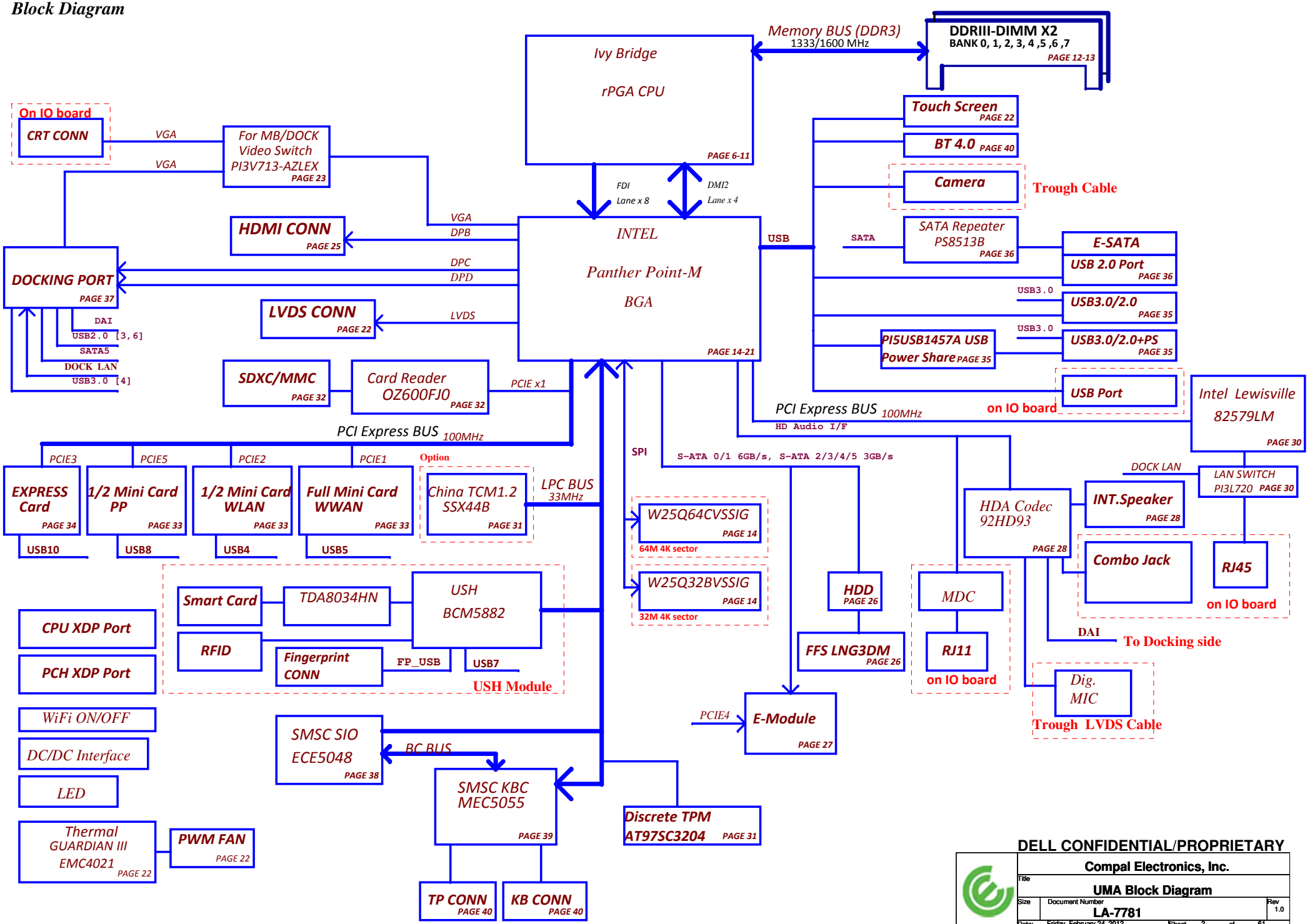
Compal Electronics, Inc.

Title: Cover Sheet

Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 Sheet 1 of 61

Block Diagram



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: UMA Block Diagram		
Size	Document Number: LA-7781	Rev: 1.0
Date: Friday, February 24, 2012	Sheet 2 of 61	

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane \ State	+PWR_SRC_S +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

	USB PORT#	DESTINATION
PCH	0	JUSB1 (Right side Top)
	1	JUSB2 (Right side Bottom)
	2	JESA1 (Right side ESATA)
	3	DOCKING
	4	WLAN
	5	WWAN
	6	DOCKING
	7	USH->BIO
	8	JMINI3(Flash)
	9	JUSB (Left side)
	10	Express card
	11	Bluetooth
	12	Camera
	13	LCD Touch

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask		0.50
			Add Plating		1.45
1	Top		Copper foil	0.5oz	0.65
			Prepreg	1080	2.80
2	VCC		Copper foil	1oz	1.35
			Core	3mil	3.00
3	Sig 1		Copper foil	1oz	1.35
			Prepreg	7628 HRC*2+2116+7628 HRC*2	33.50
4	Sig 2		Copper foil	1oz	1.35
			Core	3mil	3.00
5	GND		Copper foil	1oz	1.35
			Prepreg	1080	2.60
6	Bottom		Copper foil	0.5oz	0.65
			Add Plating		1.45
			SolderMask		0.50
Overall Thickness (1.4mm ± 10%)			55.1		55.30000

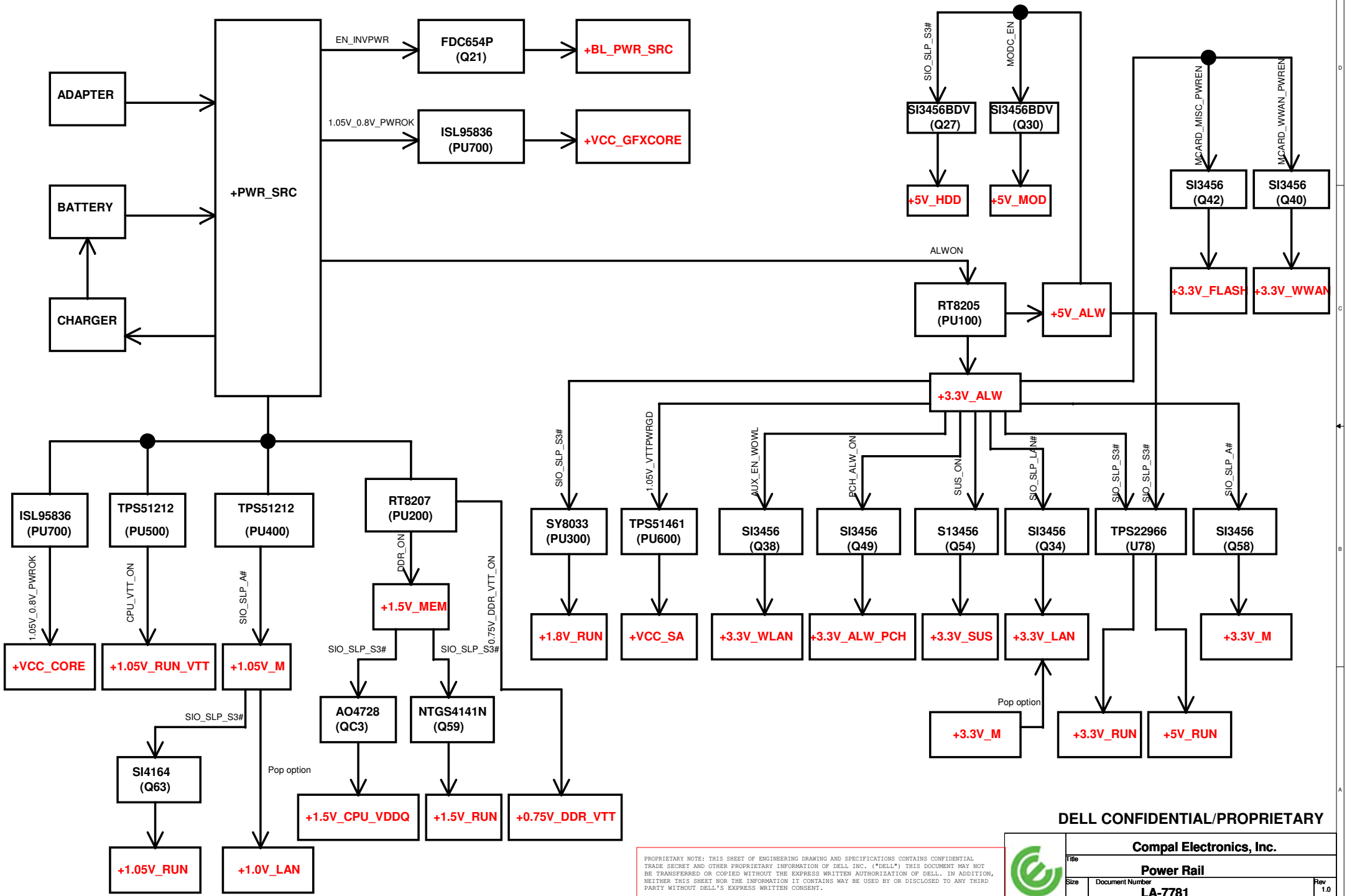
UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	Dock DP port 2
Port D	Dock DP port 1

Compal Electronics, Inc.

Title: Index and Config.

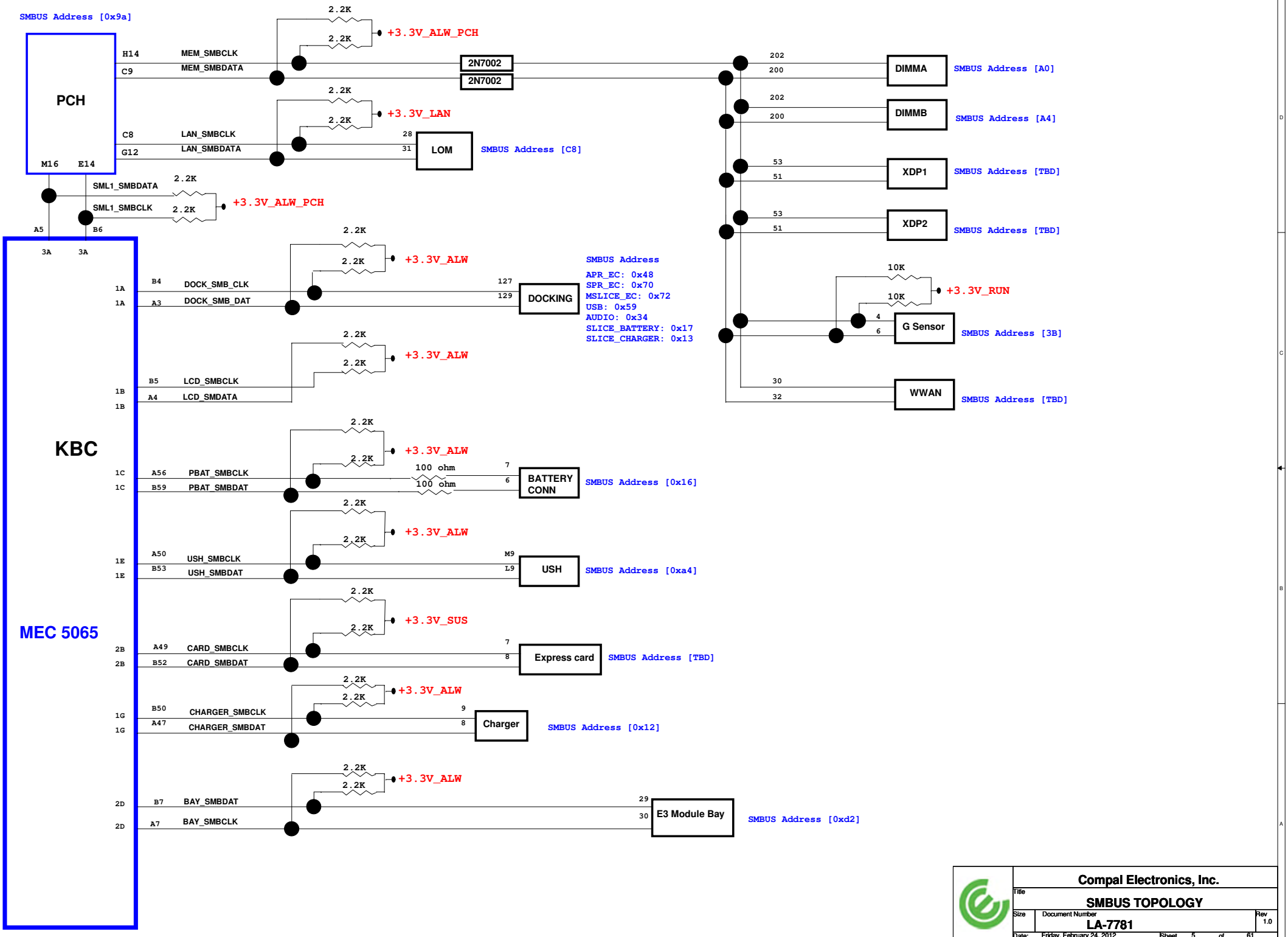
Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 3 of 61



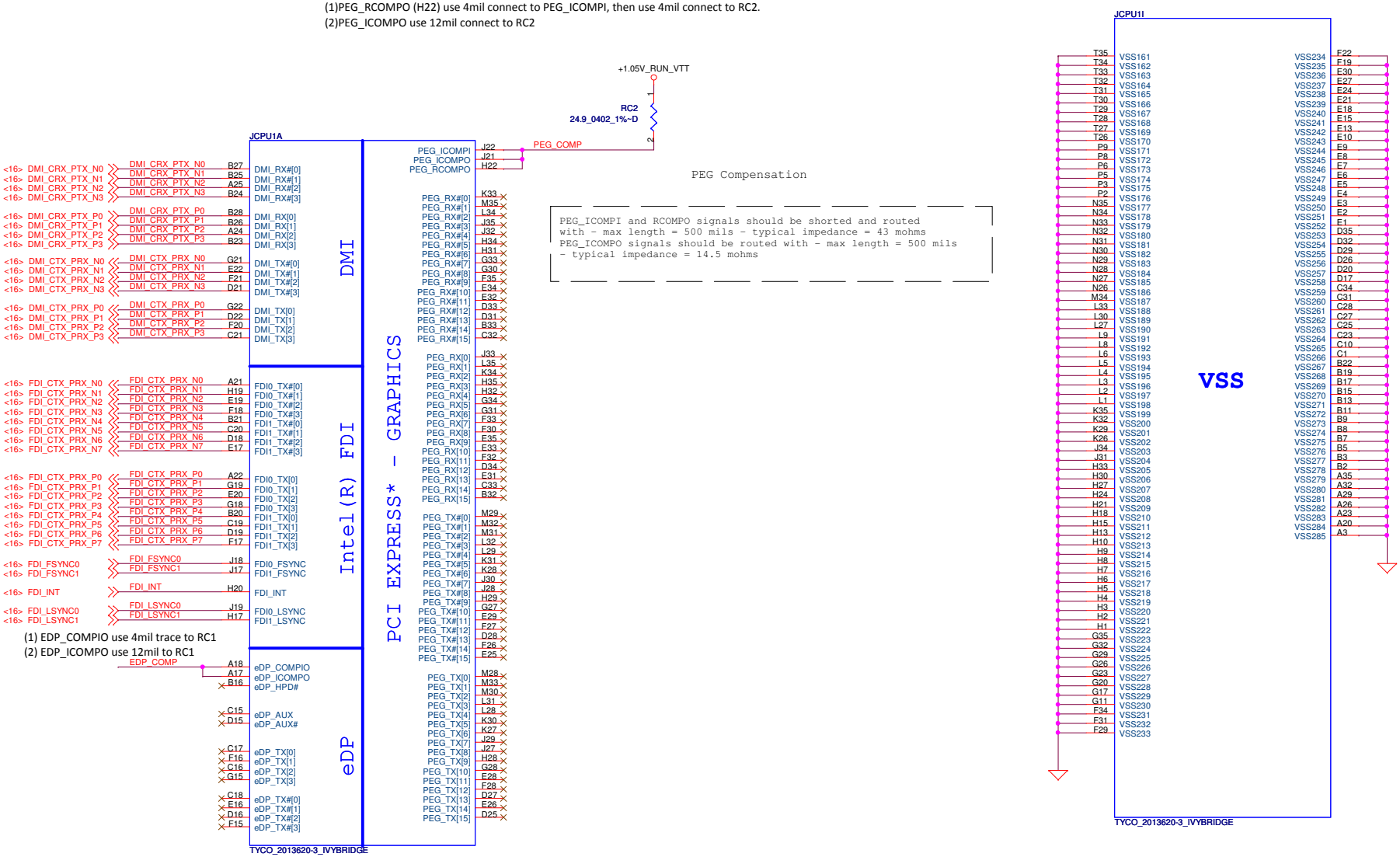
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	Power Rail
Size	Document Number: LA-7781
Rev	1.0
Date:	Friday, February 24, 2012
Sheet	4 of 61



Compal Electronics, Inc.	
Title	SMBUS TOPOLOGY
Size	Document Number: LA-7781
Rev	1.0
Date:	Friday, February 24, 2012
Sheet	5 of 61

(1)PEG_RCOMPO (H22) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC2.
(2)PEG_ICOMPO use 12mil connect to RC2



Compal Electronics, Inc.

Title: Ivy Bridge (1/6)

Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 6 of 61

Follow DG Rev0.71 SM_DRAMPWROK topology

+1.5V_CPU_VDDQ
+3.3V_ALW_PCH
CC156 0.1U_0402_25V6K~D
UC2
<39,40> RUNPWROK
RUNPWROK_AND
RC12 200_0402_1%~D
PM_DRAM_PWRGD_CPU
RC28 130_0402_1%~D
+3.3V_ALW_PCH
RC18 200_0402_1%~D
<16> PM_DRAM_PWRGD
74AHC1G09GW_TSSOP5~D
RC64 @ 39_0402_5%~D
<11,42> RUN_ON_CPU1.5VS3#
QC1@ SSM3K7002FU_SC70-3~D
INTEL suggest RC64 and QC1 NO stuff by default

+3.3V_ALW_PCH
@RC124 1K_0402_5%~D
SYS_PWROK_XDP
+1.05V_RUN_VTT
CC65 0.1U_0402_25V6K~D
CC66 0.1U_0402_25V6K~D
Place near JXDP1

+1.05V_RUN_VTT
JXDP1
GND0 OBSFN_A0 OBSFN_A1 GND2 OBSDATA_A0 OBSDATA_A1 GND4 OBSDATA_A2 OBSDATA_A3 GND6 OBSFN_B0 OBSFN_B1 GND8 OBSDATA_B0 OBSDATA_B1 GND10 OBSDATA_B2 OBSDATA_B3 GND12 PWRGOOD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 GND14 SDA SCL TCK1 TCK0 GND16
GND1 OBSFN_C0 OBSFN_C1 GND3 OBSDATA_C0 OBSDATA_C1 GND5 OBSDATA_C2 OBSDATA_C3 GND7 OBSFN_D0 OBSFN_D1 GND9 OBSDATA_D0 OBSDATA_D1 GND11 OBSDATA_D2 OBSDATA_D3 GND13 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 GND15 TD0 TRST# TDI TMS GND17
SAMTE_BSH-030-01-L-D-A CONN@
XDP_PREQ# XDP_PRDY# XDP_OBS0 XDP_OBS1 XDP_OBS2 XDP_OBS3 CFG10 CFG11 XDP_OBS4 XDP_OBS5 XDP_OBS6 XDP_OBS7 XDP_TCLK_R
CFG16 CFG17 CFG0_R CFG1_R CFG2 CFG3 CFG8 CFG9 CFG4 CFG5_R CFG6 CFG7 CLK_XDP CLK_XDP# XDP_RST# XDP_DBRESET# XDP_TDO XDP_TRST# XDP_TDI XDP_TMS_R

The resistor for HOOK2 should beplaced such that the stub is very small on CFG0 net

H_CPUPWRGD <14,16> SIO_PWRBTN#_R @RC51 @RC6 1K_0402_5%~D 0_0402_5%~D H_CPUPWRGD_XDP PLTRST_PWRBTN#_XDP
CFG0_R <16,39> SYS_PWROK @RC71 @RC9 1K_0402_5%~D 0_0402_5%~D XDP_HOOK2 SYS_PWROK_XDP
<12,13,14,15,27,34> DDR_XDP_WAN_SMBDAT <12,13,14,15,27,34> DDR_XDP_WAN_SMBCLK @RC1251 @RC127 0_0402_5%~D 0_0402_5%~D DDR_XDP_SMBDAT_R1 DDR_XDP_SMBCLK_R1
XDP_TCLK_R

+1.05V_RUN_VTT
@RC126 56_0402_5%~D H_THERMTRIP#
@RC128 49.9_0402_1%~D H_CATERR#
RC44 62_0402_5%~D H_PROCHOT#

JCPU1B

Follow check list 0.5
<18> H_SNB_IVB# C26 PROC_SELECT#
<39> CPU_DETECT# AN34 SKTOCC#
MISC

H_CATERR# AL33 CATERR#
<40> PECI_EC AN33 PECI
VR1 TOPOLOGY
<40,51,52> H_PROCHOT# RC57 56_0402_5%~D H_PROCHOT#_R AL32 PROCHOT#
Close to JCBU1
<22> H_THERMTRIP# @RC129 0_0402_5%~D H_THERMTRIP#_R AN32 THERMTRIP#
THERMAL

<16> H_PM_SYNC H_PM_SYNC AM34 PM_SYNC
<18> H_CPUPWRGD @RC25 0_0402_5%~D VCCPWRGOOD_0_R AP33 UNCOREPWRGOOD
PM_DRAM_PWRGD_CPU V8 SM_DRAMPWROK
PCH_PLTRST#_R AR33 RESET#
PWR MANAGEMENT

BCLK BCLK# A28 CPU_DMI A27 CPU_DMI# @RC13 @RC15 0_0402_5%~D 0_0402_5%~D CLK_CPU_DMI <15> CLK_CPU_DMI# <15>
DPLL_REF_CLK DPLL_REF_CLK# A16 CPU_DPLL A15 CPU_DPLL# RC16 RC17 1K_0402_5%~D 1K_0402_5%~D +1.05V_RUN_VTT
CLOCKS

Remove DPLL Ref clock (for eDP only)

SM_DRAMRST# R8 DDR3_DRAMRST#_CPU
SM_RCOMP[0] SM_RCOMP[1] SM_RCOMP[2] AK1 SM_RCOMP0 A5 SM_RCOMP1 A4 SM_RCOMP2
Max 500mils
SM_RCOMP2 --> 15mil
SM_RCOMP1/0 --> 20mil
RC50 4.99K_0402_1%~D
@RC48 0_0402_5%~D
QC2 BSS138W-7-F_SOT323-3~D
DDR3_DRAMRST# <12>
DDR_HVREF_RST
CC177 0.047U_0402_16V4Z~D
DDR3 MISC

PRDY# PREQ# AP29 XDP_PRDY# AP27 XDP_PREQ# @RE27 0_0402_5%~D XDP_PREQ#_R
TCK TMS TRST# AR26 XDP_TCLK AR27 XDP_TMS AP30 XDP_TRST# @RE28 @RE29 @RE30 0_0402_5%~D XDP_TCLK_R XDP_TMS_R XDP_TRST#_R
<15> DDR_HVREF_RST_PCH @RC46 0_0402_5%~D
<40> DDR_HVREF_RST_GATE @RC47 0_0402_5%~D
DDR_HVREF_RST <12>
M3 control
TDI TDO AR28 XDP_TDI_R AR26 XDP_TDO_R @RE31 @RE32 0_0402_5%~D XDP_TDI XDP_TDO
DBR# AL35 XDP_DBRESET#_R @RC26 0_0402_5%~D XDP_DBRESET# <14,16>
BPM#[0] BPM#[1] BPM#[2] BPM#[3] BPM#[4] BPM#[5] BPM#[6] BPM#[7] AT28 XDP_OBS0_R AR29 XDP_OBS1_R AR30 XDP_OBS2_R AT30 XDP_OBS3_R AP32 XDP_OBS4_R AR31 XDP_OBS5_R AT31 XDP_OBS6_R AR32 XDP_OBS7_R @RC30 @RC31 @RC33 @RC34 @RC36 @RC37 @RC38 @RC39 0_0402_5%~D XDP_OBS0 XDP_OBS1 XDP_OBS2 XDP_OBS3 XDP_OBS4 XDP_OBS5 XDP_OBS6 XDP_OBS7
JTAG & BPM

For ESD concern, please put near CPU

TYCO_2013620-3_IVYBRIDGE

XDP_RST#_R PXDP@ RC8 1K_0402_5%~D PLTRST_XDP# <17>
CLK_XDP @RH107 0_0402_5%~D CLK_CPU_ITP <15>
CLK_XDP# @RH106 0_0402_5%~D CLK_CPU_ITP# <15>
<9> CLK_XDP_ITP @RH109 0_0402_5%~D
<9> CLK_XDP_ITP# @RH108 0_0402_5%~D

PU/PD for JTAG signals
+3.3V_RUN
XDP_DBRESET# RC19 1K_0402_5%~D
+1.05V_RUN_VTT
XDP_TMS RC27 51_0402_1%~D
XDP_TDI_R RC29 51_0402_1%~D
XDP_PREQ# @RC32 51_0402_1%~D
XDP_TDO_R RC35 51_0402_1%~D
XDP_TCLK RC40 51_0402_1%~D
XDP_TRST# RC41 51_0402_1%~D

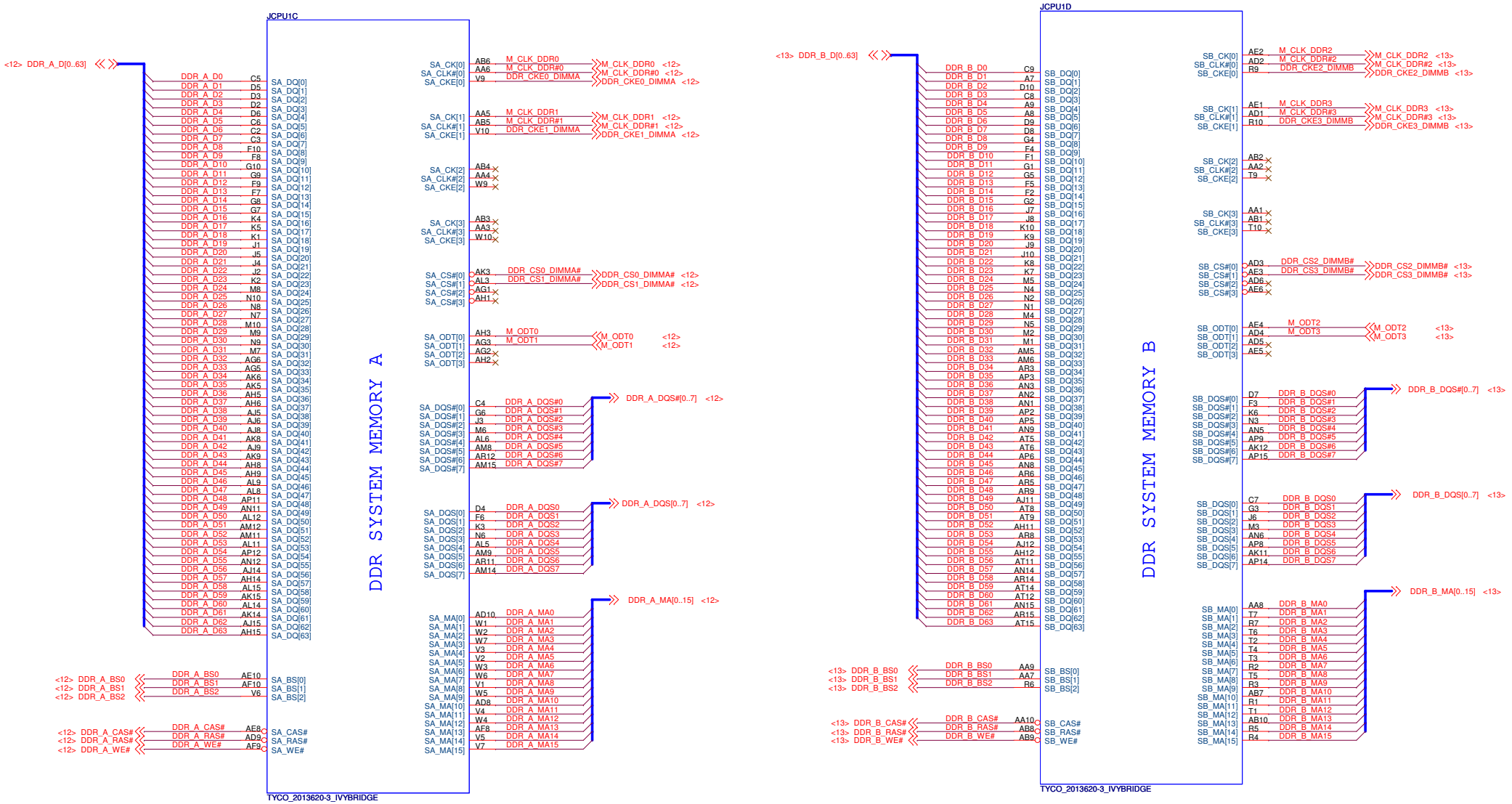
Buffered reset to CPU
+3.3V_RUN
+1.05V_RUN_VTT
CC140 0.1U_0402_25V6K~D
RC4 75_0402_1%~D
UC1
<14,17> PCH_PLTRST#
SN74LVC1G07DCKR_SC70-5~D
PCH_PLTRST#_BUF
RC10 43_0402_5%~D PCH_PLTRST#_R
Open drain buffer

VCCPWRGOOD_0_R
RC130 10K_0402_5%~D
Avoid stub in the PWRGD path while placing resistors RC25 & RC130

SM_RCOMP2
SM_RCOMP1
SM_RCOMP0
RC42 140_0402_1%~D
RC43 25.5_0402_1%~D
RC45 200_0402_1%~D

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.
Title: Ivy Bridge (1/6)
Size: Document Number: LA-7781 Rev: 1.0
Date: Friday, February 24, 2012 Sheet 7 of 61

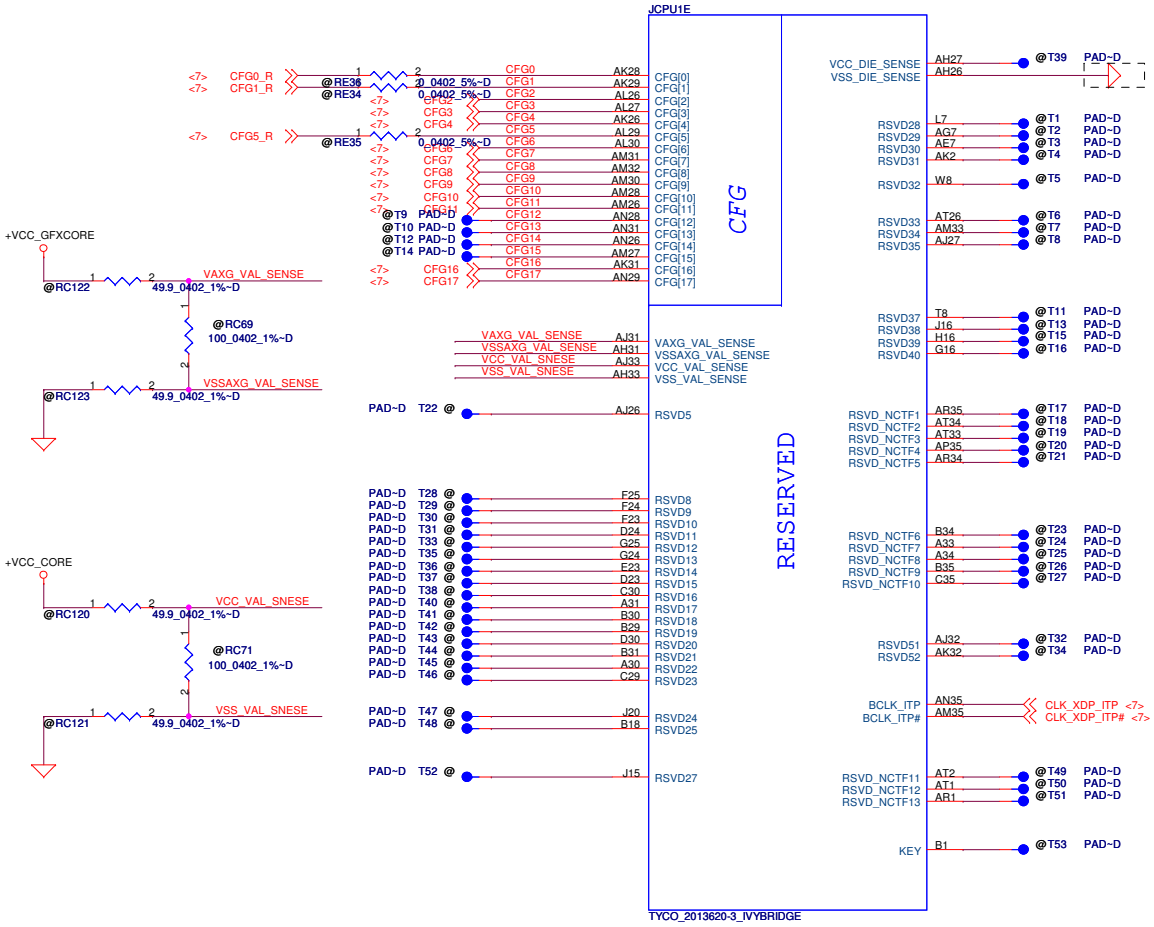


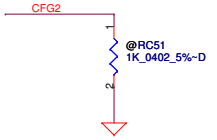
DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

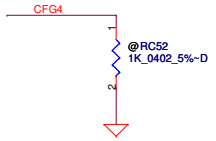
Compal Electronics, Inc.	
Title	Ivy Bridge (1/6)
Size	Document Number: LA-7781
Rev	1.0
Date:	Friday, February 24, 2012
Sheet	8 of 61

CFG Straps for Processor

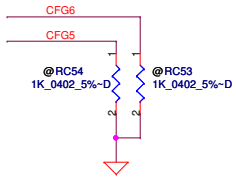




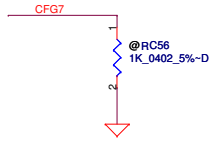
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Compal Electronics, Inc.

Title: Ivy Bridge (1/6)

Size: | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 9 of 61

POWER

JCPU1F

CORE SUPPLY

+VCC_CORE
53A

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

PEG AND DDR

+1.05V_RUN_VTT
8.5A

VCCIO1	AH13
VCCIO2	AH10
VCCIO3	AG10
VCCIO4	AC10
VCCIO5	Y10
VCCIO6	U10
VCCIO7	P10
VCCIO8	L10
VCCIO9	J14
VCCIO10	J13
VCCIO11	J12
VCCIO12	J11
VCCIO13	H14
VCCIO14	H12
VCCIO15	H11
VCCIO16	G14
VCCIO17	G13
VCCIO18	G12
VCCIO19	F14
VCCIO20	F13
VCCIO21	F12
VCCIO22	F11
VCCIO23	E14
VCCIO24	E12
VCCIO25	E11
VCCIO26	D14
VCCIO27	D13
VCCIO28	D12
VCCIO29	D11
VCCIO30	C14
VCCIO31	C13
VCCIO32	C12
VCCIO33	C11
VCCIO34	B14
VCCIO35	B12
VCCIO36	A14
VCCIO37	A13
VCCIO38	A12
VCCIO39	A11
VCCIO40	J23

+1.05V_RUN_VTT

Note: Place the PU resistors close to CPU
RC61 close to CPU 300 - 1500mils

RC60 75_0402_1%~D

H_CPU_SVIDALRT# — RC61 43_0402_5%~D — VIDALERT_N <51>

SVID

+1.05V_RUN_VTT

RC63 130_0402_1%~D

CAD Note: Place the PU resistors close to CPU
RC63 close to CPU 300 - 1500mils

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 VIDSCLK — VIDSCLK <51>
VIDSOUT AJ28 VIDSOUT — VIDSOUT <51>

H_CPU_SVIDALRT# must be routed between the VIDSOUT and VIDSCLK lines to reduce cross talk. 18 mils spacing to others.

SENSE LINES

+VCC_CORE

Place RC66, RC70, RC75 near CPU

@RC75 100_0402_1%~D

RC66 100_0402_1%~D

VCC_SENSE AJ35 VCCSENSE_R — @RC67 0_0402_5%~D — VCCSENSE <51>
VSS_SENSE AJ34 VSSSENSE_R — @RC68 0_0402_5%~D — VSSSENSE <51>

RC98 10_0402_1%~D +1.05V_RUN_VTT

VCCIO_SENSE B10 VTT_SENSE — VTT_SENSE <49>
VSS_SENSE_VCCIO A10 VSSIO_SENSE_R — VSSIO_SENSE_R <49>

RC70 100_0402_1%~D

RC133 10_0402_1%~D

TYCO_2013620-3_IVYBRIDGE

Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05	8.5
VAXG	0.0-1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 ★

★ Description

5A to Mem controller(+1.5V_CPU_VDDQ)
5-6A to 2 DIMMs/channel
2-5A to +1.5V_RUN & +0.75V_DDR_VTT

DELL CONFIDENTIAL/PROPRIETARY

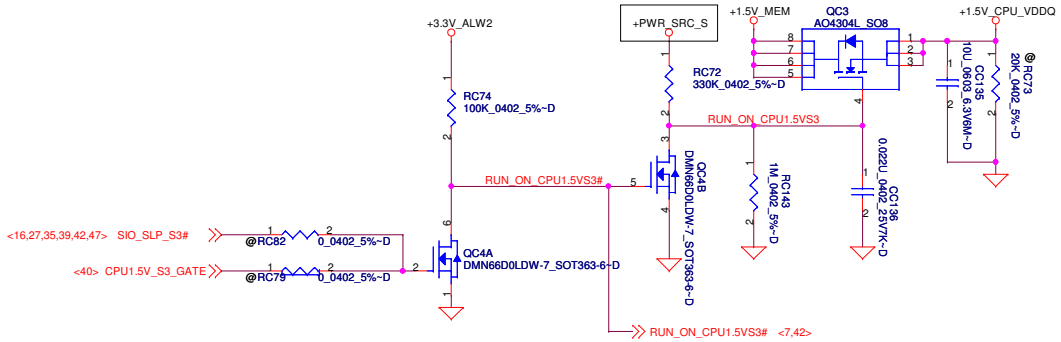
Compal Electronics, Inc.

Title: Ivy Bridge (1/6)

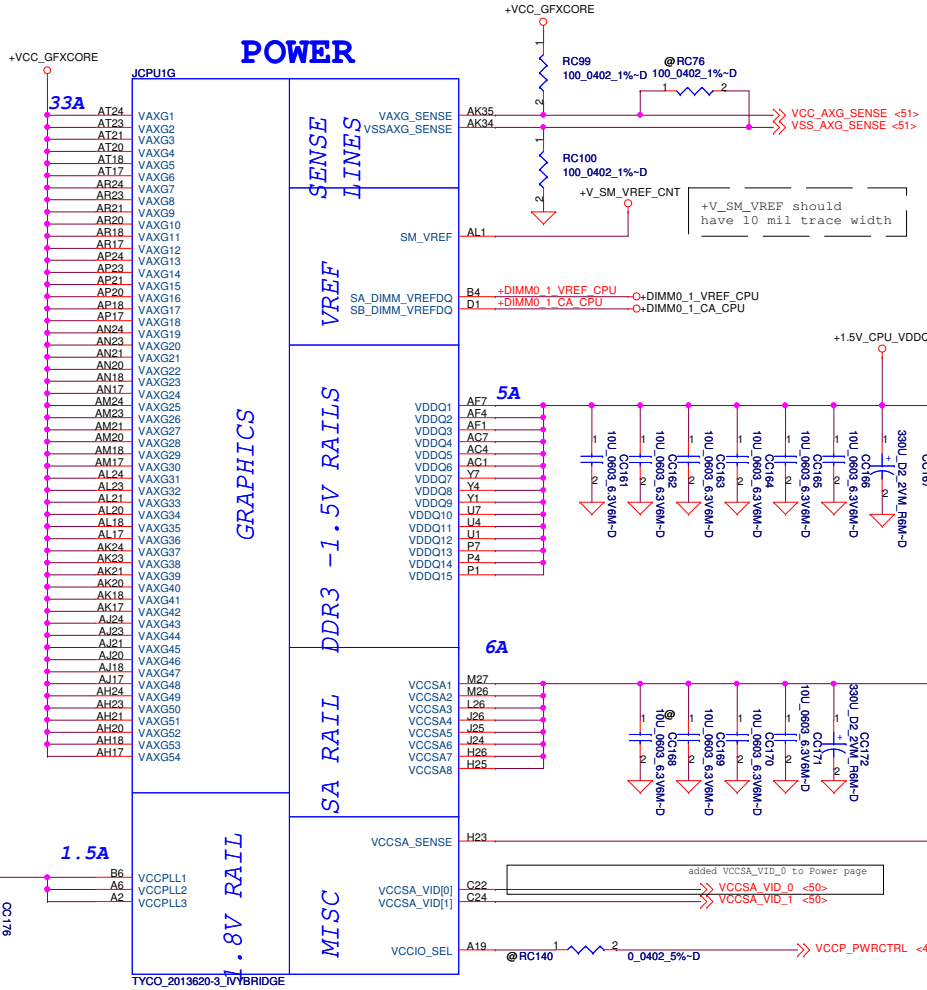
Size | Document Number: LA-7781 | Rev: 1.0

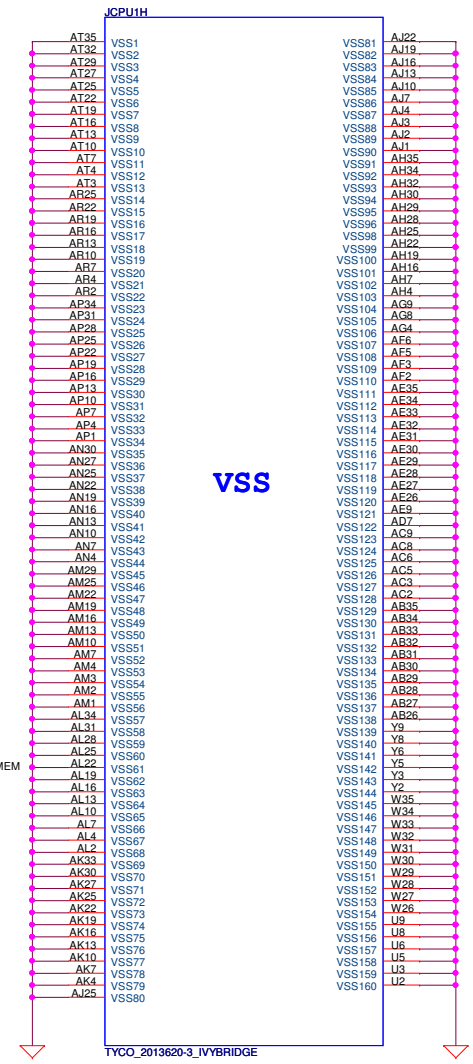
Date: Friday, February 24, 2012 | Sheet 10 of 61

+1.5V_CPU_VDDQ Source



POWER





Compal Electronics, Inc.	
Title	Ivy Bridge (1/6)
Size	Document Number: LA-7781
Rev	1.0
Date:	Friday, February 24, 2012
Sheet	11 of 61

JDIMM1 H=5.2

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	DDRIII-SODIMM SLOT1	
Size	Document Number LA-7781	Rev 1.0
Date: Friday, February 24, 2012	Sheet 12 of 61	

2-3A to 1 DIMMs/channel

JDIMMB H=9.2

Populate RD4, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

<8> DDR_B_DQS#[0..7]
<8> DDR_B_D[0..63]
<8> DDR_B_DQS[0..7]
<8> DDR_B_MA[0..15]

Layout Note: Place near JDIMM2

Layout Note: Place near JDIMM2.203,204

+V_DDR_REFB_M3 — @ RD8 0_0402_5%~D
+V_DDR_REF — @ RD4 0_0402_5%~D
+DIMM2_VREF_DQ — CD23 2.2U_0402_6.3V6M, CD24 0.1U_0402_25V6K~D

JDIMM2_CONN@
TYCO_2-2013310-2~D

+1.5V_MEM
+0.75V_DDR_VTT
+3.3V_RUN — RD5 10K_0402_5%~D
RD6 10K_0402_5%~D — CD43 0.1U_0402_25V6K~D, CD44 2.2U_0402_6.3V6M

+DIMM2_VREF_CA — @ RD15 0_0402_5%~D — +V_DDR_REF
CD37 2.2U_0402_6.3V6M, CD38 0.1U_0402_25V6K~D

CD25–CD28 1U_0402_6.3V6K~D
CD29–CD34 10U_0603_6.3V6M~D
@ CD35 330U_SX_2V~D
CD36 330U_SX_2V~D
CD39–CD42 1U_0402_6.3V6K~D

DDR3_DRAMRST# <12>
DDR_CKE2_DIMMB <8>
DDR_CKE3_DIMMB <8>
M_CLK_DDR2 <8>
M_CLK_DDR#2 <8>
M_CLK_DDR3 <8>
M_CLK_DDR#3 <8>
DDR_B_BS1 <8>
DDR_B_RAS# <8>
DDR_CS2_DIMMB# <8>
M_ODT2 <8>
M_ODT3 <8>
DDR_B_BS0 <8>
DDR_B_WE# <8>
DDR_B_CAS# <8>
DDR_CS3_DIMMB# <8>
DDR_XDP_WAN_SMBDAT <7,12,14,15,27,34>
DDR_XDP_WAN_SMBCLK <7,12,14,15,27,34>

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.
Title: DDRIII-SODIMM SLOT2
Size: Document Number: LA-7781 Rev: 1.0
Date: Friday, February 24, 2012 Sheet 13 of 61

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

PCH_AZ_SYNC is sampled at the rising edge of RSMRST# pin. So signal should be PU to the ALWAYS rail.

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs
Low - Enable External VRs

CMOS place near DIMM

Follow INTEL CRB 0.7

INTEL HDA_SYNC isolation circuit

BBS_BIT0 - BIOS BOOT STRAP BIT 0

No Reboot Strap
SPKR: Low = Default; High = No Reboot

200 MIL SO8
64Mb Flash ROM
X76@ U52
W25Q64CVSSIG_SO8~D

200 MIL SO8
32Mb Flash ROM
X76@ U53
W25Q32BVSSIG_SO8~D

X76@ configuration for ROM part

Vendor	No.	U52	U53
WINBOND	X7640631L01	SA000039A1L	SA00003K80L
WINBOND	X7640631L02	SA000039A2L	SA00003K80L
EON	X7640631L03	SA000046400	SA00004LI00
MXIC	X7640631L04	SA00004G600	SA000041P00

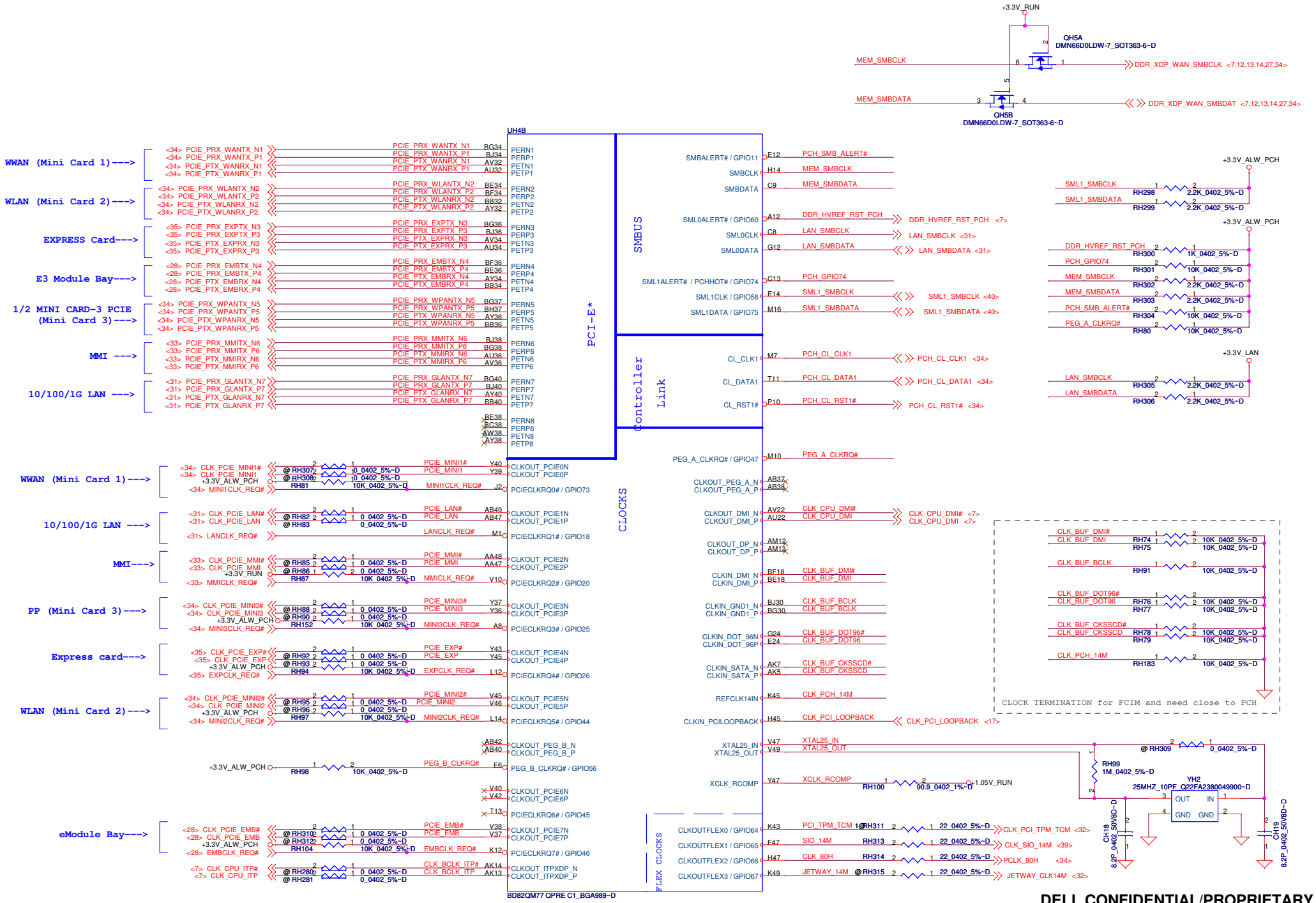
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: PCH (1/8)

Size: Document Number: LA-7781 Rev: 1.0

Date: Friday, February 24, 2012 Sheet 14 of 61

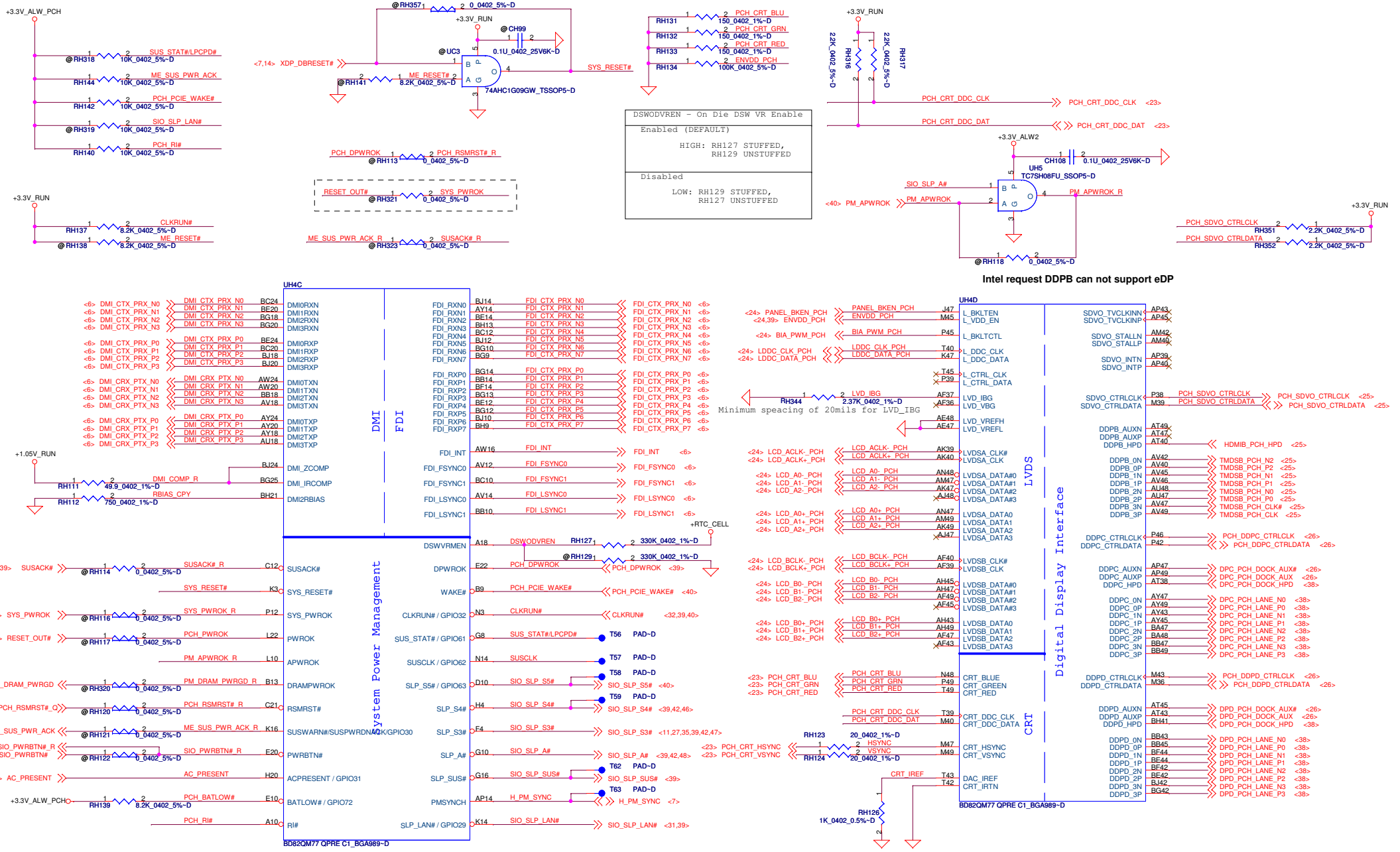


Compal Electronics, Inc.

Title: PCH (2/8)

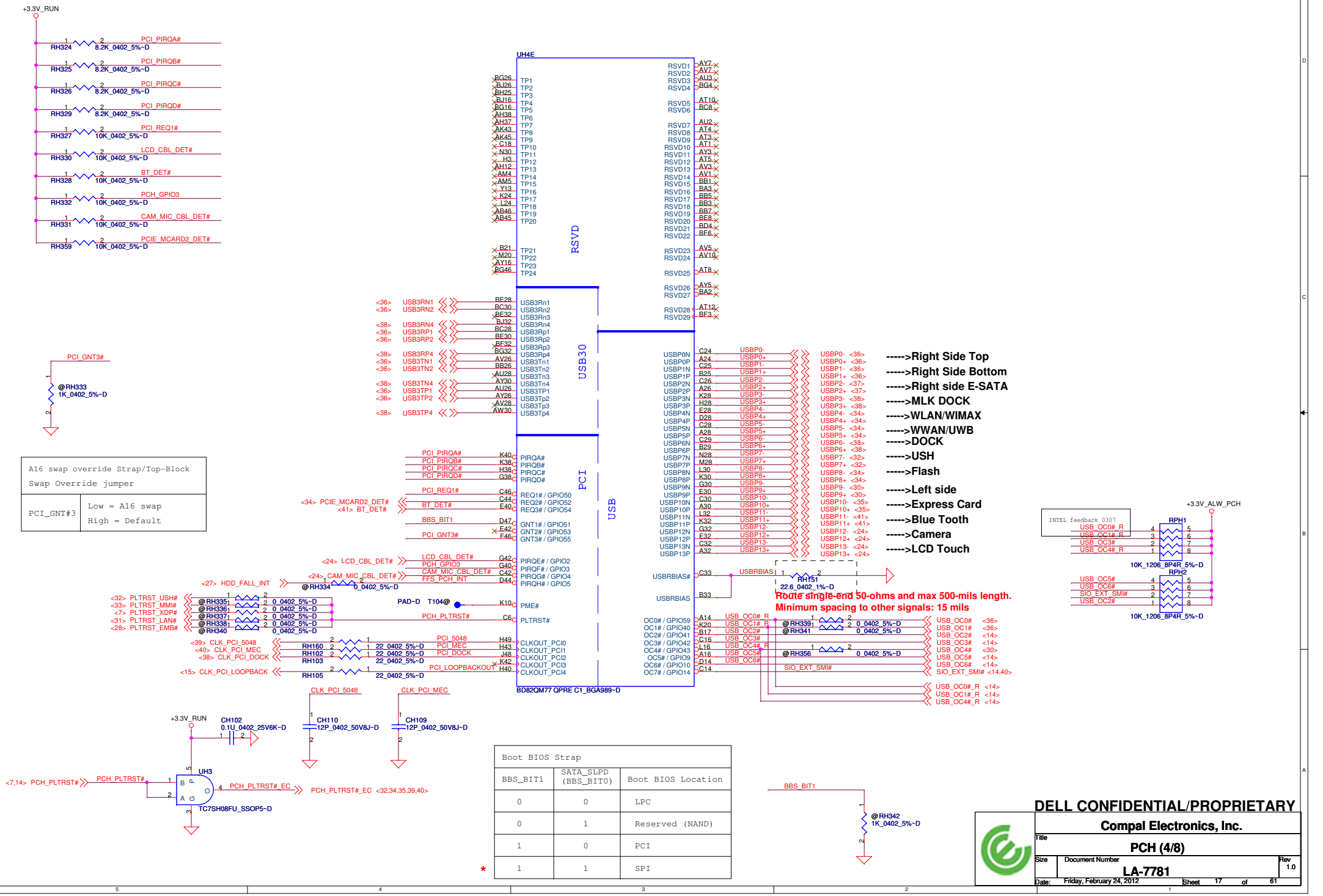
Size: | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 15 of 61



Compal Electronics, Inc.

Title	PCH (3/8)	
Size	Document Number: LA-7781	Rev: 1.0
Date: Friday, February 24, 2012	Sheet 16 of 61	


+3.3V_RUN
RH324 8.2K_0402_5%~D PCI_PIRQA#
RH325 8.2K_0402_5%~D PCI_PIRQB#
RH326 8.2K_0402_5%~D PCI_PIRQC#
RH329 8.2K_0402_5%~D PCI_PIRQD#
RH327 10K_0402_5%~D PCI_REQ1#
RH330 10K_0402_5%~D LCD_CBL_DET#
RH328 10K_0402_5%~D BT_DET#
RH332 10K_0402_5%~D PCH_GPIO3
RH331 10K_0402_5%~D CAM_MIC_CBL_DET#
RH359 10K_0402_5%~D PCIE_MCARD2_DET#
PCI_GNT3#
@RH333 1K_0402_5%~D
A16 swap override Strap/Top-Block
Swap Override jumper
PCI_GNT3# Low = A16 swap
High = Default
UH4E
RSVD
USB30
PCI
USB
BD82QM77 QPRE C1_BGA989~D
USB3Rn1 USB3Rn2 USB3Rn3 USB3Rn4 USB3Rp1 USB3Rp2 USB3Rp3 USB3Rp4 USB3Tn1 USB3Tn2 USB3Tn3 USB3Tn4 USB3TP1 USB3Tp2 USB3Tp3 USB3Tp4
PIRQA# PIRQB# PIRQC# PIRQD#
REQ1# / GPIO50 REQ2# / GPIO52 REQ3# / GPIO54
GNT1# / GPIO51 GNT2# / GPIO53 GNT3# / GPIO55
PIRQE# / GPIO2 PIRQF# / GPIO3 PIRQG# / GPIO4 PIRQH# / GPIO5
PME#
PLTRST#
CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4
USBP0- USBP0+ USBP1- USBP1+ USBP2- USBP2+ USBP3- USBP3+ USBP4- USBP4+ USBP5- USBP5+ USBP6- USBP6+ USBP7- USBP7+ USBP8- USBP8+ USBP9- USBP9+ USBP10- USBP10+ USBP11- USBP11+ USBP12- USBP12+ USBP13- USBP13+
USBRBIAS
USBRBIAS RH151 22.6_0402_1%~D
USBRBIAS
Route single-end 50-ohms and max 500-mils length.
Minimum spacing to other signals: 15 mils
OC0# / GPIO59 OC1# / GPIO40 OC2# / GPIO41 OC3# / GPIO42 OC4# / GPIO43 OC5# / GPIO9 OC6# / GPIO10 OC7# / GPIO14
USB_OC0# USB_OC1# USB_OC2# USB_OC3# USB_OC4# USB_OC5# USB_OC6#
@RH339 @RH341 @RH356 0_0402_5%~D
SIO_EXT_SMI#
INTEL feedback 0307
+3.3V_ALW_PCH
RPH1 RPH2 10K_1206_8P4R_5%~D
----->Right Side Top
----->Right Side Bottom
----->Right side E-SATA
----->MLK DOCK
----->WLAN/WIMAX
----->WWAN/UWB
----->DOCK
----->USH
----->Flash
----->Left side
----->Express Card
----->Blue Tooth
----->Camera
----->LCD Touch
PAD~D T104@
PCH_PLTRST#
PCI_5048 PCI_MEC PCI_DOCK PCI_LOOPBACKOUT
RH160 RH102 RH103 RH105 22_0402_5%~D
CLK_PCI_5048 CLK_PCI_MEC
CH110 12P_0402_50V8J~D
CH109 12P_0402_50V8J~D
+3.3V_RUN
CH102 0.1U_0402_25V6K~D
UH3
TC7SH08FU_SSOP5~D
PCH_PLTRST# PCH_PLTRST#_EC
BBS_BIT1
@RH342 1K_0402_5%~D
Boot BIOS Strap
BBS_BIT1 | SATA_SLPD (BBS_BIT0) | Boot BIOS Location
0 | 0 | LPC
0 | 1 | Reserved (NAND)
1 | 0 | PCI
1 | 1 | SPI
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Title PCH (4/8)
Size Document Number LA-7781 Rev 1.0
Date: Friday, February 24, 2012 Sheet 17 of 61

+3.3V_ALW_PCH

RH53 4.7K_0402_5%~D

SLP_ME_CSW_DEV#

RH353 1K_0402_5%~D @

Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

SLP_ME_CSW_DEV#	PLL ON DIE VR ENABLE
ENABLED - HIGH DEFAULT DISABLED - LOW	

<14> PCH_GPIO16
DBC_ENABLE for E4 12"

+3.3V_ALW_PCH

RH177 2 1 10K_0402_5%~D SIO_EXT_WAKE#

RH354 1 2 1K_0402_5%~D PCH_GPIO15

INTEL feedback 0302

RH174 2 1 10K_0402_5%~D PCH_GPIO36

RH172 2 1 10K_0402_5%~D PCH_GPIO37

@RH273 2 1 1K_0402_5%~D PCH_GPIO17

@RH265 2 1 10K_0402_5%~D PCH_GPIO16

+3.3V_ALW_PCH

RH170 2 1 10K_0402_5%~D KB_DET#

+3.3V_RUN

@RH171 2 1 10K_0402_5%~D PCH_GPIO36

@RH173 2 1 1K_0402_5%~D PCH_GPIO37

RH266 2 1 10K_0402_5%~D TEMP_ALERT#

RH181 2 1 10K_0402_5%~D PCH_GPIO22

RH178 2 1 10K_0402_5%~D PCH_GPIO7

RH269 1 2 8.2K_0402_5%~D PCH_GPIO17

RH163 1 2 10K_0402_5%~D IO_LOOP#

RH272 1 2 10K_0402_5%~D PCH_GPIO16

UH4F

<14> SIO_EXT_SCI#_R			
<40> SIO_EXT_SCI#	SIO_EXT_SCI# 1 @RH259 2 0_0402_5%~D	T7	BMBUSY# / GPIO0
<32> USH_DET#	USH_DET#	A42	TACH1 / GPIO1
<30> IO_LOOP#	IO_LOOP#	H36	TACH2 / GPIO6
	PCH_GPIO7	E38	TACH3 / GPIO7
<39> SIO_EXT_WAKE#		C10	GPIO8
<31> PM_LANPHY_ENABLE	PM_LANPHY_ENABLE	C4	LAN_PHY_PWR_CTRL / GPIO12
<14> PCH_GPIO15	PCH_GPIO15	G2	GPIO15
<14> PCH_GPIO16	PCH_GPIO16	U2	SATA4GP / GPIO16
	PCH_GPIO17	D40	TACH0 / GPIO17
	PCH_GPIO22	T5	SCLOCK / GPIO22
<34> PCIE_MCARD1_DET#		E8	GPIO24
<24> E3_PAID_TS_DET#	E3_PAID_TS_DET#	E16	GPIO27
<14,39> SLP_ME_CSW_DEV#	SLP_ME_CSW_DEV#	P8	GPIO28
		K1	STP_PCI# / GPIO34
<14,34> USB_MCARD1_DET#	USB_MCARD1_DET#	K4	GPIO35
<14> PCH_GPIO36	PCH_GPIO36	V8	SATA2GP / GPIO36
<14> PCH_GPIO37	PCH_GPIO37	M5	SATA3GP / GPIO37
	TPM_ID0	N2	SLOAD / GPIO38
	TPM_ID1	M3	SDATAOUT0 / GPIO39
<27> FFS_INT2	FFS_INT2	V13	SDATAOUT1 / GPIO48
<14,39> TEMP_ALERT#	TEMP_ALERT#	V3	SATA5GP / GPIO49 / TEMP_ALERT#
<41> KB_DET#	KB_DET#	D6	GPIO57

GPIO

		C40	TACH4 / GPIO68
		B41	TACH5 / GPIO69
		C41	TACH6 / GPIO70
		A40	TACH7 / GPIO71
	SIO_A20GATE	P4	A20GATE
		AU16	PECI
	SIO_RCIN#	P5	RCIN#
	H_CPUPWRGD	AY11	PROCPWRGD
	PCH_THRMTRIP#	AY10	THRMTRIP#
	INIT3_3V#	T14	INIT3_3V#
	DF_TVS	AY1	DF_TVS
		AH8	TS_VSS1
		AK11	TS_VSS2
		AH10	TS_VSS3
		AK10	TS_VSS4
	NC_1	P37	NC_1

CPU/MISC

NCTF

VSS_NCTF_1		A4	VSS_NCTF_1
VSS_NCTF_2		A44	VSS_NCTF_2
VSS_NCTF_3		A45	VSS_NCTF_3
VSS_NCTF_4		A46	VSS_NCTF_4
VSS_NCTF_5		A5	VSS_NCTF_5
VSS_NCTF_6		A6	VSS_NCTF_6
VSS_NCTF_7		B3	VSS_NCTF_7
VSS_NCTF_8		B47	VSS_NCTF_8
VSS_NCTF_9		BD1	VSS_NCTF_9
VSS_NCTF_10		BD49	VSS_NCTF_10
VSS_NCTF_11		BE1	VSS_NCTF_11
VSS_NCTF_12		BE49	VSS_NCTF_12
VSS_NCTF_13		BF1	VSS_NCTF_13
VSS_NCTF_14		BF49	VSS_NCTF_14
		BG2	VSS_NCTF_15
		BG48	VSS_NCTF_16
		BH3	VSS_NCTF_17
		BH47	VSS_NCTF_18
		BJ4	VSS_NCTF_19
		BJ44	VSS_NCTF_20
		BJ45	VSS_NCTF_21
		BJ46	VSS_NCTF_22
		BJ5	VSS_NCTF_23
		BJ6	VSS_NCTF_24
		C2	VSS_NCTF_25
		C48	VSS_NCTF_26
		D1	VSS_NCTF_27
		D49	VSS_NCTF_28
		E1	VSS_NCTF_29
		E49	VSS_NCTF_30
		F1	VSS_NCTF_31
		F49	VSS_NCTF_32

BD82QM77 QPRE C1_BGA989~D

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45°from the pad.

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45°from the pad.

CONTACTLESS_DET# <32>

PCH_GPIO69

PCIE_MCARD3_DET# <34>

USB_MCARD2_DET# <34>

SIO_A20GATE <40>

SIO_RCIN# <40>

H_CPUPWRGD <7>

PAD~D T106 @

PAD~D T108 @

+3.3V_RUN

RH256 2 1 10K_0402_5%~D CONTACTLESS_DET#

RH260 1 2 1.5K_0402_1%~D PCH_GPIO69

+1.05V_RUN_VTT

RH262 2 1 56_0402_5%~D PCH_THRMTRIP# R

CH97 0.1U_0402_25V6K~D

+3.3V_RUN

RH158 2 1 10K_0402_5%~D SIO_A20GATE

RH203 2 1 10K_0402_5%~D SIO_RCIN#

RH263 1 2 10K_0402_5%~D SIO_EXT_SCI#

RH164 1 2 100K_0402_5%~D USH_DET#

PLACE RH150 CLOSE TO THE BRANCHING POINT
(TO CPU and NVRAM CONNECTOR)

+VCCDFTERM

RH149 need to close to CPU

RH149 2.2K_0402_5%~D

<7> H_SNB_IVB# @RH150 1 2 0_0402_5%~D DF_TVS_R RH358 1 2 1K_0402_5%~D DF_TVS

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

+3.3V_RUN

1@ RH267 10K_0402_5%~D

TPM_ID0

2@ RH270 10K_0402_5%~D

+3.3V_RUN

RH268 20K_0402_5%~D

TPM_ID1

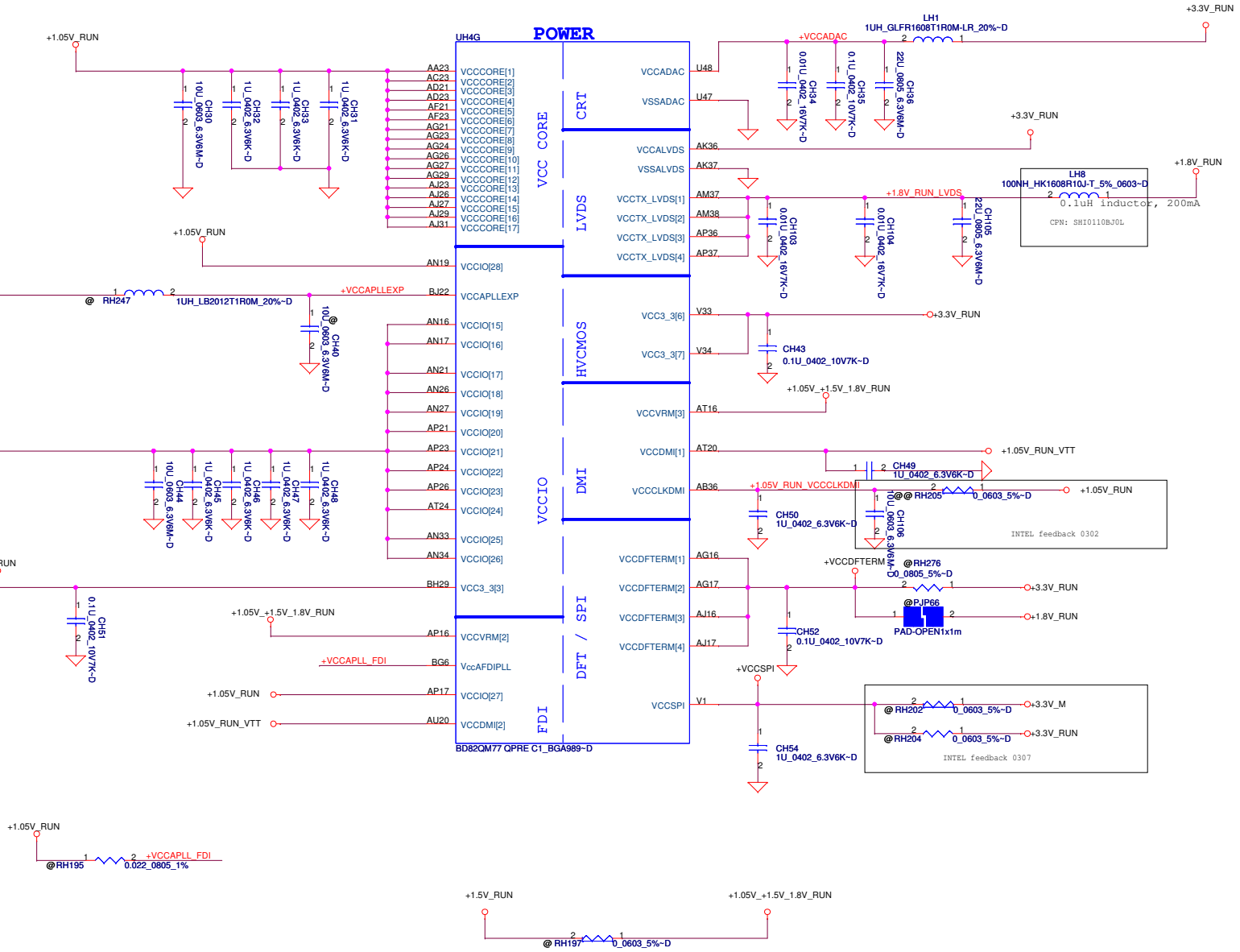
@RH271 2.2K_0402_5%~D

	TPM_ID0	TPM_ID1
Non-TPM	0	1
TPM	1	1

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	PCH (5/8)	
Size	Document Number: LA-7781	Rev: 1.0
Date: Friday, February 24, 2012	Sheet 18 of 61	



PCH Power Rail Table

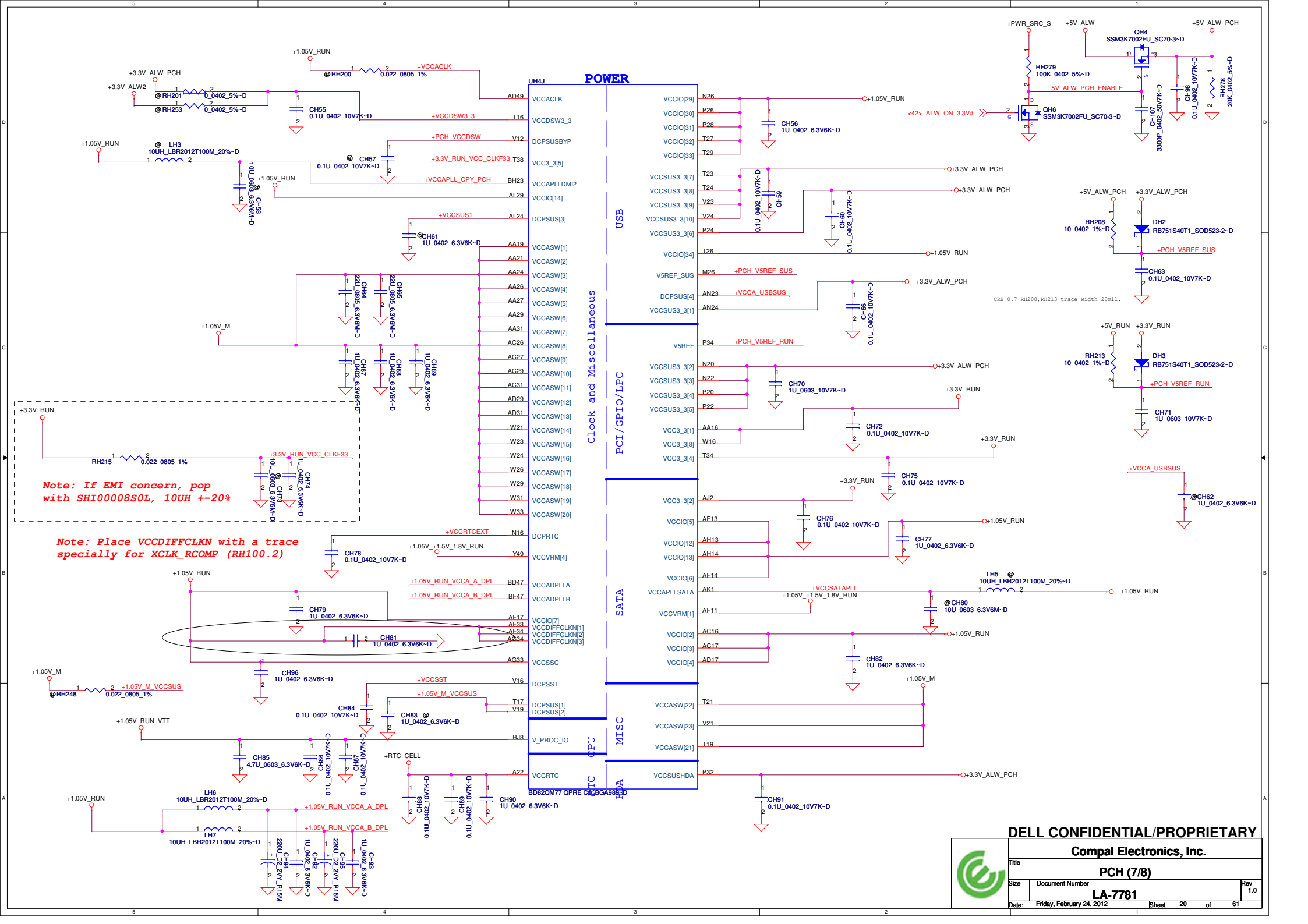
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC3	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VCCDFTERM	1.8	0.002
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Compal Electronics, Inc.

Title: PCH (6/8)

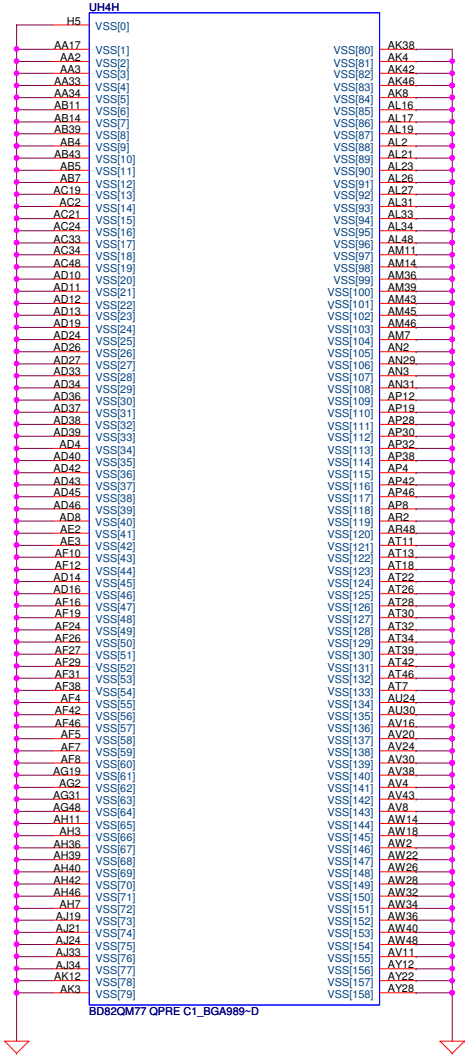
Size | Document Number: LA-7781 | Rev: 1.0

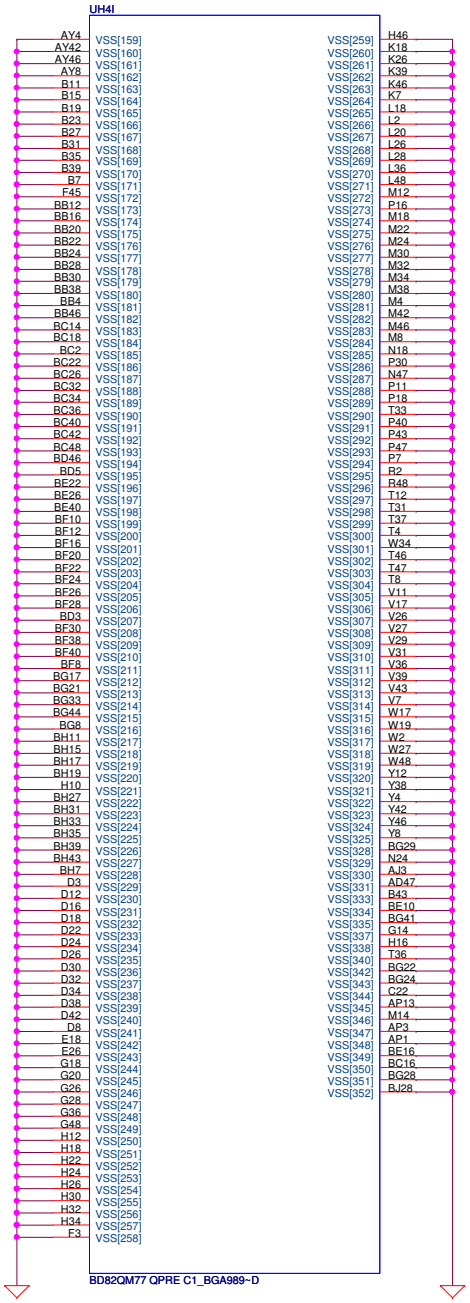
Date: Friday, February 24, 2012 | Sheet 19 of 61



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: PCH (7/8)		
Size	Document Number: LA-7781	Rev: 1.0
Date: Friday, February 24, 2012	Sheet 20 of 61	





DELL CONFIDENTIAL/PROPRIETARY

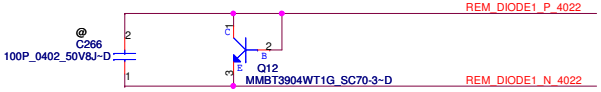
Compal Electronics, Inc.

Title: **PCH (8/8)**

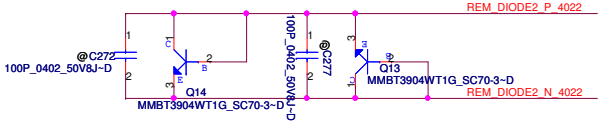
Size | Document Number: **LA-7781** | Rev: 1.0

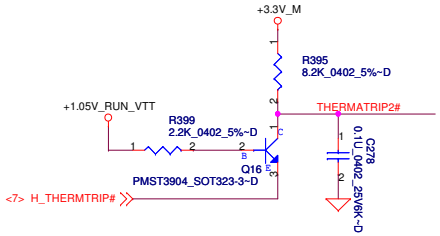
Date: Friday, February 24, 2012 | Sheet 21 of 61

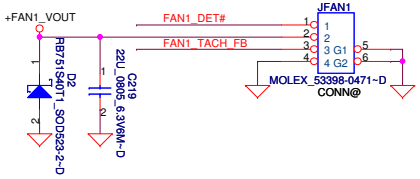
Place under CPU
Place C266 close to the Q12 as possible

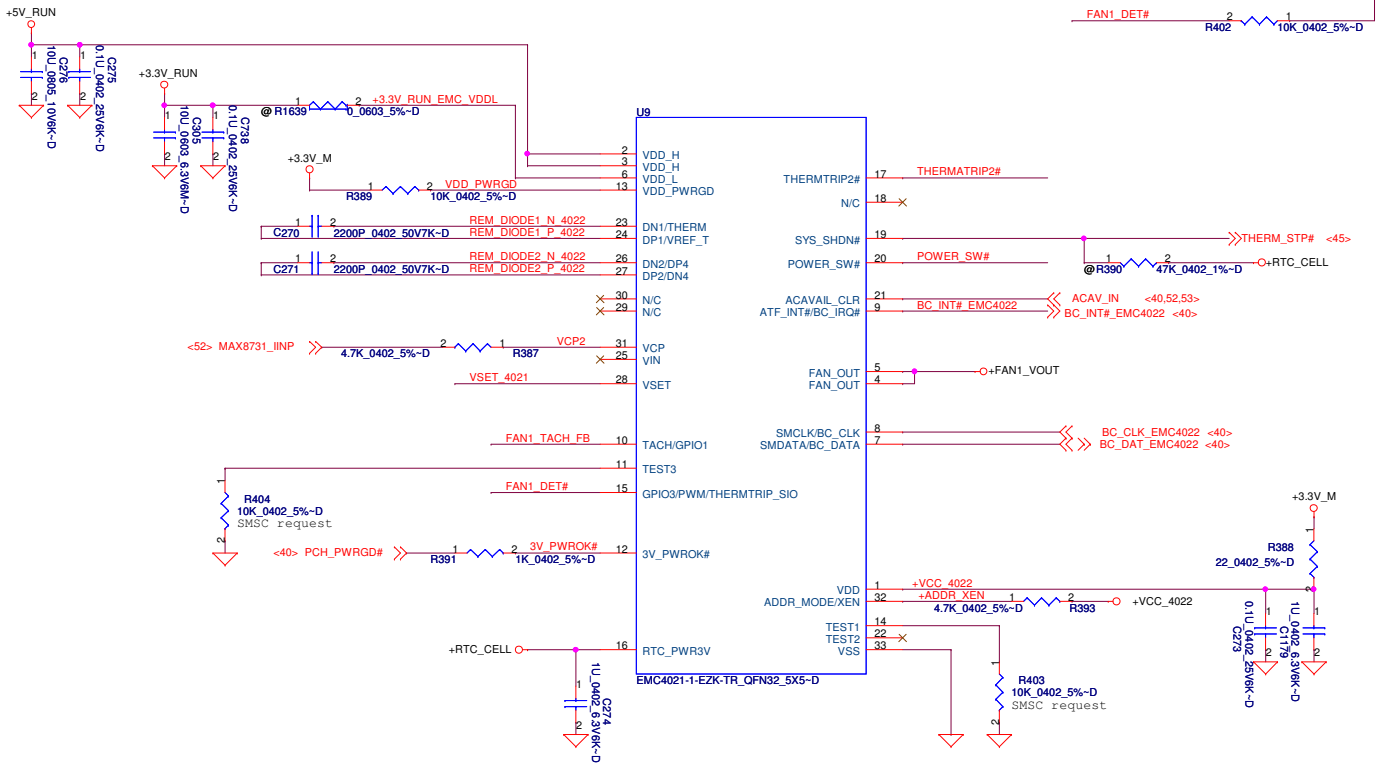


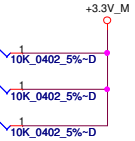
(1) DP2/DN2 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
(2) DP4/DN4 for Skin on Q13, place Q13 close to Vcore VR choke.

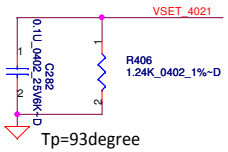


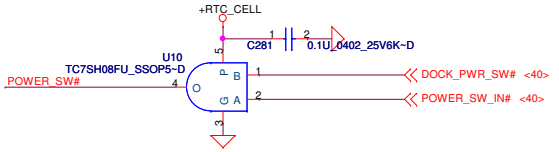












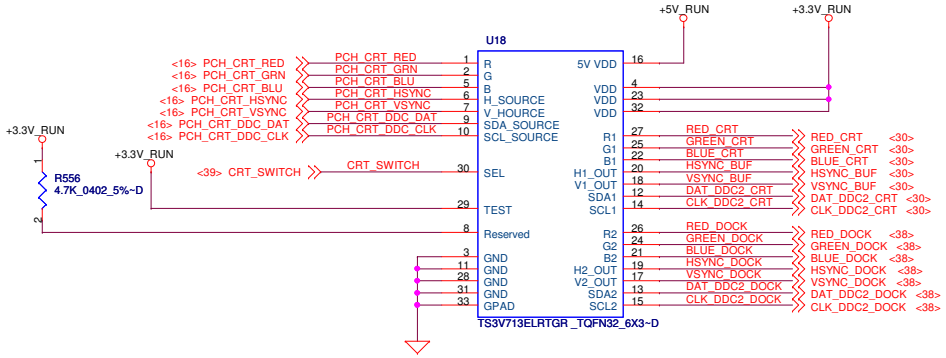
Compal Electronics, Inc.

Title: FAN & Thermal Sensor

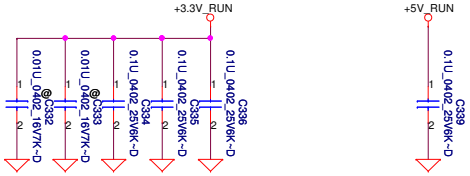
Size: | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 22 of 61

SW for MB/DOCK

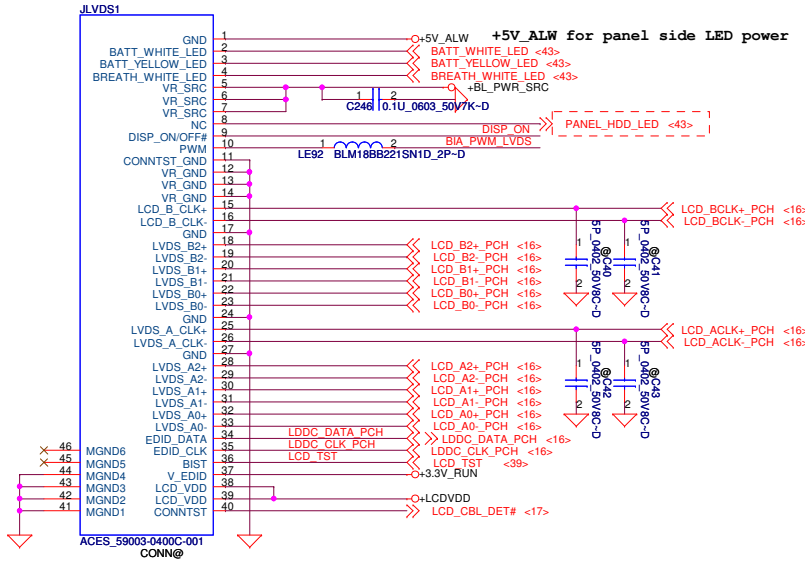


SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

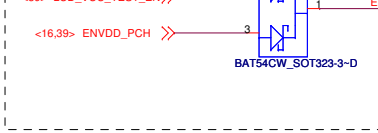


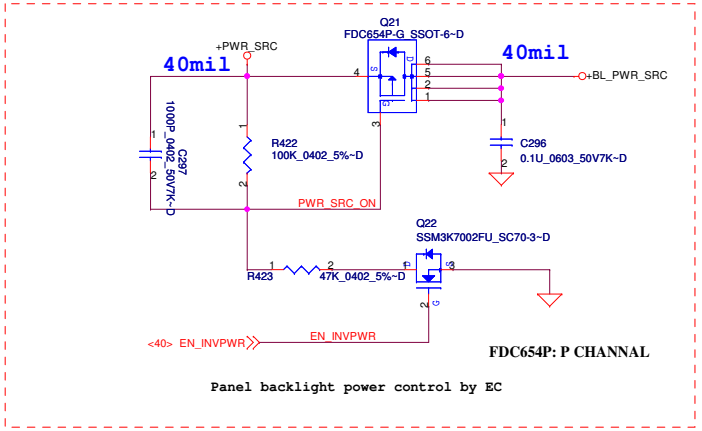
DELL CONFIDENTIAL/PROPRIETARY

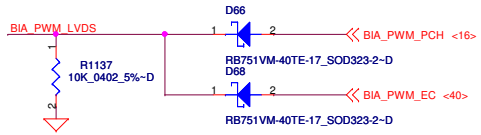
	Compal Electronics, Inc.	
	Title: CRT/Video switch	
Size	Document Number: LA-7781	Rev: 1.0
Date: Friday, February 24, 2012	Sheet 23 of 61	

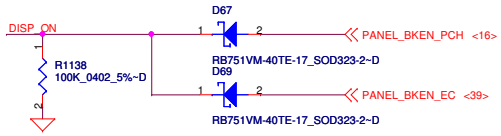


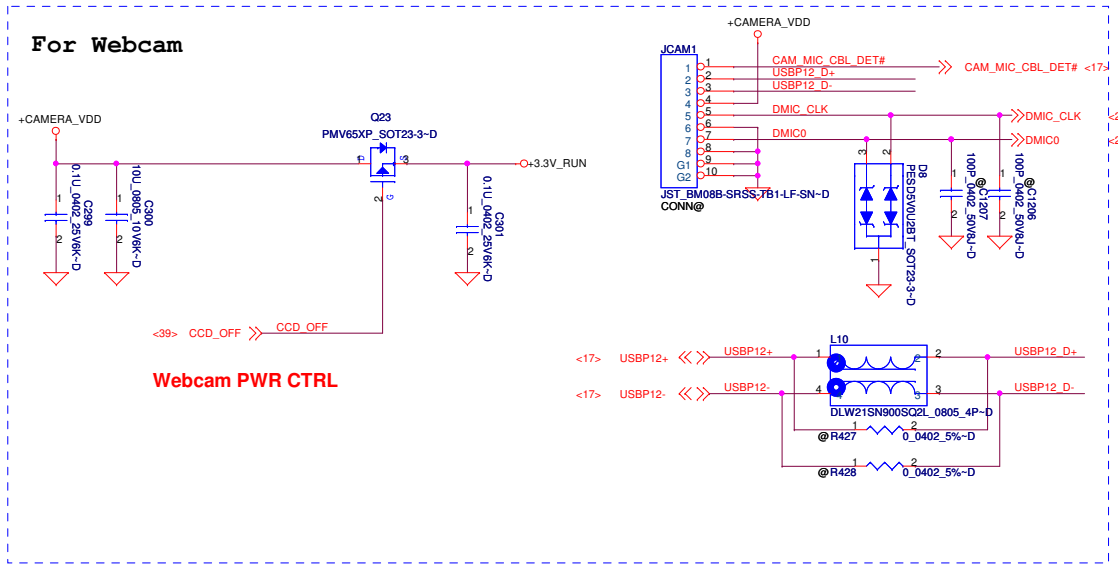
+5V_ALW for panel side LED power

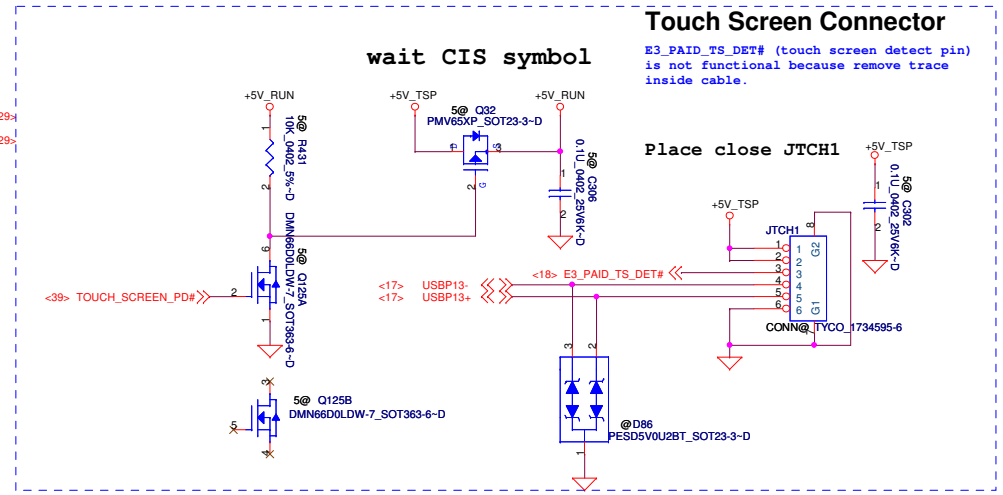






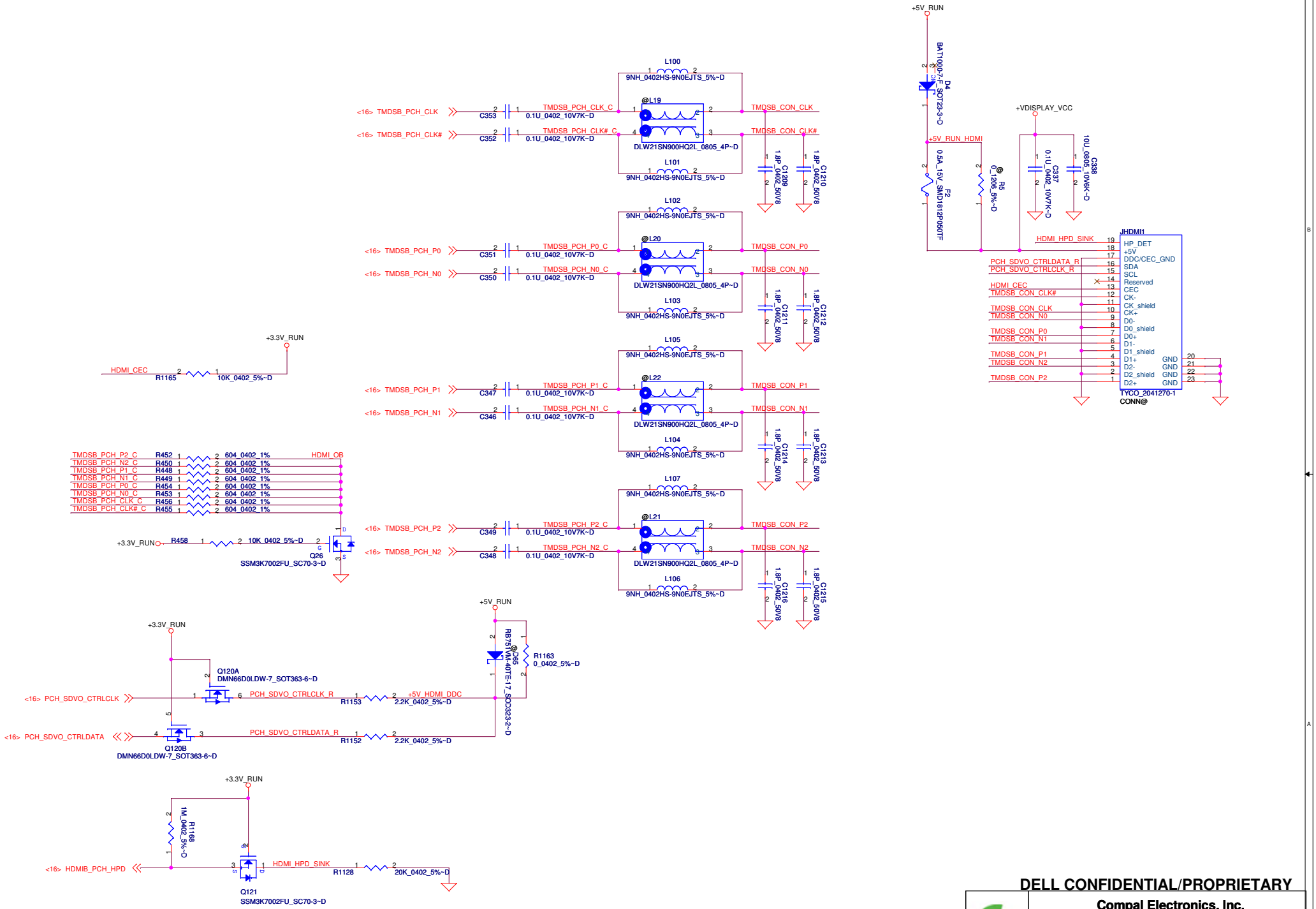






DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	eDP & CAM &TS Conn
Size	Document Number: LA-7781
Rev	1.0
Date:	Friday, February 24, 2012
Sheet	24 of 61



DELL CONFIDENTIAL/PROPRIETARY

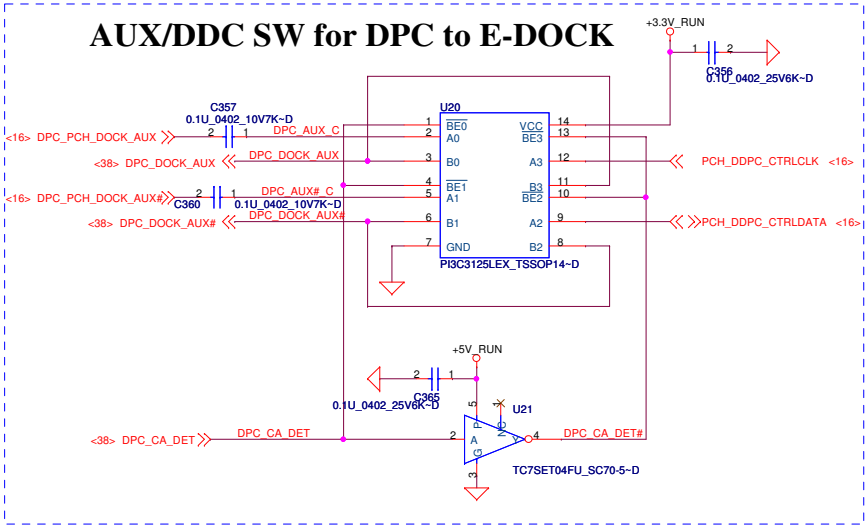
Compal Electronics, Inc.

Title: HDMI port

Size | Document Number: LA-7781 | Rev: 1.0

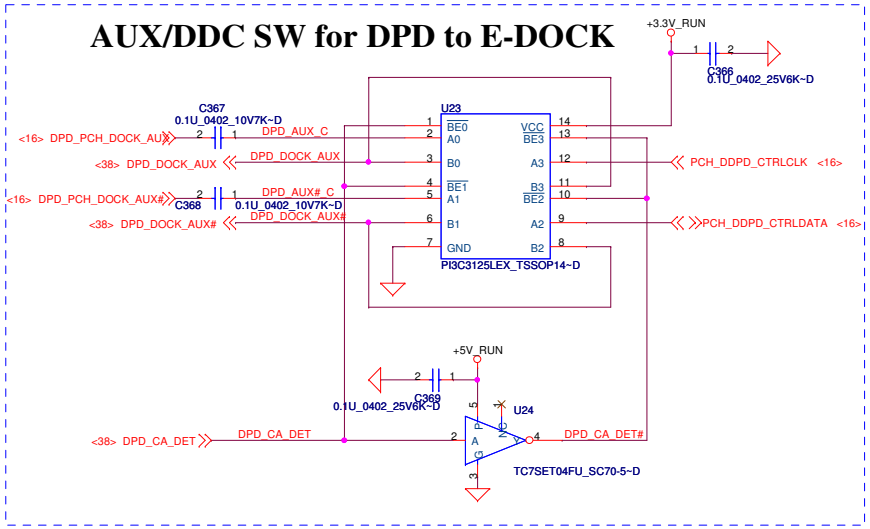
Date: Friday, February 24, 2012 | Sheet 25 of 61

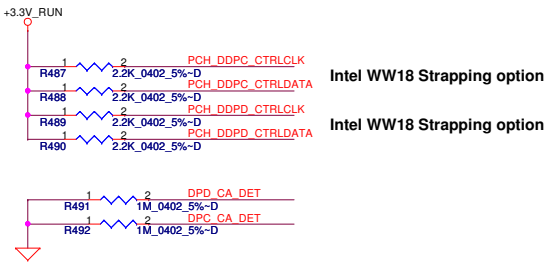
AUX/DDC SW for DPC to E-DOCK



There is a new die for PI3C3125. Sample availabe on May.

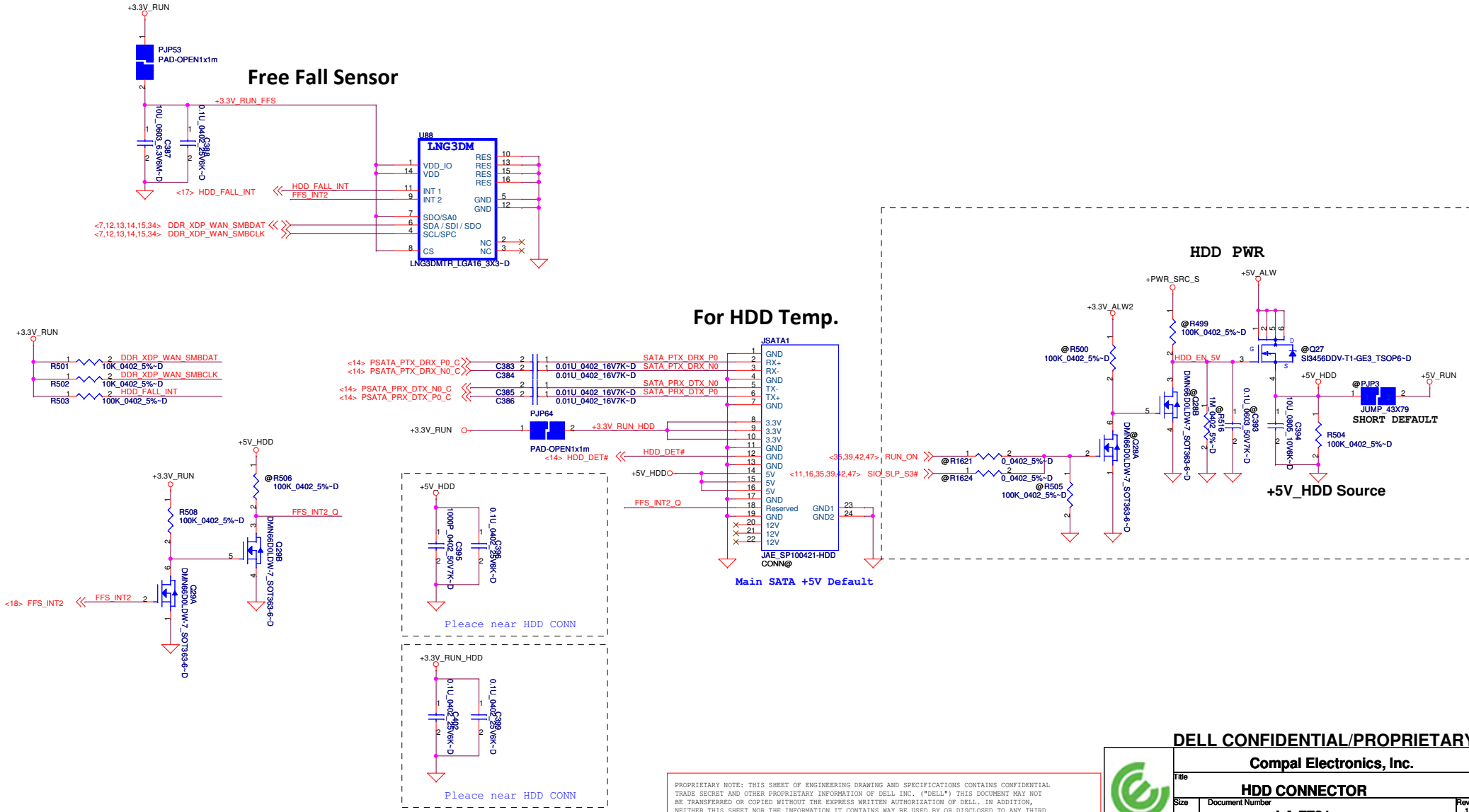
AUX/DDC SW for DPD to E-DOCK





DELL CONFIDENTIAL/PROPRIETARY

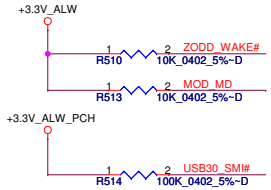
Compal Electronics, Inc.	
Title	DP AUX SW
Size	Document Number: LA-7781
Rev	1.0
Date:	Friday, February 24, 2012
Sheet	26 of 61

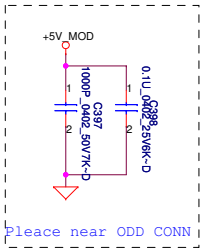


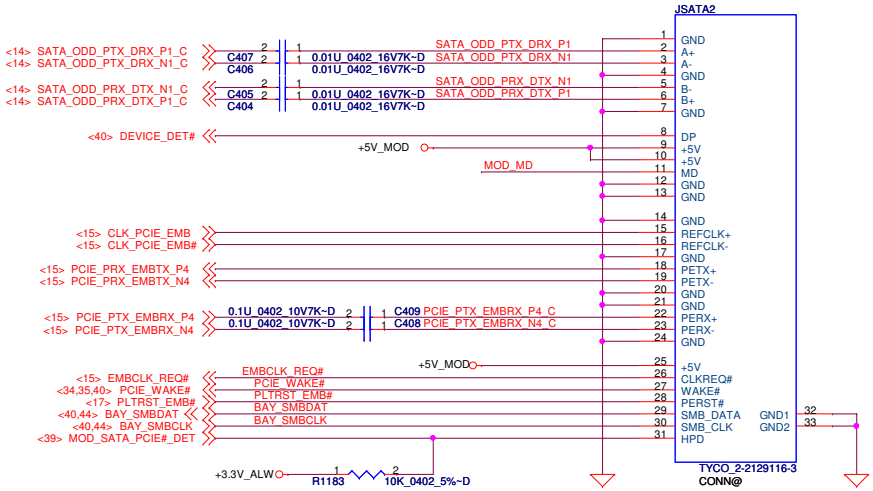
DELL CONFIDENTIAL/PROPRIETARY

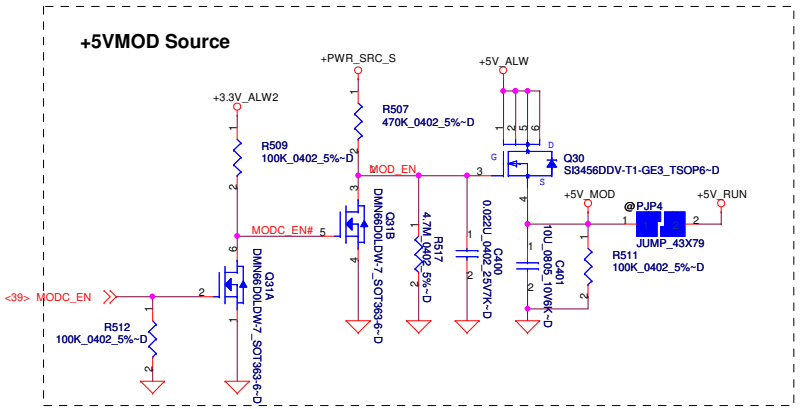
Compal Electronics, Inc.		
Title: HDD CONNECTOR		
Size	Document Number: LA-7781	Rev: 1.0
Date: Friday, February 24, 2012	Sheet 27 of 61	

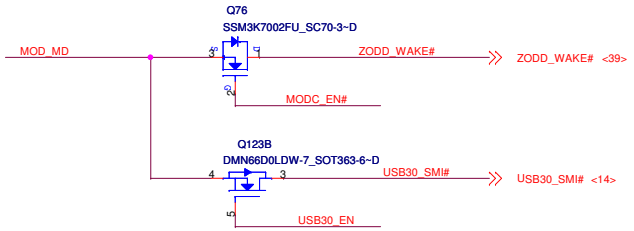
For ODD

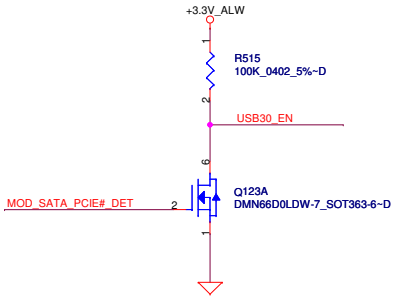












Compal Electronics, Inc.

Title: ODD CONNECTOR

Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 28 of 61

Internal Speakers Header

15 mils trace

DVDD_IO should match with HDA Bus level

Close to U72

Close to U72 pin5

Close to U72 pin6

Place closely to Pin 13.

Add for solve pop noise and detect issue

Place closely to Pin 14

Place C994, C952~C957 close to Codec

Place R1096 close to codec

Place R1097 close to codec

Place LE3 close to codec

Place C962 close to Codec

Place C963~C966 close to Codec

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK

Compal Electronics, Inc.

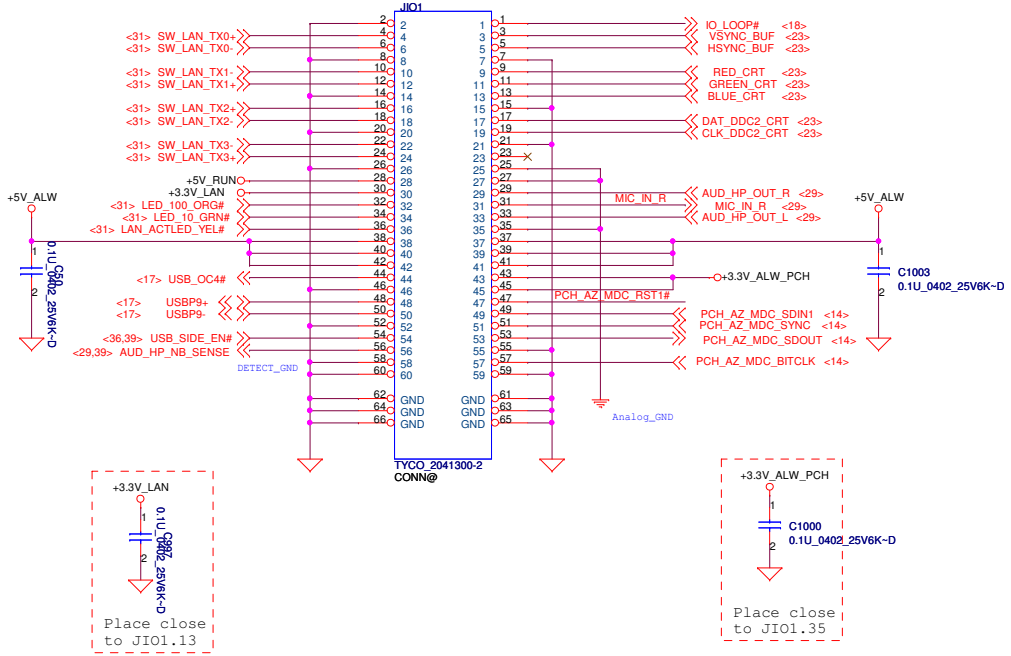
Title: Azalia (HD) Codec

Size: | Document Number: LA-7781 | Rev: 1.0

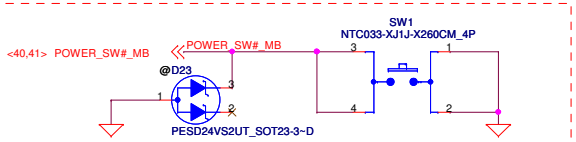
Date: Friday, February 24, 2012 | Sheet 29 of 61

I/O board CONN.

Change to TYCO_2041300-2_60P-T and Horizonal reverse to SSI

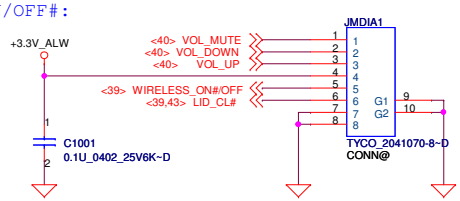


POWER & INSTANT ON SWITCH

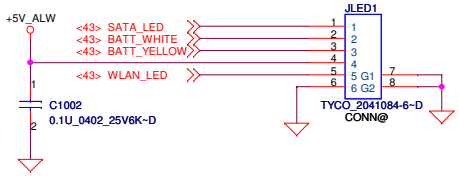


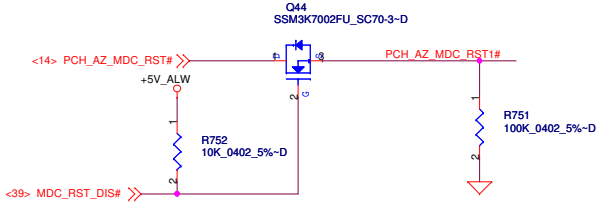
Media Board

Defult on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF



LED Board



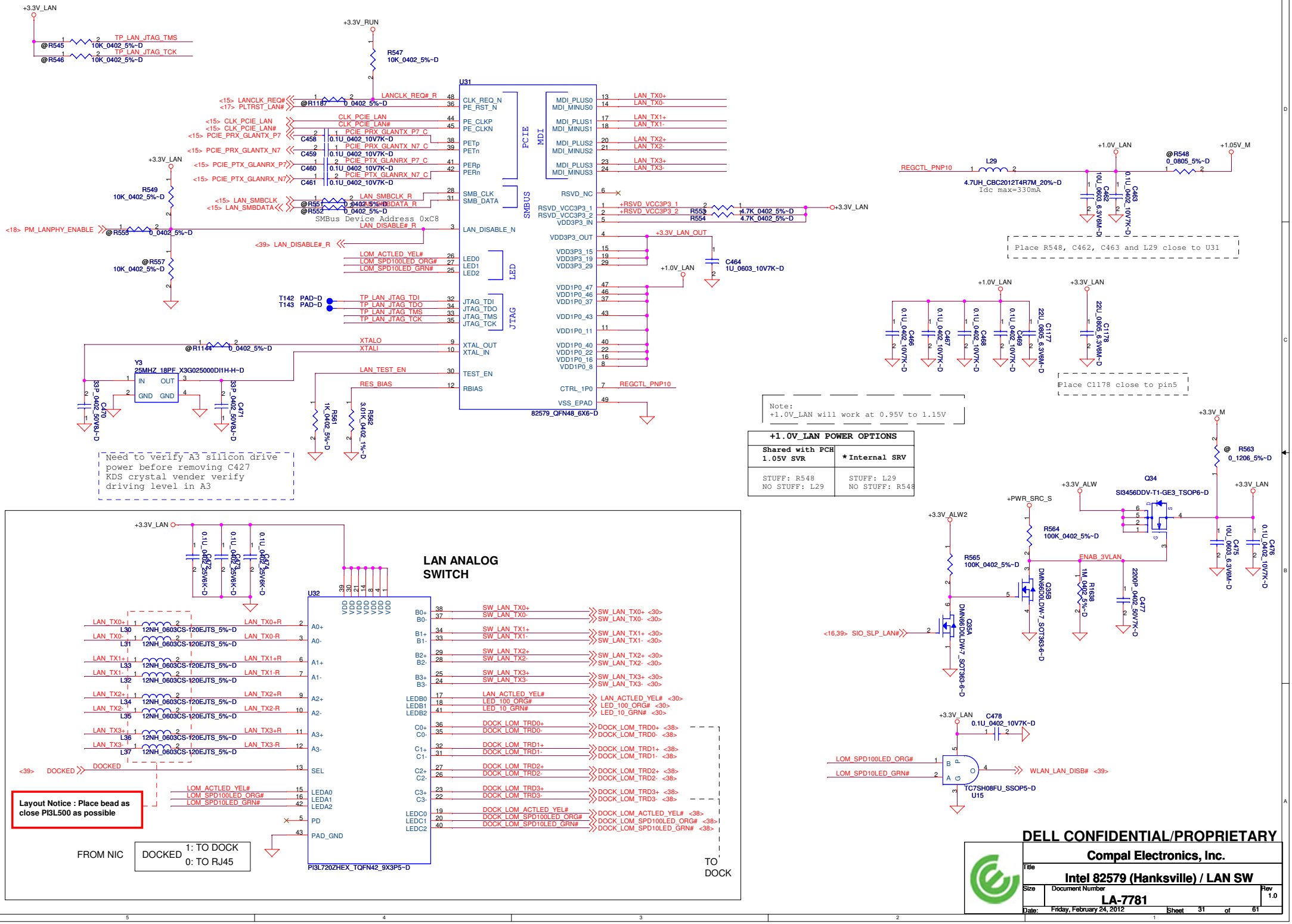


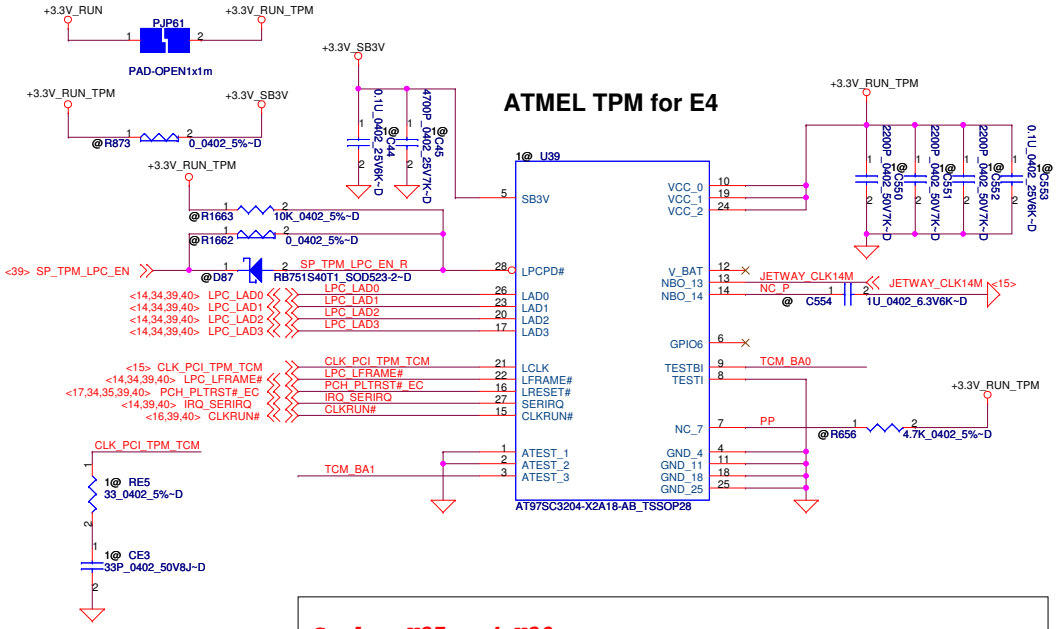
Compal Electronics, Inc.

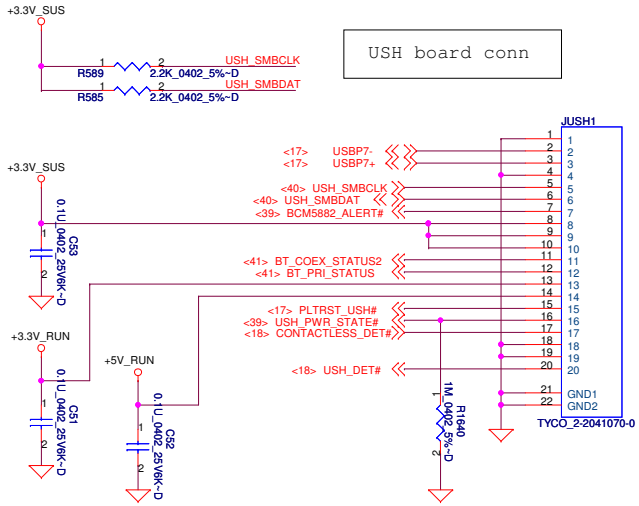
Title: PWR SW/Sub-board Connector

Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 30 of 61


+3.3V_LAN
+3.3V_RUN
TP_LAN_JTAG_TMS
TP_LAN_JTAG_TCK
@R545
@R546
10K_0402_5%~D
R547
U31
LANCLK_REQ# R
CLK_REQ_N
PE_RST_N
PE_CLKP
PE_CLKN
PETp
PETn
PERp
PERn
PCIE
MDI
SMB_CLK
SMB_DATA
SMBUS
LAN_DISABLE_N
LED0
LED1
LED2
LED
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
JTAG
XTAL_OUT
XTAL_IN
TEST_EN
RBIAS
RSVD_NC
VDD3P3_OUT
VDD1P0_47
VDD1P0_46
VDD1P0_37
VDD1P0_43
VDD1P0_11
VDD1P0_40
VDD1P0_22
VDD1P0_16
VDD1P0_8
CTRL_1P0
VSS_EPAD
82579_QFN48_6X6~D
MDI_PLUS0
MDI_MINUS0
MDI_PLUS1
MDI_MINUS1
MDI_PLUS2
MDI_MINUS2
MDI_PLUS3
MDI_MINUS3
LAN_TX0+
LAN_TX0-
LAN_TX1+
LAN_TX1-
LAN_TX2+
LAN_TX2-
LAN_TX3+
LAN_TX3-
+RSVD_VCC3P3_1
+RSVD_VCC3P3_2
R553
R554
4.7K_0402_5%~D
+3.3V_LAN_OUT
C464
1U_0603_10V7K~D
+1.0V_LAN
R549
10K_0402_5%~D
@R557
<18> PM_LANPHY_ENABLE
@R555
LAN_DISABLE# R
<39> LAN_DISABLE#_R
LOM_ACTLED_YEL#
LOM_SPD100LED_ORG#
LOM_SPD10LED_GRN#
T142 PAD~D
T143 PAD~D
XTALO
XTALI
@R1144
Y3
25MHZ_18PF_X3G025000DI1H-H~D
IN
OUT
GND
C470
C471
33P_0402_50V8J~D
LAN_TEST_EN
RES_BIAS
R561
1K_0402_5%~D
R562
3.01K_0402_1%~D
REGCTL_PNP10
Need to verify A3 silicon drive power before removing C427
KDS crystal vender verify driving level in A3
L29
4.7UH_CBC2012T4R7M_20%~D
Idc max=330mA
@R548
0_0805_5%~D
C462
C463
10U_0603_6.3V6M~D
0.1U_0402_10V7K~D
Place R548, C462, C463 and L29 close to U31
C466
C467
C468
C469
C1177
22U_0805_6.3V6M~D
C1178
Place C1178 close to pin5
Note:
+1.0V_LAN will work at 0.95V to 1.15V
+1.0V_LAN POWER OPTIONS
Shared with PCH 1.05V SVR
*Internal SRV
STUFF: R548
NO STUFF: L29
STUFF: L29
NO STUFF: R548
+3.3V_M
@ R563
0_1206_5%~D
Q34
SI3456DDV-T1-GE3_TSOP6~D
+3.3V_ALW
+PWR_SRC_S
+3.3V_ALW2
R564
100K_0402_5%~D
R565
100K_0402_5%~D
ENAB_3VLAN
Q35A
DMN66D0LDW-7_SOT363-6~D
Q35B
DMN66D0LDW-7_SOT363-6~D
<16,39> SIO_SLP_LAN#
R1638
1M_0402_5%~D
C477
2200P_0402_50V7K~D
C475
C476
C478
0.1U_0402_10V7K~D
LOM_SPD100LED_ORG#
LOM_SPD10LED_GRN#
WLAN_LAN_DISB# <39>
TC7SH08FU_SSOP5~D
U15
LAN ANALOG SWITCH
U32
LAN_TX0+R
LAN_TX0-R
LAN_TX1+R
LAN_TX1-R
LAN_TX2+R
LAN_TX2-R
LAN_TX3+R
LAN_TX3-R
L30
L31
L33
L32
L34
L35
L36
L37
12NH_0603CS-120EJTS_5%~D
A0+
A0-
A1+
A1-
A2+
A2-
A3+
A3-
SEL
LEDA0
LEDA1
LEDA2
PD
PAD_GND
<39> DOCKED
LOM_ACTLED_YEL#
LOM_SPD100LED_ORG#
LOM_SPD10LED_GRN#
Layout Notice : Place bead as close PI3L500 as possible
FROM NIC
DOCKED 1: TO DOCK 0: TO RJ45
PI3L720ZHEX_TQFN42_9X3P5~D
SW_LAN_TX0+ <30>
SW_LAN_TX0- <30>
SW_LAN_TX1+ <30>
SW_LAN_TX1- <30>
SW_LAN_TX2+ <30>
SW_LAN_TX2- <30>
SW_LAN_TX3+ <30>
SW_LAN_TX3- <30>
LAN_ACTLED_YEL# <30>
LED_100_ORG# <30>
LED_10_GRN# <30>
DOCK_LOM_TRD0+ <38>
DOCK_LOM_TRD0- <38>
DOCK_LOM_TRD1+ <38>
DOCK_LOM_TRD1- <38>
DOCK_LOM_TRD2+ <38>
DOCK_LOM_TRD2- <38>
DOCK_LOM_TRD3+ <38>
DOCK_LOM_TRD3- <38>
DOCK_LOM_ACTLED_YEL# <38>
DOCK_LOM_SPD100LED_ORG# <38>
DOCK_LOM_SPD10LED_GRN# <38>
TO DOCK
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Title
Intel 82579 (Hanksville) / LAN SW
Size
Document Number
LA-7781
Rev 1.0
Date: Friday, February 24, 2012
Sheet 31 of 61

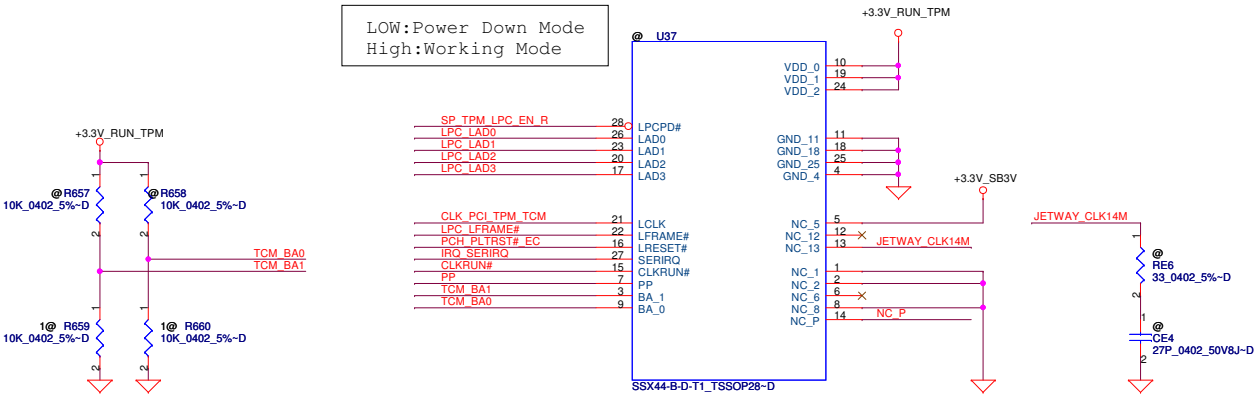




Co-lay U37 and U38

LPC layout: Place TCM first and then end LPC with TPM.

China TCM: NationZ & Jetway co-lay



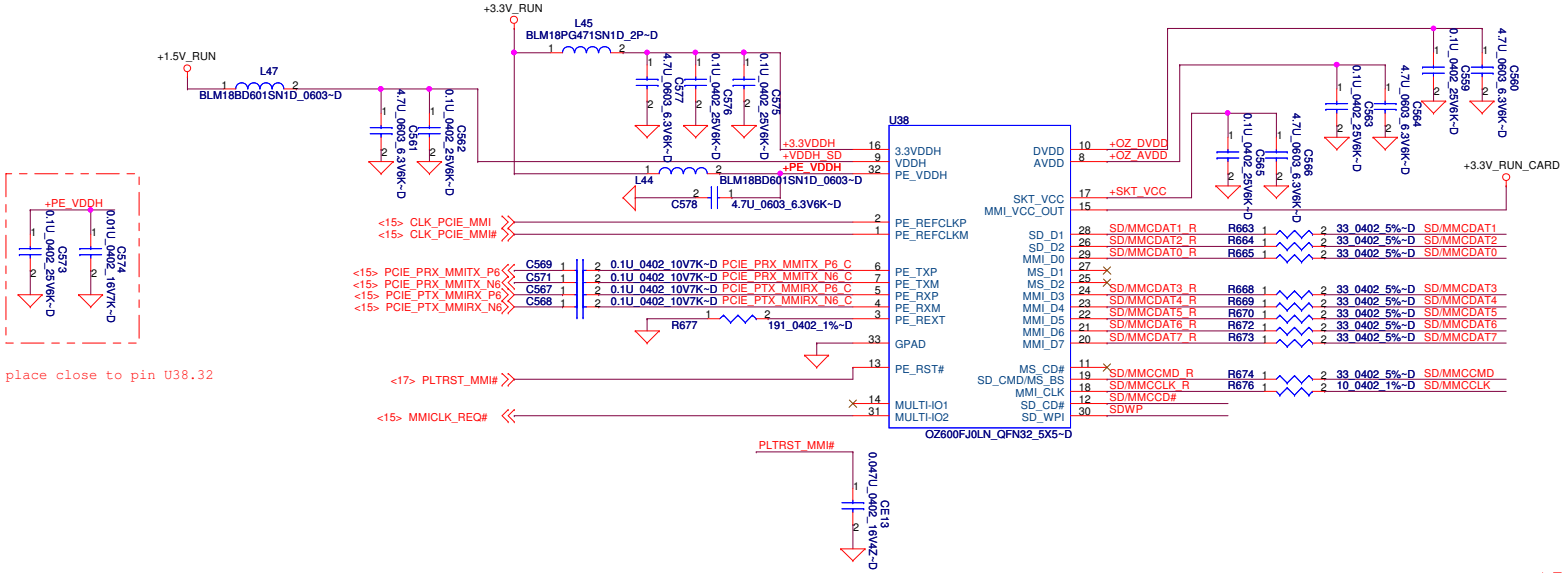
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

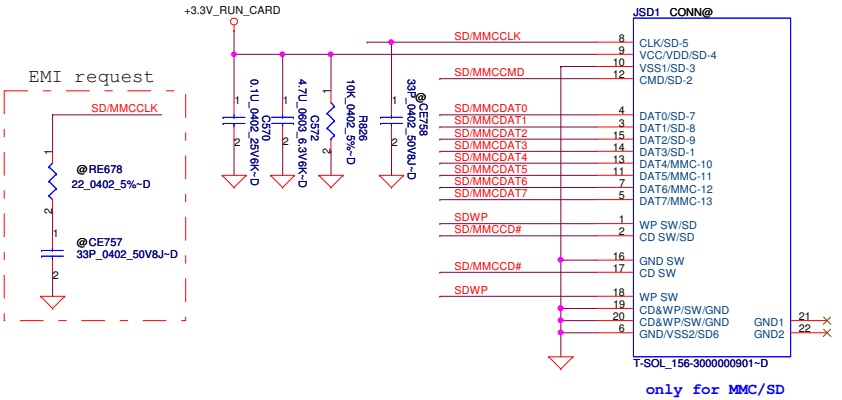
Title: TPM/TCM

Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 32 of 61



Note: The trace need to route as daisy-chain and the trace of SD signals need to route as short as possible



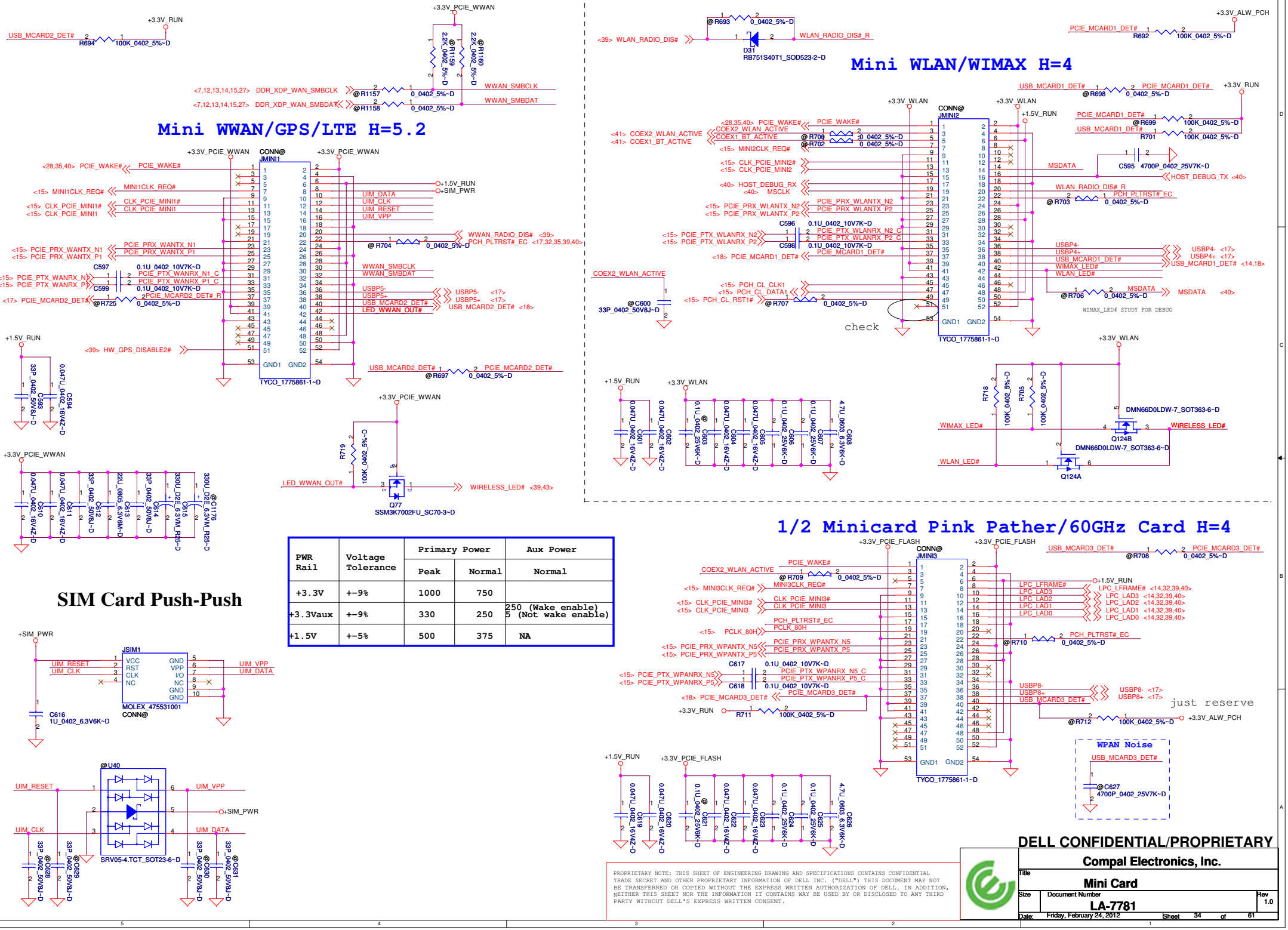
only for MMC/SD

Compal Electronics, Inc.

Title: Card Reader OZ600FJ0

Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 33 of 61



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

DELL CONFIDENTIAL/PROPRIETARY

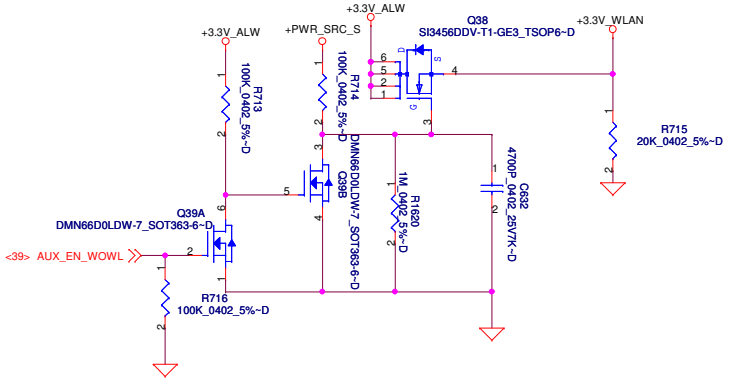
Compal Electronics, Inc.

Title: Mini Card

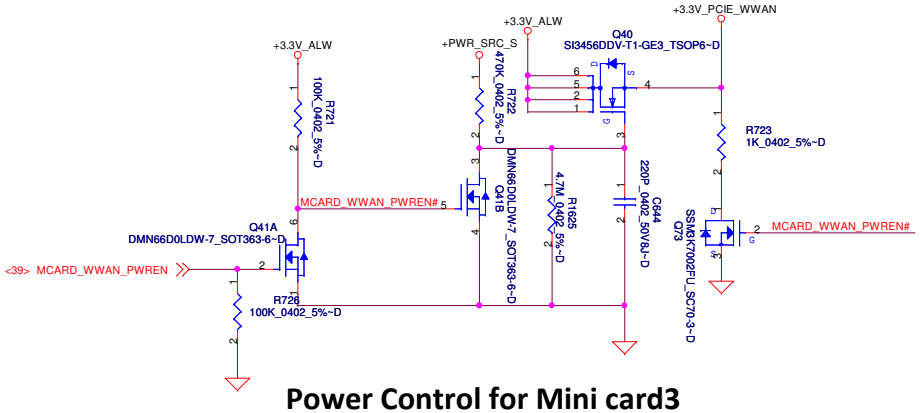
Size: | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 34 of 61

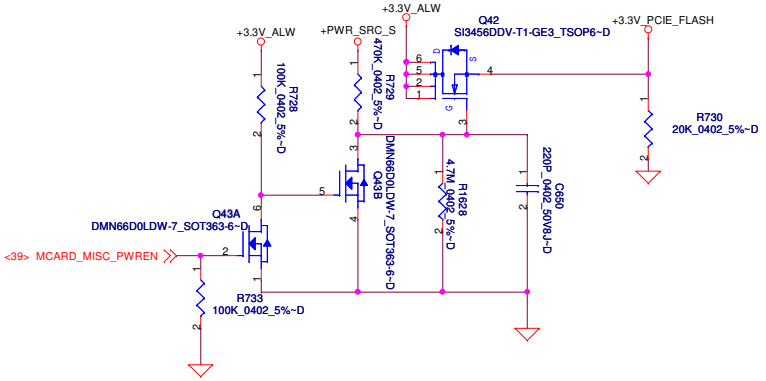
Power Control for Mini card2



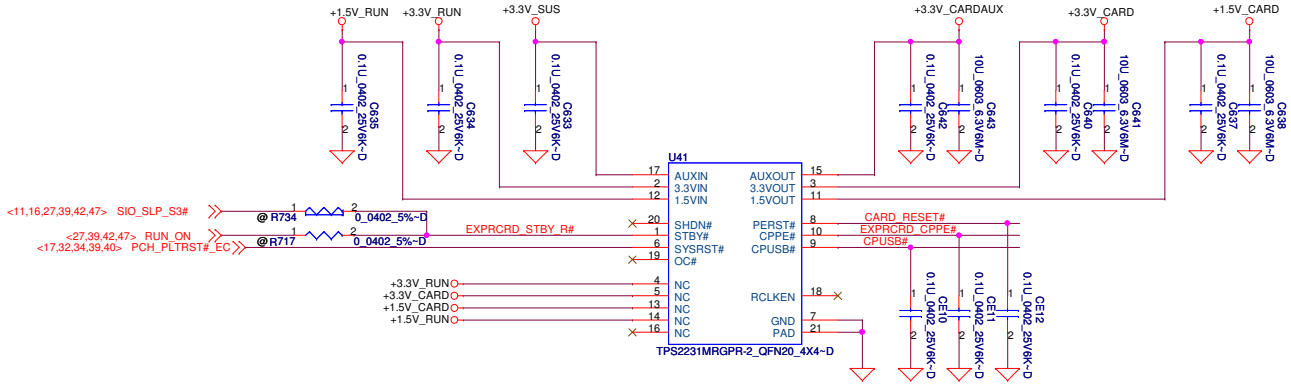
Power Control for Mini card1



Power Control for Mini card3

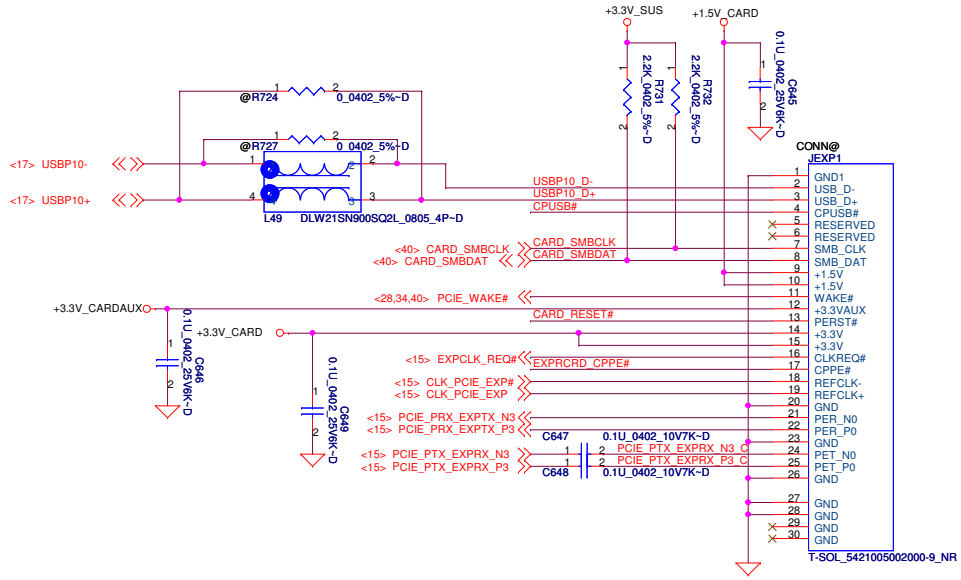


Express Card PWR S/W



Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part

Express Card Conn.

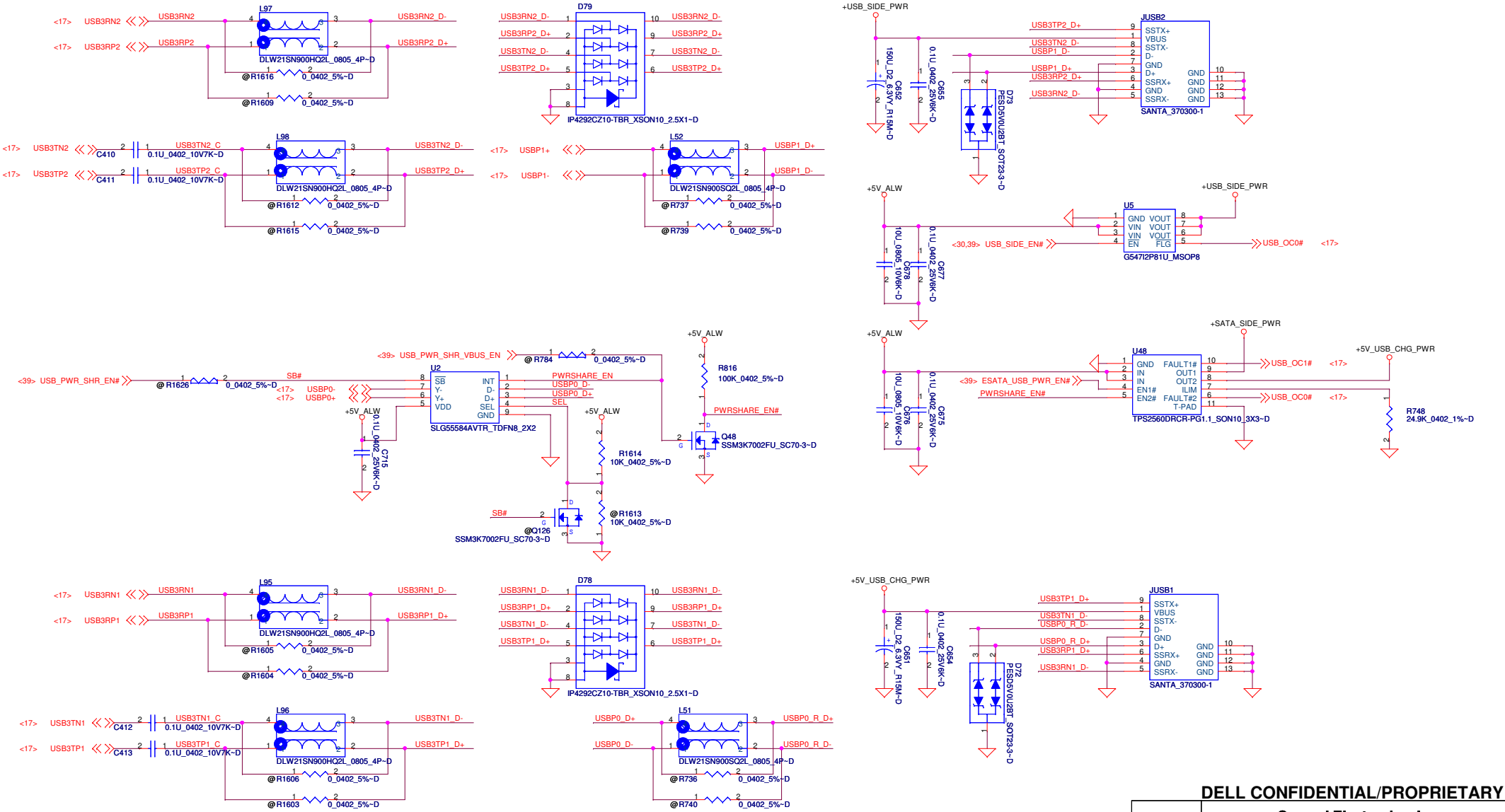


Compal Electronics, Inc.

Title: PCIE-SATA SW / PCIE PWR

Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 35 of 61



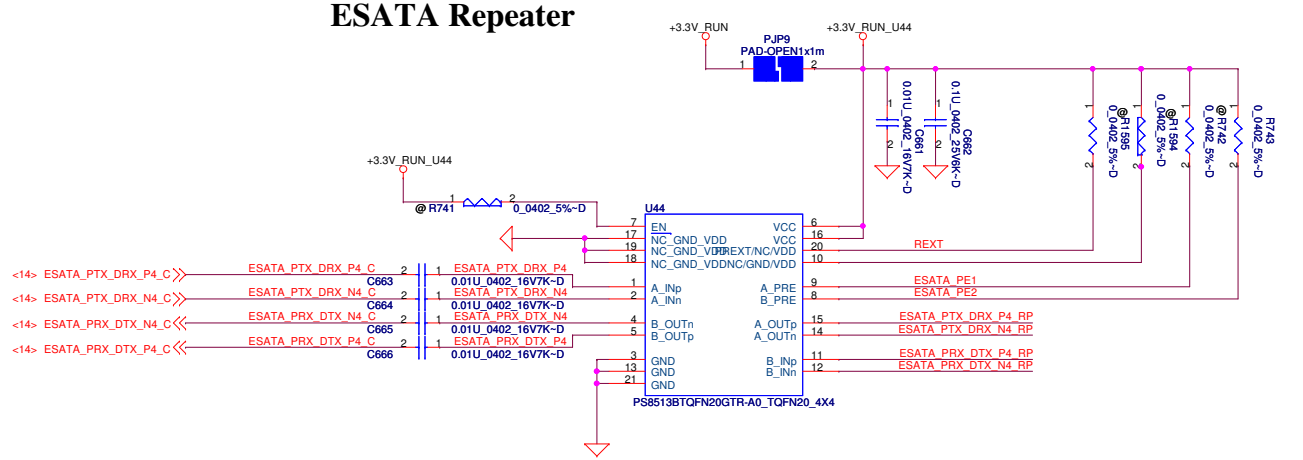
Compal Electronics, Inc.

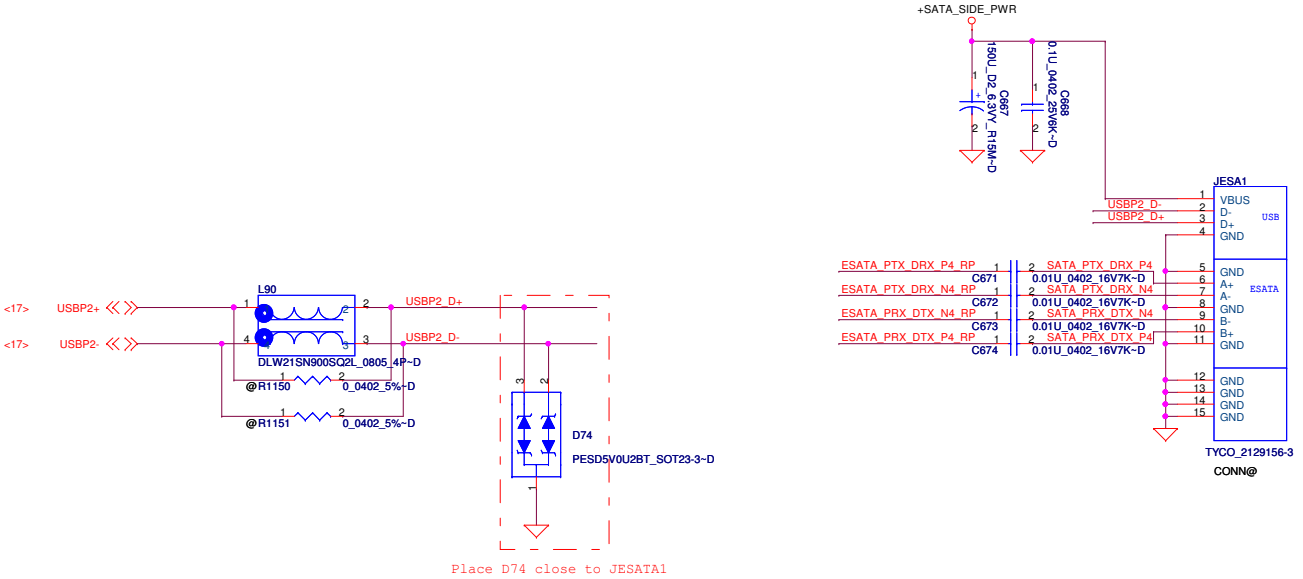
Title: USB x2

Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 36 of 61

ESATA Repeater



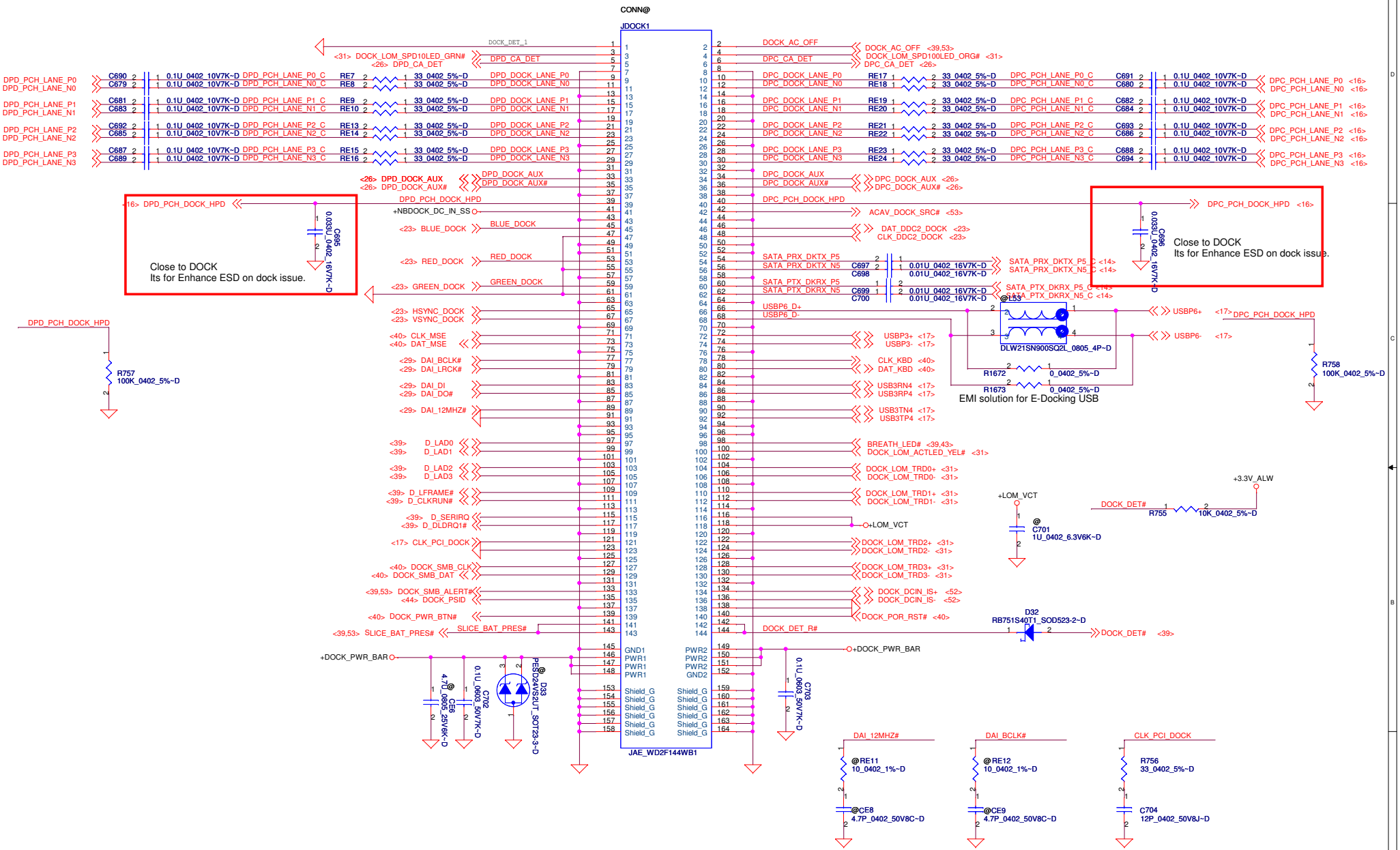


Compal Electronics, Inc.

Title: USB/ESATA/IO/MDC

Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 37 of 61

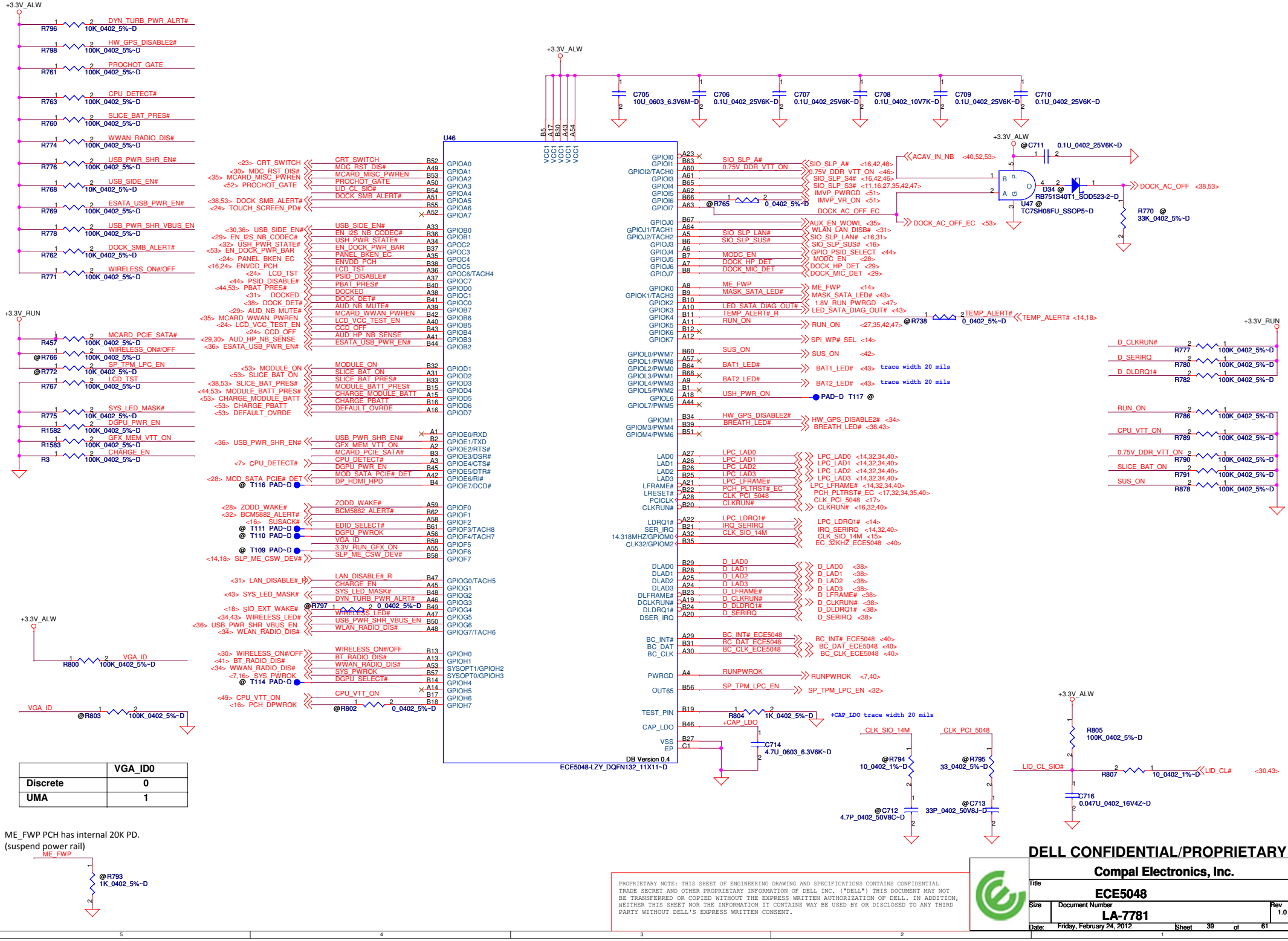


Compal Electronics, Inc.

Title: DOCKING CONN

Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 38 of 61



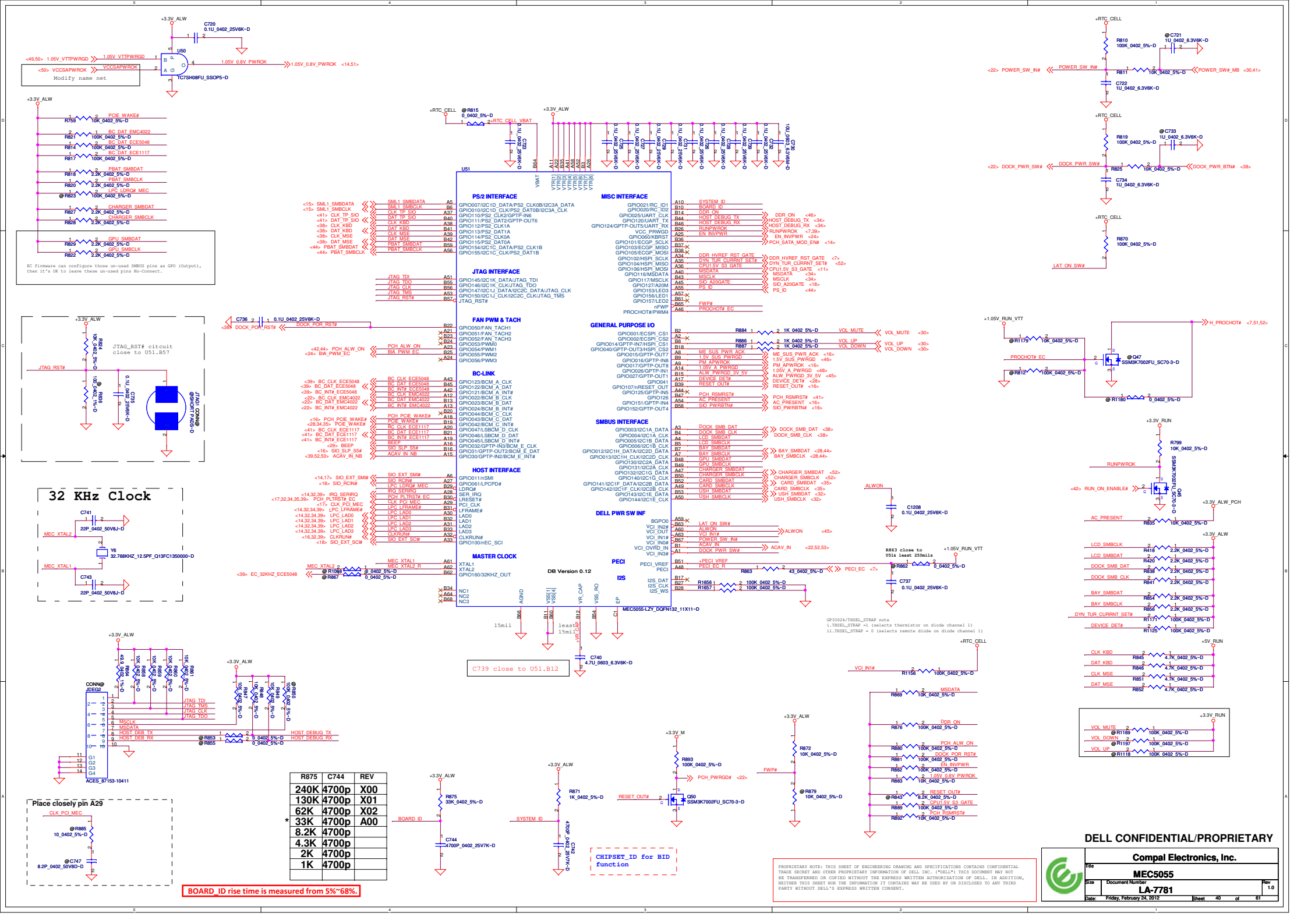
	VGA_ID0
Discrete	0
UMA	1

Compal Electronics, Inc.

Title: ECE5048

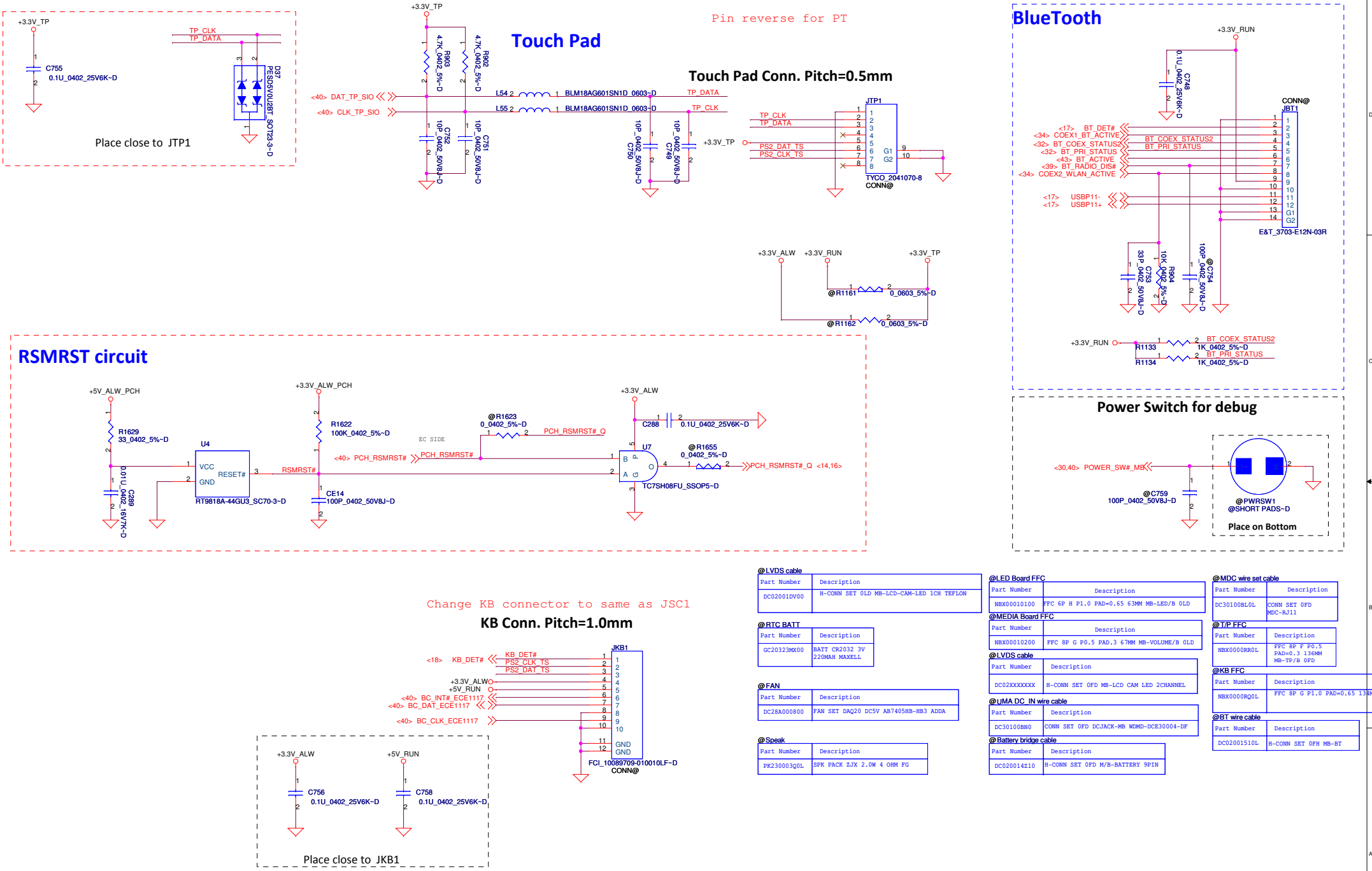
Size: | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 39 of 61



R875	C744	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
* 33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.



@LVDS cable

Part Number	Description
DC02001DV00	H-CONN SET 0LD MB-LCD-CAM-LED 1CH TEFLON

@RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

@LED Board FFC

Part Number	Description
NBX00010100	FFC 6P H P1.0 PAD=0.65 63MM MB-LED/B 0LD

@MEDIA Board FFC

Part Number	Description
NBX00010200	FFC 8P G P0.5 PAD.3 67MM MB-VOLUME/B 0LD

@LVDS cable

Part Number	Description
DC02XXXXXXX	H-CONN SET 0FD MB-LCD CAM LED 2CHANNEL

@UMA DC_IN wire cable

Part Number	Description
DC30100BN0	CONN SET 0FD DCJACK-MB WDMD-DCE30004-DF

@Battery bridge cable

Part Number	Description
DC020014Z10	H-CONN SET 0FD M/B-BATTERY 9PIN

@MDC wire set cable

Part Number	Description
DC30100BL0L	CONN SET 0FD MDC-RJ11

@T/P FFC

Part Number	Description
NBX0000RR0L	FFC 8P F P0.5 PAD=0.3 136MM MB-TP/B 0FD

@KB FFC

Part Number	Description
NBX0000RQ0L	FFC 8P G P1.0 PAD=0.65 130MM MB-KB 0FD

@BT wire cable

Part Number	Description
DC02001510L	H-CONN SET 0FH MB-BT

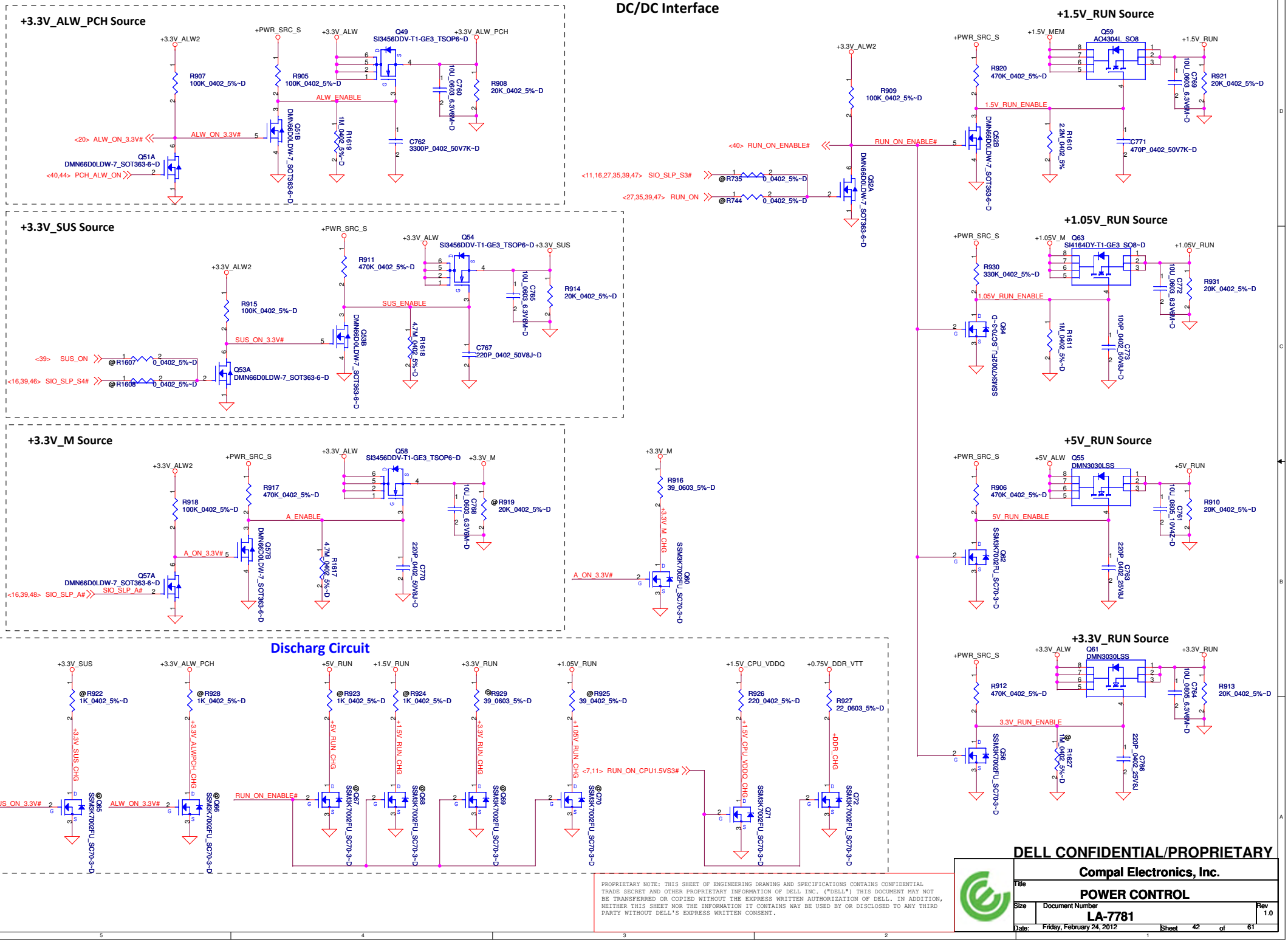
Compal Electronics, Inc.

Title: TP/KB/BT/FAN/RESET

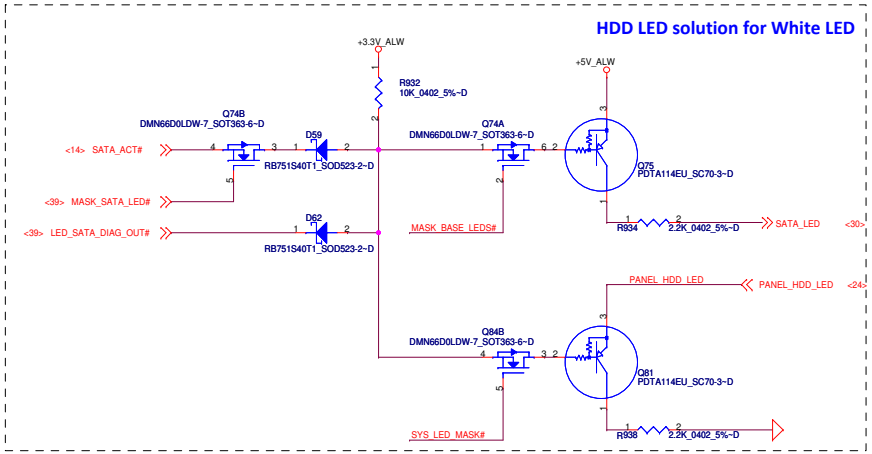
Size | Document Number: LA-7781 | Rev: 1.0

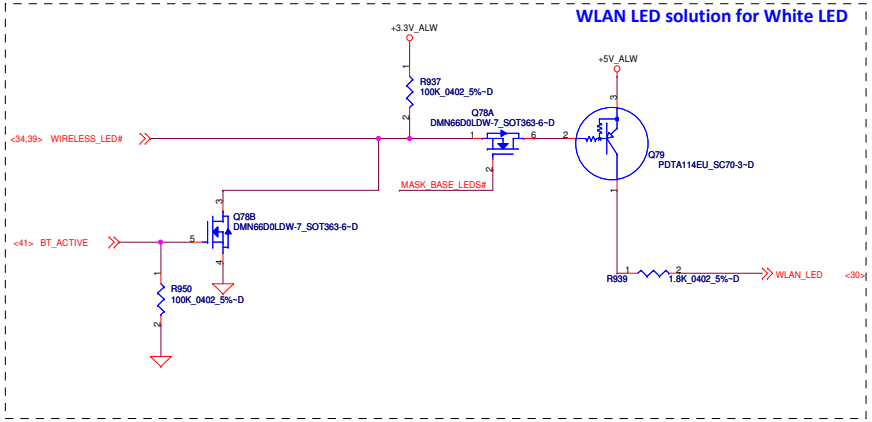
Date: Friday, February 24, 2012 | Sheet 41 of 61

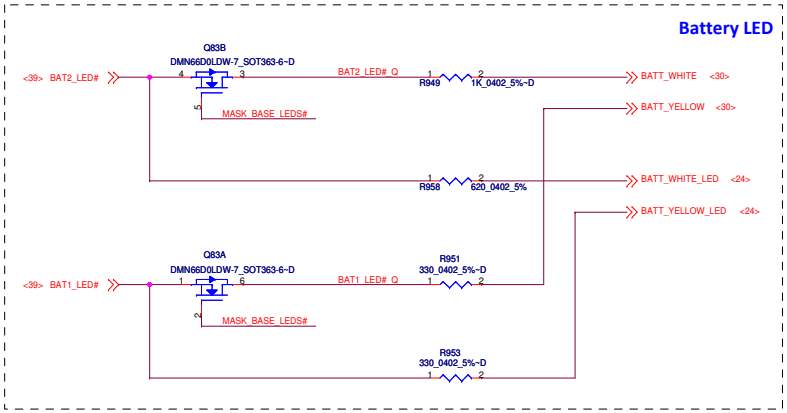
DC/DC Interface

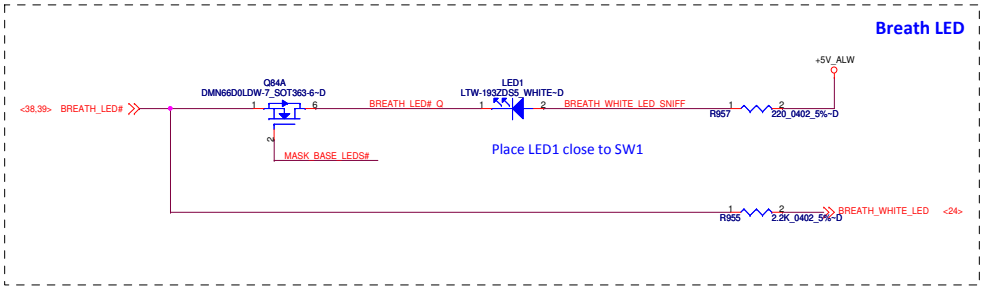


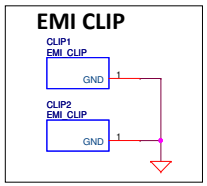
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.











Fiducial Mark

@FD1	FIDUCIAL MARK~D
@FD2	FIDUCIAL MARK~D
@FD3	FIDUCIAL MARK~D
@FD4	FIDUCIAL MARK~D

LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

@H1 H_3P3 @H2 H_3P3 @H3 H_3P0 @H4 H_3P3 @H5 H_3P0 @H6 H_3P0 @H8 H_3P2 @H9 H_3P0 @H10 H_3P3 @H12 H_3P0 @H13 H_3P0 @H14 H_3P0 @H15 H_3P0 @H16 H_3P0 @H19 H_3P0x2P0 @H20 H_2P0N @H17 H_3P0 @H24 H_2P8 @H25 H_2P8

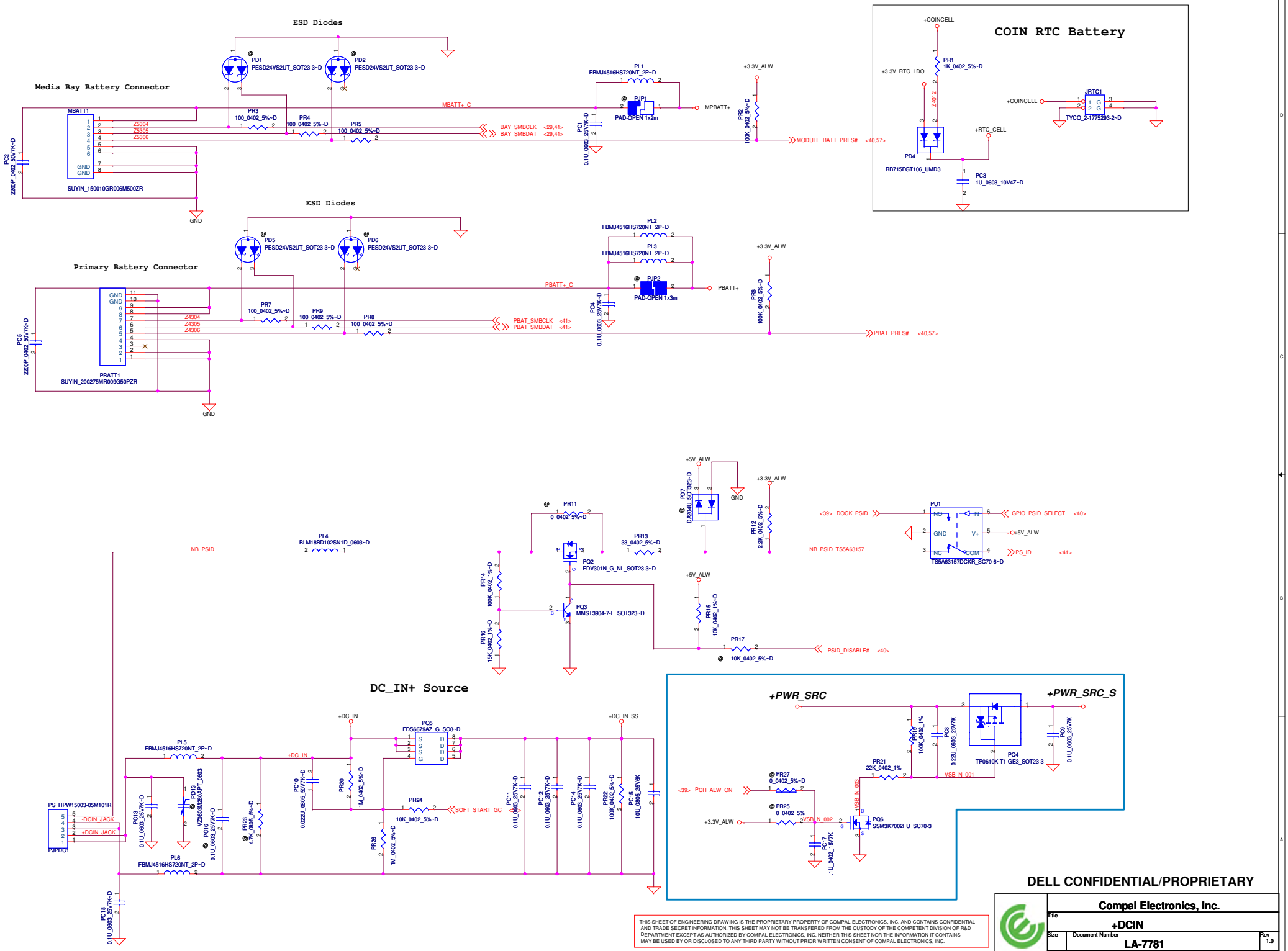
DELL CONFIDENTIAL/PROPRIETARY

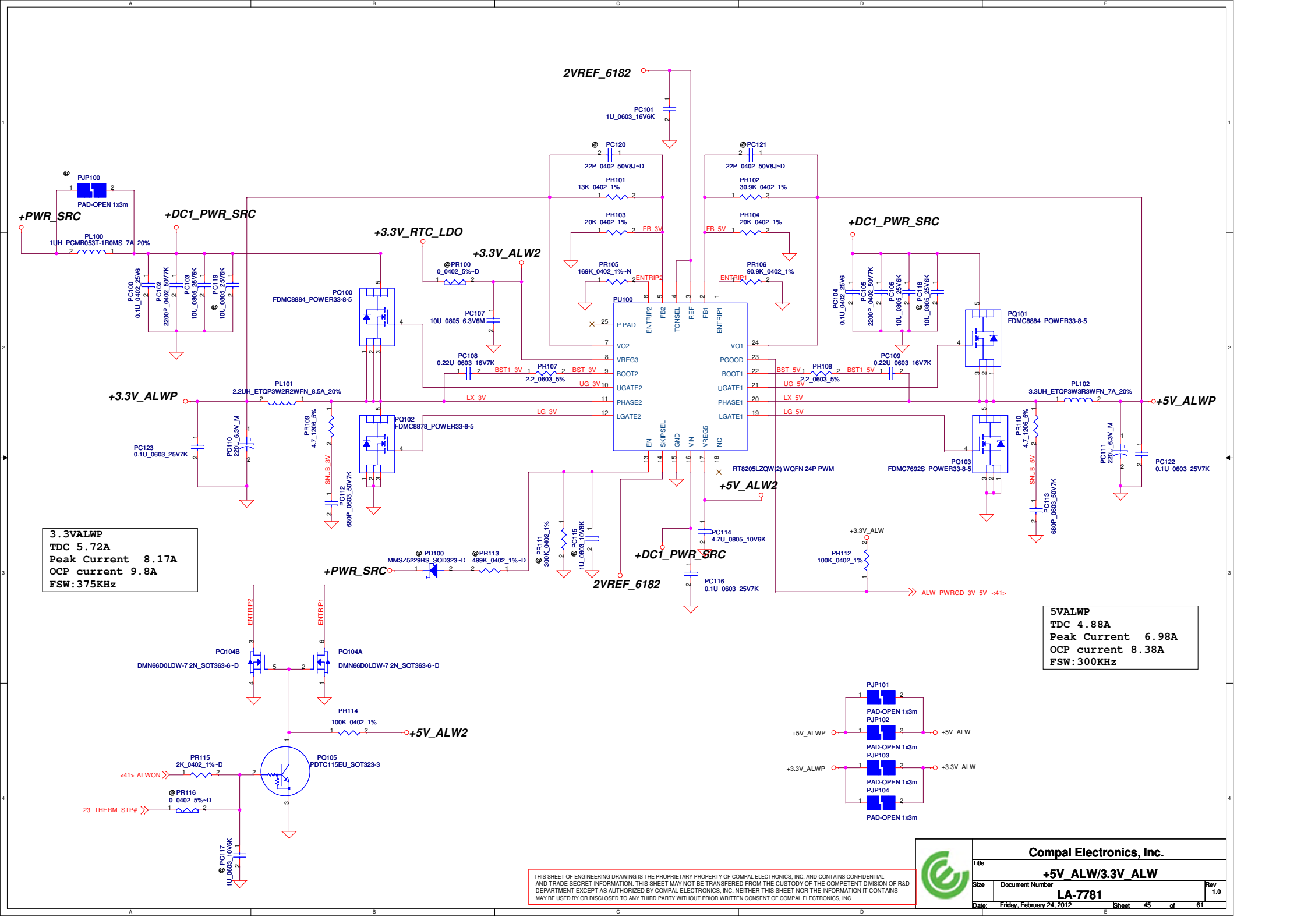
Compal Electronics, Inc.

Title: PAD and Standoff

Size: | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 43 of 61





Compal Electronics, Inc.

Title: +5V_ALW/3.3V_ALW

Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 45 of 61

1.5Volt +/- 5%
TDC 7.17A
Peak Current 10.25A
OCP current 12.3A

0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A

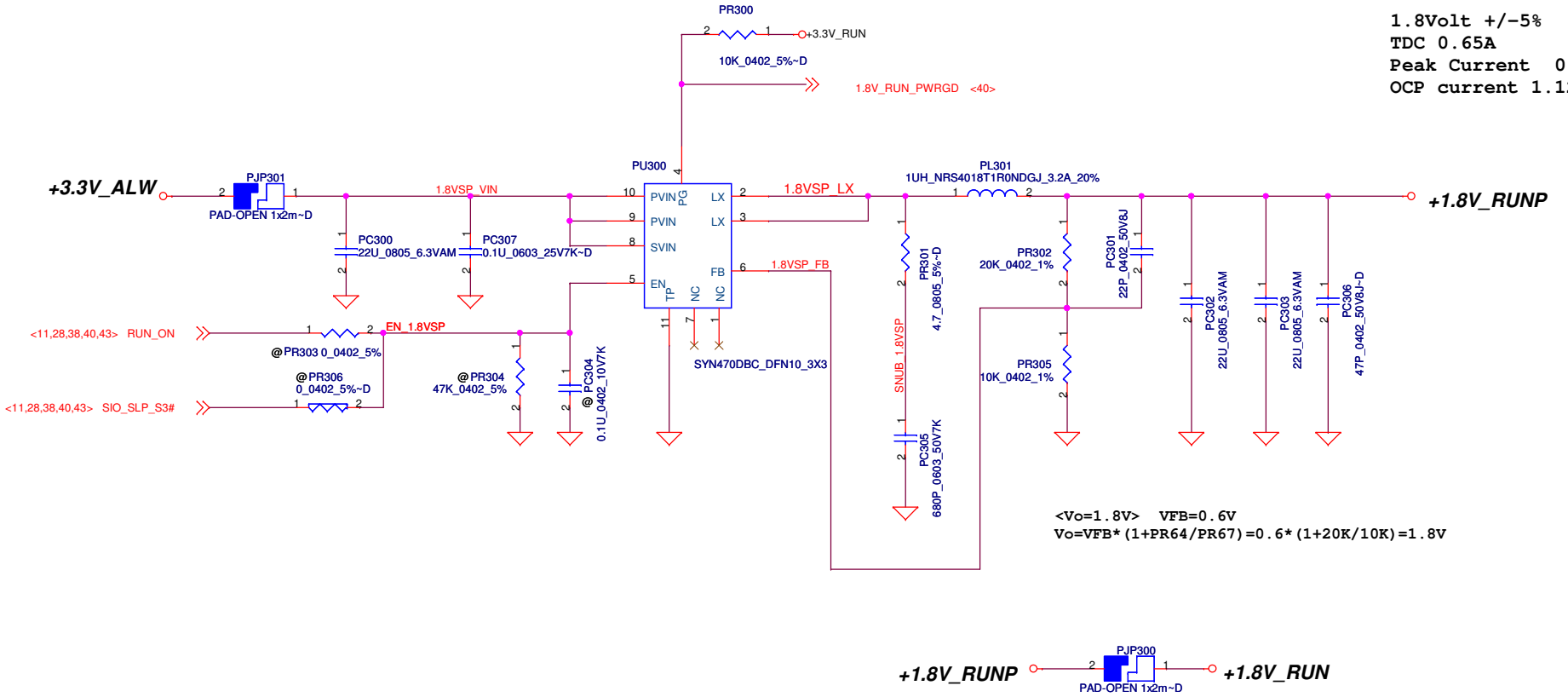
+PWR_SRC
PJP200
PAD-OPEN 1x2m~D
1.5V_B+
PC200 4.7U_0805_25V6K~D
PC201 4.7U_0805_25V6K~D
PC202 0.1U_0402_25V6K~D
PC203 2200P_0402_50V7K~D
PC204 0.22U_0603_16V7K~D
PR200 2.2_0603_5%~D
BOOT_1.5V
DH_1.5V
SW_1.5V
DL_1.5V
PQ200 SIR472DP-T1-GE3_POWERPAK8-5~D
PQ201 SIR466DP-T1-GE3_POWERPAK8-5
+1.5V_MEN_P
PL200 1UH 20% FDUE1040D-H-1R0M=P3_21.3A_20%~D
@PC214 330U_SX_2V~D
PC208 390U_2.5V_M
PC209 680P_0603_50V7K
PR203 4.7_1206_5%
1SNUB_1.5V
+5V_ALW
PR201 5.62K_0402_1%
CS_1.5V
PC207 1U_0603_10V6K~D
PR202 5.1_0603_5%~D
PC210 1U_0603_10V6K~D
VDD_1.5V
+3.3V_ALW
PR204 100K_0402_1%~D
<41> 1.5V_SUS_PWRGD
1.5V_SUS_PWRGD
PR205 1M_0402_1%~D
1.5V_B+
@PR206 0_0402_5%~D
<41> DDR_ON
S5_1.5V
@PR210 0_0402_5%~D
<41> SIO_SLP_S4#
@PC212 0.1U_0402_16V7K~D
PU200 RT8207MZQW_WQFN20_3X3
PHASE UGATE BOOT VLDOIN VTT PAD
LGATE PGND CS VDDP VDD PGOOD TON S5 S3 FB
VTTGND VTTSNS GND VTTREF VDDQ
VLDOIN_1.5V
PJP204
PAD-OPEN1x1m
+1.5V_MEN_P
+0.75V_P
PC205 10U_0805_6.3V6M~D
PC206 10U_0805_6.3V6M~D
+V_DDR_REF
+V_DDR_REF
VDDQ_1.5V
+1.5V_MEN_P
FB sense trace
when FB pull down to GND
PC211 0.033U_0402_16V7~D
@PR207 0_0402_5%~D
1.5V_FB
@PC215 22P_0402_50V8J~D
PR209 0_0402_5%~D
PC213 @0.1U_0402_16V7K~D
@PR208 0_0402_5%~D
<41> 0.75V_DDR_VTT_ON
+1.5V_MEN_P
FB sense trace

Mode	S3	S5	+1.5V_MEN	+V_DDR_REF	+0.75V_P
S5	L	L	off	off	off
S3	L	H	on	on	off(Hi-Z)
S0	H	H	on	on	on

+0.75V_P
PJP203
PAD-OPEN1x1m
+0.75V_DDR_VTT

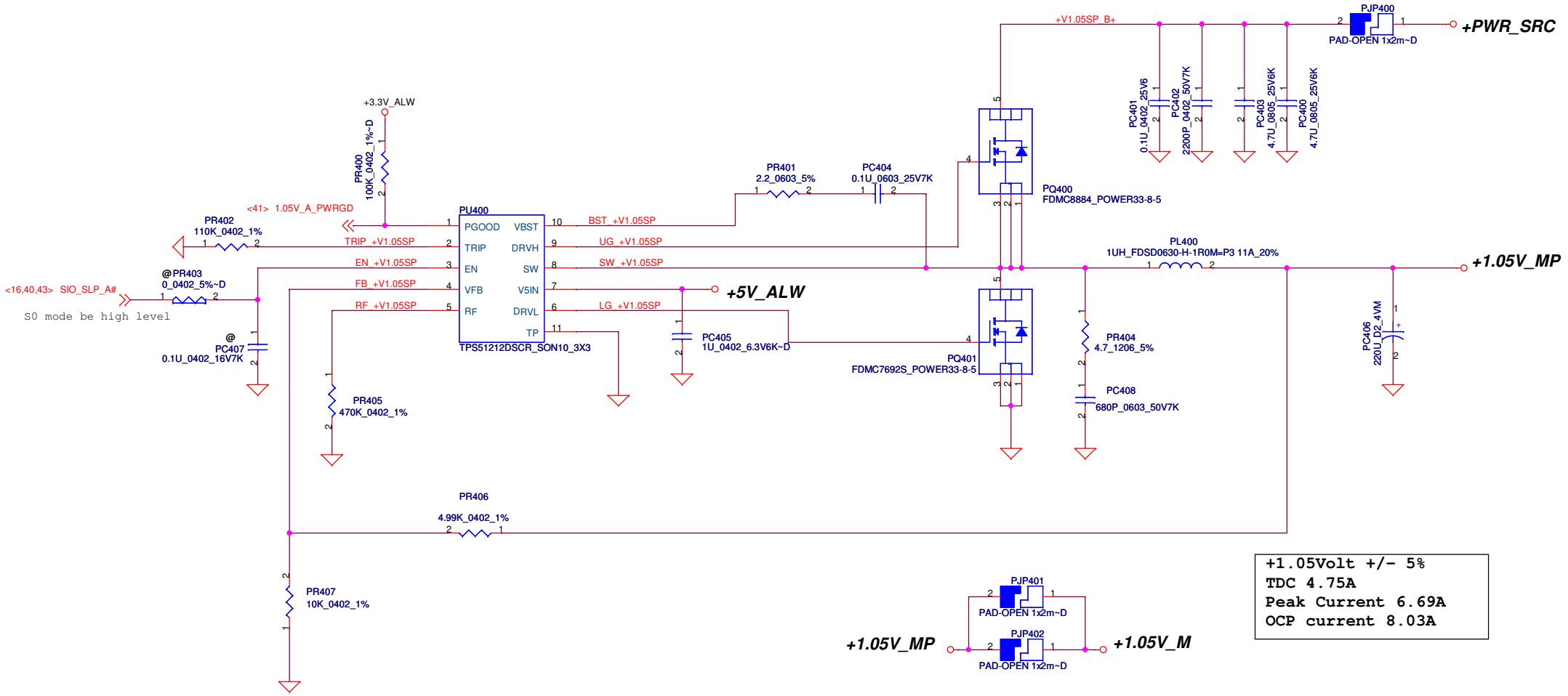
+1.5V_MEN_P
PJP201
JUMP_1x3m
PJP202
JUMP_1x3m
+1.5V_MEM

Compal Electronics, Inc.
Title: +1.5V_MEN/+0.75V_DDR_VTT
Size: | Document Number: LA-7781 | Rev: 1.0
Date: Friday, February 24, 2012 | Sheet 46 of 61



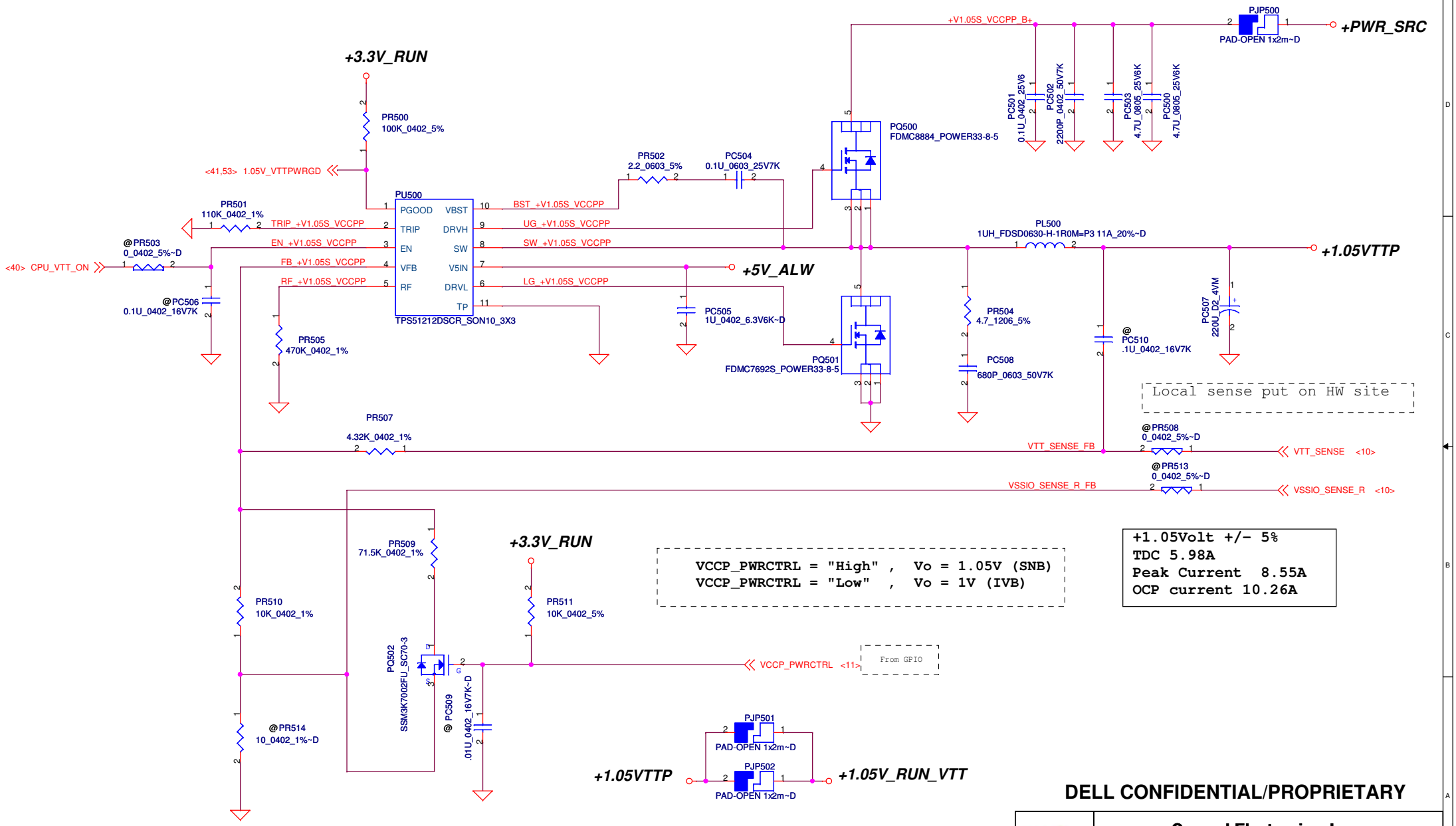
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: +1.8V_RUN		
Size	Document Number: LA-7781	Rev: 1.0
Date: Friday, February 24, 2012	Sheet 47 of 61	



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: +1.05V_M		
Size	Document Number: LA-7781	Rev: 1.0
Date: Friday, February 24, 2012	Sheet 48 of 61	



DELL CONFIDENTIAL/PROPRIETARY

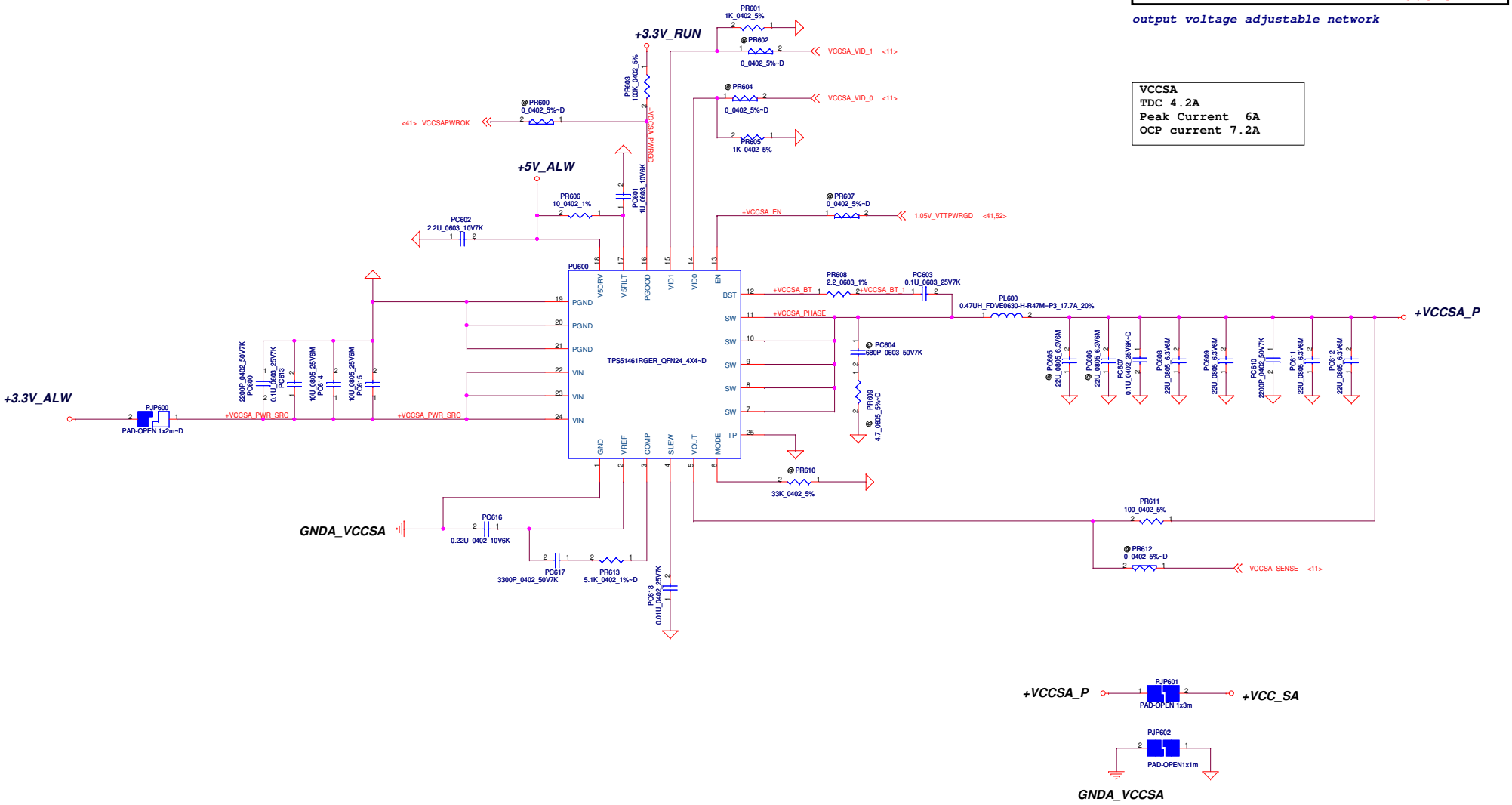
Compal Electronics, Inc.	
Title	+1.05V_RUN_VTT
Size	Document Number: LA-7781
Rev	1.0
Date:	Friday, February 24, 2012
Sheet	49 of 61

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VCCSA
TDC 4.2A
Peak Current 6A
OCP current 7.2A



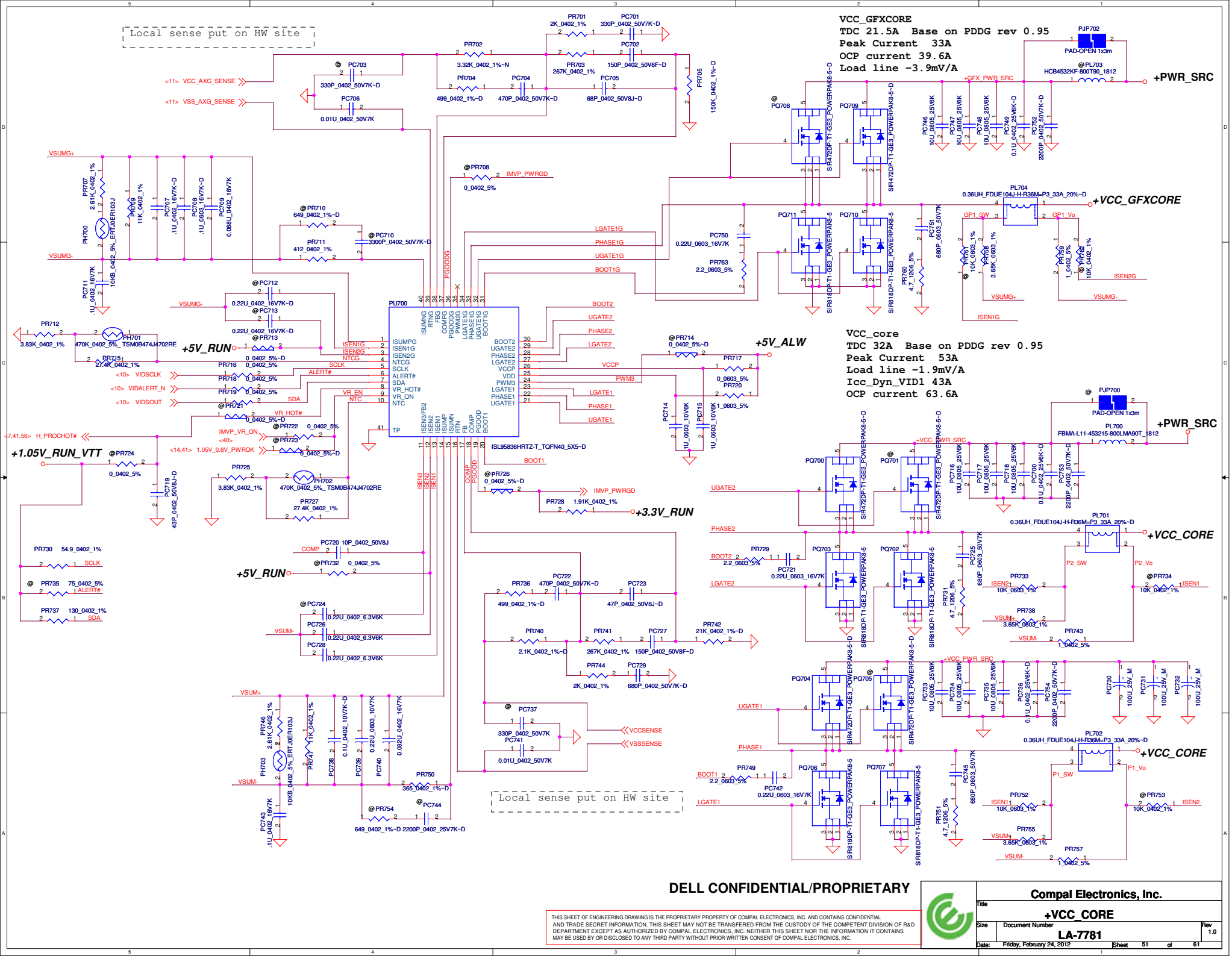
DELL CONFIDENTIAL/PROPRIETARY

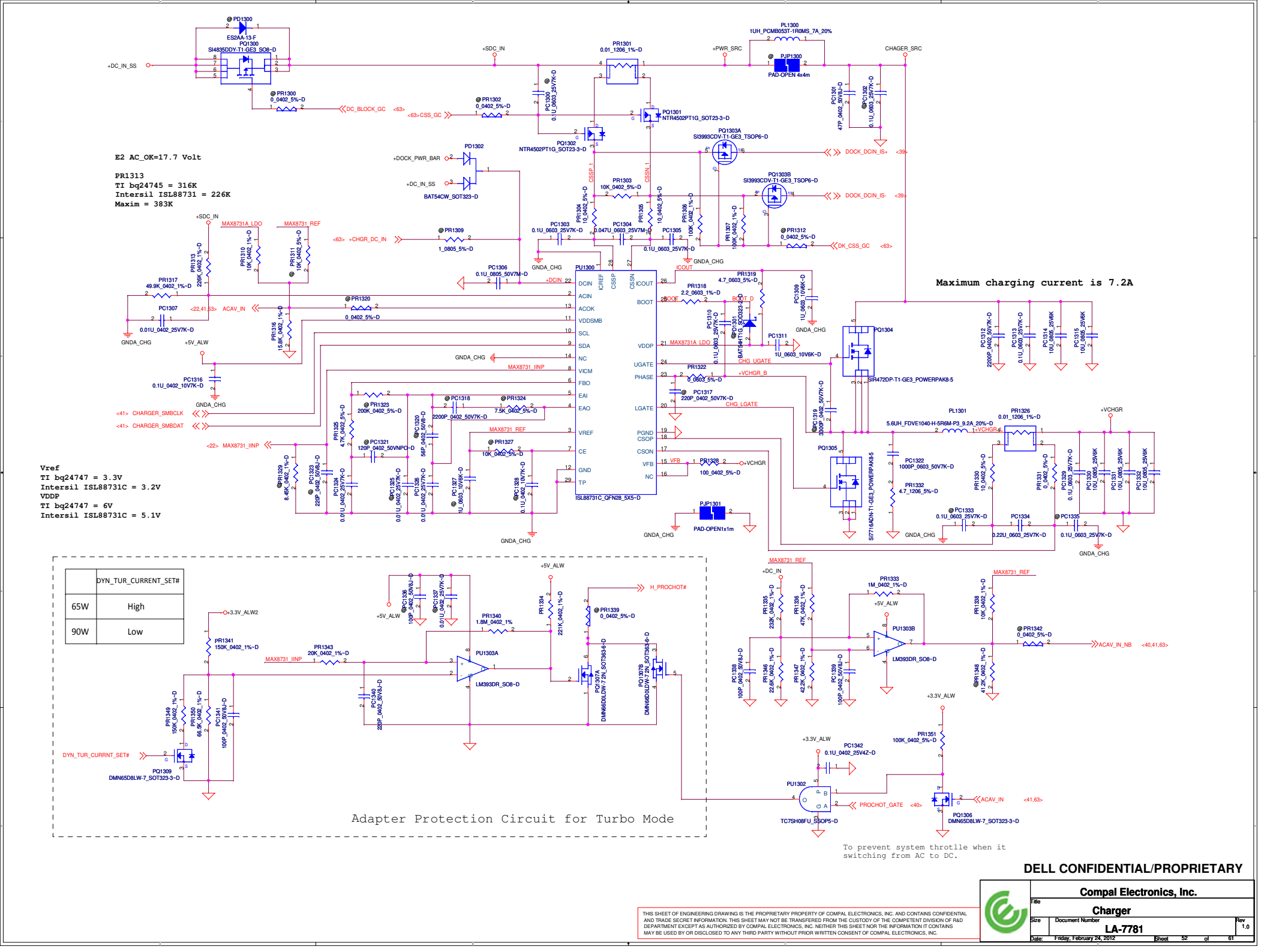
Compal Electronics, Inc.

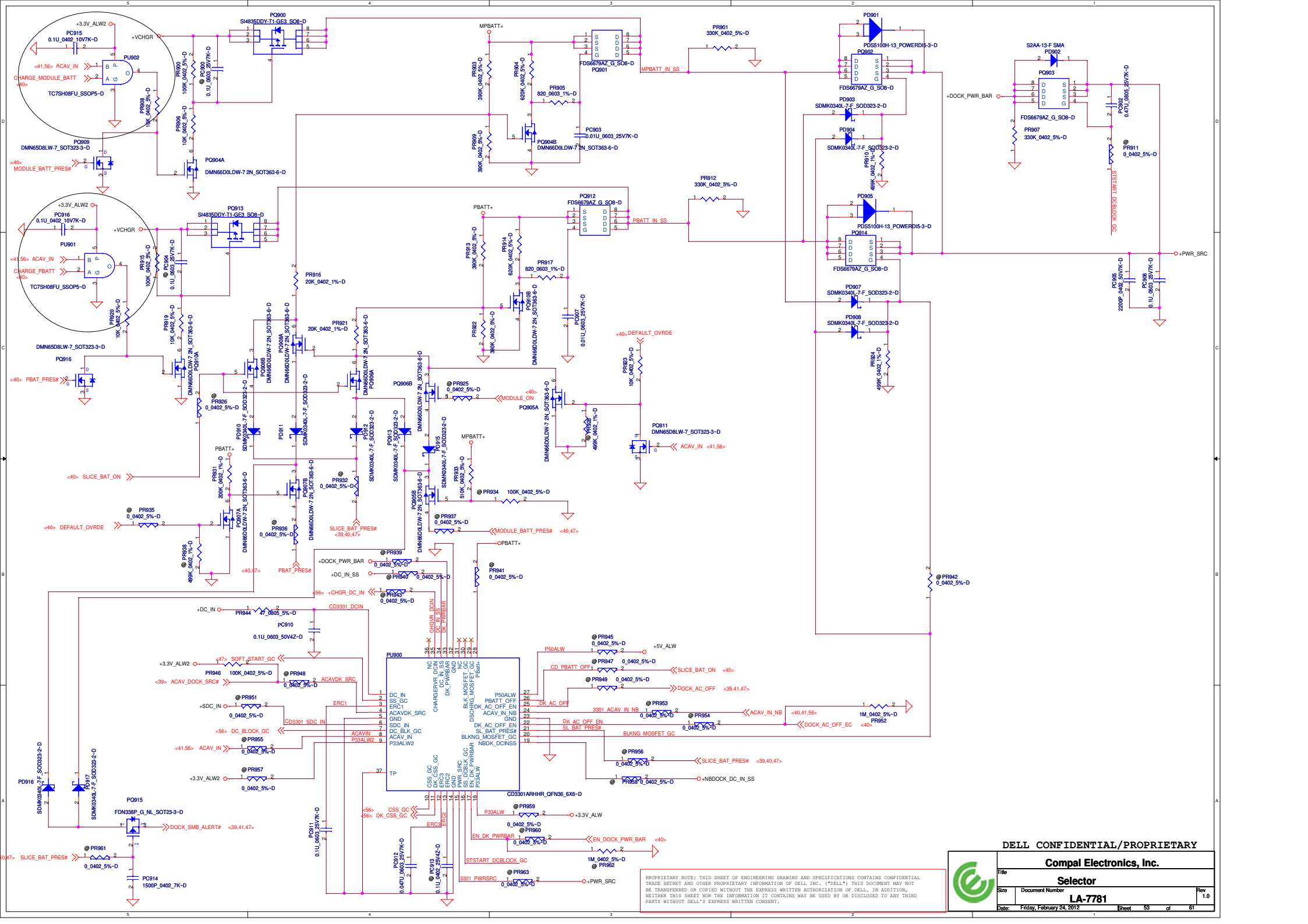
Title: +VCC_SA

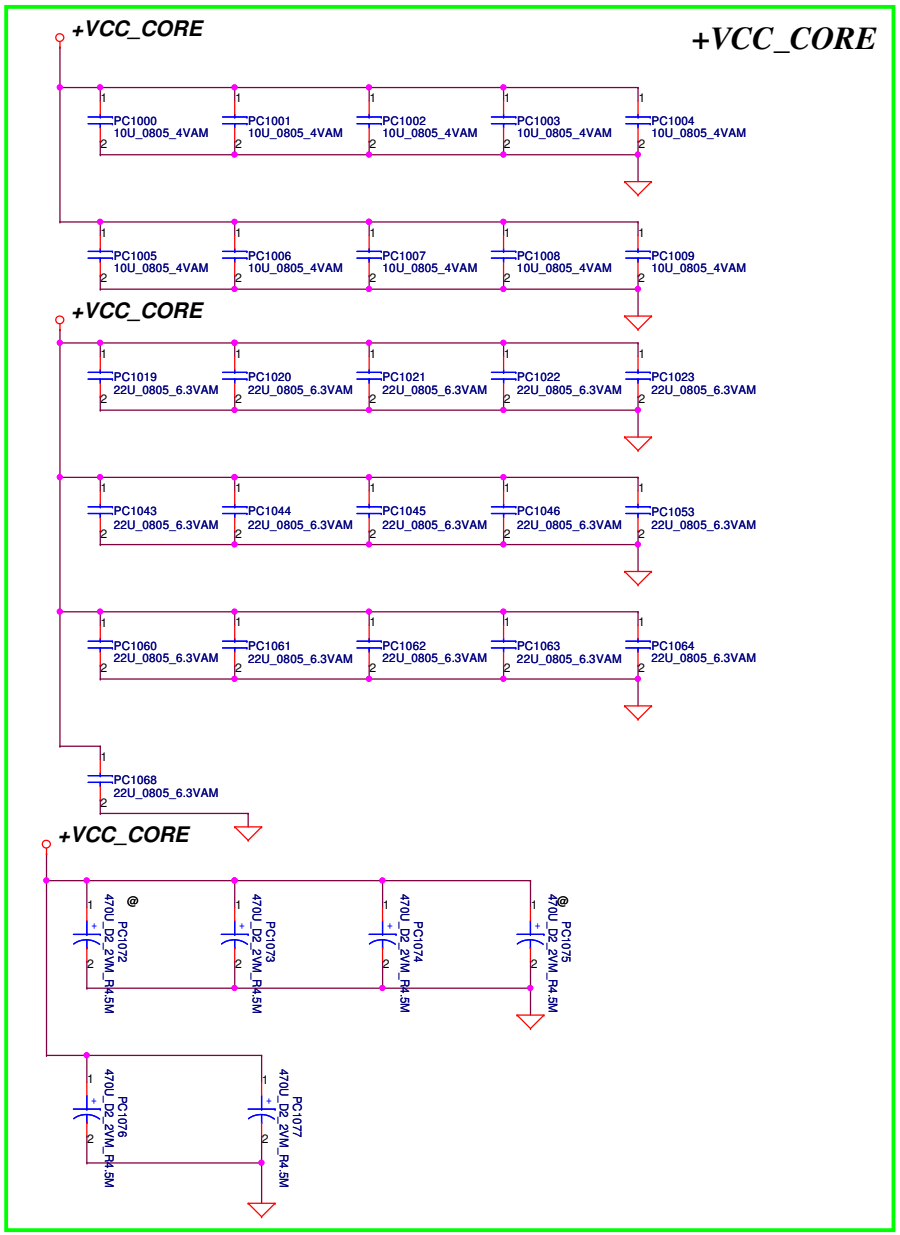
Size | Document Number: LA-7781 | Rev: 1.0

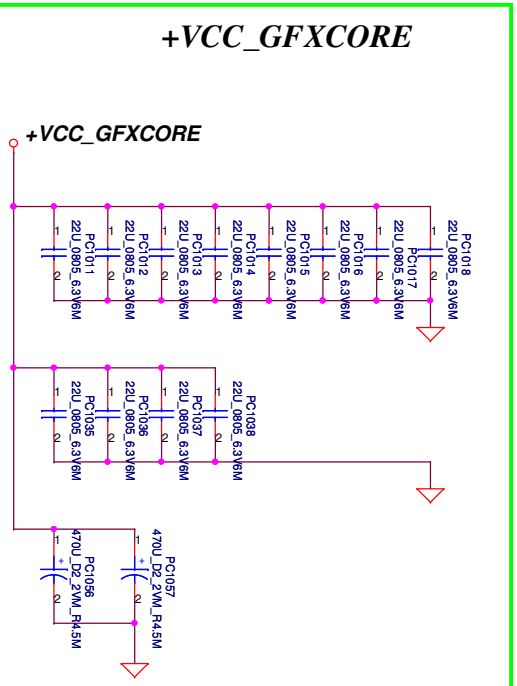
Date: Friday, February 24, 2012 | Sheet 50 of 61


Local sense put on HW site
VCC_GFXCORE
TDC 21.5A Base on PDDG rev 0.95
Peak Current 33A
OCP current 39.6A
Load line -3.9mV/A
+PWR_SRC
+VCC_GFXCORE
+5V_RUN
+5V_ALW
VCC_core
TDC 32A Base on PDDG rev 0.95
Peak Current 53A
Load line -1.9mV/A
Icc_Dyn_VID1 43A
OCP current 63.6A
+1.05V_RUN_VTT
+3.3V_RUN
+VCC_CORE
ISL95836HRTZ-T_TQFN40_5X5~D
Local sense put on HW site
DELL CONFIDENTIAL/PROPRIETARY
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
+VCC_CORE
Size
Document Number
LA-7781
Rev
1.0
Date: Friday, February 24, 2012
Sheet 51 of 61


E2 AC_OK=17.7 Volt
PR1313
TI bq24745 = 316K
Intersil ISL88731 = 226K
Maxim = 383K
Vref
TI bq24747 = 3.3V
Intersil ISL88731C = 3.2V
VDDP
TI bq24747 = 6V
Intersil ISL88731C = 5.1V
Maximum charging current is 7.2A
DYN_TUR_CURRENT_SET#
65W
High
90W
Low
Adapter Protection Circuit for Turbo Mode
To prevent system throtlle when it switching from AC to DC.
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Charger
LA-7781
Friday, February 24, 2012
52
61

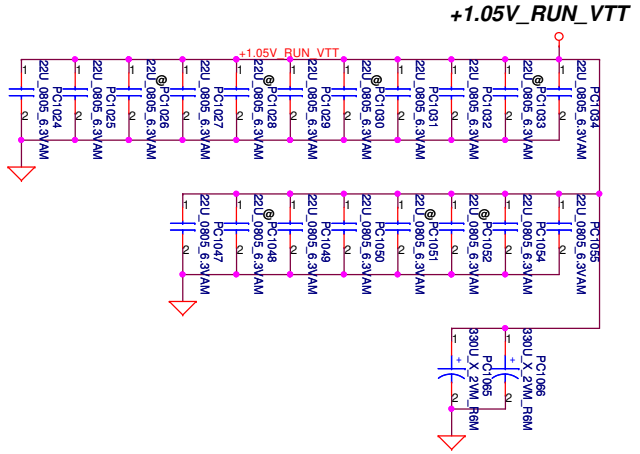

PU900
CD3301ARHHR_QFN36_6X6~D
PU902
TC7SH08FU_SSOP5~D
PU901
PQ900
SI4835DDY-T1-GE3_SO8~D
PQ901
FDS6679AZ_G_SO8~D
PQ902
PQ903
PQ904
PQ905
PQ906
PQ907
PQ908
PQ909
DMN65D8LW-7_SOT323-3~D
PQ910
PQ911
PQ912
PQ913
PQ914
PQ915
FDN338P_G_NL_SOT23-3~D
PQ916
PQ917
PD900
PDS5100H-13_POWERDI5-3~D
PD901
PD902
S2AA-13-F SMA
PD903
SDMK0340L-7-F_SOD323-2~D
PD904
PD905
PD906
PD907
PD908
PD909
PD910
PD911
PD912
PD913
PD914
PD915
PD916
PD917
MPBATT+
PBATT+
+3.3V_ALW2
+VCHGR
+PWR_SRC
+5V_ALW
+NBDOCK_DC_IN_SS
MPBATT_IN_SS
PBATT_IN_SS
+DOCK_PWR_BAR
+DC_IN_SS
+DC_IN
ACAV_IN
CHARGE_MODULE_BATT
MODULE_BATT_PRES#
PBAT_PRES#
CHARGE_PBATT
DEFAULT_OVRDE
SLICE_BAT_ON
SLICE_BAT_PRES#
MODULE_BATT_PRES#
MODULE_ON
DOCK_AC_OFF
DOCK_AC_OFF_EC
ACAV_IN_NB
EN_DOCK_PWR_BAR
DOCK_SMB_ALERT#
STSTART_DCBLOCK_GC
SOFT_START_GC
DC_BLOCK_GC
CSS_GC
DK_CSS_GC
CHGVR_DCIN
DC_IN_SS
DK_PWRBAR
P50ALW
P33ALW
CD_PBATT_OFF
DK_AC_OFF
DK_AC_OFF_EN
SL_BAT_PRES#
BLKNG_MOSFET_GC
3301_ACAV_IN_NB
3301_PWRSRC
EN_DK_PWRBAR
ACAVDK_SRC
ACAVDK_SRC#
CD3301_DCIN
CD3301_SDC_IN
+SDC_IN
ERC1
ERC2
ERC3
PR900
PR901
PR902
PR903
PR904
PR905
PR906
PR907
PR908
PR909
PR910
PR911
PR912
PR913
PR914
PR915
PR916
PR917
PR918
PR919
PR920
PR921
PR922
PR923
PR924
PR925
PR926
PR927
PR928
PR929
PR930
PR931
PR932
PR933
PR934
PR935
PR936
PR937
PR938
PR939
PR940
PR941
PR942
PR943
PR944
PR945
PR946
PR947
PR948
PR949
PR950
PR951
PR952
PR953
PR954
PR955
PR956
PR957
PR958
PR959
PR960
PR961
PR962
PR963
PC900
PC901
PC902
PC903
PC904
PC905
PC906
PC907
PC908
PC909
PC910
PC911
PC912
PC913
PC914
PC915
PC916
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Selector
LA-7781
Rev 1.0
Friday, February 24, 2012
Sheet 53 of 61
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.





Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



For sandy bridge depop PC1267
For ivy bridge pop PC1267

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size | Document Number: LA-7781 | Rev: 1.0

Date: Friday, February 24, 2012 | Sheet 54 of 61

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	46	+1.5V_MEN	7/5	Dell	Follow VC , enable use SIO_SLP_S4#.	Add PR210 for net "SIO_SLP_S4#"	X01
2	44	DCIN	8/4	Dell	ME design change.	PJPDC1 change from 7pin to 5pin	X01
3	45	+5V/3.3V	8/4	Compal	Main and 2nd IC common setting.	De-pop PD100,PR113,PR111	X01
4	51	Vcore/GFX core	8/4	Compal JimmyCC_Kuo	Suppress WWAN BB noise.	Pop PC751,PR760,PC725,PR731, PC745,PR751(680pF 0603, 4.7 ohm 1206)	X01
5	45	+5V/3.3V	8/4	Compal	DFX concern, choke change from 10*10 to 7*7	PL101 change from 3.3u 10*10 to 2.2u 7*7 PL102 change from 3.3u 10*10 to 3.3u 7*7	X01
6	45 46	+5V/3.3V +1.5V_MEN	8/4	Compal	COS concern, change from D2 Polymer cap to OScon cap	PC110,PC111 change from 220u polymer cap to 220u OScon cap PC208 change from 330u polymer cap to 390u OScon cap	X01
7	45 46	+5V/3.3V +1.5V_MEN	8/4	Compal	Prevent Jitter issue.	Add PC120,PC121,PC215 parallel with PR101,PR102,PR207	X01
8	51	Vcore/GFX core	8/4	Compal	Prevent output voltage glitch when power up.	PU700 VCCP and VDD change form +5V_RUN to +5V_ALW	X01
9	51,52 45	Vcore, Charger +5V/3.3V	8/8	Compal Justin_Hsu	EMI solution.	Pop PL700.PL1300,PL100	X01
10	45 46	+5V/3.3V +1.5V_MEN	8/8	Compal JimmyCC_Kuo	Suppress WWAN BB noise.	Pop PR109,PC112,PR110,PC113,PC209,PR203 (680pF 0603, 4.7 ohm 1206)	X01
11	47,48 49	+1.8V/+1.05VM +1.05V_VTT	8/8	Compal JimmyCC_Kuo	Suppress WWAN BB noise.	Pop PR301(0805),PC305,PR404,PC408,PR504, PC508(680pF 0603, 4.7 ohm 1206)	X01
12	45	+5V/3.3V	8/10	Compal JimmyCC_Kuo	Suppress WWAN BB noise.	Add PC122,PC123 on +5V_ALWP and +3.3V_ALWP	X01
13	45-53		11/16	Compal	For cost saving, change the 0ohm resistors to layout short PAD.	Footprint change PR100,PR116,PR208,PR210, PR306,PR403,PR503,PR508,PR513,PR600,PR607, PR612,PR602,PR604,PR714,PR726,PR713,PR721, PR723,PR1300,PR1302,PR1312,PR1320,PR1339, PR1342,PR911,PR925,PR937,PR941,PR932,PR936, PR926,PR935,PR945,PR947,PR949,PR939,PR940, PR943,PR948,PR951,PR955,PR957,PR961,PR953, PR954,PR956,PR958,PR959,PR960,PR963	X02
14	44	DCIN	11/30	Compal	Reduce power consumption in S5.	Add PCH_ALW_ON for +PWR_SRC_S enable signal.	X02

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	51	VCORE/GFXcore	12/09	Compal	Fine tune load line,OCP,transient response.	PR740 change from 2K to 2.1K ohm. PC740 change from 0.033uF to 0.082uF. PR750 change from 348 to 365 ohm. PC707 change from 0.022uF to 0.1uF. PR711 change from 357 to 412 ohm. PR702 change from 2.55k to 3.32K ohm.	X02

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	42	HW	07/11/2011	COMPAL	E4 uses SIO_SLP_S4# for power control	DDR_ON and SUS_ON are replaced by SIO_SLP_S4#	X01
2	14,39	HW	07/11/2011	COMPAL	SMSC request to delete LPC_LDRQ0#	Leave LDRQ0# no connection on both of 5048 and PCH side	X01
3	11	HW	07/11/2011	COMPAL	Follow INTEL DG	Change RC99, RC100 from SD034100A8L (S RES 1/16W 10 +-1% 0402) to SD03410008L (S RES 1/16W 100 +-1% 0402)	X01
4	24	HW	07/11/2011	COMPAL	ATG needs touch screen circuit	Add "5@" for touch screen circuit of Dalmore 14" ATG	X01
5	22	HW	07/11/2011	COMPAL	UMA uses EMC4021 for cost concern	Change thermal sensor to EMC4021 for UMA	X01
6	42	HW	07/14/2011	COMPAL	Load SW sources output rising time mismatch and COS. cost concern	Change back to E3 +3.3V/5V_RUN discrete solution	X01
7	20	HW	07/14/2011	COMPAL	CH94 and CH95 to D2 size for cost concern	Change CH94 and CH95 from SGA0000170L to SGA00004L0L	X01
8	29	HW	07/19/2011	COMPAL	Codec is change to 92HD93	Pop R162~R166 and de-pop U73	X01
9	20,42	HW	07/21/2011	COMPAL	Vgs less than cut-in voltage in battery mode	Add control circuit for +5V_ALW_PCH	X01
10	27,28,42	HW	07/25/2011	COMPAL	Vgs of 5V MOS maybe large than max rating	Add R516, R517. Change Q55 from SB00000KQ0L to SB00000GV00	X01
11	11	HW	07/25/2011	COMPAL	Follow INTEL PDDG 0.8	De-pop RC140	X01
12	32	HW	07/25/2011	COMPAL	RESET_OUT# power sequence issue	Add R1640, 1M ohms pull down for USH_PWR_STATE# at M/B side	X01
13	15	HW	07/25/2011	COMPAL	Follow crystal measurement report	Change CH18 and CH19 to 8.2pF	X01
14	40	HW	07/27/2011	COMPAL	Change board ID to X01	Change R875 to 130Kohms	X01
15	34	HW	07/27/2011	COMPAL	PCH GPIO52 need 8.2~10K pull up +3.3VS	Change R695 from 100K to 10Kohms	X01
16	23	HW	07/28/2011	COMPAL	CRT SW 2nd source TI, TS3V713 pin29 is VDD	Connect pin29 to +3.3V_RUN	X01
17	16	HW	07/28/2011	COMPAL	+1.05V_M turn off before APWROK de-assert	Add UH5 circuit for HW solution	X01
~~18~~	~~29~~	~~HW~~	~~08/01/2011~~	~~COMPAL~~	~~Co-lay 92HD93 with ALC290~~	~~Pop option for 92HD93/ALC290=>R1646/C1164; R1644/R1643; C965/R1642; Q107/R171 Reserve for ALC290 only: C1204, C1205, R1647, C1165, R1648 Reserve for 92HD93 only: R1645, C963~~	~~X01~~
19	41	HW	08/02/2011	COMPAL	Reset IC threshold voltage issue	Change U4 to RT9801A (threshold adjustable)	X01
20	29	HW	08/02/2011	COMPAL	EMI request to add solution for BITCLK	Pop R1076 (33ohms) and C977 (10pF) for PCH_AZ_CODEC_BITCLK	X01
21	26	HW	08/03/2011	COMPAL	DPX_CA_DET voltage too low through dongle	Change U21 and U24 to SA000055G0L	X01
22	17	HW	08/03/2011	COMPAL	Request from INTEL review feedback	Pop RH332 for PCH_GPIO3	X01

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
23	42,43	HW	08/04/2011	COMPAL	For cost saving	Change Q61 to SB00000GV00; HDD and breath LED control share Q84; Power team request Q59 change to SB00000L80L	X01
24	24, 29, 33	HW	08/08/2011	COMPAL	EMI request to add solution	Pop RE678 (22ohms), CE757 (33pF) and C981~3 (0.1uF). Add CE758 (33pF). Reserve C1206 and C1207.	X01
25	41	HW	08/08/2011	COMPAL	For RSMRST# debug	Reserve R1655 and pop R1623	X01
26	39	HW	08/08/2011	COMPAL	RF request to add solution	Pop R795 (33ohms), C713 (32pF), RE5 (33ohms), CE3 (32pF), R885 (10ohms) and C747 (8.2pF)	X01
27	43	HW	08/08/2011	COMPAL	White light LED brightness is abnormal	Change R934, R938, R939, R949, R958, R957 and R955 to 2.2 Kohms	X01
28	40	HW	08/09/2011	COMPAL	ESD request add 0.1uF on ALWON	Reserve C1208 for ESD backup plan	X01
29	17	HW	08/10/2011	COMPAL	RF request 10pF on MEC and 5048 PCI CLK	Reserve 10pF bypass cap. at CH109 and CH110	X01
30	18	HW	08/11/2011	COMPAL	Delete TCM and Non-TPM configuration	De-pop RH270 and RH271. Always pop RH267 and RH268	X01
31	11	HW	08/12/2011	COMPAL	S3 can't resume issue	Control 1.5V_VDDQ by EC. Pop RC79 and de-pop RC82	X01
32	40	HW	08/15/2011	COMPAL	Change board ID to X02	Change R875 to 62Kohms	X02
~~33~~	~~14~21~~	~~HW~~	~~08/15/2011~~	~~COMPAL~~	~~Change PCH to B0 version~~	~~Change UH4 to SA00004NQ2L~~	~~X02~~
34	42	HW	08/18/2011	COMPAL	Rated Vgs of Q61 is 25V	De-pop R1627	X02
35	36	HW	08/19/2011	COMPAL	Follow INTEL DG	Change C410~C413 from 0.01uF to 0.1uF	X02
36	19	HW	08/19/2011	COMPAL	CRT ripple garbage display issue	Change LH1 from 180ohms bead to 1uH inductor	X02
37	29	HW	08/29/2011	COMPAL	IDT request and codec version change	Change C1163 from 1uF to 2.2uF and codec from WA to WB version	X02
~~38~~	~~43~~	~~HW~~	~~08/29/2011~~	~~COMPAL~~	~~To meet current limit resistor of LED spec~~	~~Change R949, R958, R957, R955, R939, R938, R934 from 2.2K to 1.2Kohms~~	~~X02~~
~~39~~	~~42~~	~~HW~~	~~09/02/2011~~	~~COMPAL~~	~~DMN3030LSS-13 poor soldering issue~~	~~Change Q55 and Q61 to AO4478L~~	~~X02~~
40	39	HW	09/02/2011	COMPAL	SMSC change 5048 pin A23 to GPIOI0	Re-link ECE 5048 symbol	X02
~~41~~	~~25~~	~~HW~~	~~09/14/2011~~	~~COMPAL~~	~~HDMI EMI low cost solution~~	~~De-pop L19~L22. Add L100~107 (9nH) and C1209~C1216 (3.3pF)~~	~~X02~~
42	40	HW	09/14/2011	COMPAL	SMSC review feedback	Add R1656 and R1657 100Kohms to GND for I2S disabled	X02
43	29	HW	09/16/2011	COMPAL	Remove ALC290 co-lay circuit	Remove R1648, R1647, R1646, R1645, C1165, C1164, R1643, R1644, R1642, R171, C1204, C1205	X02
44	29	HW	09/16/2011	COMPAL	15" UMA speaker no sound issue	Add snubber on speaker trace with C: 2200pF and R: 3.3ohms. Change bead rated current from 200mA to 2A.	X02
45	33	HW	09/26/2011	COMPAL	EMI request to change SD CLK series R	R676 is changed from 33ohms to 10ohms	X02
~~46~~	~~42~~	~~HW~~	~~09/26/2011~~	~~COMPAL~~	~~1V leakage on +3.3V_RUN during system boot~~	~~Pop Q69 and R929 discharge circuit~~	~~X02~~
47	40	HW	09/26/2011	COMPAL	EC has internal pull up for volume signals	De-pop R1169, R1197 and R1118	X02

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
~~48~~	~~42~~	~~HW~~	~~09/28/2011~~	~~COMPAL~~	~~INTEL timing spec, V2 fail~~	~~Change C763 to 470pF as that of +3.3V_RUN~~	~~X02~~
49	41	HW	10/05/2011	COMPAL	Chane reset IC to RT9818A-44GU3	Update U4 symbol and add R1629 for backup of inrush prevention. Change RSMRST# pull up with 100Koms. Pop R1655 and de-pop R1623.	X02
50	39	HW	10/05/2011	COMPAL	When suspend/resume cycles, wireless SW GPIO IRQs keeps giving	Add R771 pulling up to +3.3V_ALW for WIRELESS_ON#/OFF and de-pop R766	X02
51	19	HW	10/11/2011	COMPAL	CRT ripple garbage display issue	Change CH36 from 10uF to 22uF	X02
52	7~42	HW	10/11/2011	COMPAL	For cost saving	Change 0 ohm resistor to short pad	X02
53	29	HW	10/11/2011	COMPAL	Change C973~C976 P/N and R1658~R1661 size	Change C973~C976 P/N to SE074222K8L. Change R1658~R1661 size to 0402.	X02
~~54~~	~~42~~	~~HW~~	~~10/18/2011~~	~~COMPAL~~	~~+3.3V_SUS sequence timing probelm~~	~~Change C767 to 470pF, the same as that of +3.3V_RUN~~	~~X02~~
55	22	HW	10/18/2011	COMPAL	Thermal requests to change OTP from 88 to 93	Change R406 from 953ohms to 1.24Kohms	X02
~~56~~	~~43~~	~~HW~~	~~10/20/2011~~	~~COMPAL~~	~~BREATH LED flash issue when AC plugin~~	~~Add Q126 to control BREATH LED~~	~~X02~~
57	32	HW	10/24/2011	COMPAL	TPM is changed to AT97SC3204-X2A18-AB	U39(TPM) is changed to SA00004WQ10(AT97SC3204-X2A18-AB) for WIN8 support	X02
58	42	HW	10/25/2011	COMPAL	+3.3/5V_RUN inrush curren issue with 470pF	Change C763 and C766 form 470pF to 2200pF	X02
59	33	HW	10/25/2011	COMPAL	EMI change to reserve solution for SD/MMCCLK	De-pop RE678 and CE757	X02
60	34	HW	11/04/2011	COMPAL	PCH GPIO52 changed to be free	De-pop R725, remove R695 and add RH359	X02
61	17,39,40	HW	11/07/2011	COMPAL	RF final solution for PCI clock noise	De-pop R795, C713, R885 and C747. Pop CH109 and CH110 with 12pF	X02
62	43	HW	11/07/2011	COMPAL	Change current limit resistors of LED	R949 from 2.2K to 1K, R939 from 2.2K to 1.8K, R957 from 2.2K to 220, R951 from 475 to 330, R953 from 475 to 330 and R958 from 2.2K to 620	X02
~~67~~	~~14~21~~	~~HW~~	~~11/07/2011~~	~~COMPAL~~	~~Change PCH to C0 version~~	~~Change UH4 to SA00005BU0L~~	~~X02~~
68	11,42	HW	11/07/2011	COMPAL	AO4728L leakage issue	Change QC3 and Q59 to AO4304L (SB00000RV00)	X02
69	32	HW	11/07/2011	COMPAL	+3.3V_RUN Giltch when AC plugin	Add R1662 0ohm resistor. Reserve D87 and R1663 (pull high to +3.3V_RUN_TPM) for HW solution backup.	X02
70		HW	11/07/2011	COMPAL	Change 1Kohms tolerance for cost saving	Change 1Kohms +-1% to +-5% except RC78, RC80, RC81 and RC84	X02
71	38	HW	11/11/2011	COMPAL	EMI request to add 33ohms for DP port	Add RE7~RE24 for DP portD and portC	X02
72		HW	11/16/2011	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing	RC72 from 100K to 330K; RC143 from 330K to 1M; CC136 from 0.1u to 0.022u R412 from 100K to 470K; R1632 from 1M to 4.7M; C293 from 0.1u to 0.022u R507 from 100K to 470K; R517 from 1M to 4.7M; C400 from 0.1u to 0.022u R722 from 100K to 470K; R1625 from 1M to 4.7M; C644 from 4700p to 220p R729 from 100K to 470K; R1628 from 1M to 4.7M; C650 from 4700p to 220p R917 from 100K to 470K; R1617 from 1M to 4.7M; C770 from 4700p to 220p R920 from 100K to 470K; R1610 from 470K to 2.2M; C771 from 4700p to 470p R930 from 100K to 470K; R1611 from 470K to 2.2M; C773 from 2200p to 100p R906 from 100K to 470K; C763 from 2200p to 220p R912 from 100K to 470K; C766 from 470p to 220p	X02

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
73	36	HW	11/21/2011	COMPAL	ESD team modify USB3.0 ESD diode package	Change D78 and D79 to NXP IP4292CZ10-TBR(SC300002F0L, Package: XSON10)	X02
74	42	HW	11/21/2011	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing	R930 from 470K to 330K; R1611 form 2.2M to 1M	X02
75	36	HW	11/23/2011	COMPAL	Add USB PWR SW circuit with G547 for JUSB2	Add single channel USB PWR SW U5, G547. Add decoupling cap. C677 and C678 for SW IC input. Add decoupling cap. C652 and C655 at conn. side.	X02
~~76~~	~~38~~	~~HW~~	~~11/29/2011~~	~~COMPAL~~	~~EMI solution for E-Docking USB (port8)~~	~~Add bypass resistors, R1672 and R1673; choke L99 for backup~~	~~X02~~
77	35	HW	11/30/2011	COMPAL	From ESD team request	Pop C1208 for UMA trace, ALWON Add CE10~CE12 for EXP PWR SW signals, CPUSB#, EXPRCRD_CPPE# and CARD_RESET# Add 0ohm resistors, RE27~RE32 and RE34~RE36 to block ESD from XDP	X02
78	17,34,38	HW	12/02/2011	COMPAL	EMI solution for E-Docking USB port	Swap USB Port6 and Port8; reserve a 90ohms choke at E-Docking conn.: Port6 from Mini3 Pink Panther card to E-docking Port8 from E-Docking to Mini3 Pink Panther card	X02
79	14~21	HW	12/05/2011	COMPAL	Change PCH to C1 version (QS)	Change UH4 to SA00005BU1L	X02
80	24	HW	12/06/2011	COMPAL	EMI solution for USB port12 of camera	Pop 90ohms choke, L10; De-pop R427 and R428	X02
81	42	HW	12/07/2011	COMPAL	+3.3V_SUS sequence timing	R911 from 100K to 470K; R1618 from 1M to 4.7M; C767 from 470p to 220p	X02
82	43	HW	12/07/2011	COMPAL	Add EMI solution	Add C1217 with 0.1uF	X02
83	25	HW	12/08/2011	COMPAL	EMI final solution for HDMI port	Pop L100~L107 with 9nH. Change C1209~C1216 from 3.3pF to 1.8pF. Change R450, R452~R456 and R458~R459 from 680ohms to 604ohms.	X02
84	41	HW	12/08/2011	COMPAL	To prevent inrush current at reset IC input	Change R1629 from 0ohms to 33ohms resistor	X02
85	25	HW	12/28/2011	COMPAL	SMT request to change F2 footprint	For DFX conern of F2 2nd source, SP040003H0L, change F2 footprint to F_MF-MSMF050-2	X02
86	40	HW	01/13/2012	COMPAL	Change board ID to A00	Change R875 to 33Kohms	A00
87	14	HW	01/13/2012	COMPAL	Add X76@ for ROM part	Add X76@ for U52 and U53	A00
88	40	HW	01/13/2012	COMPAL	Change MEC5055 P/N for MP	Change U51 P/N to SA00003TZ2L	A00
89	38	HW	01/13/2012	COMPAL	System hangs after hot dock (DF531758)	Change R755 from 100Kohms to 10Kohms	A00
90	14~21,32	HW	02/01/2012	COMPAL	Chnage PCH, LAN chip P/N for X-build	UH4 is changed to SA00005BU3L U31 is changed to SA00003SI5L	A00
~~91~~	~~31~~	~~HW~~	~~02/01/2012~~	~~COMPAL~~	~~Change PWR button, SW1 back to E3 solution~~	~~change SW1 back to E3 solution, ALPS SKRBAAE010~~	~~A00~~
92	15,18,32	HW	02/03/2012	COMPAL	Add BOM config for Non-TPM	Add 1@ for TPM and 2@ for Non-TPM config	A00
93	14	HW	02/16/2012	COMPAL	De-pop resistor on PCH JTAG for power saving	De-pop RH288, RH47, RH48 and RH49	A00
94	33	HW	02/20/2012	COMPAL	For SD card reader and KB ESD issue	Add 47nF CE13 close to reset input of SD card reader IC Add 100pF CE14 close to U4.3	A00
95	36	HW	02/24/2012	COMPAL	Samsung cell phone can't support CDP	Change charging mode to SDP only in S0 Add Q126 and change R1614 to 100Kohms (reserve this solution and R1614 10kohms)	A00

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
96	36	HW	02/24/2012	COMPAL	Samsung cell phone can't support CDP	Change U2 to Seligo SA00004VH00	A00
97	41	HW	02/24/2012	COMPAL	Pericom IC fail	Change U4 to Richtek SA00005A60L	A00