

COMPAL CONFIDENTIAL

MODEL NAME : *QAL81*
PCB NO : *LA-7782P (DAA00002J00)*
BOM P/N : *TBD*
GPIO MAP: E4_VC_GPIO_map_rev_0.8

Dalmore 14 DSC

Ivy Bridge + Panther POINT

2011-05-12

REV : 0.1 (X00)

@ : Nopop Component

CONN@ : Connector Component

MB Type	BOM P/N
TPM	1@ 3@
TCM	2@ 4@
TPM DIS/TCM DIS	2@ 3@

Part Number	Description
DAA00002J00	PCB 0LE LA-7782P REV0 M/B DSC

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Title		
Cover Sheet		
Size	Document Number	Rev
	LA-7782	0.1
Date:	Tuesday, May 24, 2011	Sheet 1 of 66

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

need to update Power Status and PM Table

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Right side Top)
	1	JUSB2 (Right side Bottom)
	2	JESA1 (Right side ESATA)
	3	MLK DOCK
	4	WLAN
	5	WWAN
	6	JMINI3(Flash)
	7	USH->BIO
	8	DOCKING
	9	JUSB (Left side)
	10	Express card
	11	Bluetooth
	12	Camera
13	LCD Touch	

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

Layer No.	Name	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
		SolderMask	min 0.4	0.50000
		Add Plating		1.45000
1	Top	Copper foil	0.5oz(0.68)	0.65000
		Prepreg	1080	2.75000
2	GND1	Copper foil	1oz(1.35)	1.35000
		Core	4mil	3.89000
3	IN 1	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506	5.50000
4	GND2	Copper foil	1oz(1.35)	1.35000
		Core	3mil	3.09000
5	IN 2	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506*2	11.50000
6	IN 3	Copper foil	1oz(1.35)	1.35000
		Core	3mil	3.09000
7	VCC	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506	5.50000
8	IN 4	Copper foil	1oz(1.35)	1.35000
		Core	4mil	3.89000
9	GND 3	Copper foil	1oz(1.35)	1.35000
		Prepreg	1080	2.75000
10	Bottom	Copper foil	0.5oz(0.68)	0.65000
		Add Plating		1.45000
		SolderMask	min 0.4	0.50000
	Overall Thickness (1.45mm ± 10%)			57.91000

DSC DP/HDMI Port	Connetion
Port C	Dock DP port 2
Port D	Dock DP port 1
Port E	MB HDMI Conn

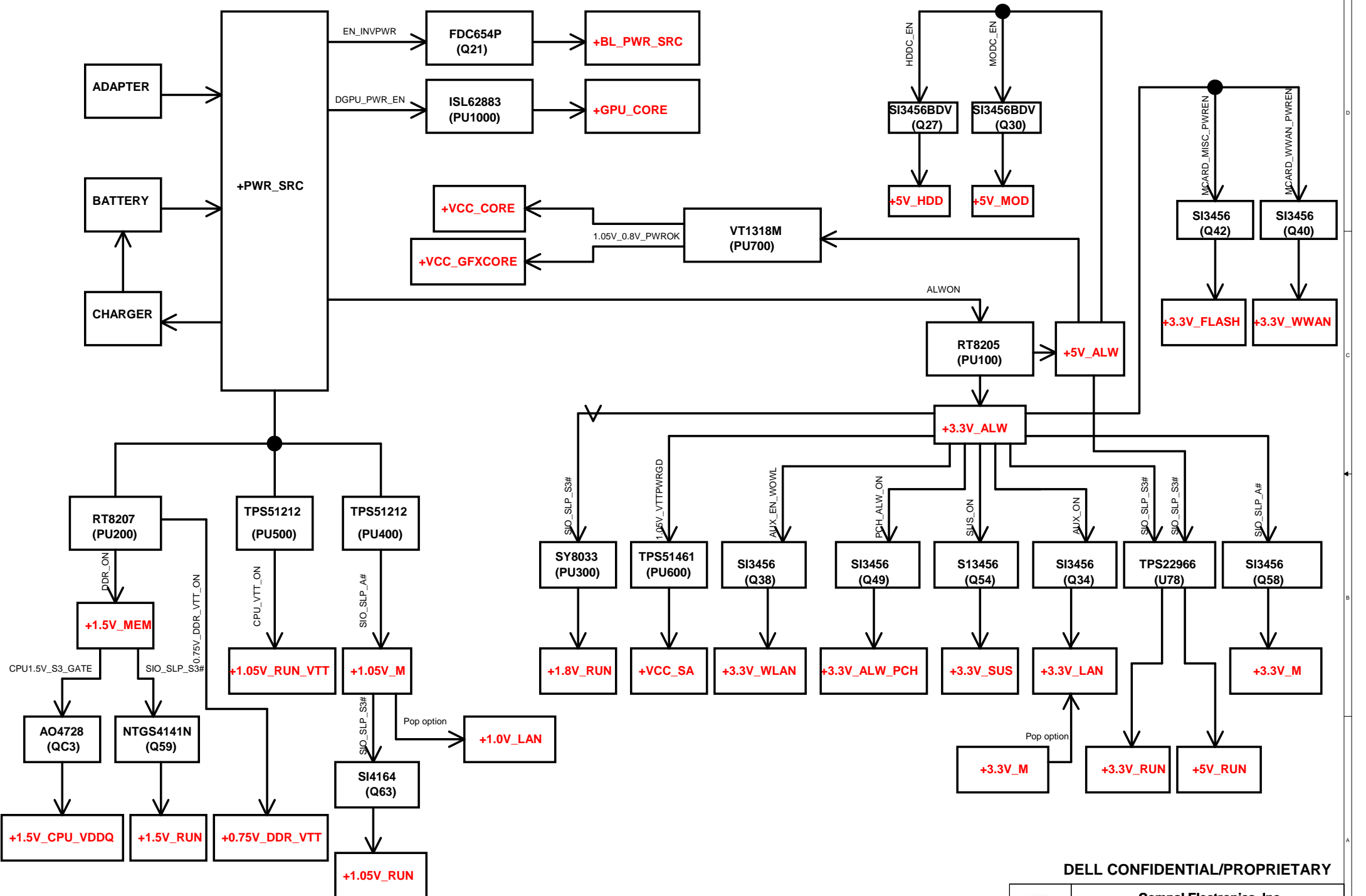
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Index and Config.			Rev
Title	LA-7782		0.1
Size	Document Number		
Date	Friday, May 20, 2011	Sheet	3 of 66

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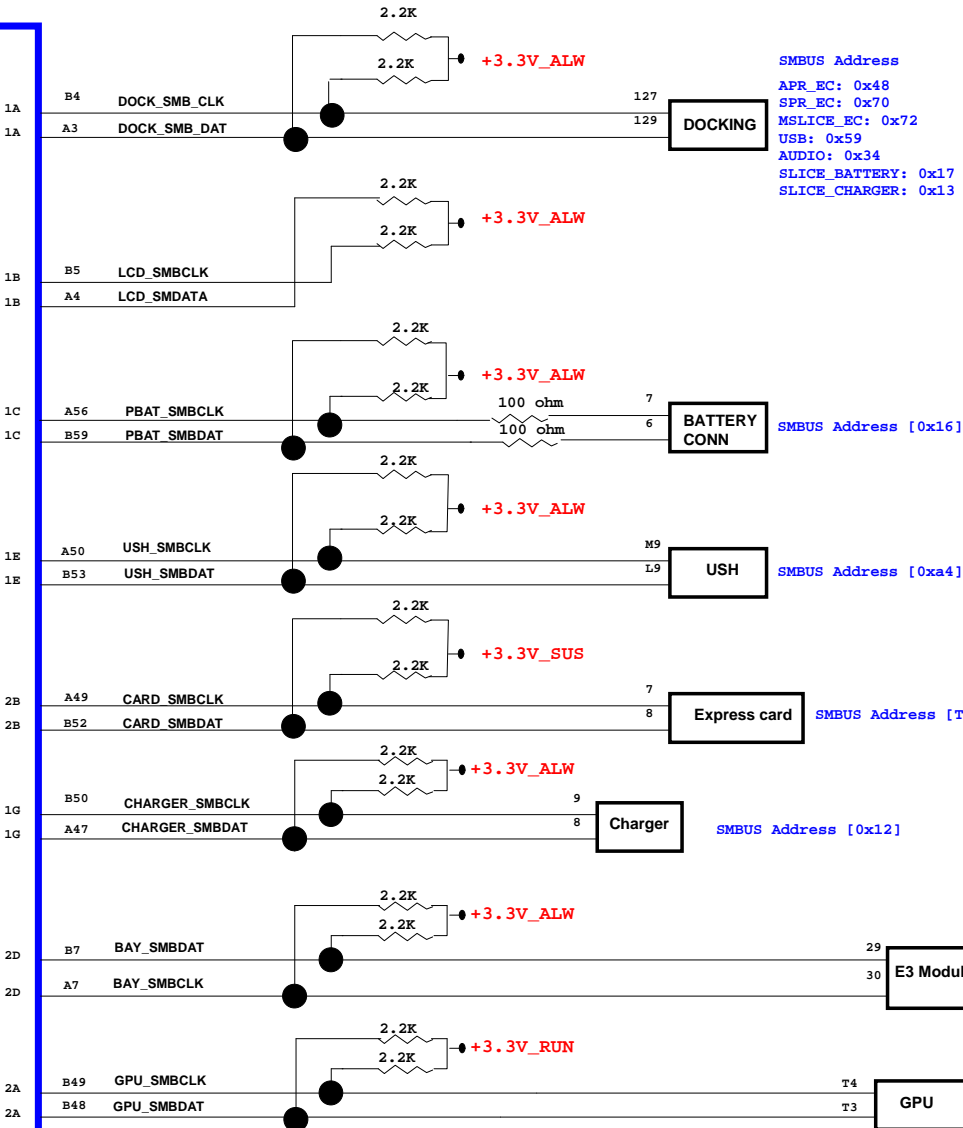
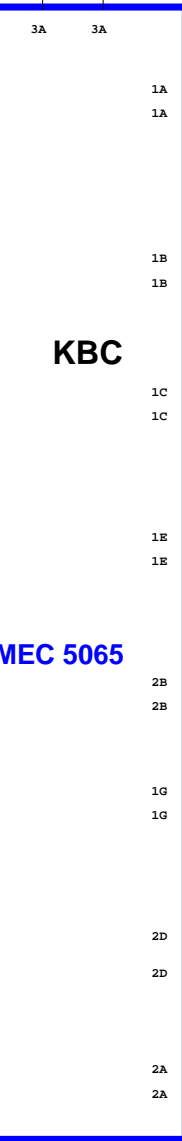
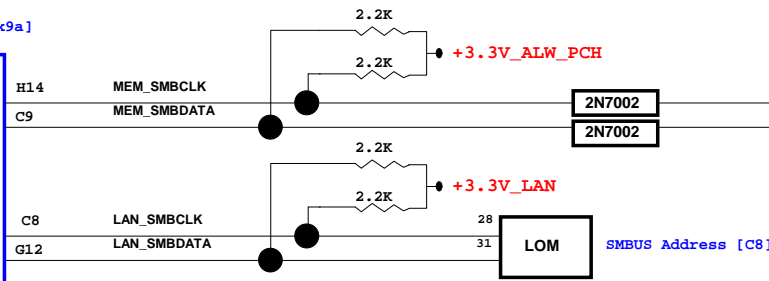
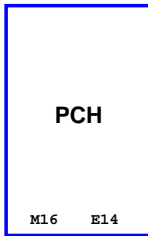


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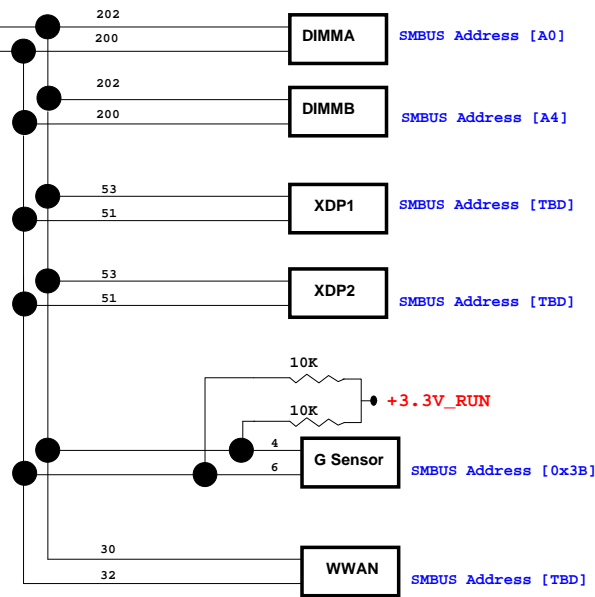
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Power Rail			
Title		Document Number	
		LA-7782	
Date:	Friday, May 20, 2011	Sheet	4 of 66
Rev	0.1		

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SMBUS Address [0x9a]

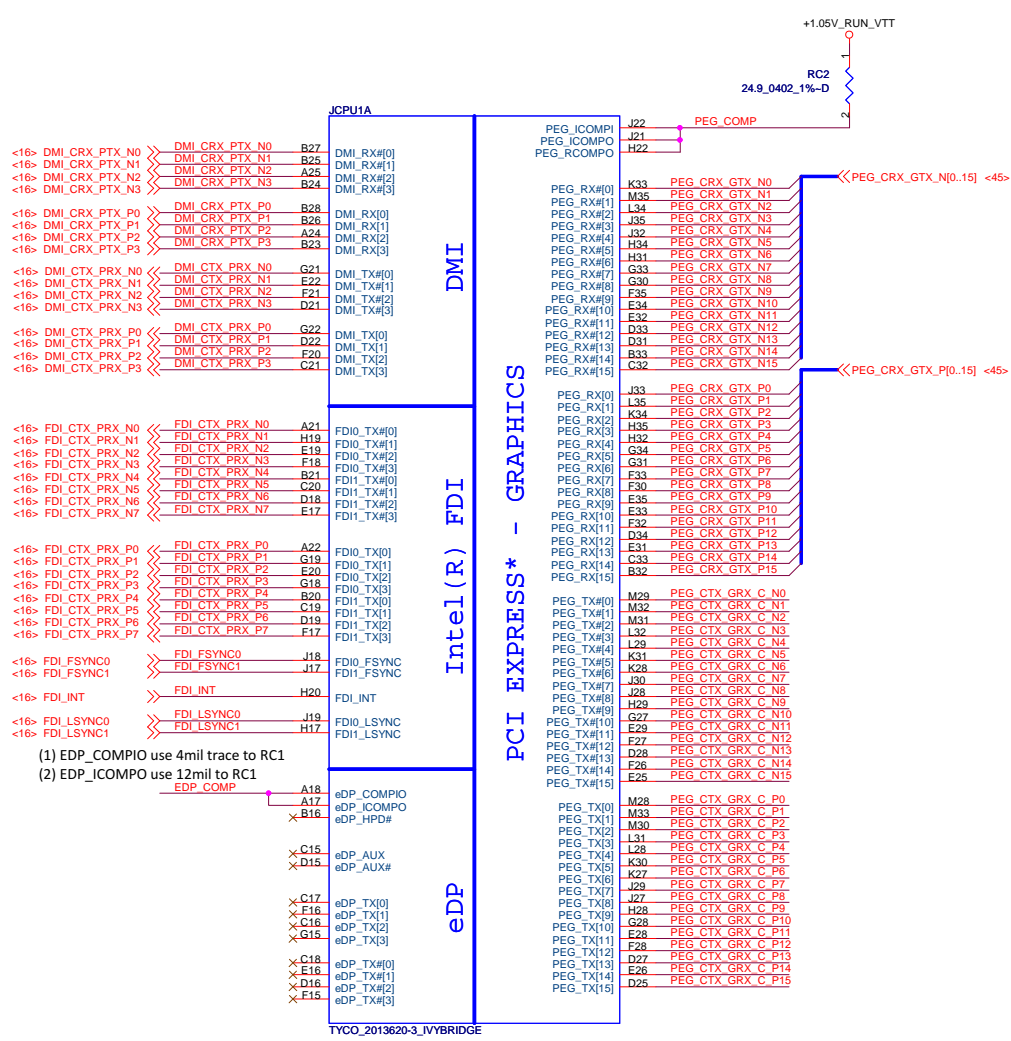


SMBUS Address
APR_EC: 0x48
SPR_EC: 0x70
MSLICE_EC: 0x72
USB: 0x59
AUDIO: 0x34
SLICE_BATTERY: 0x17
SLICE_CHARGER: 0x13

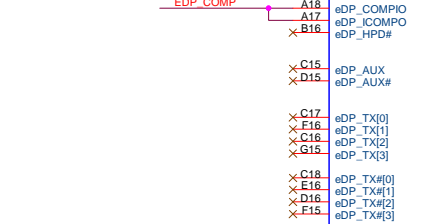


MEC 5065

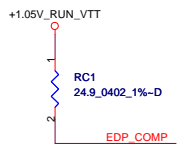
(1) PEG_RCOMP0 (H22) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC2.
 (2) PEG_ICOMPO use 12mil connect to RC2



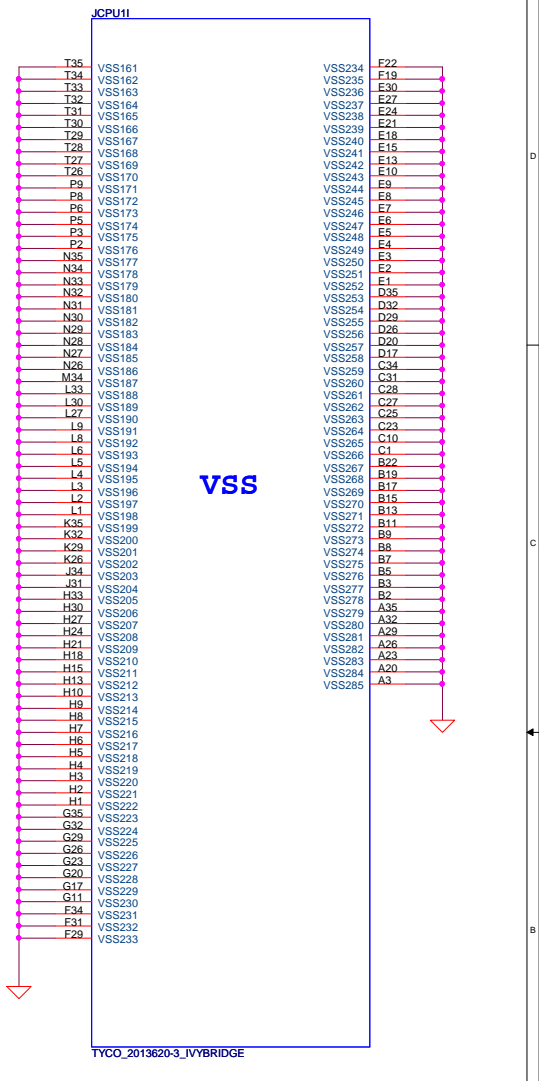
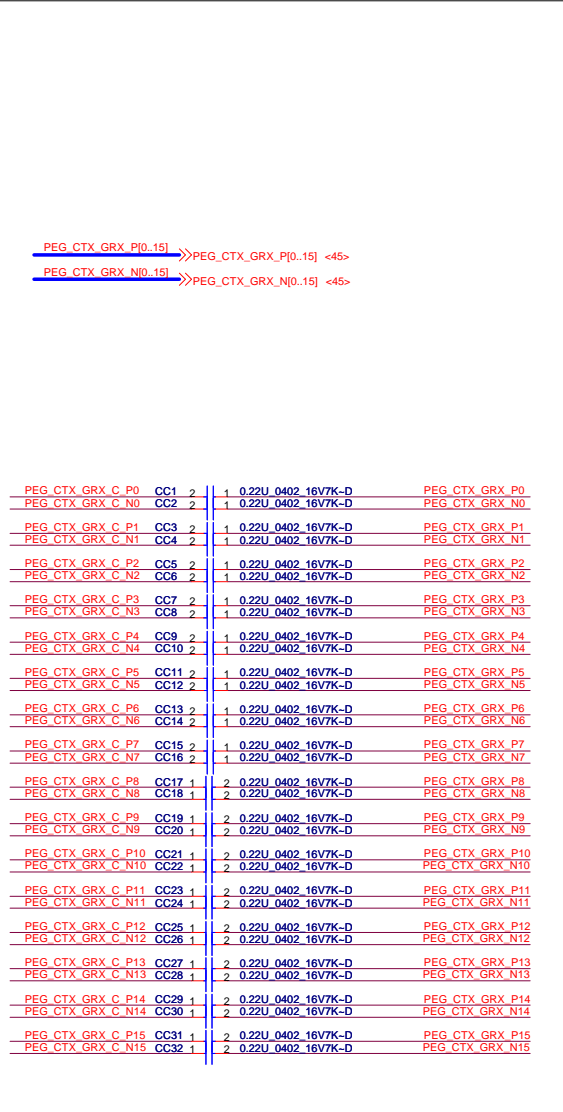
(1) EDP_COMPIO use 4mil trace to RC1
 (2) EDP_ICOMPO use 12mil to RC1



DP Compensation



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



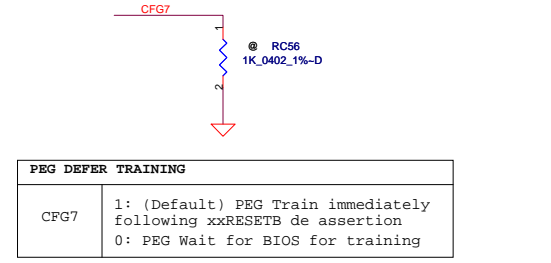
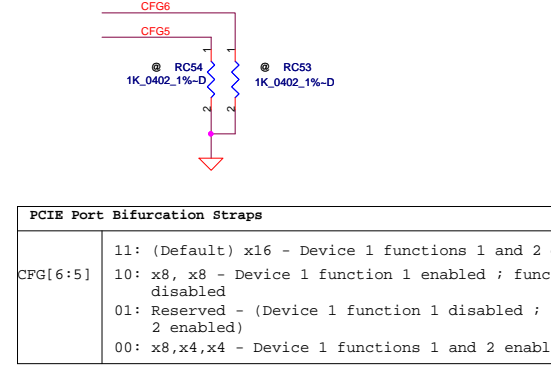
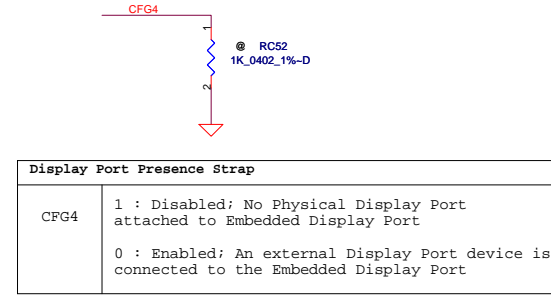
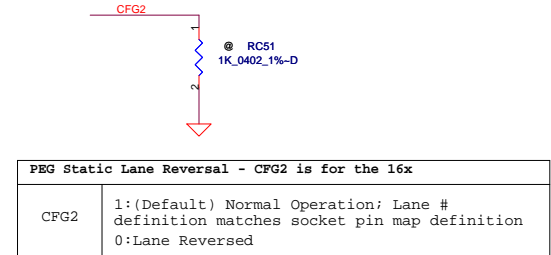
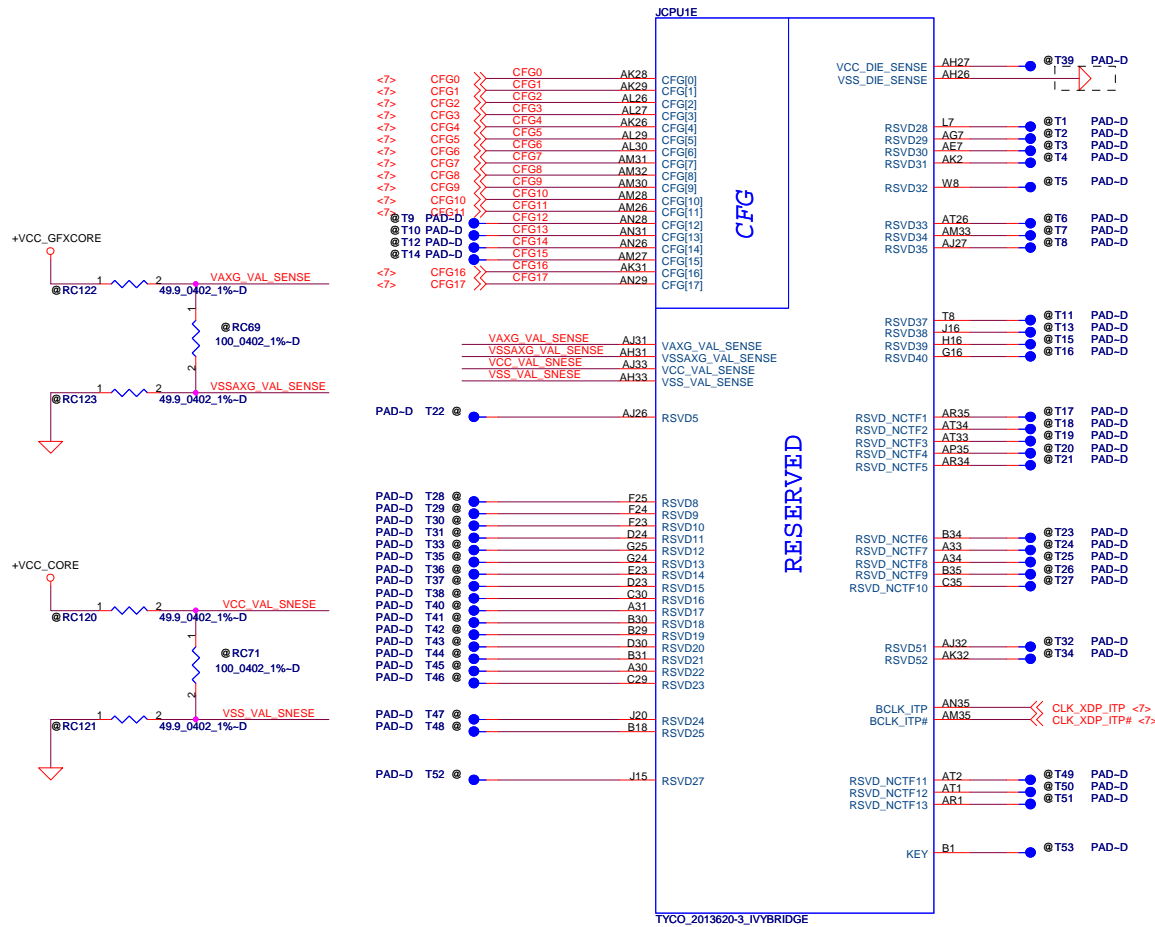
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Ivy Bridge (1/6)			
LA-7782			
Size	Document Number	Rev	0.1
Date:	Friday, June 10, 2011	Sheet	6 of 66

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CFG Straps for Processor



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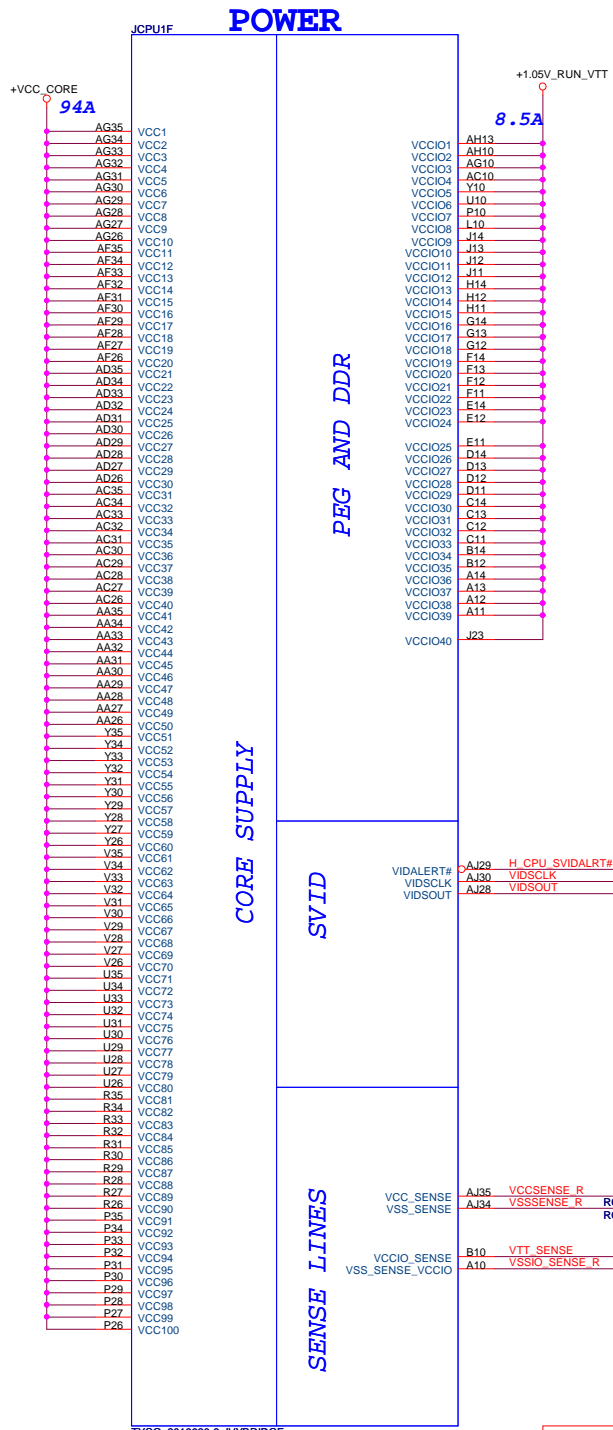
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Ivy Bridge (1/6)

LA-7782

Rev 0.1

Date: Friday, June 10, 2011 Sheet 9 of 66



Note: Place the PU resistors close to CPU
RC61 close to CPU 300 - 1500mils

CAD Note: Place the PU resistors close to CPU
RC63 close to CPU 300 - 1500mils

H_CPU_SVIDALRT# must be routed between the VIDSOUT and VIDSCLK lines to reduce cross talk. 18 mils spacing to others.

Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05	8.5
VAXG	0.0-1.1	26
VDDQ	1.5	5
VCCSA	0.65-0.9	6
* Description		
5A to Mem controller(+1.5V_CPU_VDDQ)		
5-6A to 2 DIMMs/channel		
2-5A to +1.5V_RUN & +0.75V_DDR_VTT		

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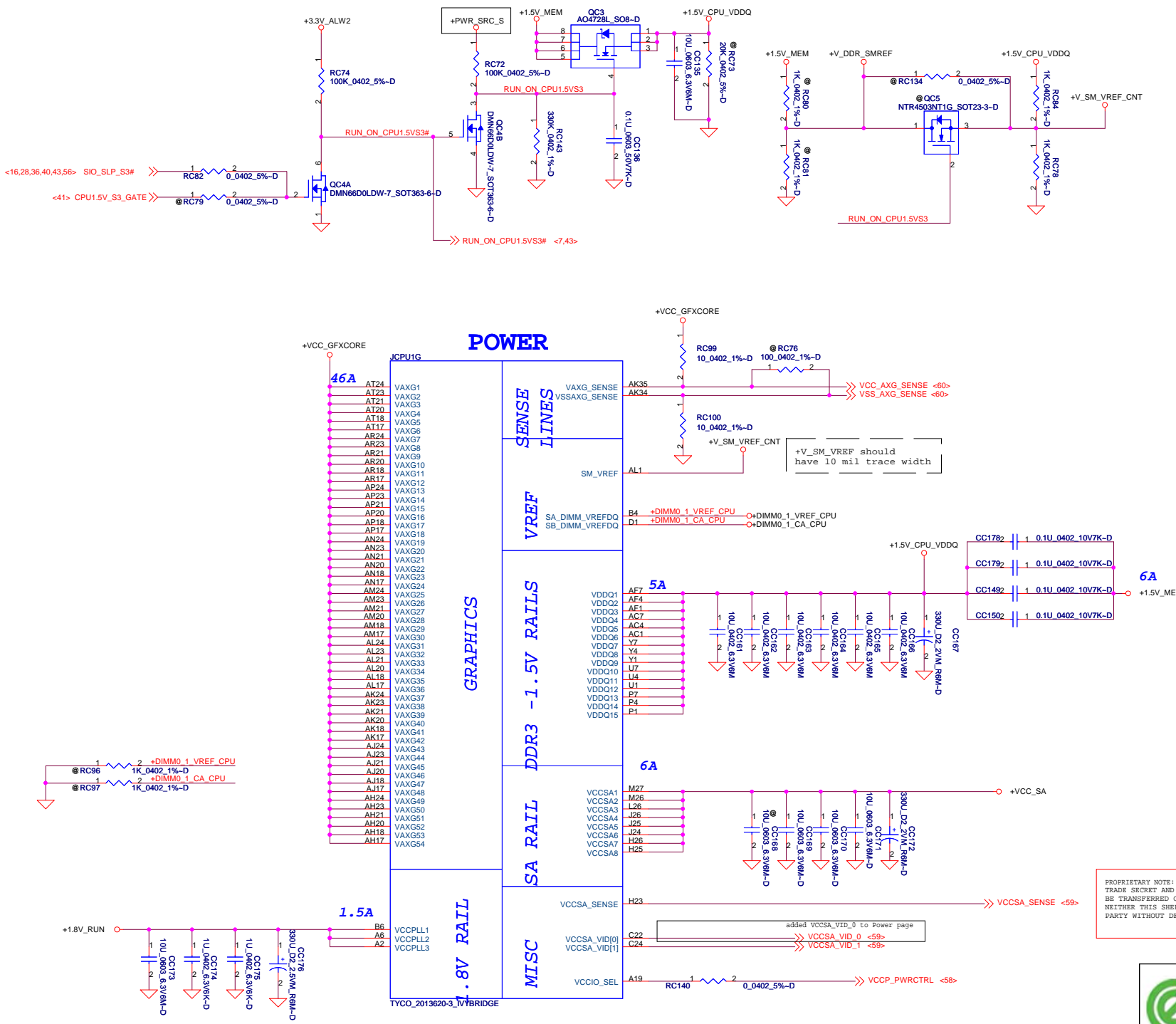
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Size Document Number LA-7782 Rev 0.1
Date: Friday, June 10, 2011 Sheet 10 of 66

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+1.5V_CPU_VDDQ Source



JCPU1H		
AT35	VSS1	VSS81
AT32	VSS2	AJ19
VSS3	VSS83	AJ16
AT27	VSS4	AJ13
AT25	VSS5	AJ10
AT22	VSS6	AJ7
AT19	VSS7	AJ4
AT16	VSS8	AJ3
AT13	VSS9	AJ2
AT10	VSS10	AJ1
AT7	VSS11	AH35
AT4	VSS12	VSS92
AR7	VSS13	AH22
AR3	VSS14	VSS94
AR25	VSS15	VSS95
AR19	VSS16	VSS98
AR16	VSS17	VSS99
AR13	VSS18	VSS99
AR10	VSS19	VSS99
AR7	VSS20	VSS101
AR4	VSS21	VSS102
AR2	VSS22	VSS103
AP34	VSS23	VSS104
AP31	VSS24	VSS105
AP28	VSS25	VSS106
AP25	VSS26	VSS107
AP22	VSS27	VSS108
AP19	VSS28	VSS109
AP16	VSS29	VSS110
AP13	VSS30	VSS111
AP10	VSS31	VSS112
AP7	VSS32	VSS113
AP4	VSS33	VSS114
AN30	VSS34	VSS115
AN27	VSS35	VSS116
AN25	VSS36	VSS117
AN22	VSS37	VSS118
AN20	VSS38	VSS119
AN18	VSS39	VSS120
AN16	VSS40	VSS121
AN13	VSS41	VSS122
AN10	VSS42	VSS123
AN7	VSS43	VSS124
AN4	VSS44	VSS125
AM29	VSS45	VSS126
AM25	VSS46	VSS127
AM22	VSS47	VSS128
AM19	VSS48	VSS129
AM16	VSS49	VSS130
AM13	VSS50	VSS131
AM10	VSS51	VSS132
AM7	VSS52	VSS133
AM4	VSS53	VSS134
AM3	VSS54	VSS135
AM2	VSS55	VSS136
AM1	VSS56	VSS137
AL34	VSS57	VSS138
AL31	VSS58	VSS139
AL28	VSS59	VSS140
AL25	VSS60	VSS141
AL22	VSS61	VSS142
AL19	VSS62	VSS143
AL16	VSS63	VSS144
AL13	VSS64	VSS145
AL10	VSS65	VSS146
AL7	VSS66	VSS147
AL4	VSS67	VSS148
AK3	VSS68	VSS149
AK33	VSS69	VSS150
AK30	VSS70	VSS151
AK27	VSS71	VSS152
AK25	VSS72	VSS153
AK22	VSS73	VSS154
AK19	VSS74	VSS155
AK16	VSS75	VSS156
AK13	VSS76	VSS157
AK10	VSS77	VSS158
AK7	VSS78	VSS159
AK4	VSS79	VSS160
AJ25	VSS80	VSS160
AJ22	VSS81	AJ19
AJ19	VSS82	AJ16
AJ16	VSS83	AJ13
AJ13	VSS84	AJ10
AJ10	VSS85	AJ7
AJ7	VSS86	AJ4
AJ4	VSS87	AJ3
AJ3	VSS88	AJ2
AJ2	VSS89	AJ1
AJ1	VSS90	AH35
AH35	VSS91	AH22
AH22	VSS92	AH29
AH29	VSS93	AH22
AH22	VSS94	AH29
AH29	VSS95	AH30
AH30	VSS96	AH28
AH28	VSS97	AH25
AH25	VSS98	AH22
AH22	VSS99	AH19
AH19	VSS100	AH16
AH16	VSS101	AH7
AH7	VSS102	AH4
AH4	VSS103	AG9
AG9	VSS104	AG8
AG8	VSS105	AG4
AG4	VSS106	AF6
AF6	VSS107	AF5
AF5	VSS108	AF3
AF3	VSS109	AF2
AF2	VSS110	AE35
AE35	VSS111	AE34
AE34	VSS112	AE33
AE33	VSS113	AE31
AE31	VSS114	AE30
AE30	VSS115	AE29
AE29	VSS116	AE28
AE28	VSS117	AE27
AE27	VSS118	AE26
AE26	VSS119	AE9
AE9	VSS120	AD7
AD7	VSS121	AC9
AC9	VSS122	AC8
AC8	VSS123	AC6
AC6	VSS124	AC5
AC5	VSS125	AC3
AC3	VSS126	AC2
AC2	VSS127	AB35
AB35	VSS128	AB34
AB34	VSS129	AB33
AB33	VSS130	AB32
AB32	VSS131	AB31
AB31	VSS132	AB30
AB30	VSS133	AB29
AB29	VSS134	AB28
AB28	VSS135	AB27
AB27	VSS136	AB26
AB26	VSS137	Y9
Y9	VSS138	Y8
Y8	VSS139	Y5
Y5	VSS140	Y3
Y3	VSS141	Y2
Y2	VSS142	W35
W35	VSS143	W34
W34	VSS144	W33
W33	VSS145	W32
W32	VSS146	W31
W31	VSS147	W30
W30	VSS148	W29
W29	VSS149	W28
W28	VSS150	W27
W27	VSS151	W26
W26	VSS152	U9
U9	VSS153	U8
U8	VSS154	U6
U6	VSS155	U5
U5	VSS156	U3
U3	VSS157	U2
U2	VSS158	
U1	VSS159	
	VSS160	

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Ivy Bridge (1/6)

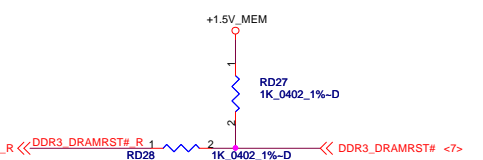
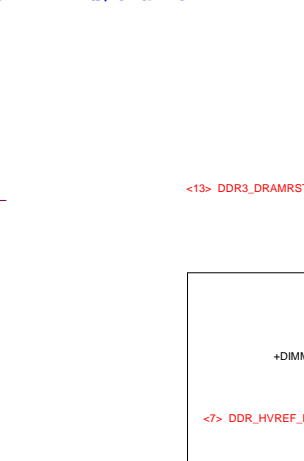
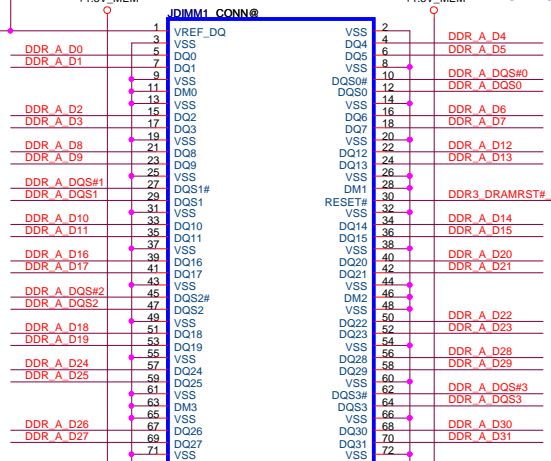
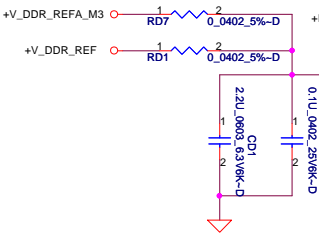
LA-7782

Friday, June 10, 2011

Sheet 11 of 66

JDIMM1 H=5.2

2-3A to 1 DIMMs/channel

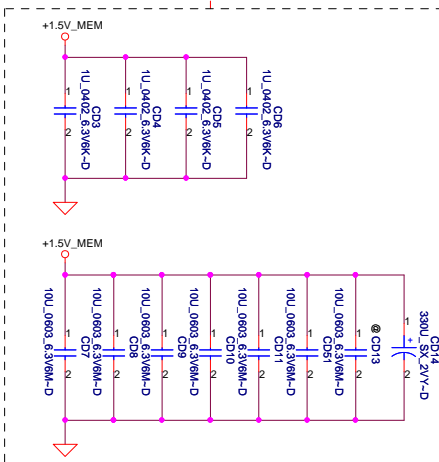


Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

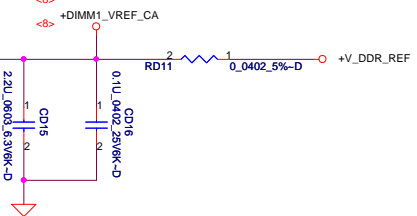
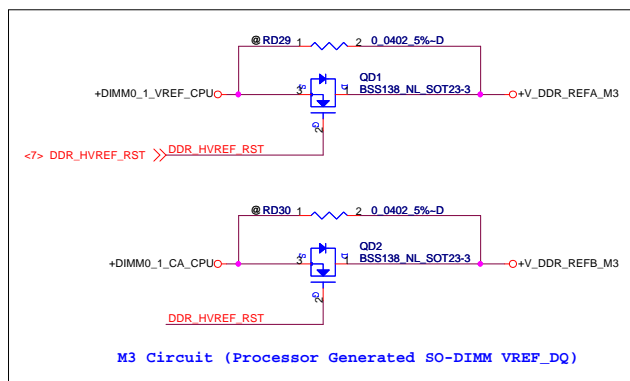
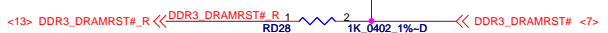
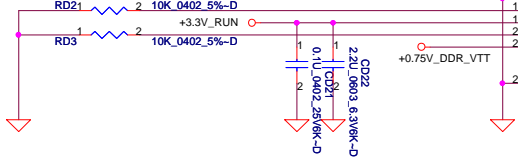
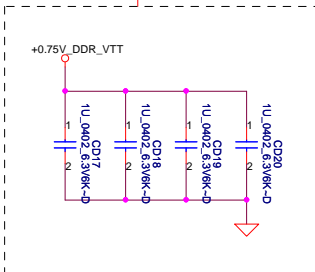
All VREF traces should have 10 mil trace width



Layout Note: Place near JDIMM1



Layout Note: Place near JDIMM1.203,204

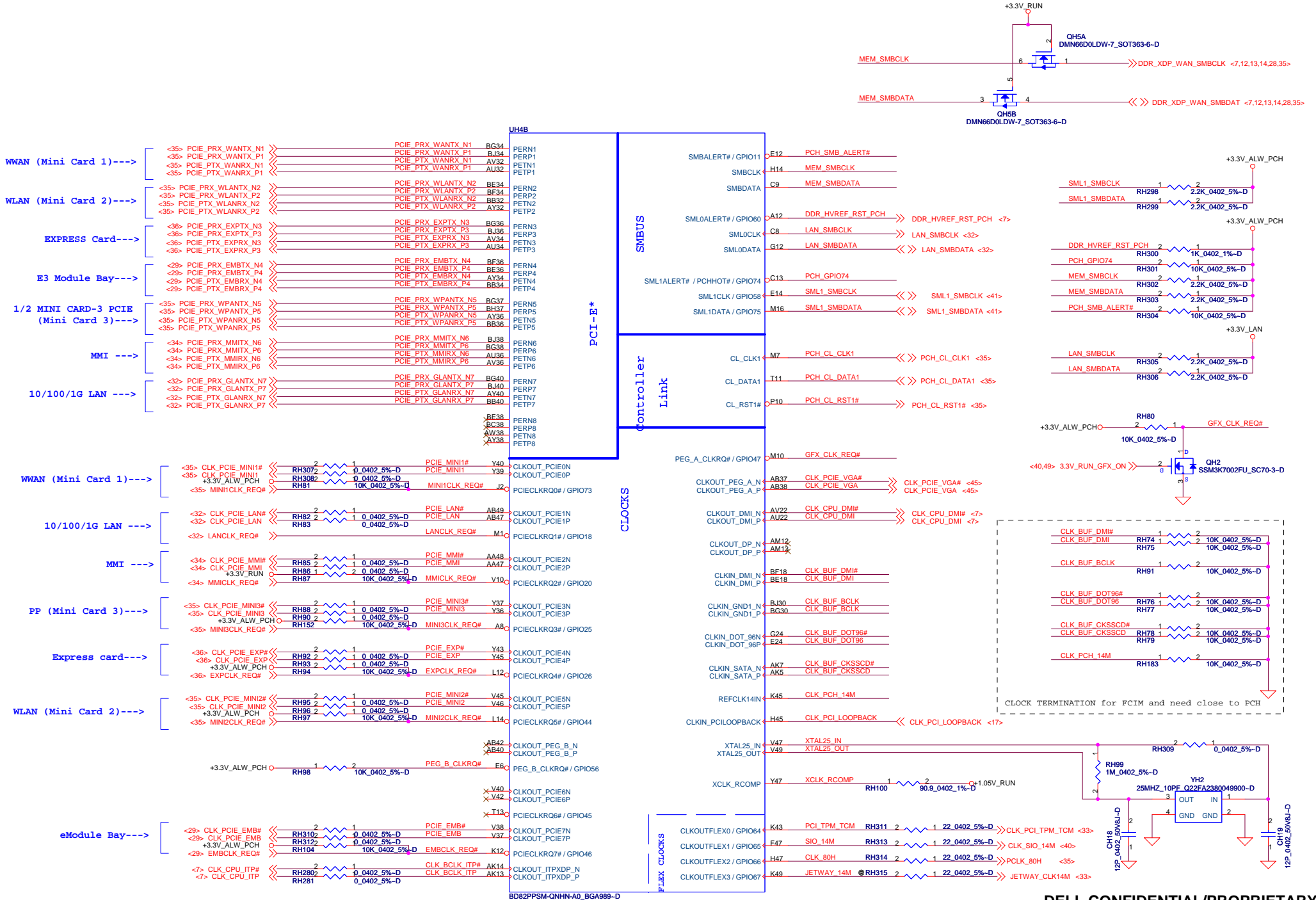


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Title DDRIII-SODIMM SLOT1		
Size	Document Number LA-7782	Rev 0.1
Date	Friday, June 10, 2011	Sheet 12 of 66

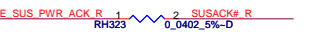
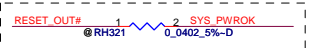
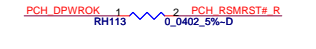
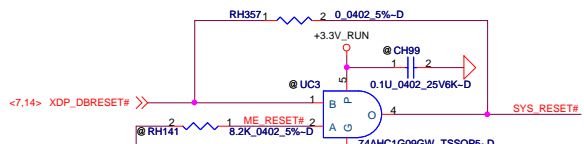
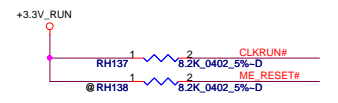
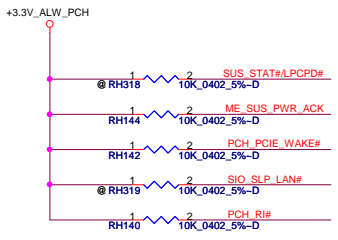


PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2

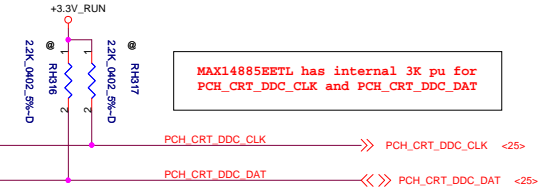
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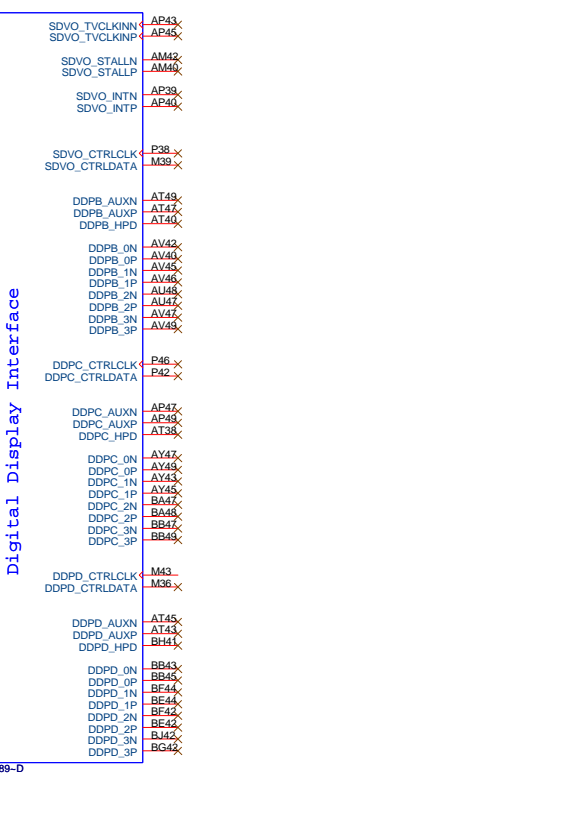
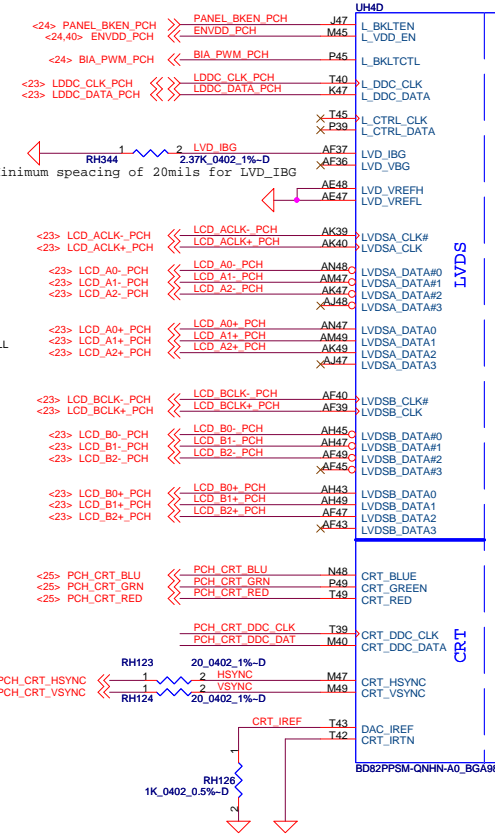
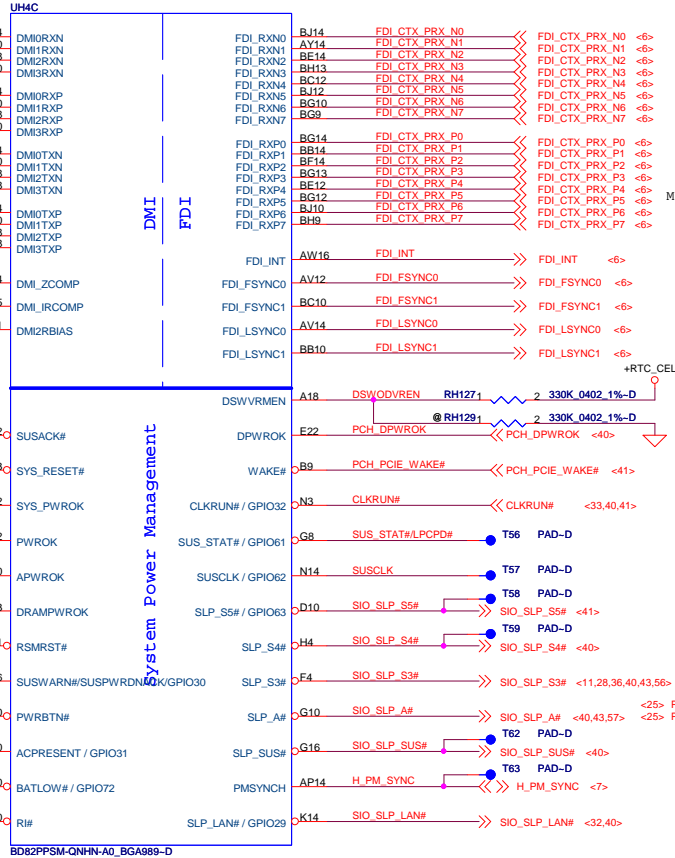
Compal Electronics, Inc.			
PCH (2/8)			
LA-7782			
Size	Document Number	Rev	0.1
Date:	Friday, June 10, 2011	Sheet	15 of 66



DSWODVREN - On Die DSW VR Enable
Enabled (DEFAULT)
HIGH: RH127 STUFFED, RH129 UNSTUFFED
Disabled
LOW: RH129 STUFFED, RH127 UNSTUFFED



MAX1485EETL has internal 3K pu for PCH_CRT_DDC_CLK and PCH_CRT_DDC_DAT



Intel request DDPB can not support eDP

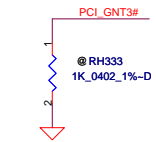
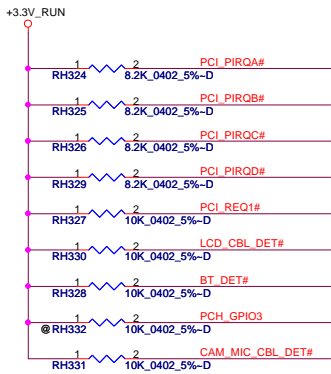
Digital Display Interface

CRT

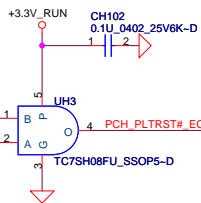
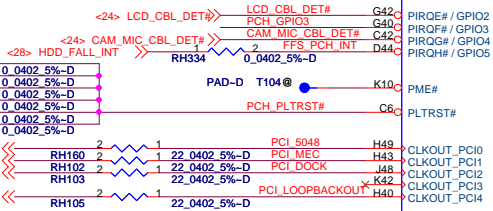
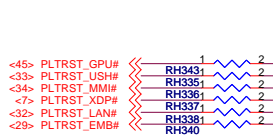
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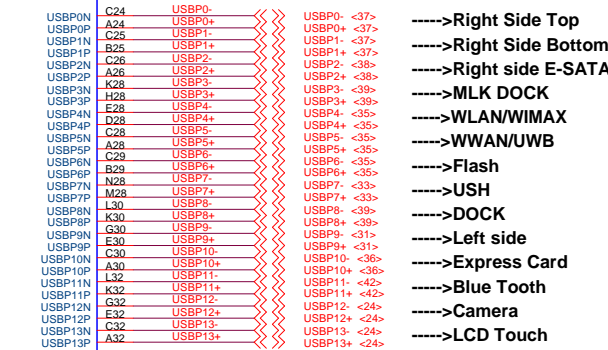
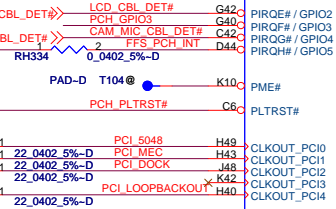
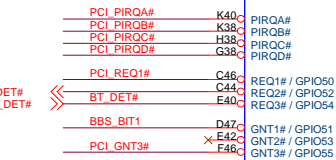
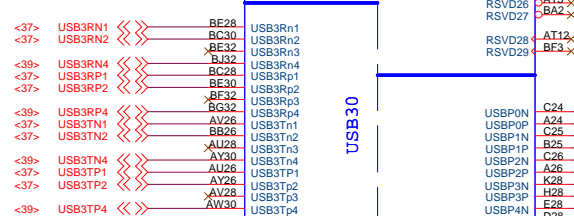
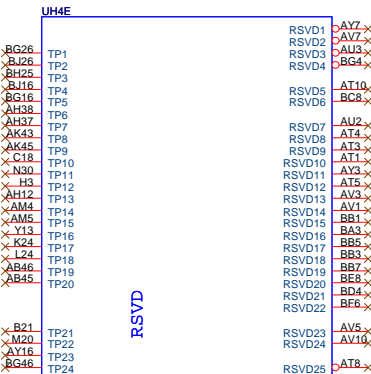
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Compal Electronics, Inc.			
PCH (3/8)			
Size	Document Number	Rev 0.1	
	LA-7782		
Date:	Friday, June 10, 2011	Sheet	16 of 66



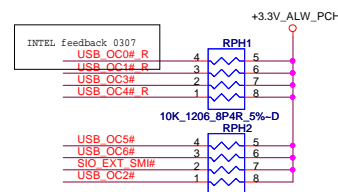
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



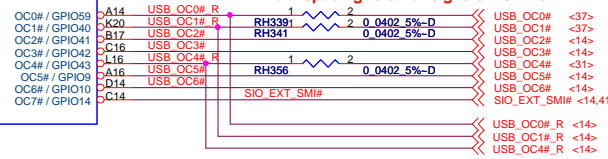
<7,14> PCH_PLTRST# >> PCH_PLTRST# >> PCH_PLTRST#_EC <33,35,36,40,41>



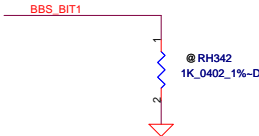
- >Right Side Top
- >Right Side Bottom
- >Right side E-SATA
- >MLK DOCK
- >WLAN/WIMAX
- >WWAN/UWB
- >Flash
- >USH
- >DOCK
- >Left side
- >Express Card
- >Blue Tooth
- >Camera
- >LCD Touch



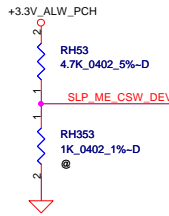
Route single-end 50-ohms and max 500-mils length. Minimum spacing to other signals: 15 mils



Boot BIOS Strap		
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

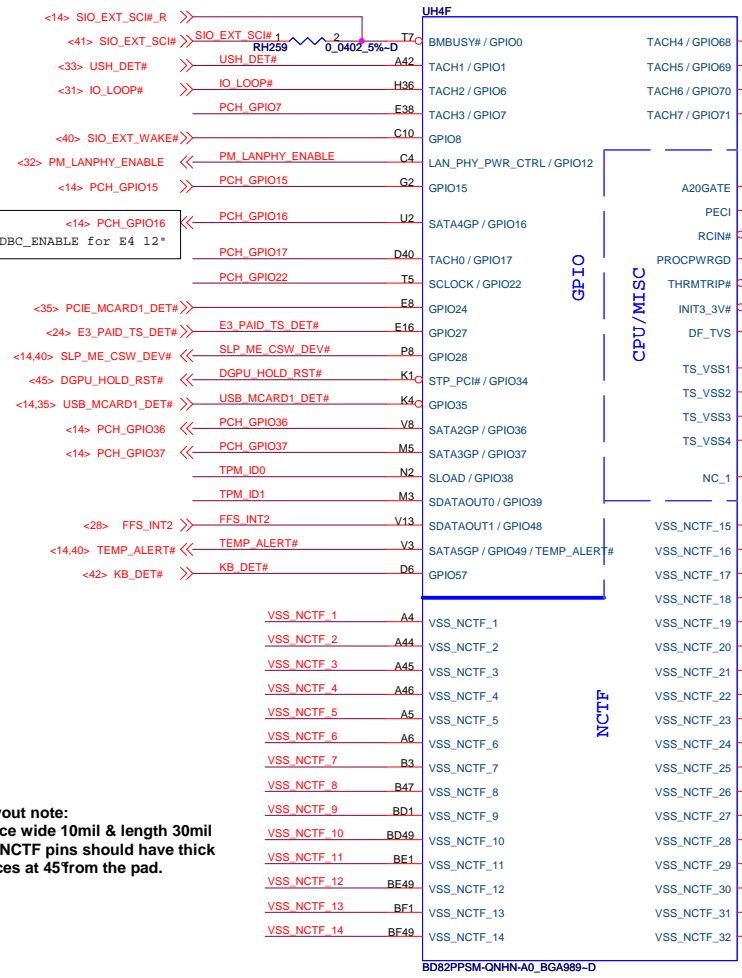
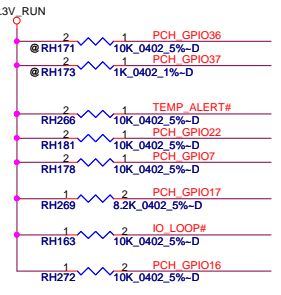
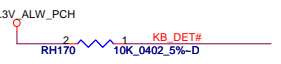
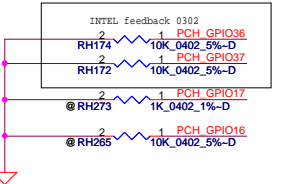
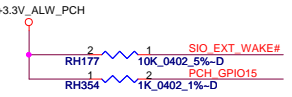


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Compal Electronics, Inc.
PCH (4/8)
 Title: PCH (4/8)
 Size: Document Number LA-7782
 Date: Friday, June 10, 2011 Sheet 17 of 66
 Rev 0.1

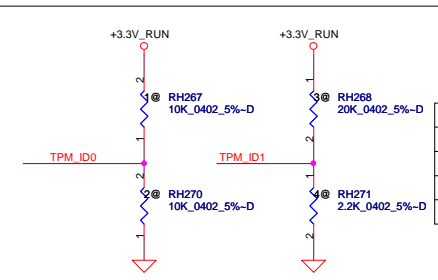


Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

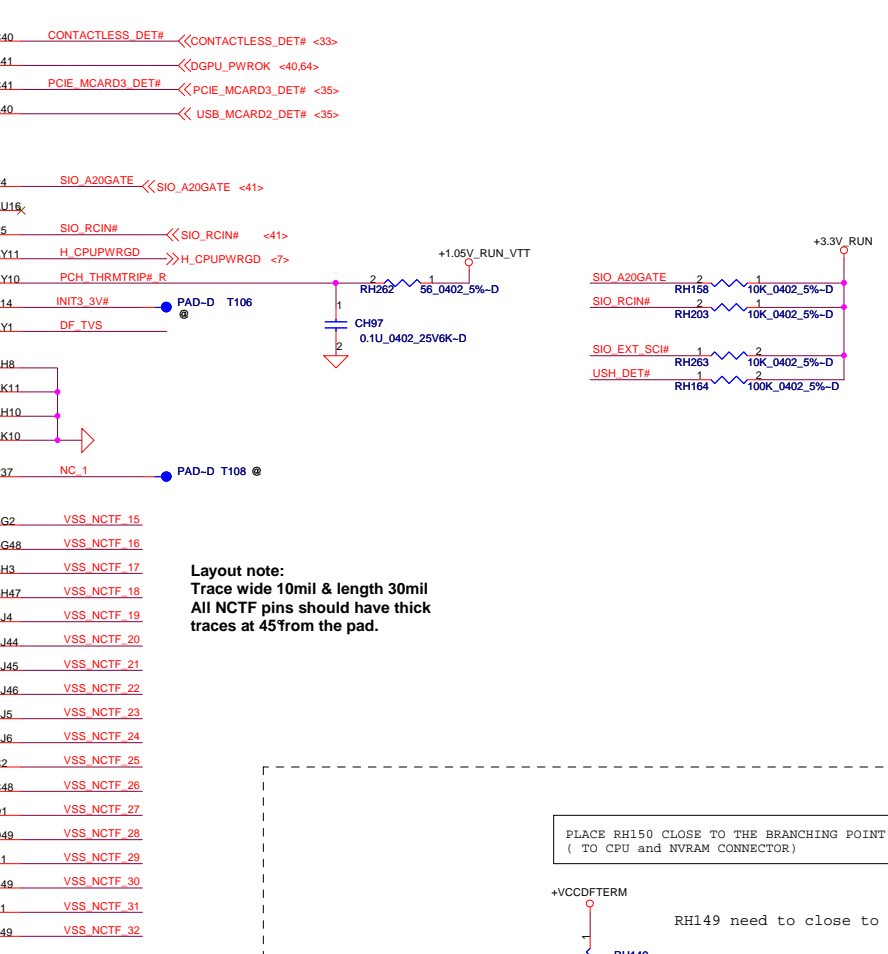
SLP_ME_CSW_DEV# PLL ON DIE VR ENABLE
 ENABLED - HIGH DEFAULT
 DISABLED - LOW



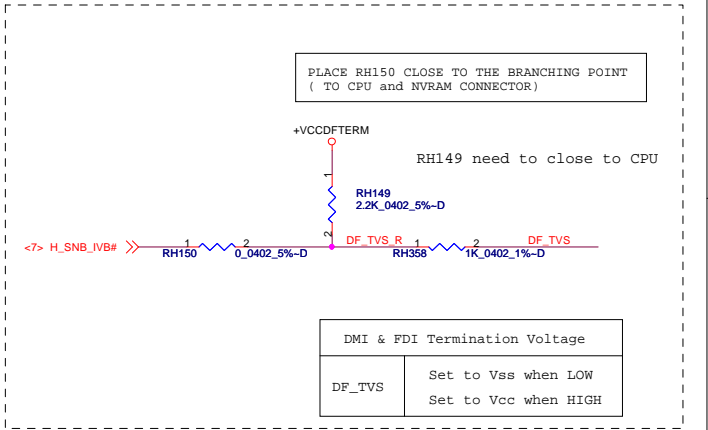
Layout note:
 Trace wide 10mil & length 30mil
 All NCTF pins should have thick traces at 45mil from the pad.



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
TBD		
TPM	1	1



Layout note:
 Trace wide 10mil & length 30mil
 All NCTF pins should have thick traces at 45mil from the pad.



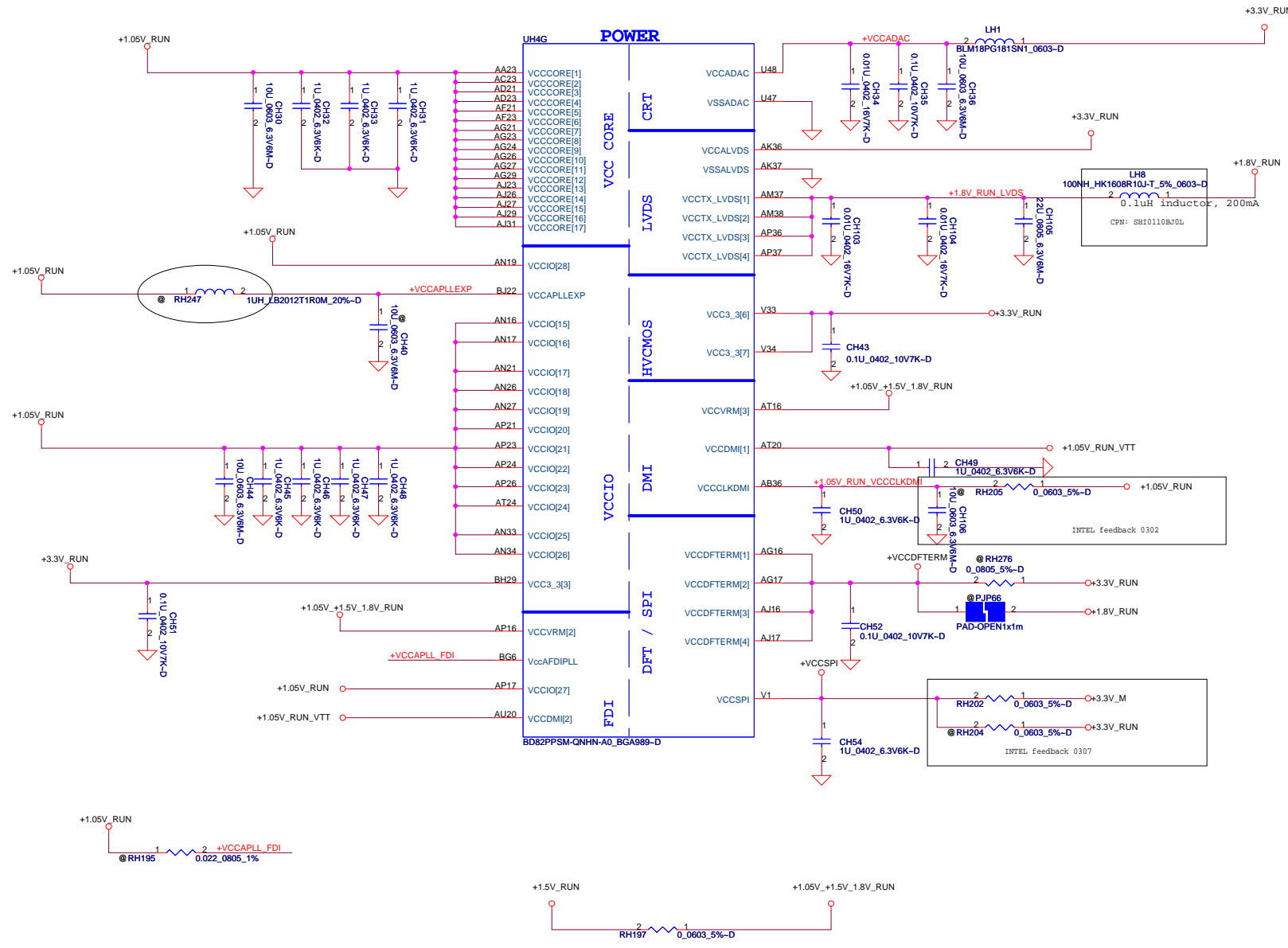
DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH



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Compal Electronics, Inc.

Title PCH (5/8)		
Size	Document Number LA-7782	Rev 0.1
Date	Friday, June 10, 2011	Sheet 18 of 66



PCH Power Rail Table		
Voltage Rail	Voltage	60 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC3	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VCCDFTERM	1.8	0.002
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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Title			PCH (6/8)		
Size	Document Number				Rev
	LA-7782				0.1
Date:	Tuesday, June 07, 2011	Sheet	19	of	66

UH4H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK4
AA33	VSS[4]	VSS[83] AK46
AA34	VSS[5]	VSS[84] AK8
AB11	VSS[6]	VSS[85] AL16
AB14	VSS[7]	VSS[86] AL17
AB39	VSS[8]	VSS[87] AL19
AB4	VSS[9]	VSS[88] AL2
AB43	VSS[10]	VSS[89] AL21
AB5	VSS[11]	VSS[90] AL23
AB7	VSS[12]	VSS[91] AL26
AC19	VSS[13]	VSS[92] AL27
AC2	VSS[14]	VSS[93] AL31
AC21	VSS[15]	VSS[94] AL33
AC24	VSS[16]	VSS[95] AL34
AC33	VSS[17]	VSS[96] AL48
AC34	VSS[18]	VSS[97] AM11
AC48	VSS[19]	VSS[98] AM14
AD10	VSS[20]	VSS[99] AM36
AD11	VSS[21]	VSS[100] AM39
AD12	VSS[22]	VSS[101] AM43
AD13	VSS[23]	VSS[102] AM45
AD19	VSS[24]	VSS[103] AM46
AD24	VSS[25]	VSS[104] AM7
AD26	VSS[26]	VSS[105] AN2
AD27	VSS[27]	VSS[106] AN29
AD33	VSS[28]	VSS[107] AN3
AD36	VSS[29]	VSS[108] AN31
AD37	VSS[30]	VSS[109] AP12
AD38	VSS[31]	VSS[110] AP19
AD39	VSS[32]	VSS[111] AP28
AD4	VSS[33]	VSS[112] AP32
AD40	VSS[34]	VSS[113] AP38
AD42	VSS[35]	VSS[114] AP38
AD43	VSS[36]	VSS[115] AP4
AD45	VSS[37]	VSS[116] AP42
AD46	VSS[38]	VSS[117] AP46
AD5	VSS[39]	VSS[118] AP8
AD8	VSS[40]	VSS[119] AR2
AE2	VSS[41]	VSS[120] AR48
AE3	VSS[42]	VSS[121] AT11
AF10	VSS[43]	VSS[122] AT13
AF12	VSS[44]	VSS[123] AT18
AD14	VSS[45]	VSS[124] AT22
AF16	VSS[46]	VSS[125] AT26
AF19	VSS[47]	VSS[126] AT28
AF24	VSS[48]	VSS[127] AT30
AF26	VSS[49]	VSS[128] AT32
AF27	VSS[50]	VSS[129] AT34
AF29	VSS[51]	VSS[130] AT39
AF31	VSS[52]	VSS[131] AT42
AF38	VSS[53]	VSS[132] AT46
AF4	VSS[54]	VSS[133] AT7
AF42	VSS[55]	VSS[134] AU24
AF46	VSS[56]	VSS[135] AU30
AF5	VSS[57]	VSS[136] AV16
AF7	VSS[58]	VSS[137] AV20
AF8	VSS[59]	VSS[138] AV30
AG19	VSS[60]	VSS[139] AV38
AG2	VSS[61]	VSS[140] AV38
AG31	VSS[62]	VSS[141] AV4
AG48	VSS[63]	VSS[142] AV8
AH3	VSS[64]	VSS[143] AV14
AH11	VSS[65]	VSS[144] AW14
AH36	VSS[66]	VSS[145] AW18
AH39	VSS[67]	VSS[146] AW22
AH40	VSS[68]	VSS[147] AW22
AH40	VSS[69]	VSS[148] AW26
AH42	VSS[70]	VSS[149] AW28
AH46	VSS[71]	VSS[150] AW32
AH7	VSS[72]	VSS[151] AW34
AJ19	VSS[73]	VSS[152] AW36
AJ21	VSS[74]	VSS[153] AW40
AJ24	VSS[75]	VSS[154] AW48
AJ33	VSS[76]	VSS[155] AV11
AJ34	VSS[77]	VSS[156] AY12
AK12	VSS[78]	VSS[157] AY22
AK3	VSS[79]	VSS[158] AY28

BD82PPSM-QNHN-A0_BGA989-D

UH4I		
	VSS[159]	VSS[259]
AY4	VSS[159]	H46
AY42	VSS[160]	K18
AY46	VSS[161]	K26
AY8	VSS[162]	K39
B11	VSS[163]	K46
B15	VSS[164]	K7
B19	VSS[165]	L18
B23	VSS[166]	L2
B27	VSS[167]	L20
B31	VSS[168]	L26
B35	VSS[169]	L28
B39	VSS[170]	L36
B7	VSS[171]	L48
F45	VSS[172]	M12
BB12	VSS[173]	P16
BB16	VSS[174]	M18
BB20	VSS[175]	M22
BB22	VSS[176]	M24
BB24	VSS[177]	M30
BB28	VSS[178]	M32
BB30	VSS[179]	M34
BB38	VSS[180]	M38
BB4	VSS[181]	M4
BB46	VSS[182]	M42
BC14	VSS[183]	M46
BC18	VSS[184]	M8
BC2	VSS[185]	N18
BC22	VSS[186]	P30
BC26	VSS[187]	N47
BC32	VSS[188]	P11
BC34	VSS[189]	P18
BC36	VSS[190]	T33
BC40	VSS[191]	P40
BC42	VSS[192]	P43
BC48	VSS[193]	P47
BD4	VSS[194]	R2
BE22	VSS[195]	R48
BE26	VSS[196]	T12
BE40	VSS[197]	T31
BF10	VSS[198]	T37
BF12	VSS[199]	T4
BF16	VSS[200]	W34
BF20	VSS[201]	T46
BF22	VSS[202]	T47
BF24	VSS[203]	T8
BF26	VSS[204]	V11
BF28	VSS[205]	V17
BF3	VSS[206]	V26
BF30	VSS[207]	V27
BF38	VSS[208]	V29
BF40	VSS[209]	V31
BF8	VSS[210]	V36
BG17	VSS[211]	V38
BG21	VSS[212]	V43
BG23	VSS[213]	V47
BG44	VSS[214]	V7
BG8	VSS[215]	W17
BH11	VSS[216]	W19
BH15	VSS[217]	W2
BH17	VSS[218]	W27
BH19	VSS[219]	W48
H10	VSS[220]	Y12
BH27	VSS[221]	Y38
BH31	VSS[222]	Y4
BH33	VSS[223]	Y42
BH35	VSS[224]	Y8
BH39	VSS[225]	BG29
BH43	VSS[226]	N24
BH7	VSS[227]	AJ3
D3	VSS[228]	AD47
D12	VSS[229]	B43
D18	VSS[230]	BG41
D16	VSS[231]	BE10
D18	VSS[232]	G14
D22	VSS[233]	H16
D24	VSS[234]	T36
D26	VSS[235]	BG22
D30	VSS[236]	BG24
D32	VSS[237]	C22
D34	VSS[238]	AP13
D38	VSS[239]	AP14
D42	VSS[240]	AP3
D8	VSS[241]	M12
E18	VSS[242]	AP1
E26	VSS[243]	BE16
G18	VSS[244]	BC16
G20	VSS[245]	BG28
G26	VSS[246]	BJ28
G28	VSS[247]	
G36	VSS[248]	
G48	VSS[249]	
H12	VSS[250]	
H18	VSS[251]	
H22	VSS[252]	
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

BD82PPSM-QNHN-A0_BGA989-D

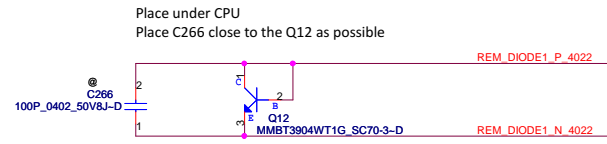
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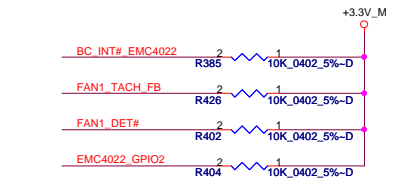
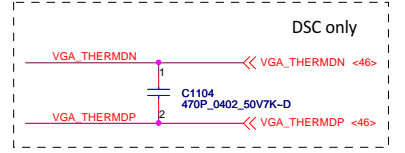
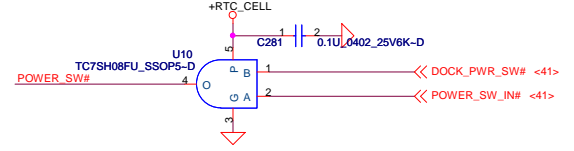
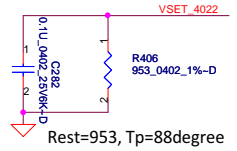
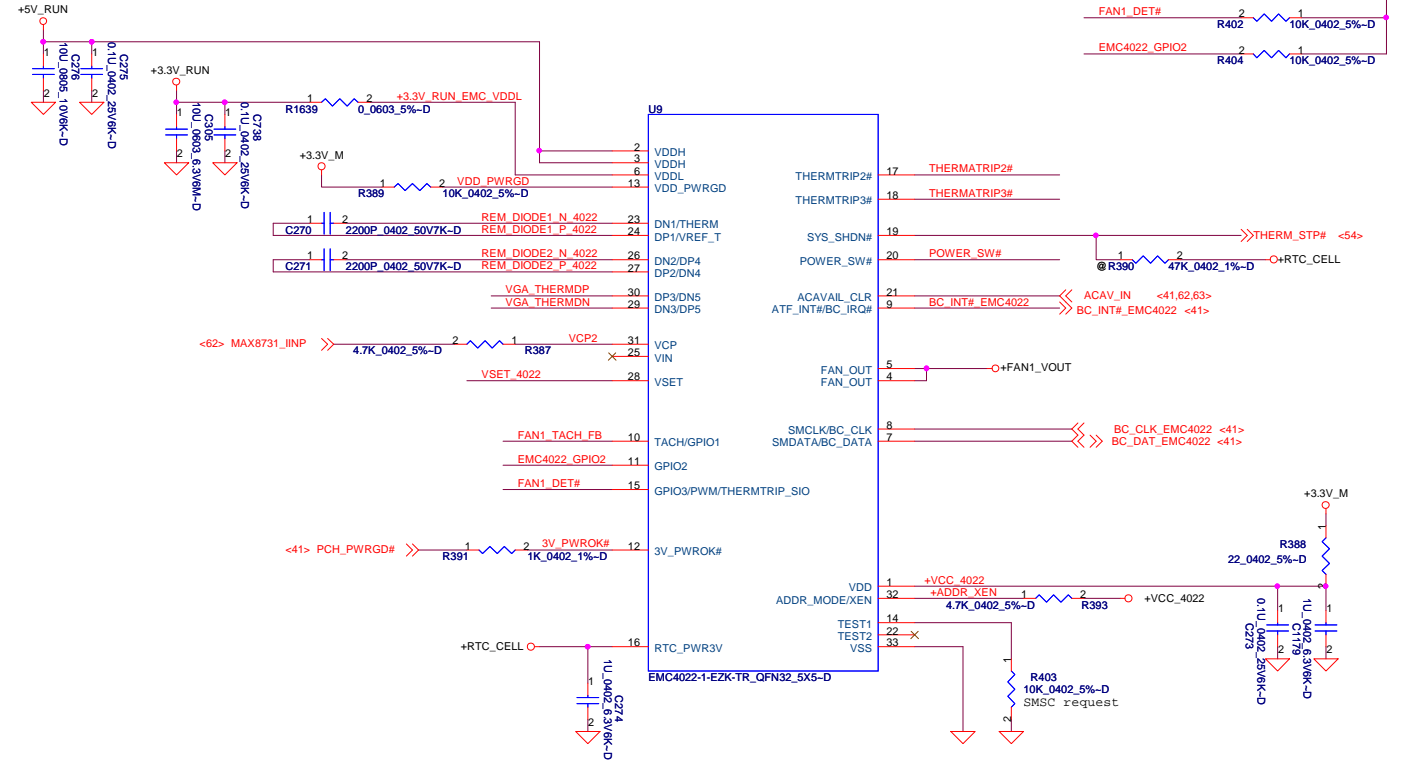
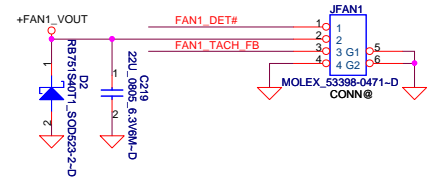
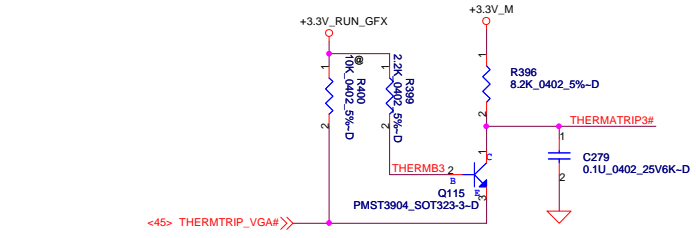
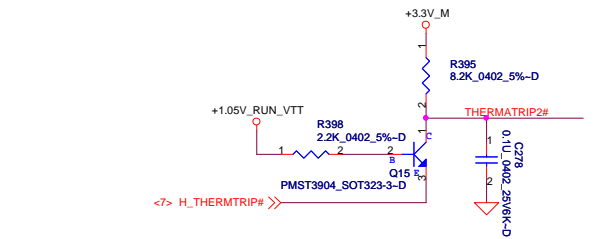
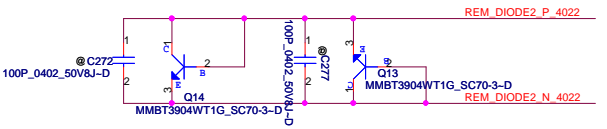
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Compal Electronics, Inc.

Title			PCH (8/8)		
Size			Document Number		
			LA-7782		
Date			Monday, May 23, 2011		
			Sheet 21 of 66		
			Rev 0.1		



- (1) DP3/DN3 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
- (2) DP5/DN5 for Skin on Q13, place Q13 close to Vcore VR choke.



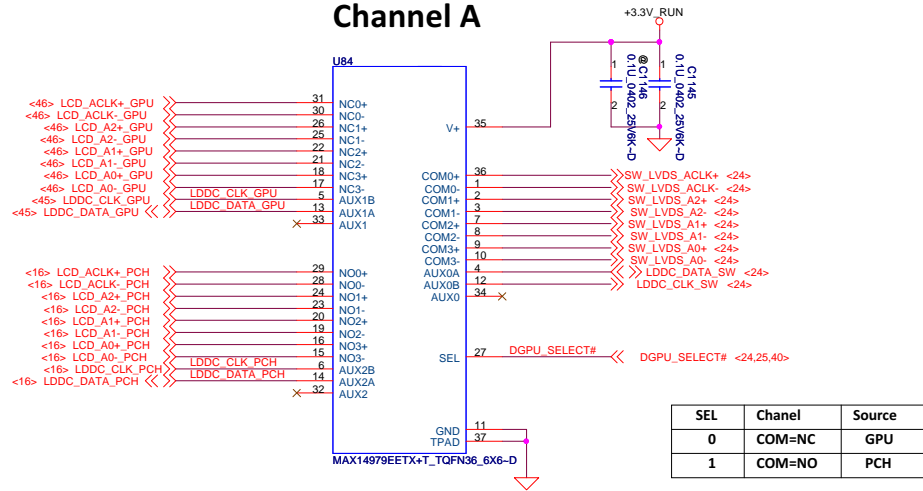
DELL CONFIDENTIAL/PROPRIETARY



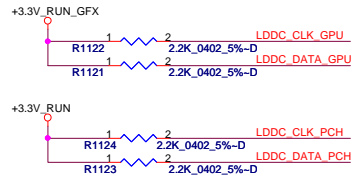
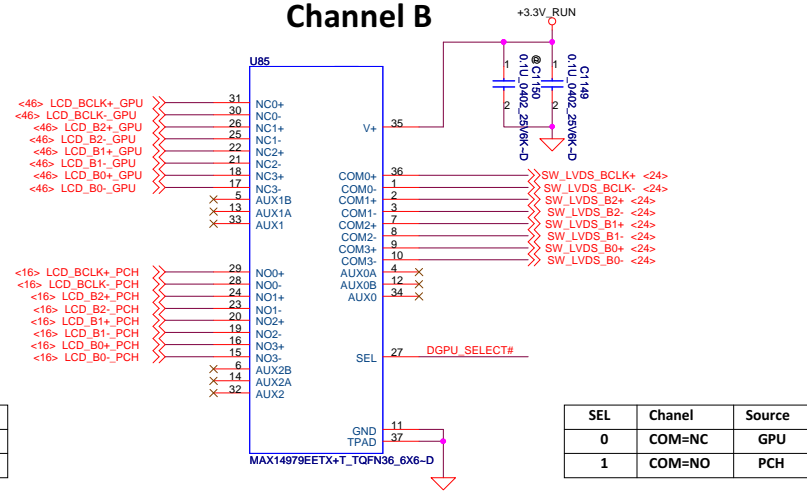
Compal Electronics, Inc.			
FAN & Thermal Sensor			
LA-7782			
Date:	Friday, June 10, 2011	Sheet	22 of 66
Rev	0.1		

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Channel A



Channel B

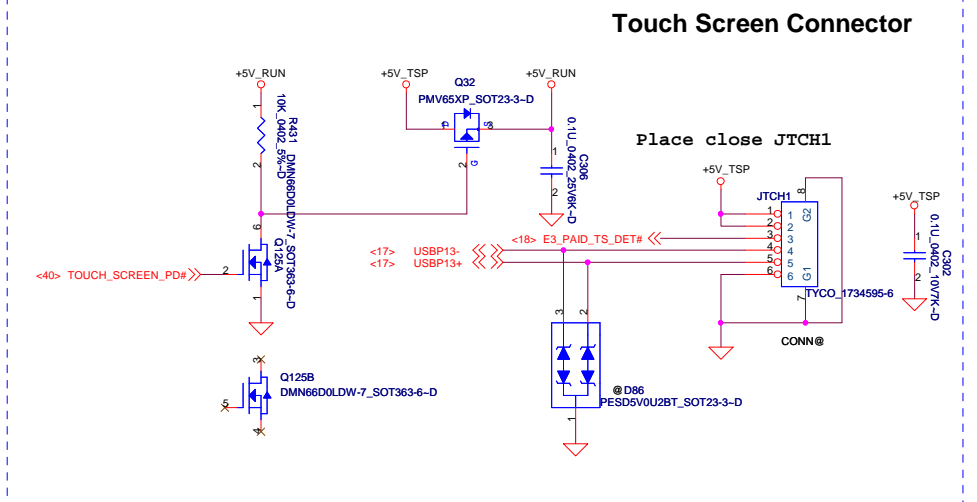
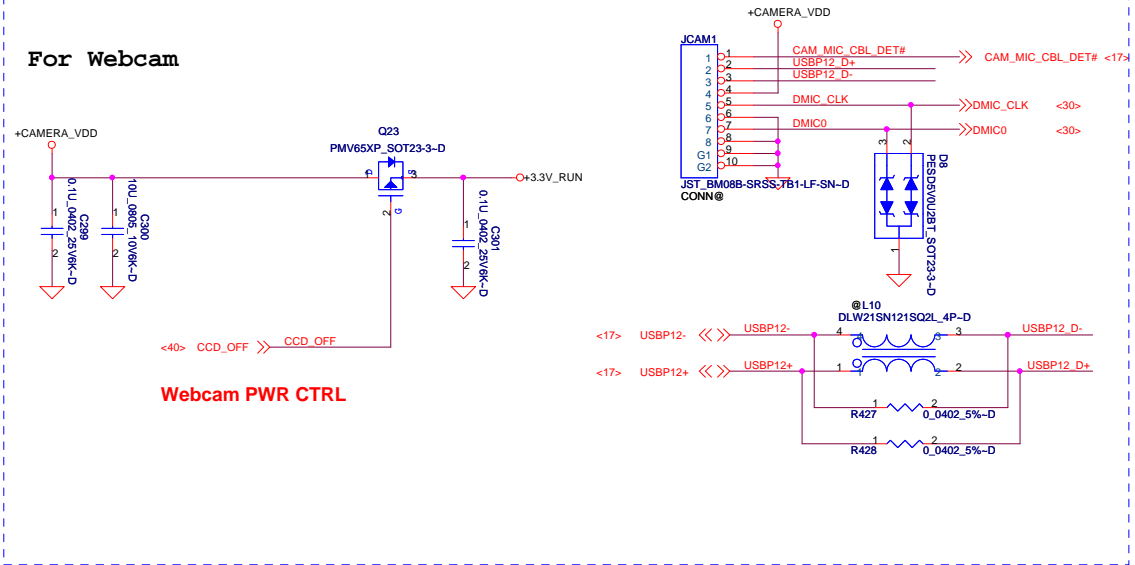
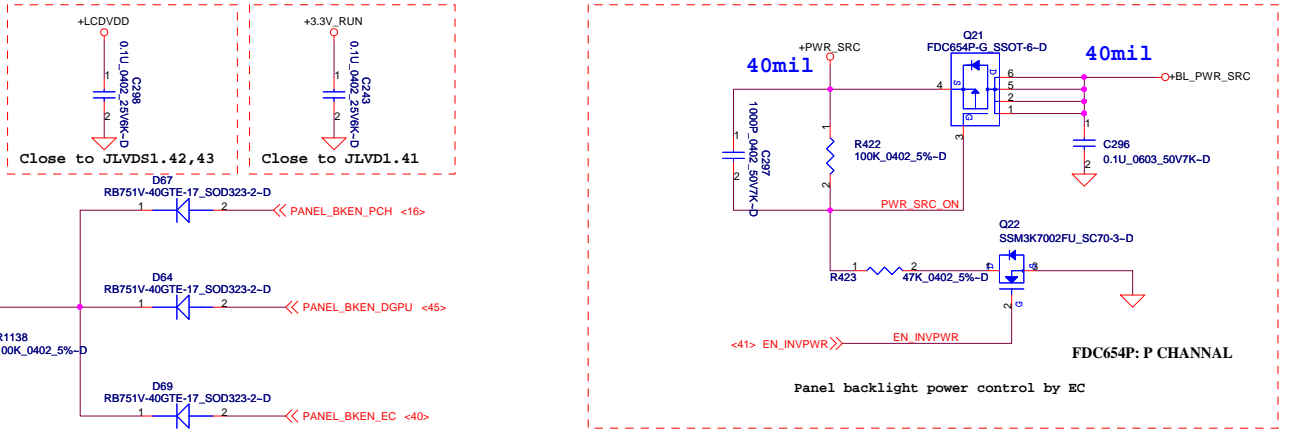
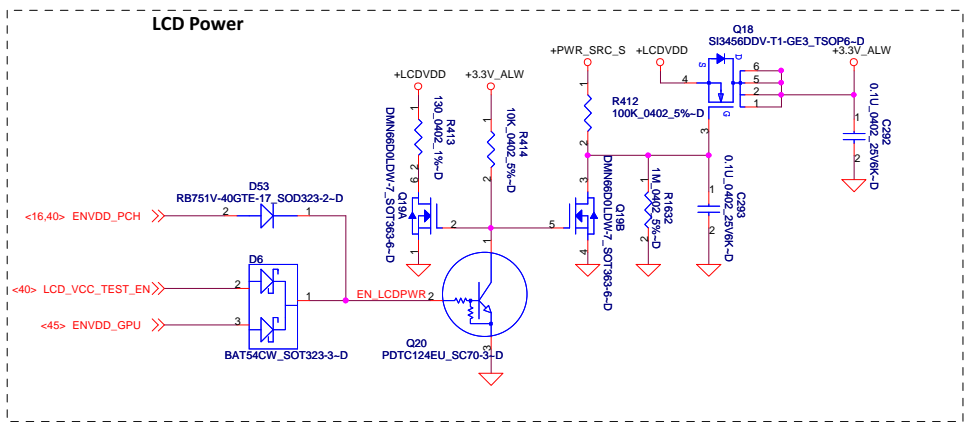
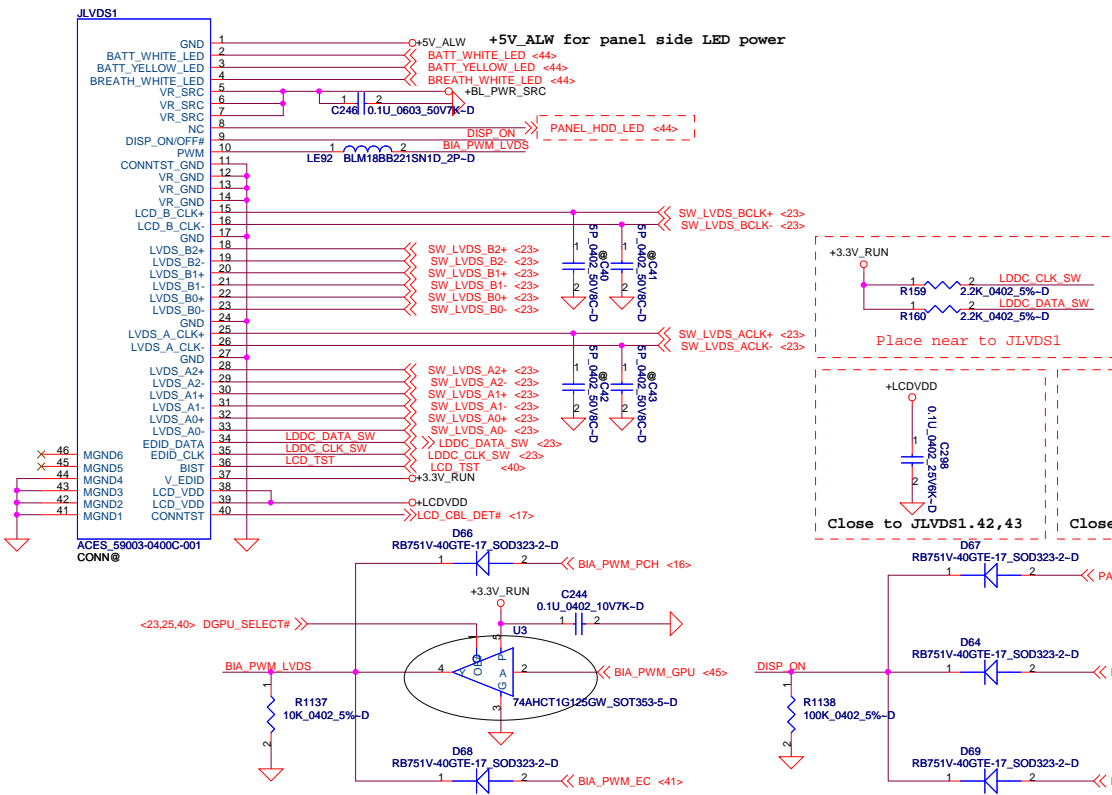


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Title			LVD SW		
Size	Document Number				Rev
	LA-7782				0.1
Date:	Friday, June 10, 2011	Sheet	23	of	66

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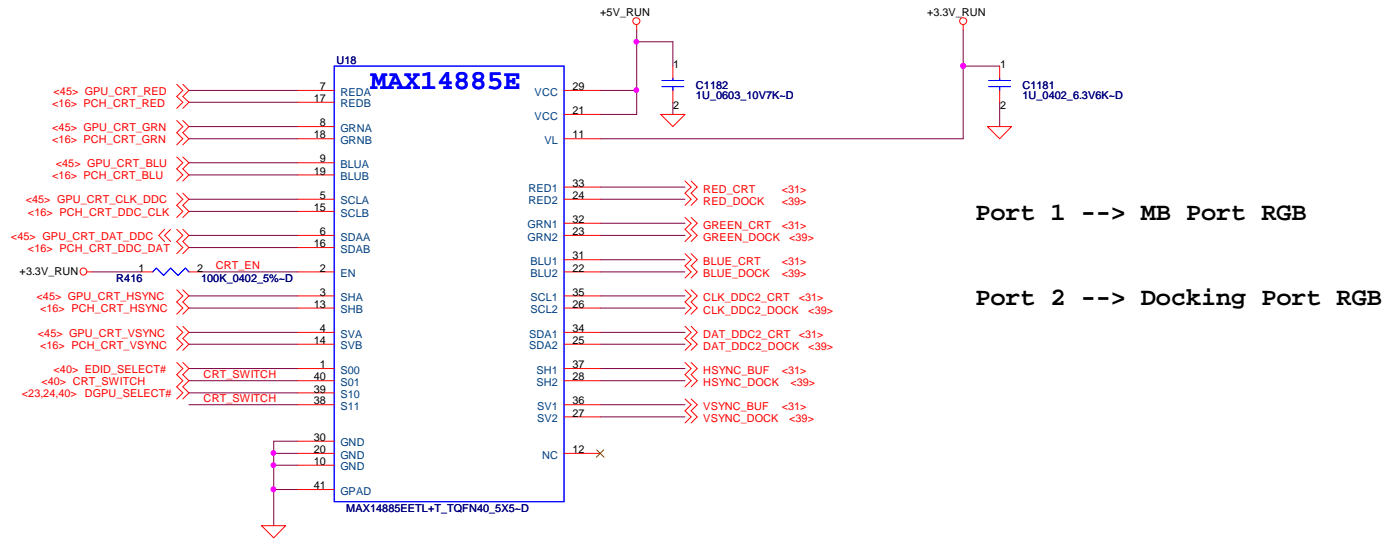
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eDP & CAM & TS Conn			
LA-7782			
Date:	Friday, June 10, 2011	Sheet	24 of 66
Rev	0.1		

Channel A --> GPU

Channel B --> PCH



Port 1 --> MB Port RGB

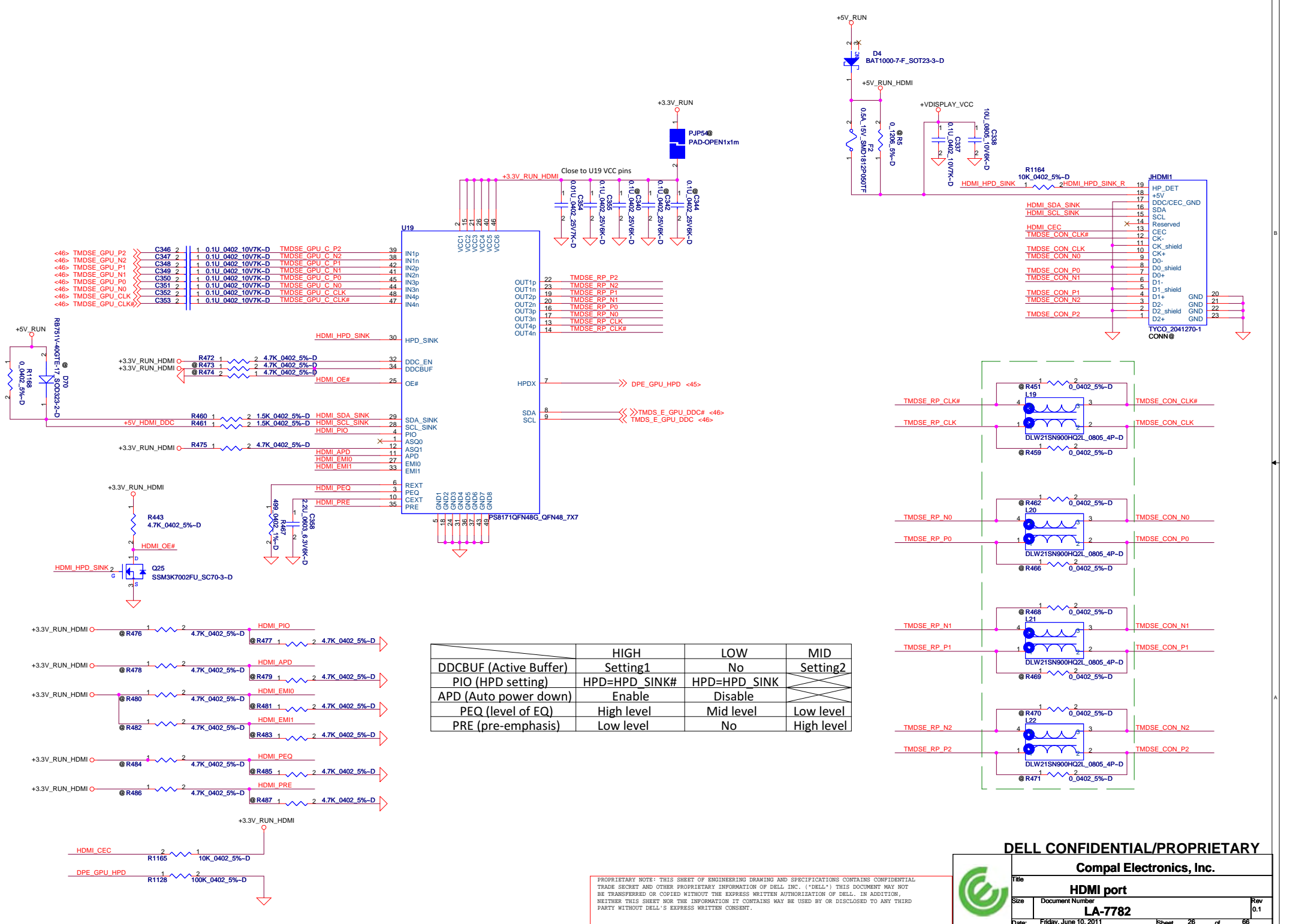
Port 2 --> Docking Port RGB

CRT_SWITCH	0	0	1	1
DGPU_SELECT#	0	1	0	1
EDID_SELECT#	0	1	0	1
	A --> Port 1	B --> Port 1	A --> Port 2	B --> Port 2

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CRT/Video switch			
Title	Document Number		
Size	LA-7782		Rev 0.1
Date: Friday, June 10, 2011	Sheet 25	of 66	

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	HIGH	LOW	MID
DDCBUF (Active Buffer)	Setting1	No	Setting2
PIO (HPD setting)	HPD=HPD_SINK#	HPD=HPD_SINK	
APD (Auto power down)	Enable	Disable	
PEQ (level of EQ)	High level	Mid level	Low level
PRE (pre-emphasis)	Low level	No	High level

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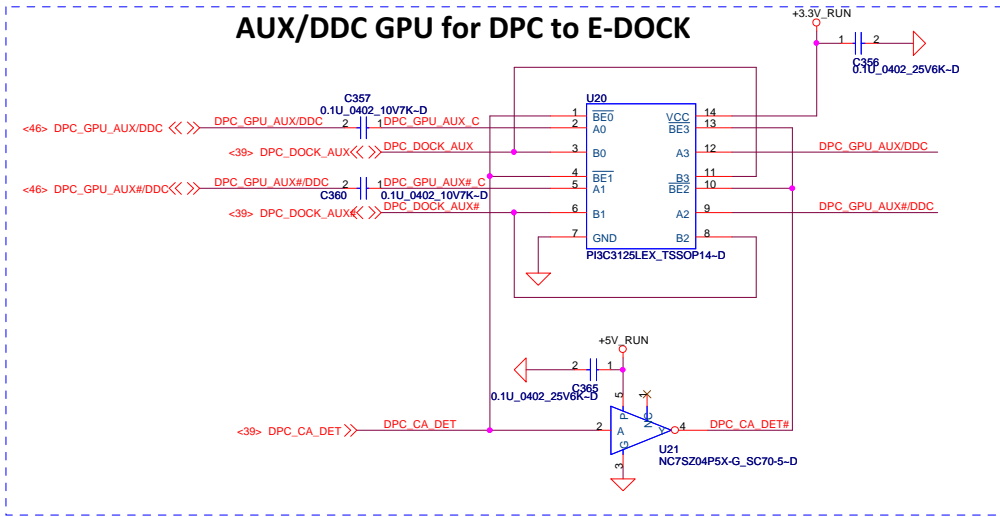
HDMI port

LA-7782

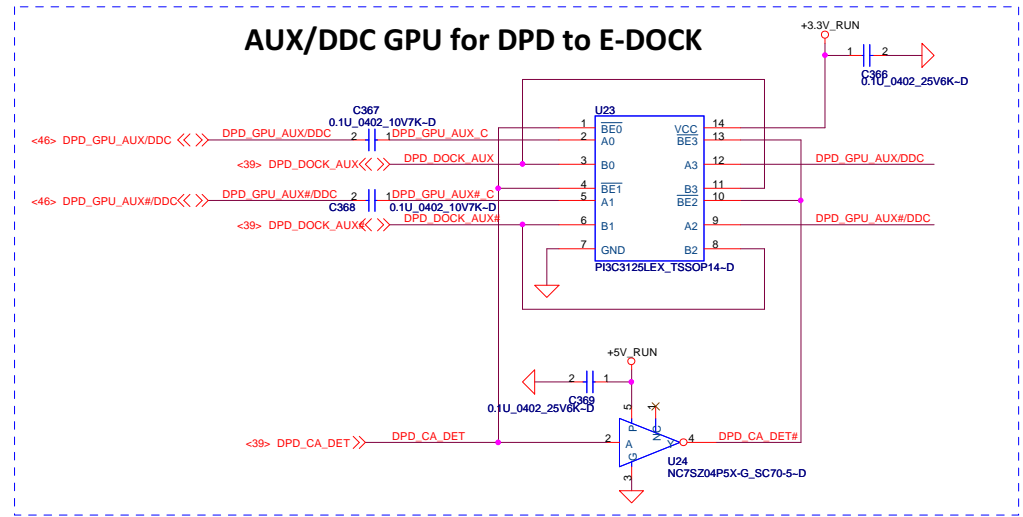
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		0.1
Date:	Friday, June 10, 2011	Sheet 26 of 66

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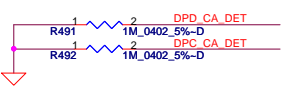
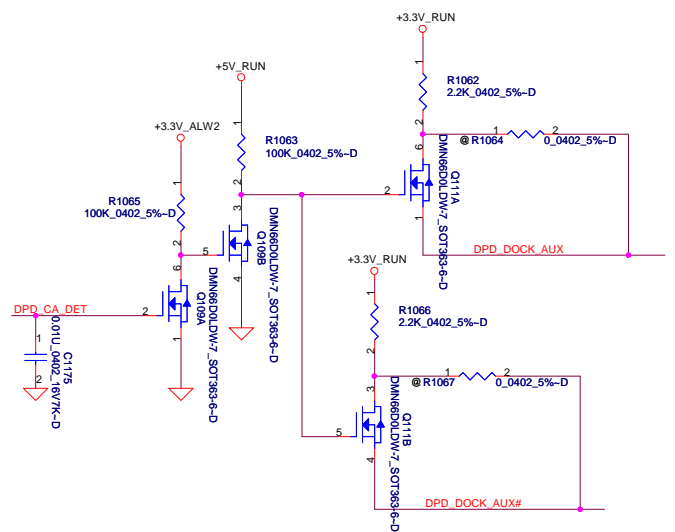
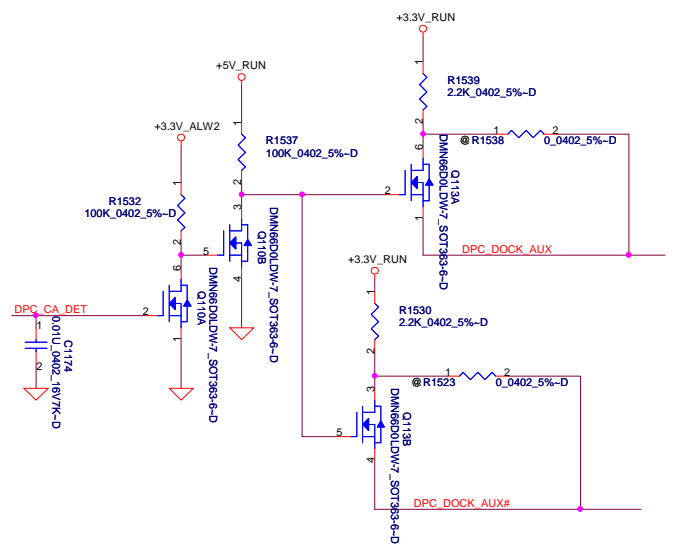
AUX/DDC GPU for DPC to E-DOCK



AUX/DDC GPU for DPD to E-DOCK



There is a new die for PI3C3125. Sample available on May.

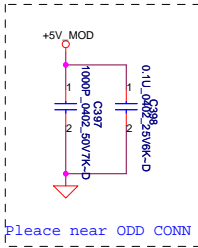
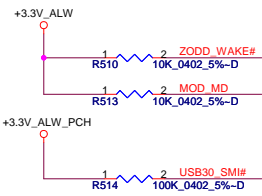


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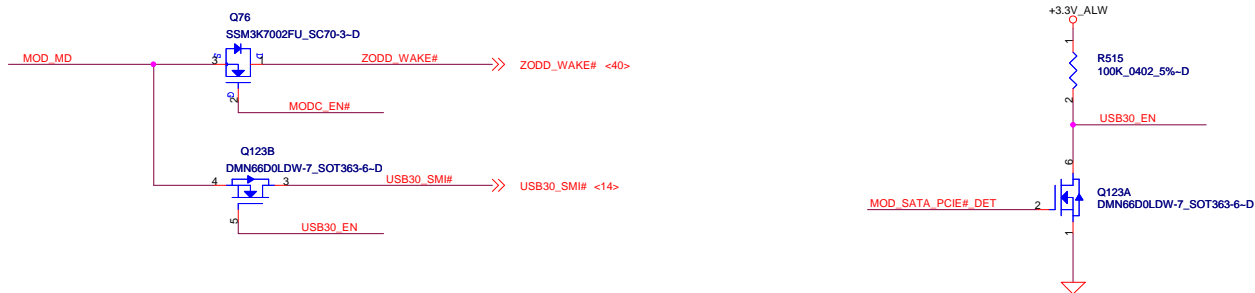
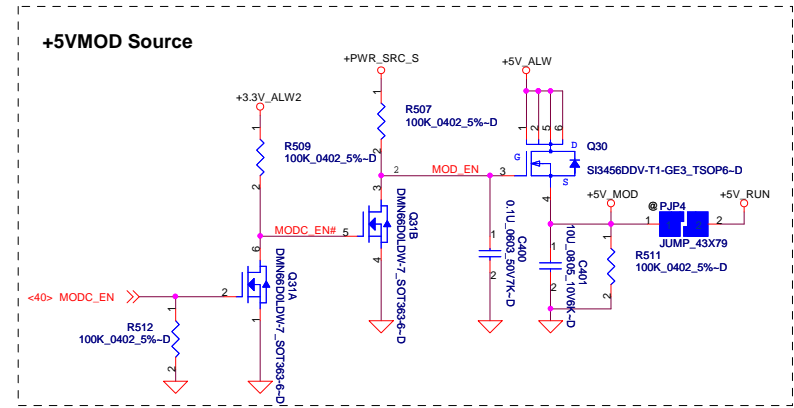
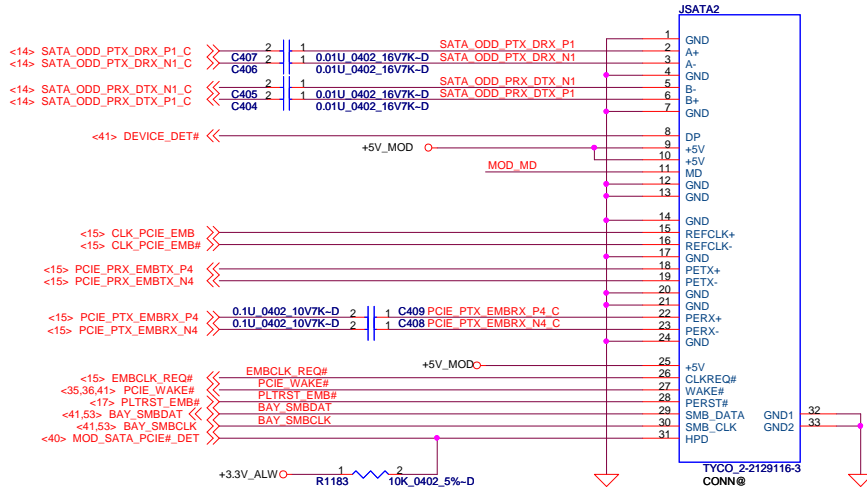
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DP AUX SW			
File			
Size	Document Number	Rev	
	LA-7782	0.1	
Date:	Friday, June 10, 2011	Sheet	27 of 66

For ODD



place near ODD CONN



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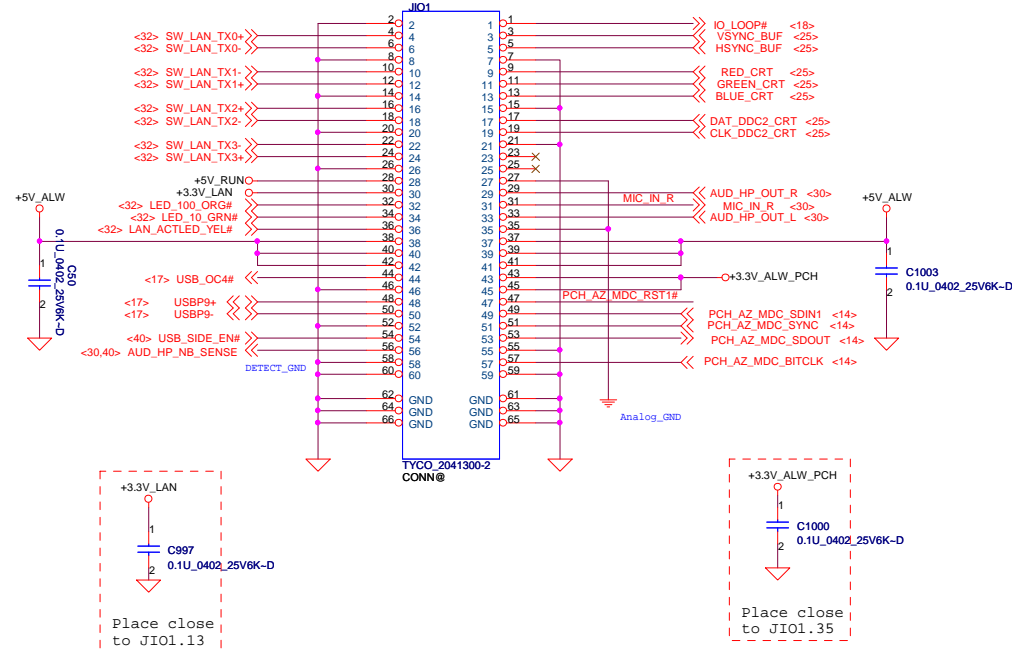
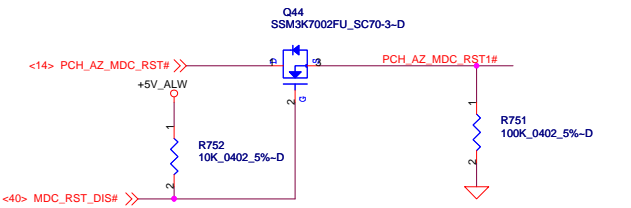
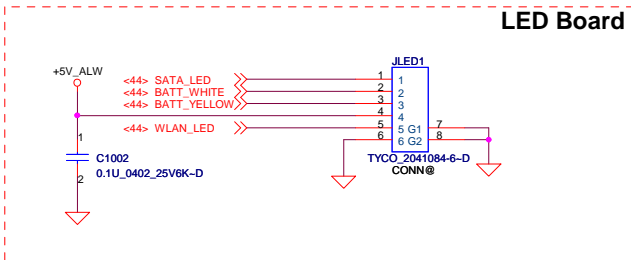
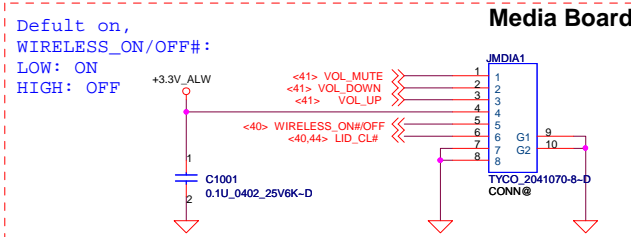
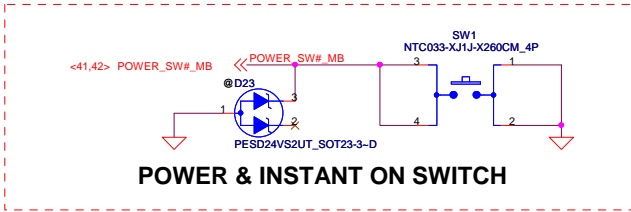
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Title: **ODD CONNECTOR**
 Size: Document Number
 Date: Friday, June 10, 2011

Rev: 0.1
 LA-7782
 Sheet 29 of 66

I/O board CONN.

Change to TYCO_2041300-2_60P-T and Horizontal reverse to SSI



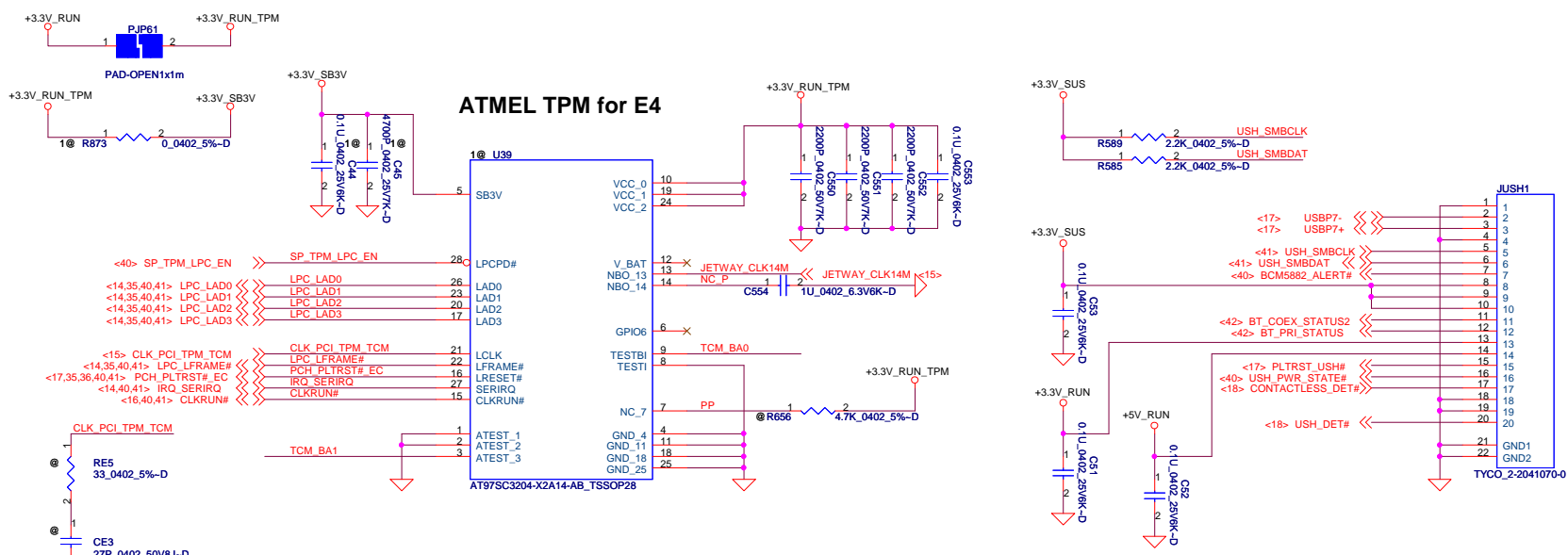
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Title: **PWR SW/Sub-board Connector**

Size: **LA-7782** Rev: **0.1**

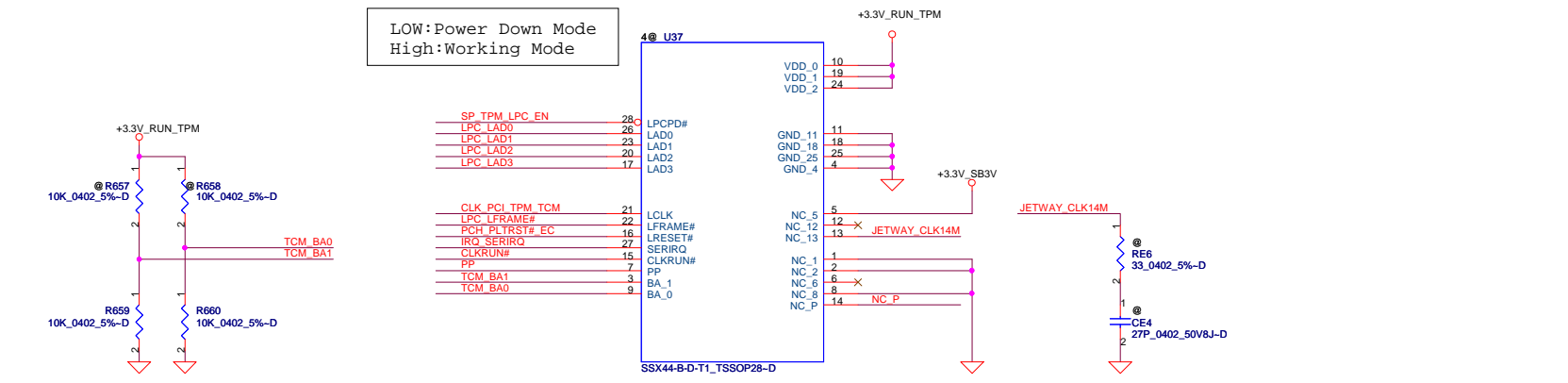
Date: **Friday, June 10, 2011** Sheet: **31** of **66**



Co-lay U37 and U38
LPC layout: Place TCM first and then end LPC with TPM.

China TCM: NationZ & Jetway co-lay

LOW:Power Down Mode
 High:Working Mode



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Title: **USH conn/TPM**

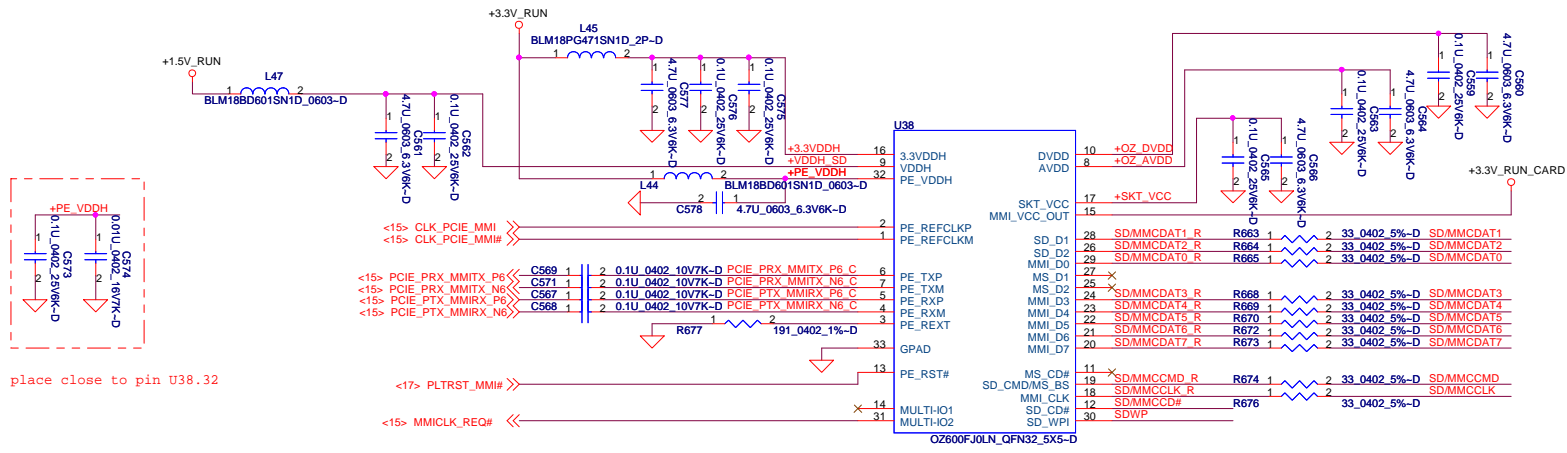
Size: **LA-7782**

Document Number: **LA-7782**

Date: **Friday, June 10, 2011**

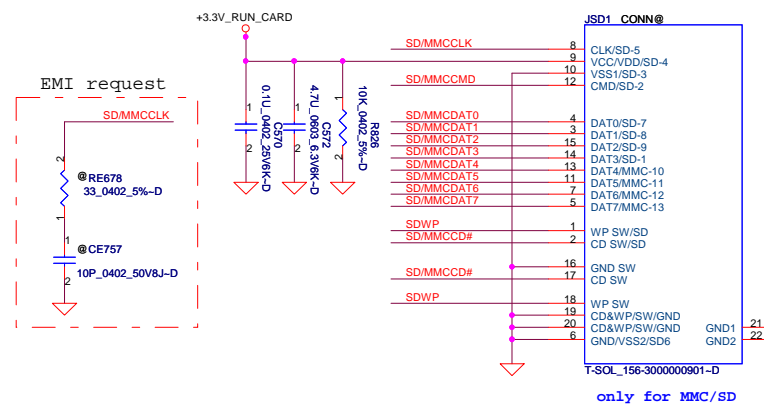
Rev: **0.1**

Sheet: **33** of **66**



place close to pin U38.32

Note: The trace need to route as daisy-chain and the trace of SD signals need to route as short as possible



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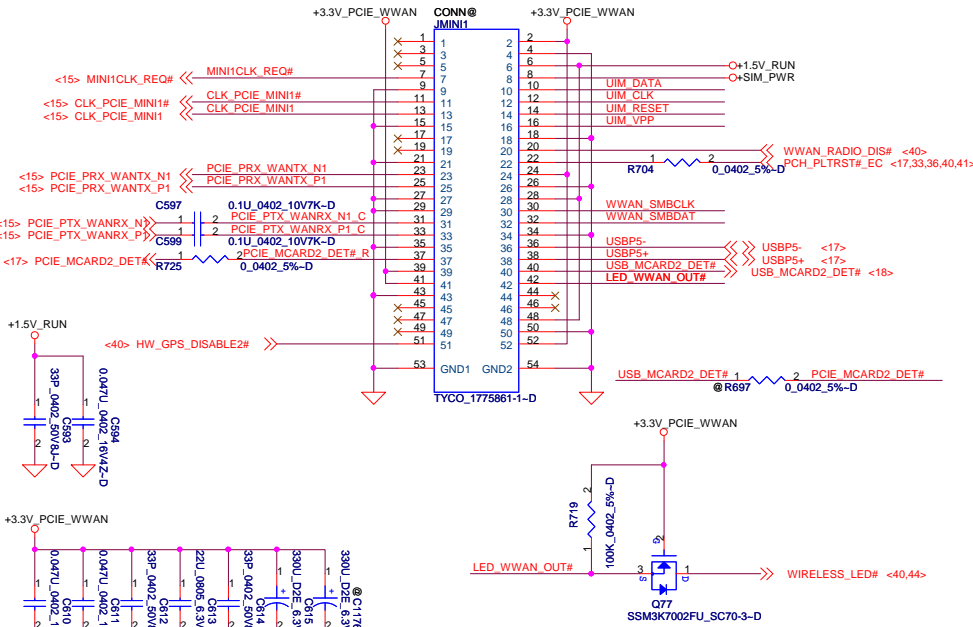
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Card Reader OZ600FJ0

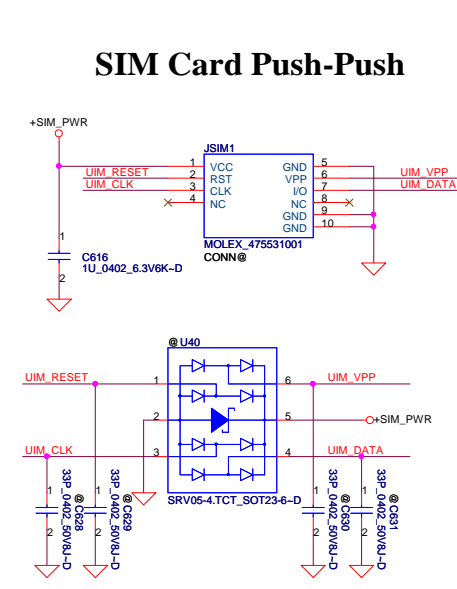
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 Size: _____ Document Number: **LA-7782** Rev: **0.1**
 Date: **Friday, June 10, 2011** Sheet: **34** of **66**



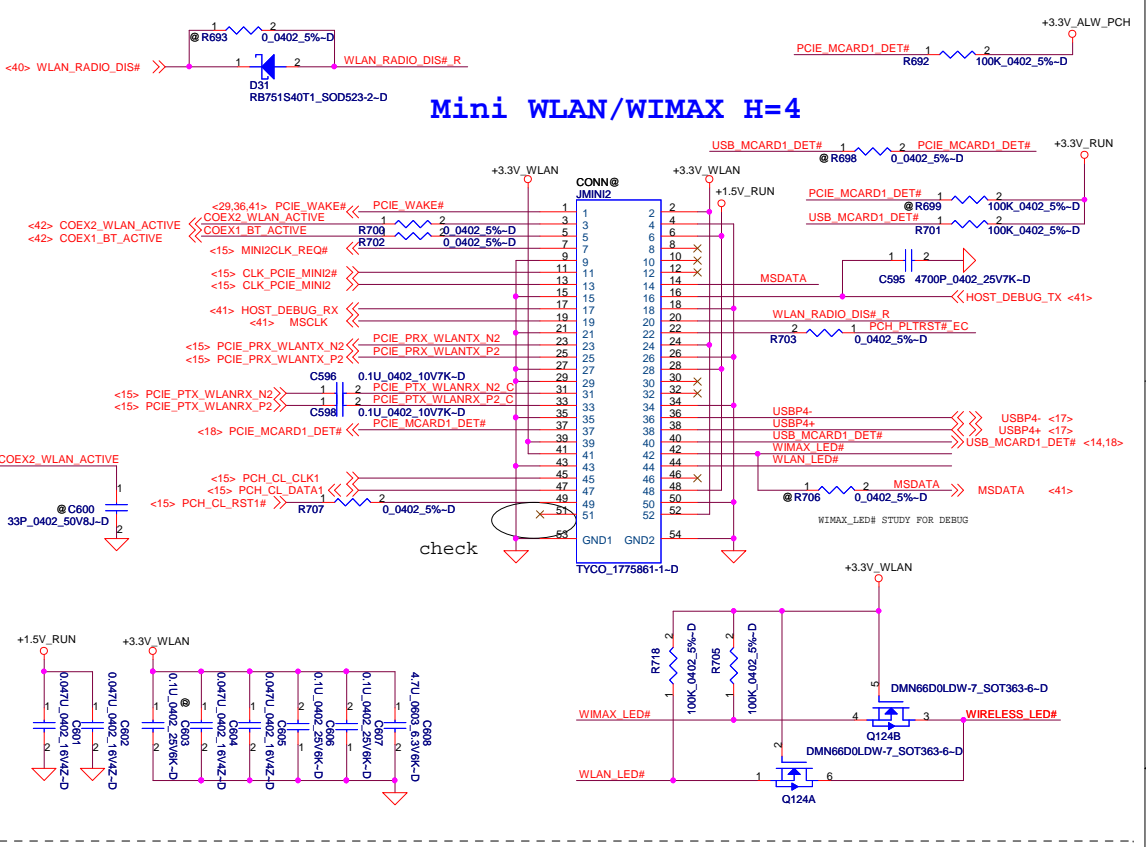
Mini WWAN/GPS/LTE H=5.2



SIM Card Push-Push

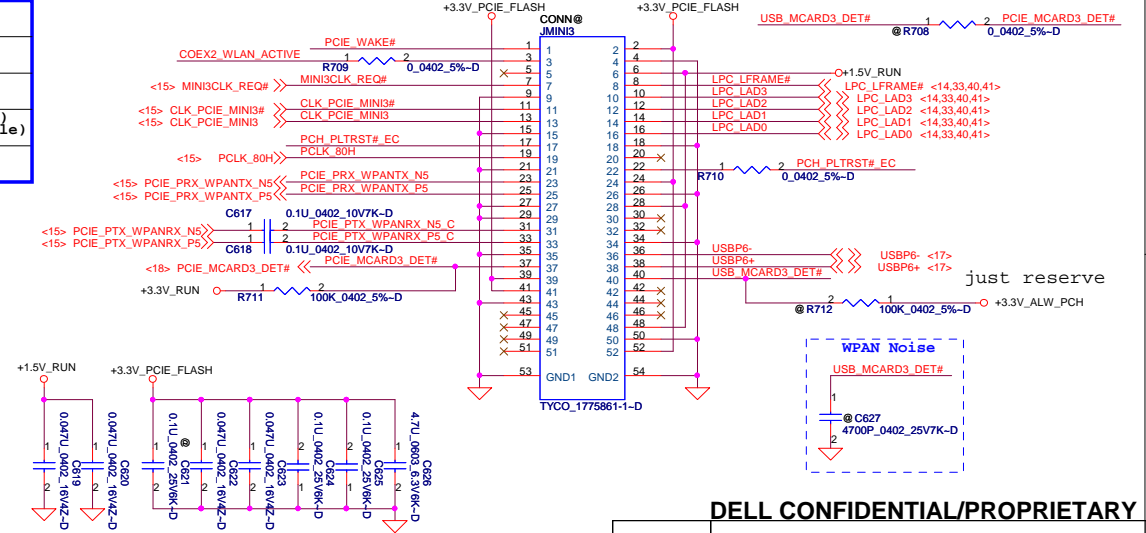


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+ -9%	1000	750	
+3.3Vaux	+ -9%	330	250 (Wake enable) 5 (Not wake enable)	
+1.5V	+ -5%	500	375	NA



Mini WLAN/WIMAX H=4

1/2 Minicard Pink Pather/60GHZ Card H=4



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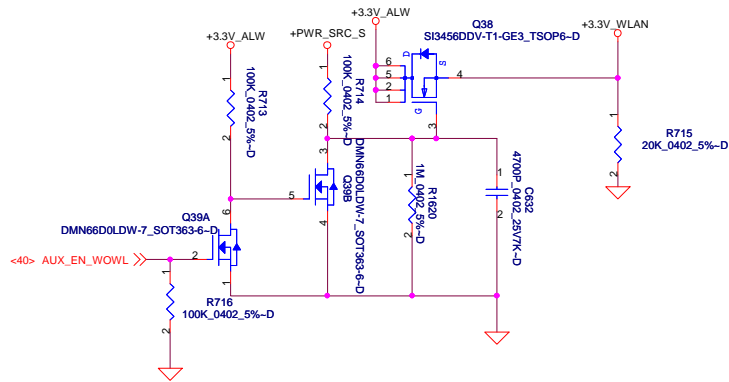
Mini Card

LA-7782

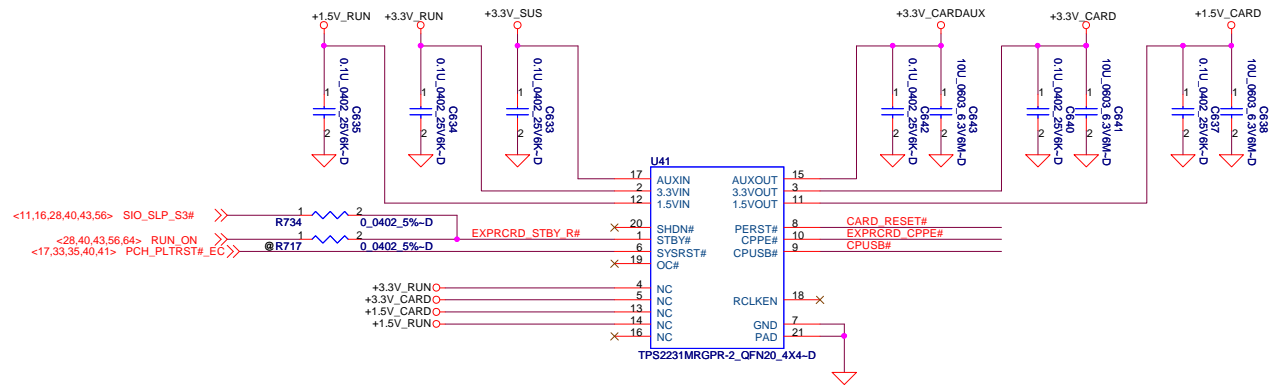
Friday, June 10, 2011

Sheet 35 of 66

Power Control for Mini card2

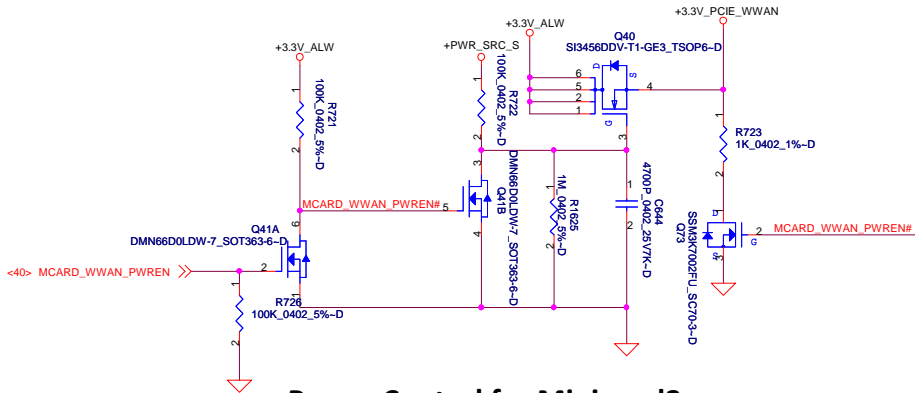


Express Card PWR S/W

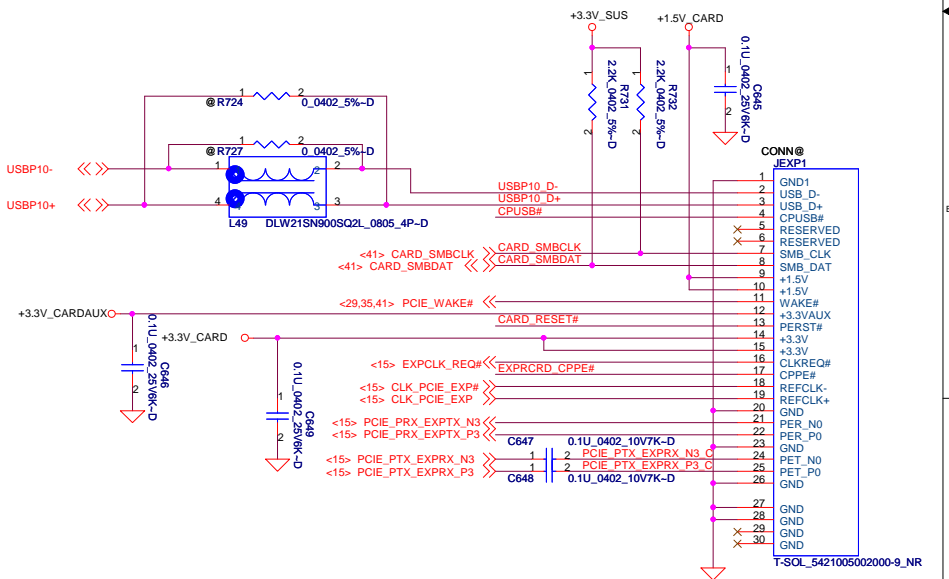


[Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part]

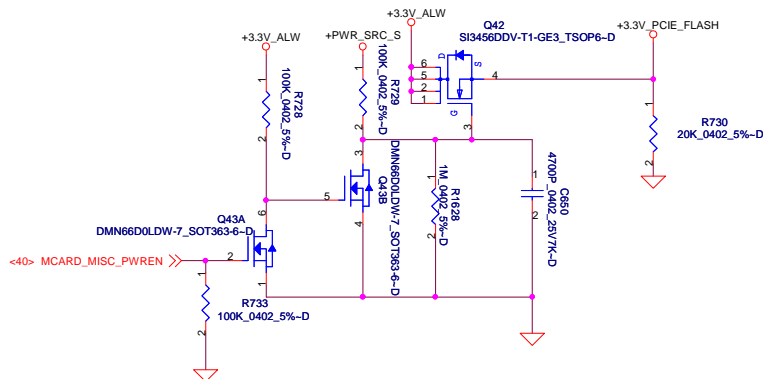
Power Control for Mini card1



Express Card Conn.



Power Control for Mini card3



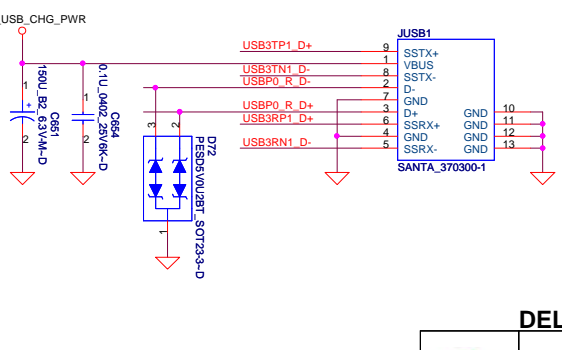
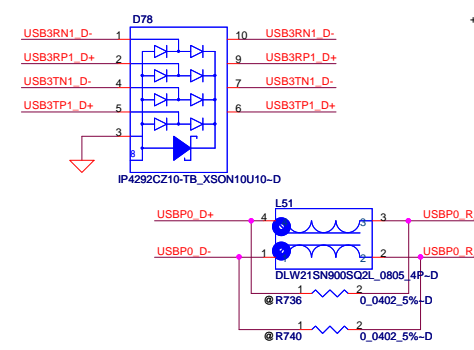
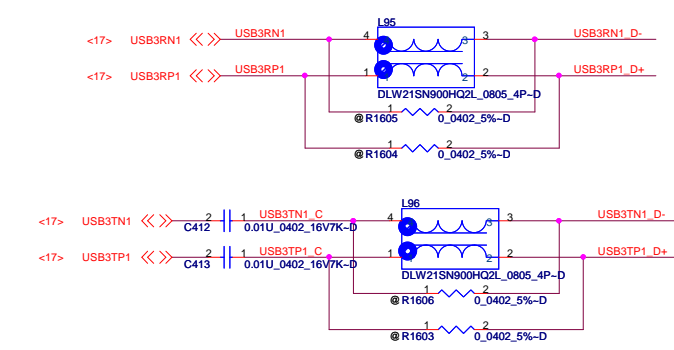
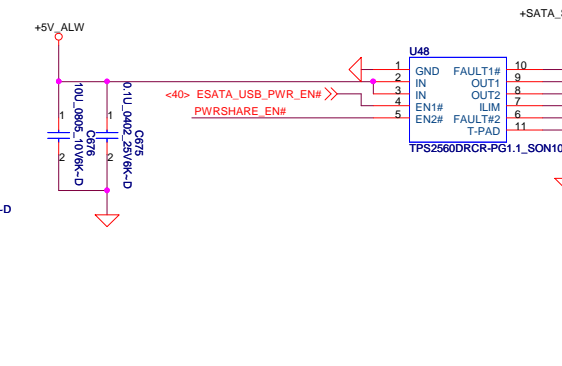
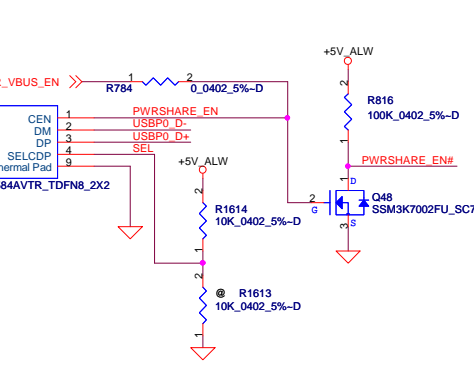
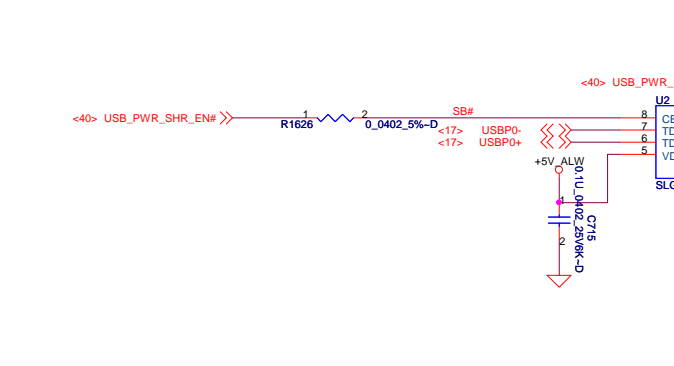
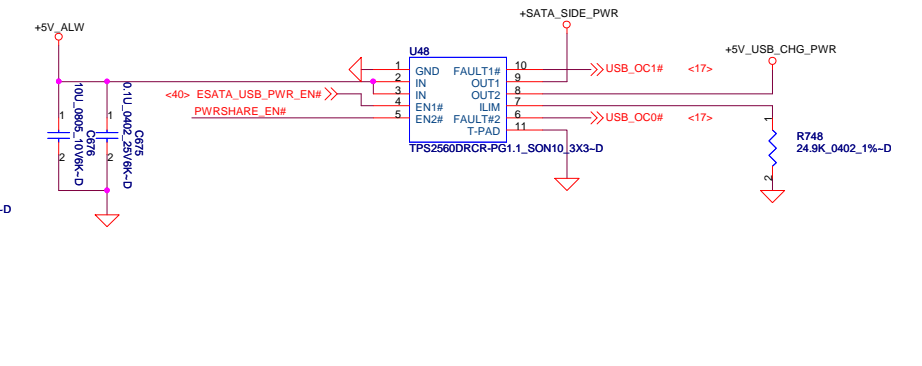
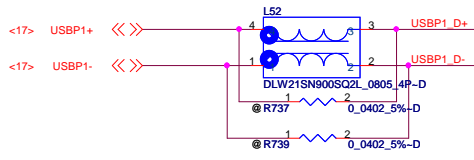
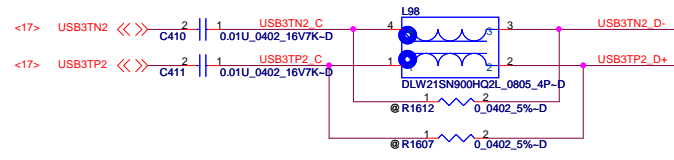
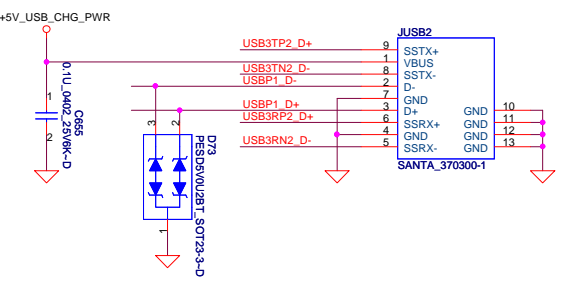
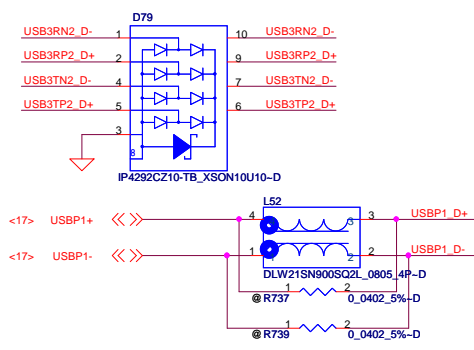
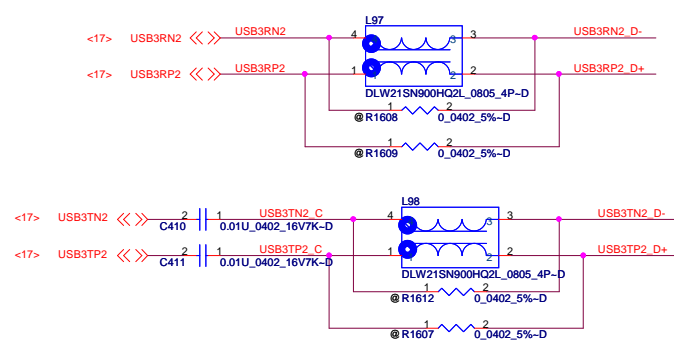
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Title		PCIE-SATA SW / PCIE PWR	
Size	Document Number	LA-7782	
Date	Friday, June 10, 2011	Sheet	36 of 66

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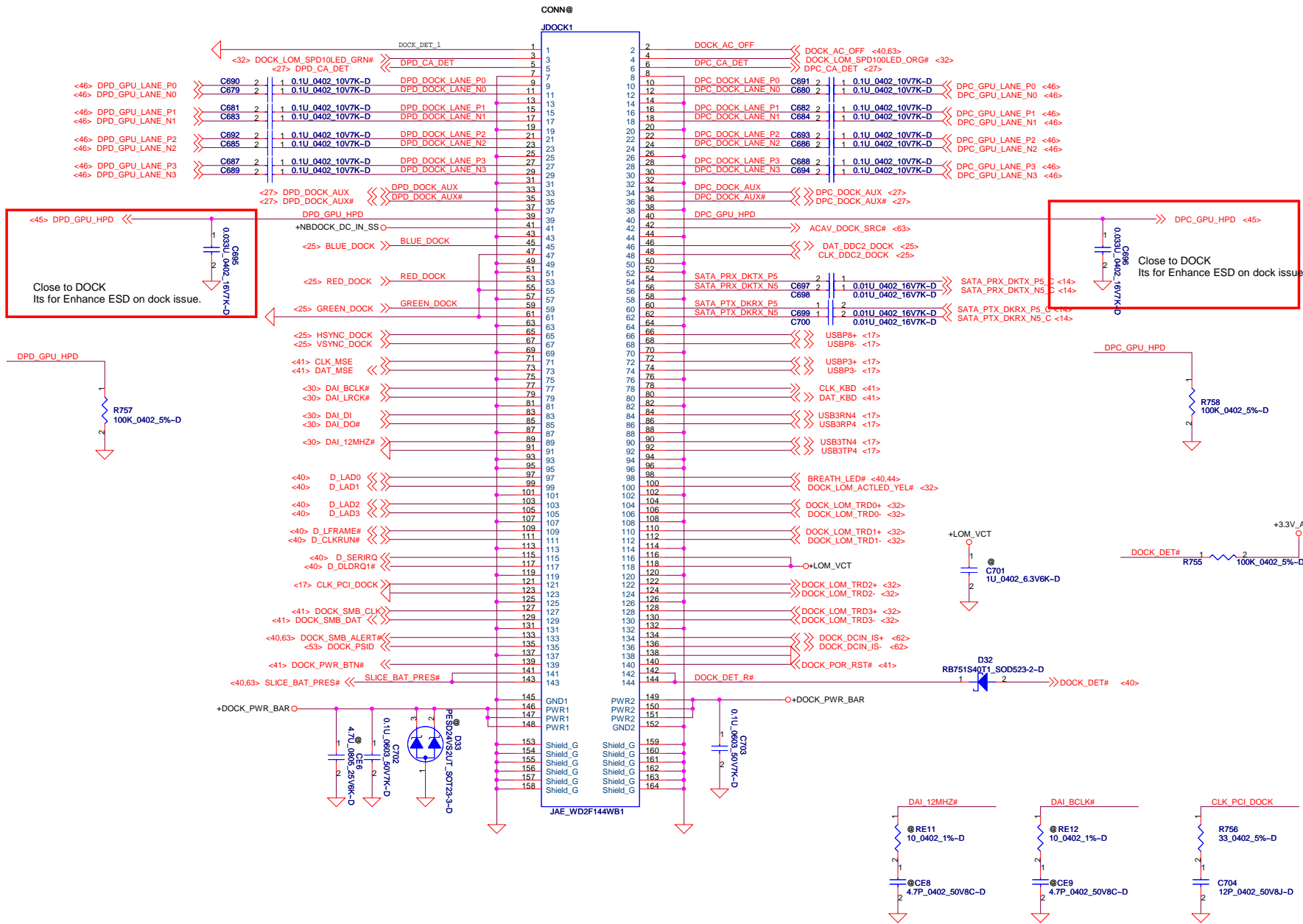
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Compal Electronics, Inc.

Title		USB x2	
Size	Document Number	LA-7782	
Date	Friday, June 10, 2011	Sheet	37 of 66

Rev 0.1



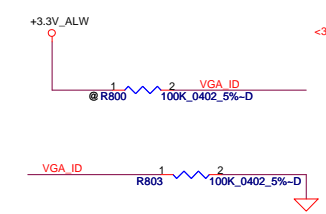
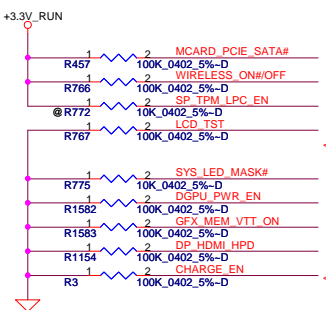
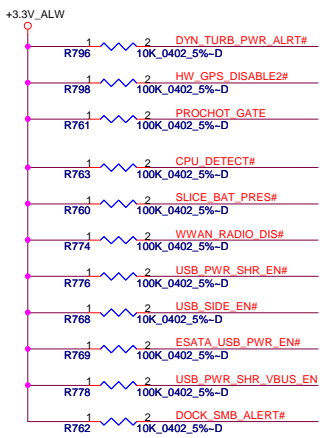
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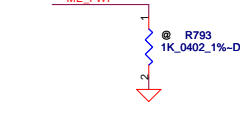


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Date			Rev		
Friday, June 10, 2011			0.1		
Sheet			of		
39			66		

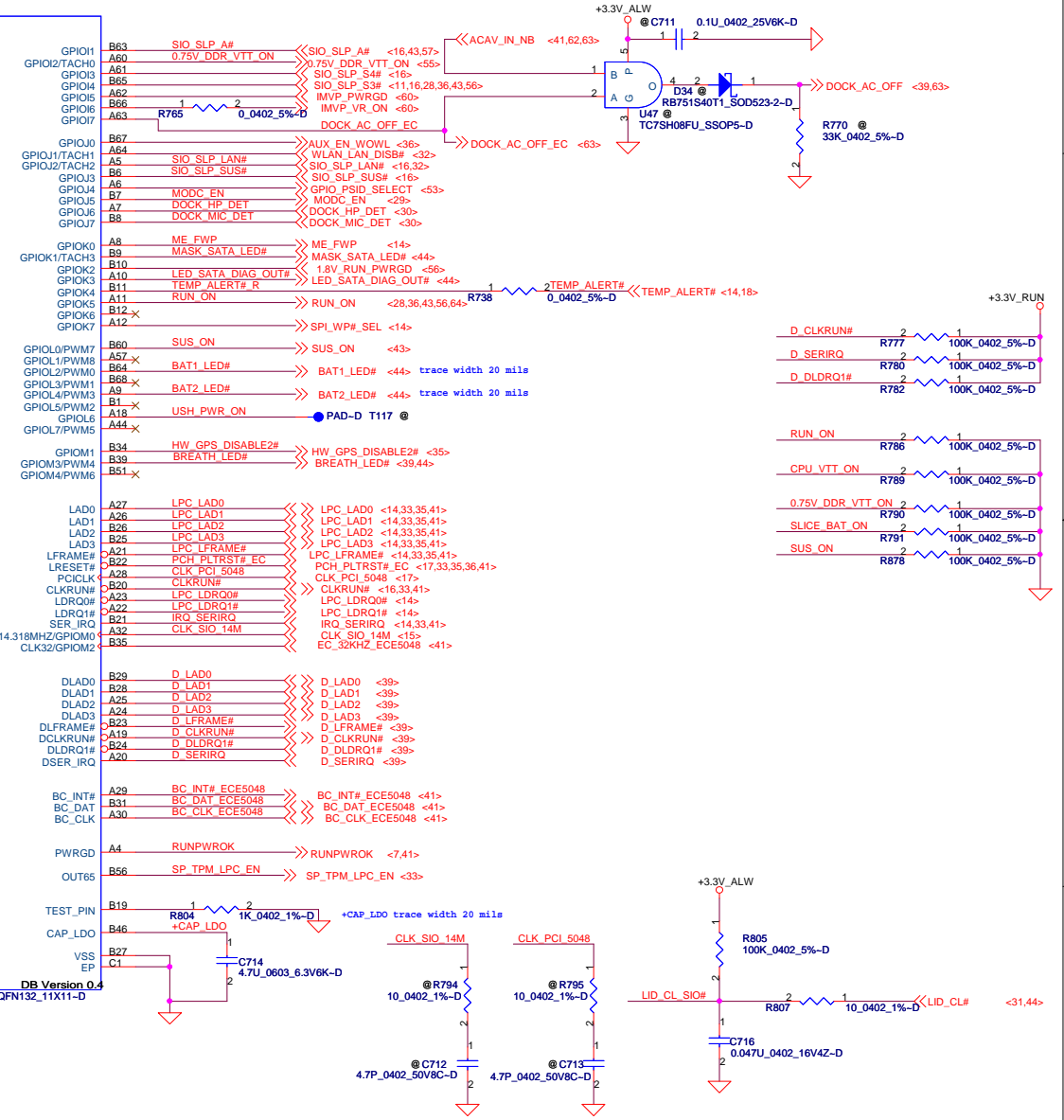


	VGA_ID0
Discrete	0
UMA	1

ME_FWP PCH has internal 20K PD.
(suspend power rail)



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- <31> MDC_RST_DIS# MCARD_MISC_PWREN B53
- <36> MCARD_MISC_PWREN PROC_HOT_GATE A50
- <62> PROC_HOT_GATE LID_CL_SIG# A51
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- <33> USH_PWR_STATE# EN_DOCK_PWR_BAR B37
- <63> EN_DOCK_PWR_BAR PANEL_BKEN_EC A35
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- <30> AUD_NB_MUTE# MCARD_WWAN_PWREN B42
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- <24> LCD_VCC_TEST_EN COD_OFF A41
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- <63> CHARGE_MODULE_BATT CHARGE_PBAT B16
- <63> CHARGE_PBAT DEFAULT_OVRDE A16
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- <45.64> DGPU_PWR_EN MOD_SATA_PCIE#_DET A42
- <29> MOD_SATA_PCIE#_DET DP_HDMI_HPD B4
- <29> ZODD_WAKE# BCM5882_ALERT# B62
- <33> BCM5882_ALERT# SUSACK# A58
- <16> SUSACK# EDID_SELECT# B61
- <25> EDID_SELECT# DGPU_PWROK A56
- <18.64> DGPU_PWROK VGA_ID A55
- <15.49> 3.3V_RUN_GFX_ON 3.3V_RUN_GFX_ON A55
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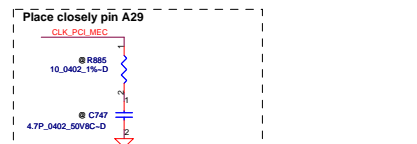
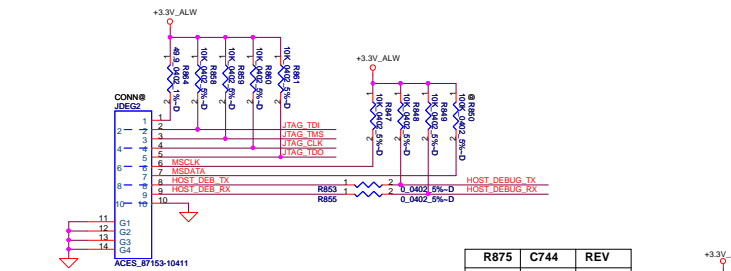
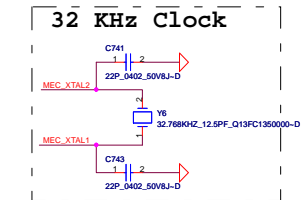
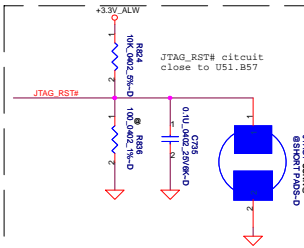
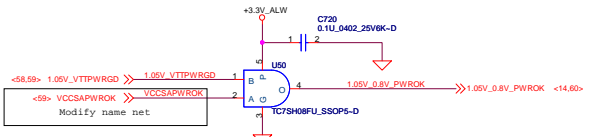


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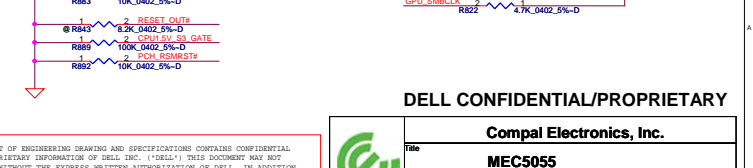
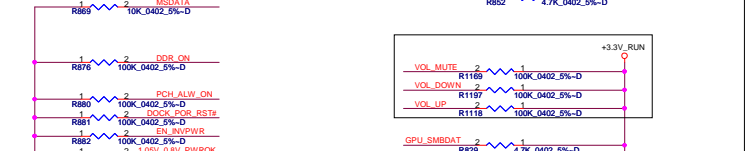
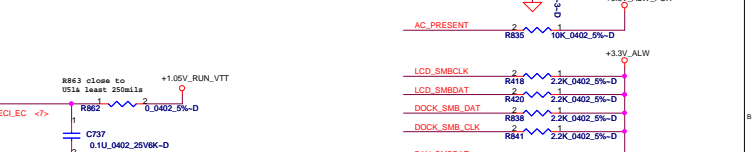
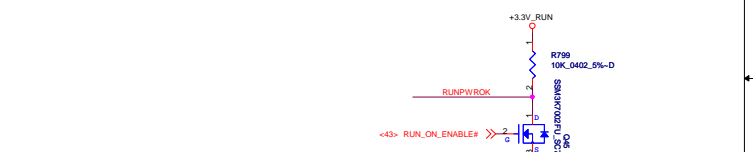
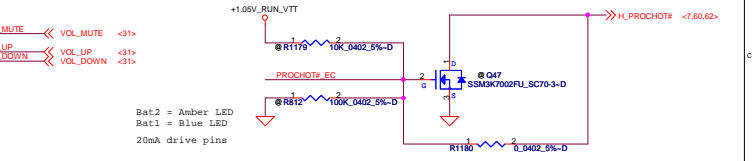
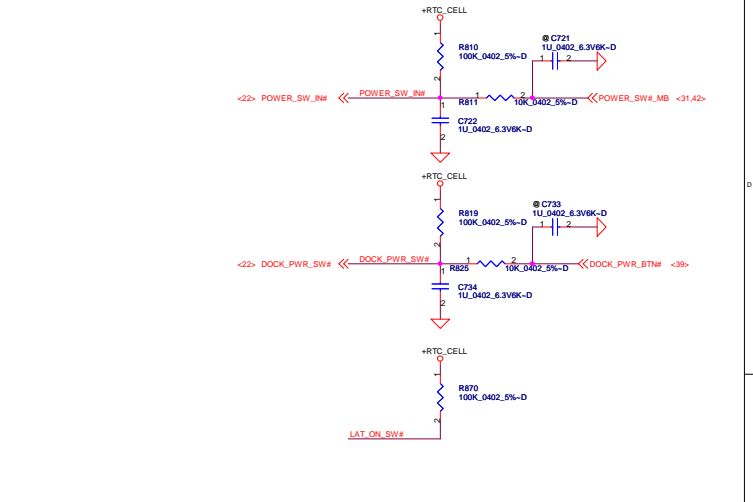
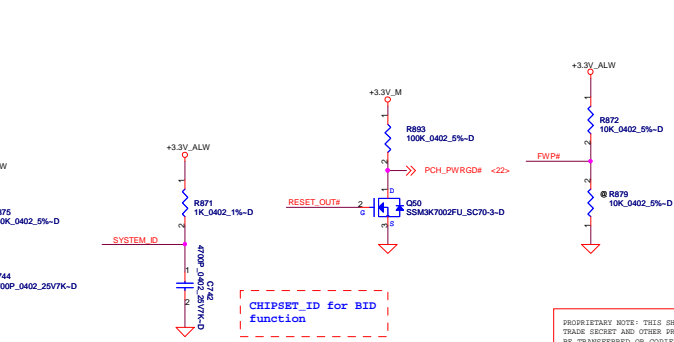
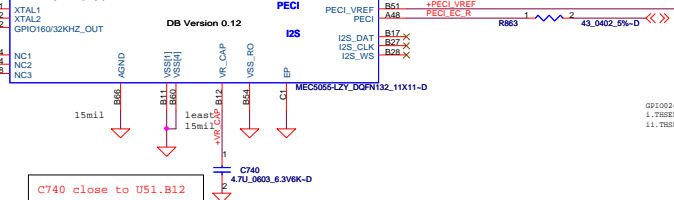
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Compal Electronics, Inc.		
Title ECE5048		
Size	Document Number LA-7782	Rev 0.1
Date	Friday, June 10, 2011	Sheet 40 of 66



R875	C744	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
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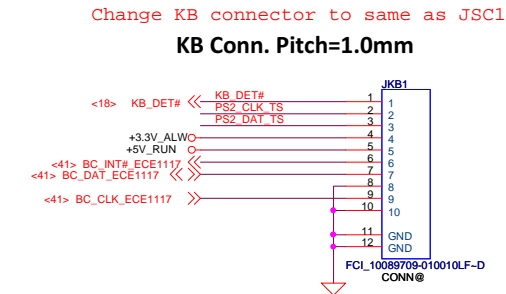
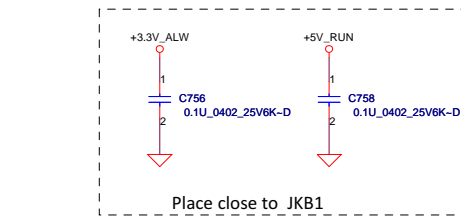
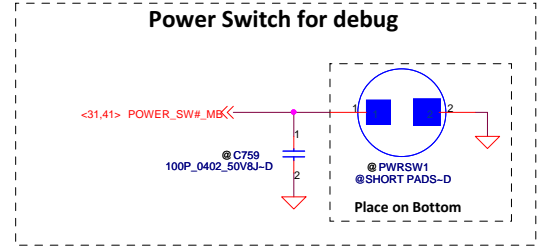
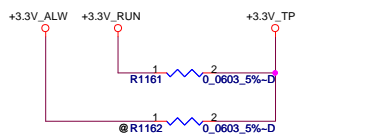
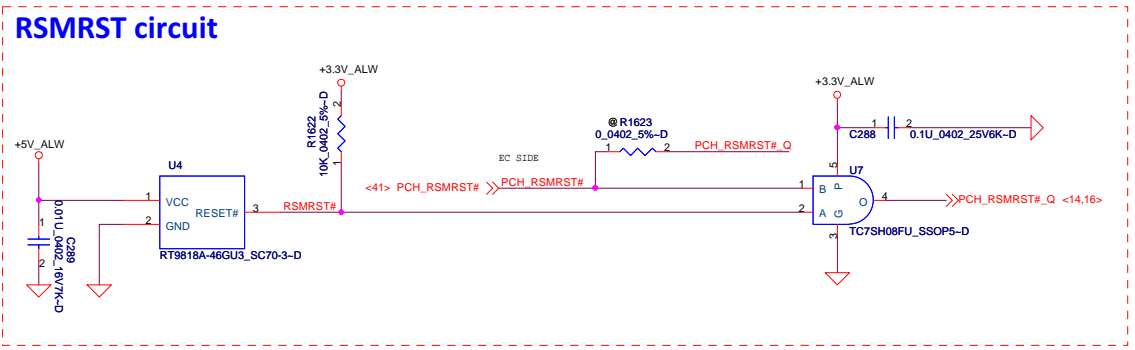
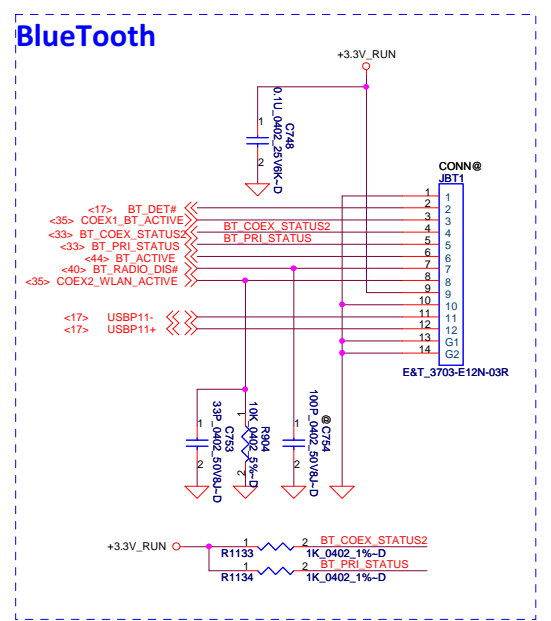
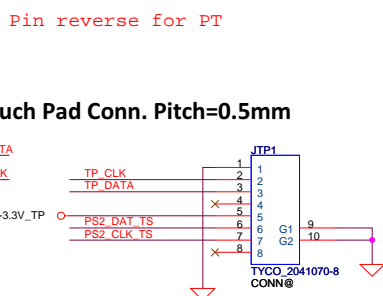
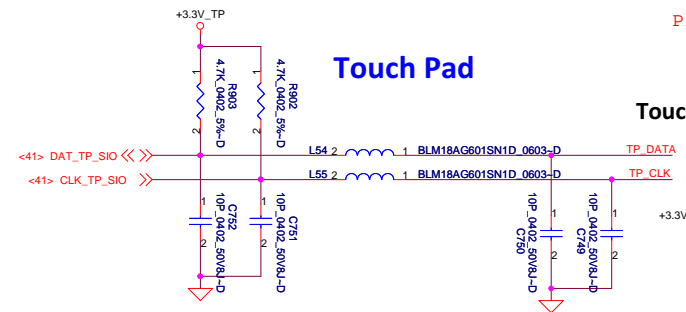
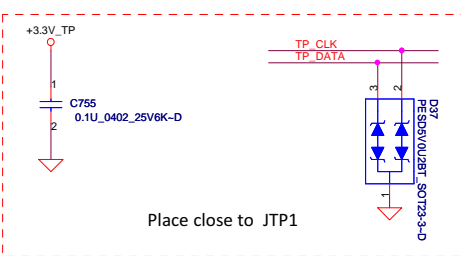
BOARD_ID rise time is measured from 5%~68%.



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 Part Number: **MEC5055**
 Title: **LA-7782**
 Date: **Friday, June 10, 2011**

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@ LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET 2.5X MB-LCD 14 WXGA+(1-lch)

@ RTC BATT

Part Number	Description
GC20323M0X0	BATT CR2032 3V 220MAH MAXELL

@ FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@ Speak

Part Number	Description
PK230003Q0L	SPK PACK 2.5X 2.0W 4 OHM FG

@ LED Board FFC

Part Number	Description
NBX0000RFP0L	FFC 6P H P1 PAD=0.7 87.4MM MB-LED/B 0PFD

@ MEDIA Board FFC

Part Number	Description
NBX0000RS0L	FFC 12P G P.5 PAD.3 75MM MB-VOLUME/B 0PFD

@ LVDS cable

Part Number	Description
DC02C00180L	H-CONN SET 0PFD MB-LCD CAM LED 2CHANNEL

@ UMA DC IN wire cable

Part Number	Description
DC30100BN0	CONN SET 0PFD DCJACK-MB NMD-DCE30004-0P

@ Battery bridge cable

Part Number	Description
DC020014210	H-CONN SET 0PFD H/B-BATTERY 9PIN

@ MDC wire set cable

Part Number	Description
DC03100RL0L	CONN SET 0PFD MDC-RJ11

@ T/P FFC

Part Number	Description
NBX0000RR0L	FFC 8P F PD.5 PAD=0.3 136MM MB-TP/B 0PFD

@ KB FFC

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

@ BT wire cable

Part Number	Description
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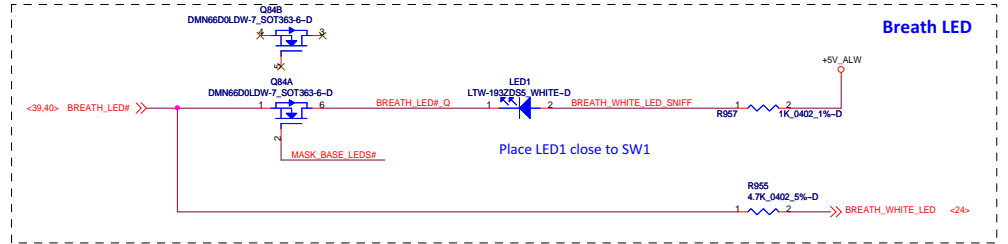
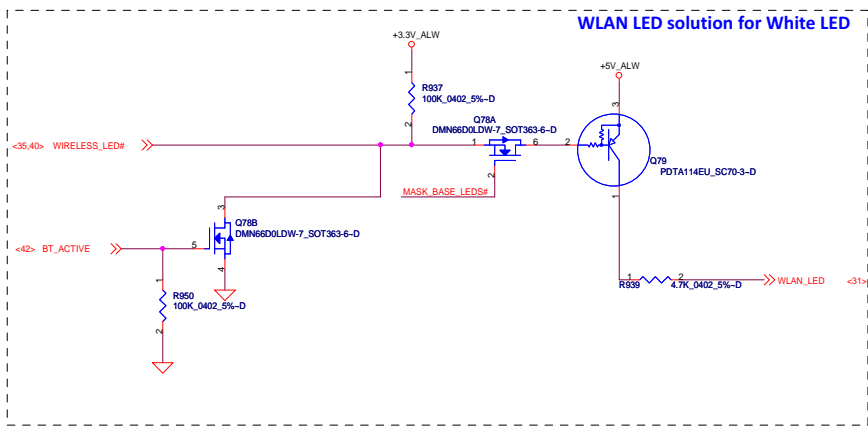
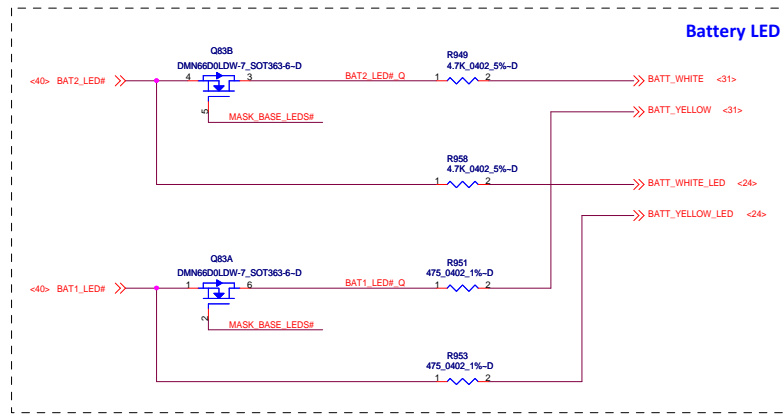
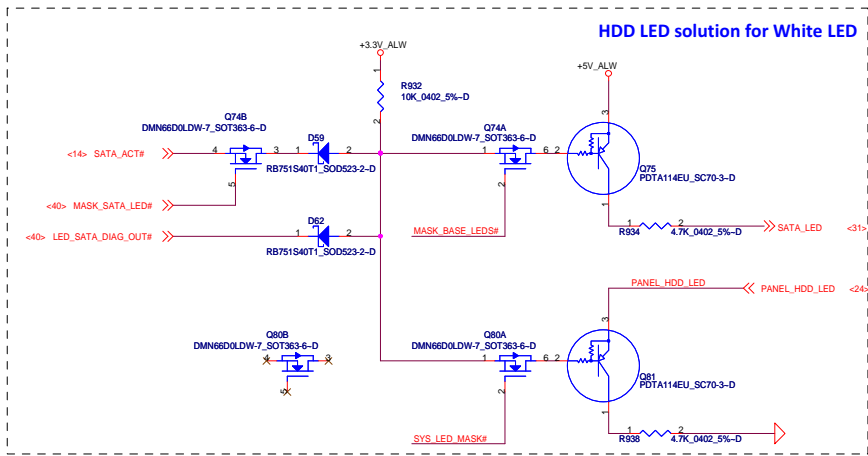
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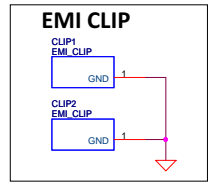
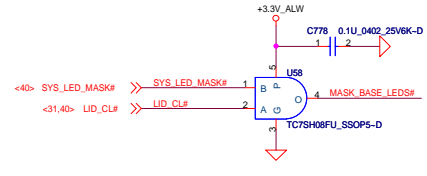
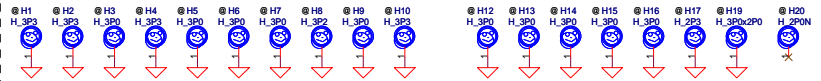
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	LA-7782	0.1	
Date:	Friday, June 10, 2011	Sheet	42 of 66

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- Fiducial Mark**
- FD1
 - FIDUCIAL MARK-D
 - FD2
 - FIDUCIAL MARK-D
 - FD3
 - FIDUCIAL MARK-D
 - FD4
 - FIDUCIAL MARK-D

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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PAD and Standoff

LA-7782

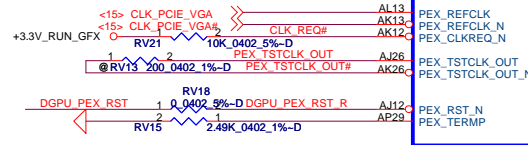
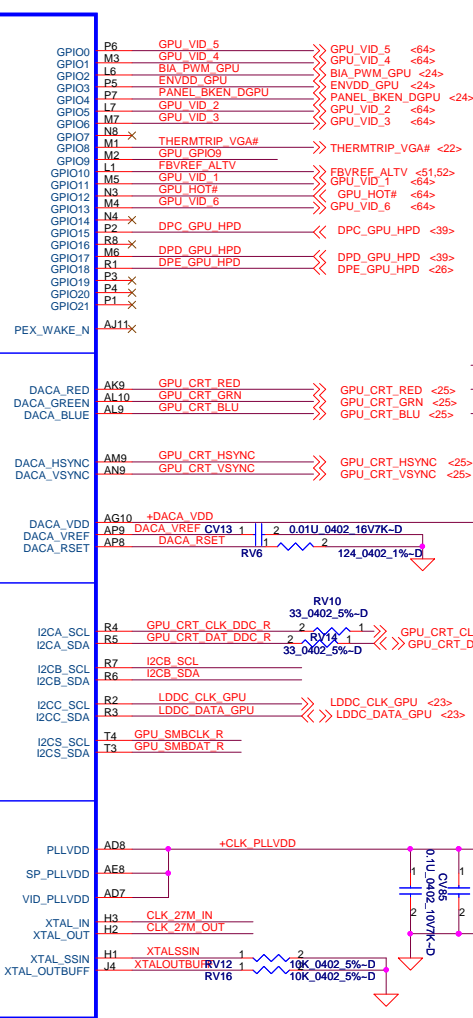
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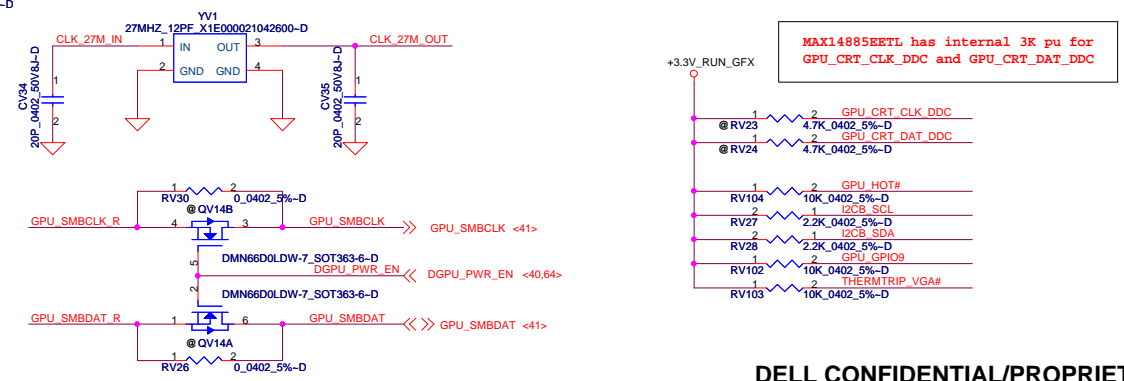
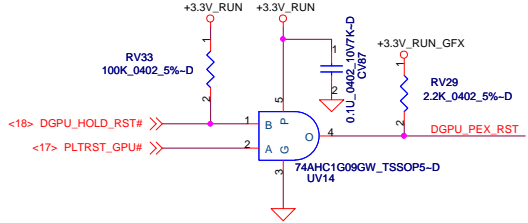
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PEG_CTX_GRX_P8	AP20	PEX_RX8
PEG_CTX_GRX_N8	AP20	PEX_RX8_N
PEG_CTX_GRX_P9	AM21	PEX_RX9
PEG_CTX_GRX_N9	AM21	PEX_RX9_N
PEG_CTX_GRX_P10	AN23	PEX_RX10
PEG_CTX_GRX_N10	AN23	PEX_RX10_N
PEG_CTX_GRX_P11	AP23	PEX_RX11
PEG_CTX_GRX_N11	AP23	PEX_RX11_N
PEG_CTX_GRX_P12	AN24	PEX_RX12
PEG_CTX_GRX_N12	AN24	PEX_RX12_N
PEG_CTX_GRX_P13	AN26	PEX_RX13
PEG_CTX_GRX_N13	AN26	PEX_RX13_N
PEG_CTX_GRX_P14	AP26	PEX_RX14
PEG_CTX_GRX_N14	AP26	PEX_RX14_N
PEG_CTX_GRX_P15	AN27	PEX_RX15
PEG_CTX_GRX_N15	AN27	PEX_RX15_N
PEG_CRX_GTX_C_P0	AK14	PEX_TX0
PEG_CRX_GTX_C_N0	AH14	PEX_TX0_N
PEG_CRX_GTX_C_P1	AH14	PEX_TX1
PEG_CRX_GTX_C_N1	AG14	PEX_TX1_N
PEG_CRX_GTX_C_P2	AK15	PEX_TX2
PEG_CRX_GTX_C_N2	AH15	PEX_TX2_N
PEG_CRX_GTX_C_P3	AK16	PEX_TX3
PEG_CRX_GTX_C_N3	AK16	PEX_TX3_N
PEG_CRX_GTX_C_P4	AK17	PEX_TX4
PEG_CRX_GTX_C_N4	AH17	PEX_TX4_N
PEG_CRX_GTX_C_P5	AH17	PEX_TX5
PEG_CRX_GTX_C_N5	AG17	PEX_TX5_N
PEG_CRX_GTX_C_P6	AK18	PEX_TX6
PEG_CRX_GTX_C_N6	AH18	PEX_TX6_N
PEG_CRX_GTX_C_P7	AH18	PEX_TX7
PEG_CRX_GTX_C_N7	AK19	PEX_TX7_N
PEG_CRX_GTX_C_P8	AK20	PEX_TX8
PEG_CRX_GTX_C_N8	AH20	PEX_TX8_N
PEG_CRX_GTX_C_P9	AH20	PEX_TX9
PEG_CRX_GTX_C_N9	AG20	PEX_TX9_N
PEG_CRX_GTX_C_P10	AK21	PEX_TX10
PEG_CRX_GTX_C_N10	AJ21	PEX_TX10_N
PEG_CRX_GTX_C_P11	AL22	PEX_TX11
PEG_CRX_GTX_C_N11	AK22	PEX_TX11_N
PEG_CRX_GTX_C_P12	AK23	PEX_TX12
PEG_CRX_GTX_C_N12	AJ23	PEX_TX12_N
PEG_CRX_GTX_C_P13	AH23	PEX_TX13
PEG_CRX_GTX_C_N13	AG23	PEX_TX13_N
PEG_CRX_GTX_C_P14	AK24	PEX_TX14
PEG_CRX_GTX_C_N14	AJ24	PEX_TX14_N
PEG_CRX_GTX_C_P15	AL25	PEX_TX15
PEG_CRX_GTX_C_N15	AK25	PEX_TX15_N

Part 1 of 7
 GPIO
 DACs
 PCI EXPRESS
 I2C
 CLK



don't connect to PCH



MAX1485EETL has internal 3K pu for GPU_CRT_CLK_DDC and GPU_CRT_DAT_DDC

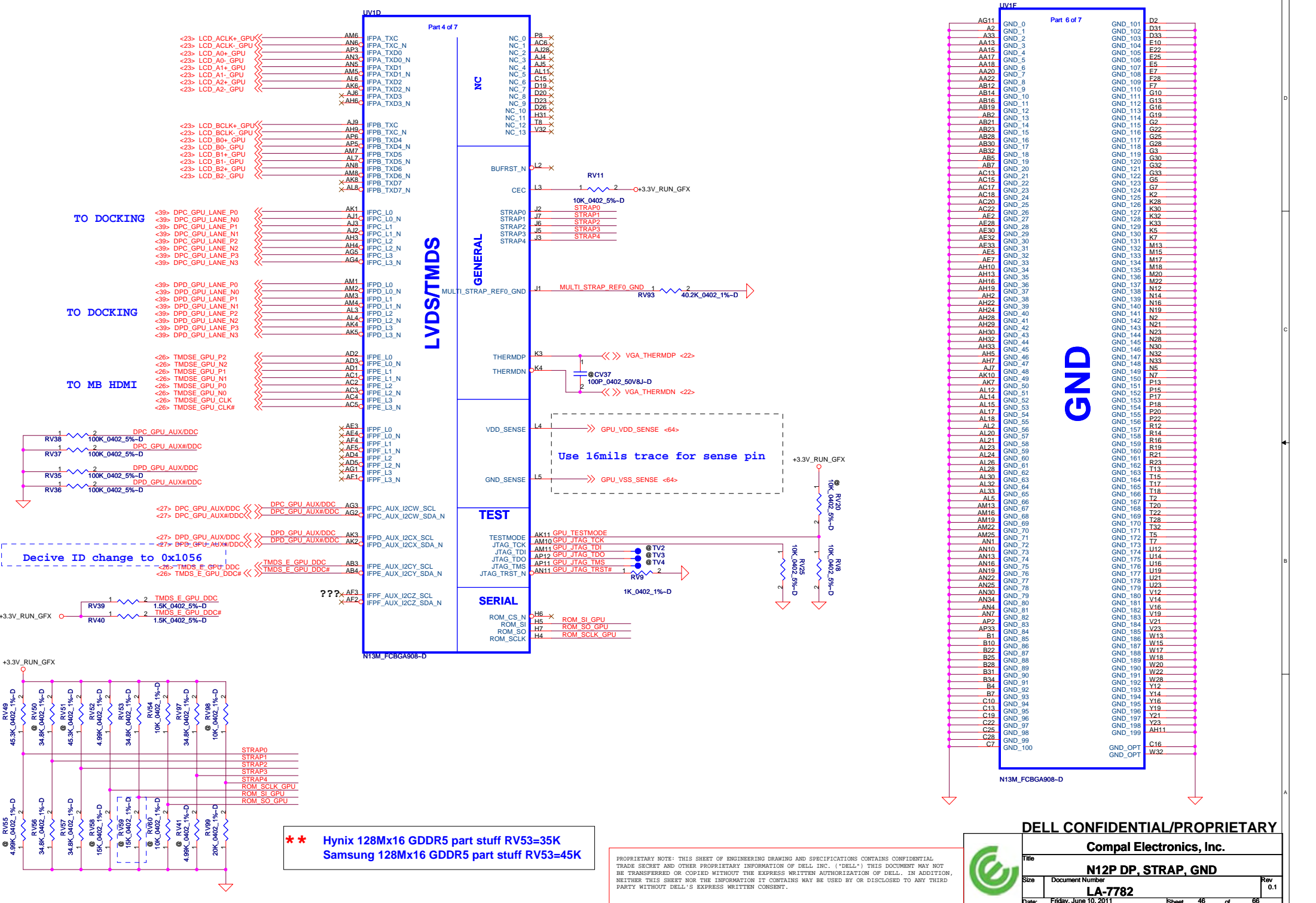
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Title	N12P PCIE,I2C,DAC,GPIO		
Size	Document Number	Rev	0.1
	LA-7782		
Date:	Friday, June 10, 2011	Sheet	45 of 66

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**** Hynix 128Mx16 GDDR5 part stuff RV53=35K
Samsung 128Mx16 GDDR5 part stuff RV53=45K**

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N12P DP, STRAP, GND

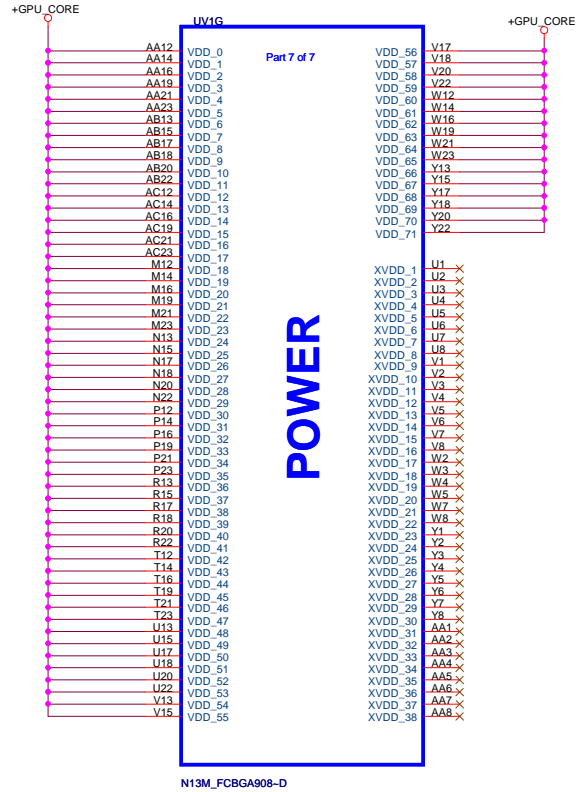
LA-7782

Rev 0.1

Date: Friday, June 10, 2011

Sheet 46 of 66

Caps on Power Side



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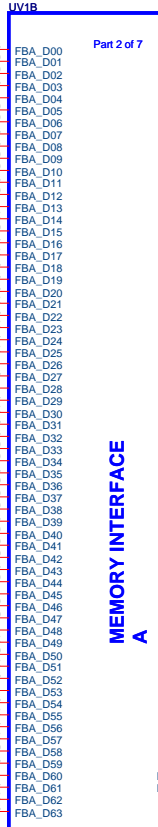
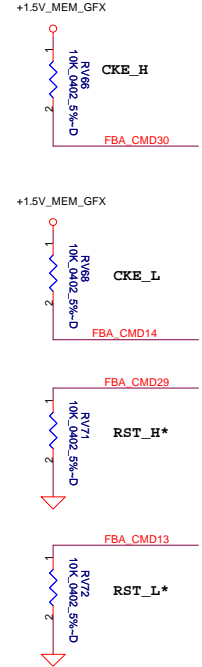


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Title			N12P Power GFX Core		
Size	Document Number	Rev			
	LA-7782	0.1			
Date:	Friday, May 20, 2011	Sheet	48	of	66

FBA_D[0..63] <<> FBA_D[0..63] <51..52>
 FBA_CMD[0..31] <<> FBA_CMD[0..31] <51..52>
 FBA_DB[0..7] <<> FBA_DB[0..7] <51..52>
 FBA_EDC[0..7] <<> FBA_EDC[0..7] <51..52>

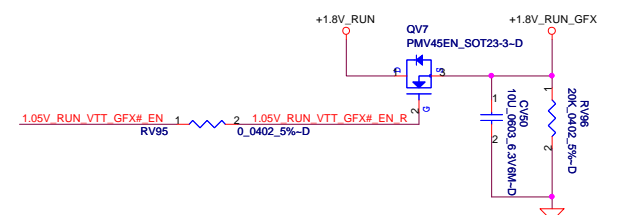


U30	FBA_CMD0	U30	FBA_CMD0
FBA_CMD0	U30	FBA_CMD0	U30
FBA_CMD1	T31	FBA_CMD1	T31
FBA_CMD2	U29	FBA_CMD2	U29
FBA_CMD3	R34	FBA_CMD3	R34
FBA_CMD4	R33	FBA_CMD4	R33
FBA_CMD5	U32	FBA_CMD5	U32
FBA_CMD6	U33	FBA_CMD6	U33
FBA_CMD7	U28	FBA_CMD7	U28
FBA_CMD8	V28	FBA_CMD8	V28
FBA_CMD9	V29	FBA_CMD9	V29
FBA_CMD10	V30	FBA_CMD10	V30
FBA_CMD11	U34	FBA_CMD11	U34
FBA_CMD12	U31	FBA_CMD12	U31
FBA_CMD13	V34	FBA_CMD13	V34
FBA_CMD14	V33	FBA_CMD14	V33
FBA_CMD15	Y32	FBA_CMD15	Y32
FBA_CMD16	AA31	FBA_CMD16	AA31
FBA_CMD17	AA29	FBA_CMD17	AA29
FBA_CMD18	AA28	FBA_CMD18	AA28
FBA_CMD19	AC34	FBA_CMD19	AC34
FBA_CMD20	AC33	FBA_CMD20	AC33
FBA_CMD21	AA32	FBA_CMD21	AA32
FBA_CMD22	AA33	FBA_CMD22	AA33
FBA_CMD23	Y28	FBA_CMD23	Y28
FBA_CMD24	Y29	FBA_CMD24	Y29
FBA_CMD25	W31	FBA_CMD25	W31
FBA_CMD26	R30	FBA_CMD26	R30
FBA_CMD27	AA34	FBA_CMD27	AA34
FBA_CMD28	Y31	FBA_CMD28	Y31
FBA_CMD29	Y34	FBA_CMD29	Y34
FBA_CMD30	Y33	FBA_CMD30	Y33
FBA_CMD31	Y31	FBA_CMD31	Y31
FBA_DB0	P30	FBA_DB0	P30
FBA_DB1	F31	FBA_DB1	F31
FBA_DB2	F34	FBA_DB2	F34
FBA_DB3	M32	FBA_DB3	M32
FBA_DB4	AD31	FBA_DB4	AD31
FBA_DB5	AL29	FBA_DB5	AL29
FBA_DB6	AM32	FBA_DB6	AM32
FBA_DB7	AF34	FBA_DB7	AF34
FBA_D0M0	F30	FBA_D0M0	F30
FBA_D0M1	F31	FBA_D0M1	F31
FBA_D0M2	M32	FBA_D0M2	M32
FBA_D0M3	AD31	FBA_D0M3	AD31
FBA_D0M4	AL29	FBA_D0M4	AL29
FBA_D0M5	AM32	FBA_D0M5	AM32
FBA_D0M6	AF34	FBA_D0M6	AF34
FBA_D0M7	F30	FBA_D0M7	F30
FBA_D0S_RN0	M30	FBA_D0S_RN0	M30
FBA_D0S_RN1	E34	FBA_D0S_RN1	E34
FBA_D0S_RN2	M34	FBA_D0S_RN2	M34
FBA_D0S_RN3	AF30	FBA_D0S_RN3	AF30
FBA_D0S_RN4	AK31	FBA_D0S_RN4	AK31
FBA_D0S_RN5	AM34	FBA_D0S_RN5	AM34
FBA_D0S_RN6	AF34	FBA_D0S_RN6	AF34
FBA_D0S_RN7	AF34	FBA_D0S_RN7	AF34
FBA_D0S_WP0	M31	FBA_D0S_WP0	M31
FBA_D0S_WP1	E33	FBA_D0S_WP1	E33
FBA_D0S_WP2	M33	FBA_D0S_WP2	M33
FBA_D0S_WP3	AK30	FBA_D0S_WP3	AK30
FBA_D0S_WP4	AN33	FBA_D0S_WP4	AN33
FBA_D0S_WP5	AE31	FBA_D0S_WP5	AE31
FBA_D0S_WP6	AN33	FBA_D0S_WP6	AN33
FBA_D0S_WP7	AF33	FBA_D0S_WP7	AF33
FBA_CMD_RFU0	R32	FBA_CMD_RFU0	R32
FBA_CMD_RFU1	AC34	FBA_CMD_RFU1	AC34
FBA_CLK0	R30	FBA_CLK0	R30
FBA_CLK0_N	R31	FBA_CLK0_N	R31
FBA_CLK1	AB31	FBA_CLK1	AB31
FBA_CLK1_N	AC31	FBA_CLK1_N	AC31
FBA_WCK01	K31	FBA_WCK01	K31
FBA_WCK01_N	L30	FBA_WCK01_N	L30
FBA_WCK23	H34	FBA_WCK23	H34
FBA_WCK23_N	AG30	FBA_WCK23_N	AG30
FBA_WCK45	AG31	FBA_WCK45	AG31
FBA_WCK45_N	AJ34	FBA_WCK45_N	AJ34
FBA_WCK67	AK34	FBA_WCK67	AK34
FBA_WCK67_N	AK34	FBA_WCK67_N	AK34
FBA_WCKB01	J30	FBA_WCKB01	J30
FBA_WCKB01_N	J31	FBA_WCKB01_N	J31
FBA_WCKB23	J32	FBA_WCKB23	J32
FBA_WCKB23_N	J33	FBA_WCKB23_N	J33
FBA_WCKB45	AH31	FBA_WCKB45	AH31
FBA_WCKB45_N	AJ31	FBA_WCKB45_N	AJ31
FBA_WCKB67	AJ32	FBA_WCKB67	AJ32
FBA_WCKB67_N	AJ33	FBA_WCKB67_N	AJ33

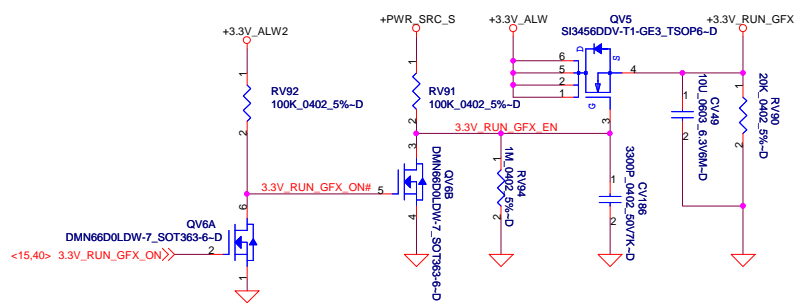
GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD16	CMD32	WE#
CMD0	CMD16	CS#
CMD8	CMD24	ABI#
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD2	CMD18	A2_BA0
CMD1	CMD17	A3_BA3
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD7	CMD23	A6_A11
CMD6	CMD22	A7_A8
CMD9	CMD25	A12_FRU
CMD14	CMD30	CKE#
CMD13	CMD29	RESET#

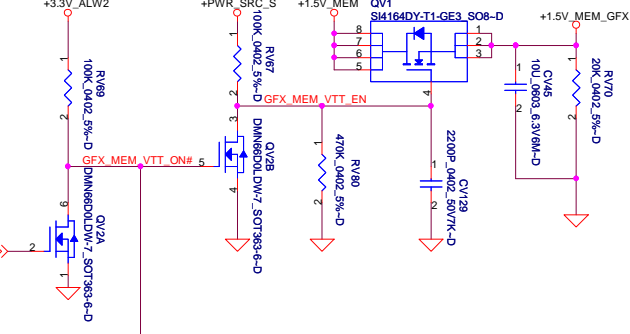
+1.8V_RUN_GFX Source



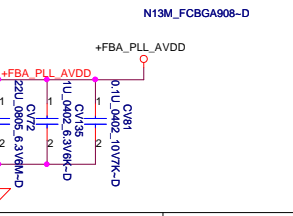
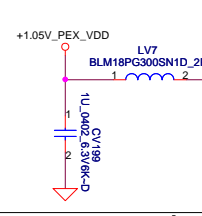
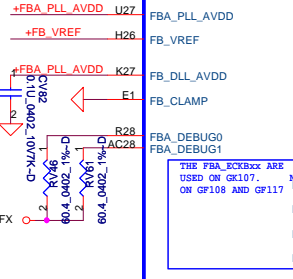
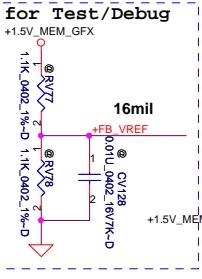
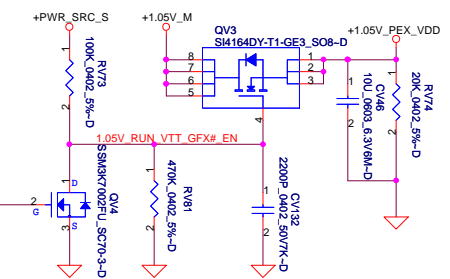
+3.3V_RUN_GFX Source



+1.5V_MEM_GFX Source



+1.05V_RUN_VTT_GFX Source



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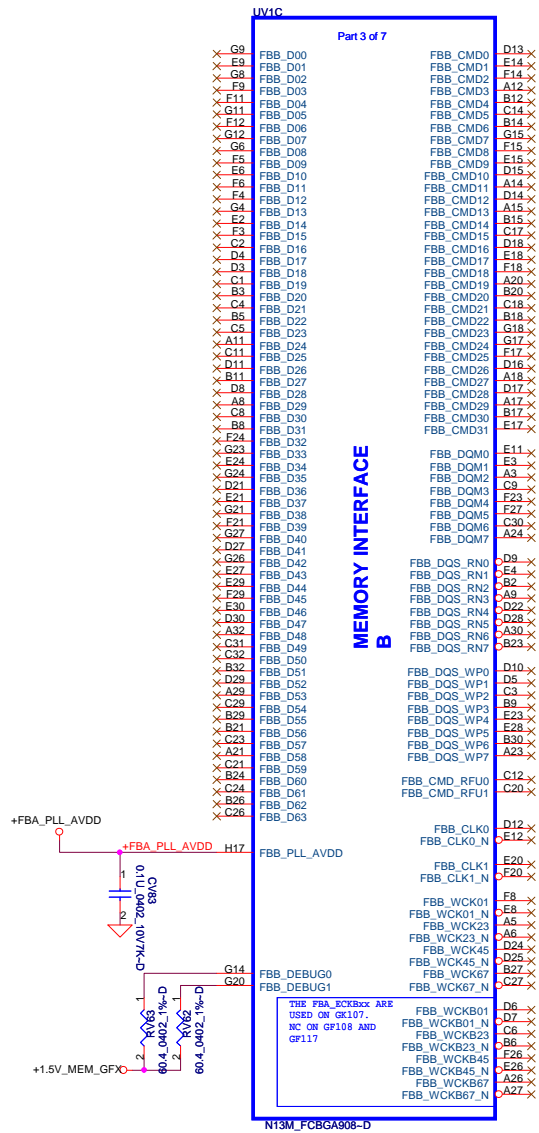


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N12P Memory			Rev 0.1
LA-7782	Document Number	Sheet 49 of 66	
Friday, June 10, 2011	Date	Friday, June 10, 2011	

CHANNEL-B NOT TO USE, NEED TO BE DISABLED



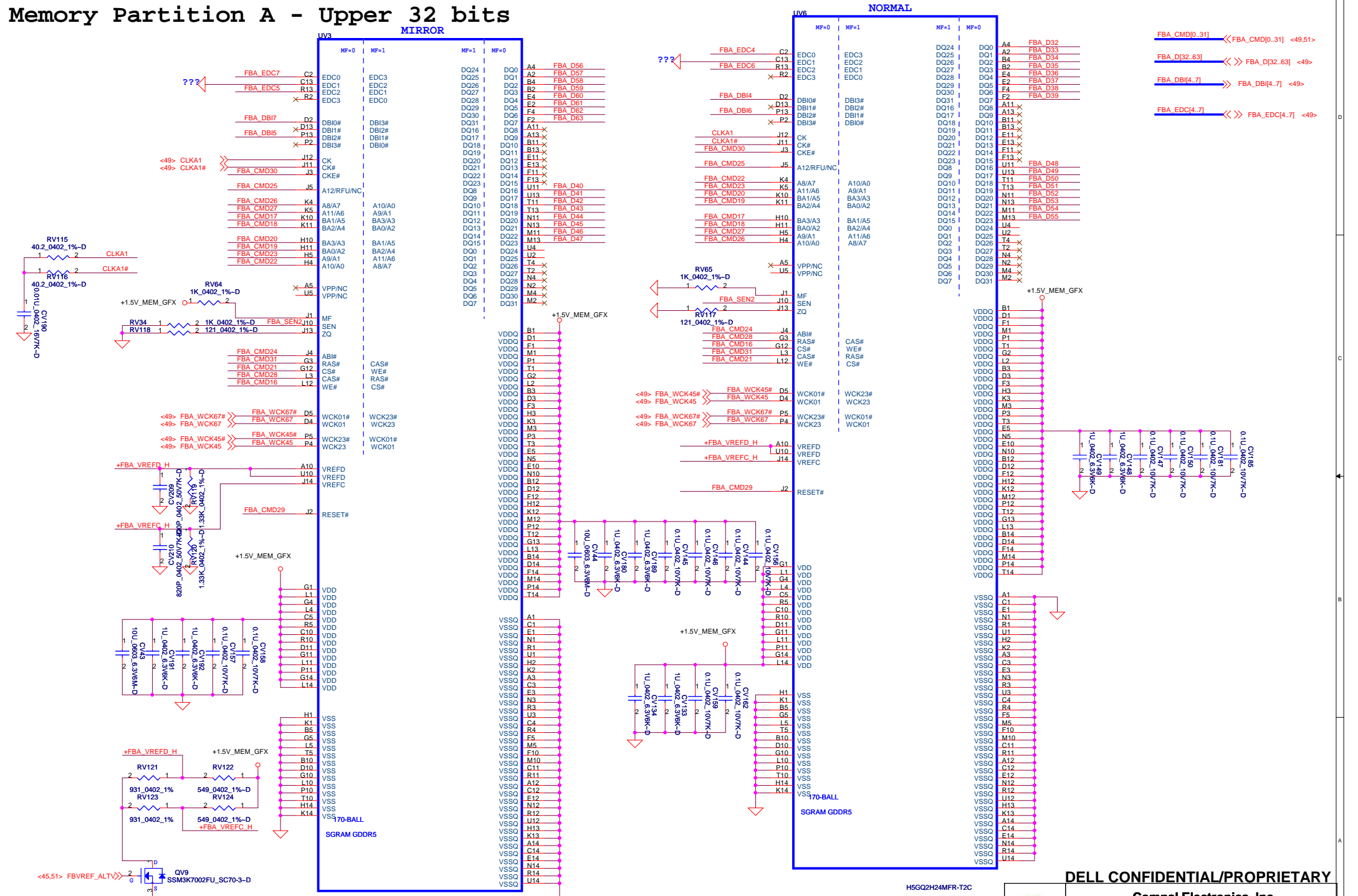
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N12P Memory (2)		
Size	Document Number LA-7782	Rev 0.1
Date:	Friday, May 20, 2011	Sheet 50 of 66

Memory Partition A - Upper 32 bits



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VRAM A Upper

LA-7782

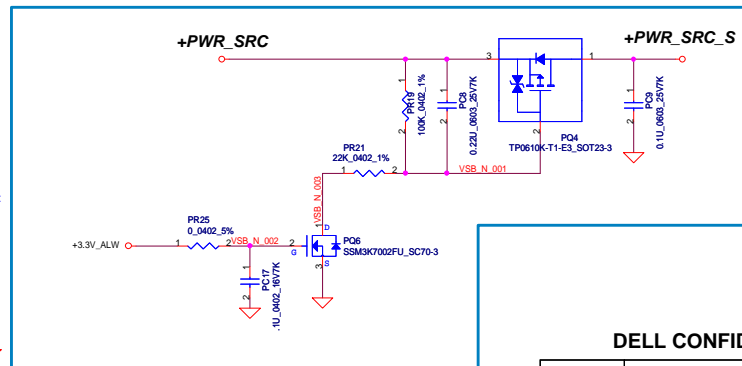
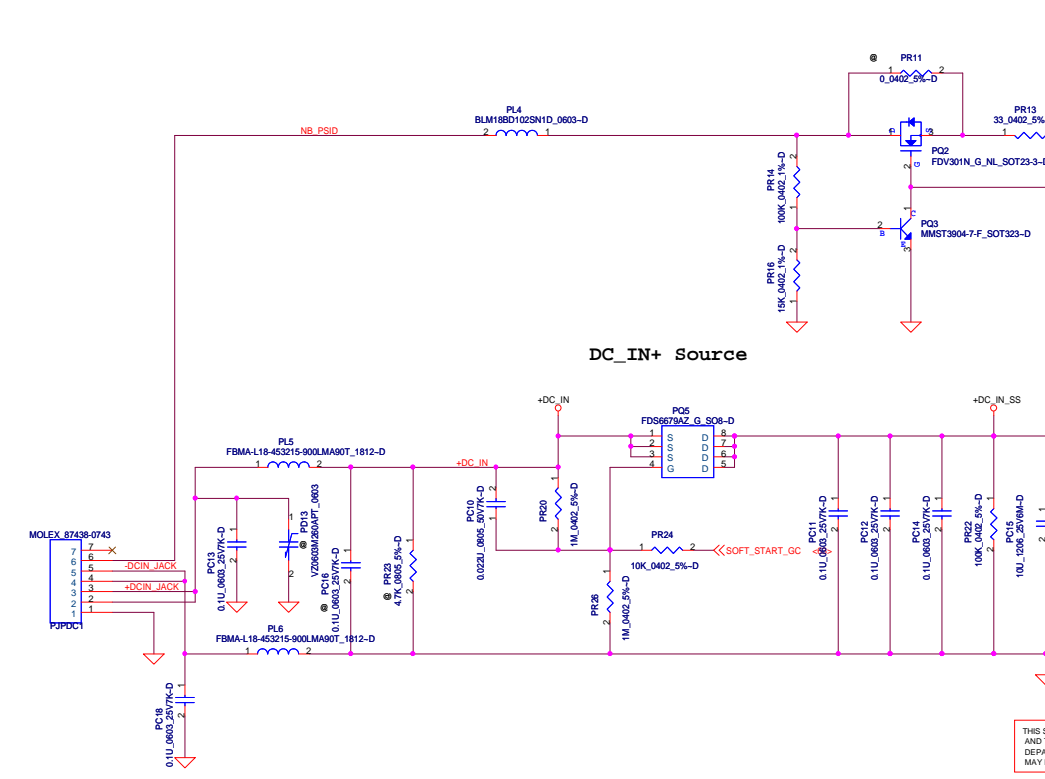
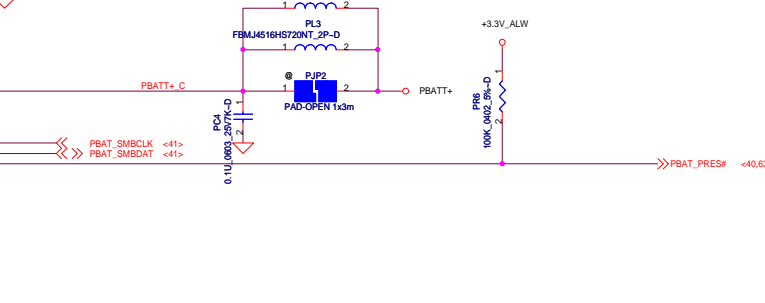
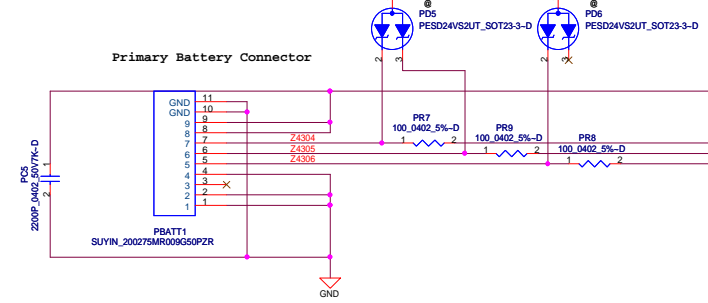
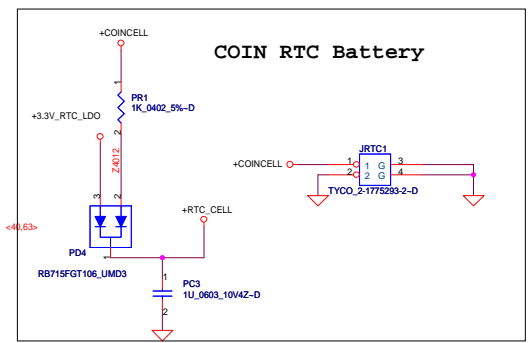
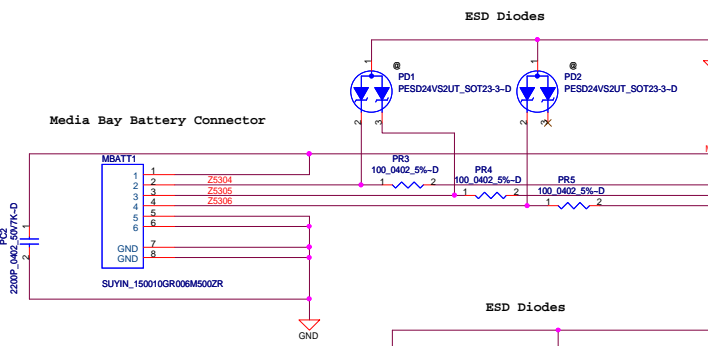
Friday, June 10, 2011 Sheet 52 of 66

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H5GQ2H4MFR-T2C

H5GQ2H4MFR-T2C



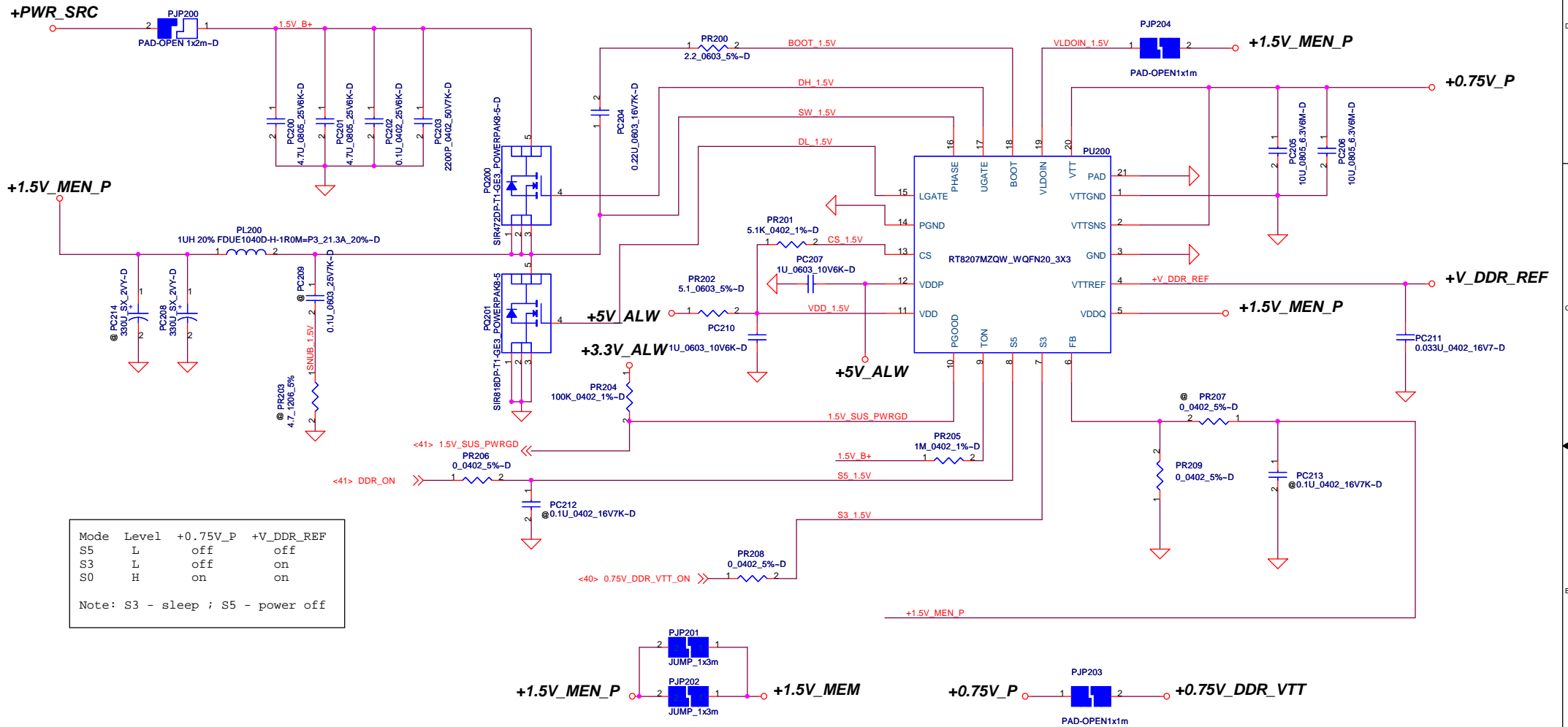
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	+DCIN		
Title	Document Number	LA-7782	Rev 0.1
Date: Friday, June 10, 2011	Sheet 53	of 66	

1.5Volt +/- 5%
 TDC 9.74A
 Peak Current 13.915A
 OCP current 16.698A

0.75Volt +/- 5%
 TDC 0.525A
 Peak Current 0.75A
 OCP Current 0.9A



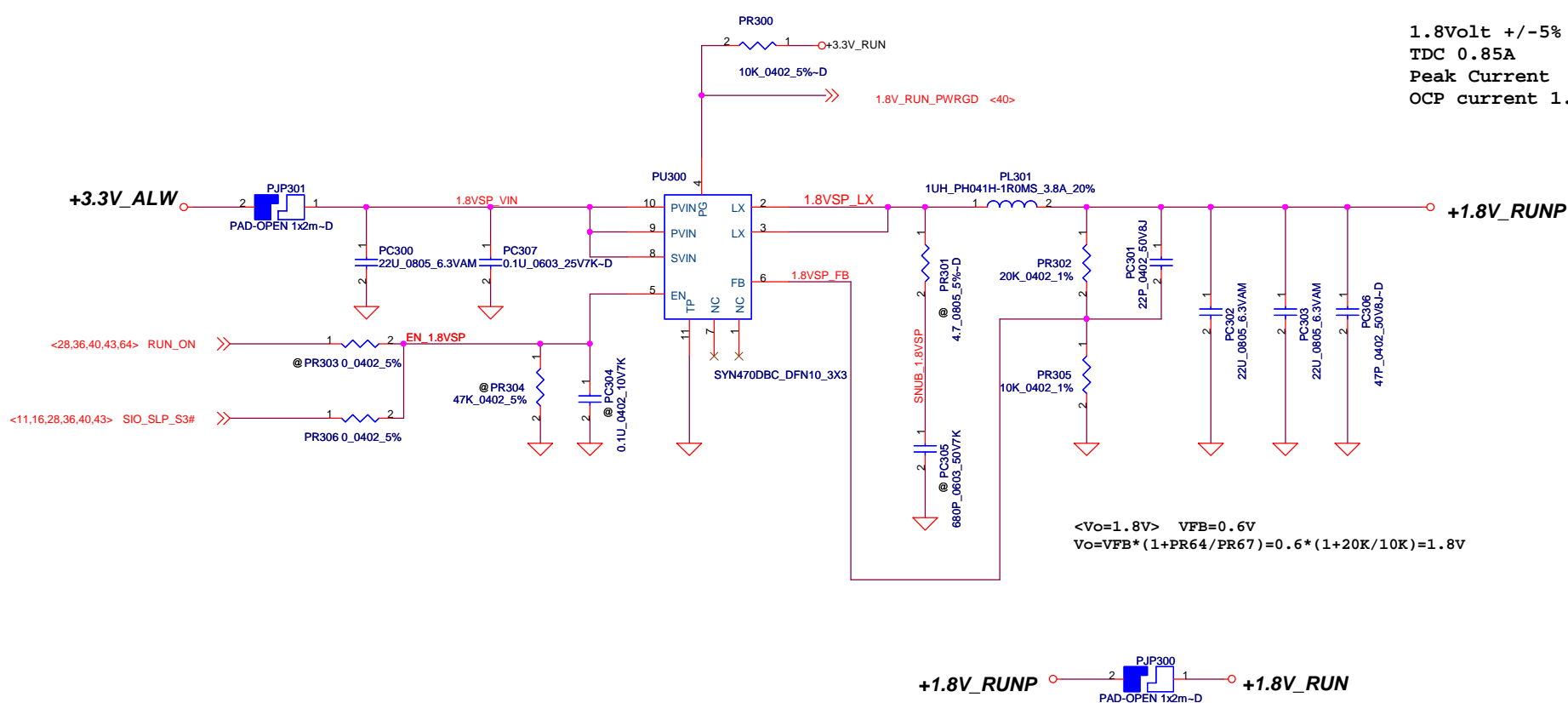
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Compal Electronics, Inc.		
Title	+1.5V_MEN+0.75V_DDR_VTT	
Size	Document Number	Rev
	LA-7782	0.1
Date	Friday, June 10, 2011	Sheet 55 of 66

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1.8VOLT +/-5%
 TDC 0.85A
 Peak Current 1.215A
 OCP current 1.458A

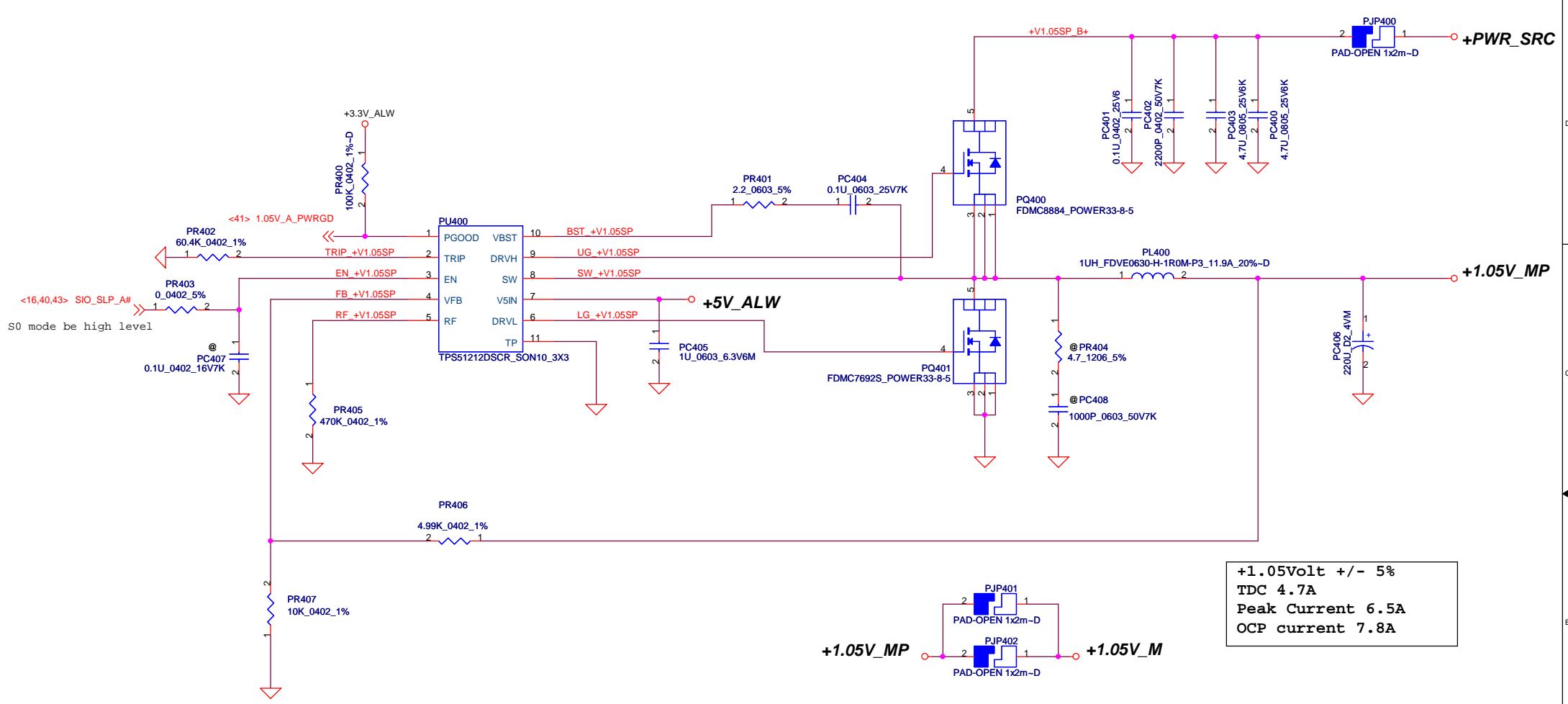


<Vo=1.8V> VFB=0.6V
 $V_o = V_{FB} * (1 + PR64 / PR67) = 0.6 * (1 + 20K / 10K) = 1.8V$

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Compal Electronics, Inc.		
Title		
+1.8V_RUN		
Size	Document Number	Rev
	LA-7782	0.1
Date: Friday, June 10, 2011		Sheet 56 of 66

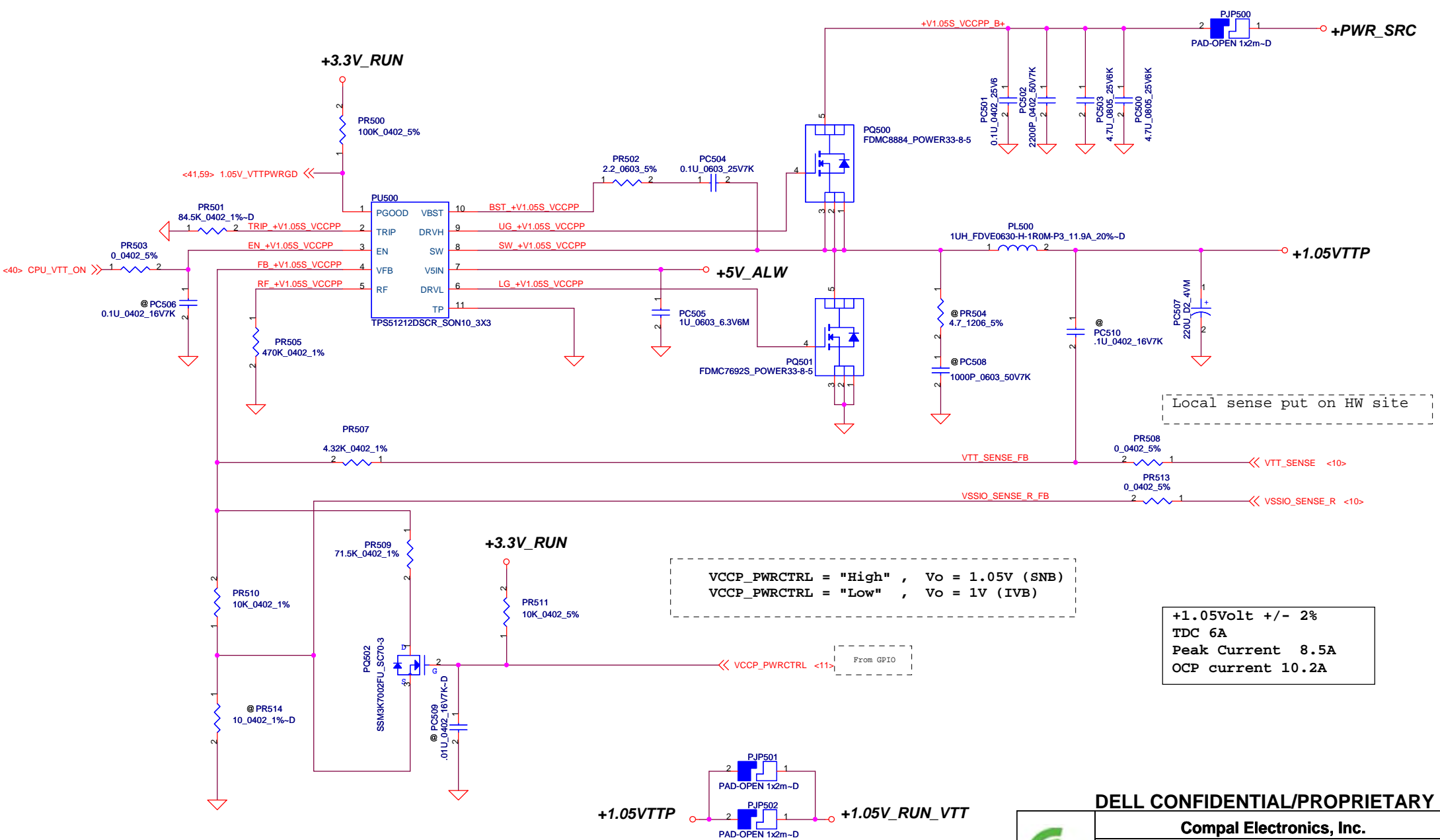


+1.05Volt +/- 5%
 TDC 4.7A
 Peak Current 6.5A
 OCP current 7.8A

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			Compal Electronics, Inc.	
			+1.05V_M	
Size	Document Number			Rev
	LA-7782			0.1
Date:	Friday, June 10, 2011	Sheet	57	of 66



VCCP_PWRCTRL = "High" , Vo = 1.05V (SNB)
 VCCP_PWRCTRL = "Low" , Vo = 1V (IVB)

+1.05Volt +/- 2%
 TDC 6A
 Peak Current 8.5A
 OCP current 10.2A

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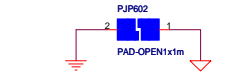
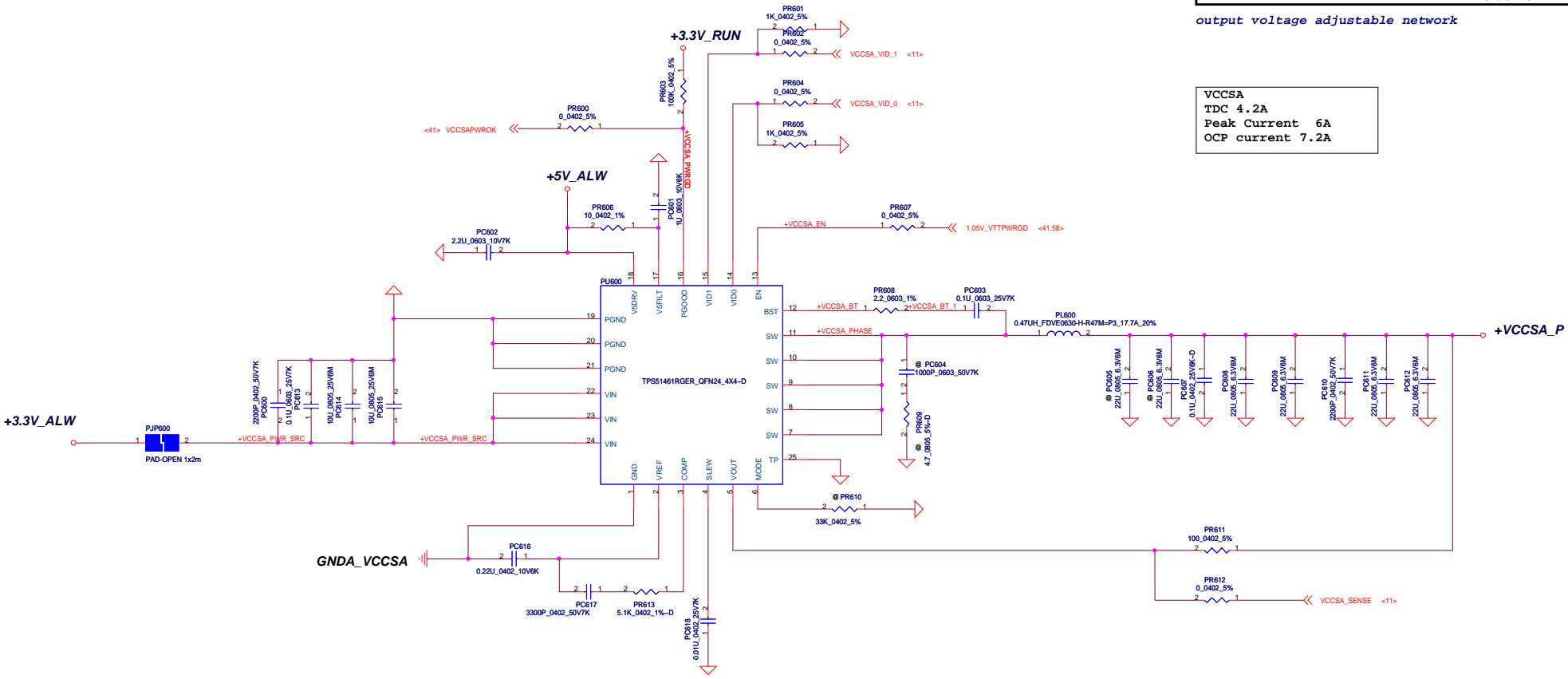
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Title +1.05V_RUN_VTT		
Size	Document Number LA-7782	Rev 0.1
Date: Friday, June 10, 2011	Sheet 58	of 66

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

VCCSA
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.



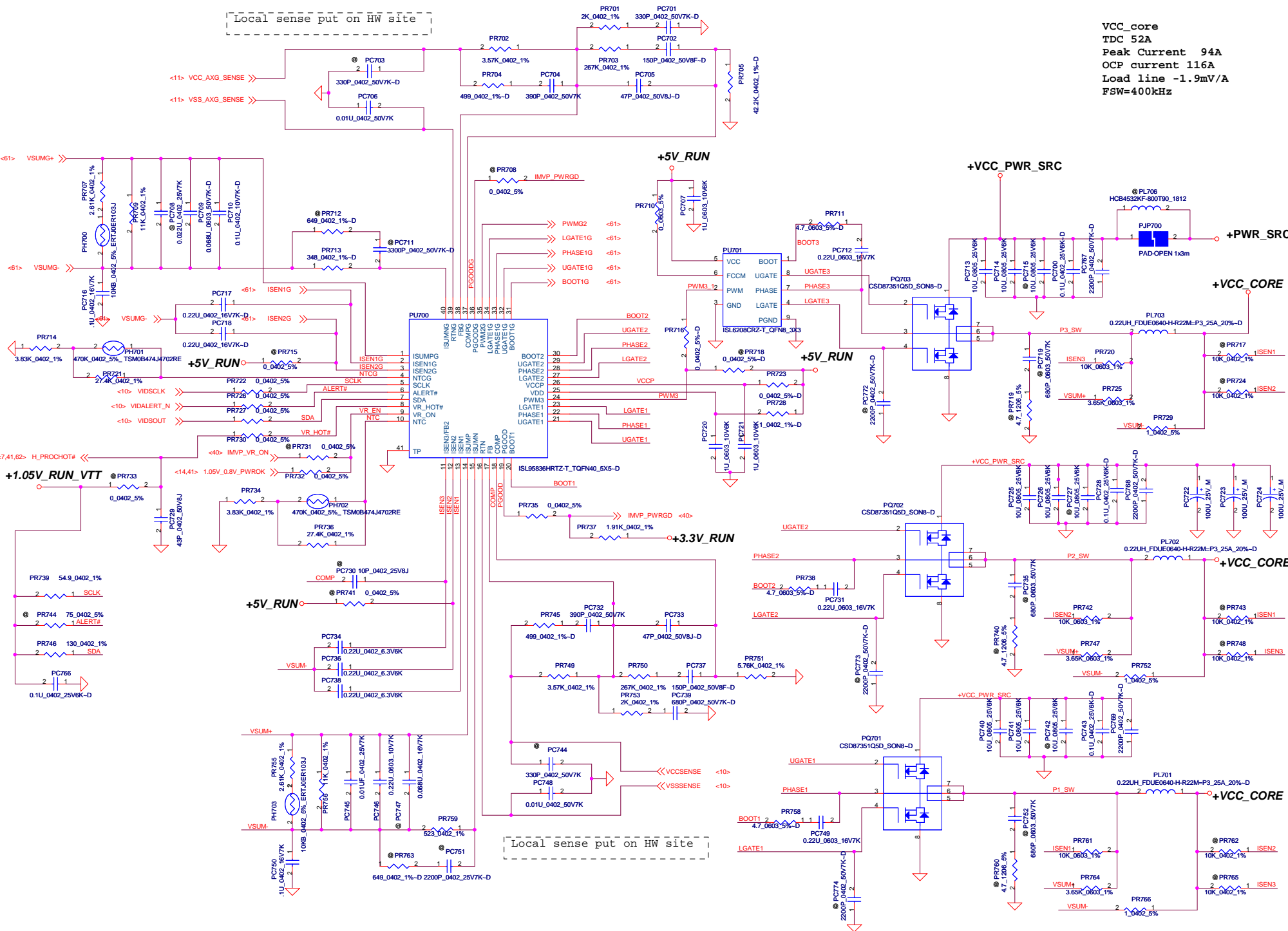
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		+VCC_SA	
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	LA-7782	0.1	
Date:	Friday, June 10, 2011	Sheet	59 of 66

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Local sense put on HW site

VCC_core
TDC 52A
Peak Current 94A
OCP current 116A
Load line -1.9mV/A
FSW=400kHz

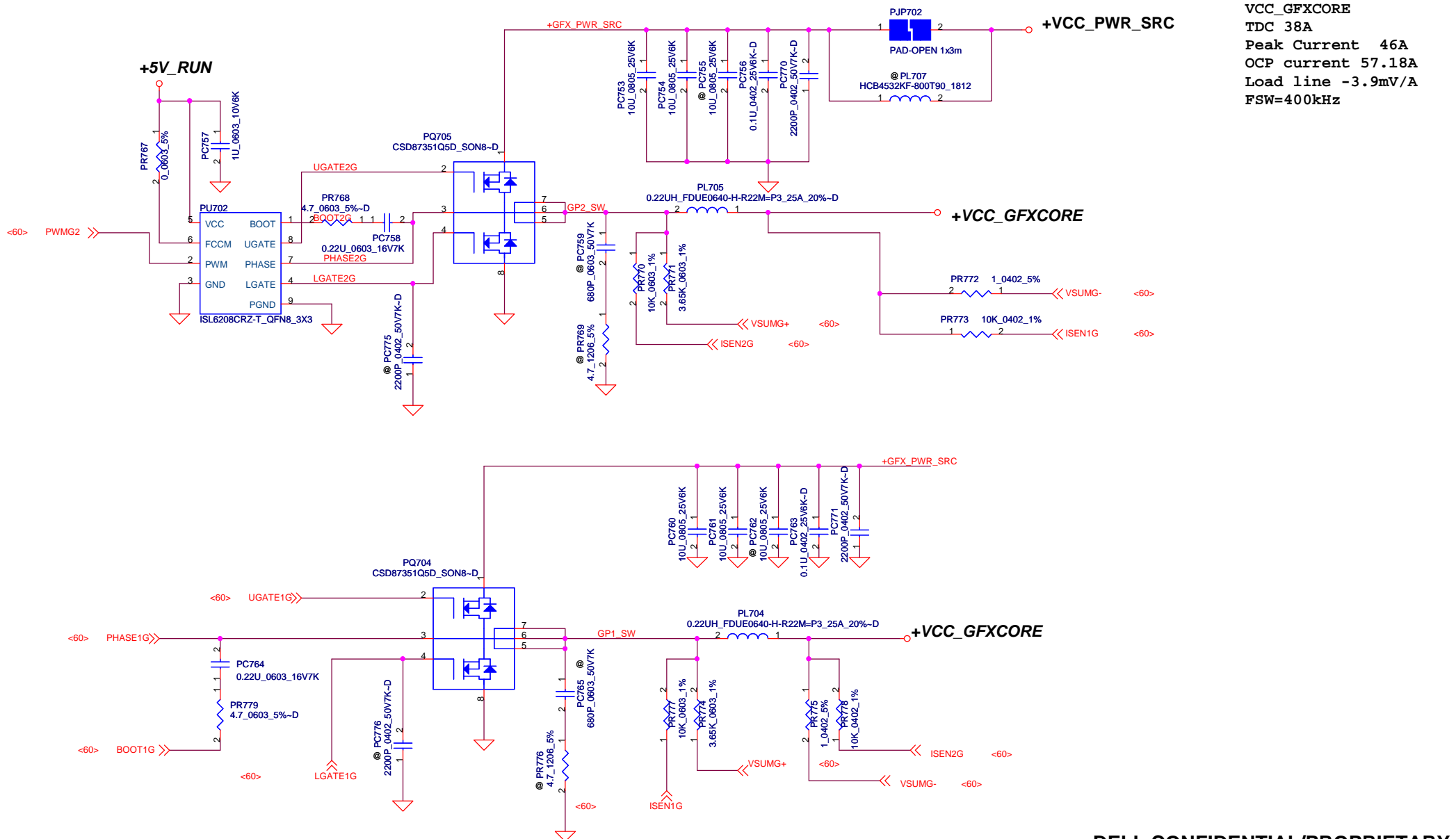


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+VCC_CORE		
File	Document Number	Rev
	LA-7782	0.1
Date	Friday, June 10, 2011	Sheet 80 of 88



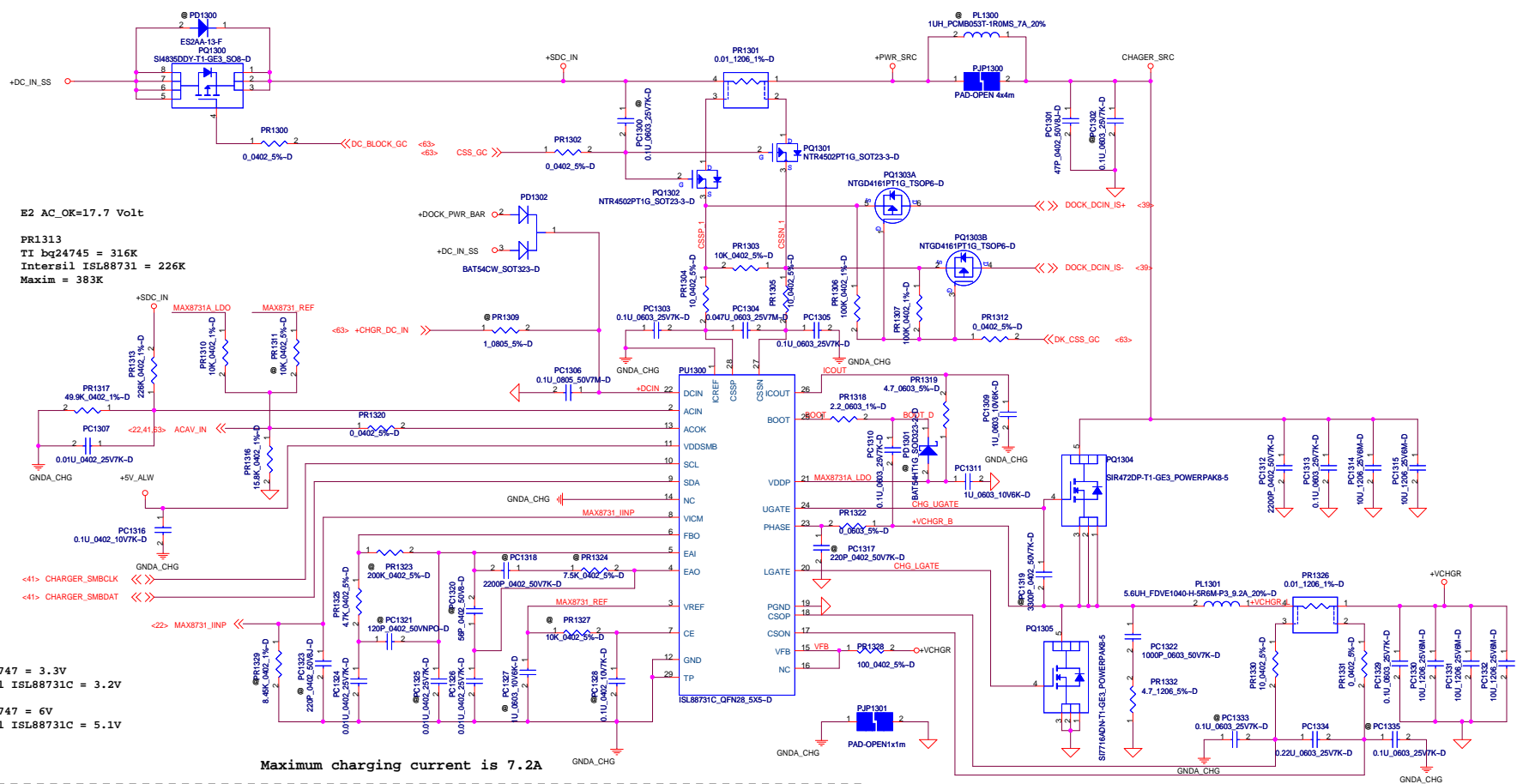
VCC_GFXCORE
 TDC 38A
 Peak Current 46A
 OCP current 57.18A
 Load line -3.9mV/A
 FSW=400kHz

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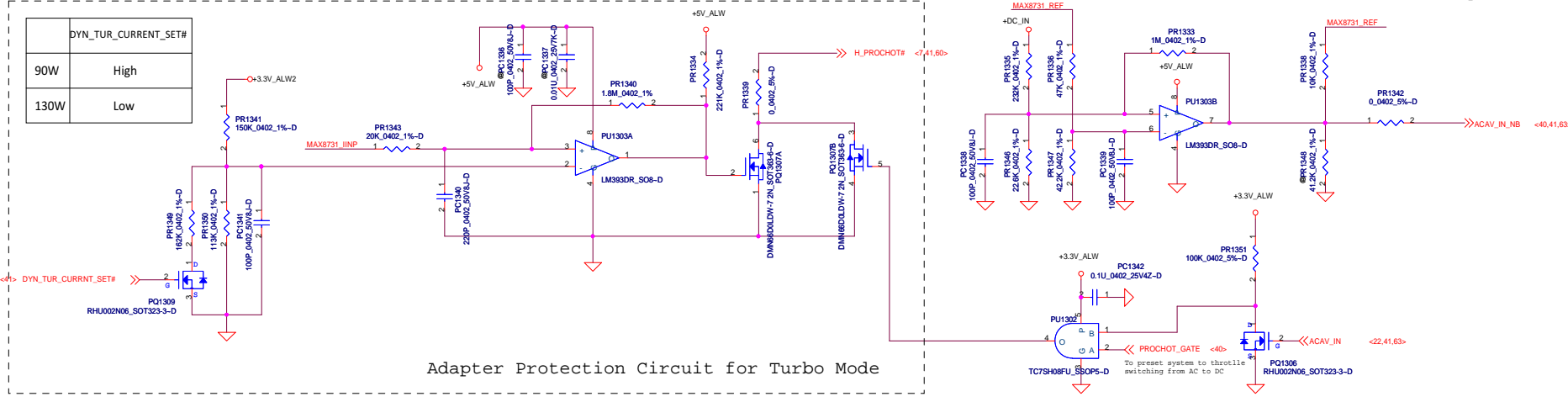
Compal Electronics, Inc.		
Title +VCC_GFXCORE		
Size	Document Number LA-7782	Rev 0.1
Date	Friday, June 10, 2011	Sheet 61 of 66



E2 AC_OK=17.7 Volt
 PR1313
 TI bq24745 = 316K
 Intersil ISL88731 = 226K
 Maxim = 383K

Vref
 TI bq24747 = 3.3V
 Intersil ISL88731C = 3.2V
 VDDP
 TI bq24747 = 6V
 Intersil ISL88731C = 5.1V

DYN_TUR_CURRENT_SET#	
90W	High
130W	Low

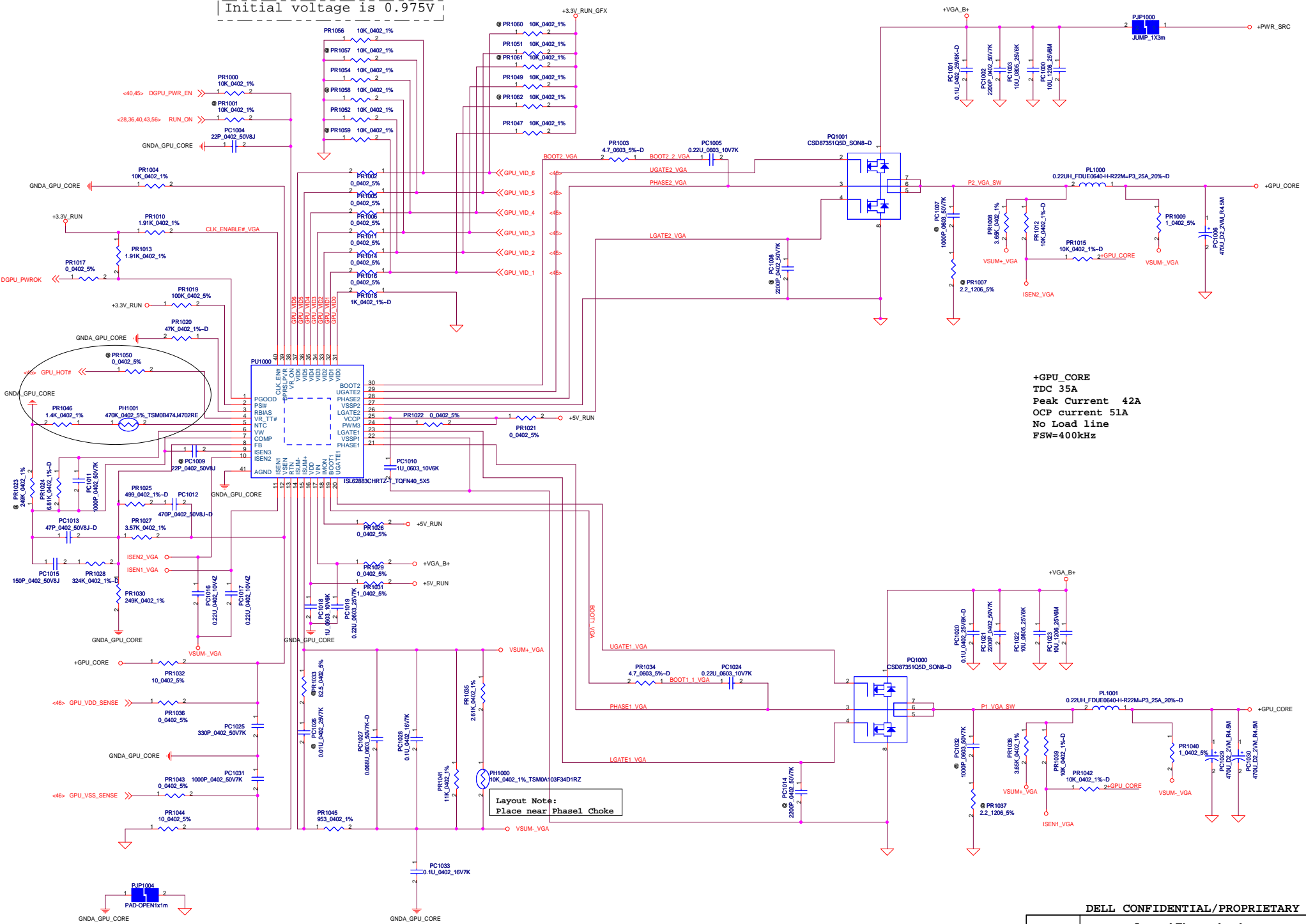


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		Compal Electronics, Inc.	
		Charger	
File	Document Number	LA-7782	
Size	Rev	0.1	
Date: Friday, June 10, 2011	Sheet	62	of 66

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Initial voltage is 0.975V



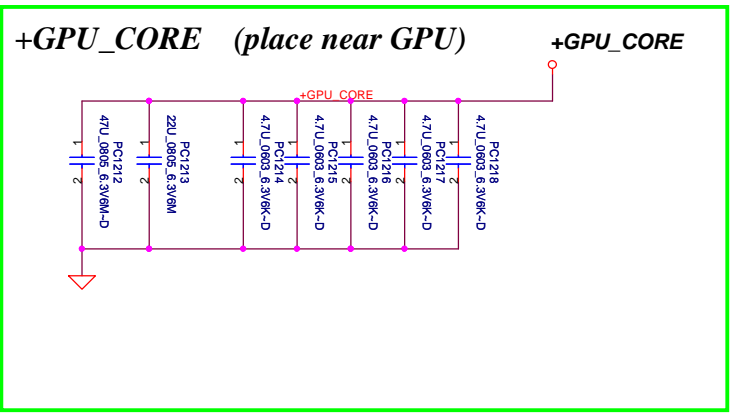
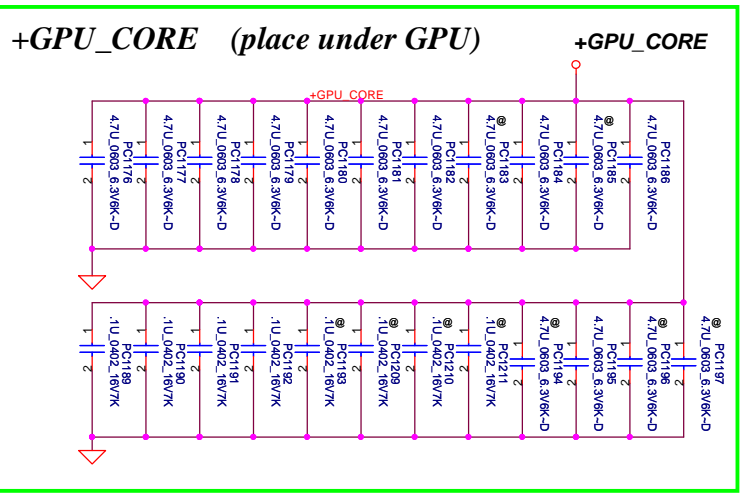
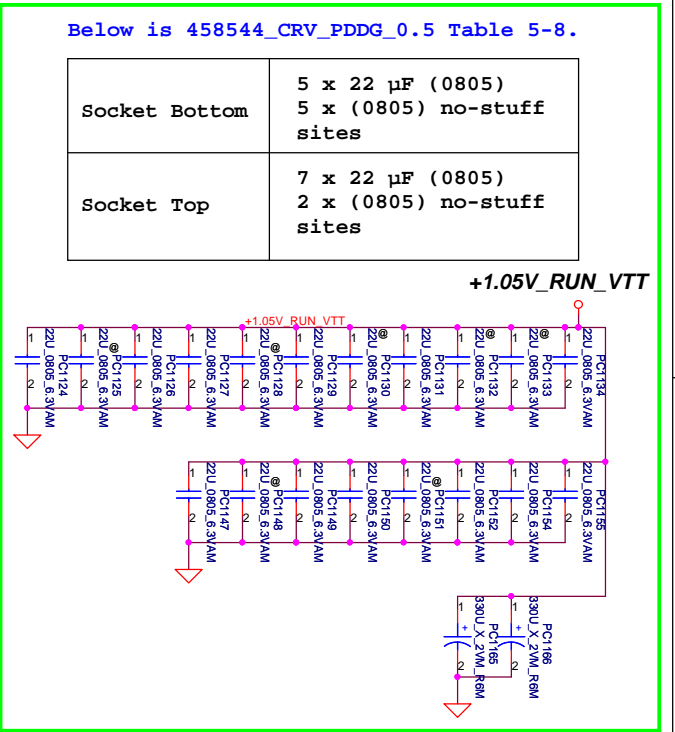
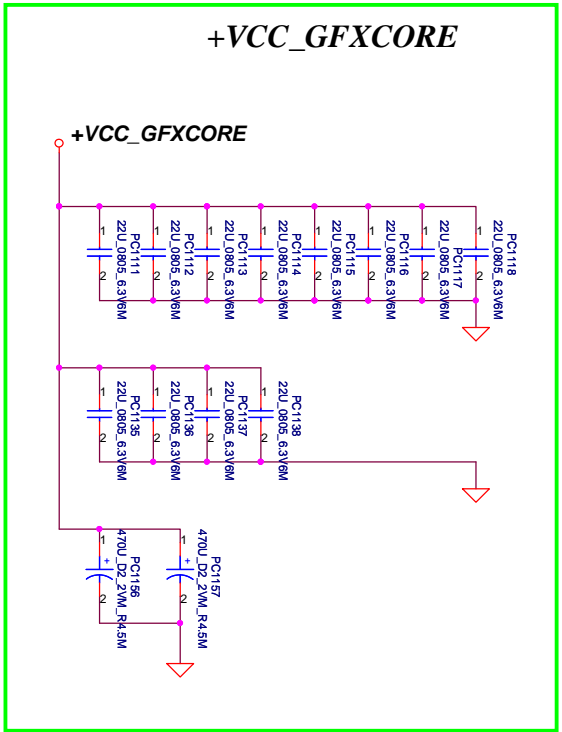
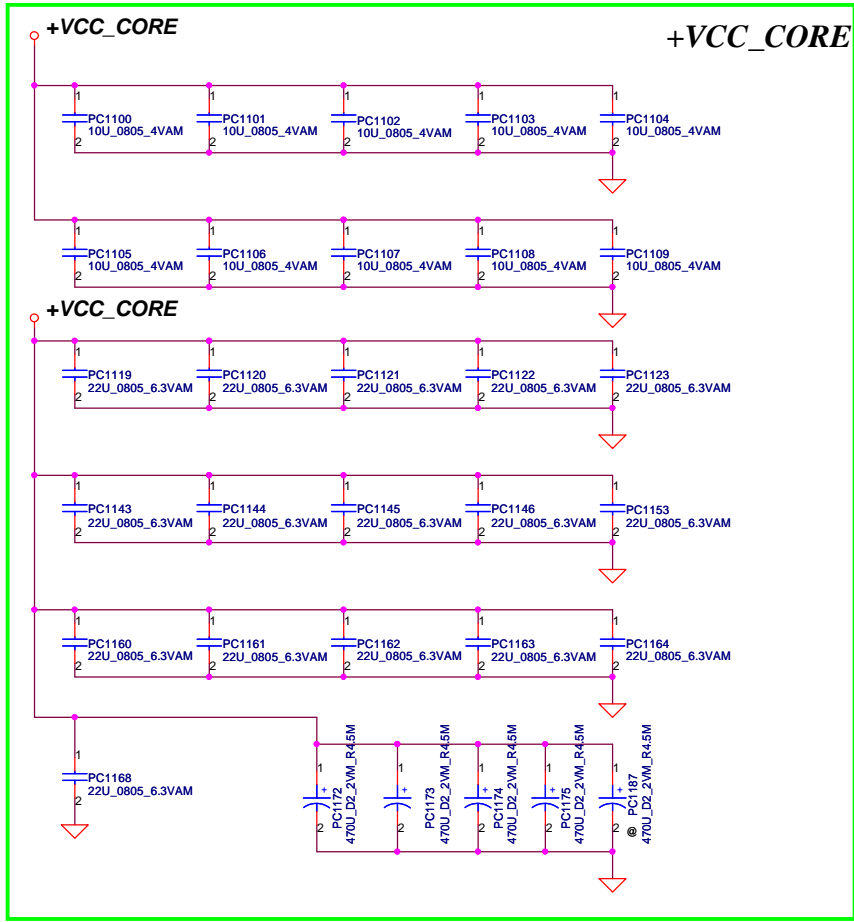
+GPU_CORE
 TDC 35A
 Peak Current 42A
 OCP current 51A
 No Load line
 FSW=400kHz

Layout Note:
 Place near Phase Choke

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	Compaq Electronics, Inc.		
	+GPU CORE		
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Size	Document Number			Rev
	LA-7782			0.1
Date:	Friday, June 10, 2011	Sheet	65	of 66

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
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Size	Document Number	Rev
	LA-7782	0.1
Date: Friday, June 10, 2011		Sheet 66 of 66

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