

Compal Confidential

Qiao Hong Schematics Document

Intel Diamondville Processor with Calistoga(945GSE) + DDRII + ICH7M

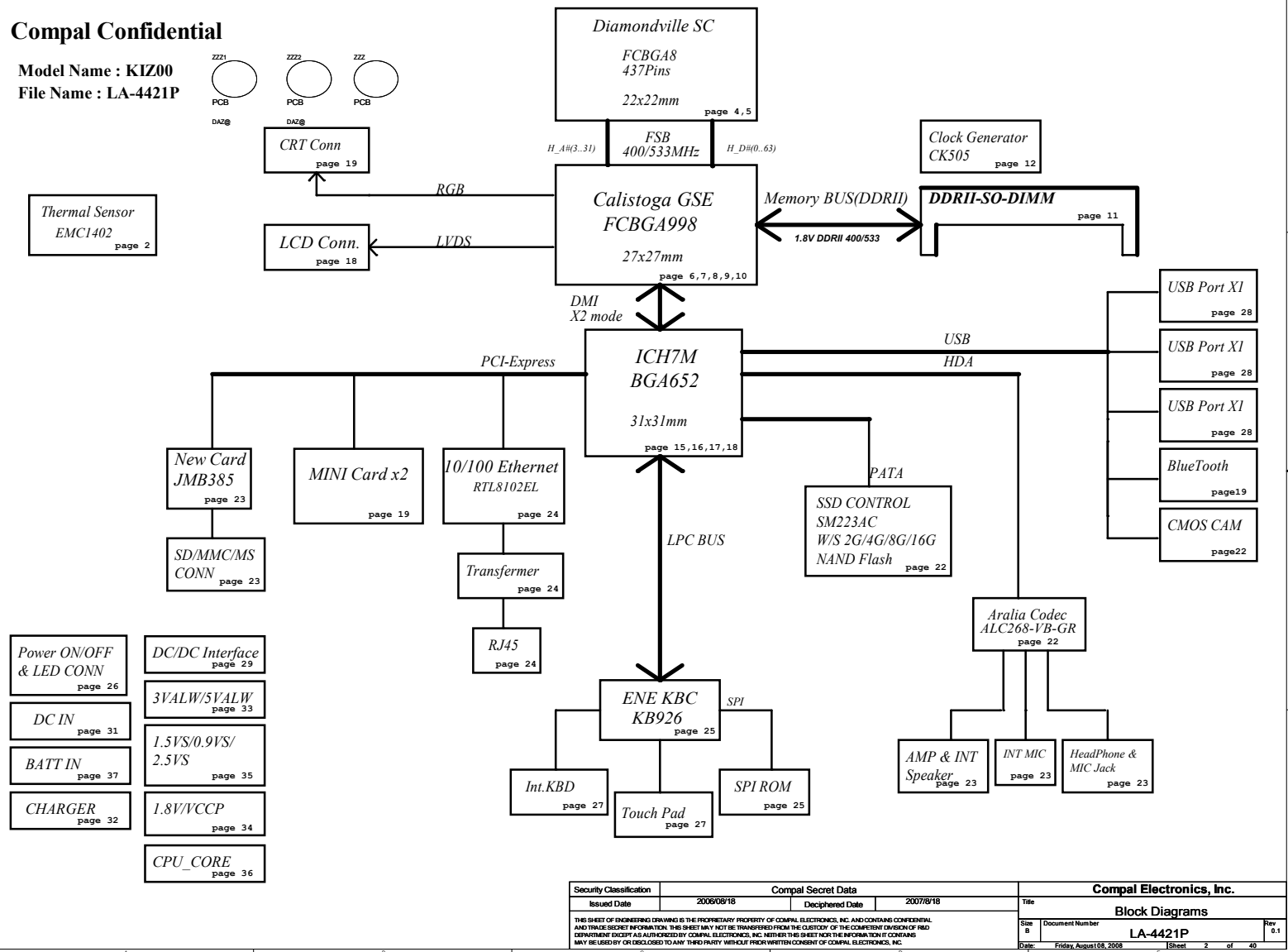
2008-07-07

REV: 1.0

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				Cover Page
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Model Name : KIZ00
File Name : LA-4421P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 25)

ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
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No PCI Device

EC SM Bus1 address

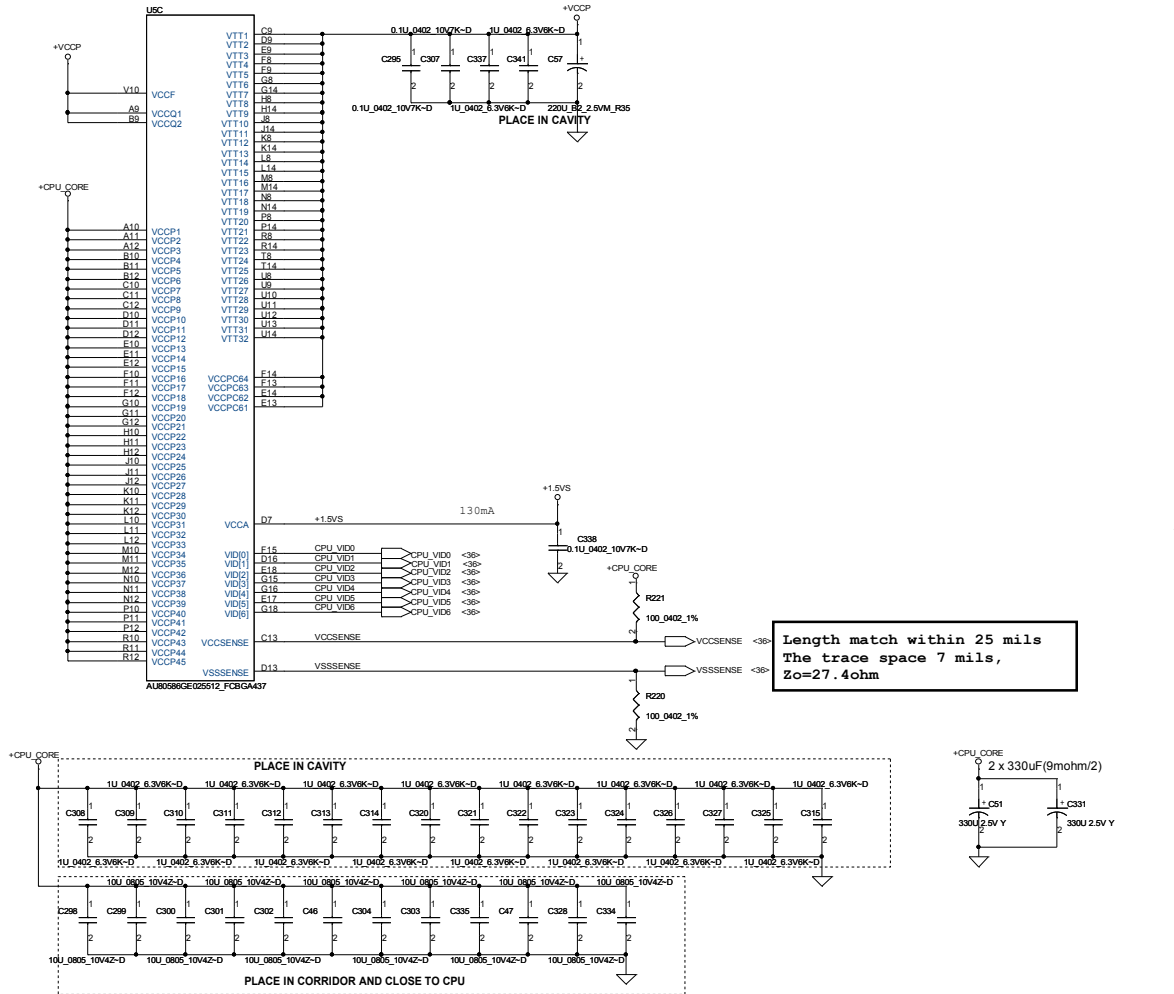
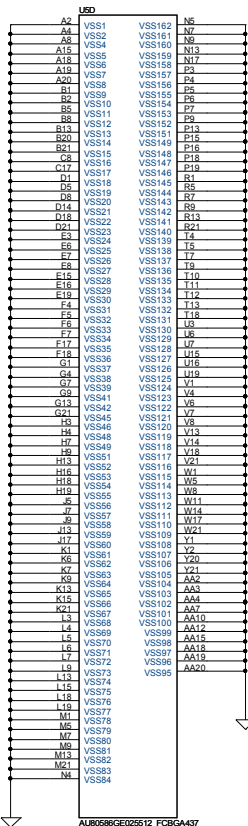
Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 100X b
EEPROM(24C16/02)	1010 000X b		

EC SM Bus2 address

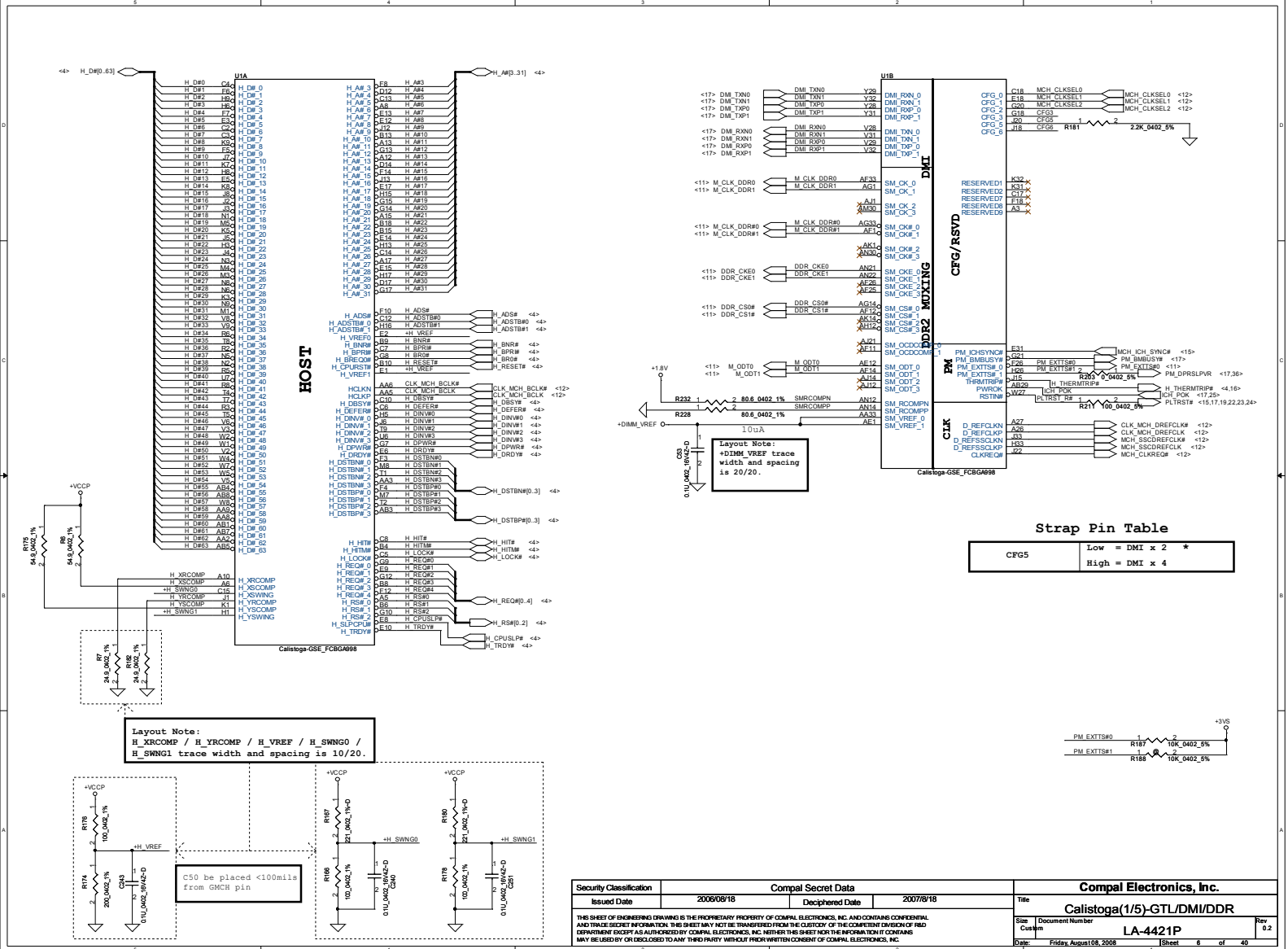
ICH7M SM Bus address

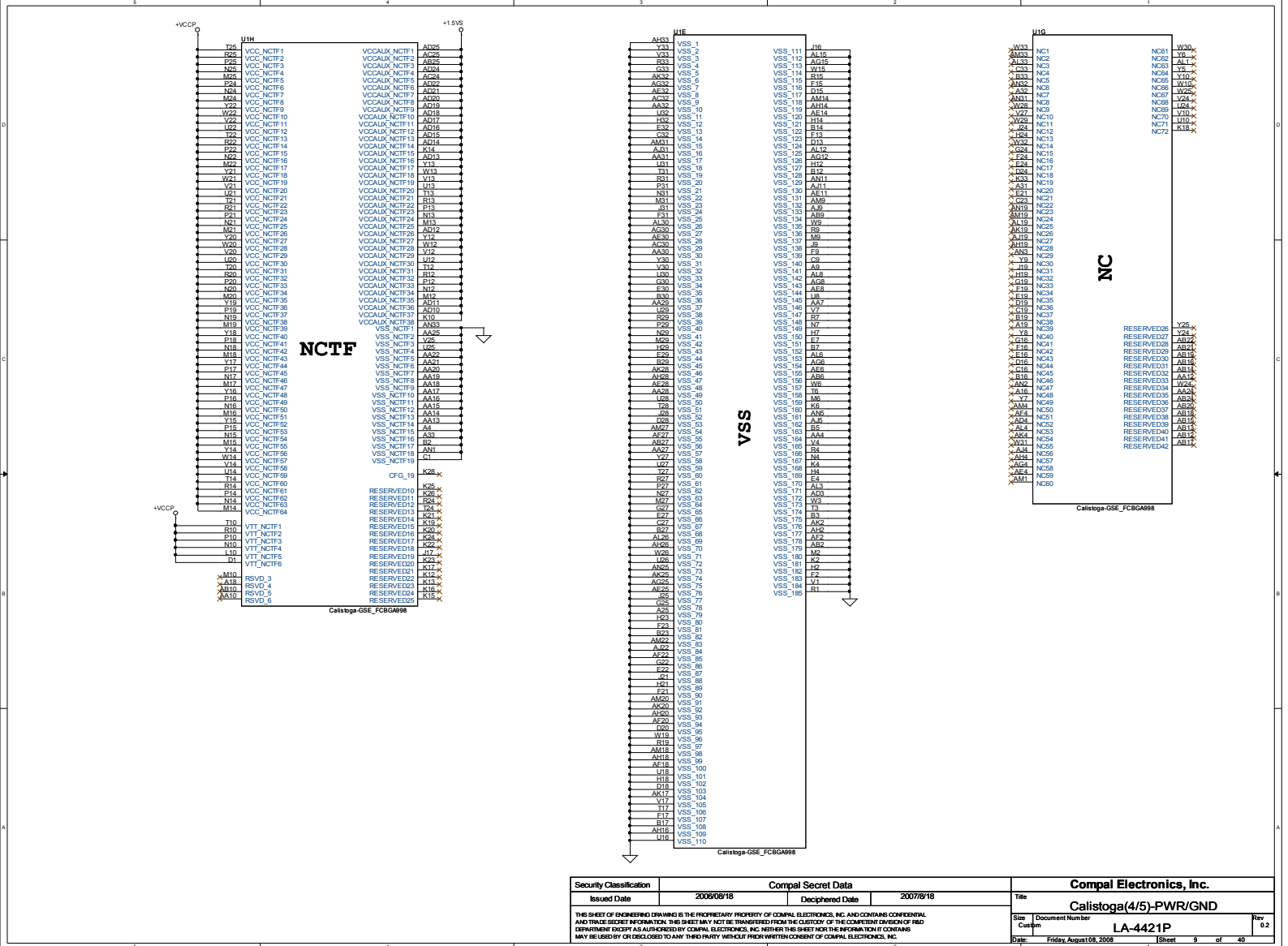
Device	Address
Clock Generator (SL6SP55SVTR)	1101 001Xb
DDR DIMMA	1010 000Xb

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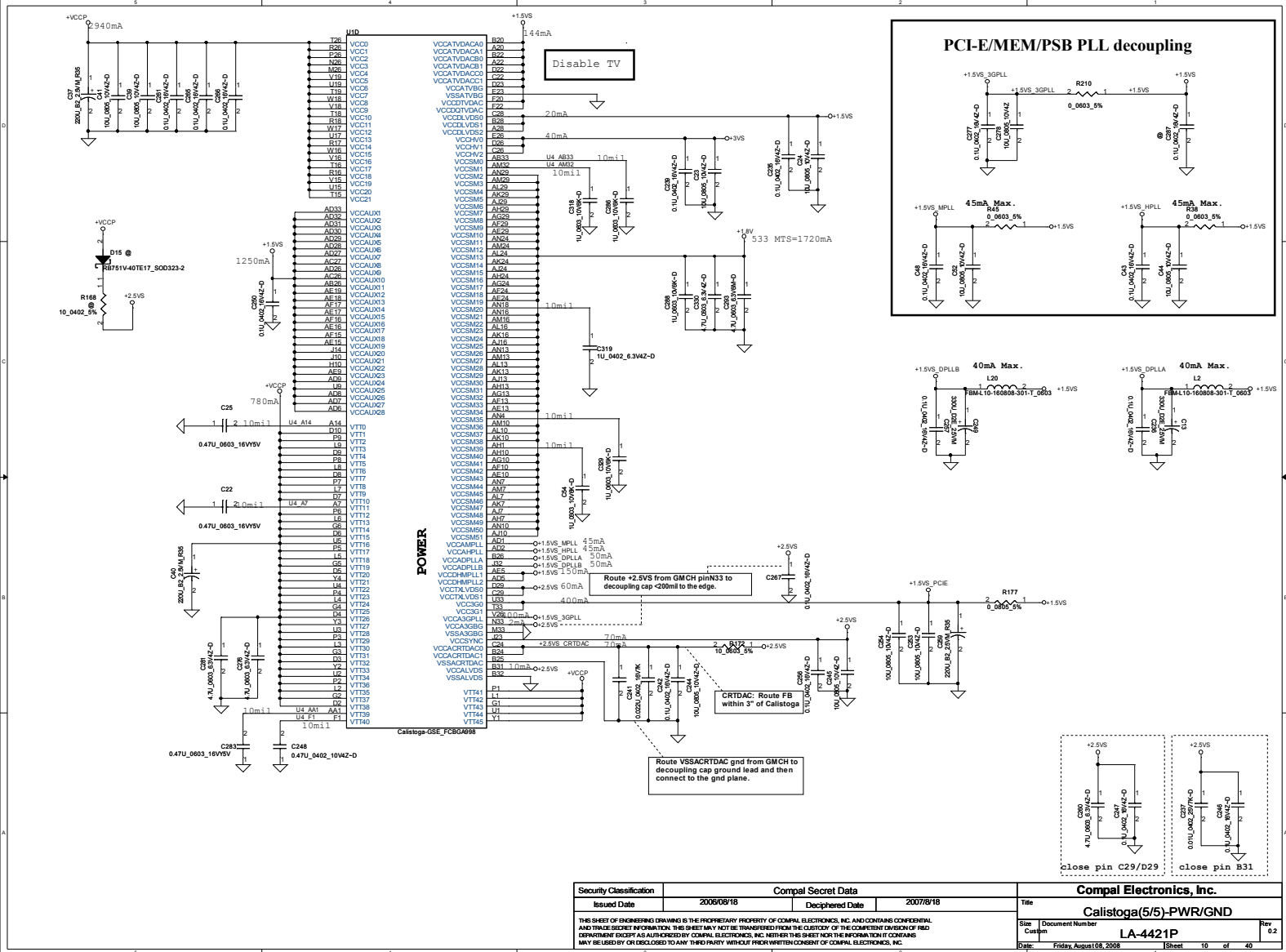


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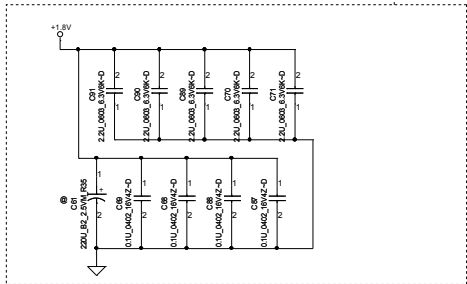


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						Size		Document Number		Rev	
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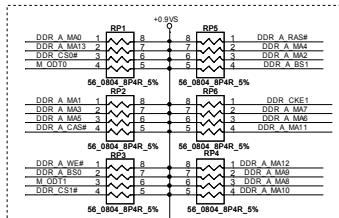
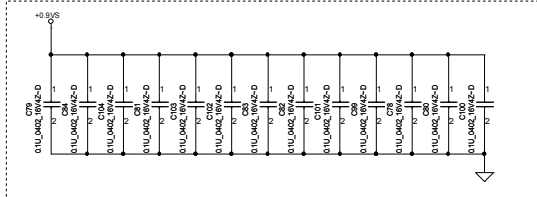


<7> DDR_A_DQS#0..7
<7> DDR_A_DP0..63
<7> DDR_A_DM0..7
<7> DDR_A_DQS#0..7
<7> DDR_A_MA0..13

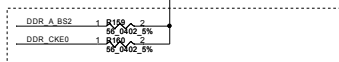
Layout Note:
Place near JDIM1



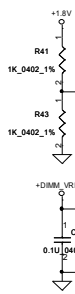
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



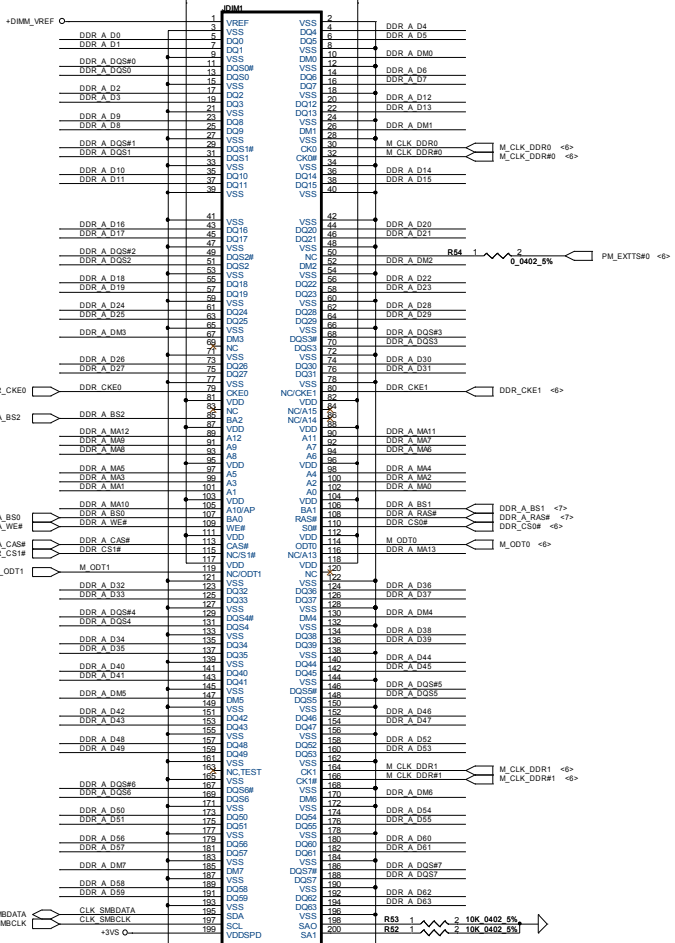
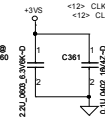
Layout Note:
Place these resistor closely DIMM0, all trace length <750 mil



Layout Note:
Place these resistor closely DIMM0, all trace length Max=1.3"

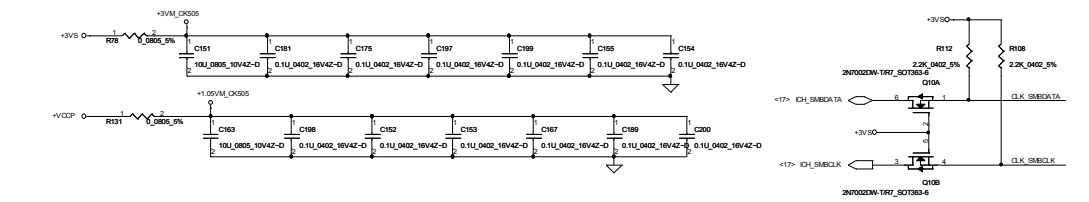


Share +DIMM VREF for
1. DDRII VREF
2. GMCR SM_VREF_0
SM_VREF_1

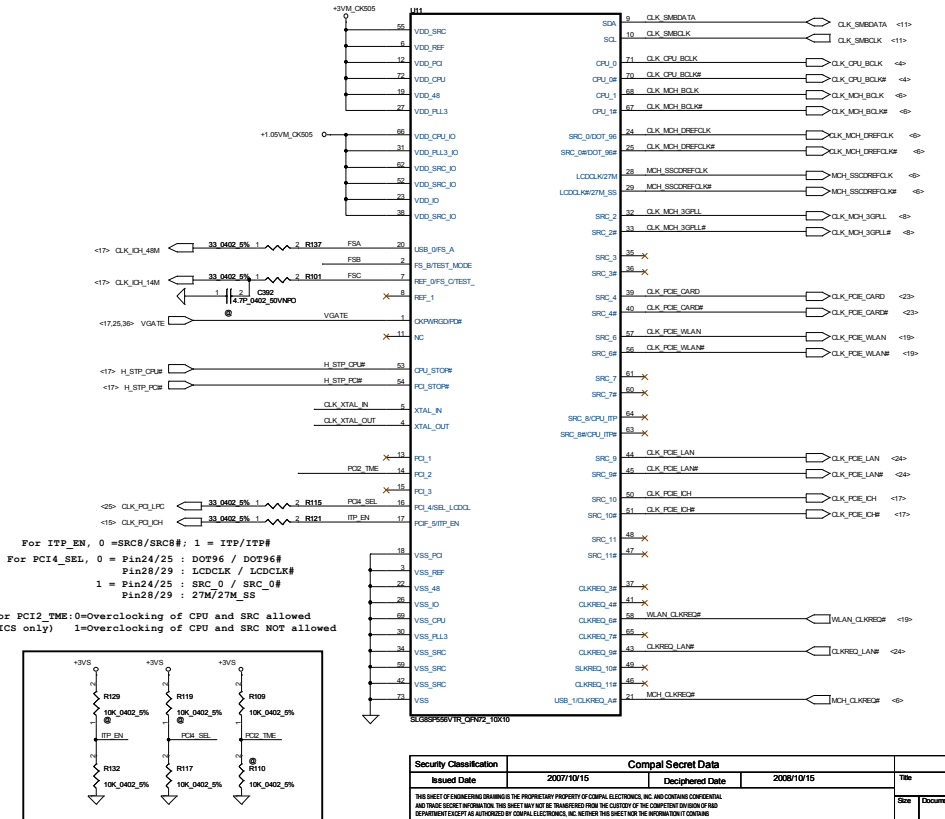


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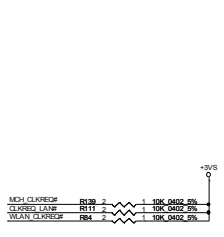
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



SA000020K00 (Silego : SLG8SP556VTR)
SA000020H10 (ICS : ICS9LPRS387AKLFT)



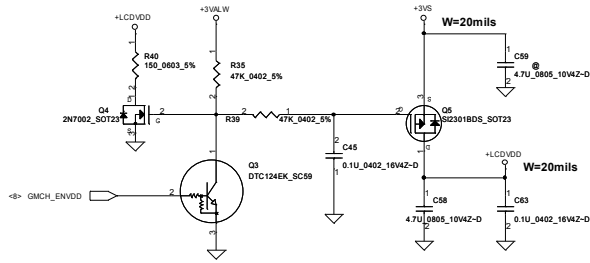
PORT	DEVICE
SRC0	MCH DREFCLK
SRC2	MCH 3GPPLL
SRC3	
SRC4	PCIE CARDREADER
SRC6	PCIE WLAN
SRC7	
SRC8	PCIE LAN
SRC9	PCIE ICH
SRC10	
SRC11	



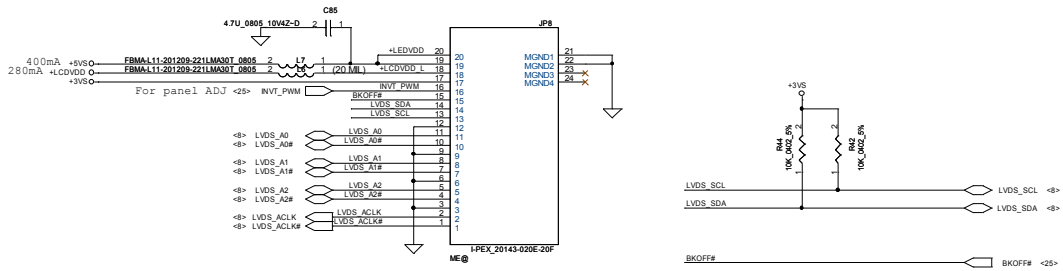
PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	PCIE WLAN
REQ_7#	
REQ_9#	PCIE LAN
REQ_10#	
REQ_11#	
REQ_A#	MCH 3GPPLL

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LCD POWER CIRCUIT

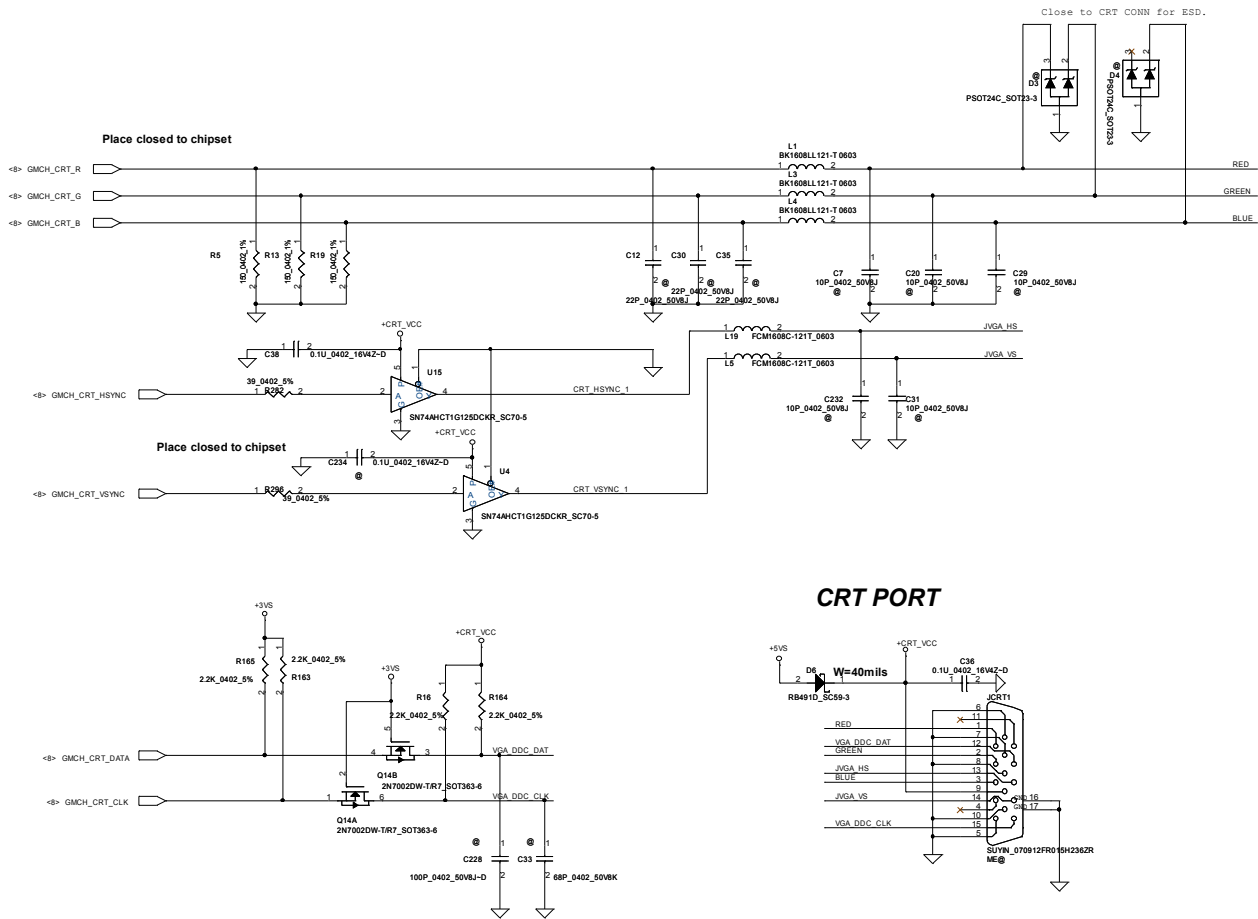


LCD/PANEL BD. Conn.

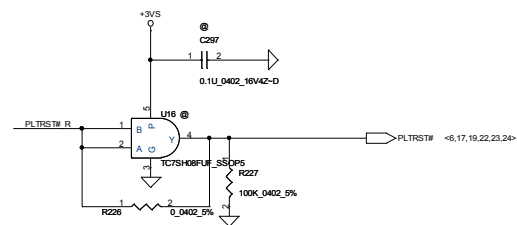
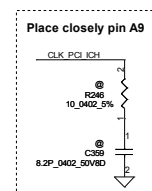
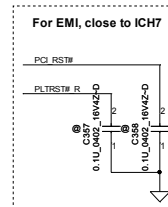
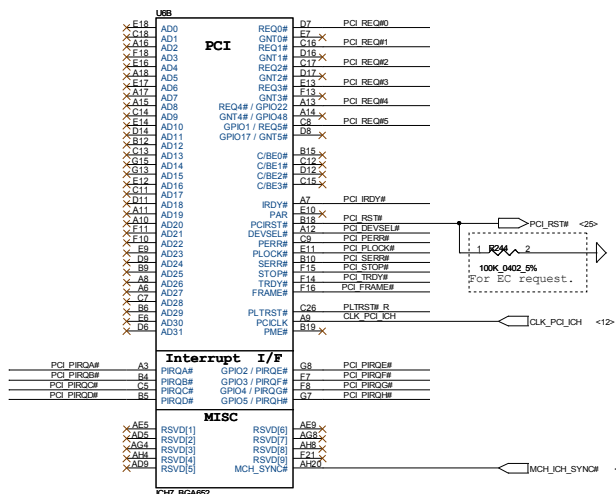
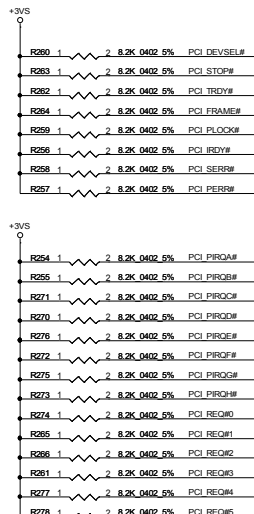


Coaxial LVDS Conn

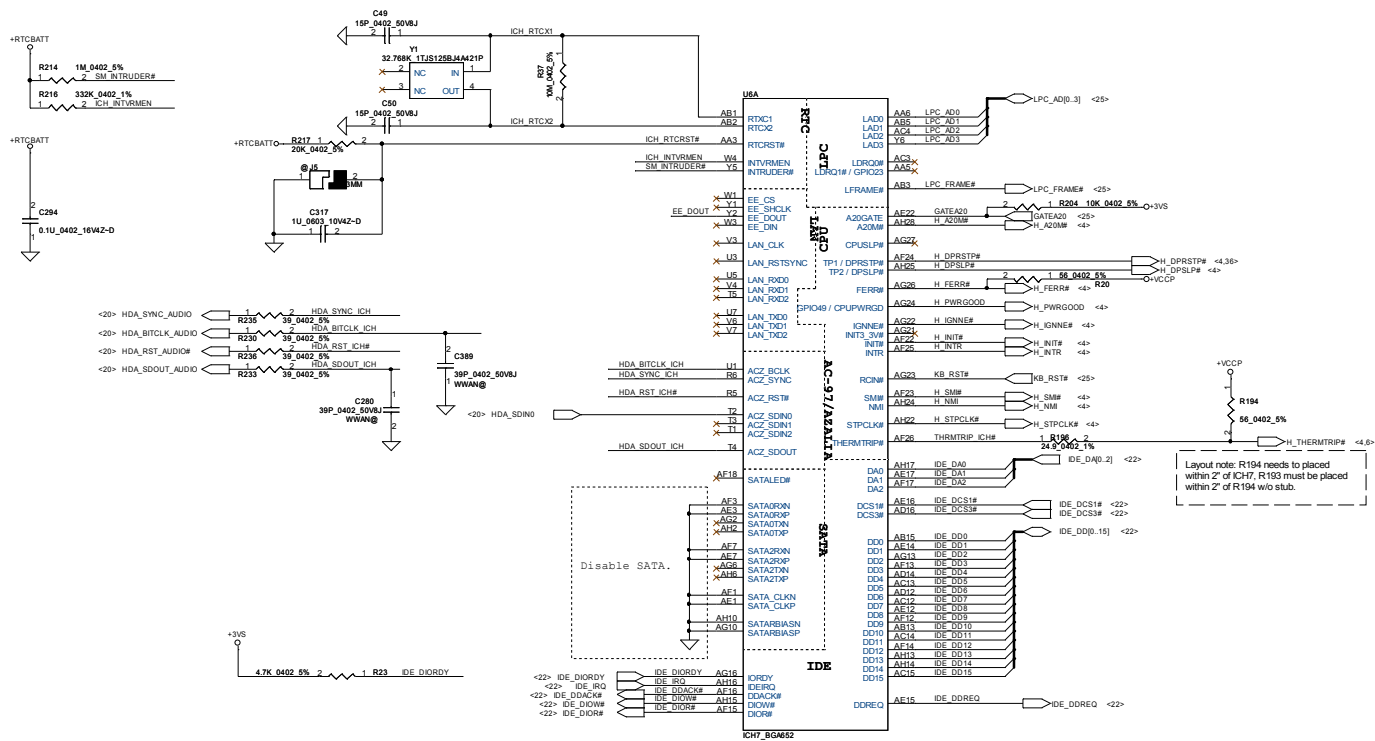
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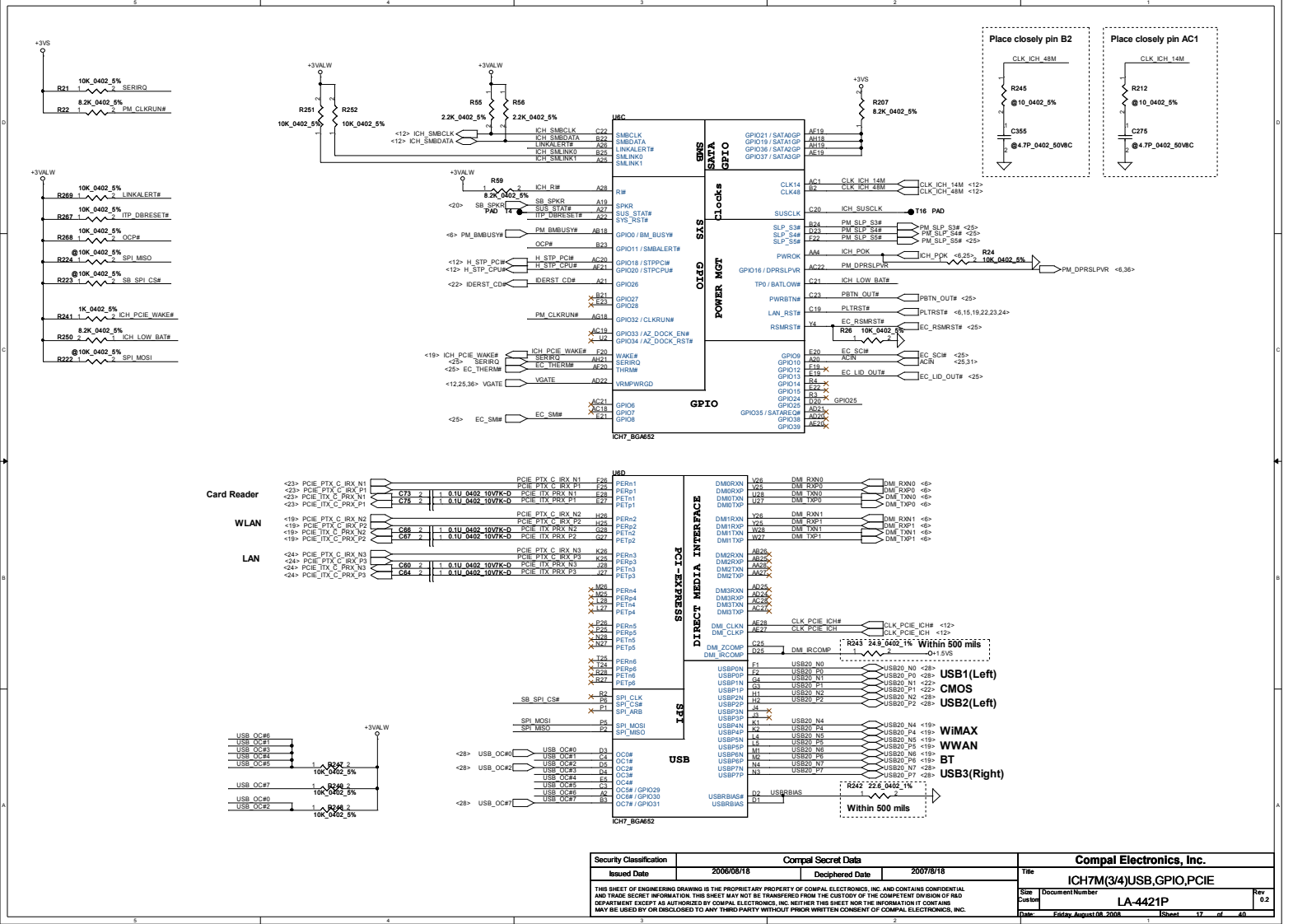
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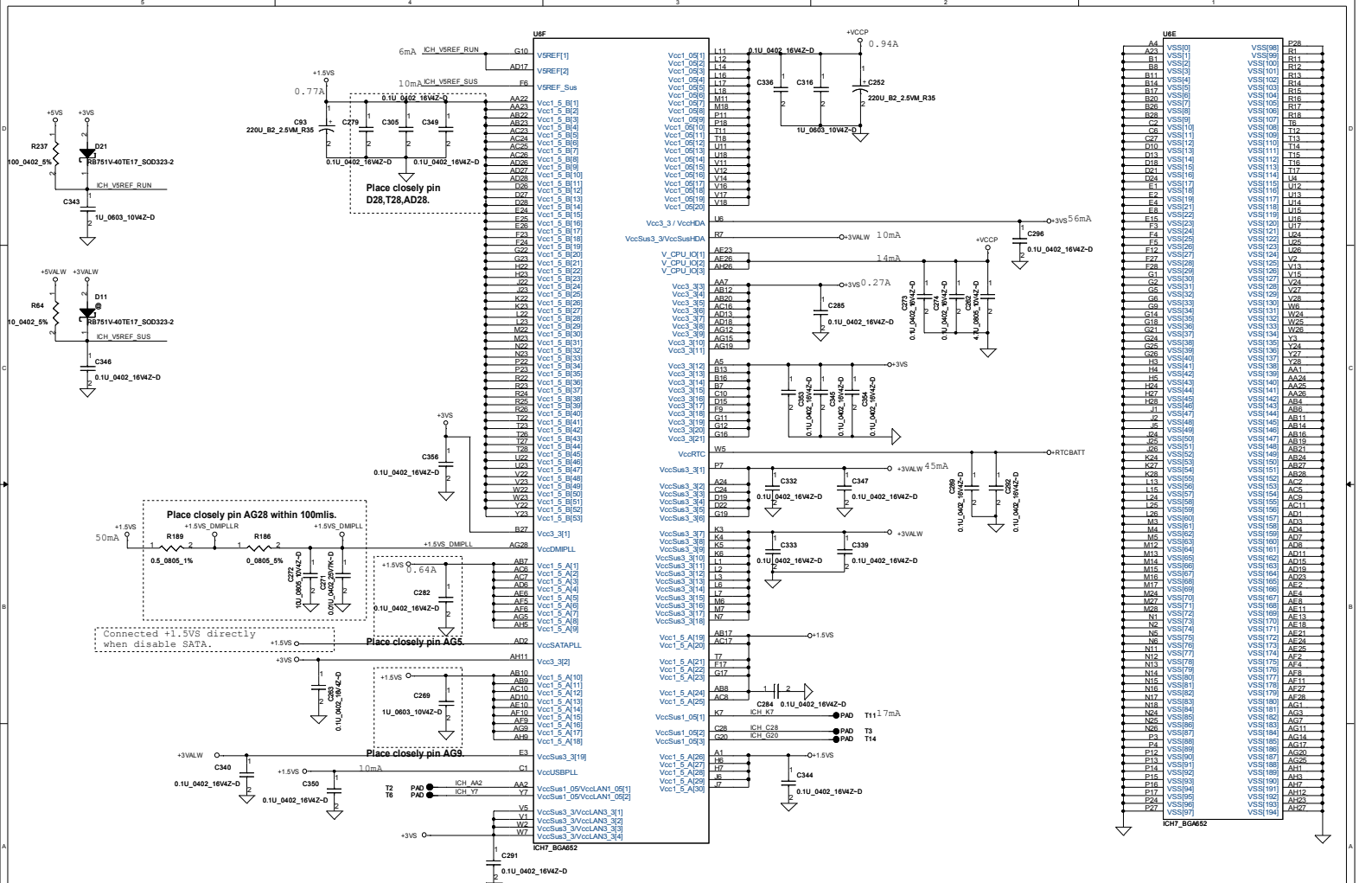
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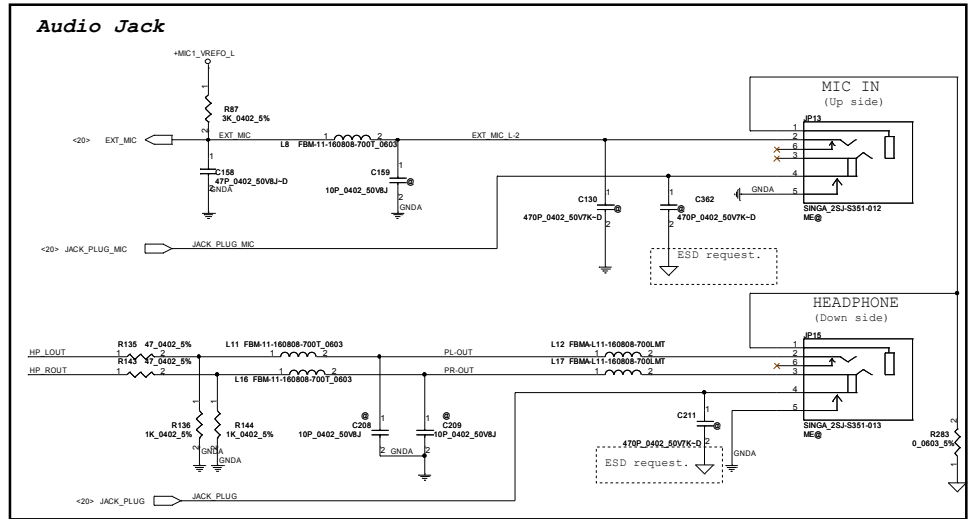
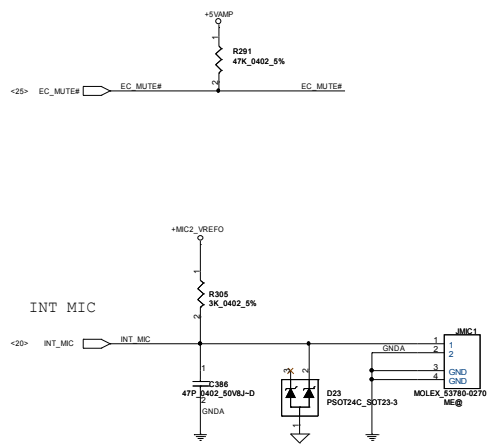
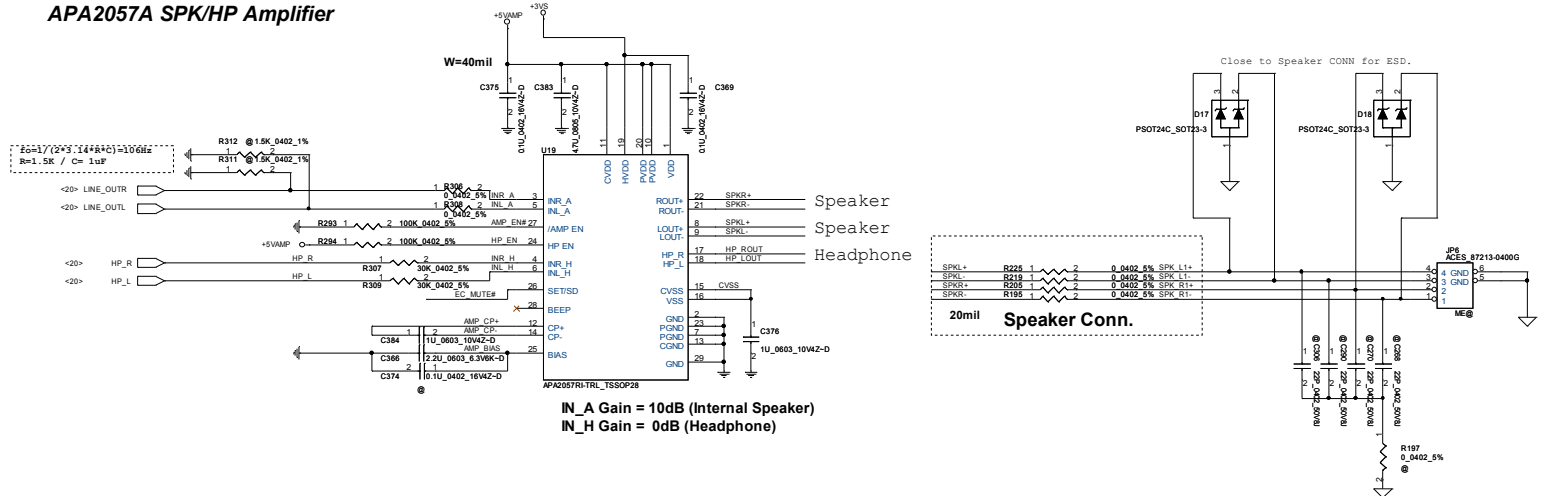
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The schematic diagram illustrates the power and signal architecture of the ACES 6810-6204 ME8 module. At the top, a 3V5 WLAN regulator is connected to a 0.1U_0402_16V4Z-D capacitor (C98) and a 0.1U_0402_25V7K-D capacitor (C113). A 47U_0805_10V4Z-D capacitor (C195) is connected to the 3V5 WLAN input. A 0.1U_0402_16V4Z-D capacitor (C121) is connected to the 3V5 WLAN output. A 0.1U_0402_16V4Z-D capacitor (C118) is connected to the 3V5 WLAN output. A 0.1U_0402_25V7K-D capacitor (C113) is connected to the 3V5 WLAN output. The bottom section shows a pin header (JP19) with 54 pins. Pins 1 through 54 are connected to various signals. Pins 1 through 10 are connected to ICH_PCIE_WAK#*. Pins 11 through 12 are connected to ICH_PCIE_WAK#. Pins 13 through 14 are connected to WLAN_ACTIVE. Pins 15 through 16 are connected to WLAN_CLKREQ. Pins 17 through 18 are connected to CLK_PCIE_WLAN#. Pins 19 through 20 are connected to CLK_PCIE_WLAN. Pins 21 through 22 are connected to PCIE_PTX_C_RX_N2. Pins 23 through 24 are connected to PCIE_PTX_C_RX_P2. Pins 25 through 26 are connected to PCIE_ITX_C_PRX_N2. Pins 27 through 28 are connected to PCIE_ITX_C_PRX_P2. Pins 29 through 30 are connected to EC_TX_P8B_DATA. Pins 31 through 32 are connected to EC_TX_P8B_CLK. Pins 33 through 34 are connected to EC_RX_P8B_CLK. Pins 35 through 36 are connected to EC_RX_P8B_DATA. Pins 37 through 38 are connected to GND1. Pins 39 through 40 are connected to GND2. Pins 41 through 42 are connected to 3V5 WLAN. Pins 43 through 44 are connected to 3V5 WLAN. Pins 45 through 46 are connected to 3V5 WLAN. Pins 47 through 48 are connected to 3V5 WLAN. Pins 49 through 50 are connected to 3V5 WLAN. Pins 51 through 52 are connected to 3V5 WLAN. Pins 53 through 54 are connected to 3V5 WLAN. The module is labeled ACES 6810-6204 ME8.

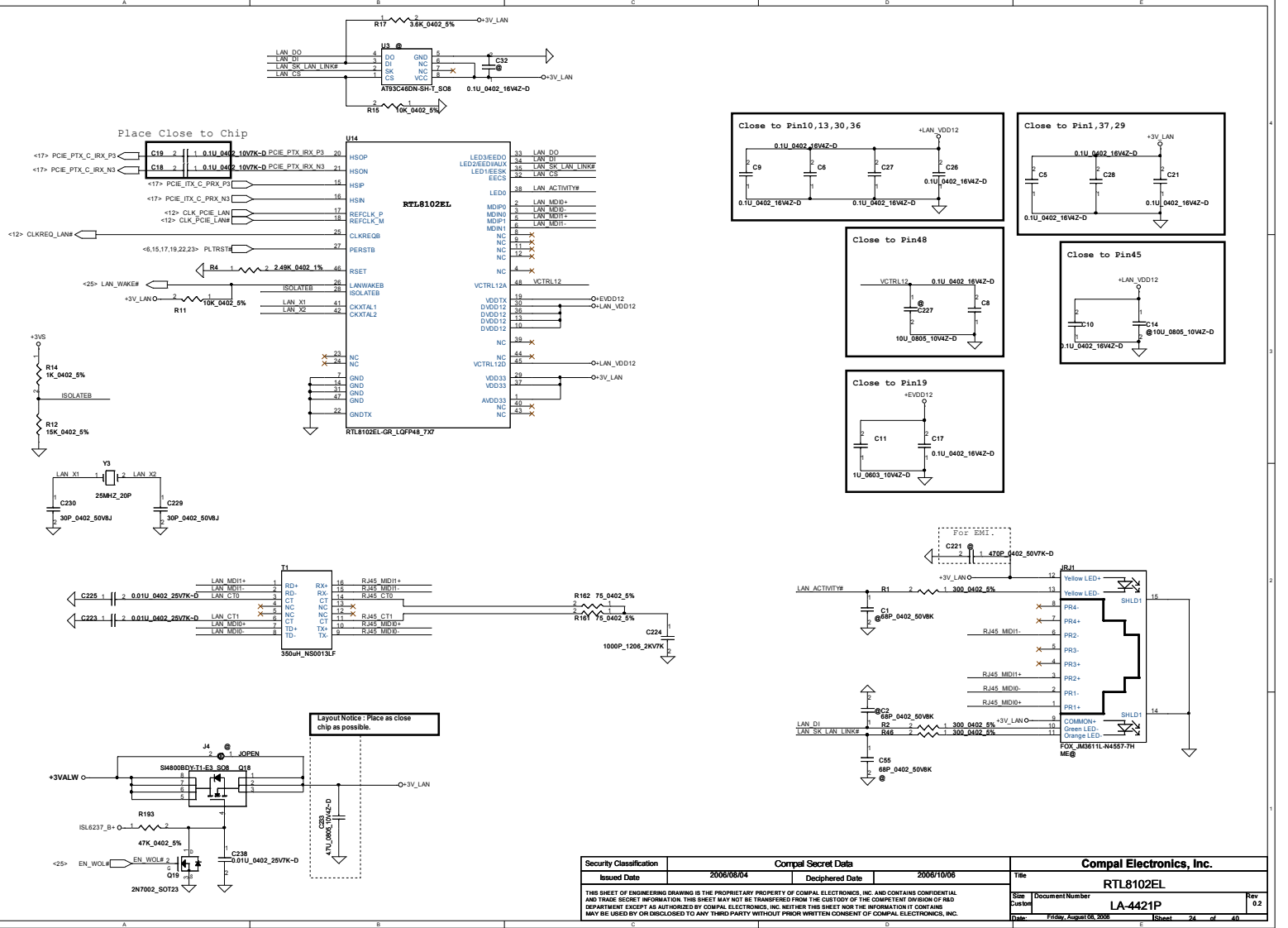
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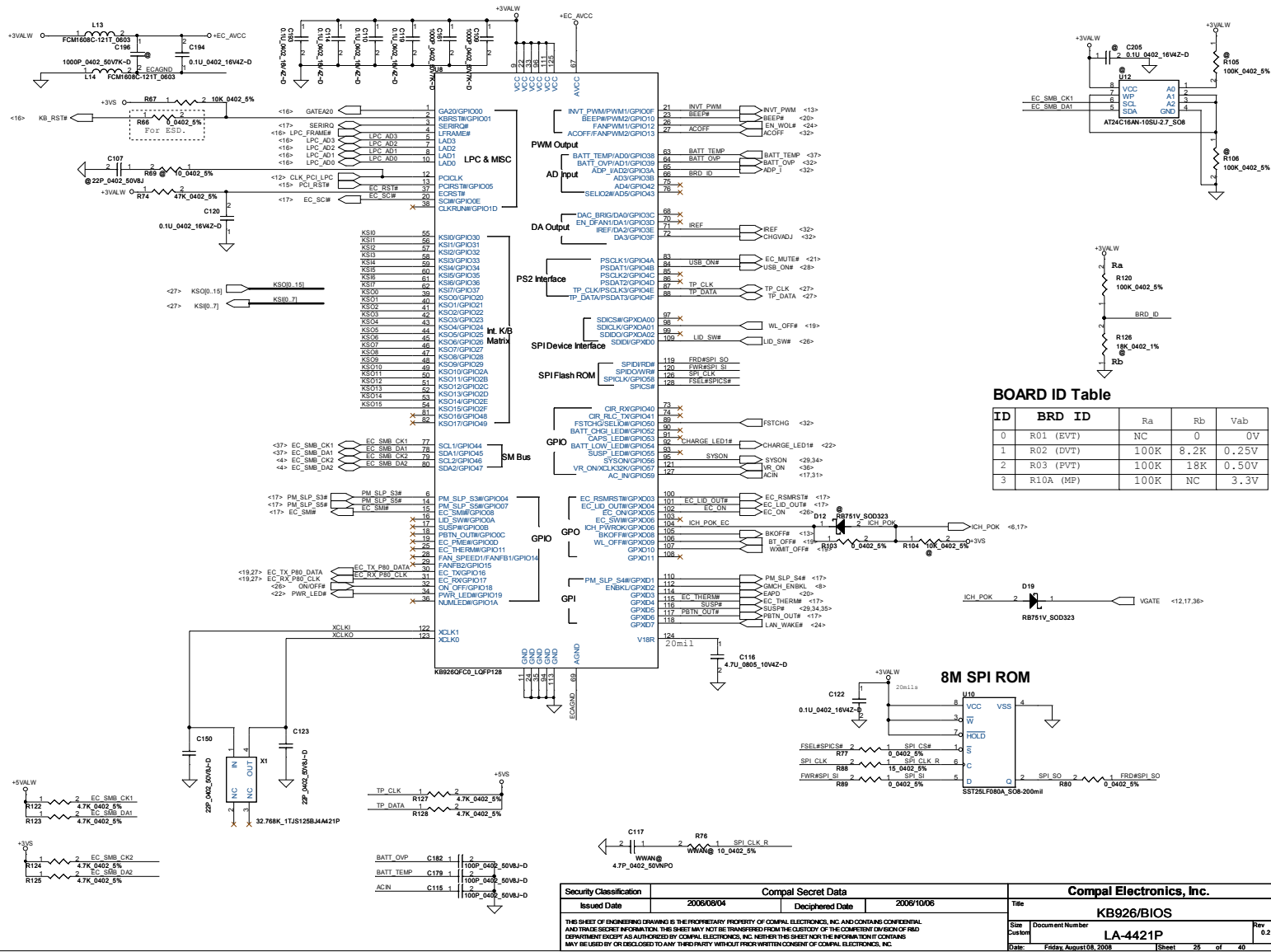
APA2057A SPK/HP Amplifier

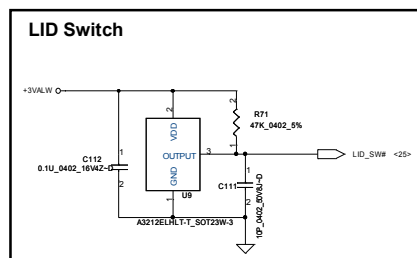


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				Date	LA-4421P
				Drawn	1997, August 08
				Sheet	21 of 40

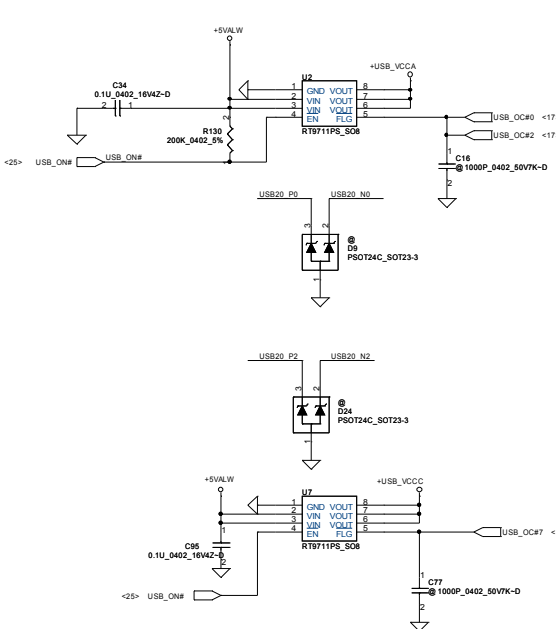


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2006/06/04		2006/10/06		Rev	
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		Date		Friday, August 08, 2008	
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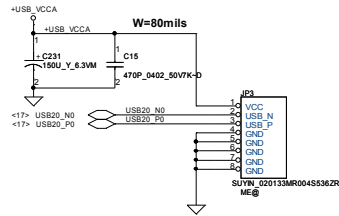




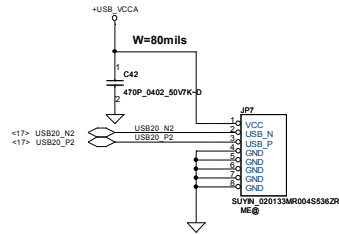
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	LID SW	
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				A	LA-4421P
				File	Release August 08 2008
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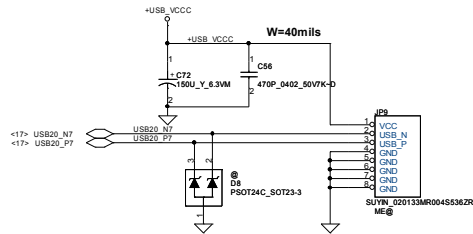
USB CONN. 1



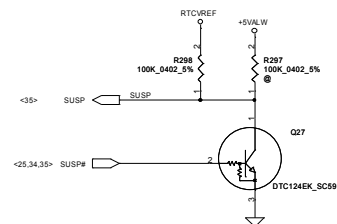
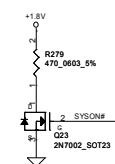
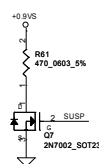
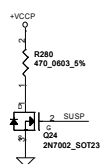
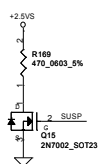
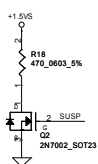
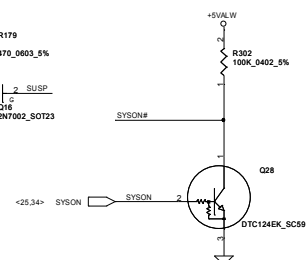
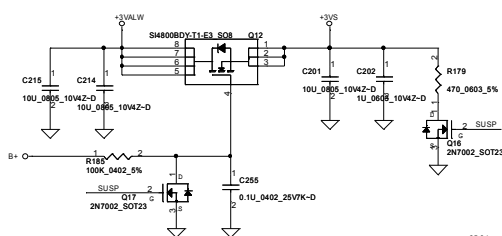
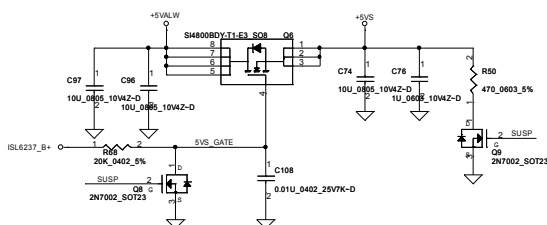
USB CONN. 2



USB CONN. 3



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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H23
H
 H_5P6X3P6N

H15
H
 H_3P6X5P6N

H7
H
 H_9P0X6P0N

H4
H

H_3P6

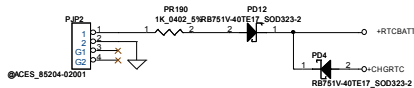
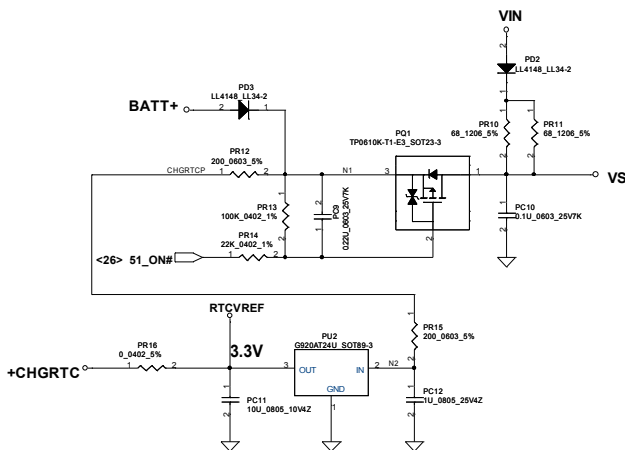
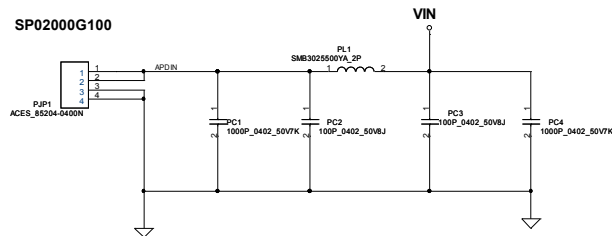
H20 H19 H11 H18 H10 H8 H9 H21 H13 H12
H H H H H H H H H H
         
H_3P2

H3 H22 H16 H1 H28 H27 H17 H26 H14 H25 H6 H5 H2
H H H H H H H H H H H H H H
            
H_2P8

FMD FM FM5 FM5 FMD FMH
      FIDUCIAL_C40M80

Security Classification		Compal Secret Data			Compal Electronics, Inc.		
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							Screw
							LA-4421P
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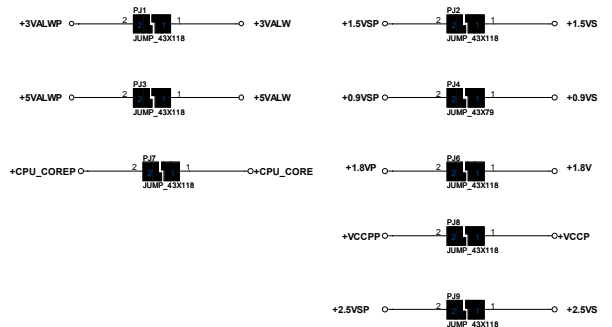
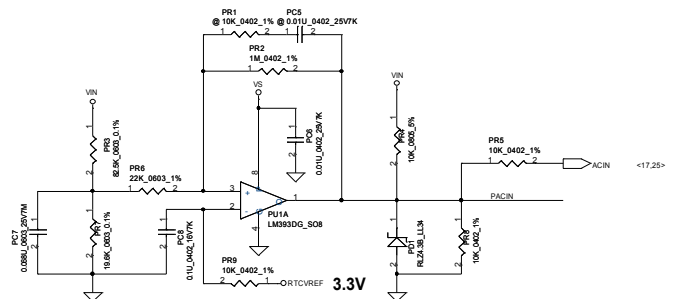
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SP02000D000

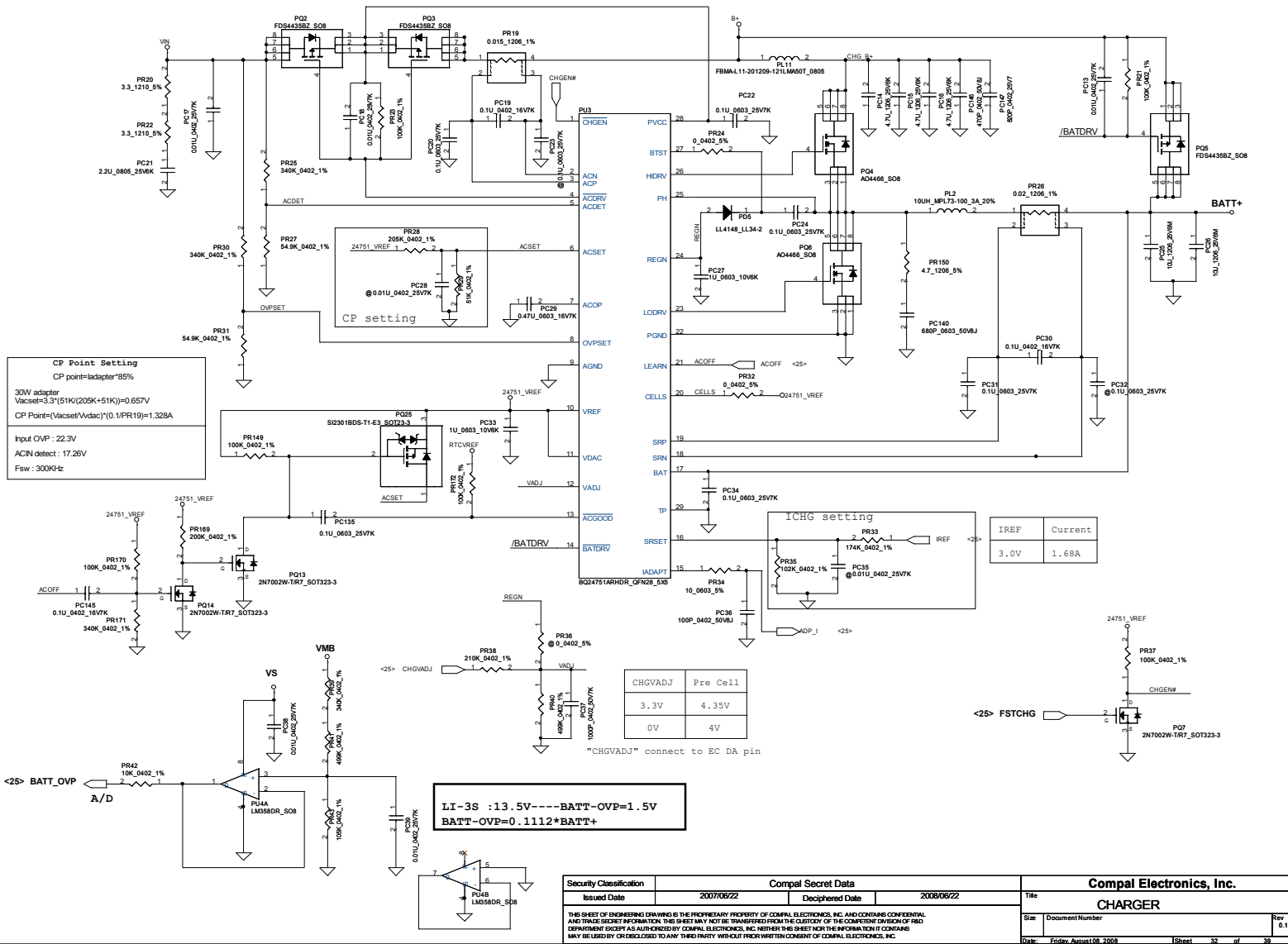
Vin Detector

High 18.059 17.841 17.624
Low 17.418 17.210 16.998

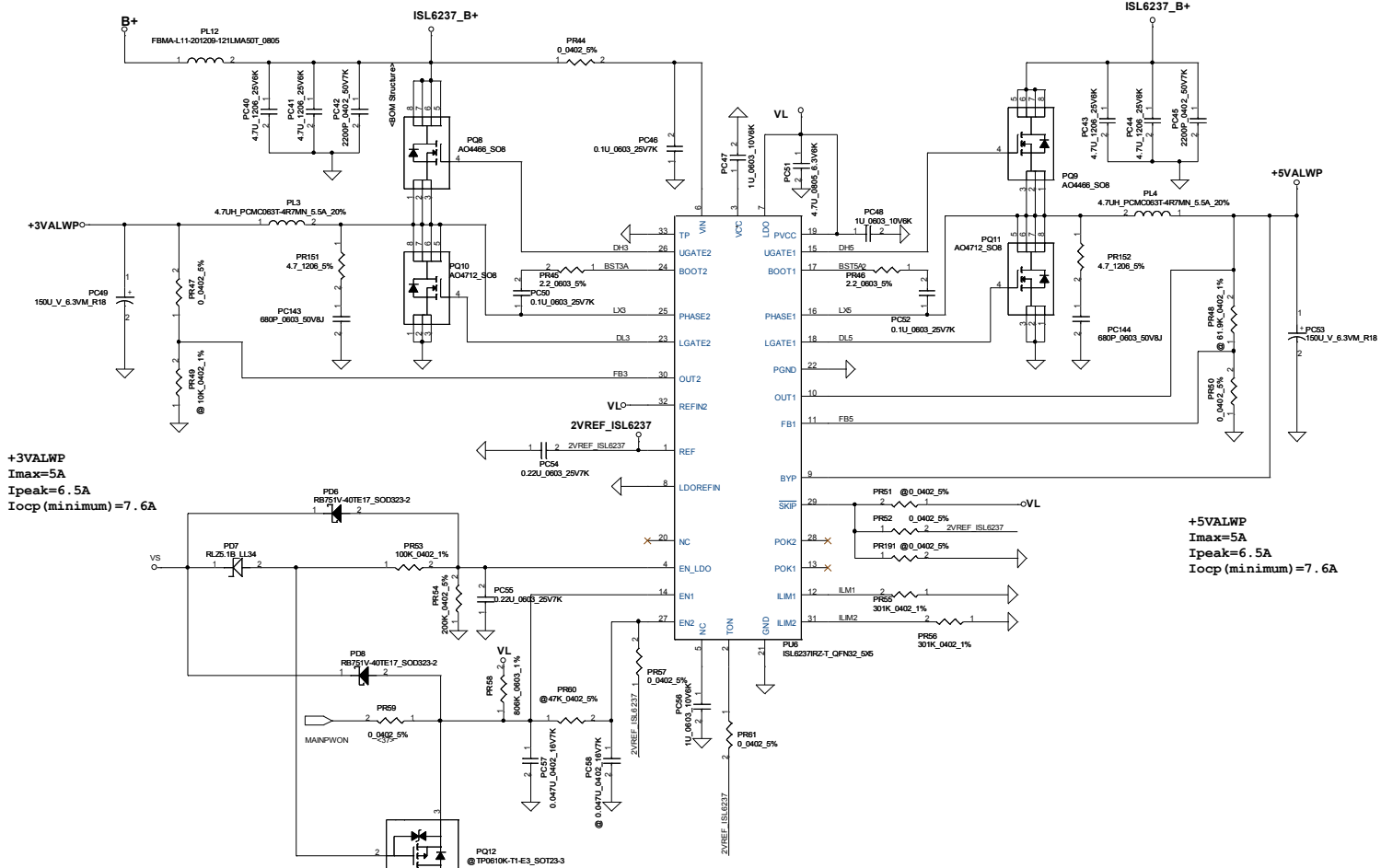


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				DCIN & DETECTOR	
				Size	Rev
				Custom	0.1
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				Sheet	31 of 30

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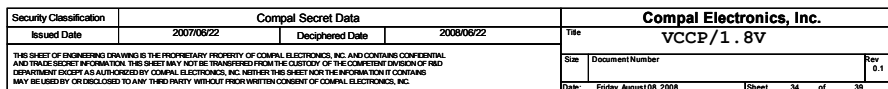
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Issued Date	2007/08/22	Deciphered Date	2008/06/22	Title	CHARGER
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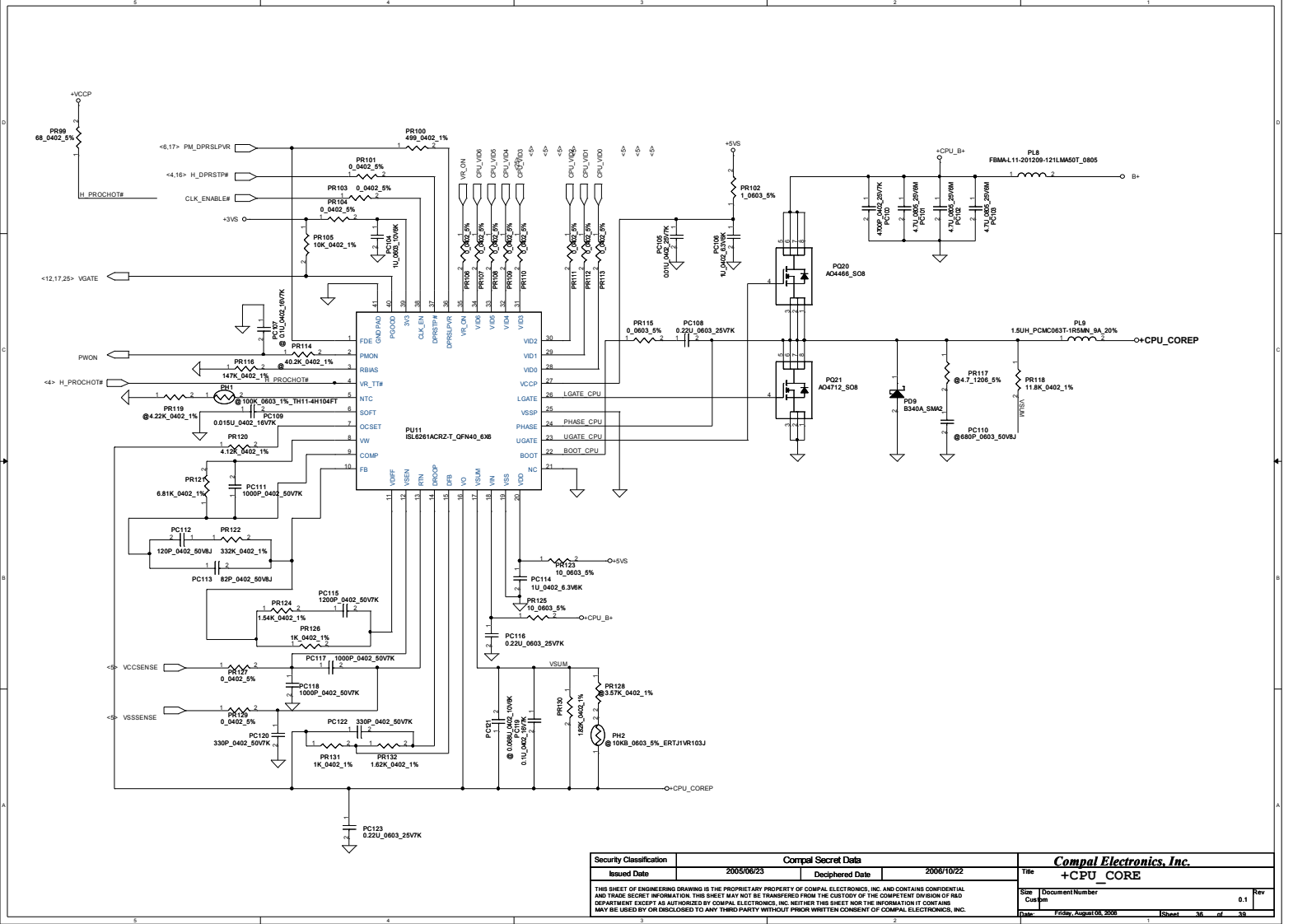


+3VALWP
Imax=5A
Ipeak=6.5A
Iocp (minimum)=7.6A

+5VALWP
Imax=5A
Ipeak=6.5A
Iocp (minimum)=7.6A

Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		3V/5V	
2007/06/22		2008/06/22			
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Item	Fixed Issue	Rev.	PG#	Modify List
1	Deleted Kill switch circuit.	0.2	P26	1.Deleted R60,C85,SW2
2	Changed to Dell PN.	0.2	--	1.Change C305,309,310,311,312,313,314,315,320,321,322,323,324,325,326,327,337,341 from SE000000K80 (0402) to SE000000K8L (0402) 2.Change C46,47,298,299,300,301,302,303,304,328,334,335 from SE000005TM8 (0603) to SE00000480L (0805) 3.Change C22,25,248,283 from SE1244748K0 (0402) to SE027474Z8L (0603) 4.Change C108,255,238 from SE042104R80 (0603) to SE068103K8L (0402) 5.Change C11,369,376,384 from SE100105Z80 (0402) to SE052105Z8L (0603) 6.Change C44,52 from SE077106M80 (1206) to SE053106Z8L (0805) 7.Change C373 from SE054106Z80 (1206) to SE053106Z8L (0805) 8.Change C260,276,281,293,330 from SE107475K80 (0603) to SE053475Z8L (0805) 9.Change C92 from SE064225R80 (0805) to SE107225K8L (0603) 9.Change C54,286,288,318,319,329 from SE100105Z80 (0402) to SE080105K8L (0603)
3	Use LAN internal EEPROM and CLKREQ	0.2	P24	Unstuff U3 C32 R173 stuff R170 R111
4	LCD sequence	0.2	P13	Change R35,39 to 47K ohm and C45 to 0.1u
5	Changed to Dell PN.	0.2	P28	U2,7 change from SA00001H600 (Dell not approve) to SA000017B00 part
6	Add C390 and 391 for SSD	0.2	P22	Add C390 and 391 and udstuff C59 for SSD
7	Follow LAN report	0.2	P24	Short C22,226, C229,230 change from 27p to 30p
8	Follow checklist	0.2	P10	Delete C280
9	Changed to Dell PN.	0.2	P6	Change R167,180 to SD000000680L
10	Follow power sequence	0.2	--	Unstuff D11 D15 R168 SW1
11	Change symbol	0.2	P11	Update DIMM termination to 8P4R
12	Remove LED function	0.2	--	Delete Q25,26,11,22,LED3,R159,JF4 Change LED2 to white
13	EC code for B phase	0.2	P25	R126 change 0ohm to 8.2k ohm and stuff R120
14	For derating report	0.2	P20	Change R148,149,150,152 to 10k ohm
15	EA test	0.2	P25	C123,150 change from 15p to 22p
16	EA test	0.2	P23	Change R295 to 9.1k ohm
17	EA test	0.2	P14	GMCH_CRT_VSYNC and GMCH_CRT_HSYNC add R282,296 390ohm
18	single part	0.2	P24	R193 change to 47k ohm
19	SPEC change	0.2	P19	Change BT pin define
20	improve power consumption	0.2	P29	Change R298 to 100K
21		0.2	P25	Unstuff C194
22	ME change	0.2	P13	Change LVDS connect to 20pin
23	Dell request	0.2	--	Change M/B to OSP
24		0.2	P22	Delete LPC debug connect (JP20,R102,296)
25		0.2	P13	Add C85 for +LEDVDD, Delete R46,C55
26		0.2	P21	Delete L21,C383 change to 4.7u,unstuff C374,R291 change to 47k ohm
27		0.2	P20	Change U20 to Anpec and Delete R304,310 change C373,387 to 1u Delete L18,unstuff C372,Change C369 to 0.1u
28	Change EC susp# to 116 pin PBTN_out# to 117 pin LID_SW# to 109 pin EC_PWM# to 118 pin			Change EC_Therm# 25 to 115 pin BT_OFF# 98 to 106 pin WL_OFF# 106 to 98 pin
29				Delete R290,285
30	DPX request	0.3	P21	Change JP13,15 PCB footprint from SINGA 28U-B351-012_6P to FOX JW63331-B350-7F_6P
31	EC code for C phase	0.3	P25	R126 change 18Kohm
32	ENE request	0.3	P25	C116 change to 1u
33		0.3		Delete R215, Change netname +RTCVCC to +RTCBATT ,Add J6 D18, C191 with C185 switch,
34	EMI request	0.3		Add C389
35	LAN LED	0.3		Add R46 and C55 LAN LED add orange
36	ENE request	1.0	P25	C116 change to 4.7u
37		1.0		Delete J1,J3,SW1,JF18
38		1.0		C127 change to 1000p

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Compal Electronics, Inc.

Title		HW PIR	
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Cahnge RTC battery to CR2032.	To meet customer specification (3 years).	R.02	31	Add PD12 (RB751) and PR190 (1K).	20080428	DVT
2	Adjust Vin detector setting.	Change Vin "High==>Low" voltage from 14.355V to 17.210V.	R.02	31	Change PR6 to 22K and PR7 to 19.6K.	20080428	DVT
3	Adjust VCCP OCP setting.	Change VCCP OCP to 9A.	R.02	34	Cahnge PR87 and PR93 to 24K and PC86 to 6800P.	20080428	DVT
4	Adjust 1.8V output voltage.	Change 1.8V power rail voltage from 1.8V to 1.828V.	R.02	34	Change PR88 from 34K to 33.2K.	20080428	DVT
5	Change Vin and battery discharge MOSFET.	Due to SI4835BDY will EOL, so, we change to Compal standard 2nd source, FDS4435BZ.	R.02	32	Change PQ2, PQ3 and PQ5 from SI4835BDY to FDS4435BZ.	20080428	DVT
6	Change battery connector.	The new battery connector has screw hole.	R.02	32	Change battery connector.	20080430	DVT
7	Power board-band.	EMI requests to add soltion to reduce power board-band.	R.02	32 33 34	Change PJ10,PJ11 and PJ14 from Jump to bead. Change PR45,PR46,PR96 and PR97 from 0 ohm to 2.2 ohm. Add PR151,PR152,PC143,PC144,PR147,PR148,PC131,PC132,PC146,PC147, PR150 AND PC140.	20080506	DVT
8	Modify CPU CORE OCP.	Change CPU CORE OCP from 10A to 7A.	R.02	36	Change PR120 from 5.9K to 4.12K.	20080514	DVT
9	Remove PR16 and PR17.	Change RTC battery, so, remove PR17 and PR16.	R.03	31	Delete PR17 and change PR16 to 0 Ohm.	20080605	FVT
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	
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				Rev 0.1	
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Item	Fixed Issue	Rev.	PG#	Modify List
1	Deleted Kill switch circuit.	0.2	P26	1.Deleted R60,C85,SW2
2	Changed to Dell PN.	0.2	--	1.Change C308,309,310,311,312,313,314,315,320,321,322,323,324,325,326,327,337,341 from SE000000K80(0402) to SE000000K8L(0402) 2.Change C46,47,298,299,300,301,302,303,304,328,334,335 from SE000005TM8(0603) to SE00000480L(0805) 3.Change C22,25,248,283 from SE1244748K0(0402) to SE02747428L(0603) 4.Change C108,255,238 from SE042104K80(0603) to SE068103K8L(0402) 5.Change C11,369,376,384 from SE100105Z80(0402) to SE052105Z8L(0603) 6.Change C44,52 from SE077106M80(1206) to SE053106Z8L(0805) 7.Change C373 from SE054106Z80(1206) to SE053106Z8L(0805) 8.Change C260,276,281,293,330 from SE107475K80(0603) to SE053475Z8L(0805) 9.Change C92 from SE064225K80(0805) to SE107225K8L(0603) 9.Change C54,286,288,318,319,329 from SE100105Z80(0402) to SE080105K8L(0603)
3	Use LAN internal EEPROM and CLKREQ	0.2	P24	Unstuff U3 C32 R173 stuff R170 R111
4	LCD squence	0.2	P13	Change R35,39 to 47K ohm and C45 to 0.1u
5	LVDS connect	0.2	P13	LVDS connector change to 20 pins
6	Changed to Dell PN.	0.2	P28	U2,7 change from SA00001H600(Dell not approve) to SA000017B00 part
7	EA test	0.2	P23	Change R295 to 9.1k ohm
8	Follow LAN report	0.2	P24	Short C222,226, C229,230 change from 27p to 30p
9	Delete A -phase reserve	0.2	P20	Delete L18,
10	Changed to Dell PN.	0.2	P6	Change R167,180 to SD00000680L
11		0.2		Change M/B to OSP
12		0.2	--	Delete Q25,26,11,22,LED3,R159 Change LED2 to white
13	Remove LED function	0.2	P25	R126 change 0ohm to 8.2k ohm and stuff R120
14	EC code for B phase	0.2	P20	Change R148,149,150,152 to 10k ohm
15	For derating report	0.2	P25	C123,150 change from 15p to 22p
16	EA test	0.2	P13	Add C85 for +LEDVDD
17		0.2	P22	Delete LPC debug connect (JP20,R102,296)
18		0.2	P25	change SUSP# to U8.116 due to KB926 C0 bug
19	ENE	0.2	P22	add C390&C391 for Dell consign SSD
20	SSD	0.2	P22	add white LED
21	LED	0.2		
22		0.2		
23		0.2		
24				

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Compal Electronics, Inc.		
Title	HW PIR	
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