

Compal Confidential

HBL51 Schematics Document

Intel Yonah Processor with 945GM/940GML + DDRII + ICH7M

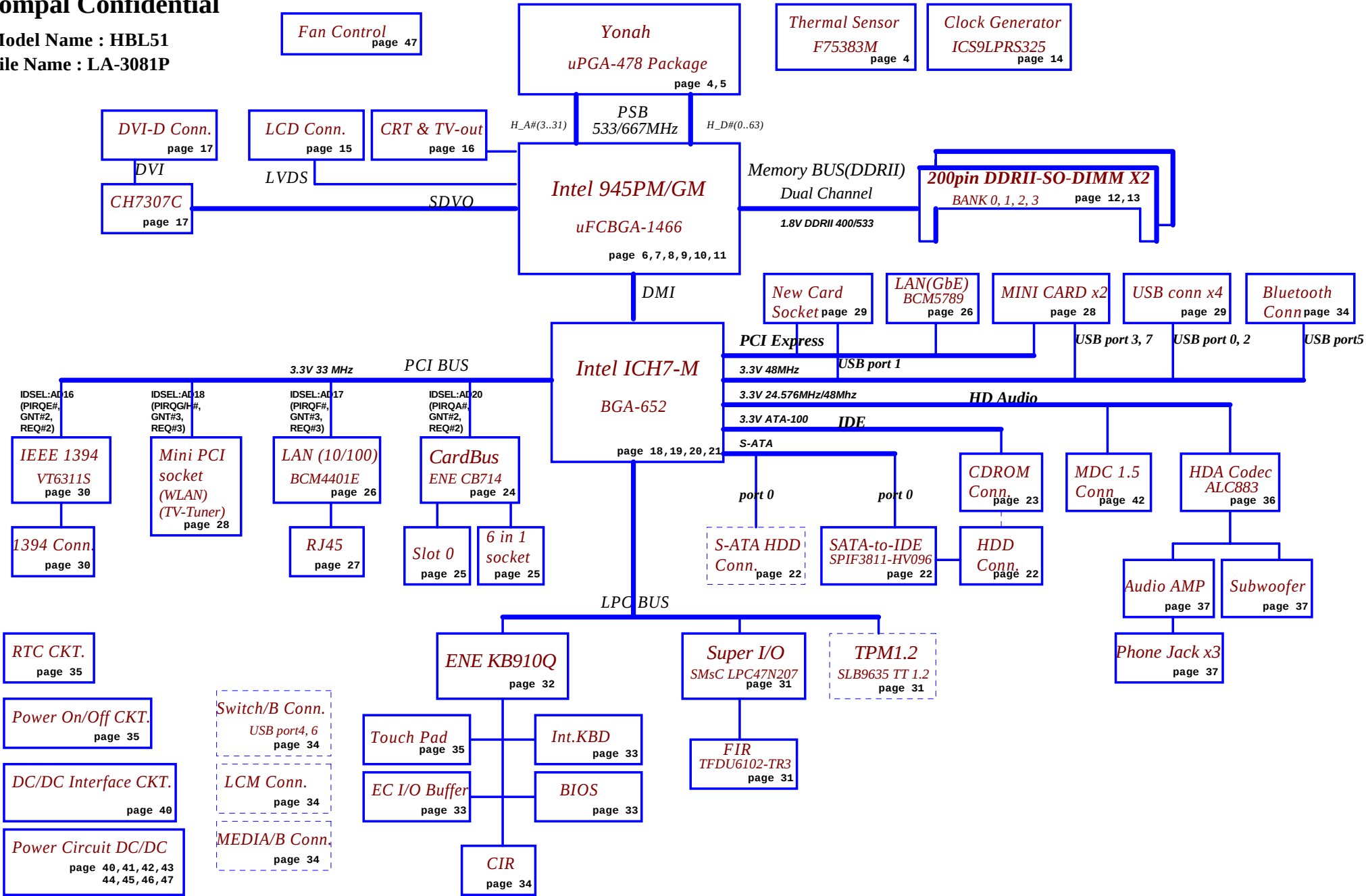
2006-10-04

REV: 5.0

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				Date: 星期四, 十月 05, 2006	Sheet 1 of 47

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Model Name : HBL51
File Name : LA-3081P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

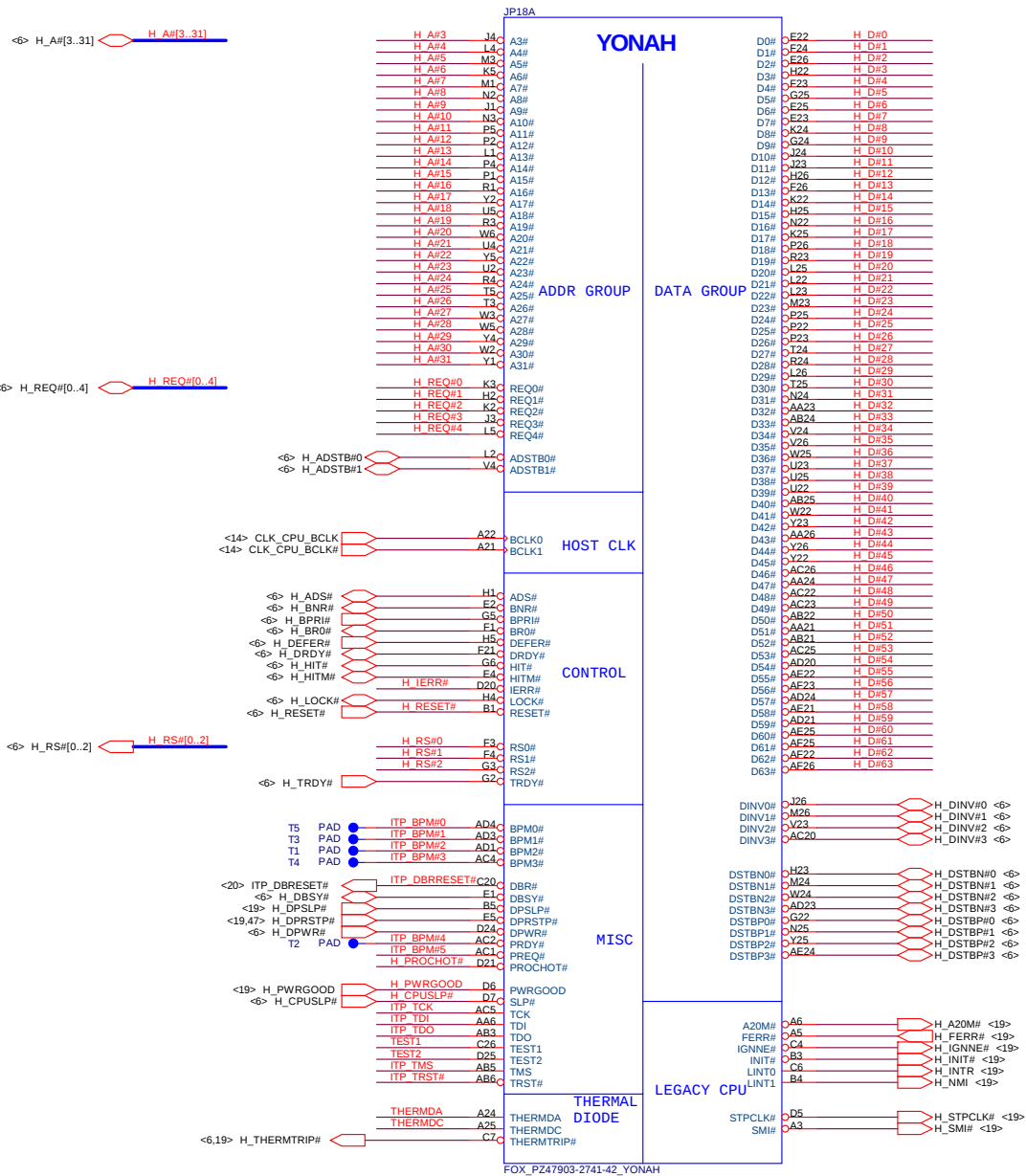
BTO Option Table

BTO Item	BOM Structure
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI CARD1	MINI1@
MINI CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
LCM	LCM@
TVOUT	TVOUT@
1394	6311S@
CARDREADER	4IN1@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@

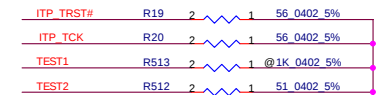
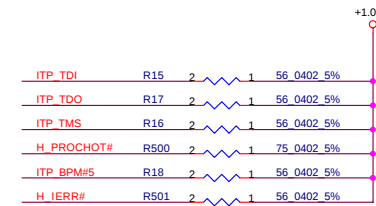
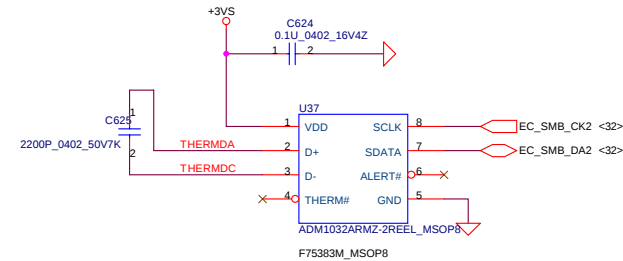
SKU ID Table

SKU ID	SKU
0	
1	GM
2	
3	
4	
5	
6	
7	

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				Date: 星期四, 十月 05, 2006	Sheet 3	of 47



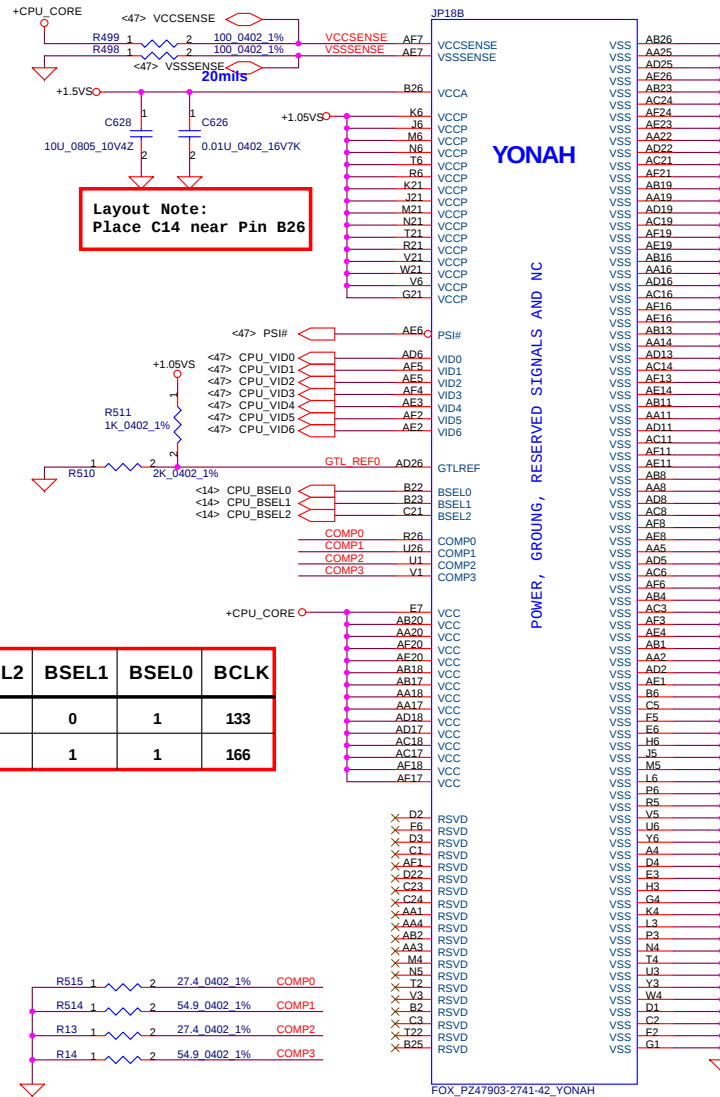
H_D#(0..63) H_D#(0..63) <6>



Layout Note:
THERMDA & THERMDC Trace / Space = 10 / 10 mil

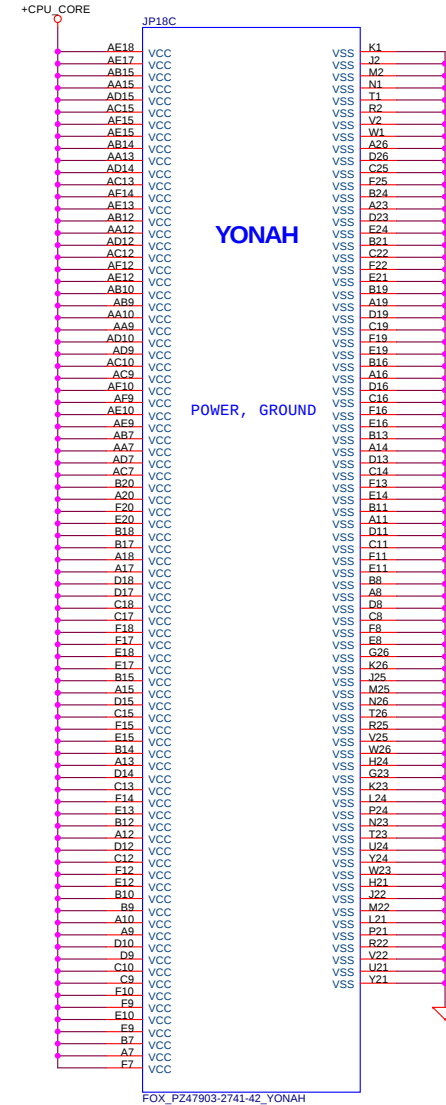
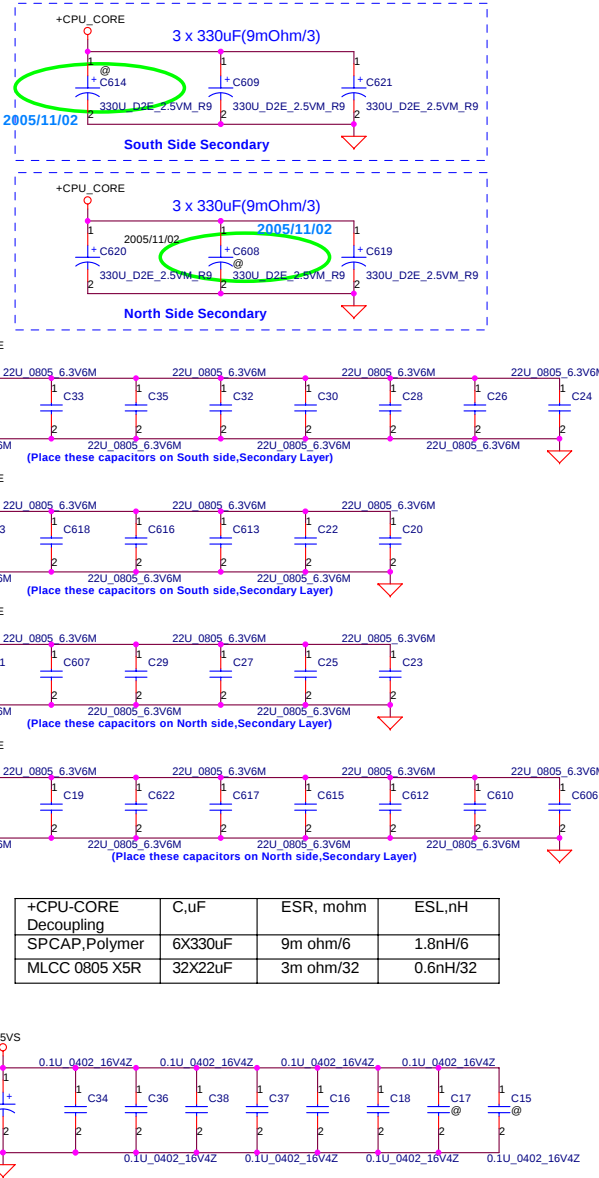
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Size	Document Number	Rev		Date	
Custom	401405	G		星期四, 十月 05, 2006	
Sheet		4		of	
47		1			

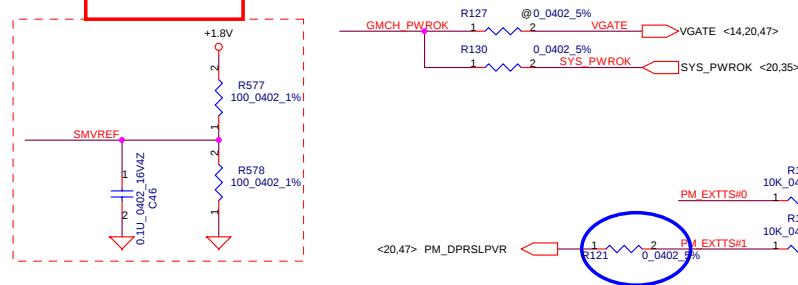
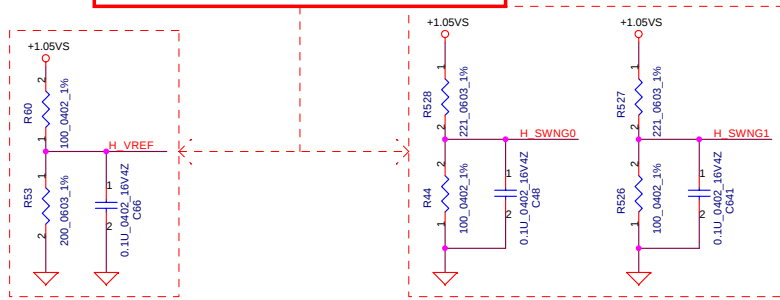
Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.40hms
with 50 mil spacing.
Place PU and PD within 1 inch of CPU.

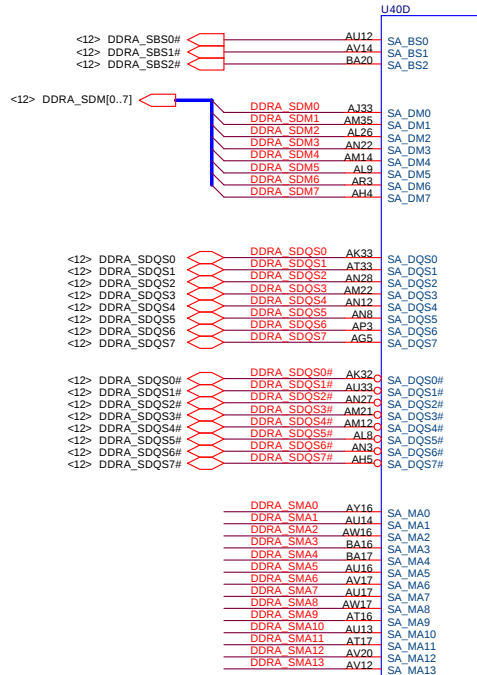
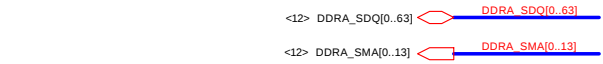


BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133
0	1	1	166

TRACE CLOSELY CPU < 0.5'
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.40hms)
COMP1, COMP3 layout : Space 25mils (550hms)



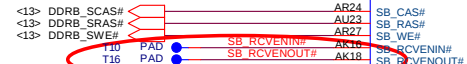
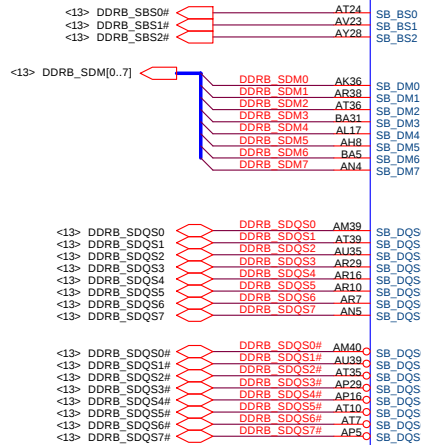
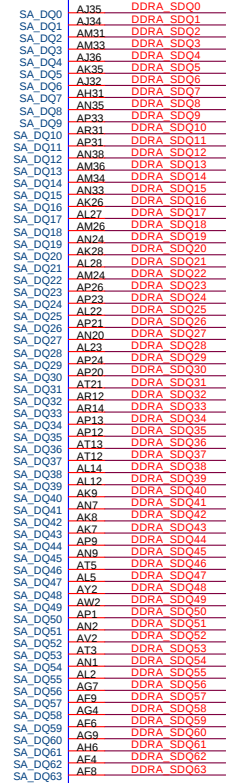




check layout

CALISTOGA_FCBGA1466-D

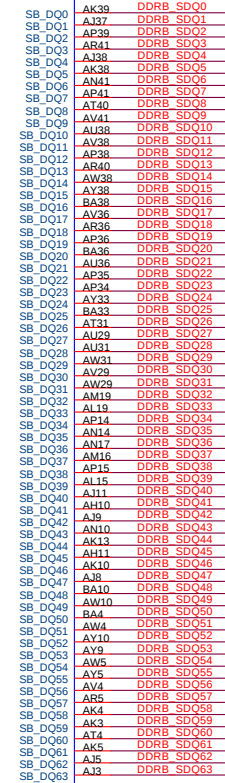
DDR SYS MEMORY A



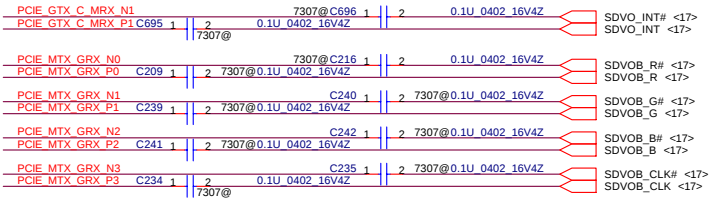
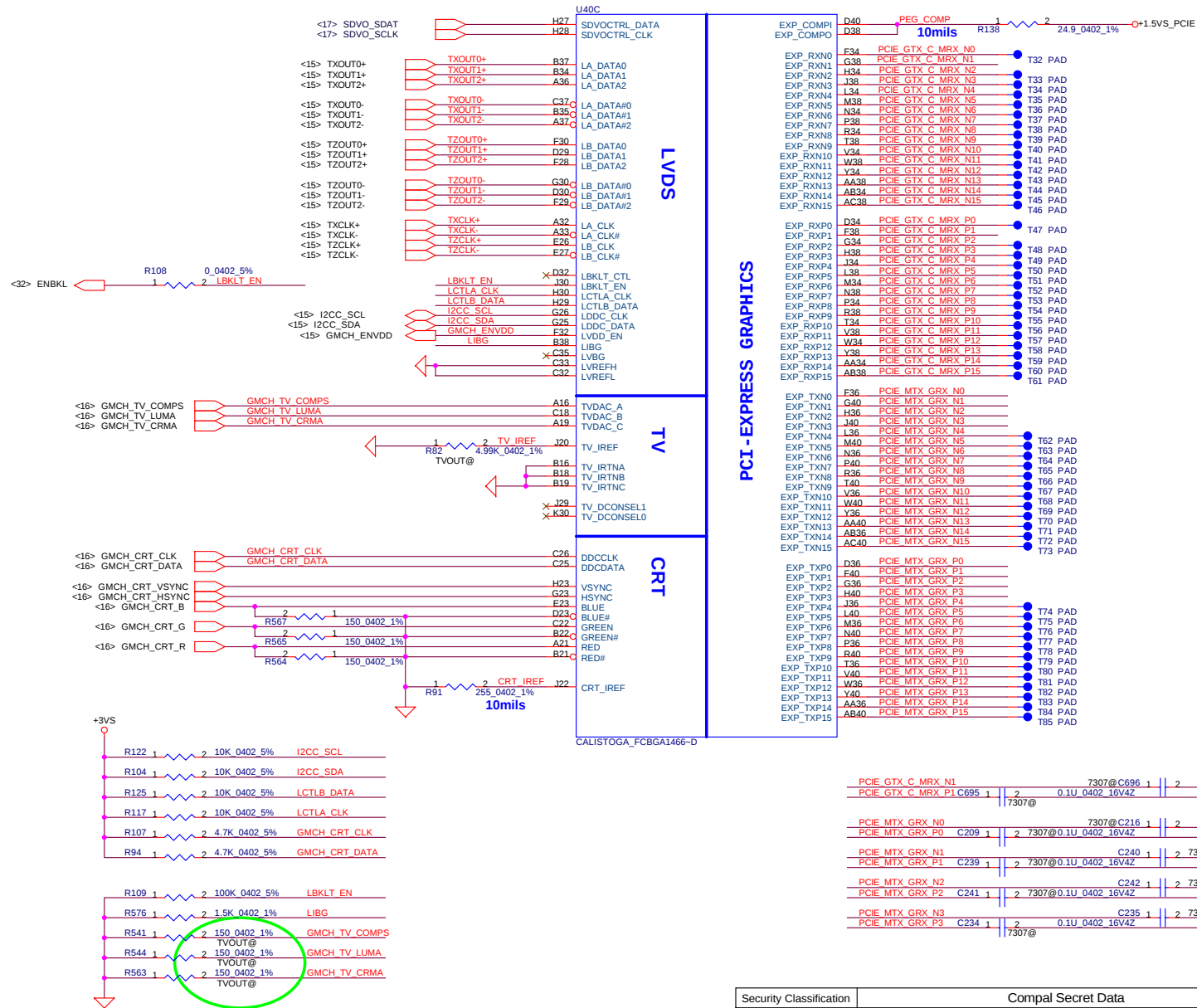
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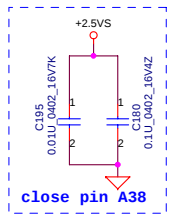
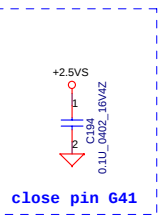
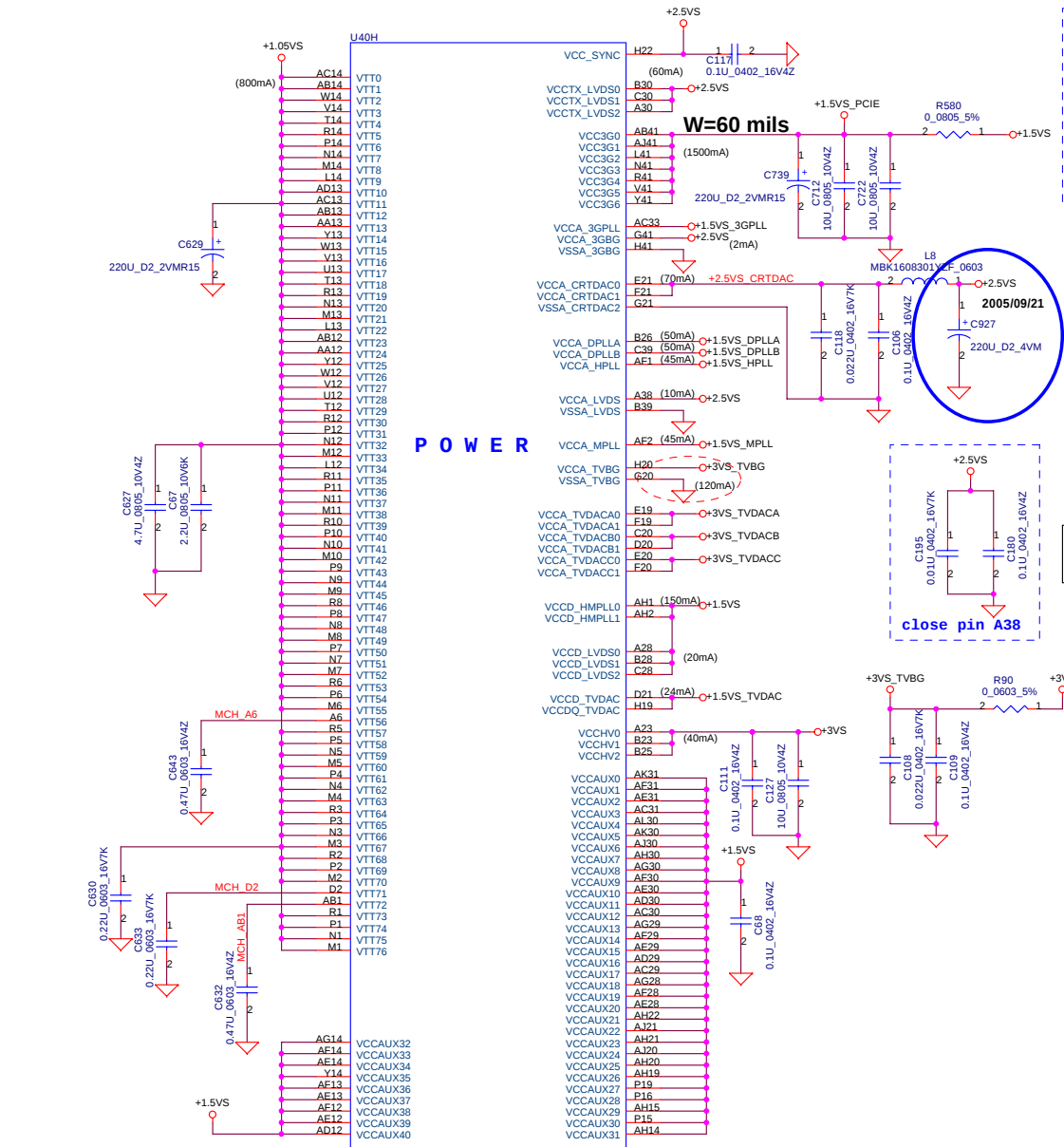
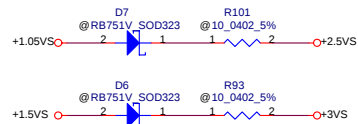
DDR SYS MEMORY B



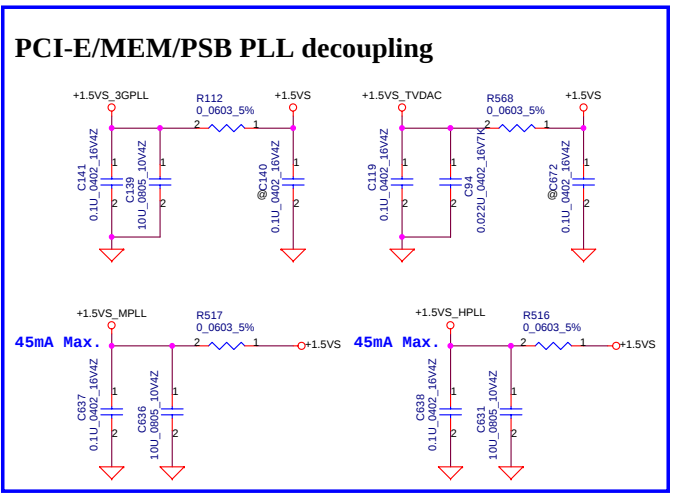
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Date: 星期四, 十月 05, 2006				401405	Sheet 7 of 47



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				Date: 星期四, 十月 05, 2006	Sheet 8	of 47



CR2AC: Route caps within 250mil of Alviso. Route FB within 3" of Calistoga

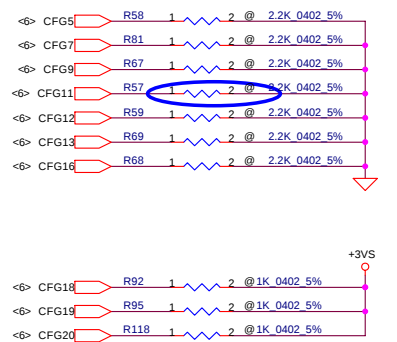
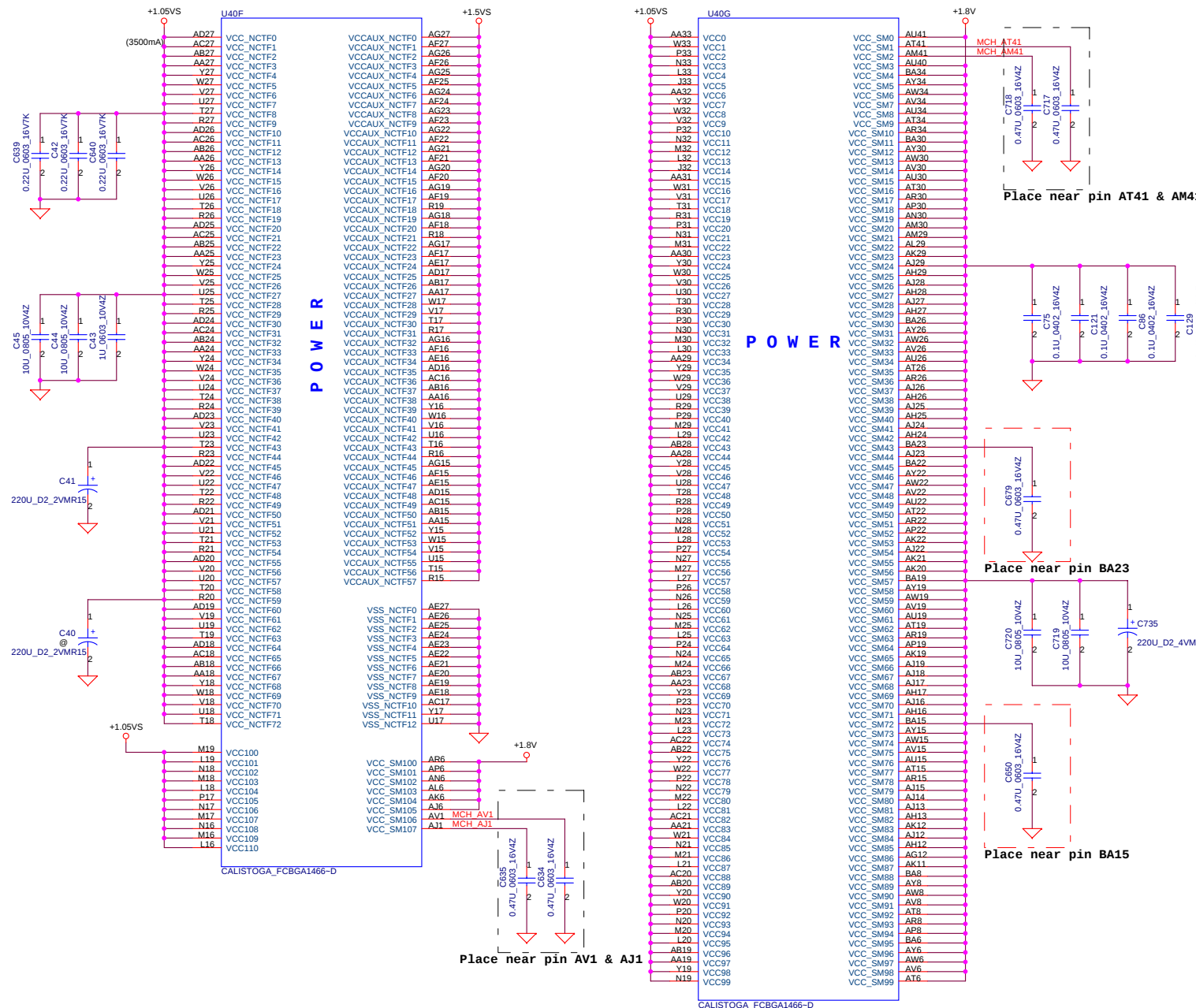


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				401405	Rev G
				Date: 星期四, 十月 05, 2006	Sheet 9 of 47

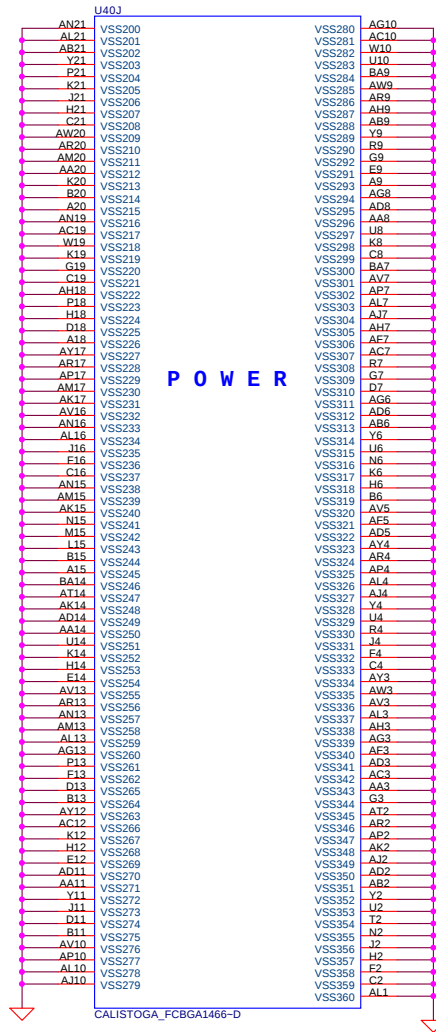
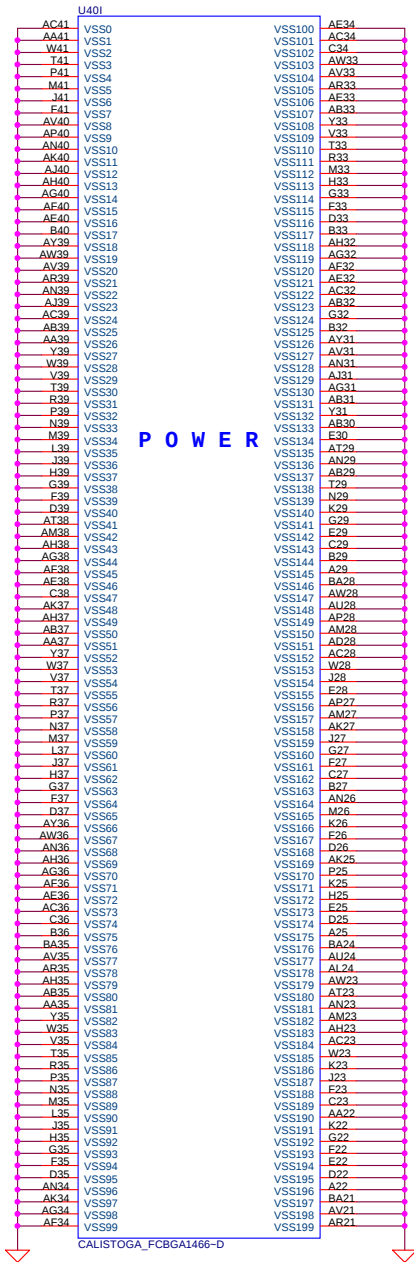
Strap Pin Table

CF6[3:17] have internal pull up
CF6[19:18] have internal pull down

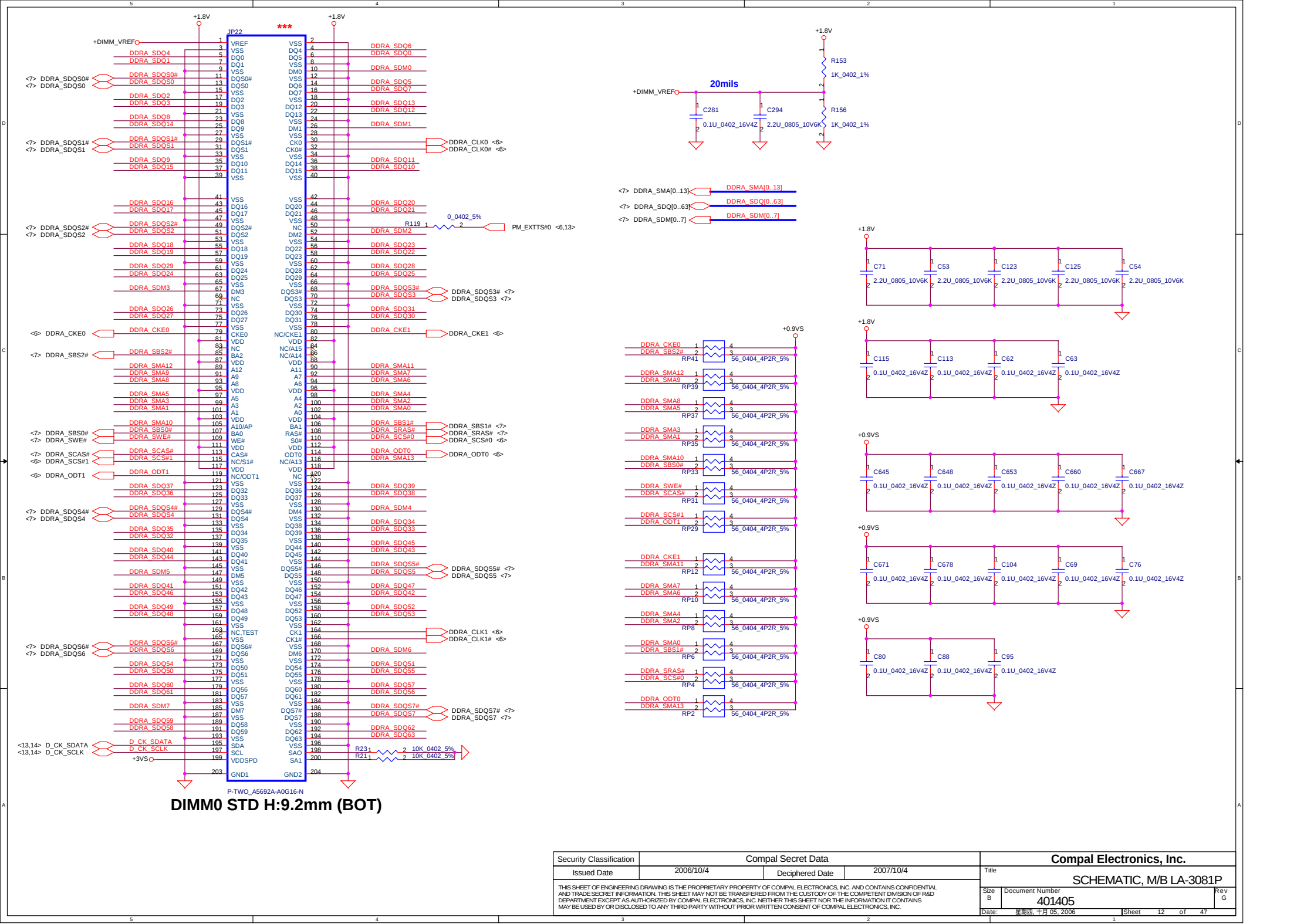
CF6[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CF65	0 = DMI x 2 1 = DMI x 4 *(Default)
CF67	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CF69	0 = Lane Reversal Enable 1 = Normal Operation*(Default)
CF611	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CF6[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CF616	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CF618	0 = 1.95V *(Default) 1 = 1.5V
CF619	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CF620 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



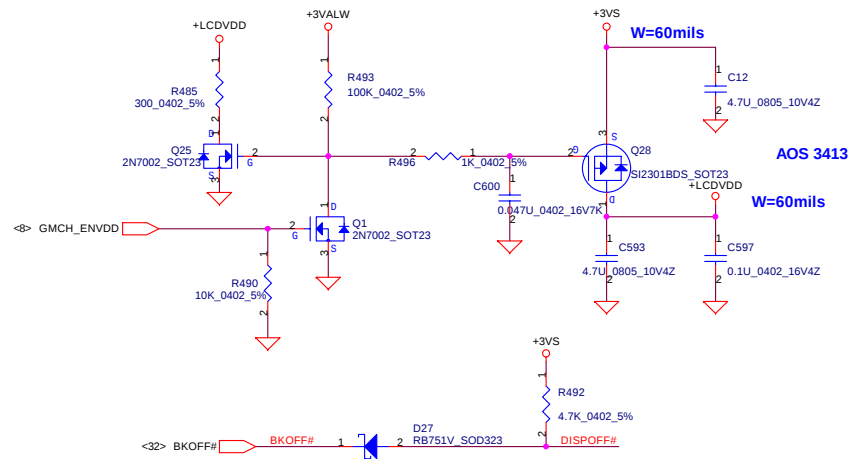
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Date: 星期四, 十月 05, 2006	Sheet 10	of 47				



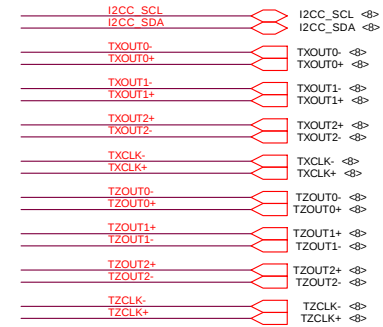
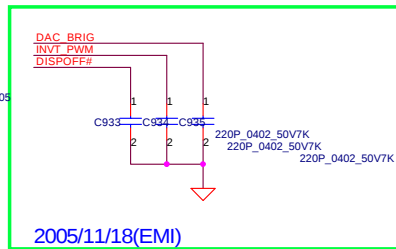
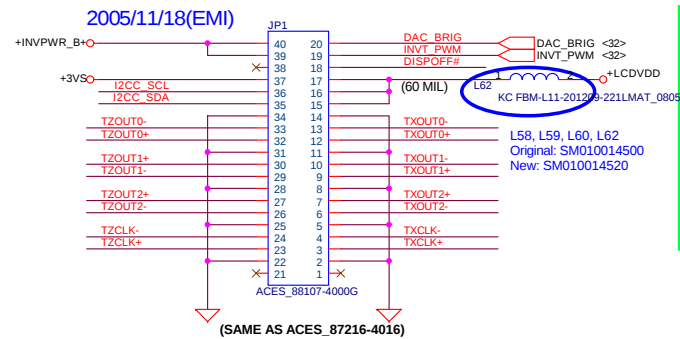
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				Date	星期四, 十月 05, 2006	Sheet 11 of 47



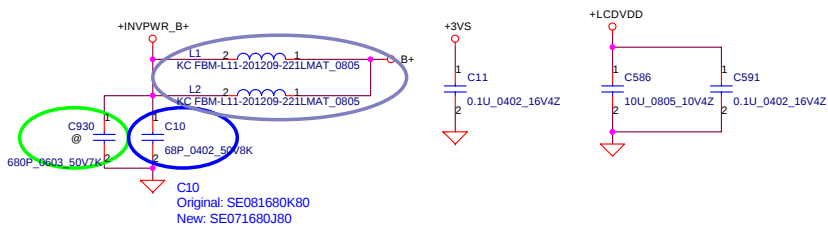
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.



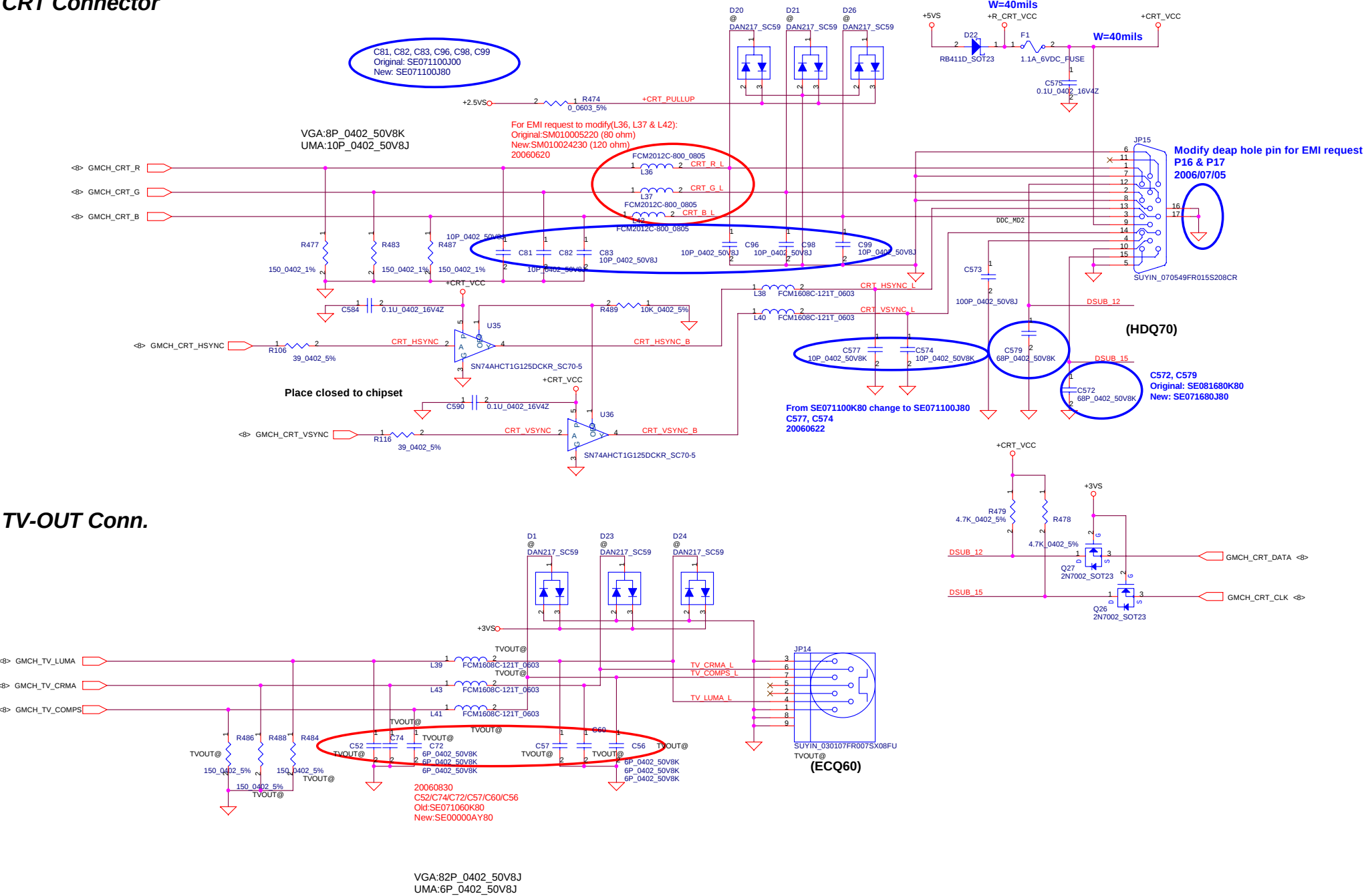
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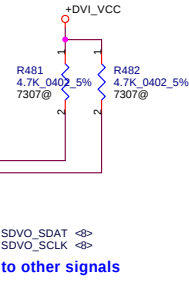
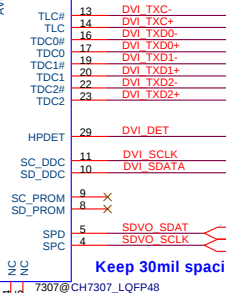
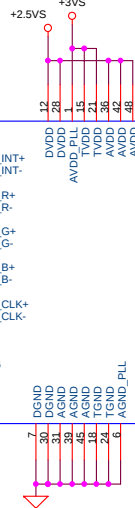
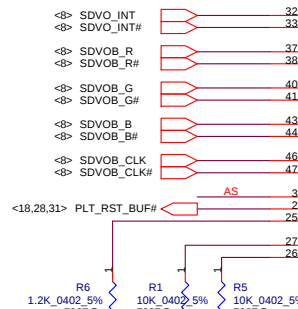
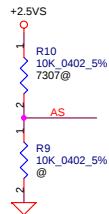
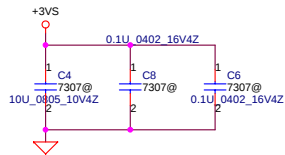
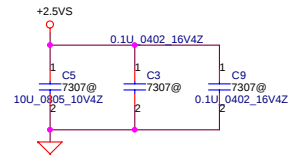
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				401405	
				Date: 星期四, 10月 05, 2006	Sheet 15 of 47

CRT Connector

TV-OUT Conn.

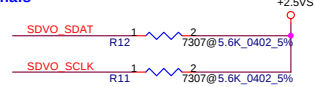


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	401405	星期四, 十月 05, 2006		16 of 47	G

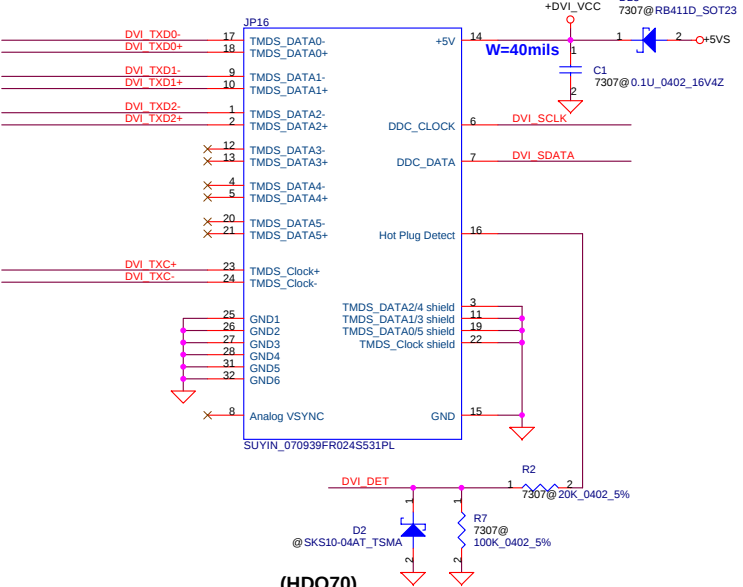


BOM structure	DVI from SDVO
7307@	Stuff
@	No_Stuff

Keep 30mil spacing to other signals



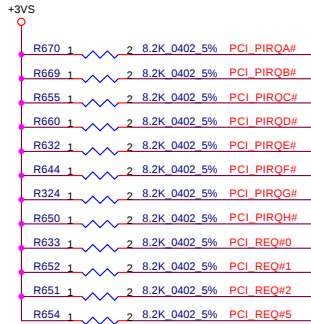
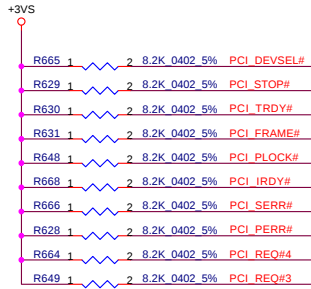
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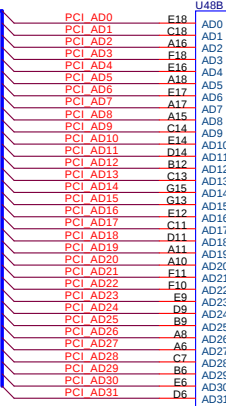
(HDQ70)

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				Size B	Document Number 401405	Rev G
				Date: 星期四, 十月 05, 2006	Sheet 17	of 47

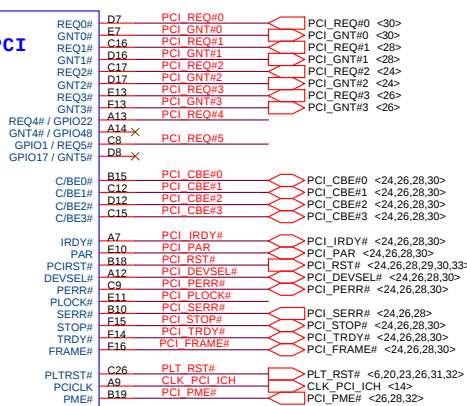
ICH7M(B-0) (QK17) [ES3] : SA00000JK30



<24,26,28,30> PCI_AD[0..31]



PCI



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<24> PCI_PIRQB#



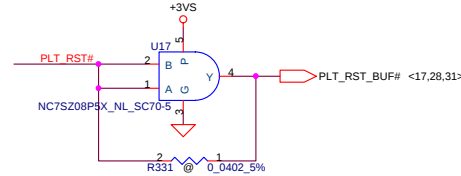
Interrupt I/F



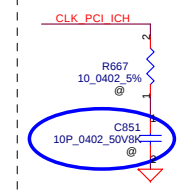
MISC



ICH7_BGA652-D

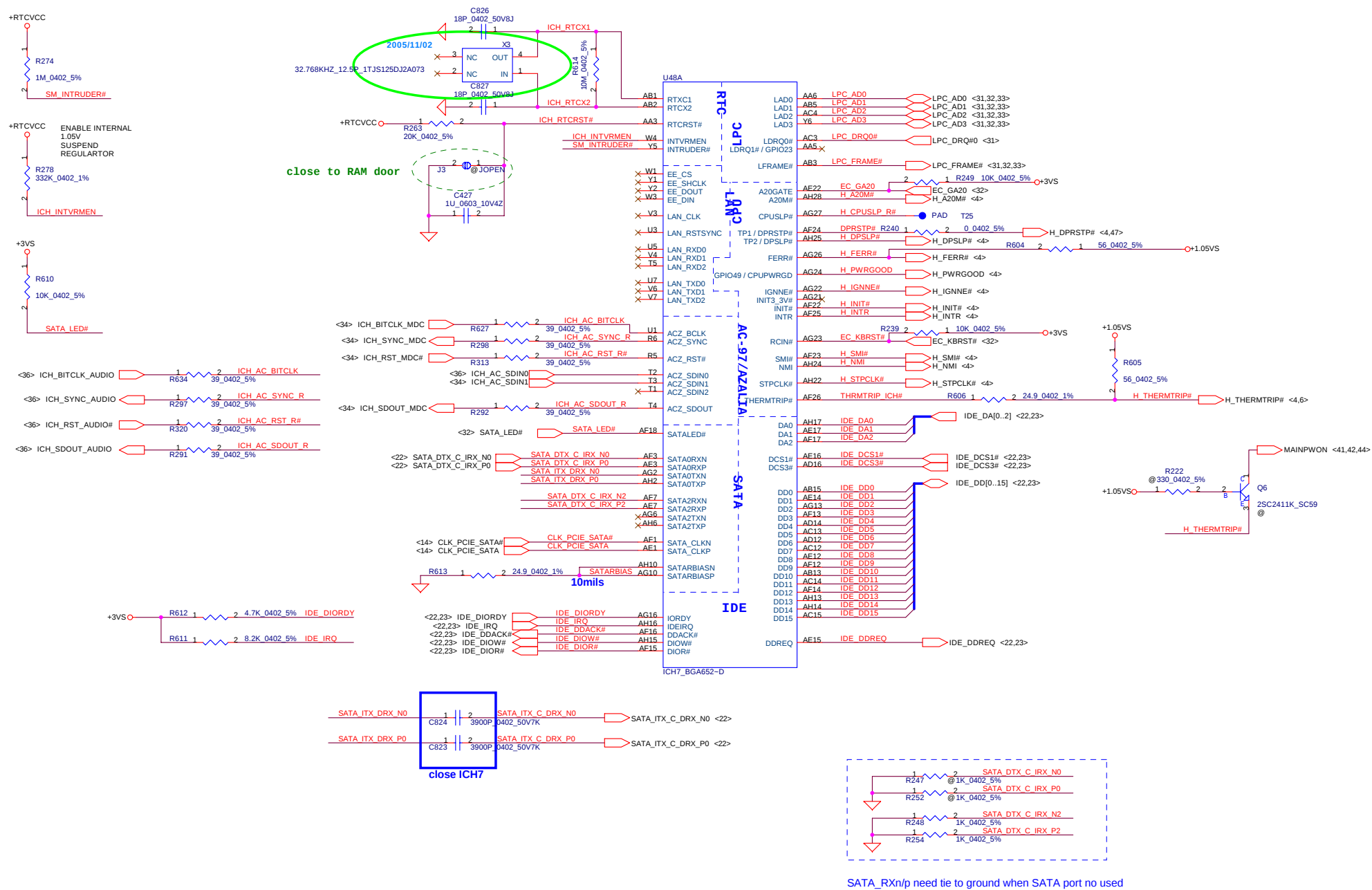


Place closely pin A9

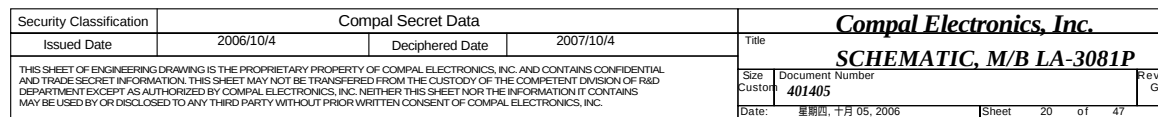
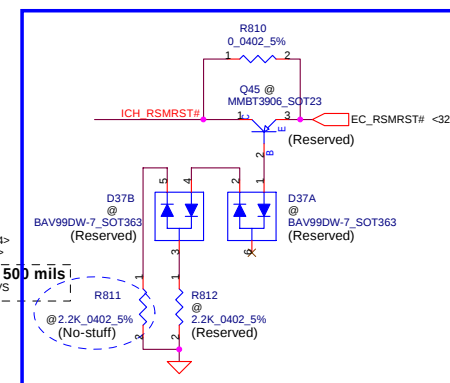
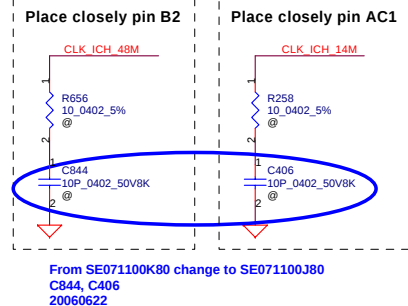
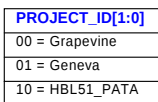


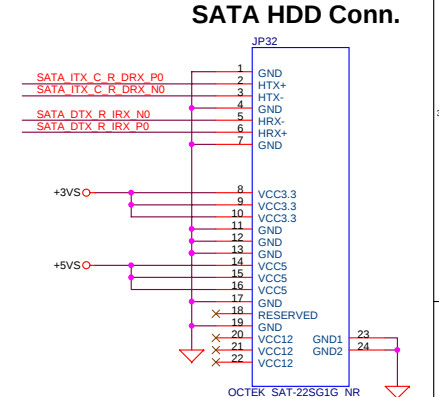
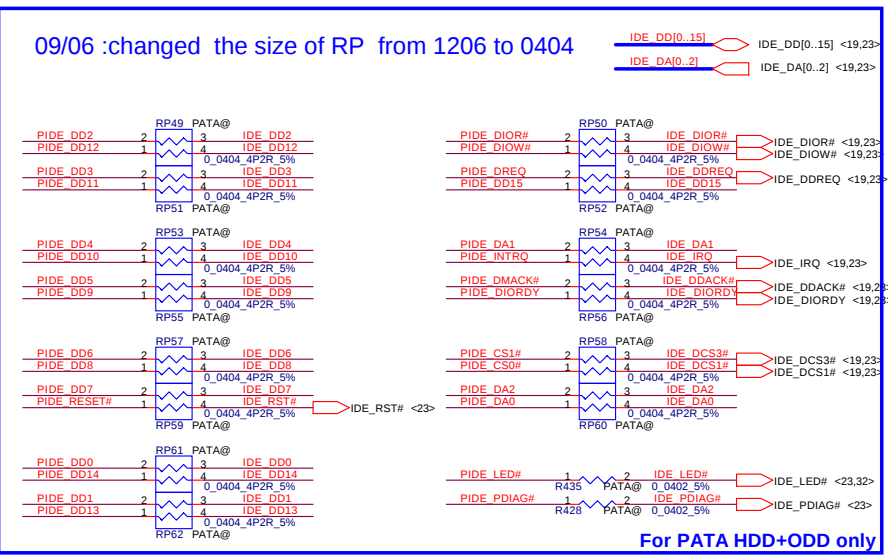
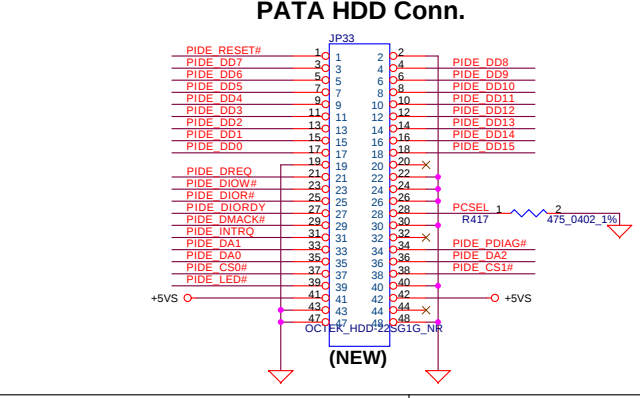
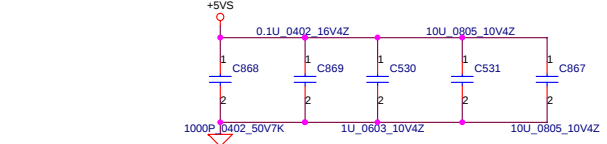
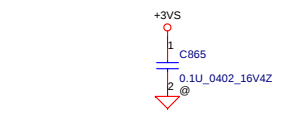
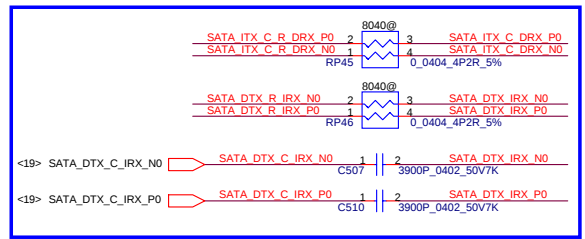
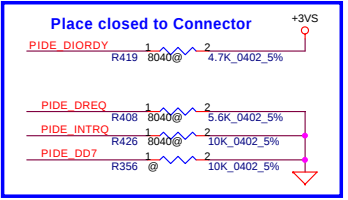
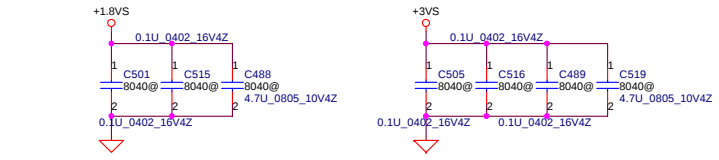
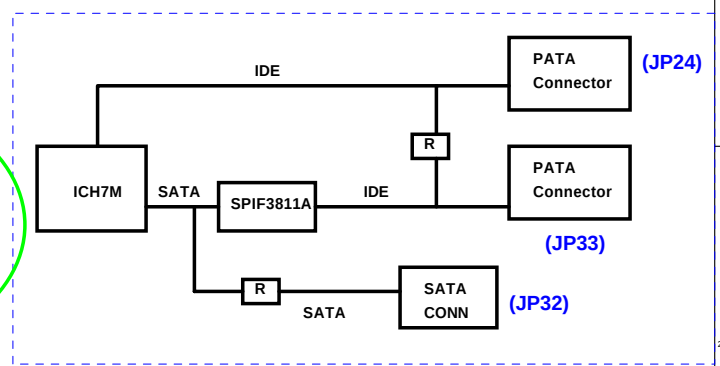
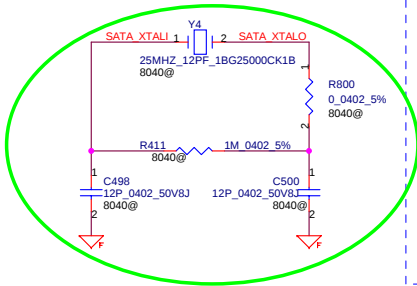
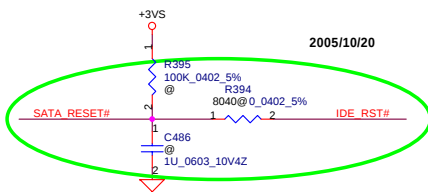
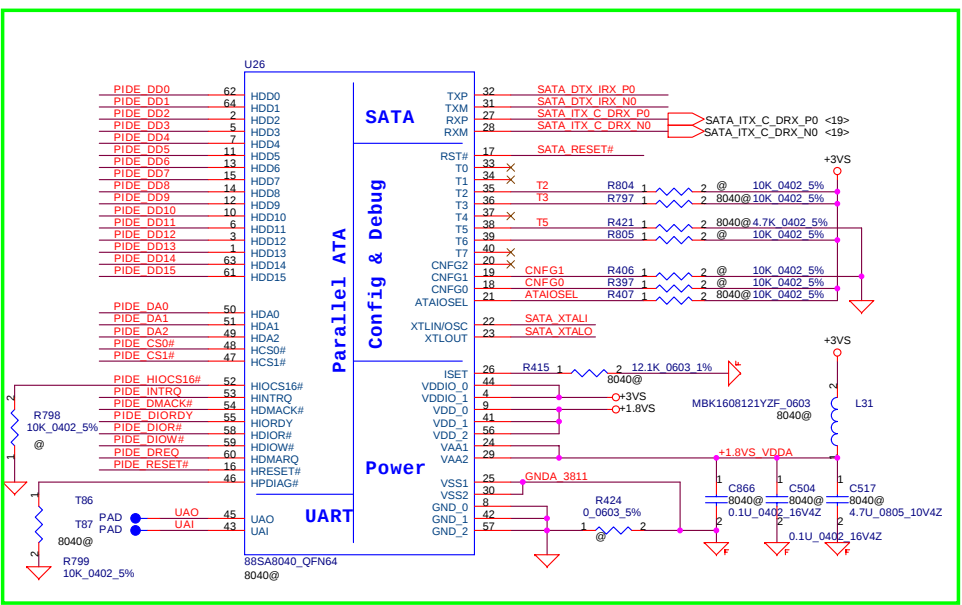
From SE071100K80 change to SE071100J80
20060622

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					401405
				Date	Rev
				星期四, 十月 05, 2006	G
				Sheet	18 of 47



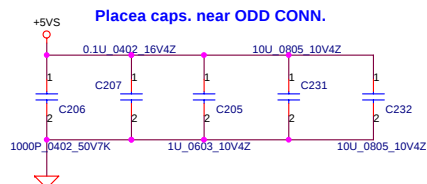
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				Custom	401405
				Date	Rev
				星期四, 十月 05, 2006	G
				Sheet	19 of 47



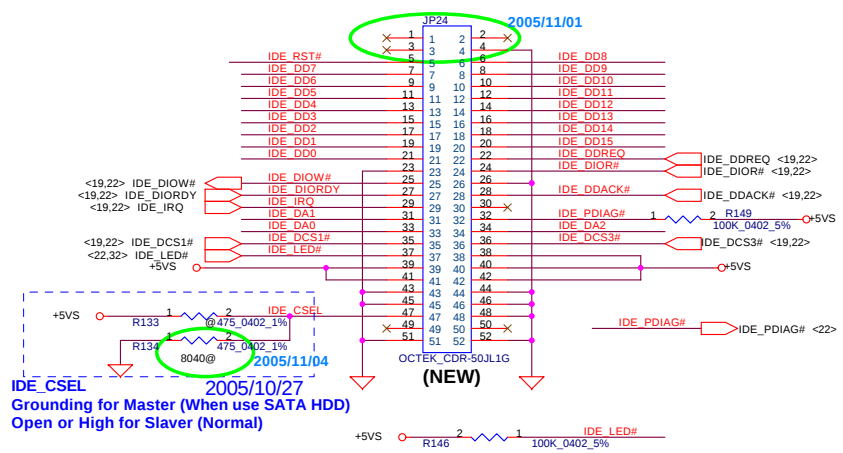
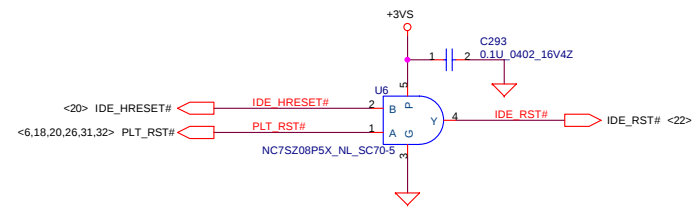


(NEW)
Change Library

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Size B	Document Number	401405		Rev G	
Date	星期四, 十月 05, 2006	Sheet	22	of 47	

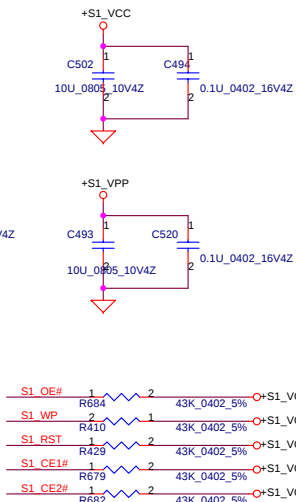
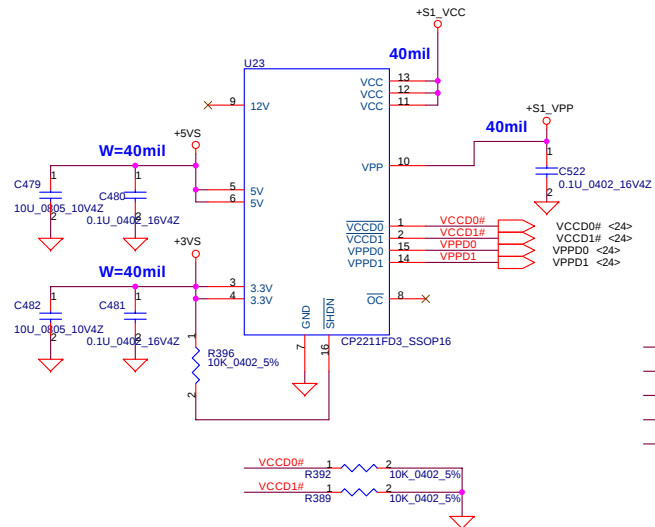


<19,22> IDE_DD[0..15] IDE_DD[0..15]
<19,22> IDE_DA[0..2] IDE_DA[0..2]

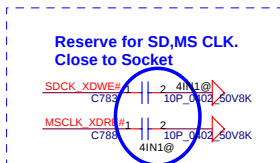
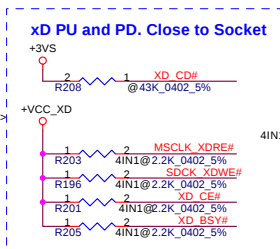
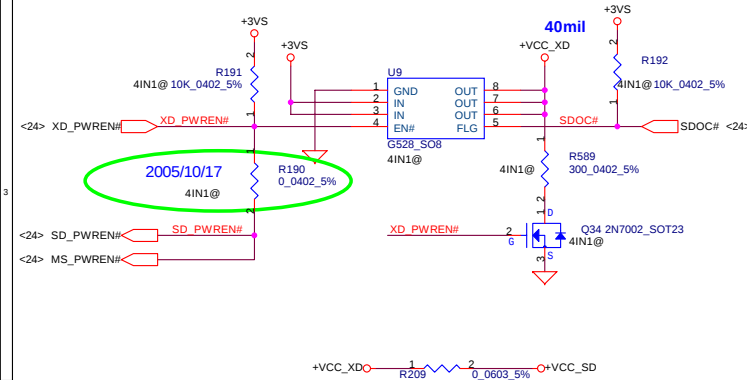


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				401405	
				Date: 星期四, 十月 05, 2006	Sheet 23 of 47

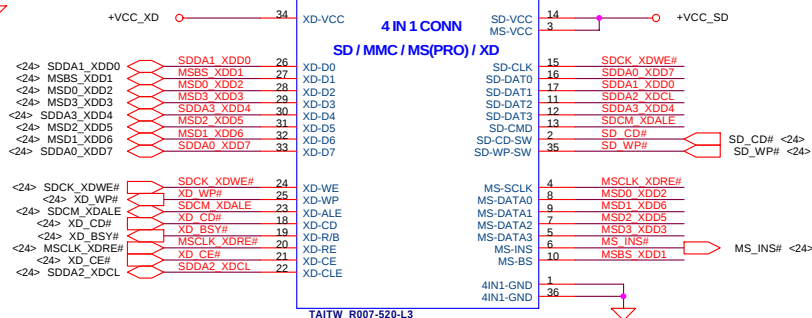
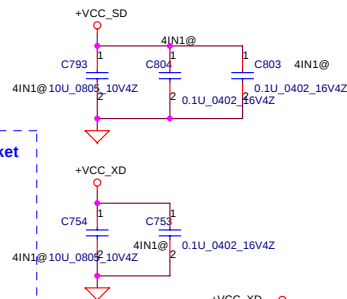
PCMCIA Power Control



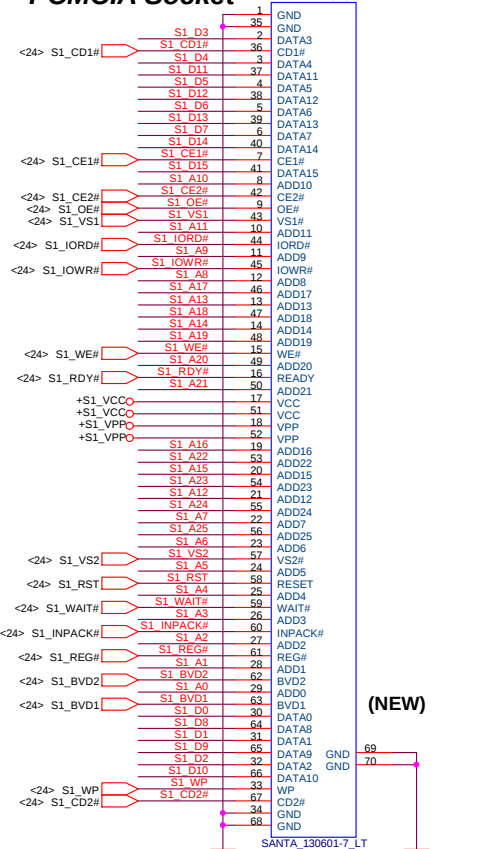
SD/MS Power Control
XD Power Control



From SE071100K80 change to SE071100J80
C783, C788
20060622

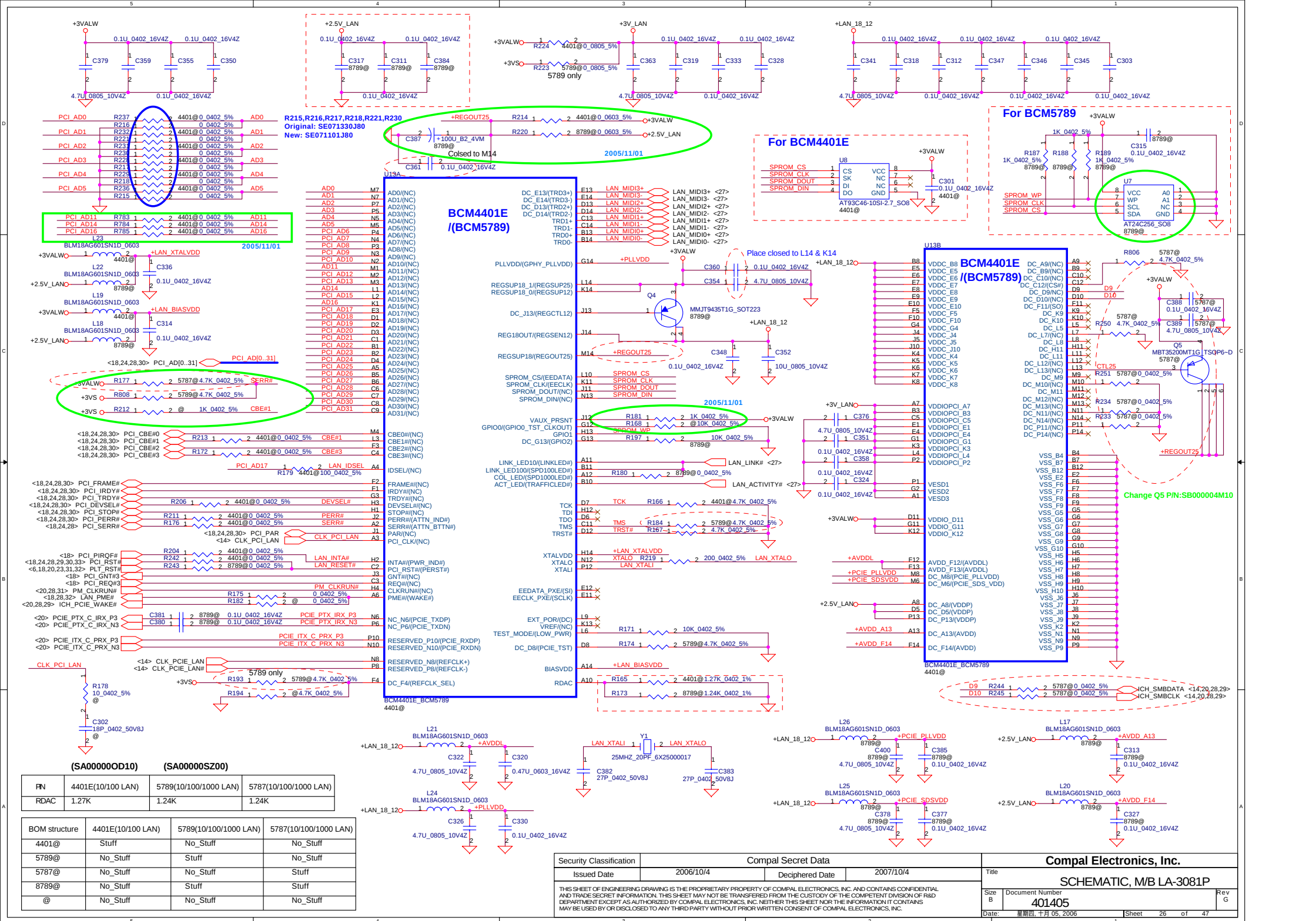


PCMCIA Socket

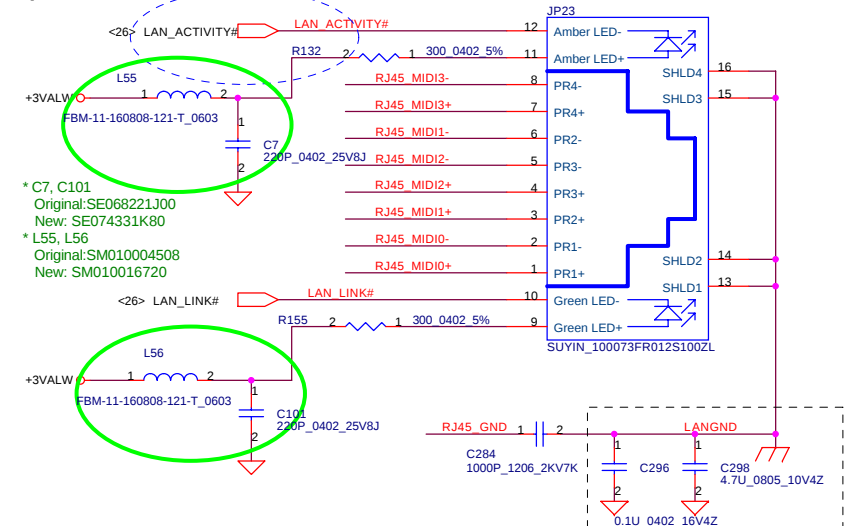


4 IN 1 Socket
(HDQ70)

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				Size	Document Number	Rev
				Date	星期四, 10月 05, 2006	Sheet 25 of 47



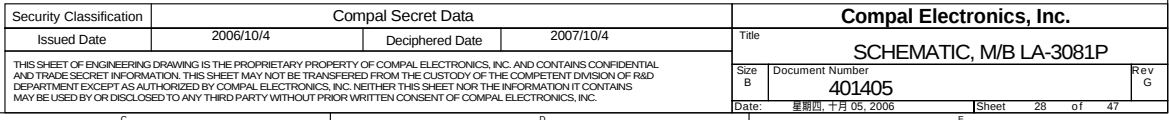
unpop when use BCM4401E(10/100)



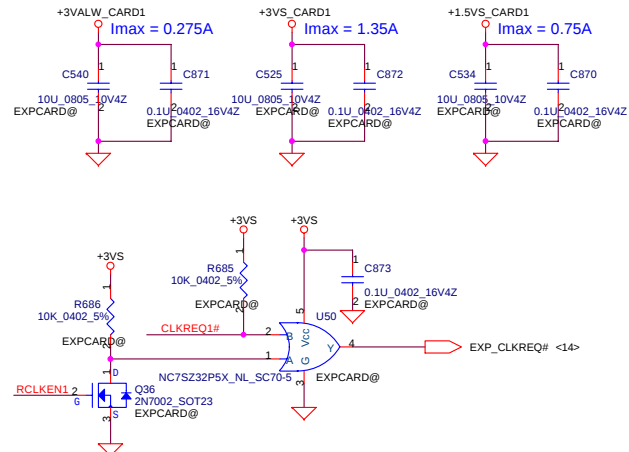
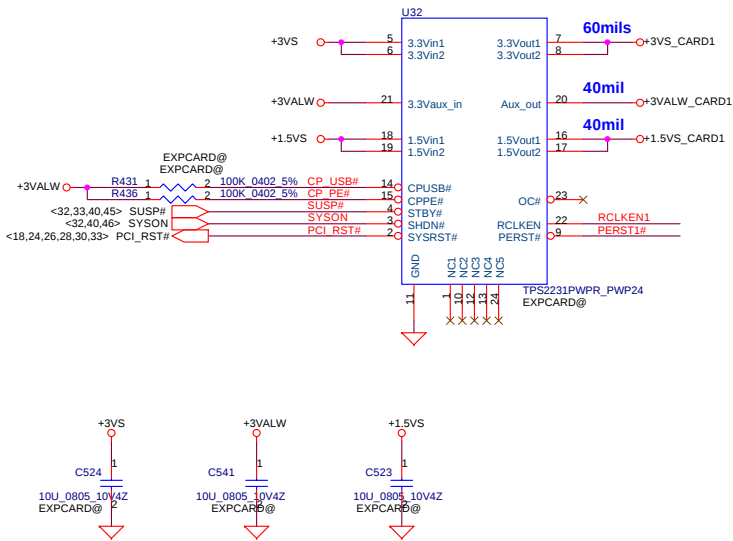
C286, C285
Original: SE070104Z80 (0.1U)
New: SE076103K80 (0.01U_BCM4401E_10/100)
20060711

reseved for BCM4401E(10/100)

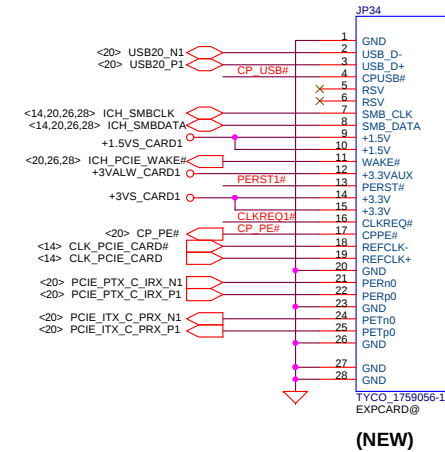
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				401405		
				Date: 星期四, 10月 05, 2006	Sheet 27 of 47	



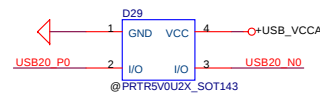
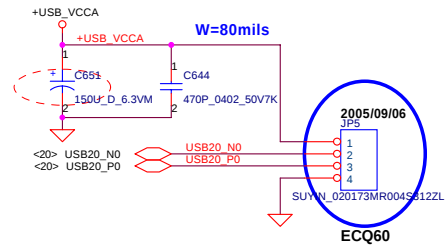
New Card Power Switch



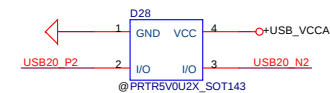
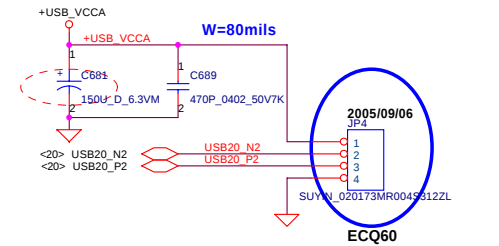
New Card Socket (Left)



USB CONN. 1 & 2

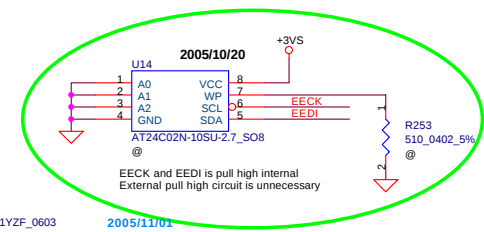
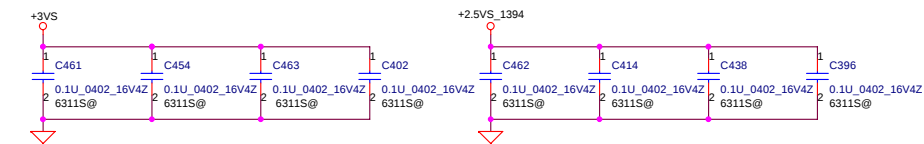


SUYIN_020173MR004G533ZR_4P



SUYIN_020173MR004G533ZR_4P

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				401405		
				Date: 星期四, 10月 05, 2006	Sheet 29	of 47



When use external EEPROM
Populate U14, R246, R253
Un-populate R261



VT6311S

EEPROM

others

OSCILLATOR

PHY PORT0

PHY PORT1

PCI I/F

<18,24,26,28> PCI_AD[0..31]

IDSEL:PCI_AD16

PCI_AD16 1 2 1394 IDSEL
R341 6311S@ 100_0402_5%

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<18,24,26,28> PCI_CBE#2
<18,24,26,28> PCI_CBE#1
<18,24,26,28> PCI_CBE#0
<18,24,26,28> PCI_STOP#
<18,24,26,28> PCI_PERR#
<18,24,26,28> PCI_PAR#
<18> PCI_PIRQE#
<18,24,26,28,29,33> PCI_RST#
<14,33> CLK PCI_1394
<18> PCI_GNT#0
<18> PCI_REQ#0

<18,24,26,28> PCI_IRDY#
<18,24,26,28> PCI_TRDY#
<18,24,26,28> PCI_DEVSEL#
<18,24,26,28> PCI_FRAME#

CLK PCI_1394

R319 @10_0402_5%

C456 @10P_0402_50V8K

From SE071100K80 change to SE071100J80
20060622

6311S@ R261 1 2 4.7K 0402_5%

2005/11/01

6311S@ C391 1 2 1U 0603 10V4Z
R279 1 2 @ 4.7K 0402_5%
R246 1 2 @ 4.7K 0402_5%
R257 1 2 6311S@ 4.7K 0402_5%
C407 1 2 0.1U 0402 16V4Z
6311S@

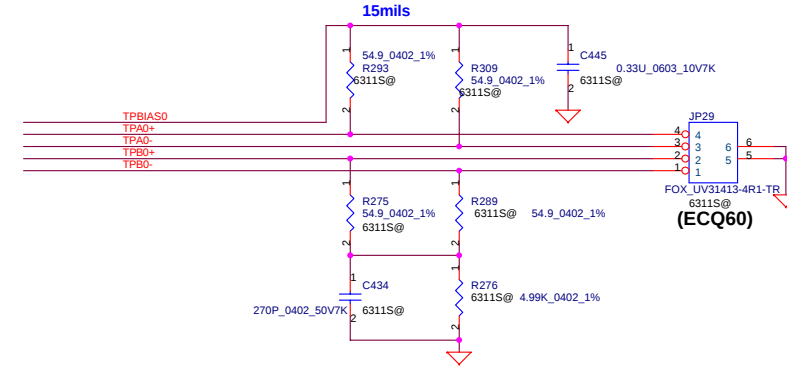
2005/11/01

From SE071100K80 change to SE071100J80
C398, C401
20060622

C398 1P_0402_50V8K
C401 1P_0402_50V8K
24.576MHZ_16P XBA024576FG1H
6311S@

REG_OUT
REG_FB
Q35 2SB1197K_SOT23
+3VS
+2.5VS_1394

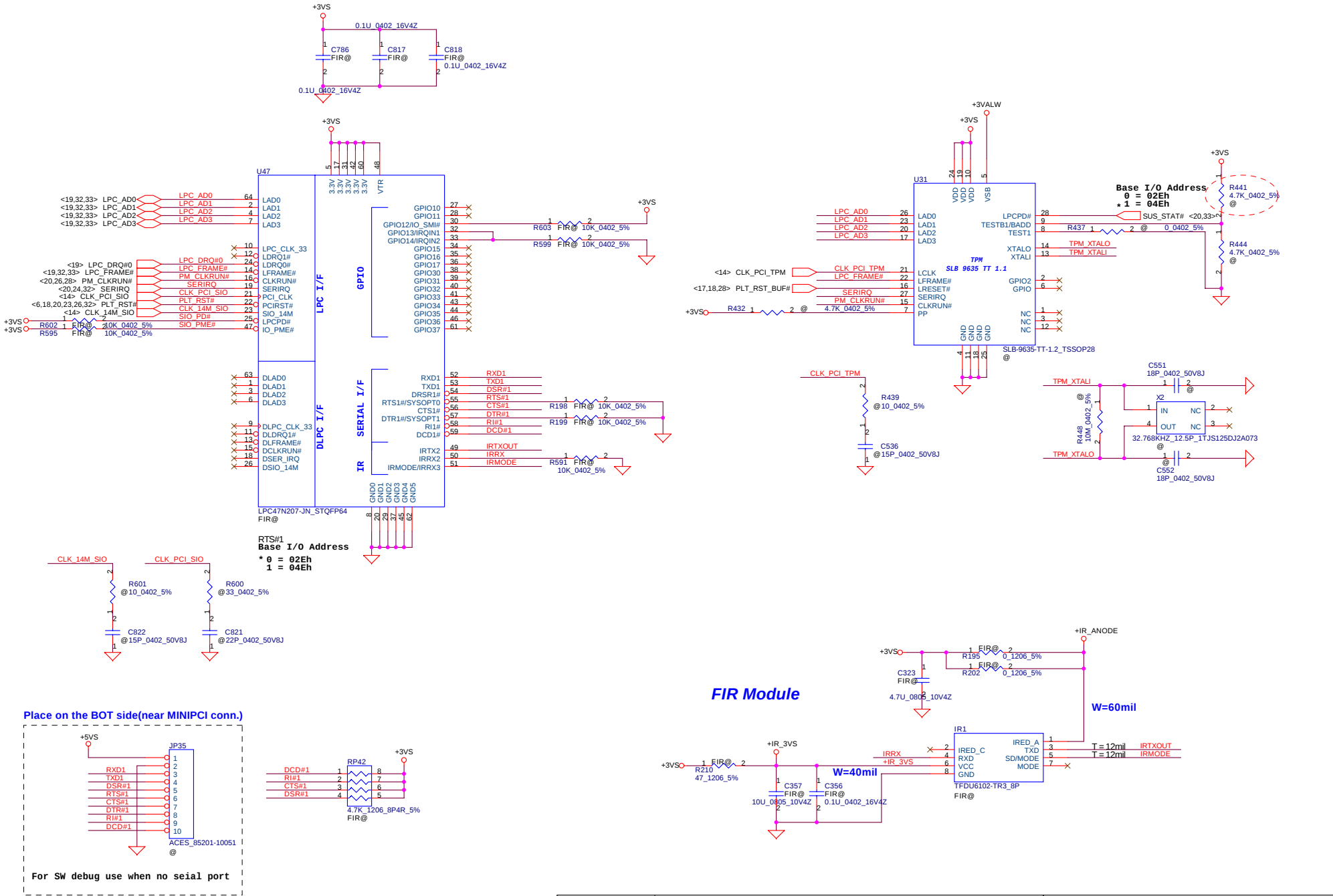
When use external BJT
Populate Q35, R279



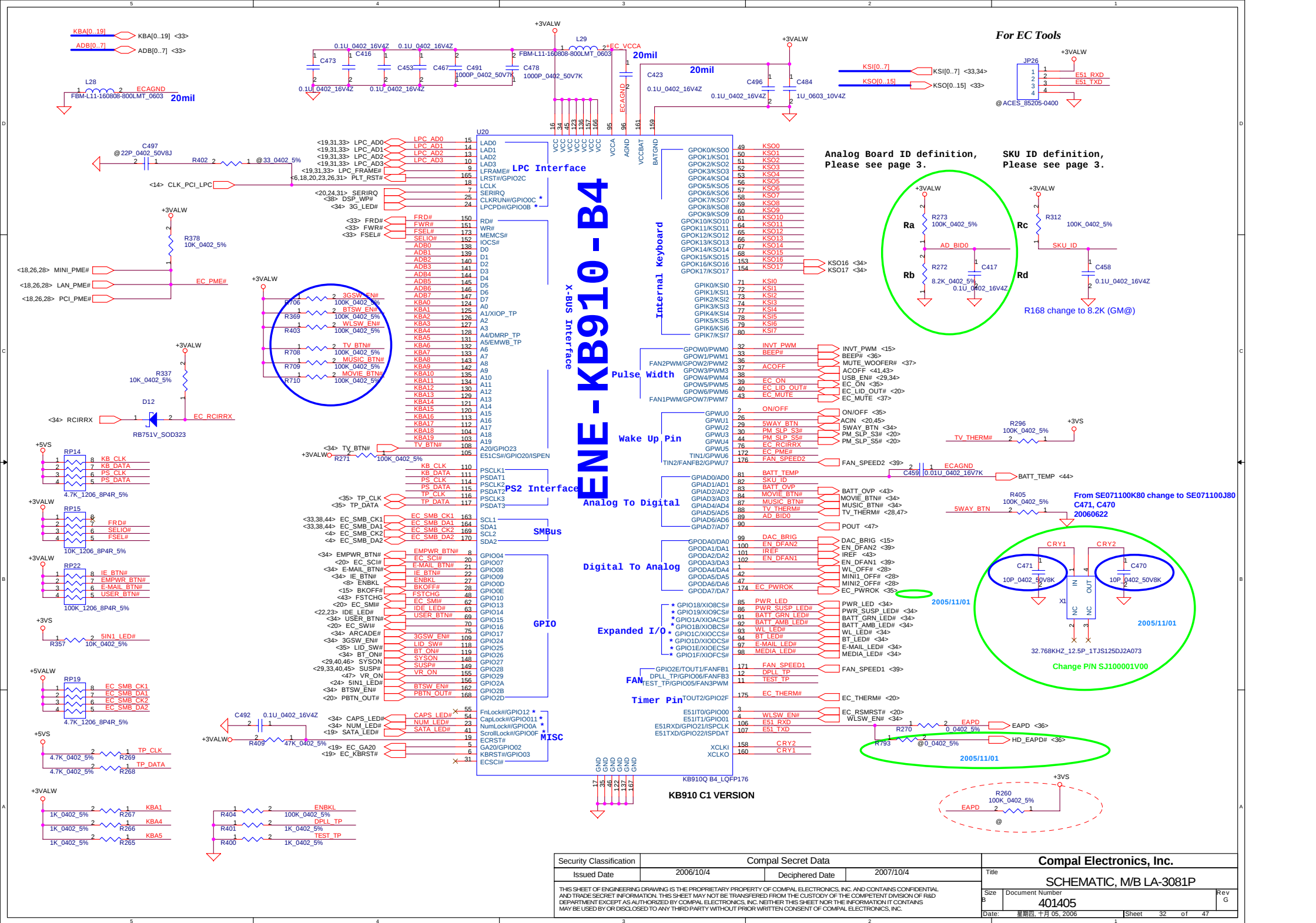
JP29
FOX_UV31413-4R1-TR
6311S@
(ECQ60)

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				401405	Rev G
Date: 星期四, 十月 05, 2006				Sheet 30	of 47

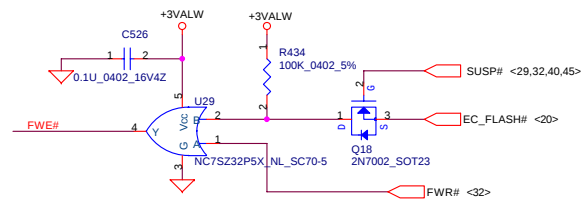
SUPER I/O SMsC LPC47N207



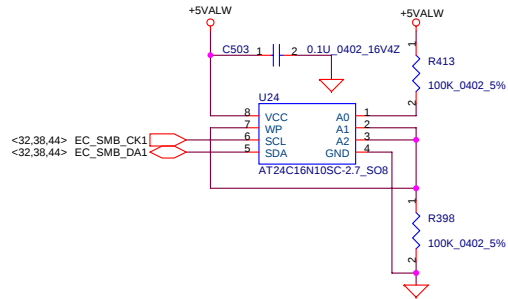
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Size	B	Document Number	401405	Rev		
Date:	星期四, 十月 05, 2006	Sheet	31	of	47	



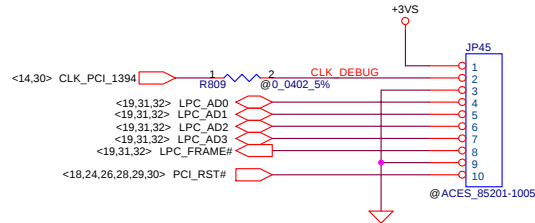
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				401405			
				Date:	星期四, 10月 05, 2006		Sheet 32 of 47
3	1	2					



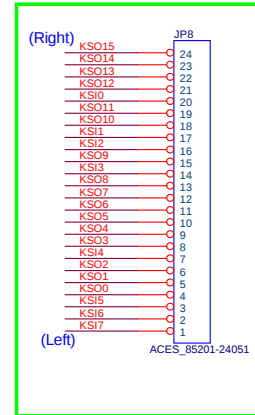
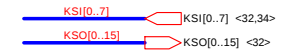
Check PCB Footprint



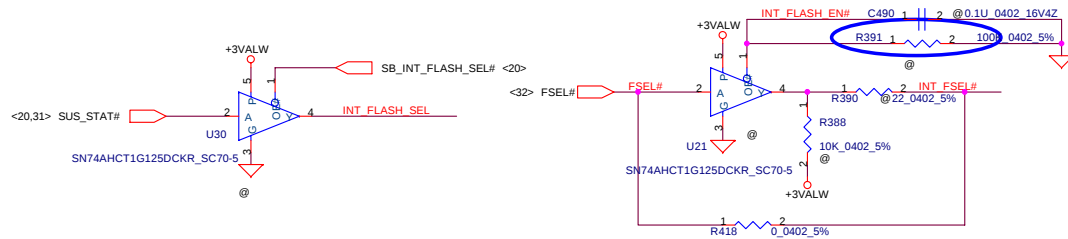
For LPC Debug Card



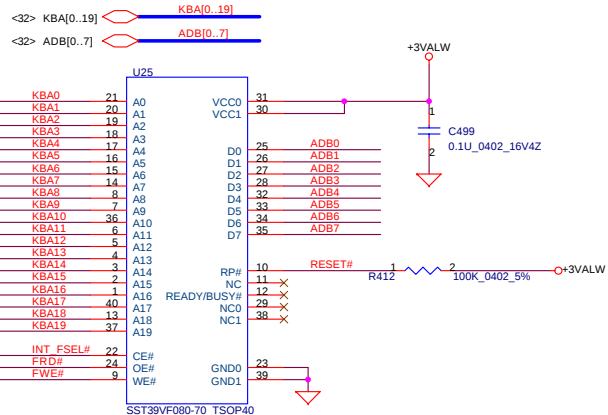
INT_KBD Conn.



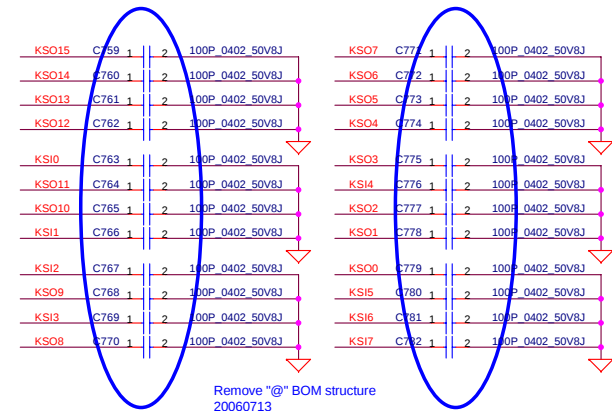
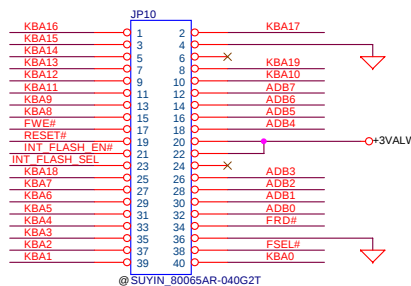
2005/11/03



1MB Flash ROM

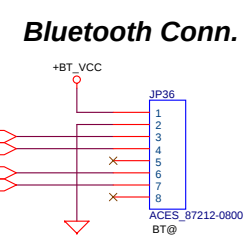
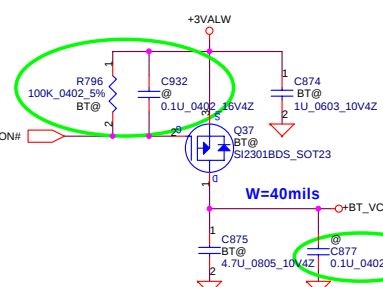
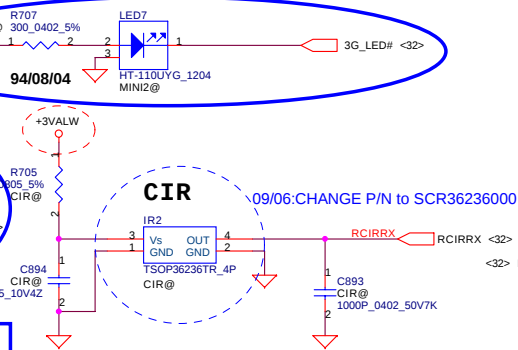
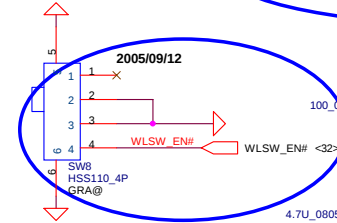
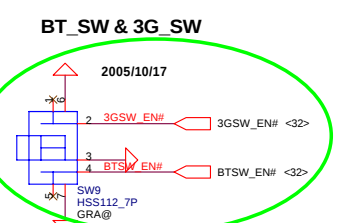
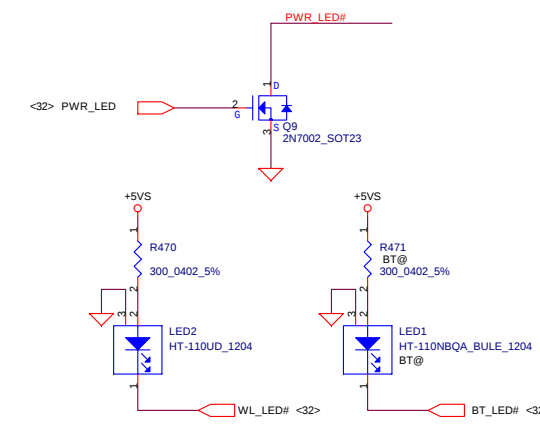
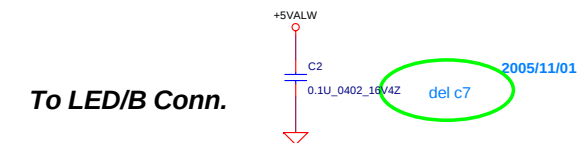
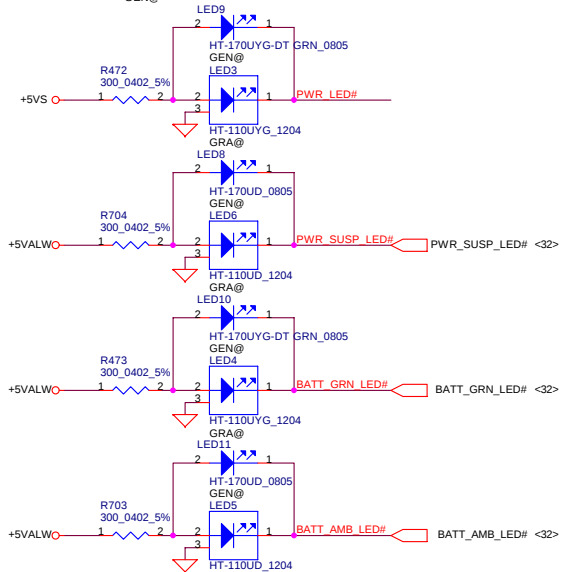
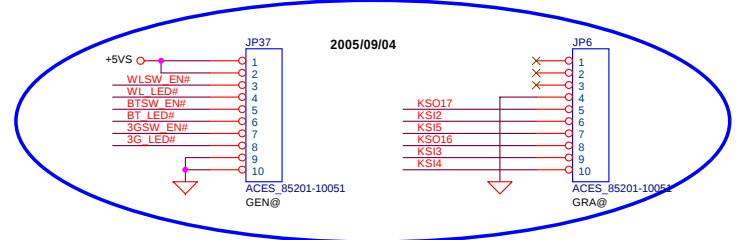
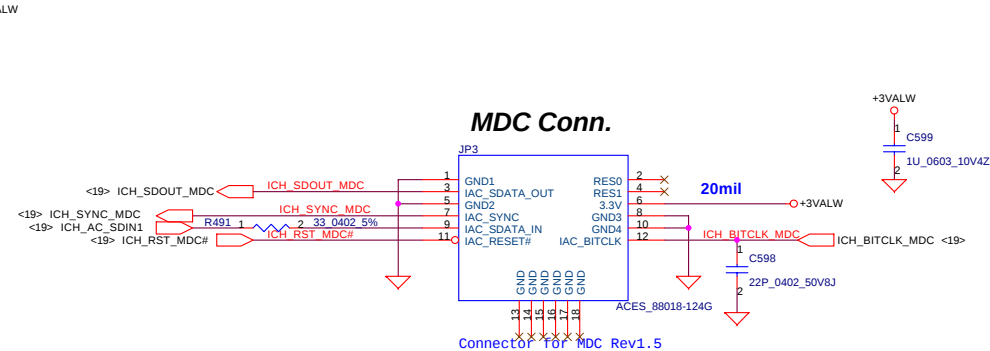
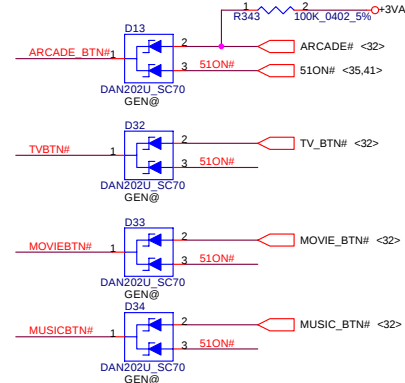
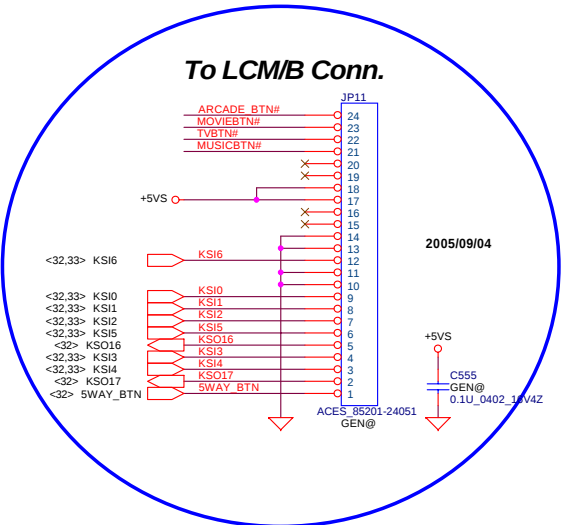


1MB ROM Socket



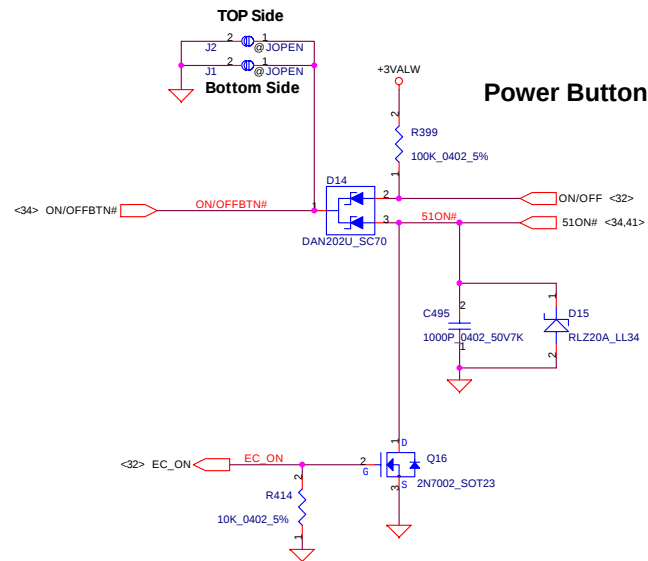
Remove "*" BOM structure
20060713

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						Size B	Document Number			Rev G		
						401405						
						Date:	星期四, 十月 05, 2006		Sheet	33	of	47

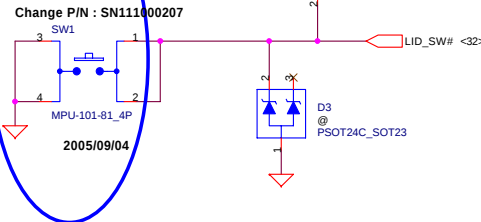


Geneva		Grapevine	
	KSO16	KSO17	
KSI0	VOL_UP	LEFT	
KSI1	RIGHT	VOL_DOWN	
KSI2	PLAY	ENTER	
KSI3	STOP		
KSI4	NEXT	VOL_UP	
KSI5	REV	VOL_DOWN	
KSI6		RECORD	
		ARCADE_TV	

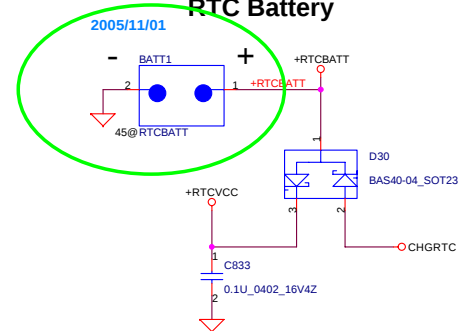
ON/OFF switch



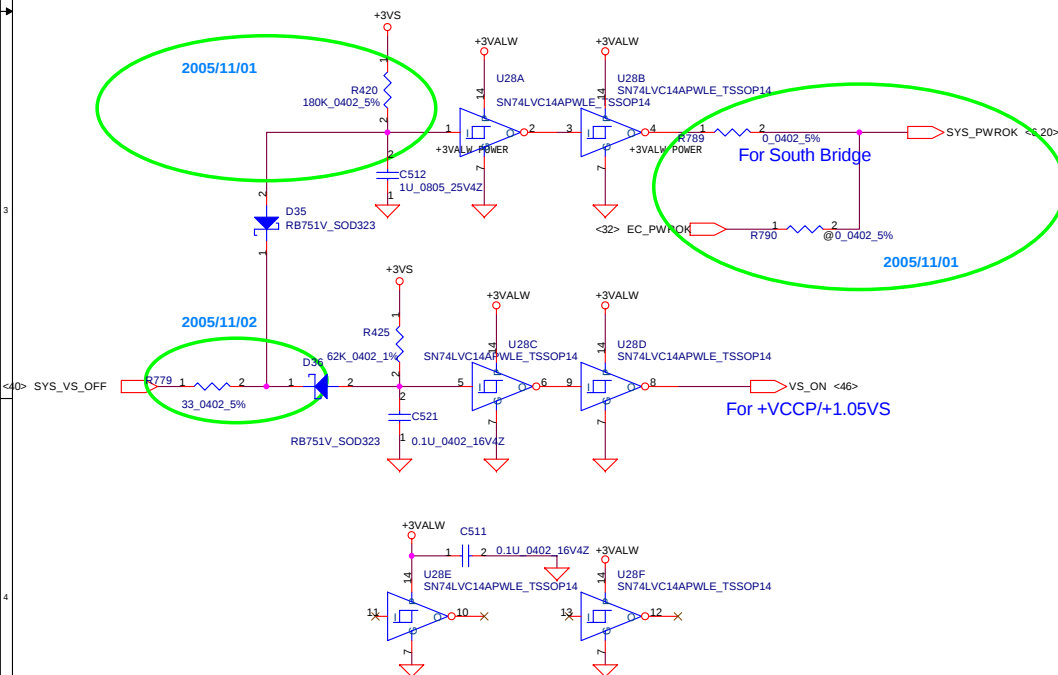
Lid Switch



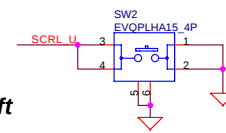
RTC Battery



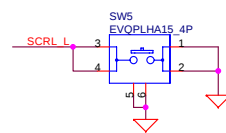
Power ON Circuit



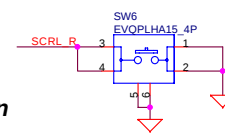
Scroll Up



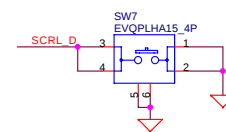
Scroll Left



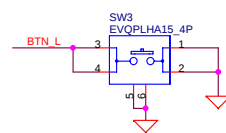
Scroll Right



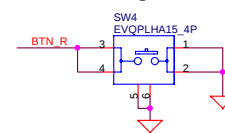
Scroll Down



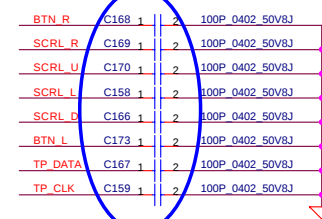
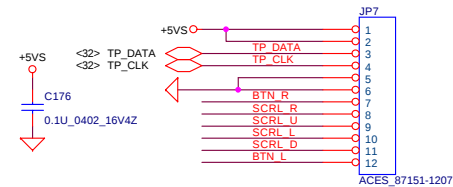
Left



Right

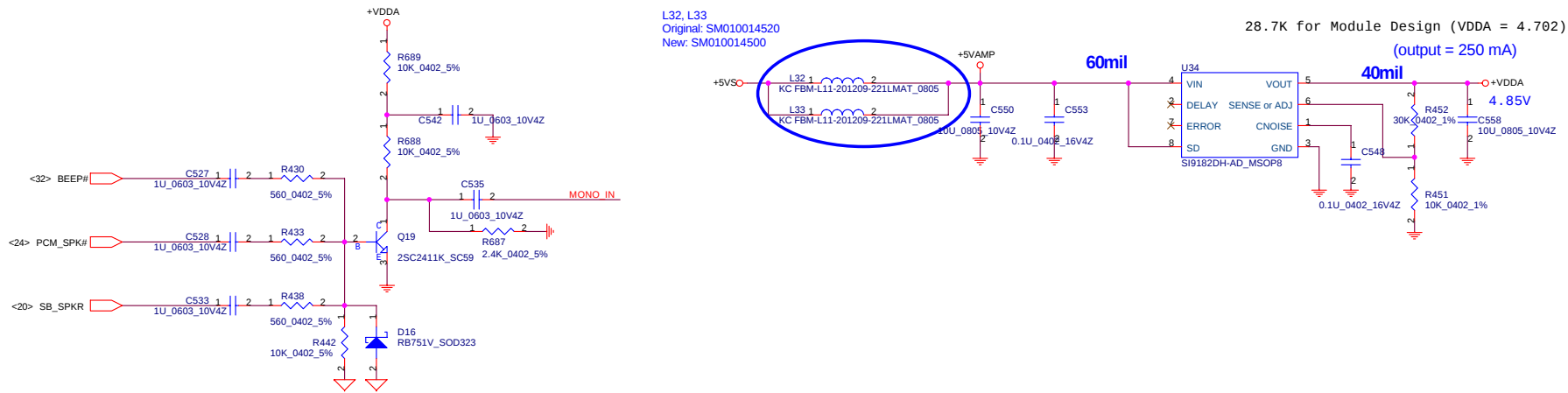


To TP/B Conn.

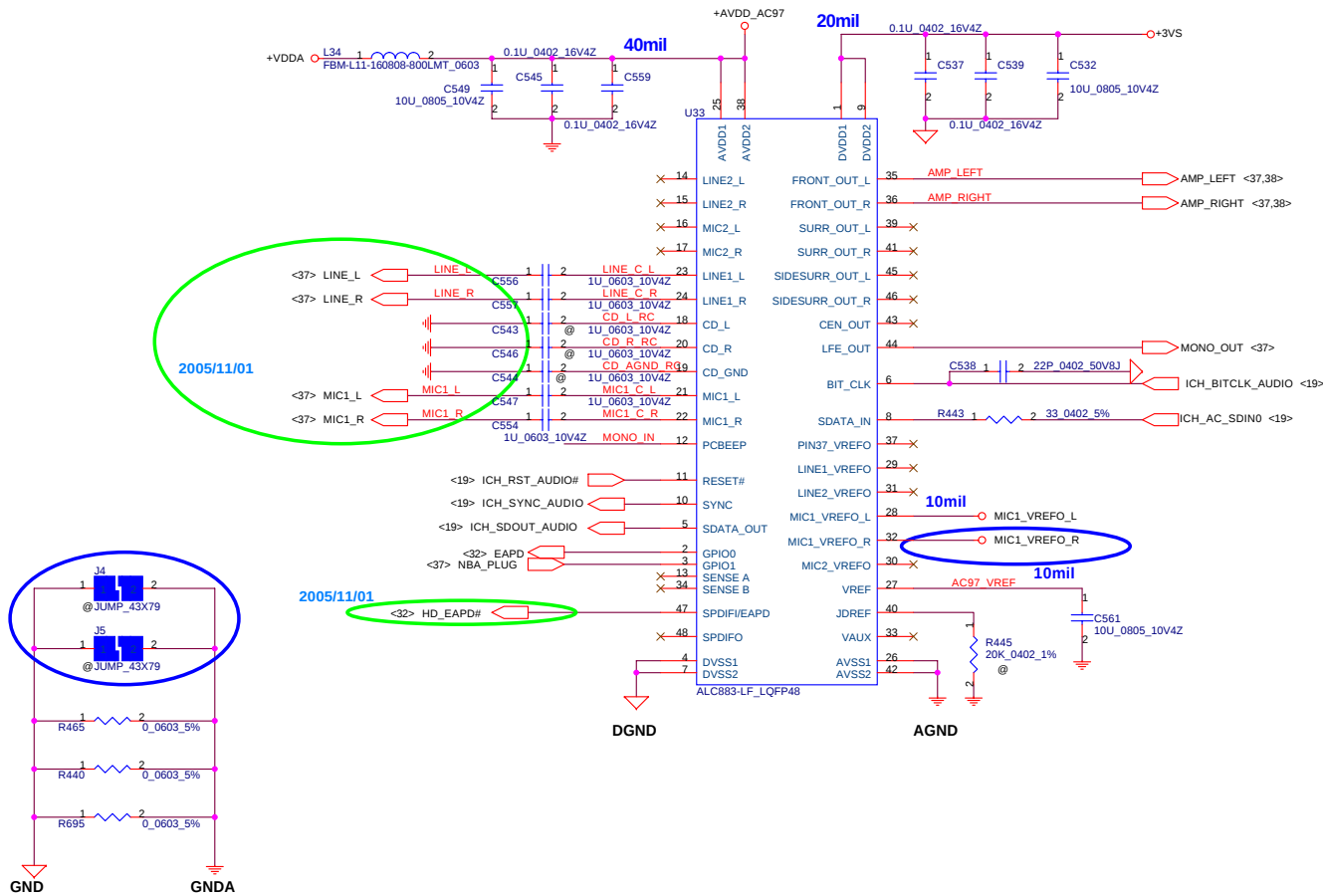


Remove "@" BOM structure

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				Date: 星期四, 十月 05, 2006	Rev G
				Sheet 35 of 47	

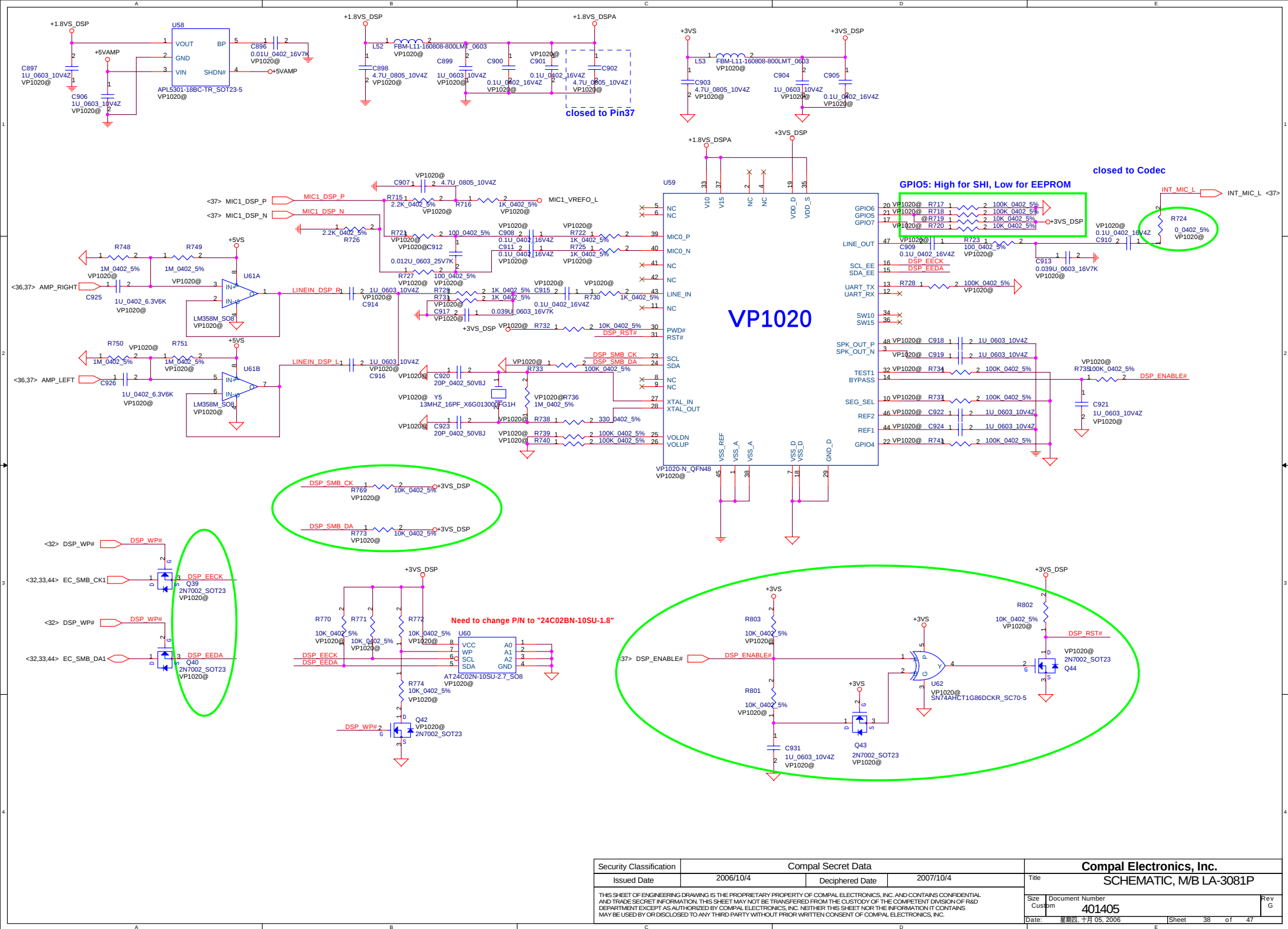


HD Audio Codec



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				Date: 星期四, 十月 05, 2006	Sheet 36 of 47



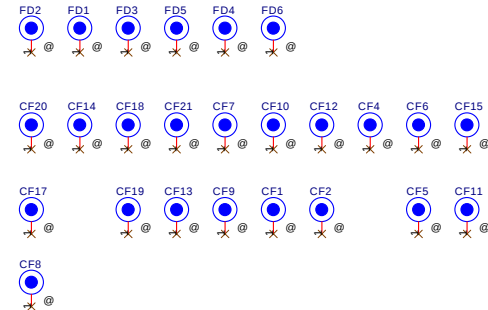
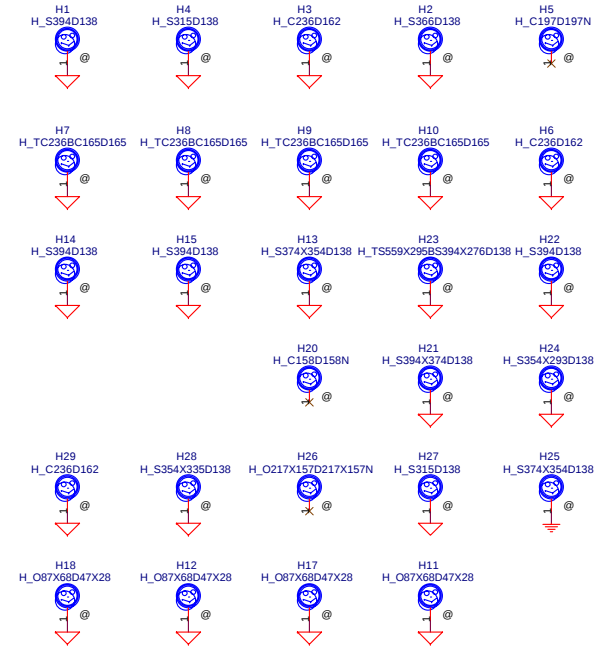


The schematic diagram illustrates the power supply section of the ACES_85205-03001 board, featuring two DC-DC converters (U2 and U3) and associated components.

Top Converter (U2): A buck converter powered by +5VS. It includes an input capacitor C47 (10U_1206_16V4Z) and an output capacitor C51 (10U_1206_16V4Z). The output is +VCC_FAN1, which is also connected to EN_DFAN1. The converter is labeled G993P1UF_SOP8.

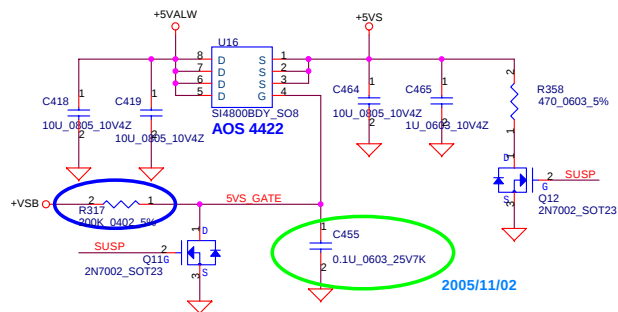
Bottom Converter (U3): A buck converter powered by +3VS. It includes an input capacitor C58 (1000P_0402_50V7K) and an output capacitor C59 (1000P_0402_50V7K). The output is +VCC_FAN1, which is also connected to FAN_SPEED1. The converter is labeled G993P1UF_SOP8.

Other Components: Diodes D4 (1SS385_SOD323) and D5 (1N4148_SOT23) are used for rectification. A 40mil trace is indicated for the +VCC_FAN1 line. A connector JF19 (ACES_85205-03001) is shown at the bottom right.

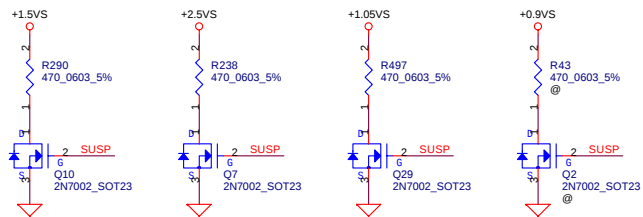
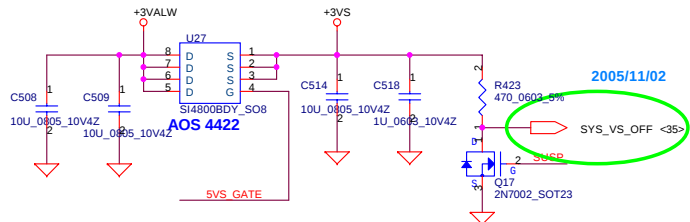
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					401405	G
Date		星期四, 10月 05, 2006		Sheet		39 of 47

+5VALW TO +5VS

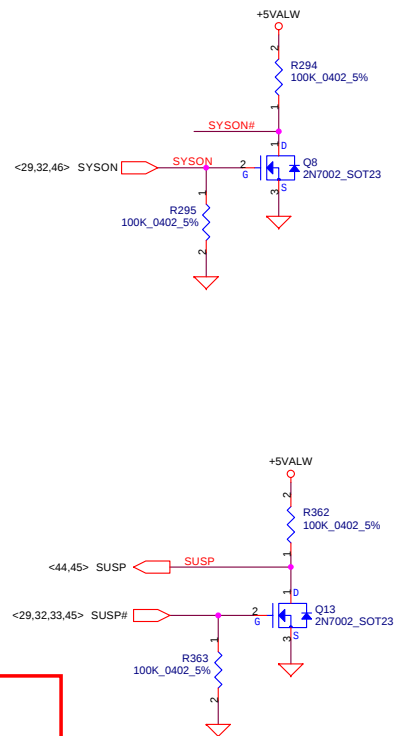
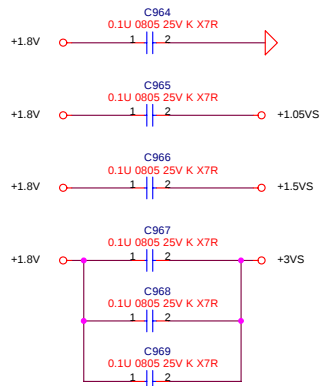


+3VALW TO +3VS



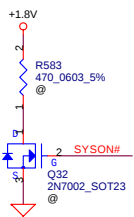
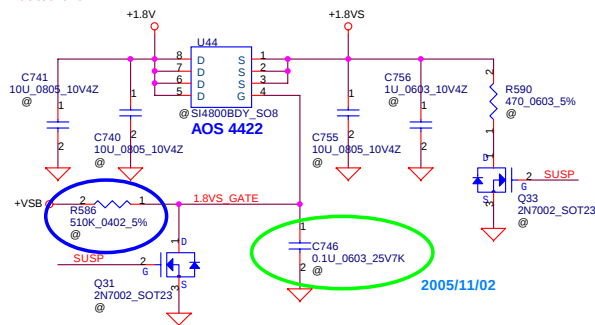
For EMI Request to add:

2006/7/05



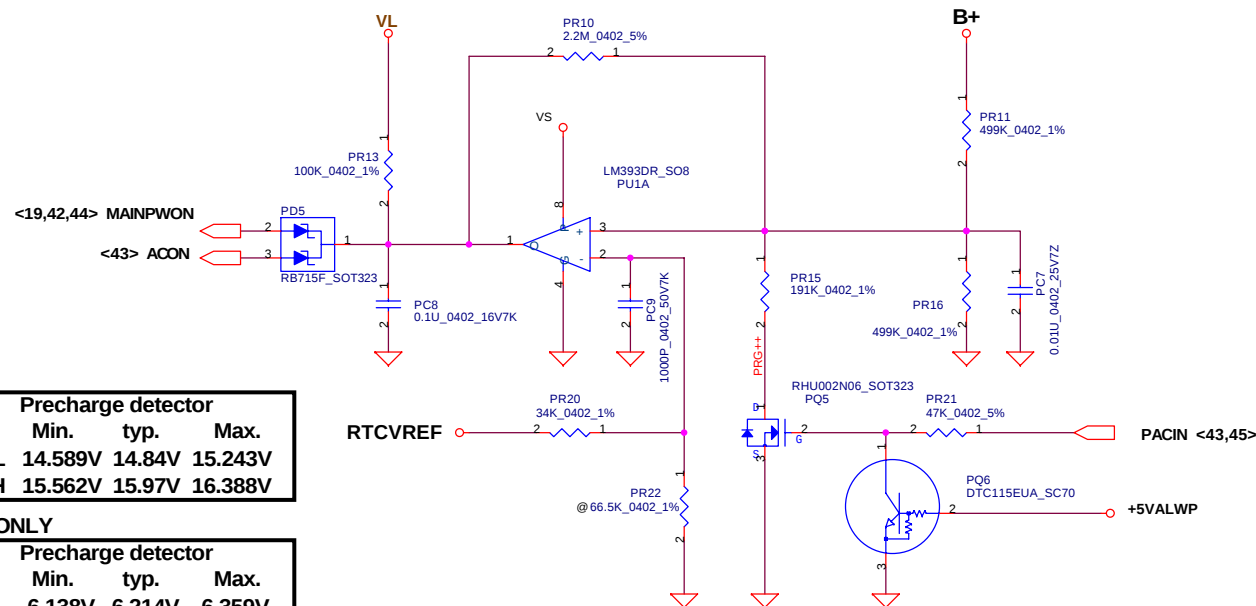
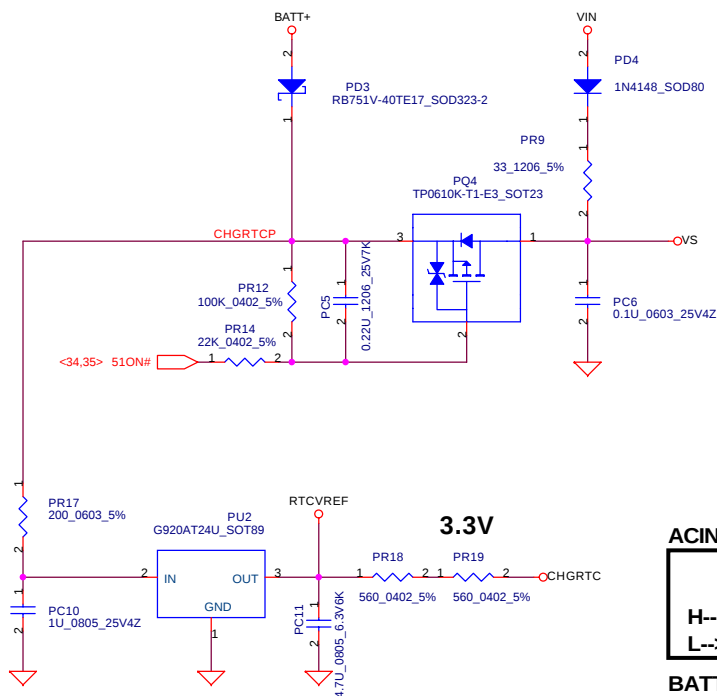
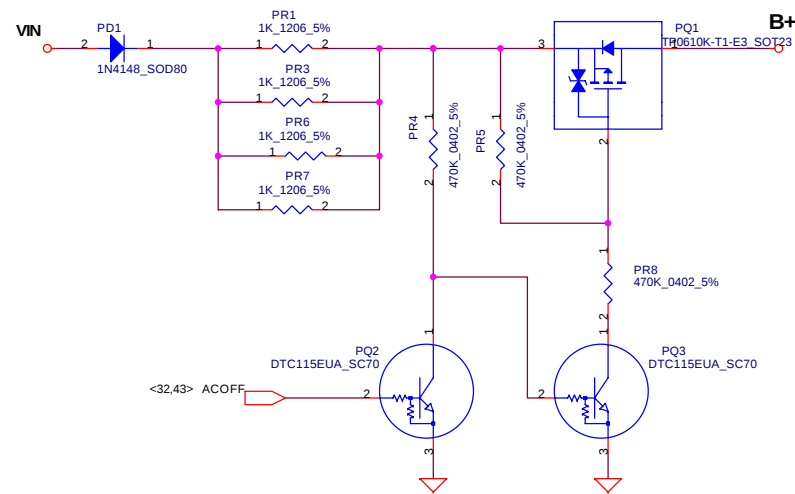
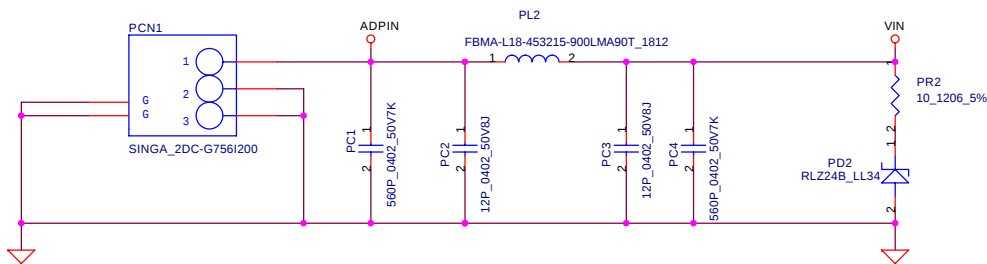
+1.8V to +1.8VS (change BOM structure to "@")

2006/04/19



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					401405	
				Date	星期四, 十月 05, 2006	Sheet 40 of 47

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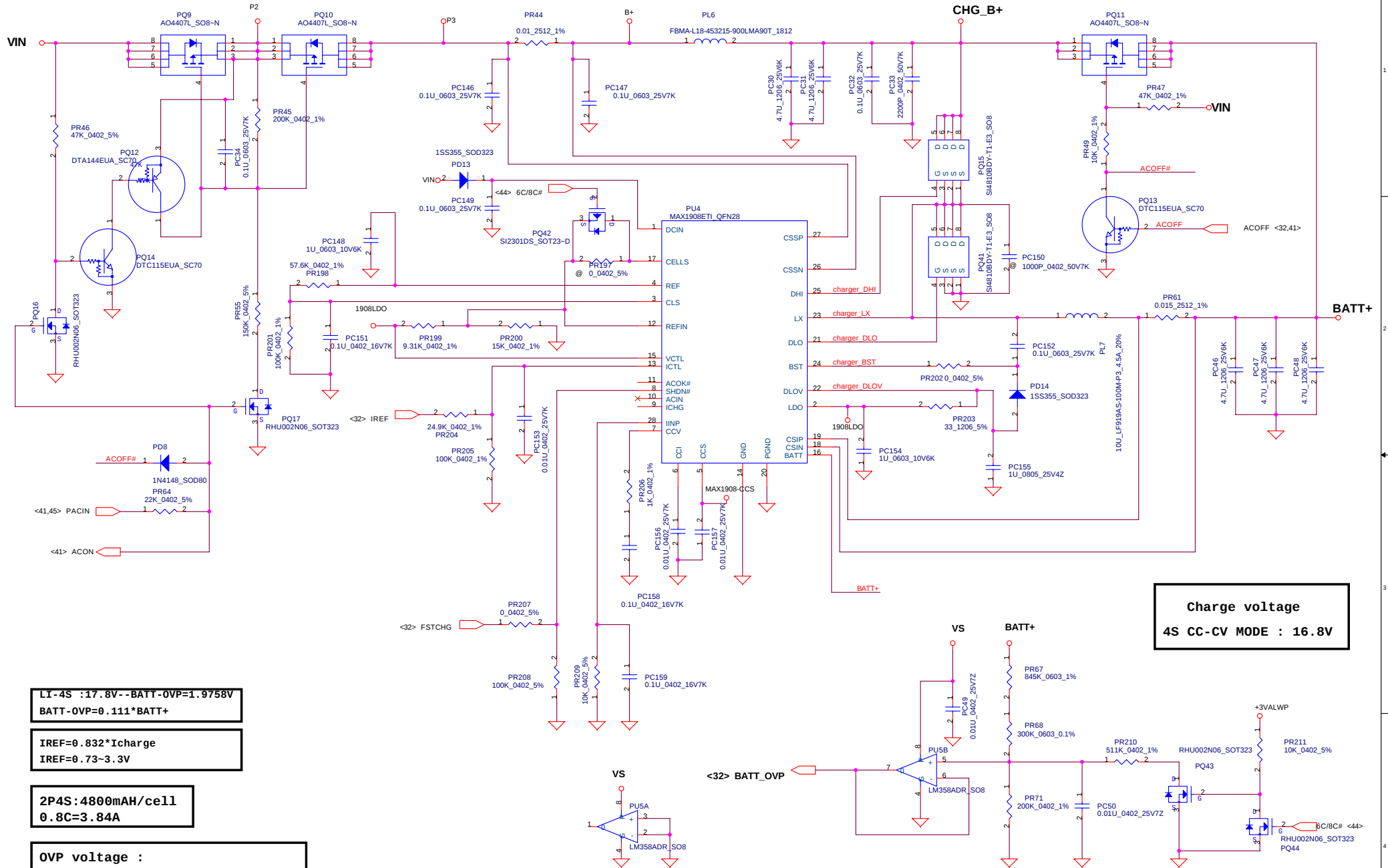


ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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					401405
				Date:	星期四, 十月 05, 2006
				Sheet	41 of 47

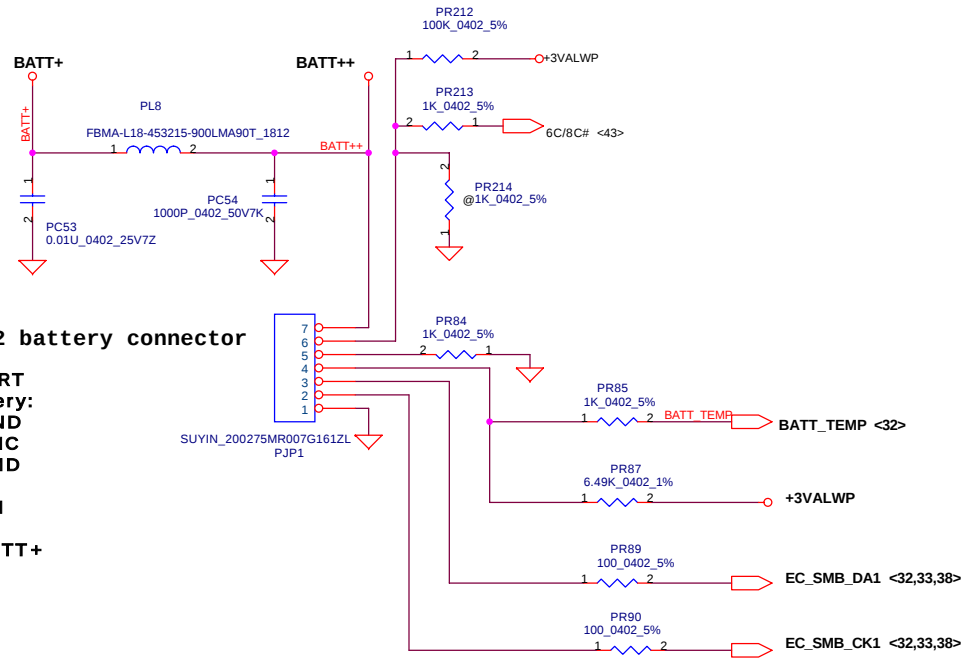
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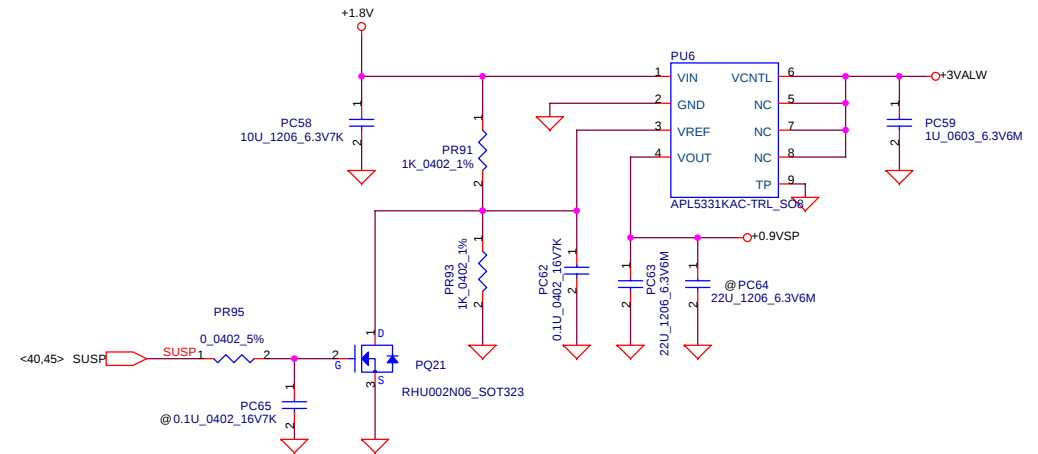
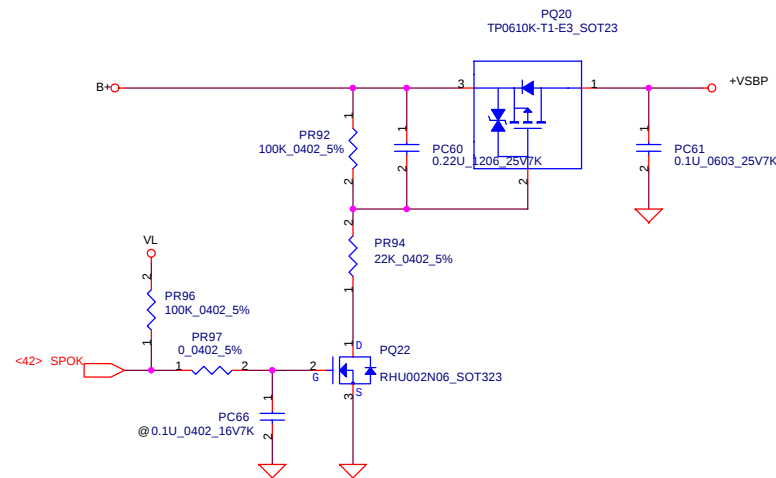
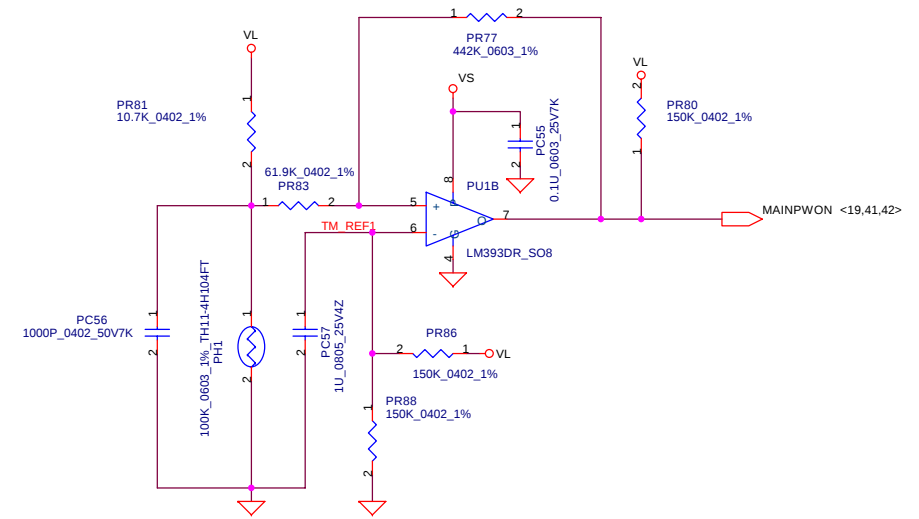
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				401405	
				Date	Rev G
				星期四, 十月 05, 2006	Sheet 43 of 47

PJP2 battery connector

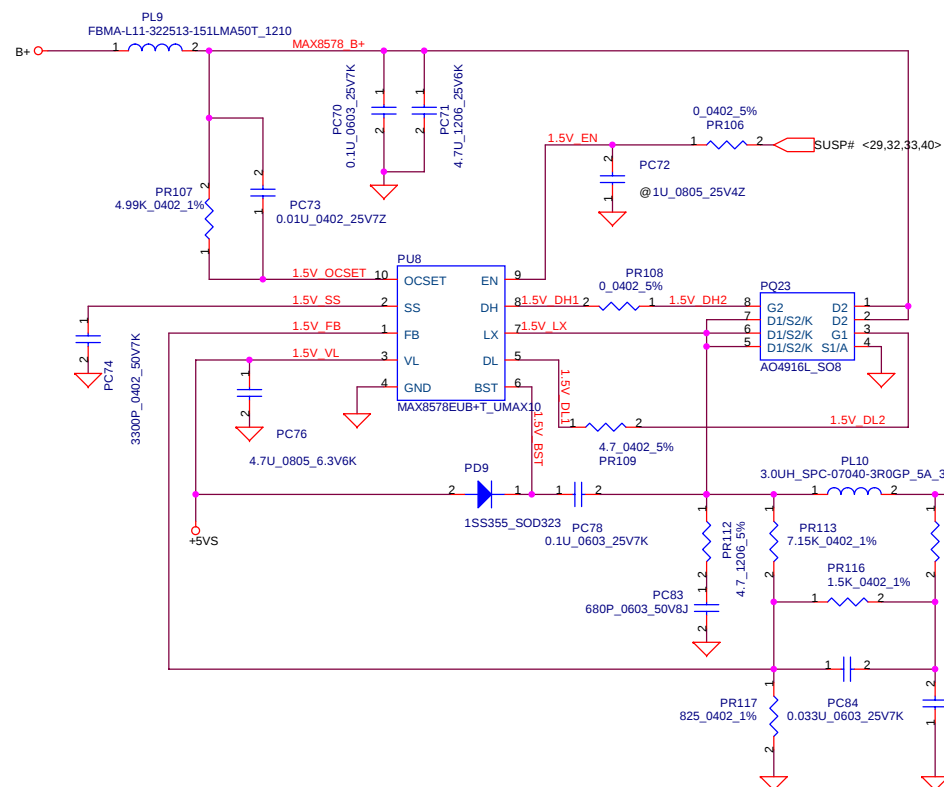
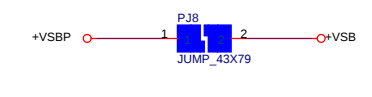
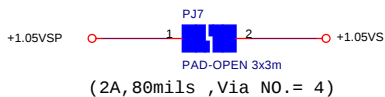
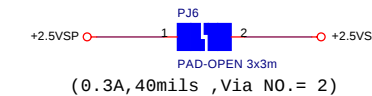
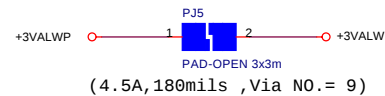
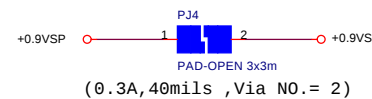
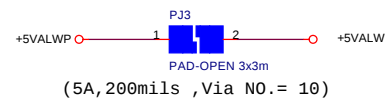
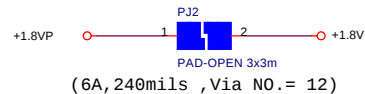
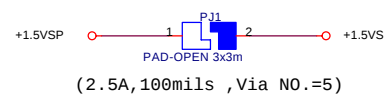
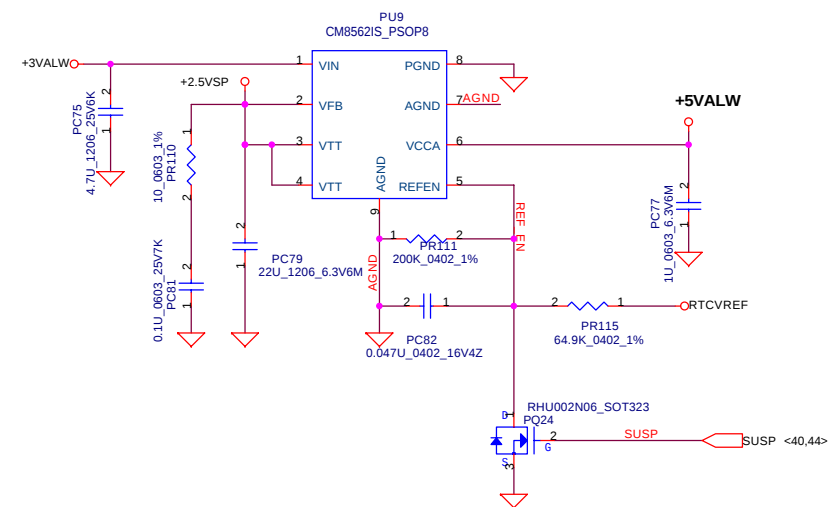
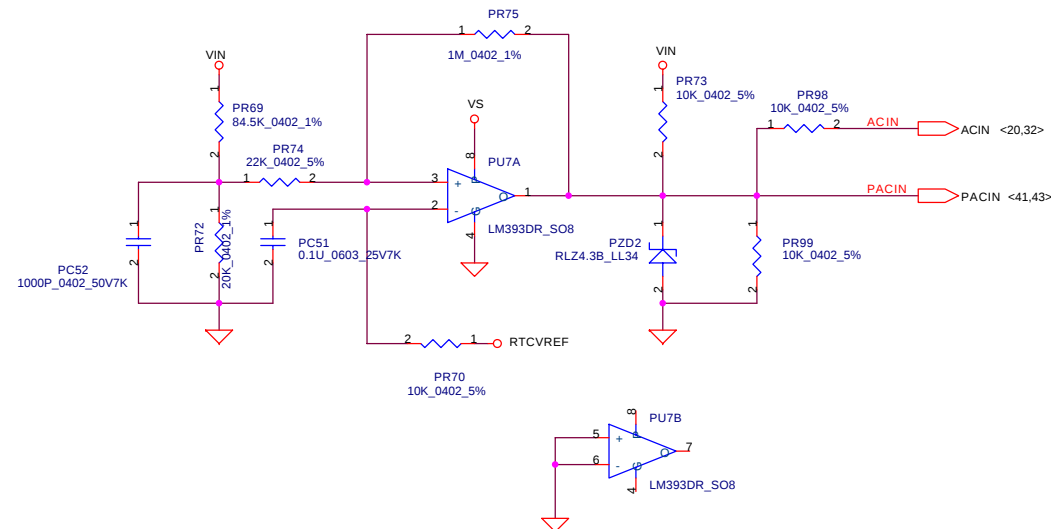
SMART Battery:
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+



PH1 under CPU botten side :
CPU thermal protection at 80 degree C
Recovery at 44(45) degree C



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				Date: 星期四, 十月 05, 2006	Sheet 44 of 47

**Vin Detector**
17.90V/17.24V

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				401405	
				Date: 星期四, 十月 05, 2006	Sheet 45 of 47

