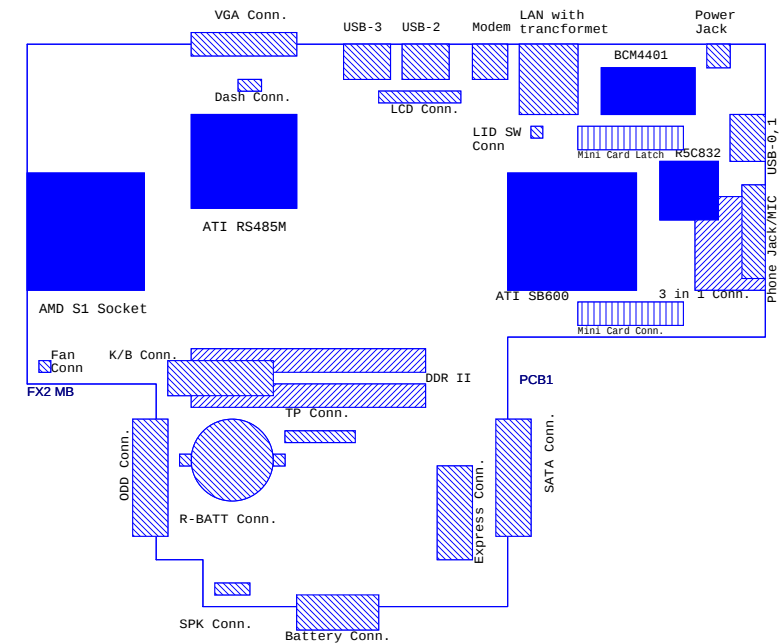
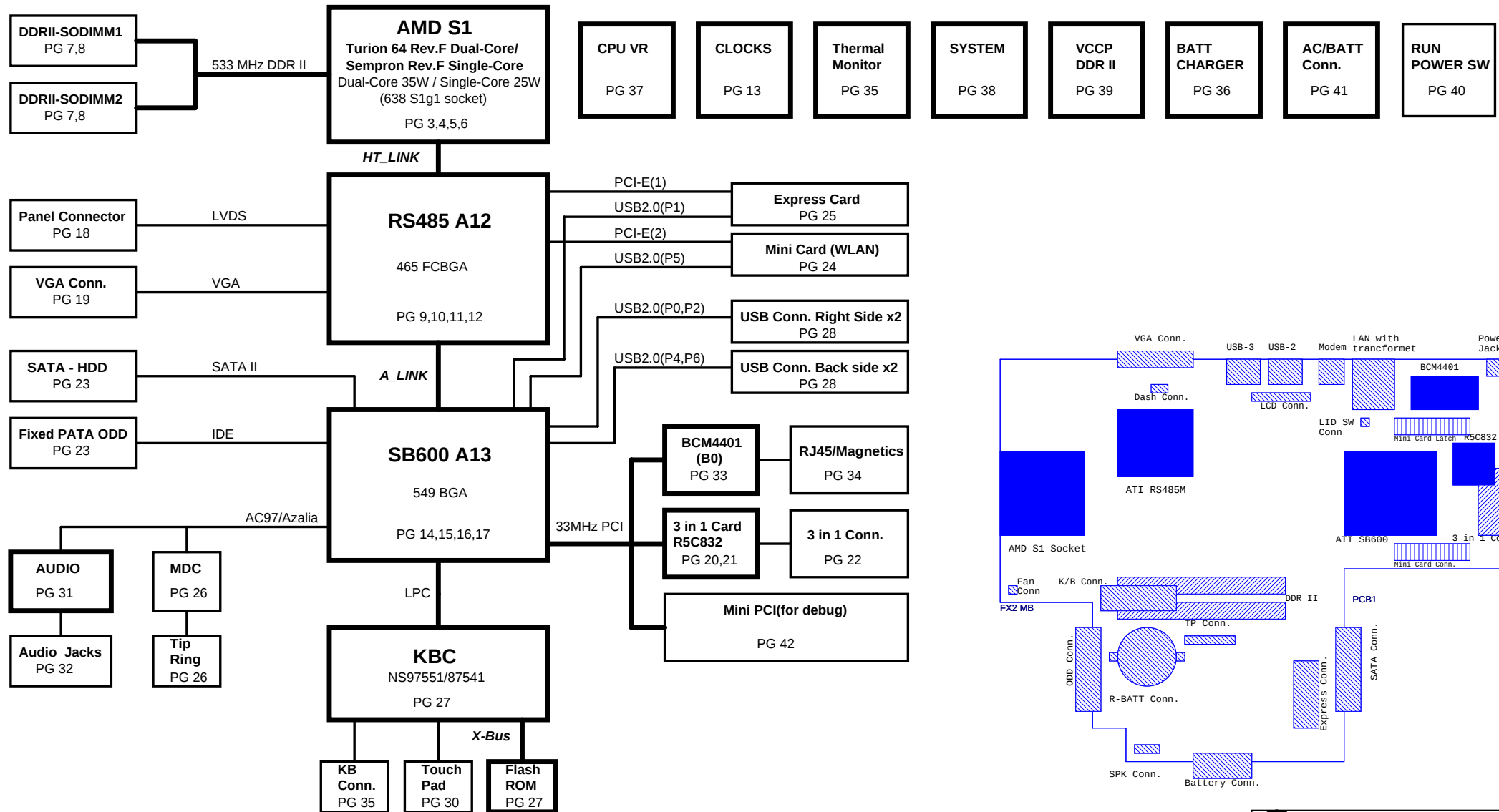


Kirin (FX2 with NS) VER : 1A



Title			BLOCK DIAGRAM
Size	Document Number	Rev	
	FX2	1A	
Date:	Friday, May 05, 2006	Sheet	1 of 47

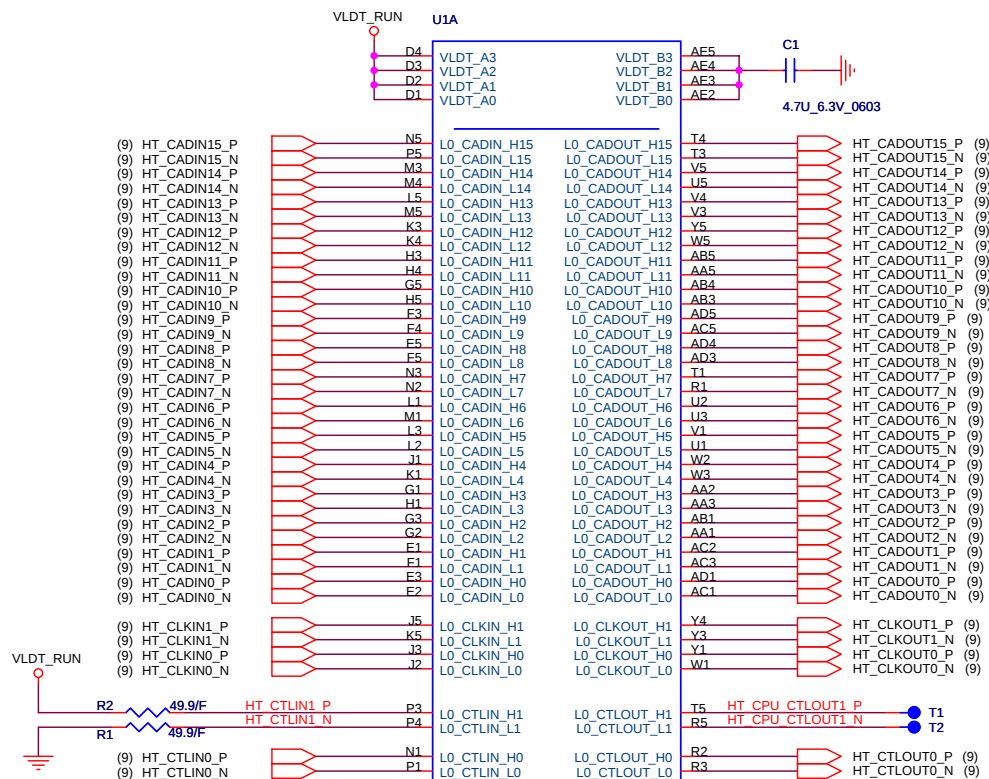
INDEX

Page	Description
1	BLOCK DIAGRAM
2	FRONT PAGE
3	ATHLON64 HT I/F
4	ATHLON64 DDRII MEMORY
5	ATHLON64 CTRL & DEBUG
6	ATHLON64 PWR & GND
7	DDRII SODIMMX2
8	DDRII TERMINATION
9	RS485-HT LINK0 I/F
10	RS485-PCIE LINK I/F
11	RS485-LVDS
12	RS485-POWER
13	CLOCK GENERATOR
14	SB600M-PCIE/PCI/LPC
15	SB600M ACPI/USB/AC97
16	SB600M HDD/POWER
17	SB600M STRAPS
18	LCD CONN
19	CRT
20	5C832/PCI
21	CARD READER
22	CARD READER CONN
23	SATA HDD & PATA ODD
24	MINI Card
25	MINI Card
26	MDC CONN
27	PC97551 & FLASH
28	USB
29	EMI & Screw hole
30	SWITCH & TP & LED
31	Azelia CODEC
32	AUDIO CONN
33	LAN(BCM4401)
34	LAN JACK
35	KB & THERMAL & FAN
36	CHARGER (MAX8731)
37	VHCORE (MAX8774)
38	SYSTEM (MAX8734)
39	VCCP & DDR2 (MAX8743)
40	RUN POWER SW
41	DCIN,Batt
42	MINI PCI(for debug)
43	Power On Sequence
44	Power On Diagram
45	SMBUS BLOCK

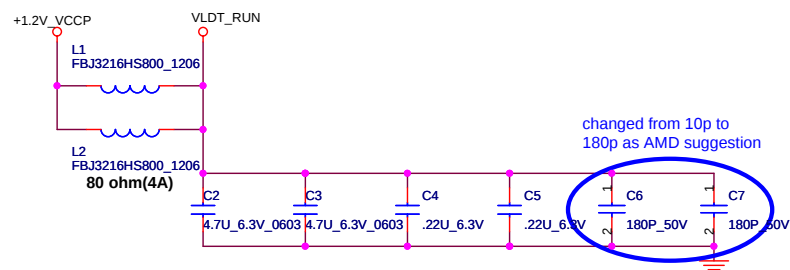


PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1
Processor Socket



LAYOUT: Place bypass cap on topside of board



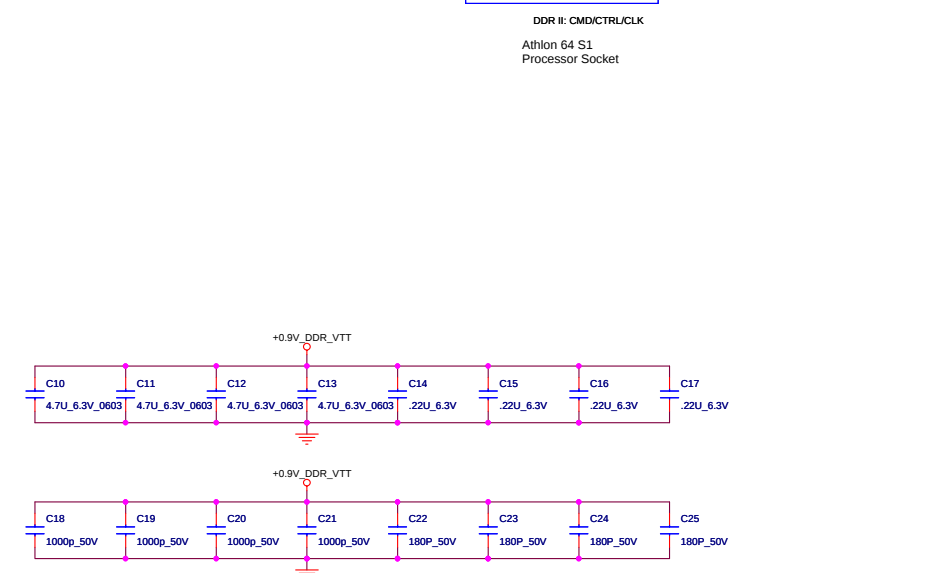
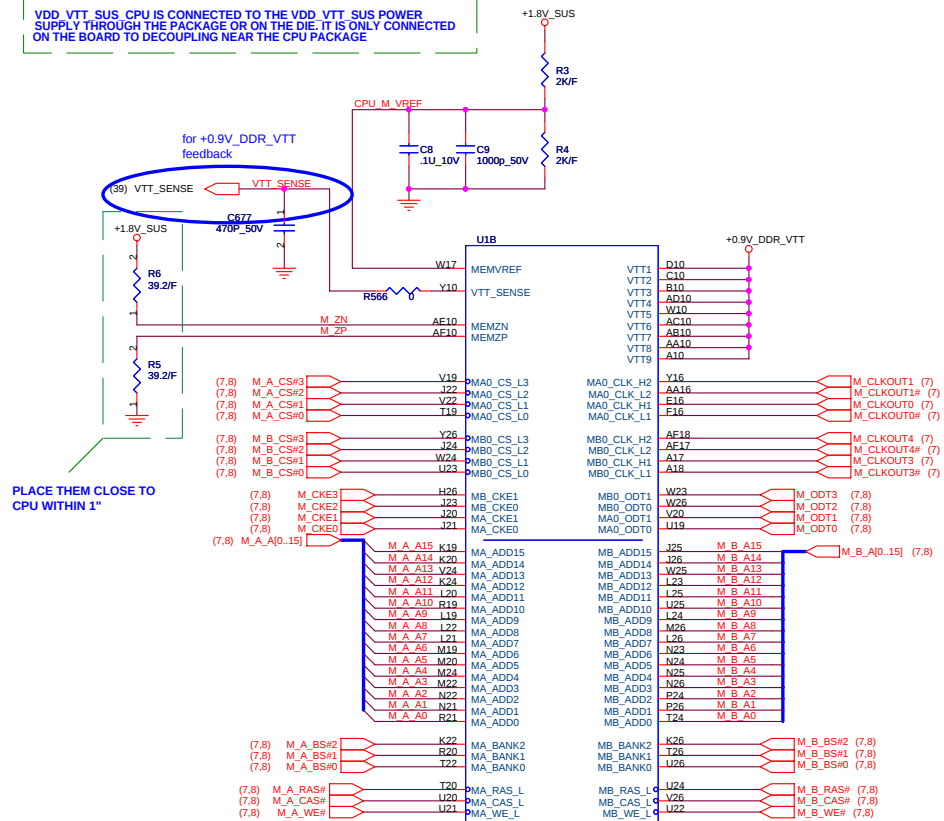
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



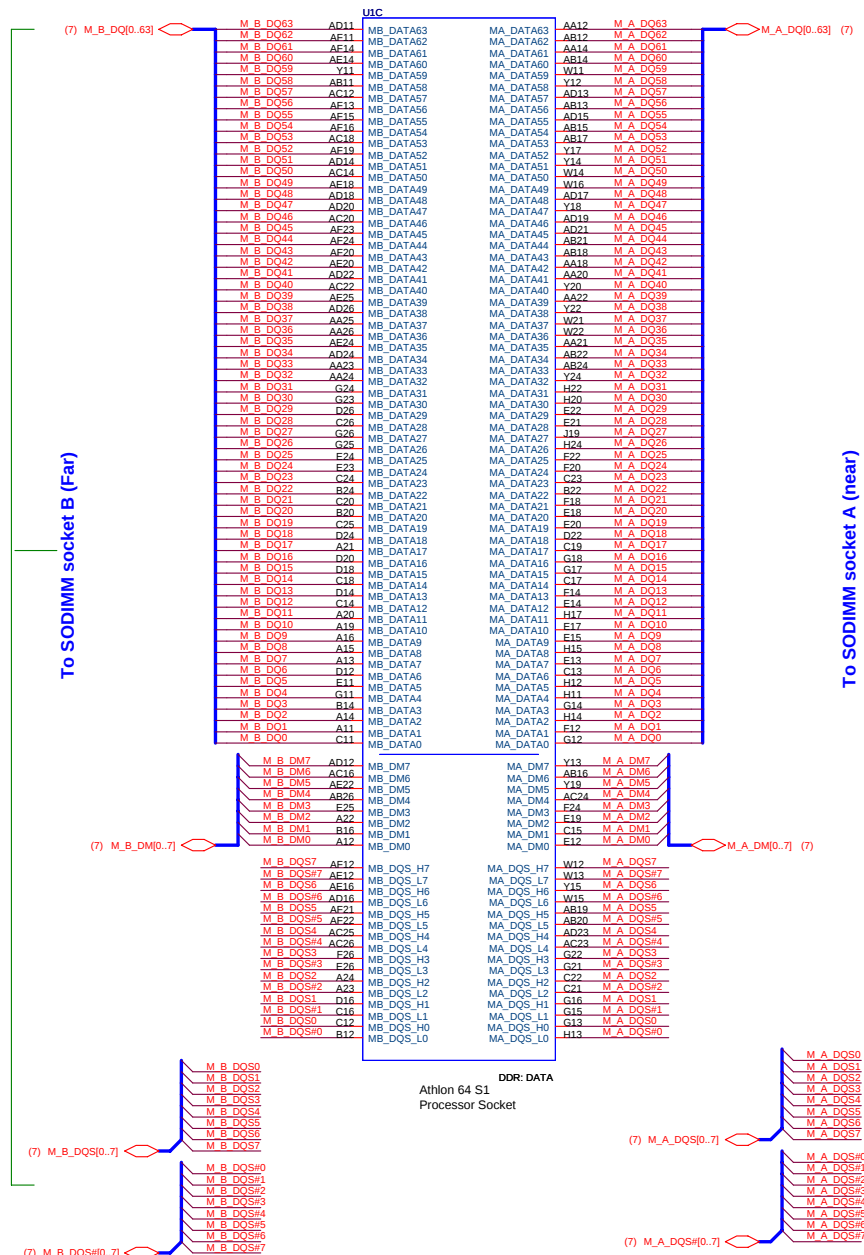
QUANTA
COMPUTER

Title		
ATHLON64 HT I/F		
Size	Document Number FX2	Rev 1A
Date:	Friday, May 05, 2006	Sheet 3 of 47

VDD, VTT, SUS, CPU, IS CONNECTED TO THE VDD, VTT, SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



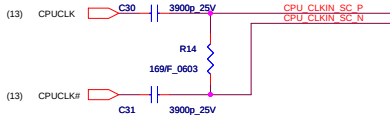
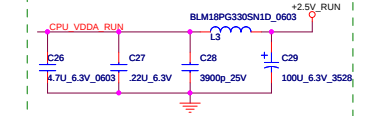
Processor DDR2 Memory Interface



ATHLON Control and Debug

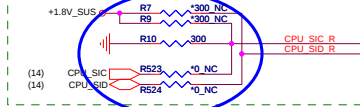
LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN



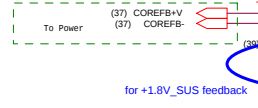
R14 close U1 within 600 mil, C30 & C31 close U1 within 1250 mil

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pull-down to VSS.

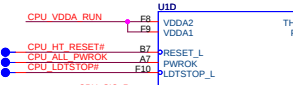


for CPU rev.F; if for rev.G, populate R7,R9,R523,R524 and depopulate R10

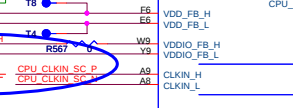
place them to CPU within 1"



for +1.8V_SUS feedback



place them to CPU within 1"



for +1.8V_SUS feedback

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

add port to Page 35 U36 Thermal IC

delete ED5 H_THERMTRIP# circuit

delete ED5 thermal sensor

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

add HDT connector for debug convenience

delete ED5 thermal sensor

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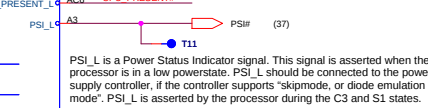
delete ED5 thermal sensor

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add HDT connector for debug convenience



place them to CPU within 1"



for +1.8V_SUS feedback

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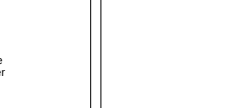
delete ED5 thermal sensor

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

add HDT connector for debug convenience



place them to CPU within 1"



for +1.8V_SUS feedback

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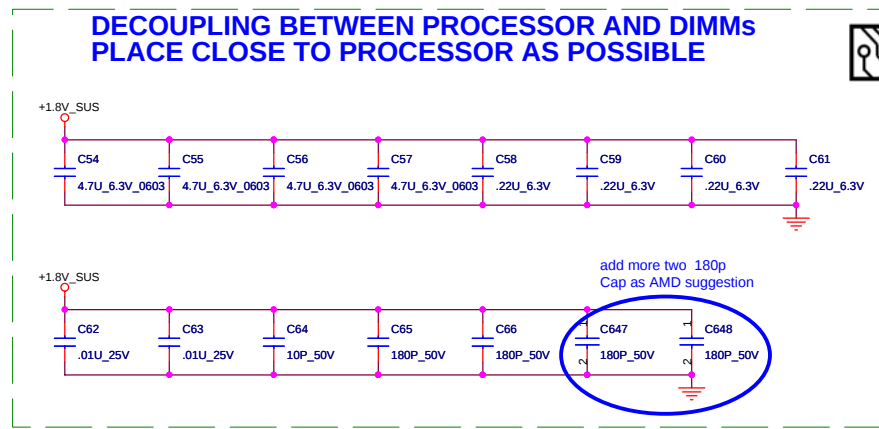
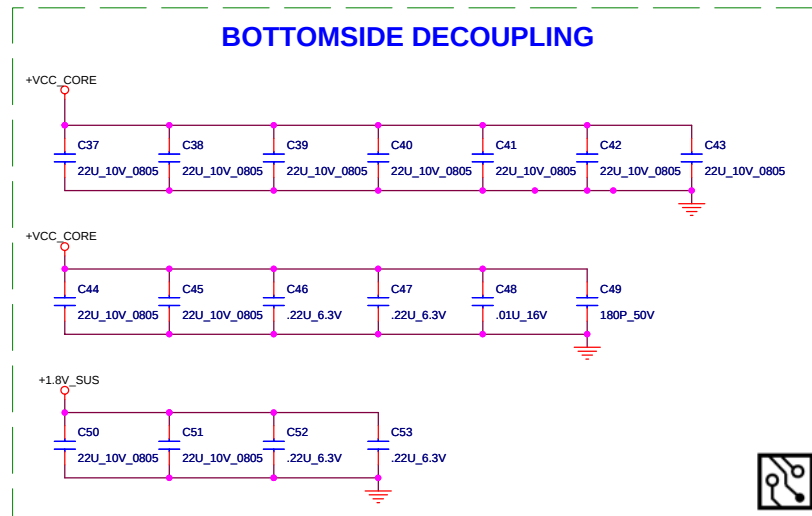
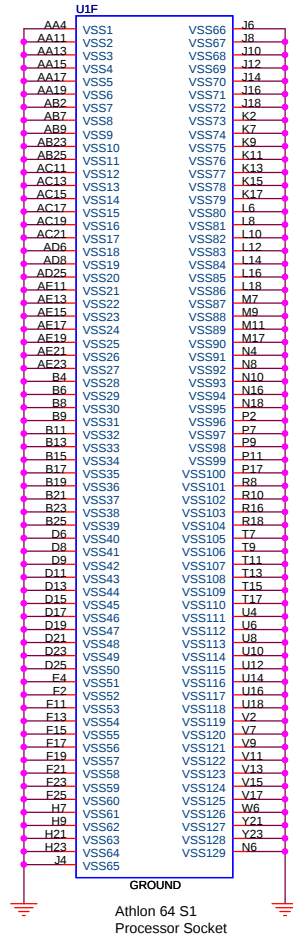
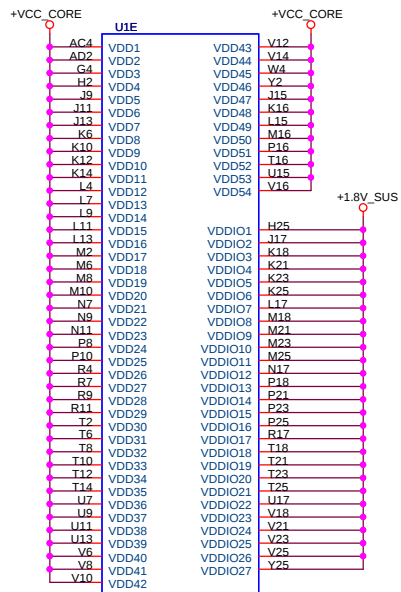
add port to Page 35 U36 Thermal IC

delete ED5 H_THERMTRIP# circuit

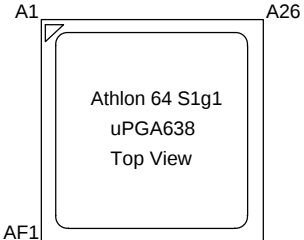
delete ED5 thermal sensor

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

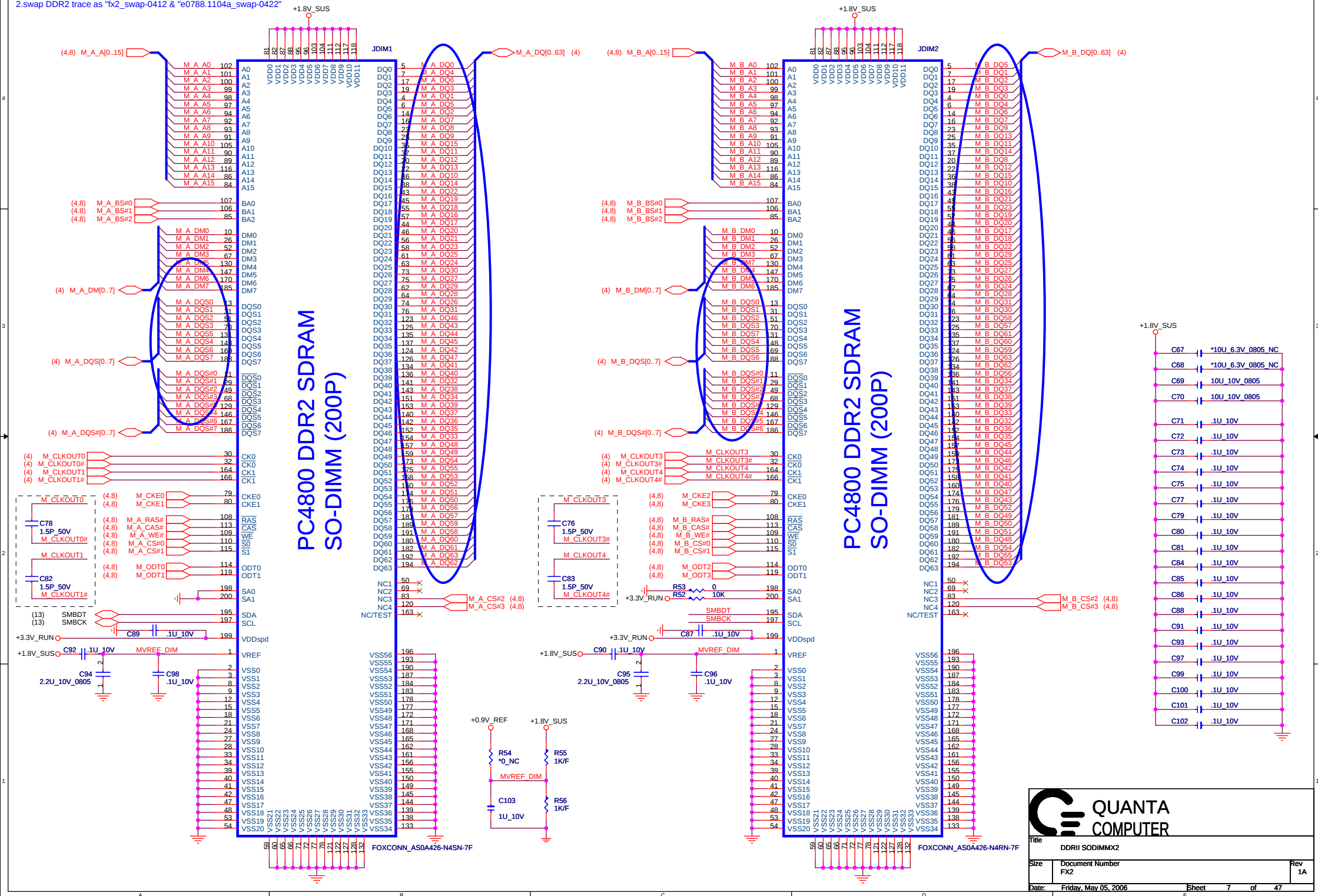
add HDT connector for debug convenience

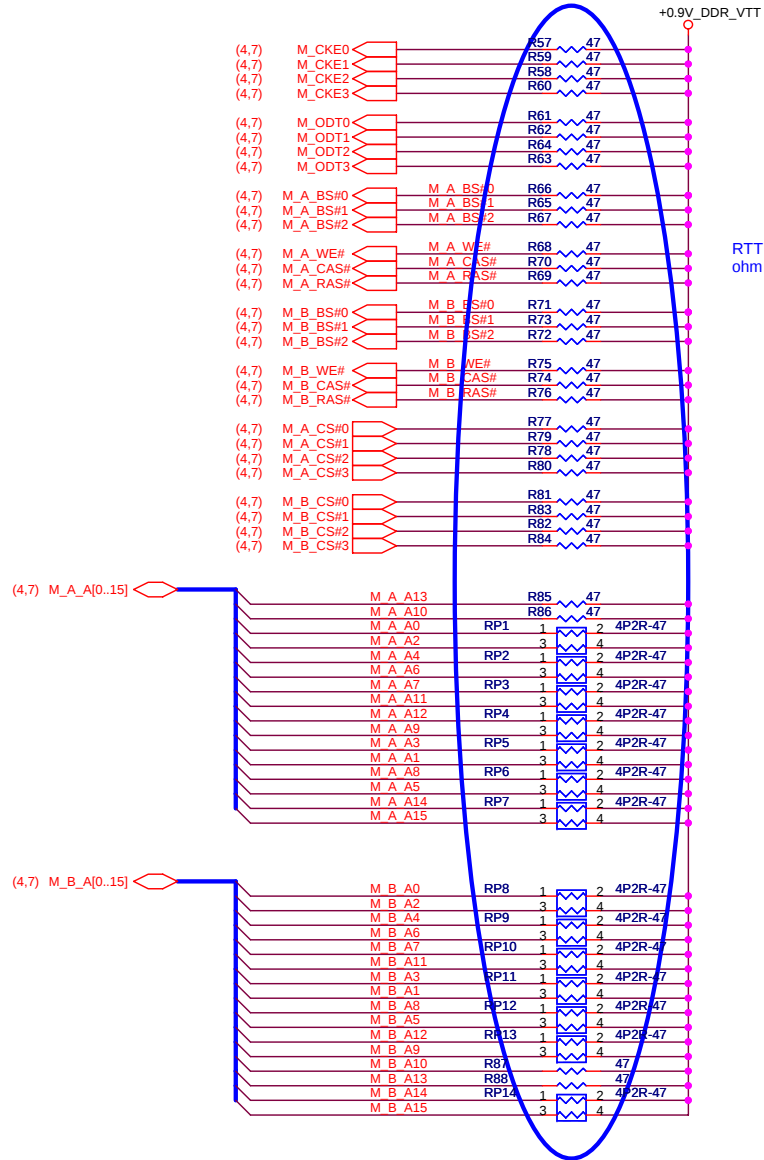
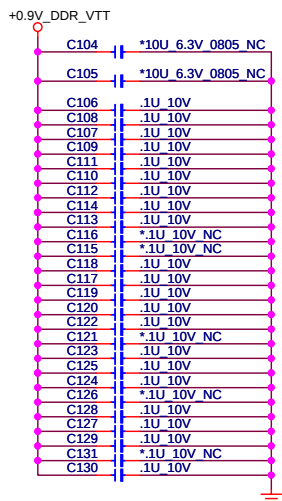


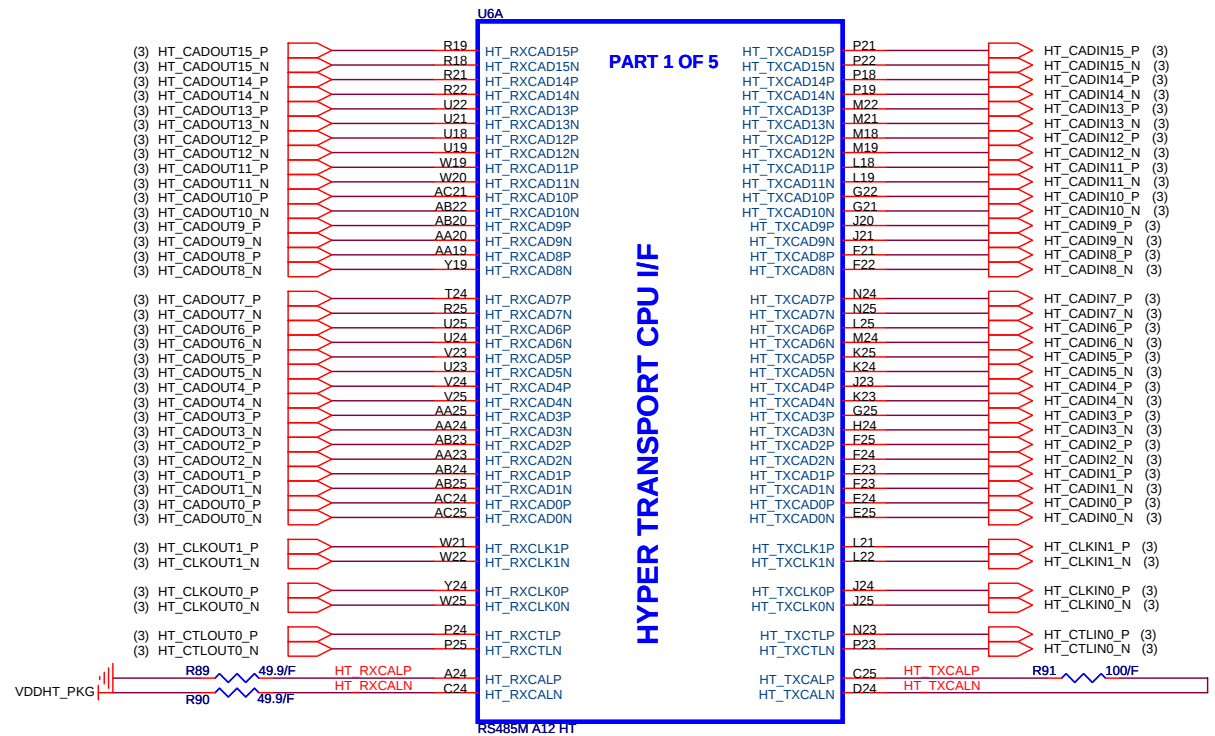
PROCESSOR POWER AND GROUND



- 2.swap DDR2 trace as "fx2_swap-0412" & "e0788.1104a_swap-0422"









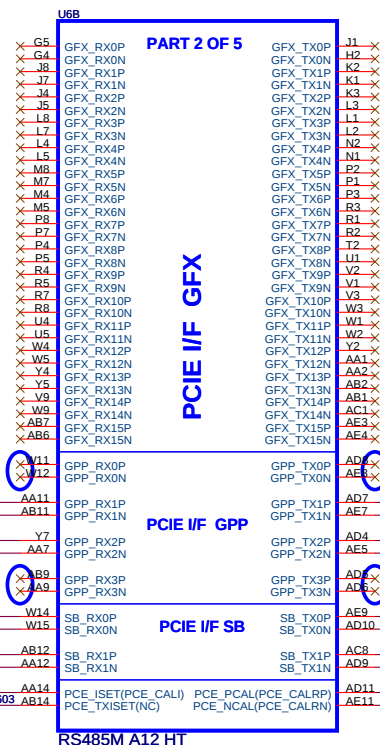
(25) PCIE_RXP1
(25) PCIE_RXN1

(24) MINI_PCIE_RXP2
(24) MINI_PCIE_RXN2

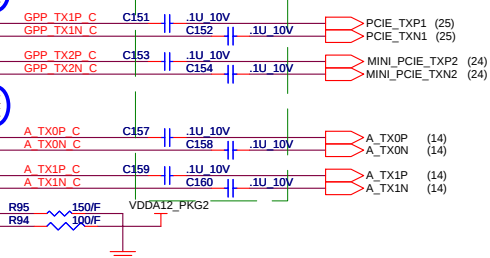


R93: 10KOhm FOR RS485
1.47KOhm FOR RS690

R92: 8.25KOhm FOR RS485
DNI FOR RS690



Place these caps
close to connector



R95: 150 Ohm FOR RS485
562 Ohm FOR RS690

R94: Ward update to 100 Ohm FOR RS485
2KOhm FOR RS690



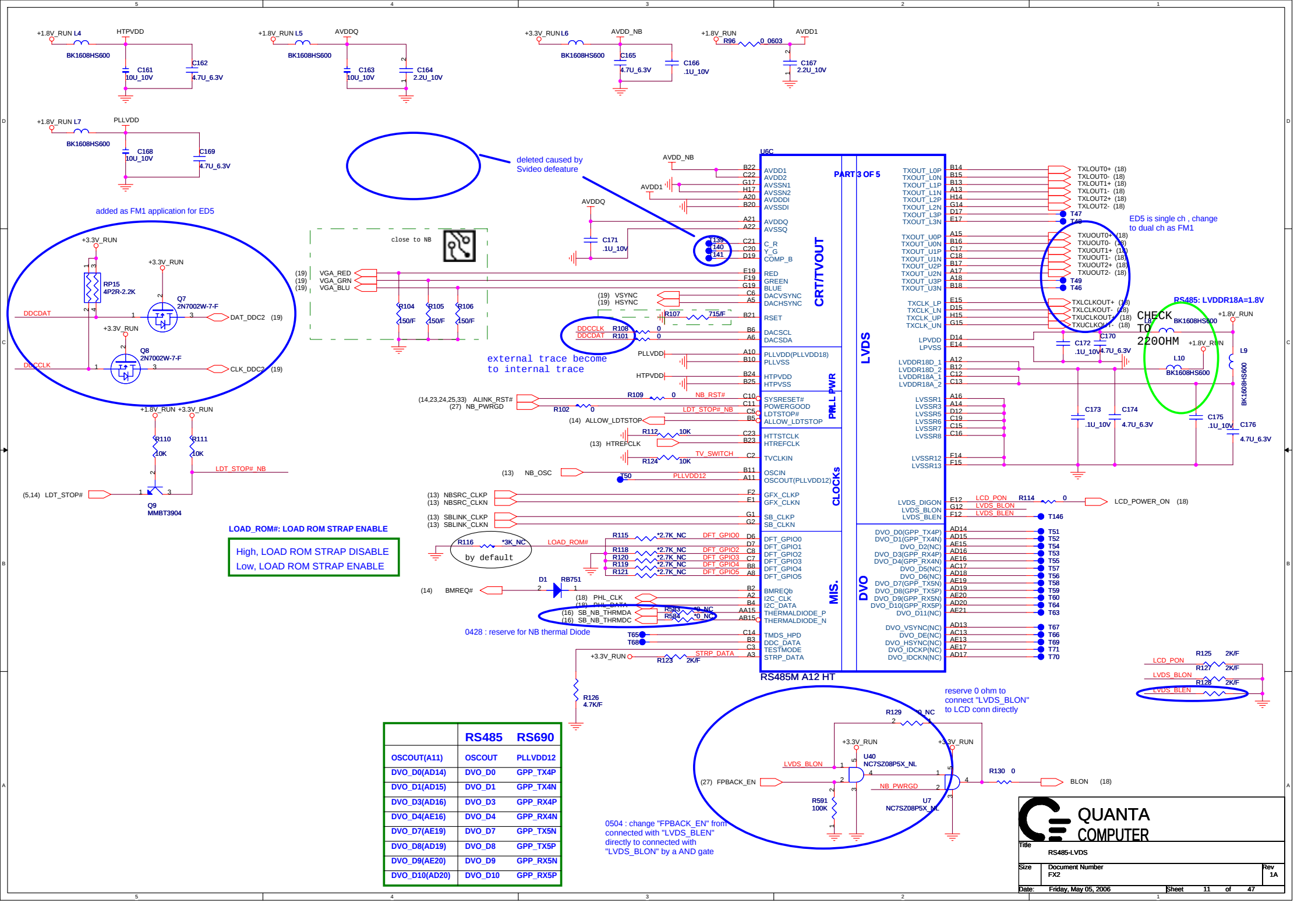
Title RS485-PCIE LINK I/F

Size	Document Number FX2
------	------------------------

Date: Friday, May 05, 2006

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Rev
1A



deleted caused by
Svideo defeature

added as FM1 application for ED5

close to NB

external trace become
to internal trace

LOAD_ROM#: LOAD ROM STRAP ENABLE

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

0428 : reserve for NB thermal Diode

0504 : change "FPBACK_EN" from
connected with "LVDS_BLEN"
directly to connected with
"LVDS_BLON" by a AND gate

reserve 0 ohm to
connect "LVDS_BLEN"
to LCD conn directly

ED5 is single ch , change
to dual ch as FM1

CHECK
TO

2200HM

RS485: LVDDR18A=1.8V

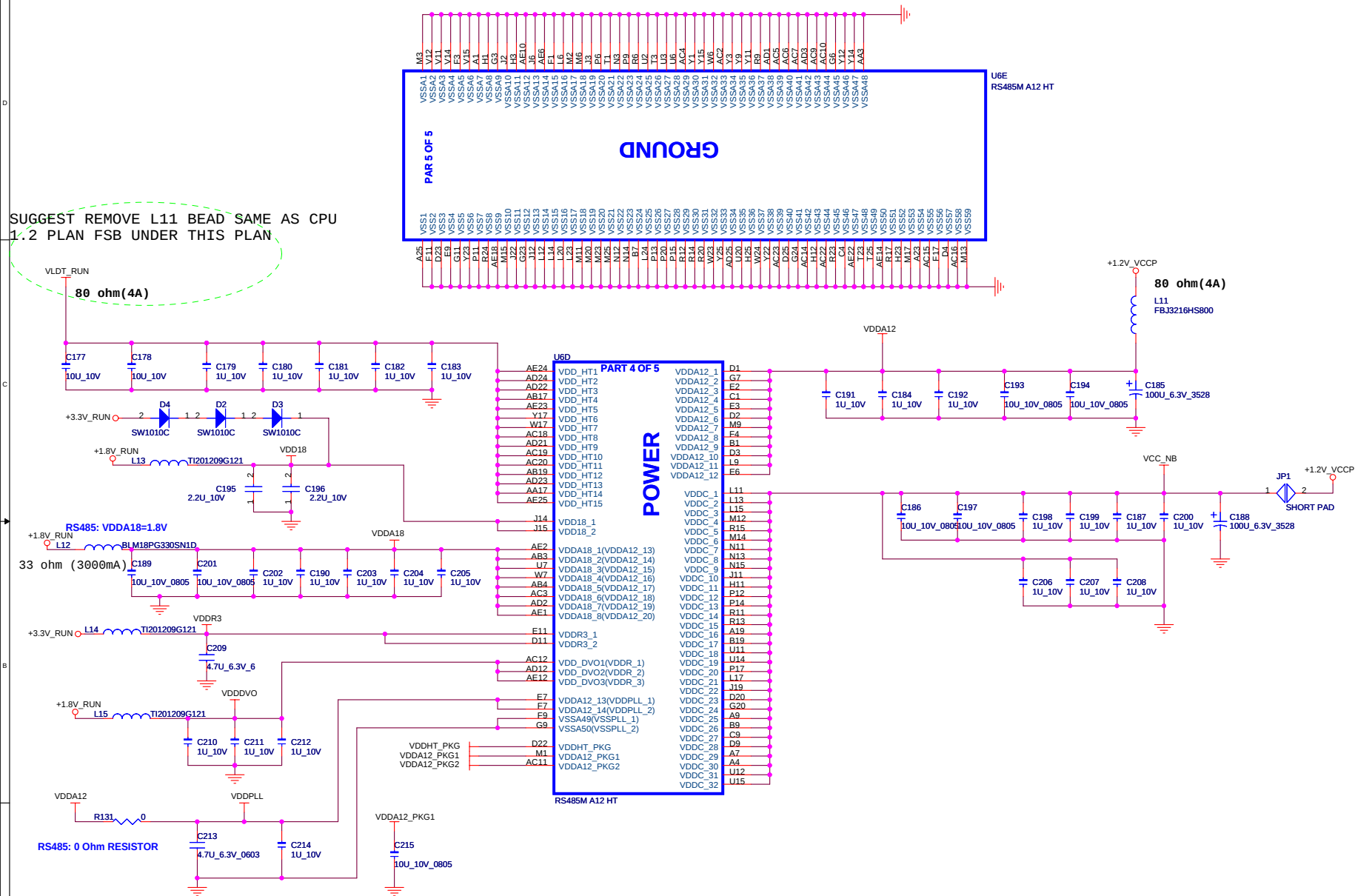
	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P

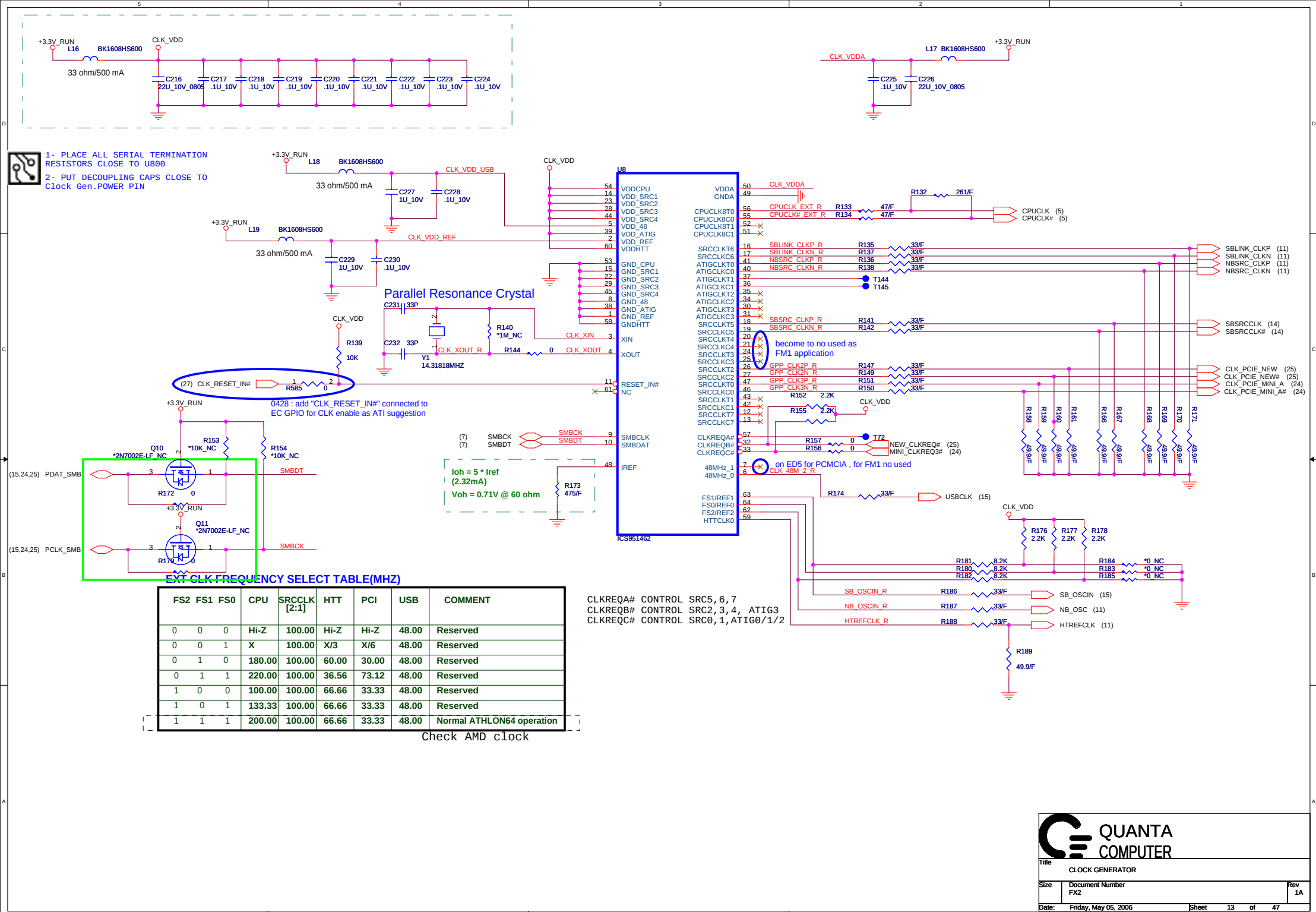


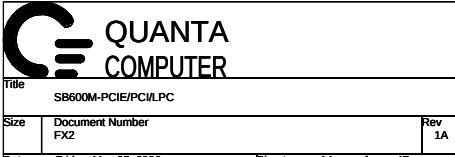
QUANTA
COMPUTER

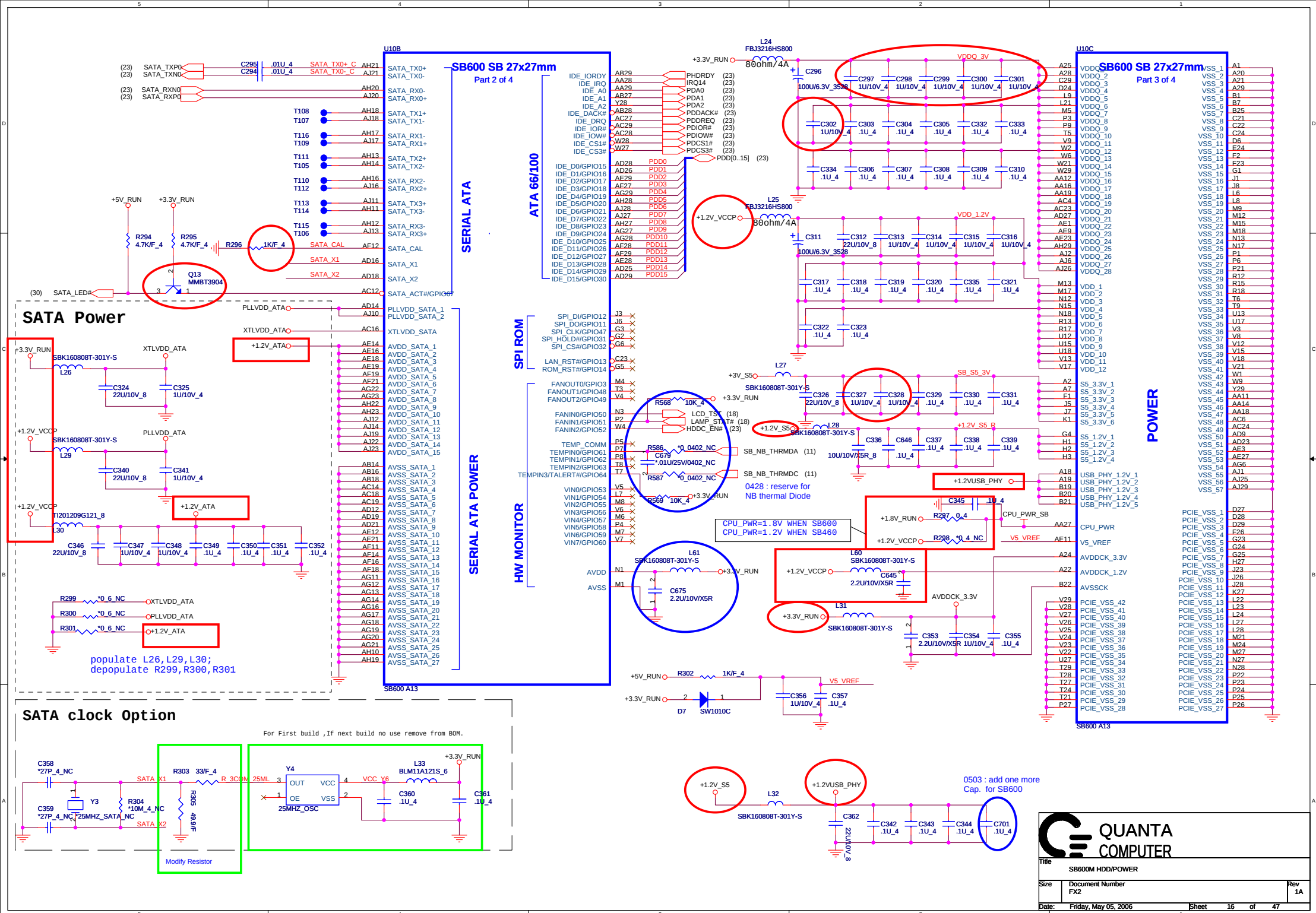
Title RS485-LVDS		
Size FX2	Document Number	Rev 1A
Date Friday, May 05, 2006	Sheet 11	of 47

SUGGEST REMOVE L11 BEAD SAME AS CPU
1.2 PLAN FSB UNDER THIS PLAN

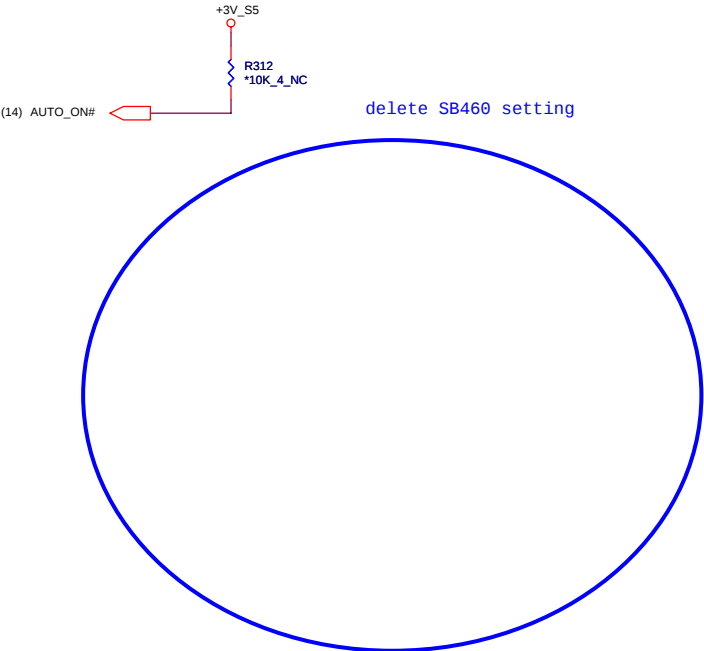
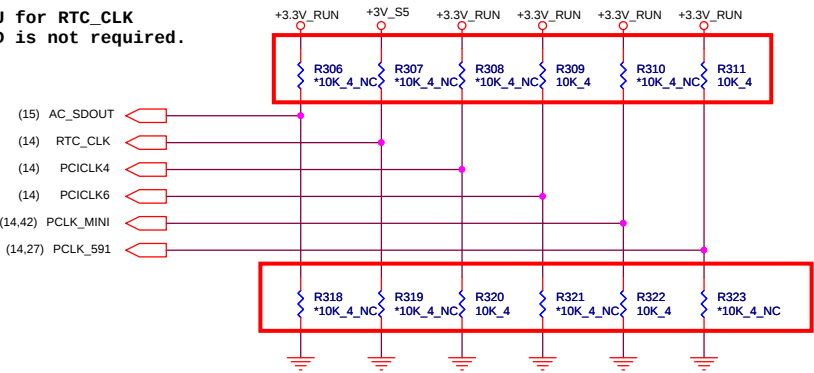






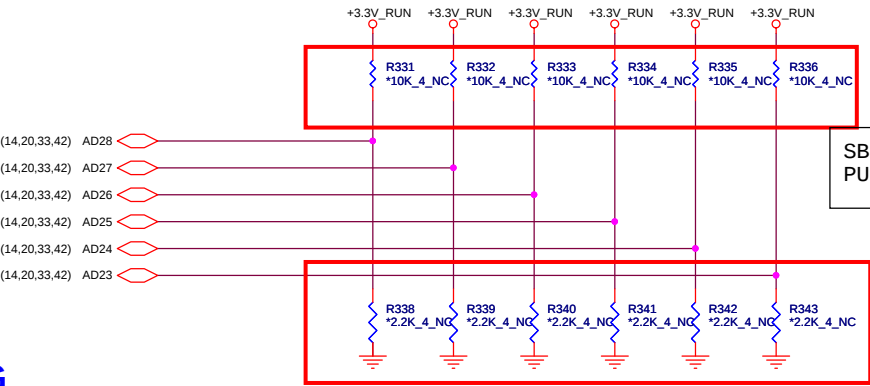


SB600 has 15K internal PD for AC_SDOUT
15K internal PU for RTC_CLK
,External PU/PD is not required.



REQUIRED STRAPS

	PCLK_MINI PCLK_591					
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	H, H = PCI ROM H, L = SPI ROM	
PULL LOW	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	L, H = LPC ROM L, L = FWH ROM	DEFAULT



SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET	Use Long Reset	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	boot fail time disabled
PULL LOW	USE SHORT RESET	Use Short Reset	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	boot fail time enabled
SB460 Only		SB600 Only		SB600 Only			



QUANTA
COMPUTER

TitleSB600M STRAPS

SizeDocument NumberFX2Rev1A

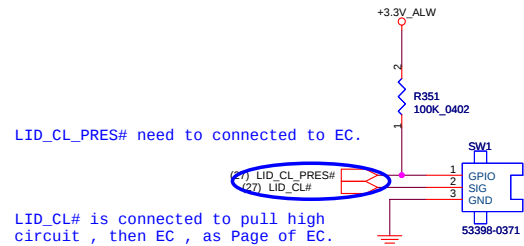
DateFriday, May 05, 2006Sheet17 of 47

change name as ED5 SB.

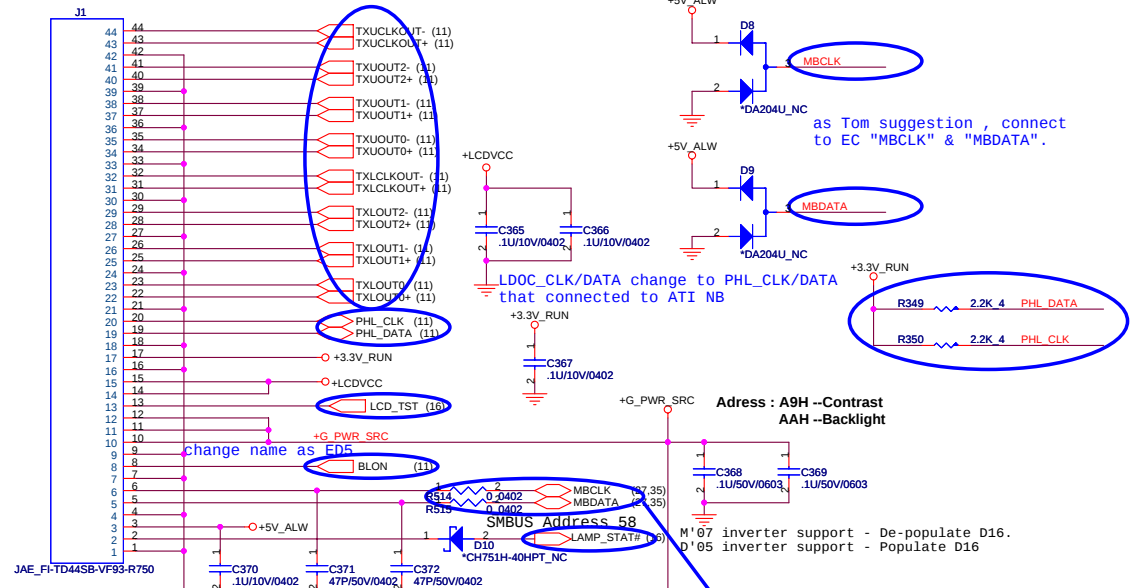


LID_CL_PRES# need to connected to EC.

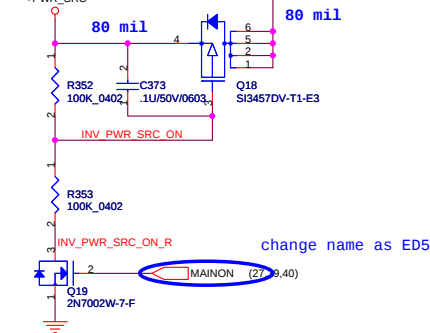
LID_CL# is connected to pull high circuit, then EC, as Page of EC.



change name as ED5 SB.

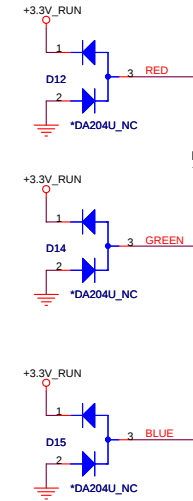
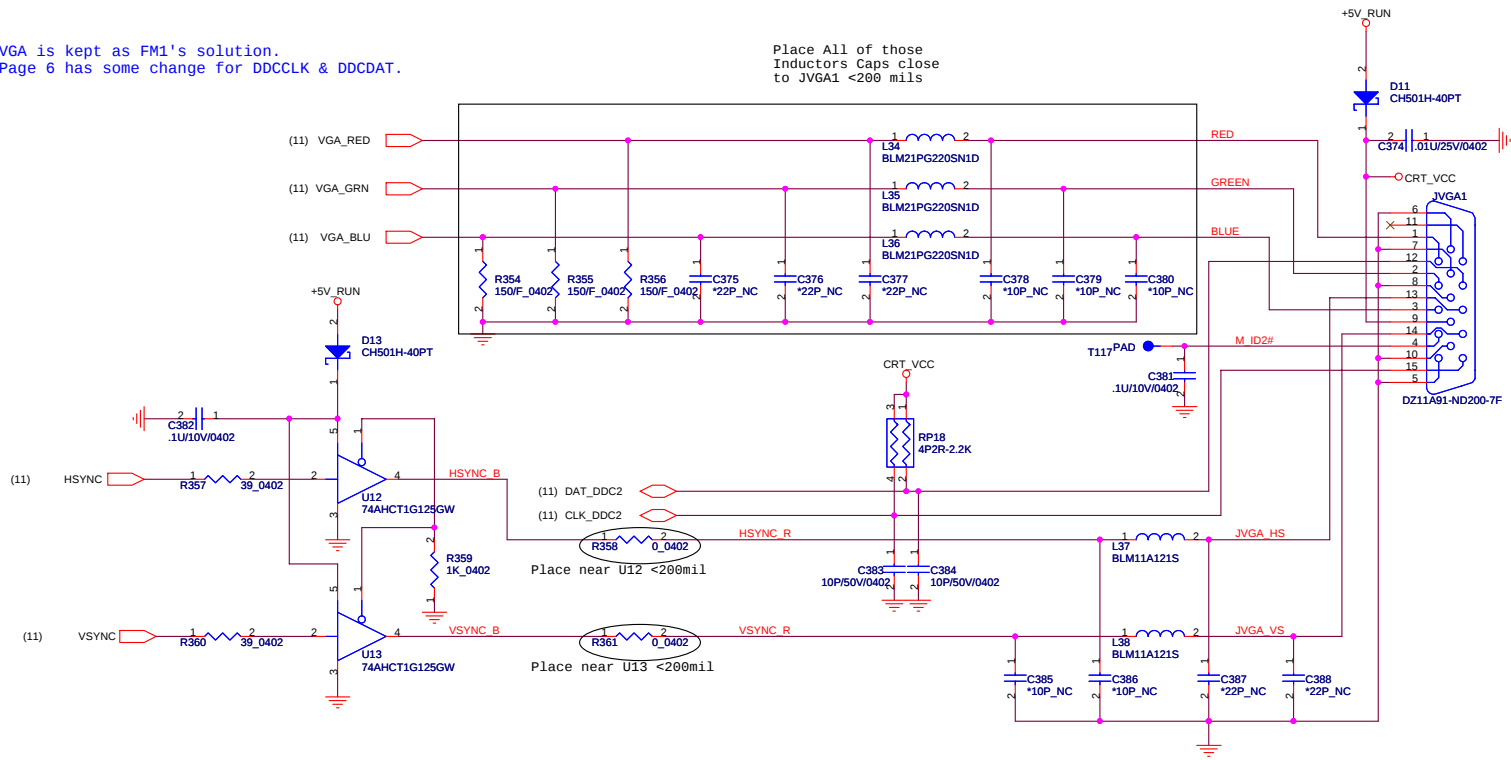


For Discrete:
De-populate J1, R230, C311, C331, C332, D16, C333, C329, C341, C324, C326



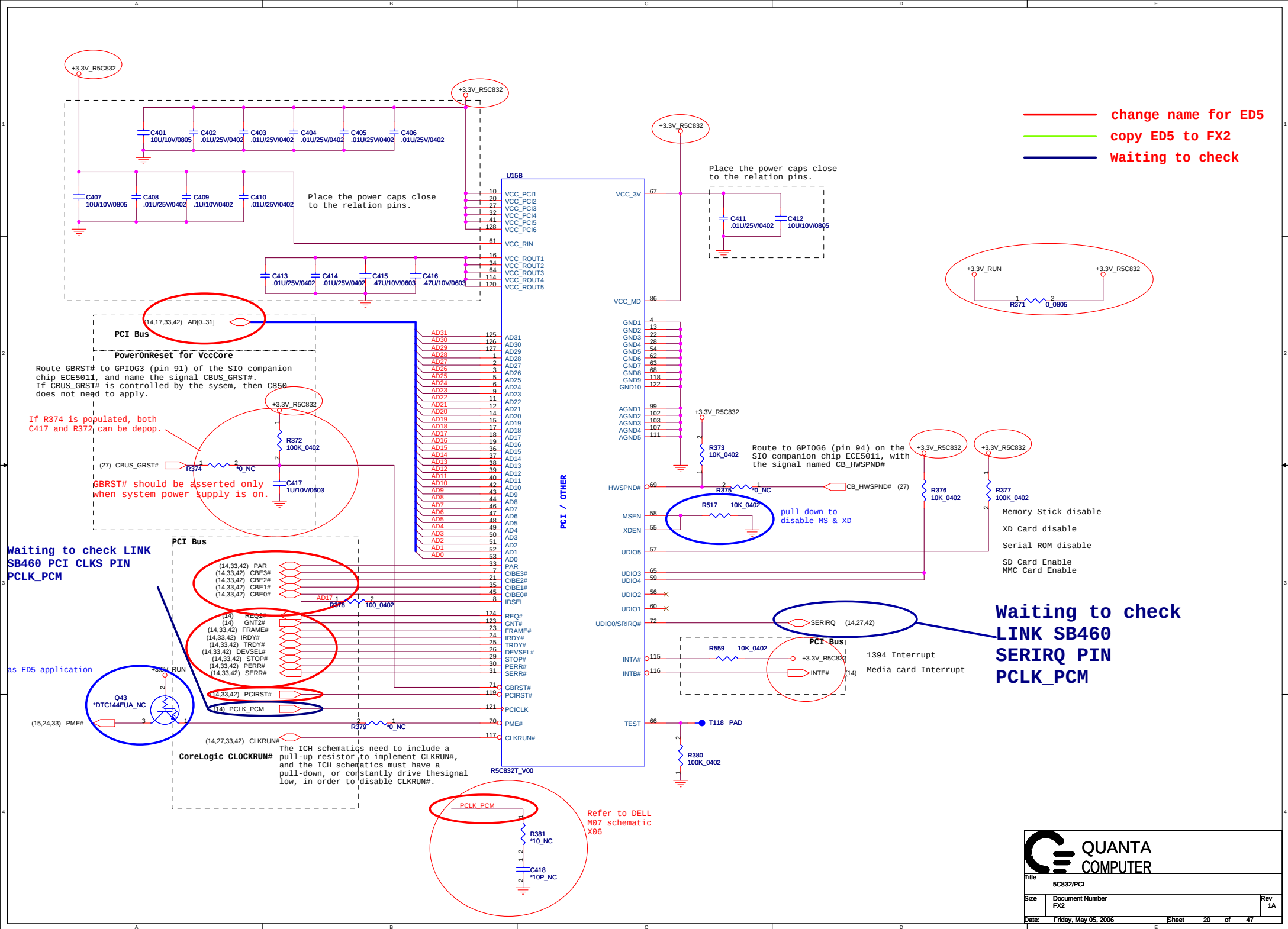
VGA is kept as FM1's solution.
Page 6 has some change for DDCCLK & DDCDAT.

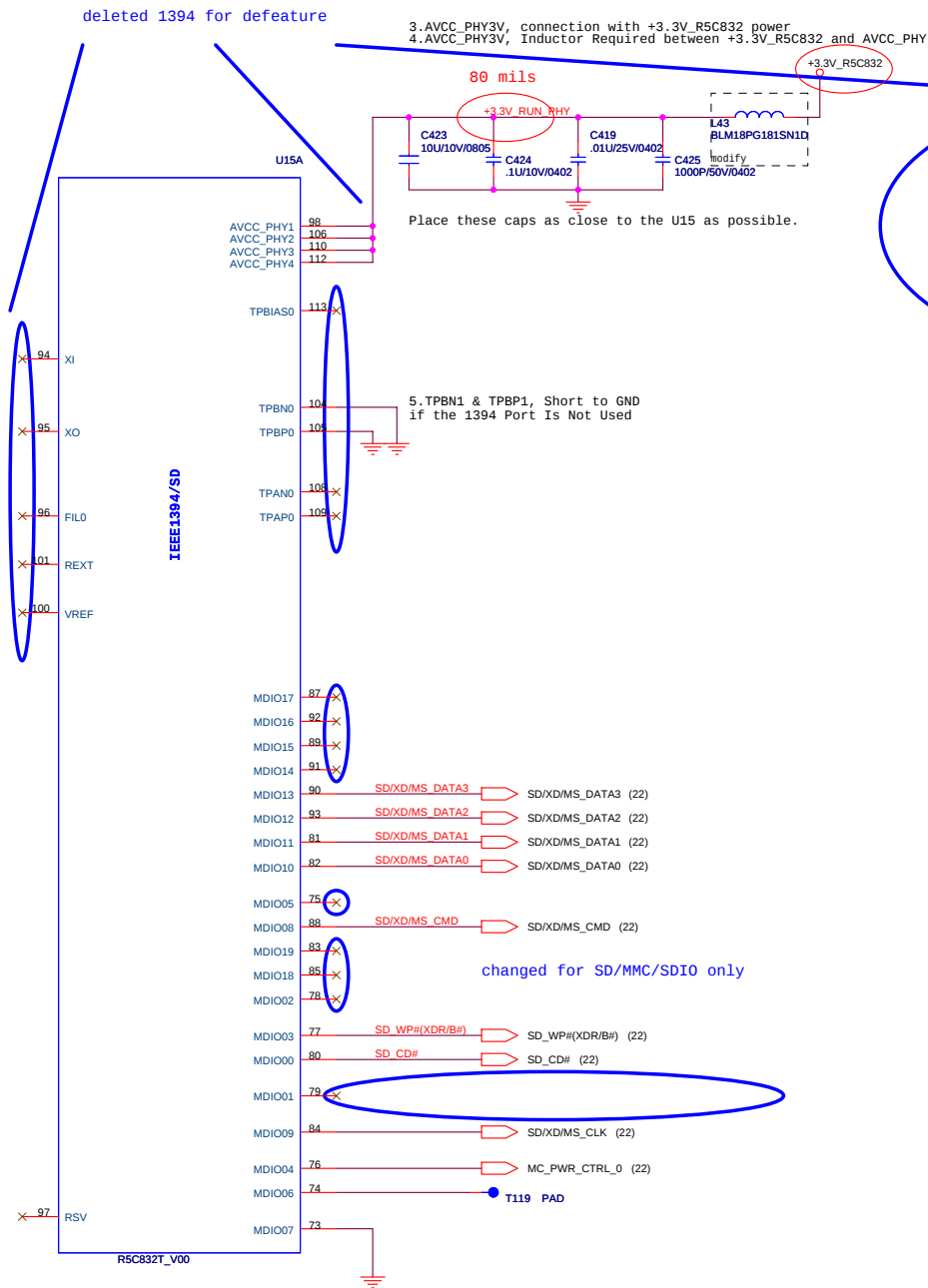
Place All of those
Inductors Caps close
to JVGA1 <200 mils



Place D4, D5, D6 close
to JVGA1 <200 mils

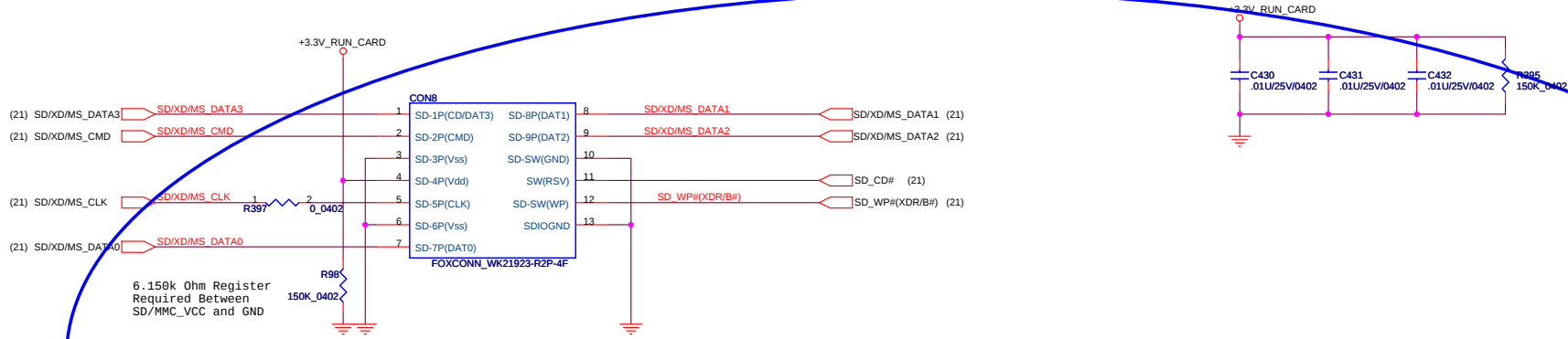
delete Svideo for defeature



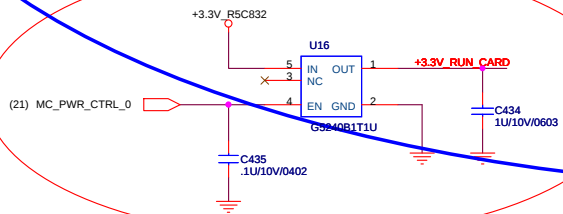


DO NOT INSERT SD/MMC SIMULTANEOUSLY.

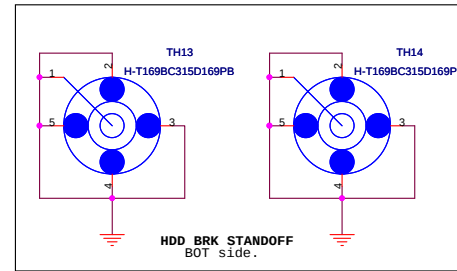
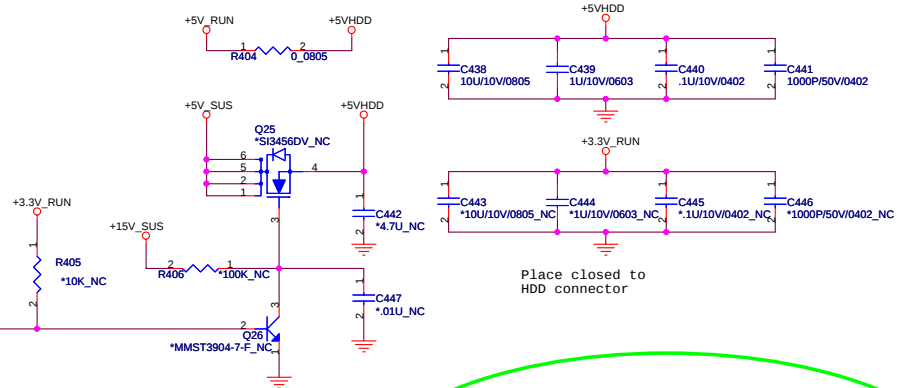
changed for SD/MMC/SDIO only



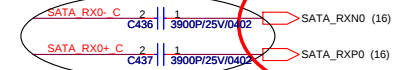
For SD/MS power



SATA HDD



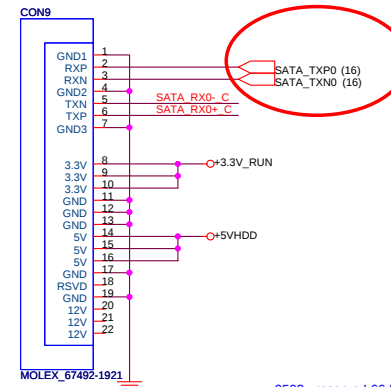
Place close to
connector side



Locate caps C558, C559 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.

SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

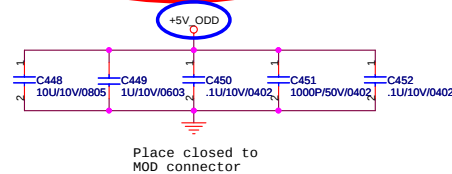
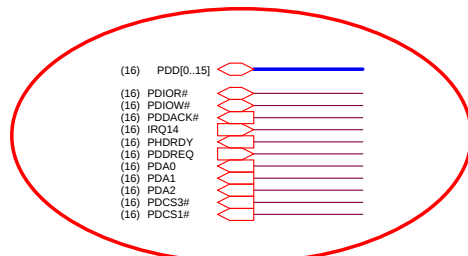
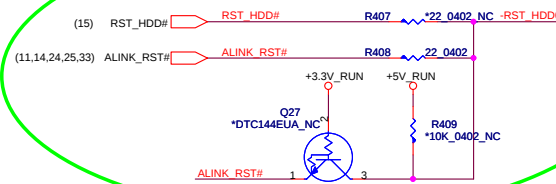


change name for ED5

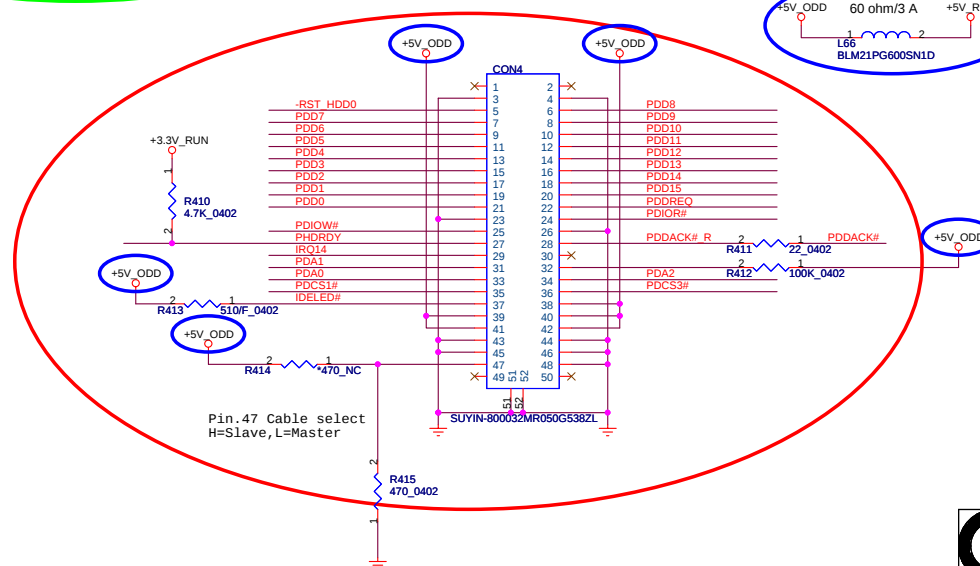
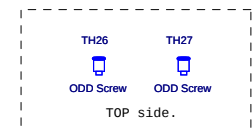
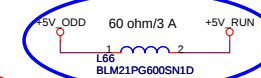
copy ED5 to FX2

Waiting to check

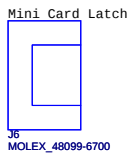
PATA ODD



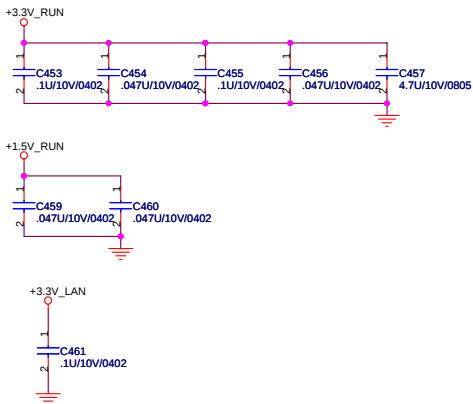
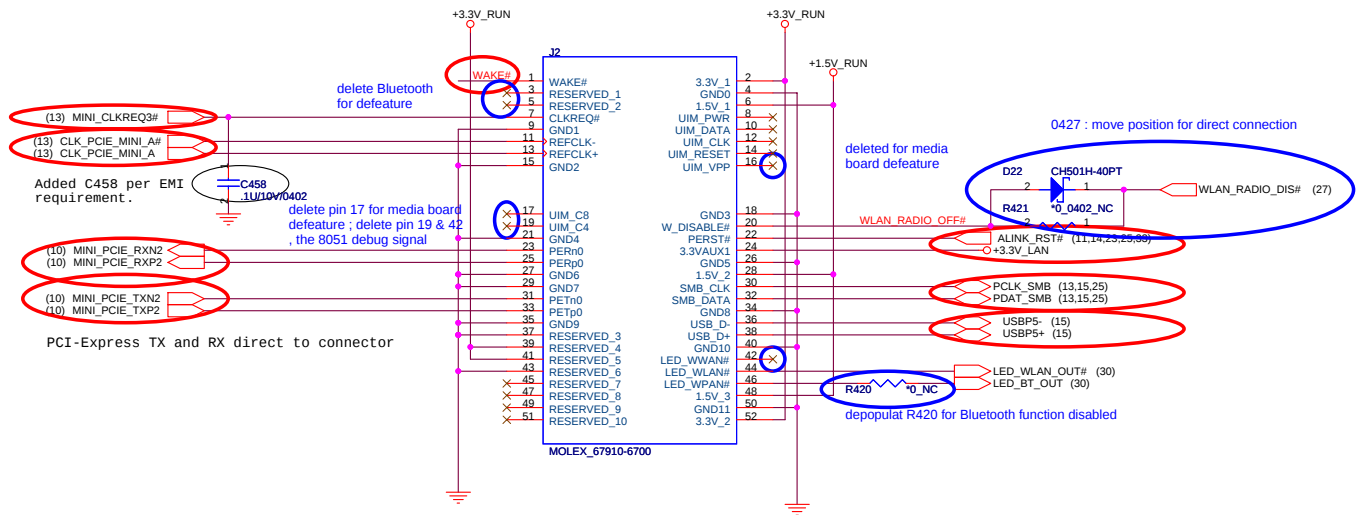
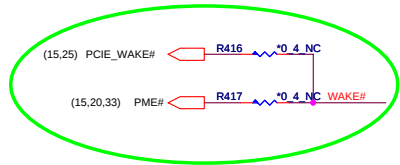
0502 : reserve L66 for current measurement , can be removed and short directly after RTS ; and change +5V_RUN to +5V_ODD for ODD side power



MINI CARD



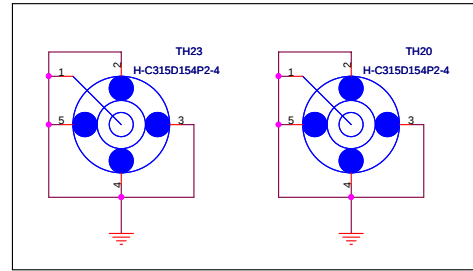
- change name for ED5
- copy ED5 to FX2
- Waiting to check



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Title			Mini Card
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Express Card



- change name for ED5
- copy ED5 to FX2
- Waiting to check

NEW CARD GUIDE POST
TOP side.

swap traces as "fx2_swap-0412"

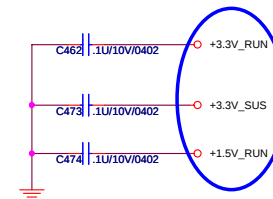
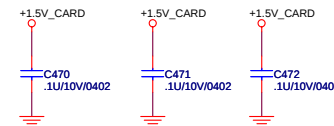
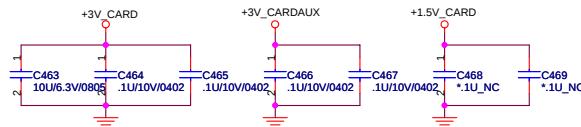
as ED5 application

reserve for pull up

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

0427 : change from only net
name to symbol "power point"

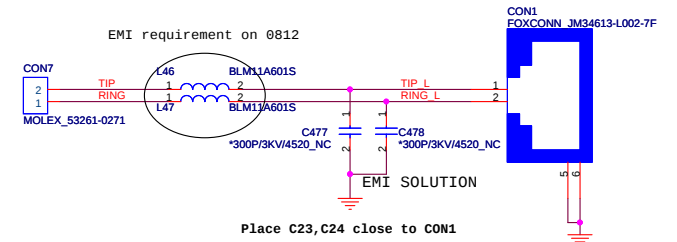
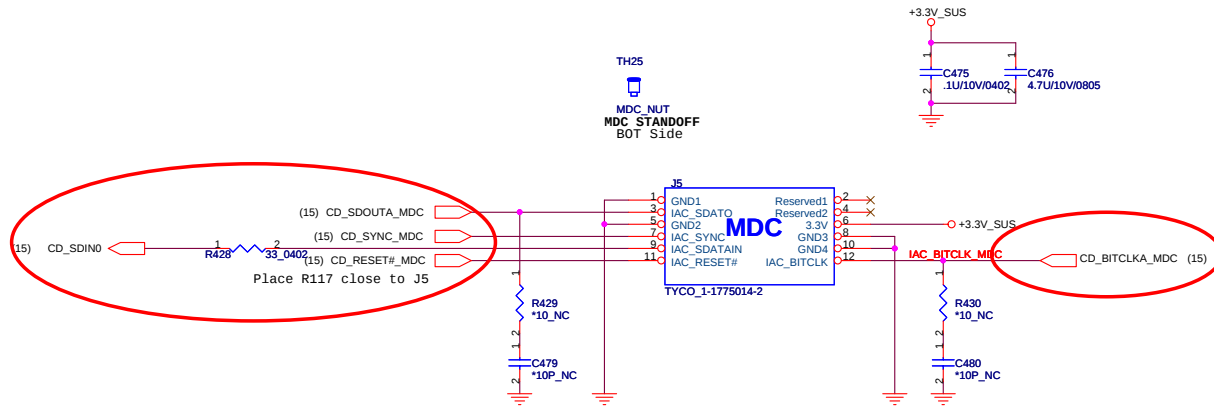


MDC INTERFACE

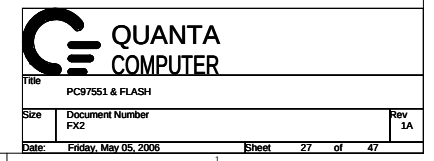
MDC Layout Notes

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG (stranded or twisted pair wire)

- change name for ED5
- copy ED5 to FX2
- Waiting to check

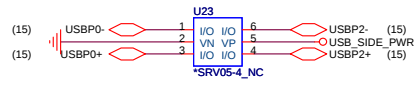


delete Bluetooth
for defeature

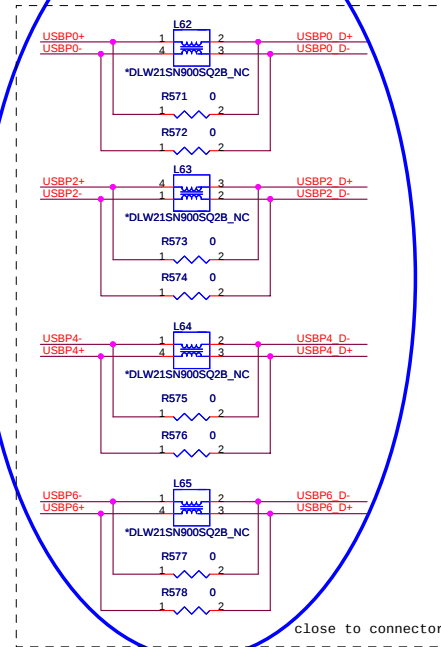
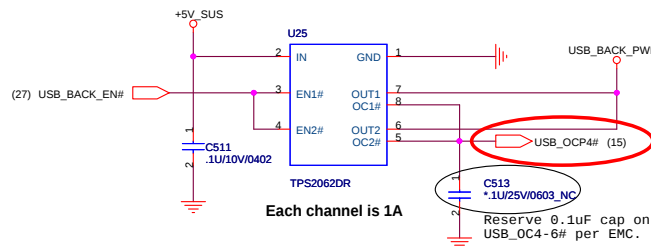
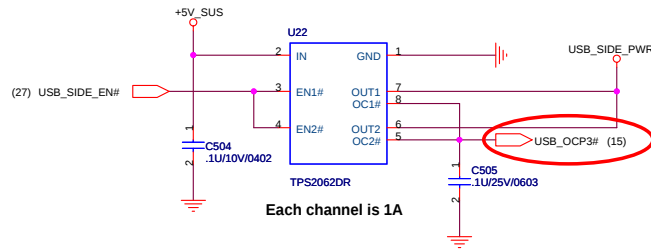
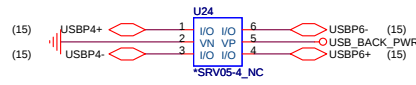


8Mbit (1M Byte), SPI

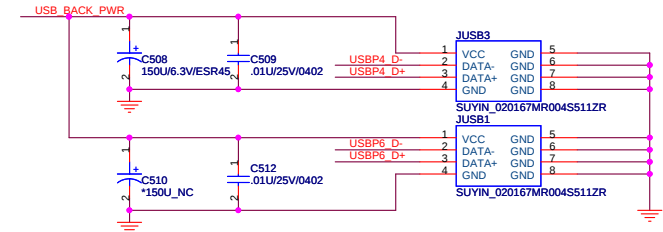
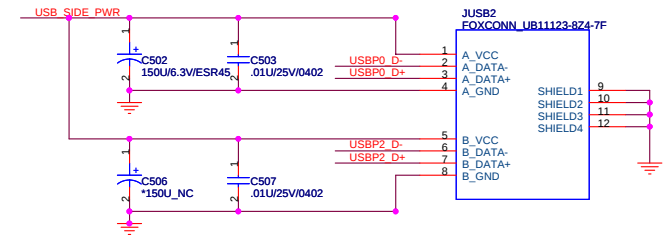
- change name for ED5
- copy ED5 to FX2
- Waiting to check

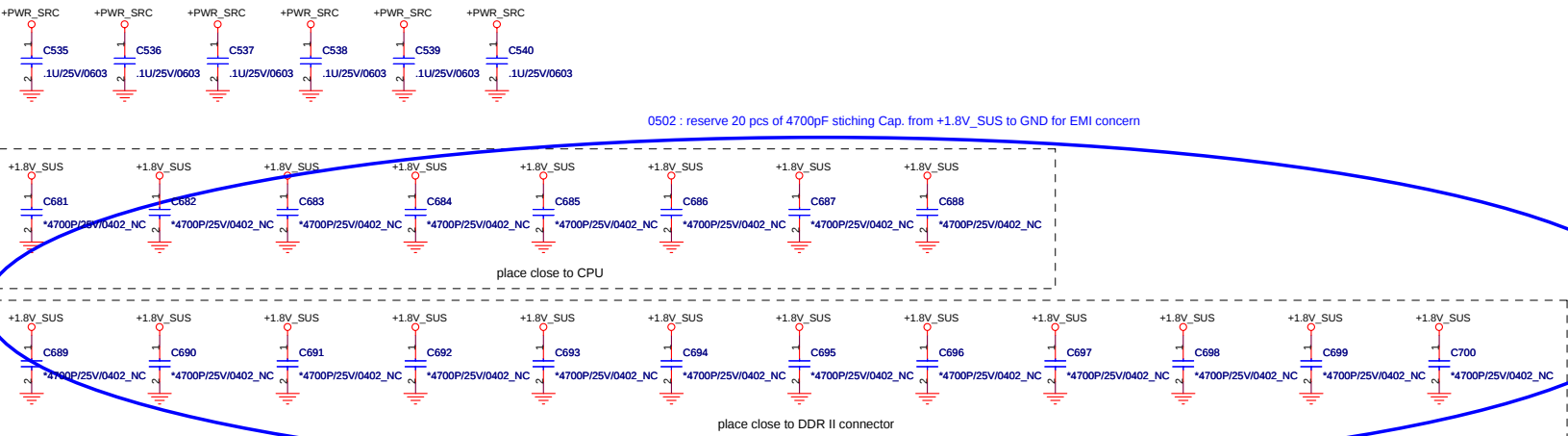
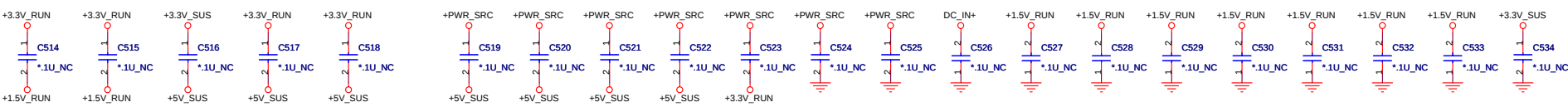
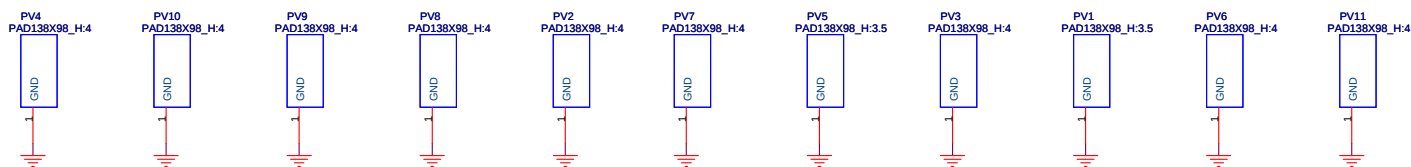
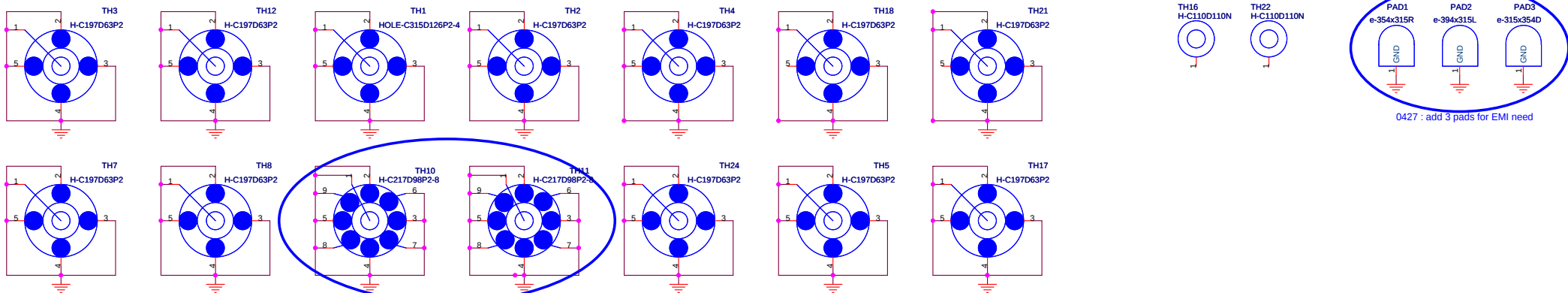


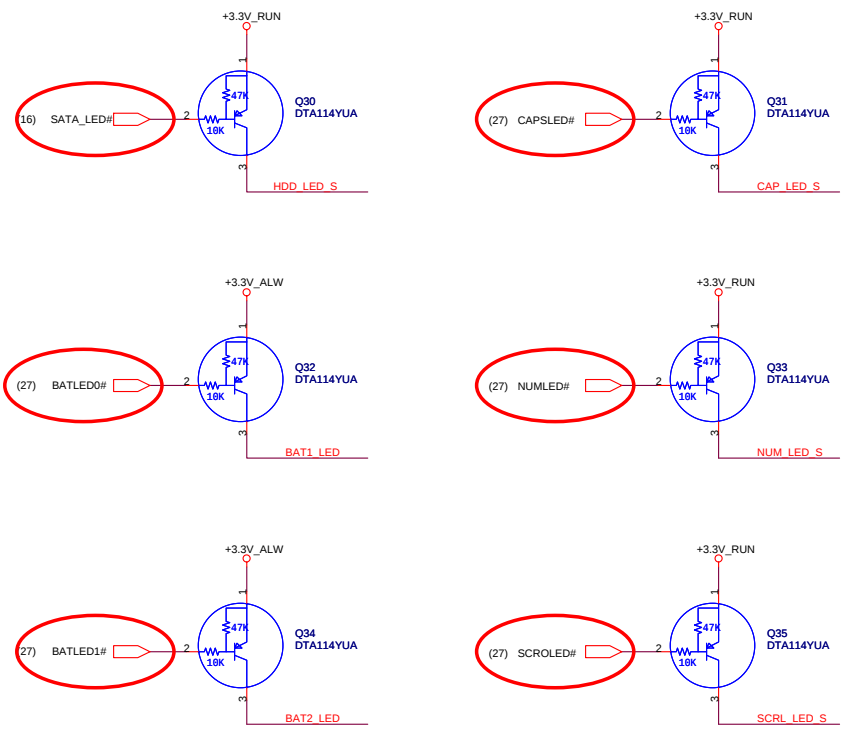
Place ESD diodes as close as USB connector.



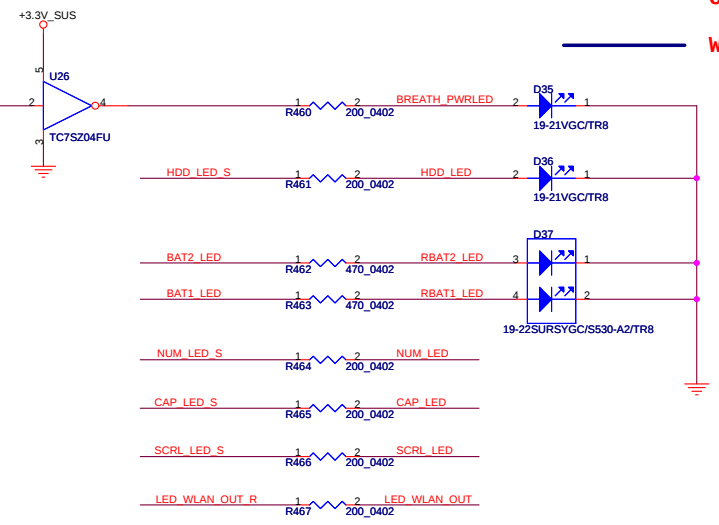
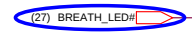
add for EMI suggestion ,
0502 : swap P0/P2 traces as "fx2-swap-0502"



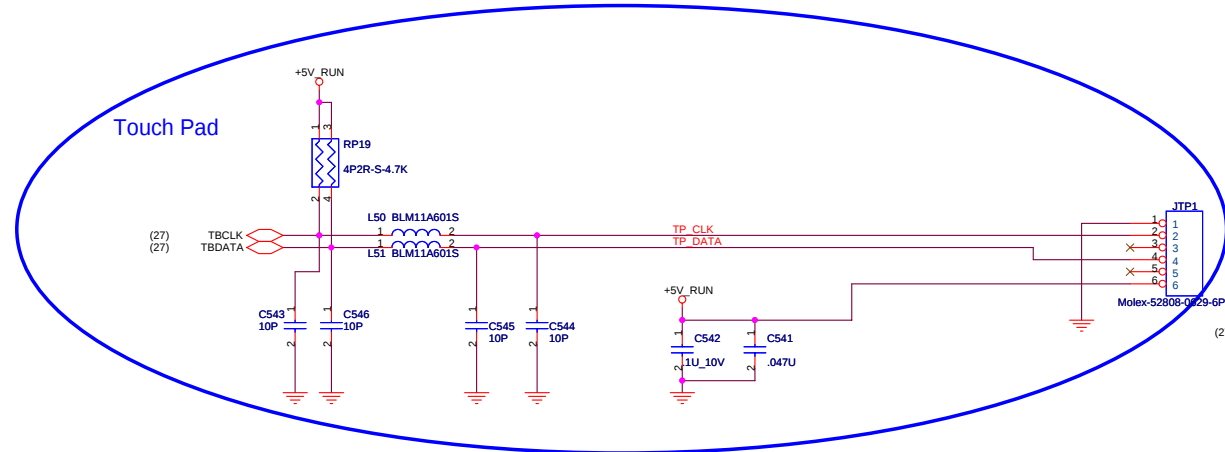




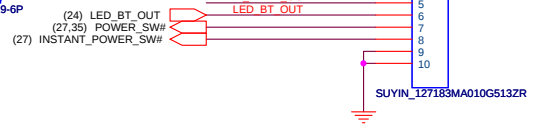
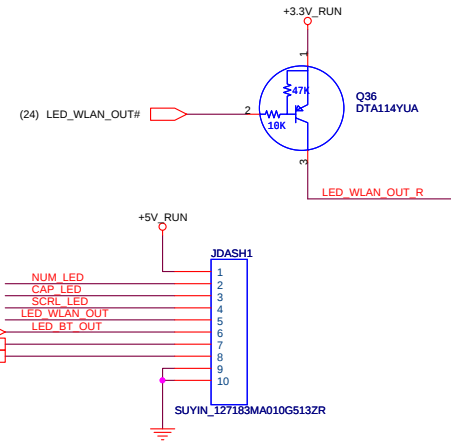
0427 : change from
BREATH_LED to BREATH_LED#

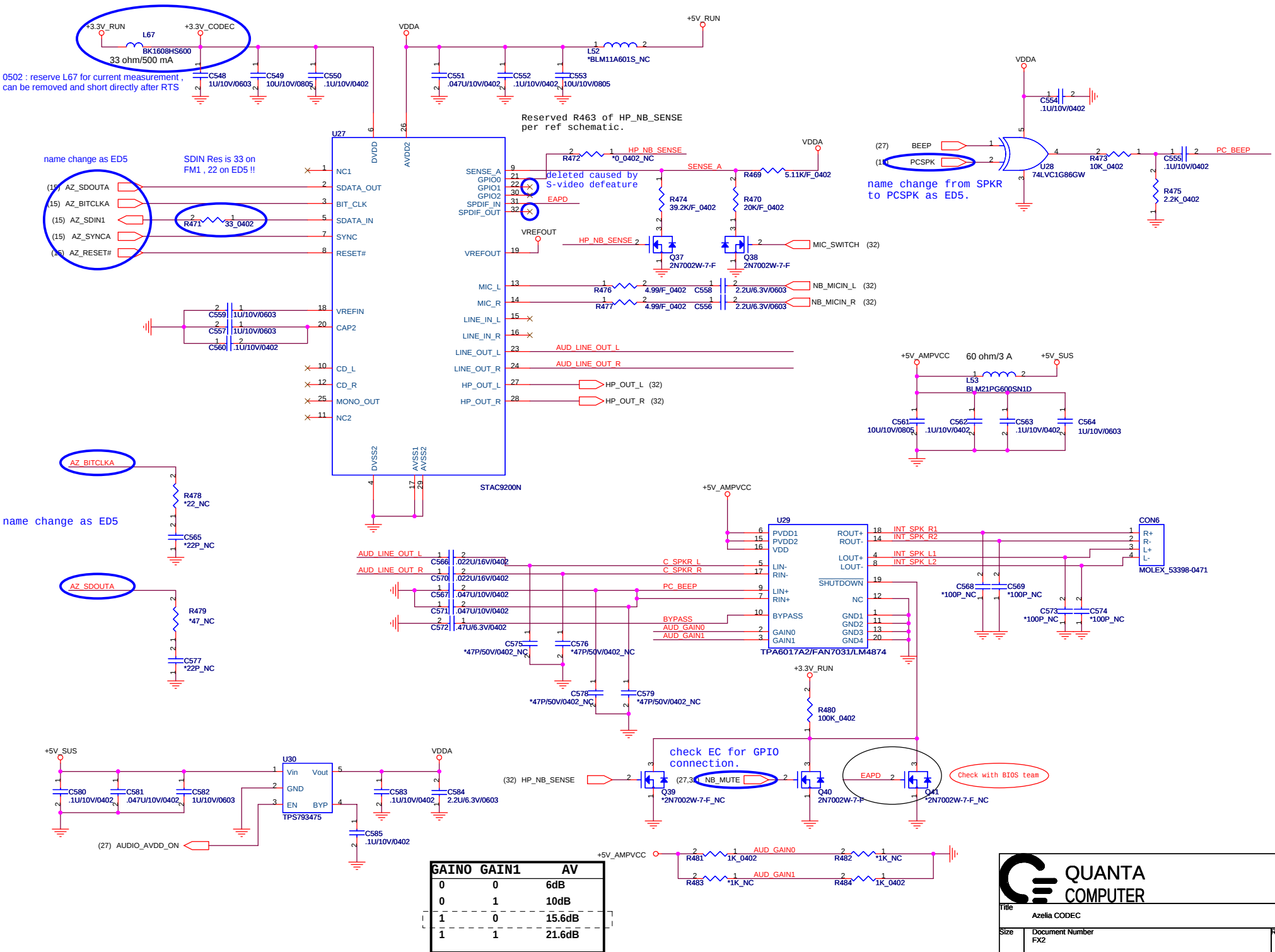


— change name for ED5
 — copy ED5 to FX2
 — Waiting to check



FM1 media board changed to TP only as DM5





0502 : reserve L67 for current measurement , can be removed and short directly after RTS

name change as ED5

name change as ED5

check EC for GPIO connection.

name change from SPKR to PCSPK as ED5.

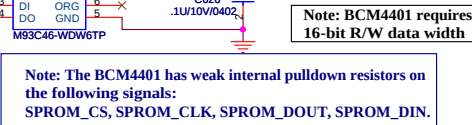
GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



Place C607 close to pin65

EMI requirement on 0812

change name for ED5
copy ED5 to FX2
Waiting to check

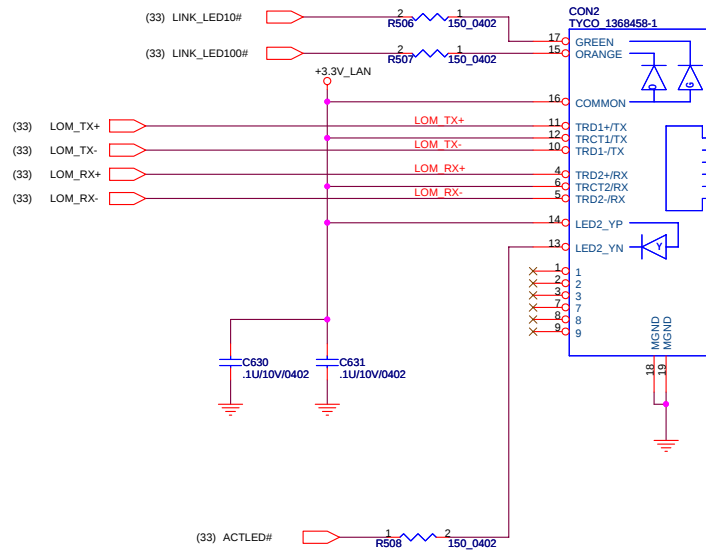


Note: The BCM4401 has weak internal pulldown resistors on the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.

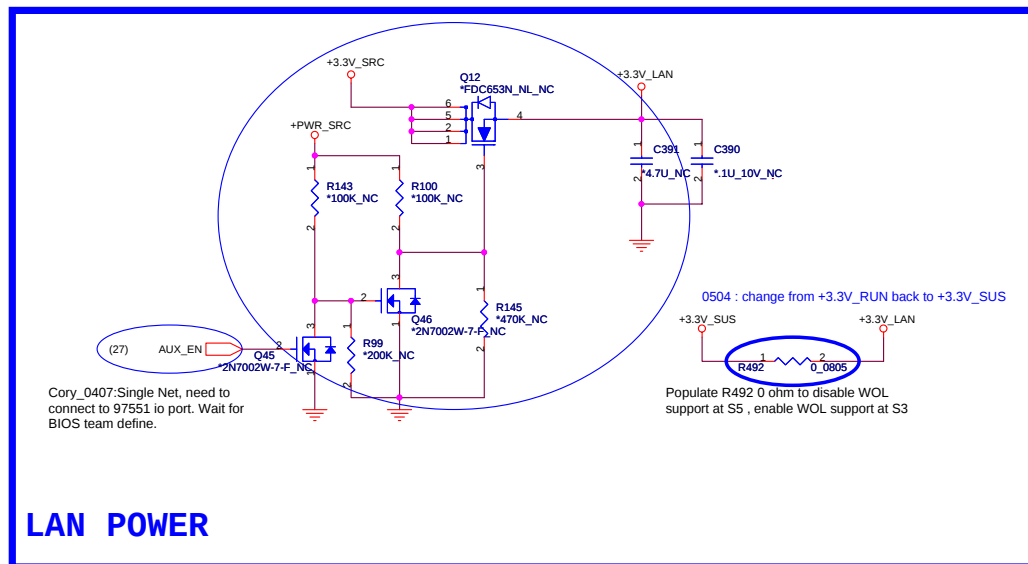
Note: BCM4401 requires 16-bit B/W data width.

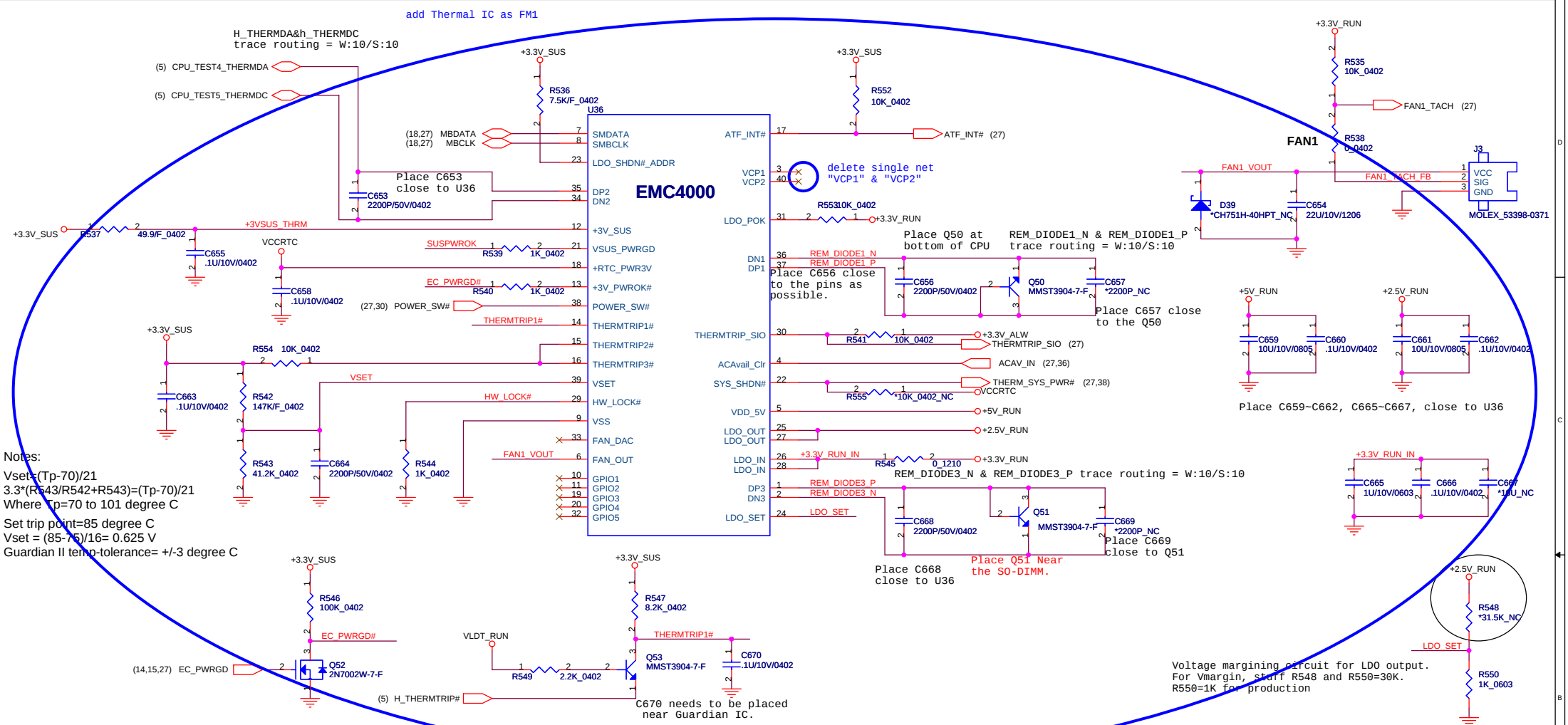


Title			
LAN(BCM4401)			
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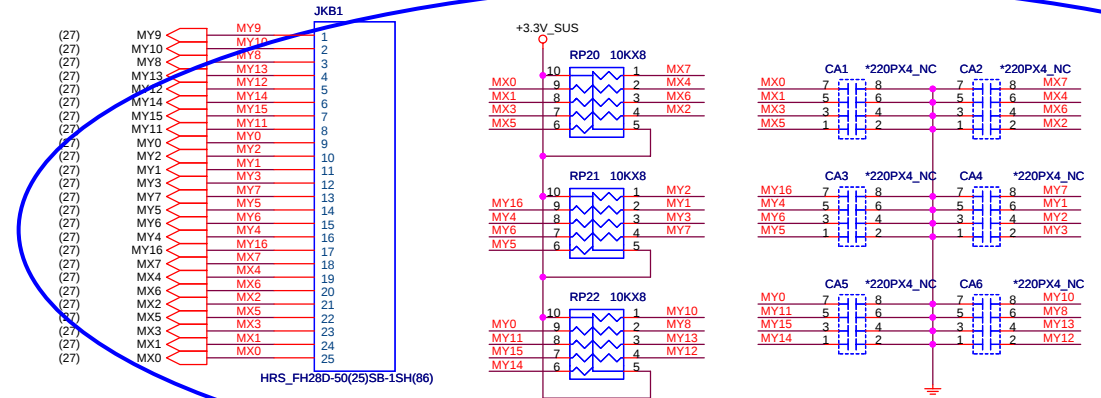
- change name for ED5
- copy ED5 to FX2
- Waiting to check
- copy DM5 to FX2





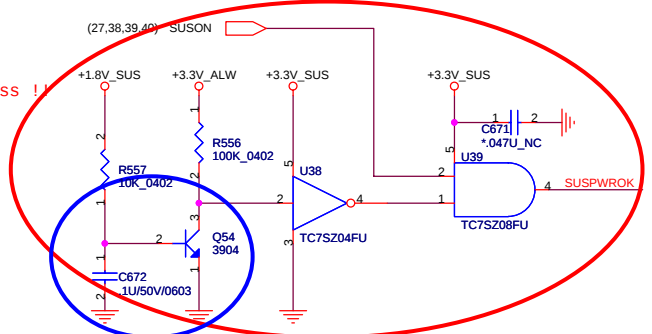
Notes:
Vset=(Tp-70)/21
3.3*(R543/R542+R543)=(Tp-70)/21
Where Tp=70 to 101 degree C
Set trip point=85 degree C
Vset = (85-76)/16= 0.625 V
Guardian II temp-tolerance= +/-3 degree C

as FM1 keyboard matrix & "e0788.1104a_swap-0422"



KBC

wait to discuss !!



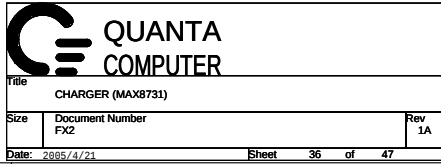
0427 : change Q54 from 2N7002W-7-F to 3904 ; C672 from .1U/10V/0402 to .1U/50V/0603 as voltage level & timing concern

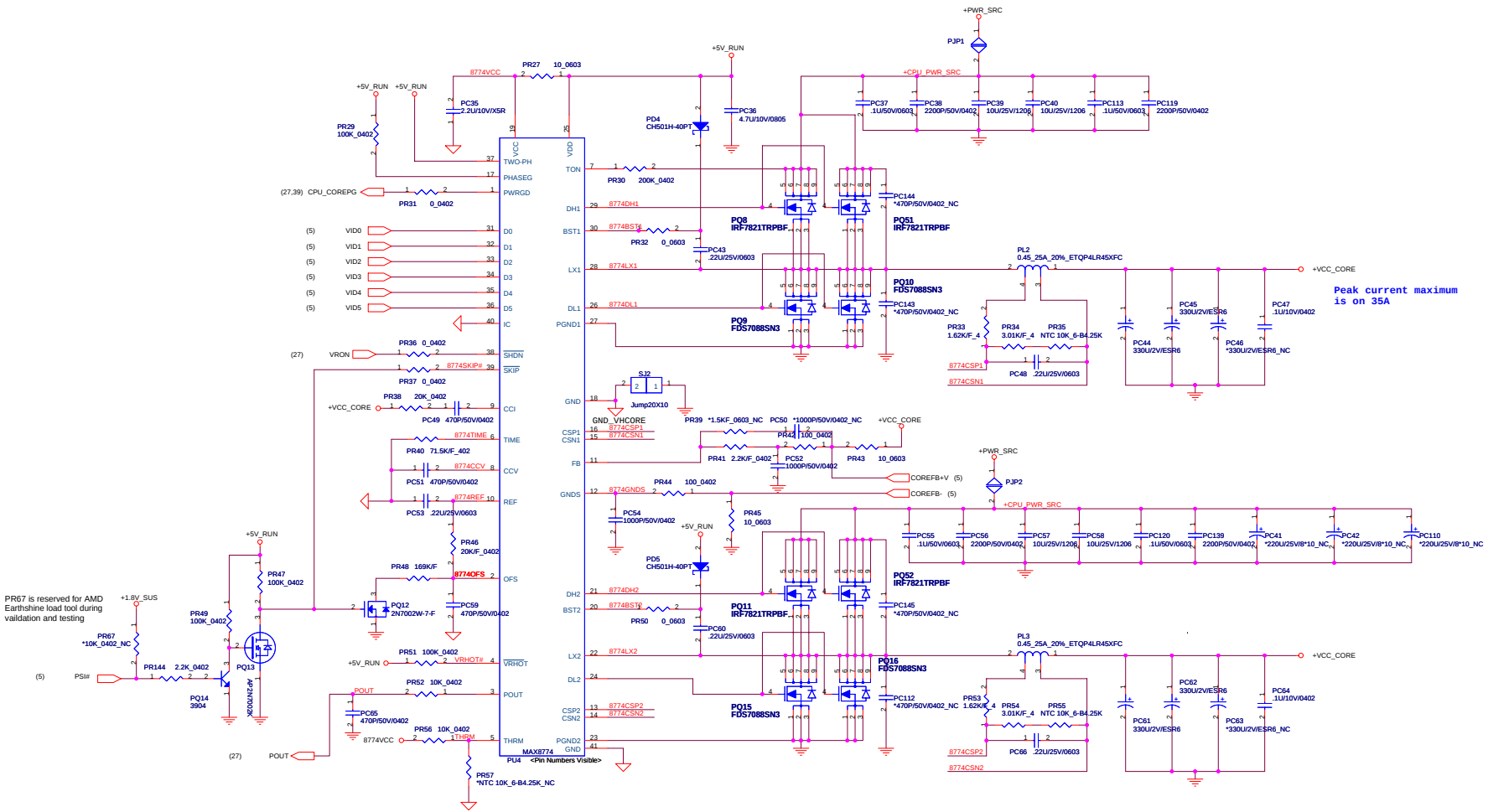


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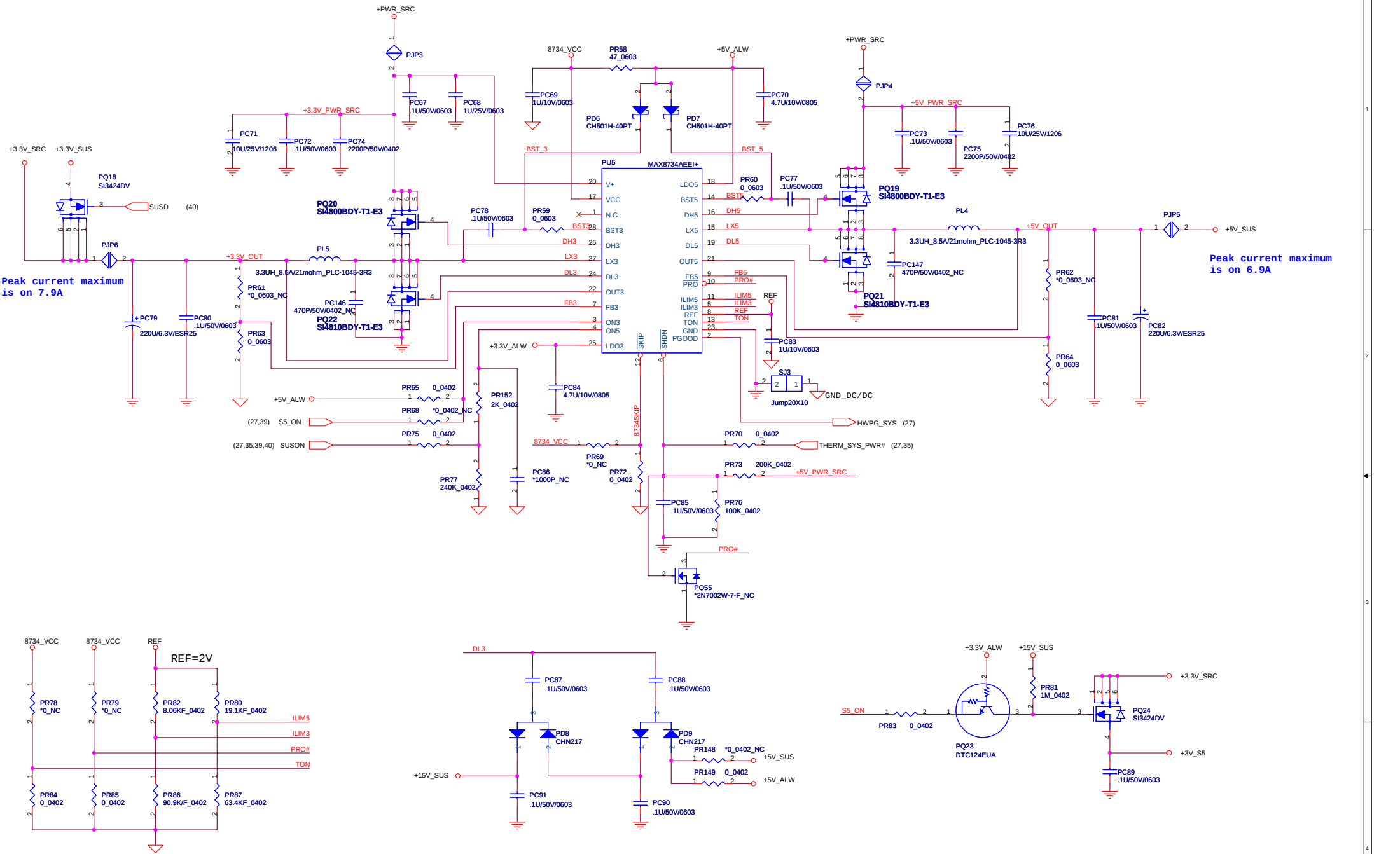
Title		
KB & THERMAL & FAN		
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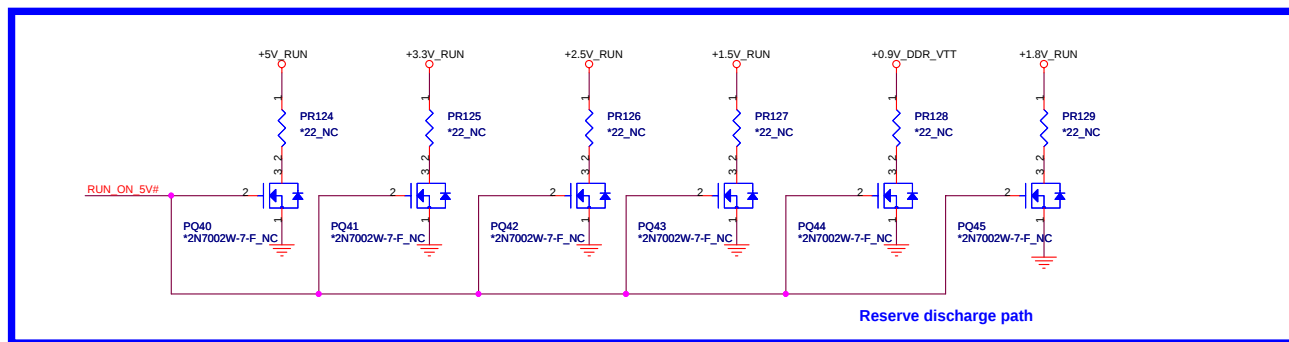
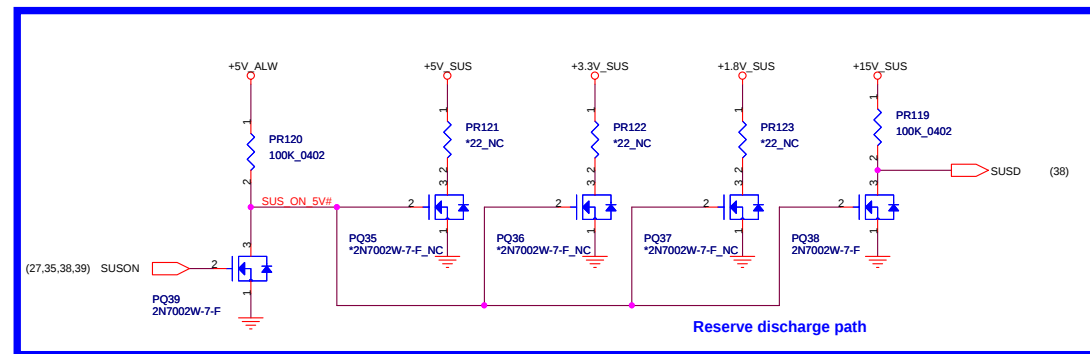
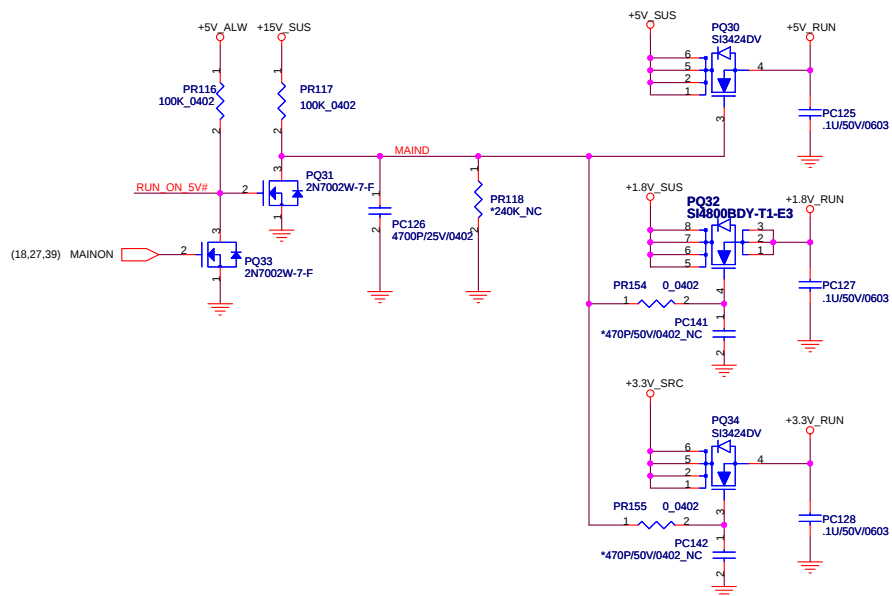


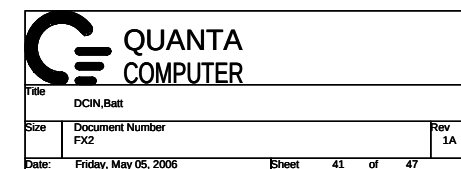


D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V
0	0	0	0	0	1	1.5250V
0	0	0	0	1	0	1.5000V
0	0	0	0	1	1	1.4750V
0	0	0	1	0	0	1.4500V
0	0	0	1	0	1	1.4250V
0	0	0	1	1	0	1.4000V
0	0	1	0	0	0	1.3750V
0	0	1	0	0	1	1.3500V
0	0	1	0	1	0	1.3250V
0	0	1	0	1	1	1.3000V
0	0	1	1	0	0	1.2750V
0	0	1	1	0	1	1.2500V
0	0	1	1	1	0	1.2250V
0	0	1	1	1	1	1.2000V
0	1	0	0	0	0	1.1750V
0	1	0	0	0	1	1.1500V
0	1	0	0	1	0	1.1250V
0	1	0	0	1	1	1.1000V
0	1	0	1	0	0	1.0750V
0	1	0	1	0	1	1.0500V
0	1	0	1	1	0	1.0250V
0	1	0	1	1	1	1.0000V
0	1	1	0	0	0	0.9750V
0	1	1	0	0	1	0.9500V
0	1	1	0	1	0	0.9250V
0	1	1	0	1	1	0.9000V
0	1	1	1	0	0	0.8750V
0	1	1	1	0	1	0.8500V
0	1	1	1	1	0	0.8250V
0	1	1	1	1	1	0.8000V
0	1	1	1	1	1	0.7750V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	0.7500V
1	0	0	0	0	1	0.7250V
1	0	0	0	1	0	0.7000V
1	0	0	0	1	1	0.6750V
1	0	0	1	0	0	0.6500V
1	0	0	1	0	1	0.6250V
1	0	0	1	1	0	0.6000V
1	0	0	1	1	1	0.5750V
1	0	1	0	0	0	0.5500V
1	0	1	0	0	1	0.5250V
1	0	1	0	1	0	0.5000V
1	0	1	0	1	1	0.4750V
1	0	1	1	0	0	0.4500V
1	0	1	1	0	1	0.4250V
1	0	1	1	1	0	0.4000V
1	0	1	1	1	1	0.3750V

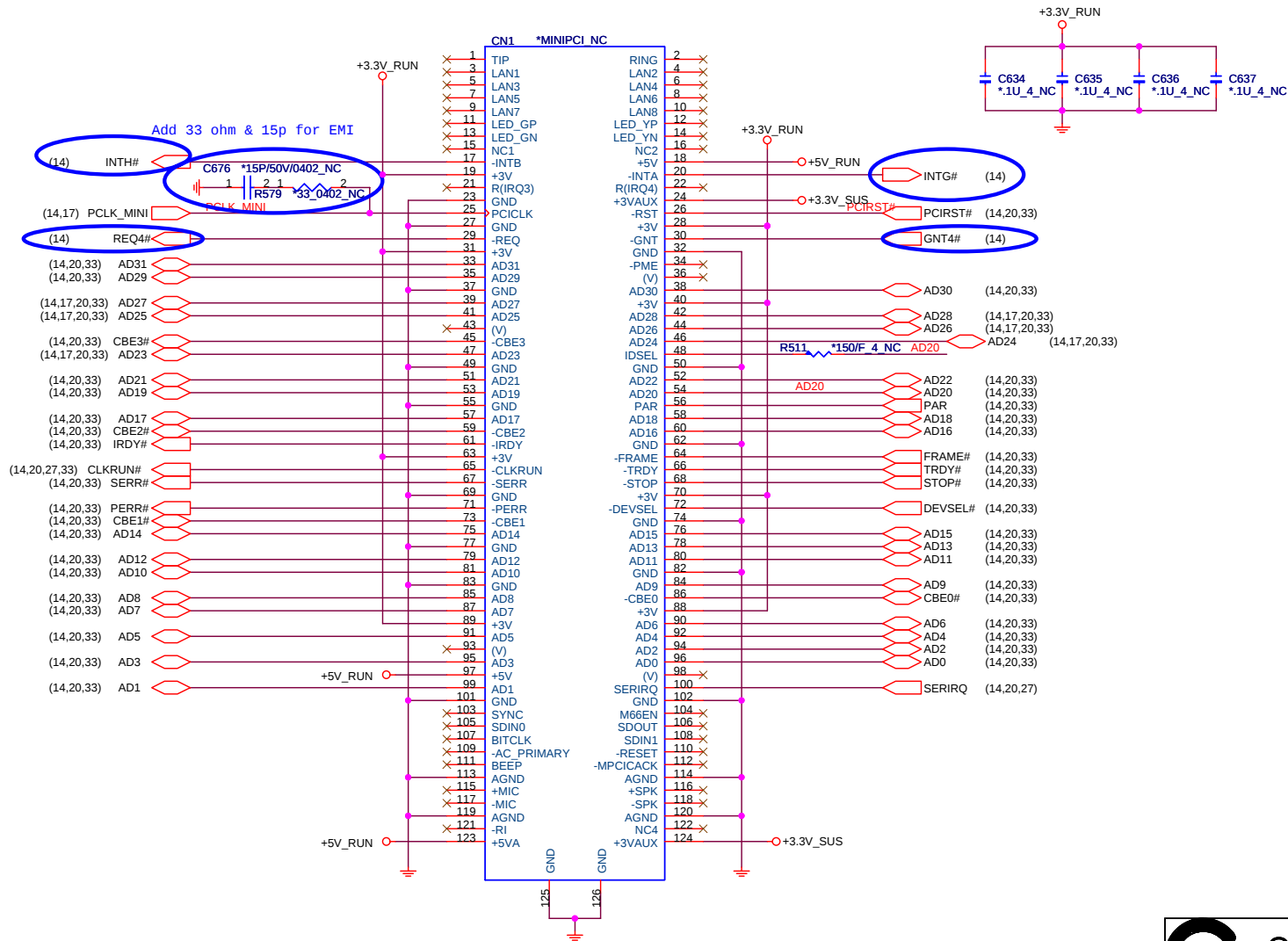






ID Select : AD20
Interrupt Pin : INTG# , INTH#
Request Indicate : REQ4#
Grant Indicate : GNT4#

DEBUG PURPOSE ONLY



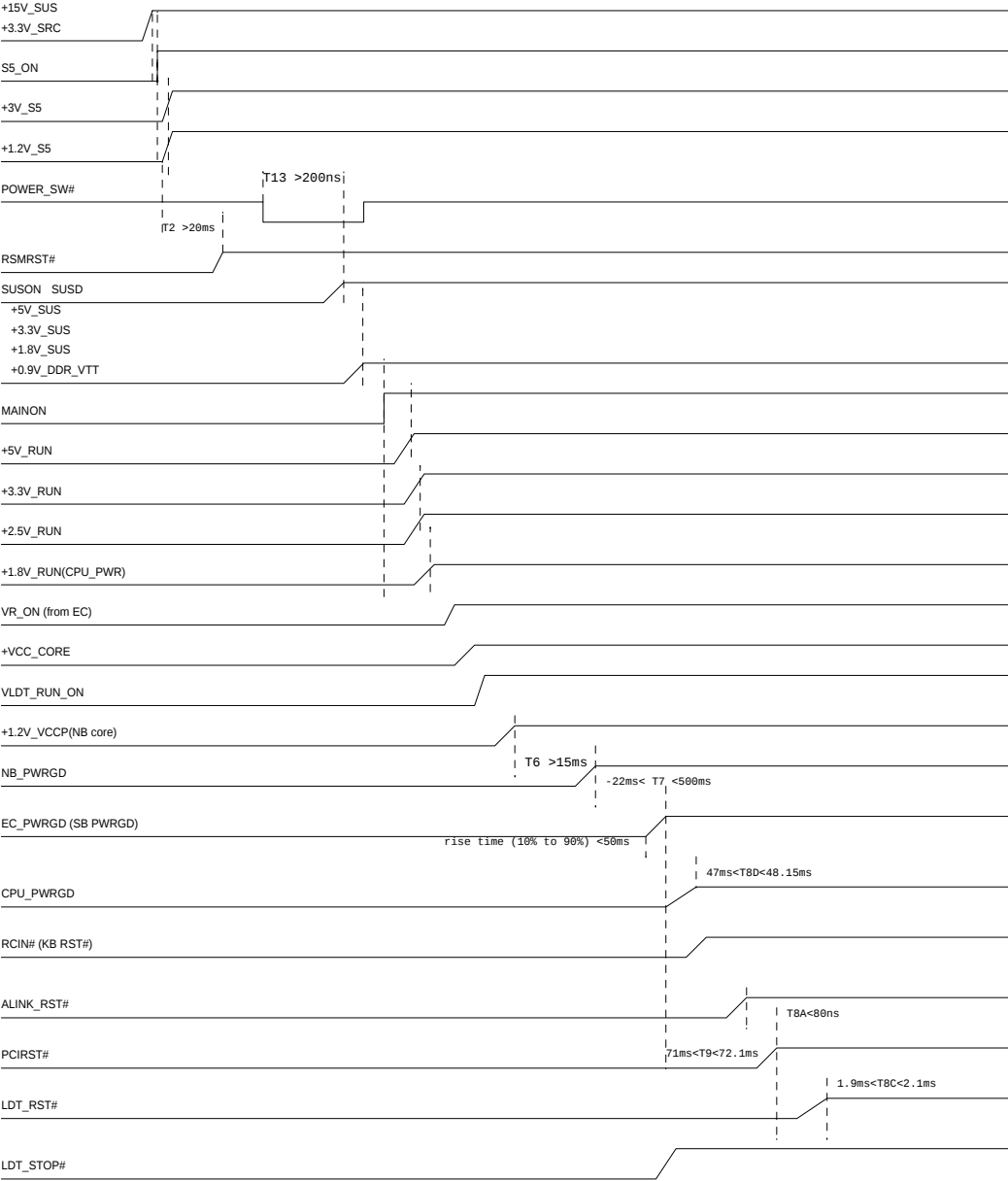
MPC



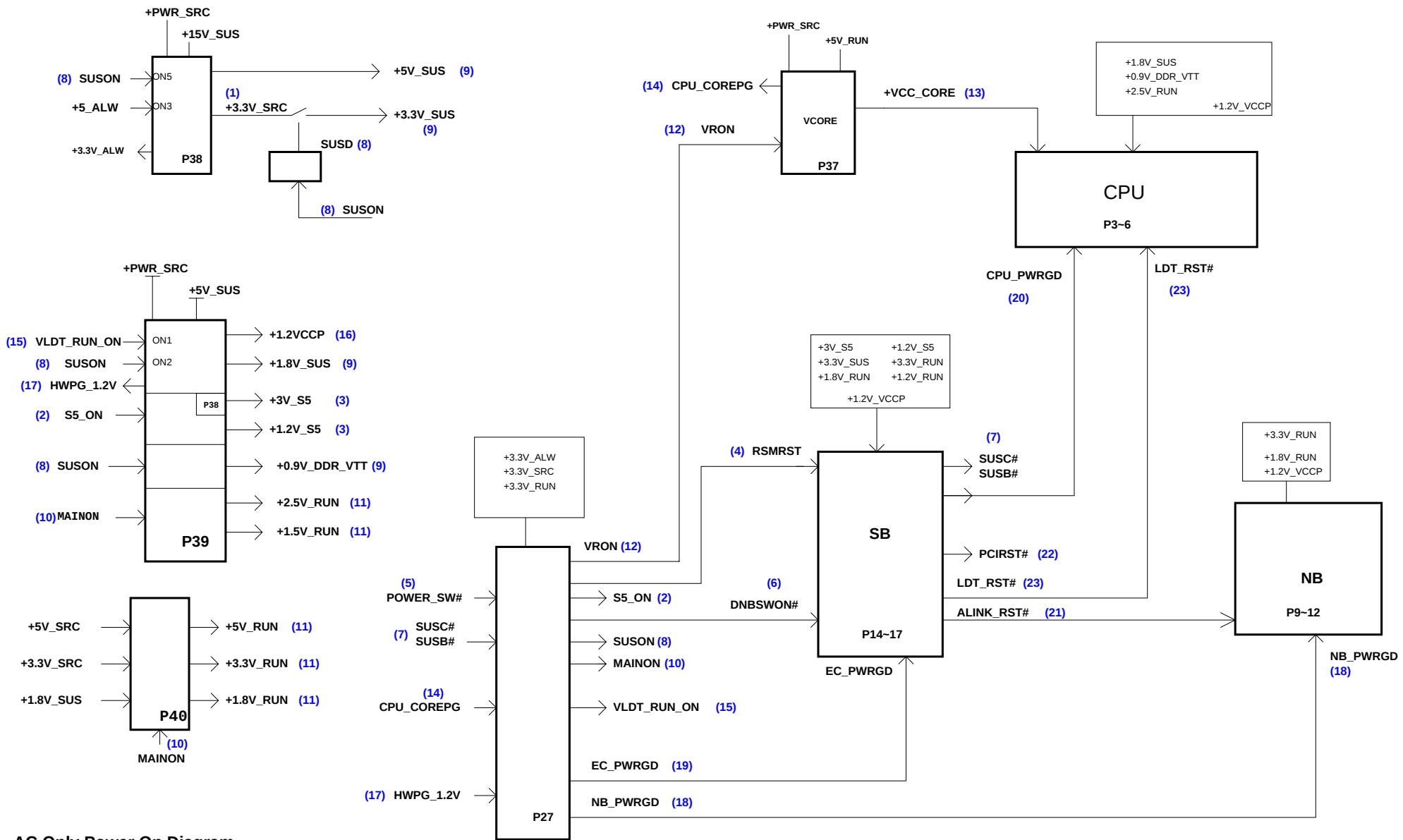
QUANTA
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Title MINI PCI(for debug)		
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Power On Sequence



T6: NB core voltage to NB_PWRGD
T7: NB_PWRGD to SB_PWRGD
T8D: SB_PWRGD to CPU_PWRGD
T8A: ALINK_RST# to PCIRST#
T9: SB_PWRGD to PCIRST#
T8C: PCIRST# to LDT_RST#



AC Only Power On Diagram

- | | | | |
|----------------------|-------------------------|------------------|-----------------|
| (1) +3.3V_SRC | (8) SUSON, SUSD | (13) +VCC_CORE | (20) CPU_PWRGD |
| (2) S5_ON | (9) +5V_SUS | (14) CPU_COREPG | (21) ALINK_RST# |
| (3) +3V_S5, +1.2V_S5 | (10) MAINON | (15) VLDT_RUN_ON | (22) PCI_RST# |
| (4) RSMRST | (11) +5V_RUN, +3.3V_RUN | (16) +1.2_VCCP | (23) LDT_RST# |
| (5) POWER_SW# | (12) VRON | (17) HWPG_1.2V | |
| (6) DNBSWON# | | (18) NB_PWRGD | |
| (7) SUSC#, SUSB# | | (19) EC_PWRGD | |

