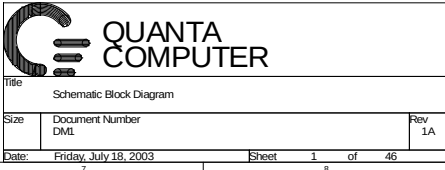


Dothan

(Micro-FCPGA)

PG 2,3





CPU_VCCA

C446 0.1uF

C93 0.1uF

C71 0.1uF

C429 0.1uF

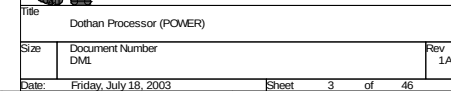
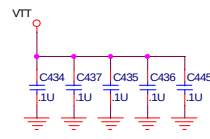
C431 10uF, 4V XSR

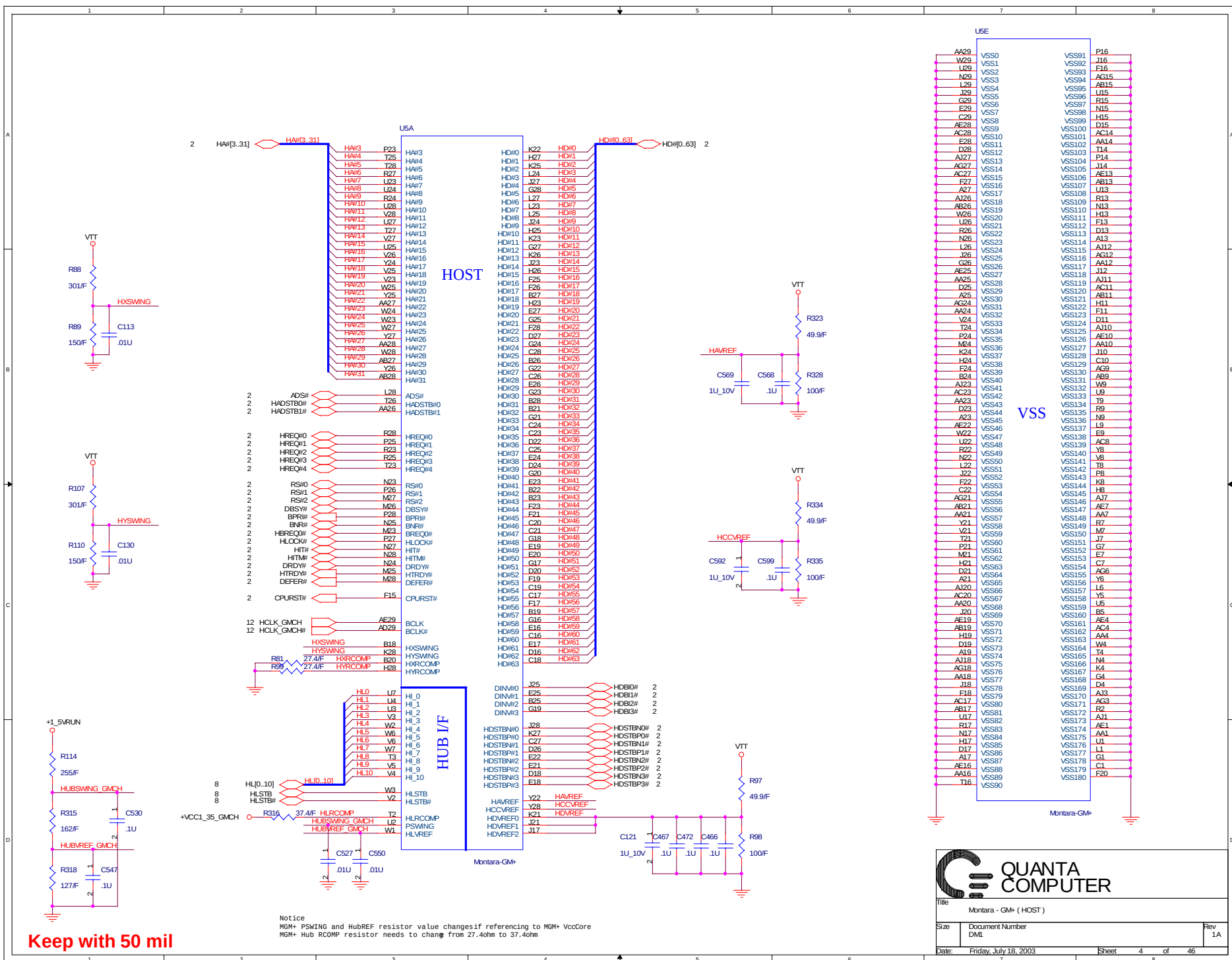
C72 10uF, 4V XSR

C91 10uF, 4V XSR

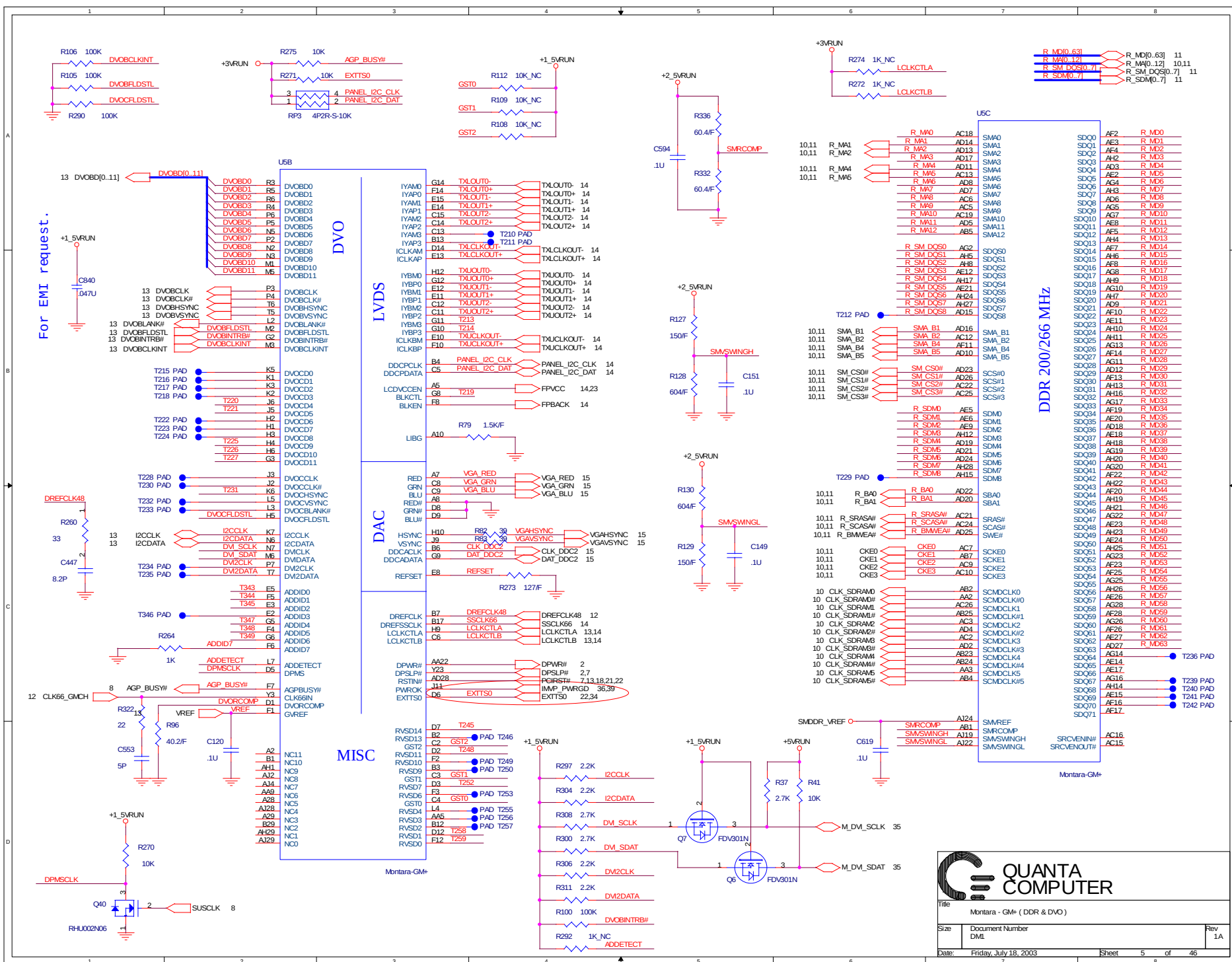
C443 10uF, 4V XSR

Ground





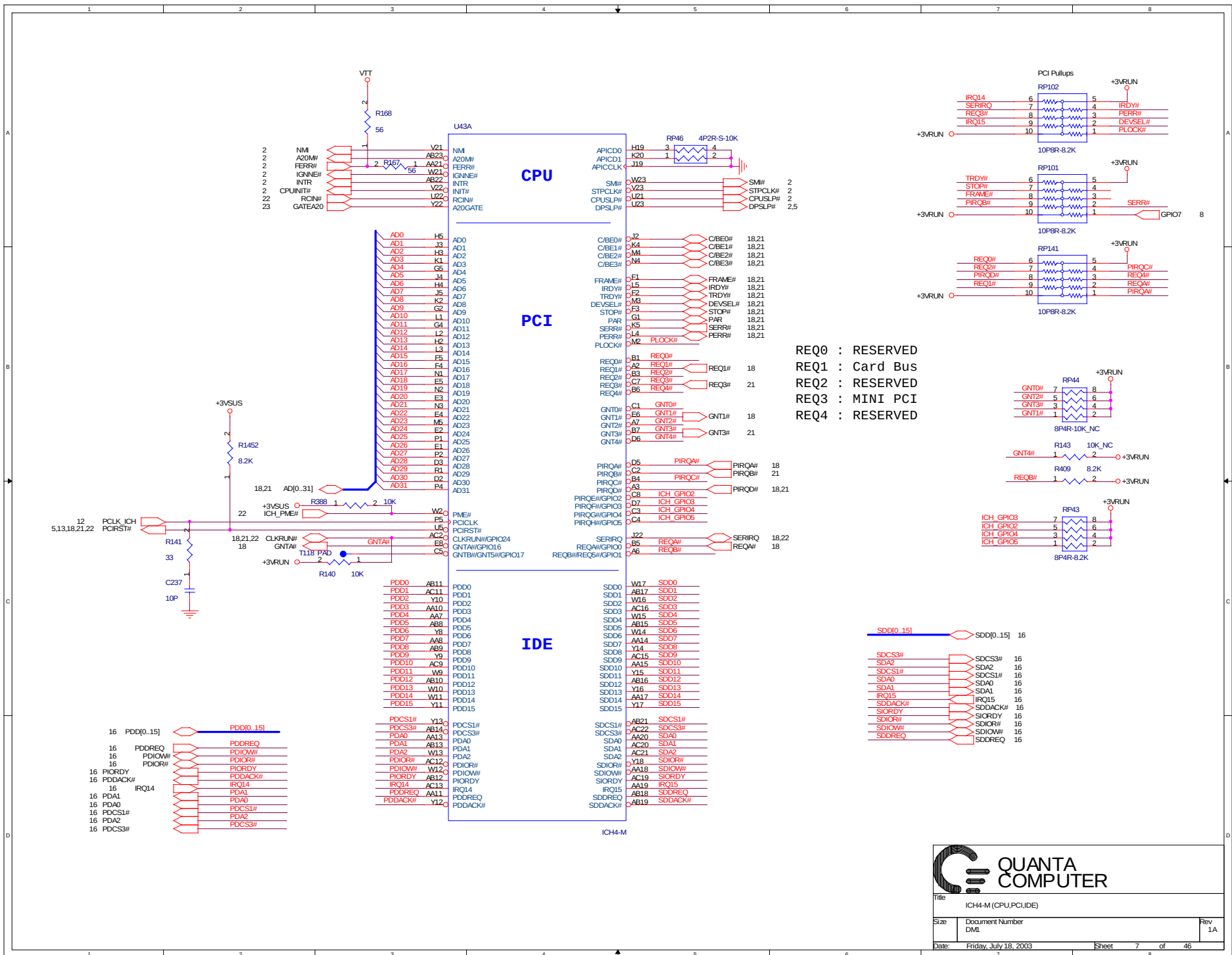
Title			Montara - GM+ (HOST)	
Size	Document Number	Rev		
	DMT	1A		
Date:	Friday, July 18, 2003	Sheet	4	of 46

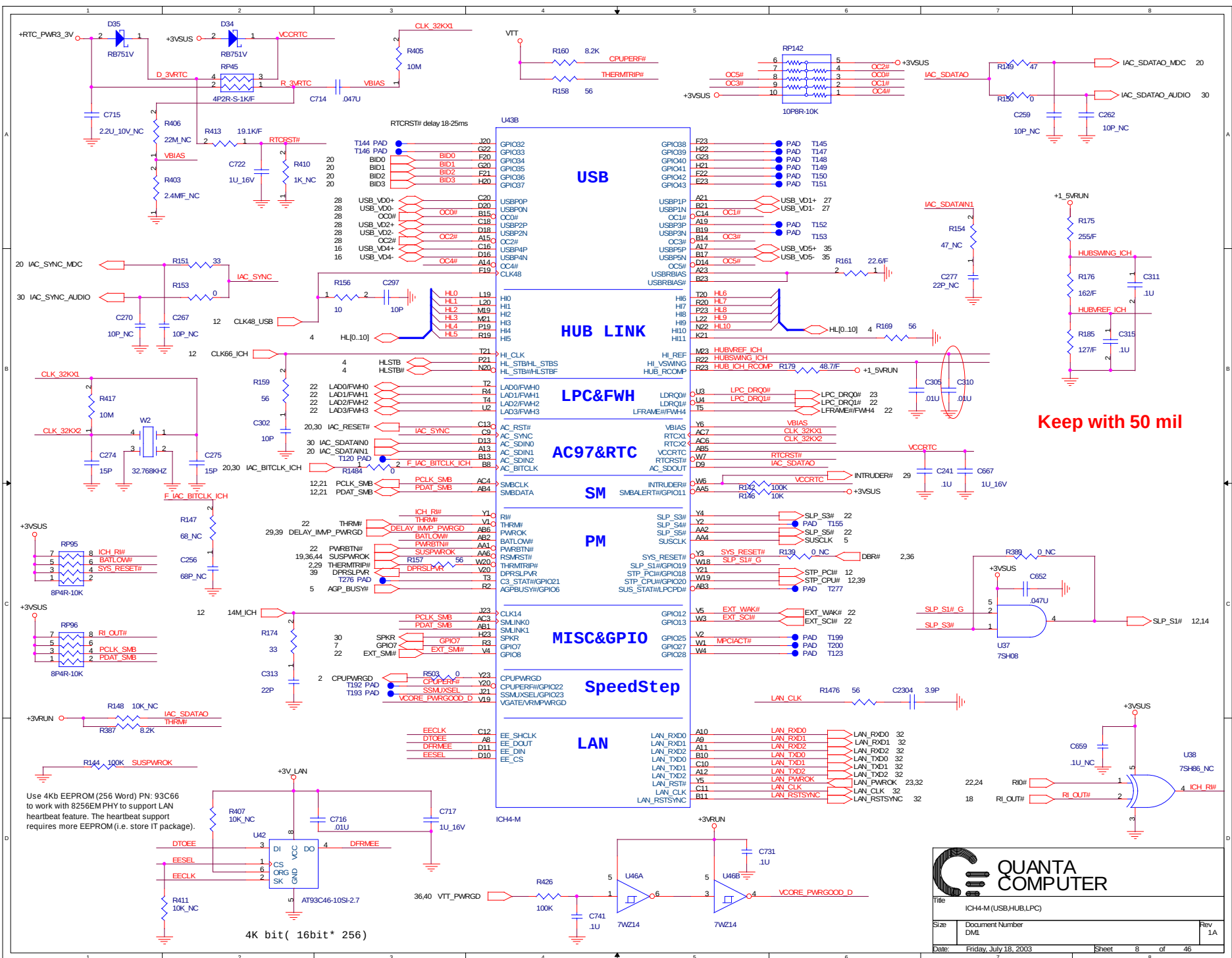


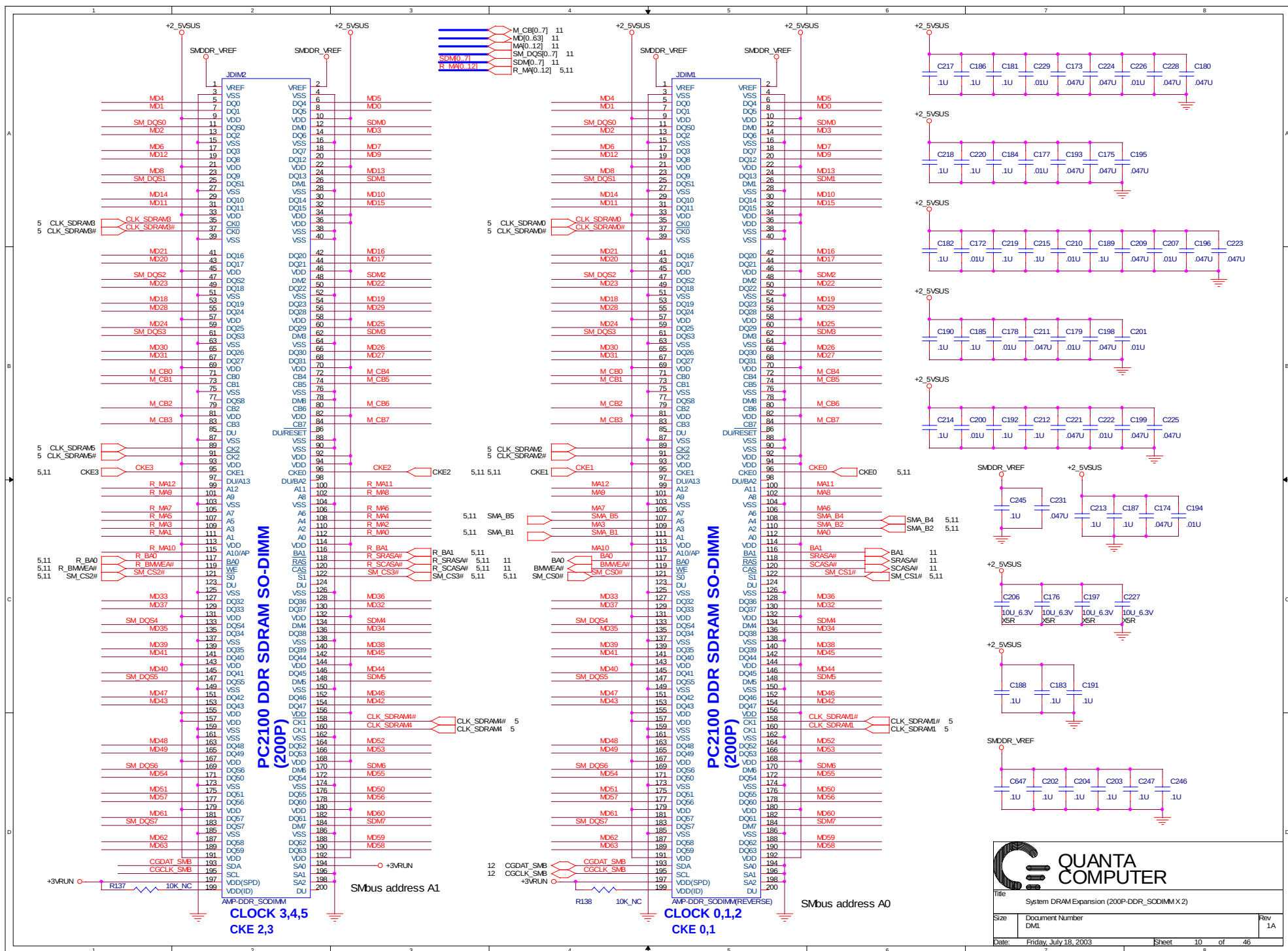
PSLB20G157M(150U_4V)

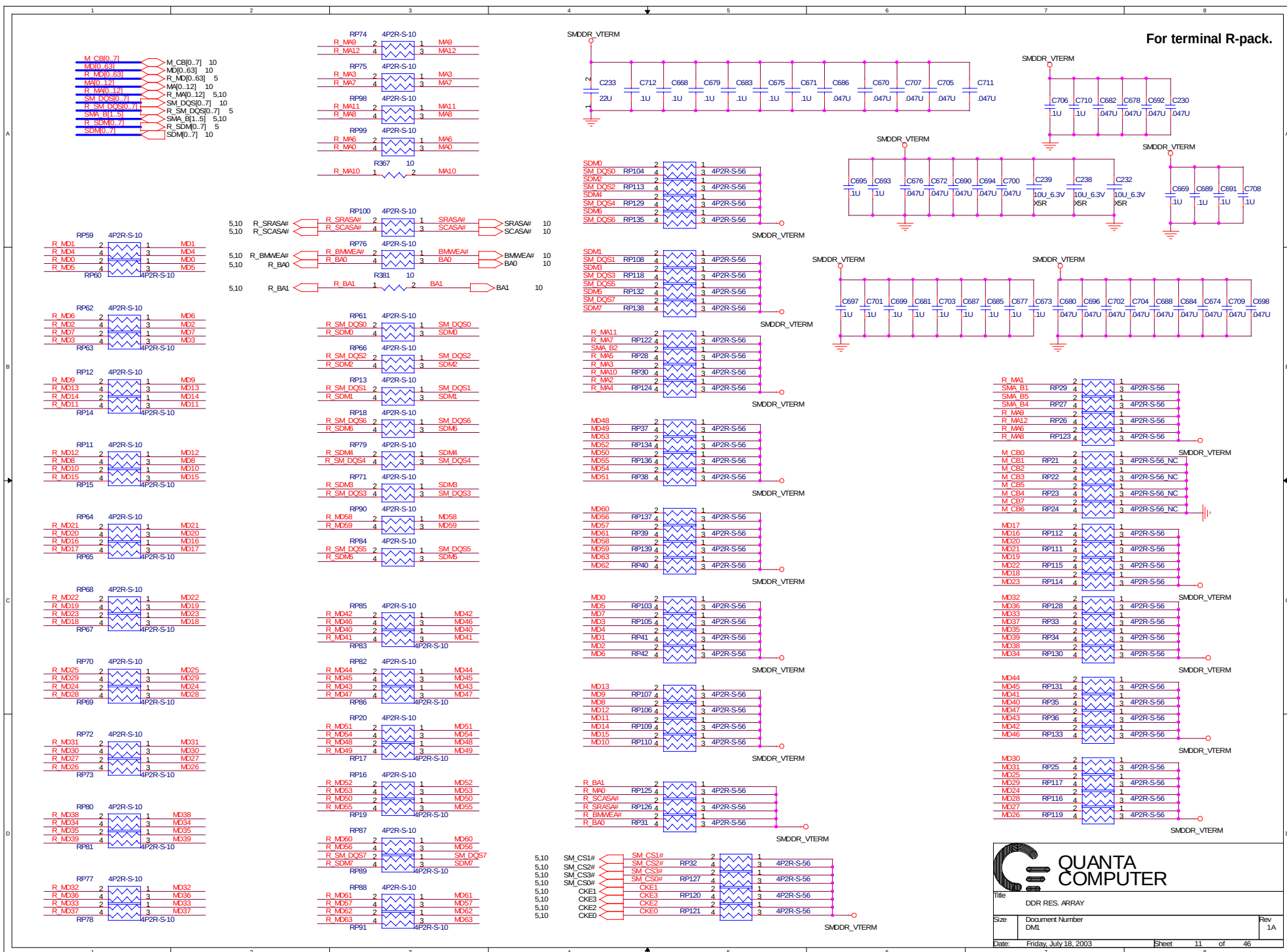
POWER



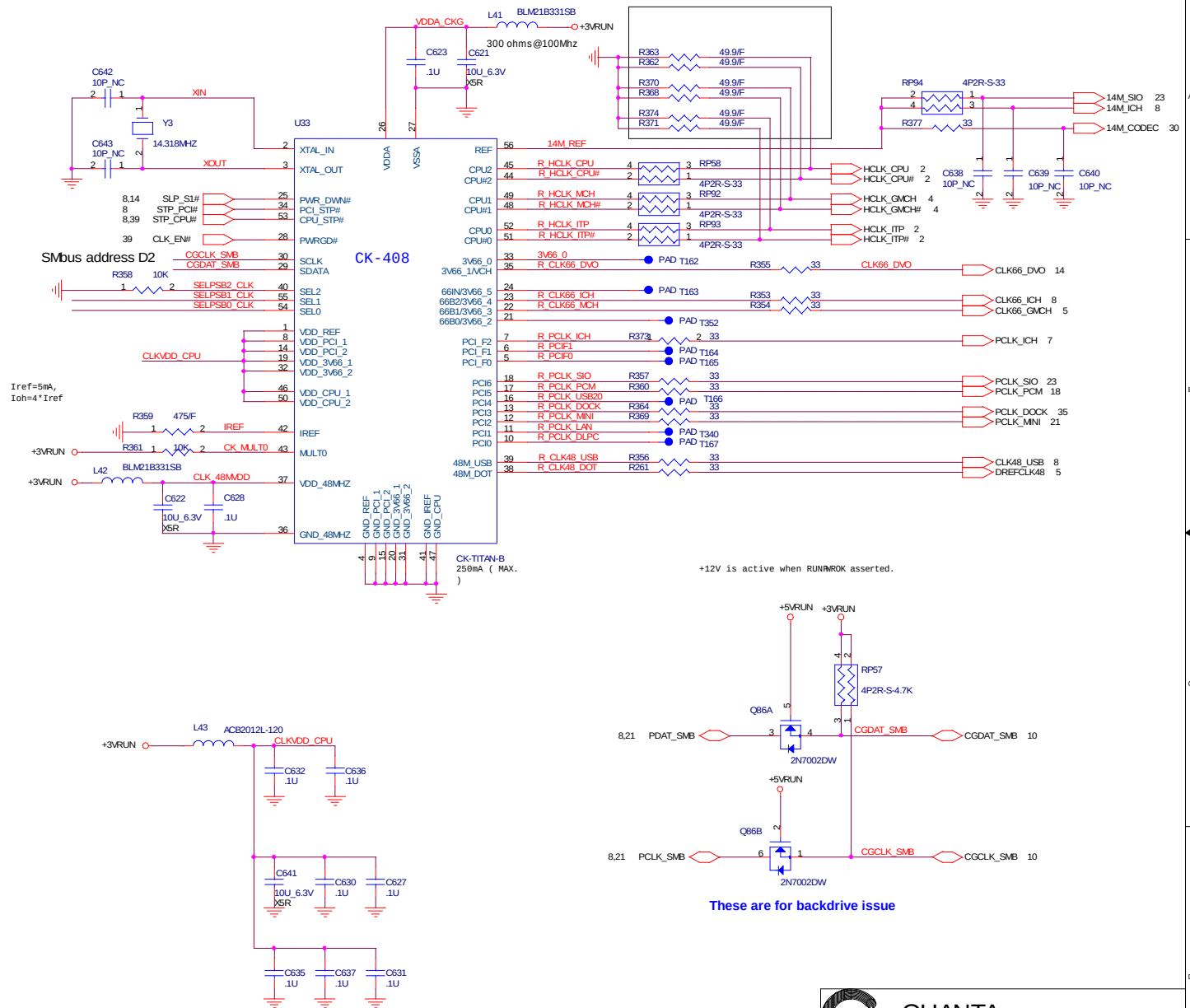




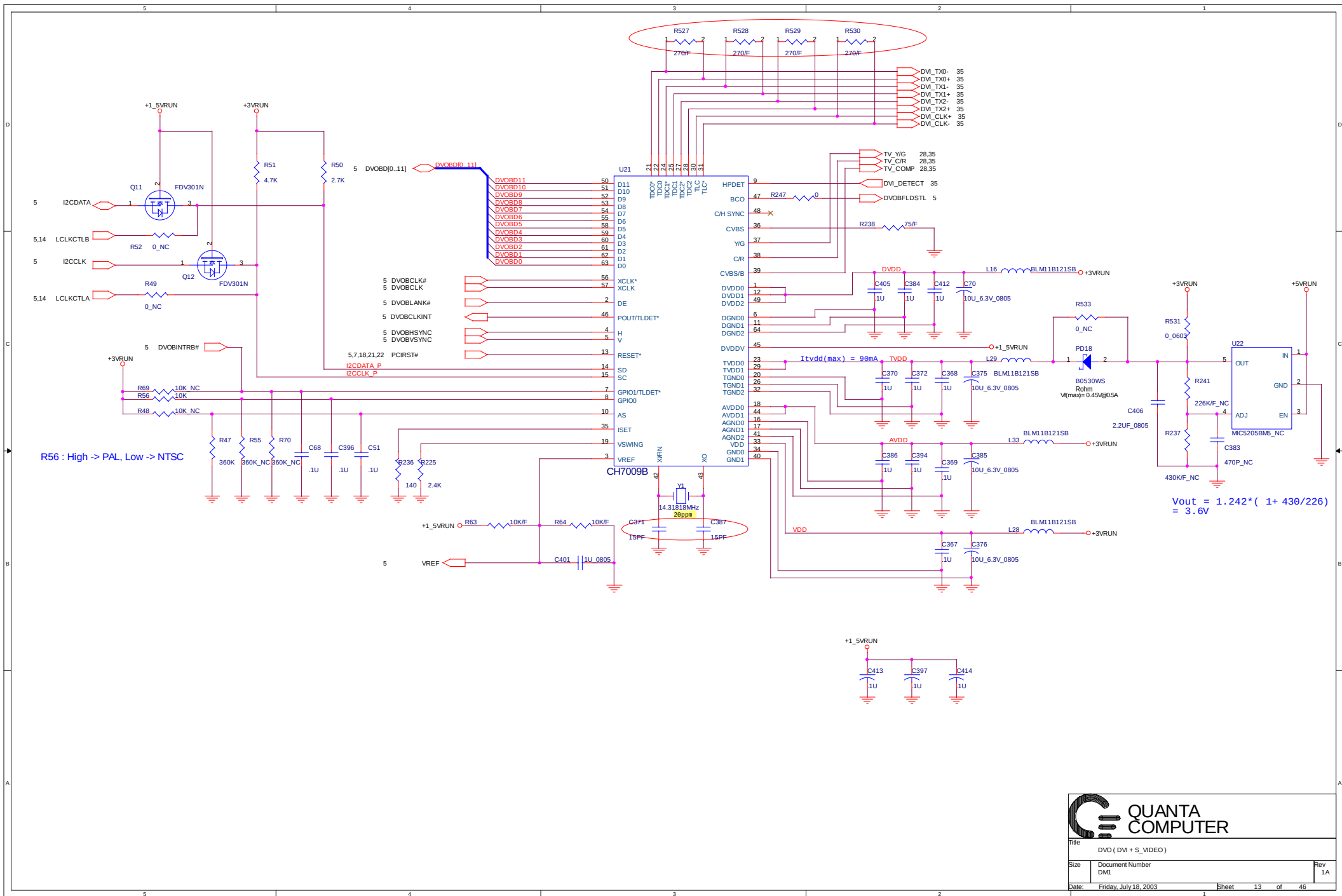


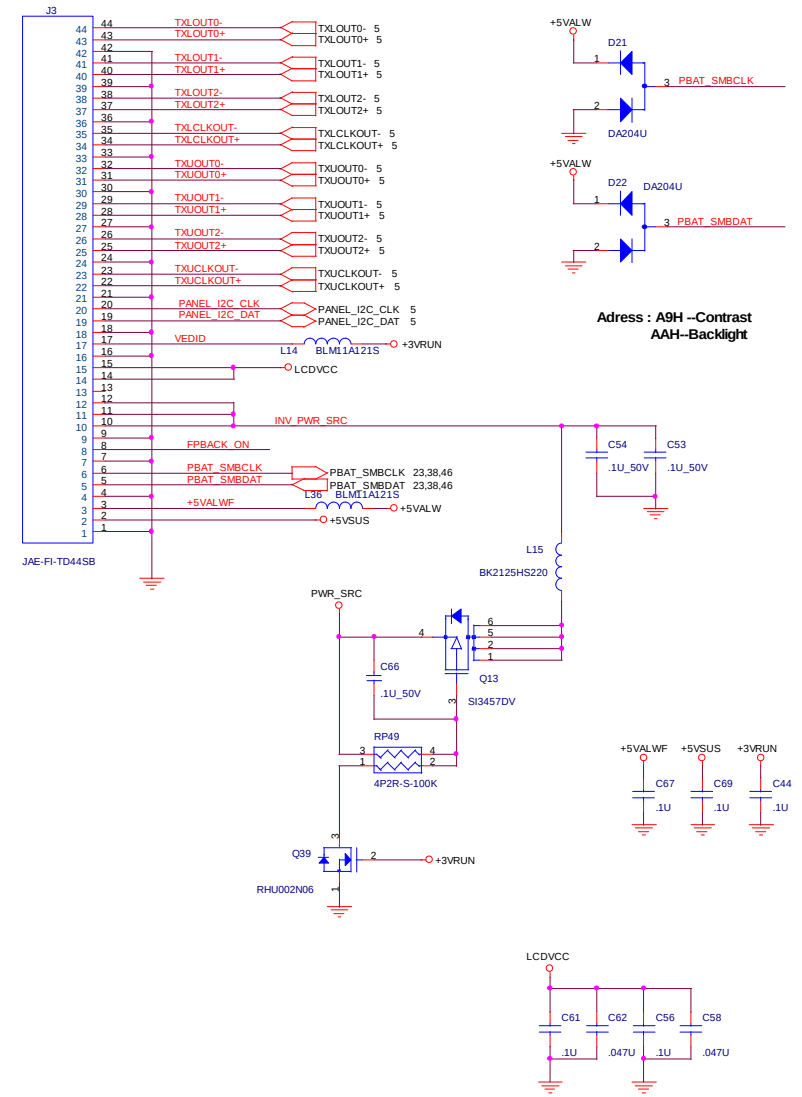
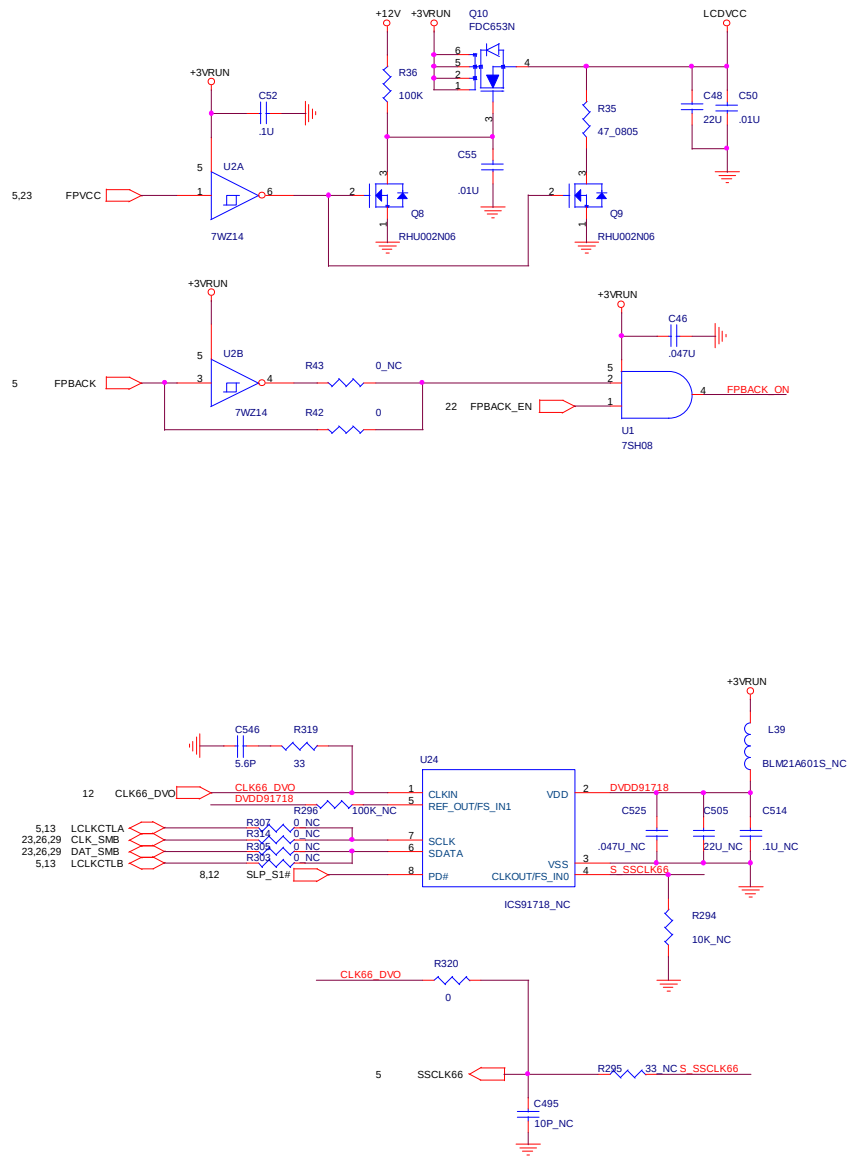


S2	S1	S0	CPU	3V66[0..4]	3V66_5/66IN
1	0	0	66	66IN	66 Input
1	0	1	100	66IN	66 Input
1	1	0	200	66IN	66 Input
1	1	1	133	66IN	66 Input
0	0	0	66	66	66 Input
0	0	1	100	66	66 Input
0	1	0	200	66	66 Input
0	1	1	133	66	66 Input



Title			
CLOCK GENERATOR			
Size	Document Number DML		Rev 1A
Date:	Friday, July 18, 2003	Sheet	12 of 46

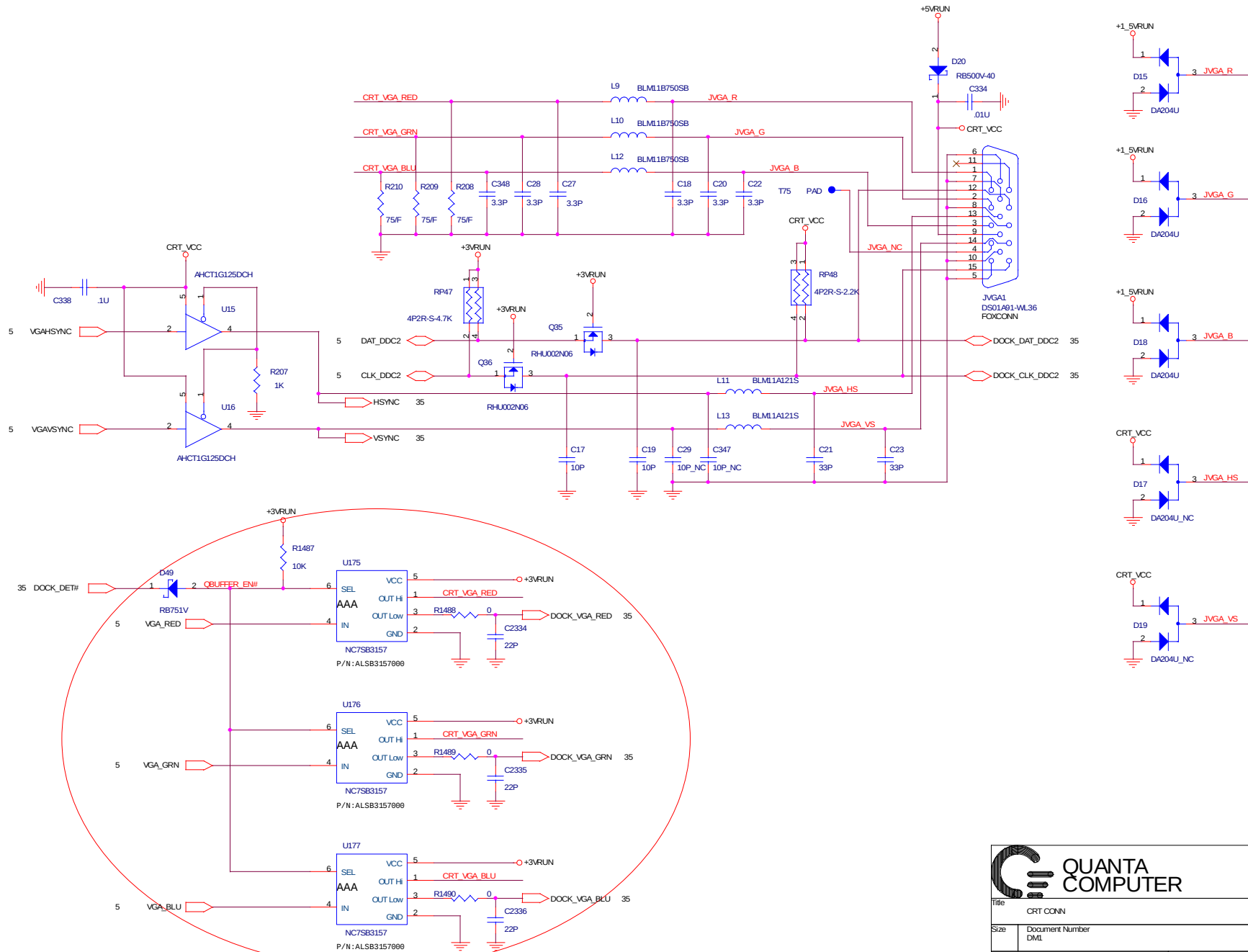




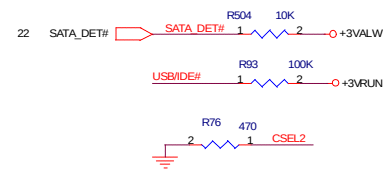
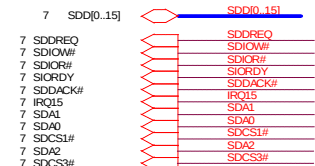
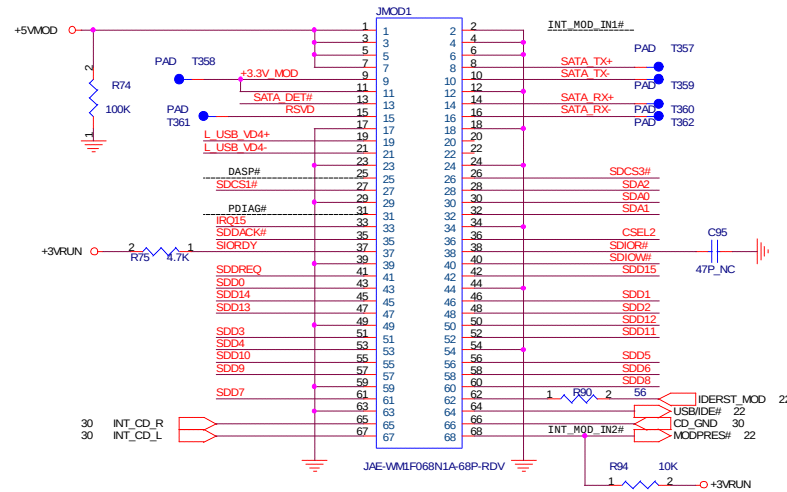
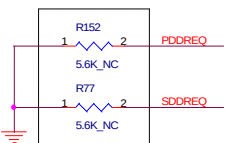
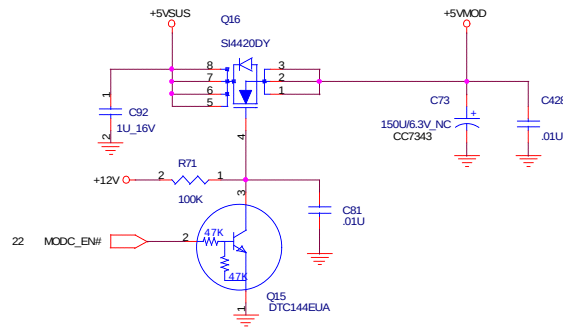
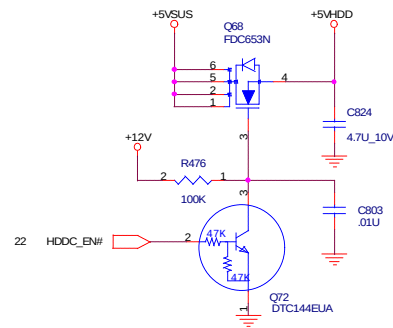
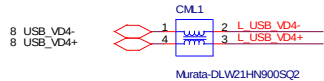
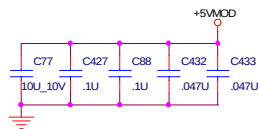
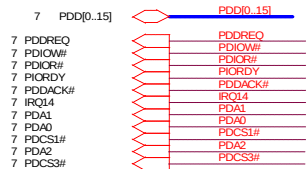
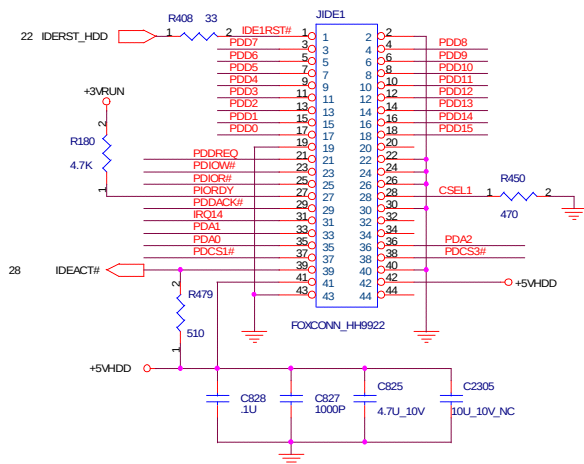
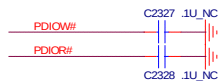
Address : A9H --Contrast
AAH--Backlight



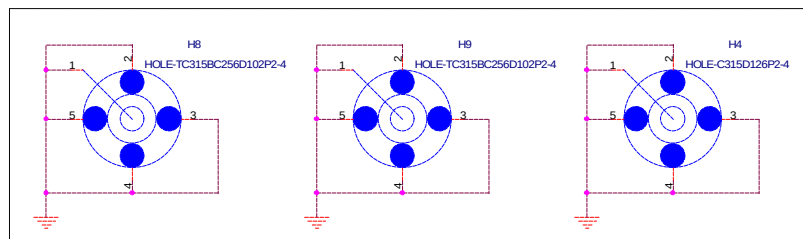
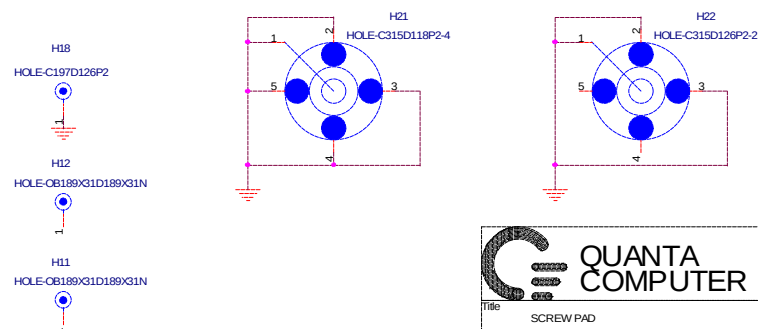
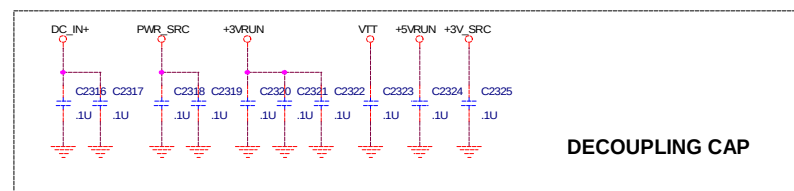
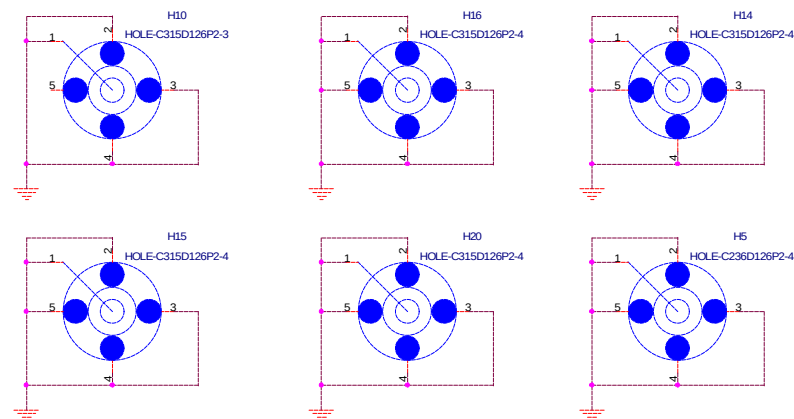
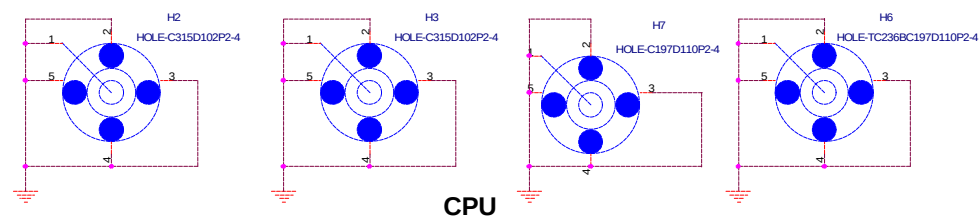
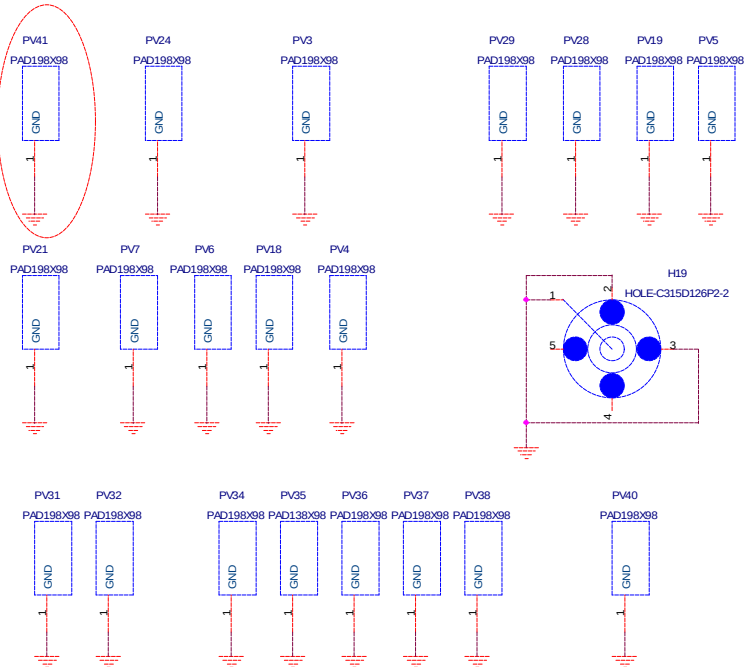
Title			LCD CONN/ICS91718
Size	Document Number	Rev	1A
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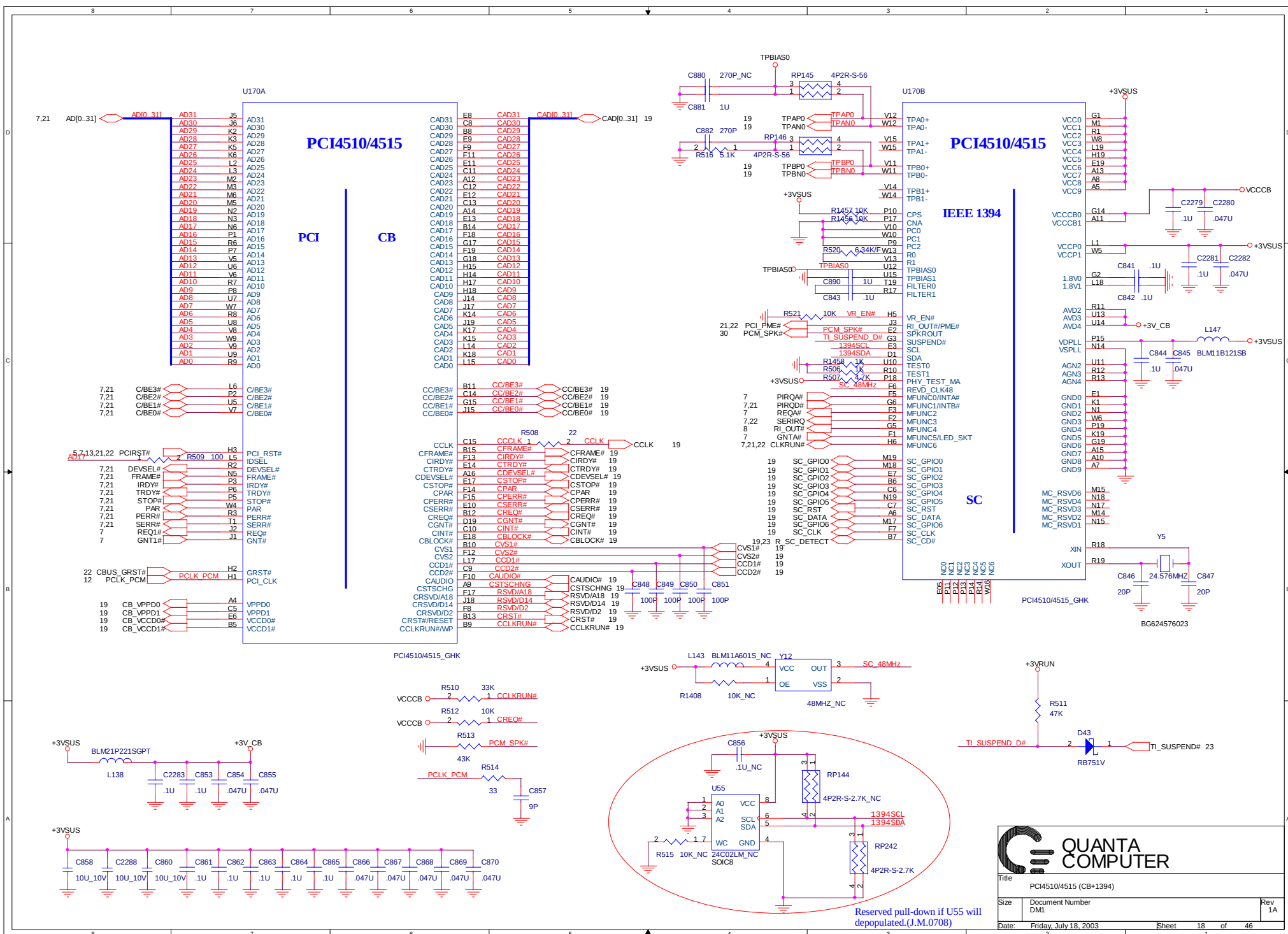


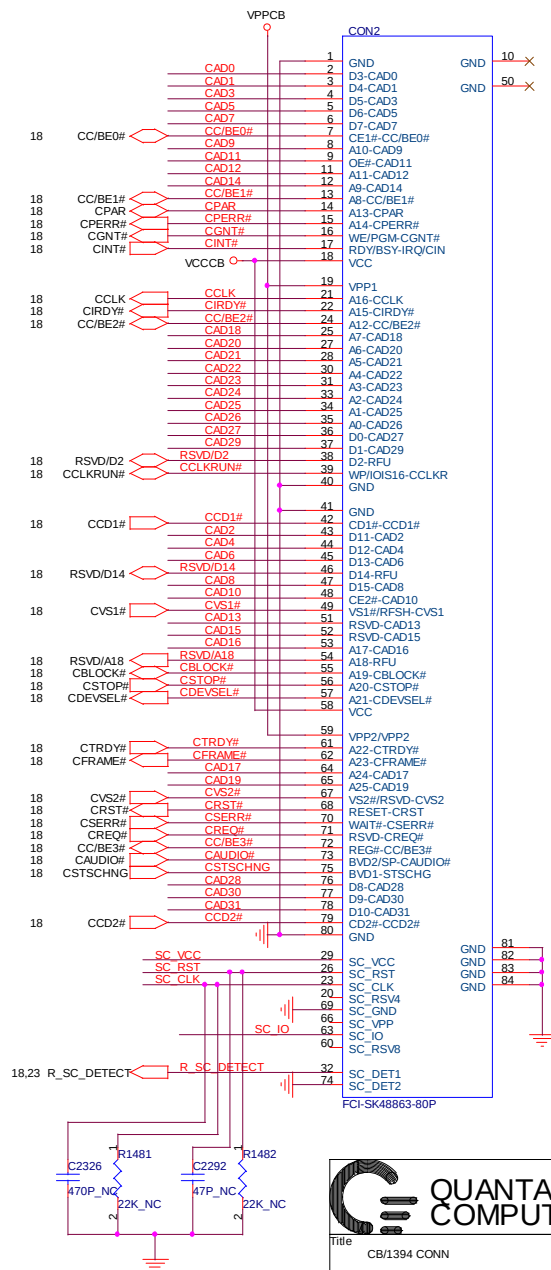
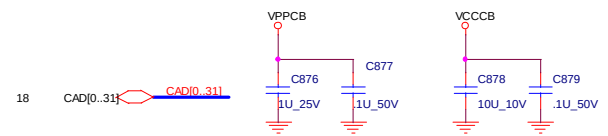
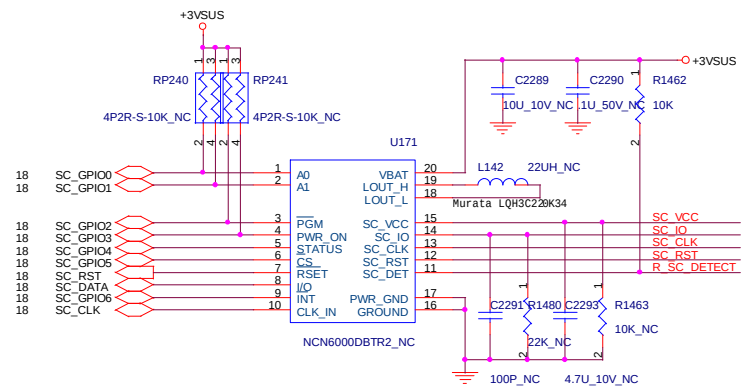
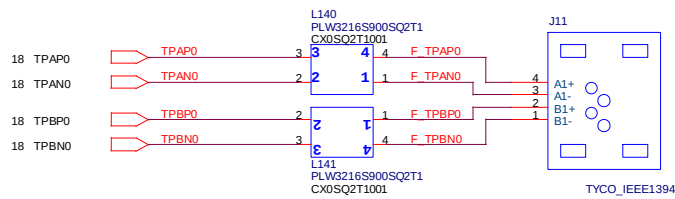
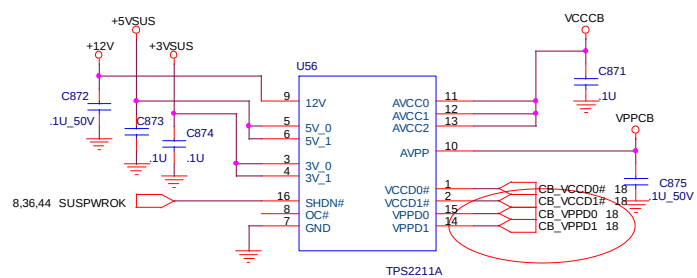
Title			CRT CONN
Size	Document Number	Rev	
	DMT	1A	
Date:	Friday, July 18, 2003	Sheet	15 of 46



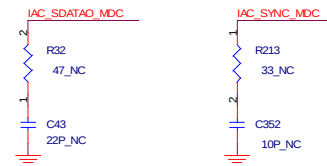
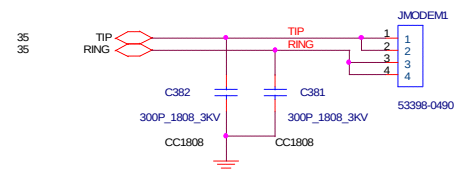
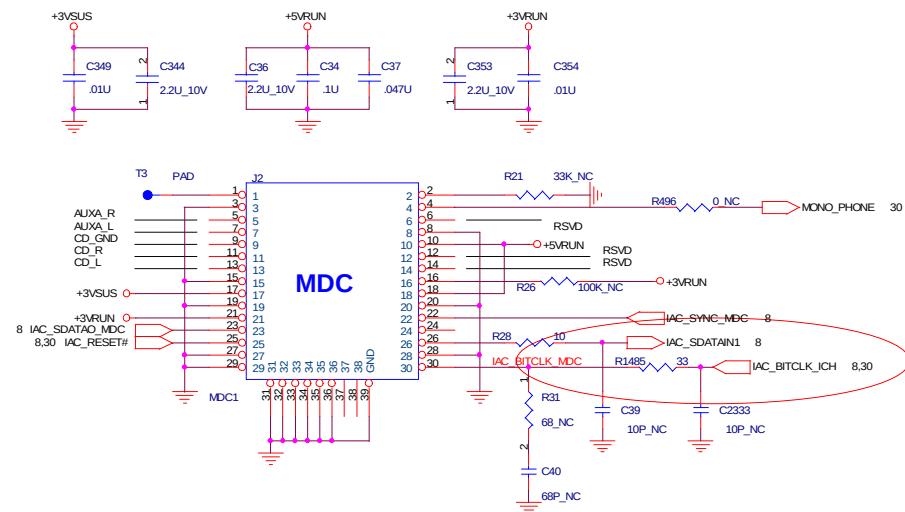
Title			IDE (HDD&CD_ROM)
Size	Document Number	Rev	
	DML	1A	
Date:	Friday, July 18, 2003	Sheet	16 of 46





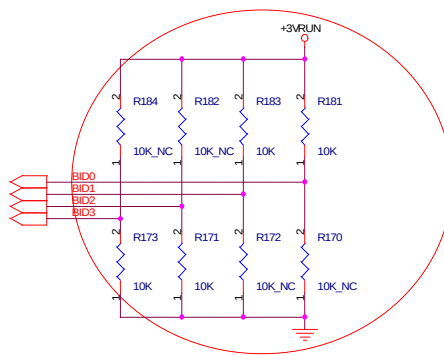


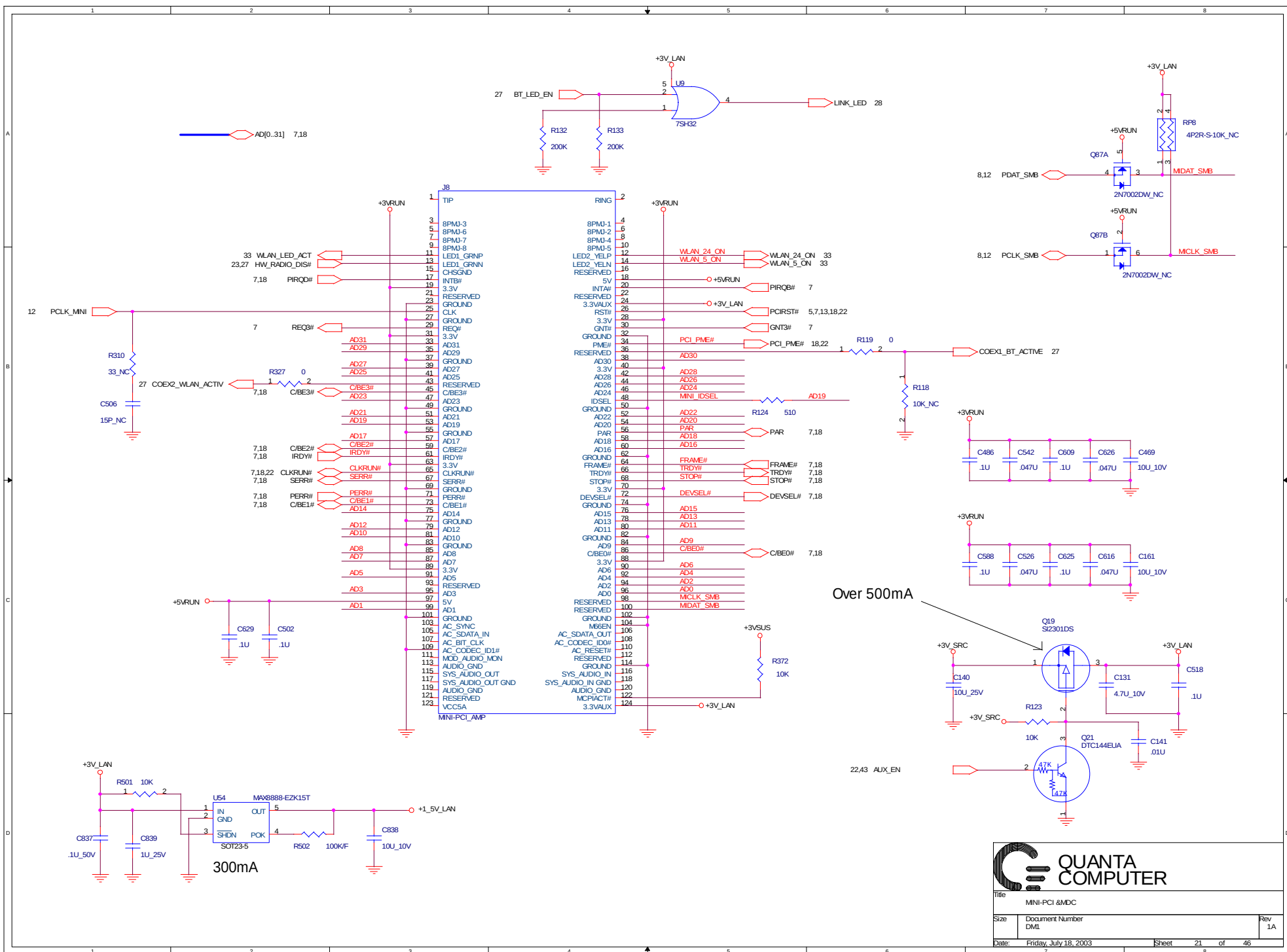
Title CB/1394 CONN			
Size	Document Number DM1	Rev 1A	
Date	Friday, July 18, 2003	Sheet	19 of 46

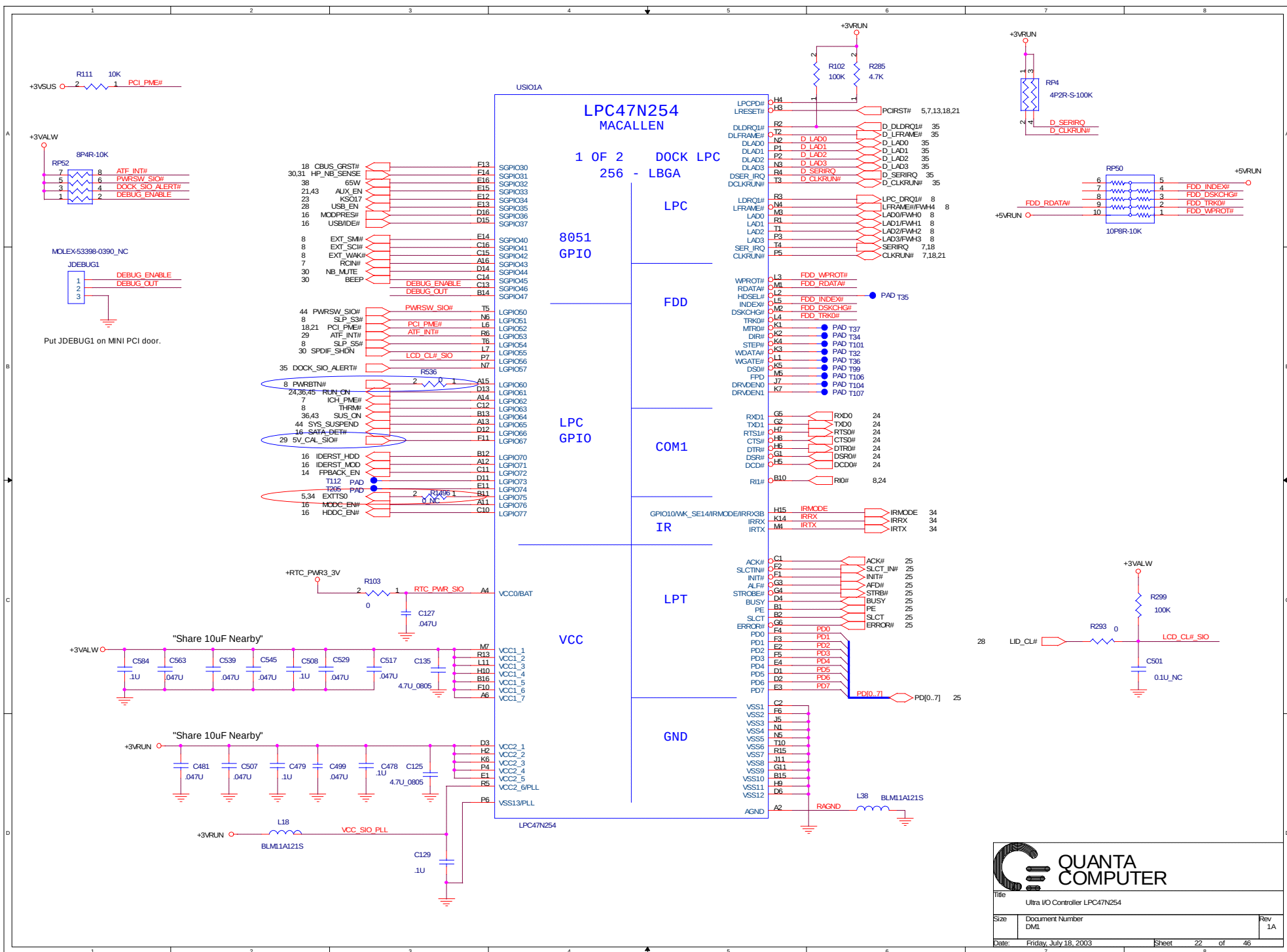


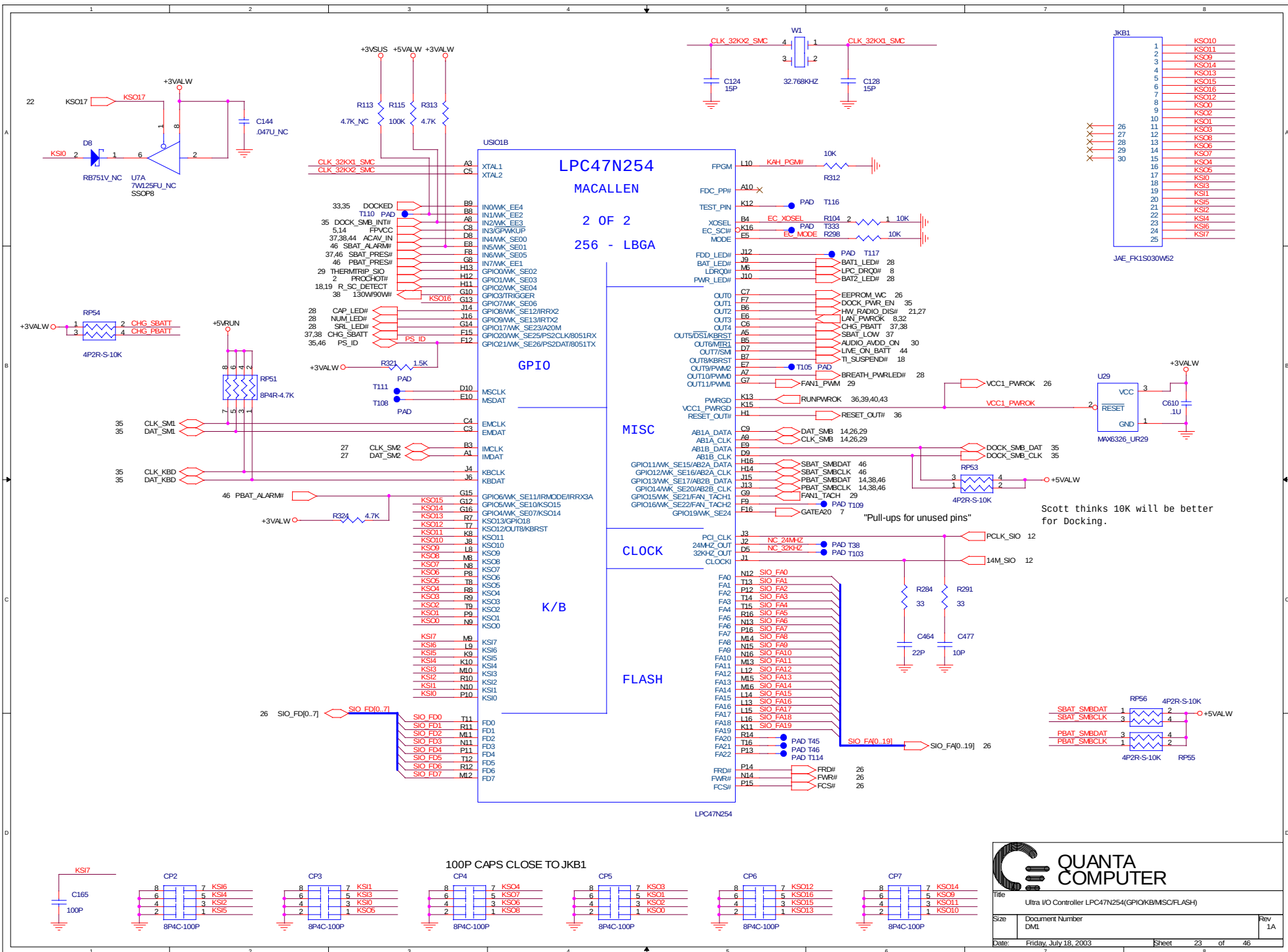
BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	PROT01
0	0	1	0	PROT02
0	0	1	1	PROT03
0	1	0	0	PROT04
0	1	0	1	QT1
0	1	1	0	RAMP

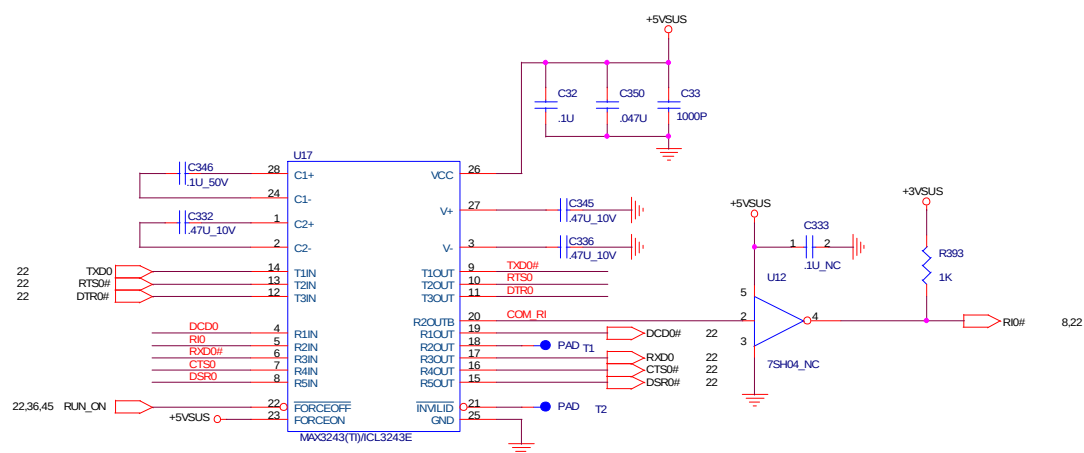
8 BID0
8 BID1
8 BID2
8 BID3



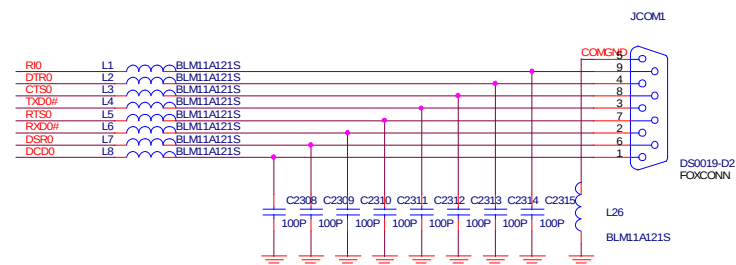








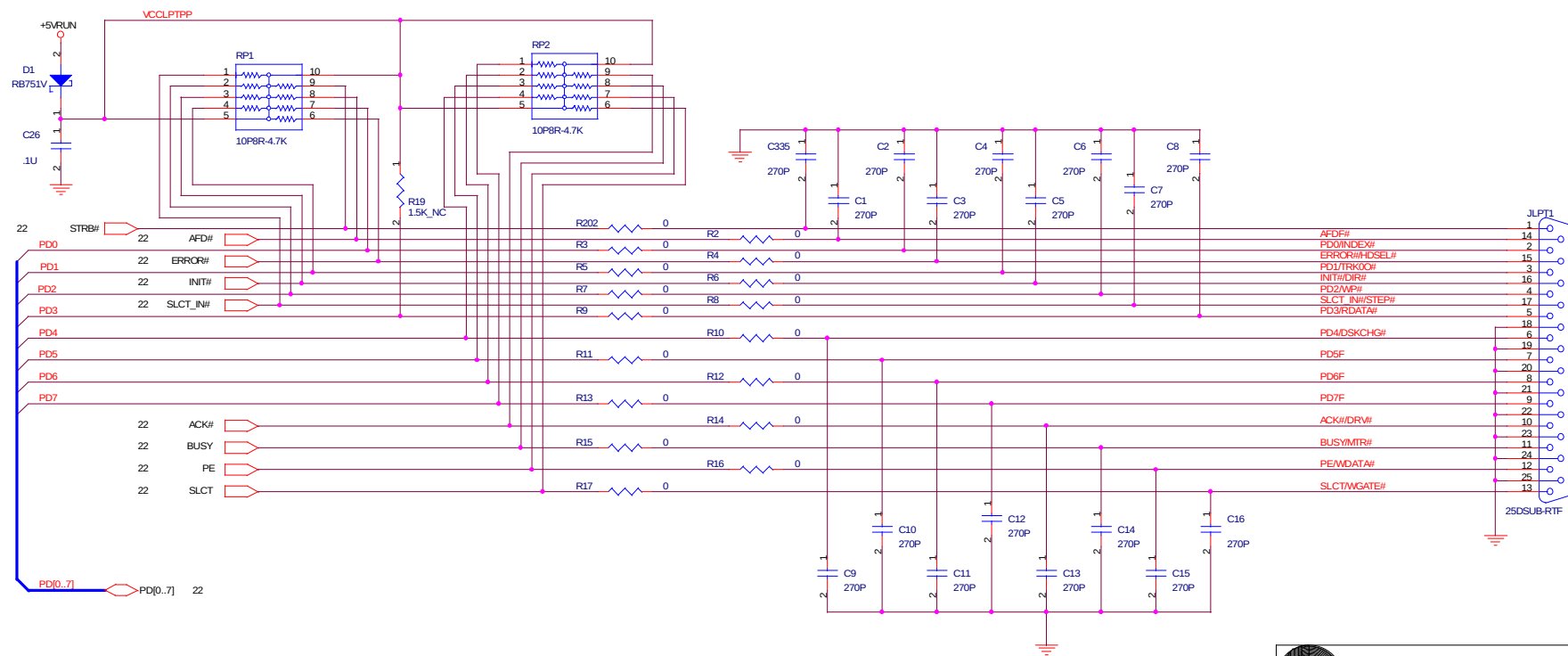
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out



Place these beads to JCOM1 as close as possible

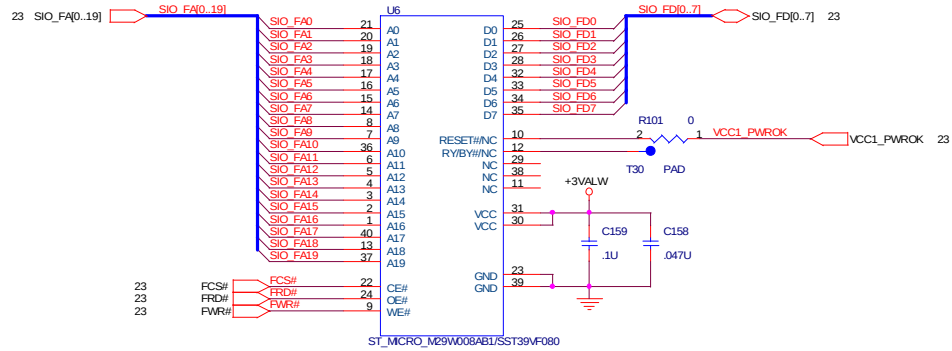


Title			SERIAL PORT	
Size	Document Number	Rev		1A
Date:	Friday, July 18, 2003	Sheet	24	of 46



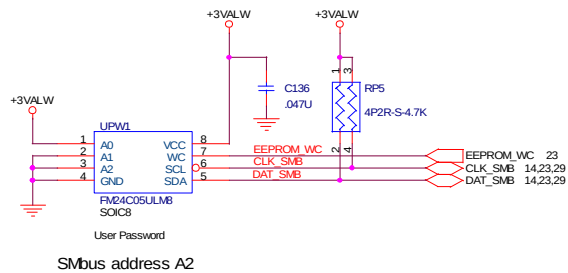
Title			PARALLEL CONN.
Size	Document Number	Rev	
	DMT	1A	
Date:	Friday, July 18, 2003	Sheet	25 of 46

8Mbit (1MByte),NO PLCC TYPE

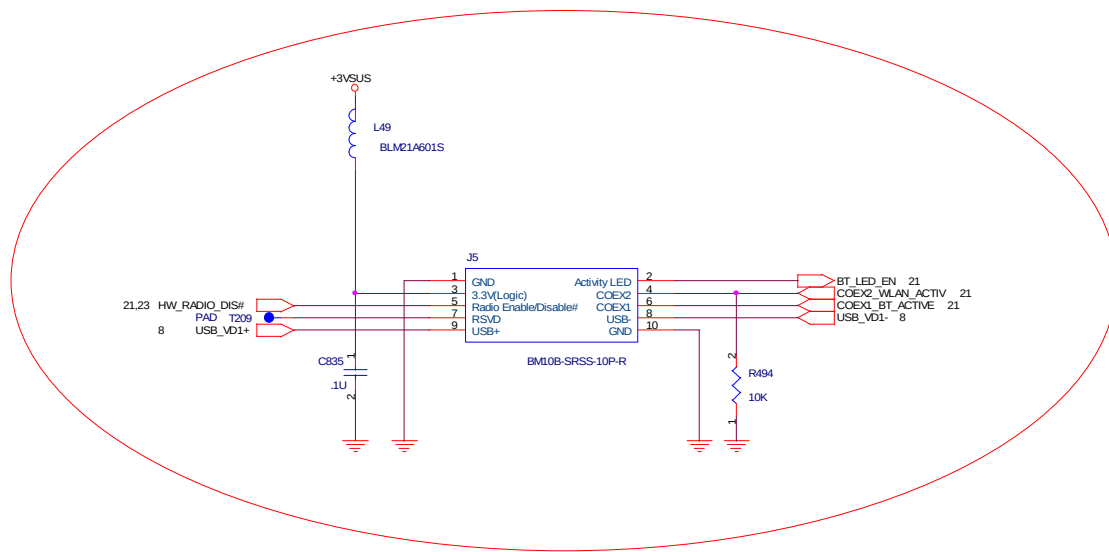
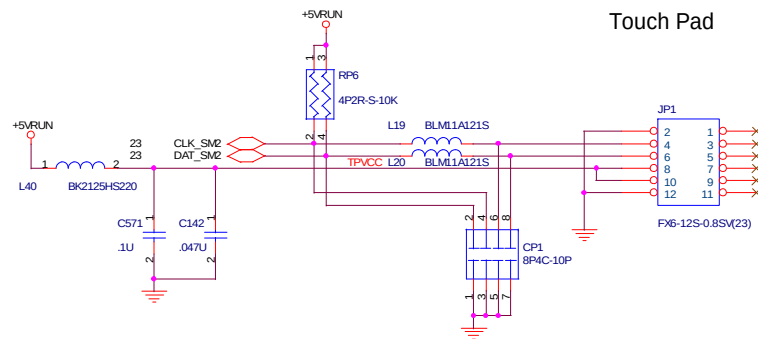


SST :Pin10,12 are NC

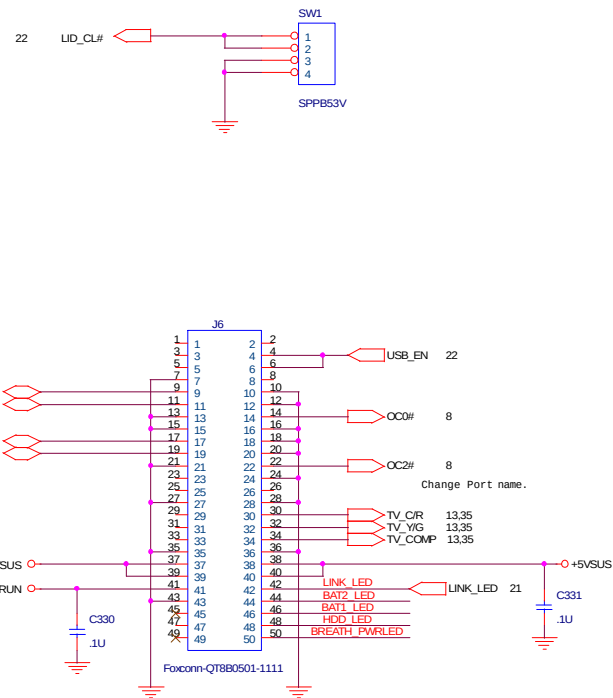
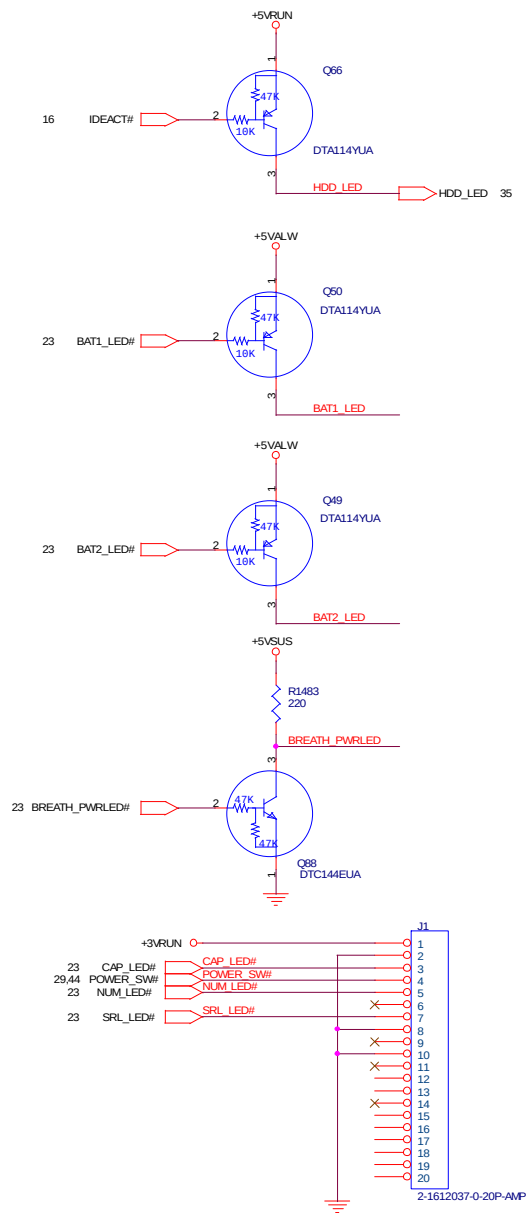
- 1.MAX6326 UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK



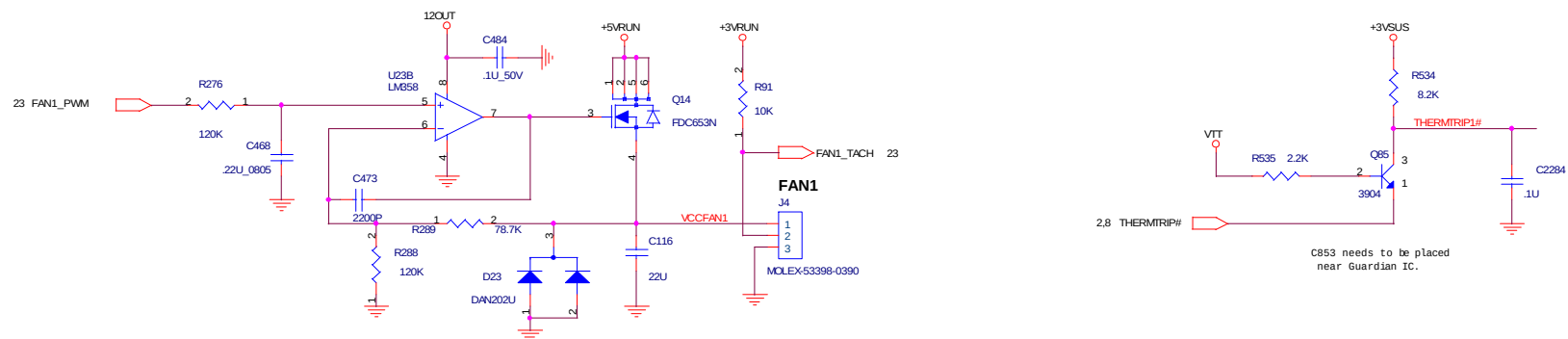
Title FLASH		
Size	Document Number DMT	Rev 1A
Date:	Friday, July 18, 2003	Sheet 26 of 46



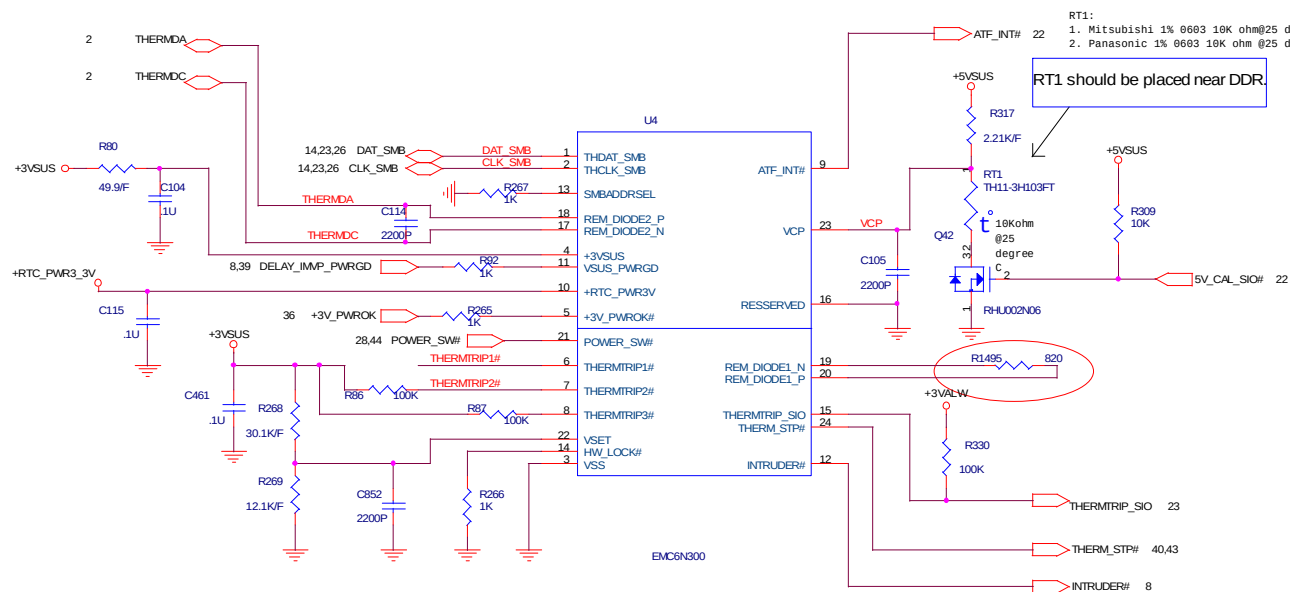
Title			TOUCH PAD & BULE TOOTH
Size	Document Number	Rev	
	DM1	1A	
Date:	Friday, July 18, 2003	Sheet	27 of 46



Title			SWITCH & LED
Size	Document Number	Rev	
	DMT	1A	
Date:	Friday, July 18, 2003	Sheet	28 of 46

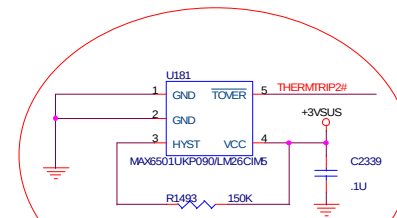


C853 needs to be placed near Guardian IC.



RT1:
1. Mitsubishi 1% 0603 10K ohm @25 degree C. P/N: TH11-3H103FT
2. Panasonic 1% 0603 10K ohm @25 degree C. P/N: ERT31V6103FA

RT1 should be placed near DDR.



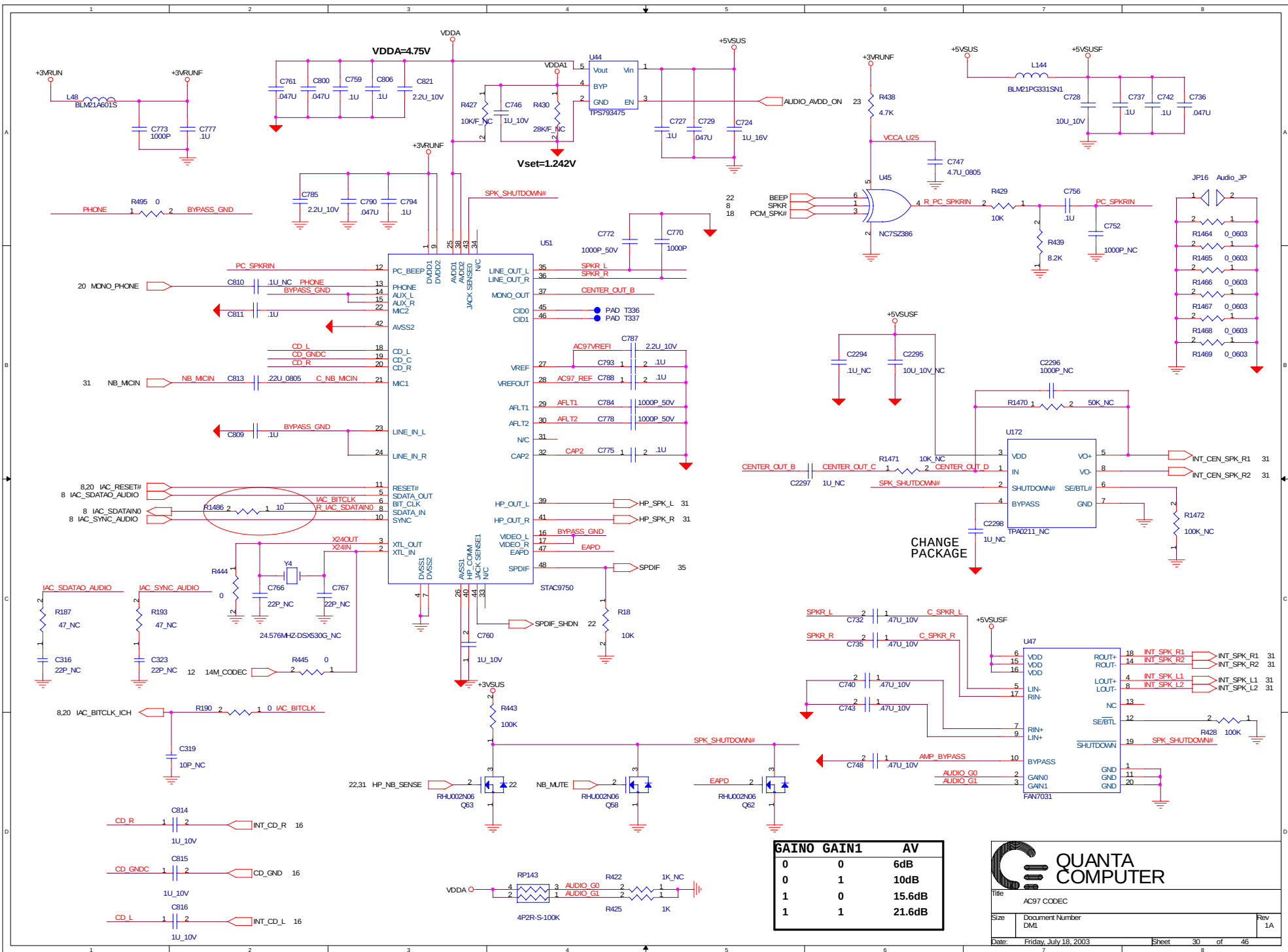
U136=LM26
HYST | GND | VCC
10 degree | 2 degree

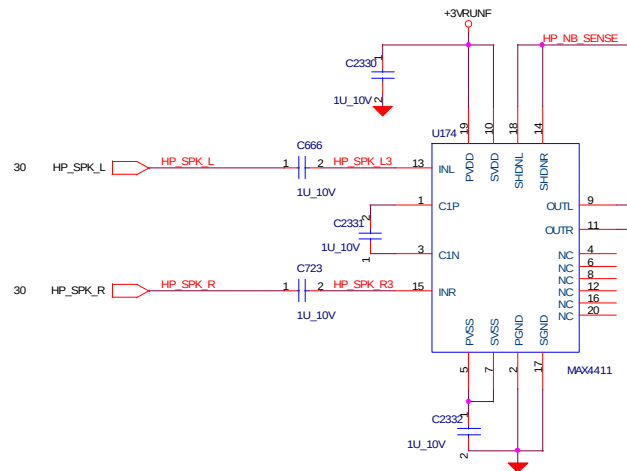
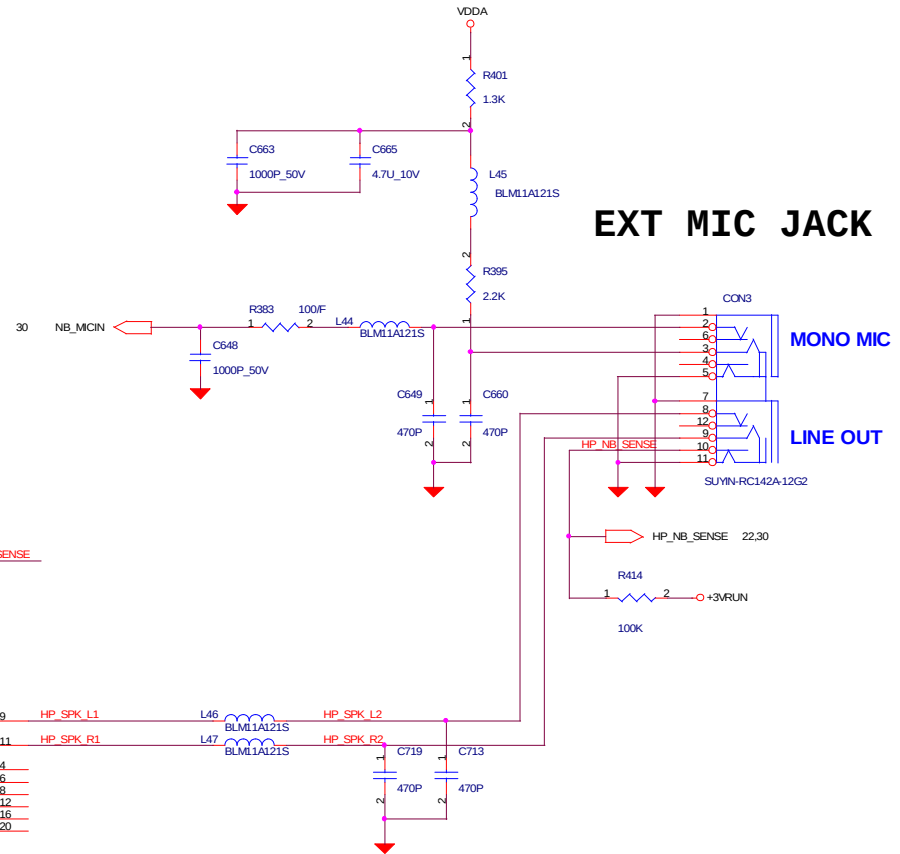
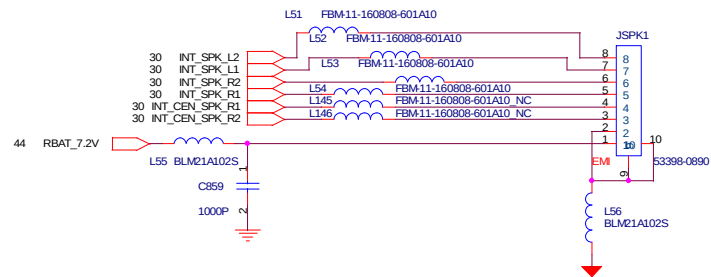
U136=MAX6501
HYST | GND | VCC
2 degree | 10 degree

Notes:
 $V_{set} = (T_p - 75) / 16$
Where $T_p = 75$ to 106 degree C
Set trip point = 90 degree C
 $V_{set} = (90 - 75) / 16 = 0.9375 V$
Guardian temp-tolerance = ± 3 degree C



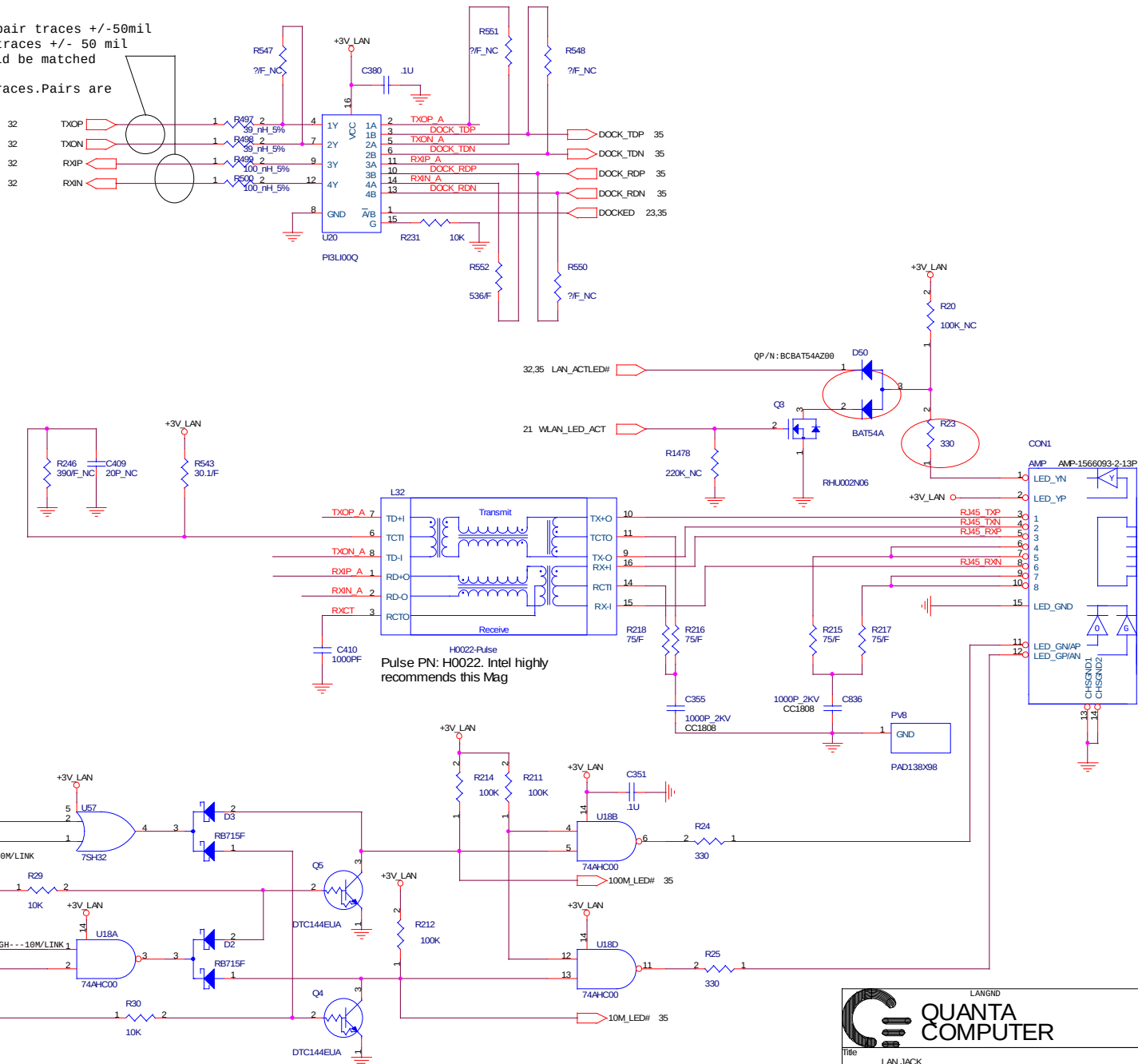
Title: FAN & THERMAL		
Size: DMT	Document Number: 1A	Rev: 1A
Date: Friday, July 18, 2003	Sheet: 29	of 46



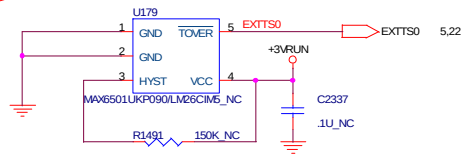
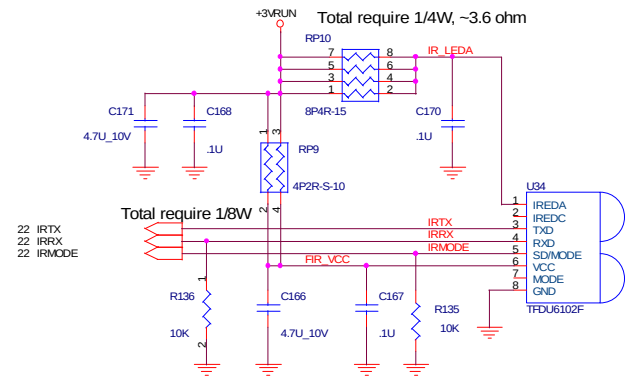


Title			AUDIO CONN
Size	Document Number	Rev	
	DMT	1A	
Date:	Friday, July 18, 2003	Sheet	31 of 46

LAYOUT NOTES:
Match total length of chip side Rx and Tx pair traces +/-50mil
Match length of cable side Rx and Tx pair traces +/- 50 mil
Total line TX+ to TX- and RX- and RX+ should be matched within 50 mils.
Keep 50mil space between pairs and other traces.Pairs are 100ohm differential,



LAN_SPDLED#	SPEED
HI	10M
LO	100M

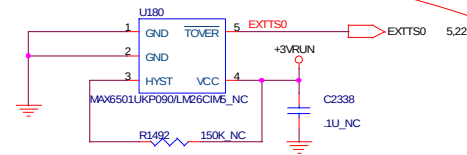


U136=LM26

	GND	VCC
HYST	10 degree	2 degree

U136=MAX6501

	GND	VCC
HYST	2 degree	10 degree



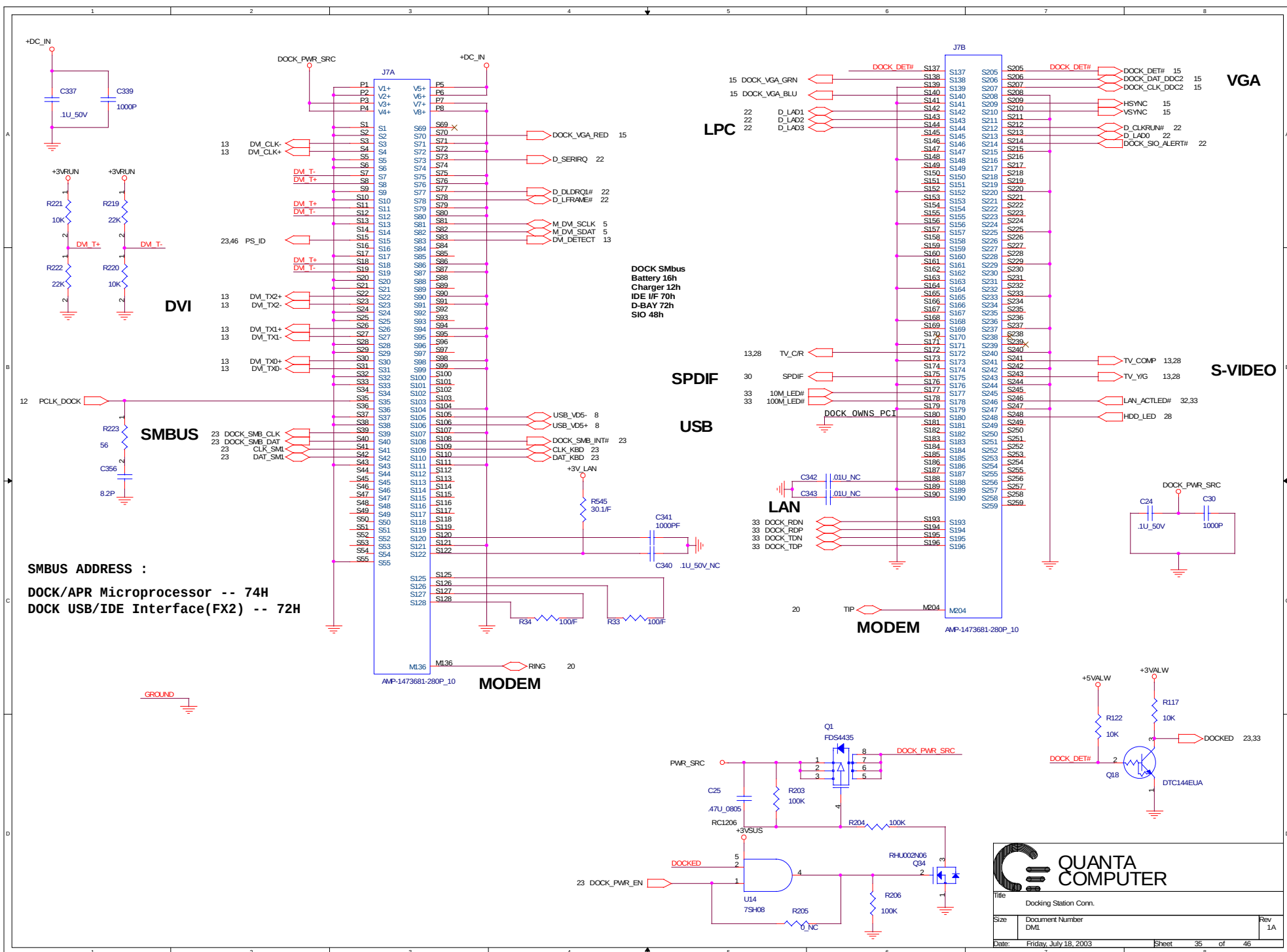
U136=LM26

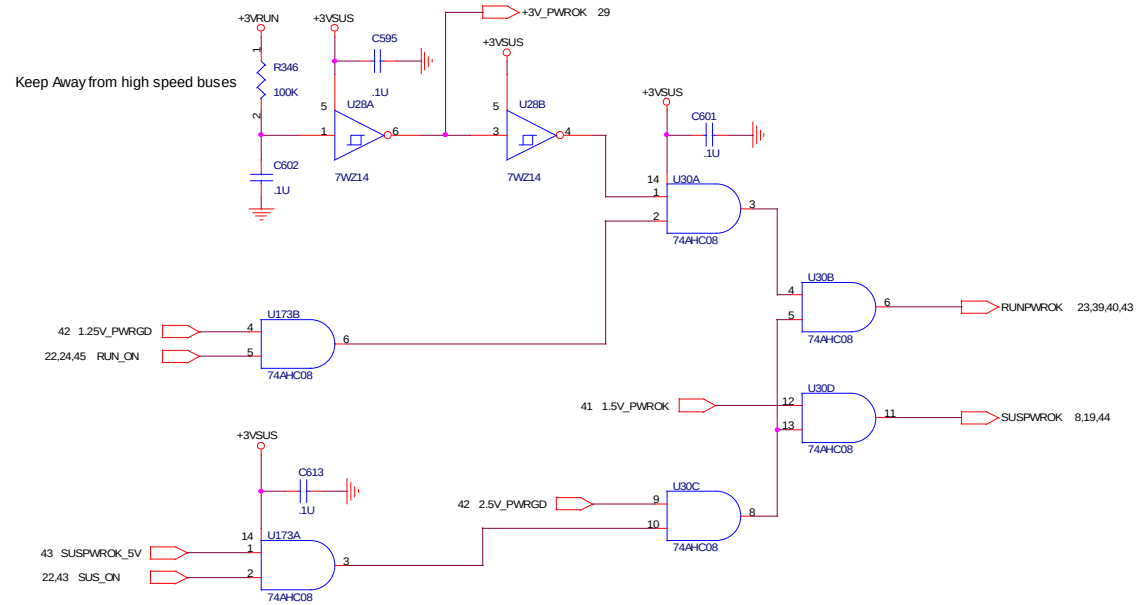
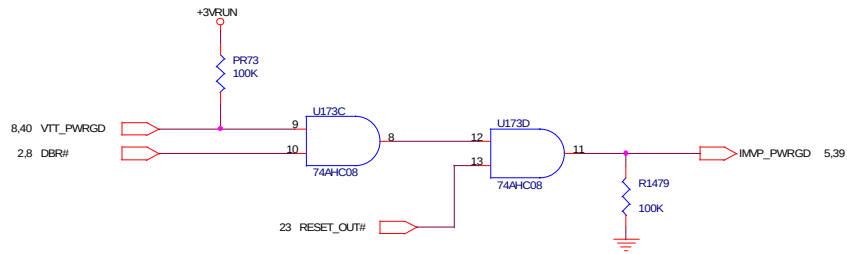
	GND	VCC
HYST	10 degree	2 degree

U136=MAX6501

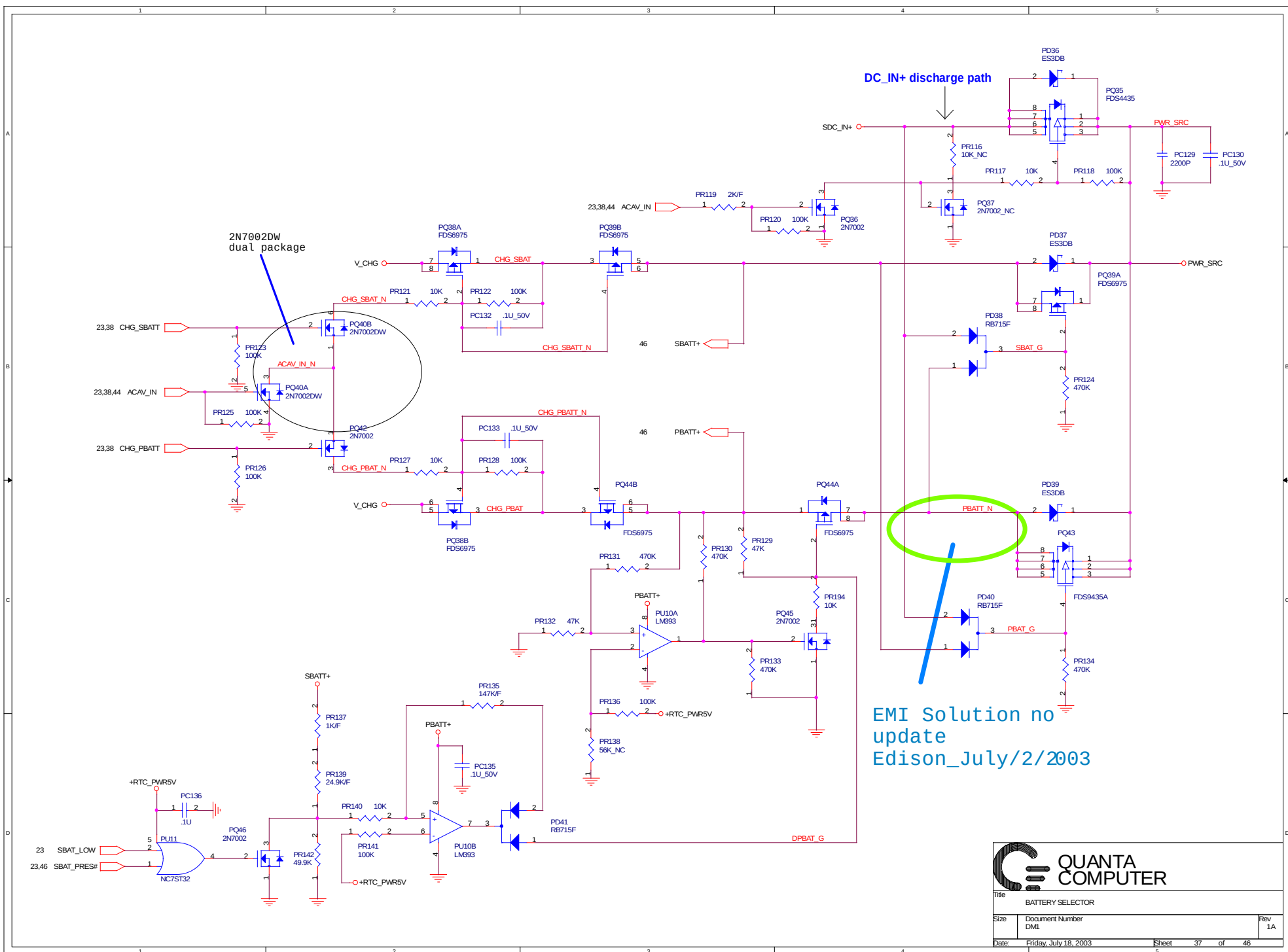
	GND	VCC
HYST	2 degree	10 degree



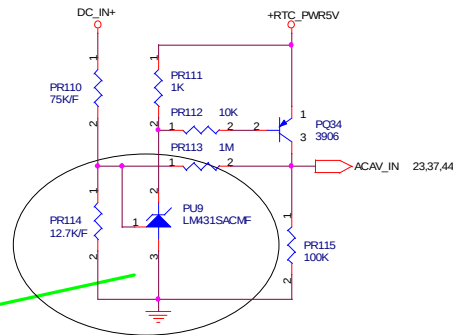




Title			POWER GOOD
Size	Document Number	Rev	
	DMT	1A	
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Title			BATTERY SELECTOR
Size	Document Number	Rev	
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The library of PU9
will modify
April/8_Edison

Adding Caps
July/14_Edison

IMVP-VI(Rev :1.0)
For load-line
Specification
June/23_Edison

IMVP-VI(Rev :1.0)
offset update 1.2%
May/6_Edison

CPI-1350-0R6_TOKIN
height 5mm MAX.
30A
March/3_Edison

Limited Current Point =28.5A

Adding Caps
May/6_Edison

100 mil Trace list for layout

DH_VCORE
LX_VCORE
DL_VCORE

The PC155 from 1uF
change to 0.22uF
April/8_Edison

V I D							Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V	
0	0	1	1	1	1	1.468	
0	1	0	1	1	1	1.340	
0	1	1	0	0	0	1.324	
0	1	1	0	1	0	1.292	
0	1	1	1	0	0	1.260	
0	1	1	1	0	1	1.244	
0	1	1	1	1	1	1.212	
1	0	0	0	0	1	1.180	
1	0	0	0	1	1	1.148	
1	0	0	1	1	0	1.100	
1	0	1	0	0	1	1.052	
1	0	1	0	1	1	1.020	
1	0	1	1	1	0	0.972	
1	1	0	0	0	0	0.940	

PR84 OR
1907_S0
PR89 OR
1907_S1
PR90 OR_NC
1907_S2

The C4 mode voltage is 0.748V

PBOOT VOLTAGE
SETTING UP ON
1.212V

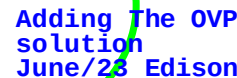


CPU POWER		
Size	Document Number DMI	Rev 1A
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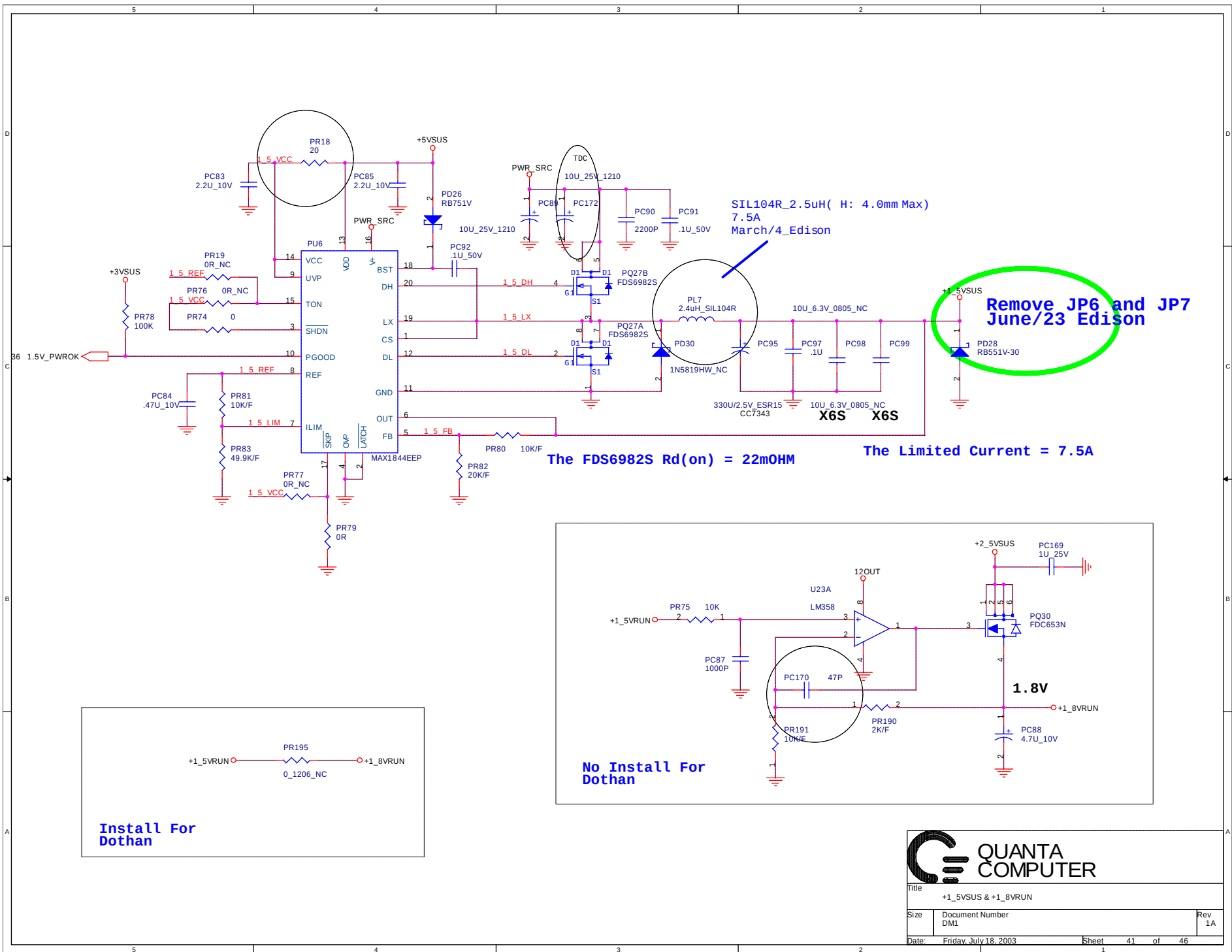


Remove JP3 and JP5
June/23 Edison

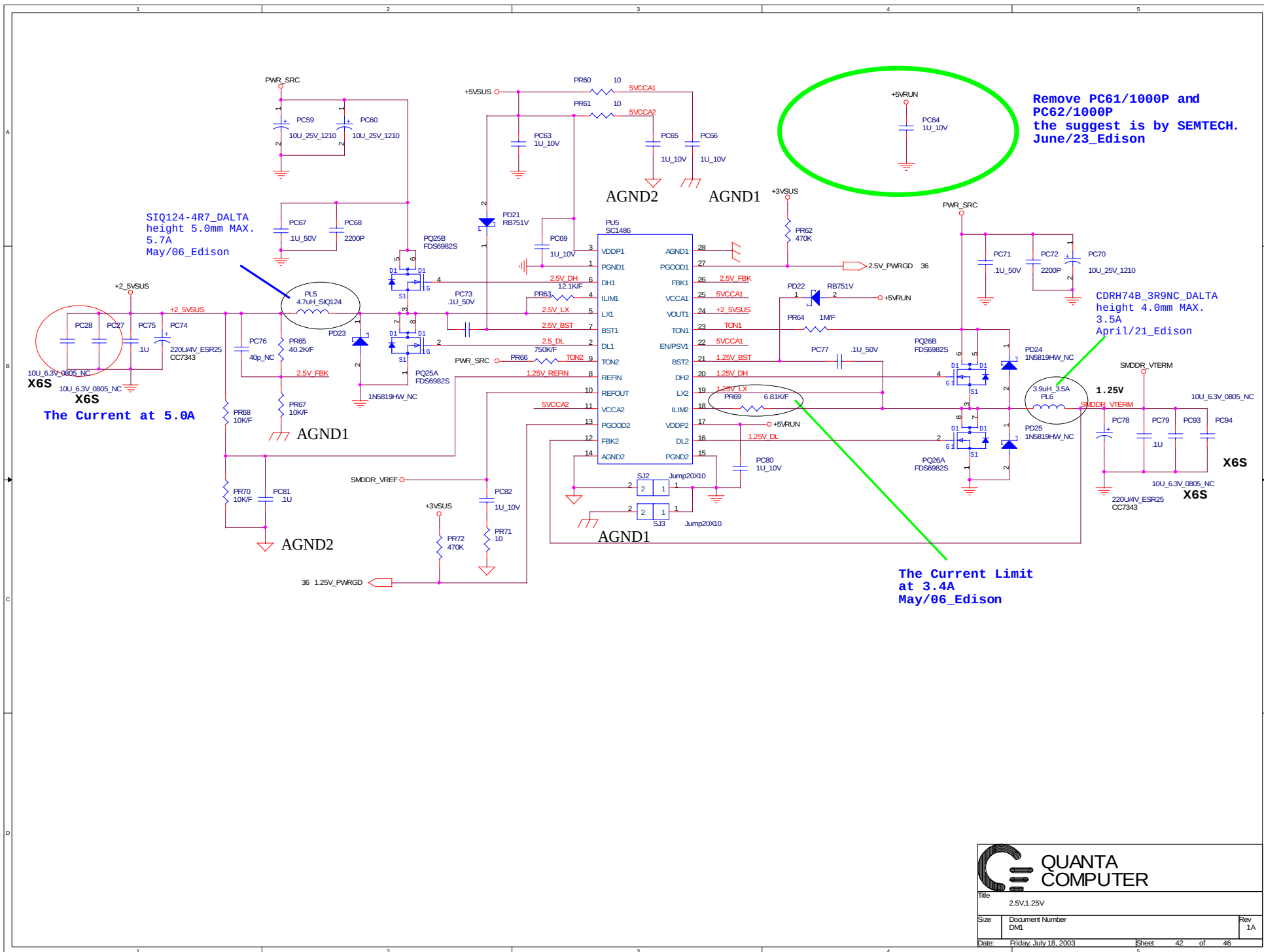
```
1.20V - GM1 PR23=14.0K/F
1.35V - GM1 PR23=16.9K/F
+VCC1 2 GMCH Current Limite 3.2A
```



VTT OVP Point = 1.15V
+VCC1_2_GMCHOVP Point = 1.48V



Title		
+1_5VSUS & +1_8VRUN		
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Remove JP12 and JP14
June/23 Edison

Current limit at 4A for +3.3V

Place these CAPS close to FETs
SIL104R_100NC_DELTA
height 4.0mm MAX.
4.4A
April/8_Edison

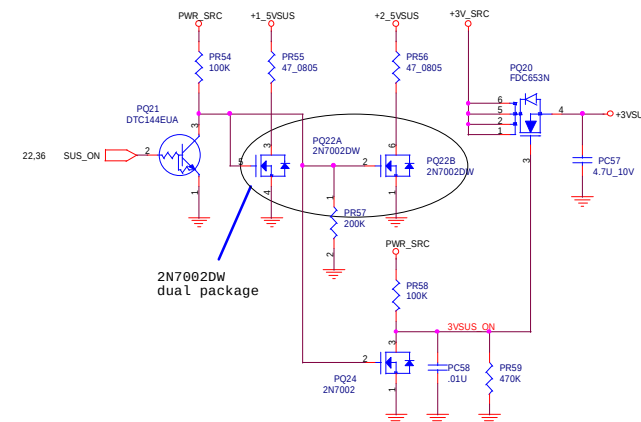
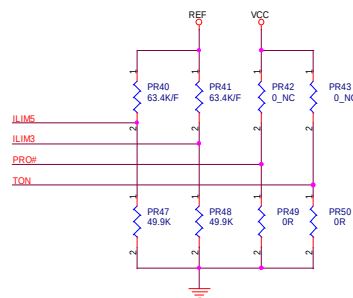
Place these CAPS close to FETs

Current limit at 4A for +5VSUS

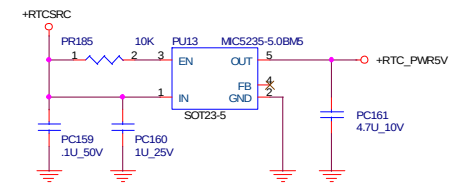
Remove JP13 and JP15
June/23 Edison

From CC1206 change to CC0805
April/8_Edison

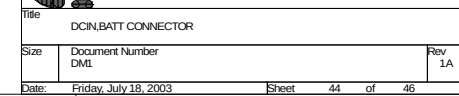
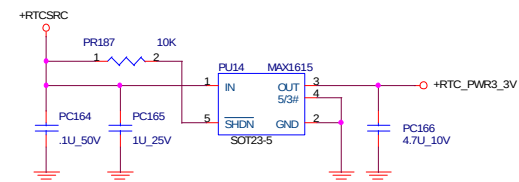
STQ125-1022A
height 6mm MAX.
4.3A
March/3_Edison

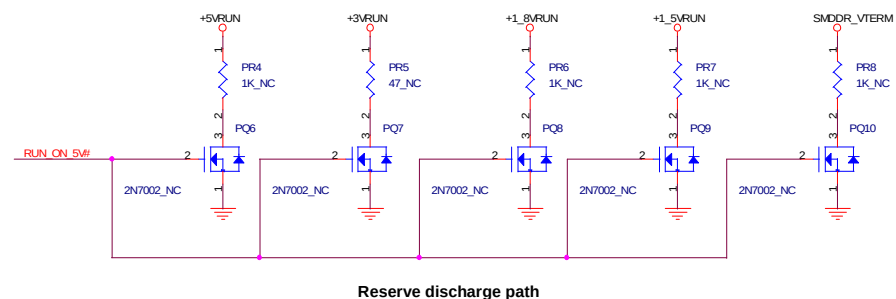
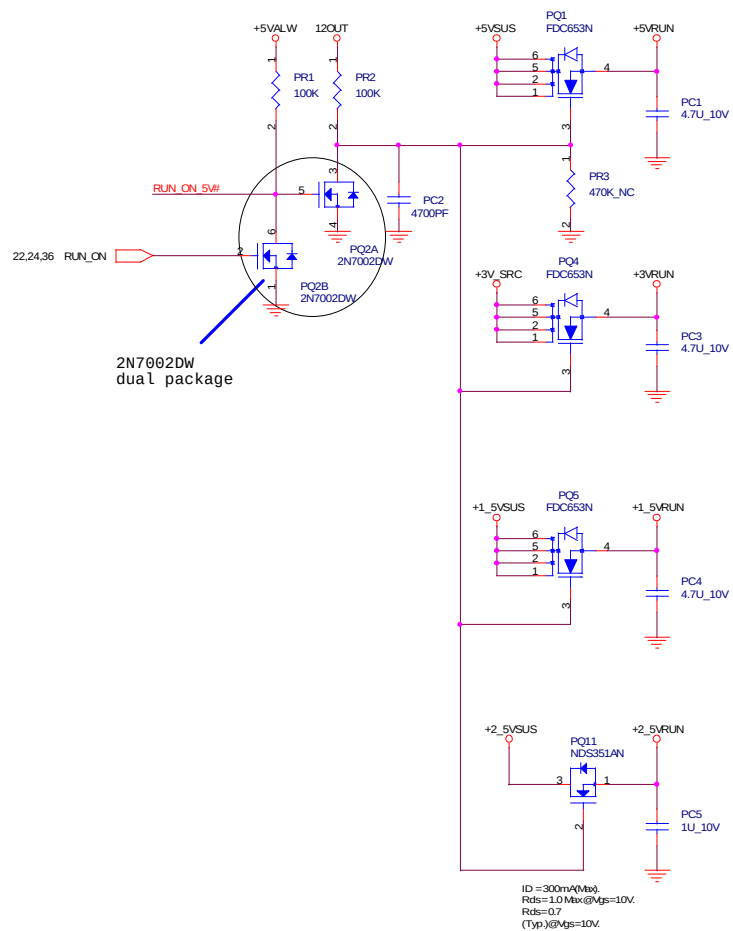


Title				
+3VSRC & +3VSUS & +5VSUS				
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The schematic diagram illustrates the logic for the ALWON signal. It features three NAND gates: PU15 (7SH04), PU16 (7SH32), and PU17 (7SH32). The ALWON signal is generated by the output of PU16. The inputs to PU16 are the outputs of PU15 and PU17. PU15's inputs are POWER_SW# (pin 28.29) and PWRSW_SIO# (pin 22). PU17's inputs are LIVE_ON_BATT (pin 23) and ACAV_IN (pin 23.37,38). The circuit includes several resistors (PR188, PR189, PC162, PC163, PC167, PC168) and capacitors (PD48) for signal conditioning and timing.





Title			RUN POWER SW	
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will the library of
JABT1&JABT2 modify
same with DAYTONA.
April/8_Edison

EMI Solution no update
Edison July/2/2003

