ASUS CONFIDENTIAL

MODEL NAME : ***Elsa***

PCB NO : ***???***

ASUS P/N : ***???***

Lanai Discrete VGA nVidia NB8M Schematics Document

uFCPGA Mobile Merom
Intel Crestline-PM + ICH8M

2007-03-19

REV : 1.2(DELL: X02)

MB PCB

Part Number	Description
DA80004H0L	PCB 00B LA-3071P REV0 M/B

BOM NO. ???
PCB P/N: ???

<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007** SHEET **1** OF **69**	DESCRIPTION: ***Cover Page***	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : ***Terry Lin***

LANAI: DISCRETE

CLOCK
CK410M+LP
PG 21

POWER
- POWER CON. PG 59
- POWER SEQUENCE LOGIC PG 51
- POWER CHARGER PG 57
- POWER CONTROL SWITCH PG 49
- DISCHARGE PATH PG 49
  +3.3V_SUS/+5V_SUS/+3.3V_RUN
  +5V/+3.3V/+1.8V/+1.25_RUN

Merom
(478 Micro-FCPGA)
PG 7,8
(Symbol Rev.09)

XDP PG 52

POWER
- POWER I/O PG 55
  +1.5V_RUN/+1.05V_VCCP
- REGULATOR PG 58
  +VCC_GFX_CORE/+1.25V_RUN
- POWER VCORE PG 53
- POWER SYSTEM PG 54
  5V_ALW & 3.3V_ALW
- REGULATOR PG 56
  +1.8V_SUS/+0.9V_DDR_VTT

Panel Connector PG 28 — LVDS — **nVIDIA G86M**
PCI EXPRESS GFX
PG 22,23,24,25,26,27

PCIEx16 — **Crestline**
1299 uFCBGA
PG 9,10,11,12,13,14
(Symbol Rev.09)

533/667 MHZ DDR II — **DDR2-SODIMM1** PG 19
533/667 MHZ DDR II — **DDR2-SODIMM2** PG 19

IO Board
- CRT CONN. — VGA
- TV CONN. — TVOUT
- USB CONN.x2 — USB2.0(P2,3)
- MINI-CARD WLAN — PCIEx1 (Lane2)
- MINI-CARD WWAN — USB2.0(P9)

→ **D.B CON** PG 50 (VGA, TVOUT)

MINI-CARD WWAN → **SIM CARD** — SIM CARD Board

DMI INTERFACE

ICH8-M
676 BGA
PG 15,16,17,18
(Symbol Rev.09)

- USB2.0(P0,P1) → **USB CONN.** PG 39 — USB Board
- USB2.0(P2,3) (from D.B CON)
- PCIEx1 (Lane2) (from D.B CON)
- USB2.0(P9) (from D.B CON)
- PCIE (Lane6) → **BCM5906KMLG** QFN-68 PG 47 → **RJ45/Magnetic** PG 48
- PCI → **CARD READER 1394/R5C833** PG 32,33,34
- PCIE (Lane4) → **EXPRESS-CARD R5538** PG 35
- USB2.0(P6)
- USB2.0(P7) → **Bluetooth** PG 41
- USB2.0(P5) → **CAMERA** PG 28
- SATA → **SATA-HDD** PG 31
- IDE → **CD-ROM** PG 31
- IHDA → **AUDIO/AMP** PG 44,45,46 and **MDC** PG 36
- SPI, LPC → **SIO** MEC5025 128KB Flash TMKBC, 128 Pins VTQFP, PG 37
- BC → **SIO** ECE5011 Expander USB 2.0 Hub(4), 128 Pins VTQFP, PG 38

AUDIO/AMP:
- S/PDIF TO TV CONN. PG 30
- DIGITAL MIC. PG 28
- Speaker CON PG 46
- WtoB CON PG 46

MDC → **RJ11** — RJ11 Board

Audio Jacks *3 — JACK Board

SIO MEC5025 (SPI, PS/2):
- CIR PG 41
- FLASH PG 40
- Touchpad CON. PG 41
- FAN &THERMAL EMC4001 PG 43
- USER INTERFACE PG 42
- SNIFFER PG 42
- CAPBTN CON. PG 40

<Variant Name>

PROJECT: Lanai	REVISION: 1.2	DATE: Monday, March 19, 2007	SHEET 2 OF 69	DESCRIPTION: BLOCK DIAGRAM	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : STANLY_HSU

INDEX

Pg#	Description	DNI LIST
01	Cover Page	
02	Schematic Block Diagram	
03	INDEX	
04	Bus connection	
05	SMBUS BLOCK	
06	Power Rail	
07-08	CPU (Merom 、 Penryn)	
09-14	Crestline	
15-18	ICH8M	
19-20	DDRII SO-DIMM(533MHz 、 667MHz)	
21	Clock Generator (CK410M+LP)	
22-27	VGA (nVIADA - G86M & GDDR3)	
28	LVDS CON & Camera & DMIC	
29	RGB CON	
30	TV OUT CON	
31	SATA(HDD & CD_ROM)	
32-34	MEDIA CARD READER / 1394 (R5C833)	
35	PCI-Express Card	
36	MDC CONN	
37	EC (MEC5025)	
38	SIO (ECE5011)	
39	USB PORT x 2	
40	FLASH & RTC & CAPBTN CONN	
41	TOUCH PAD & BT & CIR & LID	
42	SWITCH & LED	
43	HARDWARE MONITOR (EMC4001)	
44-46	AUDIO CODEC & AMP	
47	LOM BCM5906	
48	Magnetics and RJ-45	
49	Power Control Switch	
50	BtoB CON	
51	Power Sequence Logic	
52	XDP	
53-59	Power Circuit	
60	SCREW PAD	
61	Change list (1)	
62	Change list (2)	
63	Change list (3)	

Pg#	Description	DNI LIST
64	Power circuit Change list	
R01	Modem board cover page	
R02	RJ-11 CONN	
R03	Modem board Change list	
U01	USB board cover page	
U02	USB PORT (SINGLE * 2)	

<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***INDEX***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Terry_Lin***
		SHEET **3** OF **69**		RELEASE DATE :	

Footprint Definition

Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

Layout Note

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

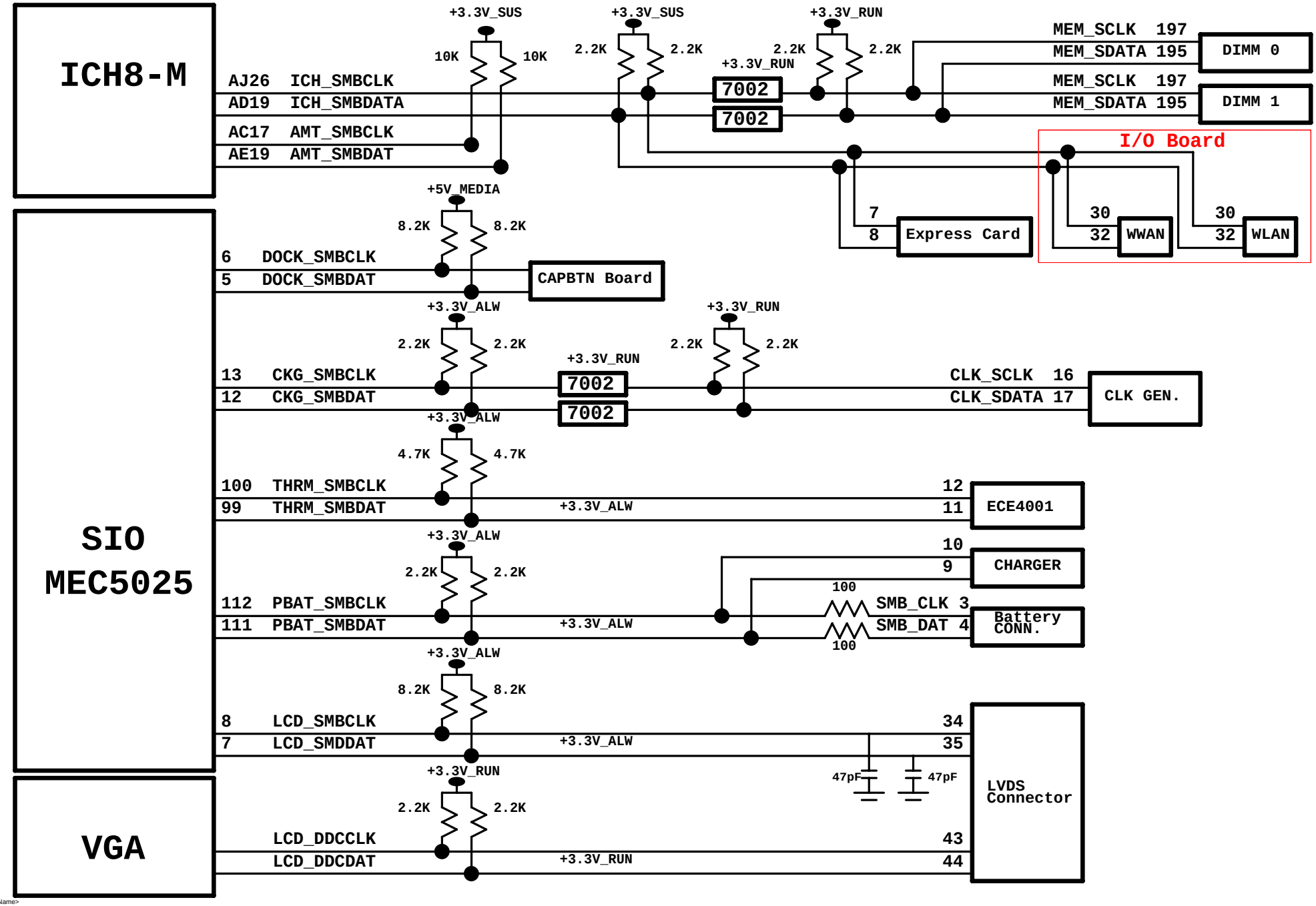
PCI Express TABLE

Lane 1	WWAN / Mini Card
Lane 2	WLAN / Mini Card
Lane 3	
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5906KMLG

USB TABLE

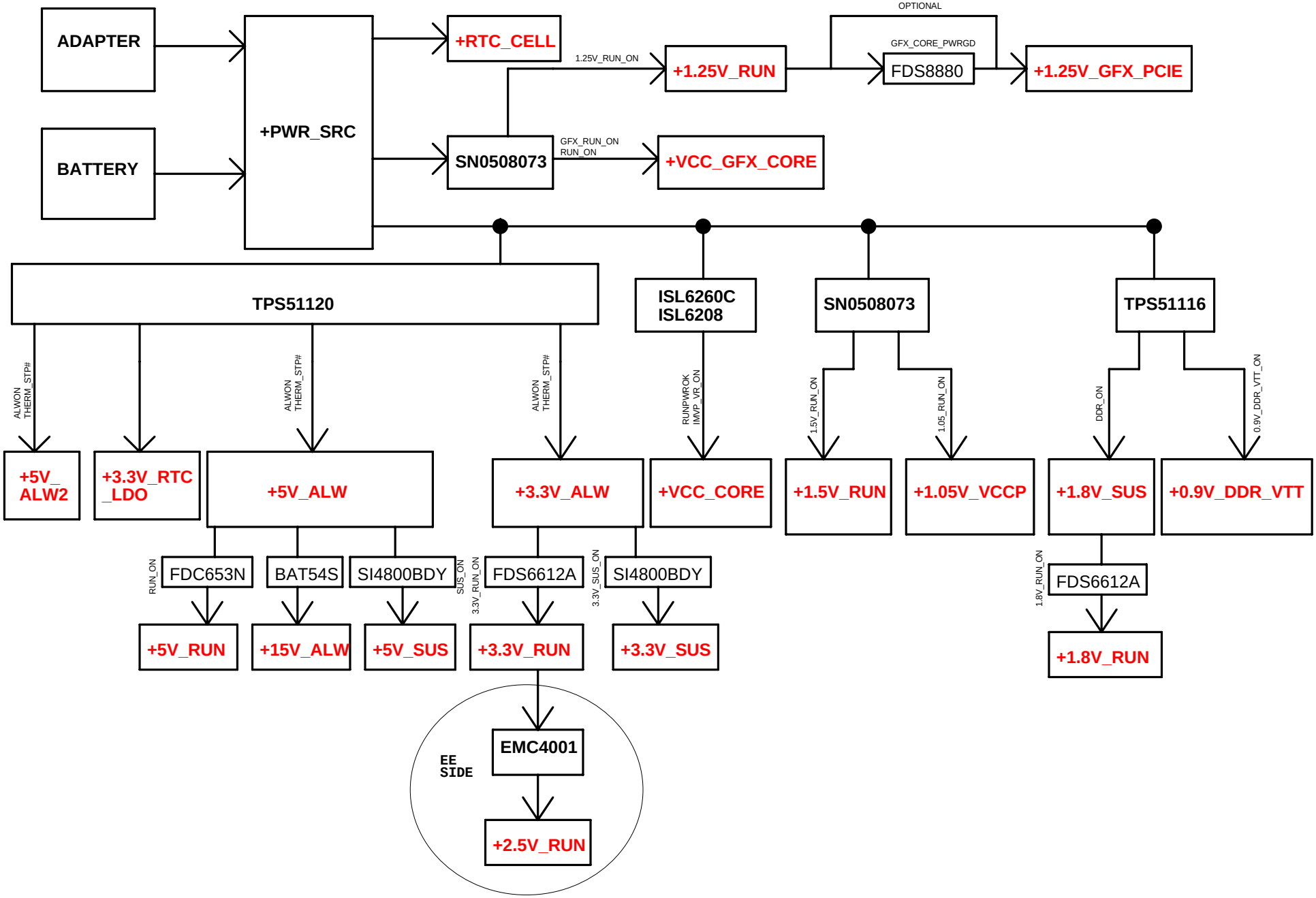
ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	User2 (Single port , in USB BD)
ICH8-2 (EHCI#1)	User3 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User4 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	
ICH8-5 (EHCI#1)	Camera
ICH8-6 (EHCI#2)	ExpressCard
ICH8-7 (EHCI#2)	BT Module
ICH8-8 (EHCI#2)	
ICH8-9 (EHCI#2)	WWAN / Mini Card

Note : No USB for WLAN



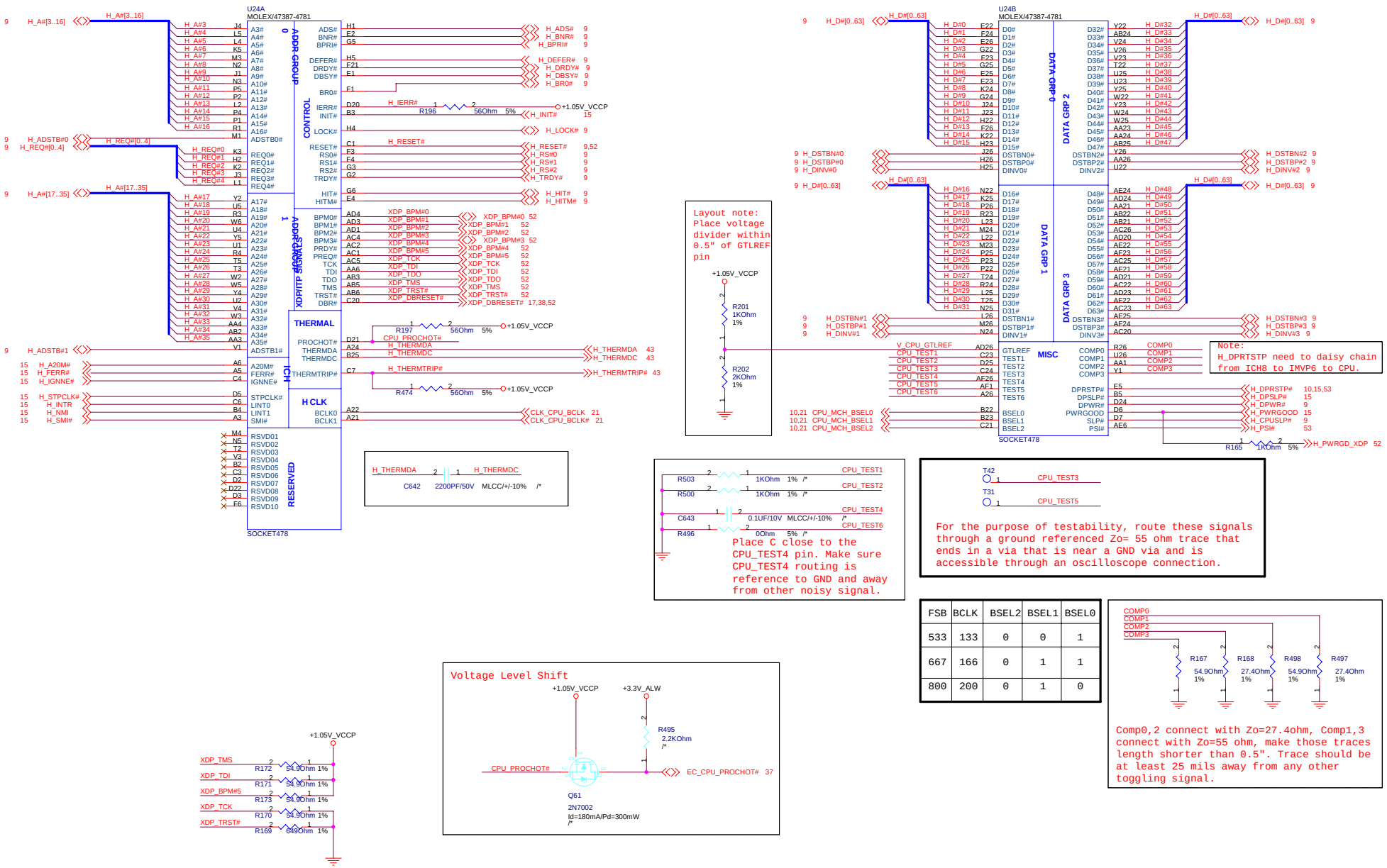
<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: SMBUS BLOCK	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Terry_Lin
		SHEET 5 OF 69		RELEASE DATE :	



<Variant Name>

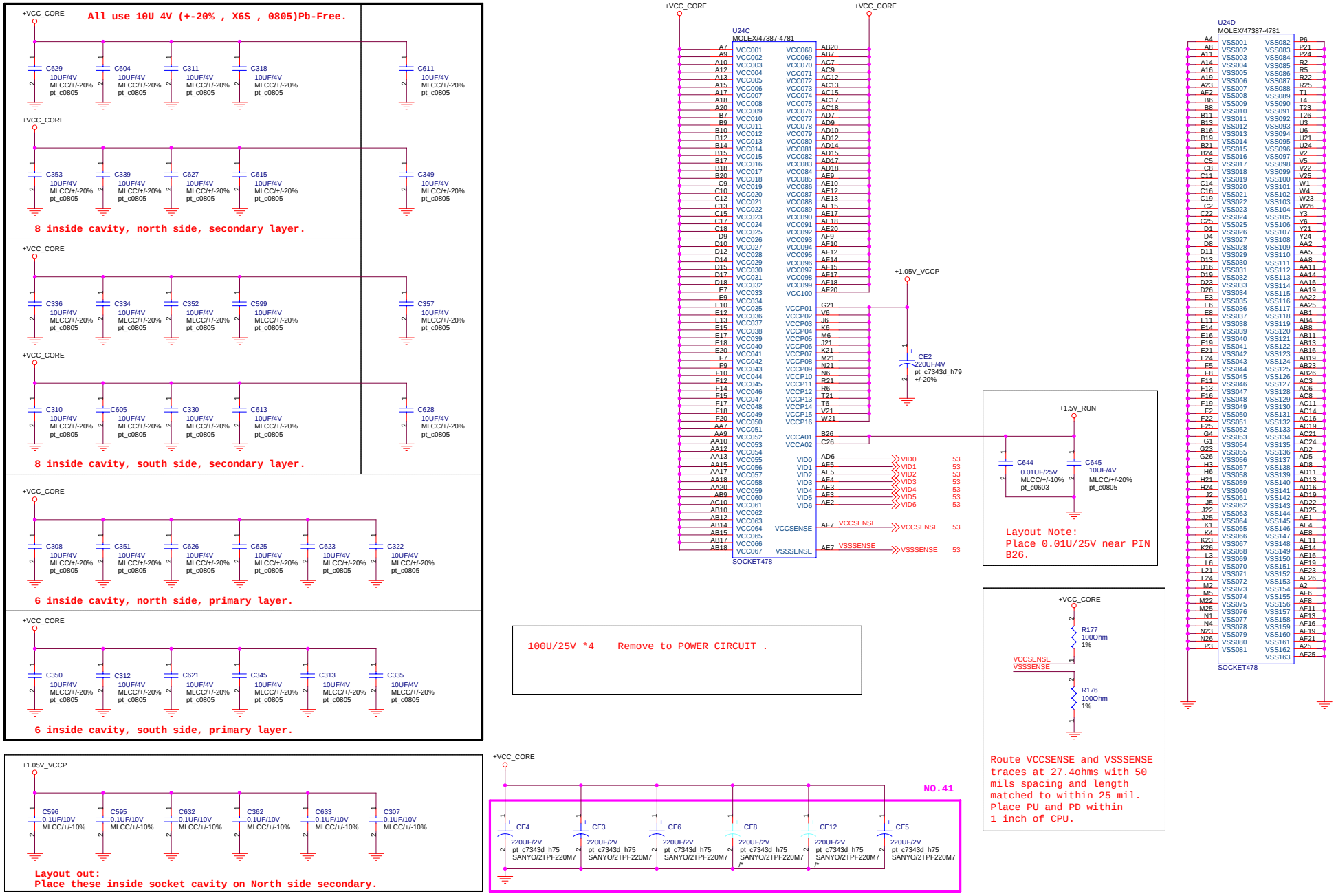
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Power Rail	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Eric_Ko
		SHEET 6 OF 69		RELEASE DATE :	



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

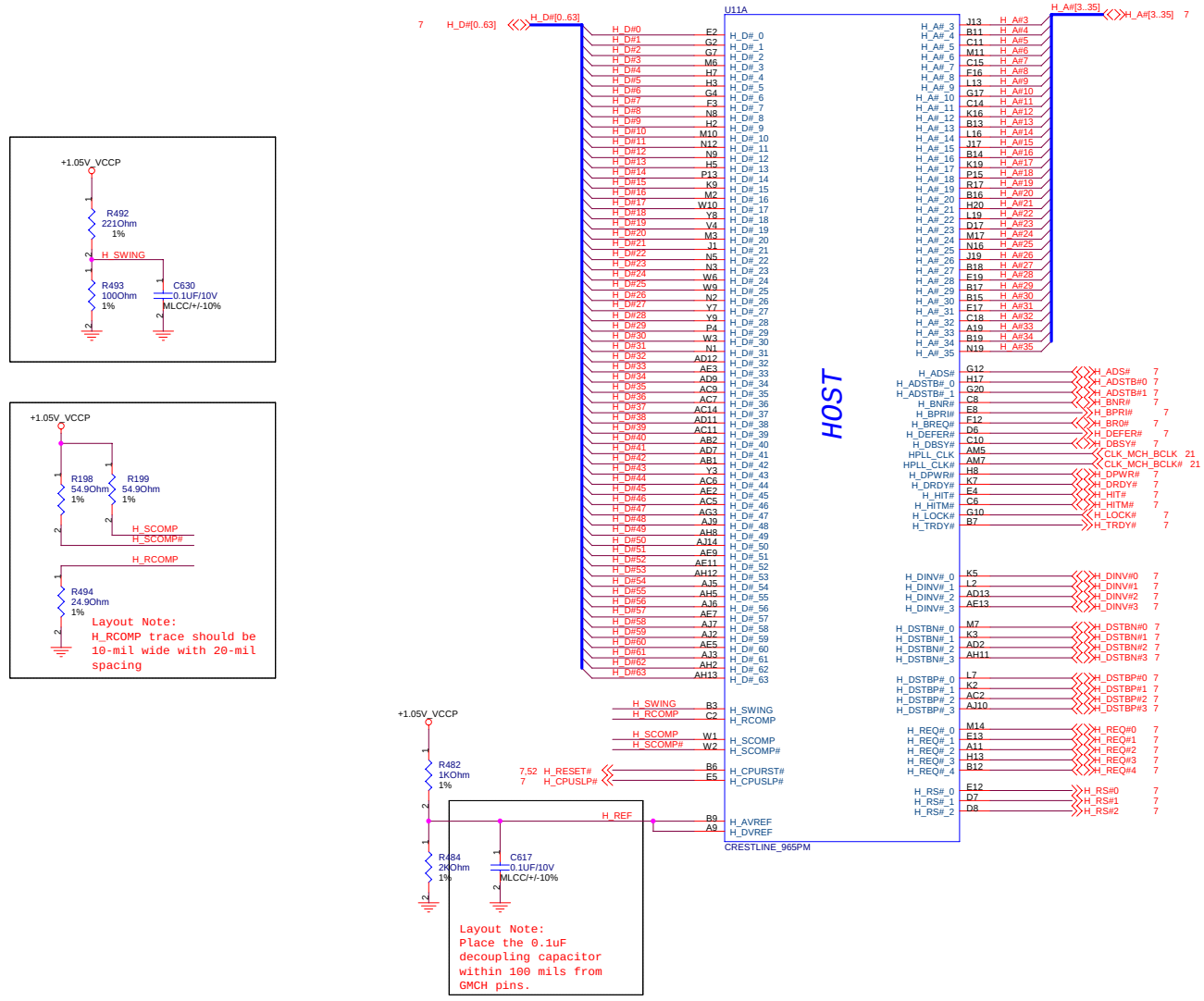
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***MEROM CPU (1)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Terry_Lin***
		SHEET 7 OF 69		RELEASE DATE :	



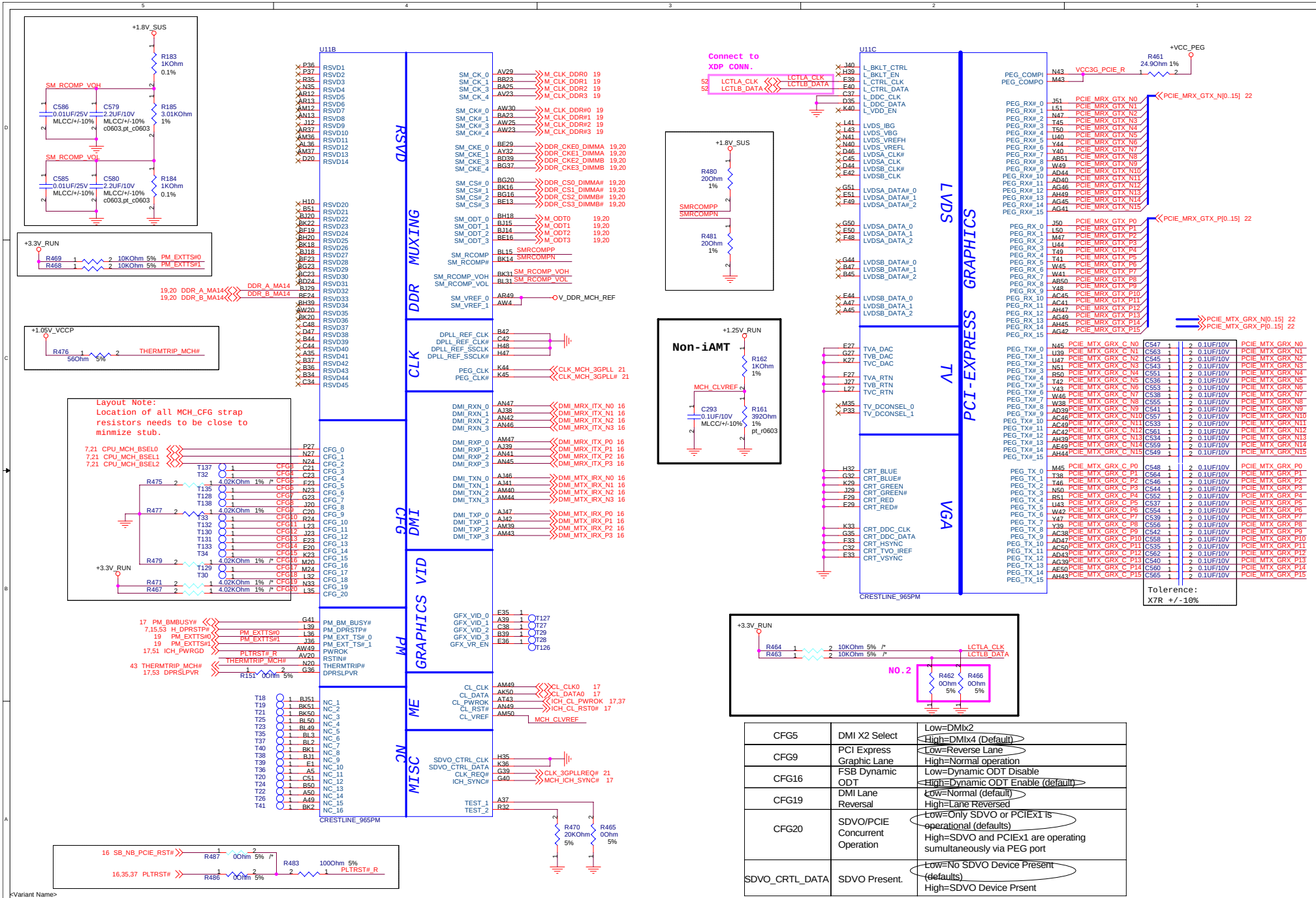
<Variant Name>

PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Merom CPU (2)*	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: *Terry_Lin*	
		SHEET 8 OF 69		RELEASE DATE:		



<Variant Name>

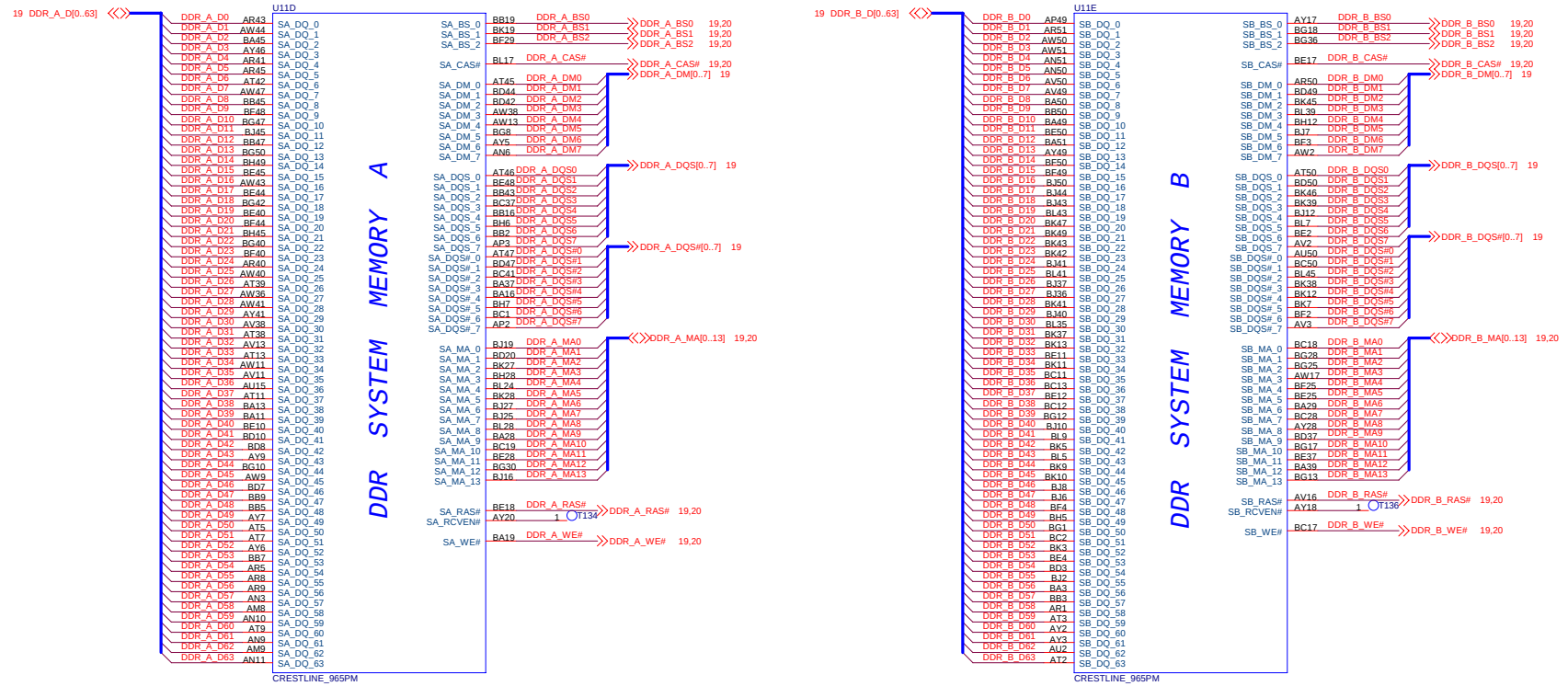
PROJECT: **Lanai**	REVISION: **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***Crestline(HOST)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Ivan_Chou***
		SHEET **9** OF **69**		RELEASE DATE :	



CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4 (Default)
CFG9	PCI Express Graphic Lane	Low=Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable (default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating sumultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present.	Low=No SDVO Device Present (defaults) High=SDVO Device Prsent

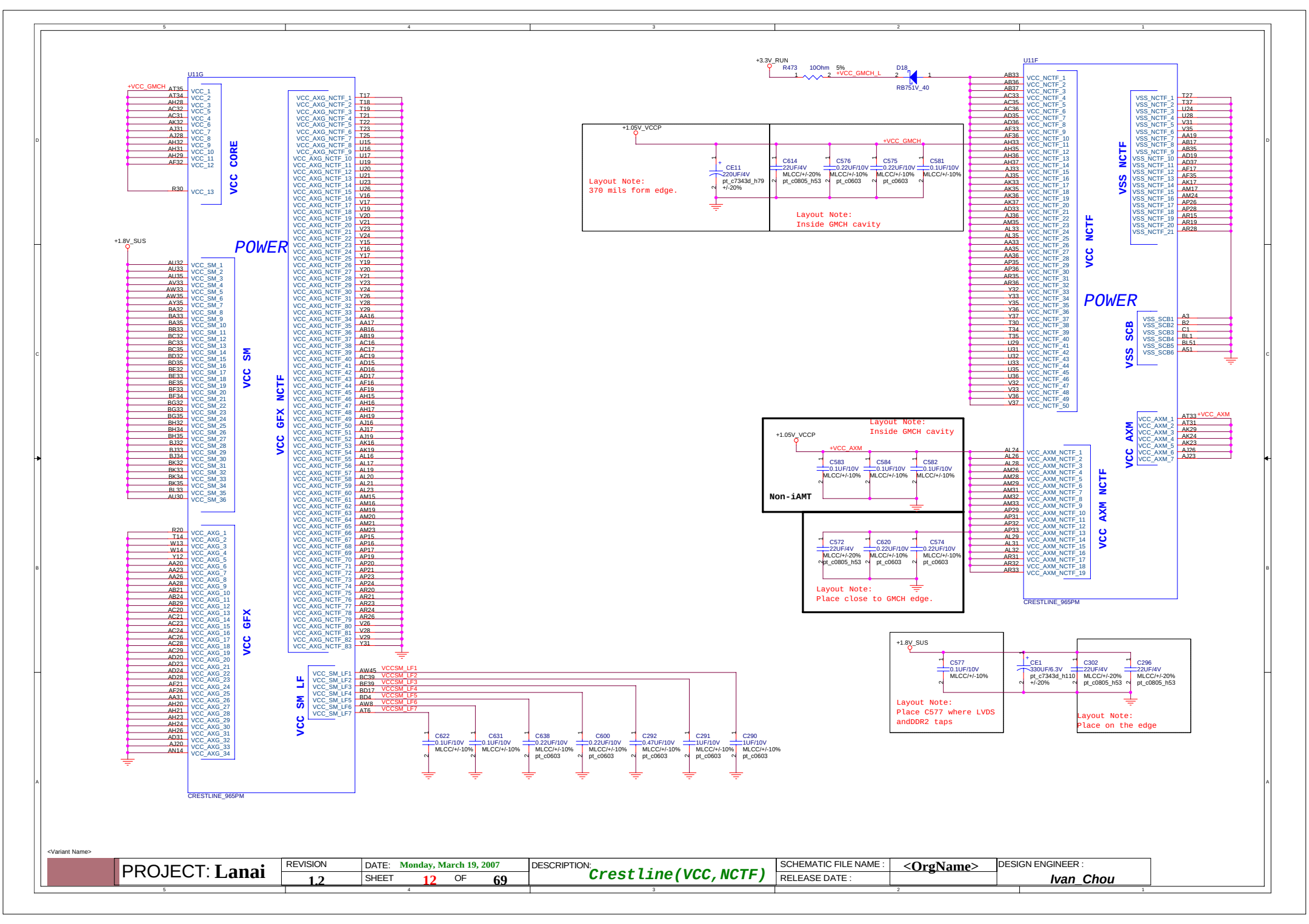
<Variant Name>

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Crestline(VGA,DMI)*	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER : *Ivan_Chou*
		SHEET 10 OF 69		RELEASE DATE :		



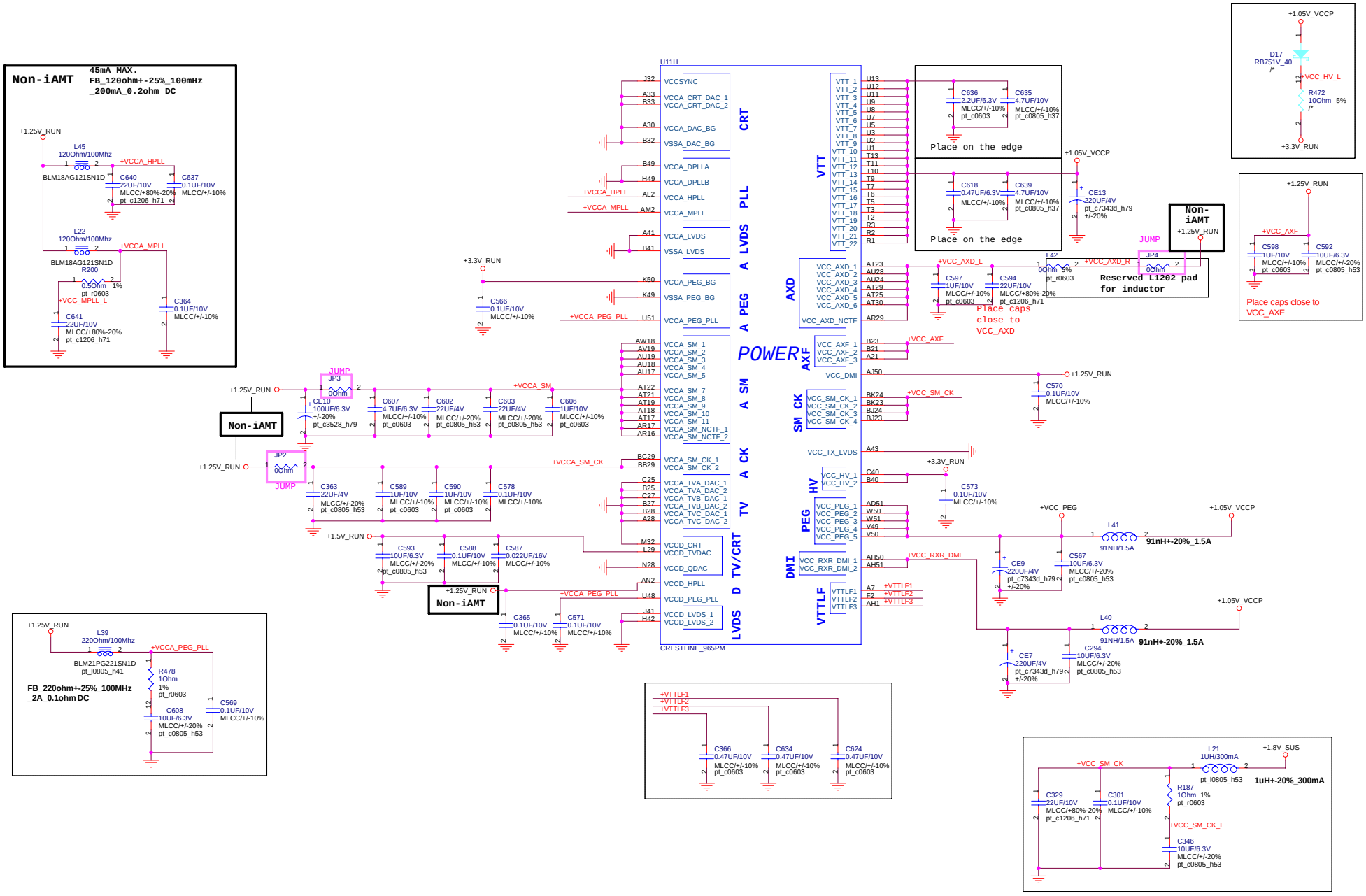
<Variant Name>

PROJECT: **Lanai**	REVISION: **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***Crestline(DDR2)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Ivan_Chou***
		SHEET **11** OF **69**		RELEASE DATE :	



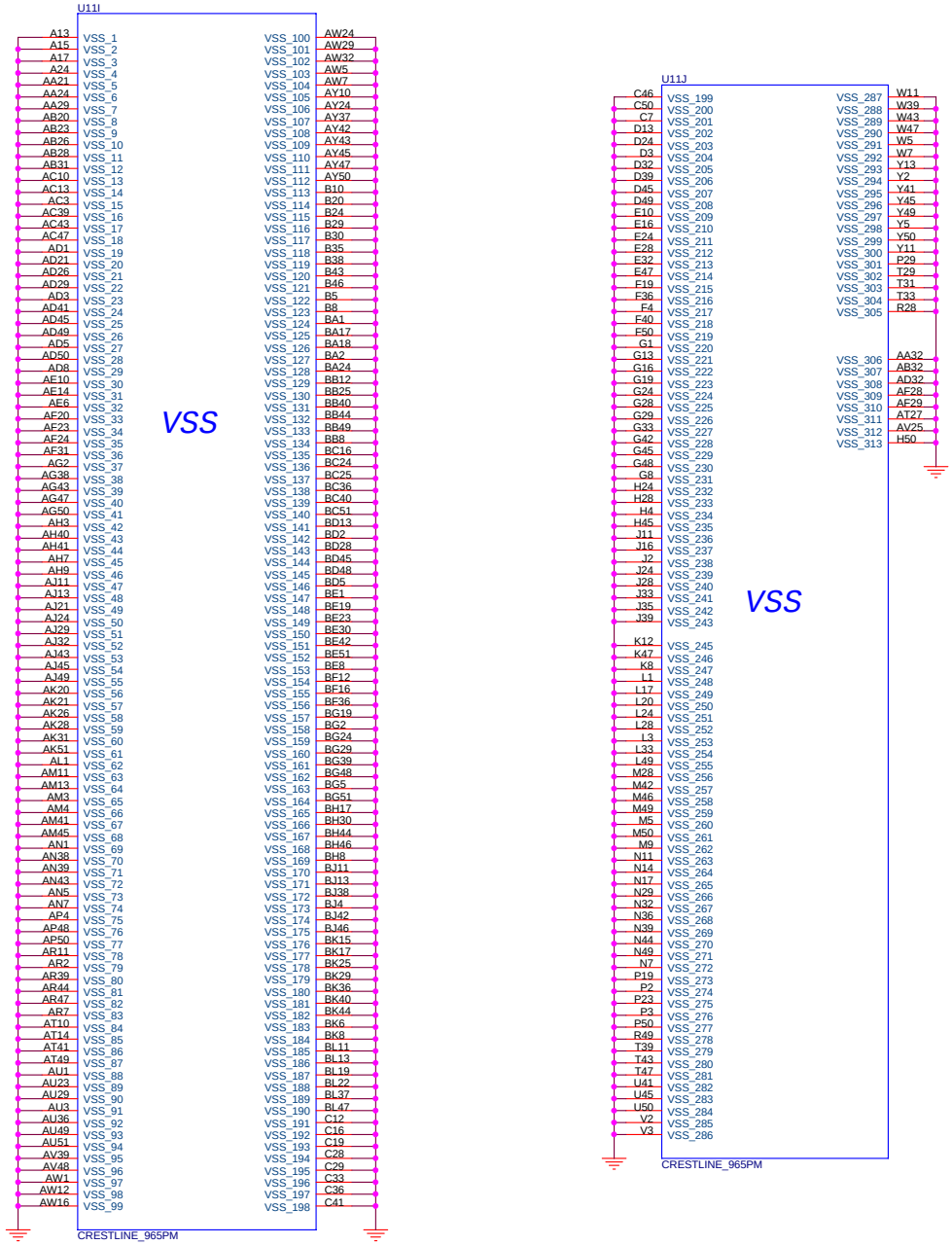
<Variant Name>

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Crestline(VCC,NCTF)*	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : *Ivan_Chou*
		SHEET 12 OF 69		RELEASE DATE :	



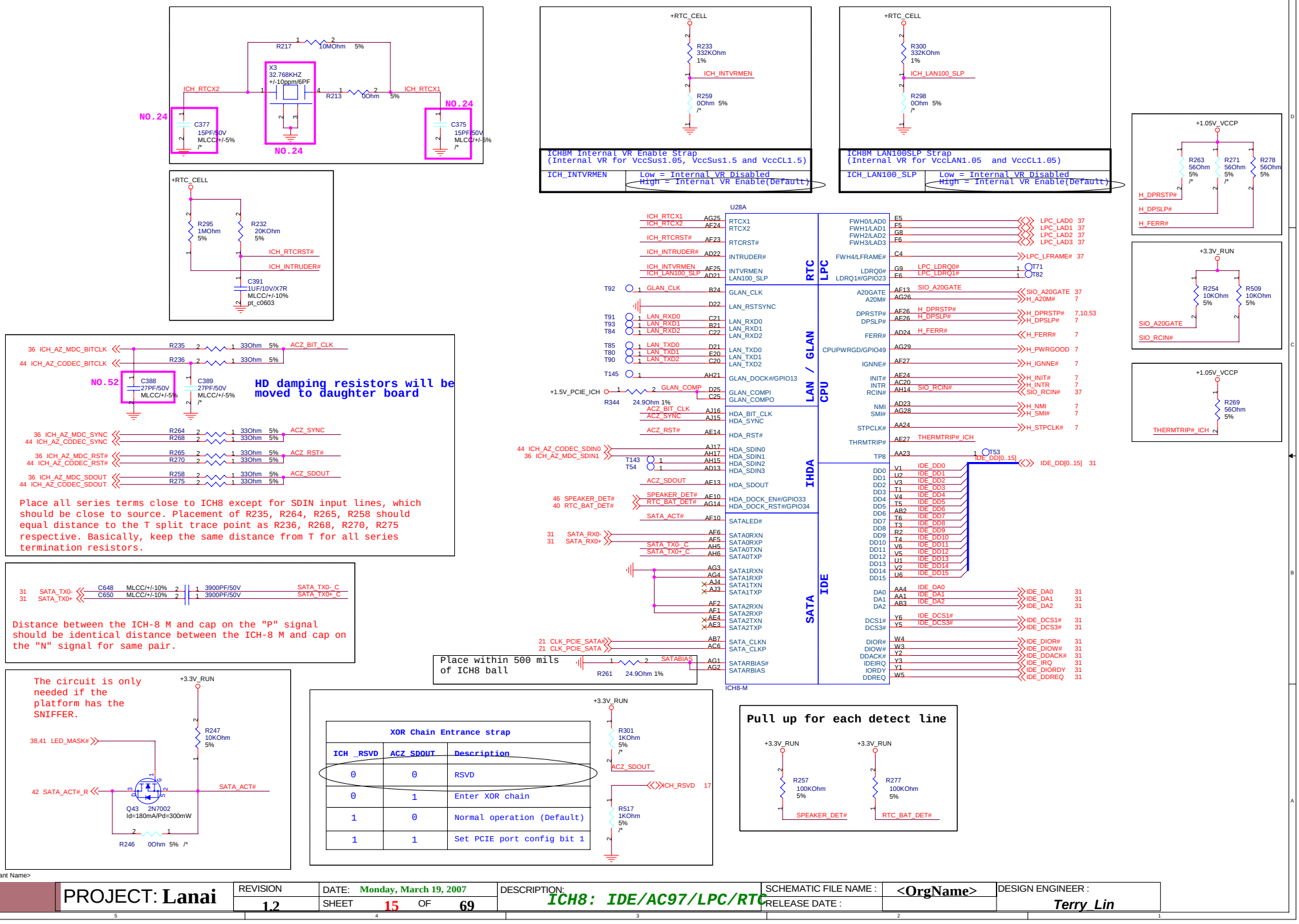
<Variant Name>

PROJECT: **Lanai**	REVISION: **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***Crestline(POWER)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Ivan_Chou***
		SHEET **13** OF **69**		RELEASE DATE :	



<Variant Name>

PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 14 OF 69	Crestline(VSS)	RELEASE DATE :		Ivan_Chou



<Variant Name>

PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *ICH8: IDE/AC97/LPC/RTC*	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: *Terry_Lin*
		SHEET 15 OF 69		RELEASE DATE:	

Place TX DC blocking caps close ICH8.

50 PCIE_TX1- C434 0.1UF/10V MLCC/+/-10% PCIE_TXN1_C
50 PCIE_TX1+ C436 0.1UF/10V MLCC/+/-10% PCIE_TXP1_C
50 PCIE_TX2- C443 0.1UF/10V MLCC/+/-10% PCIE_TXN2_C
50 PCIE_TX2+ C439 0.1UF/10V MLCC/+/-10% PCIE_TXP2_C
35 PCIE_TX4- C458 0.1UF/10V MLCC/+/-10% PCIE_TXN4_C
35 PCIE_TX4+ C461 0.1UF/10V MLCC/+/-10% PCIE_TXP4_C
47 PCIE_TX6-/GLAN_TX- C714 0.1UF/10V MLCC/+/-10% GLAN_TXN_C
47 PCIE_TX6+/GLAN_TX+ C713 0.1UF/10V MLCC/+/-10% GLAN_TXP_C

U28D

50 PCIE_RX1- P27 PERN1
50 PCIE_RX1+ P26 PERP1
PCIE_TXN1_C N29 PETN1
PCIE_TXP1_C N28 PETP1
MiniWWAN

50 PCIE_RX2- M27 PERN2
50 PCIE_RX2+ M26 PERP2
PCIE_TXN2_C L29 PETN2
PCIE_TXP2_C L28 PETP2
MiniWWAN

K27 PERN3
K26 PERP3
J29 PETN3
J28 PETP3

35 PCIE_RX4- H27 PERN4
35 PCIE_RX4+ H26 PERP4
PCIE_TXN4_C G29 PETN4
PCIE_TXP4_C G28 PETP4
ExpressCard

F27 PERN5
F26 PERP5
E29 PETN5
E28 PETP5

47 PCIE_RX6-/GLAN_RX- D27 PERN6/GLAN_RXN
47 PCIE_RX6+/GLAN_RX+ D26 PERP6/GLAN_RXP
GLAN_TXN_C C29 PETN6/GLAN_TXN
GLAN_TXP_C C28 PETP6/GLAN_TXP

PCI-Express Direct Media Interface

DMI0RXN V27 DMI_MTX_IRX_N0 10
DMI0RXP V26 DMI_MTX_IRX_P0 10
DMI0TXN U29 DMI_MRX_ITX_N0 10
DMI0TXP U28 DMI_MRX_ITX_P0 10

DMI1RXN Y27 DMI_MTX_IRX_N1 10
DMI1RXP Y26 DMI_MTX_IRX_P1 10
DMI1TXN W29 DMI_MRX_ITX_N1 10
DMI1TXP W28 DMI_MRX_ITX_P1 10

DMI2RXN AB26 DMI_MTX_IRX_N2 10
DMI2RXP AB25 DMI_MTX_IRX_P2 10
DMI2TXN AA29 DMI_MRX_ITX_N2 10
DMI2TXP AA28 DMI_MRX_ITX_P2 10

DMI3RXN AD27 DMI_MTX_IRX_N3 10
DMI3RXP AD26 DMI_MTX_IRX_P3 10
DMI3TXN AC29 DMI_MRX_ITX_N3 10
DMI3TXP AC28 DMI_MRX_ITX_P3 10

DMI_CLKN T26 CLK_PCIE_ICH# 21
DMI_CLKP T25 CLK_PCIE_ICH 21

DMI_ZCOMP Y23
DMI_IRCOMP Y24
DMI_COMP R286 24.9Ohm 1% +1.5V_PCIE_ICH

Place within 500 mils of ICH8

BIOS should not enable the internal GPIO pull up resistor

+3.3V_RUN
SB_NB_PCIE_RST# R338 10KOhm 5%
SB_WLAN_PCIE_RST# R147 10KOhm 5%
SB_NB_PCIE_RST# R491 100KOhm 5%
SB_WLAN_PCIE_RST# R334 100KOhm 5%
SB_LOM_PCIE_RST# R354 20KOhm 5%
SB_WWAN_PCIE_RST# R356 20KOhm 5%

Layout Note:
Place 15 ohm within 500 mils from ICH.

37 ICH_EC_SPI_CLK R353 15Ohm 5% ICH_EC_SPI_CLK_R C23 ICH_SPI_CS#
T78 B23 ICH_SPI_CS1#_R E22
37 ICH_EC_SPI_DO R343 15Ohm 5% ICH_EC_SPI_DO_R D23 SPI_MOSI
37 ICH_EC_SPI_DIN F21 SPI_MISO
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI

USB

39 USB_OC0_1# USB_OC0_1# A19 OC0#
50 USB_OC2_3# USB_OC2_3# AG16 OC1#/GPIO40
AG15 OC2#/GPIO41
AE15 OC3#/GPIO42
AE15 OC4#/GPIO43
AG17 OC5#/GPIO29
AD12 OC6#/GPIO30
AJ18 OC7#/GPIO31
AD14 OC8#
AH18 OC9#

USBP0N G3 ICH_USBP0- 39 USER1 Left side pair top/left
USBP0P G2 ICH_USBP0+ 39
USBP1N H5 ICH_USBP1- 39 USER2 Left side pair bottom/right
USBP1P H4 ICH_USBP1+ 39
USBP2N H2 ICH_USBP2- 50 USER3 Right side pair top/left
USBP2P H1 ICH_USBP2+ 50
USBP3N J3 ICH_USBP3- 50 USER3 Right side pair bottom/right
USBP3P J2 ICH_USBP3+ 50
USBP4N K5 ICH_USBP4- T63
USBP4P K4 ICH_USBP4+ T68
USBP5N K2 ICH_USBP5- 28 CCD
USBP5P K1 ICH_USBP5+ 28
USBP6N L3 ICH_USBP6- 35 Express Card
USBP6P L2 ICH_USBP6+ 35
USBP7N M5 ICH_USBP7- 41 BlueTooth NO.5
USBP7P M4 ICH_USBP7+ 41
USBP8N M2 ICH_USBP8- T59
USBP8P M1 ICH_USBP8+ T62
USBP9N N3 ICH_USBP9- 50 WWAN
USBP9P N2 ICH_USBP9+ 50

USBRBIAS# F2
USBRBIAS F3 USBRBIAS

ICH8-M

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

R561 22.6Ohm 1% pt_r0603

+3.3V_ALW
U33
SPI_CS0# R595 15Ohm 5% /*
ICH_SPI_CS#_R R596 15Ohm 5% ICH_SPI_CS#
SIO_SPI_CS# 37
74AHC1G08GW /*
R594 0Ohm 5%

PCI Pullups

PCI_STOP# R350 8.2KOhm 5% +3.3V_RUN
PCIE_MCARD2_DET# R613 100KOhm 5% +3.3V_RUN NO.13
PCI_DEVSEL# RP4E 8.2KOhm 5% +3.3V_RUN
PCI_FRAME# RP4F 8.2KOhm 5% RP4D PCI_REQ1# 8.2KOhm 5%
ICH_GPIO2_PIRQE# RP4G 8.2KOhm 5% RP4C PCI_PIRQD# 8.2KOhm 5%
PCI_SERR# RP4H 8.2KOhm 5% RP4B 8.2KOhm 5%
RP4A PCI_TRDY# 8.2KOhm 5%
RP3E 8.2KOhm 5% +3.3V_RUN
PCI_REQ0# RP3F 8.2KOhm 5% RP3D PCI_PIRQC# 8.2KOhm 5%
PCI_PLOCK# RP3G 8.2KOhm 5% RP3C PCI_PIRQB# 8.2KOhm 5%
PCI_PERR# RP3H 8.2KOhm 5% RP3B PCI_PIRQA# 8.2KOhm 5%
RP3A PCI_IRDY# 8.2KOhm 5%

Non-iAMT

+3.3V_SUS
OC4# RP1E 10KOhm 5%
OC7# RP1F 10KOhm 5% RP1D USB_OC2_3# 10KOhm 5%
OC6# RP1G 10KOhm 5% RP1C OC8# 10KOhm 5%
OC9# RP1H 10KOhm 5% RP1B OC5# 10KOhm 5%
RP1A USB_OC0_1# 10KOhm 5%

ICH_SPI_CS1#_R
PCI_GNT0#
R347 1KOhm 5%
R337 1KOhm 5% /*

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

PCI_GNT3#
R346 1KOhm 5% /*

A16 away override strap.

PCI_GNT3#	Low = A16 swap override enabled.
	High = Default.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

+3.3V_SUS
C689 0.047UF/10V MLCC/+/-10%
U30 SN74AHC1G32DBVR
PCI_RST#_G PCI_RST# 32
C382 0.047UF/10V MLCC/+/-10%
U14 SN74AHC1G32DBVR
PCI_PLTRST# PLTRST# 10,35,37
NO.36
C747 0.047UF/10V MLCC/+/-10%
U37 SN74AHC1G32DBVR
PCI_PLTRST# PLTRST_LAN_MINICARD# 47,50
C758 47PF/50V MLCC/+/-5%
NO.51

32 PCI_AD[0..31]

U28B

PCI_AD0 D20 AD0
PCI_AD1 E19 AD1
PCI_AD2 D19 AD2
PCI_AD3 A20 AD3
PCI_AD4 D17 AD4
PCI_AD5 A21 AD5
PCI_AD6 A19 AD6
PCI_AD7 C19 AD7
PCI_AD8 A18 AD8
PCI_AD9 B16 AD9
PCI_AD10 A12 AD10
PCI_AD11 E16 AD11
PCI_AD12 A14 AD12
PCI_AD13 G16 AD13
PCI_AD14 A15 AD14
PCI_AD15 B6 AD15
PCI_AD16 C11 AD16
PCI_AD17 A9 AD17
PCI_AD18 D11 AD18
PCI_AD19 B12 AD19
PCI_AD20 C12 AD20
PCI_AD21 D10 AD21
PCI_AD22 C7 AD22
PCI_AD23 F13 AD23
PCI_AD24 E11 AD24
PCI_AD25 E13 AD25
PCI_AD26 E12 AD26
PCI_AD27 D8 AD27
PCI_AD28 A6 AD28
PCI_AD29 E8 AD29
PCI_AD30 D6 AD30
PCI_AD31 A3 AD31

PCI

A4 REQ0# PCI_REQ0#
D7 GNT0# PCI_GNT0#
E18 REQ1#/GPIO50 PCI_REQ1# PCI_REQ1# 32
C18 GNT1#/GPIO51 PCI_GNT1# PCI_GNT1# 32
B19 REQ2#/GPIO52 SB_WWAN_PCIE_RST# SB_WWAN_PCIE_RST# 50 T77
F18 GNT2#/GPIO53 PCI_GNT2#
A11 REQ3#/GPIO54 SB_LOM_PCIE_RST# SB_LOM_PCIE_RST# 47 T89
C10 GNT3#/GPIO55 PCI_GNT3#

C17 C/BE0# PCI_C_BE0# 32
E15 C/BE1# PCI_C_BE1# 32
F16 C/BE2# PCI_C_BE2# 32
E17 C/BE3# PCI_C_BE3# 32

C8 IRDY# PCI_IRDY# PCI_IRDY# 32
D9 PAR PCI_PAR 32
G6 PCIRST# PCI_RST#_G
D16 DEVSEL# PCI_DEVSEL# PCI_DEVSEL# 32
A7 PERR# PCI_PERR# PCI_PERR# 32
B7 PLOCK# PCI_PLOCK#
F10 SERR# PCI_SERR# PCI_SERR# 32
C16 STOP# PCI_STOP# PCI_STOP# 32
C9 TRDY# PCI_TRDY# PCI_TRDY# 32
A17 FRAME# PCI_FRAME# PCI_FRAME# 32

AG24 PLTRST# PCI_PLTRST#
B10 PCICLK CLK_PCI_ICH CLK_PCI_ICH 21
G7 PME# ICH_PME# 38

Interrupt I/F

T95 F9 PIRQA# PCI_PIRQA#
PCI_PIRQB# B5 PIRQB# PCI_PIRQB#
32 PCI_PIRQC# C5 PIRQC# PCI_PIRQC#
32 PCI_PIRQD# A10 PIRQD# PCI_PIRQD#

F8 PIRQE#/GPIO2 ICH_GPIO2_PIRQE#
G11 PIRQF#/GPIO3 SB_WLAN_PCIE_RST# SB_WLAN_PCIE_RST# 50
F12 PIRQG#/GPIO4 SB_NB_PCIE_RST# SB_NB_PCIE_RST# 10
B3 PIRQH#/GPIO5 PCIE_MCARD2_DET# 50 NO.13

ICH8-M

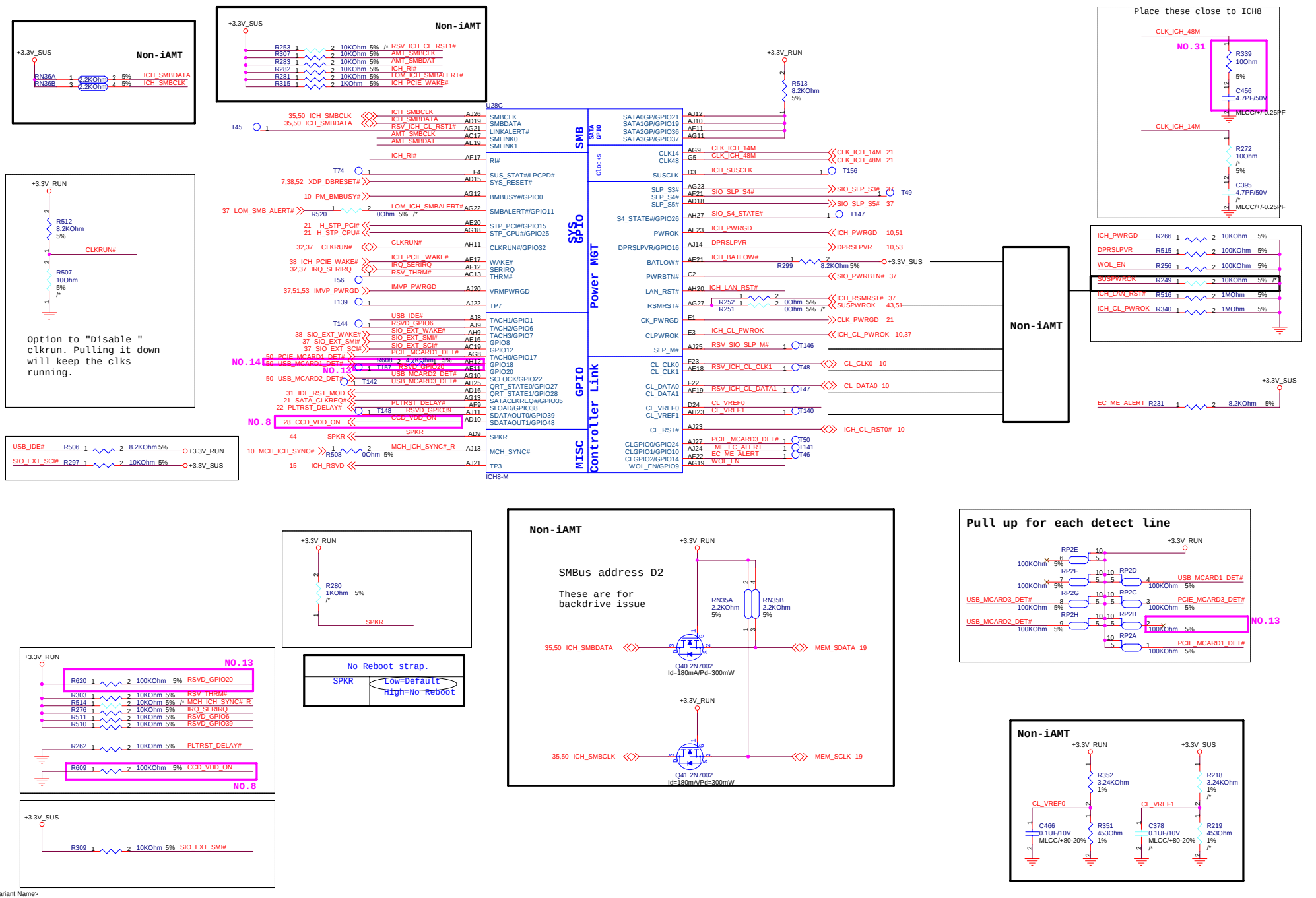
R5C833	REQ1 GNT1	PIRQC PIRQD

CLK_PCI_ICH
R355 10Ohm 5% /*
C475 8.2PF/50V MLCC/+/-0.25PF /*

Reserved for EMI. Place resister and cap close to ICH.

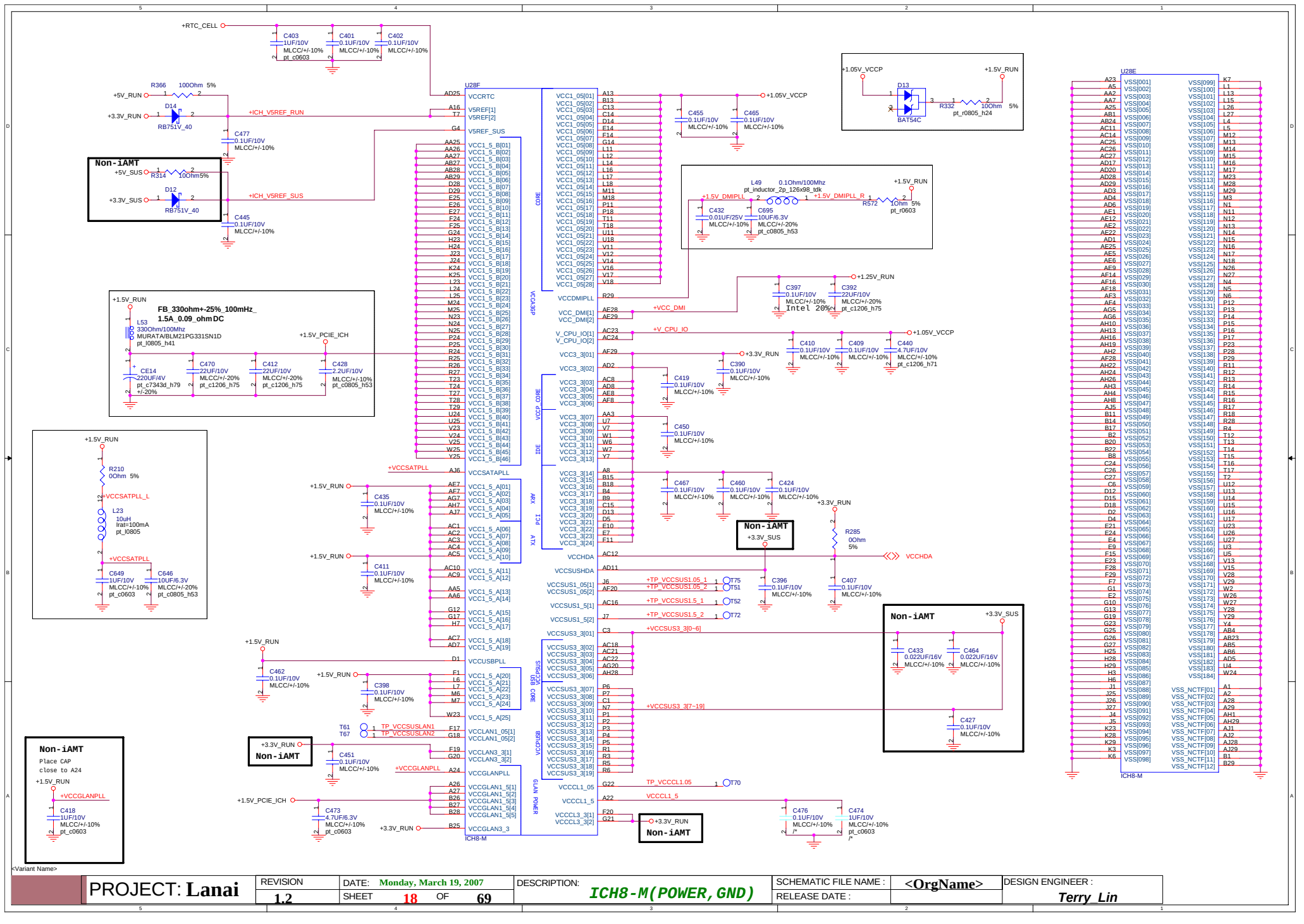
<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: ICH8: PCI/INT/DMI/USB	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Terry_Lin
		SHEET 16 OF 69		RELEASE DATE :	



<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***ICH8: SMB/PWR/CLK/GPIO***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Terry_Lin***
		SHEET **17** OF **69**		RELEASE DATE :	



PROJECT: **Lanai**	REVISION: **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***ICH8-M(POWER, GND)***	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: *Terry_Lin*
		SHEET 18 OF 69		RELEASE DATE:	

A is required to route to Top SODIMM for AMT to function Ch.A SODIMM needs to be populated for Intel AMT support.

TOP

+1.8V_SUS

V_DDR_MCH_REF

DDR_A_DM[0..7] 11
DDR_A_D[0..63] 11
DDR_A_DQS[0..7] 11
DDR_A_DQS#[0..7] 11
DDR_A_MA[0..14] 10,11,20

CON14

	1 VREF	VSS46 2	
DDR_A_D5	3 VSS47	DQ4 4	DDR_A_D4
DDR_A_D0	5 DQ0	DQ5 6	DDR_A_D6
	7 DQ1	VSS15 8	
DDR_A_DQS#0	9 VSS37	DM0 10	DDR_A_DM0
DDR_A_DQS0	11 DQS#0	VSS5 12	
	13 DQS0	DQ6 14	DDR_A_D2
DDR_A_D1	15 VSS48	DQ7 16	DDR_A_D7
DDR_A_D3	17 DQ2	VSS16 18	
	19 DQ3	DQ12 20	DDR_A_D8
DDR_A_D15	21 VSS38	DQ13 22	DDR_A_D12
DDR_A_D9	23 DQ8	VSS17 24	
	25 DQ9	DM1 26	DDR_A_DM1
DDR_A_DQS#1	27 VSS49	VSS53 28	
DDR_A_DQS1	29 DQS#1	CK0 30	M_CLK_DDR0 10
	31 DQS1	CK0# 32	M_CLK_DDR#0 10
DDR_A_D11	33 VSS39	VSS41 34	
DDR_A_D10	35 DQ10	DQ14 36	DDR_A_D14
	37 DQ11	DQ15 38	DDR_A_D13
	39 VSS50	VSS54 40	
	41 VSS18	VSS20 42	
DDR_A_D16	43 DQ16	DQ20 44	DDR_A_D17
DDR_A_D21	45 DQ17	DQ21 46	DDR_A_D20
	47 VSS1	VSS6 48	
DDR_A_DQS#2	49 DQS#2	NC3 50	PM_EXTTS#0 10
DDR_A_DQS2	51 DQS2	DM2 52	DDR_A_DM2
	53 VSS19	VSS21 54	
DDR_A_D19	55 DQ18	DQ22 56	DDR_A_D18
DDR_A_D22	57 DQ19	DQ23 58	DDR_A_D23
	59 VSS22	VSS24 60	
DDR_A_D25	61 DQ24	DQ28 62	DDR_A_D28
DDR_A_D27	63 DQ25	DQ29 64	DDR_A_D29
	65 VSS23	VSS25 66	
DDR_A_DM3	67 DM3	DQS#3 68	DDR_A_DQS#3
	69 NC4	DQS3 70	DDR_A_DQS3
	71 VSS9	VSS10 72	
DDR_A_D31	73 DQ26	DQ30 74	DDR_A_D30
DDR_A_D24	75 DQ27	DQ31 76	DDR_A_D26
	77 VSS4	VSS8 78	
10,20 DDR_CKE0_DIMMA	79 CKE0	CKE1 80	DDR_CKE1_DIMMA 10,20
	81 VDD7	VDD8 82	
	83 NC1	A15 84	DDR_A_MA14
11,20 DDR_A_BS2	85 A16_BA2	A14 86	
	87 VDD9	VDD11 88	DDR_A_MA11
DDR_A_MA12	89 A12	A11 90	DDR_A_MA7
DDR_A_MA9	91 A9	A7 92	DDR_A_MA6
DDR_A_MA8	93 A8	A6 94	
	95 VDD5	VDD4 96	
DDR_A_MA5	97 A5	A4 98	DDR_A_MA4
DDR_A_MA3	99 A3	A2 100	DDR_A_MA2
DDR_A_MA1	101 A1	A0 102	DDR_A_MA0
	103 VDD10	VDD12 104	
DDR_A_MA10	105 A10/AP	BA1 106	DDR_A_BS1 11,20
11,20 DDR_A_BS0 DDR_A_BS0	107 BA0	RAS# 108	DDR_A_RAS# 11,20
11,20 DDR_A_WE# DDR_A_WE#	109 WE#	S0# 110	DDR_CS0_DIMMA# 10,20
	111 VDD2	VDD1 112	
11,20 DDR_A_CAS# DDR_A_CAS#	113 CAS#	ODT0 114	M_ODT0 10,20
10,20 DDR_CS1_DIMMA#	115 S1#	A13 116	DDR_A_MA13
	117 VDD3	VDD6 118	
10,20 M_ODT1 M_ODT1	119 ODT1	NC2 120	
	121 VSS11	VSS12 122	
DDR_A_D36	123 DQ32	DQ36 124	DDR_A_D32
DDR_A_D33	125 DQ33	DQ37 126	DDR_A_D38
	127 VSS26	VSS28 128	
DDR_A_DQS#4	129 DQS#4	DM4 130	DDR_A_DM4
DDR_A_DQS4	131 DQS4	VSS42 132	
	133 VSS2	DQ38 134	DDR_A_D37
DDR_A_D39	135 DQ34	DQ39 136	DDR_A_D35
DDR_A_D34	137 DQ35	VSS55 138	
	139 VSS27	DQ44 140	DDR_A_D45
DDR_A_D40	141 DQ40	DQ45 142	DDR_A_D44
DDR_A_D47	143 DQ41	VSS43 144	
	145 VSS29	DQS#5 146	DDR_A_DQS#5
DDR_A_DM5	147 DM5	DQS5 148	DDR_A_DQS5
	149 VSS51	VSS56 150	
DDR_A_D42	151 DQ42	DQ46 152	DDR_A_D41
DDR_A_D43	153 DQ43	DQ47 154	DDR_A_D46
	155 VSS40	VSS44 156	
DDR_A_D48	157 DQ48	DQ52 158	DDR_A_D53
DDR_A_D49	159 DQ49	DQ53 160	DDR_A_D52
	161 VSS52	VSS57 162	
	163 NCTEST	CK1 164	M_CLK_DDR1 10
	165 VSS30	CK1# 166	M_CLK_DDR#1 10
DDR_A_DQS#6	167 DQS#6	VSS45 168	
DDR_A_DQS6	169 DQS6	DM6 170	DDR_A_DM6
	171 VSS31	VSS32 172	
DDR_A_D50	173 DQ50	DQ54 174	DDR_A_D51
DDR_A_D54	175 DQ51	DQ55 176	DDR_A_D55
	177 VSS33	VSS35 178	
DDR_A_D56	179 DQ56	DQ60 180	DDR_A_D58
DDR_A_D60	181 DQ57	DQ61 182	DDR_A_D57
	183 VSS3	VSS7 184	
DDR_A_DM7	185 DM7	DQS#7 186	DDR_A_DQS#7
	187 VSS34	DQS7 188	DDR_A_DQS7
DDR_A_D61	189 DQ58	VSS36 190	
DDR_A_D59	191 DQ59	DQ62 192	DDR_A_D63
	193 VSS14	DQ63 194	DDR_A_D62
MEM_SDATA 17	195 SDA	VSS13 196	
MEM_SCLK 17	197 SCL	SA0 198	
+3.3V_RUN	199 VDDSPD	SA1 200	
	201 GND0	GND1 202	
	203 NP_NC1NP_NC2	204	

STD FOXCONN/AS0A426-N2SN-7F

CLOCK 0 , 1
CKE 0 , 1

V_DDR_MCH_REF
C280 0.1UF/10V MLCC/+80-20%
C278 2.2UF/6.3V MLCC/+/-10%
pt_c0805_h53

R505 10KOhm 5%
R501 10KOhm 5%

+3.3V_RUN
Non-iAMT
C373 2.2UF/6.3V MLCC/+/-10%
C374 0.1UF/10V MLCC/+80-20%
pt_c0805_h53

Non-iAMT
SMbus address A0

BOT

+1.8V_SUS

V_DDR_MCH_REF

DDR_B_DM[0..7] 11
DDR_B_D[0..63] 11
DDR_B_DQS[0..7] 11
DDR_B_DQS#[0..7] 11
DDR_B_MA[0..14] 10,11,20

CON15

	1 VREF	VSS46 2	
DDR_B_D0	3 VSS47	DQ4 4	DDR_B_D5
DDR_B_D1	5 DQ0	DQ5 6	DDR_B_D4
	7 DQ1	VSS15 8	
DDR_B_DQS#0	9 VSS37	DM0 10	DDR_B_DM0
DDR_B_DQS0	11 DQS#0	VSS5 12	
	13 DQS0	DQ6 14	DDR_B_D6
DDR_B_D3	15 VSS48	DQ7 16	DDR_B_D7
DDR_B_D2	17 DQ2	VSS16 18	
	19 DQ3	DQ12 20	DDR_B_D8
DDR_B_D9	21 VSS38	DQ13 22	DDR_B_D12
DDR_B_D13	23 DQ8	VSS17 24	
	25 DQ9	DM1 26	DDR_B_DM1
DDR_B_DQS#1	27 VSS49	VSS53 28	
DDR_B_DQS1	29 DQS#1	CK0 30	M_CLK_DDR2 10
	31 DQS1	CK0# 32	M_CLK_DDR#2 10
DDR_B_D10	33 VSS39	VSS41 34	
DDR_B_D14	35 DQ10	DQ14 36	DDR_B_D11
	37 DQ11	DQ15 38	DDR_B_D15
	39 VSS50	VSS54 40	
	41 VSS18	VSS20 42	
DDR_B_D20	43 DQ16	DQ20 44	DDR_B_D21
DDR_B_D16	45 DQ17	DQ21 46	DDR_B_D23
	47 VSS1	VSS6 48	
DDR_B_DQS#2	49 DQS#2	NC3 50	PM_EXTTS#1 10
DDR_B_DQS2	51 DQS2	DM2 52	DDR_B_DM2
	53 VSS19	VSS21 54	
DDR_B_D18	55 DQ18	DQ22 56	DDR_B_D22
DDR_B_D19	57 DQ19	DQ23 58	DDR_B_D17
	59 VSS22	VSS24 60	
DDR_B_D25	61 DQ24	DQ28 62	DDR_B_D29
DDR_B_D28	63 DQ25	DQ29 64	DDR_B_D31
	65 VSS23	VSS25 66	
DDR_B_DM3	67 DM3	DQS#3 68	DDR_B_DQS#3
	69 NC4	DQS3 70	DDR_B_DQS3
	71 VSS9	VSS10 72	
DDR_B_D27	73 DQ26	DQ30 74	DDR_B_D24
DDR_B_D30	75 DQ27	DQ31 76	DDR_B_D26
	77 VSS4	VSS8 78	
10,20 DDR_CKE2_DIMMB	79 CKE0	CKE1 80	DDR_CKE3_DIMMB 10,20
	81 VDD7	VDD8 82	
	83 NC1	A15 84	DDR_B_MA14
11,20 DDR_B_BS2	85 A16_BA2	A14 86	
	87 VDD9	VDD11 88	DDR_B_MA11
DDR_B_MA12	89 A12	A11 90	DDR_B_MA7
DDR_B_MA9	91 A9	A7 92	DDR_B_MA6
DDR_B_MA8	93 A8	A6 94	
	95 VDD5	VDD4 96	
DDR_B_MA5	97 A5	A4 98	DDR_B_MA4
DDR_B_MA3	99 A3	A2 100	DDR_B_MA2
DDR_B_MA1	101 A1	A0 102	DDR_B_MA0
	103 VDD10	VDD12 104	
DDR_B_MA10	105 A10/AP	BA1 106	DDR_B_BS1 11,20
DDR_B_BS0 11,20 DDR_B_BS0	107 BA0	RAS# 108	DDR_B_RAS# 11,20
11,20 DDR_B_WE# DDR_B_WE#	109 WE#	S0# 110	DDR_CS2_DIMMB# 10,20
	111 VDD2	VDD1 112	
11,20 DDR_B_CAS# DDR_B_CAS#	113 CAS#	ODT0 114	M_ODT2 10,20
10,20 DDR_CS3_DIMMB#	115 S1#	A13 116	DDR_B_MA13
	117 VDD3	VDD6 118	
10,20 M_ODT3 M_ODT3	119 ODT1	NC2 120	
	121 VSS11	VSS12 122	
DDR_B_D38	123 DQ32	DQ36 124	DDR_B_D35
DDR_B_D36	125 DQ33	DQ37 126	DDR_B_D32
	127 VSS26	VSS28 128	
DDR_B_DQS#4	129 DQS#4	DM4 130	DDR_B_DM4
DDR_B_DQS4	131 DQS4	VSS42 132	
	133 VSS2	DQ38 134	DDR_B_D39
DDR_B_D34	135 DQ34	DQ39 136	DDR_B_D37
DDR_B_D33	137 DQ35	VSS55 138	
	139 VSS27	DQ44 140	DDR_B_D40
DDR_B_D45	141 DQ40	DQ45 142	DDR_B_D41
DDR_B_D46	143 DQ41	VSS43 144	
	145 VSS29	DQS#5 146	DDR_B_DQS#5
DDR_B_DM5	147 DM5	DQS5 148	DDR_B_DQS5
	149 VSS51	VSS56 150	
DDR_B_D44	151 DQ42	DQ46 152	DDR_B_D47
DDR_B_D42	153 DQ43	DQ47 154	DDR_B_D43
	155 VSS40	VSS44 156	
DDR_B_D53	157 DQ48	DQ52 158	DDR_B_D52
DDR_B_D48	159 DQ49	DQ53 160	DDR_B_D49
	161 VSS52	VSS57 162	
	163 NCTEST	CK1 164	M_CLK_DDR3 10
	165 VSS30	CK1# 166	M_CLK_DDR#3 10
DDR_B_DQS#6	167 DQS#6	VSS45 168	
DDR_B_DQS6	169 DQS6	DM6 170	DDR_B_DM6
	171 VSS31	VSS32 172	
DDR_B_D51	173 DQ50	DQ54 174	DDR_B_D55
DDR_B_D54	175 DQ51	DQ55 176	DDR_B_D50
	177 VSS33	VSS35 178	
DDR_B_D56	179 DQ56	DQ60 180	DDR_B_D57
DDR_B_D62	181 DQ57	DQ61 182	DDR_B_D61
	183 VSS3	VSS7 184	
DDR_B_DM7	185 DM7	DQS#7 186	DDR_B_DQS#7
	187 VSS34	DQS7 188	DDR_B_DQS7
DDR_B_D63	189 DQ58	VSS36 190	
DDR_B_D60	191 DQ59	DQ62 192	DDR_B_D58
MEM_SDATA	193 VSS14	DQ63 194	DDR_B_D59
MEM_SCLK	195 SDA	VSS13 196	
+3.3V_RUN	197 SCL	SA0 198	
	199 VDDSPD	SA1 200	
	201 GND0	GND1 202	
	203 NP_NC1NP_NC2	204	

STD FOXCONN/AS0A426-NASN-7F

CLOCK 2 , 3
CKE 2 , 3

Non-iAMT
+3.3V_RUN
SMbus address A4

V_DDR_MCH_REF
C281 0.1UF/10V MLCC/+80-20%
C275 2.2UF/6.3V MLCC/+/-10%
pt_c0805_h53

+1.8V_SUS
Please these Caps near So-Dimm1
C327 C300 C333 C341 C342
2.2UF/6.3V MLCC/+/-10% pt_c0603
0.1UF/10V MLCC/+80-20% pt_c0603

+1.8V_SUS
Please these Caps near So-Dimm2
C321 C619 C591 C331 C317
2.2UF/6.3V MLCC/+/-10% pt_c0603
0.1UF/10V MLCC/+80-20% pt_c0603

+1.8V_SUS
Please these Caps near So-Dimm1
C315 C325 C319 C323
0.1UF/10V MLCC/+80-20%

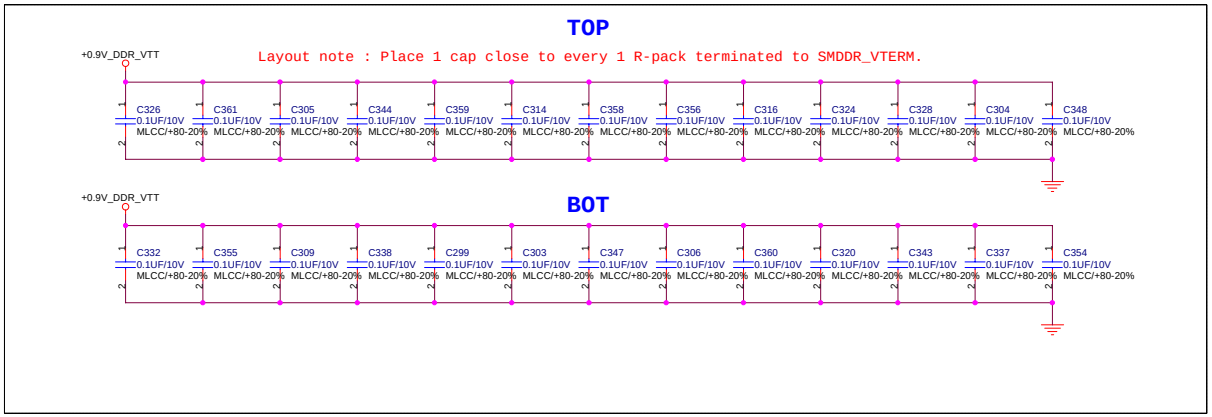
+1.8V_SUS
Please these Caps near So-Dimm2
C340 C601 C609 C616
0.1UF/10V MLCC/+80-20%

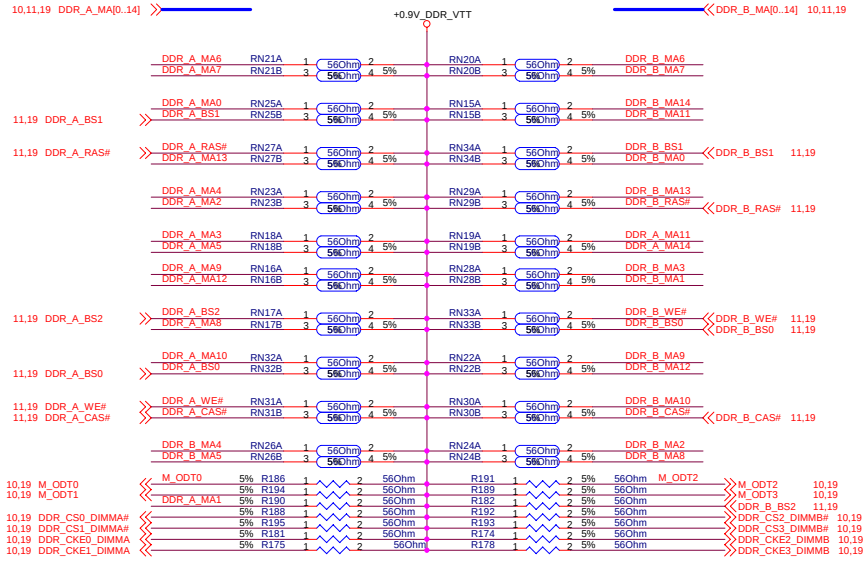
+3.3V_RUN
Non-iAMT
C651 2.2UF/6.3V MLCC/+/-10%
C647 0.1UF/10V MLCC/+80-20%
pt_c0805_h53

Non-iAMT
+3.3V_RUN
R211
R212 10KOhm 5%

<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***DDR2 SO-DIMM (0)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***STANLY_HSU***
		SHEET **19** OF **69**		RELEASE DATE :	



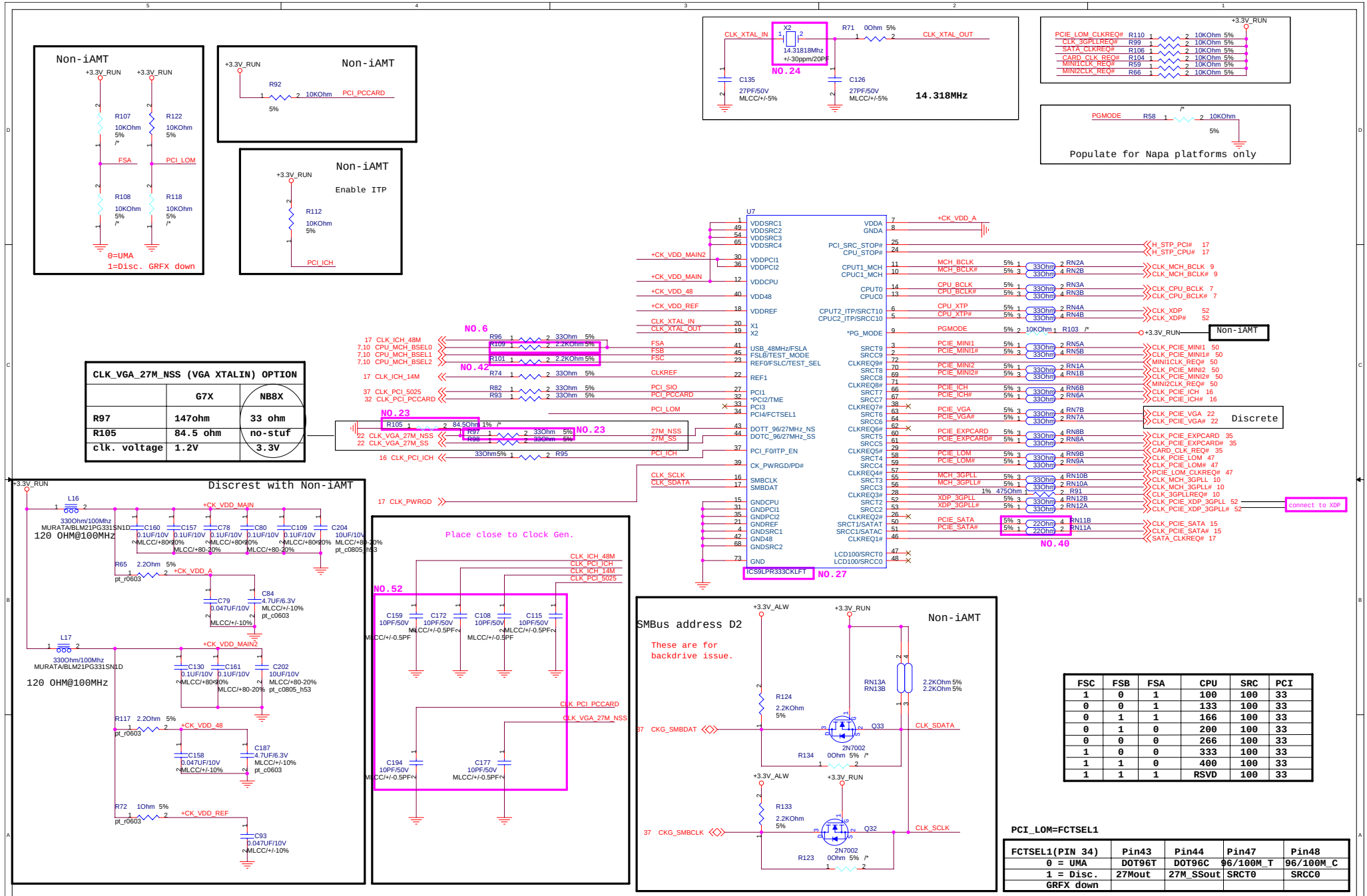


Please these resistor closely DIMMA, all trace length<750 mil.

Please these resistor closely DIMMB, all trace length<750 mil.

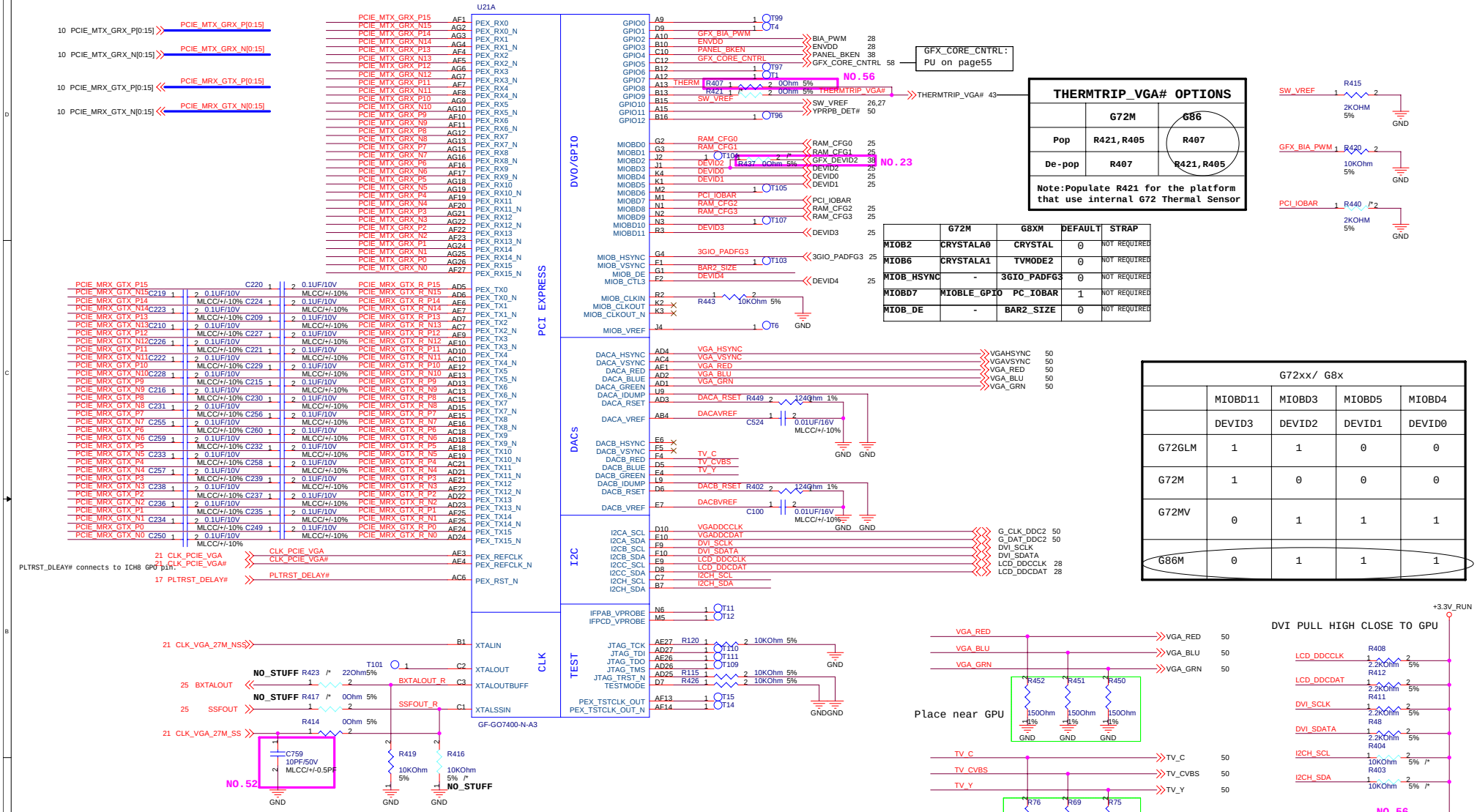
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***DDR2 SO-DIMM (1)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***STANLY_HSU***
		SHEET **20** OF **69**		RELEASE DATE :	



<Variant Name>

PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *CLK GEN. CY28547*	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: *STANLY_HSU*
		SHEET 21 OF 69		RELEASE DATE:	



THERMTRIP_VGA# OPTIONS		
	G72M	G86
Pop	R421,R405	R407
De-pop	R407	R421,R405
Note:Populate R421 for the platform that use internal G72 Thermal Sensor		

	G72M	G8XM	DEFAULT	STRAP
MIOB2	CRYSTALA0	CRYSTAL	0	NOT REQUIRED
MIOB6	CRYSTALA1	TVMODE2	0	NOT REQUIRED
MIOB_HSYNC	-	3GIO_PADFG3	0	NOT REQUIRED
MIOBD7	MIOBLE_GPIO	PC_IOBAR	1	NOT REQUIRED
MIOB_DE	-	BAR2_SIZE	0	NOT REQUIRED

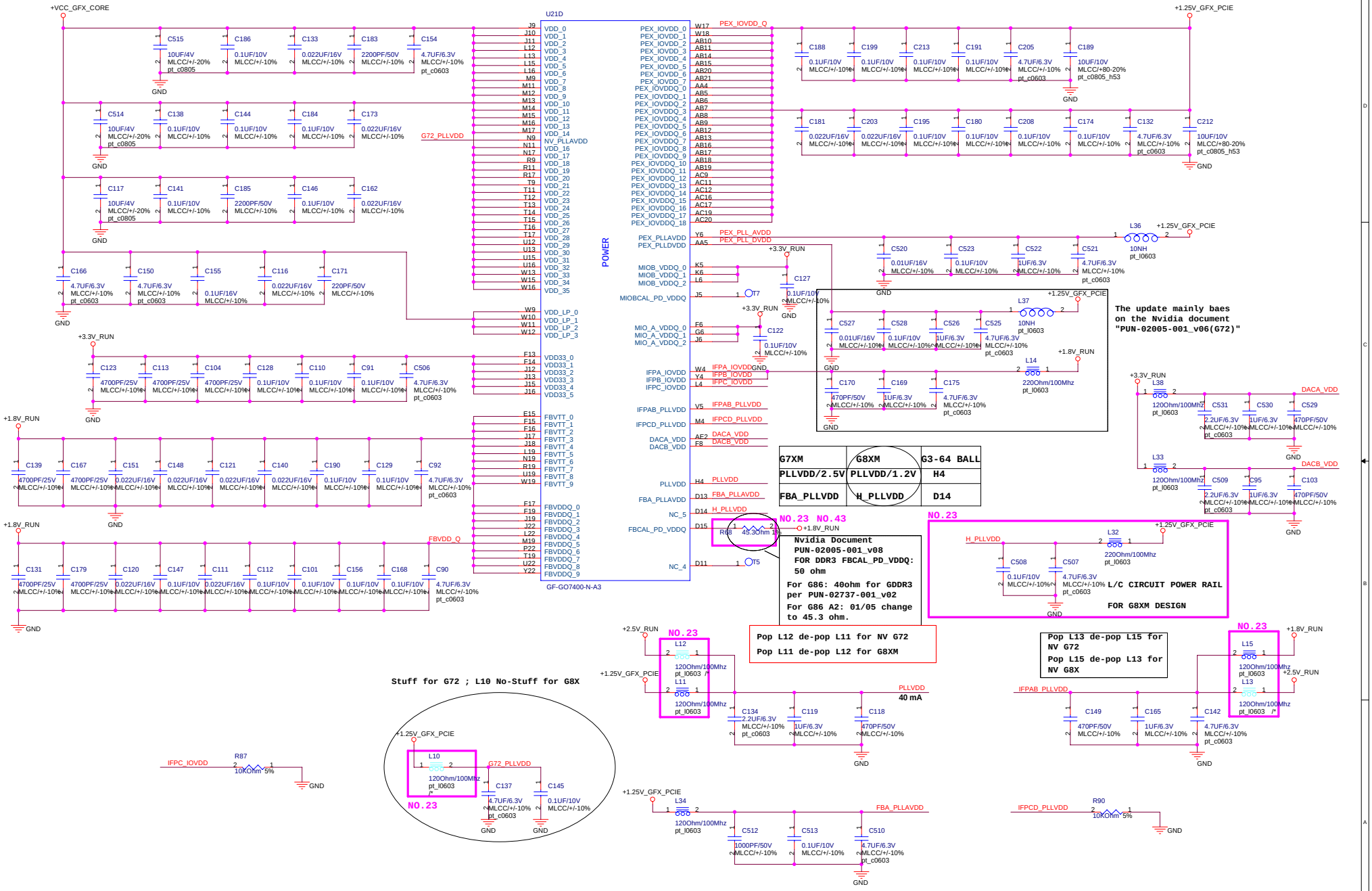
G72xx/ G8x				
	MIOBD11	MIOBD3	MIOBD5	MIOBD4
	DEVID3	DEVID2	DEVID1	DEVID0
G72GLM	1	1	0	0
G72M	1	0	0	0
G72MV	0	1	1	1
G86M	0	1	1	1

POPULATION OPTIONS			
	CY28547+SS	CY28547+U5	CY28547 wo/SS
Pop	R414,R419, R98	R423,R417, U5	R416,R419
De-pop	U5,R423, R417,R416	R414,R416, R419,R98	U5,R98, R414,R417, R423
'U5'indicate all ckt.related to U5 in Page.25			

Layout comments: Place R423,R419 as close as possible to C3. . Place R414,R416and R417 as close as posisble to pin C1.

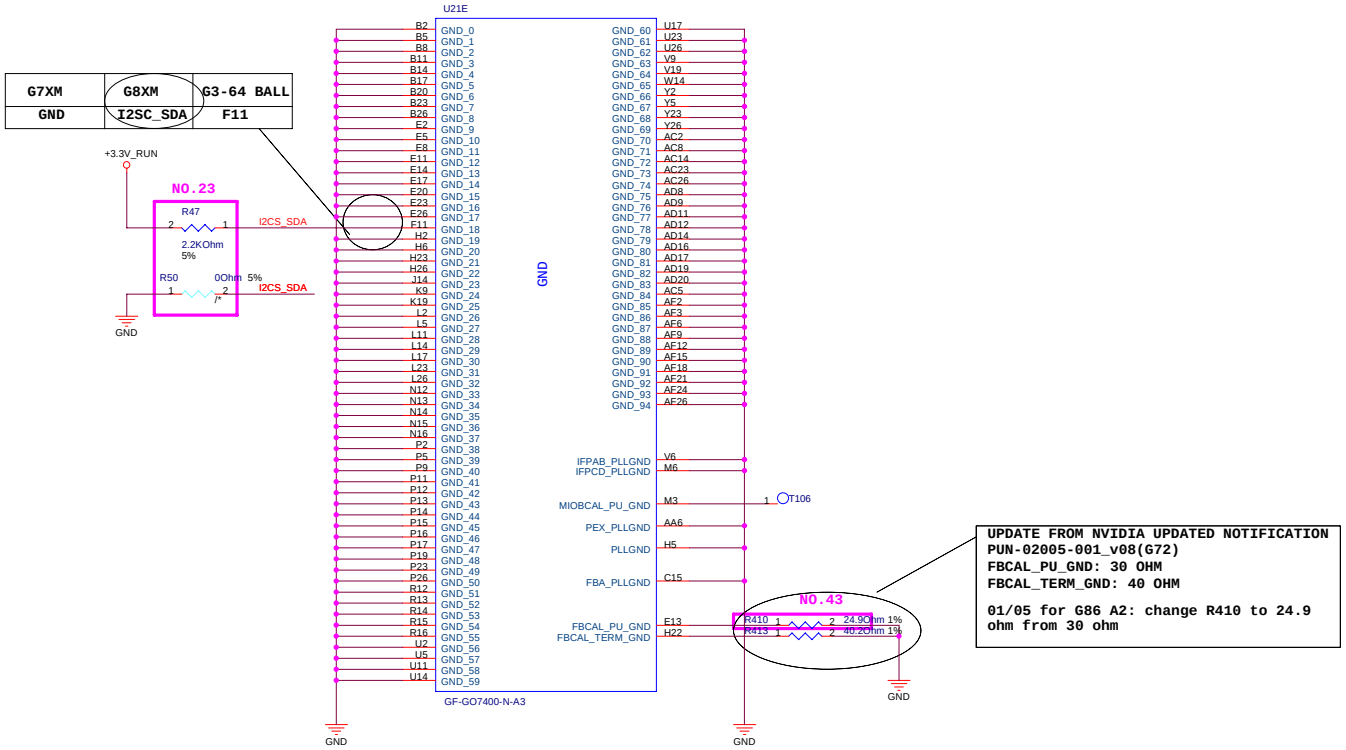
<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: G72M/G8X CORE PCIE	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Sean Kuo
		SHEET 22 OF 69		RELEASE DATE :	



<Variant Name>

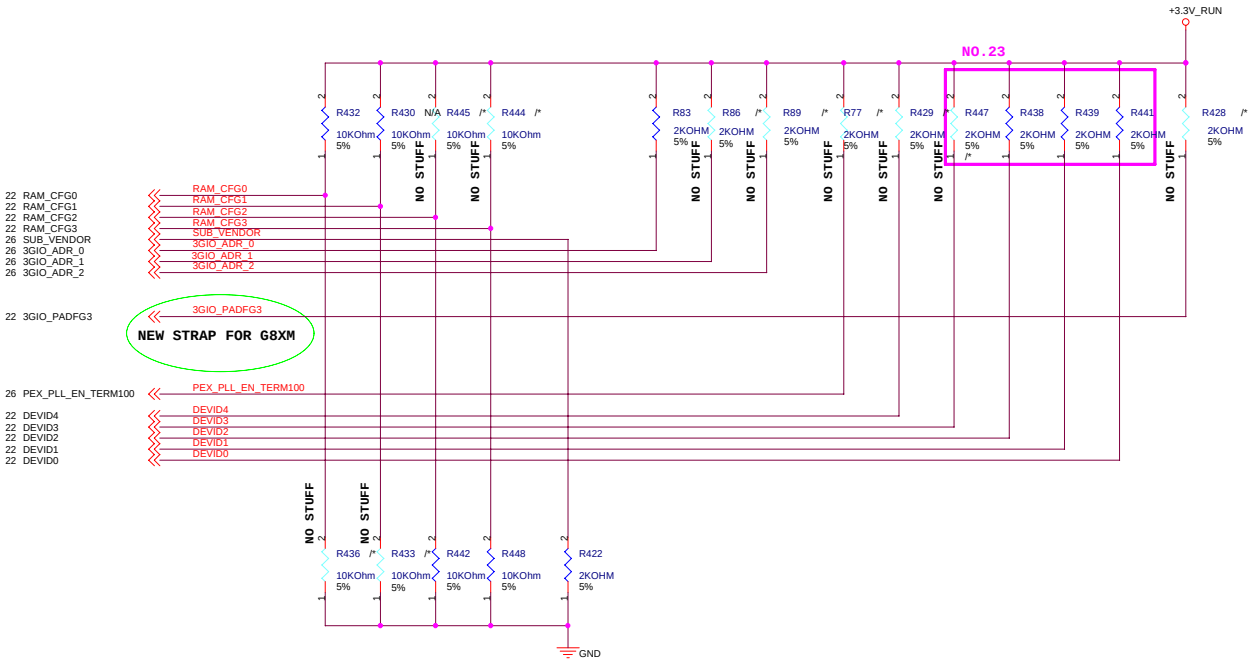
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***G72M/G8X POWER***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Sean Kuo***
		SHEET **23** OF **69**		RELEASE DATE :	



<Variant Name>

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *G7XM/G8X CORE GND*	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :	*Sean Kuo*
		SHEET 24 OF 69		RELEASE DATE :			

NV44M



STRAPS	PIN	DESCRIPTION		Value
ROM_TYPE[1:0]	MIOBD10 MIOB_VSYNC	Parallel=00, SERIAL AT25F=01 DEFAULT,Serial SST45VF=10, LPC=11		01
SUB_VENDOR	MIOAD1			0
PEX_PLL_TERM	MIOAD0			0
RAM_CFG[3:0]	MIOBD0 MIOBD1 MIOBD8 MIOBD9	FOR GDDR1	8Mx32 DDR monolithic (32bit) 300MHz,1.8V	1001
			4Mx32 DDR generic (64bit) 1.8V I/O	0100
			4Mx32 DDR generic (32bit) 1.8V I/O	1100
		FOR GDDR3	Infineon 8Mx32 500MHz, 1.8V	0101
			Hynix 8Mx32 500MHz, 1.8V	0111
			Samsung 8Mx32 500MHz, 1.8V	0110
			Infineon 16Mx32 GDDR3 ,1.8V	0001
			Hynix 16Mx32 GDDR3 1.8V	0010
			Samsung 16Mx32 GDDR3 1.8V	0011

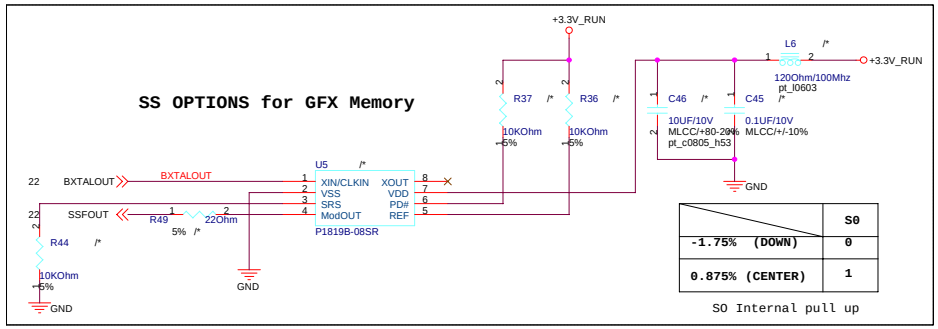
Internal Pull-down
MIOAD0, MIOAD6,
MIOAD8, MIOAD9

MIOAD1----SUB_VENDOR 0, SYSTEM BIOS

MIOAD0----PEX_PLL_EN_TERM

MIOAD6----3GIO_ADR_0 [2:0] 001 for NV43/NV44
MIOAD8----3GIO_ADR_1 010 for G7x, NV42
MIOAD9----3GIO_ADR_2

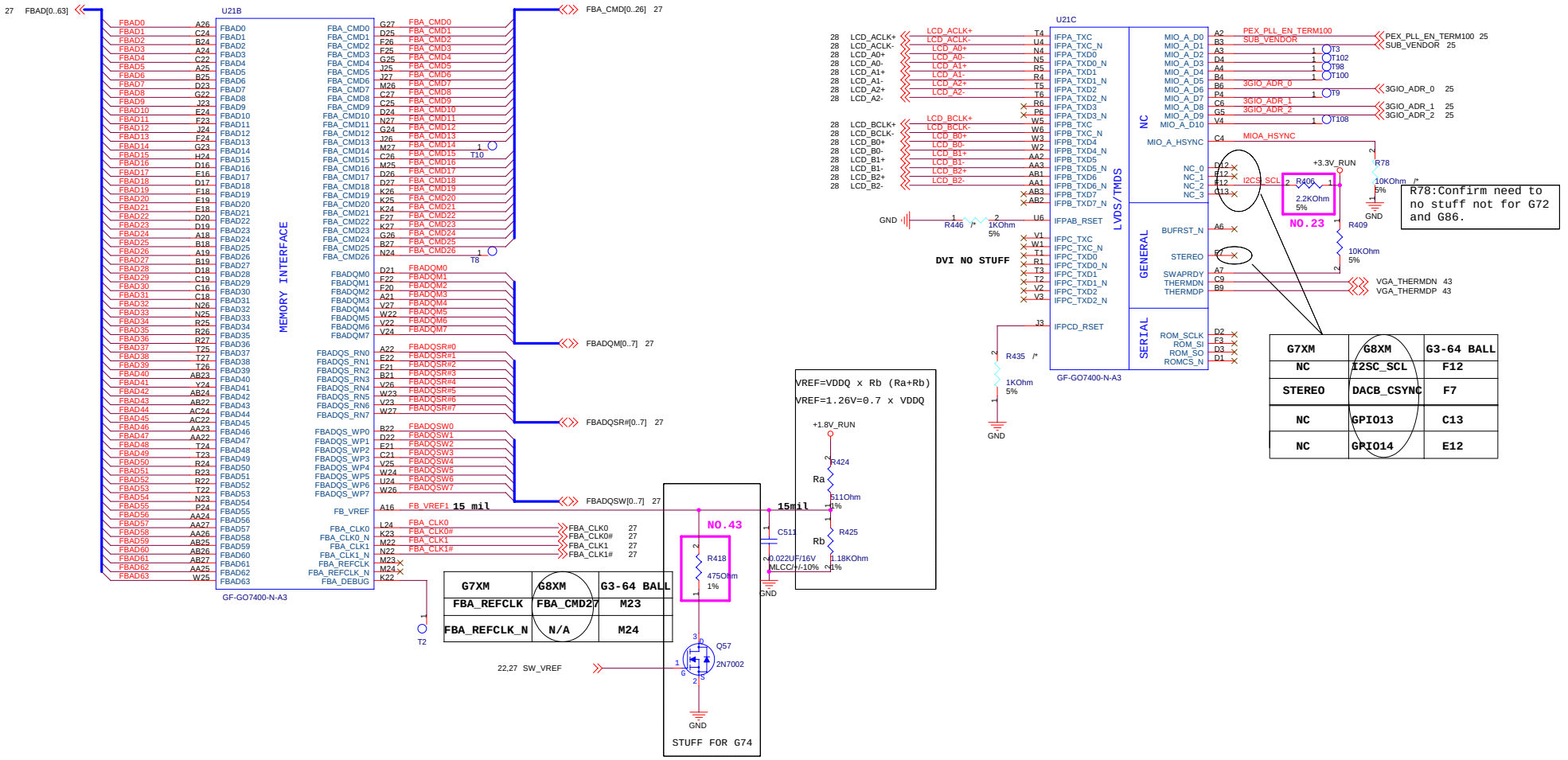
MIOBD4----PCI_DEVID0 1000,G72M
MIOBD5----PCI_DEVID1 0111,G72MV
MIOBD3----PCI_DEVID2
MIOBD11---PCI_DEVID3



M08 HAS REMOVED THIS PORTION
INSTALL OR NOT?

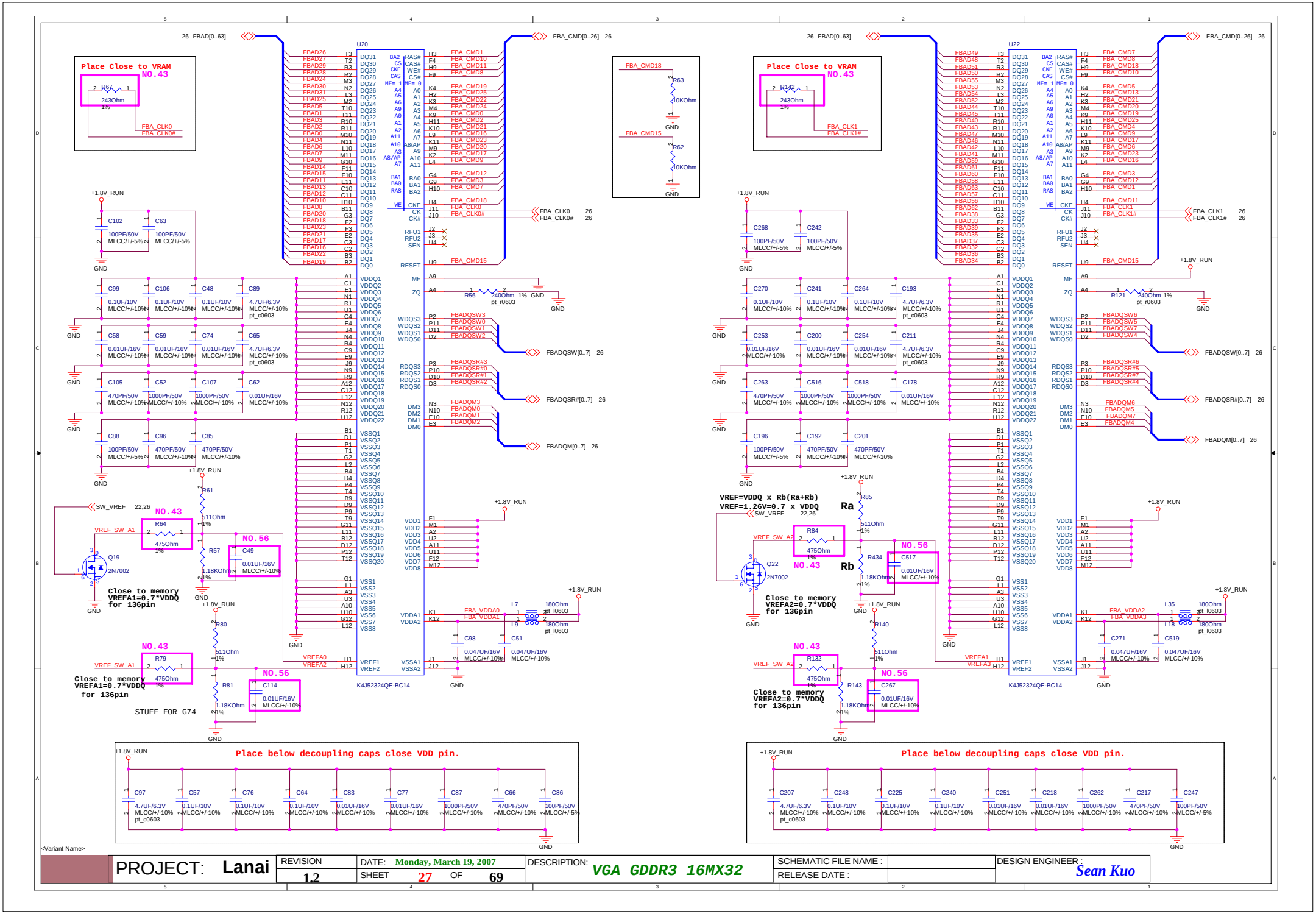
<Variant Name>

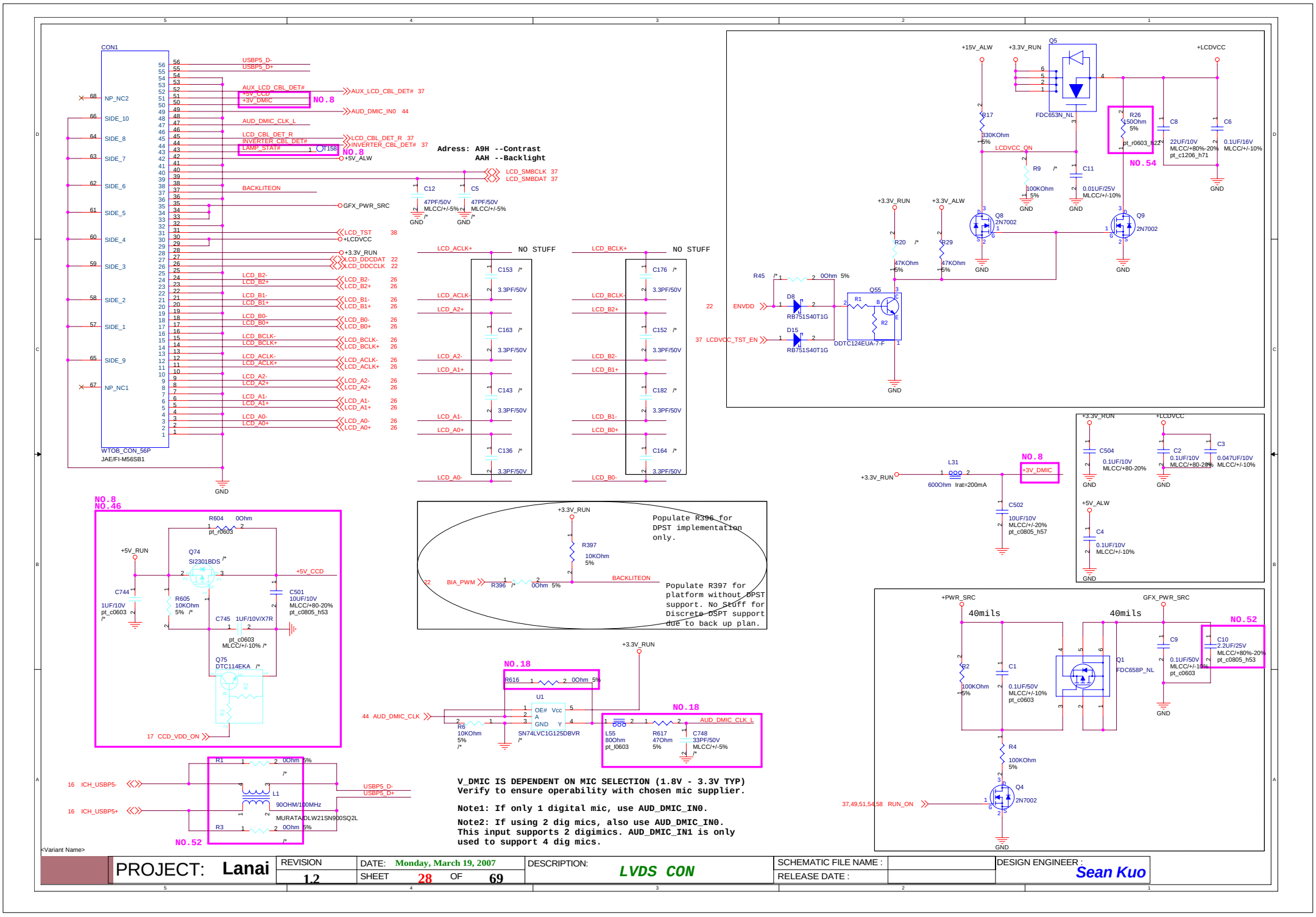
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: *G72M/G8X STRAPPING PAGE*	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : *Sean Kuo*
		SHEET 25 OF 69		RELEASE DATE :	



<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: G72M/G8X FBA/LVDS	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Sean Kuo
		SHEET 26 OF 69		RELEASE DATE :	


Place Close to VRAM
NO.43
R67
243Ohm
1%
FBA_CLK0
FBA_CLK0#
Place Close to VRAM
NO.43
R142
243Ohm
1%
FBA_CLK1
FBA_CLK1#
U20
U22
K4J52324QE-BC14
FBA_CMD[0..26]
FBADQSW[0..7]
FBADQSR#[0..7]
FBADQM[0..7]
R63
10KOhm
R62
10KOhm
FBA_CMD18
FBA_CMD15
+1.8V_RUN
GND
R56
240Ohm 1% pt_r0603
R121
240Ohm 1% pt_r0603
SW_VREF
VREF_SW_A1
VREF_SW_A2
Q19
Q22
2N7002
R61
511Ohm
1%
R57
1.18KOhm
1%
R80
511Ohm
1%
R81
1.18KOhm
1%
R79
475Ohm
1%
R64
475Ohm
1%
R84
475Ohm
1%
R85
511Ohm
1%
R434
1.18KOhm
1%
R140
511Ohm
1%
R143
1.18KOhm
1%
R132
475Ohm
1%
Ra
Rb
NO.56
C49
0.01UF/16V
MLCC/+/-10%
C114
0.01UF/16V
MLCC/+/-10%
C517
0.01UF/16V
MLCC/+/-10%
C267
0.01UF/16V
MLCC/+/-10%
Close to memory
VREFA1=0.7*VDDQ
for 136pin
Close to memory
VREFA2=0.7*VDDQ
for 136pin
Close to memory
VREFA1=0.7*VDDQ
for 136pin
Close to memory
VREFA2=0.7*VDDQ
for 136pin
VREF=VDDQ x Rb(Ra+Rb)
VREF=1.26V=0.7 x VDDQ
STUFF FOR G74
FBA_VDDA0
FBA_VDDA1
FBA_VDDA2
FBA_VDDA3
L7
L9
L35
L18
180Ohm pt_l0603
C98
0.047UF/16V
MLCC/+/-10%
C51
0.047UF/16V
MLCC/+/-10%
C271
0.047UF/16V
MLCC/+/-10%
C519
0.047UF/16V
MLCC/+/-10%
Place below decoupling caps close VDD pin.
C97
4.7UF/6.3V
MLCC/+/-10%
pt_c0603
C57
0.1UF/10V
MLCC/+/-10%
C76
0.1UF/10V
MLCC/+/-10%
C64
0.1UF/10V
MLCC/+/-10%
C83
0.01UF/16V
MLCC/+/-10%
C77
0.01UF/16V
MLCC/+/-10%
C87
1000PF/50V
MLCC/+/-10%
C66
470PF/50V
MLCC/+/-10%
C86
100PF/50V
MLCC/+/-5%
C207
4.7UF/6.3V
MLCC/+/-10%
pt_c0603
C248
0.1UF/10V
MLCC/+/-10%
C225
0.1UF/10V
MLCC/+/-10%
C240
0.1UF/10V
MLCC/+/-10%
C251
0.01UF/16V
MLCC/+/-10%
C218
0.01UF/16V
MLCC/+/-10%
C262
1000PF/50V
MLCC/+/-10%
C217
470PF/50V
MLCC/+/-10%
C247
100PF/50V
MLCC/+/-5%
<Variant Name>
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 27 OF 69
DESCRIPTION: VGA GDDR3 16MX32
SCHEMATIC FILE NAME :
RELEASE DATE :
DESIGN ENGINEER : Sean Kuo


CON1
WTOB_CON_56P
JAE/FI-M56SB1
NP_NC2
SIDE_10
SIDE_8
SIDE_7
SIDE_6
SIDE_5
SIDE_4
SIDE_3
SIDE_2
SIDE_1
SIDE_9
NP_NC1
USBP5_D-
USBP5_D+
AUX_LCD_CBL_DET#
+5V_CCD
+3V_DMIC
NO.8
AUD_DMIC_IN0 44
AUD_DMIC_CLK_L
LCD_CBL_DET_R
INVERTER_CBL_DET#
LAMP_STAT#
T158
+5V_ALW
Adress: A9H --Contrast
AAH --Backlight
LCD_SMBCLK 37
LCD_SMBDAT 37
BACKLITEON
GFX_PWR_SRC
LCD_TST 38
+LCDVCC
+3.3V_RUN
LCD_DDCDAT 22
LCD_DDCCLK 22
LCD_B2- 26
LCD_B2+ 26
LCD_B1- 26
LCD_B1+ 26
LCD_B0- 26
LCD_B0+ 26
LCD_BCLK- 26
LCD_BCLK+ 26
LCD_ACLK- 26
LCD_ACLK+ 26
LCD_A2- 26
LCD_A2+ 26
LCD_A1- 26
LCD_A1+ 26
LCD_A0- 26
LCD_A0+ 26
C12 47PF/50V MLCC/+/-5%
C5 47PF/50V MLCC/+/-5%
GND
NO STUFF
LCD_ACLK+
LCD_ACLK-
LCD_A2+
LCD_A2-
LCD_A1+
LCD_A1-
LCD_A0+
LCD_A0-
C153 3.3PF/50V
C163 3.3PF/50V
C143 3.3PF/50V
C136 3.3PF/50V
LCD_BCLK+
LCD_BCLK-
LCD_B2+
LCD_B2-
LCD_B1+
LCD_B1-
LCD_B0+
LCD_B0-
C176 3.3PF/50V
C152 3.3PF/50V
C182 3.3PF/50V
C164 3.3PF/50V
+15V_ALW
+3.3V_RUN
+LCDVCC
Q5
FDC653N_NL
R17 330KOhm 5%
LCDVCC_ON
R9 100KOhm 5%
C11 0.01UF/25V MLCC/+/-10%
R26 150Ohm 5%
pt_r0603_h22
NO.54
C8 22UF/10V MLCC/+80%-20% pt_c1206_h71
C6 0.1UF/16V MLCC/+/-10%
Q8 2N7002
Q9 2N7002
R20 47KOhm 5%
R29 47KOhm 5%
R45 0Ohm 5%
D8 RB751S40T1G
D15 RB751S40T1G
ENVDD
LCDVCC_TST_EN
Q55 DDTC124EUA-7-F
R1
R2
L31 600Ohm Irat=200mA
NO.8
+3V_DMIC
C502 10UF/10V MLCC/+/-20% pt_c0805_h57
C504 0.1UF/10V MLCC/+80-20%
C2 0.1UF/10V MLCC/+80-20%
C3 0.047UF/10V MLCC/+/-10%
+5V_ALW
C4 0.1UF/10V MLCC/+/-10%
NO.46
R604 0Ohm pt_r0603
Q74 SI2301BDS
+5V_RUN
+5V_CCD
C744 1UF/10V pt_c0603
R605 10KOhm 5%
C745 1UF/10V/X7R pt_c0603 MLCC/+/-10%
C501 10UF/10V MLCC/+80-20% pt_c0805_h53
Q75 DTC114EKA
17 CCD_VDD_ON
Populate R396 for DPST implementation only.
R397 10KOhm 5%
BIA_PWM
R396 0Ohm 5%
BACKLITEON
Populate R397 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.
NO.18
R616 0Ohm 5%
U1
OE# Vcc
A
GND Y
SN74LVC1G125DBVR
44 AUD_DMIC_CLK
R6 10KOhm 5%
L55 80Ohm pt_l0603
R617 47Ohm 5%
C748 33PF/50V MLCC/+/-5%
AUD_DMIC_CLK_L
+PWR_SRC
GFX_PWR_SRC
40mils
R2 100KOhm 5%
C1 0.1UF/50V MLCC/+/-10% pt_c0603
Q1 FDC658P_NL
C9 0.1UF/50V MLCC/+/-10% pt_c0603
C10 2.2UF/25V MLCC/+80%-20% pt_c0805_h53
NO.52
R4 100KOhm 5%
Q4 2N7002
37,49,51,54,58 RUN_ON
16 ICH_USBP5-
16 ICH_USBP5+
R1 0Ohm 5%
L1 90OHM/100MHz
MURATA/DLW21SN900SQ2L
R3 0Ohm 5%
USBP5_D-
USBP5_D+
V_DMIC IS DEPENDENT ON MIC SELECTION (1.8V - 3.3V TYP)
Verify to ensure operability with chosen mic supplier.
Note1: If only 1 digital mic, use AUD_DMIC_IN0.
Note2: If using 2 dig mics, also use AUD_DMIC_IN0.
This input supports 2 digimics. AUD_DMIC_IN1 is only used to support 4 dig mics.
<Variant Name>
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 28 OF 69
DESCRIPTION: LVDS CON
SCHEMATIC FILE NAME :
RELEASE DATE :
DESIGN ENGINEER : Sean Kuo

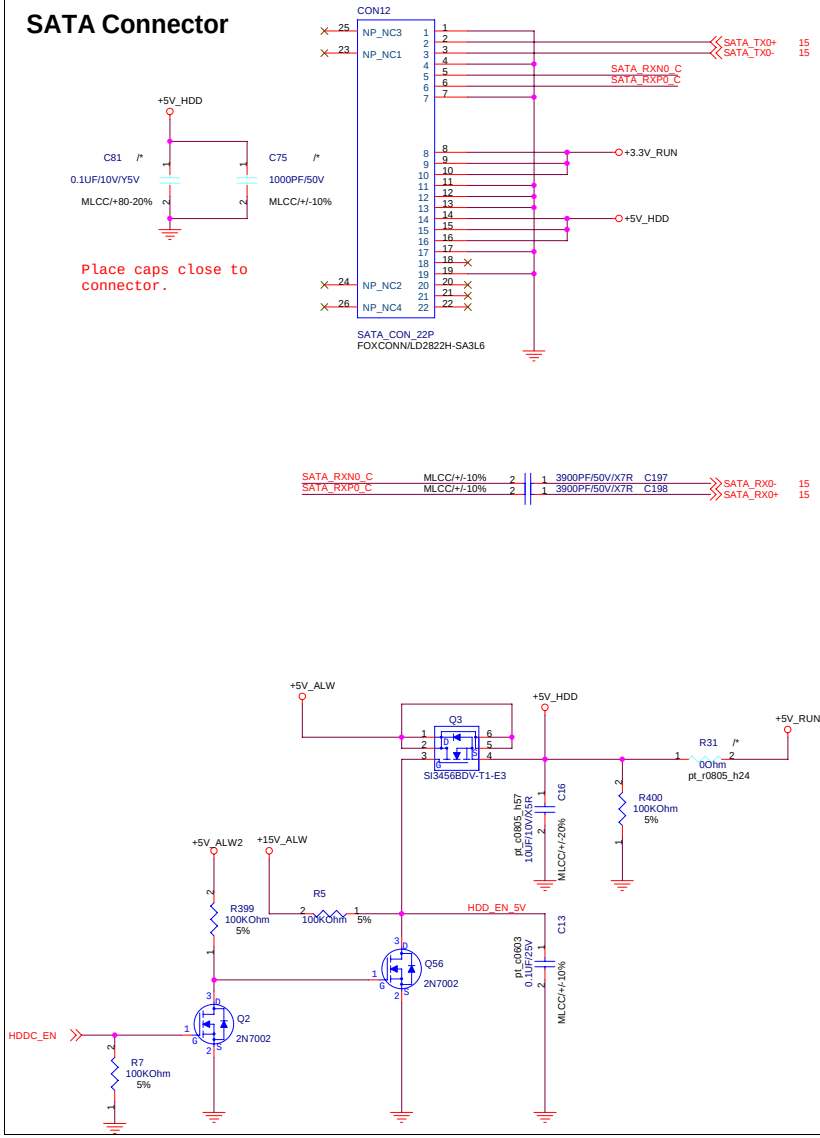
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***VGA CRT CON***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Sean Kuo***
		SHEET **29** OF **69**		RELEASE DATE :	

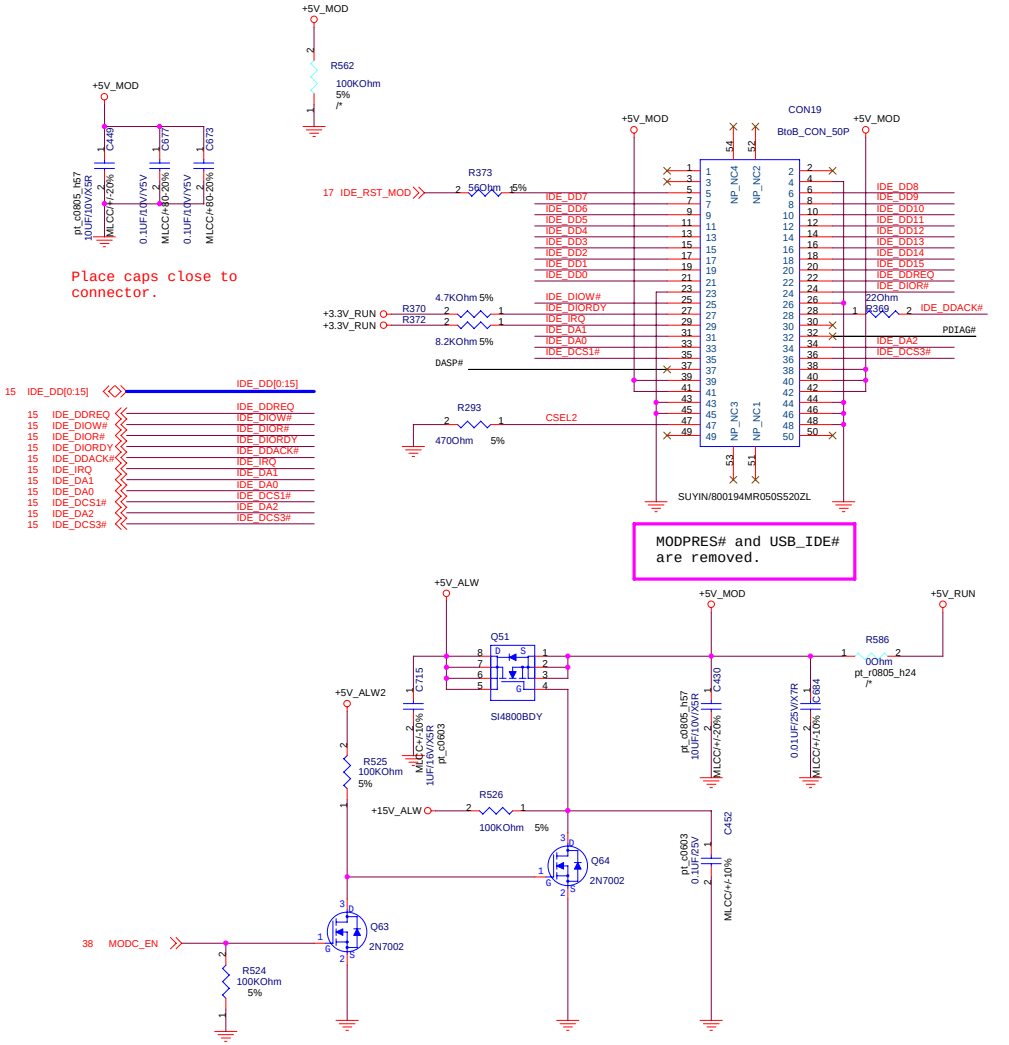
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***TV OUT CON***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Sean Kuo***
		SHEET **30** OF **69**		RELEASE DATE :	

SATA Connector

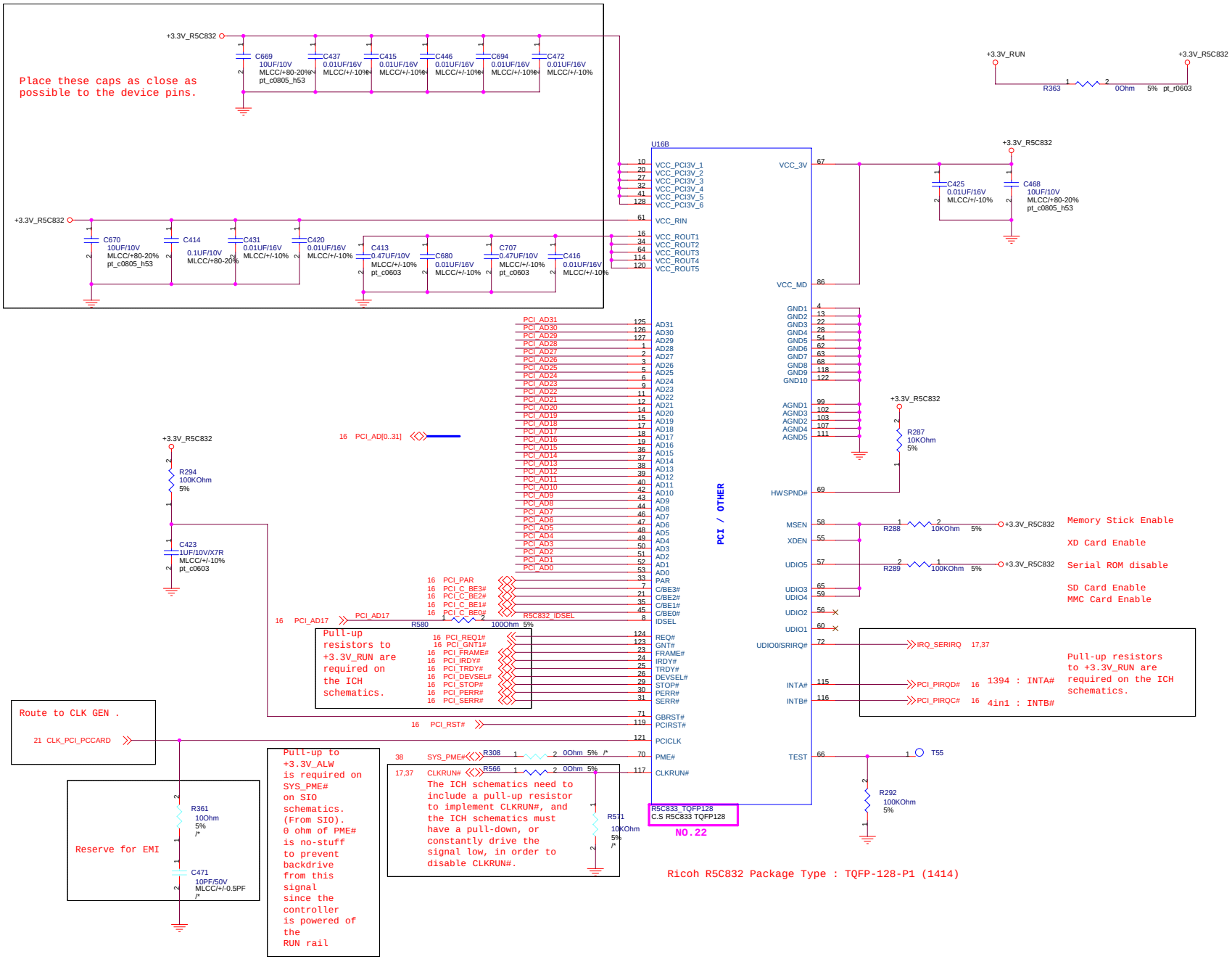


ODD Connector



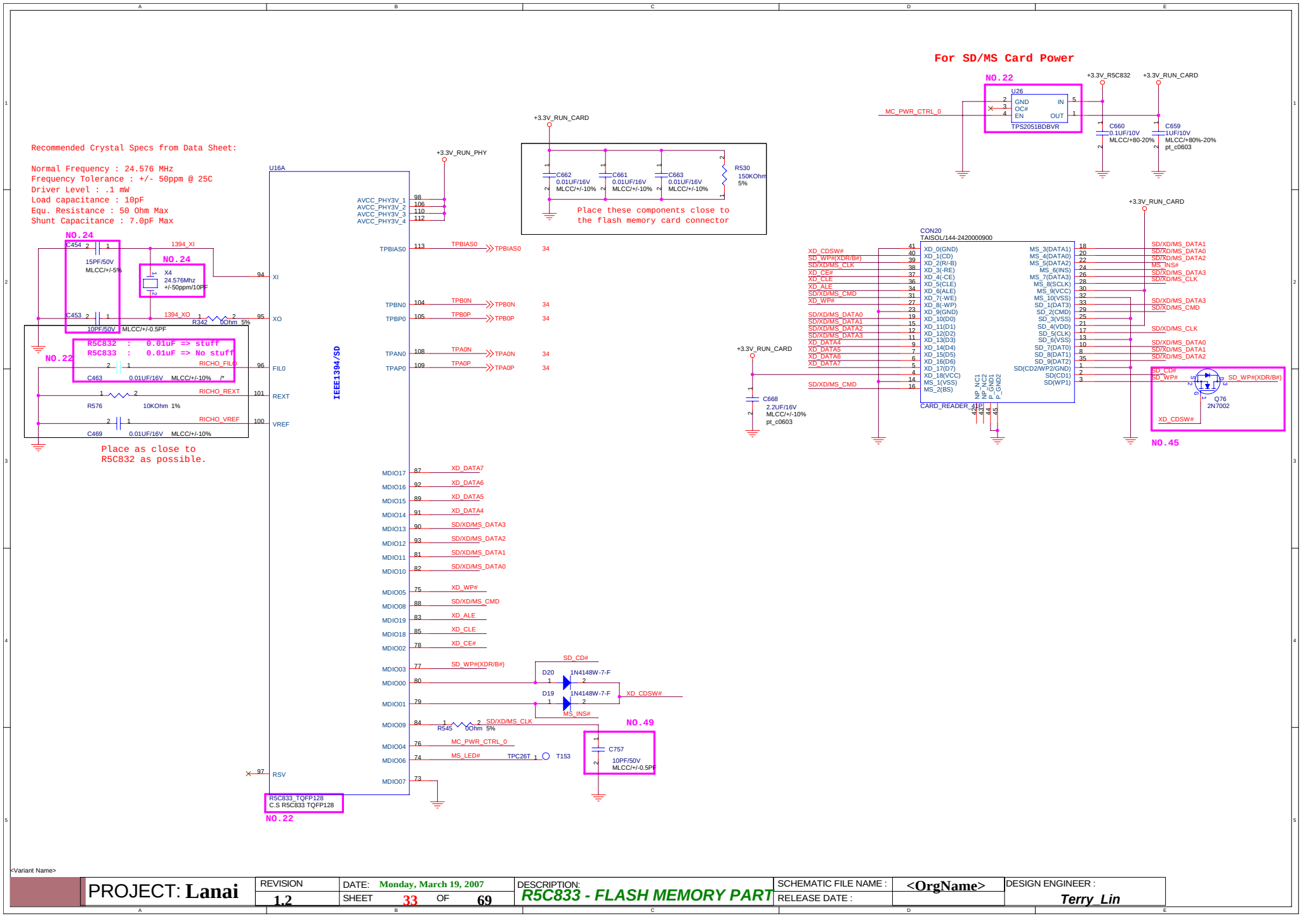
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***SATA(HDD & CD_ROM)***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
		SHEET **31** OF **69**		RELEASE DATE :		***Yihao Yeh***



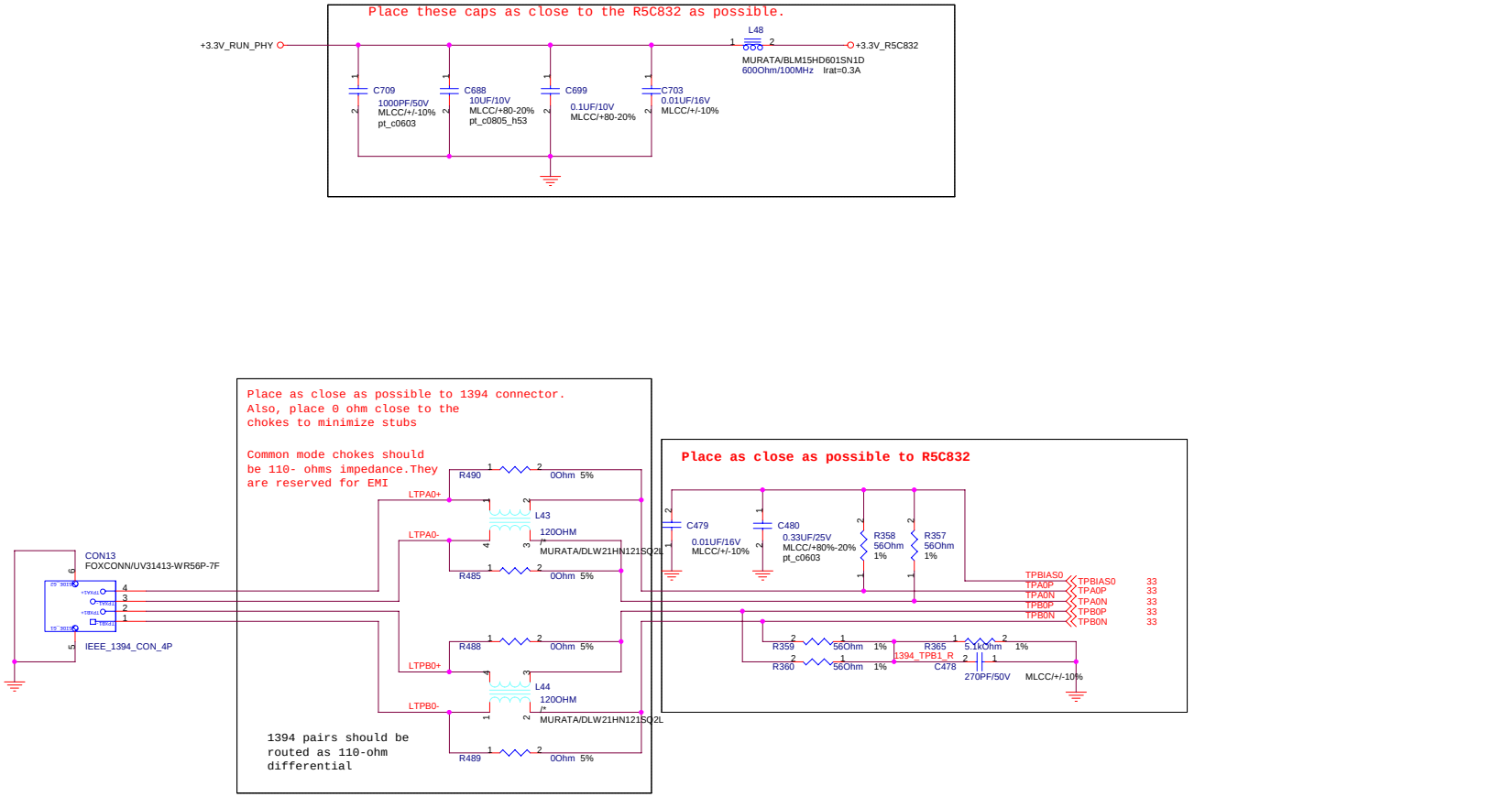
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***R5C833 - PCI INTERFACE***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Terry_Lin***
		SHEET **32** OF **69**		RELEASE DATE :	



<Variant Name>

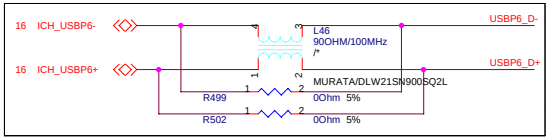
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***R5C833 - FLASH MEMORY PART***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Terry_Lin***
		SHEET **33** OF **69**		RELEASE DATE :	

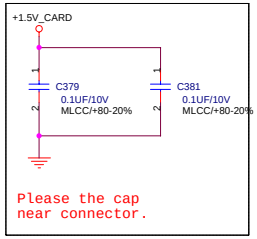


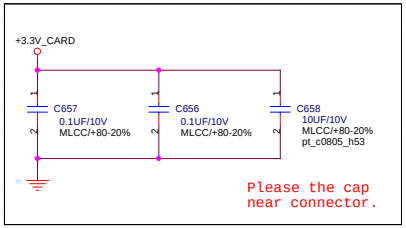
<Variant Name>

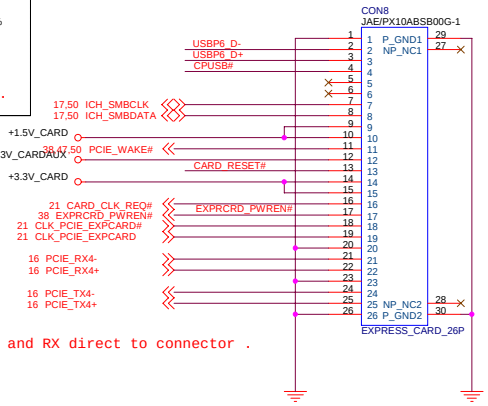
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***R5C833 - IEEE1394 PART***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Terry_Lin***
		SHEET **34** OF **69**		RELEASE DATE :		

Express Card



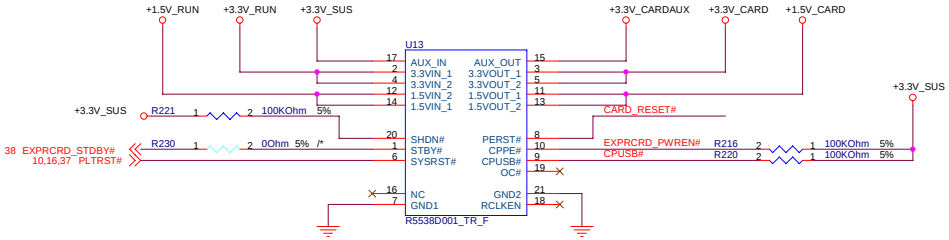


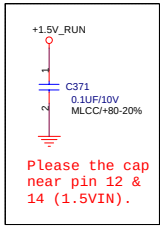


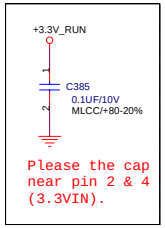


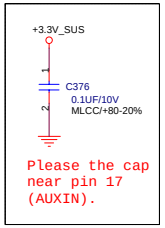
PCI-Express TX and RX direct to connector .

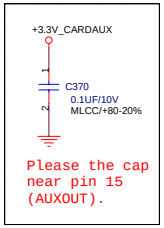
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

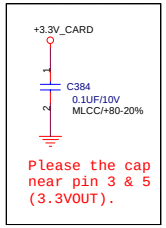


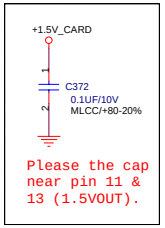






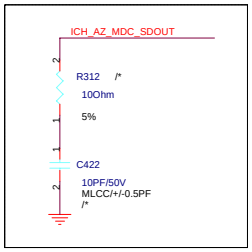


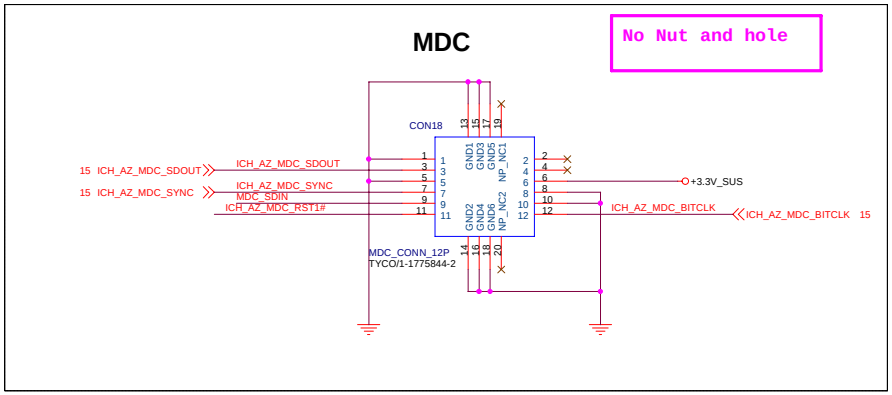


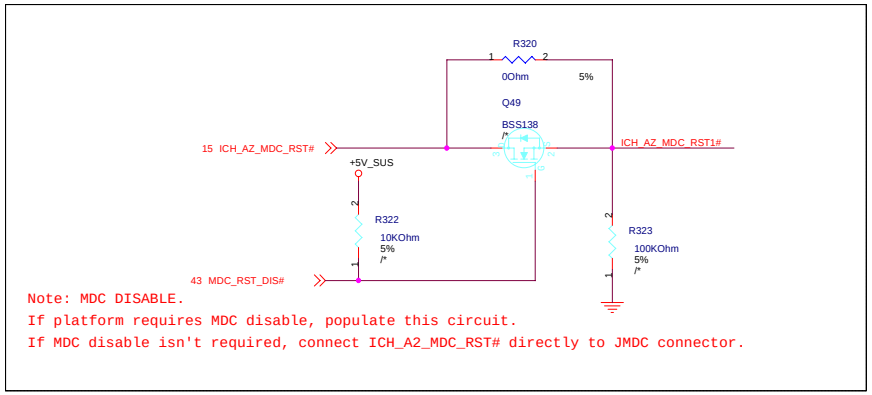


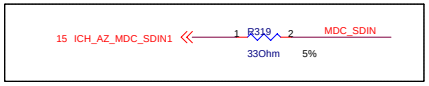
<Variant Name>

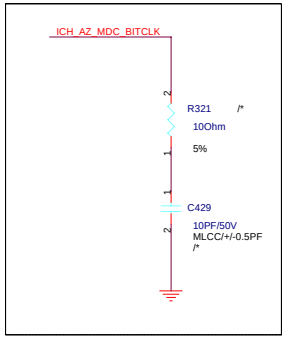
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***PCI-Express Card***	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 35 OF 69		RELEASE DATE :		*Terry_Lin*

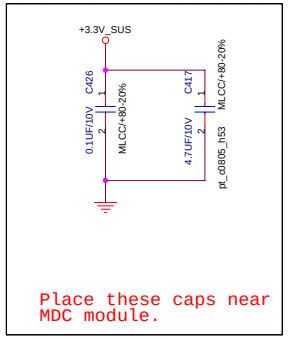






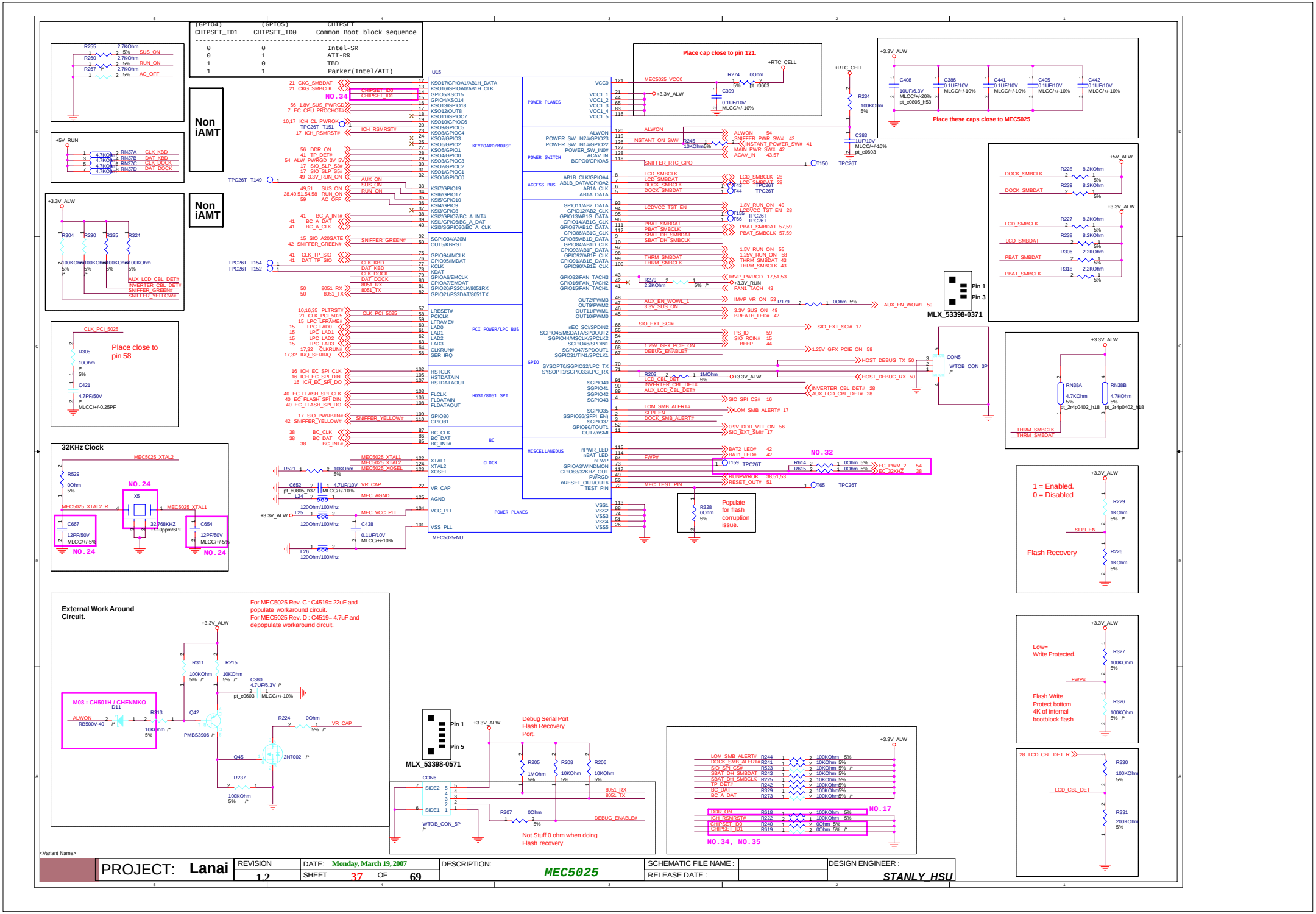


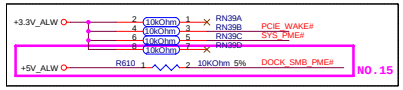


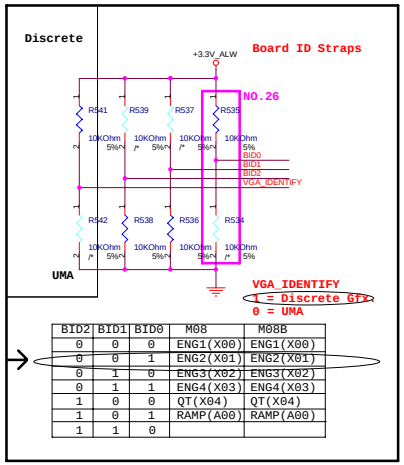


<Variant Name>

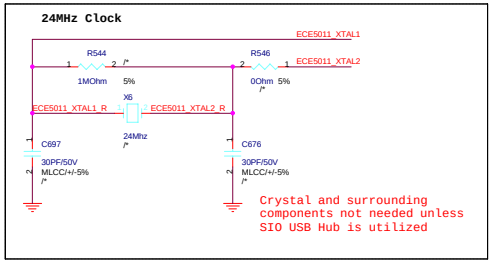
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***MDC CONN***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Yihao_Yeh***
		SHEET **36** OF **69**		RELEASE DATE :		

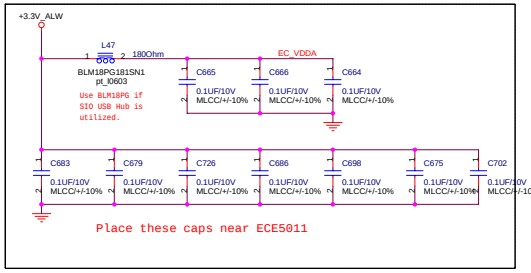

(GPIO4) (GPIO5) CHIPSET
CHIPSET_ID1 CHIPSET_ID0 Common Boot block sequence
0 0 Intel-SR
0 1 ATI-RR
1 0 TBD
1 1 Parker(Intel/ATI)
Non iAMT
Non iAMT
U15
MEC5025-NU
Place cap close to pin 121.
Place these caps close to MEC5025
Place close to pin 58
32KHz Clock
MLX_53398-0371
MLX_53398-0371
Pin 1
Pin 3
Pin 1
Pin 5
NO.24
NO.24
NO.24
NO.34
NO.32
NO.17
NO.34, NO.35
1 = Enabled.
0 = Disabled
Flash Recovery
Low=
Write Protected.
Flash Write
Protect bottom
4K of internal
bootblock flash
Populate
for flash
corruption
issue.
Debug Serial Port
Flash Recovery
Port.
Not Stuff 0 ohm when doing
Flash recovery.
External Work Around
Circuit.
For MEC5025 Rev. C : C4519= 22uF and
populate workaround circuit.
For MEC5025 Rev. D : C4519= 4.7uF and
depopulate workaround circuit.
M08 : CH501H / CHENMKO
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 37 OF 69
DESCRIPTION: MEC5025
SCHEMATIC FILE NAME :
RELEASE DATE :
DESIGN ENGINEER : STANLY_HSU
<Variant Name>

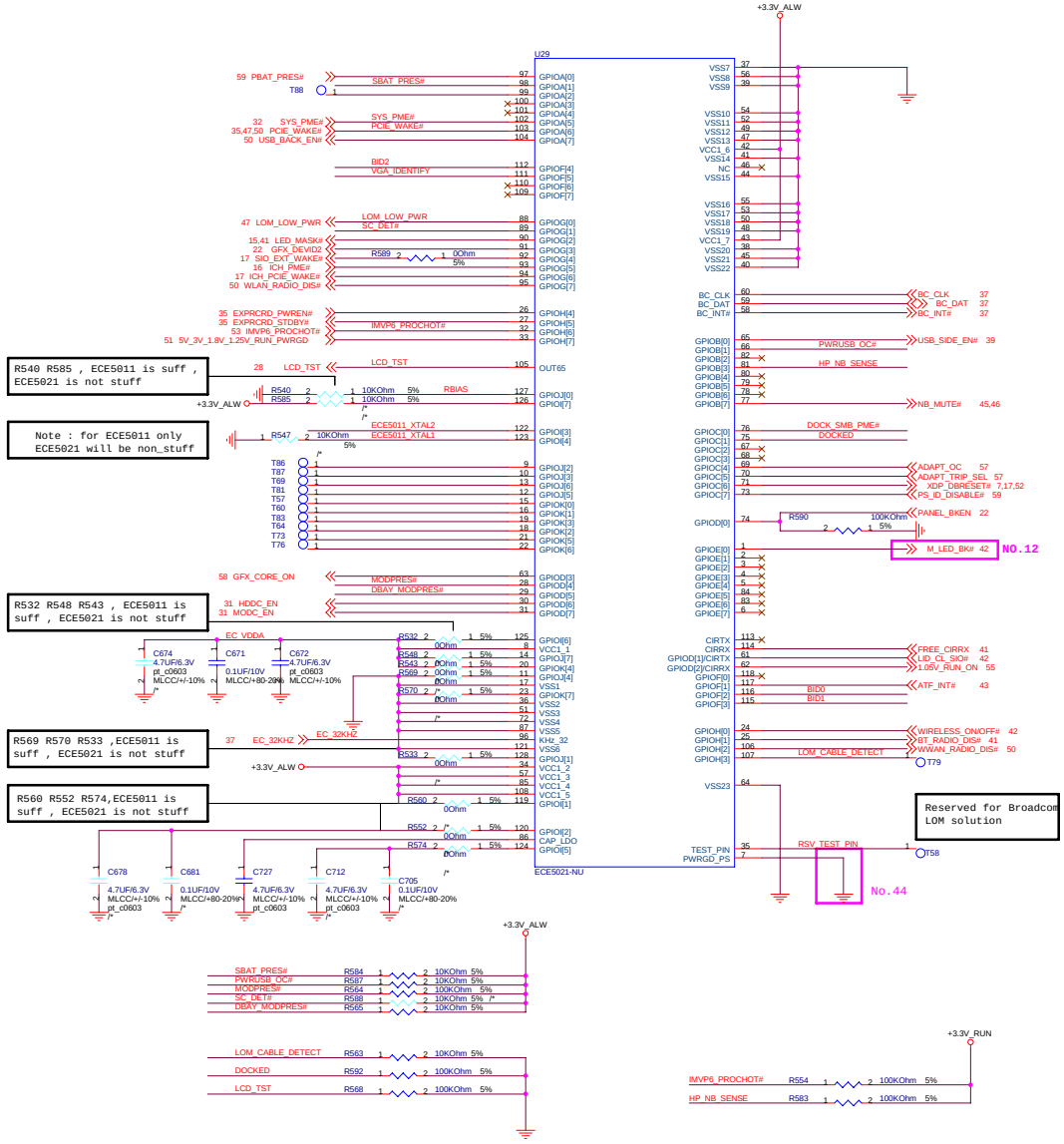




BID2	BID1	BID0	M08	M08B
0	0	0	ENG1(X00)	ENG1(X00)
0	0	1	ENG2(X01)	ENG2(X01)
0	1	0	ENG3(X02)	ENG3(X02)
0	1	1	ENG4(X03)	ENG4(X03)
1	0	0	QT(X04)	QT(X04)
1	0	1	RAMP(A00)	RAMP(A00)
1	1	0		

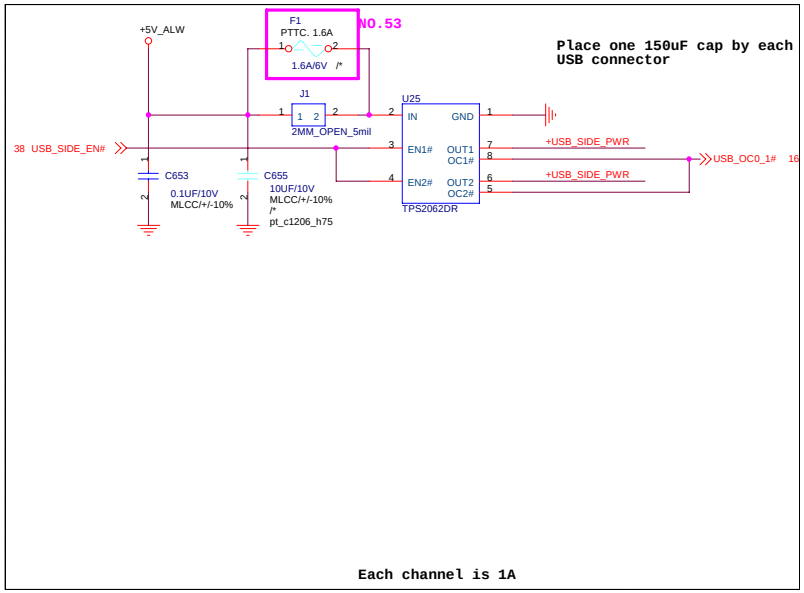


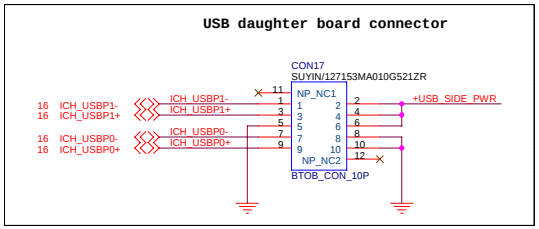




<Variant Name>

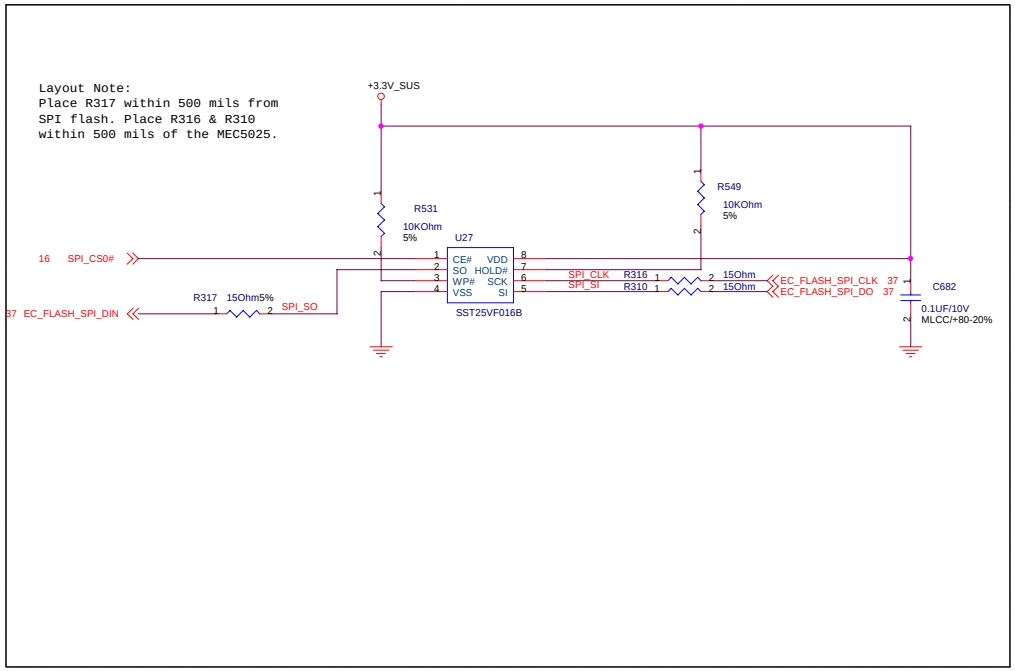
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	SHEET 38 OF 69	DESCRIPTION: ECE5021	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : STANLY_HSU

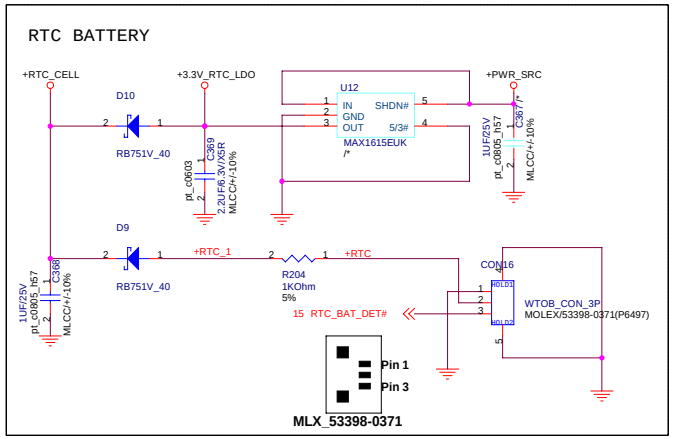




<Variant Name>

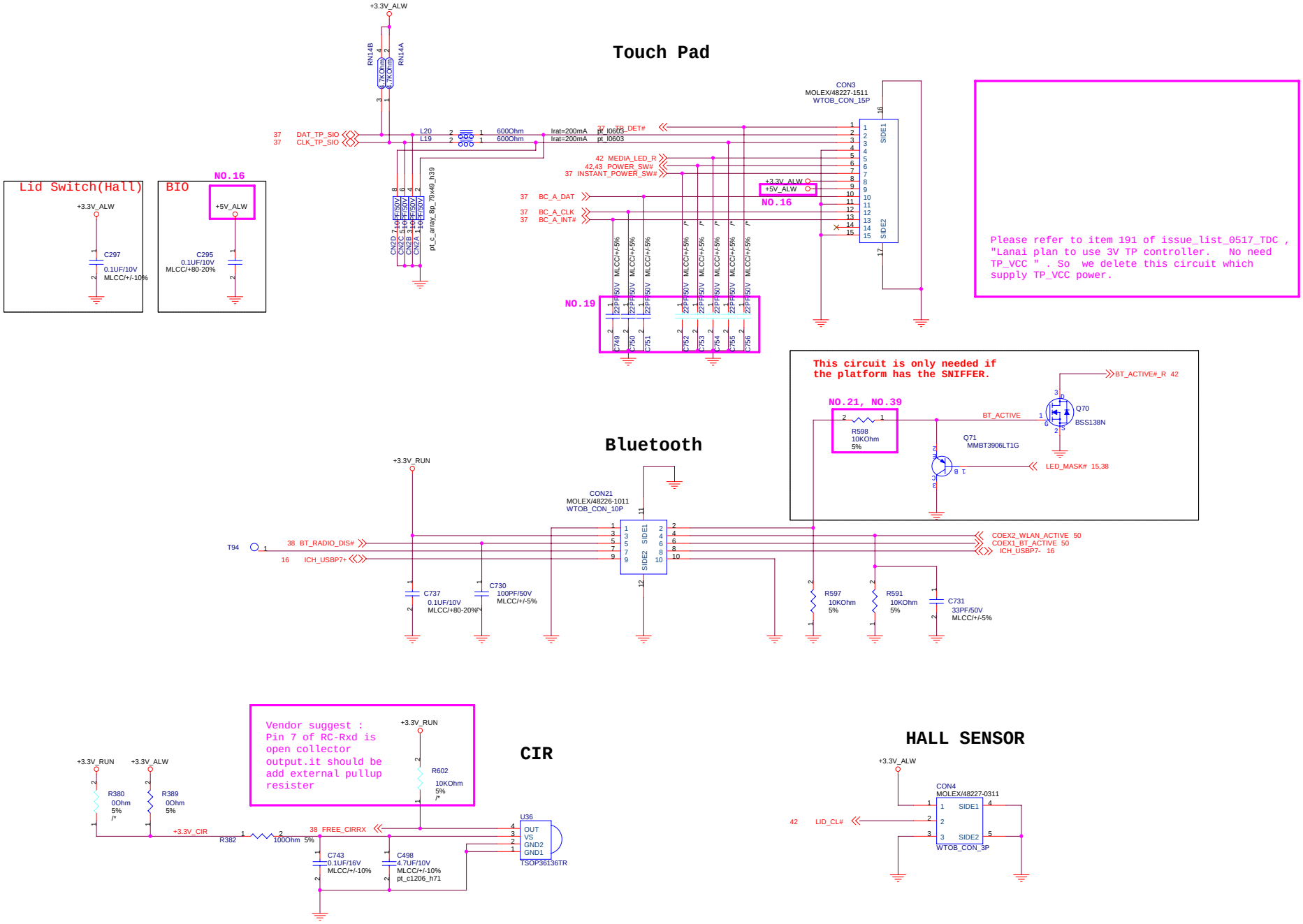
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***USB PORT x 2***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Terry_Lin***
		SHEET **39** OF **69**		RELEASE DATE :		





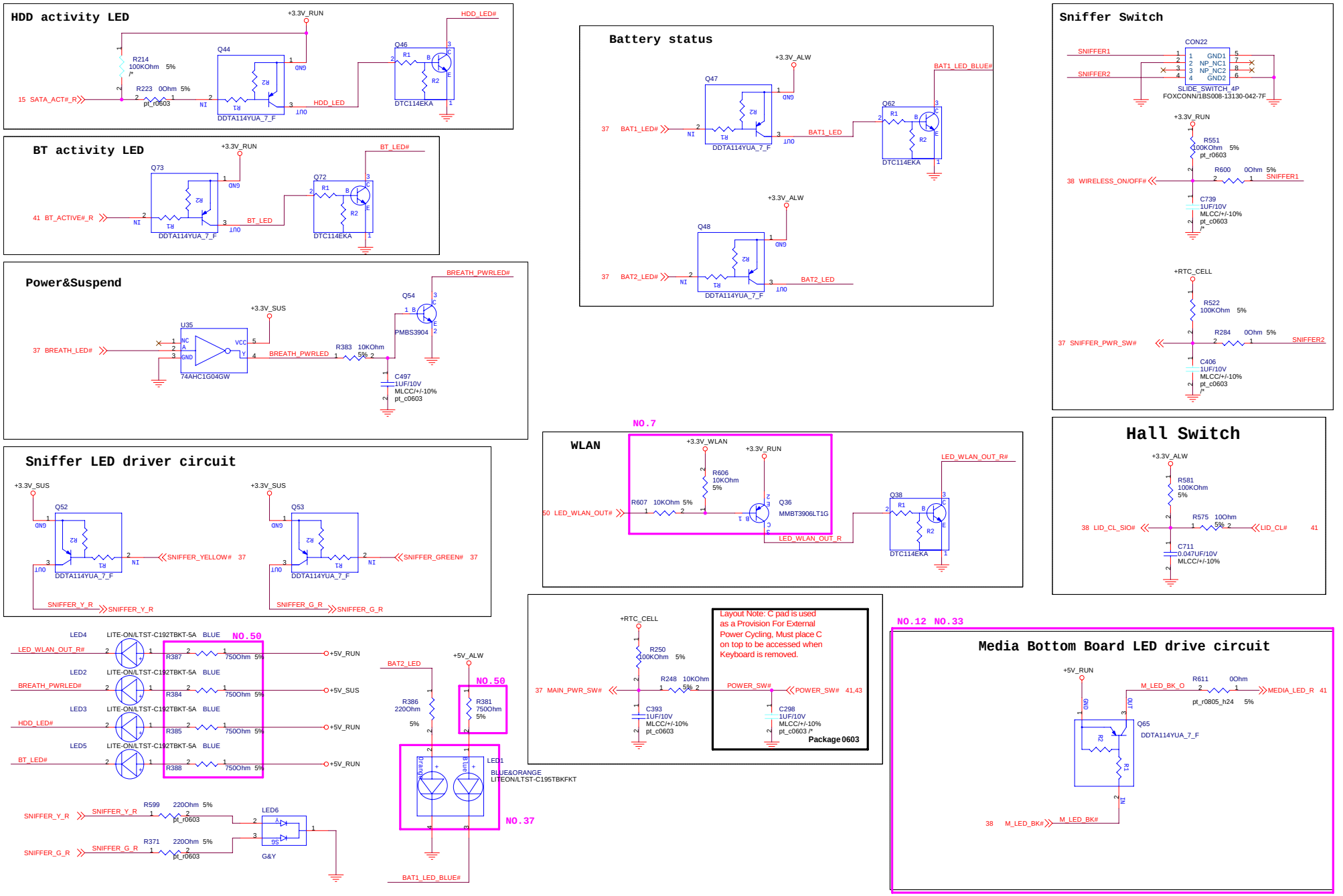
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***FLASH & RTC***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***C.L. Ho***
		SHEET **40** OF **69**		RELEASE DATE :		



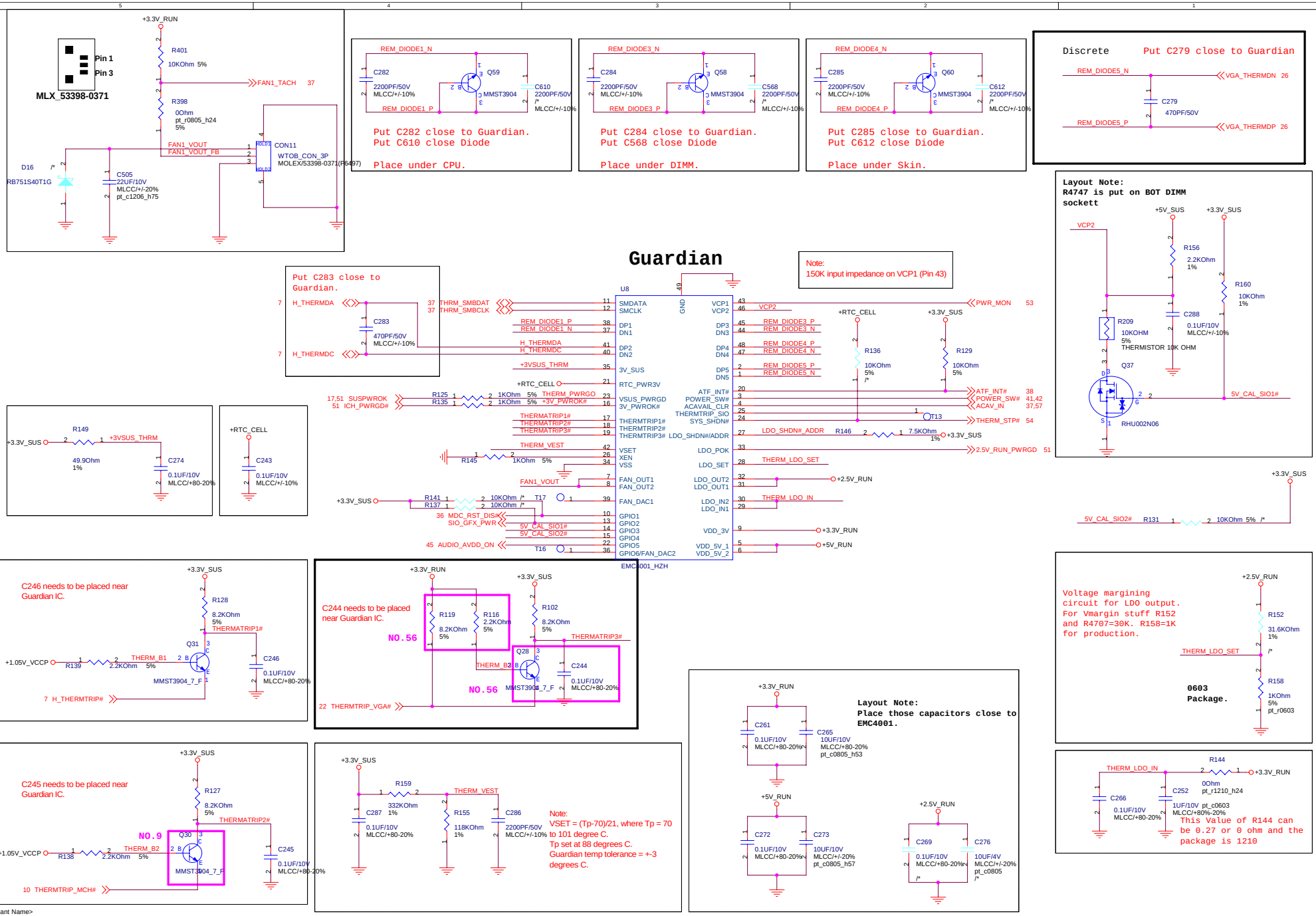
<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	SHEET 41 OF 69	DESCRIPTION: TOUCH PAD & BT & CIR & HD	SCHEMATIC FILE NAME : <OrgName>	RELEASE DATE :	DESIGN ENGINEER : Terry_Lin



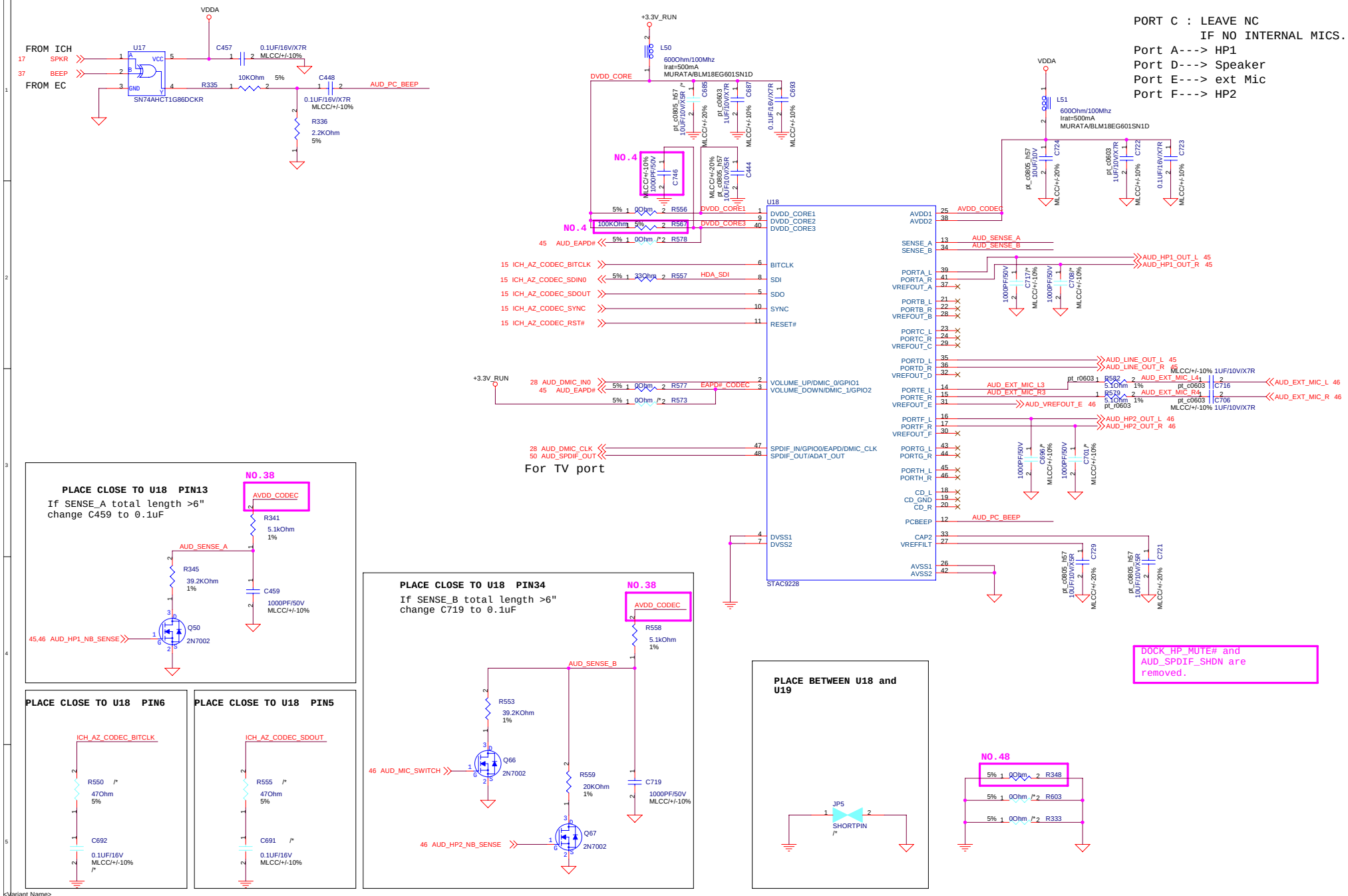
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***SWITCH & LED***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Ivan_Chou***
		SHEET **42** OF **69**		RELEASE DATE :	



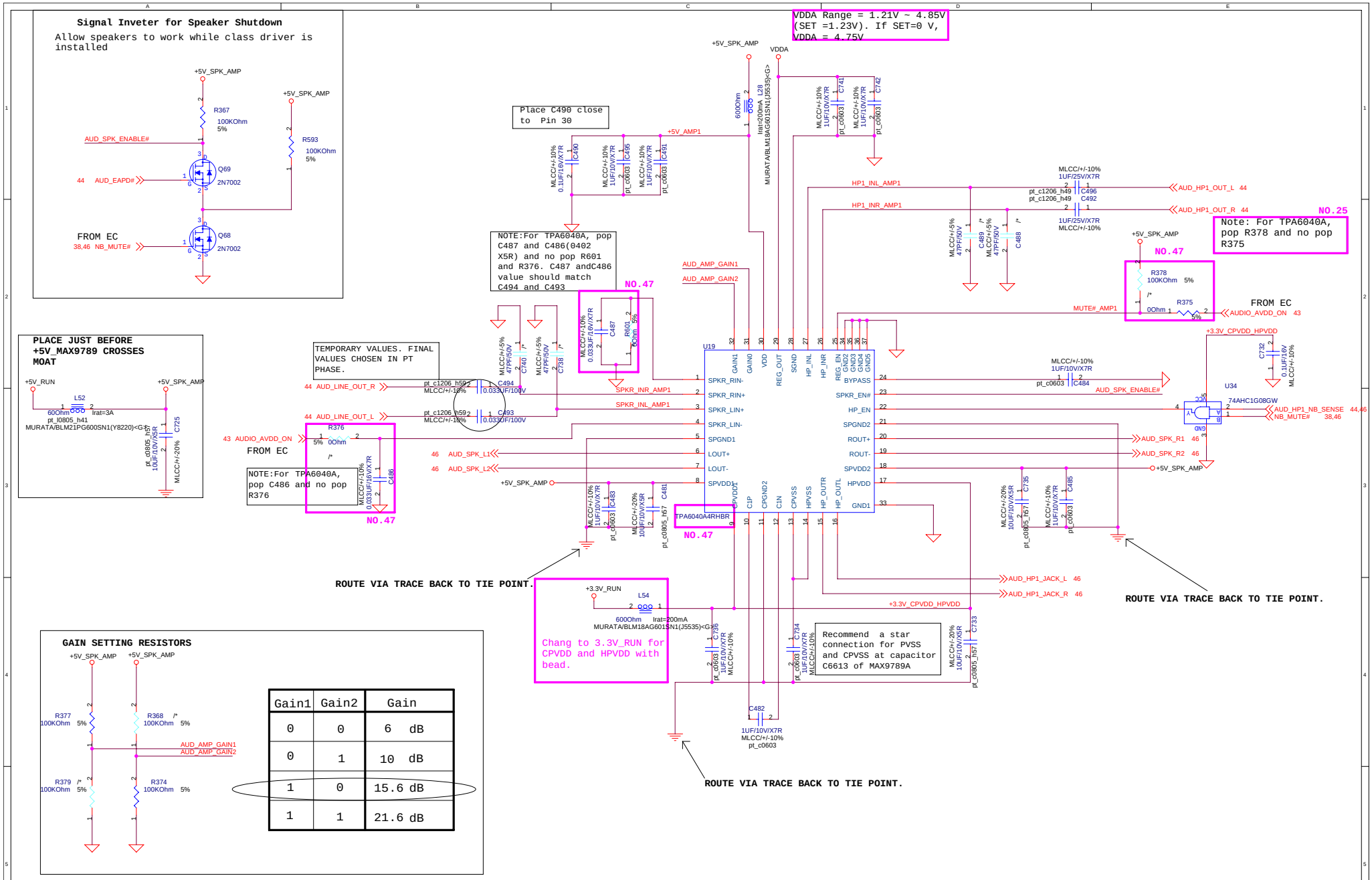
<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	SHEET 43 OF 69	DESCRIPTION: EMC4001	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : STANLY_HSU



<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***STAC9228***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Yihao Yeh***
		SHEET **44** OF **69**		RELEASE DATE :	



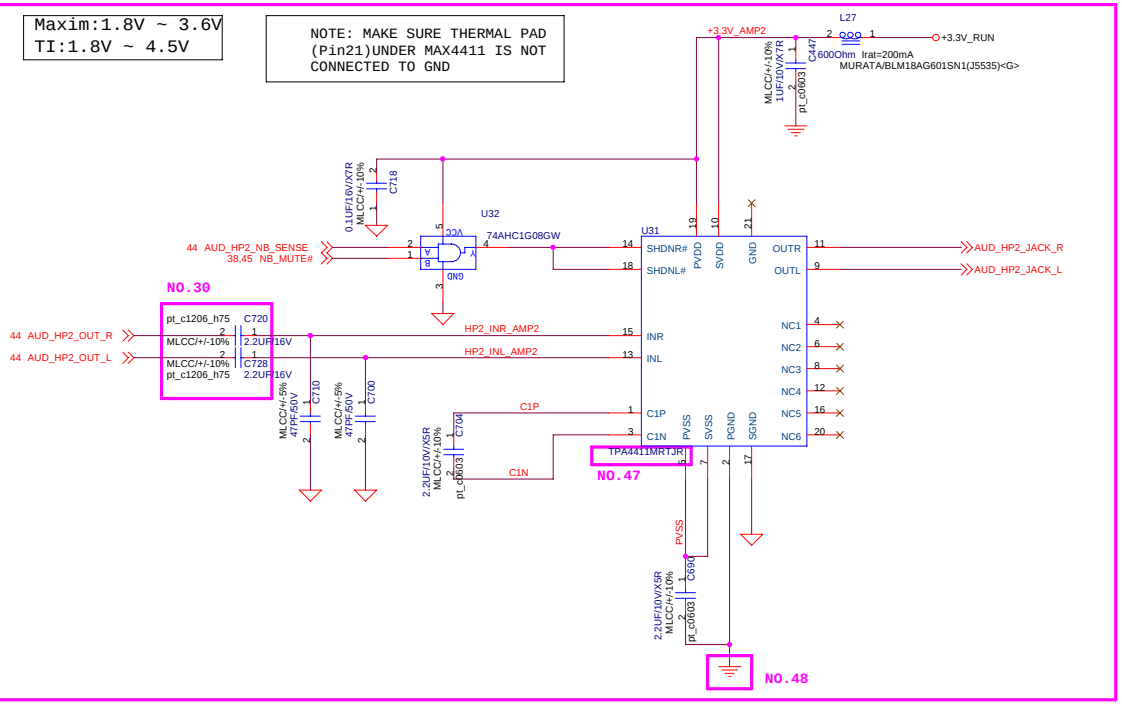
Gain1	Gain2	Gain
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

<Variant Name>

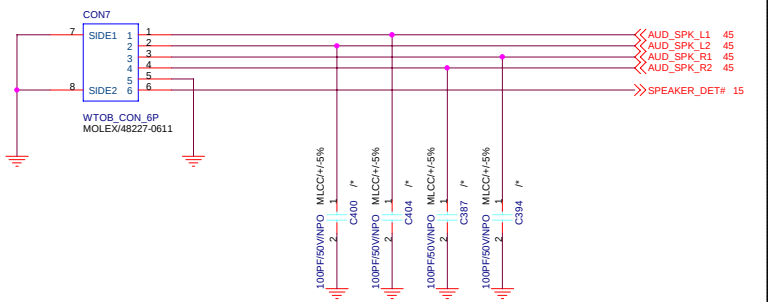
PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *AMP MAX9789*	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :	*Yihao Yeh*
		SHEET 45 OF 69		RELEASE DATE :			

Maxim:1.8V ~ 3.6V
TI:1.8V ~ 4.5V

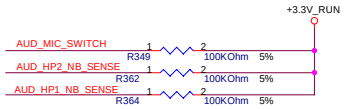
NOTE: MAKE SURE THERMAL PAD (Pin21)UNDER MAX4411 IS NOT CONNECTED TO GND

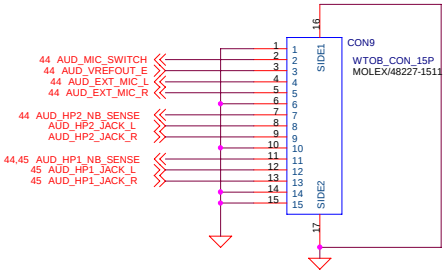


Speaker CON



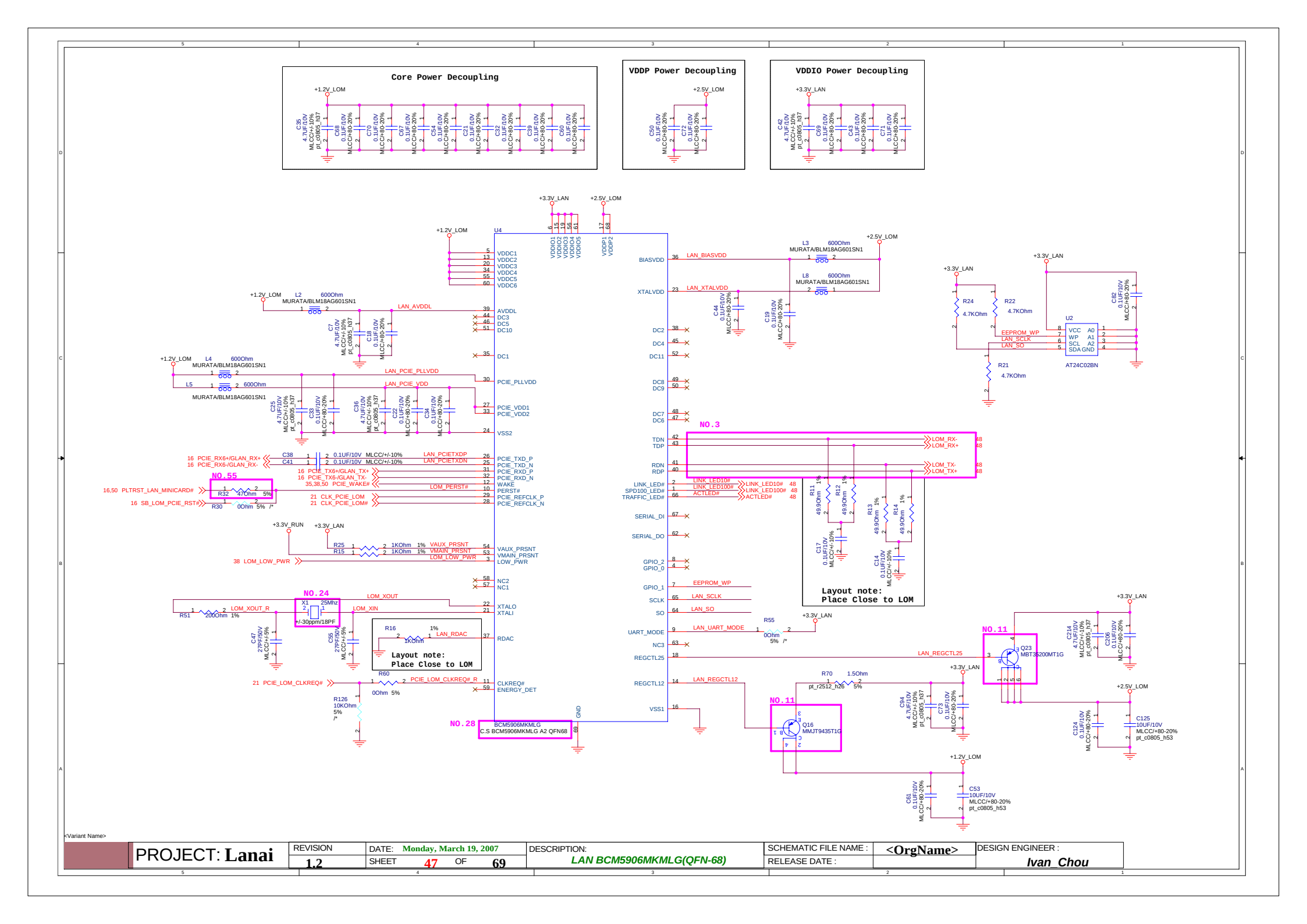
Need to adjust EMI cap values as necessary.





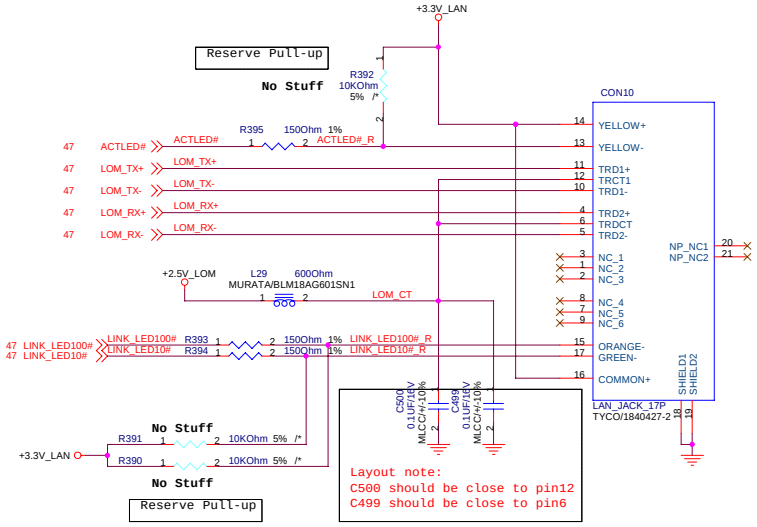
<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 46 OF 69	DESCRIPTION: AMP MAX4411 & AUDIO JACK	SCHEMATIC FILE NAME : <OrgName> RELEASE DATE :	DESIGN ENGINEER : Yihao Yeh



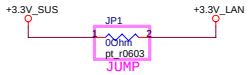
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***LAN BCM5906MKMLG(QFN-68)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Ivan_Chou***
		SHEET **47** OF **69**		RELEASE DATE :	



+3.3V_LAN Source Guideline:

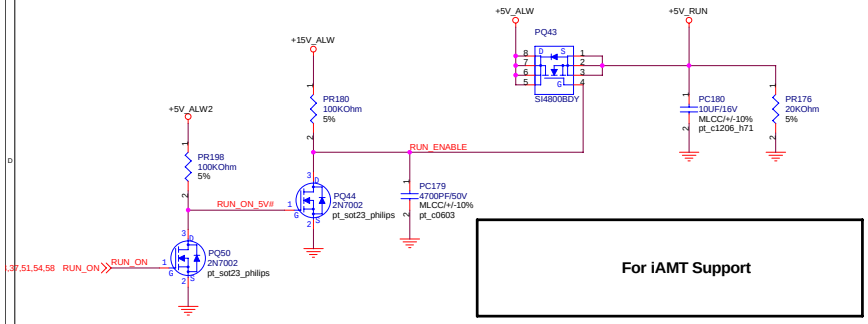
1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V_SRC if Wake-on_LAN is required out of S4, S5



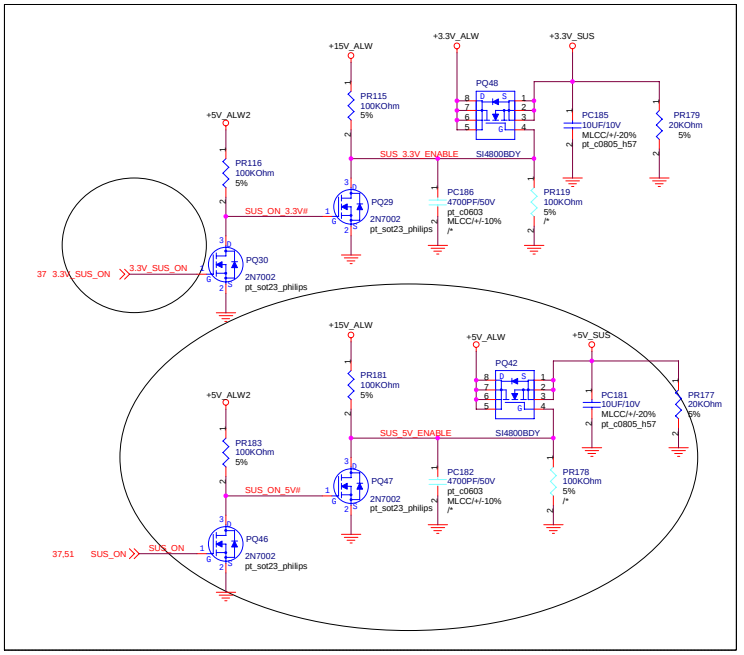
Per EE schematic checklist item.87: Only support wake up from S3

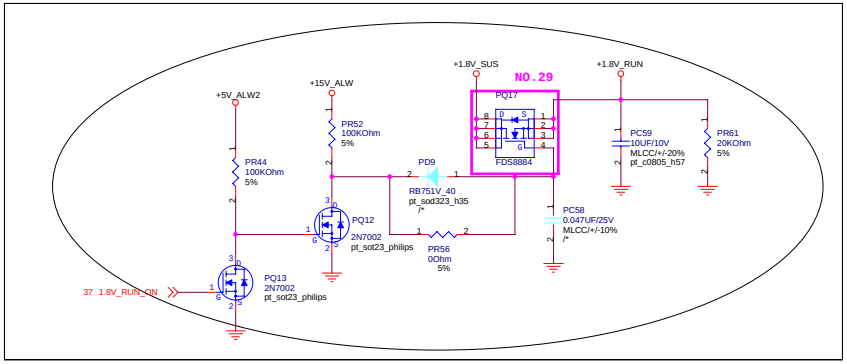
<Variant Name>

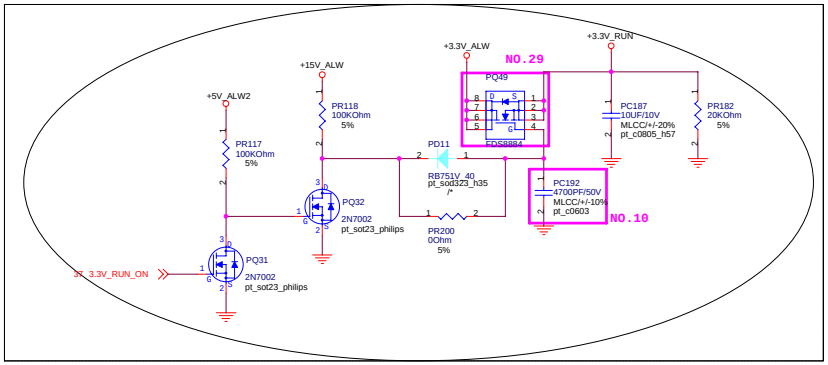
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***Magnetics and RJ-45***	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 48 OF 69		RELEASE DATE :		*Ivan_Chou*

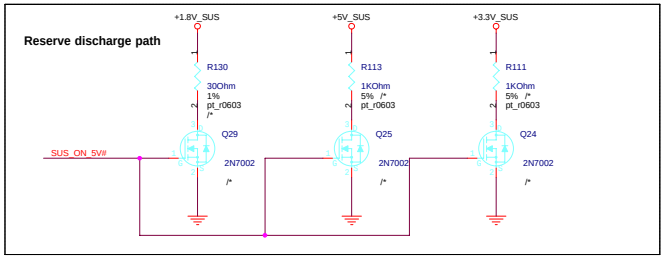


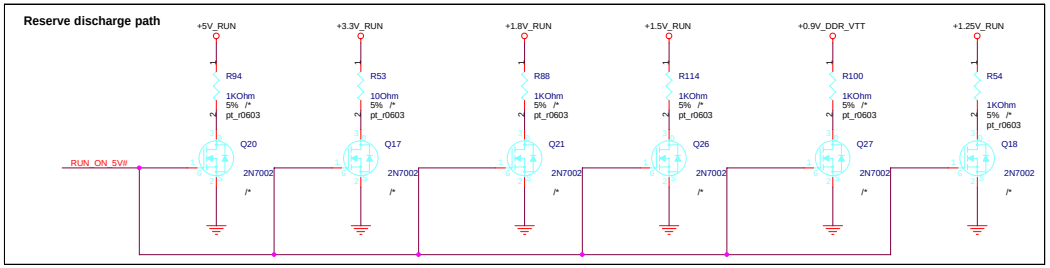
For iAMT Support









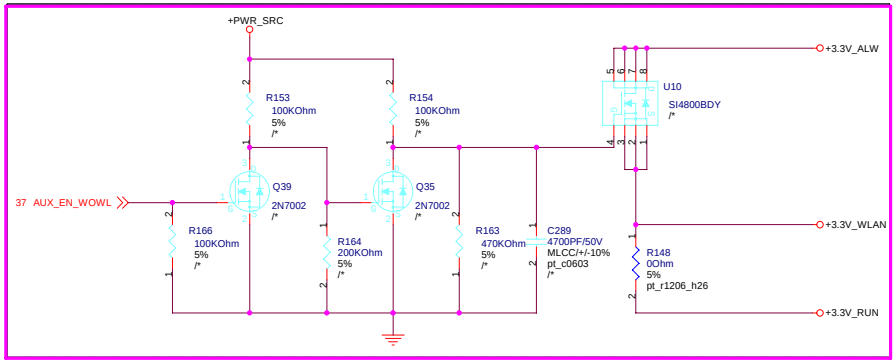


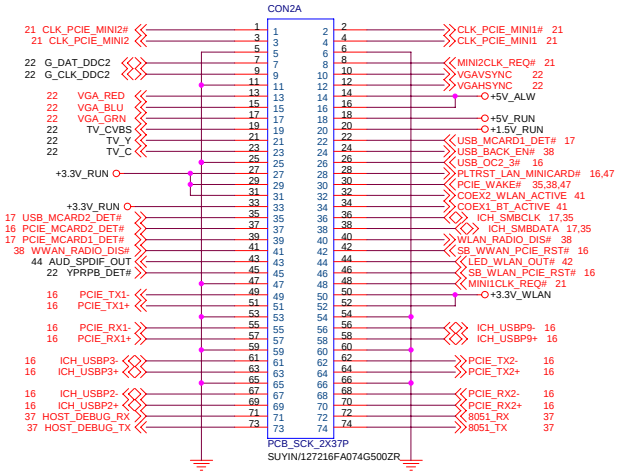
For iAMT Support

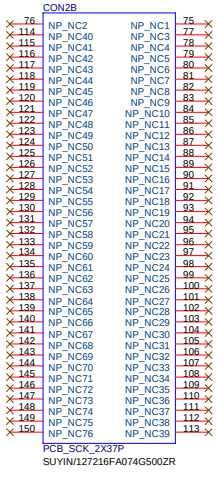
<Variant Name>

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Power Control Switch*	SCHEMATIC FILE NAME :		DESIGN ENGINEER : *Eric Ko*
		SHEET 49 OF 69		RELEASE DATE :		

NO.20

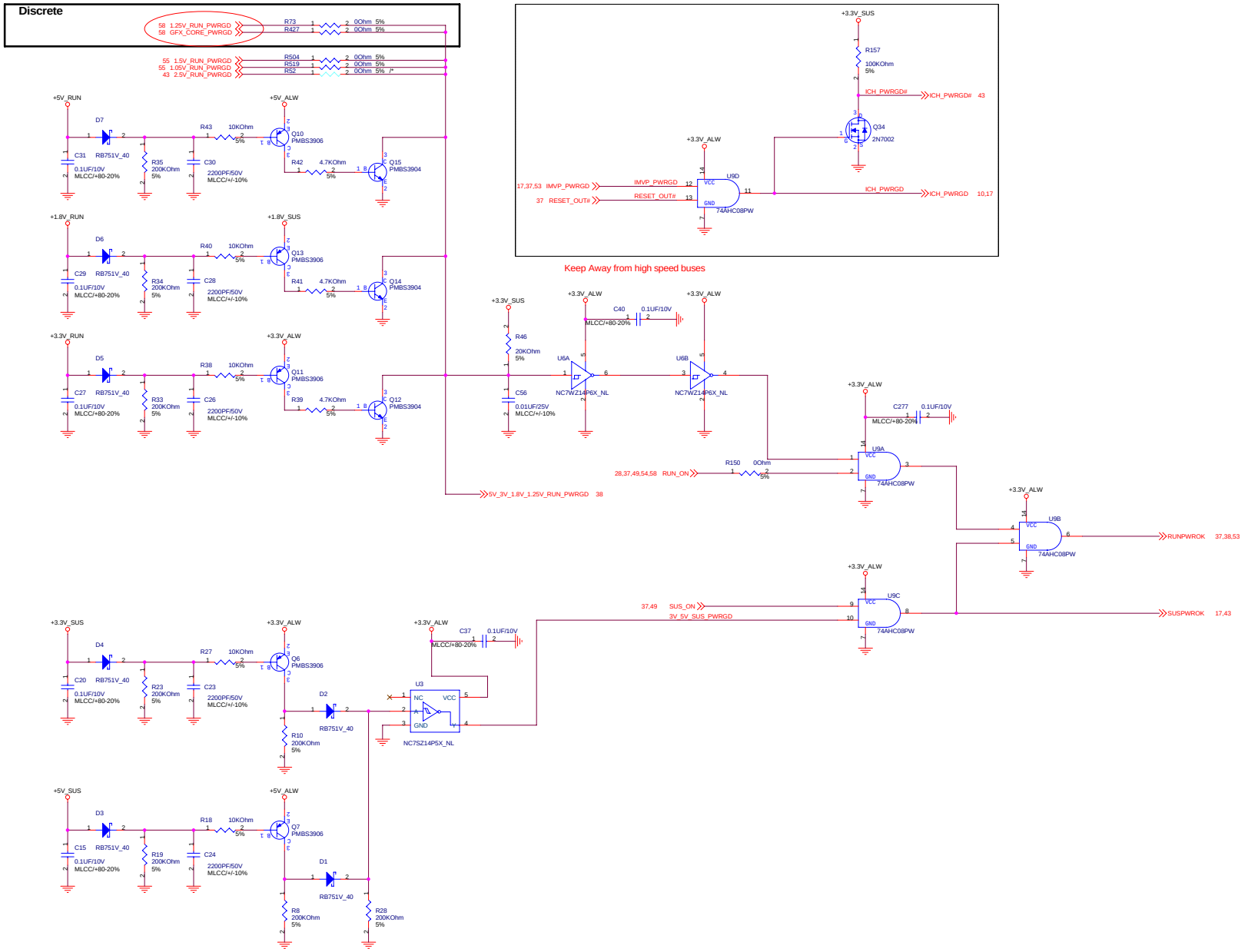






<Variant Name>

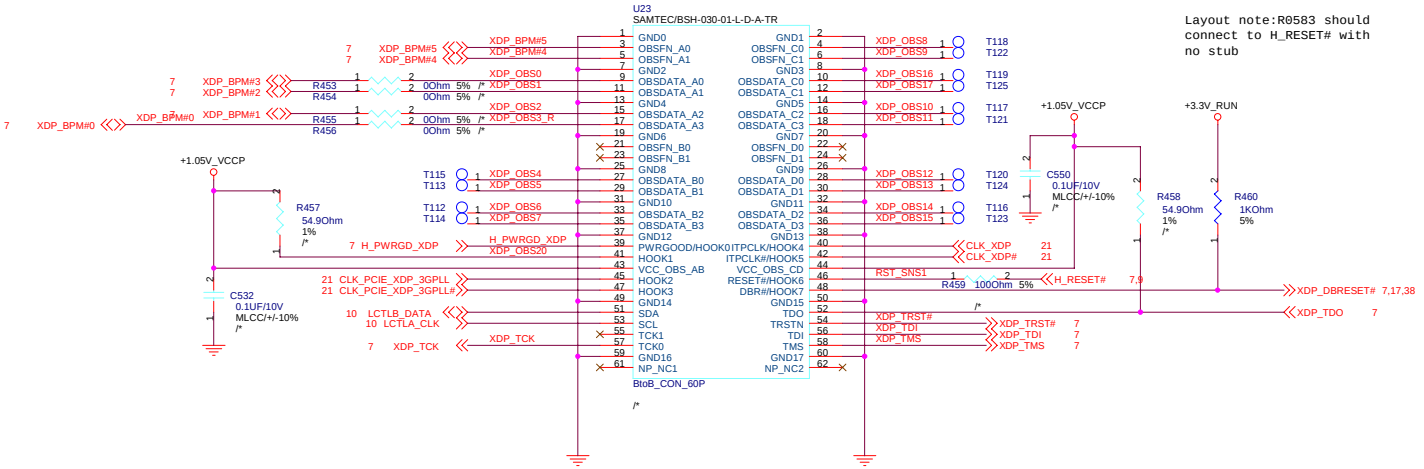
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***BtoB CON***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***STANLY_HSU***
		SHEET **50** OF **69**		RELEASE DATE :	



<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	SHEET 51 OF 69	DESCRIPTION: Power Sequence Logic	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : C.L. Ho

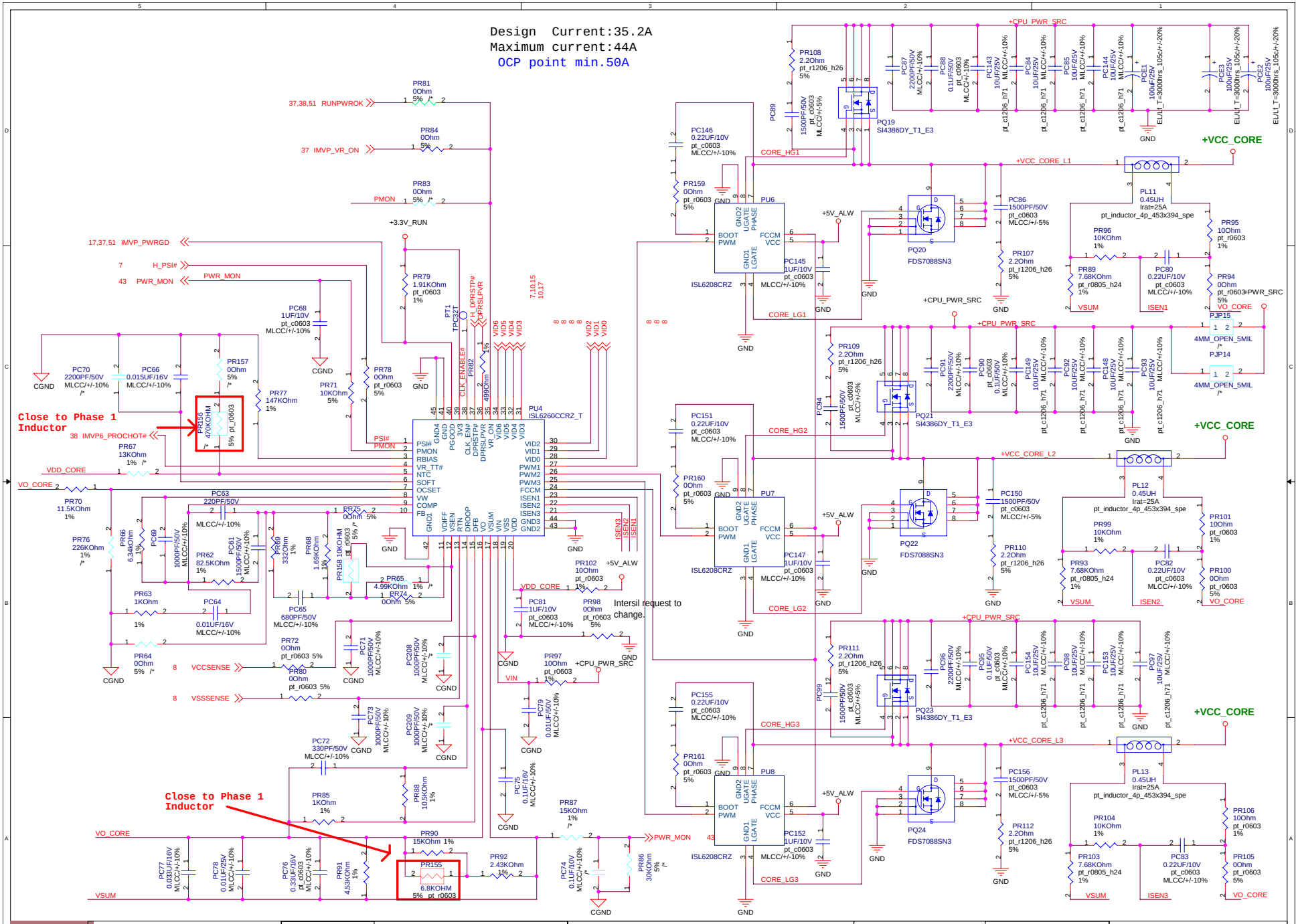
XDP

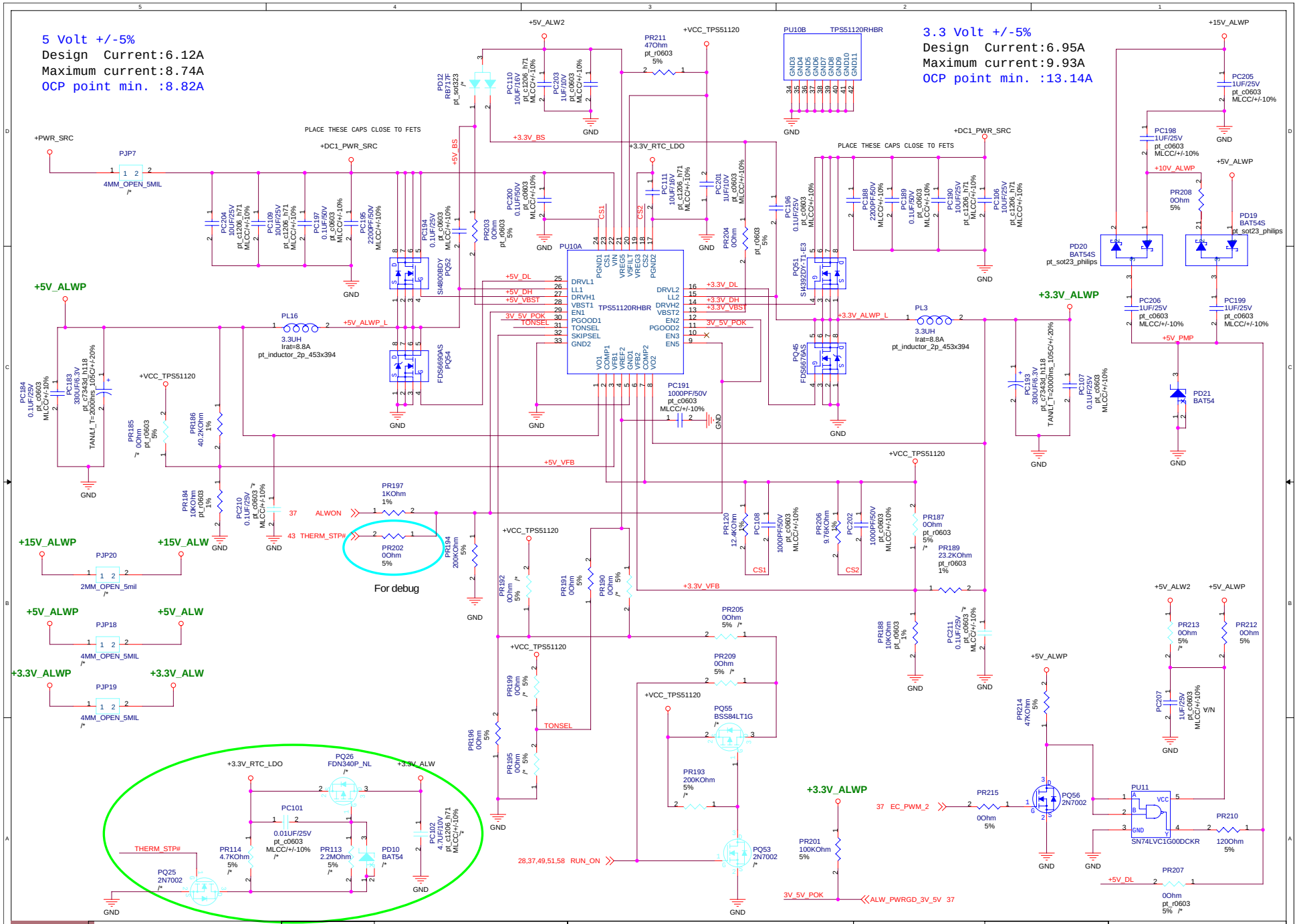


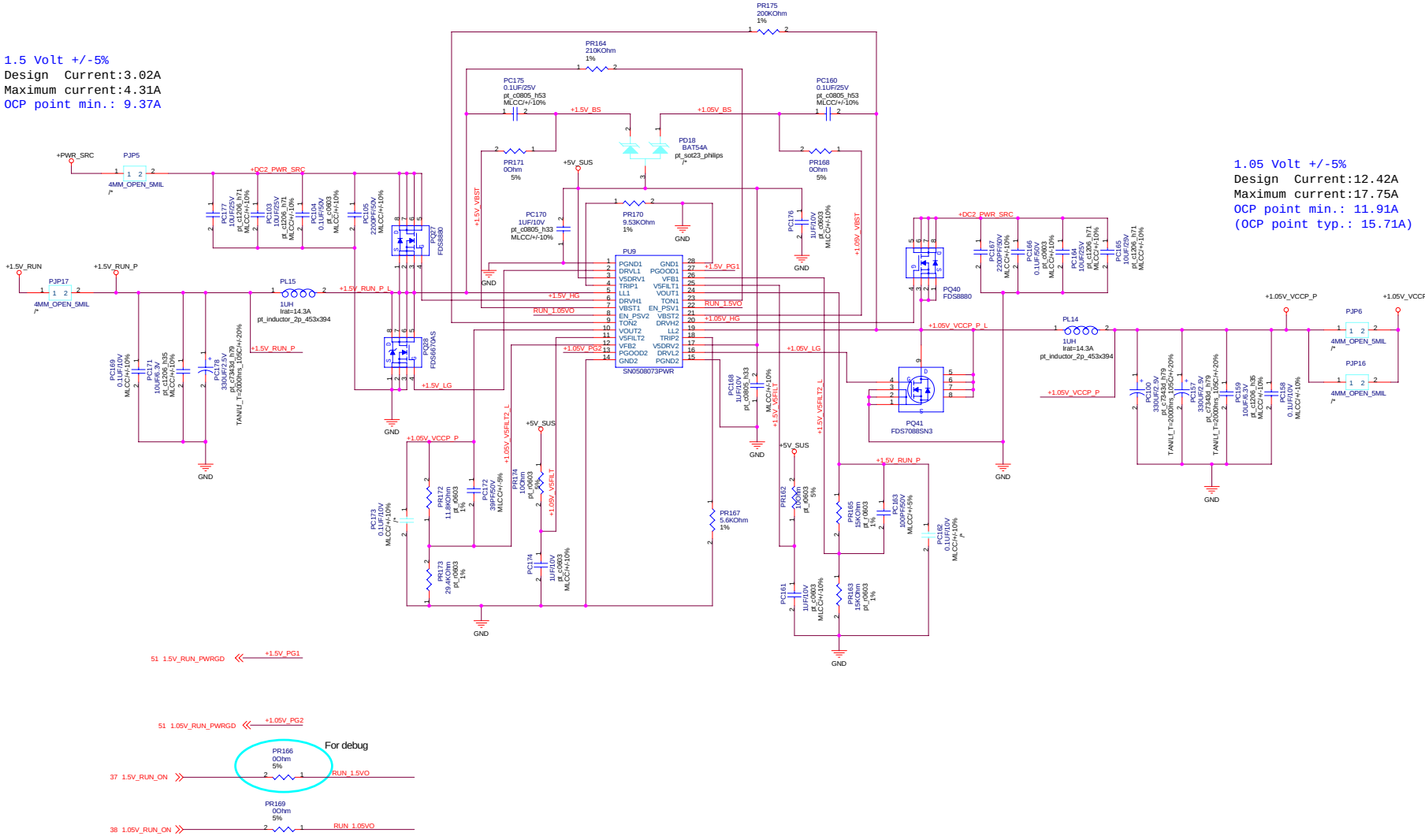
CAD NOTE:
Place the XDP connector on the primary side of the CRB and place all components near the connector.

<Variant Name>

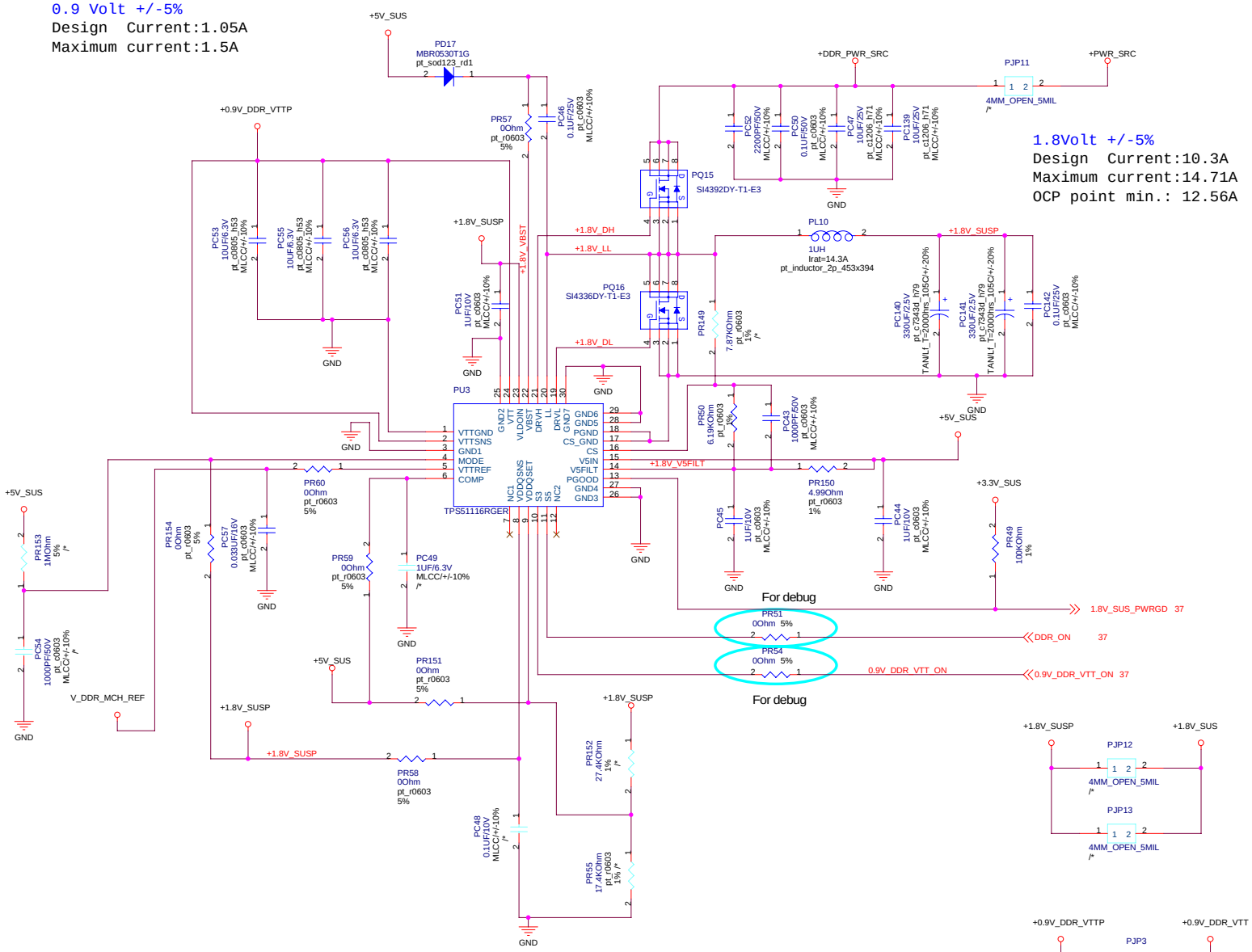
PROJECT: **Lanai**	REVISION: **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***XDP***	SCHEMATIC FILE NAME: **<OrgName>**	DESIGN ENGINEER: ***Terry_Lin***	
		SHEET **52** OF **69**		RELEASE DATE:		


Design Current:35.2A
Maximum current:44A
OCP point min.50A
Close to Phase 1 Inductor
Close to Phase 1 Inductor
Intersil request to change.
+VCC_CORE
+CPU_PWR_SRC
+5V_ALW
+3.3V_RUN
PU4 ISL6260CCRZ_T
PU6 ISL6208CRZ
PU7 ISL6208CRZ
PU8 ISL6208CRZ
PQ19 SI4386DY_T1_E3
PQ20 FDS7088SN3
PQ21 SI4386DY_T1_E3
PQ22 FDS7088SN3
PQ23 SI4386DY_T1_E3
PQ24 FDS7088SN3
PROJECT: Lanai
REVISION 1.1
DATE: Monday, March 19, 2007
SHEET 53 OF 69
DESCRIPTION: POWER_VCORE
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : JEFF


5 Volt +/-5%
Design Current:6.12A
Maximum current:8.74A
OCP point min. :8.82A
3.3 Volt +/-5%
Design Current:6.95A
Maximum current:9.93A
OCP point min. :13.14A
TPS51120RHBR
PLACE THESE CAPS CLOSE TO FETS
For debug
PROJECT: Lanai
REVISION 1.1
DATE: Monday, March 19, 2007
SHEET 54 OF 69
DESCRIPTION: POWER_SYSTEM 5V_ALW&3.3V_ALW
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : JEFF

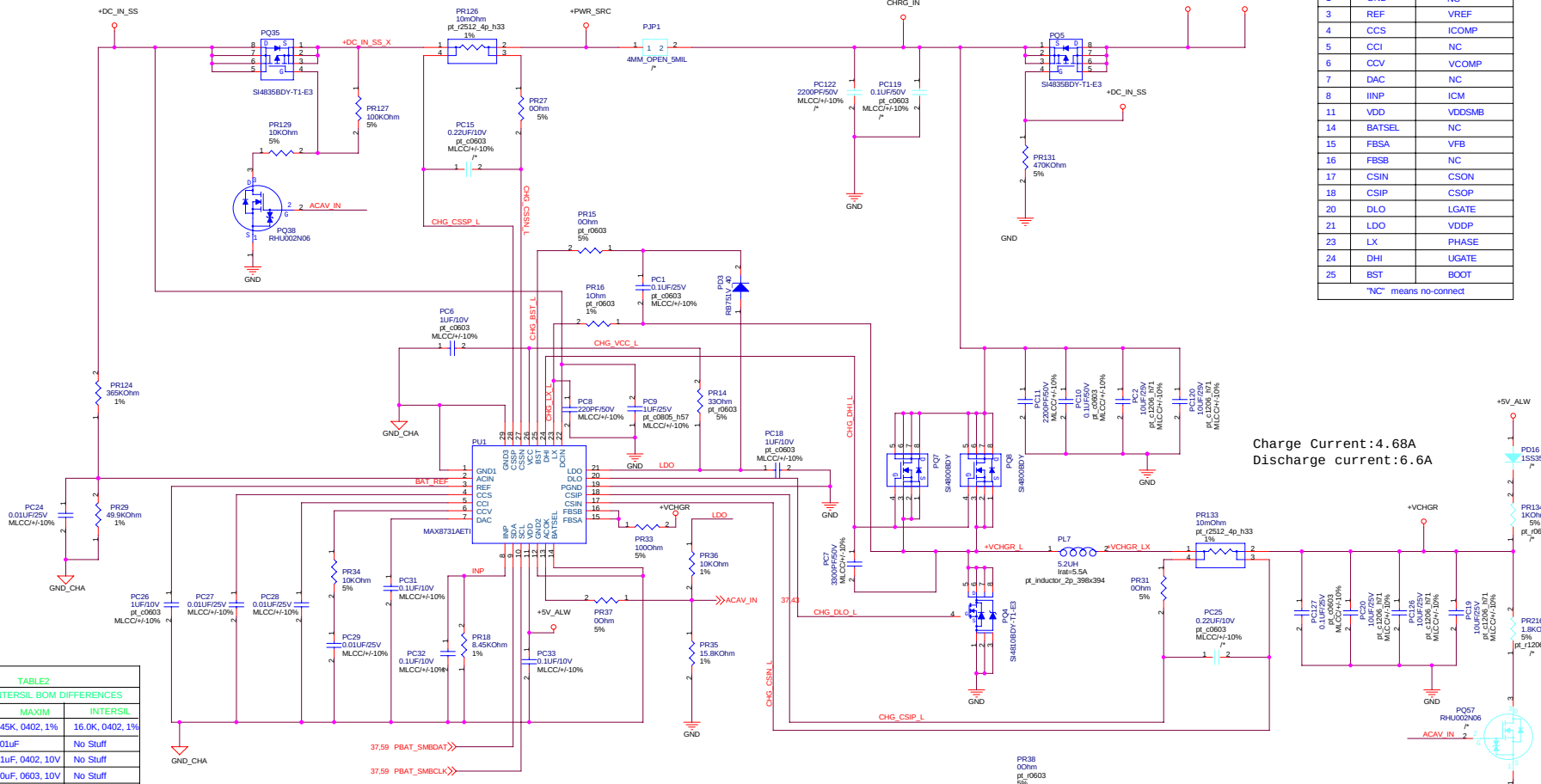


PROJECT: **Lanai**	REVISION: 1.1	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 55 OF 69	POWER I/O 1.5VS & 1.05VS	RELEASE DATE :		JEFF



PROJECT: **Lanai**	REVISION: 1.1	DATE: Monday, March 19, 2007	DESCRIPTION: ***POWER_I/O_DDR & VTT***	SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName>	DESIGN ENGINEER : ***JEFF***
		SHEET 56 OF 69			

TOTAL POWER=90W
-->4.62A



Charge Current:4.68A
Discharge current:6.6A

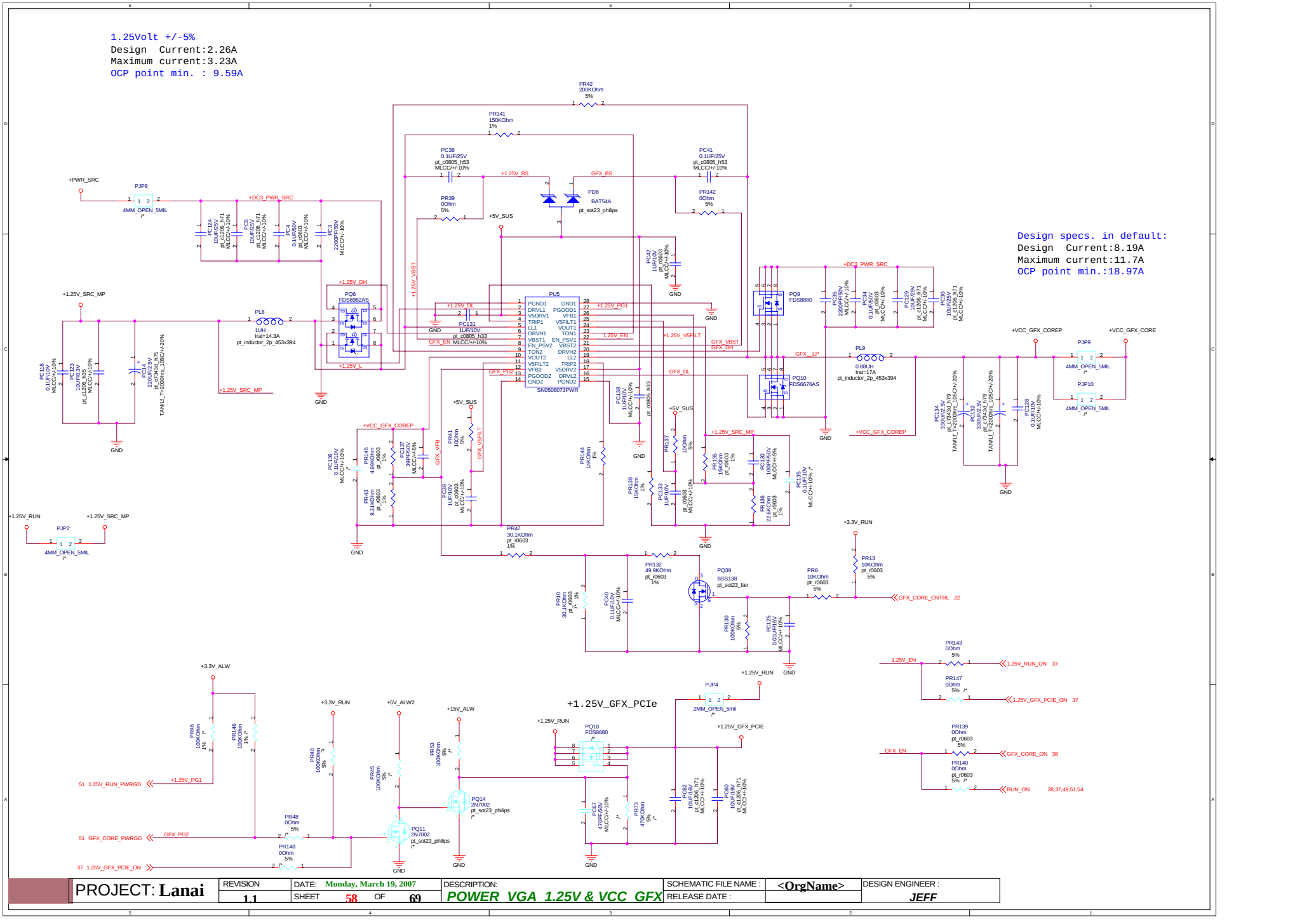
TABLE3		
PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT
"NC" means no-connect		

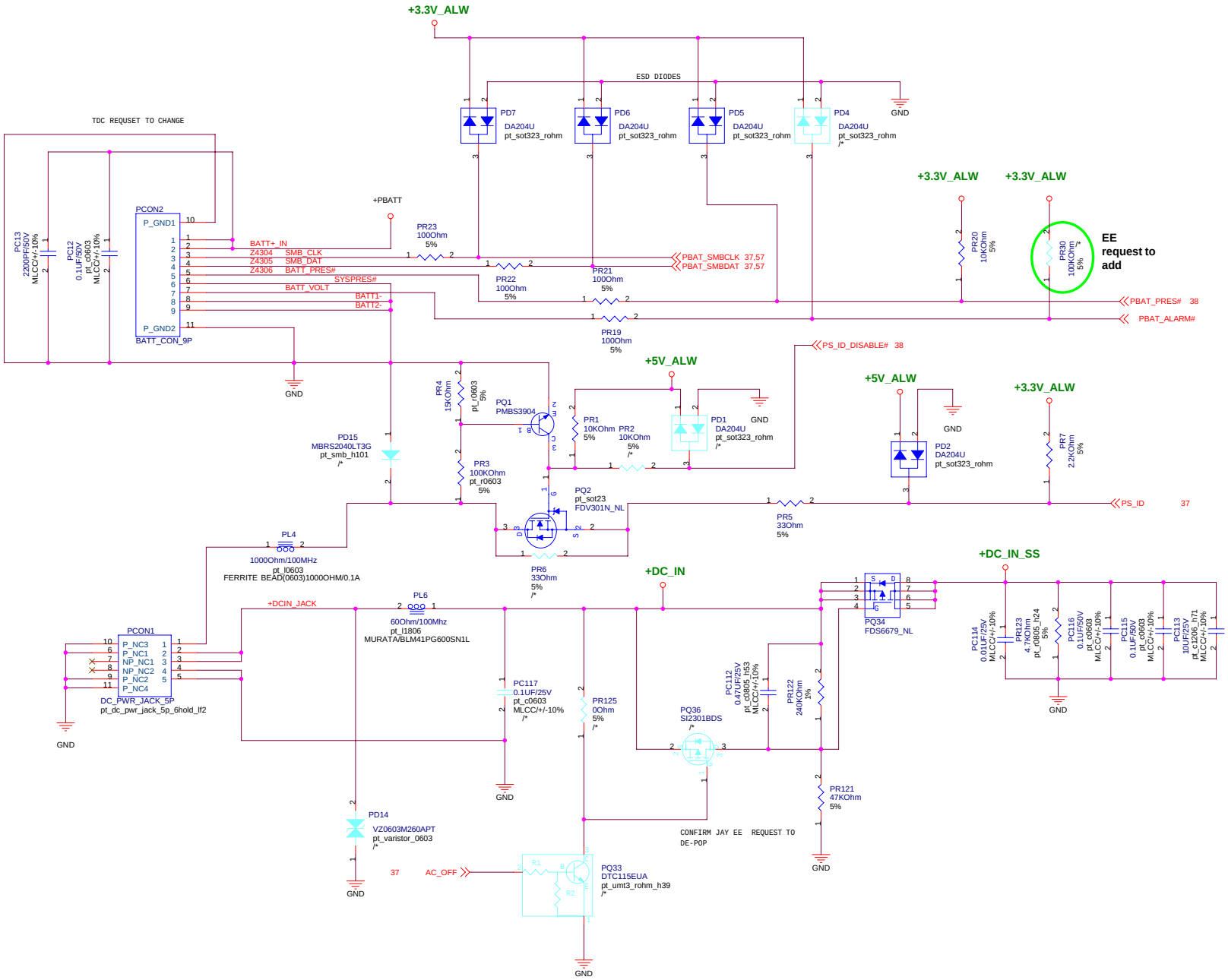
TABLE2		
MAXIM & INTERSIL BOM DIFFERENCES		
REF DES	MAXIM	INTERSIL
PR18	8.45K, 0402, 1%	16.0K, 0402, 1%
PC22	0.01uF	No Stuff
PC32	0.1uF, 0402, 10V	No Stuff
PC26	1.0uF, 0603, 10V	No Stuff
PR124	365K, 0402, 1%	215K, 0402, 1%
PR31	0, 0402, 5%	10, 0402, 5%
PR27	0, 0402, 5%	10, 0402, 5%
PC25	No Stuff	0.22uF
PC15	No Stuff	0.22uF
PC28	0.01uF	No Stuff
PC31	0.1uF, 0402, 10V	No Stuff
PC8	220pF, 0402, 50V	No Stuff
PD3	RB751V-40	No Stuff
PC7	3.3nF	No Stuff
PR16	1, 0603, 1%	0, 0603, 5%
PR33	100, 0402, 5%	0, 0402, 5%
PR34	4.7K, 0402, 5%	4.7K, 0402, 5%
PC29	0.01uF	0.01uF
PC27	0.01uF	0.01uF
PD16	1SS355	No stuff
PR134	1K, 0603, 5%	No stuff

TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR32	PR17	PR12	PR24
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR24 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor
Note 2: 24.9K at PR24 allows the 65W adaptor setting to switch down to 45W. (now is 33.2K for 90W)
Note 3: PR126 must be 5m ohm instead of 10m ohm for the 230W adaptor

PROJECT: Lanai	REVISION 1.1	DATE: Monday, March 19, 2007	DESCRIPTION: POWER_CHARGER	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : JEFF
		SHEET 57 OF 69		RELEASE DATE :	


1.25Volt +/-5%
Design Current:2.26A
Maximum current:3.23A
OCP point min. : 9.59A
Design specs. in default:
Design Current:8.19A
Maximum current:11.7A
OCP point min.:18.97A
+1.25V_GFX_PCIe
PROJECT: Lanai
REVISION 1.1
DATE: Monday, March 19, 2007
SHEET 58 OF 69
DESCRIPTION: POWER VGA 1.25V & VCC GFX
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : JEFF



PROJECT: **Lanai**	REVISION **1.1**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***POWER_CONNECTOR***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***JEFF***
		SHEET **59** OF **69**		RELEASE DATE :		

PM screw pad

H1
C256I138D118

H2
CT315B295I158D118

H3
CRT354X315B394D138

H4
CRT337X413B394D138

13G021049200DE

H5
ESA1-1A_NUT_M2_H2.5_1

H6
O118X98DO118X98N

13G021049200DE

H7
ESA1-1A_NUT_M2_H2.5_2

H8
C98D98N

13G021052020DE

H9
ESA1-1A_NUT_M2_H7_1

H10
O47X31DO47X31N

13G021052020DE

H11
ESA1-1A_NUT_M2_H7_2

H12
RT197X413D91

H13
CT315B394I158D138

H14
CT315B394I158D138

CPU

H15
CT295B276I158D138

H30
CT295B276I162D142

H31
CT295B276I162D142

H32
CT295B276DO138X154

13G021052010DE

H18
ESA1-1A_NUT_M2_H8

H17
CT354B295I158D138

H37
CT354B295I177D157

SATA

H20
CT236B217D102

H33
CT236B217D102

H21
CT138B295D118

Header2 13G021052030DE

H24
CRT335X386B276D138

H25
ESA1-1A_NUT_H0.4

H34
ESA1-1A_NUT_H0.4

H26
CRT394X413B394D138

H35
CRT394X413B394D138

Shielding case

H27
O43X98DO20X75

H38
O43X98DO20X75

H28
CT315B394I158D138

H36
CT315B394I158D138

H29
crt413x394b394d138

SPRING1
EMI_SPRING_PAD
/*

PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***SCREW PAD***	SCHEMATIC FILE NAME :		DESIGN ENGINEER : ***Sean Kuo***
		SHEET **60** OF **69**		RELEASE DATE :		

ASUS CONFIDENTIAL

MODEL NAME : ***Elsa***

PCB NO : ***???***

ASUS P/N : ***???***

Lanai USB Board

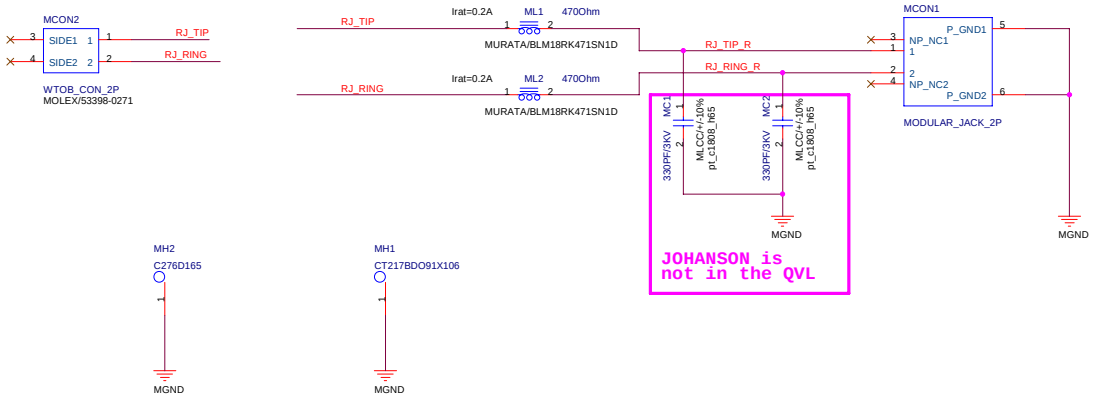
REV :1.1(DELL: X01)

MB PCB

Part Number	Description
DA80004H0L	PCB 00B LA-3071P REV0 M/B

BOM NO. ???
PCB P/N: ???

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007** SHEET **65** OF **69**	DESCRIPTION: ***Cover Page***	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : ***Terry Lin***



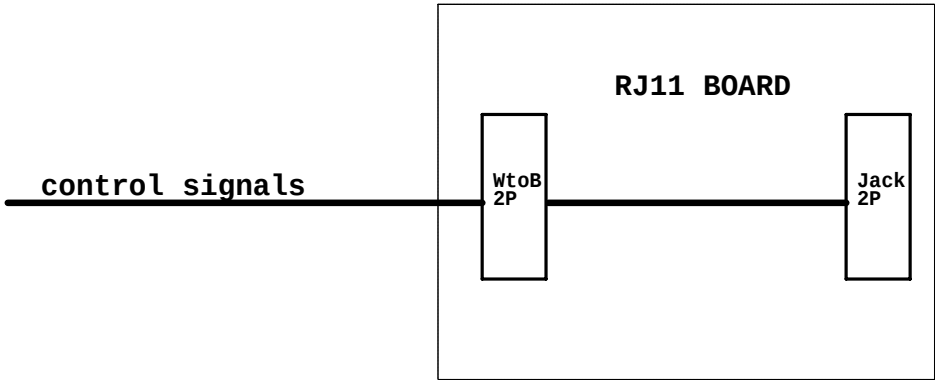
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***RJ-11 CONN***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Stanly_Hsu***
		SHEET **66** OF **69**		RELEASE DATE :		

ASUS CONFIDENTIAL

MODEL NAME : *Elsa*

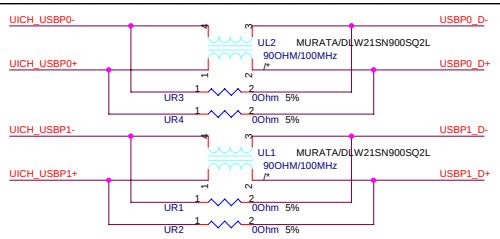
Lanai Modem Board

REV :1.1(DELL: X01)

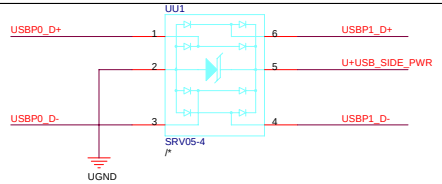


PROJECT: **Lanai**	REVISION: **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***BLOCK DIAGRAM***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Stanly_Hsu***
		SHEET **68** OF **69**		RELEASE DATE :	

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .



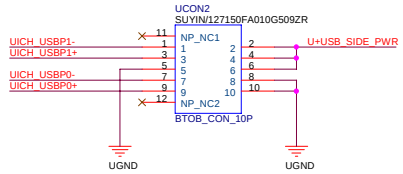
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



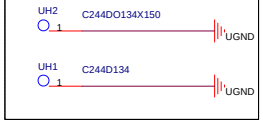
Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C (1pf vs 3pf).

Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines.
Add PADS ONLY until proven diodes are really needed.

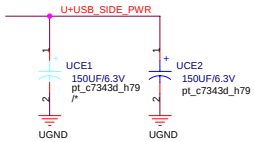
USB daughter board connector



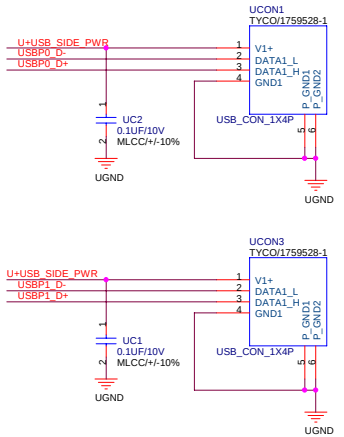
Screw hole



Place one 150uF cap by each USB connector



Each channel is 1A



PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: **USB PORT (SINGLE *2)**	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Terry_Lin
		SHEET 69 OF 69		RELEASE DATE :	