ASUS CONFIDENTIAL

MODEL NAME : ***Elsa***

PCB NO : ***???***

ASUS P/N : ***???***

Lanai UMA Schematics Document

uFCPGA Mobile Merom
Intel Crestline-GM + ICH8M

2007-03-19

REV :1.2(DELL: X02)

MB PCB

Part Number	Description
DA80004H0L	PCB 00B LA-3071P REV0 M/B

BOM NO. ???
PCB P/N: ???

PROJECT:	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 1 OF 68	Cover Page	RELEASE DATE :	

LANAI: UMA

CLOCK
CK410M+LP
PG 21

POWER
- POWER CON. PG 59
- POWER SEQUENCE LOGIC PG 51
- POWER CHARGER PG 57
- POWER CONTROL SWITCH PG 49
- DISCHARGE PATH PG 49
  +3.3V_SUS/+5V_SUS/+3.3V_RUN
  +5V/+3.3V/+1.8V/+1.25_RUN

XDP PG 52

Merom
(478 Micro-FCPGA)
PG 7,8
(Symbol Rev.09)

POWER
- POWER I/O PG 55
  +1.5V_RUN/+1.05V_VCCP
- REGULATOR PG 58
  +VCC_GFX_CORE/+1.25V_RUN
- POWER VCORE PG 53
- POWER SYSTEM PG 54
  5V_ALW & 3.3V_ALW
- REGULATOR PG 56
  +1.8V_SUS/+0.9V_DDR_VTT

Panel Connector PG 28 — LVDS

Crestline
1299 uFCBGA
PG 9,10,11,12,13,14
(Symbol Rev.09)

533/667 MHZ DDR II → **DDR2-SODIMM1** PG 19

533/667 MHZ DDR II → **DDR2-SODIMM2** PG 19

IO Board
- CRT CONN. — VGA
- TV CONN. — TVOUT
- USB CONN.x2 — USB2.0(P2,3)
- MINI-CARD WLAN — PCIEx1 (Lane2)
- MINI-CARD WWAN — USB2.0(P9)

→ **D.B CON** PG 50 (VGA, TVOUT)

SIM CARD → **SIM CARD Board**

DMI INTERFACE

USB2.0(P0,P1) → **USB CONN.** PG 39 — **USB Board**

ICH8-M
676 BGA
PG 15,16,17,18
(Symbol Rev.09)

- USB2.0(P2,3)
- PCIEx1 (Lane2)
- USB2.0(P9)
- IHDA
- PCIE (Lane6) → **CARD READER 1394/R5C833** PG 32,33,34
- PCI → **BCM5906KMLG** QFN-68 PG 47 → **RJ45/Magnetic** PG 48
- PCIE (Lane4) → **EXPRESS-CARD R5538** PG 35
- USB2.0(P6)
- USB2.0(P7) → **Bluetooth** PG 41
- USB2.0(P5) → **CAMERA** PG 28
- SATA → **SATA-HDD** PG 31
- IDE → **CD-ROM** PG 31
- SPI, LPC

AUDIO/AMP PG 44,45,46
- **S/PDIF TO TV CONN.** PG 30
- **DIGITAL MIC.** PG 28
- **Speaker CON** PG 46
- **WtoB CON** PG 46

MDC PG 36

SIO
MEC5025
128KB Flash
TMKBC
128 Pins VTQFP
PG 37

BC

SIO
ECE5011
Expander
USB 2.0 Hub(4)
128 Pins VTQFP
PG 38

SPI, PS/2

- **CIR** PG 41
- **FLASH** PG 40
- **Touchpad CON.** PG 41
- **FAN &THERMAL** EMC4001 PG 43
- **USER INTERFACE** PG 42
- **SNIFFER** PG 42
- **CAPBTN CON.** PG 40

Audio Jacks *3 — **JACK Board**

RJ11 — **RJ11 Board**

PROJECT:	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 2 OF 68	BLOCK DIAGRAM	RELEASE DATE :	

INDEX

Pg#	Description	DNI LIST
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03	INDEX	
04	Bus connection	
05	SMBUS BLOCK	
06	Power Rail	
07-08	CPU (Merom 、 Penryn)	
09-14	Crestline	
15-18	ICH8M	
19-20	DDRII SO-DIMM(533MHz 、 667MHz)	
21	Clock Generator (CK410M+LP)	
22-27	BLANK PAGE	
28	LVDS CON & Camera & DMIC	
29	RGB CON	
30	TV OUT CON	
31	SATA(HDD & CD_ROM)	
32-34	MEDIA CARD READER / 1394 (R5C833)	
35	PCI-Express Card	
36	MDC CONN	
37	EC (MEC5025)	
38	SIO (ECE5011)	
39	USB PORT x 2	
40	FLASH & RTC & CAPBTN CONN	
41	TOUCH PAD & BT & CIR & LID	
42	SWITCH & LED	
43	HARDWARE MONITOR (EMC4001)	
44-46	AUDIO CODEC & AMP	
47	LOM BCM5906	
48	Magnetics and RJ-45	
49	Power Control Switch	
50	BtoB CON	
51	Power Sequence Logic	
52	XDP	
53-59	Power Circuit	
60	SCREW PAD	
61	Change List 1	
62	Change List 2	

Pg#	Description	DNI LIST
63	POWER CIRCUIT CHANGE LIST	
64	Modem board cover page	
65	RJ-11 CONN	
66	Modem board change List	
67	USB board cover page	
68	USB PORT (SINGLE * 2)	

Footprint Definition

Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

Layout Note

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

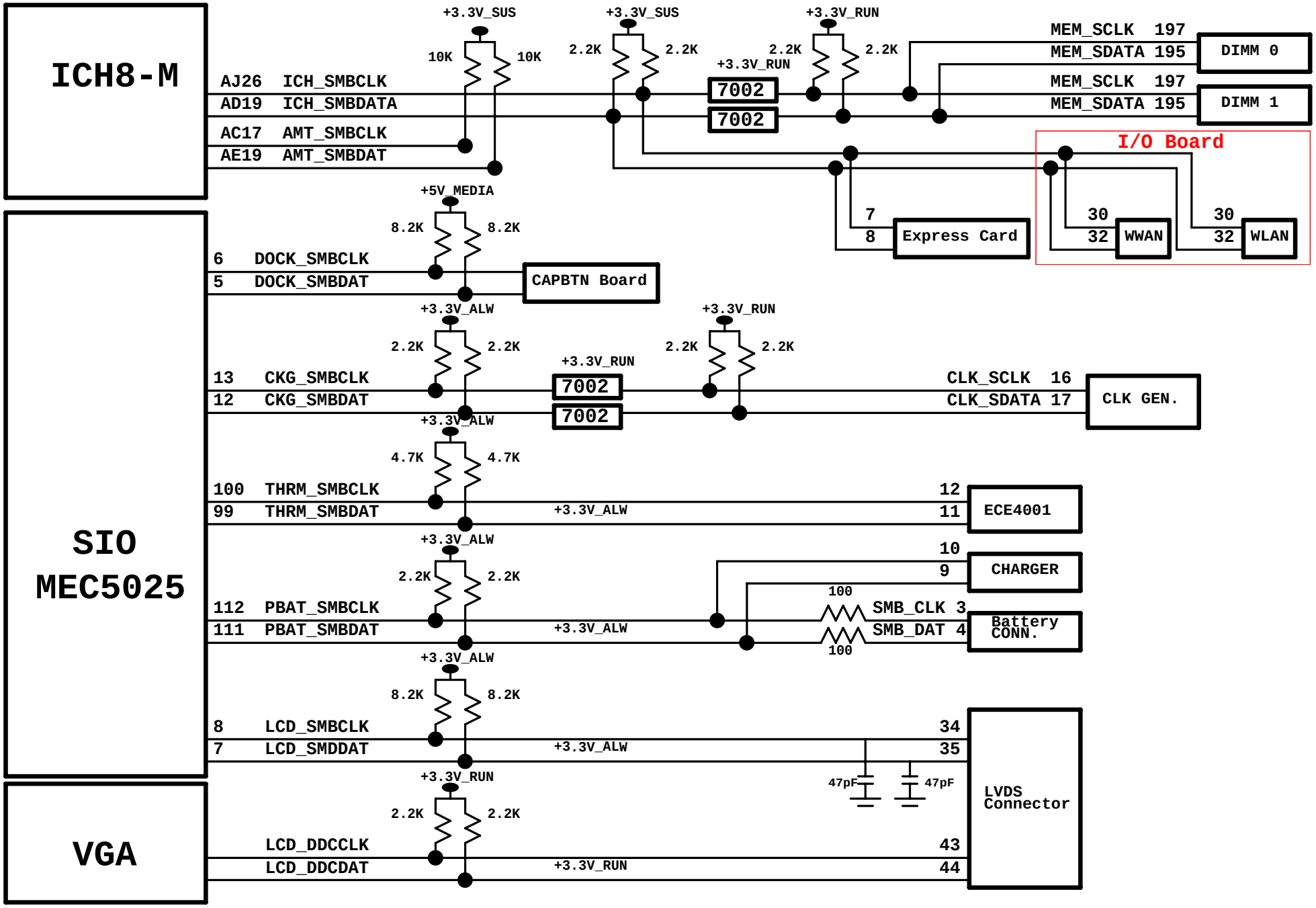
PCI Express TABLE

Lane 1	WWAN / Mini Card
Lane 2	WLAN / Mini Card
Lane 3	
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5906KMLG

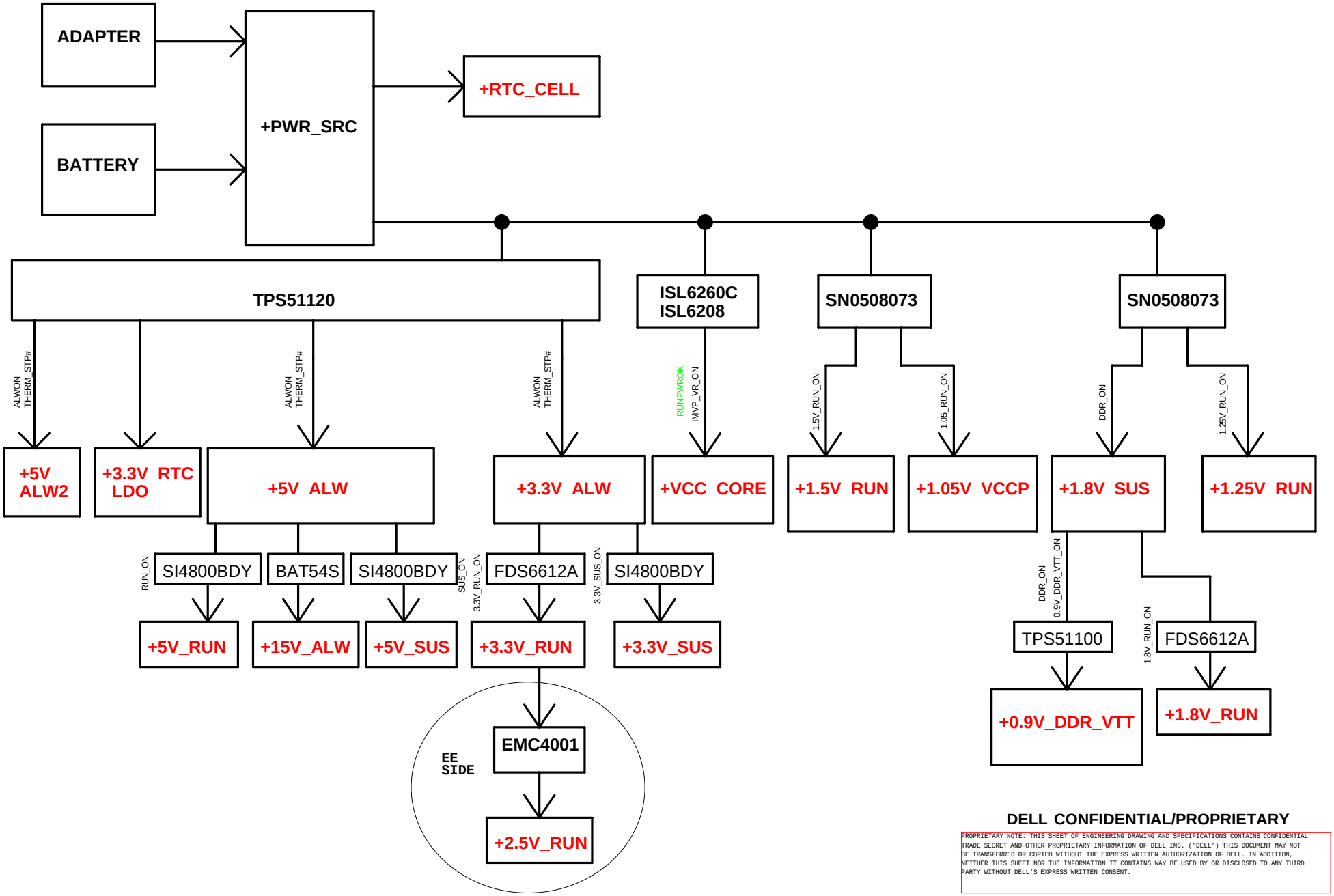
USB TABLE

ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	User2 (Single port , in USB BD)
ICH8-2 (EHCI#1)	User3 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User4 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	
ICH8-5 (EHCI#1)	Camera
ICH8-6 (EHCI#2)	ExpressCard
ICH8-7 (EHCI#2)	BT Module
ICH8-8 (EHCI#2)	
ICH8-9 (EHCI#2)	WWAN / Mini Card

Note : No USB for WLAN

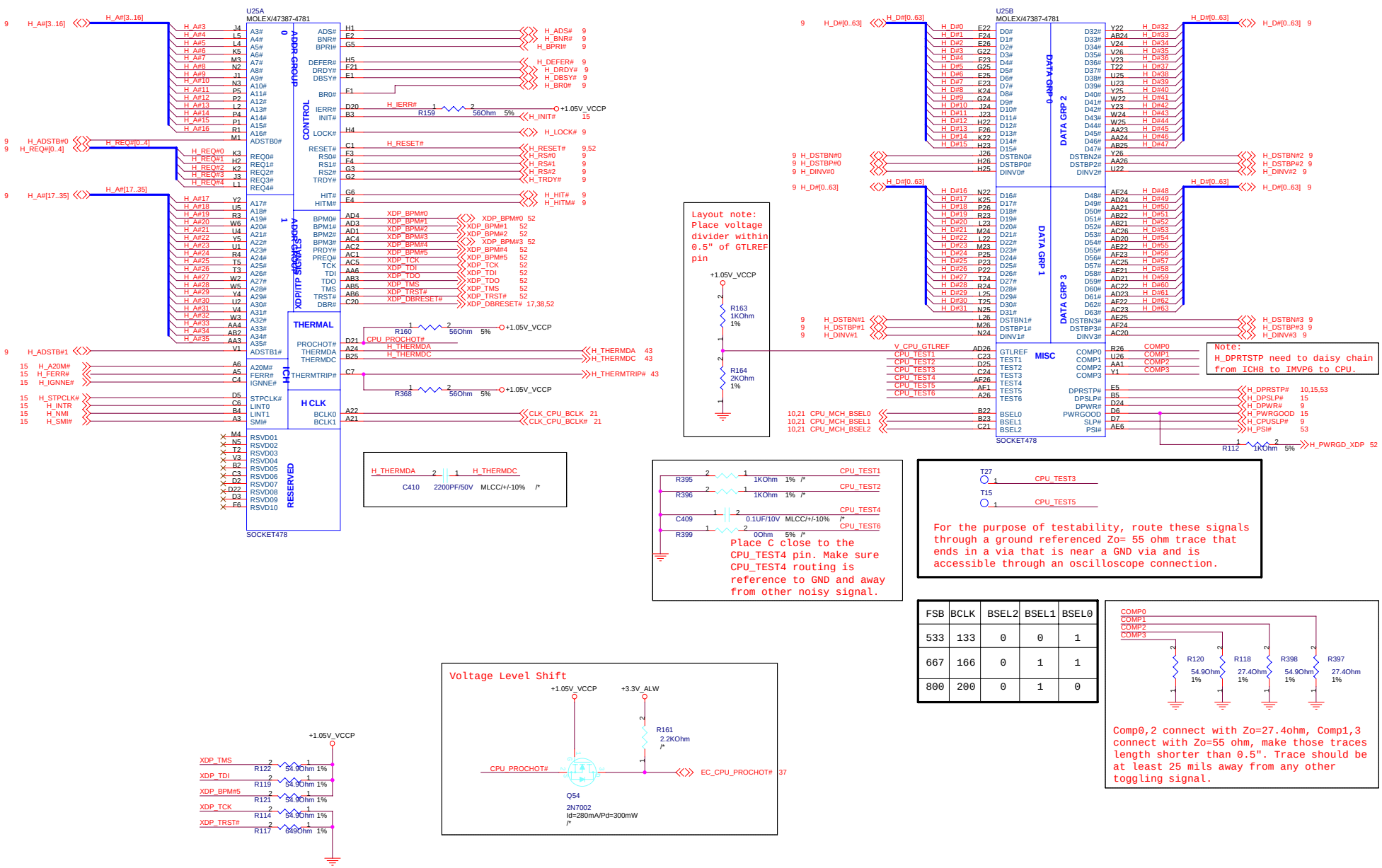


PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: SMBUS BLOCK	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 5 OF 68		RELEASE DATE :	



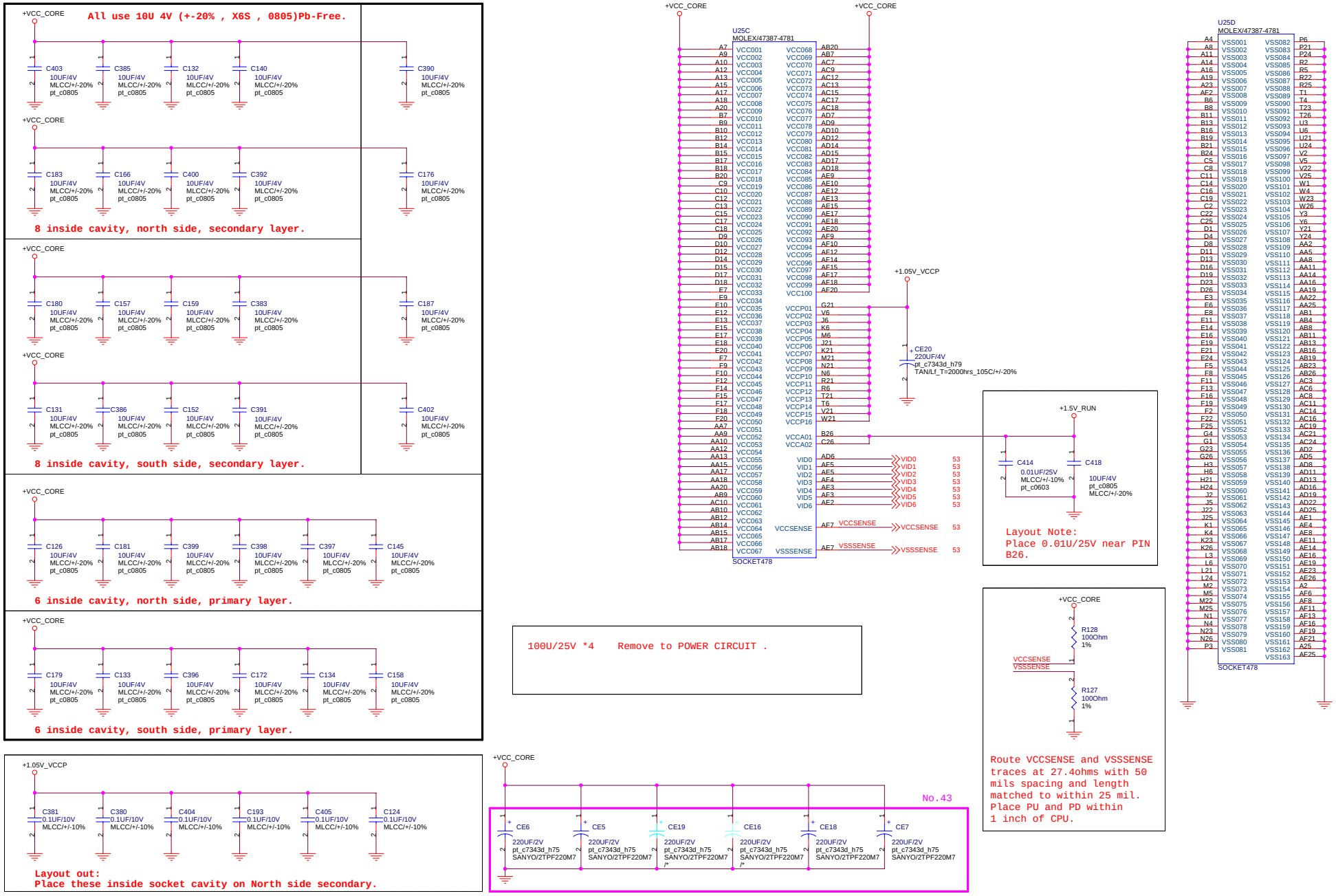
DELL CONFIDENTIAL/PROPRIETARY

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 6 OF 68	Power Rail	RELEASE DATE :	

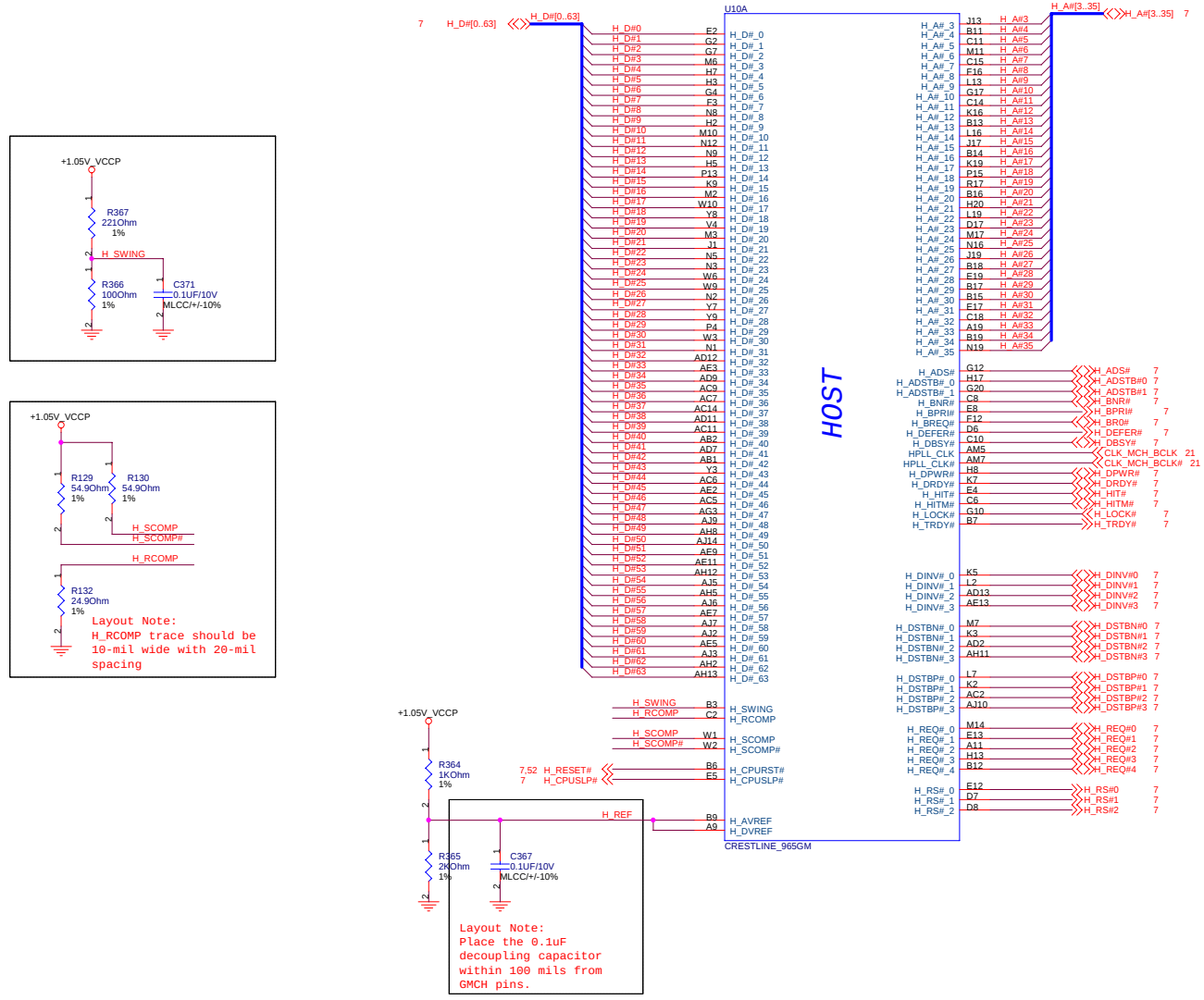


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

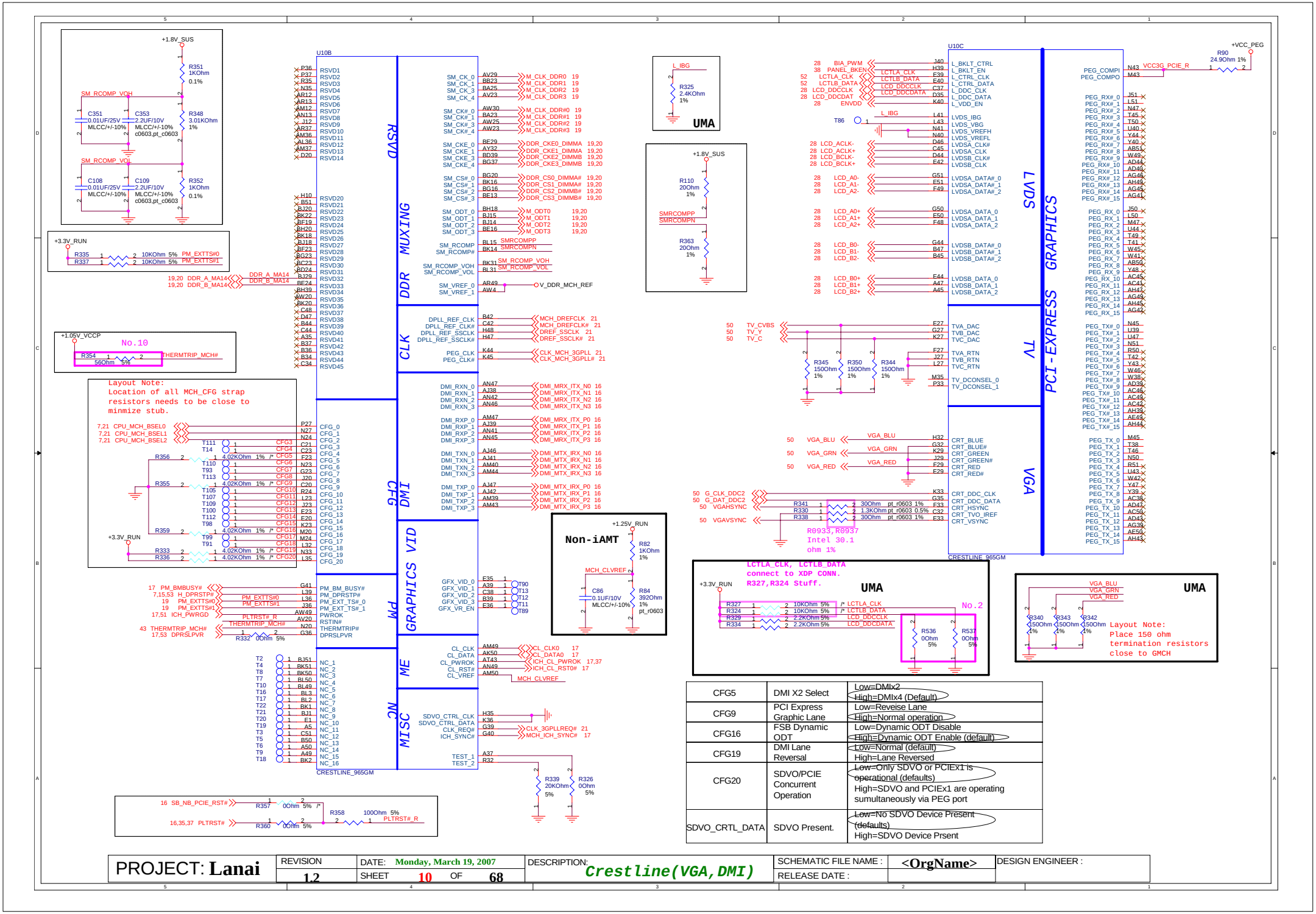
PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 7 OF 68	***MEROM CPU (1)***	RELEASE DATE :		



PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***Merom CPU (2)***	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET **8** OF **68**		RELEASE DATE :		

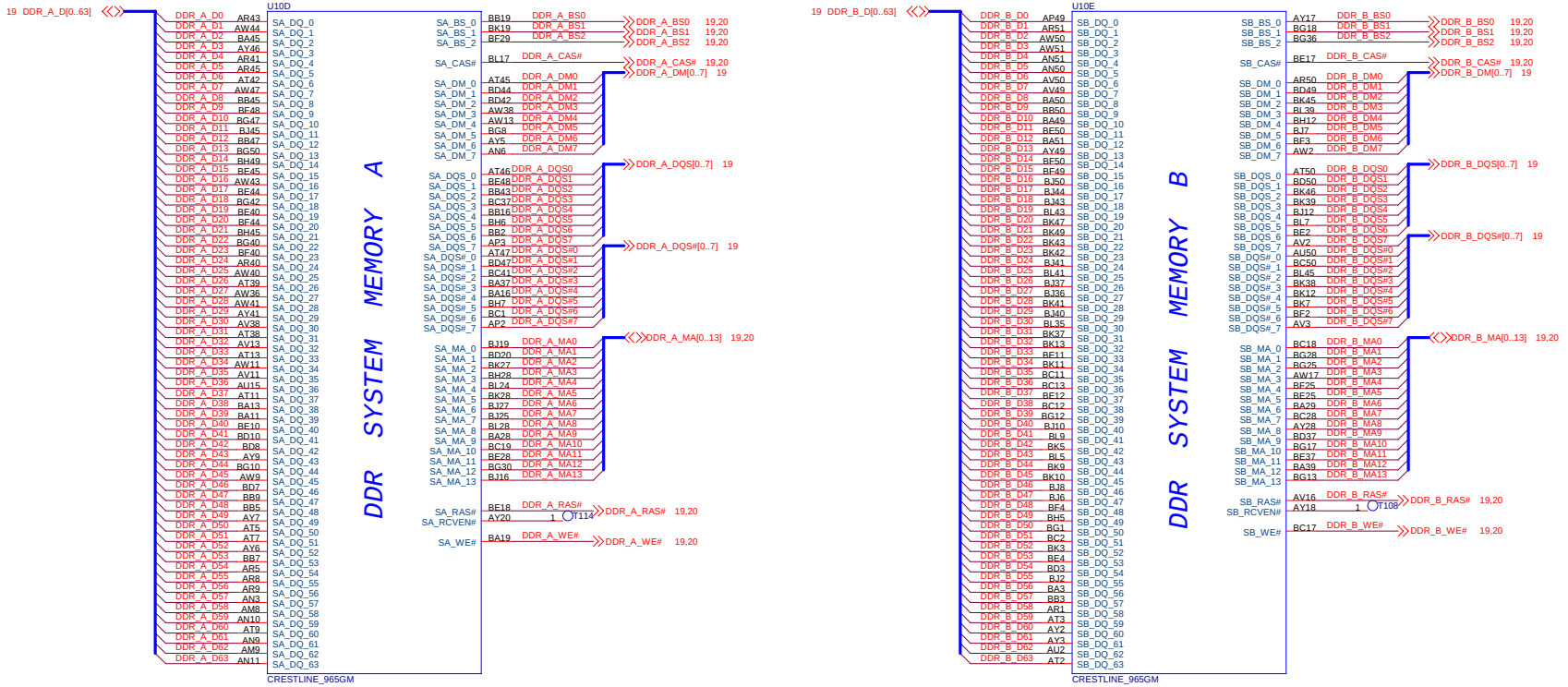


PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***Crestline(HOST)***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
		SHEET **9** OF **68**		RELEASE DATE :		

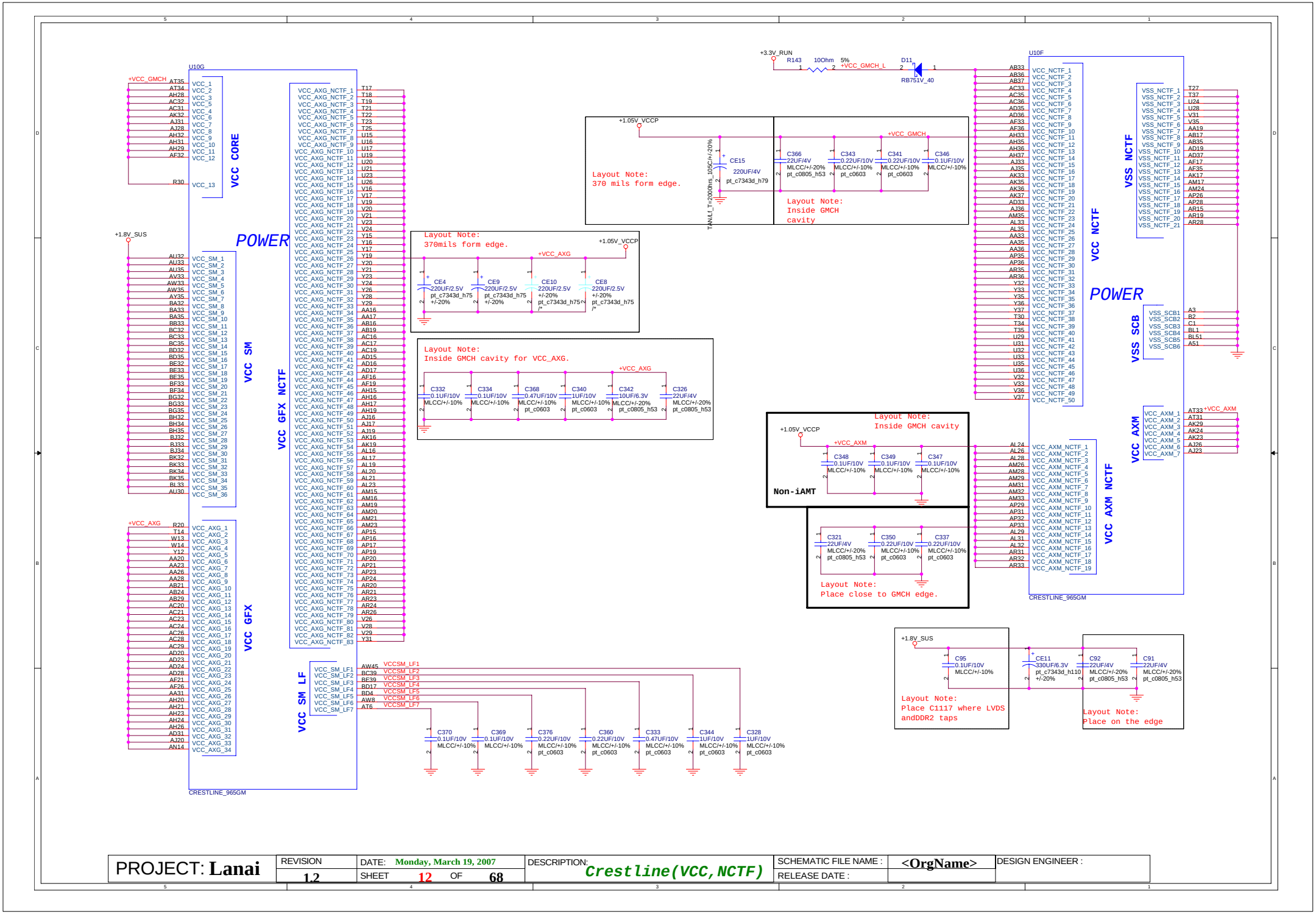


CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4 (Default)
CFG9	PCI Express Graphic Lane	Low=Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable (default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating sumultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present.	Low=No SDVO Device Present (defaults) High=SDVO Device Prsent

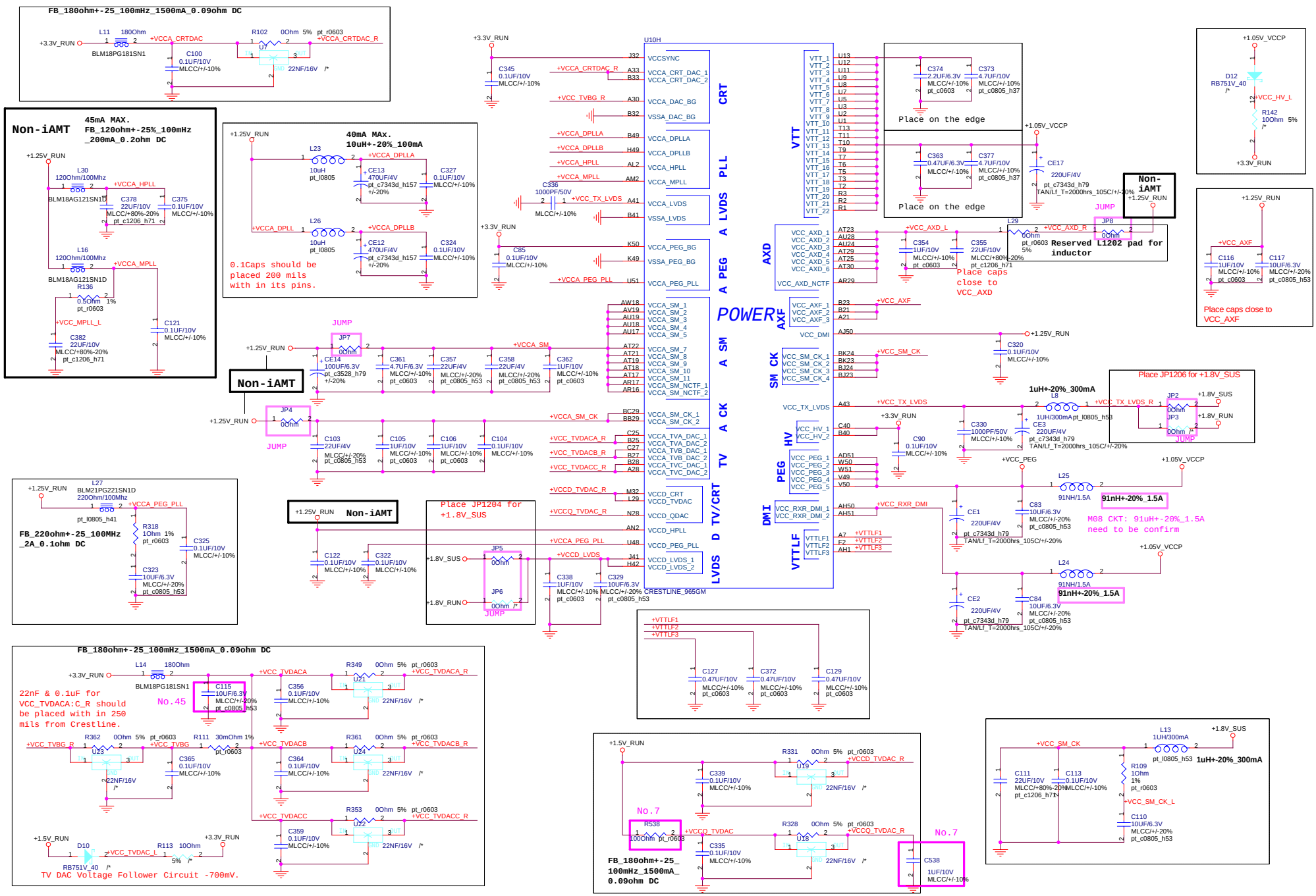
PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Crestline(VGA,DMI)*	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 10 OF 68		RELEASE DATE :	

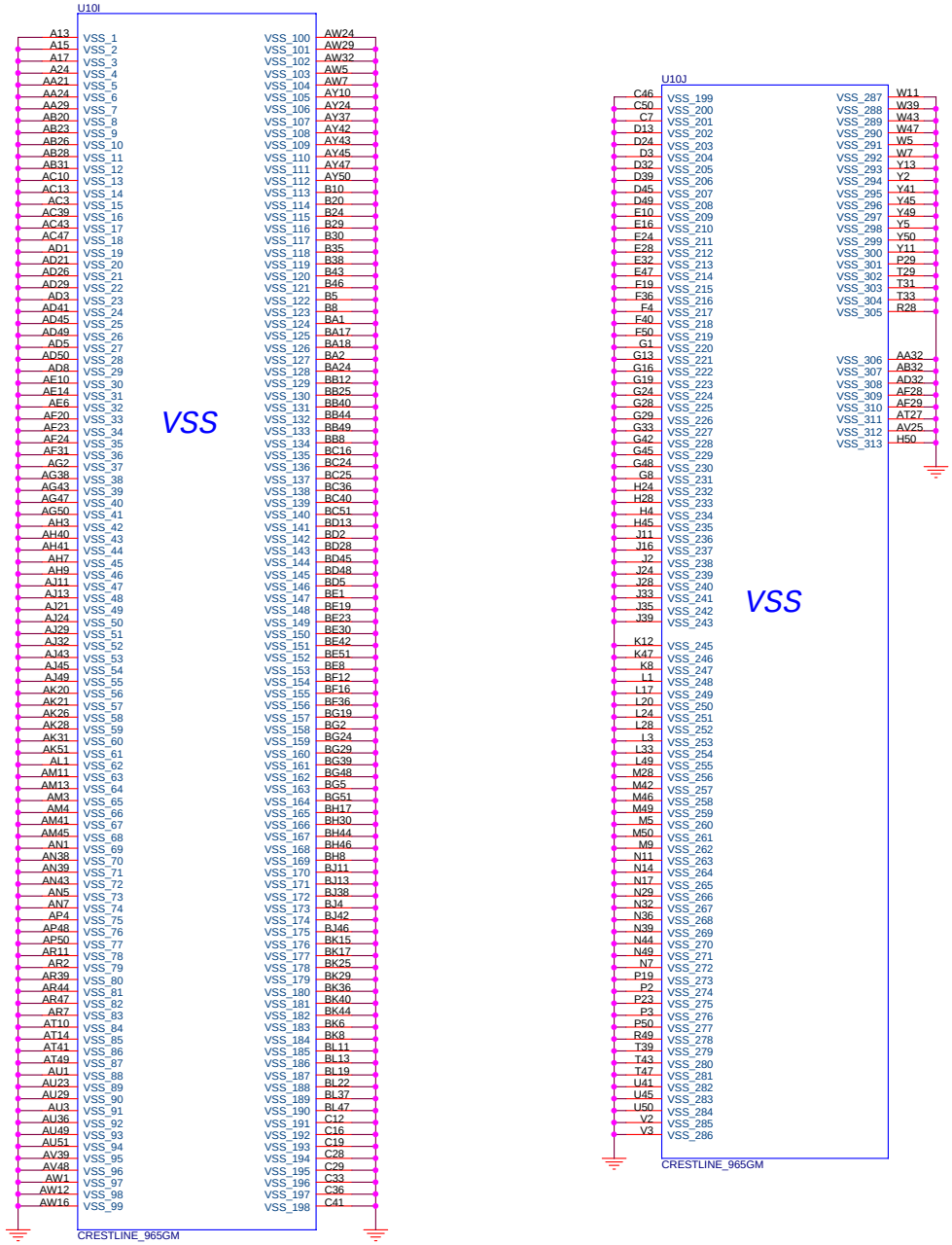


PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 11 OF 68	*Crestline(DDR2)*	RELEASE DATE :		

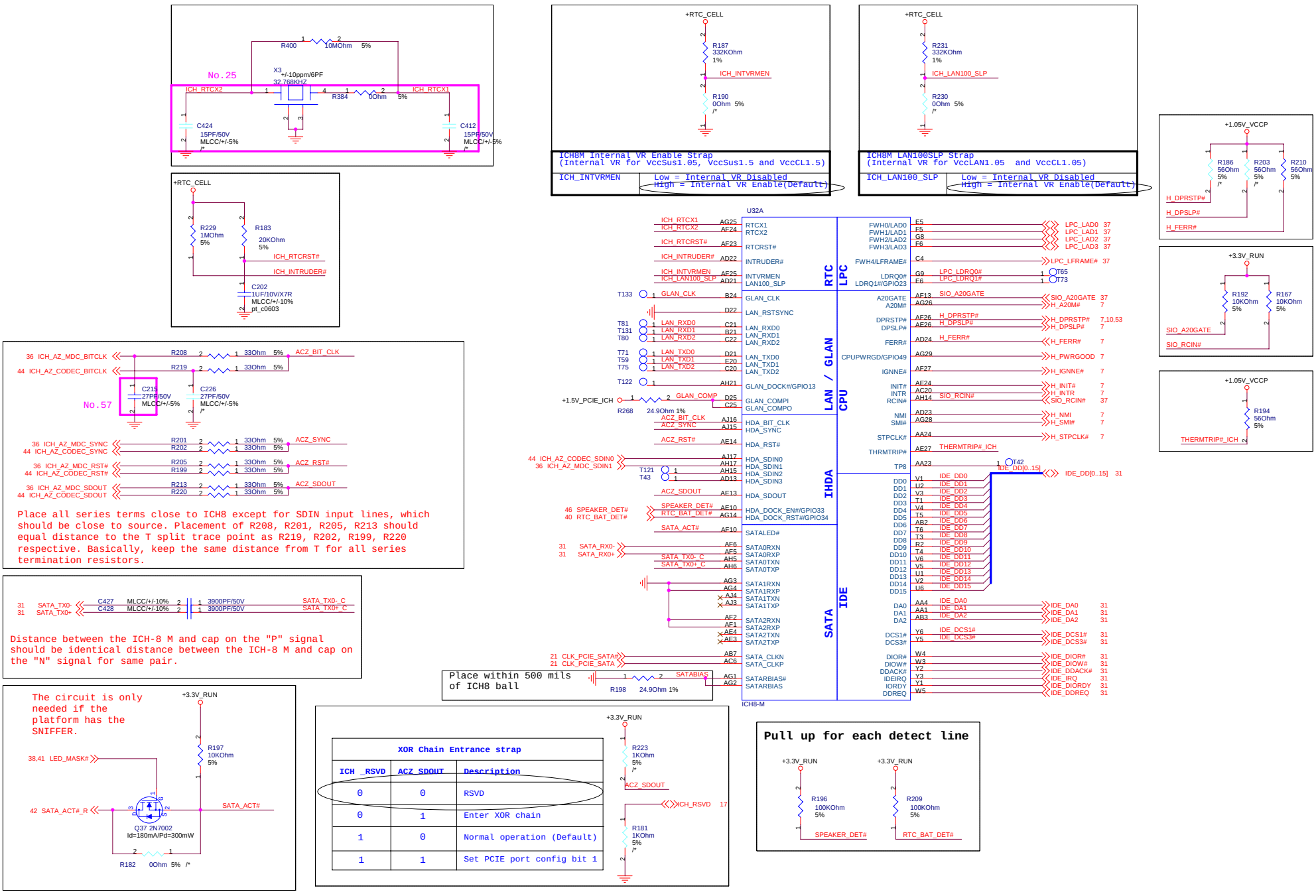


PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 12 OF 68	*Crestline(VCC,NCTF)*	RELEASE DATE :		


FB_180ohm+-25_100mHz_1500mA_0.09ohm DC
Non-iAMT
45mA MAX.
FB_120ohm+-25%_100mHz
_200mA_0.2ohm DC
40mA MAx.
10uH+-20%_100mA
0.1Caps should be
placed 200 mils
with in its pins.
Non-iAMT
JUMP
Non-iAMT
Place JP1204 for
+1.8V_SUS
FB_220ohm+-25_100MHz
_2A_0.1ohm DC
22nF & 0.1uF for
VCC_TVDACA:C_R should
be placed with in 250
mils from Crestline.
No.45
TV DAC Voltage Follower Circuit -700mV.
POWER
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
D TV/CRT
VTT
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF
Place on the edge
Place on the edge
Place caps
close to
VCC_AXD
Reserved L1202 pad for
inductor
Place caps close to
VCC_AXF
Place JP1206 for +1.8V_SUS
1uH+-20%_300mA
91nH+-20%_1.5A
M08 CKT: 91uH+-20%_1.5A
need to be confirm
FB_180ohm+-25_
100mHz_1500mA_
0.09ohm DC
No.7
No.7
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 13 OF 68
DESCRIPTION: Crestline(POWER)
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER :



PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 14 OF 68	*Crestline(VSS)*	RELEASE DATE :		



PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *ICH8: IDE/AC97/LPC/RTC*	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER:	
		SHEET 15 OF 68		RELEASE DATE:		

Place TX DC blocking caps close ICH8.

50 PCIE_TX1- C465 0.1UF/10V MLCC/+/-10% PCIE_TXN1_C
50 PCIE_TX1+ C469 0.1UF/10V MLCC/+/-10% PCIE_TXP1_C
50 PCIE_TX2- C475 0.1UF/10V MLCC/+/-10% PCIE_TXN2_C
50 PCIE_TX2+ C473 0.1UF/10V MLCC/+/-10% PCIE_TXP2_C
35 PCIE_TX4- C483 0.1UF/10V MLCC/+/-10% PCIE_TXN4_C
35 PCIE_TX4+ C485 0.1UF/10V MLCC/+/-10% PCIE_TXP4_C
47 PCIE_TX6-/GLAN_TX- C494 0.1UF/10V MLCC/+/-10% GLAN_TXN_C
47 PCIE_TX6+/GLAN_TX+ C496 0.1UF/10V MLCC/+/-10% GLAN_TXP_C

U32D

50 PCIE_RX1- / 50 PCIE_RX1+ → PCIE_TXN1_C / PCIE_TXP1_C — MiniWWAN
50 PCIE_RX2- / 50 PCIE_RX2+ → PCIE_TXN2_C / PCIE_TXP2_C — MiniWLAN
35 PCIE_RX4- / 35 PCIE_RX4+ → PCIE_TXN4_C / PCIE_TXP4_C — ExpressCard
47 PCIE_RX6-/GLAN_RX- / 47 PCIE_RX6+/GLAN_RX+ → GLAN_TXN_C / GLAN_TXP_C

PCI-Express / Direct Media Interface

DMI0RXN V27 → DMI_MTX_IRX_N0 10
DMI0RXP V26 → DMI_MTX_IRX_P0 10
DMI0TXN U29 → DMI_MRX_ITX_N0 10
DMI0TXP U28 → DMI_MRX_ITX_P0 10
DMI1RXN Y27 → DMI_MTX_IRX_N1 10
DMI1RXP Y26 → DMI_MTX_IRX_P1 10
DMI1TXN W29 → DMI_MRX_ITX_N1 10
DMI1TXP W28 → DMI_MRX_ITX_P1 10
DMI2RXN AB26 → DMI_MTX_IRX_N2 10
DMI2RXP AB25 → DMI_MTX_IRX_P2 10
DMI2TXN AA29 → DMI_MRX_ITX_N2 10
DMI2TXP AA28 → DMI_MRX_ITX_P2 10
DMI3RXN AD27 → DMI_MTX_IRX_N3 10
DMI3RXP AD26 → DMI_MTX_IRX_P3 10
DMI3TXN AC29 → DMI_MRX_ITX_N3 10
DMI3TXP AC28 → DMI_MRX_ITX_P3 10
DMI_CLKN T26 → CLK_PCIE_ICH# 21
DMI_CLKP T25 → CLK_PCIE_ICH 21
DMI_ZCOMP Y23
DMI_IRCOMP Y24 → DMI_COMP R221 24.9Ohm 1% → +1.5V_PCIE_ICH

Place within 500 mils of ICH8

SPI

SPI_CLK C23
SPI_CS0# B23
SPI_CS1# E22
SPI_MOSI D23
SPI_MISO F21

Layout Note:
Place 15 ohm within
500 mils from ICH.

37 ICH_EC_SPI_CLK → R275 15Ohm 5% → ICH_EC_SPI_CLK_R → ICH_SPI_CS#
T55
37 ICH_EC_SPI_DO → R267 15Ohm 5% → ICH_EC_SPI_DO_R → ICH_SPI_CS#
37 ICH_EC_SPI_DIN

USB

USB_OC0_1# A19
USB_OC2_3# AG16
OC4# AE15
OC5# AG15
OC6# AE15
OC7# AG17
OC8# AD12
OC9# AJ18
AD14
AH18
OC0#/GPIO40
OC1#/GPIO41
OC2#/GPIO42
OC3#/GPIO43
OC4#/GPIO29
OC5#/GPIO30
OC6#/GPIO31
OC7#
OC8#
OC9#

39 USB_OC0_1# / 50 USB_OC2_3#

USBP0N G3 → ICH_USBP0- 39 — USER1 Left side pair top/left
USBP0P G2 → ICH_USBP0+ 39
USBP1N H5 → ICH_USBP1- 39 — USER2 Left side pair bottom/right
USBP1P H4 → ICH_USBP1+ 39
USBP2N H2 → ICH_USBP2- 50 — USER3 Right side pair top/left
USBP2P H1 → ICH_USBP2+ 50
USBP3N J3 → ICH_USBP3- 50 — USER3 Right side pair bottom/right
USBP3P J2 → ICH_USBP3+ 50
USBP4N K5 → ICH_USBP4- → T60
USBP4P K4 → ICH_USBP4+ → T56
USBP5N K2 → ICH_USBP5- 28 — CCD
USBP5P K1 → ICH_USBP5+ 28
USBP6N L3 → ICH_USBP6- 35 — Express Card
USBP6P L2 → ICH_USBP6+ 35
USBP7N M5 → ICH_USBP7- 41 — BlueTooth
USBP7P M4 → ICH_USBP7+ 41
USBP8N M2 → ICH_USBP8- → T48
USBP8P M1 → ICH_USBP8+ → T49 — No.5
USBP9N N3 → ICH_USBP9- 50 — WWAN
USBP9P N2 → ICH_USBP9+ 50
USBRBIAS# F2
USBRBIAS F3 → USBRBIAS → R492 22.6Ohm 1% pt_r0603

ICH8-M

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

BIOS should not enable the internal GPIO pull up resistor

+3.3V_RUN
SB_NB_PCIE_RST# R519 10KOhm 5%
SB_WLAN_PCIE_RST# R253 10KOhm 5%
SB_NB_PCIE_RST# R520 100KOhm 5%
SB_WLAN_PCIE_RST# R250 100KOhm 5%
SB_LOM_PCIE_RST# R280 20KOhm 5%
SB_WWAN_PCIE_RST# R274 20KOhm 5%

PCI Pullups

PCI_STOP# R276 8.2KOhm 5% +3.3V_RUN
PCIE_MCARD2_DET# R548 100KOhm 5% +3.3V_RUN
PCI_DEVSEL# RP4E 8.2KOhm 5% +3.3V_RUN — No.14
PCI_FRAME# RP4F 8.2KOhm 5% PCI_REQ1#
ICH_GPIO2_PIRQE# RP4G 8.2KOhm 5% PCI_PIRQD#
PCI_SERR# RP4H 8.2KOhm 5%
PCI_TRDY# RP4A 8.2KOhm 5%
PCI_REQ0# RP3E 8.2KOhm 5% +3.3V_RUN
PCI_PLOCK# RP3F 8.2KOhm 5% PCI_PIRQC#
PCI_PERR# RP3G 8.2KOhm 5% PCI_PIRQB#
RP3H 8.2KOhm 5% PCI_PIRQA#
RP3A 8.2KOhm 5% PCI_IRDY#

+3.3V_ALW
U36 74AHC1G08GW
SPI_CS0# → R517 15Ohm 5% → R518 15Ohm 5% → ICH_SPI_CS# / SIO_SPI_CS# 37
R521 0Ohm 5%

Non-iAMT

+3.3V_SUS
USB_OC0_1# RP1E 10KOhm 5%
OC9# RP1F 10KOhm 5% OC5#
OC6# RP1G 10KOhm 5% OC8#
OC7# RP1H 10KOhm 5% USB_OC2_3#
RP1D 10KOhm 5%
RP1C 10KOhm 5%
RP1B 10KOhm 5%
RP1A 10KOhm 5% OC4#

ICH_SPI_CS1#_R
PCI_GNT0# → R272 1KOhm 5% → R260 1KOhm 5%

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

PCI_GNT3# → R266 1KOhm 5%

A16 away override strap.

PCI_GNT3#	Low = A16 swap override enabled.
	High = Default.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

+3.3V_SUS
C279 0.047UF/10V MLCC/+/-10%
U14 SN74AHC1G32DBVR
PCI_RST#_G → PCI_RST# 32 — No.37

+3.3V_SUS
C199 0.047UF/10V MLCC/+/-10%
U12 SN74AHC1G32DBVR
PCI_PLTRST# → PLTRST# 10,35,37
+3.3V_SUS
C542 0.047UF/10V MLCC/+/-10%
U40 SN74AHC1G32DBVR
PCI_PLTRST# → PLTRST_LAN_MINICARD# 47,50
C553 47PF/50V MLCC/+/-5% — No.54

32 PCI_AD[0..31]

PCI

PCI_AD0 D20 … PCI_AD31 A3

REQ0# A4 → PCI_REQ0#
GNT0# D7 → PCI_GNT0#
REQ1#/GPIO50 E18 → PCI_REQ1# — 32
GNT1#/GPIO51 C18 → PCI_GNT1# — 32
REQ2#/GPIO52 B19 → SB_WWAN_PCIE_RST# 50 — T72
GNT2#/GPIO53 F18 → PCI_GNT2#
REQ3#/GPIO54 A11 → SB_LOM_PCIE_RST# — T78
GNT3#/GPIO55 C10 → PCI_GNT3# 47
C/BE0# C17 → PCI_C_BE0# 32
C/BE1# E15 → PCI_C_BE1# 32
C/BE2# E16 → PCI_C_BE2# 32
C/BE3# E17 → PCI_C_BE3# 32
IRDY# C8 → PCI_IRDY# — PCI_IRDY# 32
PAR D9 → PCI_PAR 32
PCIRST# G6 → PCI_RST#_G
DEVSEL# D16 → PCI_DEVSEL# — PCI_DEVSEL# 32
PERR# A7 → PCI_PERR# — PCI_PERR# 32
PLOCK# B7 → PCI_PLOCK#
SERR# F10 → PCI_SERR# — PCI_SERR# 32
STOP# C16 → PCI_STOP# — PCI_STOP# 32
TRDY# C9 → PCI_TRDY# — PCI_TRDY# 32
FRAME# A17 → PCI_FRAME# — PCI_FRAME# 32
PLTRST# AG24 → PCI_PLTRST#
PCICLK B10 → CLK_PCI_ICH — CLK_PCI_ICH 21
PME# G7 → ICH_PME# 38

Interrupt I/F

T79
PCI_PIRQB# F9
32 PCI_PIRQC# B5
32 PCI_PIRQD# C5
PCI_PIRQA# A10
PIRQE#/GPIO2 F8 → ICH_GPIO2_PIRQE#
PIRQF#/GPIO3 G11 → SB_WLAN_PCIE_RST# — SB_WLAN_PCIE_RST# 50
PIRQG#/GPIO4 F12 → SB_NB_PCIE_RST# — SB_NB_PCIE_RST# 10
PIRQH#/GPIO5 B3 → PCIE_MCARD2_DET# — PCIE_MCARD2_DET# 50 — No.14

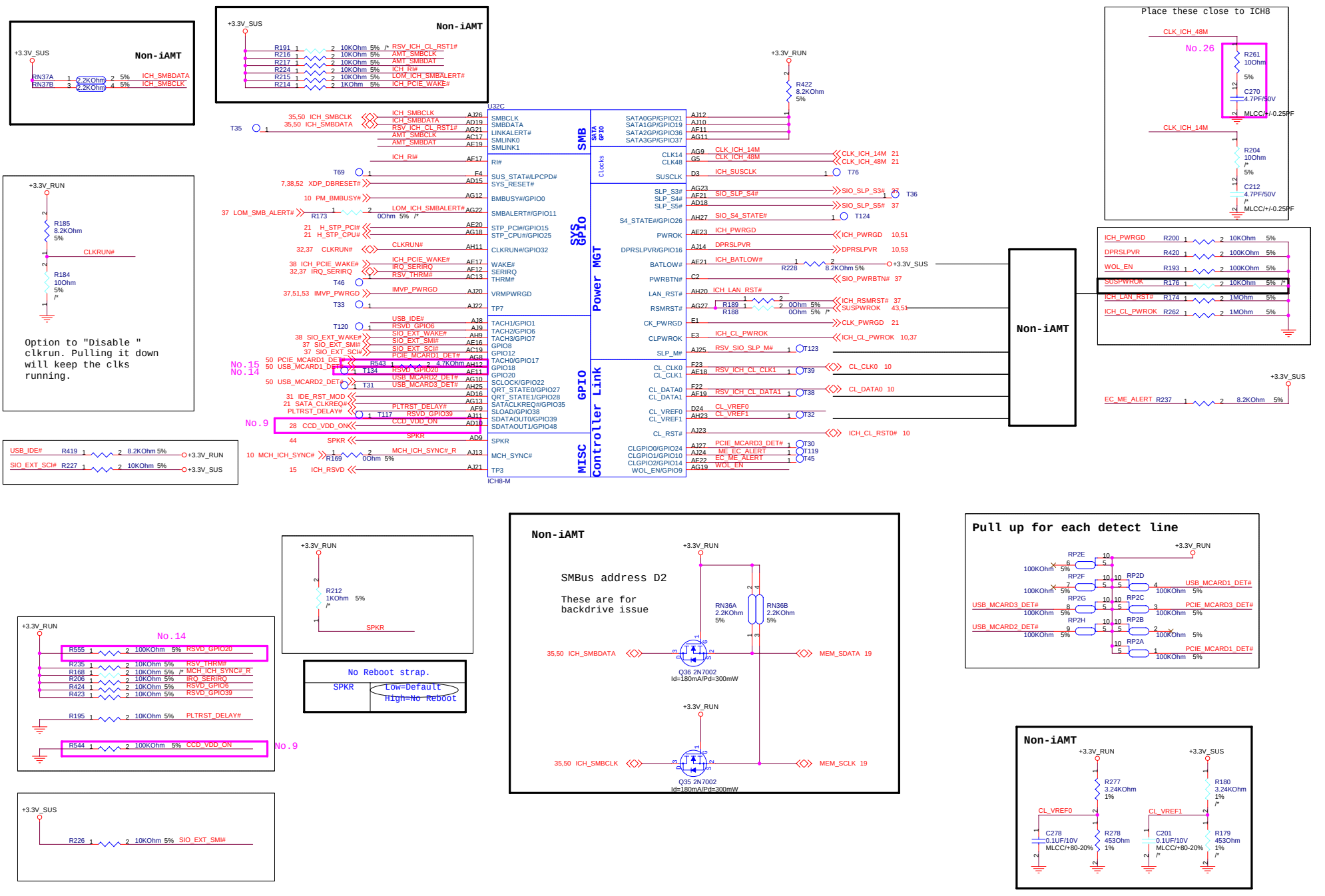
ICH8-M

R5C833	REQ1 GNT1	PIRQC PIRQD

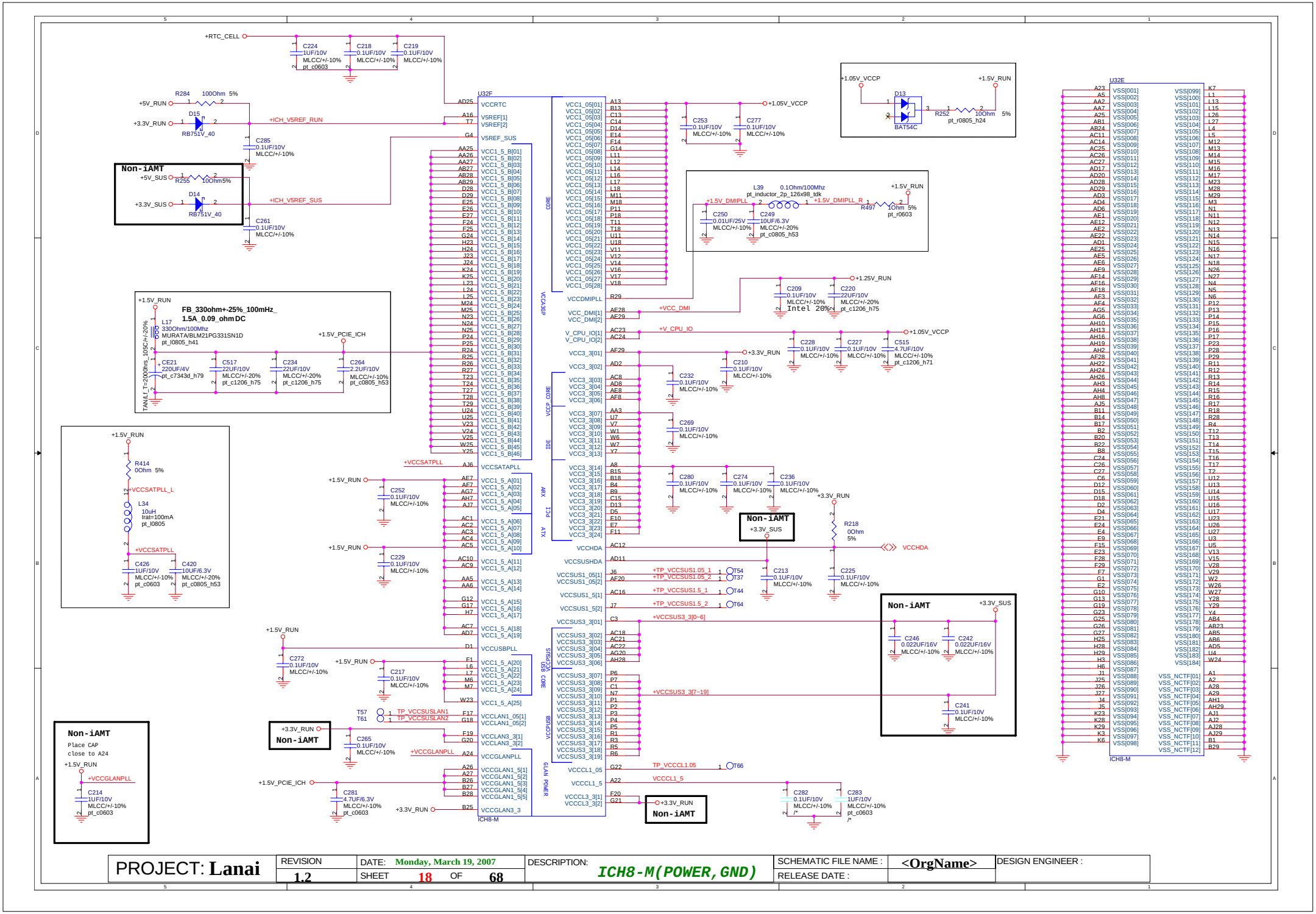
CLK_PCI_ICH → R281 10Ohm 5% → C284 8.2PF/50V MLCC/+/-0.25PF

Reserved for EMI.
Place resister and cap close to ICH.

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: ICH8: PCI/INT/DMI/USB	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 16 OF 68		RELEASE DATE :	



PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***ICH8: SMB/PWR/CLK/GPIO***	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 17 OF 68		RELEASE DATE :		



PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***ICH8-M(POWER, GND)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER :
		SHEET **18** OF **68**		RELEASE DATE :	

A is required to route to Top SODIMM for AMT to function Ch.A SODIMM needs to be populated for Intel AMT support.

TOP

+1.8V_SUS

V_DDR_MCH_REF

DDR_A_DM[0..7] 11
DDR_A_D[0..63] 11
DDR_A_DQS[0..7] 11
DDR_A_DQS#[0..7] 11
DDR_A_MA[0..14] 10,11,20

CON14

	1 VREF	VSS46 2	
DDR_A_D12	3 VSS47	DQ4 4	DDR_A_D13
DDR_A_D8	5 DQ0	DQ5 6	DDR_A_D14
	7 DQ1	VSS15 8	
DDR_A_DQS#1	9 VSS37	DM0 10	DDR_A_DM1
DDR_A_DQS1	11 DQS#0	VSS5 12	
	13 DQS0	DQ6 14	DDR_A_D11
DDR_A_D15	15 VSS48	DQ7 16	DDR_A_D10
DDR_A_D9	17 DQ2	VSS16 18	
	19 DQ3	DQ12 20	DDR_A_D3
DDR_A_D7	21 VSS38	DQ13 22	DDR_A_D1
DDR_A_D2	23 DQ8	VSS17 24	
	25 DQ9	DM1 26	DDR_A_DM0
DDR_A_DQS#0	27 VSS49	VSS53 28	
DDR_A_DQS0	29 DQS#1	CK0 30	M_CLK_DDR0 10
	31 DQS1	CK0# 32	M_CLK_DDR#0 10
DDR_A_D4	33 VSS39	VSS41 34	
DDR_A_D6	35 DQ10	DQ14 36	DDR_A_D5
	37 DQ11	DQ15 38	DDR_A_D0
	39 VSS50	VSS54 40	
	41 VSS18	VSS20 42	
DDR_A_D16	43 DQ16	DQ20 44	DDR_A_D17
DDR_A_D21	45 DQ17	DQ21 46	DDR_A_D20
	47 VSS1	VSS6 48	
DDR_A_DQS#2	49 DQS#2	NC3 50	PM_EXTTS#0 DDR_A_DM2 PM_EXTTS#0 10
DDR_A_DQS2	51 DQS2	DM2 52	
	53 VSS19	VSS21 54	
DDR_A_D19	55 DQ18	DQ22 56	DDR_A_D18
DDR_A_D22	57 DQ19	DQ23 58	DDR_A_D23
	59 VSS22	VSS24 60	
DDR_A_D25	61 DQ24	DQ28 62	DDR_A_D28
DDR_A_D27	63 DQ25	DQ29 64	DDR_A_D29
	65 VSS23	VSS25 66	
DDR_A_DM3	67 DM3	DQS#3 68	DDR_A_DQS#3
	69 NC4	DQS3 70	DDR_A_DQS3
	71 VSS9	VSS10 72	
DDR_A_D31	73 DQ26	DQ30 74	DDR_A_D30
DDR_A_D24	75 DQ27	DQ31 76	DDR_A_D26
	77 VSS4	VSS8 78	
10,20 DDR_CKE0_DIMMA	79 CKE0	CKE1 80	DDR_CKE1_DIMMA 10,20
	81 VDD7	VDD8 82	
	83 NC1	A15 84	
11,20 DDR_A_BS2	85 A16_BA2	A14 86	DDR_A_MA14
	87 VDD9	VDD11 88	
DDR_A_MA12	89 A12	A11 90	DDR_A_MA11
DDR_A_MA9	91 A9	A7 92	DDR_A_MA7
DDR_A_MA8	93 A8	A6 94	DDR_A_MA6
	95 VDD5	VDD4 96	
DDR_A_MA5	97 A5	A4 98	DDR_A_MA4
DDR_A_MA3	99 A3	A2 100	DDR_A_MA2
DDR_A_MA1	101 A1	A0 102	DDR_A_MA0
	103 VDD10	VDD12 104	
DDR_A_MA10	105 A10/AP	BA1 106	DDR_A_BS1 11,20
11,20 DDR_A_BS0 DDR_A_BS0	107 BA0	RAS# 108	DDR_A_RAS# 11,20
11,20 DDR_A_WE#	109 WE#	S0# 110	DDR_CS0_DIMMA# 10,20
	111 VDD2	VDD1 112	
11,20 DDR_A_CAS# DDR_A_CAS#	113 CAS#	ODT0 114	M_ODT0 DDR_A_MA13 M_ODT0 10,20
10,20 DDR_CS1_DIMMA#	115 S1#	A13 116	
	117 VDD3	VDD6 118	
10,20 M_ODT1 M_ODT1	119 ODT1	NC2 120	
	121 VSS11	VSS12 122	
DDR_A_D36	123 DQ32	DQ36 124	DDR_A_D32
DDR_A_D33	125 DQ33	DQ37 126	DDR_A_D38
	127 VSS26	VSS28 128	
DDR_A_DQS#4	129 DQS#4	DM4 130	DDR_A_DM4
DDR_A_DQS4	131 DQS4	VSS42 132	
	133 VSS2	DQ38 134	DDR_A_D37
DDR_A_D39	135 DQ34	DQ39 136	DDR_A_D35
DDR_A_D34	137 DQ35	VSS55 138	
	139 VSS27	DQ44 140	DDR_A_D45
DDR_A_D40	141 DQ40	DQ45 142	DDR_A_D44
DDR_A_D47	143 DQ41	VSS43 144	
	145 VSS29	DQS#5 146	DDR_A_DQS#5
DDR_A_DM5	147 DM5	DQS5 148	DDR_A_DQS5
	149 VSS51	VSS56 150	
DDR_A_D42	151 DQ42	DQ46 152	DDR_A_D41
DDR_A_D43	153 DQ43	DQ47 154	DDR_A_D46
	155 VSS40	VSS44 156	
DDR_A_D48	157 DQ48	DQ52 158	DDR_A_D53
DDR_A_D49	159 DQ49	DQ53 160	DDR_A_D52
	161 VSS52	VSS57 162	
	163 NCTEST	CK1 164	M_CLK_DDR1 10
	165 VSS30	CK1# 166	M_CLK_DDR#1 10
DDR_A_DQS#6	167 DQS#6	VSS45 168	
DDR_A_DQS6	169 DQS6	DM6 170	DDR_A_DM6
	171 VSS31	VSS32 172	
DDR_A_D50	173 DQ50	DQ54 174	DDR_A_D51
DDR_A_D54	175 DQ51	DQ55 176	DDR_A_D55
	177 VSS33	VSS35 178	
DDR_A_D56	179 DQ56	DQ60 180	DDR_A_D58
DDR_A_D60	181 DQ57	DQ61 182	DDR_A_D57
	183 VSS3	VSS7 184	
DDR_A_DM7	185 DM7	DQS#7 186	DDR_A_DQS#7
	187 VSS34	DQS7 188	DDR_A_DQS7
DDR_A_D61	189 DQ58	VSS36 190	
DDR_A_D59	191 DQ59	DQ62 192	DDR_A_D63
	193 VSS14	DQ63 194	DDR_A_D62
17 MEM_SDATA MEM_SDATA	195 SDA	VSS13 196	
17 MEM_SCLK MEM_SCLK	197 SCL	SA0 198	
+3.3V_RUN	199 VDDSPD	SA1 200	
	201 GND0	GND1 202	
	203 NP_NC1NP_NC2	204	

STD FOXCONN/AS0A426-N2SN-7F

CLOCK 0 , 1
CKE 0 , 1

V_DDR_MCH_REF
C102 0.1UF/10V MLCC/+/-10%
C99 2.2UF/6.3V MLCC/+80-20%
pt_c0805_h53

+3.3V_RUN
Non-iAMT
C445 2.2UF/6.3V MLCC/+/-10%
C200 0.1UF/10V MLCC/+80-20%
pt_c0805_h53

R178 10KOhm 5%
R171 10KOhm 5%

Non-iAMT
+3.3V_RUN
SMbus address A0

BOT

+1.8V_SUS

V_DDR_MCH_REF

DDR_B_DM[0..7] 11
DDR_B_D[0..63] 11
DDR_B_DQS[0..7] 11
DDR_B_DQS#[0..7] 11
DDR_B_MA[0..14] 10,11,20

CON15

	1 VREF	VSS46 2	
DDR_B_D0	3 VSS47	DQ4 4	DDR_B_D5
DDR_B_D1	5 DQ0	DQ5 6	DDR_B_D4
	7 DQ1	VSS15 8	
DDR_B_DQS#0	9 VSS37	DM0 10	DDR_B_DM0
DDR_B_DQS0	11 DQS#0	VSS5 12	
	13 DQS0	DQ6 14	DDR_B_D6
DDR_B_D3	15 VSS48	DQ7 16	DDR_B_D7
DDR_B_D2	17 DQ2	VSS16 18	
	19 DQ3	DQ12 20	DDR_B_D8
DDR_B_D9	21 VSS38	DQ13 22	DDR_B_D12
DDR_B_D13	23 DQ8	VSS17 24	
	25 DQ9	DM1 26	DDR_B_DM1
DDR_B_DQS#1	27 VSS49	VSS53 28	
DDR_B_DQS1	29 DQS#1	CK0 30	M_CLK_DDR2 10
	31 DQS1	CK0# 32	M_CLK_DDR#2 10
DDR_B_D10	33 VSS39	VSS41 34	
DDR_B_D14	35 DQ10	DQ14 36	DDR_B_D11
	37 DQ11	DQ15 38	DDR_B_D15
	39 VSS50	VSS54 40	
	41 VSS18	VSS20 42	
DDR_B_D20	43 DQ16	DQ20 44	DDR_B_D21
DDR_B_D16	45 DQ17	DQ21 46	DDR_B_D23
	47 VSS1	VSS6 48	
DDR_B_DQS#2	49 DQS#2	NC3 50	PM_EXTTS#1 DDR_B_DM2 PM_EXTTS#1 10
DDR_B_DQS2	51 DQS2	DM2 52	
	53 VSS19	VSS21 54	
DDR_B_D18	55 DQ18	DQ22 56	DDR_B_D22
DDR_B_D19	57 DQ19	DQ23 58	DDR_B_D17
	59 VSS22	VSS24 60	
DDR_B_D25	61 DQ24	DQ28 62	DDR_B_D29
DDR_B_D28	63 DQ25	DQ29 64	DDR_B_D31
	65 VSS23	VSS25 66	
DDR_B_DM3	67 DM3	DQS#3 68	DDR_B_DQS#3
	69 NC4	DQS3 70	DDR_B_DQS3
	71 VSS9	VSS10 72	
DDR_B_D27	73 DQ26	DQ30 74	DDR_B_D24
DDR_B_D30	75 DQ27	DQ31 76	DDR_B_D26
	77 VSS4	VSS8 78	
10,20 DDR_CKE2_DIMMB	79 CKE0	CKE1 80	DDR_CKE3_DIMMB 10,20
	81 VDD7	VDD8 82	
	83 NC1	A15 84	
11,20 DDR_B_BS2	85 A16_BA2	A14 86	DDR_B_MA14
	87 VDD9	VDD11 88	
DDR_B_MA12	89 A12	A11 90	DDR_B_MA11
DDR_B_MA9	91 A9	A7 92	DDR_B_MA7
DDR_B_MA8	93 A8	A6 94	DDR_B_MA6
	95 VDD5	VDD4 96	
DDR_B_MA5	97 A5	A4 98	DDR_B_MA4
DDR_B_MA3	99 A3	A2 100	DDR_B_MA2
DDR_B_MA1	101 A1	A0 102	DDR_B_MA0
	103 VDD10	VDD12 104	
DDR_B_MA10	105 A10/AP	BA1 106	DDR_B_BS1 11,20
11,20 DDR_B_BS0 DDR_B_BS0	107 BA0	RAS# 108	DDR_B_RAS# 11,20
11,20 DDR_B_WE#	109 WE#	S0# 110	DDR_CS2_DIMMB# 10,20
	111 VDD2	VDD1 112	
11,20 DDR_B_CAS# DDR_B_CAS#	113 CAS#	ODT0 114	M_ODT2 DDR_B_MA13 M_ODT2 10,20
10,20 DDR_CS3_DIMMB#	115 S1#	A13 116	
	117 VDD3	VDD6 118	
10,20 M_ODT3 M_ODT3	119 ODT1	NC2 120	
	121 VSS11	VSS12 122	
DDR_B_D38	123 DQ32	DQ36 124	DDR_B_D35
DDR_B_D36	125 DQ33	DQ37 126	DDR_B_D32
	127 VSS26	VSS28 128	
DDR_B_DQS#4	129 DQS#4	DM4 130	DDR_B_DM4
DDR_B_DQS4	131 DQS4	VSS42 132	
	133 VSS2	DQ38 134	DDR_B_D39
DDR_B_D34	135 DQ34	DQ39 136	DDR_B_D37
DDR_B_D33	137 DQ35	VSS55 138	
	139 VSS27	DQ44 140	DDR_B_D40
DDR_B_D45	141 DQ40	DQ45 142	DDR_B_D41
DDR_B_D46	143 DQ41	VSS43 144	
	145 VSS29	DQS#5 146	DDR_B_DQS#5
DDR_B_DM5	147 DM5	DQS5 148	DDR_B_DQS5
	149 VSS51	VSS56 150	
DDR_B_D44	151 DQ42	DQ46 152	DDR_B_D47
DDR_B_D42	153 DQ43	DQ47 154	DDR_B_D43
	155 VSS40	VSS44 156	
DDR_B_D53	157 DQ48	DQ52 158	DDR_B_D52
DDR_B_D48	159 DQ49	DQ53 160	DDR_B_D49
	161 VSS52	VSS57 162	
	163 NCTEST	CK1 164	M_CLK_DDR3 10
	165 VSS30	CK1# 166	M_CLK_DDR#3 10
DDR_B_DQS#6	167 DQS#6	VSS45 168	
DDR_B_DQS6	169 DQS6	DM6 170	DDR_B_DM6
	171 VSS31	VSS32 172	
DDR_B_D51	173 DQ50	DQ54 174	DDR_B_D55
DDR_B_D54	175 DQ51	DQ55 176	DDR_B_D50
	177 VSS33	VSS35 178	
DDR_B_D56	179 DQ56	DQ60 180	DDR_B_D57
DDR_B_D62	181 DQ57	DQ61 182	DDR_B_D61
	183 VSS3	VSS7 184	
DDR_B_DM7	185 DM7	DQS#7 186	DDR_B_DQS#7
	187 VSS34	DQS7 188	DDR_B_DQS7
DDR_B_D63	189 DQ58	VSS36 190	
DDR_B_D60	191 DQ59	DQ62 192	DDR_B_D58
	193 VSS14	DQ63 194	DDR_B_D59
MEM_SDATA	195 SDA	VSS13 196	
MEM_SCLK	197 SCL	SA0 198	
+3.3V_RUN	199 VDDSPD	SA1 200	
	201 GND0	GND1 202	
	203 NP_NC1NP_NC2	204	

STD FOXCONN/AS0A426-NASN-7F

CLOCK 2 , 3
CKE 2 , 3

Non-iAMT
+3.3V_RUN
SMbus address A4

V_DDR_MCH_REF
C101 0.1UF/10V MLCC/+/-10%
C97 2.2UF/6.3V MLCC/+80-20%
pt_c0805_h53

+3.3V_RUN
Non-iAMT
C435 2.2UF/6.3V MLCC/+/-10%
C429 0.1UF/10V MLCC/+80-20%
pt_c0805_h53

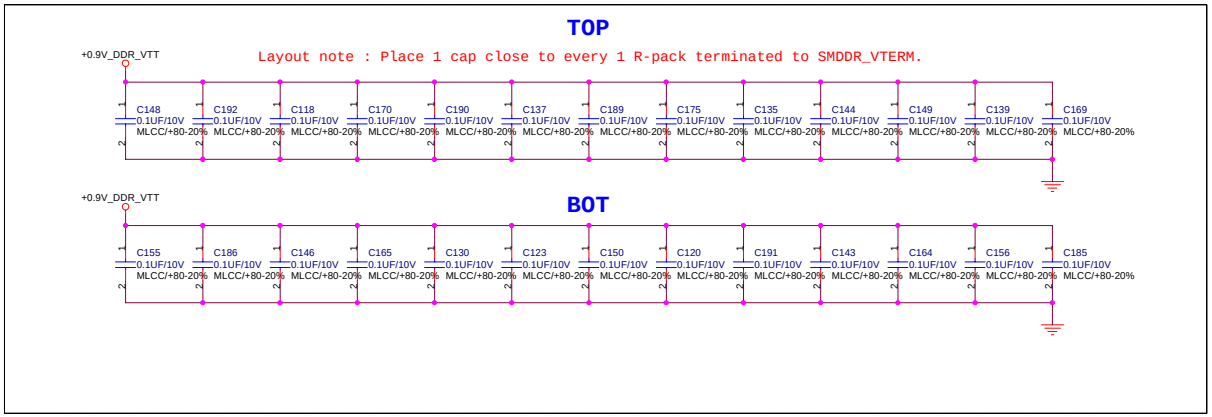
R172 10KOhm 5%
R170 10KOhm 5%

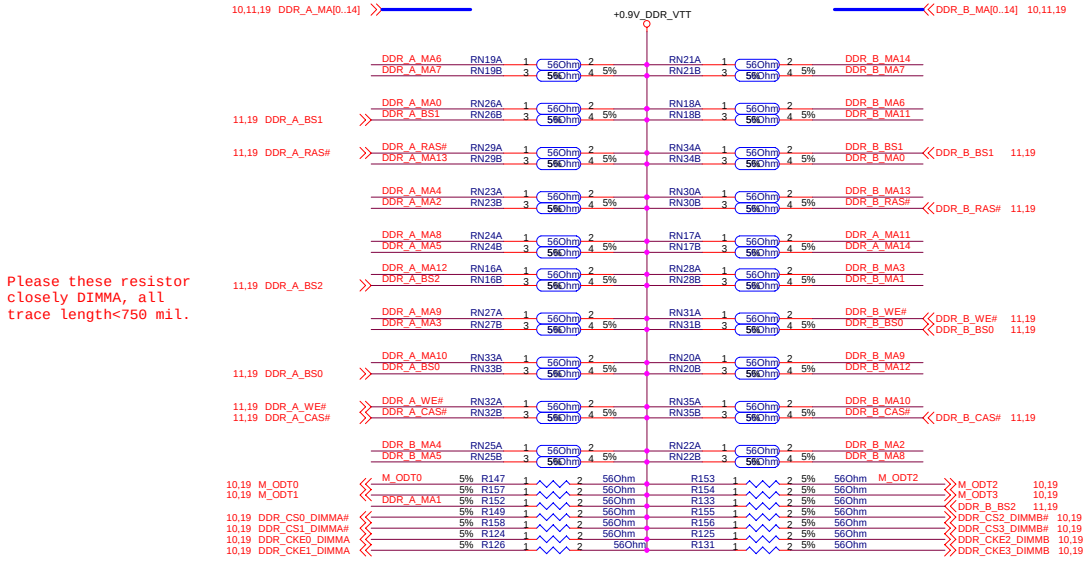
Non-iAMT
+3.3V_RUN

+1.8V_SUS
Please these Caps near So-Dimm1
C154 C119 C163 C147 C168
2.2UF/6.3V MLCC/+/-10% pt_c0603
C128 C136 C153 C125
0.1UF/10V MLCC/+80-20% pt_c0603

+1.8V_SUS
Please these Caps near So-Dimm2
C138 C395 C379 C151 C142
2.2UF/6.3V MLCC/+/-10% pt_c0603
C167 C384 C388 C393
0.1UF/10V MLCC/+80-20% pt_c0603

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***DDR2 SO-DIMM (0)***
	SHEET **19** OF **68**	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER :
		RELEASE DATE :	

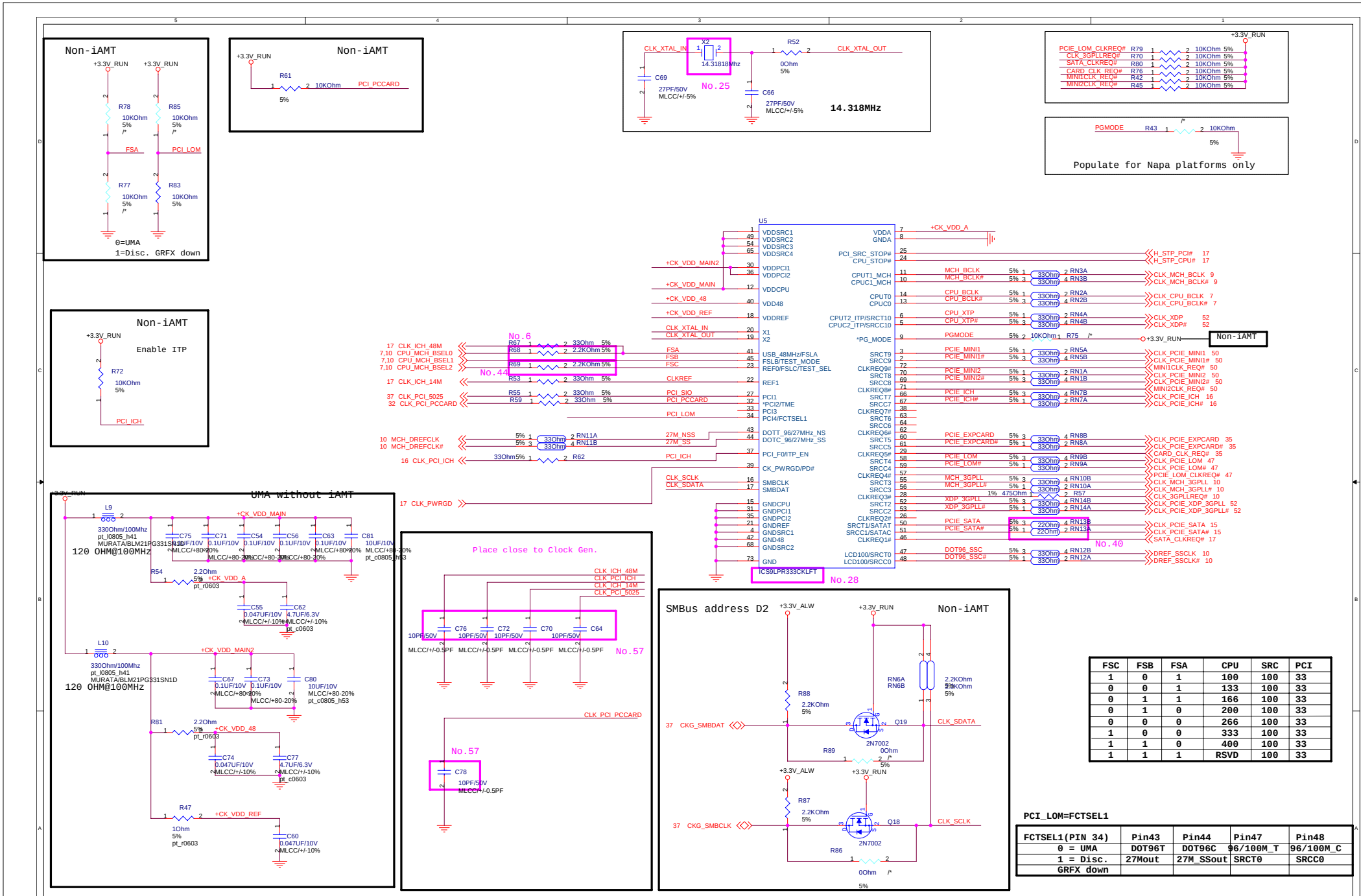




Please these resistor closely DIMMA, all trace length<750 mil.

Please these resistor closely DIMMB, all trace length<750 mil.

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***DDR2 SO-DIMM (1)***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
		SHEET **20** OF **68**		RELEASE DATE :		



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM=FCTSEL1

FCTSEL1(PIN 34)	Pin43	Pin44	Pin47	Pin48
0 = UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27M_SSout	SRCT0	SRCC0

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 21 OF 68	CLK GEN. CY28547	RELEASE DATE :		

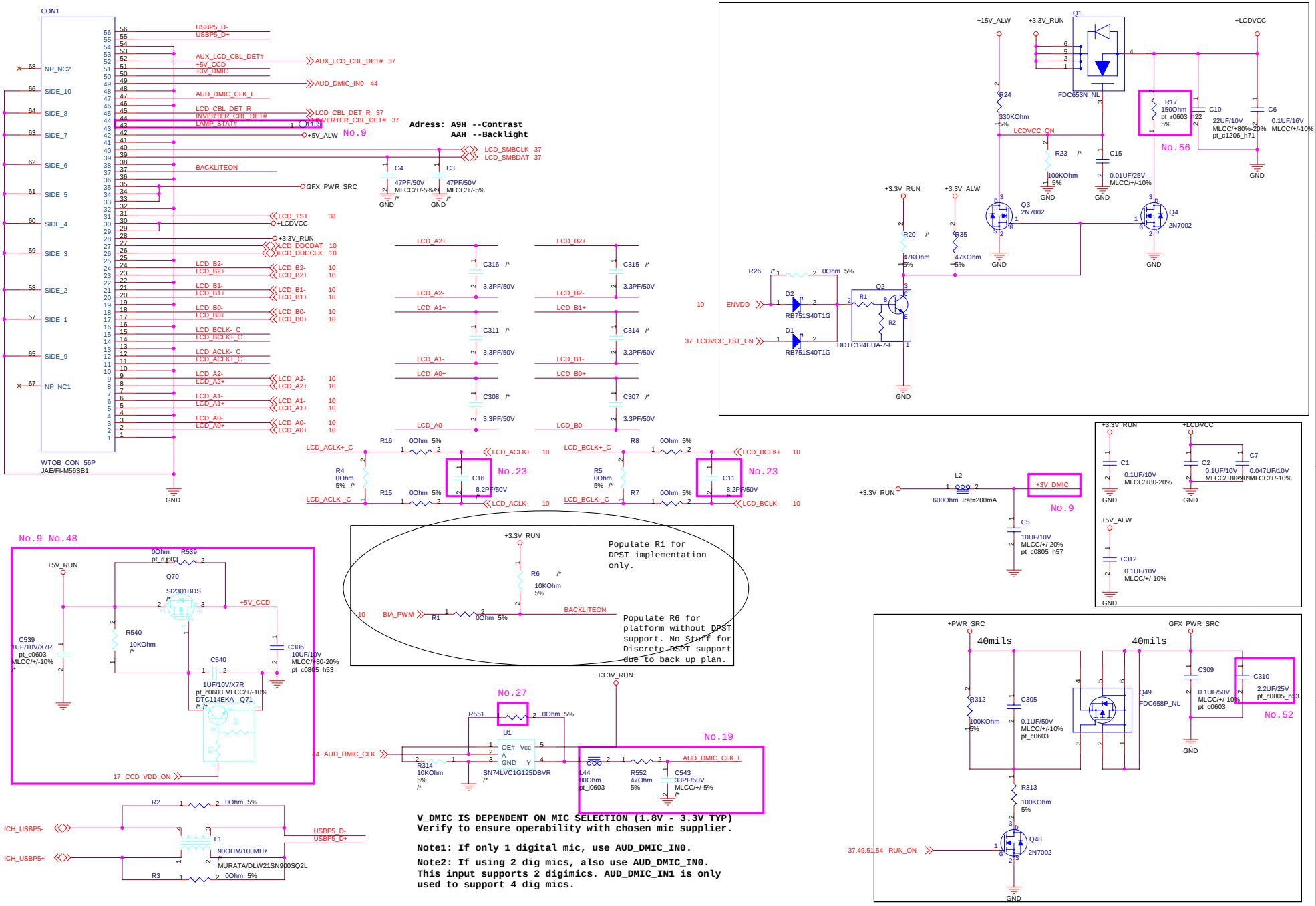
PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 23 OF 68		RELEASE DATE :		

PROJECT: **Lanai**	REVISION	DATE: **Monday, March 19, 2007**	DESCRIPTION:	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
	1.2	SHEET **24** OF **68**		RELEASE DATE :		

PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 25 OF 68		RELEASE DATE :		

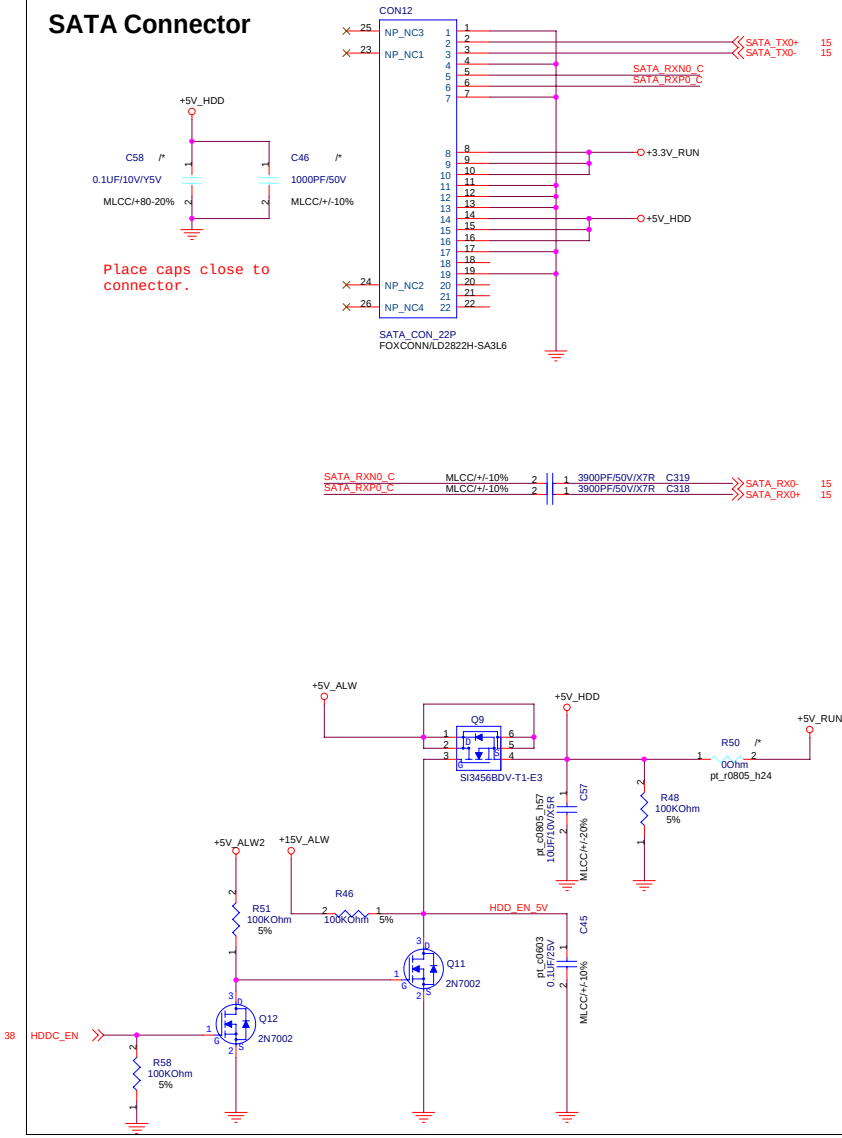
PROJECT: **Lanai**	REVISION	DATE: **Monday, March 19, 2007**	DESCRIPTION:	SCHEMATIC FILE NAME :		DESIGN ENGINEER :
	1.2	SHEET **26** OF **68**		RELEASE DATE :		

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER : *Sean Kuo*
		SHEET **27** OF **68**		RELEASE DATE :	

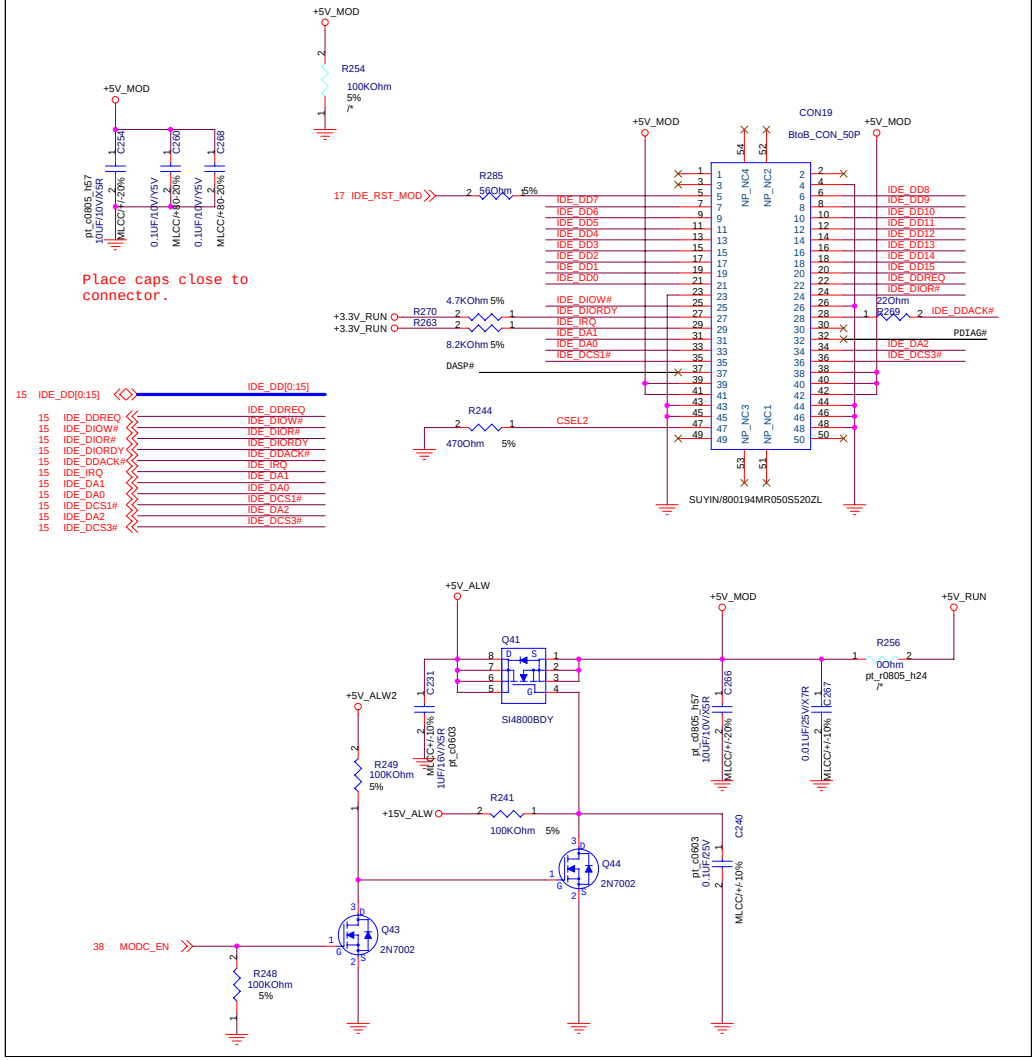


PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: LVDS CON	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 28 OF 68		RELEASE DATE :	

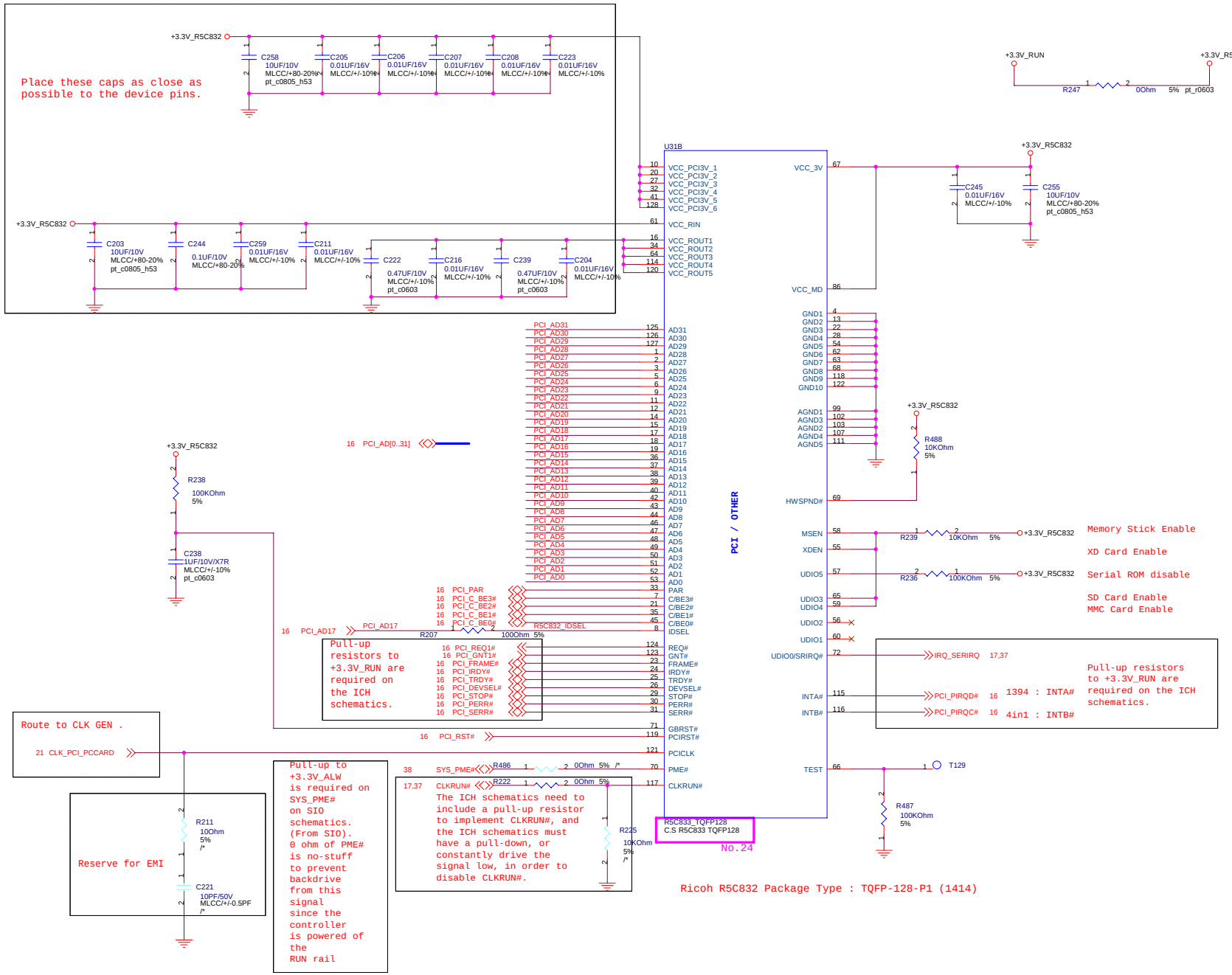
SATA Connector



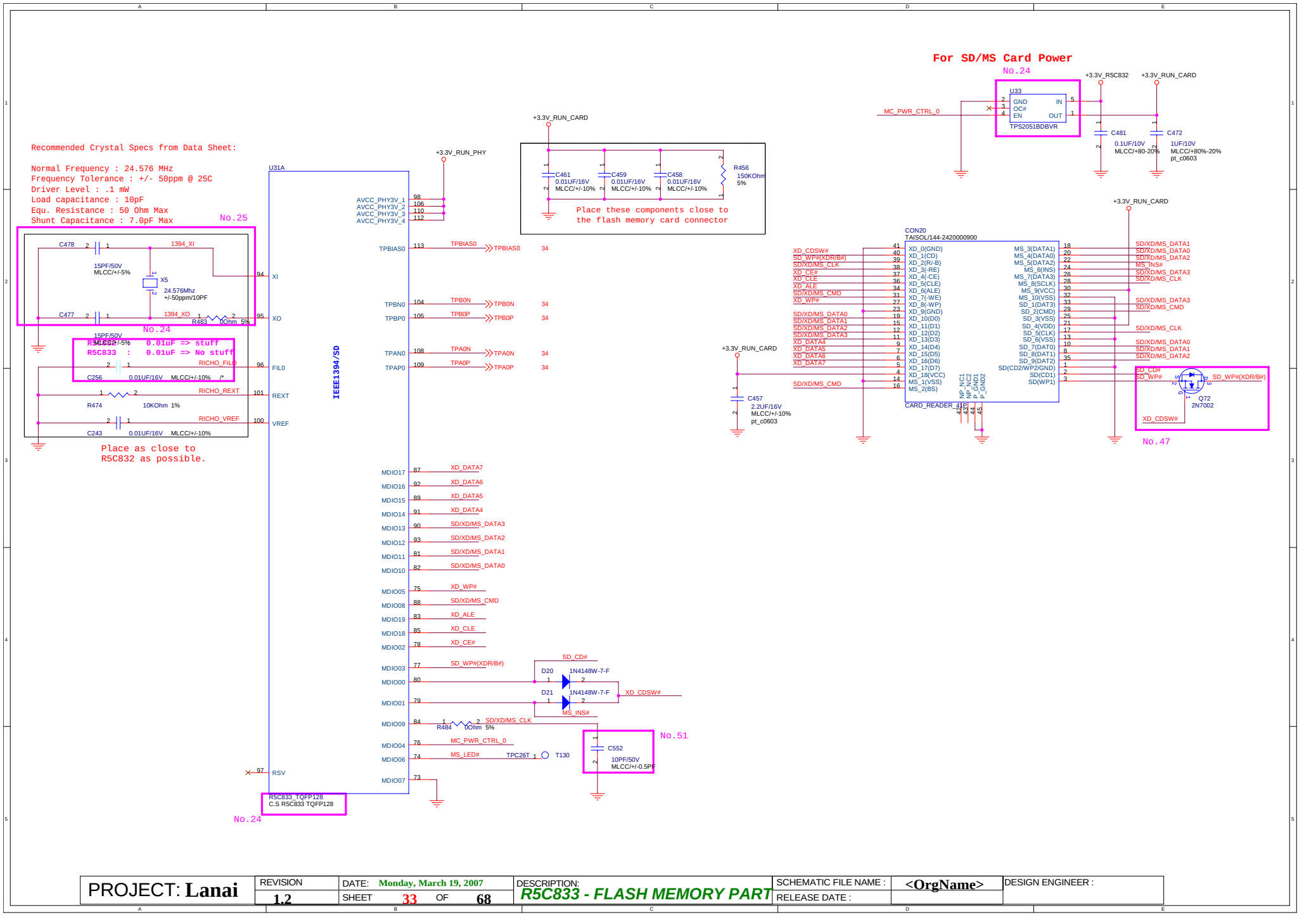
ODD Connector

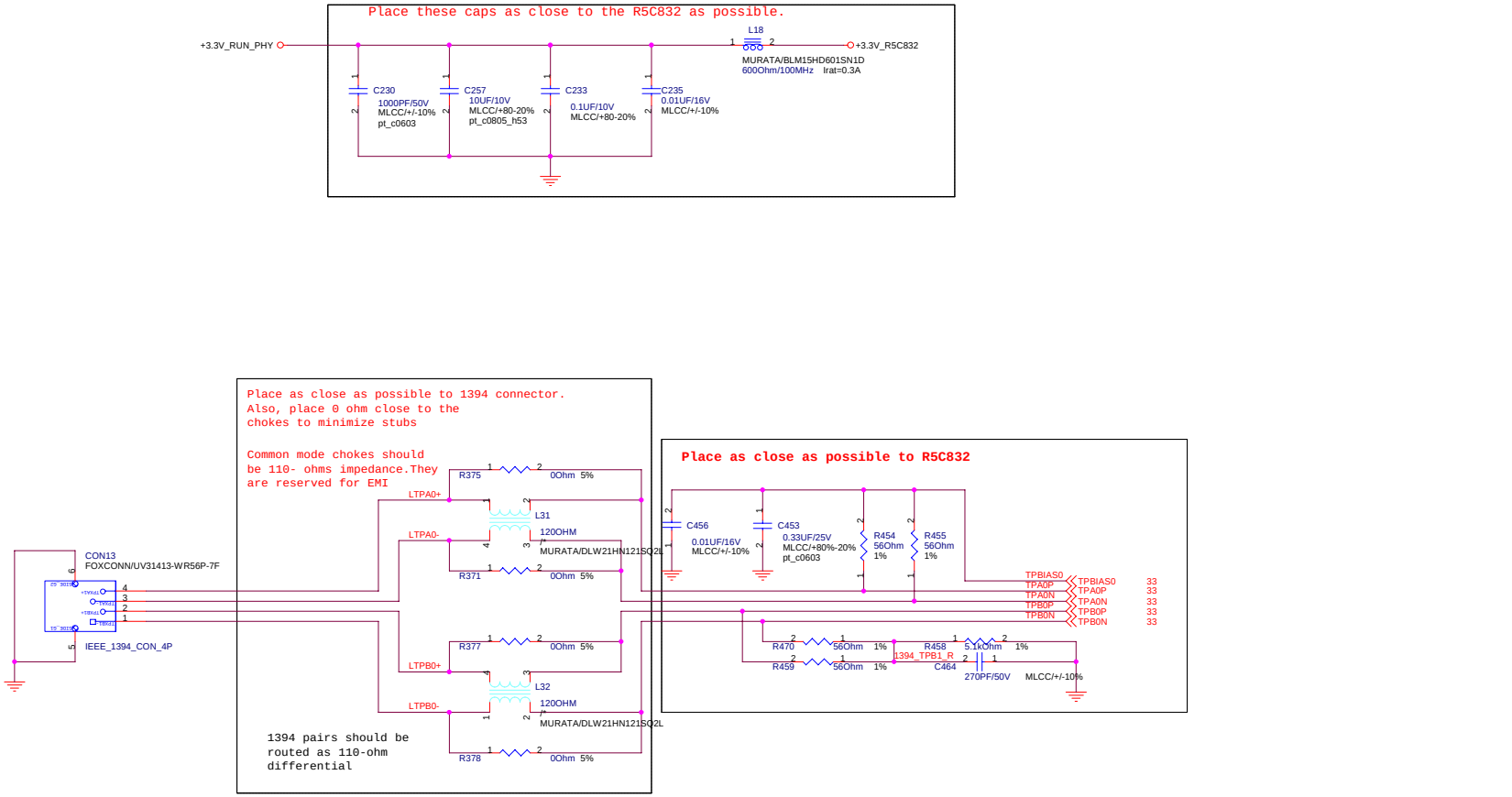


PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***SATA(HDD & CD_ROM)***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
		SHEET **31** OF **68**		RELEASE DATE :		



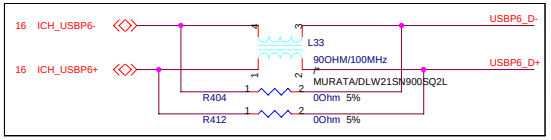
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***R5C833 - PCI INTERFACE***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
		SHEET **32** OF **68**		RELEASE DATE :		

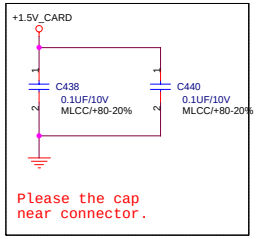

Recommended Crystal Specs from Data Sheet:
Normal Frequency : 24.576 MHz
Frequency Tolerance : +/- 50ppm @ 25C
Driver Level : .1 mW
Load capacitance : 10pF
Equ. Resistance : 50 Ohm Max
Shunt Capacitance : 7.0pF Max
No.25
C478
1394_XI
15PF/50V MLCC/+/-5%
X5
24.576Mhz +/-50ppm/10PF
C477
1394_XO
R483 0Ohm 5%
No.24
R5C832 : 0.01uF => stuff
R5C833 : 0.01uF => No stuff
C256 0.01UF/16V MLCC/+/-10% /*
RICHO_FIL0
RICHO_REXT
R474 10KOhm 1%
RICHO_VREF
C243 0.01UF/16V MLCC/+/-10%
Place as close to R5C832 as possible.
U31A
XI
XO
FIL0
REXT
VREF
RSV
IEEE1394/SD
R5C833_TQFP128
C.S R5C833 TQFP128
No.24
+3.3V_RUN_PHY
AVCC_PHY3V_1
AVCC_PHY3V_2
AVCC_PHY3V_3
AVCC_PHY3V_4
TPBIAS0
TPB0N
TPB0P
TPA0N
TPA0P
+3.3V_RUN_CARD
C461 0.01UF/16V MLCC/+/-10%
C459 0.01UF/16V MLCC/+/-10%
C458 0.01UF/16V MLCC/+/-10%
R456 150KOhm 5%
Place these components close to the flash memory card connector
MDIO17 XD_DATA7
MDIO16 XD_DATA6
MDIO15 XD_DATA5
MDIO14 XD_DATA4
MDIO13 SD/XD/MS_DATA3
MDIO12 SD/XD/MS_DATA2
MDIO11 SD/XD/MS_DATA1
MDIO10 SD/XD/MS_DATA0
MDIO05 XD_WP#
MDIO08 SD/XD/MS_CMD
MDIO19 XD_ALE
MDIO18 XD_CLE
MDIO02 XD_CE#
MDIO03 SD_WP#(XDR/B#)
MDIO00 SD_CD#
MDIO01 XD_CDSW#
MDIO09 SD/XD/MS_CLK
MDIO04 MC_PWR_CTRL_0
MDIO06 MS_LED#
MDIO07
D20 1N4148W-7-F
D21 1N4148W-7-F
MS_INS#
R484 0Ohm 5%
TPC26T
T130
C552 10PF/50V MLCC/+/-0.5PF
No.51
For SD/MS Card Power
No.24
U33
GND
OC#
EN
IN
OUT
TPS2051BDBVR
MC_PWR_CTRL_0
+3.3V_R5C832
+3.3V_RUN_CARD
C481 0.1UF/10V MLCC/+80-20%
C472 1UF/10V MLCC/+80%-20% pt_c0603
CON20
TAISOL/144-2420000900
CARD_READER_41P
XD_0(GND)
XD_1(CD)
XD_2(R/-B)
XD_3(-RE)
XD_4(-CE)
XD_5(CLE)
XD_6(ALE)
XD_7(-WE)
XD_8(-WP)
XD_9(GND)
XD_10(D0)
XD_11(D1)
XD_12(D2)
XD_13(D3)
XD_14(D4)
XD_15(D5)
XD_16(D6)
XD_17(D7)
XD_18(VCC)
MS_1(VSS)
MS_2(BS)
MS_3(DATA1)
MS_4(DATA0)
MS_5(DATA2)
MS_6(INS)
MS_7(DATA3)
MS_8(SCLK)
MS_9(VCC)
MS_10(VSS)
SD_1(DAT3)
SD_2(CMD)
SD_3(VSS)
SD_4(VDD)
SD_5(CLK)
SD_6(VSS)
SD_7(DAT0)
SD_8(DAT1)
SD_9(DAT2)
SD(CD2/WP2/GND)
SD(CD1)
SD(WP1)
NP_NC1
NP_NC2
P_GND1
P_GND2
+3.3V_RUN_CARD
C457 2.2UF/16V MLCC/+/-10% pt_c0603
SD/XD/MS_DATA1
SD/XD/MS_DATA0
SD/XD/MS_DATA2
MS_INS#
SD/XD/MS_DATA3
SD/XD/MS_CLK
SD/XD/MS_CMD
SD_CD#
SD_WP#
SD_WP#(XDR/B#)
Q72 2N7002
XD_CDSW#
No.47
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 33 OF 68
DESCRIPTION: R5C833 - FLASH MEMORY PART
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER :

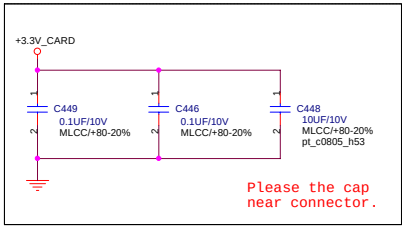


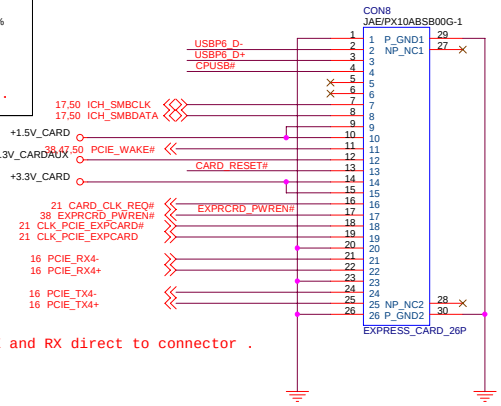
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***R5C833 - IEEE1394 PART***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
		SHEET **34** OF **68**		RELEASE DATE :		

Express Card



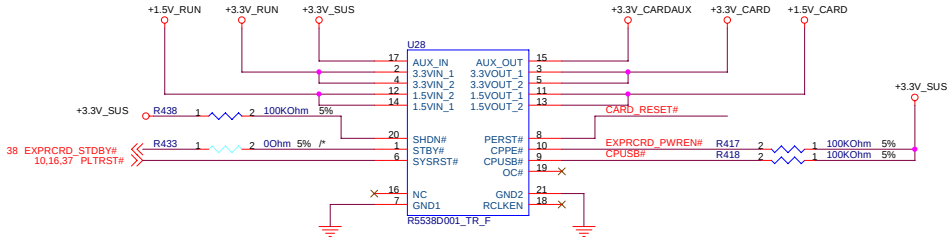


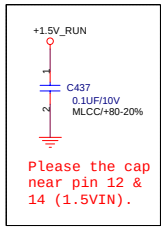


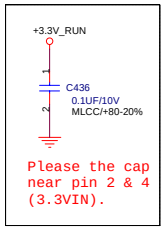


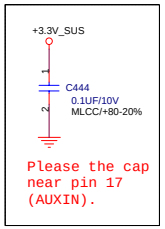
PCI-Express TX and RX direct to connector .

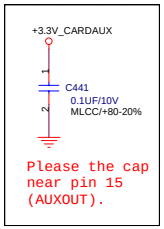
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

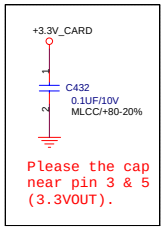


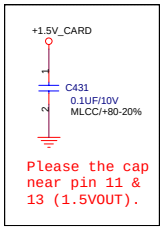




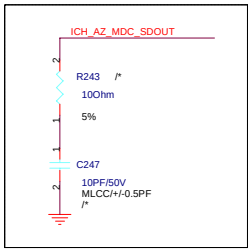


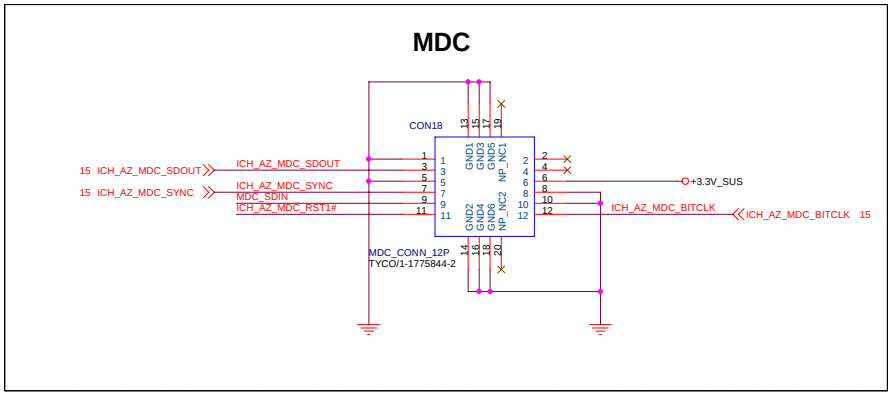


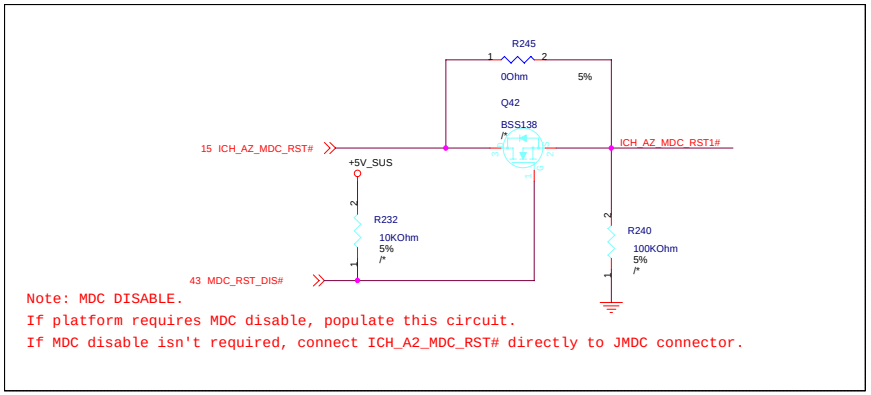


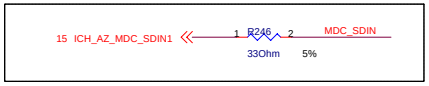


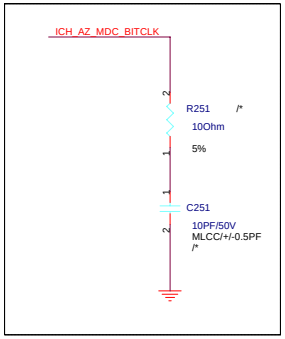
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***PCI-Express Card***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
		SHEET **35** OF **68**		RELEASE DATE :		***Terry_Lin***

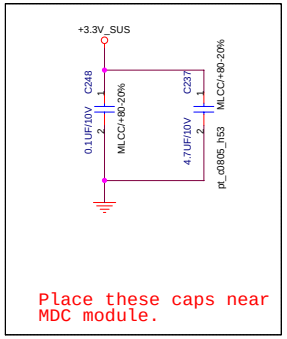




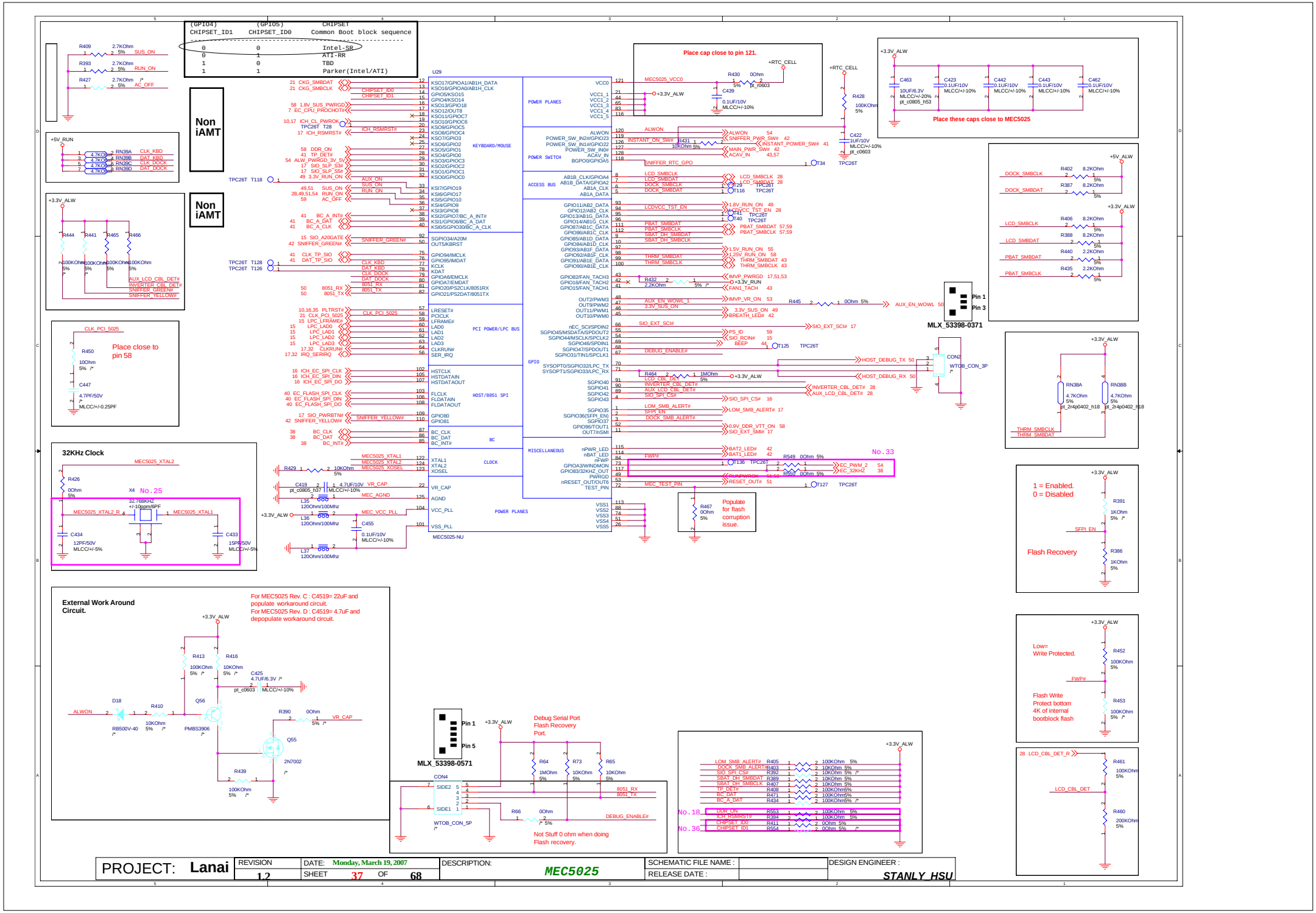


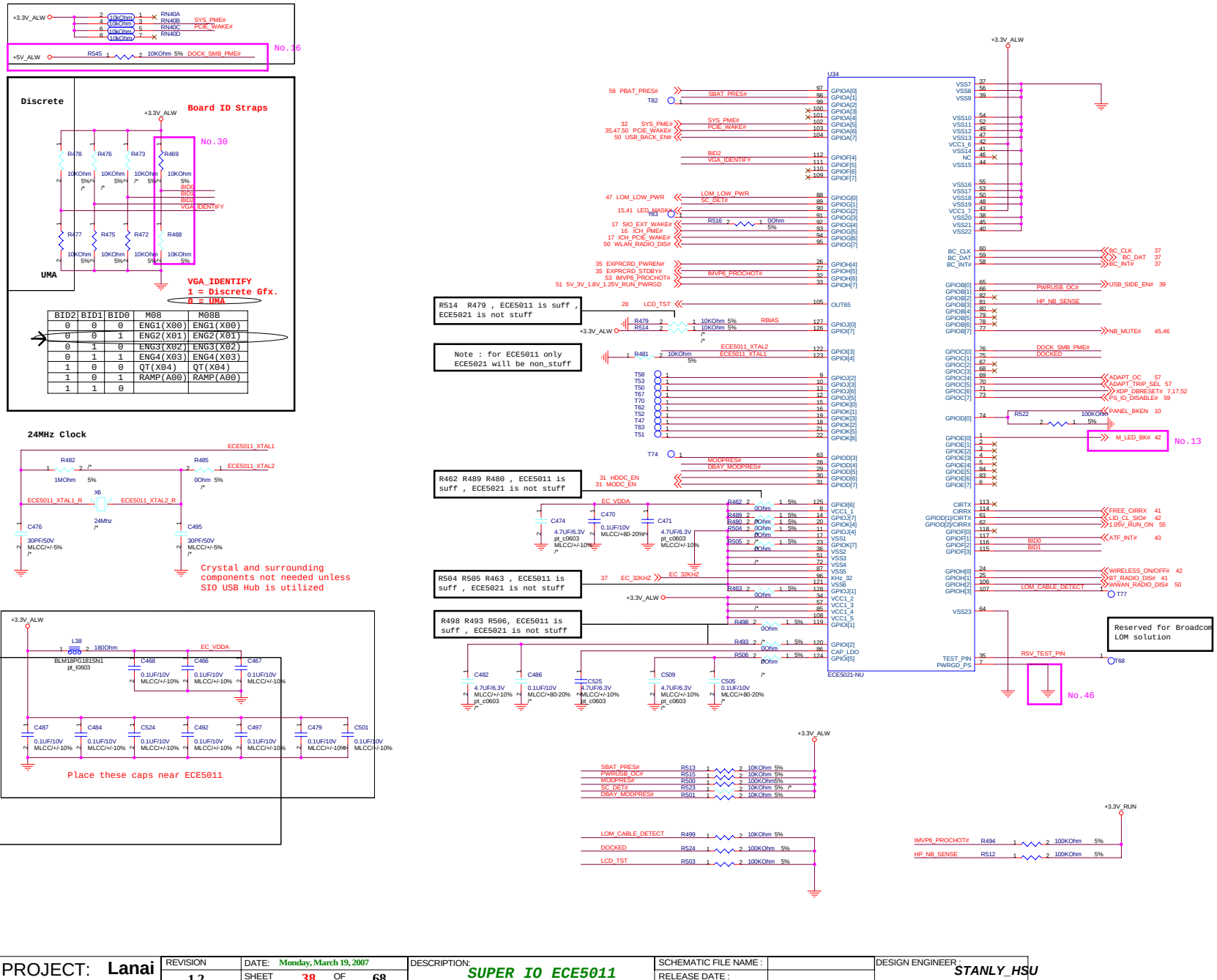




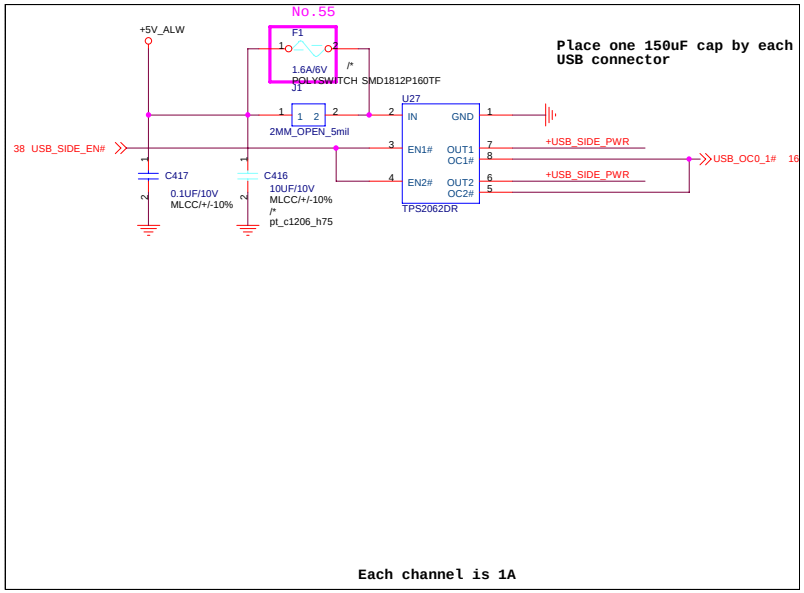


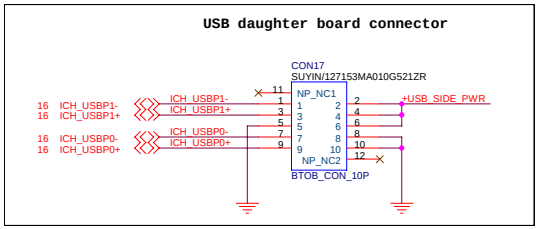
PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 36 OF 68	*MDC CONN*	RELEASE DATE :		


(GPIO4) (GPIO5) CHIPSET
CHIPSET_ID1 CHIPSET_ID0 Common Boot block sequence
0 0 Intel-SR
0 1 ATI-RR
1 0 TBD
1 1 Parker(Intel/ATI)
Non iAMT
Non iAMT
Place cap close to pin 121.
Place these caps close to MEC5025
Place close to pin 58
32KHz Clock
External Work Around Circuit.
For MEC5025 Rev. C : C4519= 22uF and populate workaround circuit.
For MEC5025 Rev. D : C4519= 4.7uF and depopulate workaround circuit.
Populate for flash corruption issue.
No.33
No.25
No.18
No.36
1 = Enabled.
0 = Disabled
Flash Recovery
Low= Write Protected.
Flash Write Protect bottom 4K of internal bootblock flash
Debug Serial Port Flash Recovery Port.
Not Stuff 0 ohm when doing Flash recovery.
MLX_53398-0371
MLX_53398-0371
U29
MEC5025-NU
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 37 OF 68
DESCRIPTION: MEC5025
SCHEMATIC FILE NAME :
RELEASE DATE :
DESIGN ENGINEER : STANLY_HSU

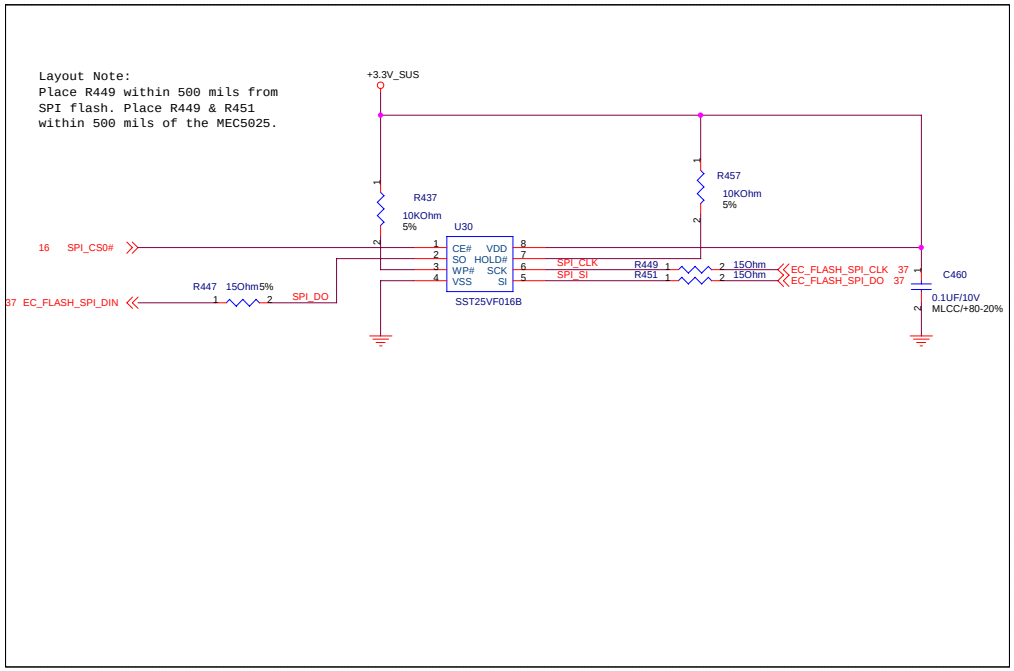


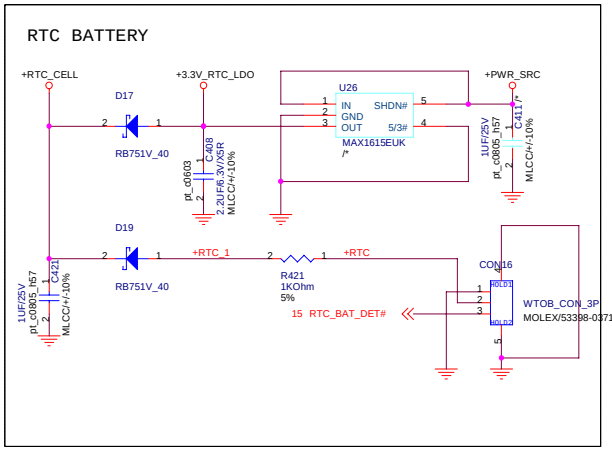
PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: ***SUPER IO ECE5011***	SCHEMATIC FILE NAME :		DESIGN ENGINEER : ***STANLY_HSU***
		SHEET 38 OF 68		RELEASE DATE :		

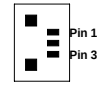




PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 39 OF 68	*USB PORT x 2*	RELEASE DATE :		*Terry_Lin*

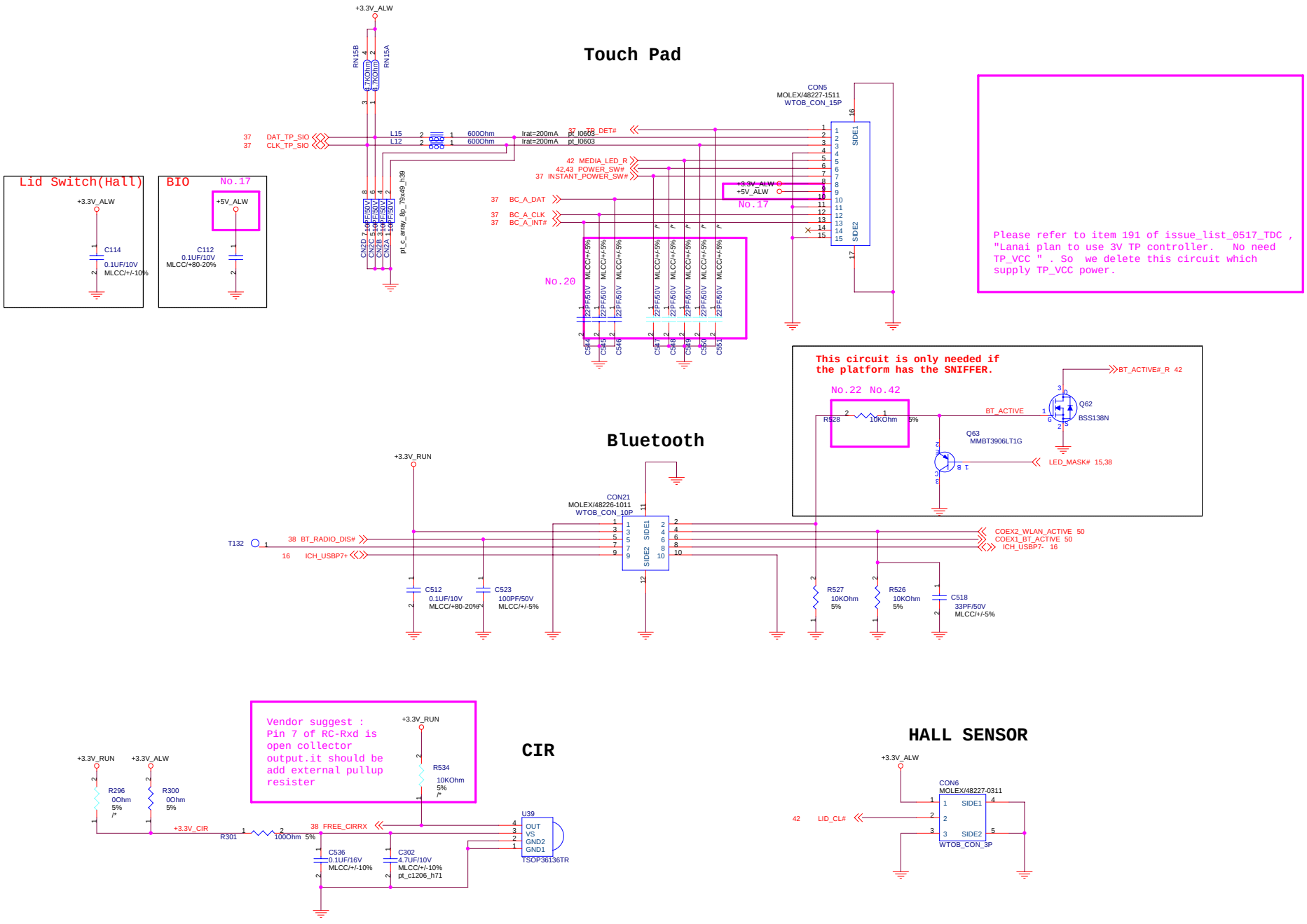




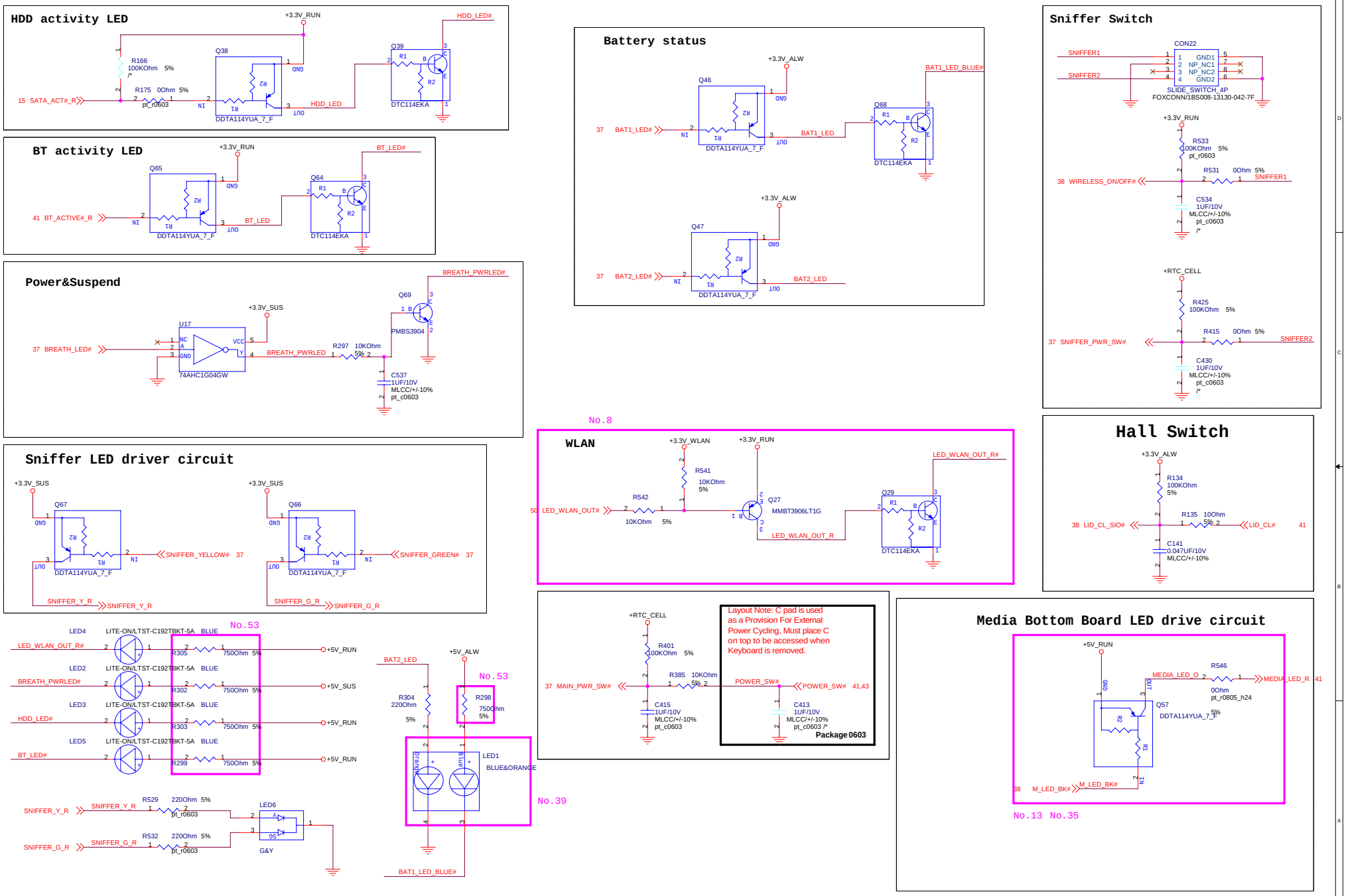


MLX_53398-0371

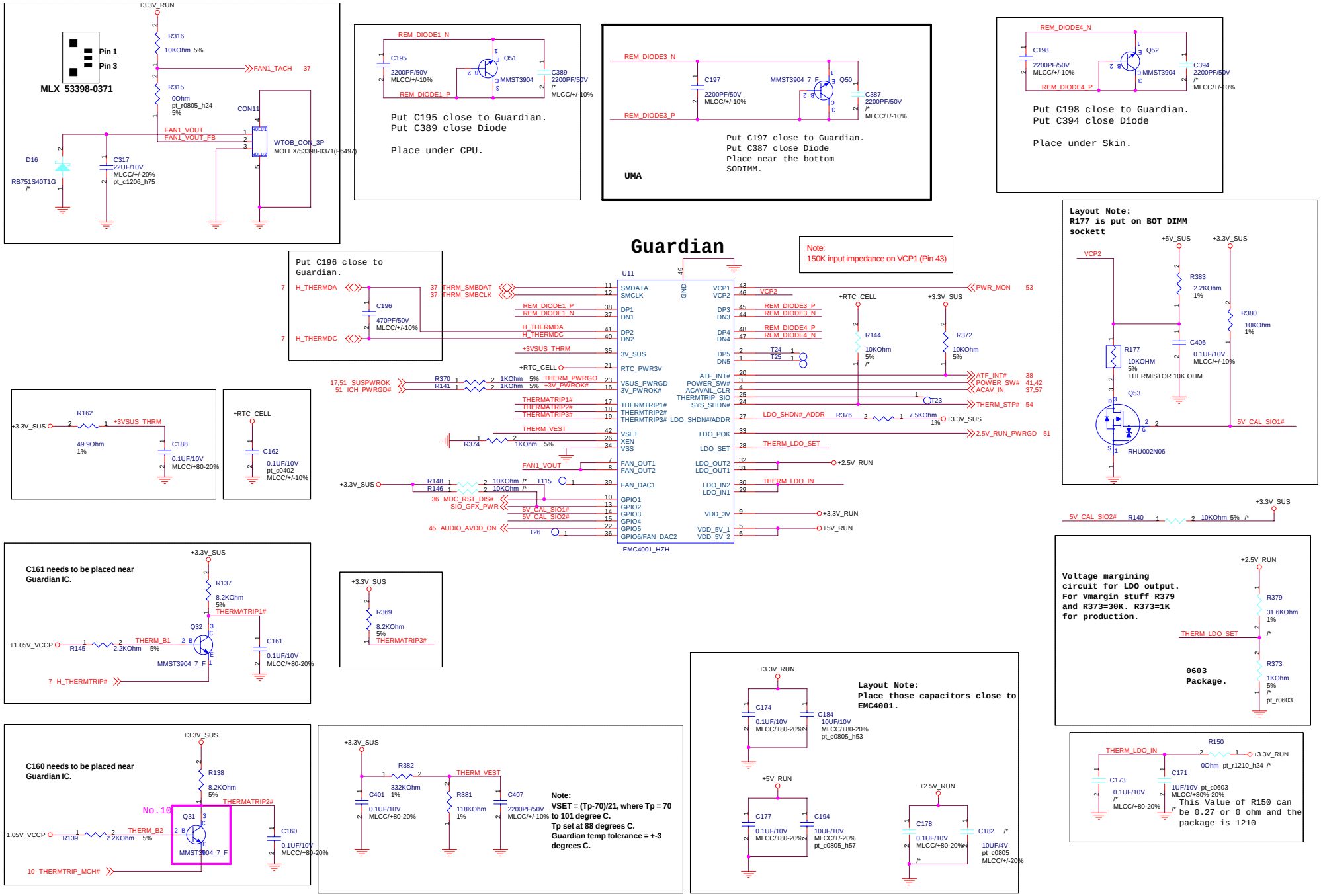
PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 40 OF 68	*FLASH & RTC*	RELEASE DATE :		*C.L. Ho*

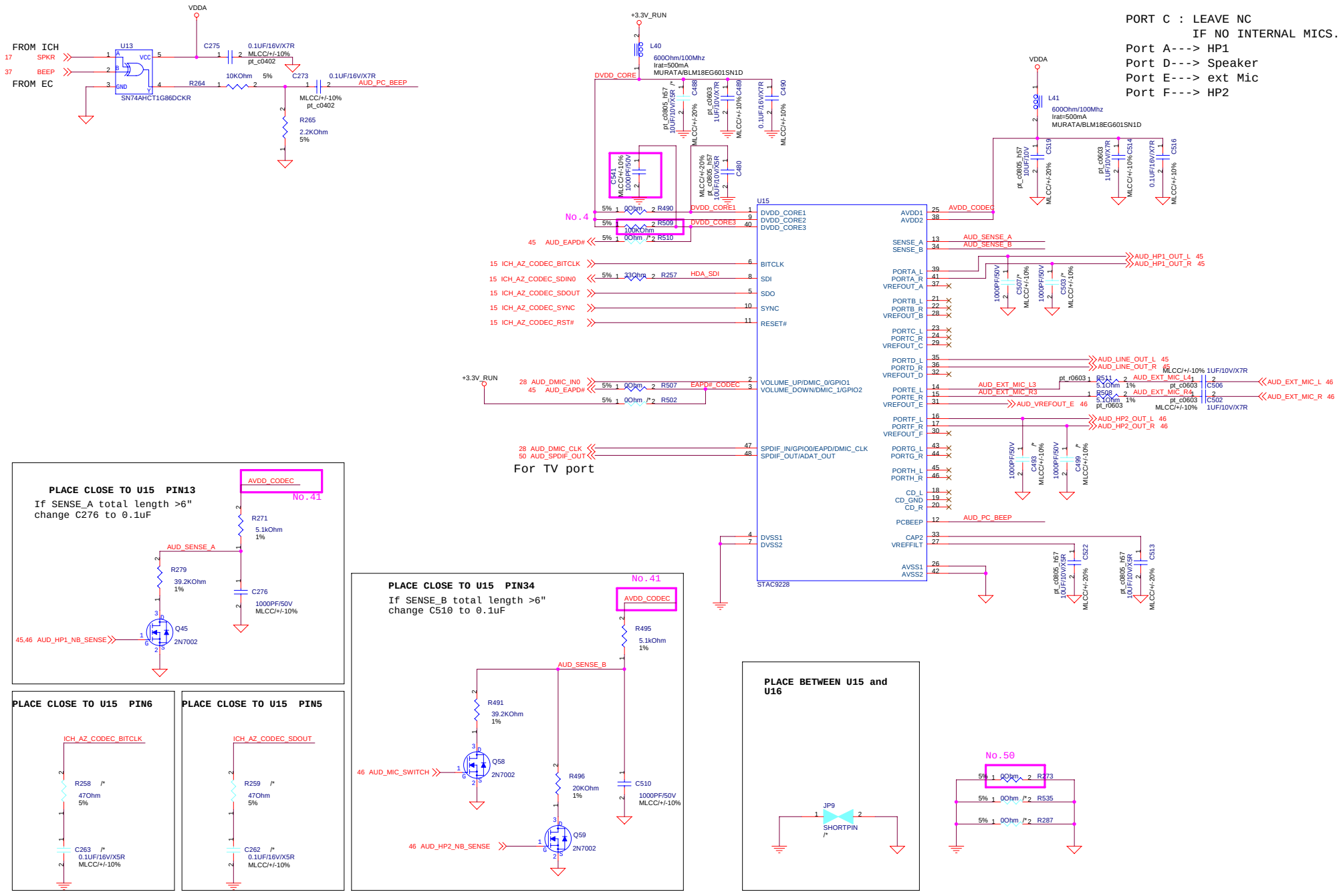


PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***TOUCH PAD & BT & CIR & LID***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
		SHEET **41** OF **68**		RELEASE DATE :		

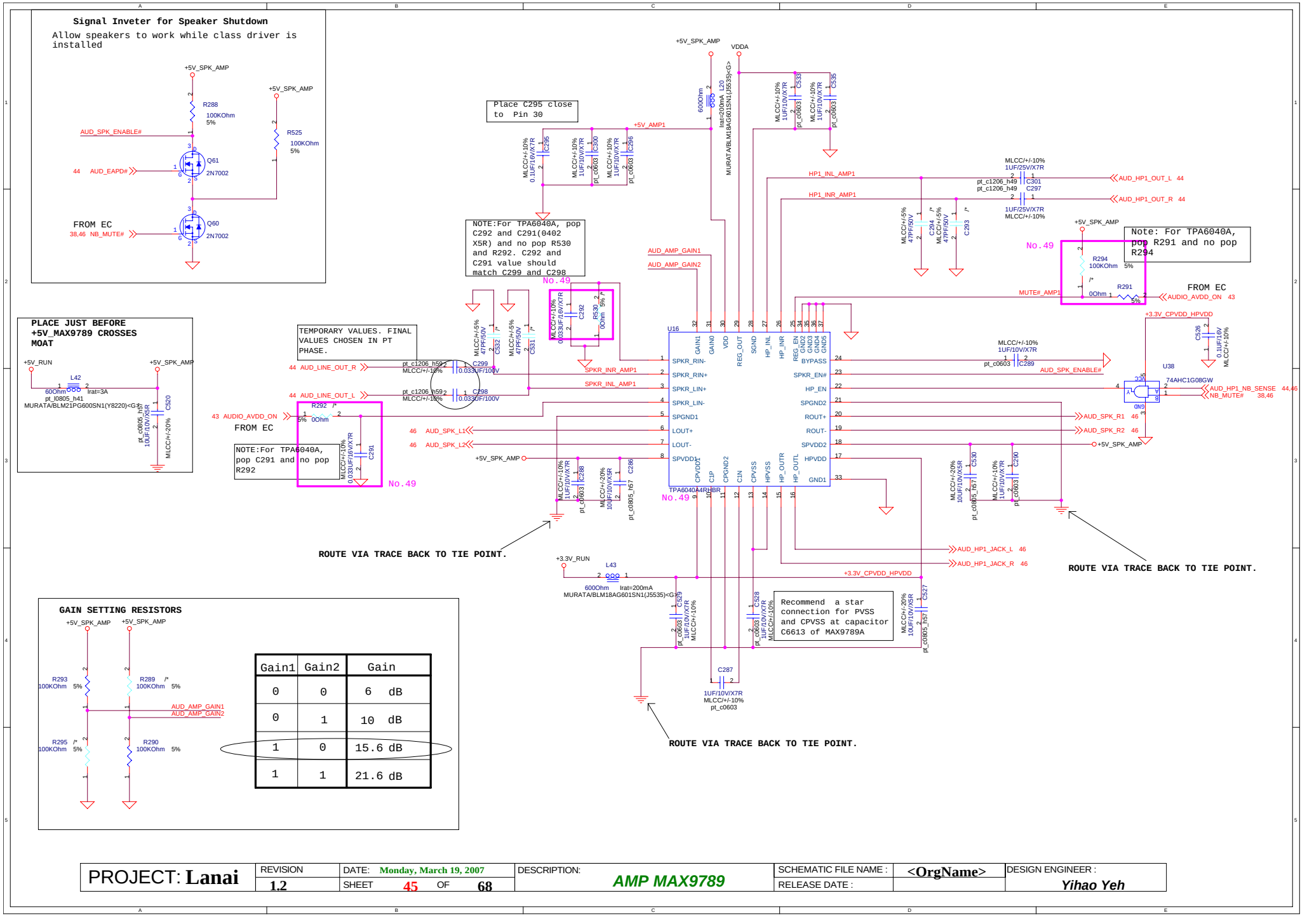


PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 42 OF 68	SWITCH & LED	RELEASE DATE :		C


Guardian
MLX_53398-0371
Pin 1
Pin 3
R316
10KOhm 5%
R315
0Ohm
pt_r0805_h24
5%
FAN1_TACH
FAN1_VOUT
FAN1_VOUT_FB
CON11
WTOB_CON_3P
MOLEX/53398-0371(F6497)
D16
RB751S40T1G
C317
22UF/10V
MLCC/+/-20%
pt_c1206_h75
REM_DIODE1_N
REM_DIODE1_P
C195
2200PF/50V
MLCC/+/-10%
Q51
MMST3904
C389
Put C195 close to Guardian.
Put C389 close Diode
Place under CPU.
REM_DIODE3_N
REM_DIODE3_P
C197
MMST3904_7_F
Q50
C387
Put C197 close to Guardian.
Put C387 close Diode
Place near the bottom SODIMM.
UMA
REM_DIODE4_N
REM_DIODE4_P
C198
Q52
C394
Put C198 close to Guardian.
Put C394 close Diode
Place under Skin.
Put C196 close to Guardian.
H_THERMDA
H_THERMDC
C196
470PF/50V
MLCC/+/-10%
U11
EMC4001_HZH
SMDATA
SMCLK
THRM_SMBDAT
THRM_SMBCLK
DP1
DN1
DP2
DN2
3V_SUS
RTC_PWR3V
VSUS_PWRGD
3V_PWROK#
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
VSET
XEN
VSS
FAN_OUT1
FAN_OUT2
FAN_DAC1
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6/FAN_DAC2
GND
VCP1
VCP2
DP3
DN3
DP4
DN4
DP5
DN5
ATF_INT#
POWER_SW#
ACAVAIL_CLR
THERMTRIP_SIO
SYS_SHDN#
LDO_SHDN#/ADDR
LDO_POK
LDO_SET
LDO_OUT2
LDO_OUT1
LDO_IN2
LDO_IN1
VDD_3V
VDD_5V_1
VDD_5V_2
PWR_MON
ACAV_IN
THERM_STP#
2.5V_RUN_PWRGD
THERM_LDO_SET
THERM_LDO_IN
Note:
150K input impedance on VCP1 (Pin 43)
Layout Note:
R177 is put on BOT DIMM sockett
R177
10KOHM
5%
THERMISTOR 10K OHM
Q53
RHU002N06
R383
2.2KOhm
1%
R380
10KOhm
C406
0.1UF/10V
MLCC/+/-10%
5V_CAL_SIO1#
5V_CAL_SIO2#
R140
R162
49.9Ohm
C188
0.1UF/10V
MLCC/+80-20%
C162
0.1UF/10V
pt_c0402
MLCC/+/-10%
C161 needs to be placed near Guardian IC.
R137
8.2KOhm
THERMATRIP1#
Q32
MMST3904_7_F
R145
2.2KOhm
THERM_B1
C161
0.1UF/10V
MLCC/+80-20%
R369
THERMATRIP3#
C160 needs to be placed near Guardian IC.
No.16
R138
THERMATRIP2#
Q31
R139
THERM_B2
C160
R382
332KOhm
C401
R381
118KOhm
C407
2200PF/50V
MLCC/+/-10%
Note:
VSET = (Tp-70)/21, where Tp = 70 to 101 degree C.
Tp set at 88 degrees C.
Guardian temp tolerance = +-3 degrees C.
Layout Note:
Place those capacitors close to EMC4001.
C174
C184
10UF/10V
MLCC/+80-20%
pt_c0805_h53
C177
C194
pt_c0805_h57
C178
C182
10UF/4V
pt_c0805
Voltage margining circuit for LDO output.
For Vmargin stuff R379 and R373=30K. R373=1K for production.
0603 Package.
R379
31.6KOhm
R373
1KOhm
pt_r0603
R150
0Ohm
pt_r1210_h24
C173
C171
1UF/10V
pt_c0603
MLCC/+80%-20%
This Value of R150 can be 0.27 or 0 ohm and the package is 1210
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 43 OF 68
DESCRIPTION: EMC4001
SCHEMATIC FILE NAME :
RELEASE DATE :
DESIGN ENGINEER : N

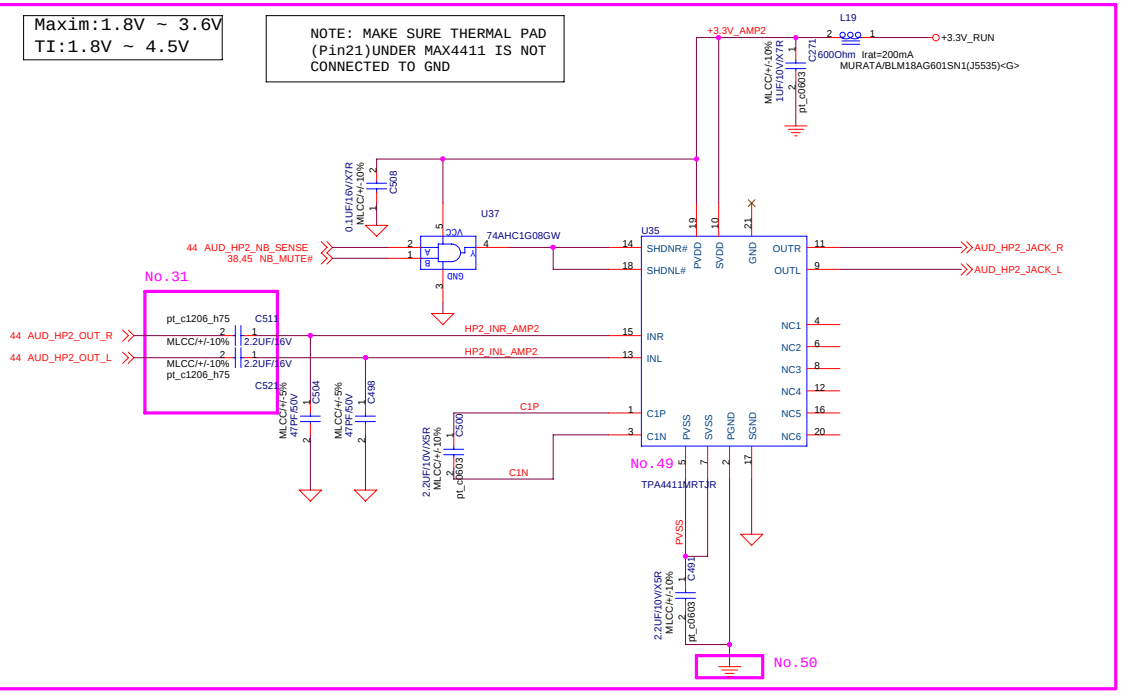


PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***STAC9228***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Yihao Yeh***
		SHEET **44** OF **68**		RELEASE DATE :	

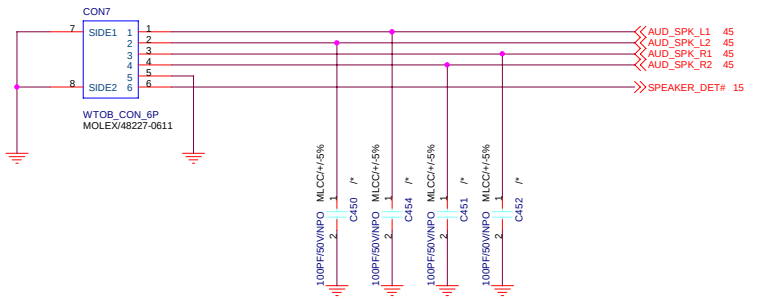

Signal Inveter for Speaker Shutdown
Allow speakers to work while class driver is installed
+5V_SPK_AMP
R288
100KOhm
5%
AUD_SPK_ENABLE#
Q61
2N7002
44 AUD_EAPD#
R525
100KOhm
5%
FROM EC
38,46 NB_MUTE#
Q60
2N7002
PLACE JUST BEFORE +5V_MAX9789 CROSSES MOAT
+5V_RUN
L42
60Ohm
Irat=3A
pt_l0805_h41
MURATA/BLM21PG600SN1(Y8220)<G>
C520
pt_c0805_h57
10UF/10V/X5R
MLCC/+/-20%
TEMPORARY VALUES. FINAL VALUES CHOSEN IN PT PHASE.
43 AUDIO_AVDD_ON
FROM EC
R292
0Ohm
NOTE:For TPA6040A, pop C291 and no pop R292
C291
0.033UF/16V/X7R
No.49
Place C295 close to Pin 30
+5V_AMP1
C295
C300
C296
0.1UF/16V/X7R
1UF/10V/X7R
pt_c0603
NOTE:For TPA6040A, pop C292 and C291(0402 X5R) and no pop R530 and R292. C292 and C291 value should match C299 and C298
C292
R530
0Ohm
C532
C531
47PF/50V
C299
C298
0.033UF/100V
44 AUD_LINE_OUT_R
44 AUD_LINE_OUT_L
pt_c1206_h59
MLCC/+/-10%
+5V_SPK_AMP
VDDA
600Ohm
Irat=200mA
L20
MURATA/BLM18AG601SN1(J5535)<G>
C535
C533
C536
HP1_INL_AMP1
HP1_INR_AMP1
AUD_HP1_OUT_L 44
AUD_HP1_OUT_R 44
1UF/25V/X7R
MLCC/+/-10%
pt_c1206_h49
C301
C297
C294
C293
MLCC/+/-5%
47PF/50V
AUD_AMP_GAIN1
AUD_AMP_GAIN2
SPKR_INR_AMP1
SPKR_INL_AMP1
MUTE#_AMP1
R294
100KOhm
5%
R291
0Ohm
FROM EC
AUDIO_AVDD_ON 43
Note: For TPA6040A, pop R291 and no pop R294
+3.3V_CPVDD_HPVDD
C526
0.1UF/16V
U16
TPA6040A4RHBR
SPKR_RIN-
SPKR_RIN+
SPKR_LIN+
SPKR_LIN-
SPGND1
LOUT+
LOUT-
SPVDD1
GAIN1
GAIN0
VDD
REG_OUT
SGND
HP_INL
HP_INR
REG_EN
GND2
GND4
GND5
BYPASS
SPKR_EN#
HP_EN
SPGND2
ROUT+
ROUT-
SPVDD2
HPVDD
GND1
CPVDD1
C1P
CPGND2
C1N
CPVSS
HPVSS
HP_OUTR
HP_OUTL
AUD_SPK_ENABLE#
AUD_SPK_R1 46
AUD_SPK_R2 46
+5V_SPK_AMP
46 AUD_SPK_L1
46 AUD_SPK_L2
U38
74AHC1G08GW
AUD_HP1_NB_SENSE 44,46
NB_MUTE# 38,46
C288
C286
C530
C290
ROUTE VIA TRACE BACK TO TIE POINT.
+3.3V_RUN
L43
600Ohm
Irat=200mA
MURATA/BLM18AG601SN1(J5535)<G>
+3.3V_CPVDD_HPVDD
AUD_HP1_JACK_L 46
AUD_HP1_JACK_R 46
C529
C528
C527
C287
1UF/10V/X7R
MLCC/+/-10%
pt_c0603
Recommend a star connection for PVSS and CPVSS at capacitor C6613 of MAX9789A
ROUTE VIA TRACE BACK TO TIE POINT.
GAIN SETTING RESISTORS
+5V_SPK_AMP
R293
100KOhm
5%
R289
100KOhm
AUD_AMP_GAIN1
AUD_AMP_GAIN2
R295
100KOhm
R290
100KOhm
Gain1 Gain2 Gain
0 0 6 dB
0 1 10 dB
1 0 15.6 dB
1 1 21.6 dB
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 45 OF 68
DESCRIPTION: AMP MAX9789
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : Yihao Yeh

Maxim:1.8V ~ 3.6V
TI:1.8V ~ 4.5V

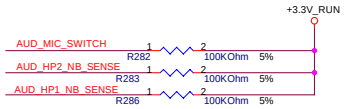
NOTE: MAKE SURE THERMAL PAD (Pin21)UNDER MAX4411 IS NOT CONNECTED TO GND

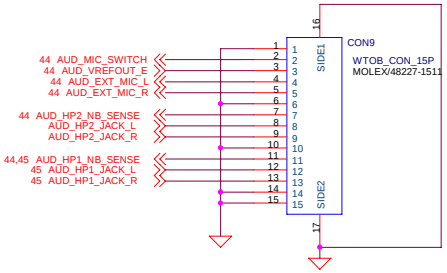


Speaker CON

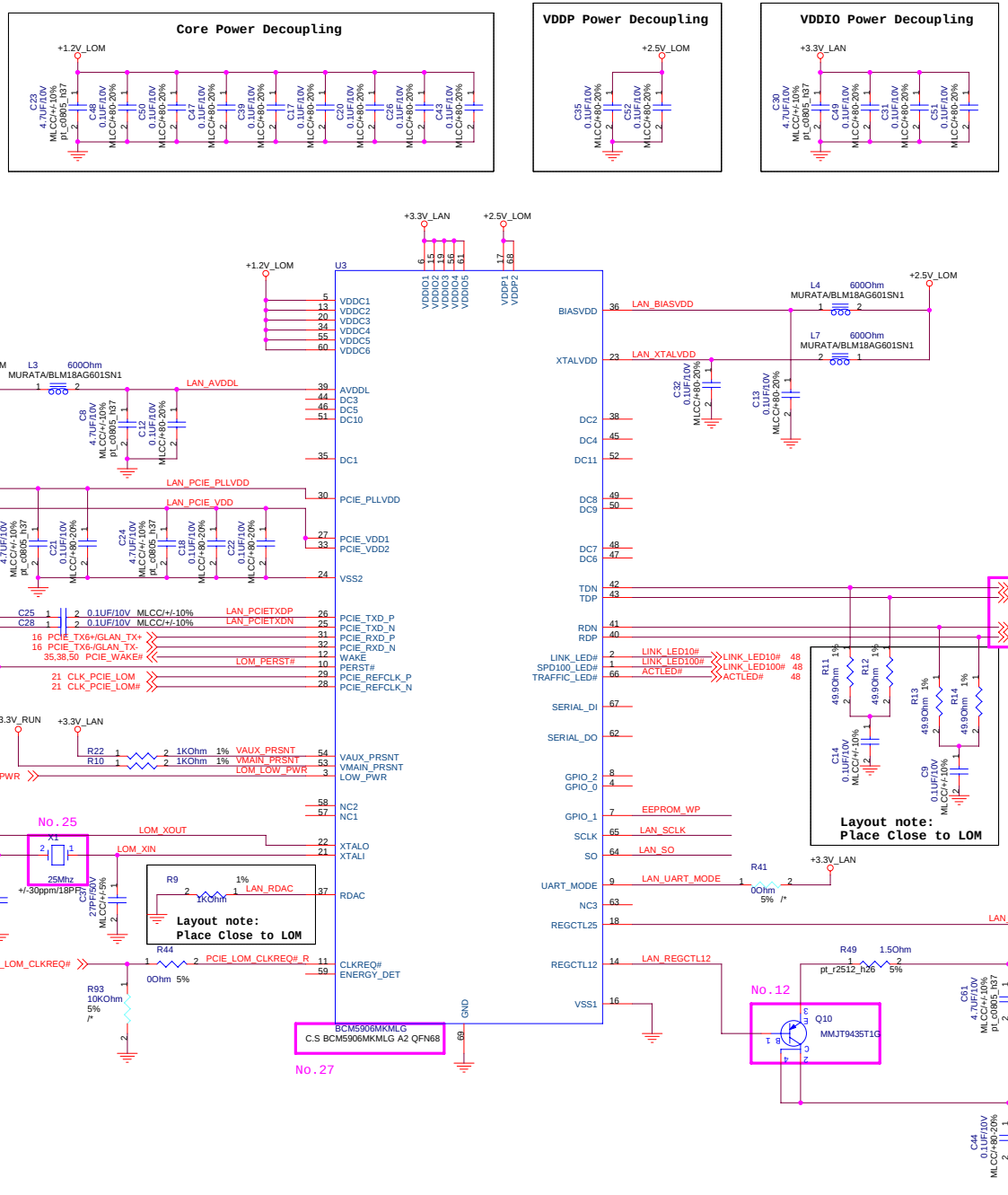


Need to adjust EMI cap values as necessary.

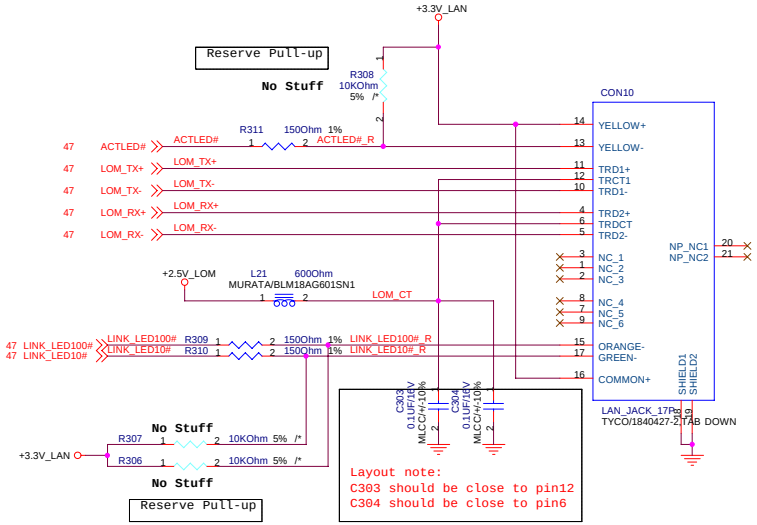




PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***AMP MAX4411 & AUDIO JACK***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Yihao Yeh***
		SHEET **46** OF **68**		RELEASE DATE :		

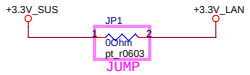


PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***LAN BCM5906MKMLG(QFN-68)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Ivan_Chou***
		SHEET **47** OF **68**		RELEASE DATE :	

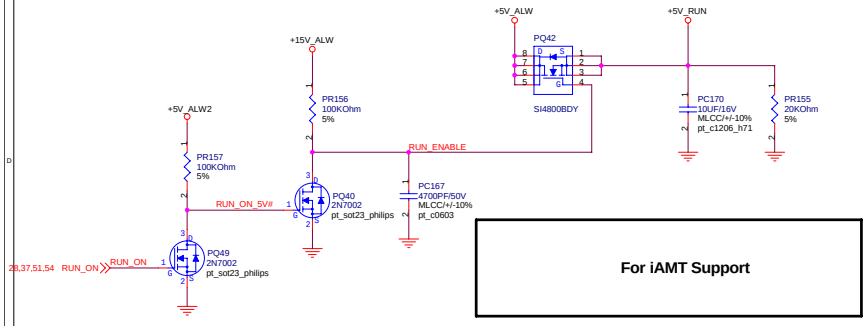


+3.3V_LAN Source Guideline:

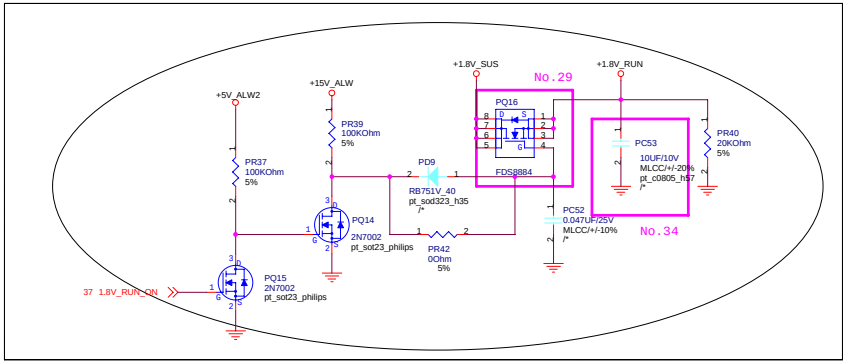
1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V_SRC if Wake-on_LAN is required out of S4, S5

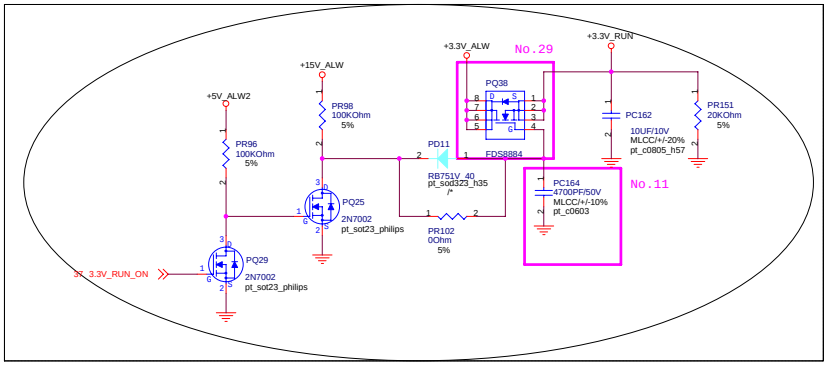


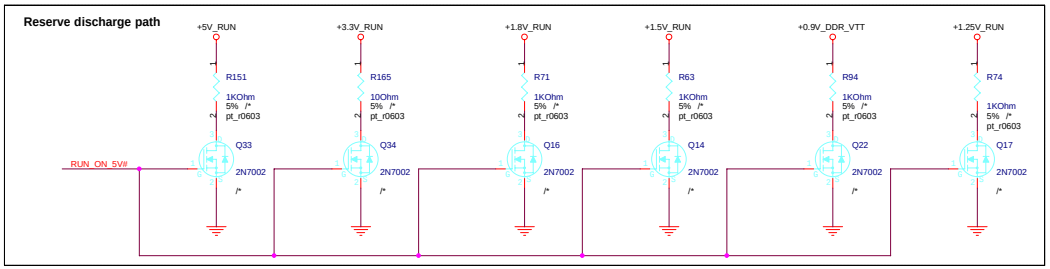
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***Magnetics and RJ-45***	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER : ***Ivan_Chou***
		SHEET 48 OF 68		RELEASE DATE :		

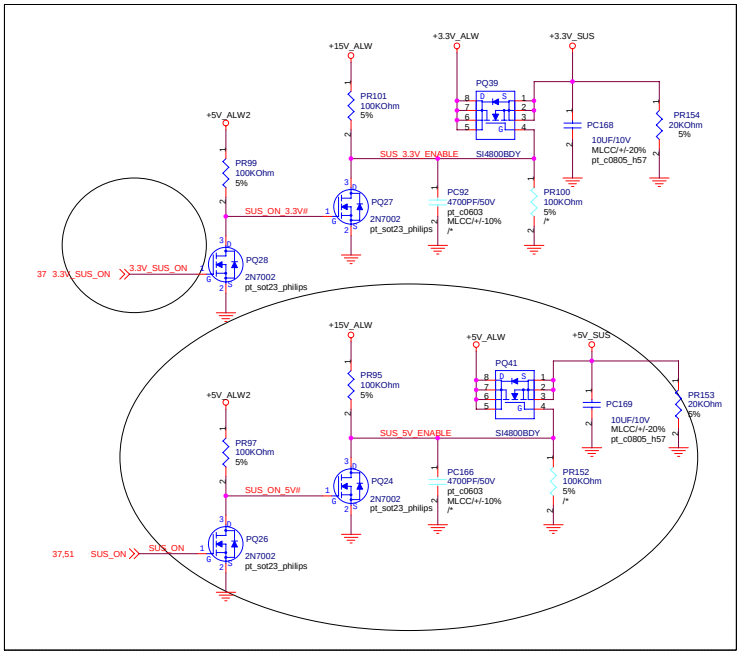


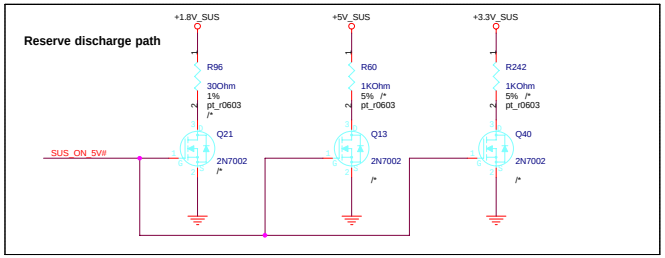
For iAMT Support







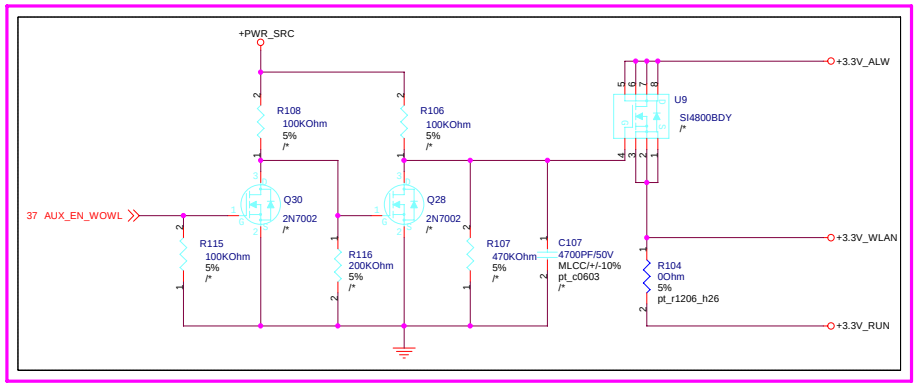


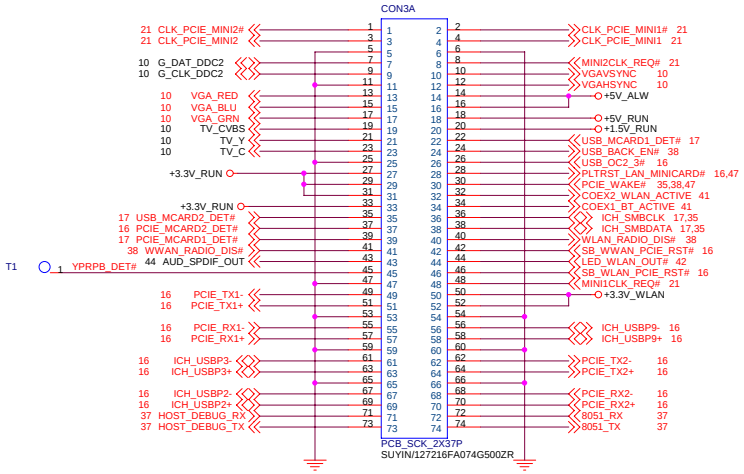


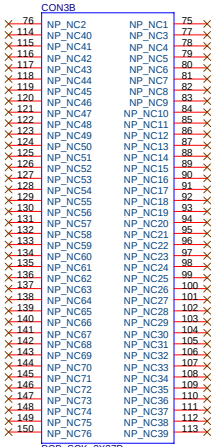
For iAMT Support

PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: ***Power Control Switch***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Eric Ko***
		SHEET 49 OF 68		RELEASE DATE :	

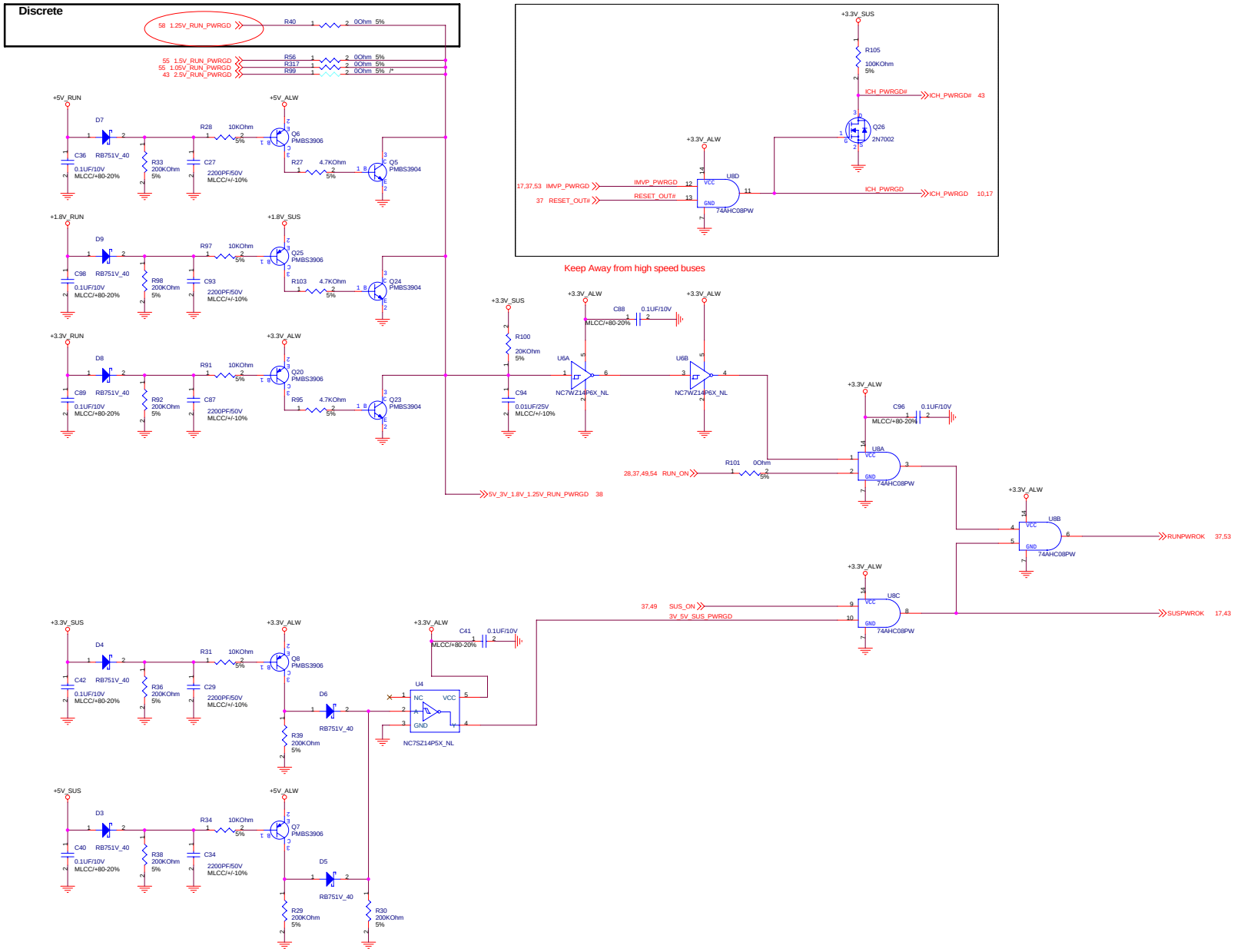
No.21





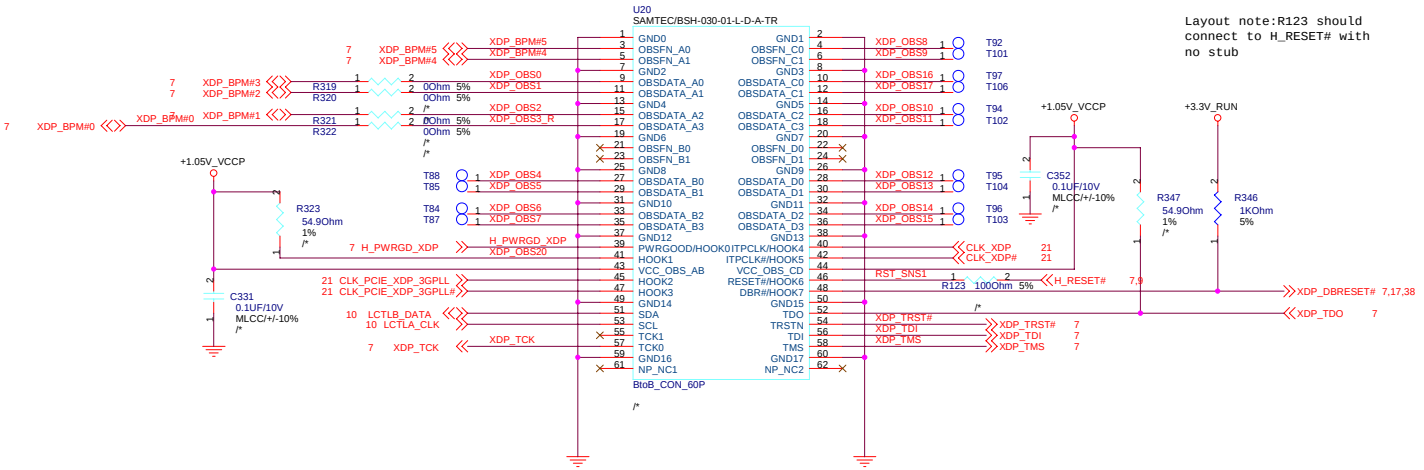


PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***BtoB CON***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***STANLY_HSU***
		SHEET **50** OF **68**		RELEASE DATE :	

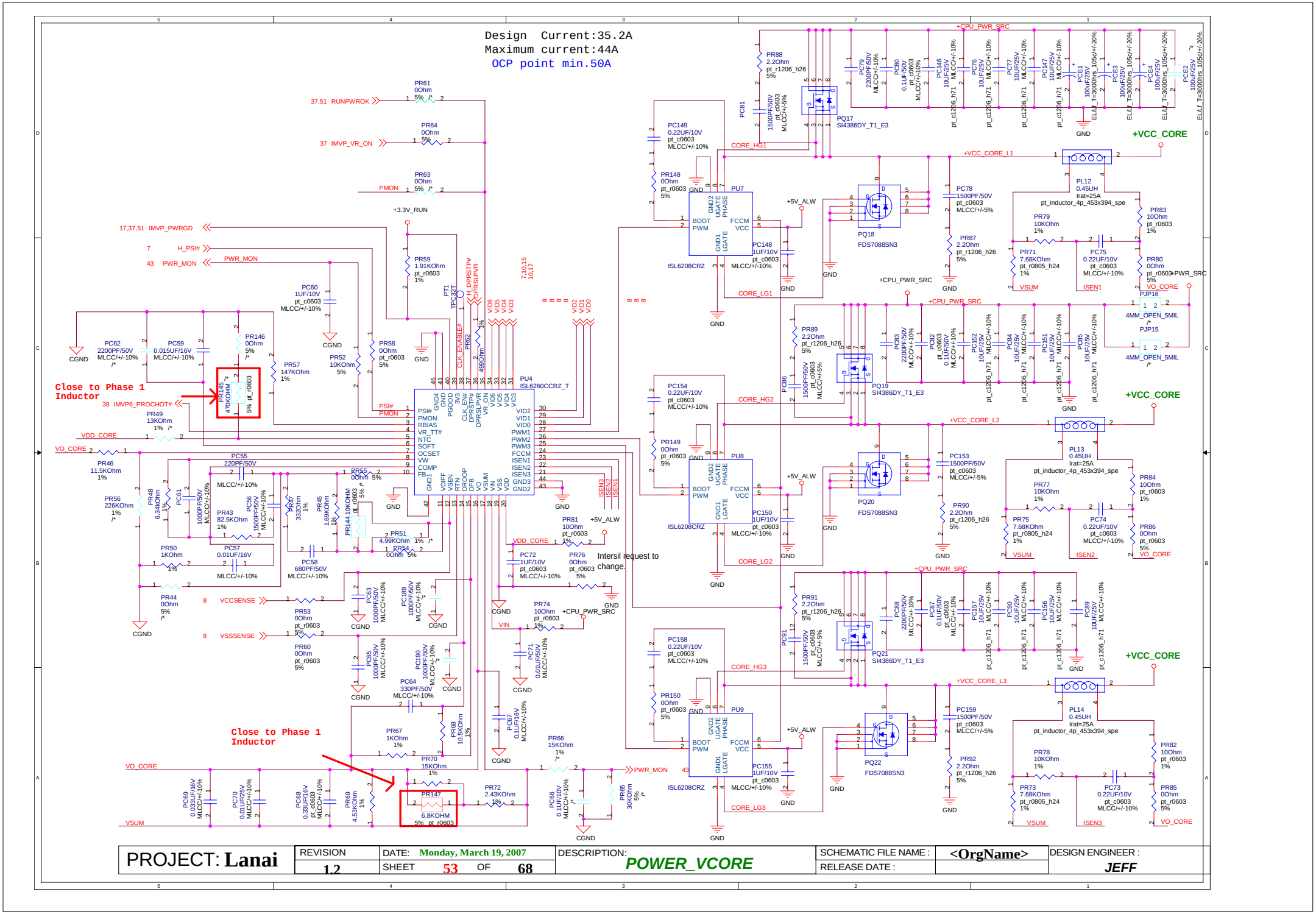


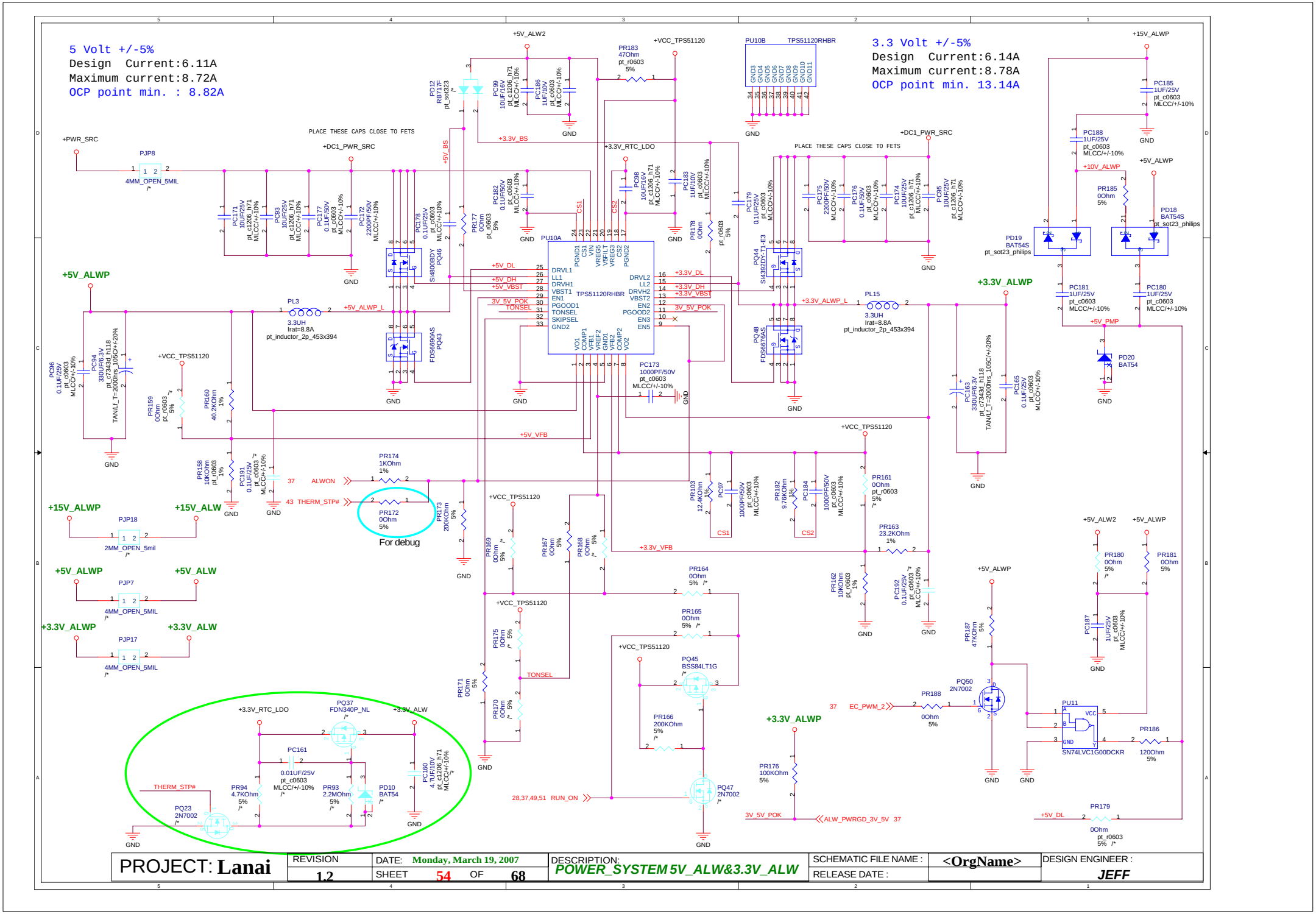
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Power Sequence Logic	SCHEMATIC FILE NAME :	DESIGN ENGINEER : C.L. Ho
		SHEET 51 OF 68		RELEASE DATE :	

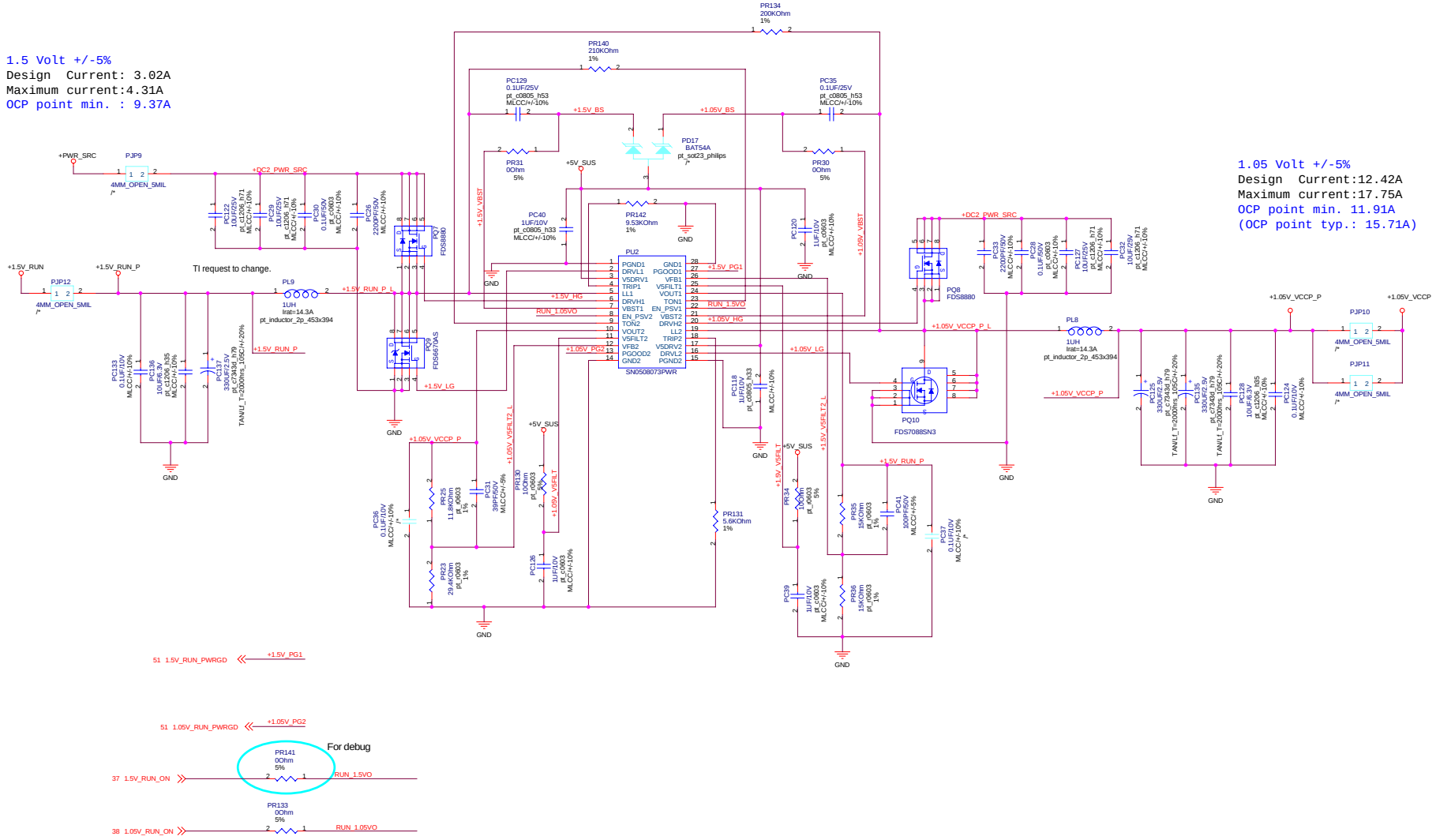
XDP



PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***XDP***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
	SHEET **52** OF **68**			RELEASE DATE :		***Terry_Lin***


Design Current:35.2A
Maximum current:44A
OCP point min.50A
Close to Phase 1 Inductor
Close to Phase 1 Inductor
Intersil request to change.
+VCC_CORE
+CPU_PWR_SRC
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 53 OF 68
DESCRIPTION: POWER_VCORE
SCHEMATIC FILE NAME :
RELEASE DATE :
<OrgName>
DESIGN ENGINEER : JEFF


5 Volt +/-5%
Design Current:6.11A
Maximum current:8.72A
OCP point min. : 8.82A
3.3 Volt +/-5%
Design Current:6.14A
Maximum current:8.78A
OCP point min. 13.14A
PLACE THESE CAPS CLOSE TO FETS
TPS51120RHBR
For debug
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 54 OF 68
DESCRIPTION: POWER_SYSTEM 5V_ALW&3.3V_ALW
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : JEFF



PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 55 OF 68	***POWER I/O 1.5VS & 1.05VS***	RELEASE DATE :		***JEFF***

TOTAL POWER=65W
-->3.34A

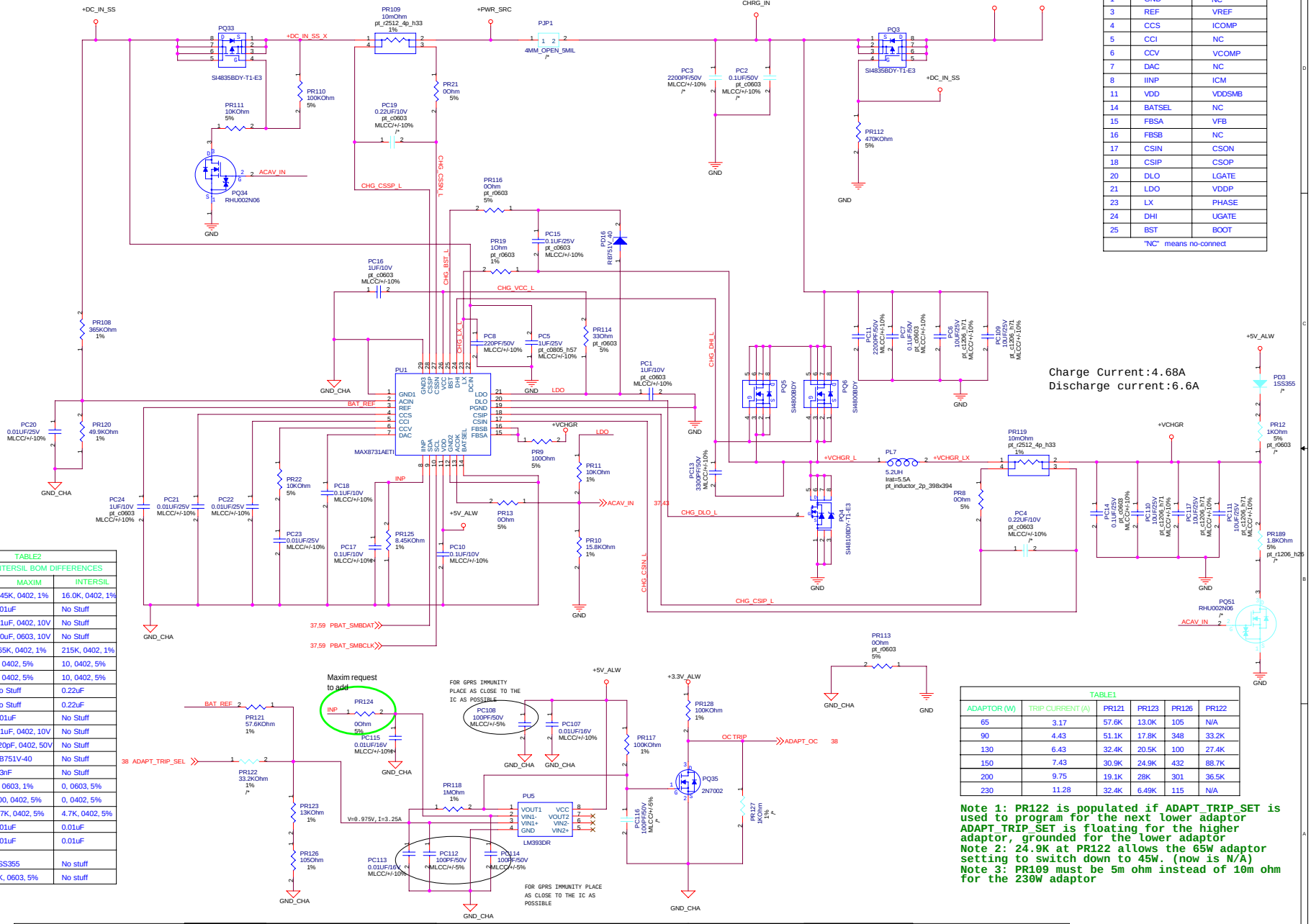


TABLE3		
PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT
"NC" means no-connect		

TABLE2		
MAXIM & INTERSIL BOM DIFFERENCES		
REF DES	MAXIM	INTERSIL
PR125	8.45K, 0402, 1%	16.0K, 0402, 1%
PC115	0.01uF	No Stuff
PC17	0.1uF, 0402, 10V	No Stuff
PC24	1.0uF, 0603, 10V	No Stuff
PR108	365K, 0402, 1%	215K, 0402, 1%
PR8	0, 0402, 5%	10, 0402, 5%
PR21	0, 0402, 5%	10, 0402, 5%
PC4	No Stuff	0.22uF
PC19	No Stuff	0.22uF
PC22	0.01uF	No Stuff
PC18	0.1uF, 0402, 10V	No Stuff
PC8	220pF, 0402, 50V	No Stuff
PD16	RB751V-40	No Stuff
PC13	3.3nF	No Stuff
PR19	1, 0603, 1%	0, 0603, 5%
PR9	100, 0402, 5%	0, 0402, 5%
PR22	4.7K, 0402, 5%	4.7K, 0402, 5%
PC23	0.01uF	0.01uF
PC21	0.01uF	0.01uF
PD3	1SS355	No stuff
PR12	1K, 0603, 5%	No stuff

TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR121	PR123	PR126	PR122
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

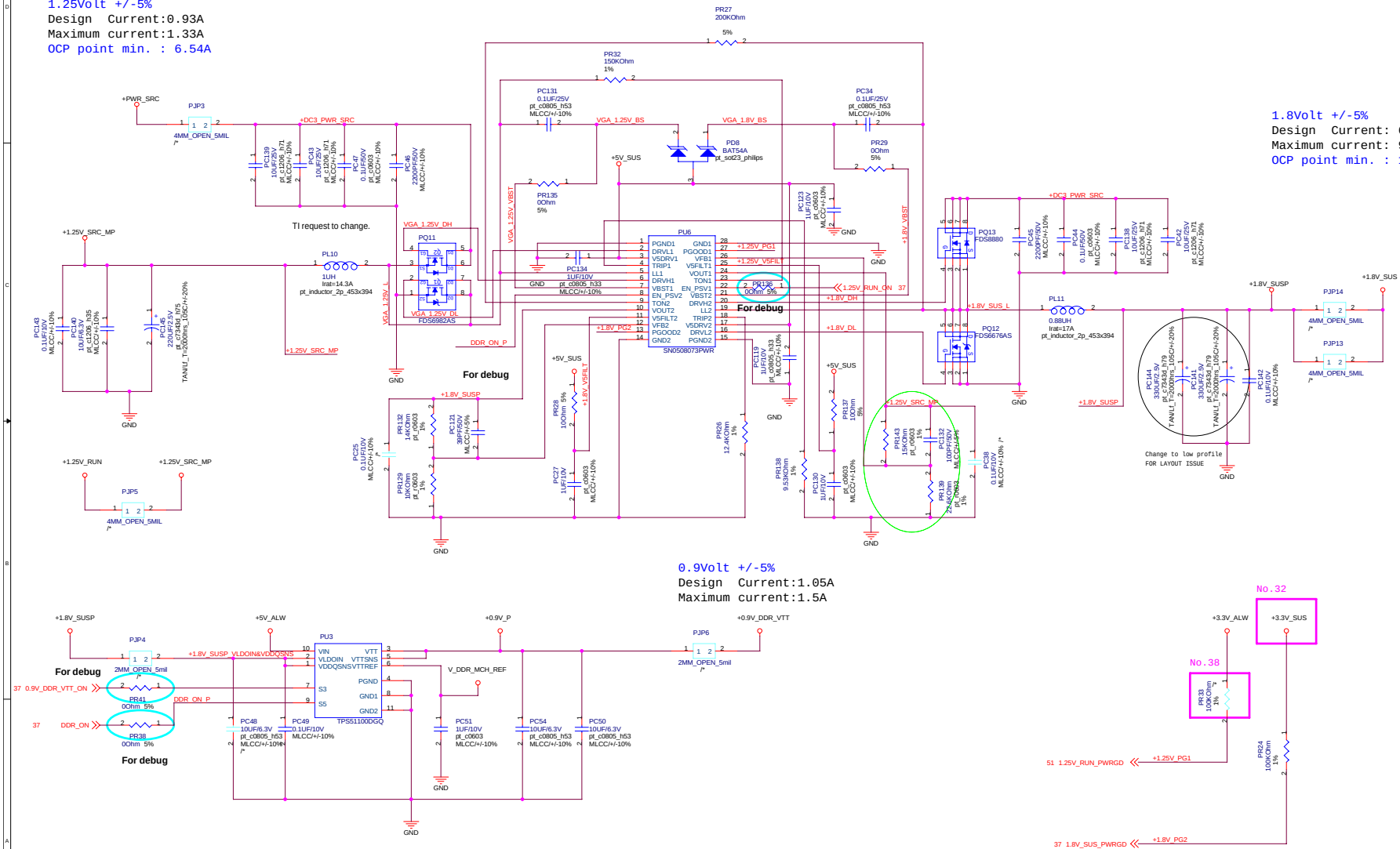
Note 1: PR122 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor
Note 2: 24.9K at PR122 allows the 65W adaptor setting to switch down to 45W. (now is N/A)
Note 3: PR109 must be 5m ohm instead of 10m ohm for the 230W adaptor

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: POWER_CHARGER	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : JEFF
		SHEET 57 OF 68		RELEASE DATE :	

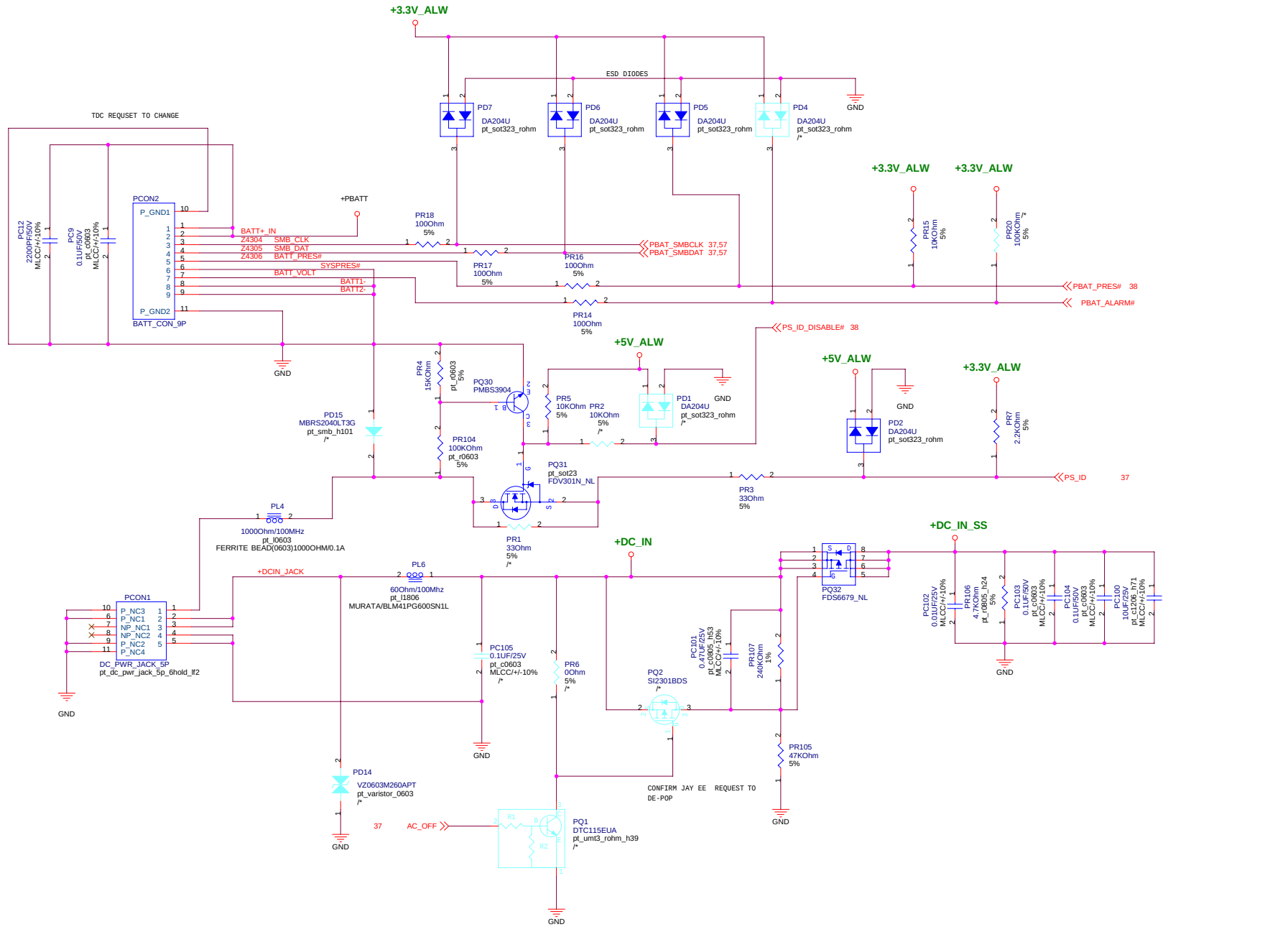
1.25Volt +/-5%
Design Current:0.93A
Maximum current:1.33A
OCP point min. : 6.54A

1.8Volt +/-5%
Design Current: 6.59A
Maximum current: 9.42A
OCP point min. : 16.93A

0.9Volt +/-5%
Design Current:1.05A
Maximum current:1.5A

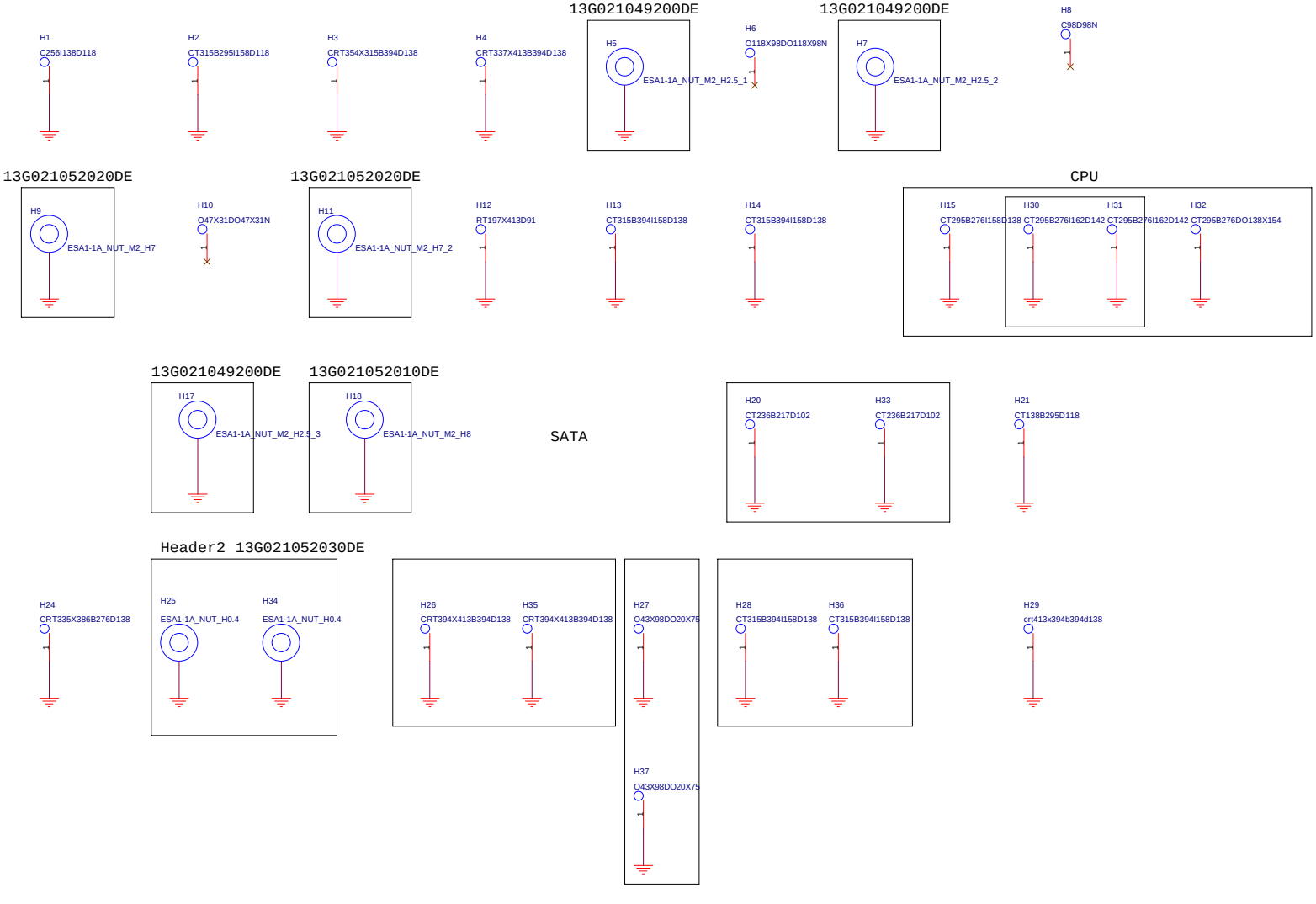


PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *POWER_VGA_1.25V & DDR & VTT*	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER : *Jeff*
		SHEET 58 OF 68		RELEASE DATE :		



PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***POWER_CONNECTOR***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***JEFF***
		SHEET **59** OF **68**		RELEASE DATE :	

GM screw pad

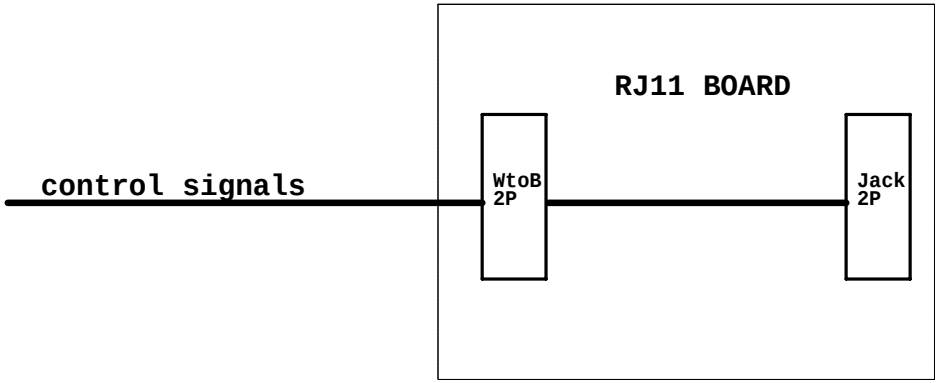


PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***SCREW PAD***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Sean Kuo***
		SHEET **60** OF **68**		RELEASE DATE :	

ASUS CONFIDENTIAL

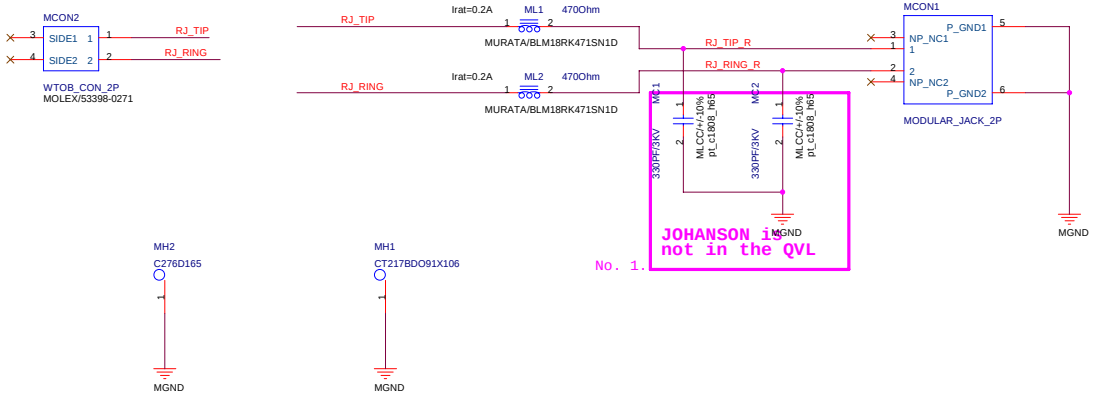
MODEL NAME : *Elsa*

Lanai:Modem Board



REV : 1.1(DELL: X01)

PROJECT: **Lanai**	REVISION: **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***BLOCK DIAGRAM***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Stanly_Hsu***
		SHEET 64 OF 68		RELEASE DATE :	



PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***RJ-11 CONN***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Stanly_Hsu***
		SHEET **65** OF **68**		RELEASE DATE :		

ASUS CONFIDENTIAL

MODEL NAME : ***Elsa***

PCB NO : ***???***

ASUS P/N : ***???***

Lanai PP2 USB Board

REV : 1.1(DELL: X01)

MB PCB

Part Number	Description
DA80004H0L	PCB 00B LA-3071P REV0 M/B

BOM NO. ???
PCB P/N: ???

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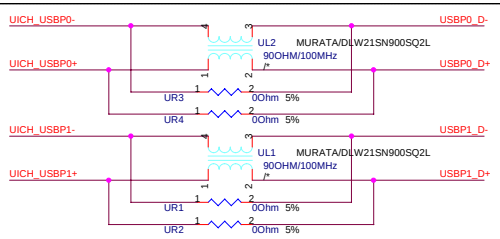
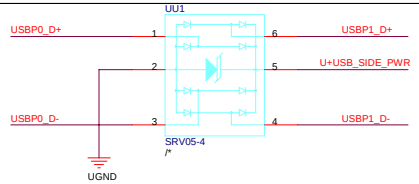
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .

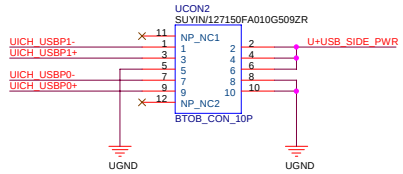


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

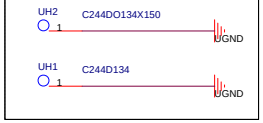


Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C (1pf vs 3pf).

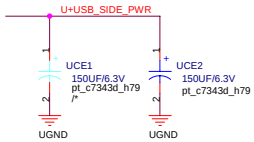
USB daughter board connector



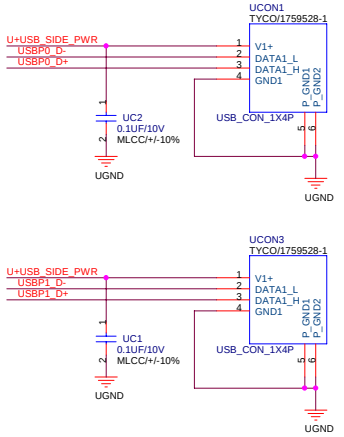
Screw hole



Place one 150uF cap by each USB connector



Each channel is 1A



Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines.
Add PADS ONLY until proven diodes are really needed.

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		SHEET 68 OF 68	USB PORT (SINGLE * 2)	RELEASE DATE :		Terry_Lin