

Compal Confidential

Schematic Document

Cantiga + ICH9

2008 / 12 / 10 Rev:1.0

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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	
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				Document Number	Rev
				LA-4841P	1.0
Date: Monday, December 15, 2008				Sheet	1 of 45

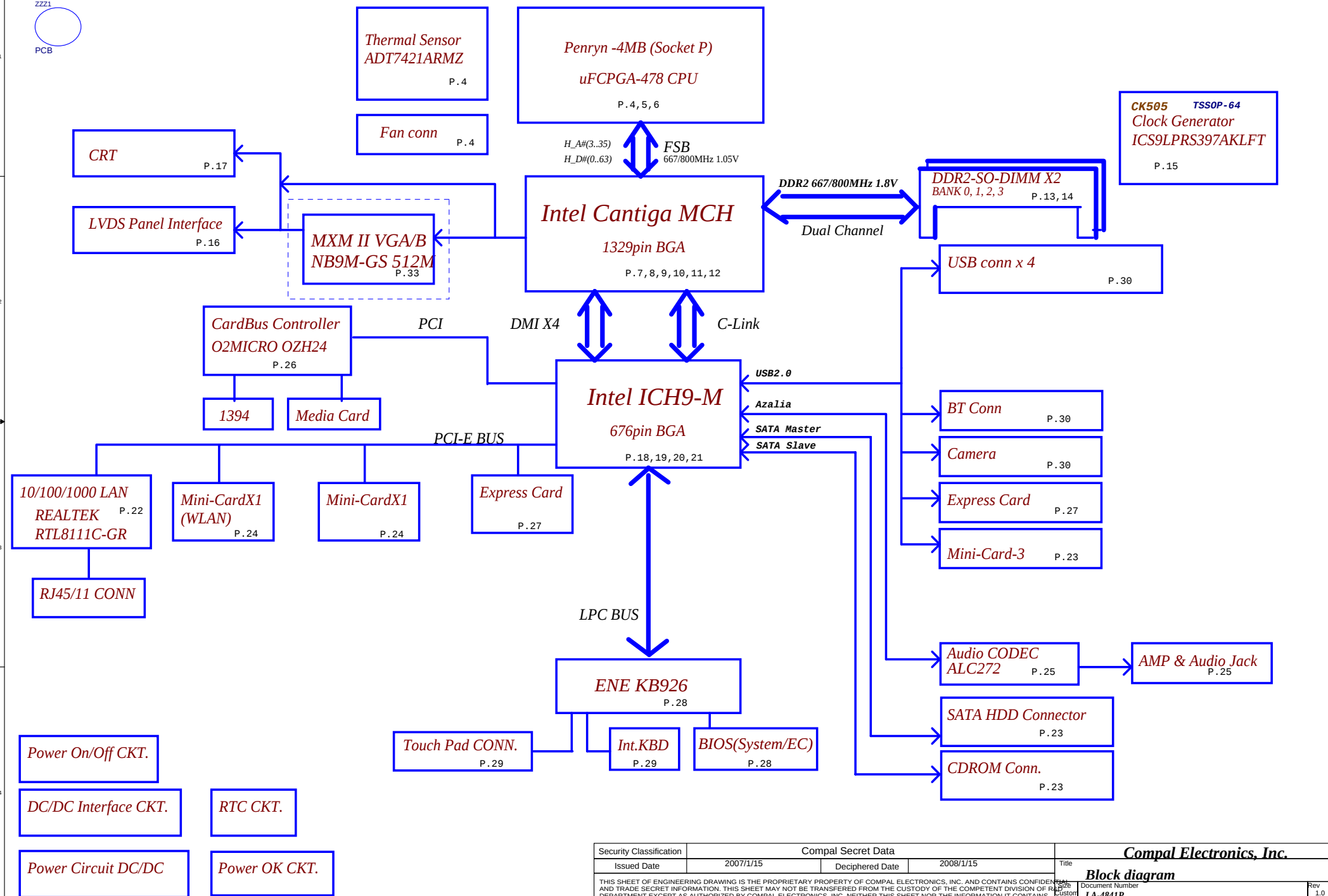
Compal confidential

File Name : LA-4841P

MLK 14

ZZZ1

PCB



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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	Block diagram
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Voltage Rails 0 MEANS ON X MEANS OFF

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +VGA_CORE +2.5VS +1.8VS +1.2VS +0.9VGA
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

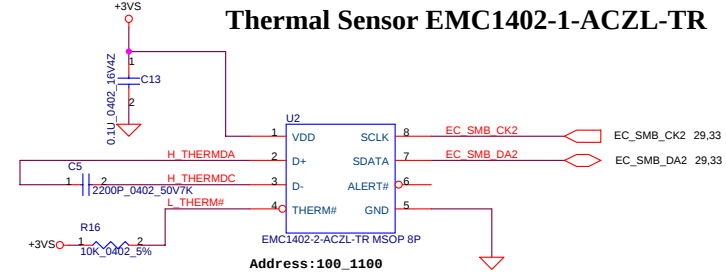
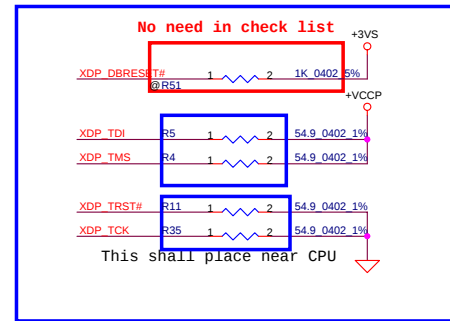
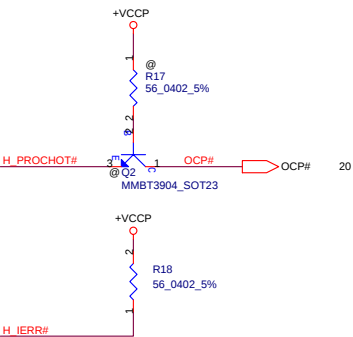
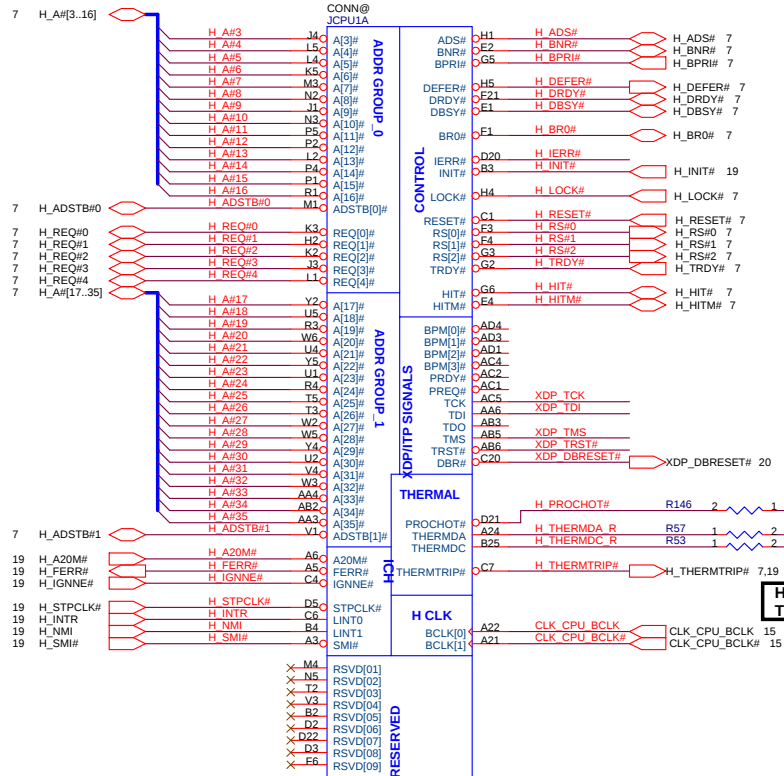
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

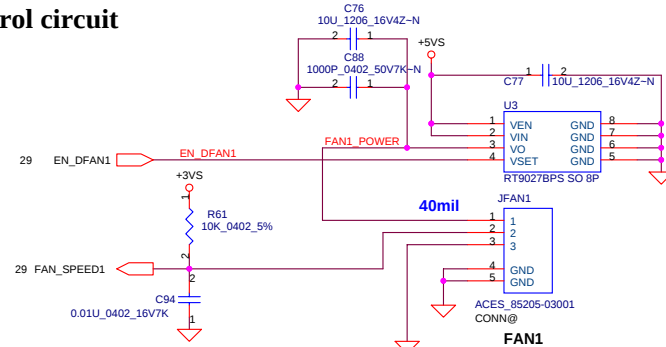
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

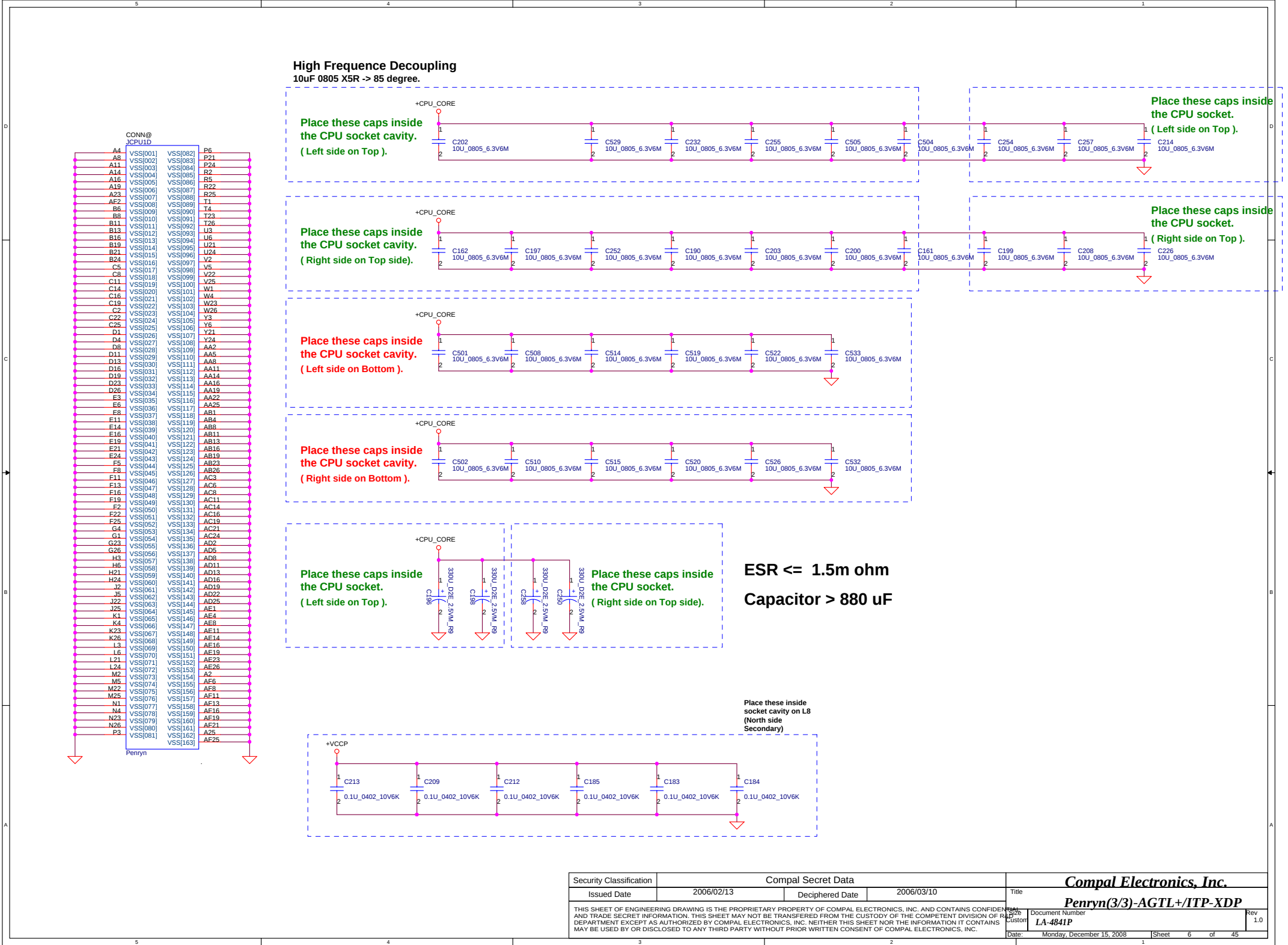
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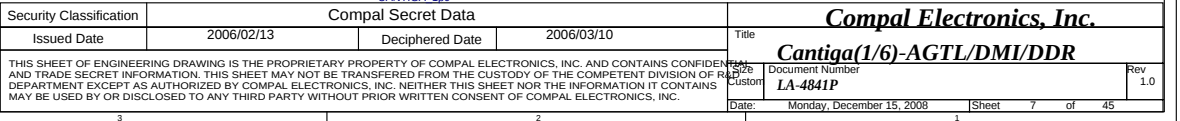


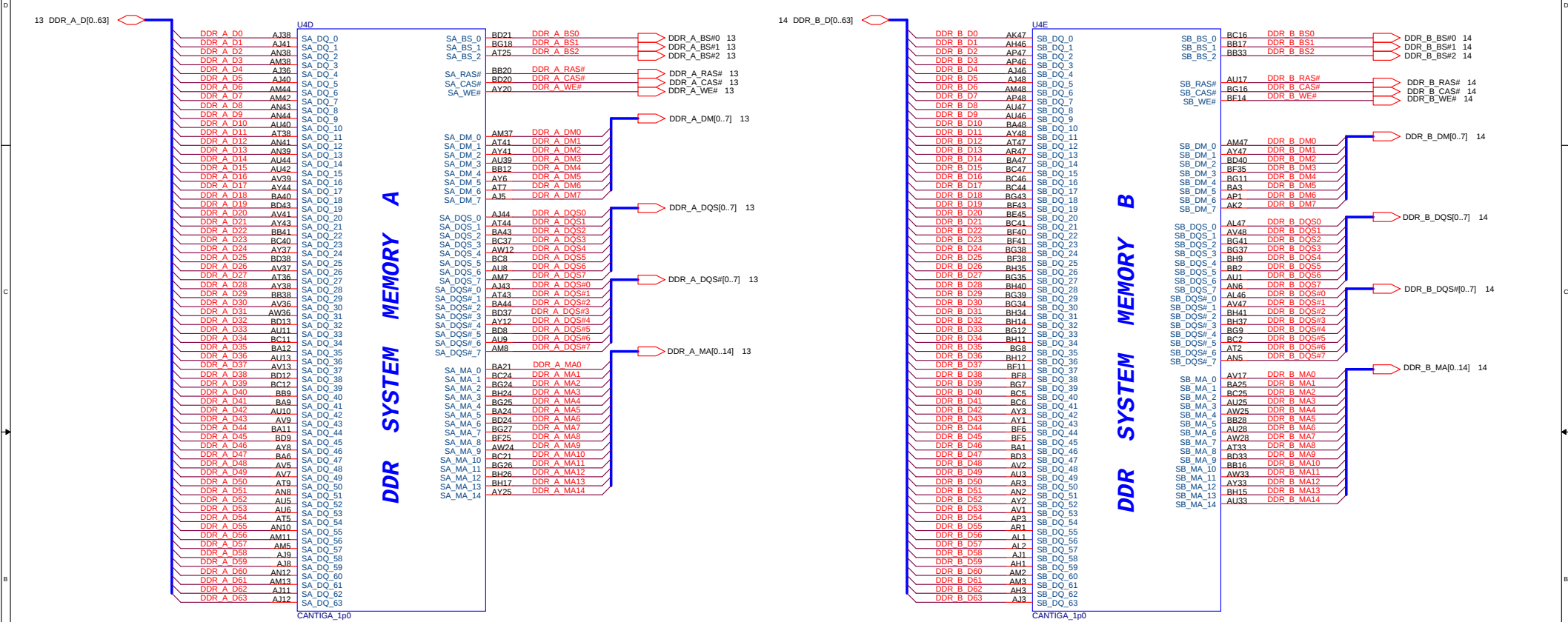
FAN Control circuit

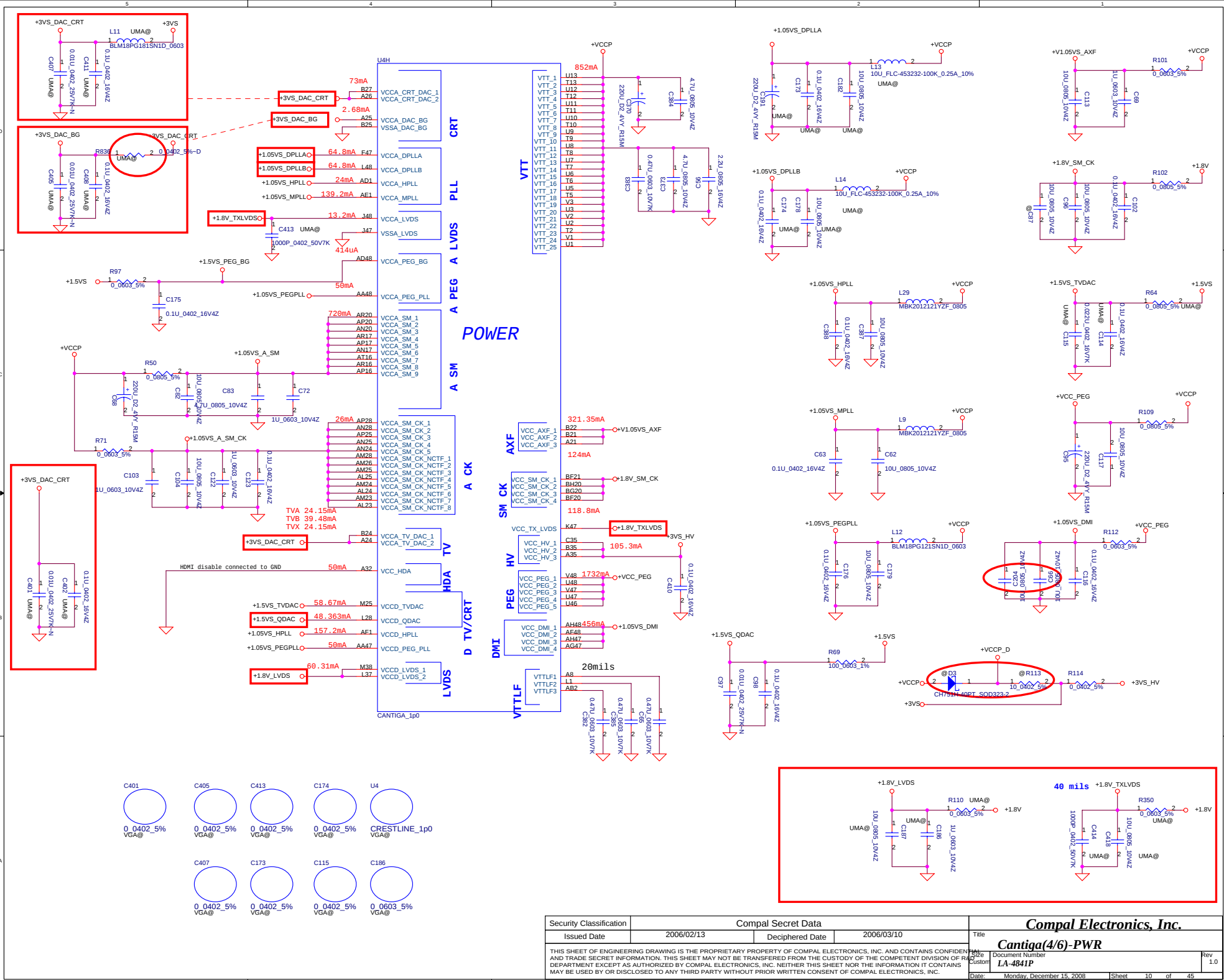


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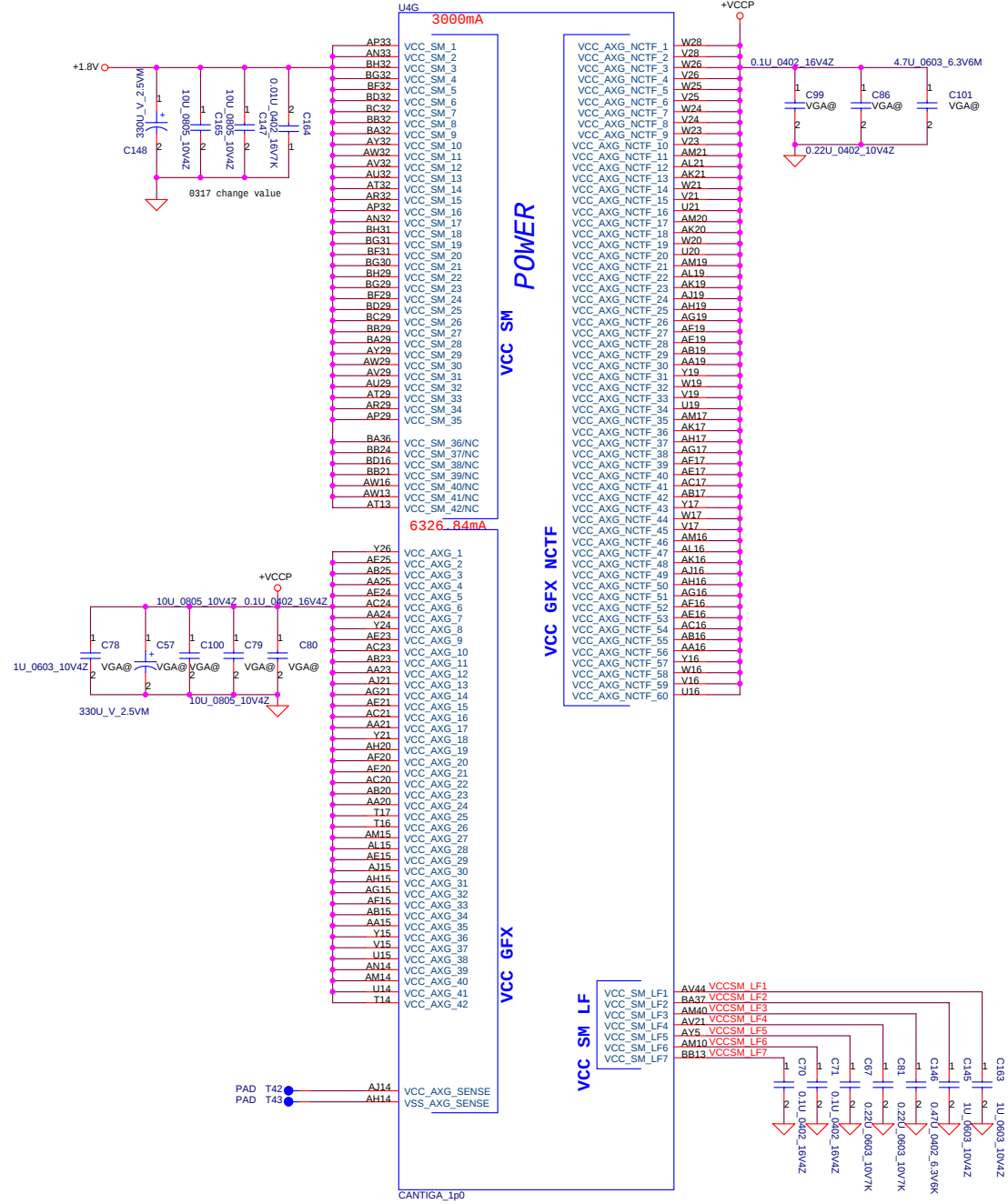
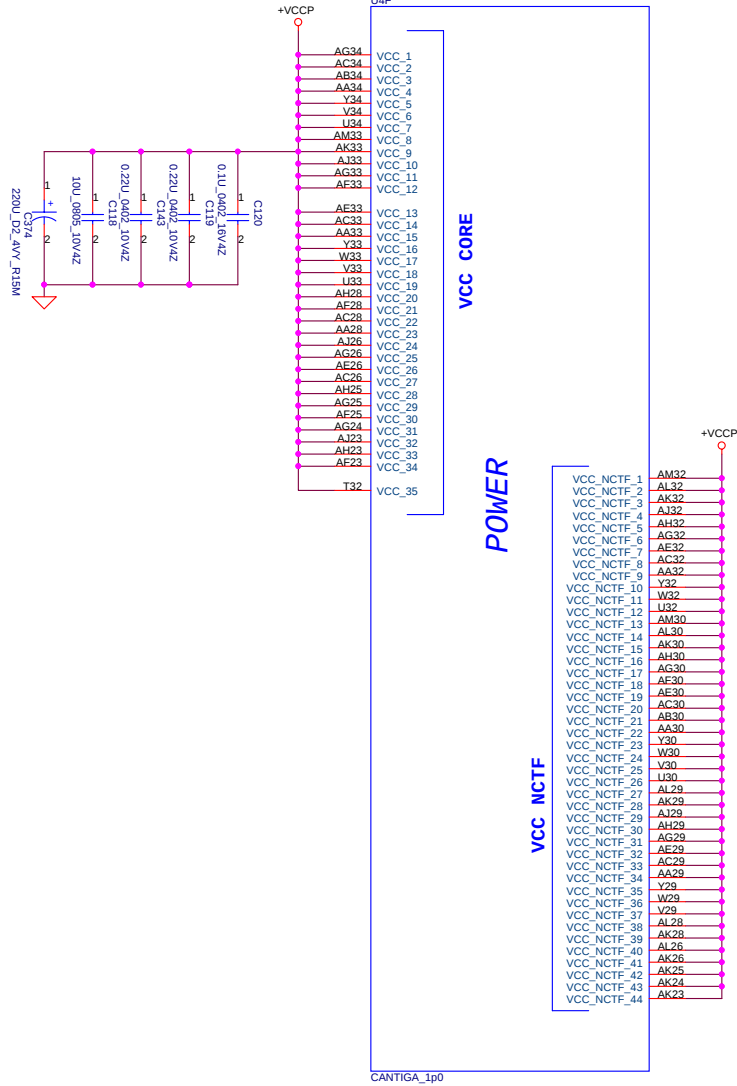




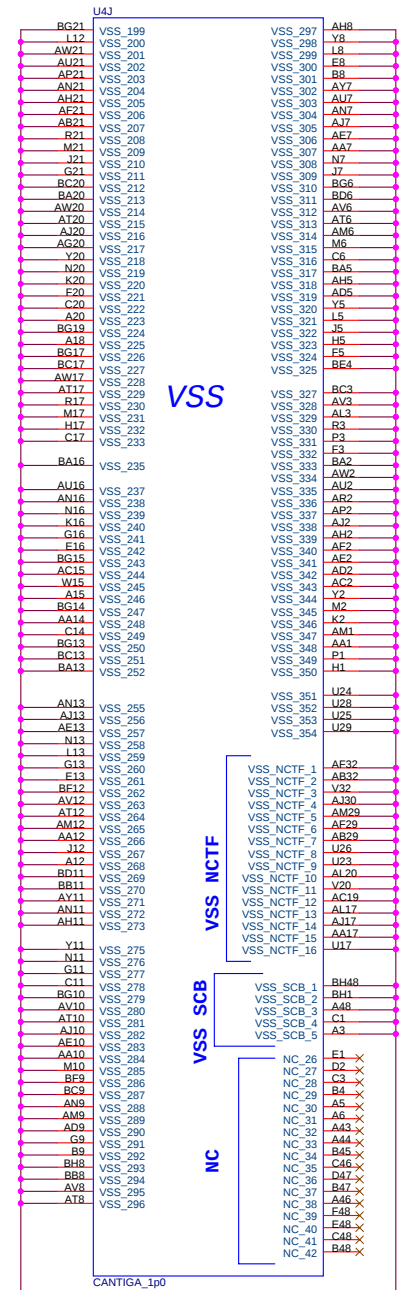
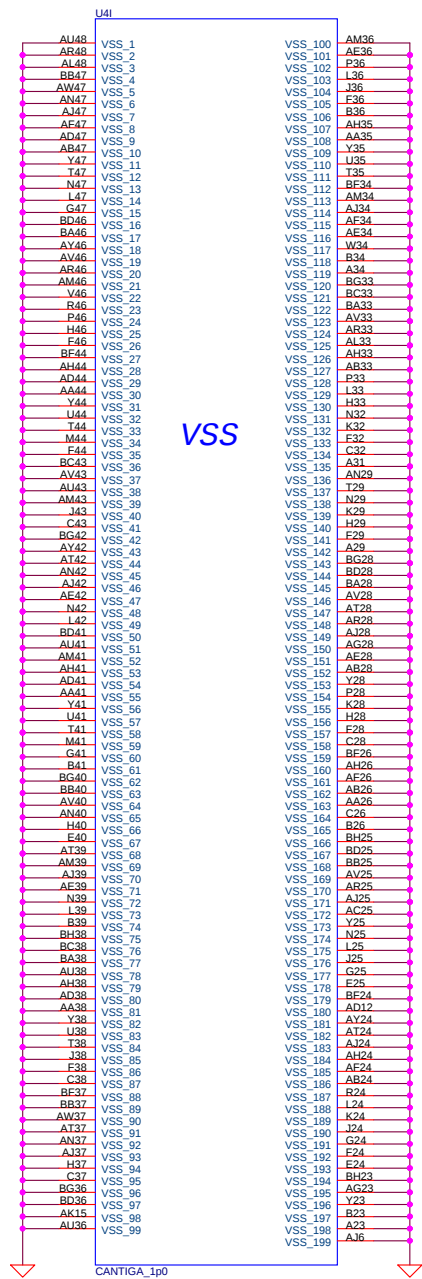


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Extnal Graphic: 1210.34mA
integrated Graphic: 1930.4mA



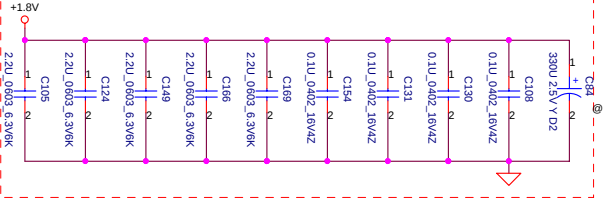
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						Date:		Monday, December 15, 2008	



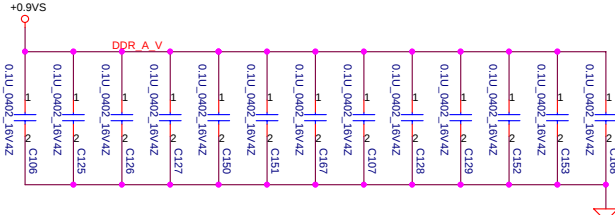
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8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]

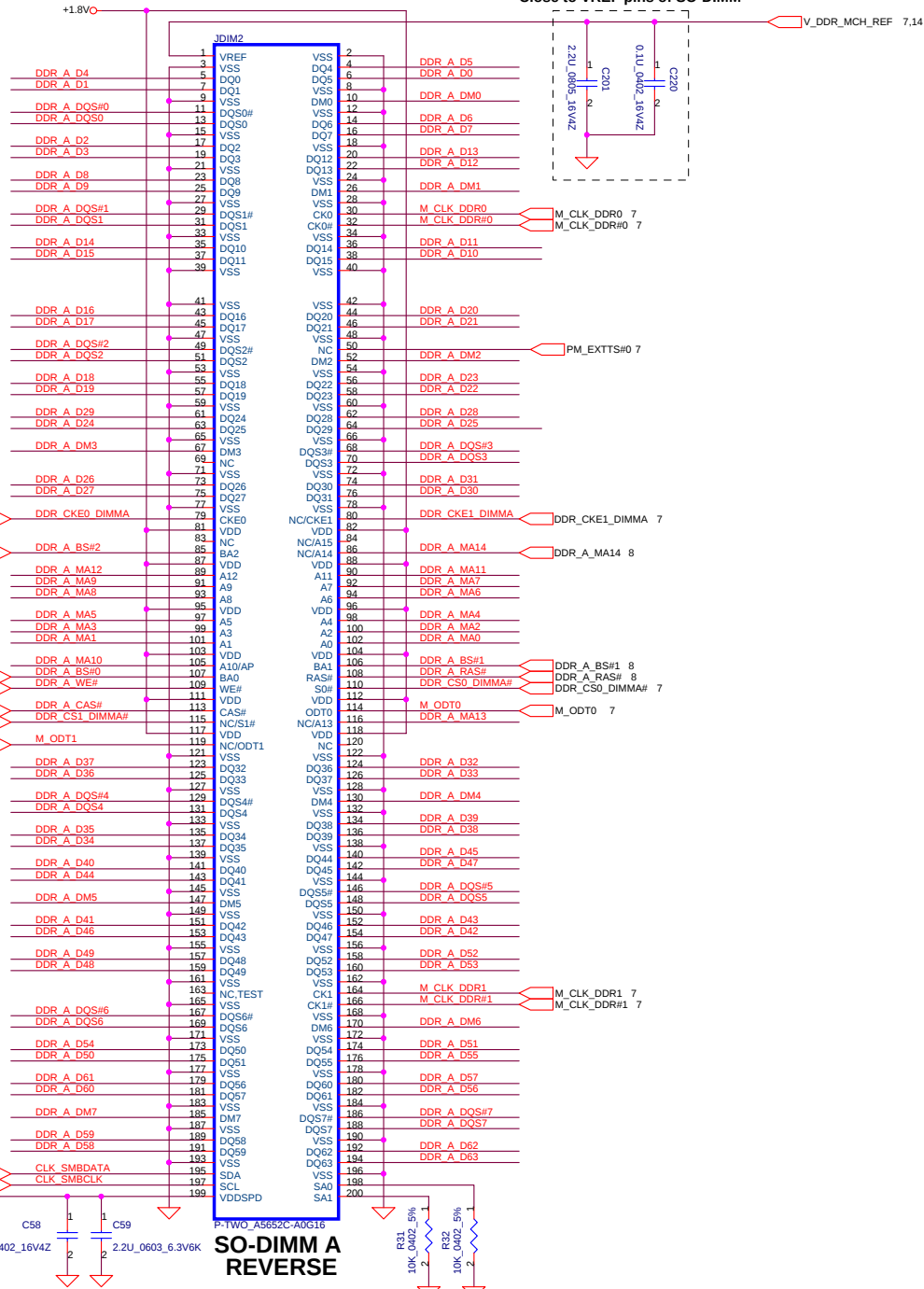
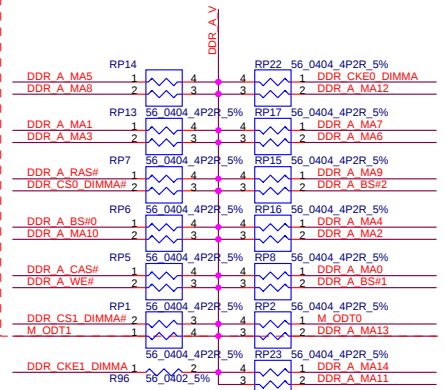
Layout Note:
Place near JDIM1



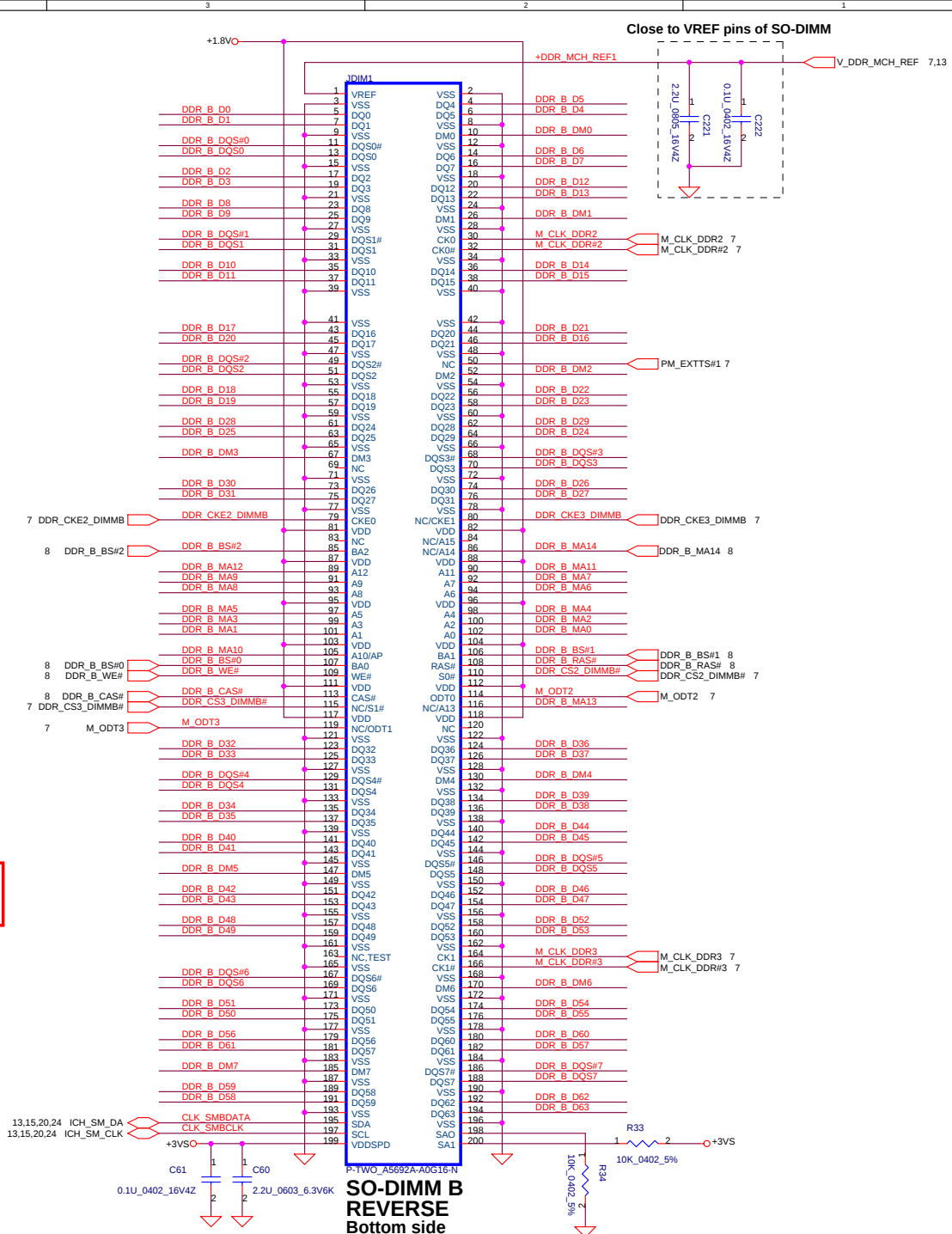
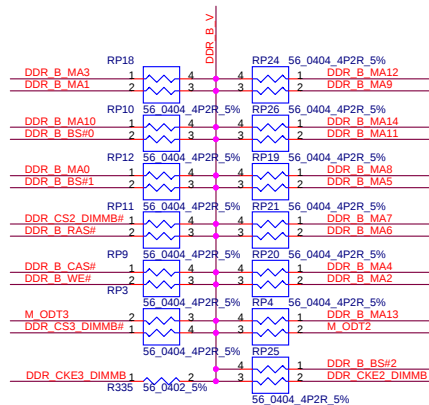
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"

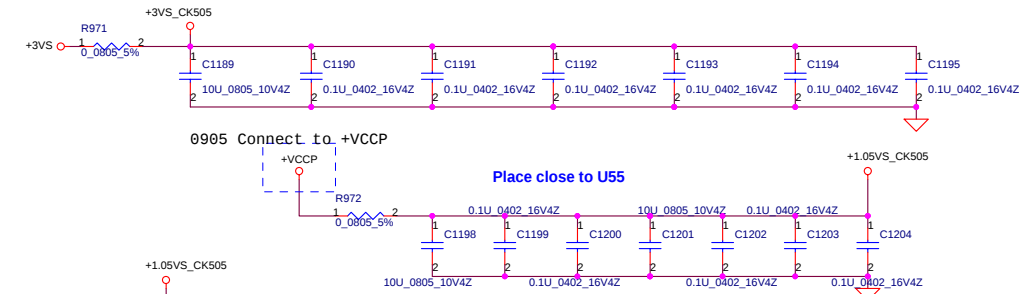
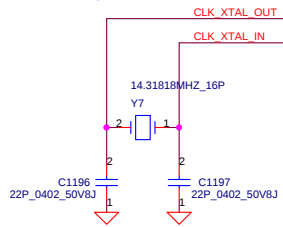


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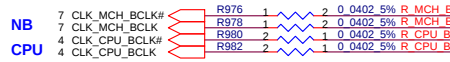


FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ	MHZ	MHZ	MHZ
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

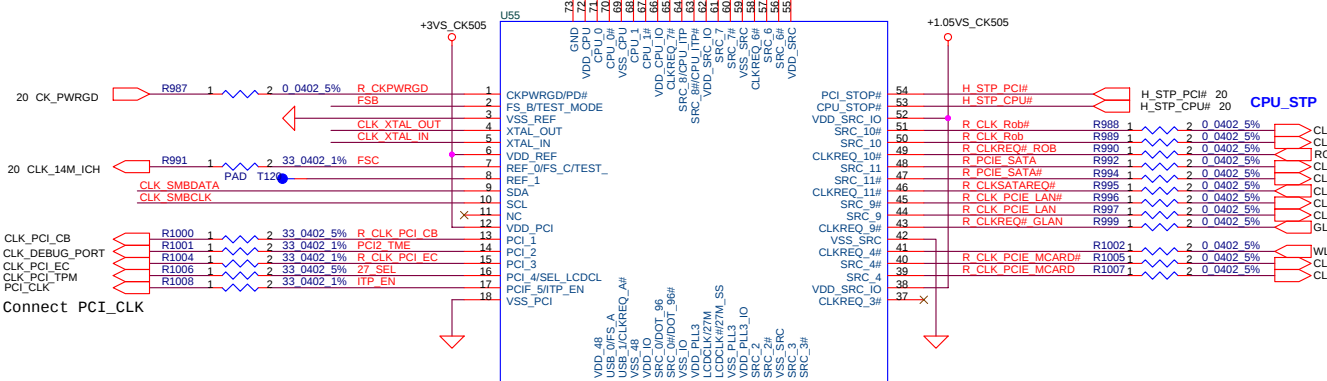
Routing the trace at least 10mil



NB
CPU



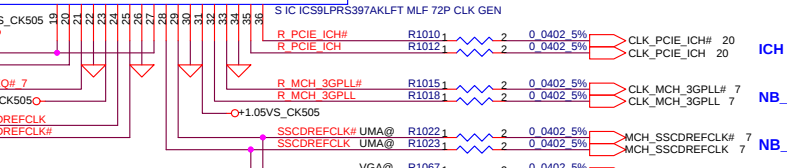
Express Card



0905 Connect PCI_CLK

NB (UMA)

VGA (Discrete)



ICH

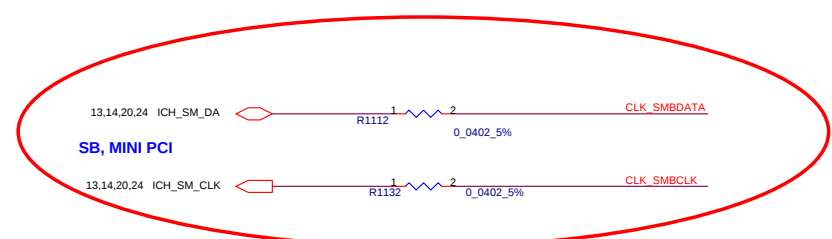
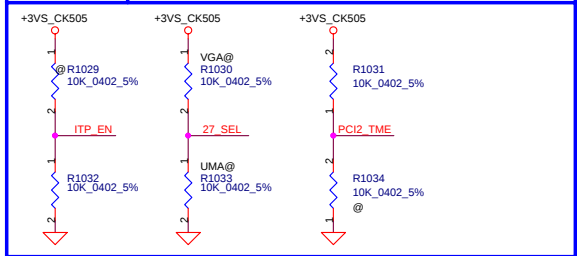
NB_3GPLL

NB_SSC (UMA)

VGA_27M (DIS)

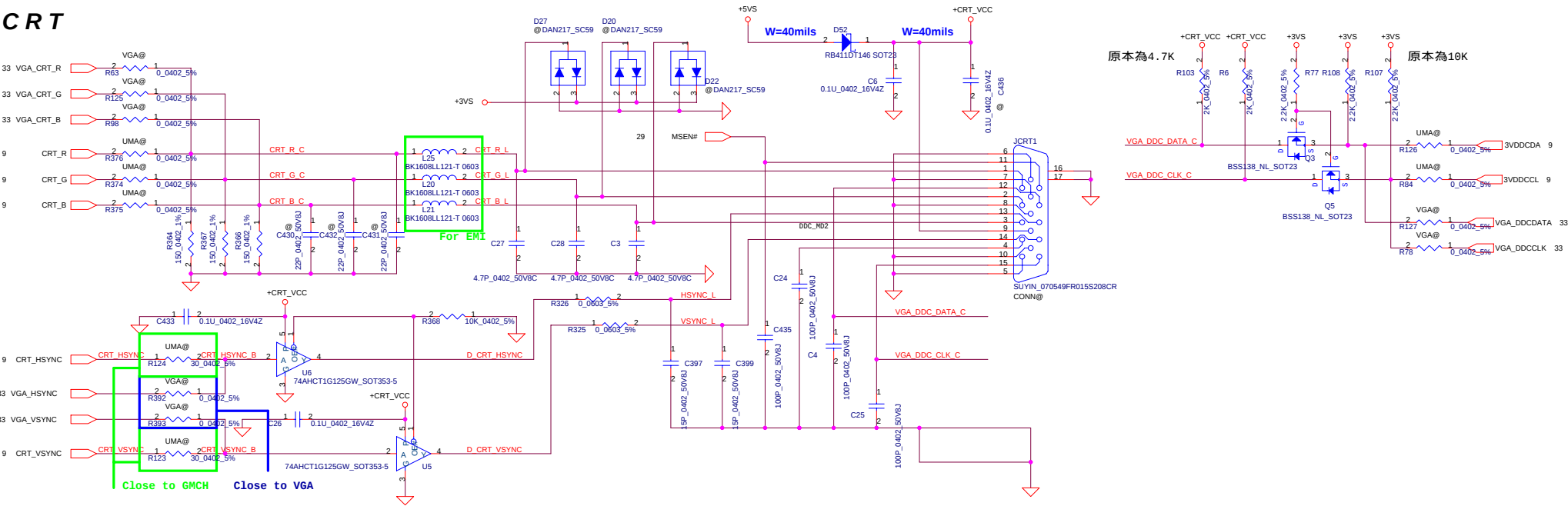
MiniCard_WLAN

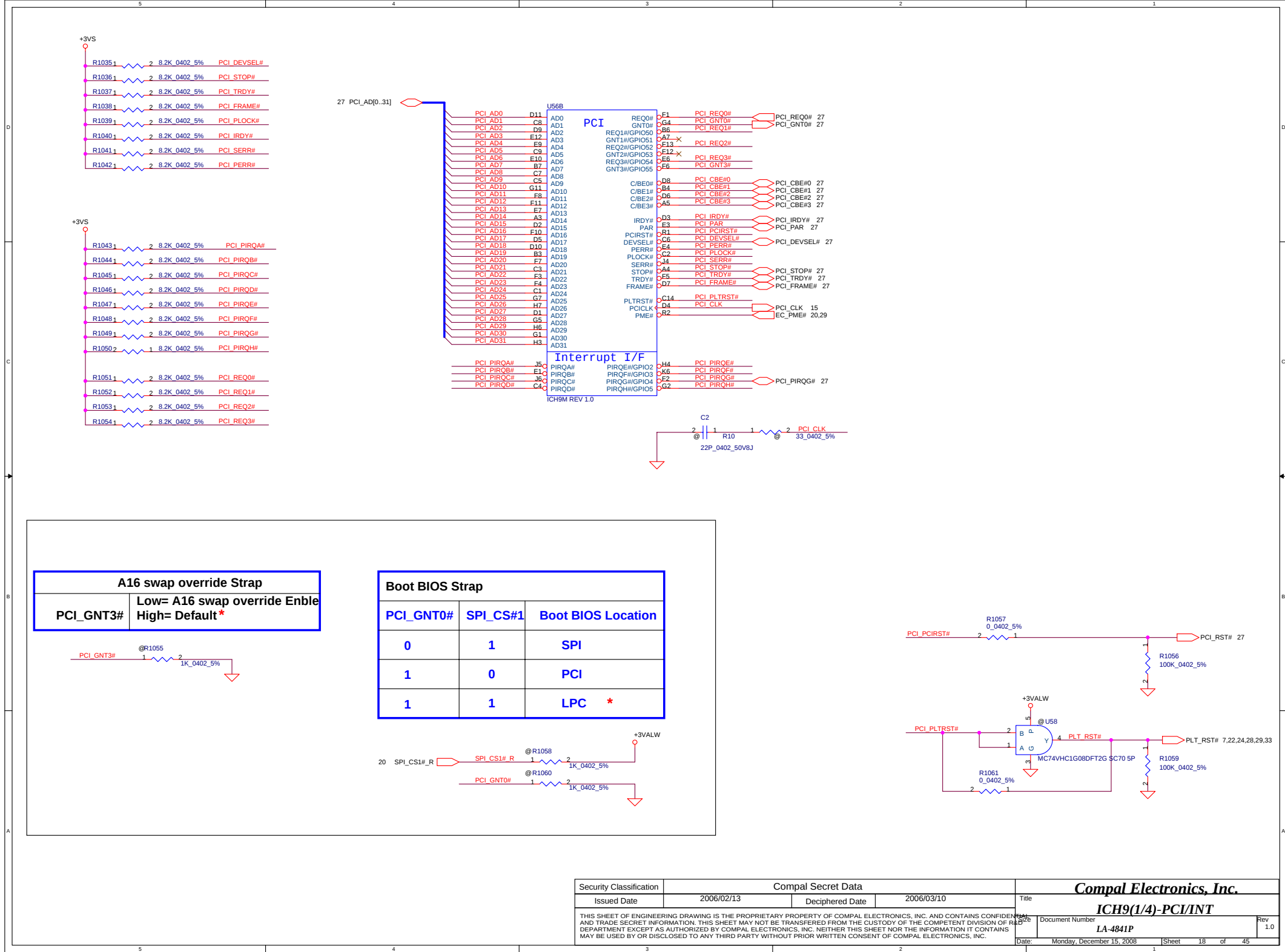
ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
27_SEL	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)
PCI2_TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed

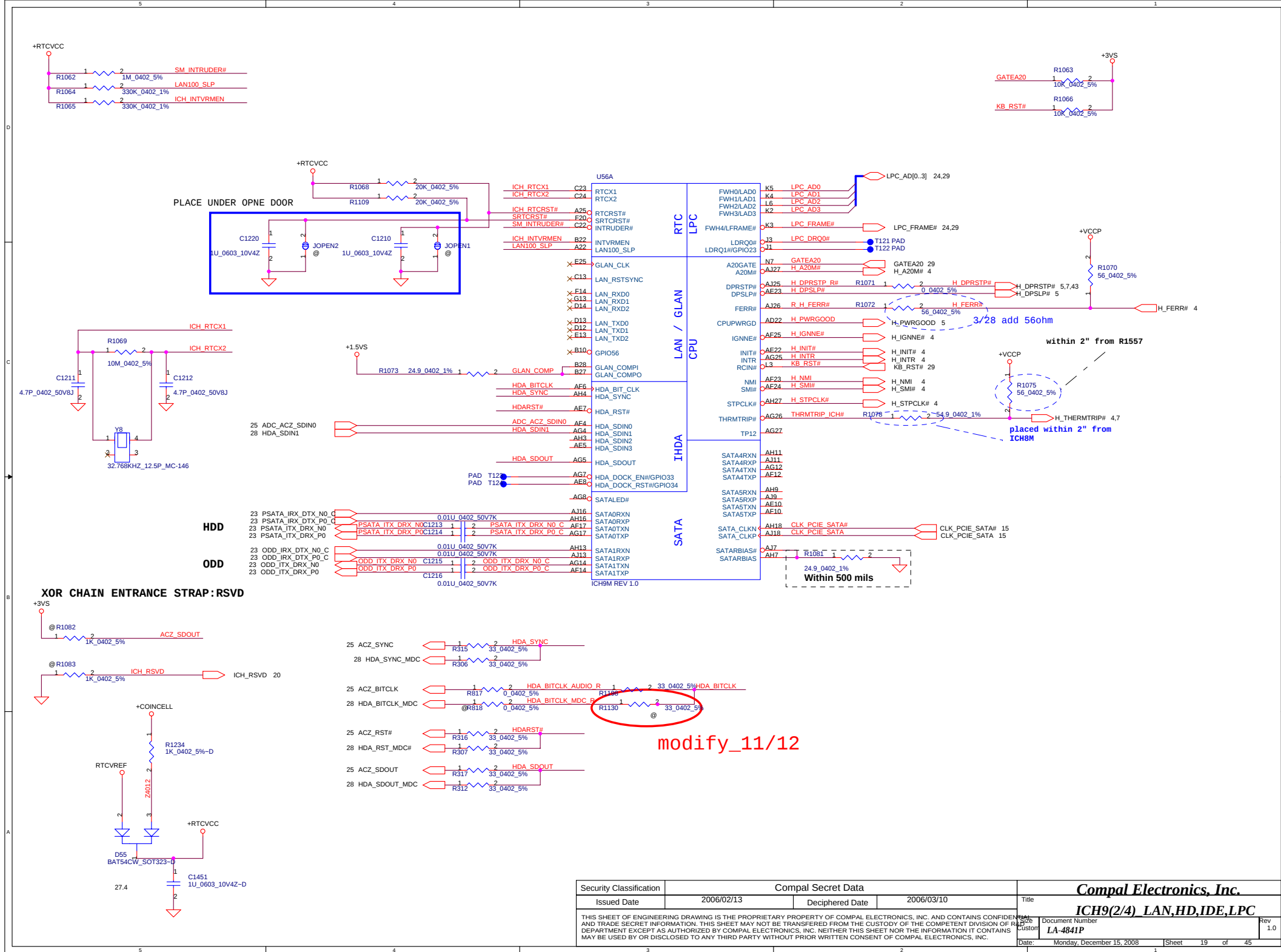


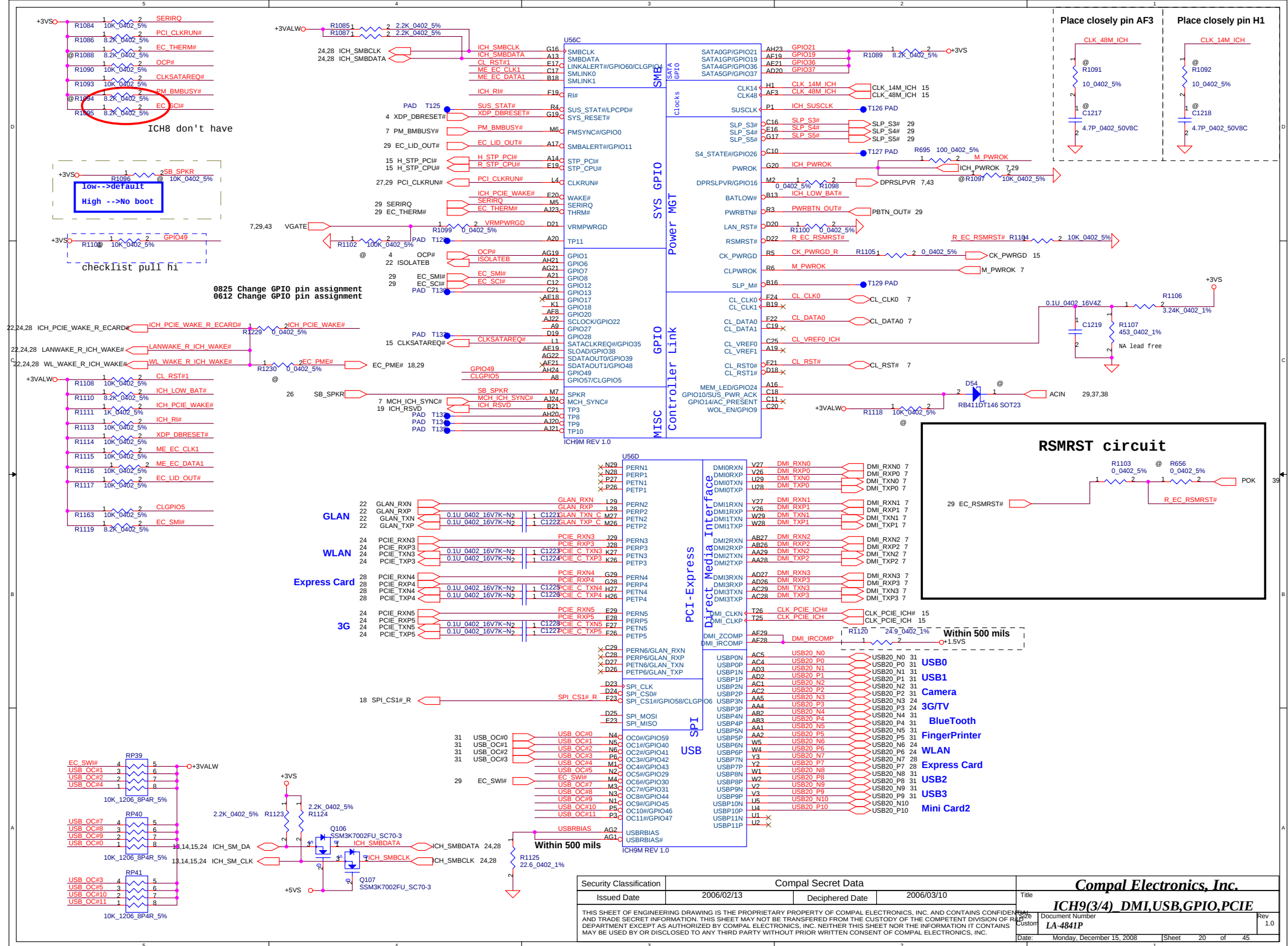
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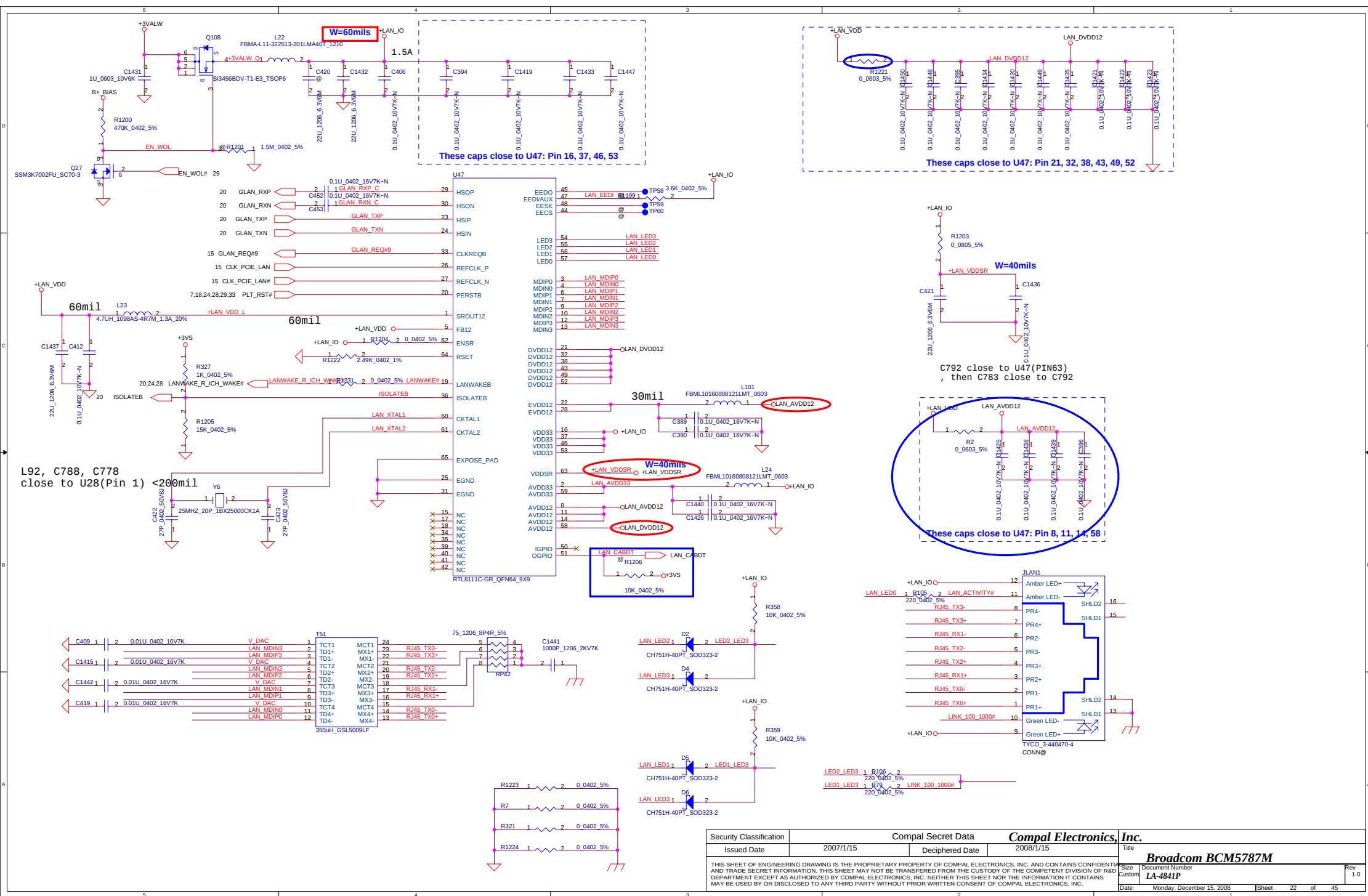
CRT



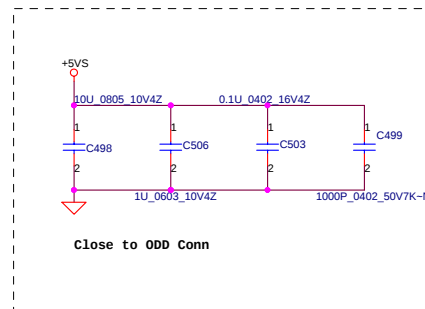
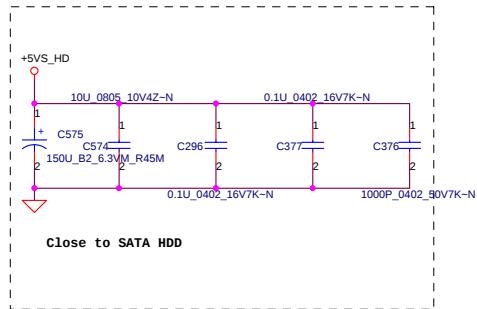
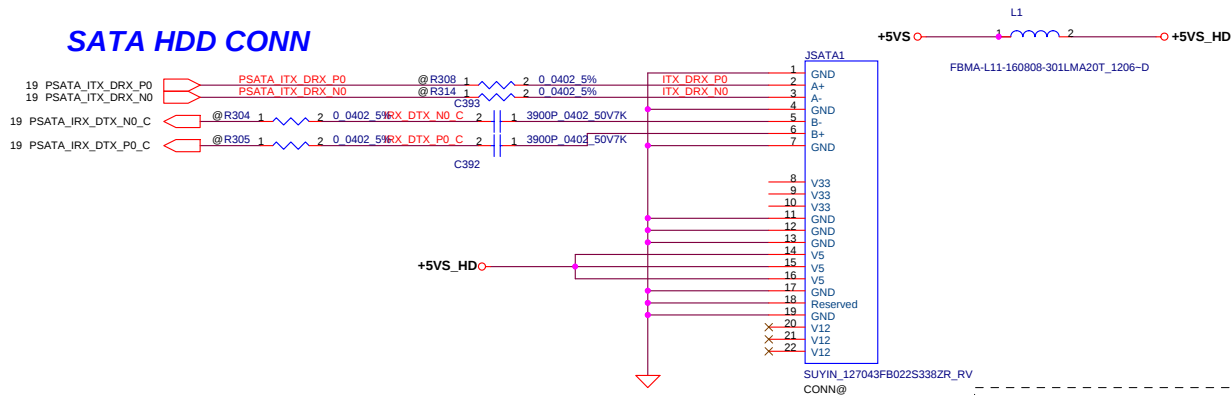




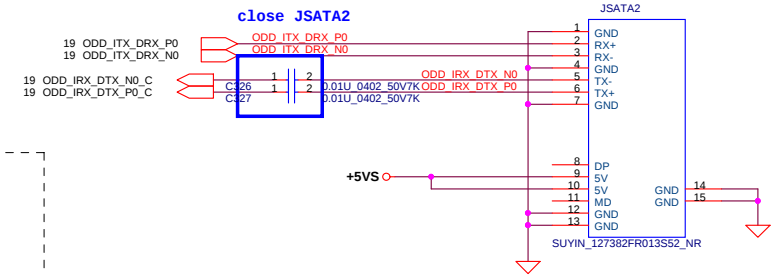




SATA HDD CONN

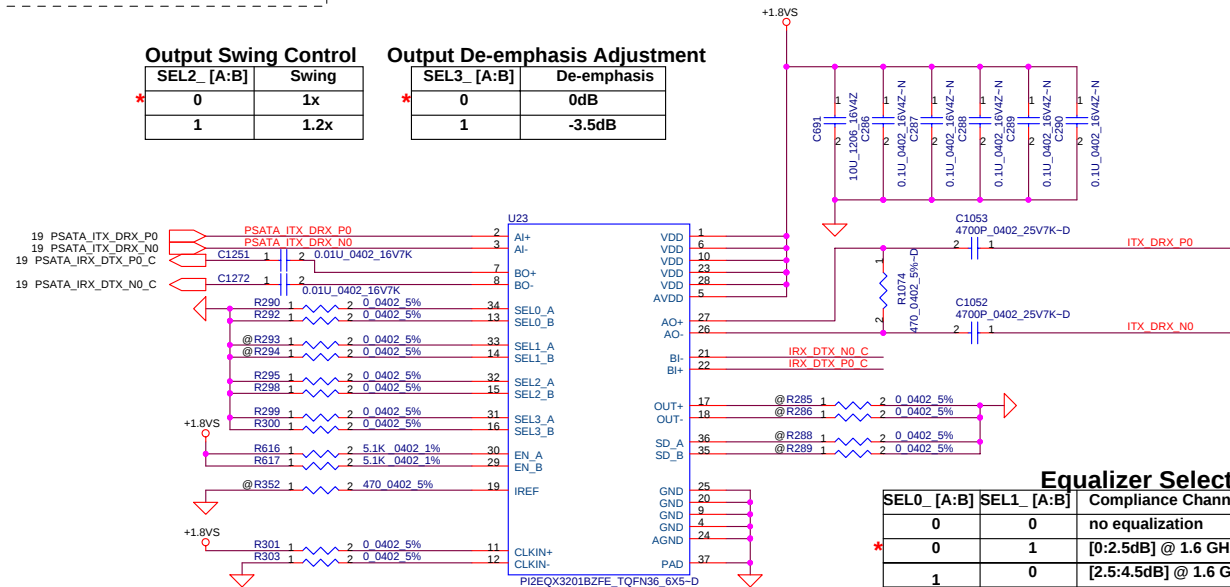


SATA ODD CONN



SEL2_ [A:B]	Swing
0	1x
1	1.2x

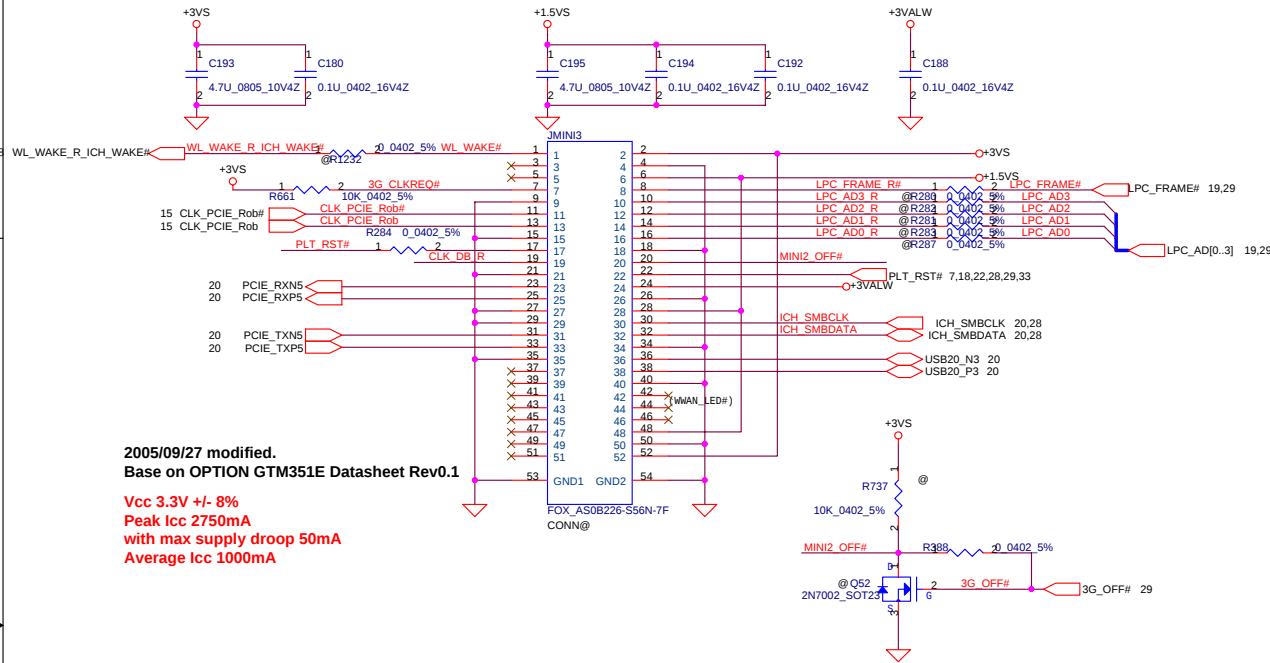
SEL3_ [A:B]	De-emphasis
0	0dB
1	-3.5dB



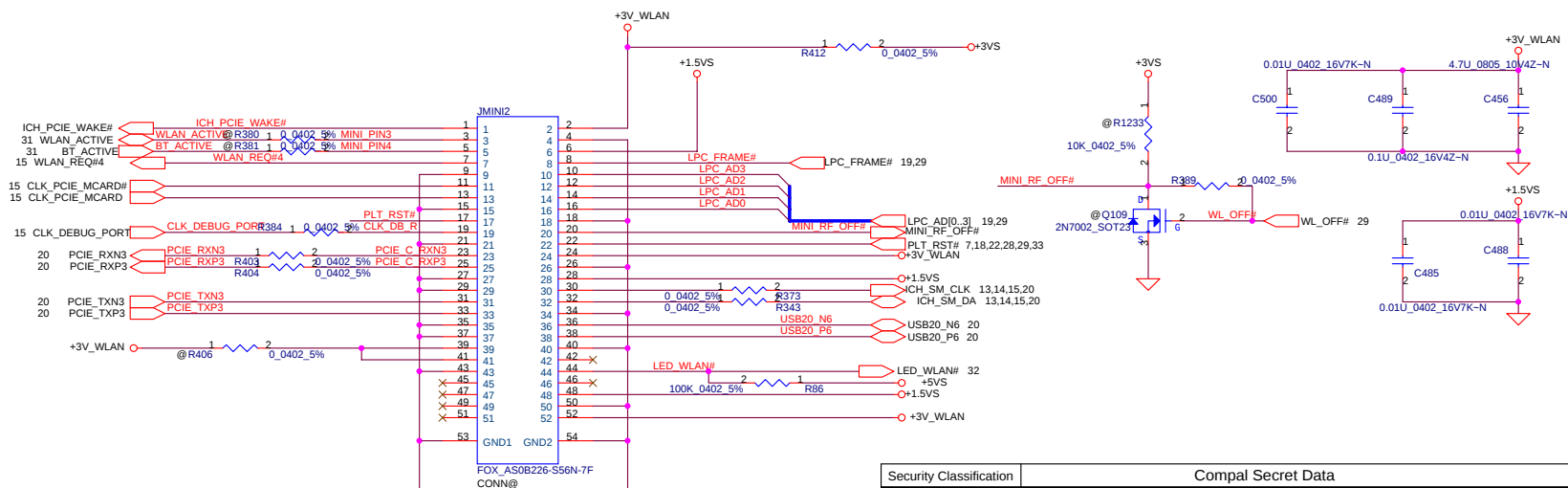
Equalizer Selection

SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz

Mini-Express Card for 3G Or TV Tuner

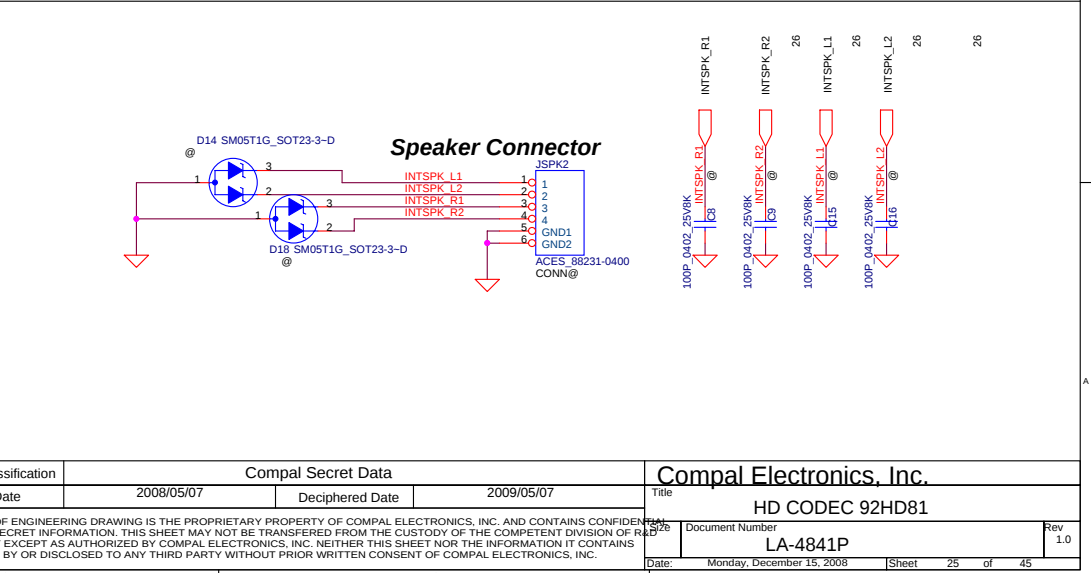
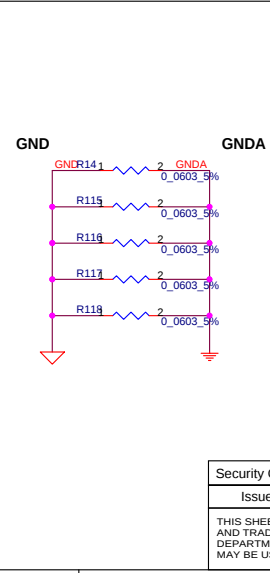
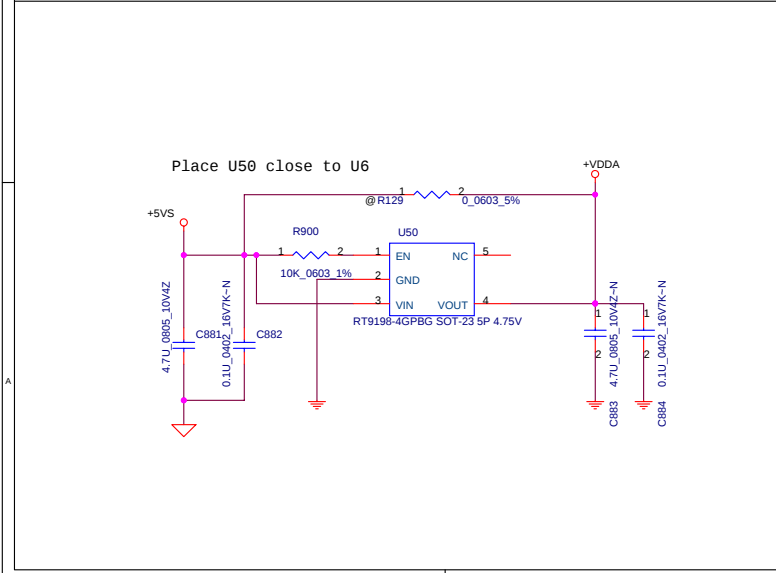
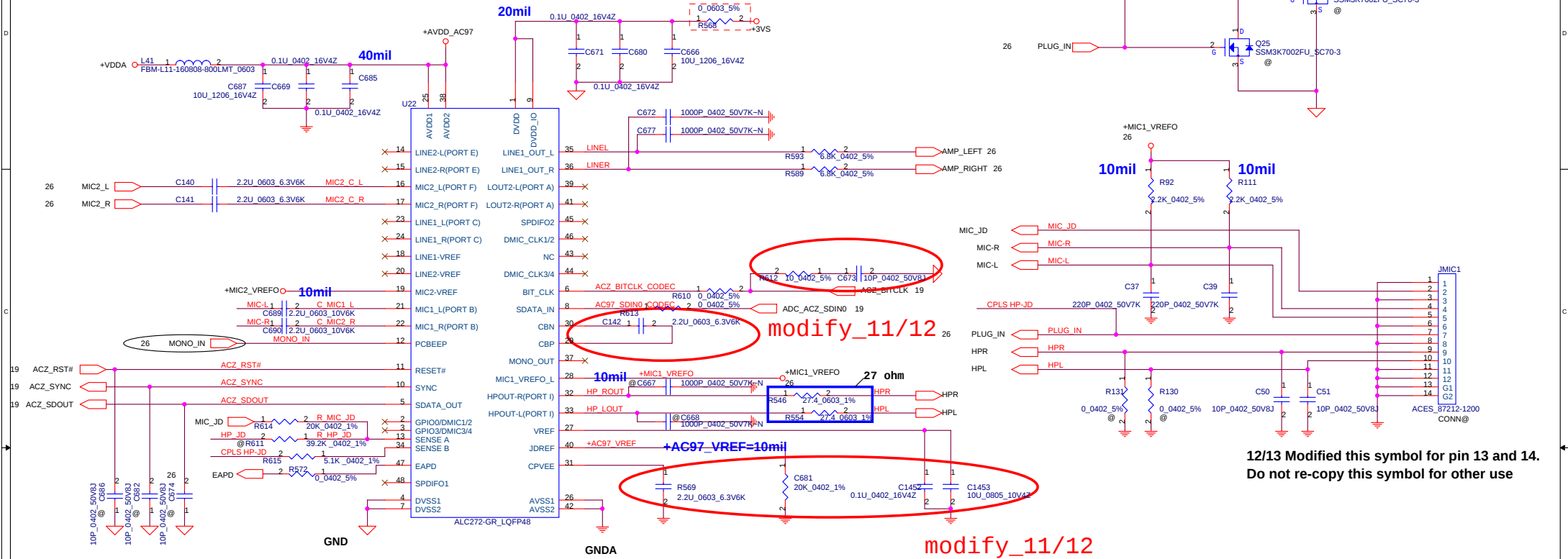


Mini-Express Card---WLAN



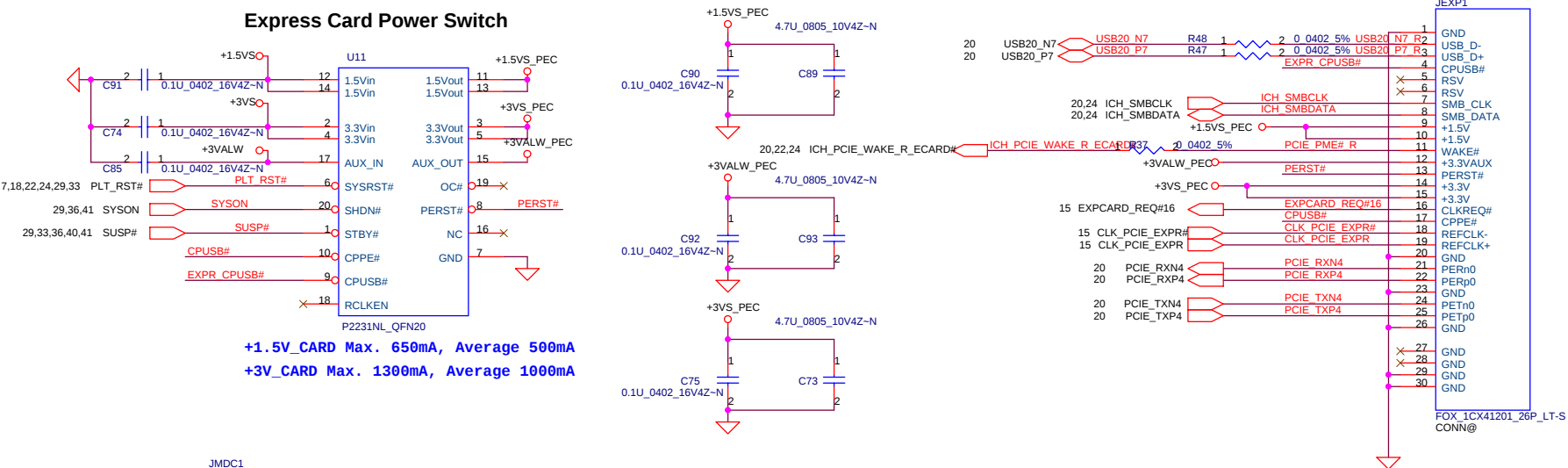
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HD Audio Codec



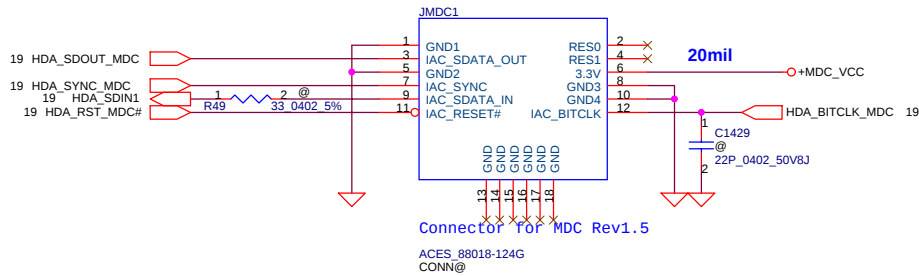
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Express card

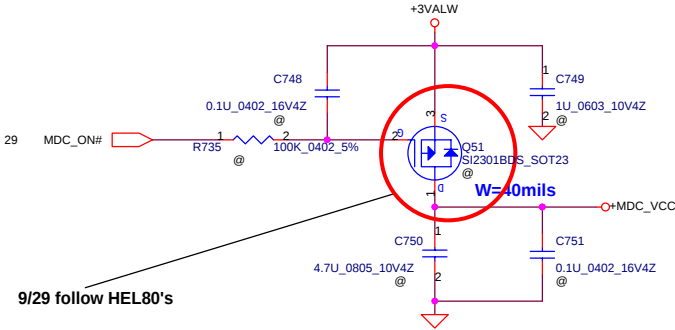


+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

MDC Conn.

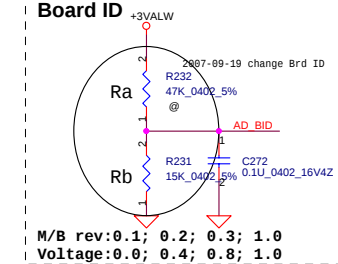


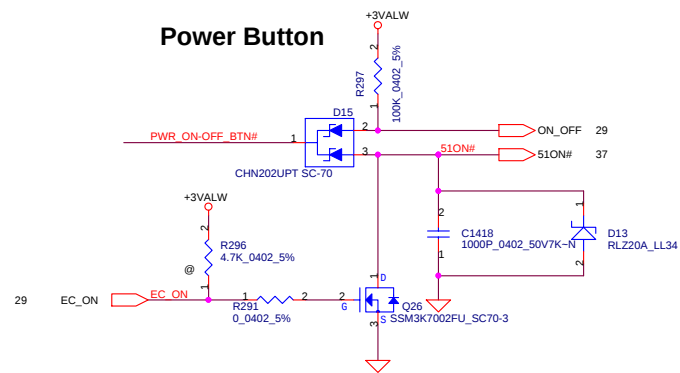
Connector for MDC Rev1.5
ACES_88018-124G
CONN@



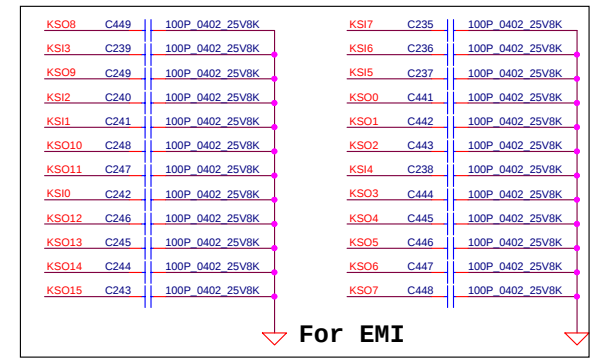
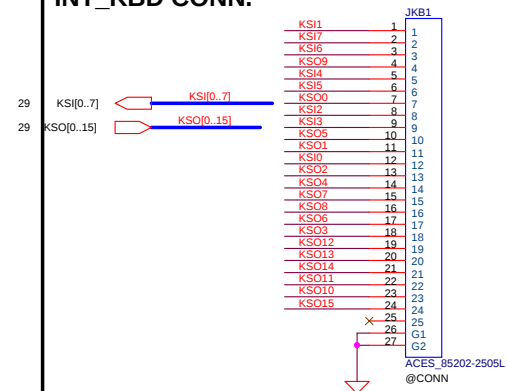
9/29 follow HEL80's

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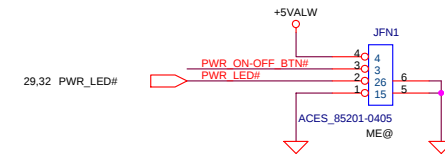




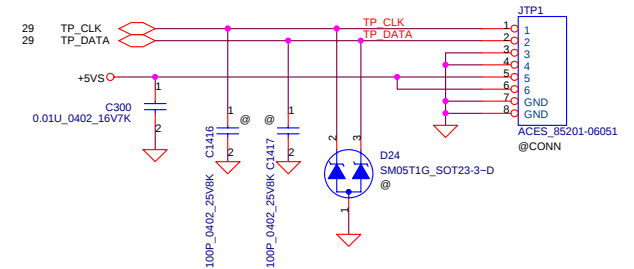
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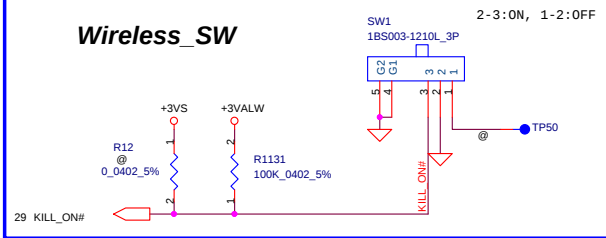
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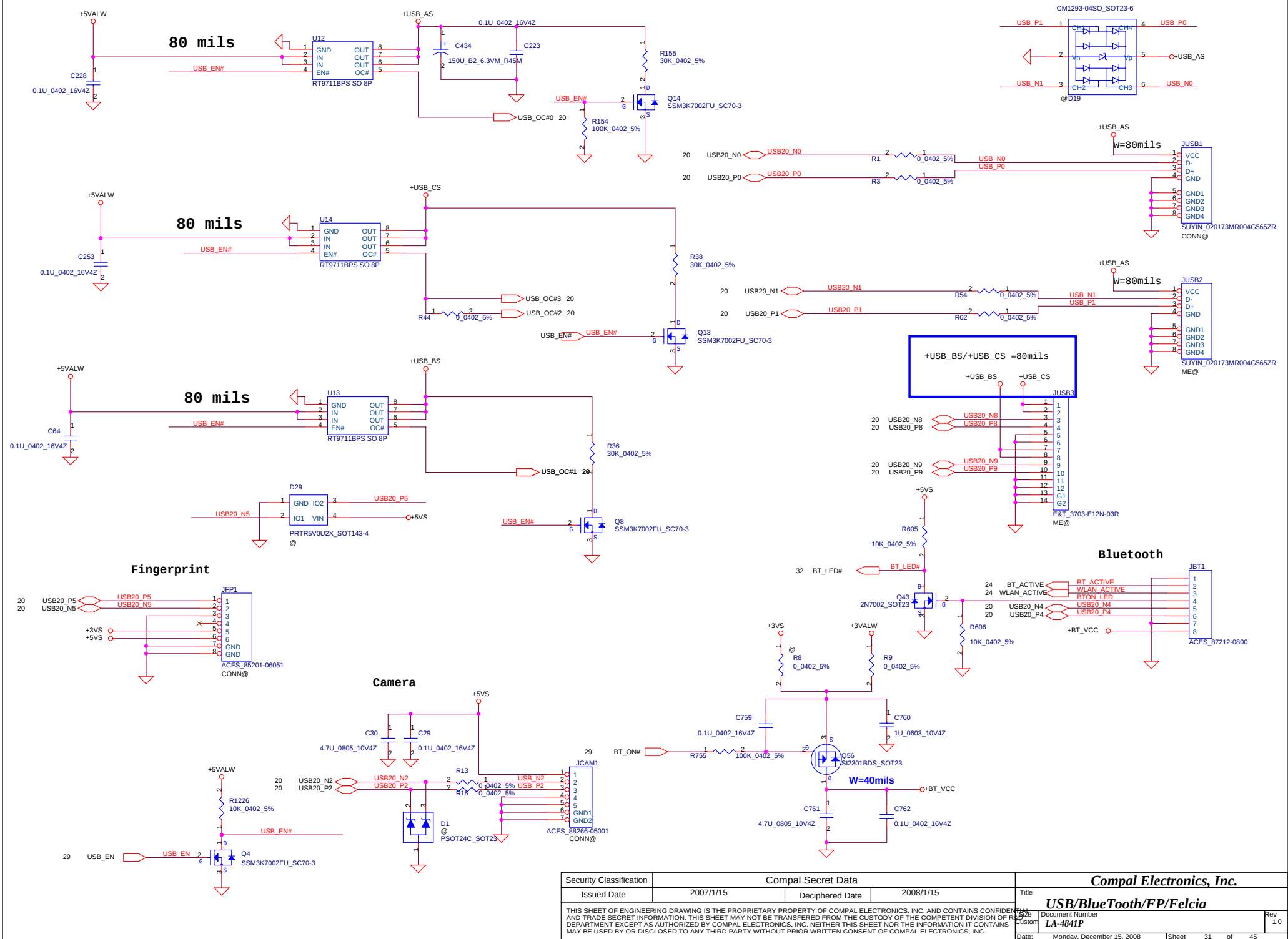


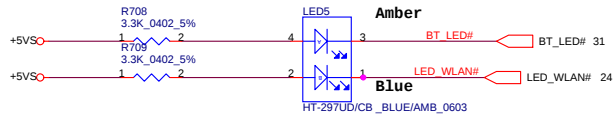
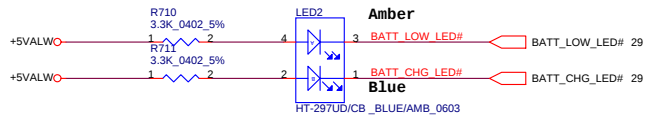
Touch PAD/B CONN.



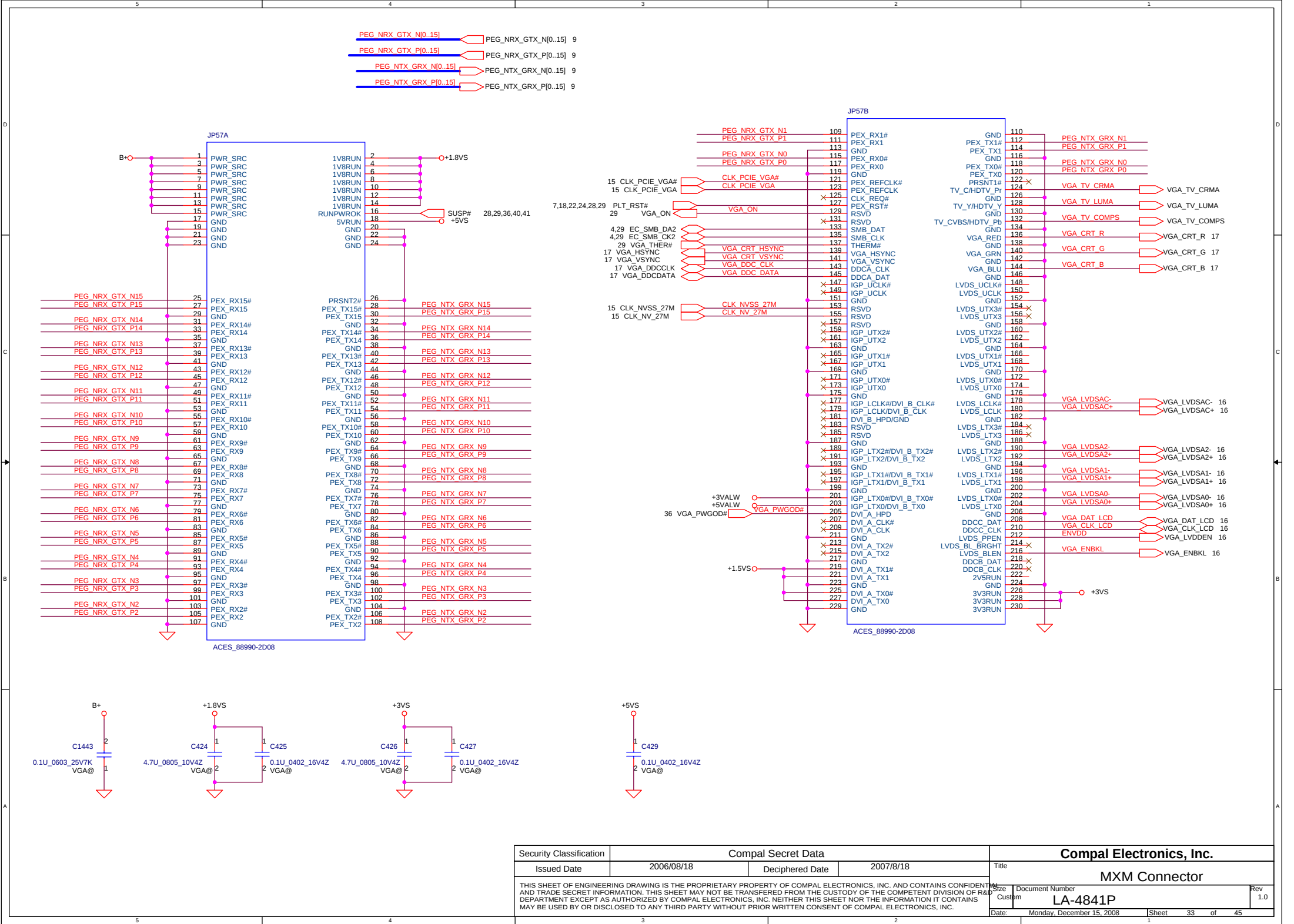
Wireless_SW

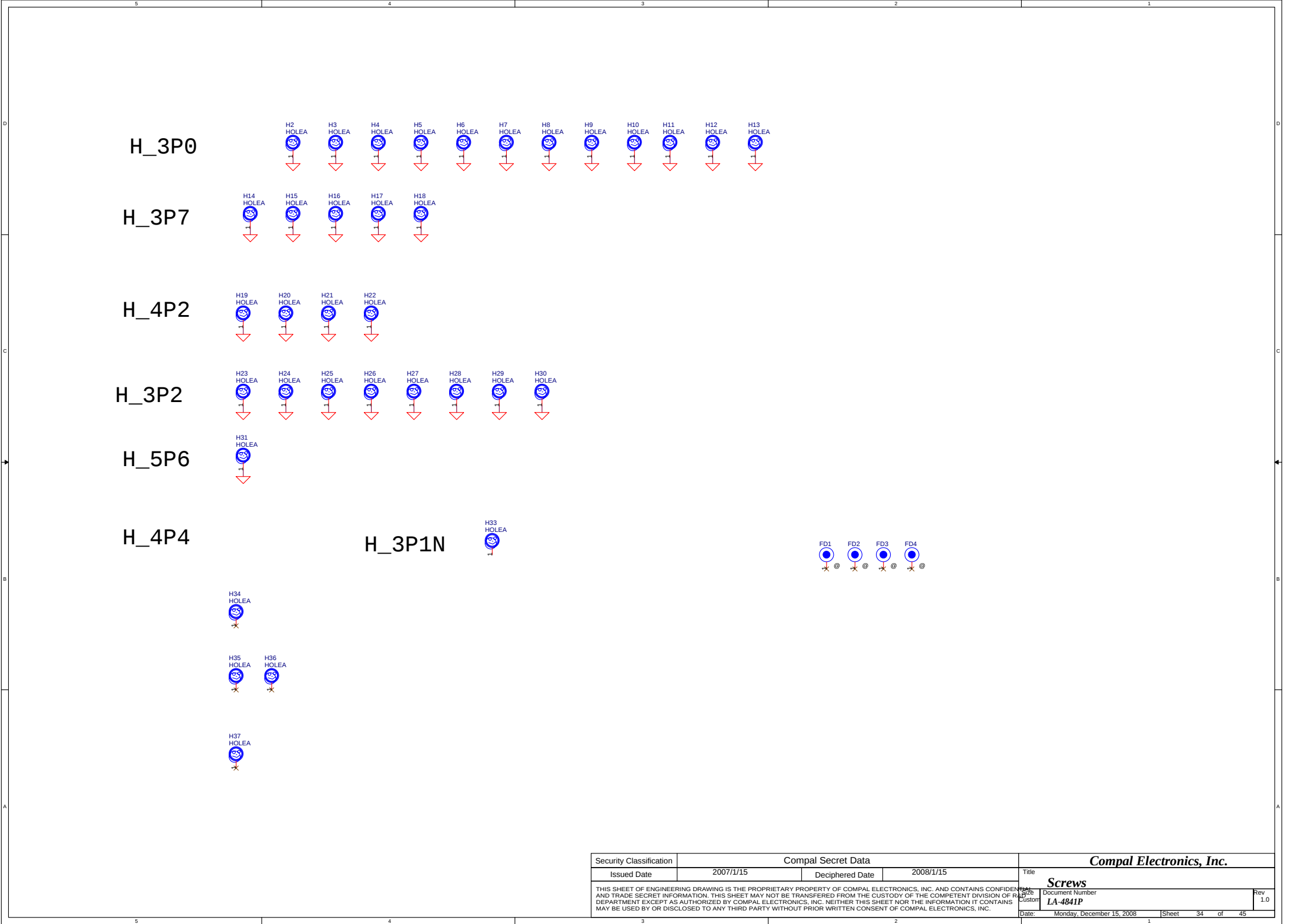






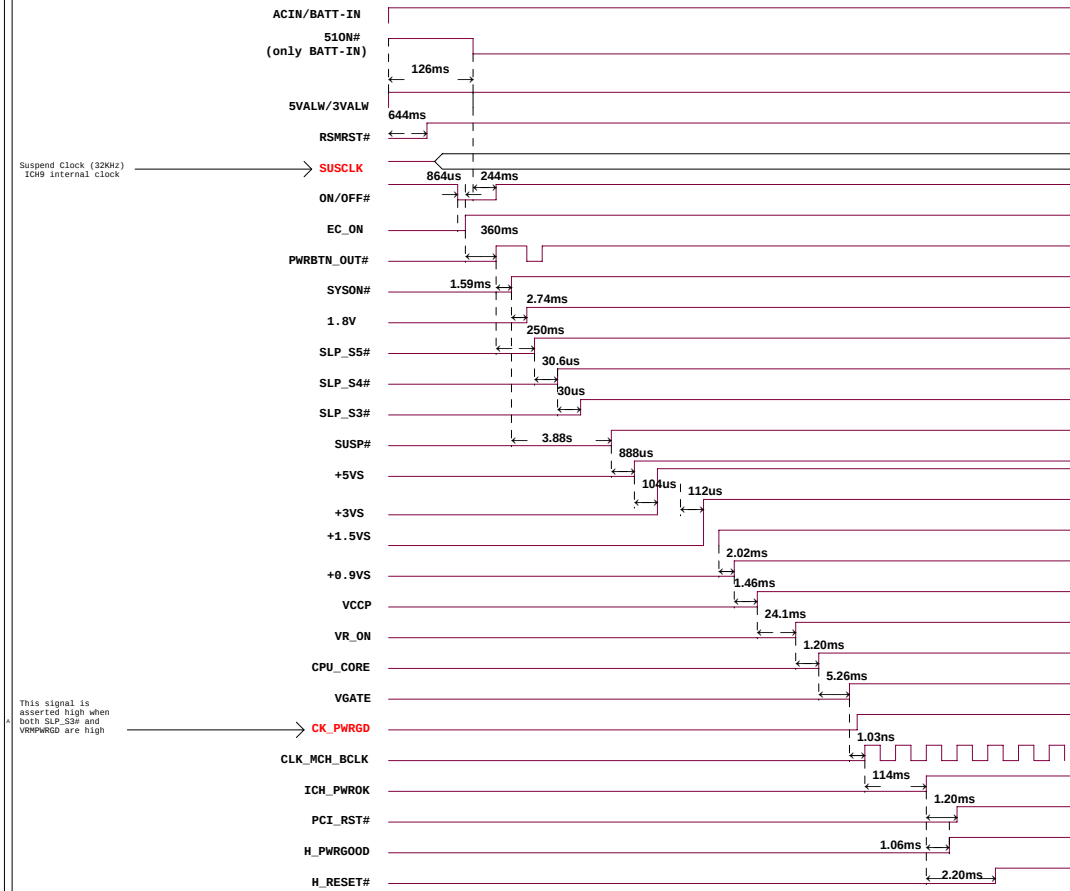
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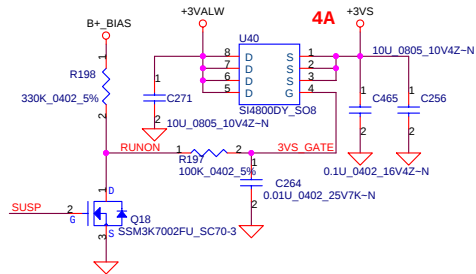


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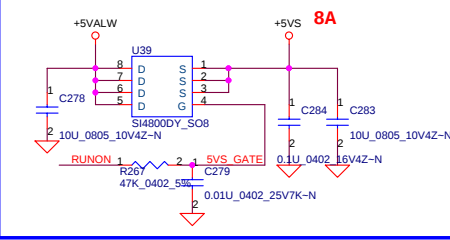
KAL80 POWER UP SEQUENCE



+3VALW to +3VS Transfer

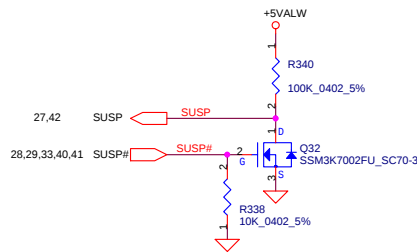
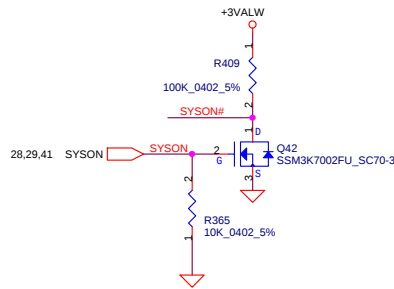
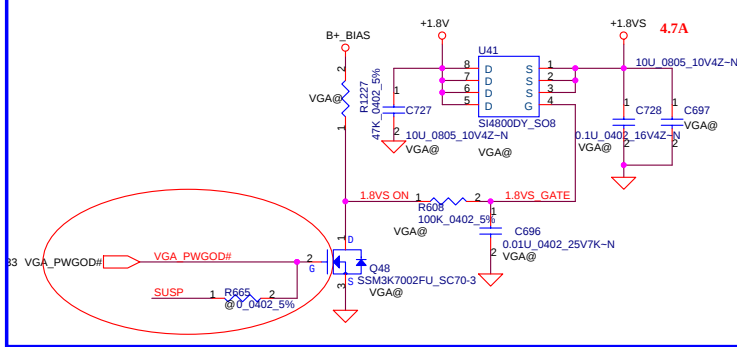


+5VALW to +5VS Transfer

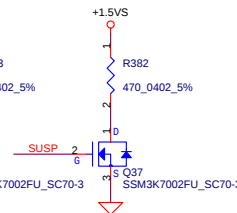
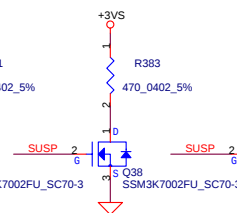
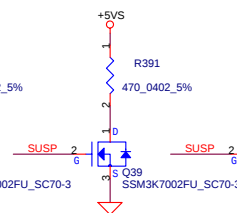
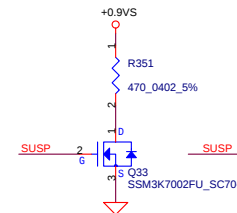
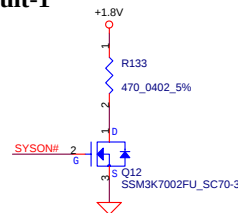


+CPU_CORE - C211 - 0.1U_0402_16V4Z-N - VCCP

+1.8V to +1.8VS Transfer



Discharge circuit-1



SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	DC/DC Circuits
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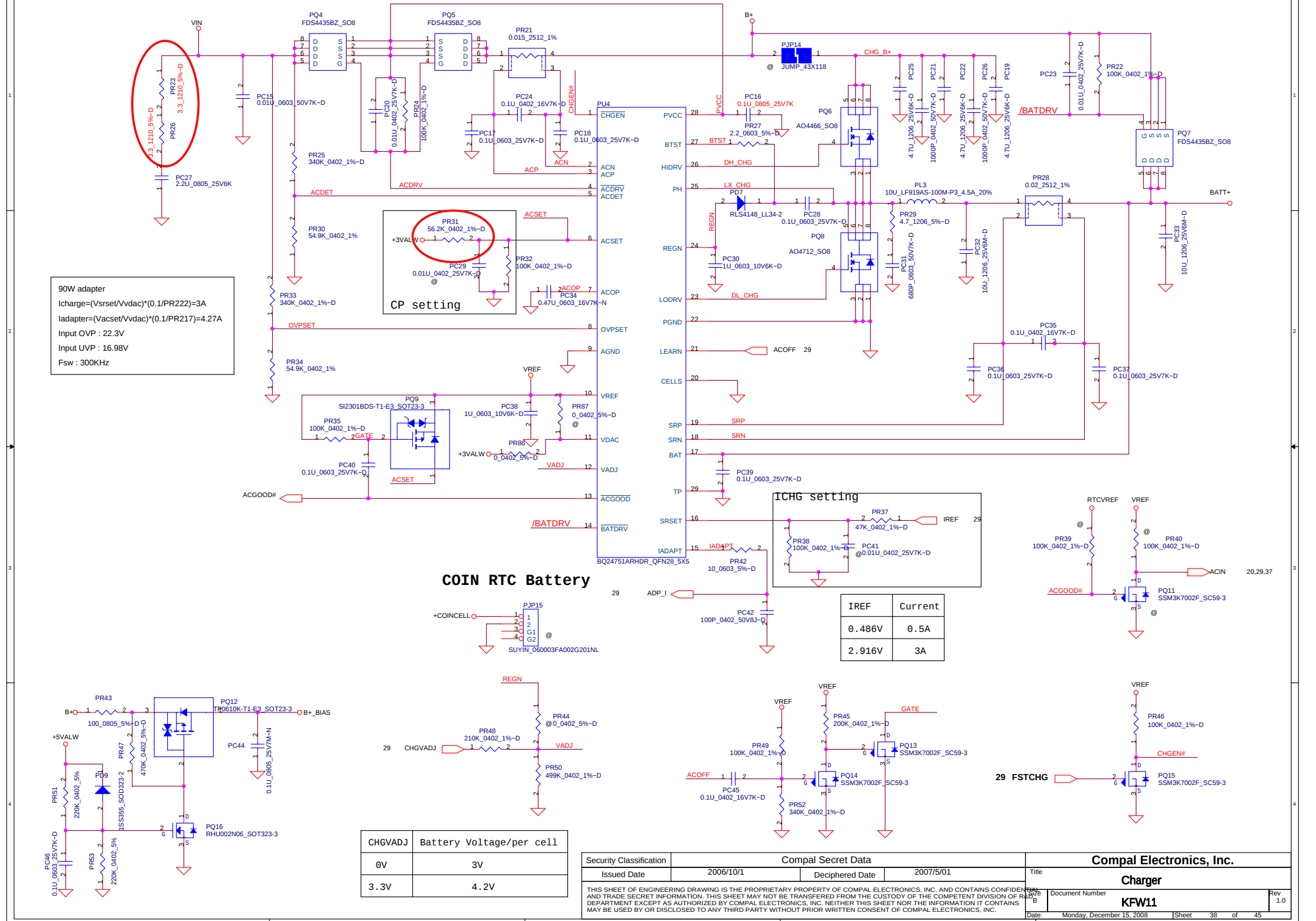
90W adapter
 $I_{charge} = (V_{srset}/V_{dca}) \times (0.1/PR222) = 3A$
 $I_{adapter} = (V_{acset}/V_{dca}) \times (0.1/PR217) = 4.27A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz

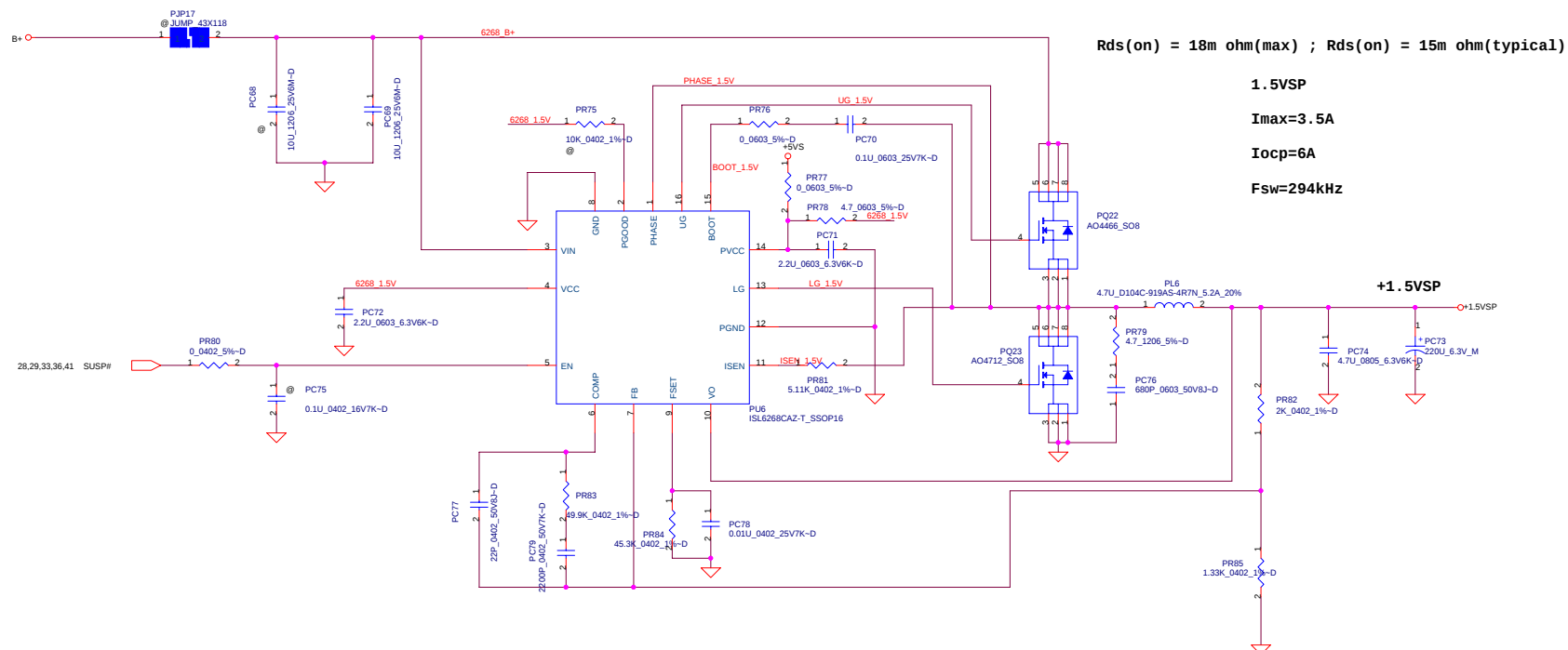
COIN RTC Battery

CHGVADJ	Battery Voltage/per cell
0V	3V
3.3V	4.2V

Security Classification	Compal Secret Data	
Issued Date	2006/10/1	Deciphered Date
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Charger		Rev 1.0
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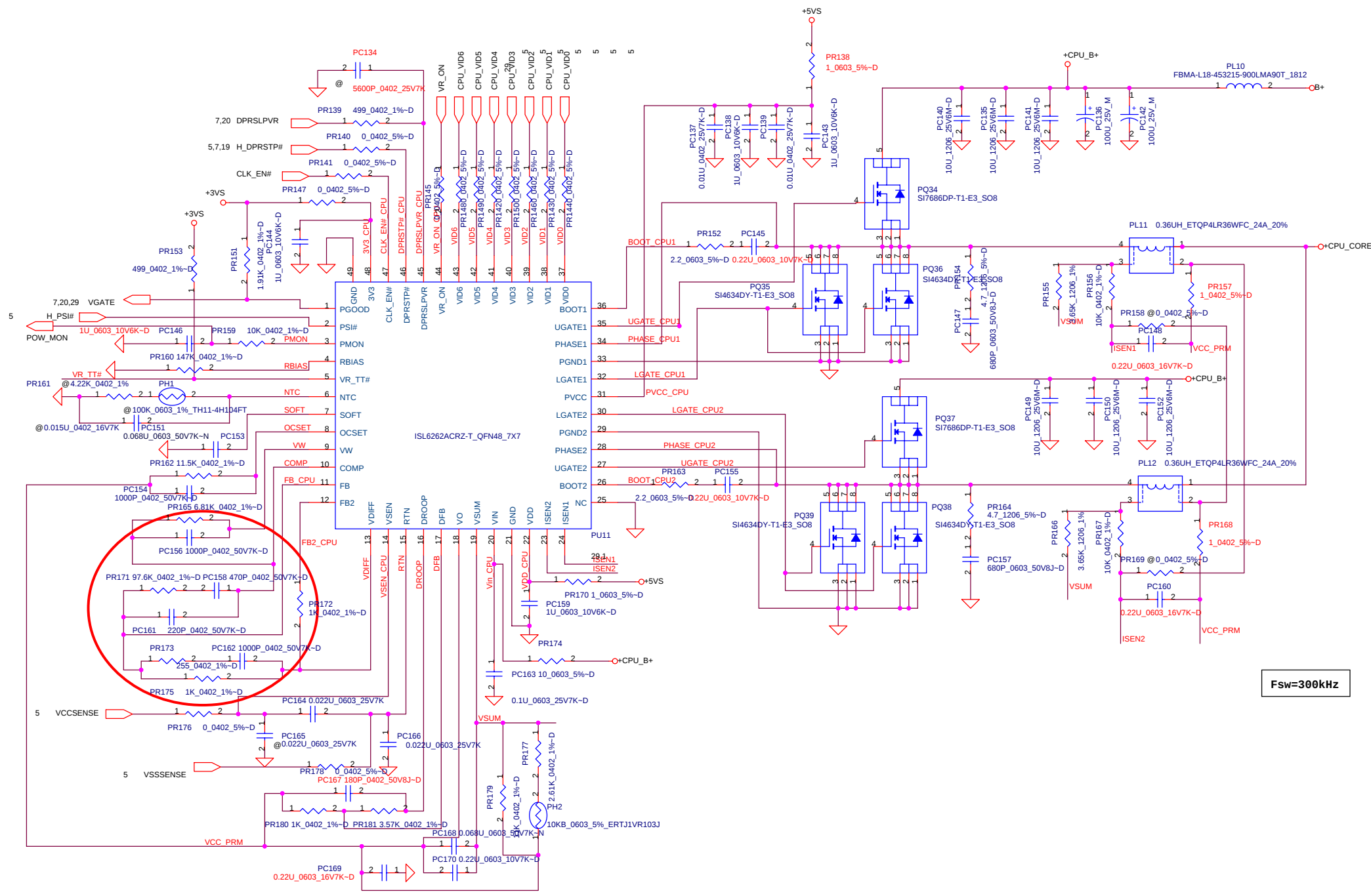


Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

1.5VSP
Imax=3.5A
Iocp=6A
Fsw=294kHz

+1.5VSP

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Issued Date	2006/10/1	Deciphered Date	2007/05/30	Title	1.5VSP
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Fsw=300kHz

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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	
				+CPU CORE	
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