Alba Discrete ATI M92-LP gDDR2 Schematics

uFCPGA Mobile Penryn

Intel Cantiga-PM + ICH9M

2009-03-23

REV : SA

DY : Nopop Component

GM : Pop when Cantiga is GM

PM : Pop when Cantiga is PM

G/P : BOM control if Cantiga is PM

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*

Size: Custom | Document Number: *Alba Discrete* | Rev: *SB*

Date: Monday, March 23, 2009 | Sheet 1 of 60

ALBA Discrete Block Diagram

PCB LAYER
L1: Top
L2: GND
L3: Signal
L4: Signal
L5: VCC
L6: Signal
L7: GND
L8: Bottom

Project code : 91.4BK01.001
Part Number : 48.4BK13.0SA
PCB P/N : 09207
Revision : SA

Clock Generator
SLG8SP513VTR 7

Intel Mobile CPU
Penryn
Socket P 8,9

FSB
800/1066MHz

VRAM(gDDR2)
32Mbx16x4 (512MB) 57,58

CRT 42
LCD 41
RGB CRT
LVDS(Dual Channel)

ATI M92-LP 53,54,55,56

PCIe x 16

Intel
Cantiga-GM
AGTL+ CPU I/F
DDR Memory I/F
External Graphics
10,11,12,13,14,15

DDRII 800 Channel A
DDR II 800 Channel B

DDRII 800 Slot 0 16
DDRII 800 Slot 1 17

DMIx4
CONTROL-LINK

Intel
ICH9-M
USB 2.0/1.1 ports (12)
PCI Express ports (6)
High Definition Audio
SATA ports (4)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
18,19,20,21

Power SW
TPS2231RGP 50

New Card
(On Express Card board) 50

PCIE x 1 & USB 2.0 x 1
PCIE x 1
10/100 LOM
RTL8103EL 25
RJ45
CONN 42

USB 2.0 x 2
Left Side:
USB x 2 46

PCIE
PCIE x 1
Mini-Card
802.11a/b/g/n 43

USB 2.0
USB 2.0 x 1
CAMERA
(Option) 47

USB 2.0 x 1
Bluetooth 45

USB 2.0 x 1
Right Side:
USB x 1 51

LPC Bus

(7 in 1)SD/MMC
MS/MS Pro/xD
(On Express Card board)

CardReader
Realtek
RTS5159 50

USB2.0

Digital Mic Array
(Option) 47
Internal Mic 44

MIC IN
HP OUT
(On Express Card board)

Azalia
CODEC
OP AMP
IDT
92HD81 22

AZALIA

2CH SPEAKER 44

SATA
SATA

HDD 44
ODD 44

SPI

KBC
WINBOND
WPCE773L 26

Flash ROM
2MB 47
Touch
PAD 45
Int.
KB 45
Thermal
& Fan
EMC2102 28,44

CPU DC/DC ISL6266A 34,35	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51117 36	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

SYSTEM DC/DC TPS51125 33	
INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

LDO L6935TR 37	
INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN

SYSTEM DC/DC TPS51117 38	
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS

SYSTEM DC/DC TPS51117 39	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

CHARGER MAX8731A 32	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

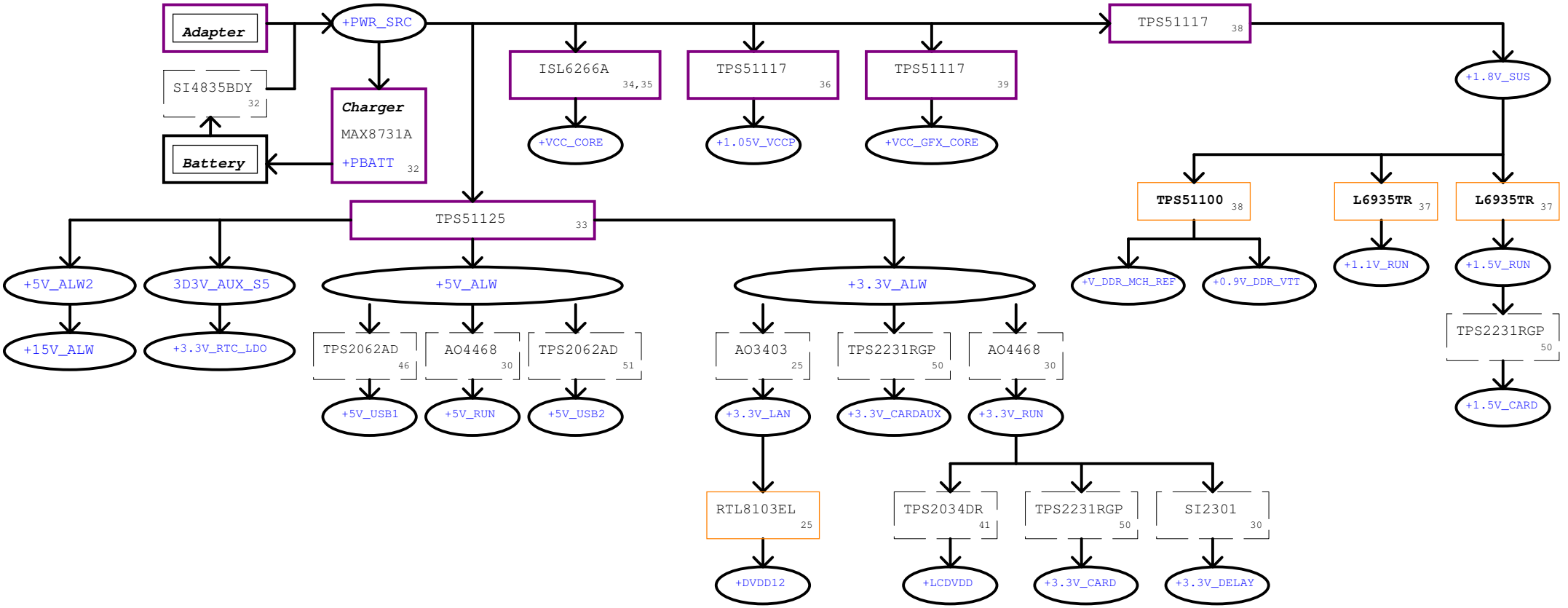
LDO TPS51100 38	
INPUTS	OUTPUTS
+1.8V_SUS	+V_DDR_MCH_REF +0.9V_DDR_VTT

LDO L6935TR 37	
INPUTS	OUTPUTS
+1.8V_SUS	+1.1V_RUN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: Custom | Document Number: Alba Discrete | Rev: SB
Date: Monday, March 23, 2009 | Sheet 2 of 60



Power Shape

Regulator	LDO	Switch

<Core Design>

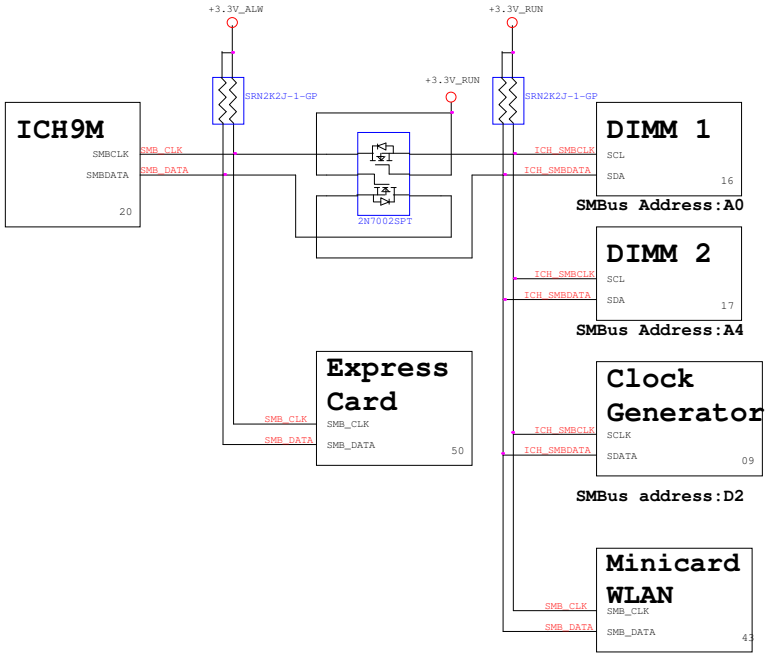
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

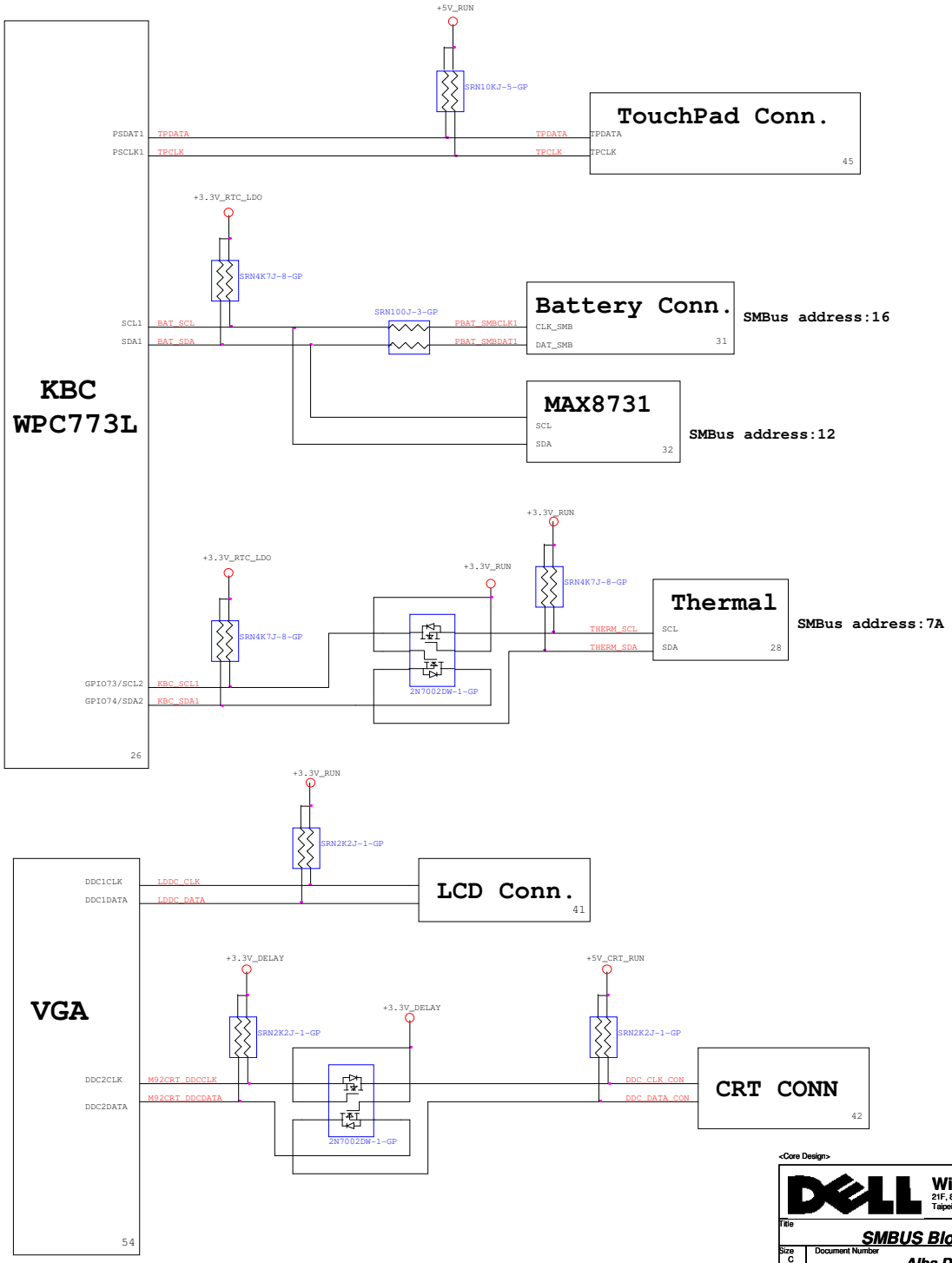
Size	Document Number	Rev
Custom	***Alba Discrete***	SB

Date: Monday, March 23, 2009 Sheet 3 of 59

ICH9M SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

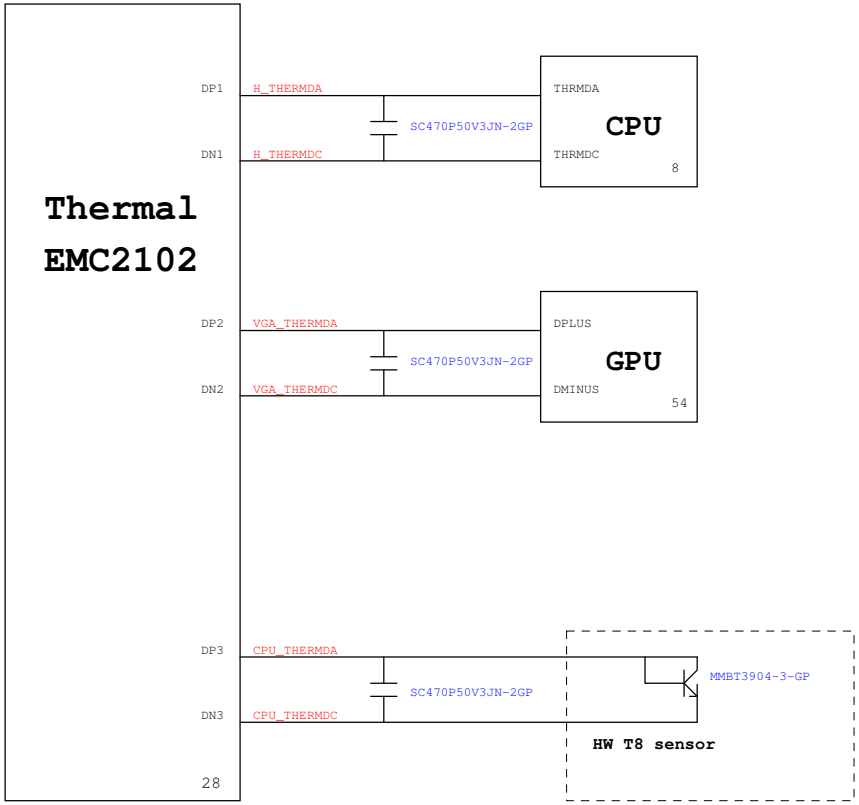
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

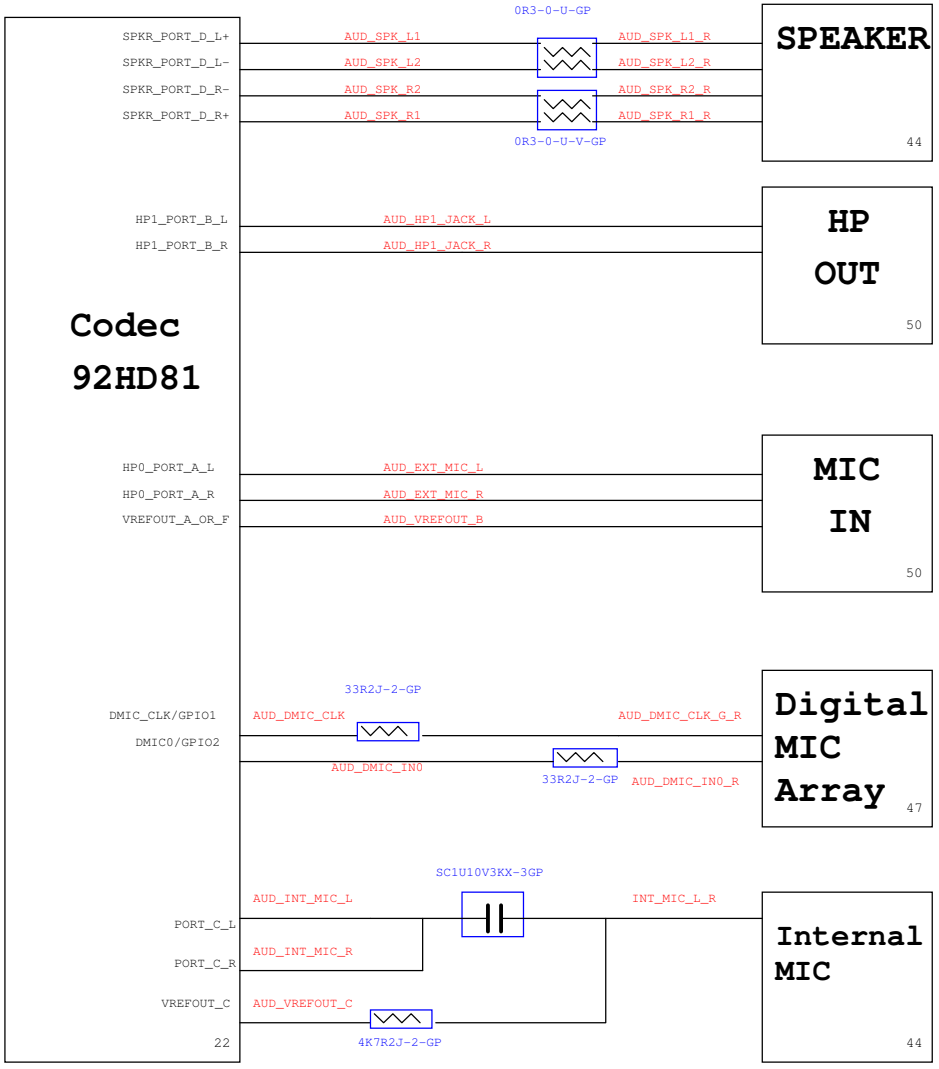
Size	Document Number	Rev
C	Alba Discrete	SB

Date: Monday, March 23, 2009 Sheet 4 of 59

Thermal Block Diagram



Audio Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 5 of 59

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

<Core Design>

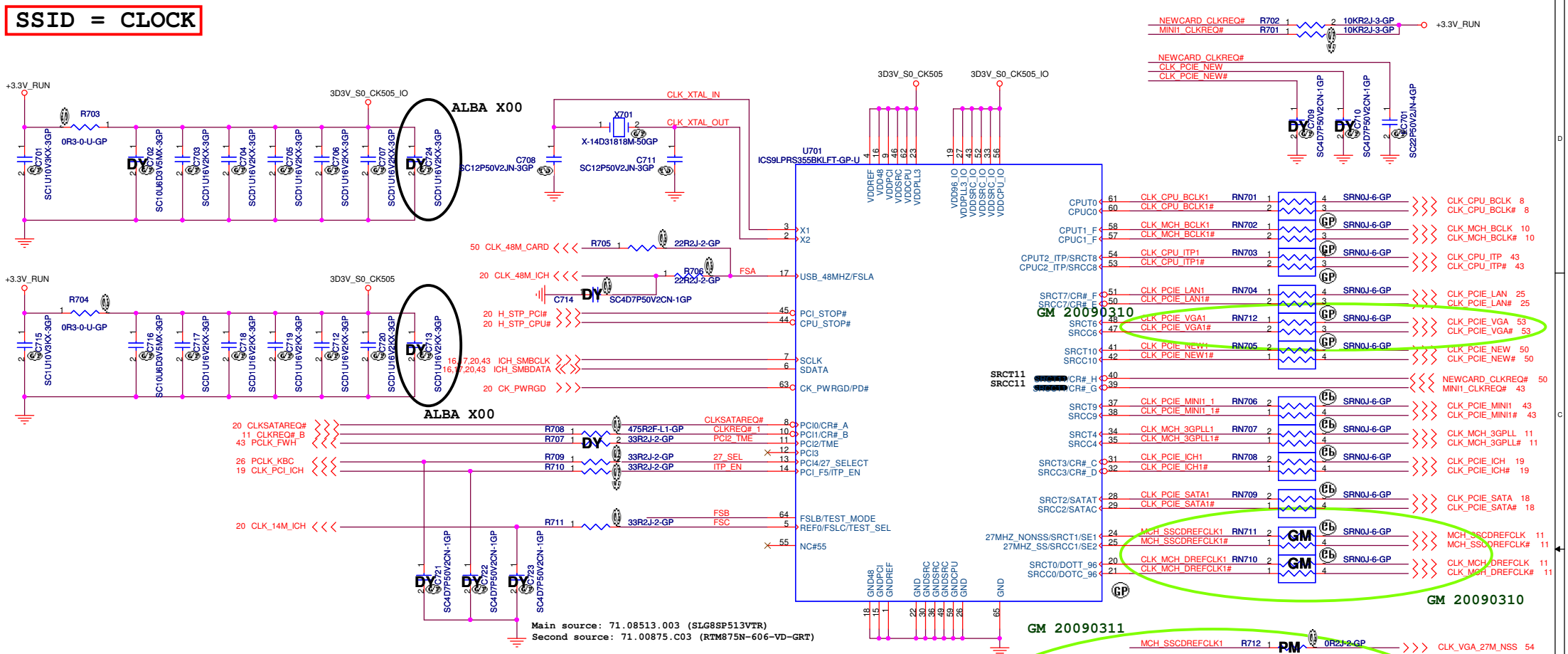
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 6 of 59

SSID = CLOCK



ITP_EN	Output
0	SRC8
1	CPU_ITP

PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

27_SEL	PIN 20	PIN 21	
0	DOT96T	DOT96C	UMA
1	SRCT0	SRCC0	Discrete

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator SLG8SP513VTR

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 7 of 59

SSID = CPU

CPU1A 1 OF 4

ADDR GROUP 0 / CONTROL

H_A#[35..3] ↔ A3# A4# A5# A6# A7# A8# A9# A10# A11# A12# A13# A14# A15# A16# ADSTB0#

H_REQ#[4..0] ↔ REQ0# REQ1# REQ2# REQ3# REQ4#

ADDR GROUP 1 / XDP/ITP SIGNALS

A17# A18# A19# A20# A21# A22# A23# A24# A25# A26# A27# A28# A29# A30# A31# A32# A33# A34# A35# ADSTB1#

ICH

A20M# FERR# IGNNE# STPCLK# LINT0 LINT1 SMI#

RESERVED

RSVD#M4 RSVD#N5 RSVD#T2 RSVD#V3 RSVD#B2 RSVD#D2 RSVD#D22 RSVD#D3 RSVD#F6 KEY_NC

TP807 RSVD_CPU_1 M4
TP808 RSVD_CPU_2 N5
TP802 RSVD_CPU_3 T2
TP804 RSVD_CPU_4 V3
TP803 RSVD_CPU_5 B2
TP805 RSVD_CPU_6 C3
TP813 RSVD_CPU_7 D2
TP810 RSVD_CPU_8 D22
TP806 RSVD_CPU_9 D3
TP809 RSVD_CPU_10 F6
TP801 RSVD_CPU_11 B1

BGA479-SKT6-GPU7
62.10040.221

TP814

ADS# BNR# BPRI# DEFER# DRDY# DBSY# BR0# IERR# INIT# LOCK# RESET# RS0# RS1# RS2# TRDY# HIT# HITM#

H_ADS# 10 H_BNR# 10 H_BPRI# 10 H_DEFER# 10 H_DRDY# 10 H_DBSY# 10 H_BREQ#0 10

IERR# — CPU_IERR# — R804 1 — 56R2J-4-GP — +1.05V_VCCP

INIT# — H_INIT# 18

H_LOCK# 10 H_CPURST# 10,43 H_RS#[2..0] 10

H_CPURST# — H_RS#0 — H_RS#1 — H_RS#2

H_TRDY# 10 H_HIT# 10 H_HITM# 10

XDP/ITP SIGNALS

BPM0# BPM1# BPM2# BPM3# PRDY# PREQ# TCK TDI TDO TMS TRST# DBR#

ITP_BPM#0 ITP_BPM#1 ITP_BPM#2 ITP_BPM#3 ITP_BPM#4 ITP_BPM#5 ITP_TCK ITP_TDI ITP_TDO ITP_TMS ITP_TRST# ITP_DBRESET#

ITP_BPM#0 43 ITP_BPM#1 43 ITP_BPM#2 43 ITP_BPM#3 43 ITP_BPM#4 43 ITP_BPM#5 43 ITP_TCK 43 ITP_TDI 43 ITP_TDO 43 ITP_TMS 43 ITP_TRST# 43 ITP_DBRESET# 20,43

THERMAL

PROCHOT# — R805 1 — DY — 0R2J-2-GP — CPU_PROCHOT# 34

THRMDA THRMDC — R806 1 — DY — 56R2J-4-GP — +1.05V_VCCP

H_THERMDA — H_THERMDC

H_THERMDA 28 H_THERMDC 28

THERMTRIP# — R810 1 — DY — 56R2J-4-GP — +1.05V_VCCP

H_THRMTRIP# 11,18,26,30,54

H_THRMTRIP# should connect to ICH9 and MCH without T-ing.

HCLK BCLK0 BCLK1

CLK_CPU_BCLK 7 CLK_CPU_BCLK# 7

H_ADSTB#1 10

H_A20M# 18 H_FERR# 18 H_IGNNE# 18

H_STPCLK# 18 H_INTR 18 H_NMI 18 H_SMI# 18

+1.05V_VCCP

R814 1KR2F-3-GP

CPU_GTLREF0

R813 2KR2F-3-GP

C802 SC1KP50V2KX-1GP

X01 20090112

Layout notes
Z= 55 Ohm 0.5" MAX for CPU_GTLREF0

H_DINV#[3..0] ↔ H_DINV#[3..0] 10
H_DSTBN#[3..0] ↔ H_DSTBN#[3..0] 10
H_DSTBP#[3..0] ↔ H_DSTBP#[3..0] 10
H_D#[63..0] ↔ H_D#[63..0] 10

CPU1B 2 OF 4

DATA GRP2

H_D#0 H_D#1 H_D#2 H_D#3 H_D#4 H_D#5 H_D#6 H_D#7 H_D#8 H_D#9 H_D#10 H_D#11 H_D#12 H_D#13 H_D#14 H_D#15

D0# D1# D2# D3# D4# D5# D6# D7# D8# D9# D10# D11# D12# D13# D14# D15#

H_D#32 H_D#33 H_D#34 H_D#35 H_D#36 H_D#37 H_D#38 H_D#39 H_D#40 H_D#41 H_D#42 H_D#43 H_D#44 H_D#45 H_D#46 H_D#47

D32# D33# D34# D35# D36# D37# D38# D39# D40# D41# D42# D43# D44# D45# D46# D47#

10 H_DSTBN#0 10 H_DSTBP#0 10 H_DINV#0 — DSTBN0# DSTBP0# DINV0#

DSTBN2# DSTBP2# DINV2# — 10 H_DSTBN#2 10 H_DSTBP#2 10 H_DINV#2

DATA GRP3

H_D#16 H_D#17 H_D#18 H_D#19 H_D#20 H_D#21 H_D#22 H_D#23 H_D#24 H_D#25 H_D#26 H_D#27 H_D#28 H_D#29 H_D#30 H_D#31

D16# D17# D18# D19# D20# D21# D22# D23# D24# D25# D26# D27# D28# D29# D30# D31#

H_D#48 H_D#49 H_D#50 H_D#51 H_D#52 H_D#53 H_D#54 H_D#55 H_D#56 H_D#57 H_D#58 H_D#59 H_D#60 H_D#61 H_D#62 H_D#63

D48# D49# D50# D51# D52# D53# D54# D55# D56# D57# D58# D59# D60# D61# D62# D63#

10 H_DSTBN#1 10 H_DSTBP#1 10 H_DINV#1 — DSTBN1# DSTBP1# DINV1#

DSTBN3# DSTBP3# DINV3# — H_DSTBN#3 10 H_DSTBP#3 10 H_DINV#3 10

MISC

GTLREF TEST1 TEST2 TEST3 TEST4 TEST5 TEST6 BSEL0 BSEL1 BSEL2

R807 1 DY 1KR2J-1-GP TEST1
R809 1 DY 1KR2J-1-GP TEST2
R808 1 DY 1KR2J-1-GP CPU_TEST3
R801 1 DY 1KR2J-1-GP CPU_TEST5

7 CPU_BSEL0 7 CPU_BSEL1 7 CPU_BSEL2

COMP0 COMP1 COMP2 COMP3

R812 1 27D4R2F-L1-GP
R811 1 54D9R2F-L1-GP
R803 1 27D4R2F-L1-GP
R802 1 54D9R2F-L1-GP

DPRSTP# DPSLP# DPWR# PWRGOOD SLP# PSI#

H_DPRSTP# 11,18,34 H_DPSLP# 18 H_DPWR# 10 H_PWRGOOD 18,30 H_CPUSLP# 10 PSI# 34

BGA479-SKT6-GPU7
62.10040.221

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

<Core Design>

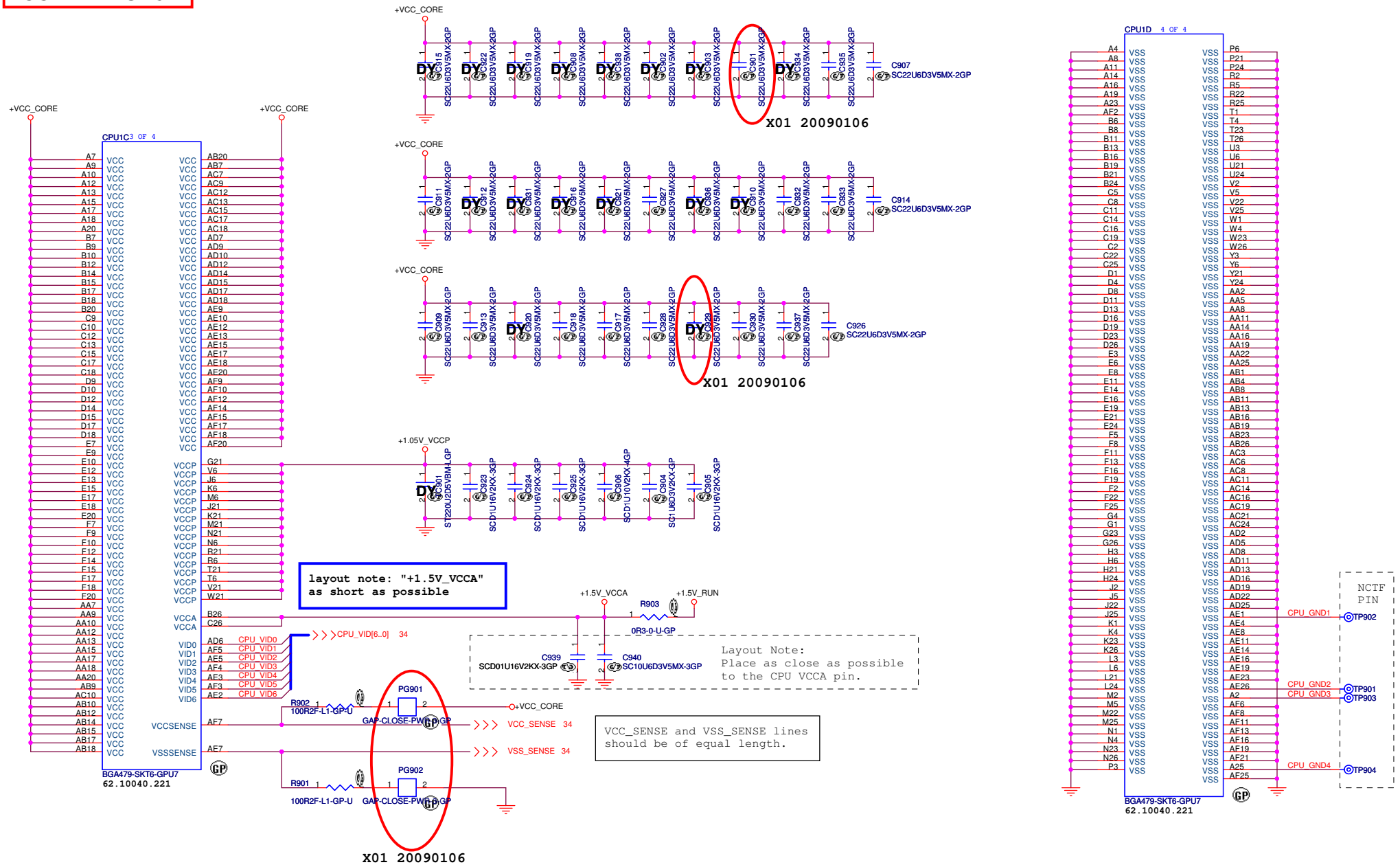
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU-FSB(1/2)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 8 of 59

SSID = CPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU-Power(2/2)

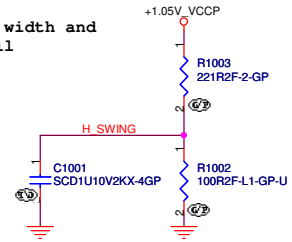
Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 9 of 59

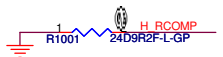
SSID = MCH

H_SWING routing Trace width and Spacing use 10 / 20 mil

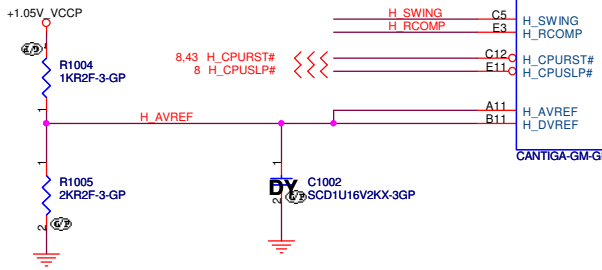
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place R1001 near to the chip (< 0.5")



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-HOST(1/6)

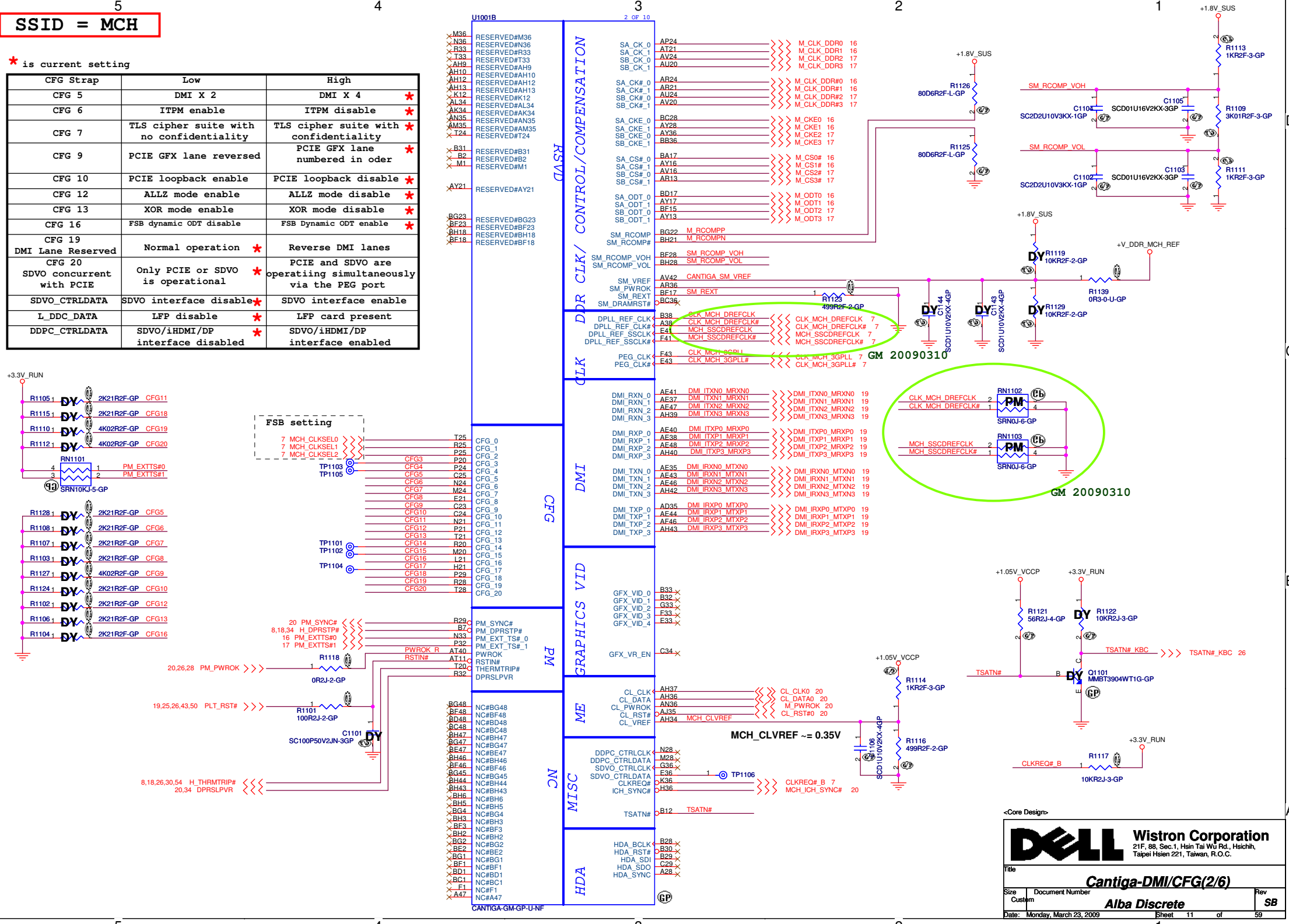
Size	Document Number	Rev
Custom	Alba Discrete	SB

Date: Monday, March 23, 2009 Sheet 10 of 59

SSID = MCH

* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in oder *
CFG 10	PCIE loopback enable	PCIE loopback disable *
CFG 12	ALLZ mode enable	ALLZ mode disable *
CFG 13	XOR mode enable	XOR mode disable *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19 DMI Lane Reserved	Normal operation *	Reverse DMI lanes
CFG 20 SDVO concurrent with PCIE	Only PCIE or SDVO is operational *	PCIE and SDVO are operatiing simultaneously via the PEG port
SDVO_CTRLDATA	SDVO interface disable *	SDVO interface enable
L_DDC_DATA	LFP disable *	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled *	SDVO/iHDMI/DP interface enabled



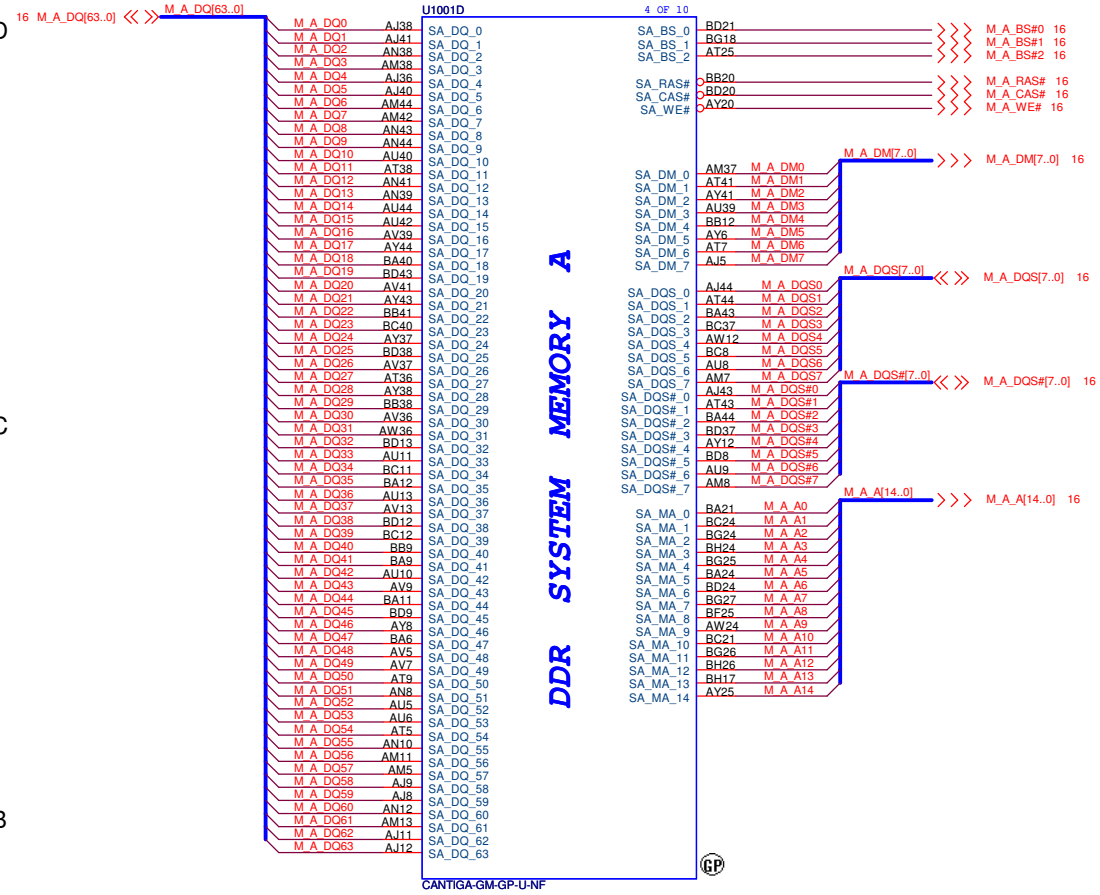
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

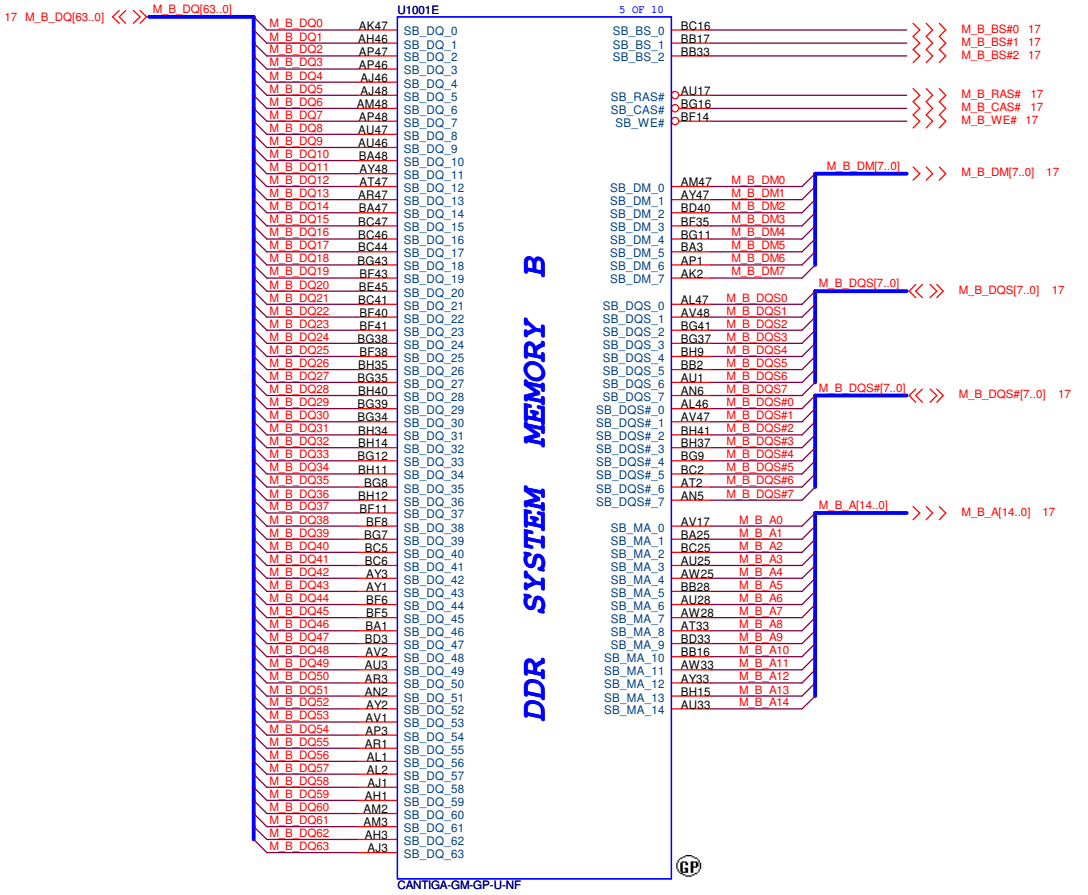
Title: Cantiga-DMI/CFG(2/6)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 11 of 59

SSID = MCH





<Core Design>

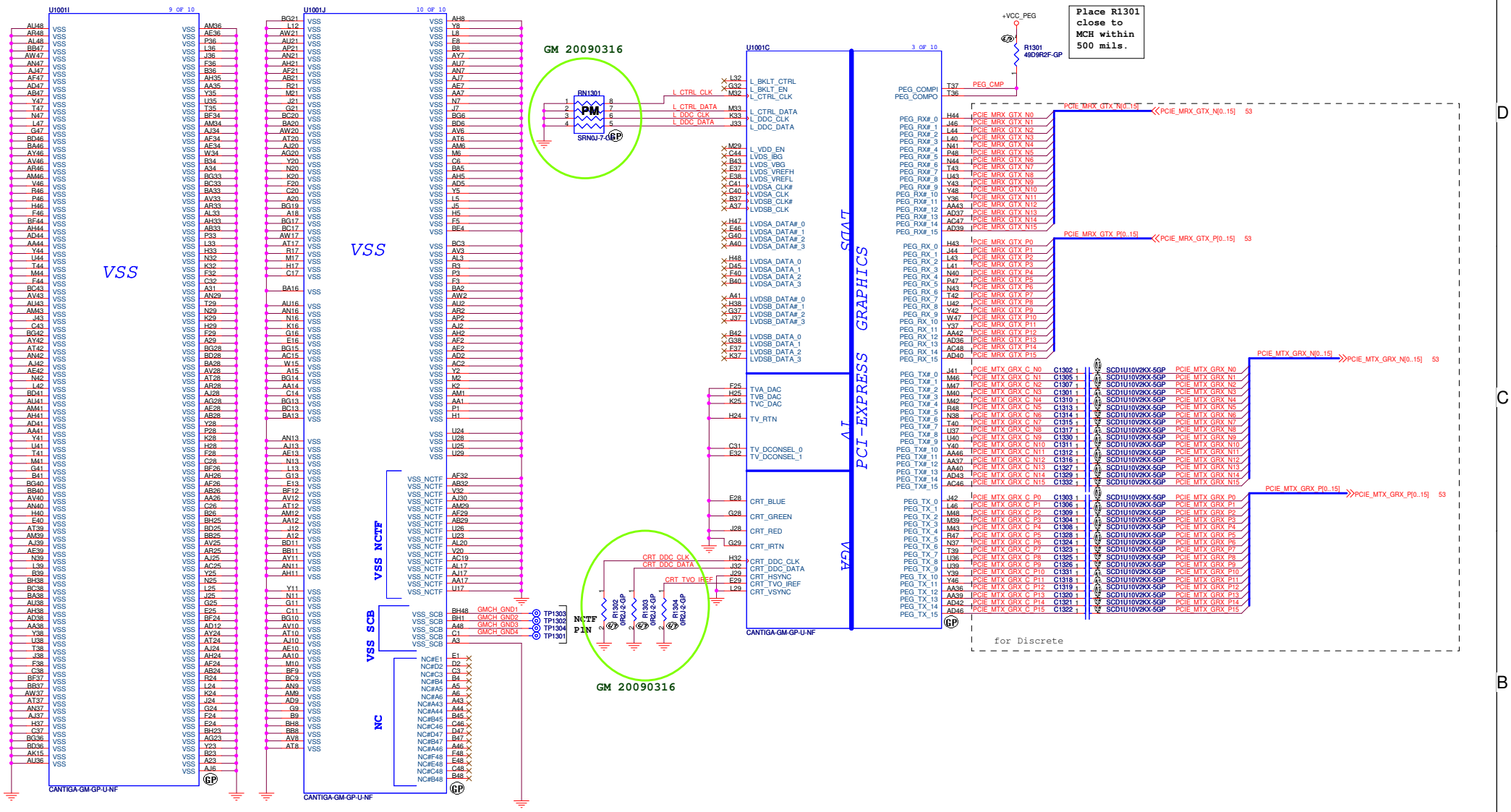
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-DDR(3/6)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 12 of 59

SSID = MCH



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cantiga-GND/LVDS/VGA(4/6)**

Size: C | Document Number: **Alba Discrete** | Rev: SB

Date: Monday, March 23, 2009 | Sheet 13 of 59

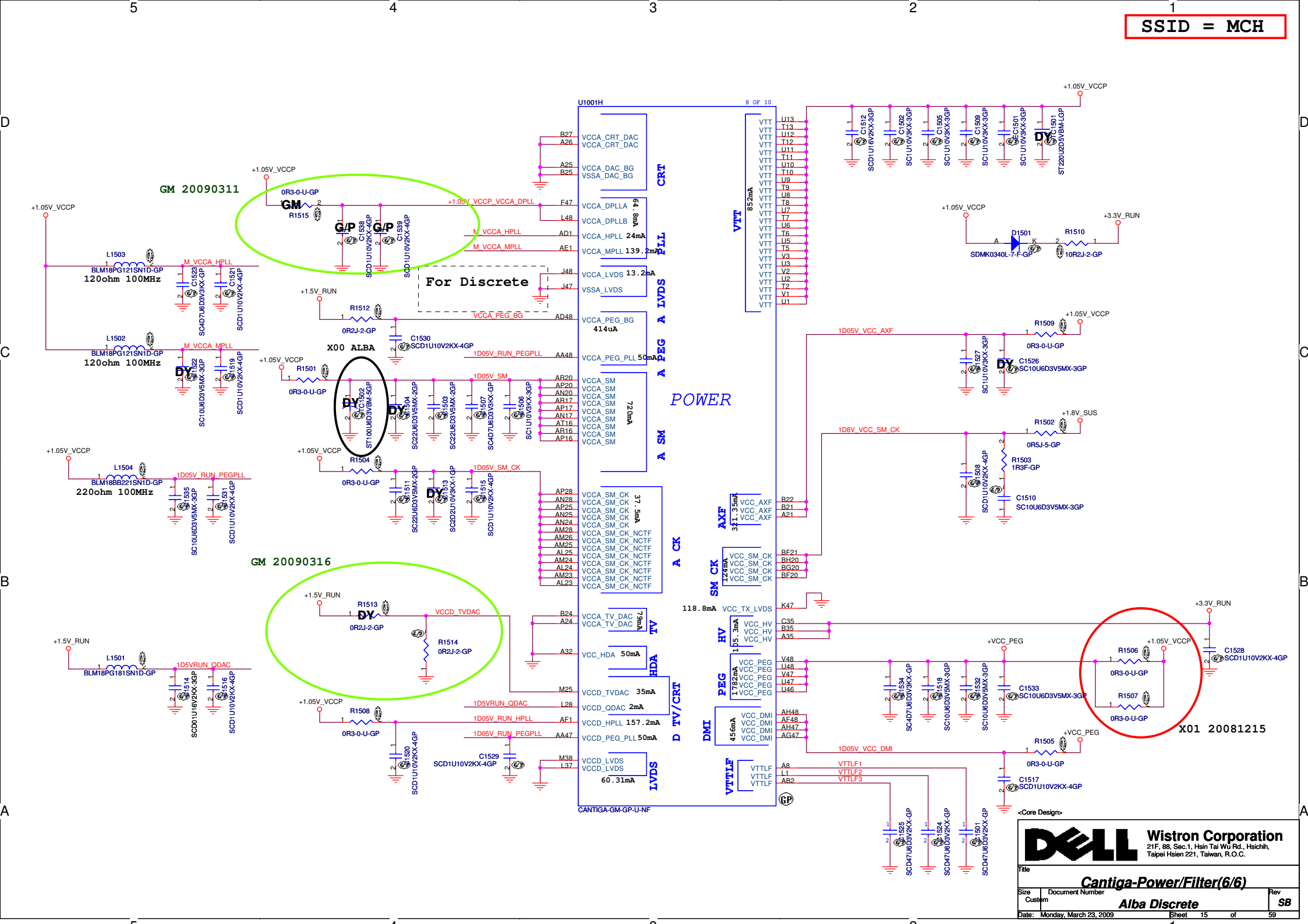
SSID = MCH

Supply	Signal Group	Imax
+1.05V_VCCP	VCC	3060mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-Power(5/6)
Size: Custom | Document Number: Alba Discrete | Rev: SB
Date: Monday, March 23, 2009 | Sheet 14 of 59

SSID = MCH


GM 20090311
GM 20090316
For Discrete
X00 ALBA
X01 20081215
POWER
U1001H
CANTIGA-GM-GP-U-NF
CRT
PLL
LVDS
PEG
SM
CK
TV
HDA
DMI
VTTLF
AXF
SM_CK
HV
VTT
+1.05V_VCCP
+1.5V_RUN
+3.3V_RUN
+1.8V_SUS
+VCC_PEG
1D05V_VCC_AXF
1D8V_VCC_SM_CK
1D05V_VCC_DMI
L1503 BLM18PG121SN1D-GP 120ohm 100MHz
L1502 BLM18PG121SN1D-GP 120ohm 100MHz
L1504 BLM18BB221SN1D-GP 220ohm 100MHz
L1501 BLM18PG181SN1D-GP
D1501 SDMK0340L-7-F-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Cantiga-Power/Filter(6/6)
Size Custom
Document Number
Alba Discrete
Rev SB
Date: Monday, March 23, 2009
Sheet 15 of 59

SSID = MEMORY

12 M_A_DQS#[7..0]
12 M_A_DQ[63..0]
12 M_A_DM[7..0]
12 M_A_DQS[7..0]
12 M_A_A[14..0]

DM1

M_A_A0 102 A0
M_A_A1 101 A1
M_A_A2 100 A2
M_A_A3 99 A3
M_A_A4 98 A4
M_A_A5 97 A5
M_A_A6 94 A6
M_A_A7 92 A7
M_A_A8 93 A8
M_A_A9 91 A9
M_A_A10 105 A10/AP
M_A_A11 90 A11
M_A_A12 89 A12
M_A_A13 116 A13
M_A_A14 86 A14
84 A15
12 M_A_BS#2 M_A_BS#2 85 A16/BA2
12 M_A_BS#0 M_A_BS#0 107 BA0
12 M_A_BS#1 M_A_BS#1 106 BA1

M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 17 DQ2
M_A_DQ3 19 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 14 DQ6
M_A_DQ7 16 DQ7
M_A_DQ8 23 DQ8
M_A_DQ9 25 DQ9
M_A_DQ10 35 DQ10
M_A_DQ11 37 DQ11
M_A_DQ12 20 DQ12
M_A_DQ13 22 DQ13
M_A_DQ14 36 DQ14
M_A_DQ15 38 DQ15
M_A_DQ16 43 DQ16
M_A_DQ17 45 DQ17
M_A_DQ18 55 DQ18
M_A_DQ19 57 DQ19
M_A_DQ20 44 DQ20
M_A_DQ21 46 DQ21
M_A_DQ22 56 DQ22
M_A_DQ23 58 DQ23
M_A_DQ24 61 DQ24
M_A_DQ25 63 DQ25
M_A_DQ26 73 DQ26
M_A_DQ27 75 DQ27
M_A_DQ28 62 DQ28
M_A_DQ29 64 DQ29
M_A_DQ30 74 DQ30
M_A_DQ31 76 DQ31
M_A_DQ32 123 DQ32
M_A_DQ33 125 DQ33
M_A_DQ34 135 DQ34
M_A_DQ35 137 DQ35
M_A_DQ36 124 DQ36
M_A_DQ37 126 DQ37
M_A_DQ38 134 DQ38
M_A_DQ39 136 DQ39
M_A_DQ40 141 DQ40
M_A_DQ41 143 DQ41
M_A_DQ42 151 DQ42
M_A_DQ43 153 DQ43
M_A_DQ44 140 DQ44
M_A_DQ45 142 DQ45
M_A_DQ46 152 DQ46
M_A_DQ47 154 DQ47
M_A_DQ48 157 DQ48
M_A_DQ49 159 DQ49
M_A_DQ50 173 DQ50
M_A_DQ51 175 DQ51
M_A_DQ52 158 DQ52
M_A_DQ53 160 DQ53
M_A_DQ54 174 DQ54
M_A_DQ55 176 DQ55
M_A_DQ56 179 DQ56
M_A_DQ57 181 DQ57
M_A_DQ58 189 DQ58
M_A_DQ59 191 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63

M_A_DQS#0 11 /DQS0
M_A_DQS#1 29 /DQS1
M_A_DQS#2 49 /DQS2
M_A_DQS#3 68 /DQS3
M_A_DQS#4 129 /DQS4
M_A_DQS#5 146 /DQS5
M_A_DQS#6 167 /DQS6
M_A_DQS#7 186 /DQS7

M_A_DQS0 13 DQS0
M_A_DQS1 31 DQS1
M_A_DQS2 51 DQS2
M_A_DQS3 70 DQS3
M_A_DQS4 131 DQS4
M_A_DQS5 148 DQS5
M_A_DQS6 169 DQS6
M_A_DQS7 188 DQS7

11 M_ODT0 M_ODT0 114 ODT0
11 M_ODT1 M_ODT1 119 ODT1

1 VREF
2 VSS
202 GND

/RAS 108
/WE 109
/CAS 113
M_A_RAS# 12
M_A_WE# 12
M_A_CAS# 12

/CS0 110
/CS1 115
M_CS0# 11
M_CS1# 11

CKE0 79
CKE1 80
M_CKE0 11
M_CKE1 11

CK0 30
/CK0 32
M_CLK_DDR0 11
M_CLK_DDR#0 11

CK1 164
/CK1 166
M_CLK_DDR1 11
M_CLK_DDR#1 11

DM0 10
DM1 26
DM2 52
DM3 67
DM4 130
DM5 147
DM6 170
DM7 185
M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7

SDA 195
SCL 197
ICH_SMBDATA
ICH_SMBCLK
ICH_SMBDATA 7,17,20,43
ICH_SMBCLK 7,17,20,43

VDDSPD 199

SA0 198
SA1 200

ALBA X00

NC#50 50
NC#69 69
NC#83 83
NC#120 120
NC#163/TEST 163
PM_EXTTS#0 11

+1.8V_SUS

VDD 81 82 87 88 95 96 103 104 111 112 117 118

VSS 3 8 9 12 15 18 21 24 27 28 33 34 39 40 41 42 47 48 53 54 59 60 65 66 71 72 77 78 121 122 127 128 132 133 138 139 144 145 149 150 155 156 161 162 165 168 171 172 177 178 183 184 187 190 193 196 201

DDR2-200P-10-U1
62.10017.881

Height 6.5mm

+V_DDR_MCH_REF
C1626 SCD1U16V2KX-3GP
DY C1625 SC2D2U10V3KX-1GP

+3.3V_RUN
C1602 SCD1U16V2KX-3GP
DY C1601 SC2D2U10V3KX-1GP

put near connector
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
C1603 DUMMY-C2
C1604 DUMMY-C2
C1623 DUMMY-C2
C1624 DUMMY-C2

Layout Note:
Place near DM1
+1.8V_SUS
C1620 SC1U10V3KX-3GP
C1619 SC1U10V3KX-3GP
DY C1622 SC2D2U10V3KX-1GP
DY C1621 SC2D2U10V3KX-1GP
C1616 SC1U10V3KX-3GP
DY C1607 SCD1U16V2KX-3GP
C1613 SCD1U10V2KX-4GP
C1609 SC1U603V2KX-GP
C1612 SCD1U10V2KX-4GP
DY C1601 ST220U2D5VBM-LGP

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT.
+0.9V_DDR_VTT
DY C1610 SCD1U16V2KX-3GP
C1627 SCD1U16V2KX-3GP
DY C1611 SCD1U16V2KX-3GP
C1608 SCD1U16V2KX-3GP
DY C1605 SCD1U16V2KX-3GP
DY C1630 SCD1U16V2KX-3GP
C1606 SCD1U16V2KX-3GP
DY C1614 SCD1U16V2KX-3GP
DY C1617 SCD1U16V2KX-3GP
C1618 SCD1U16V2KX-3GP
C1615 SCD1U16V2KX-3GP
C1629 SCD1U16V2KX-3GP
C1628 SCD1U16V2KX-3GP

Layout Note:
Place these resistors close to DM1,
all trace length Max=1.5".
+0.9V_DDR_VTT
RN1601 SRN56J-5-GP
M_A_A5 M_A_A8 M_A_A9 M_A_A12
RN1605 SRN56J-4-GP
M_CKE0 M_A_BS#2
R1663 56R2J-4-GP
M_A_A13
RN1602 SRN56J-5-GP
M_ODT0 M_CS0# M_A_BS#1 M_A_RAS#
RN1606 SRN56J-5-GP
M_A_A3 M_A_A1 M_A_A10 M_A_BS#0
RN1603 SRN56J-5-GP
M_ODT1 M_CS1# M_A_CAS# M_A_WE#
RN1607 SRN56J-5-GP
M_A_A7 M_A_A11 M_A_A14 M_CKE1
RN1604 SRN56J-5-GP
M_A_A0 M_A_A2 M_A_A4 M_A_A6

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT1
Size: Custom
Document Number: Alba Discrete
Rev: SB
Date: Monday, March 23, 2009
Sheet 16 of 59

SSID = MEMORY

12 M_B_DQS#[7..0]
12 M_B_DQ[63..0]
12 M_B_DM[7..0]
12 M_B_DQS[7..0]
12 M_B_A[14..0]

Layout Note:
Place near DM2

+1.8V_SUS

C1716 SC1U10V3KX-3GP
C1707 SC2D2U10V3KX-1GP
C1712 SC1U10V3KX-3GP
C1711 SC1U10V3KX-3GP
C1710 SC1U10V3KX-3GP
C1714 SCD1U10V2KX-4GP
C1717 SCD1U16V2KX-3GP
C1709 SC1U6D3V2KX-GP
C1715 SC1U6D3V2KX-GP
C1701 ST220U2D5V8M-LGP

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT.

+0.9V_DDR_VTT

C1729 C1726 C1728 C1727 C1725 C1723 C1722 C1706 C1724 C1713 C1705 C1721 C1708
SCD1U16V2KX-3GP

DM2

M_B_A0 102
M_B_A1 101
M_B_A2 100
M_B_A3 99
M_B_A4 98
M_B_A5 97
M_B_A6 94
M_B_A7 92
M_B_A8 93
M_B_A9 91
M_B_A10 105
M_B_A11 90
M_B_A12 89
M_B_A13 116
M_B_A14 86
M_B_BS#2 84 (12 M_B_BS#2)
M_B_BS#0 107 (12 M_B_BS#0)
M_B_BS#1 106 (12 M_B_BS#1)

M_B_DQ0 5
M_B_DQ1 7
M_B_DQ2 17
M_B_DQ3 19
M_B_DQ4 4
M_B_DQ5 6
M_B_DQ6 14
M_B_DQ7 16
M_B_DQ8 23
M_B_DQ9 25
M_B_DQ10 35
M_B_DQ11 37
M_B_DQ12 20
M_B_DQ13 22
M_B_DQ14 36
M_B_DQ15 38
M_B_DQ16 43
M_B_DQ17 45
M_B_DQ18 55
M_B_DQ19 57
M_B_DQ20 44
M_B_DQ21 46
M_B_DQ22 56
M_B_DQ23 58
M_B_DQ24 61
M_B_DQ25 63
M_B_DQ26 73
M_B_DQ27 75
M_B_DQ28 62
M_B_DQ29 64
M_B_DQ30 74
M_B_DQ31 76
M_B_DQ32 123
M_B_DQ33 125
M_B_DQ34 135
M_B_DQ35 137
M_B_DQ36 124
M_B_DQ37 126
M_B_DQ38 134
M_B_DQ39 136
M_B_DQ40 141
M_B_DQ41 143
M_B_DQ42 151
M_B_DQ43 153
M_B_DQ44 140
M_B_DQ45 142
M_B_DQ46 152
M_B_DQ47 154
M_B_DQ48 157
M_B_DQ49 159
M_B_DQ50 173
M_B_DQ51 175
M_B_DQ52 158
M_B_DQ53 160
M_B_DQ54 174
M_B_DQ55 176
M_B_DQ56 179
M_B_DQ57 181
M_B_DQ58 189
M_B_DQ59 191
M_B_DQ60 180
M_B_DQ61 182
M_B_DQ62 192
M_B_DQ63 194

M_B_DQS#0 11
M_B_DQS#1 29
M_B_DQS#2 49
M_B_DQS#3 68
M_B_DQS#4 129
M_B_DQS#5 146
M_B_DQS#6 167
M_B_DQS#7 186

M_B_DQS0 13
M_B_DQS1 31
M_B_DQS2 51
M_B_DQS3 70
M_B_DQS4 131
M_B_DQS5 148
M_B_DQS6 169
M_B_DQS7 188

M_ODT2 114 (11 M_ODT2)
M_ODT3 119 (11 M_ODT3)

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2
BA0 BA1
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
DQS0# DQS1# DQS2# DQS3# DQS4# DQS5# DQS6# DQS7#
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
ODT0 ODT1
VREF VSS
NP1 NP2
DDR2-200P-33-GP

Height 11mm

RAS# 108 (M_B_RAS# 12)
WE# 109 (M_B_WE# 12)
CAS# 113 (M_B_CAS# 12)
CS0# 110 (M_CS2# 11)
CS1# 115 (M_CS3# 11)
CKE0 79 (M_CKE2 11)
CKE1 80 (M_CKE3 11)
CK0 30 (M_CLK_DDR2)
CK0# 32 (M_CLK_DDR#2)
CK1 164 (M_CLK_DDR3)
CK1# 166 (M_CLK_DDR#3)
DM0 10 (M_B_DM0)
DM1 26 (M_B_DM1)
DM2 52 (M_B_DM2)
DM3 67 (M_B_DM3)
DM4 130 (M_B_DM4)
DM5 147 (M_B_DM5)
DM6 170 (M_B_DM6)
DM7 185 (M_B_DM7)
SDA 195 (ICH_SMBDATA)
SCL 197 (ICH_SMBCLK)
VDDSPD 199
SA0 198
SA1 200
NC#50 50 (PM_EXTTS#1 11)
NC#69 69
NC#83 83
NC#120 120
NC#163/TEST 163

ICH_SMBDATA 7,16,20,43
ICH_SMBCLK 7,16,20,43

ALBA X00

+3.3V_RUN

C1701 SCD1U16V2KX-3GP
C1702 SC2D2U10V3KX-1GP

VDD 81 82 87 88 95 96 103 104 111 112 117 118
VSS 3 8 9 12 15 18 21 24 27 28 33 34 39 40 41 42 47 48 53 54 59 60 65 66 71 72 77 78 121 122 127 128 132 133 138 139 144 145 149 150 155 156 161 162 165 168 171 172 177 178 183 184 187 190 193 196
GND 201 202

+1.8V_SUS

+V_DDR_MCH_REF

C1730 SCD1U16V2KX-3GP
C1720 SC2D2U10V3KX-1GP

put near connector

M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3

C1703 C1704 C1718 C1719 DUMMY-C2

Layout Note:
Place these resistors close to DM2, all trace length Max=1.5".

+0.9V_DDR_VTT

RN1701 SRN56J-3-GP
M_B_A8 M_B_A5 M_B_A1 M_B_A3

RN1704 SRN56J-3-GP
M_CKE3 M_B_A14 M_B_A11 M_B_A6

RN1702 SRN56J-3-GP
M_ODT3 M_CS3# M_B_A0

RN1705 SRN56J-3-GP
M_B_A7 M_B_A4 M_B_A2 M_B_BS#1

RN1703 SRN56J-3-GP
M_B_A10 M_B_BS#0 M_B_WE# M_B_CAS#

RN1706 SRN56J-3-GP
M_B_RAS# M_ODT2 M_CS2# M_B_A13

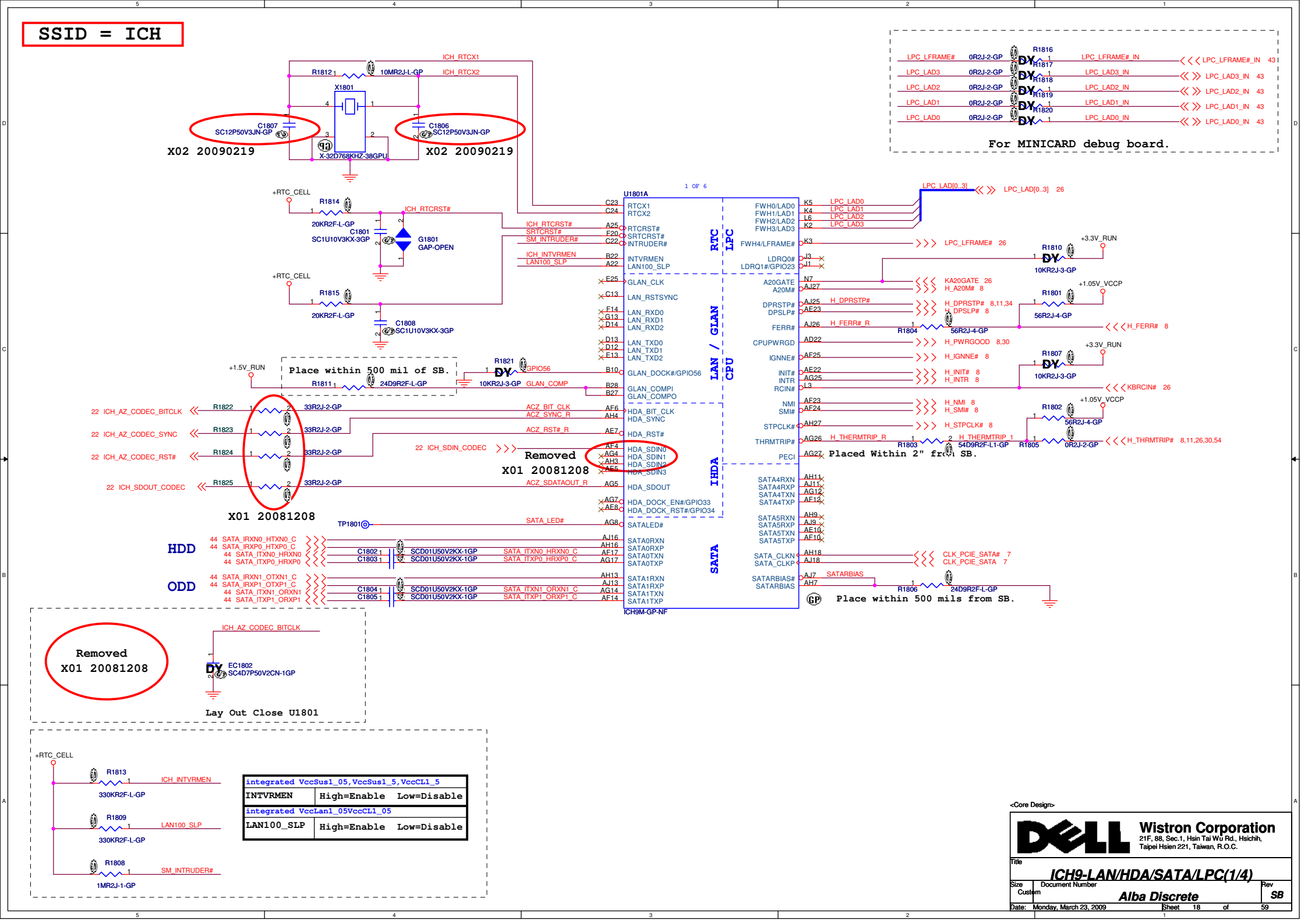
RN1707 SRN56J-3-GP
M_B_A12 M_B_BS#2 M_B_A9 M_CKE2

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT2
Size: Custom | Document Number: Alba Discrete | Rev: SB
Date: Monday, March 23, 2009 | Sheet 17 of 59

SSID = ICH



<Core Design>

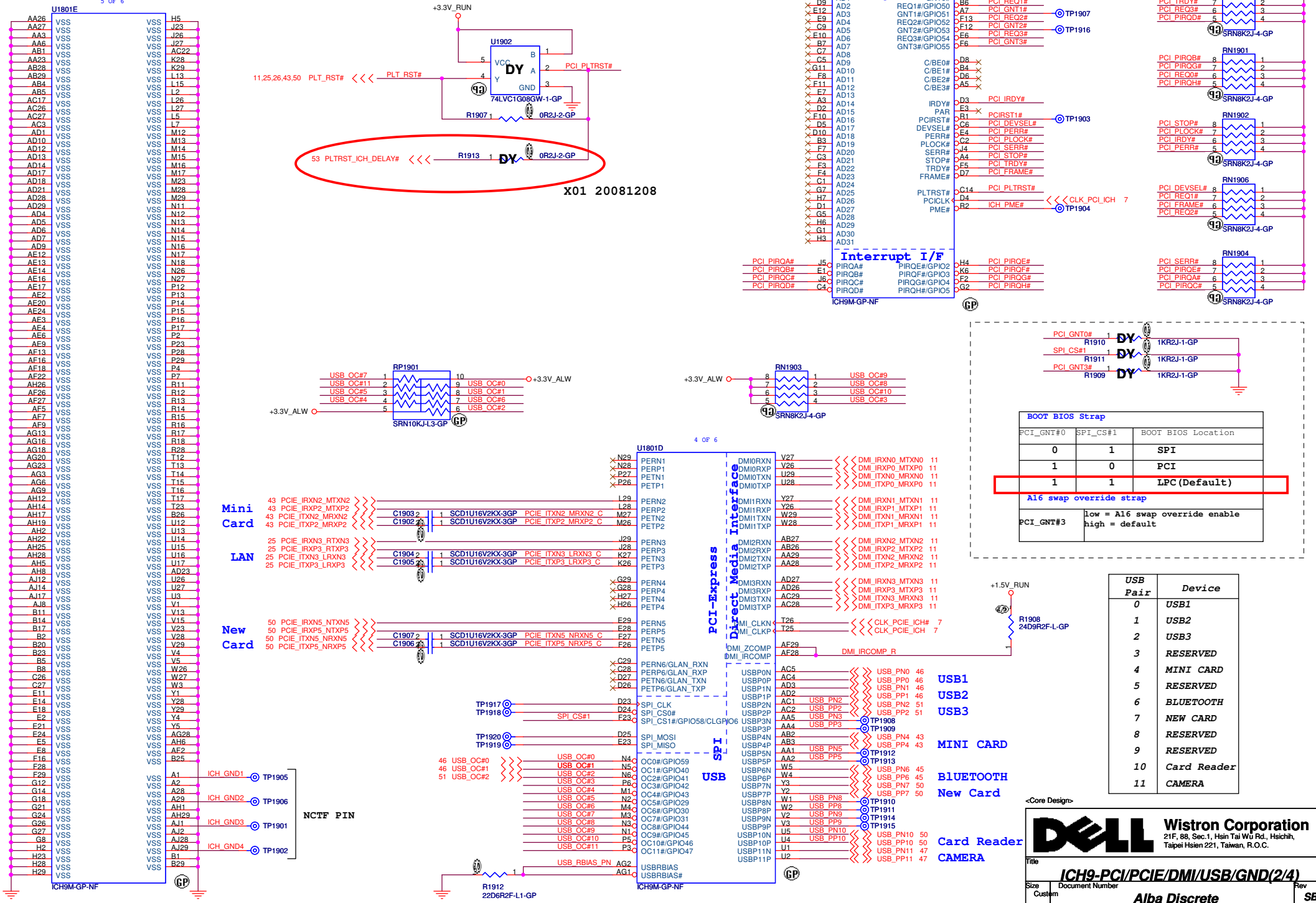
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-LAN/HDA/SATA/LPC(1/4)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 18 of 59

SSID = ICH



BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

USB Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

<Core Design>

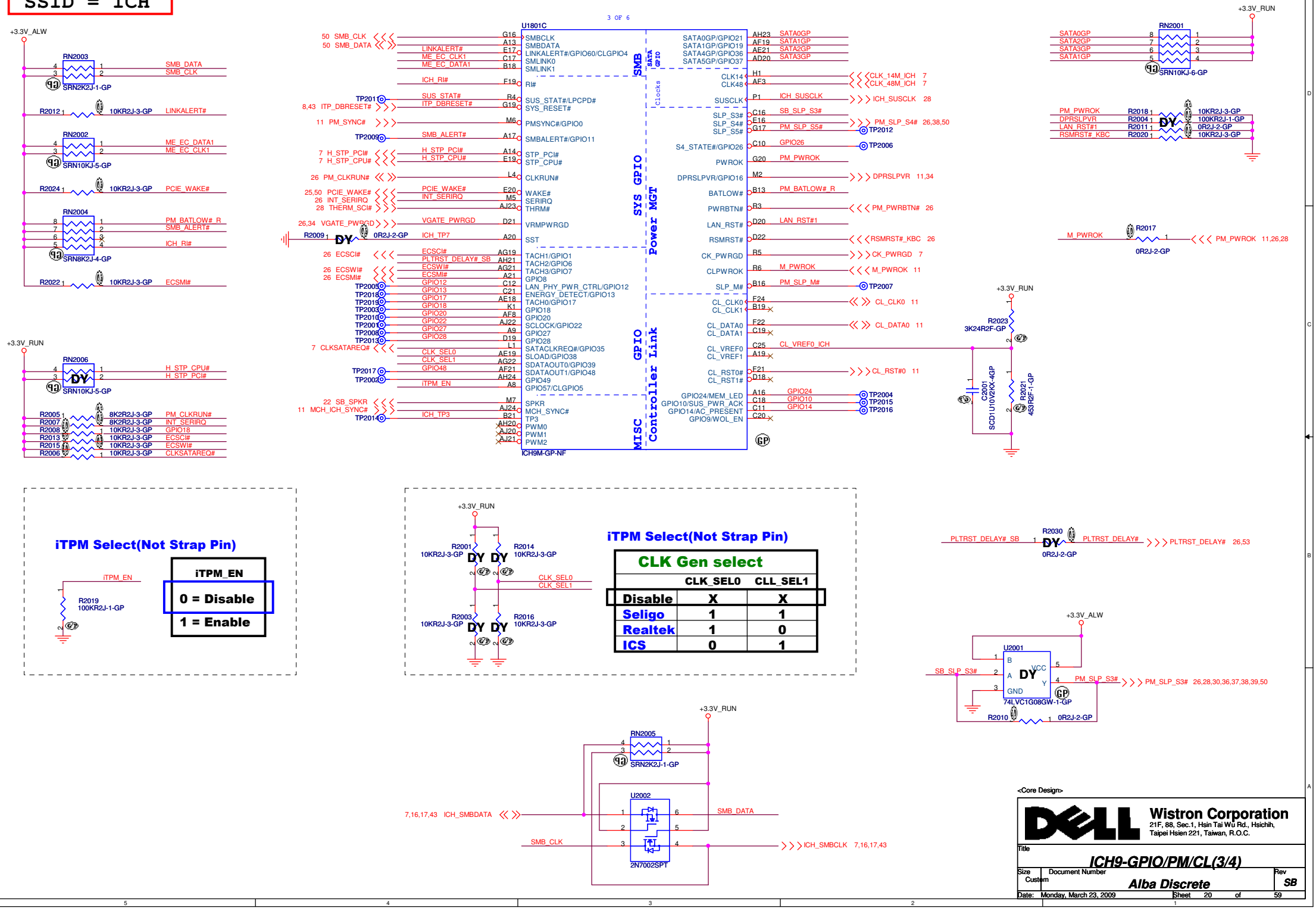
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-PCI/PCIE/DMI/USB/GND(2/4)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 19 of 59

SSID = ICH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

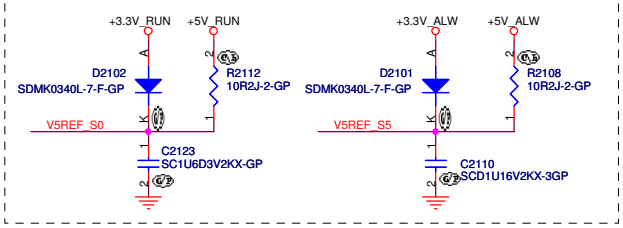
Title: ICH9-GPIO/PM/CL(3/4)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 20 of 59

SSID = ICH

**Within a given well, 5VREF needs to be up before the corresponding 3.3V rail*



<Core Design>

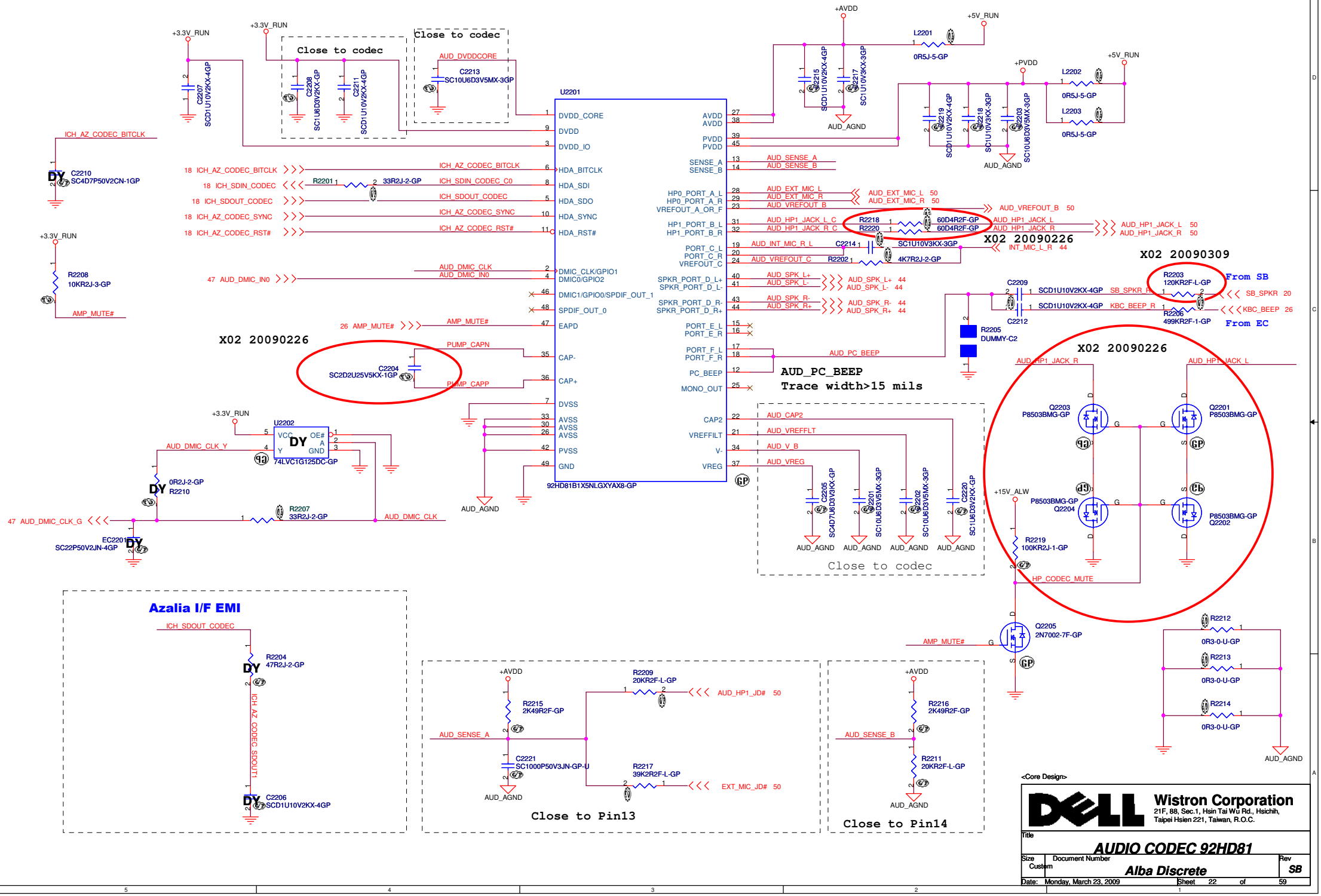
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-POWER(4/4)**

Size: Custom | Document Number: **Alba Discrete** | Rev: **SB**

Date: Monday, March 23, 2009 | Sheet 21 of 59

SSID = AUDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC 92HD81

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 22 of 59

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Alba Discrete*	*SB*

Date: Monday, March 23, 2009 Sheet 23 of 59

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

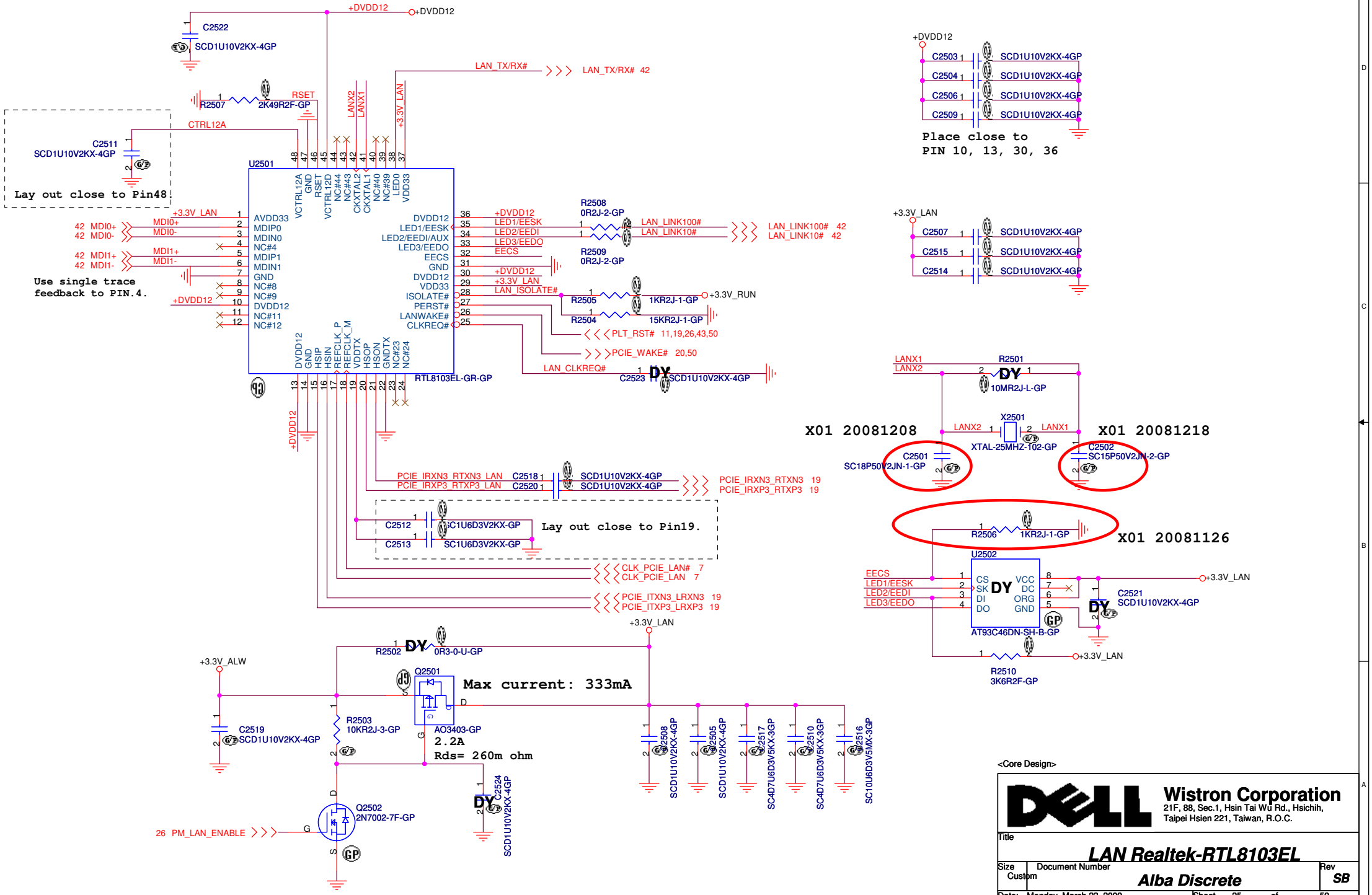
Title

(Reserve)

Size	Document Number	Rev
Custom	*Alba Discrete*	*SB*

Date: Monday, March 23, 2009 Sheet 24 of 59

SSID = LOM



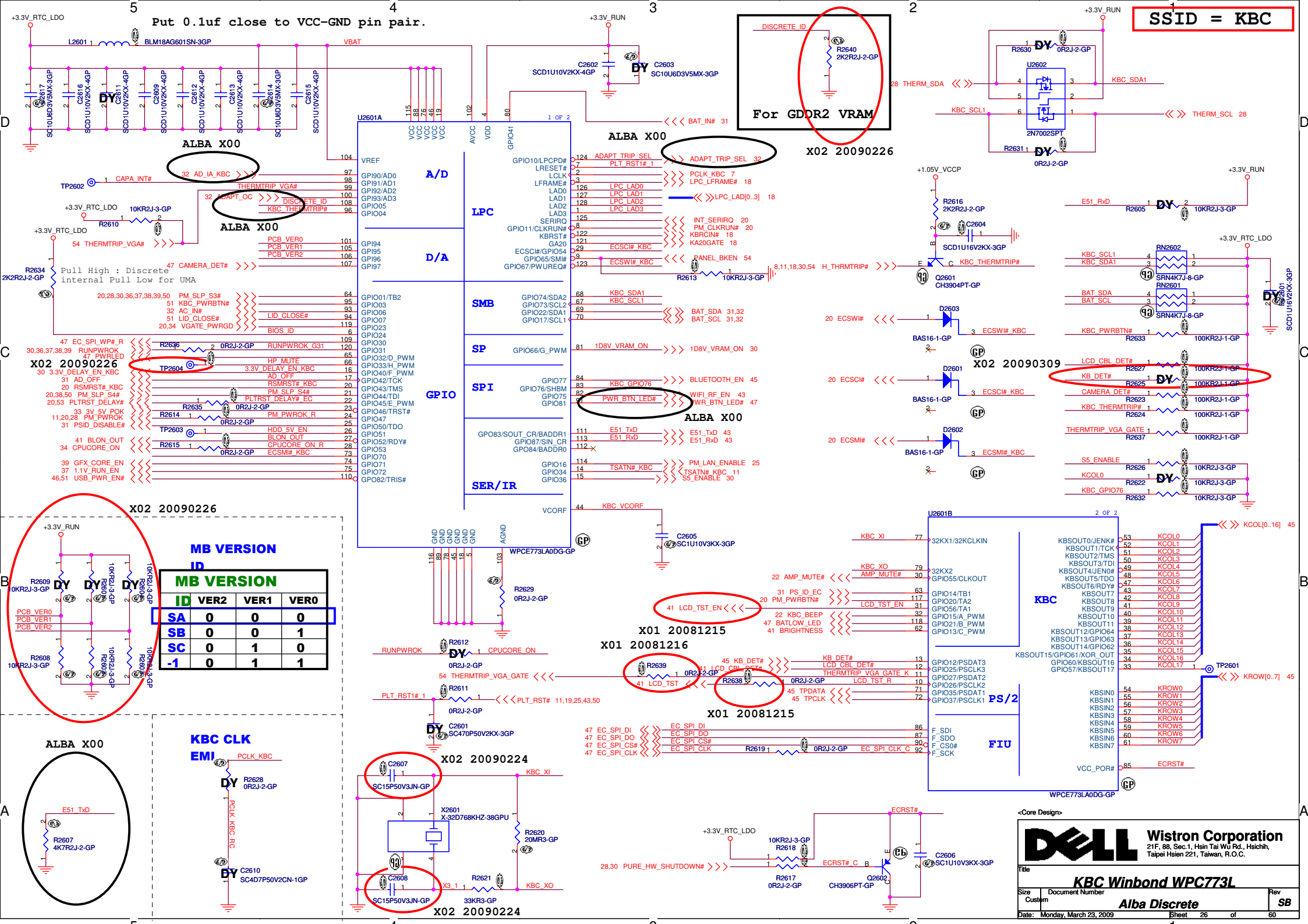
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Realtek-RTL8103EL**

Size	Document Number	Rev
Custom	Alba Discrete	SB

Date: Monday, March 23, 2009 Sheet 25 of 59


SSID = KBC
Put 0.1uf close to VCC-GND pin pair.
ALBA X00
X02 20090226
X02 20090309
X01 20081215
X01 20081216
X02 20090224
For GDDR2 VRAM
MB VERSION ID
MB VERSION
ID VER2 VER1 VER0
SA 0 0 0
SB 0 0 1
SC 0 1 0
-1 0 1 1
KBC CLK EMI
U2601A
U2601B
WPCE773LA0DG-GP
KBC
PS/2
FIU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC Winbond WPC773L
Alba Discrete
Monday, March 23, 2009

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserve)

Size	Document Number	Rev
Custom	*Alba Discrete*	*SB*

Date: Monday, March 23, 2009 Sheet 27 of 59

SSID = Thermal

X01 20081215

H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

GPU Sensor

Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.

3.HW T8 sensor

C2801 must be near Q2801

C2805 must be near EMC2102

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

EMC2102

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

ALBA X00

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)
T8 shutdown is set 88 deg-C.

32K suspend clock output

Lay out close to SKT2(CPU socket)

H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 28 of 59

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

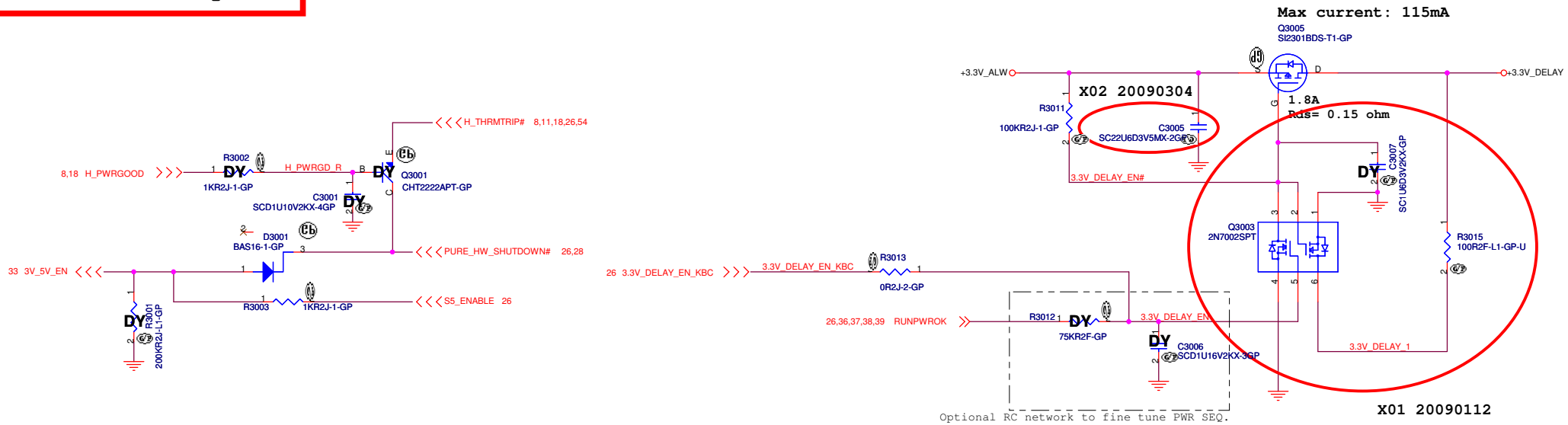
Title

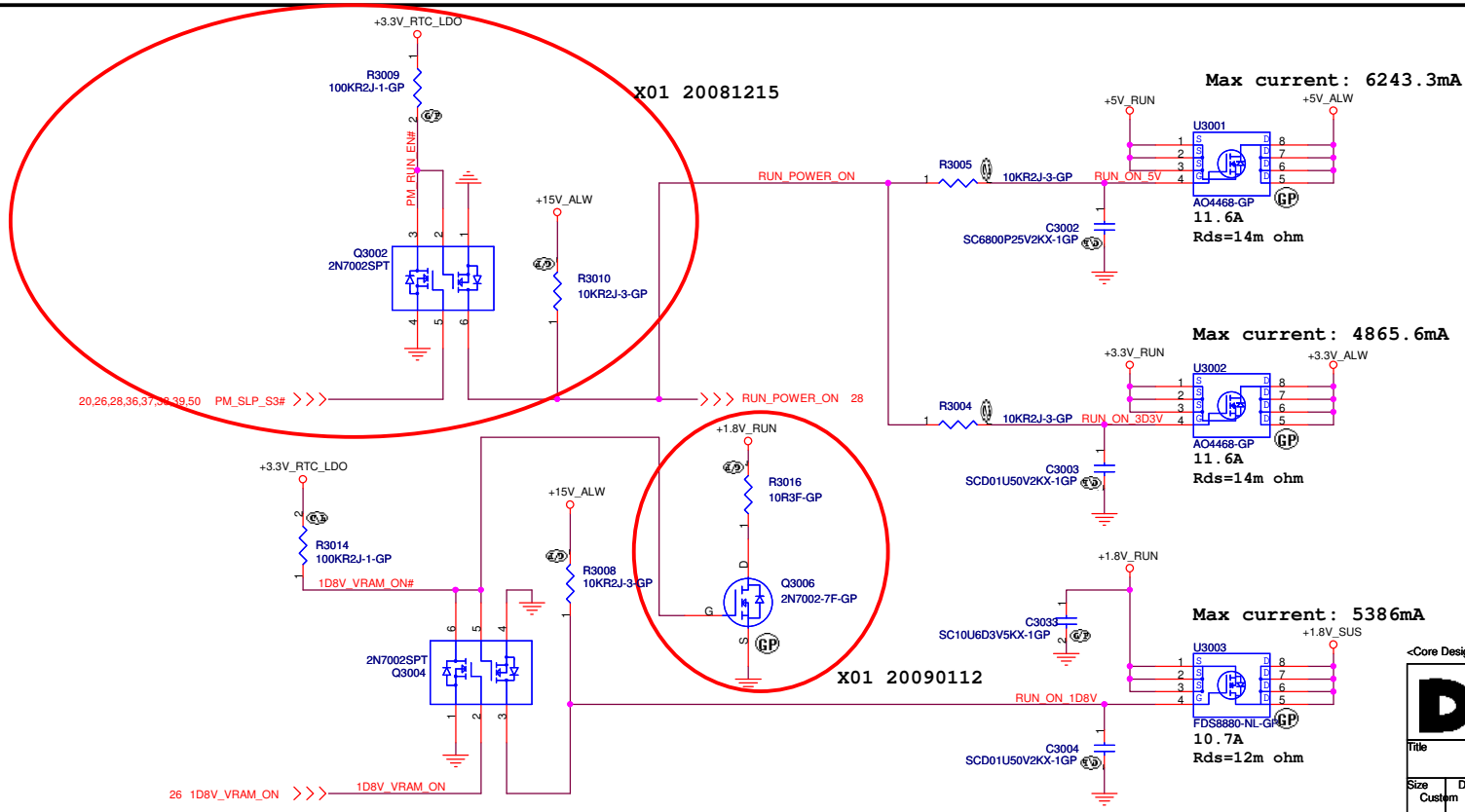
(Reserve)

Size	Document Number	Rev
Custom	*Alba Discrete*	*SB*

Date: Monday, March 23, 2009 Sheet 29 of 59

SSID = Reset.Suspend





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

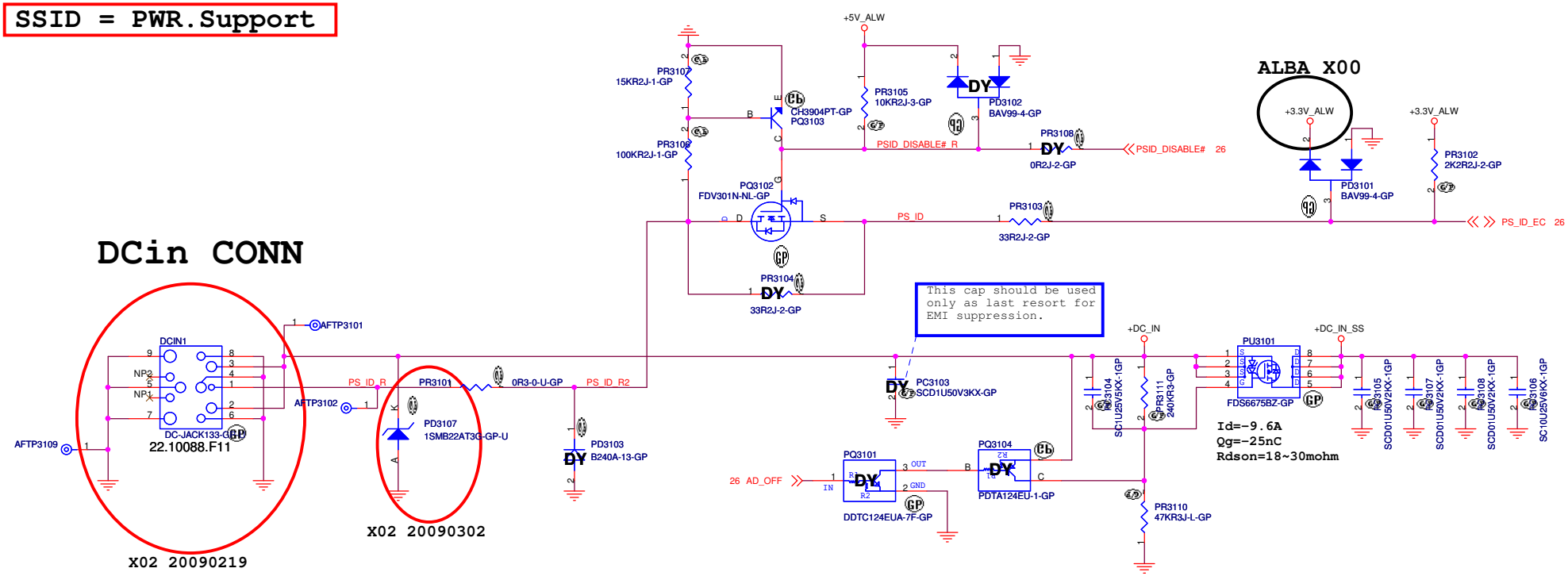
Title: *Power Plane Enable*

Size: Custom | Document Number: *Alba Discrete* | Rev: *SB*

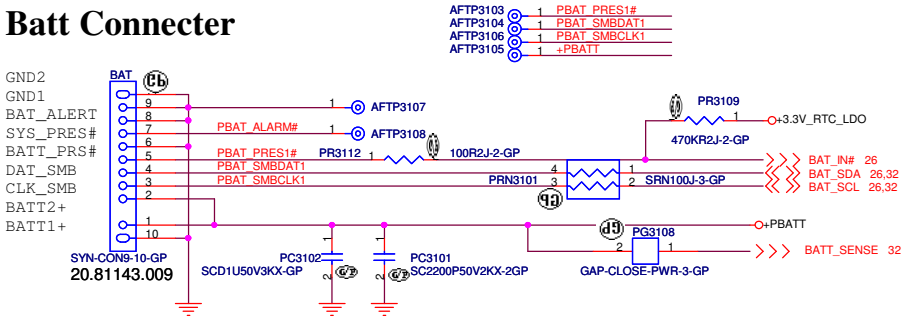
Date: Monday, March 23, 2009 | Sheet 30 of 59

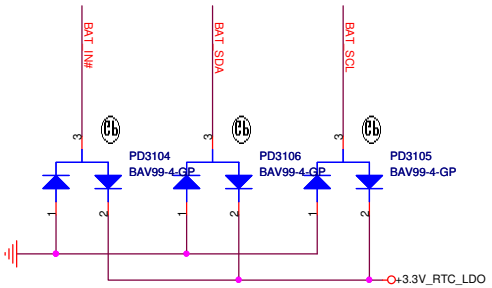
SSID = PWR.Support

DCin CONN



Batt Connecter





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC IN/BATT CONN/USB CONN

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 31 of 59

SSID = Charger

Adaptor In Soft-Start Circuit

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm

Layout Trace 250mil

Layout Trace 300mil

Layout Trace 300mil

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm

Layout Trace 300mil

X02 20090302

X02 20090302

X01 20081215

TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR3202	PR3205	PR3207	PR3208
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR6326 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor

ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor

Note 2: 24.9K at PR6326 allows the 65W adaptor setting to switch down to 45W. (now is 33.2K for 90W)

Note 3: PR6302 must be 5m ohm instead of 10m ohm for the 230W adaptor

ADAPT_TRIP_SEL=1 Adapter is 90w

ADAPT_TRIP_SEL=0 Adapter is 65w

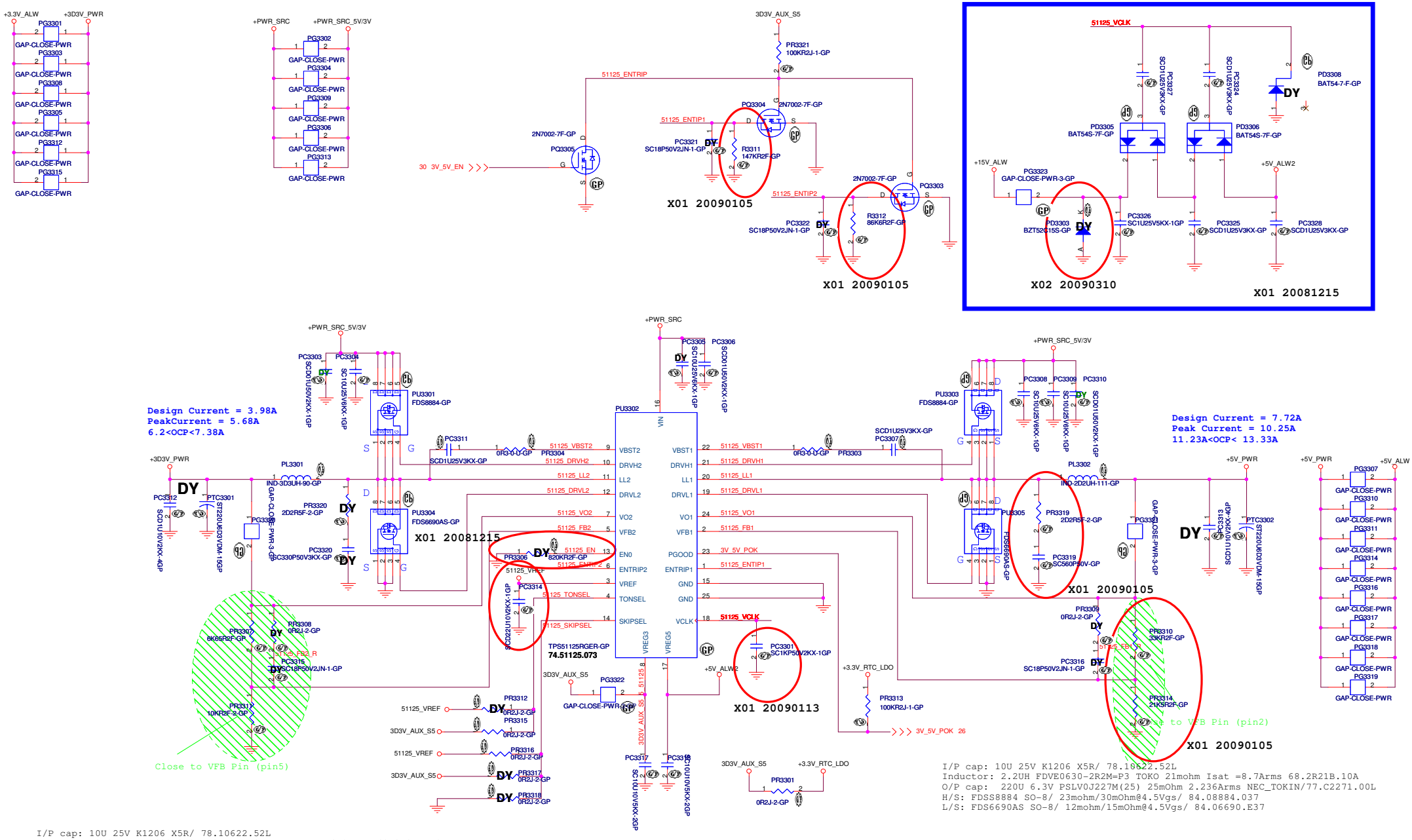
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER MAX8731

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 32 of 59



TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

Eiger

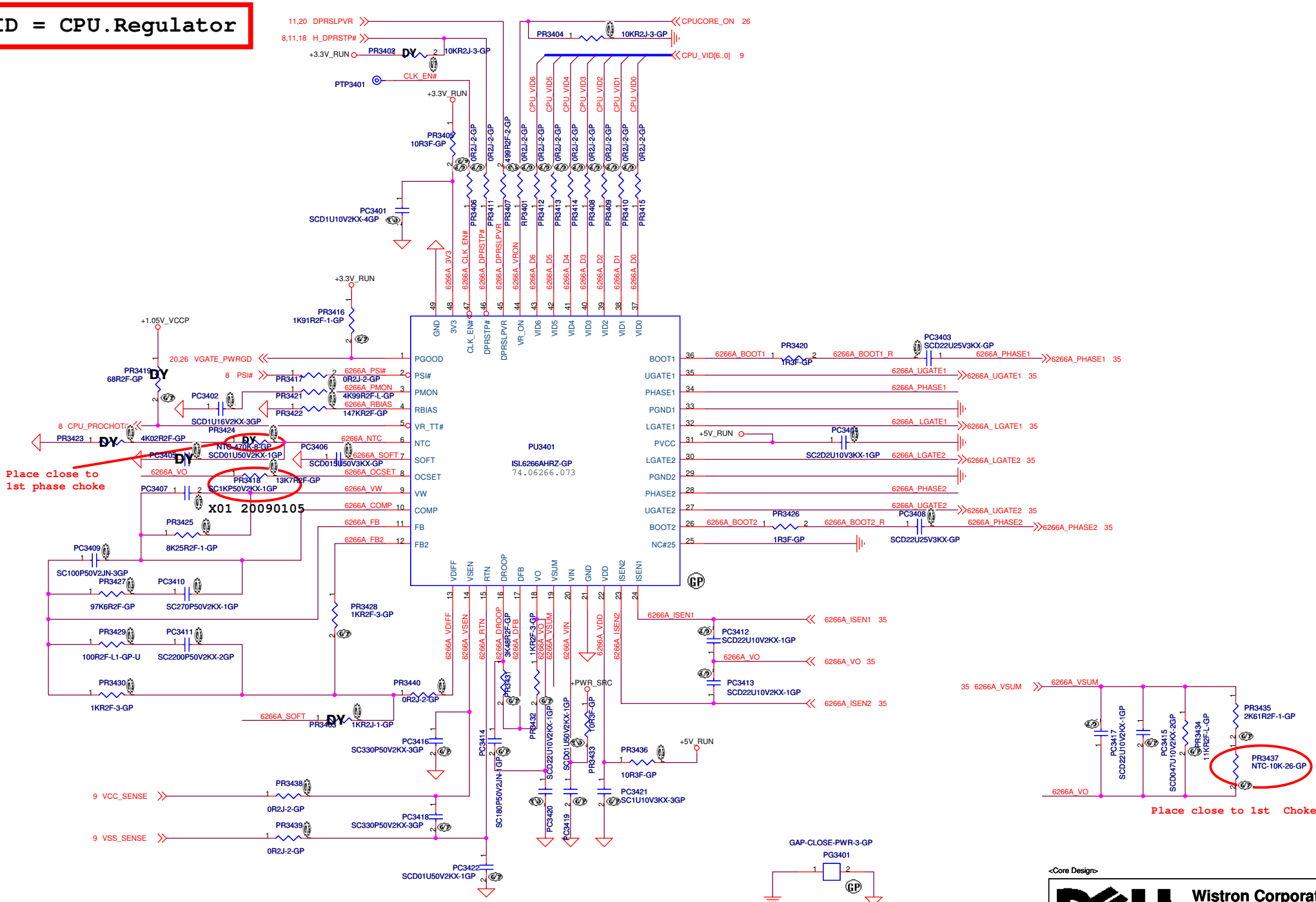
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 5V/3D3V (TPS51125)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 33 of 59

SSID = CPU.Regulator



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

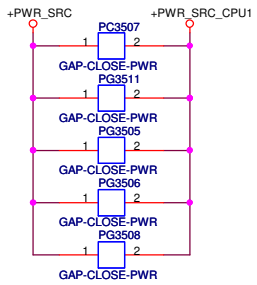
<Core Design>

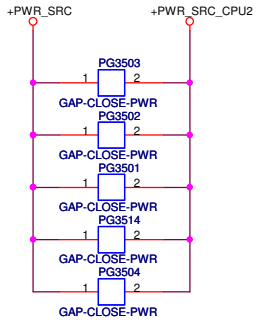
Title: CPU VCORE POWER(1/2)

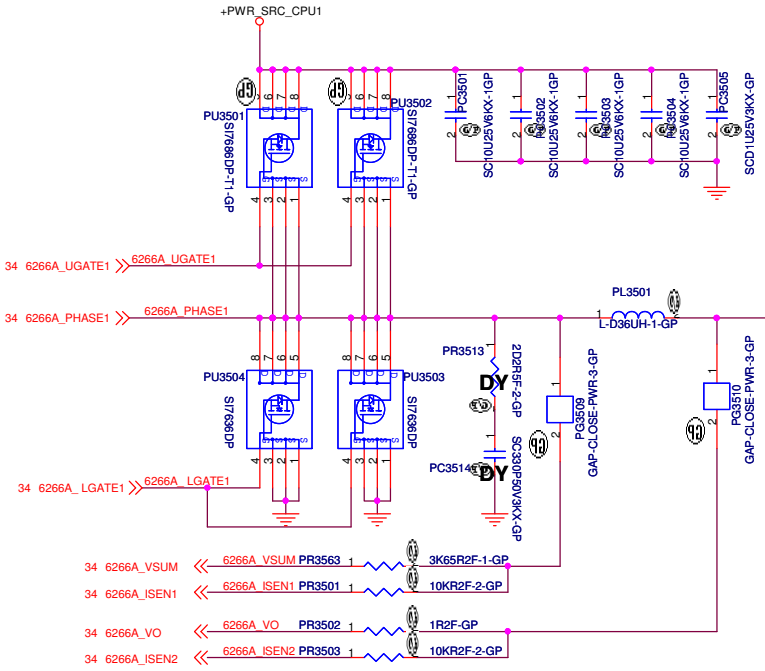
Size: Custom | Document Number: Alba Discrete | Rev: SB

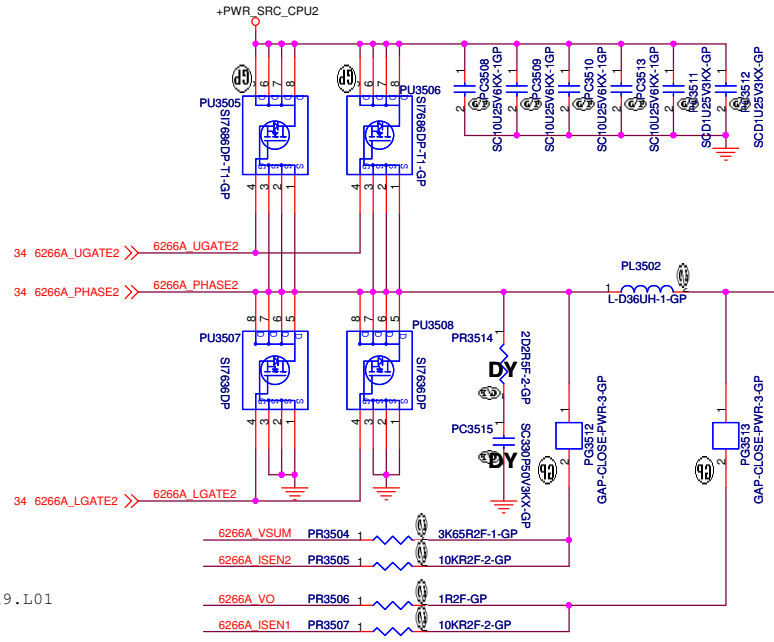
Date: Monday, March 23, 2009 | Sheet 34 of 59

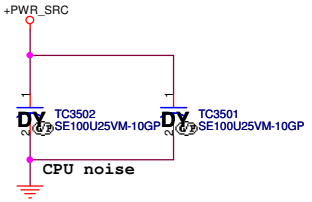
SSID = CPU.Regulator











Thermal Design Current = 34A(IMVP6+ Rev:1.35)
PeakCurrent = 47A
56.4<OCP<66A

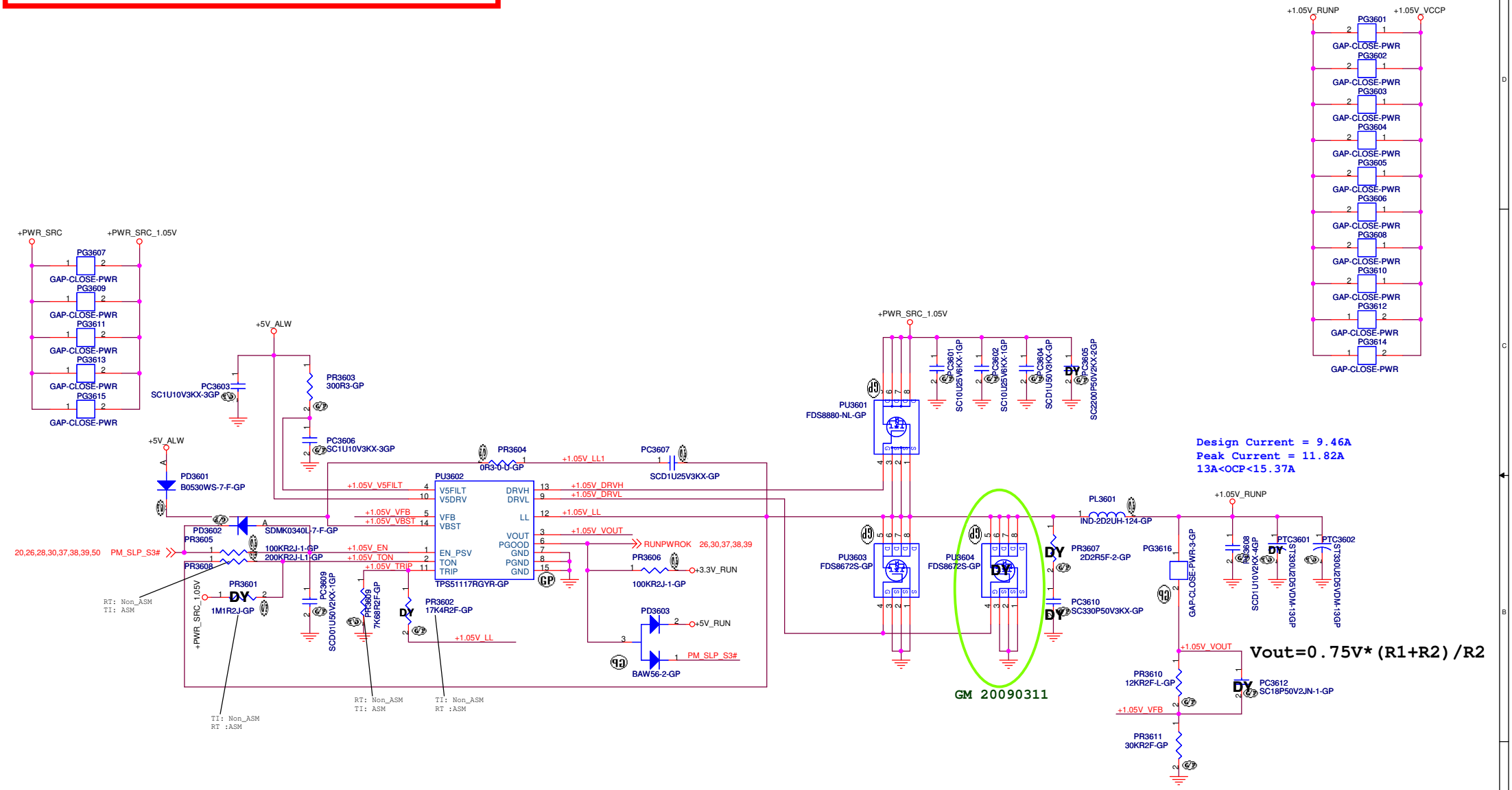
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: SI7686DP/ POWERPAK-8/ 14mOhm/ 4.5Vgs/ 84.07686.037
L/S: SI7636ADP/ POWERPAK-8/ 4.8mOhm/ 4.5Vgs/ 84.07636.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU VCORE POWER(2/2)
Size: Custom | Document Number: Alba Discrete | Rev: SB
Date: Monday, March 23, 2009 | Sheet 35 of 59

SSID = PWR.Plane.Regulator_1p05v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE1040-2R2M=P3 TOKO DCR:6.8mohm Isat =14.5Arms 68.2R21B.10M
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: FDS8880 SO-8/ 9.6mOhm/12mOhm @4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->350KHz

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.05V

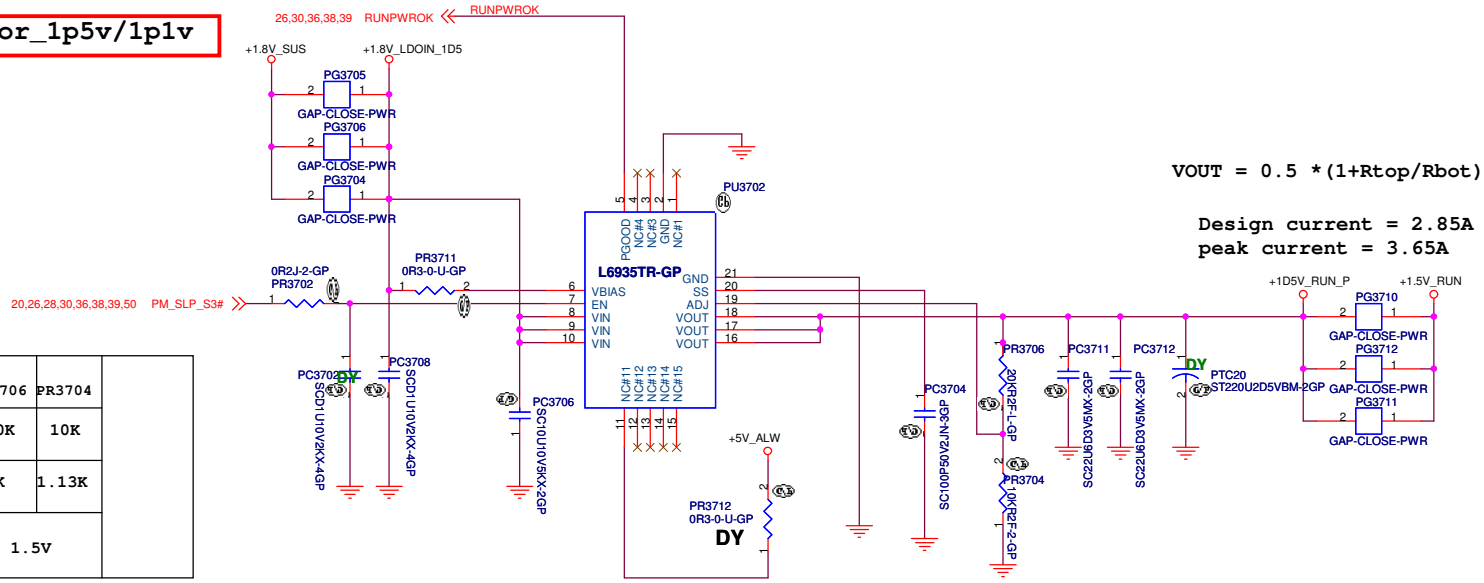
Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 36 of 59

SSID = PWR.Plane.Regulator_1p5v/1p1v

Vendor	PIN6	PIN11	PIN20
L6935	VBIAS	N.C.	SS
RTXX35	N.C.	VBIAS	N.C.

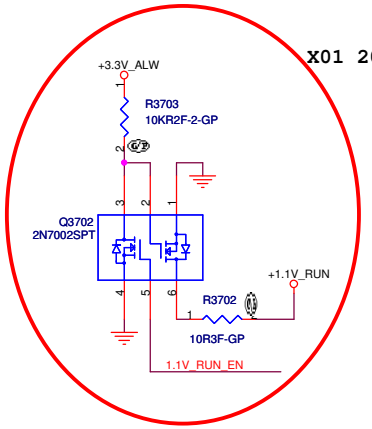
Vendor	PR3712	PR3711	PR3706	PR3704	
L6935	DY	ASM	20K	10K	
RTXX35	ASM	DY	1K	1.13K	
			1.5V		



VOUT = 0.5 *(1+Rtop/Rbot)

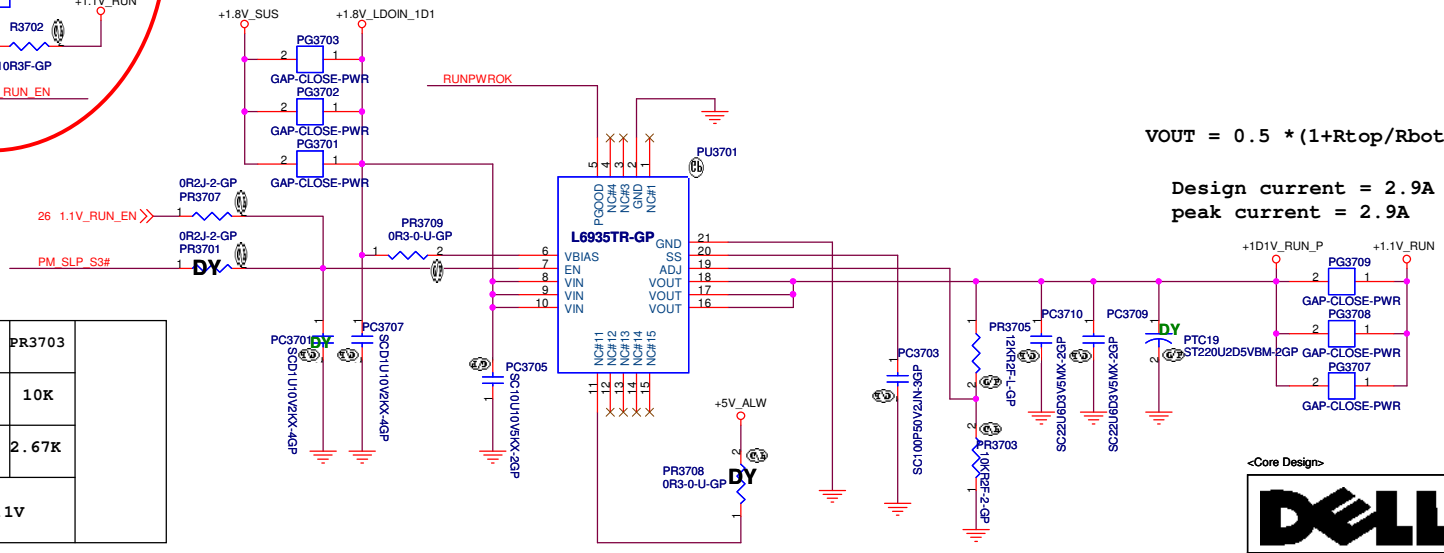
Design current = 2.85A
peak current = 3.65A

X01 20090112



Vendor	PIN6	PIN11	PIN20
L6935	VBIAS	N.C.	SS
RTXX35	N.C.	VBIAS	N.C.

Vendor	PR3708	PR3709	PR3705	PR3703	
L6935	DY	ASM	20K	10K	
RTXX35	ASM	DY	1.02K	2.67K	
			1.1V		



VOUT = 0.5 *(1+Rtop/Rbot)

Design current = 2.9A
peak current = 2.9A

<Core Design>

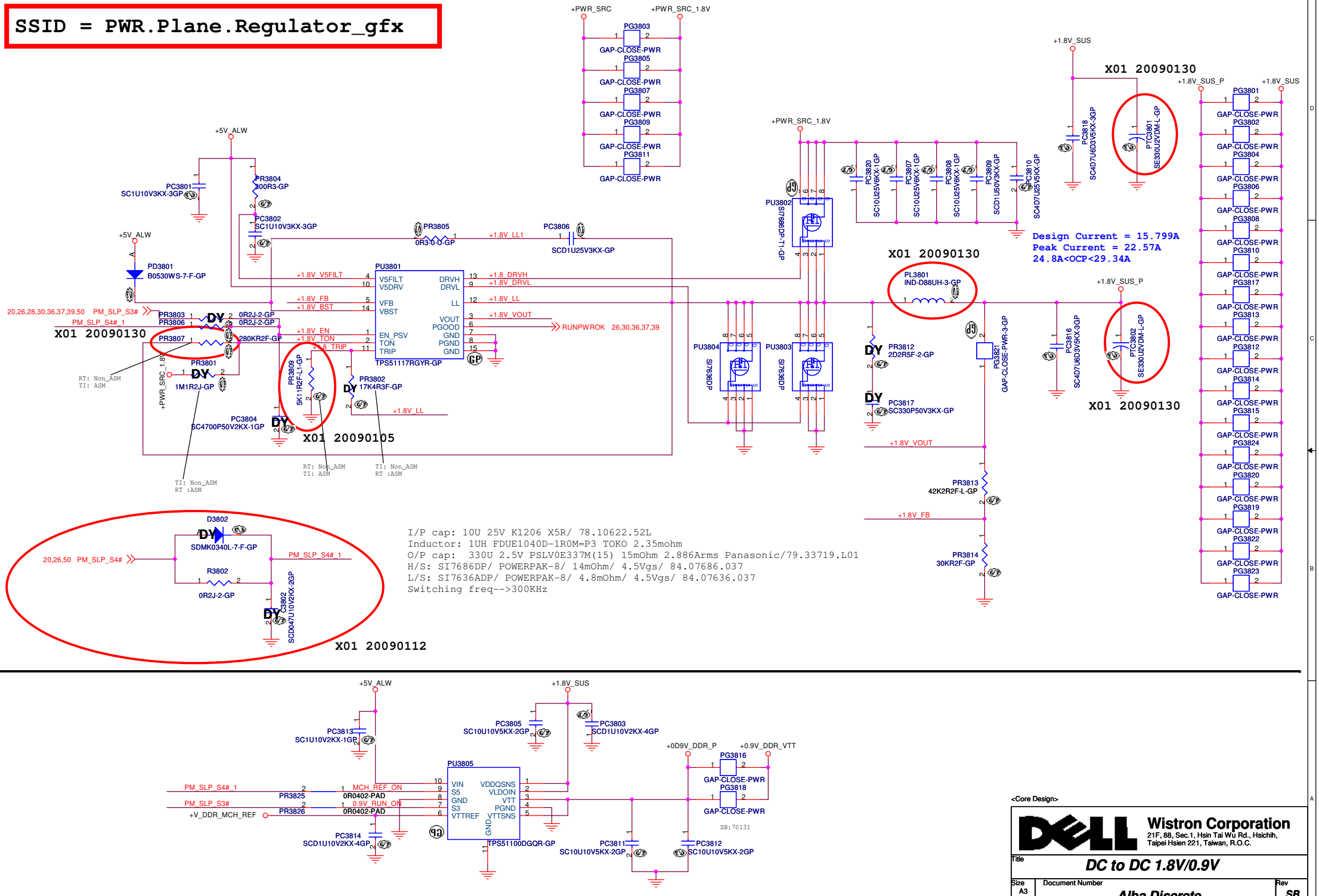
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC L6935_1.5V / L6935_1.1V

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 37 of 59

SSID = PWR.Plane.Regulator_gfx



<Core Design>

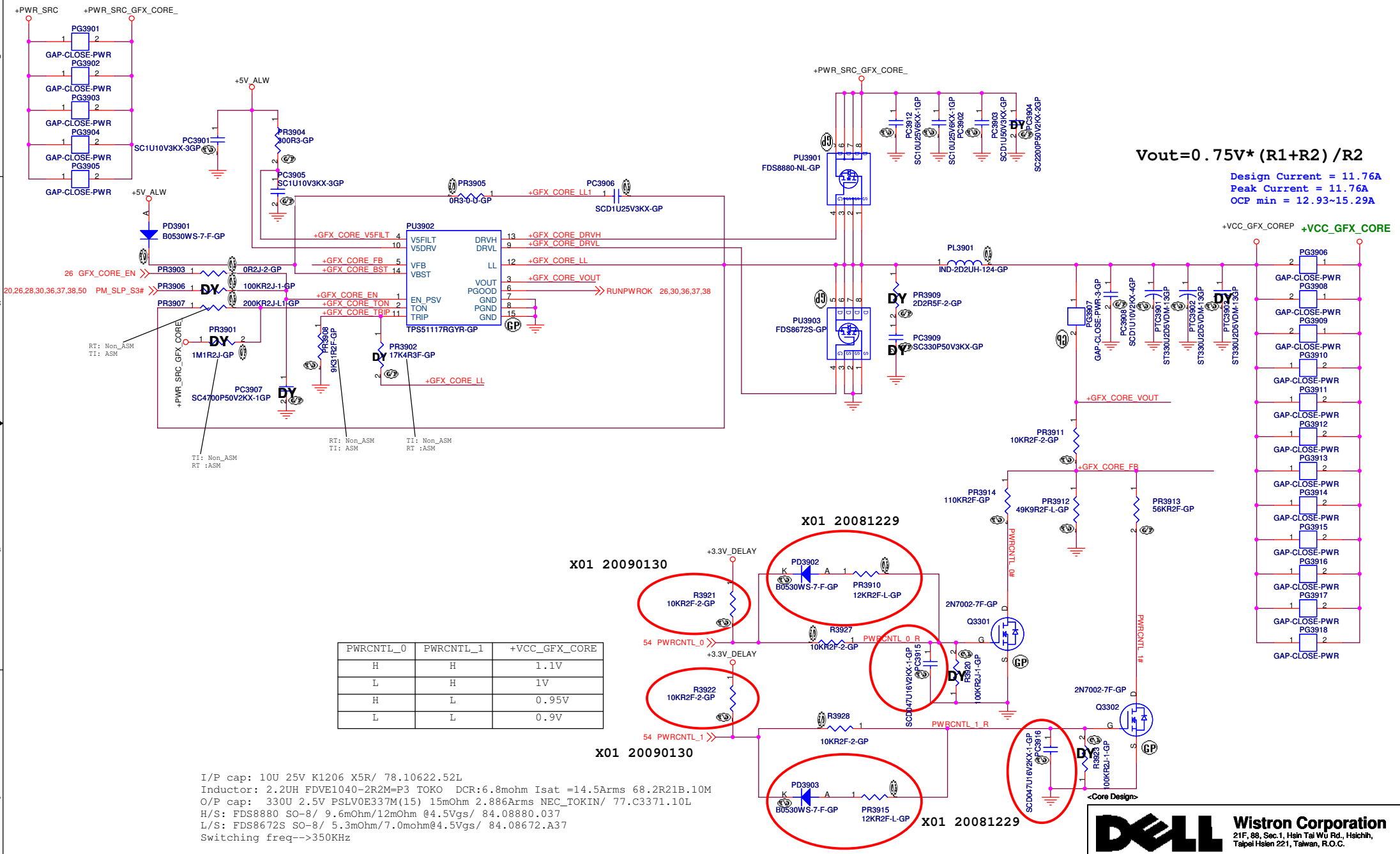
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.8V/0.9V

Size: A3 | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 38 of 59

SSID = PWR.Plane.Regulator_gfx



PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	1.1V
L	H	1V
H	L	0.95V
L	L	0.9V

Wistron Corporation	Title: VGA_CORE	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	Size: A3	Document Number: Alba Discrete
	Rev: SB	
	Date: Monday, March 23, 2009	Sheet 39 of 59

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

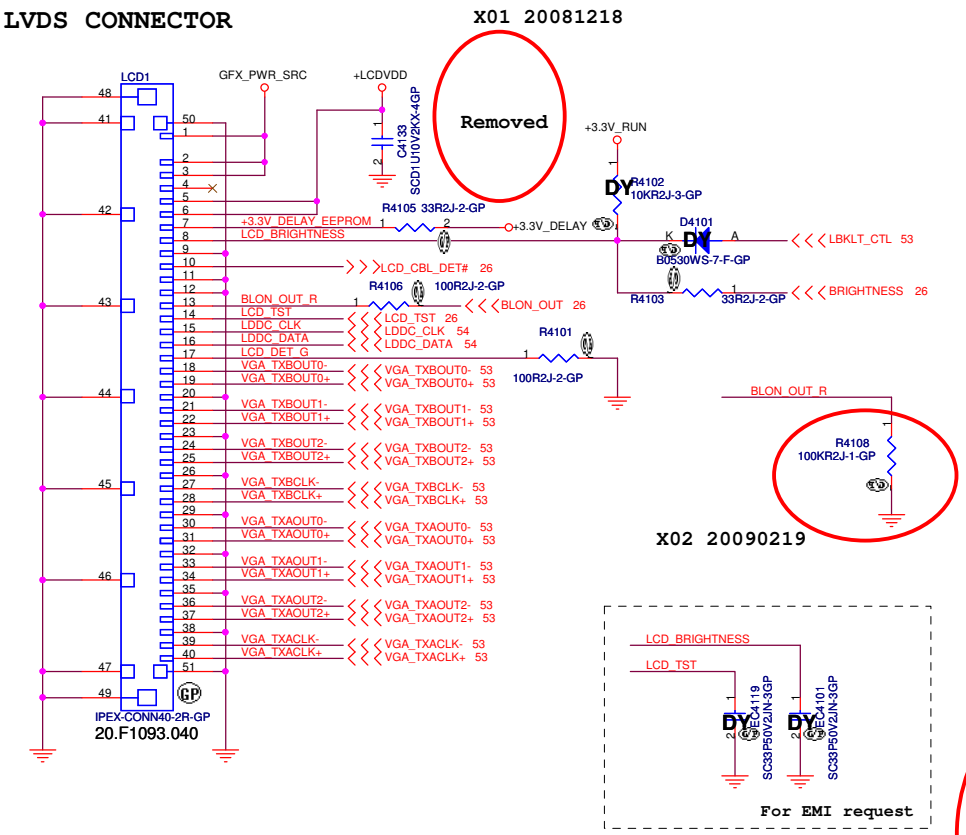
(Reserve)

Size	Document Number	Rev
Custom	*Alba Discrete*	*SB*

Date: Monday, March 23, 2009 Sheet 40 of 59

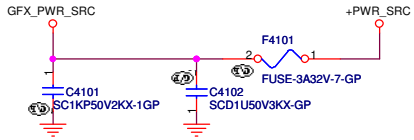
SSID = VIDEO

LVDS CONNECTOR

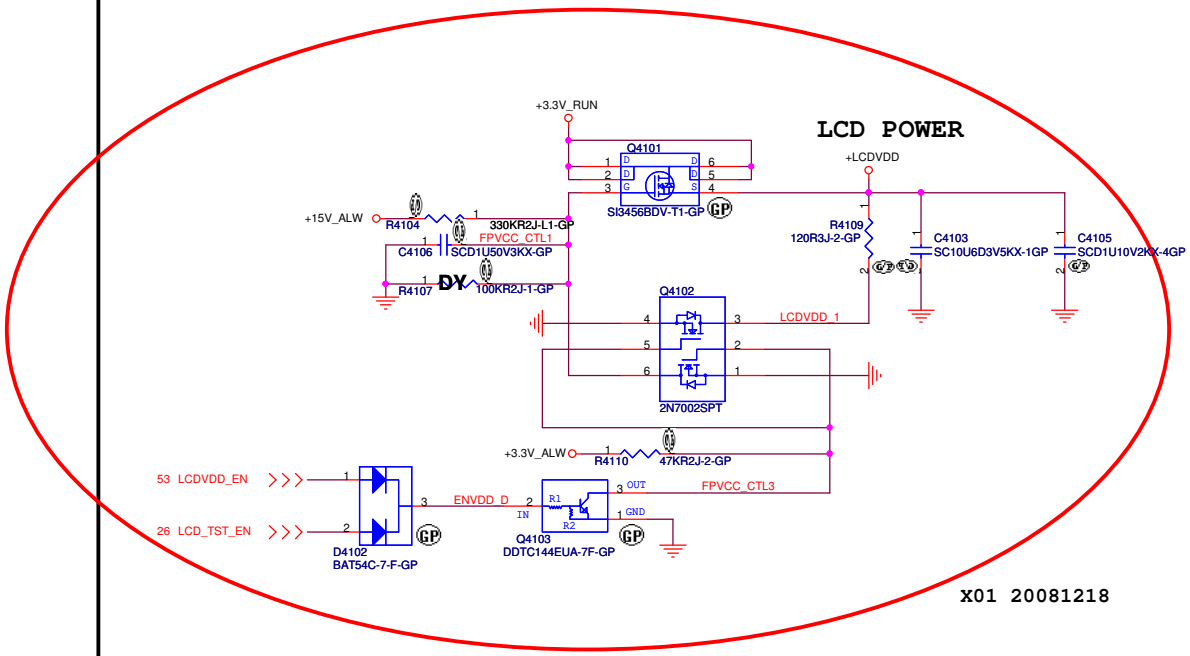


SSID = Inverter

INVERTER POWER



SSID = VIDEO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

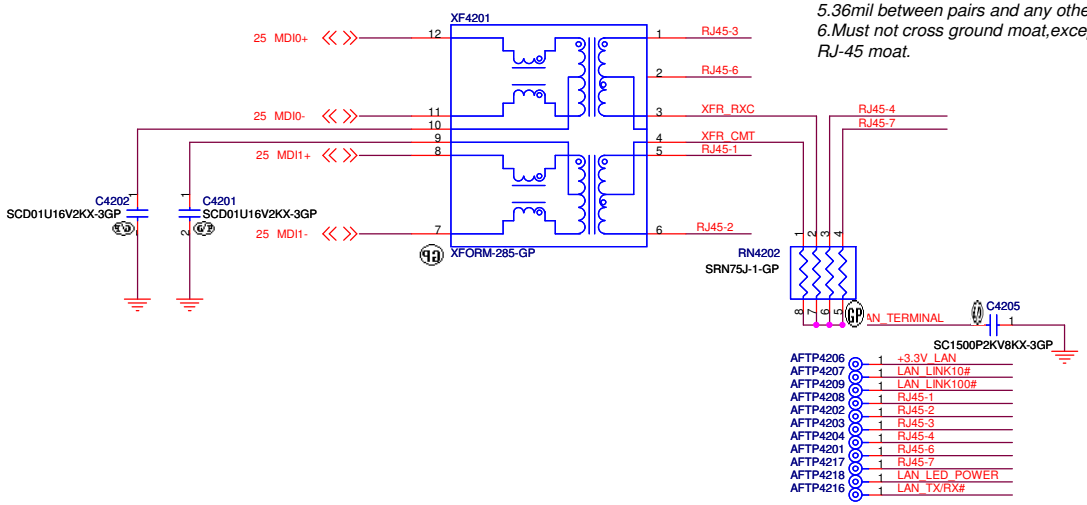
Size	Document Number	Rev
Custom	Alba Discrete	SB

Date: Monday, March 23, 2009 Sheet 41 of 59

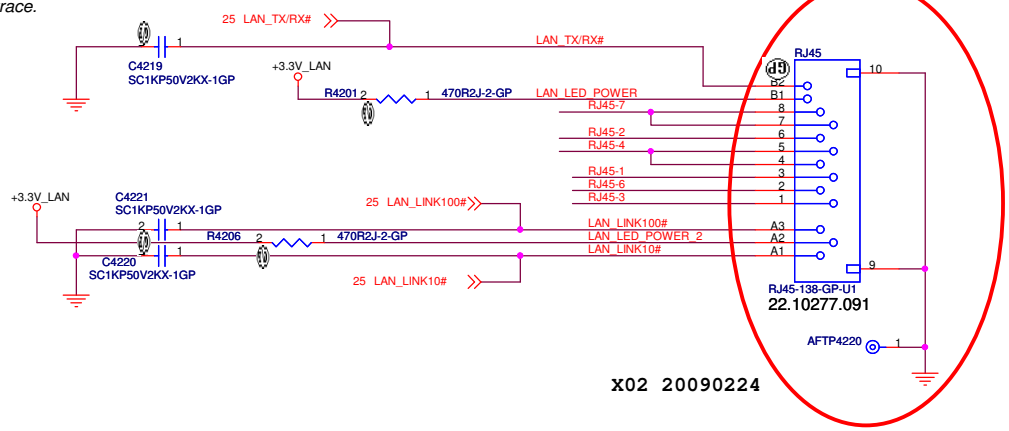
SSID = LOM

1.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
2.No vias, No 90 degree bends.
3.pairs must be equal lengths.
4.6mil trace width,12mil separation.
5.36mil between pairs and any other trace.
6.Must not cross ground moat,except RJ-45 moat.

10/100M Lan Transformer



RJ45 Connector

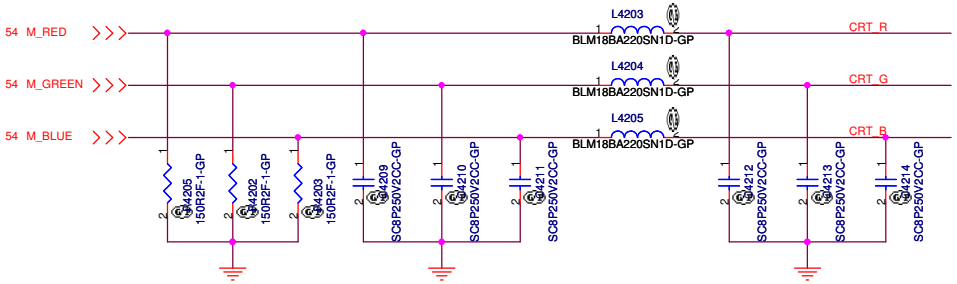


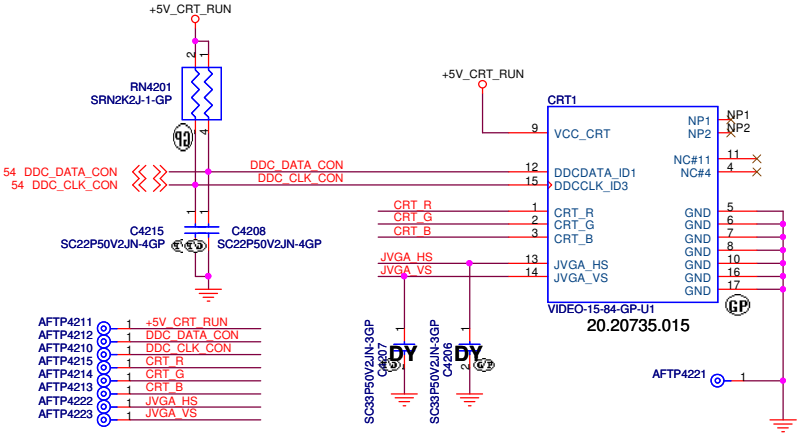
X02 20090224

SSID = VIDEO

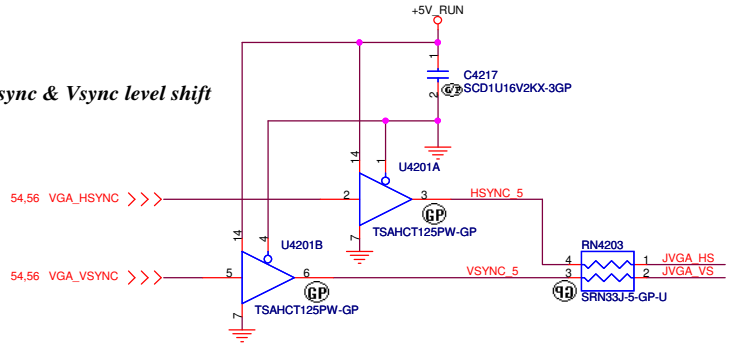
Layout Note:

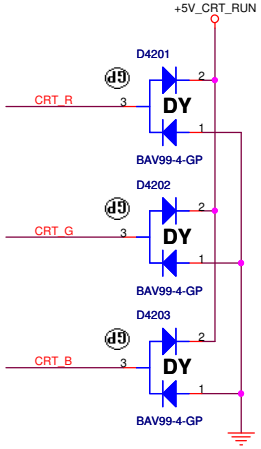
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

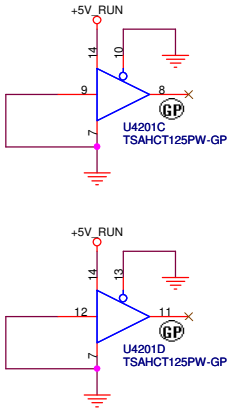


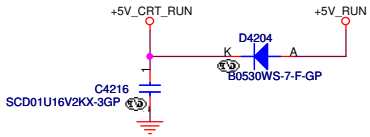


Hsync & Vsync level shift









<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

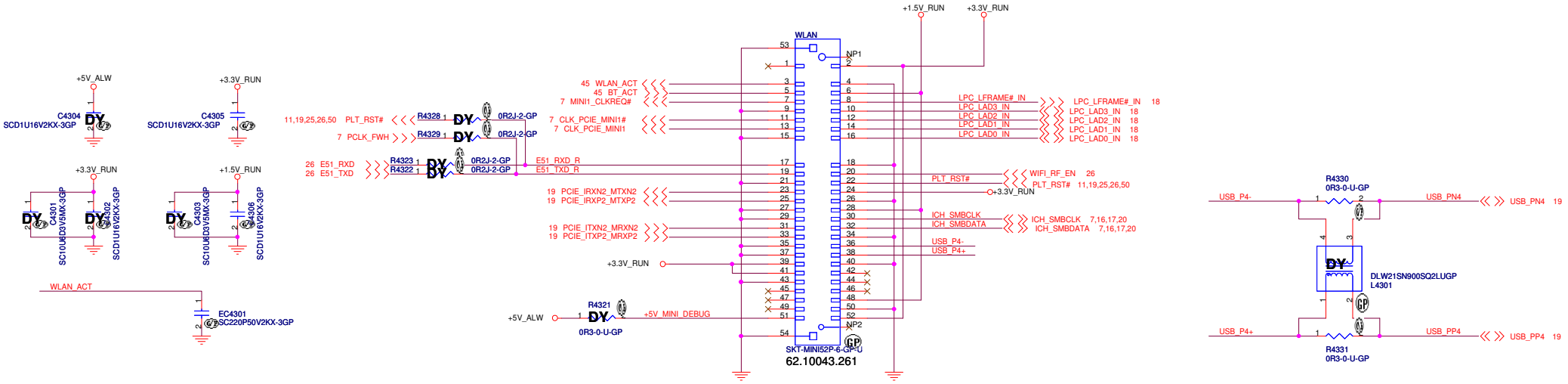
Title: **LAN/CRT Connector**

Size: Custom | Document Number: **Alba Discrete** | Rev: SB

Date: Monday, March 23, 2009 | Sheet 42 of 59

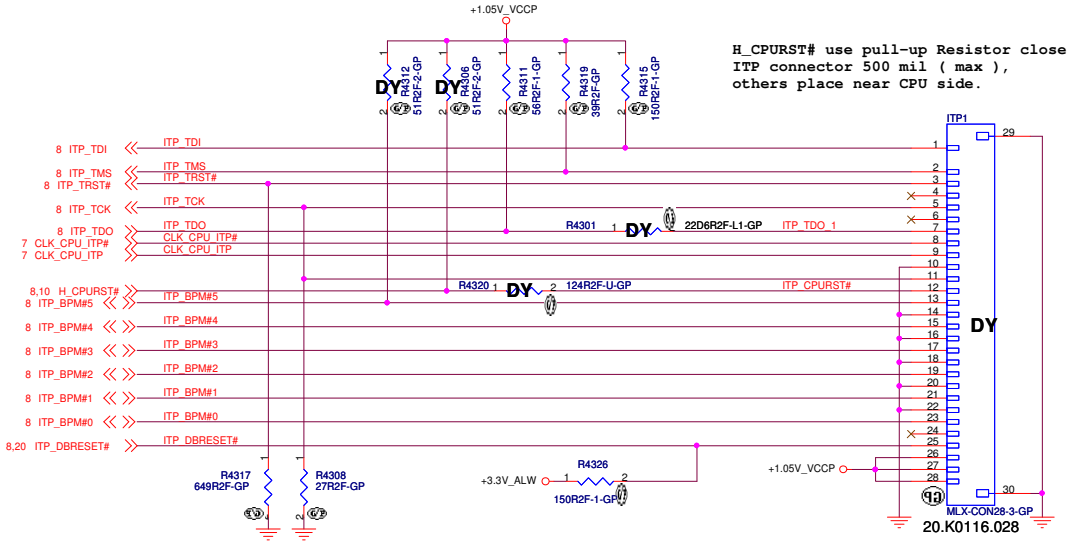
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

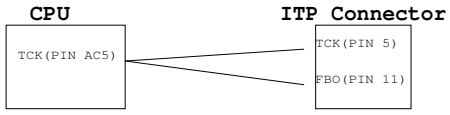


SSID = User.Interface

ITP Connector



+1.05V_VCCP use Decoupling Capacitor close
ITP connector 100 mil (max)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

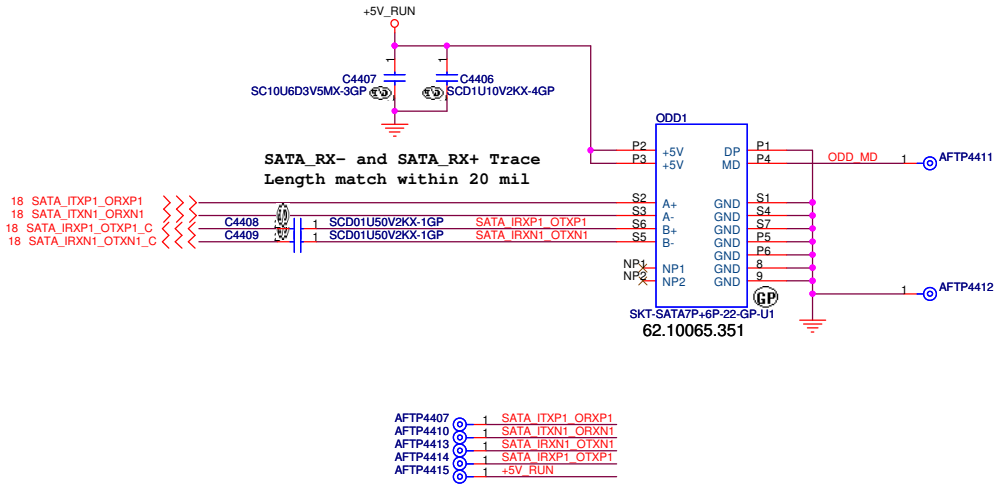
Title: MINICARD(WLAN)/ITP CONN

Size	Document Number	Rev
Custom	Alba Discrete	SB

Date: Monday, March 23, 2009 Sheet 43 of 59

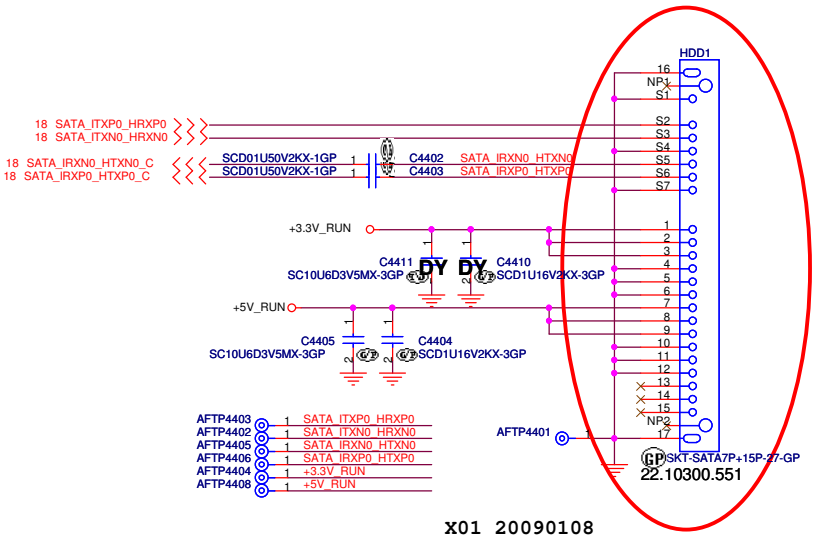
SSID = SATA

ODD Connector



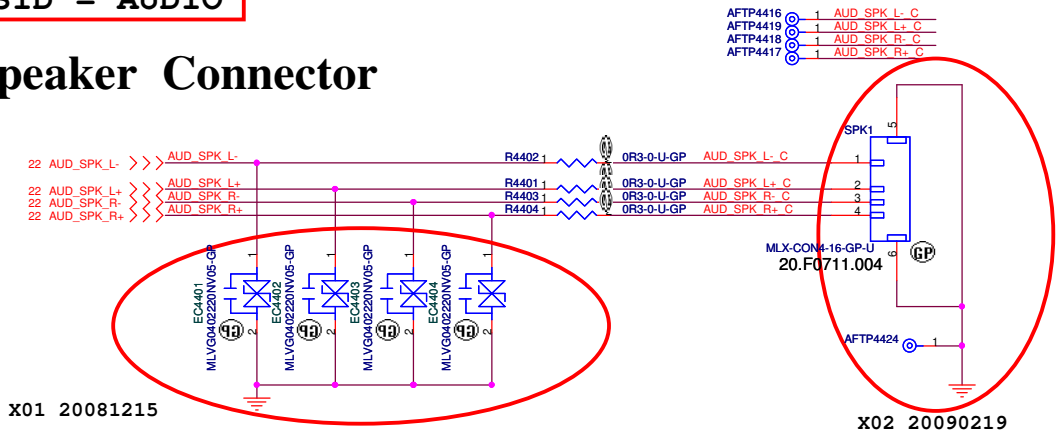
SSID = SATA

SATA HDD Connector



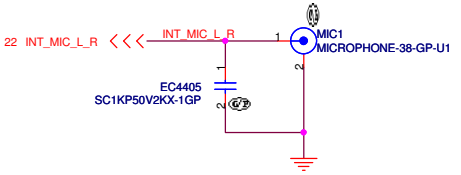
SSID = AUDIO

Speaker Connector



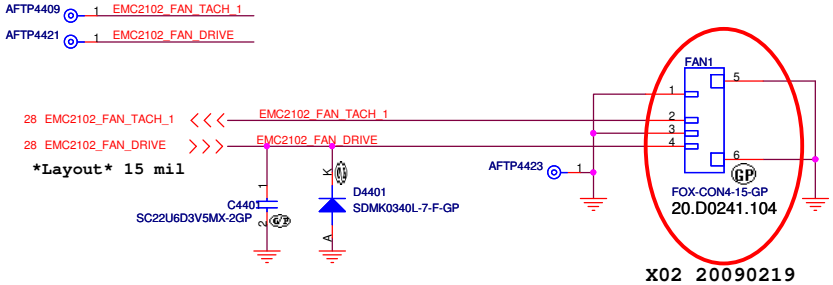
SSID = AUDIO

Internal MIC



SSID = Thermal

Fan Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

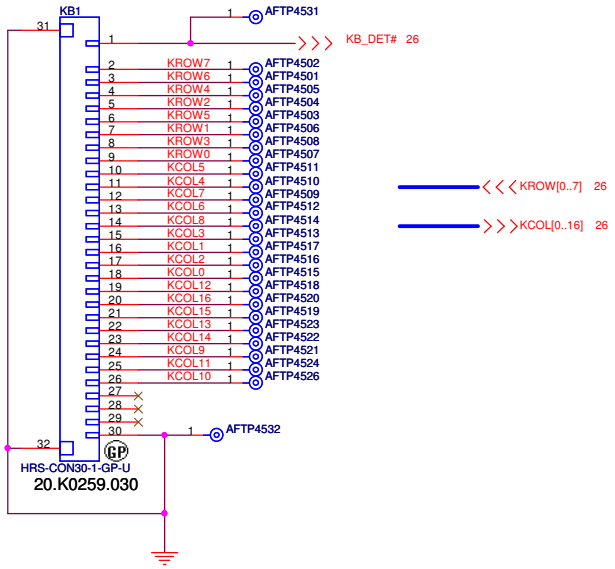
Title: HDD/ODD/FAN/SPEAKER/MIC

Size	Document Number	Rev
Custom	Alba Discrete	SB

Date: Monday, March 23, 2009 Sheet 44 of 59

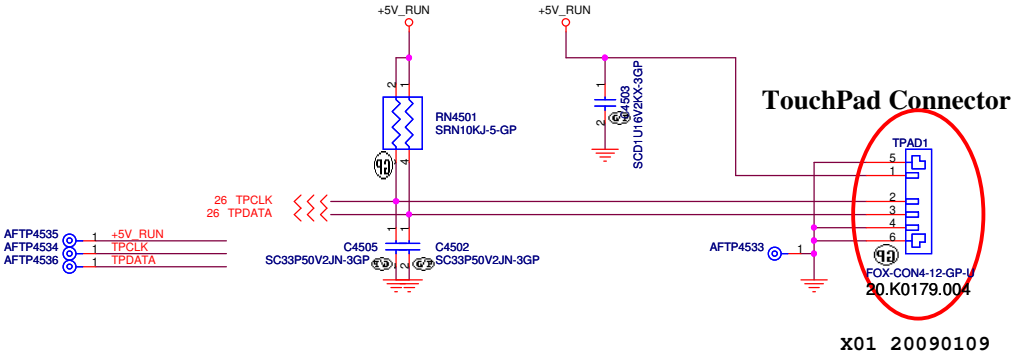
SSID = KBC

Internal KeyBoard Connector



SSID = Touch.Pad

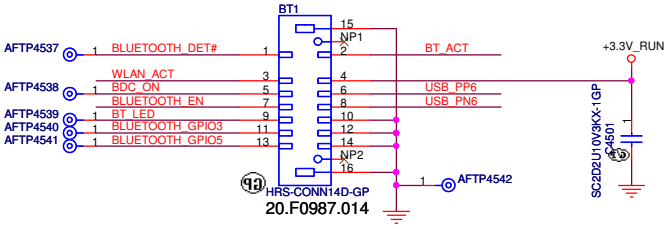
TouchPad Connector

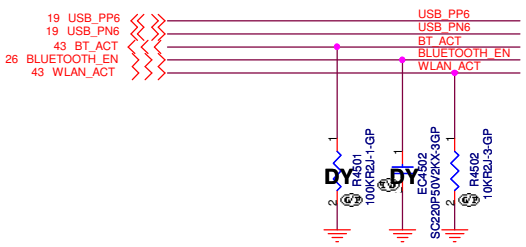


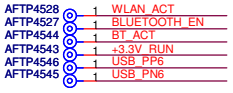
X01 20090109

SSID = User.Interface

Bluetooth Module conn.







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KeyBoard/TouchPad/BT

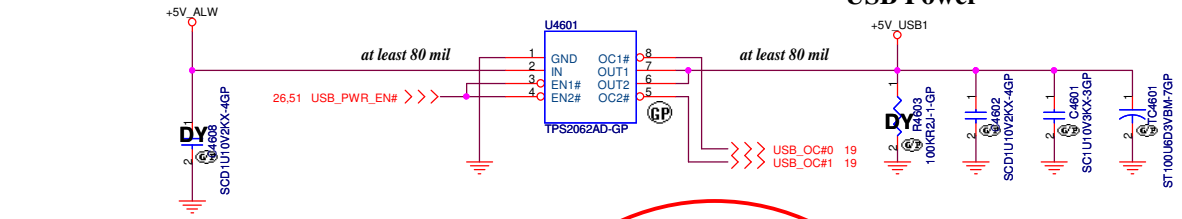
Size: Custom | Document Number: Alba Discrete | Rev: SB

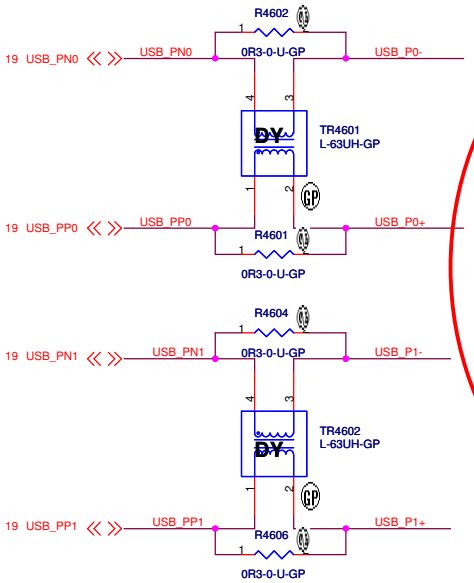
Date: Monday, March 23, 2009 | Sheet 45 of 59

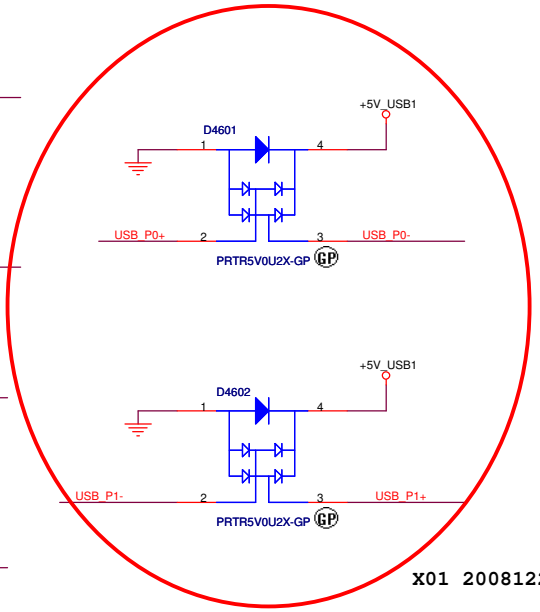
Remove Modem

X01 20081208

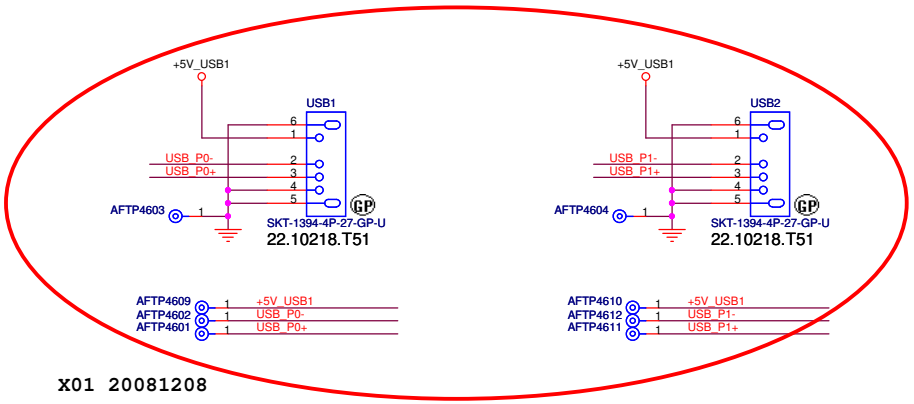
USB Power







X01 20081222



X01 20081208

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

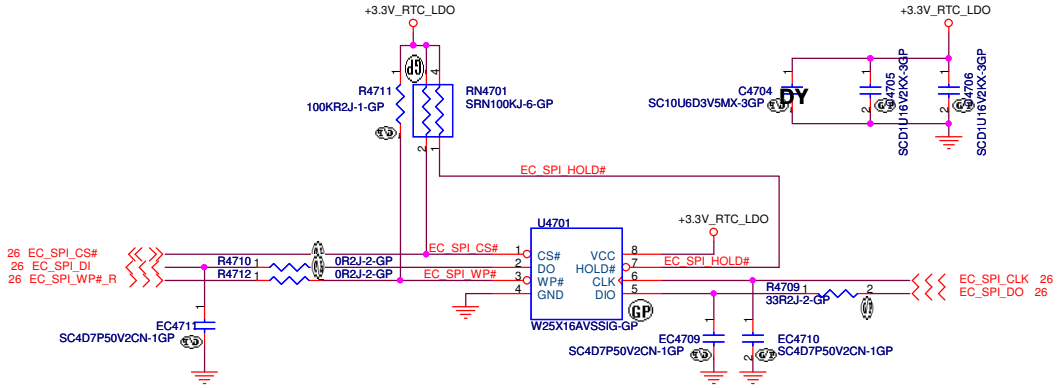
Title: MDC CONN

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 46 of 59

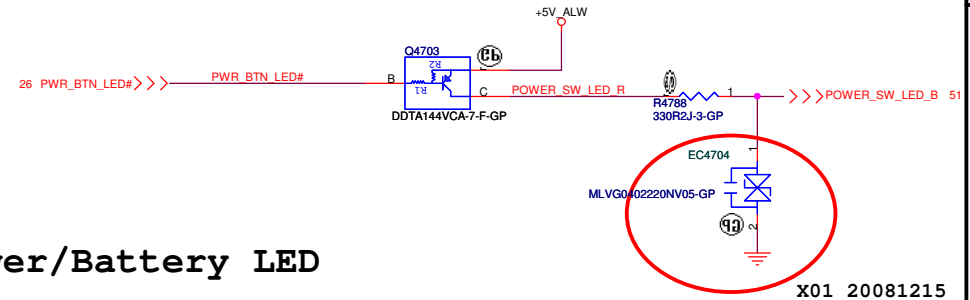
SSID = Flash.ROM

SPI FLASH ROM (16M bits)

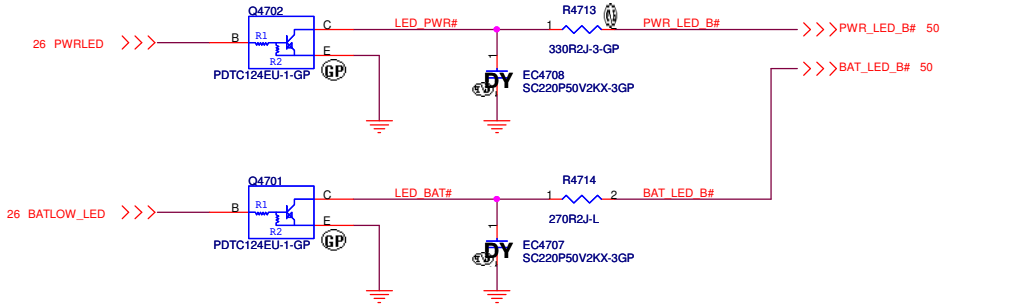


SSID = User.Interface

Power Button LED

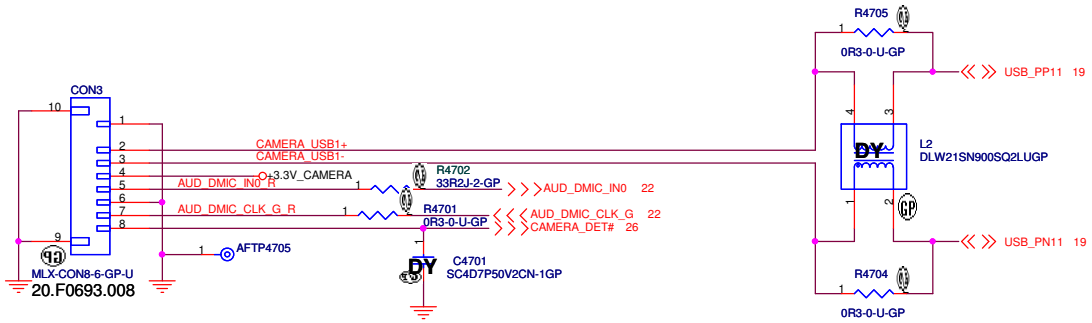


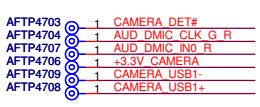
Power/Battery LED

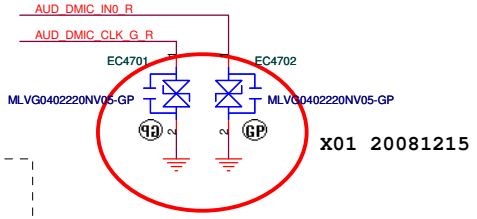


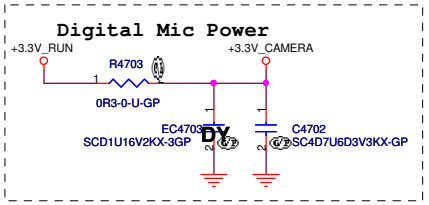
Camera Connector

SSID = User.Interface



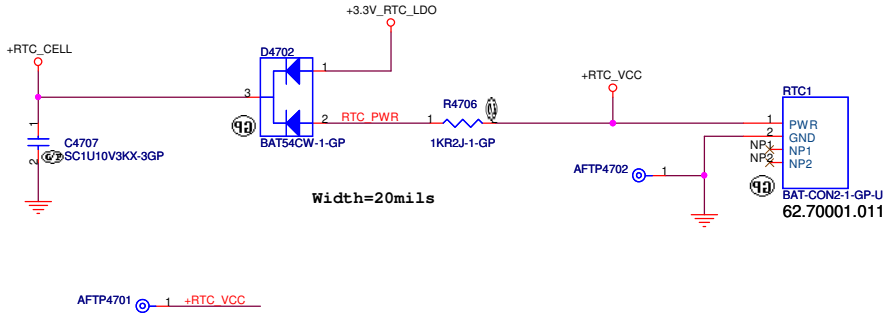






SSID = RBATT

RTC Connector



AFTP4701 1 +RTC_VCC

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPI Flash/LED/Camera/RTC

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 47 of 59

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Alba Discrete*	*SB*

Date: Monday, March 23, 2009 Sheet 48 of 59

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

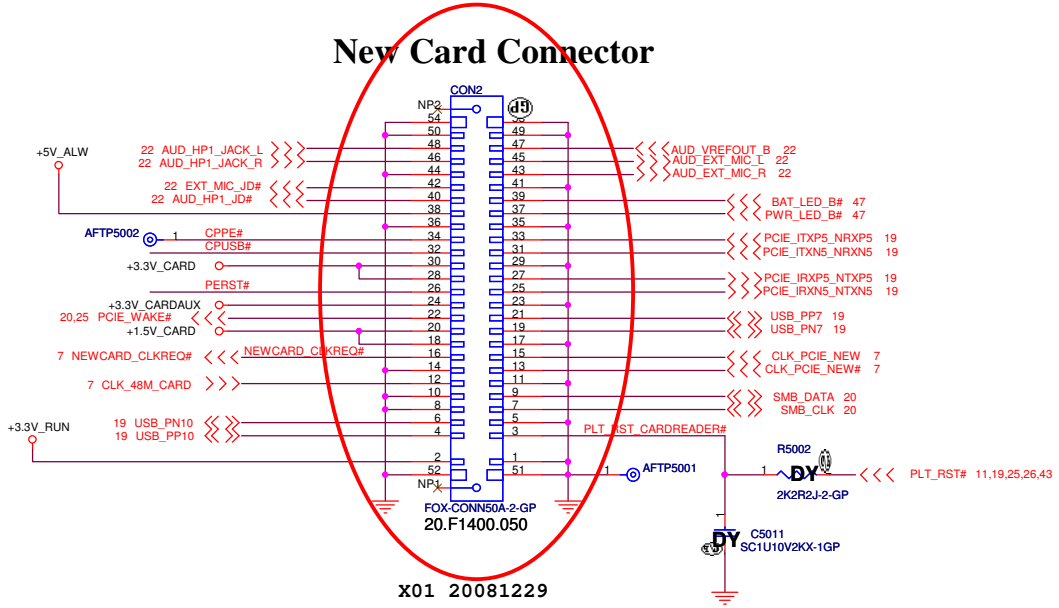
(Reserve)

Size	Document Number	Rev
Custom	*Alba Discrete*	*SB*

Date: Monday, March 23, 2009 Sheet 49 of 59

SSID = ExpressCard

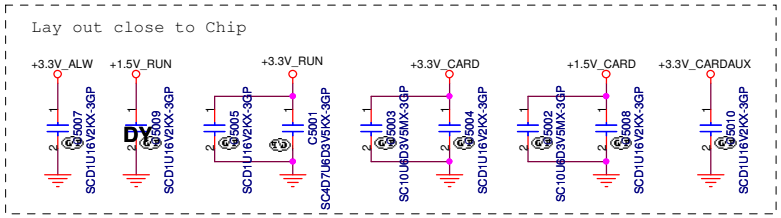
New Card Connector

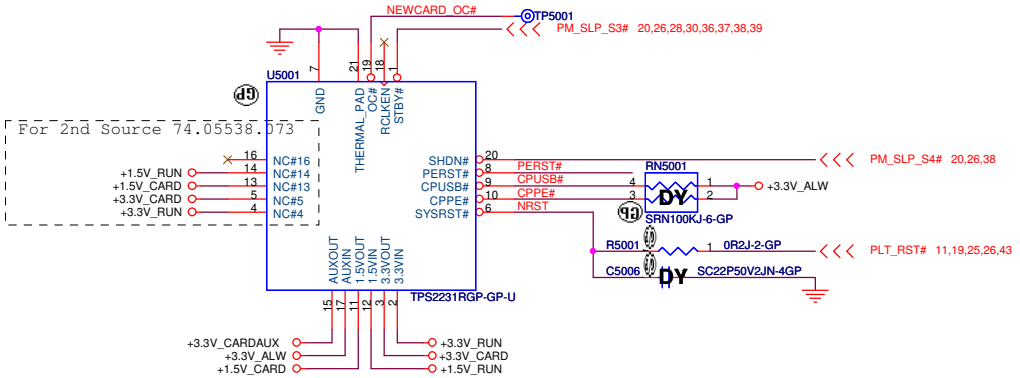


X01 20081229

AFTP5029 1 PWR_LED_B#
AFTP5032 1 BAT_LED_B#
AFTP5031 1 +5V_ALW
AFTP5030 1 PLT_RST_CARDREADER#
AFTP5020 1 PCIE_ITXP5_NRXP5
AFTP5025 1 PCIE_ITXN5_NRXN5
AFTP5023 1 PCIE_IRXP5_NTXP5
AFTP5024 1 PCIE_IRXN5_NTXN5
AFTP5026 1 AUD_VREFOUT_B
AFTP5004 1 AUD_HP1_JACK_L
AFTP5006 1 AUD_HP1_JACK_R
AFTP5007 1 +3.3V_RUN
AFTP5009 1 CPUSB#
AFTP5005 1 USB_PP7
AFTP5008 1 USB_PN7
AFTP5011 1 AUD_EXT_MIC_L
AFTP5010 1 AUD_EXT_MIC_R
AFTP5017 1 EXT_MIC_JD#
AFTP5013 1 AUD_HP1_JD#
AFTP5014 1 CLK_48M_CARD
AFTP5012 1 NEWCARD_CLKREQ#
AFTP5019 1 +3.3V_CARD
AFTP5015 1 PERST#
AFTP5022 1 +3.3V_CARDAUX
AFTP5021 1 PCIE_WAKE#
AFTP5016 1 +1.5V_CARD
AFTP5018 1 SMB_DATA
AFTP5003 1 SMB_CLK
AFTP5027 1 USB_PN10
AFTP5028 1 USB_PP10

Lay out close to Chip





+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

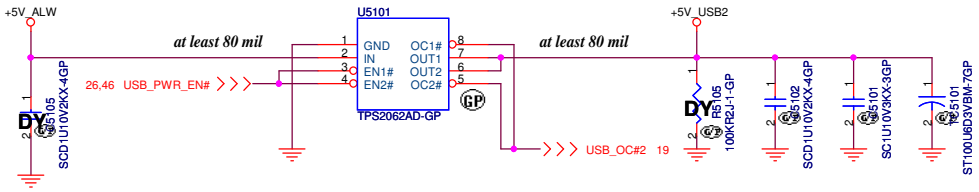
Title: Express Card Board CONN

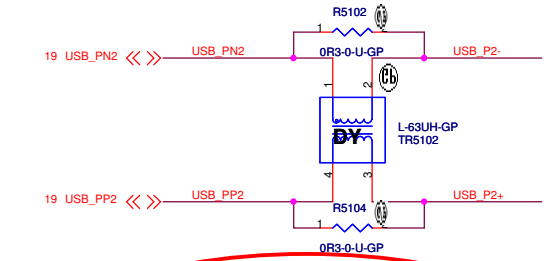
Size: Custom | Document Number: Alba Discrete | Rev: SB

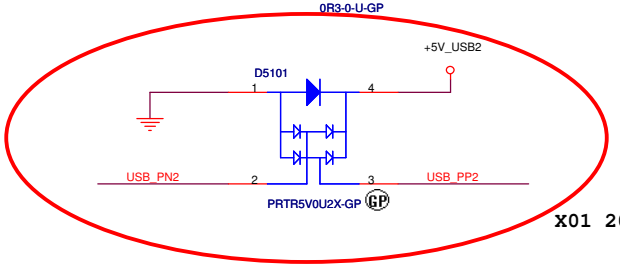
Date: Monday, March 23, 2009 | Sheet 50 of 59

SSID = USB

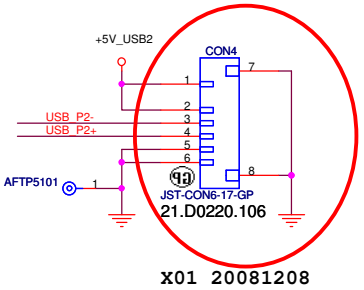
USB Power



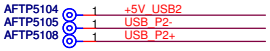




X01 20081222



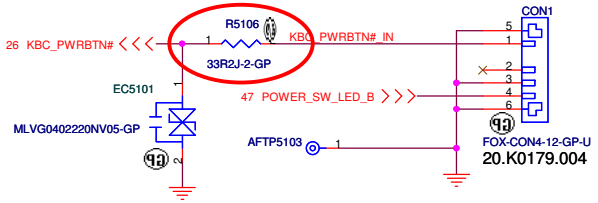
X01 20081208

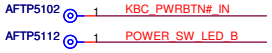


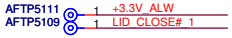
SSID = User.Interface

Power Button Board CONN

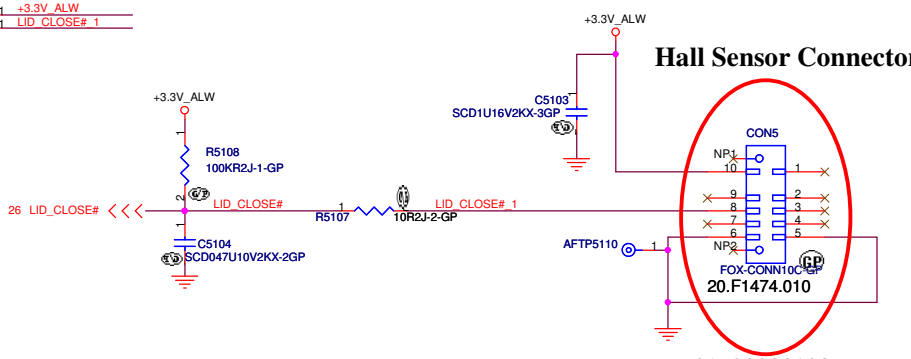
X01 20090130







Hall Sensor Connector



X01 20090109

<Core Design>

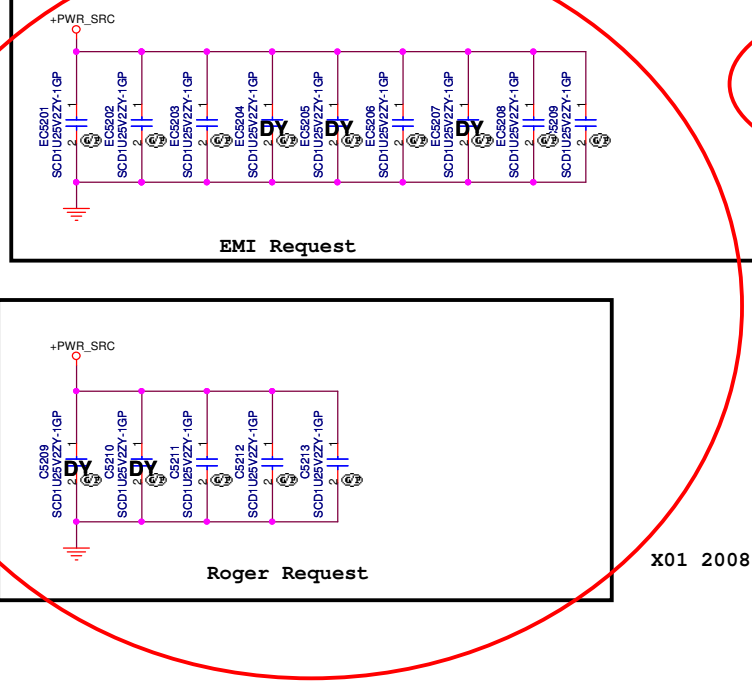
DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Button/Hall Sensor/USB Board***

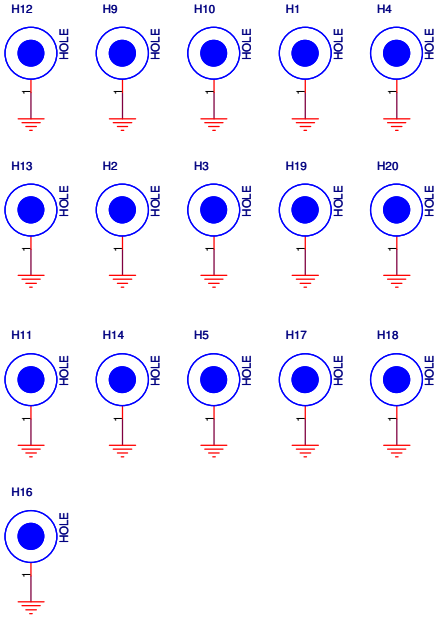
Size: Custom | Document Number: ***Alba Discrete*** | Rev: ***SB***

Date: Monday, March 23, 2009 | Sheet 51 of 59

SSID = Mechanical



Removed
X01 20081208



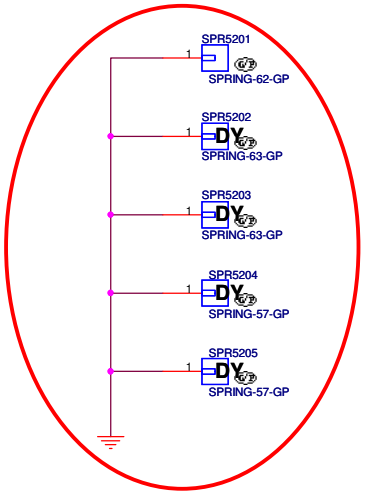
X01 20081215

Thermal
H6
STF237R117H83-1-GP
34.4CK01.001

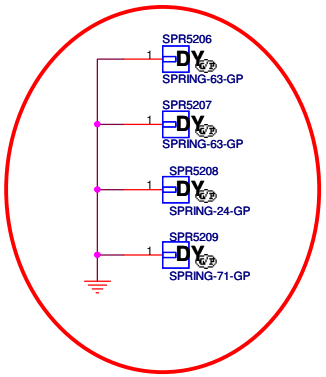
Bluetooth
H8
STF237R115H123-GP
34.4A902.001

Removed
X01 20081208

MINI CARD
H7
STF256R89H178-GP
34.4B417.001



X01 20090105



X02 20090304

<Core Design>

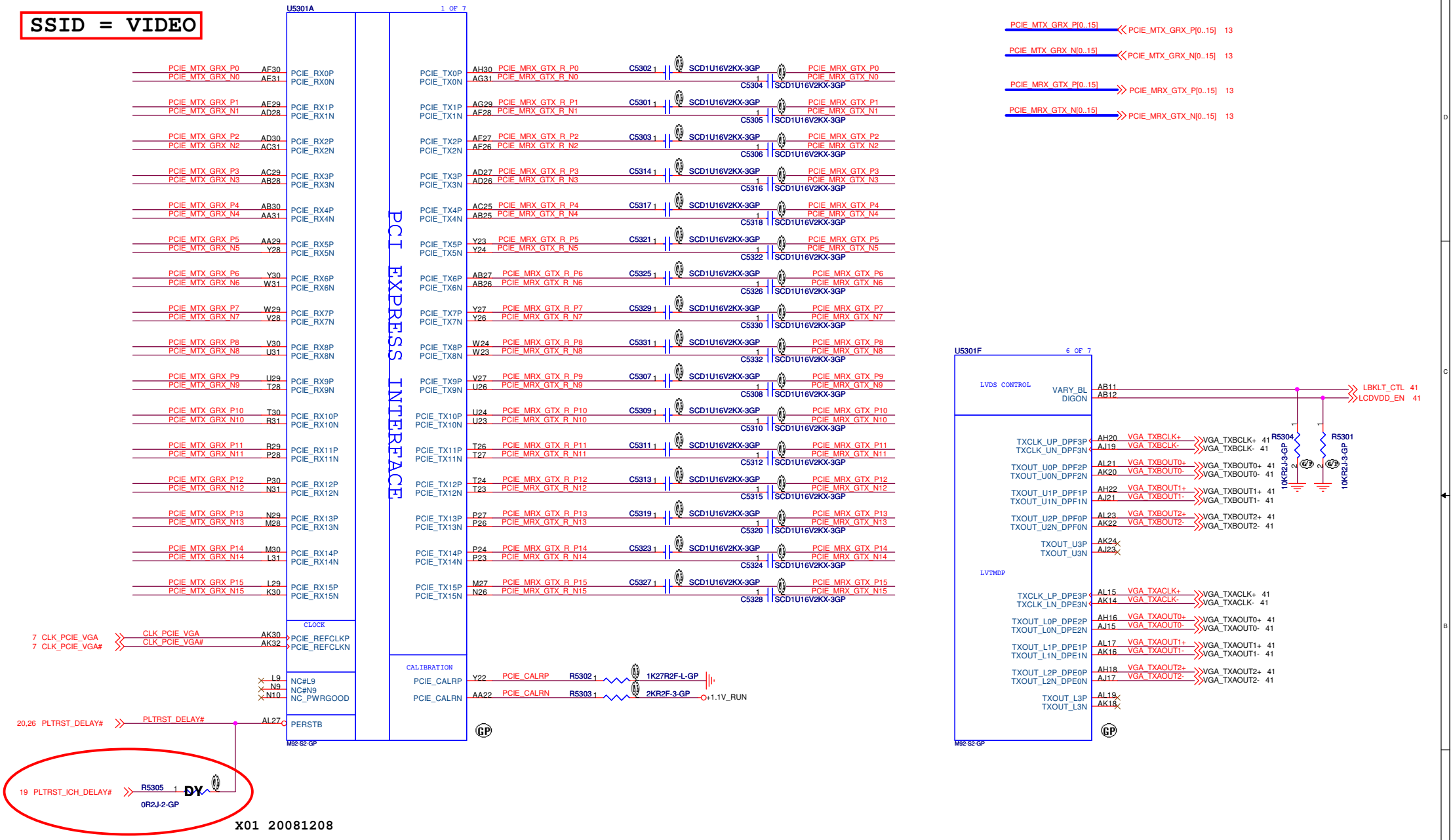
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Miscellaneous Components

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 52 of 59

SSID = VIDEO



X01 20081208

PCIE_MTX_GRX_P[0..15] → PCIE_MTX_GRX_P[0..15] 13

PCIE_MTX_GRX_N[0..15] → PCIE_MTX_GRX_N[0..15] 13

PCIE_MRX_GTX_P[0..15] → PCIE_MRX_GTX_P[0..15] 13

PCIE_MRX_GTX_N[0..15] → PCIE_MRX_GTX_N[0..15] 13

<Core Design>

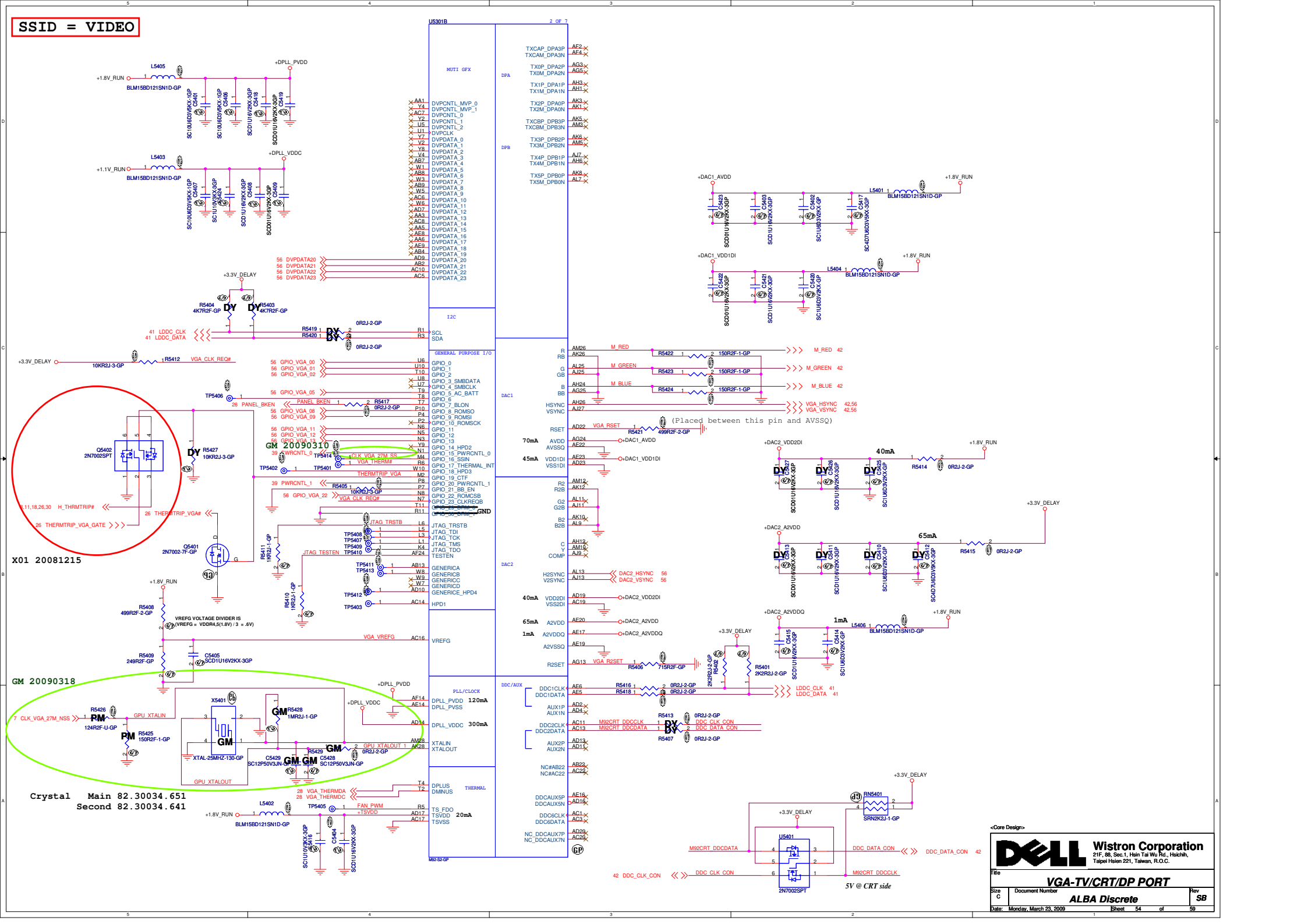
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-PCIE/LVDS(1/4)

Size: Custom | Document Number: ALBA Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 53 of 59

SSID = VIDEO



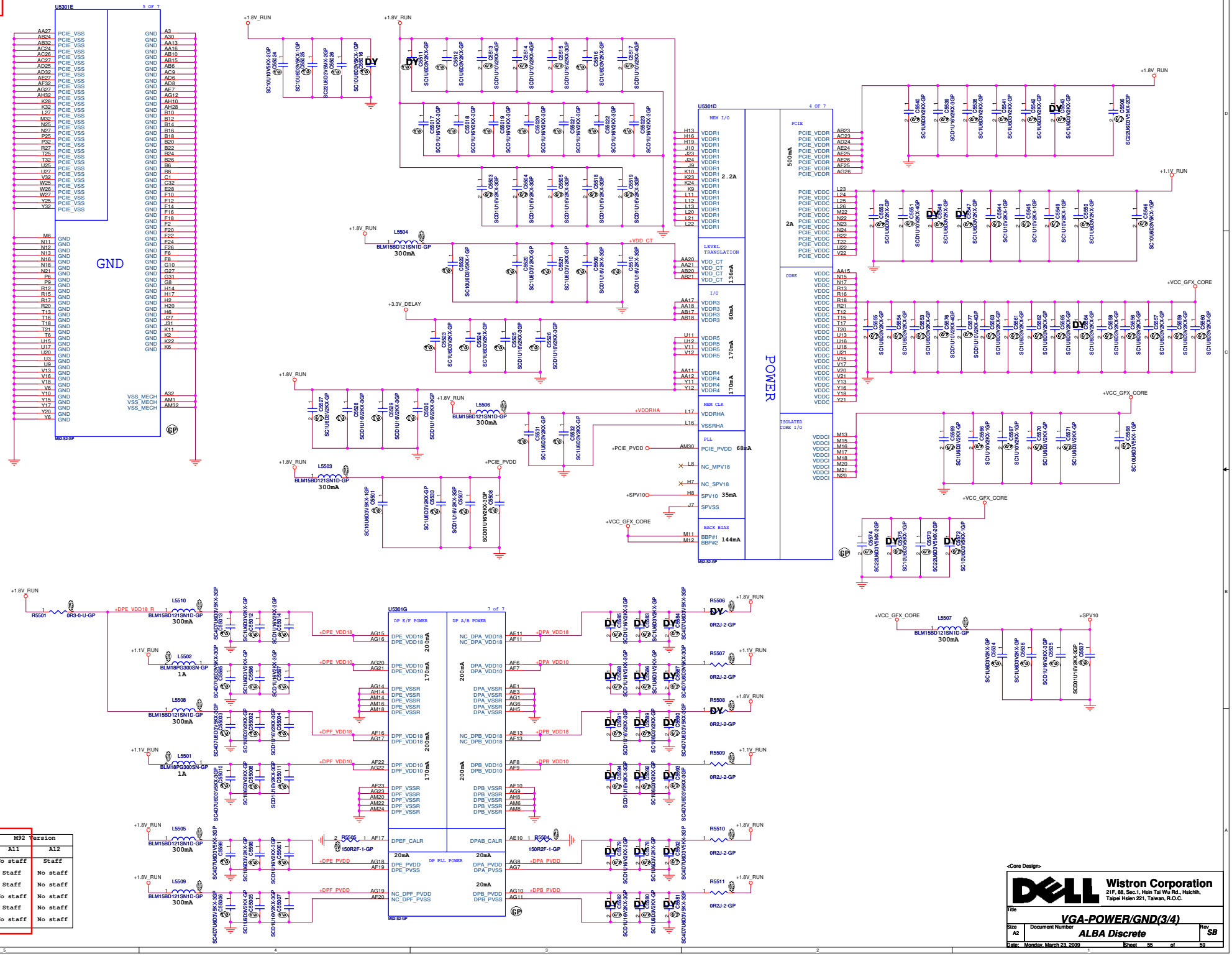
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-TV/CRT/DP PORT

Size: C | Document Number: ALBA Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 54 of 59

SSID = VIDEO

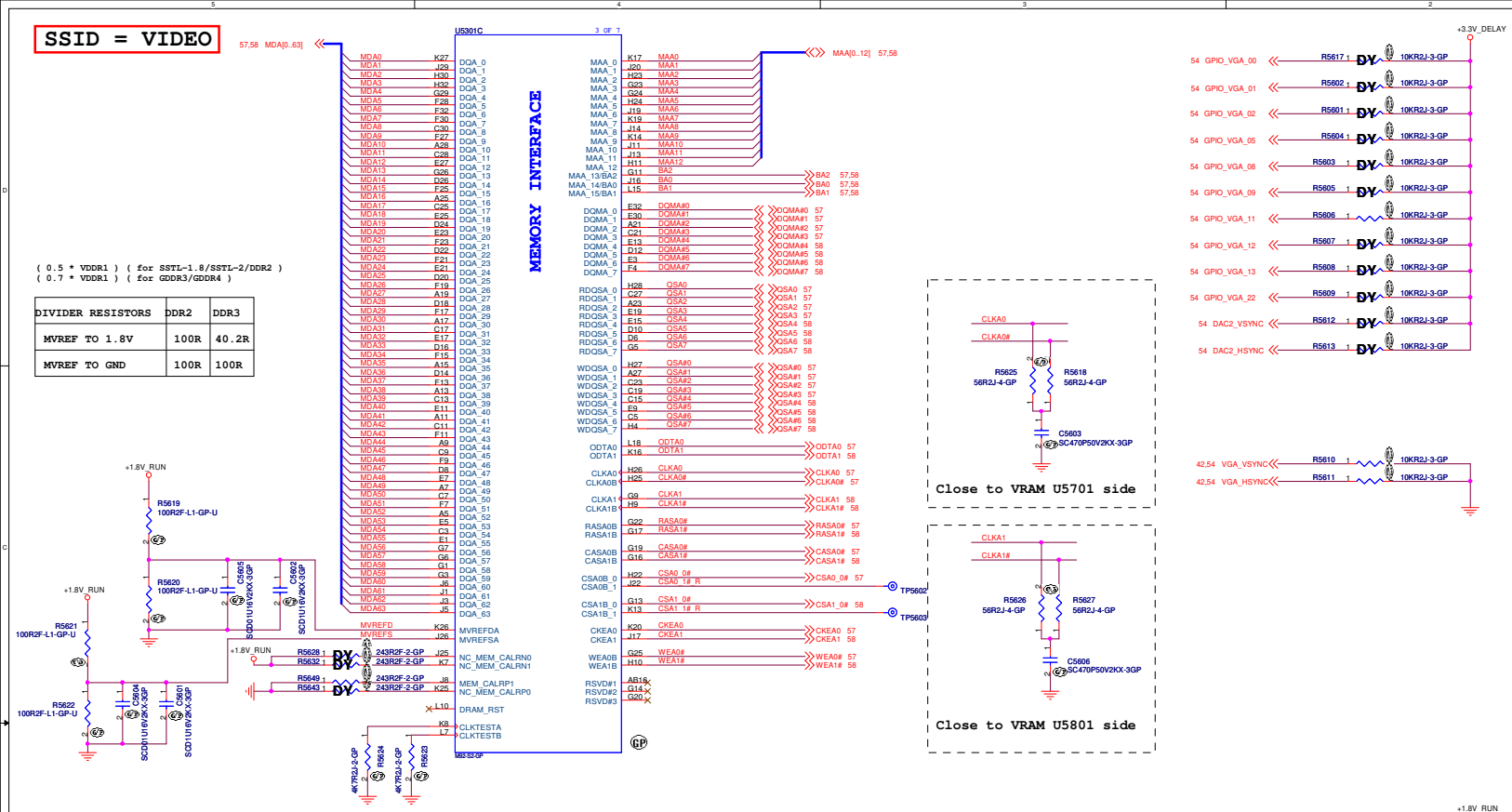


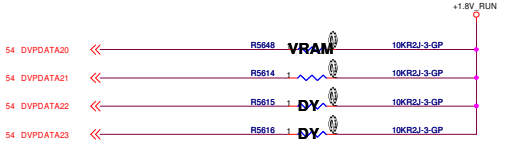
	M92 Version	
Part	A11	A12
R5401	No staff	Staff
Q5106	Staff	No staff
R5402	Staff	No staff
R5403	No staff	No staff
Q5107	Staff	No staff
C5384	No staff	No staff

SSID = VIDEO

(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R





ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO3 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
V 256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Tansmitter Power Savings Enable V 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable V 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	V 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	V 0= Disable CLKREQ#power management capability 1= Enable CLKREQ# power management capability
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] V 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(23:20) (Internal PD)	MEMORY TYPE,MAKE AND SIZE INFO 0000 - gDDR2 ---- ---- 0001 - gDDR2 64Mx16 HYNIX V 0010 - gDDR2 64Mx16 SAMSUNG 0011 - gDDR2 32Mx16 HYNIX 0100 - gDDR2 32Mx16 SAMSUNG

<Core Design>

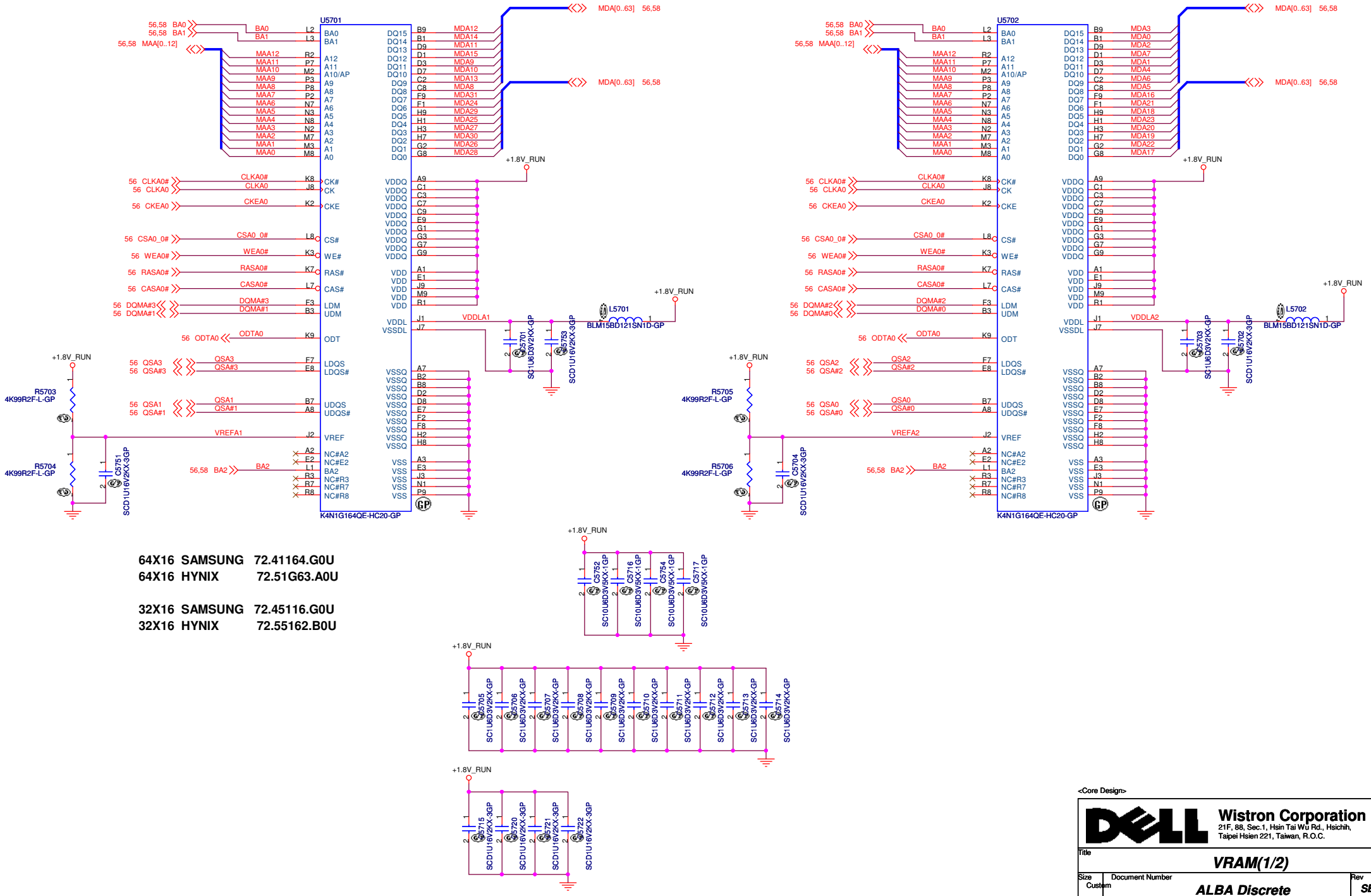
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-MEMORY/STRAPS(4/4)

Size: A2 | Document Number: ALBA Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 56 of 60

SSID = VIDEO



64X16 SAMSUNG 72.41164.G0U
64X16 HYNIX 72.51G63.A0U

32X16 SAMSUNG 72.45116.G0U
32X16 HYNIX 72.55162.B0U

<Core Design>

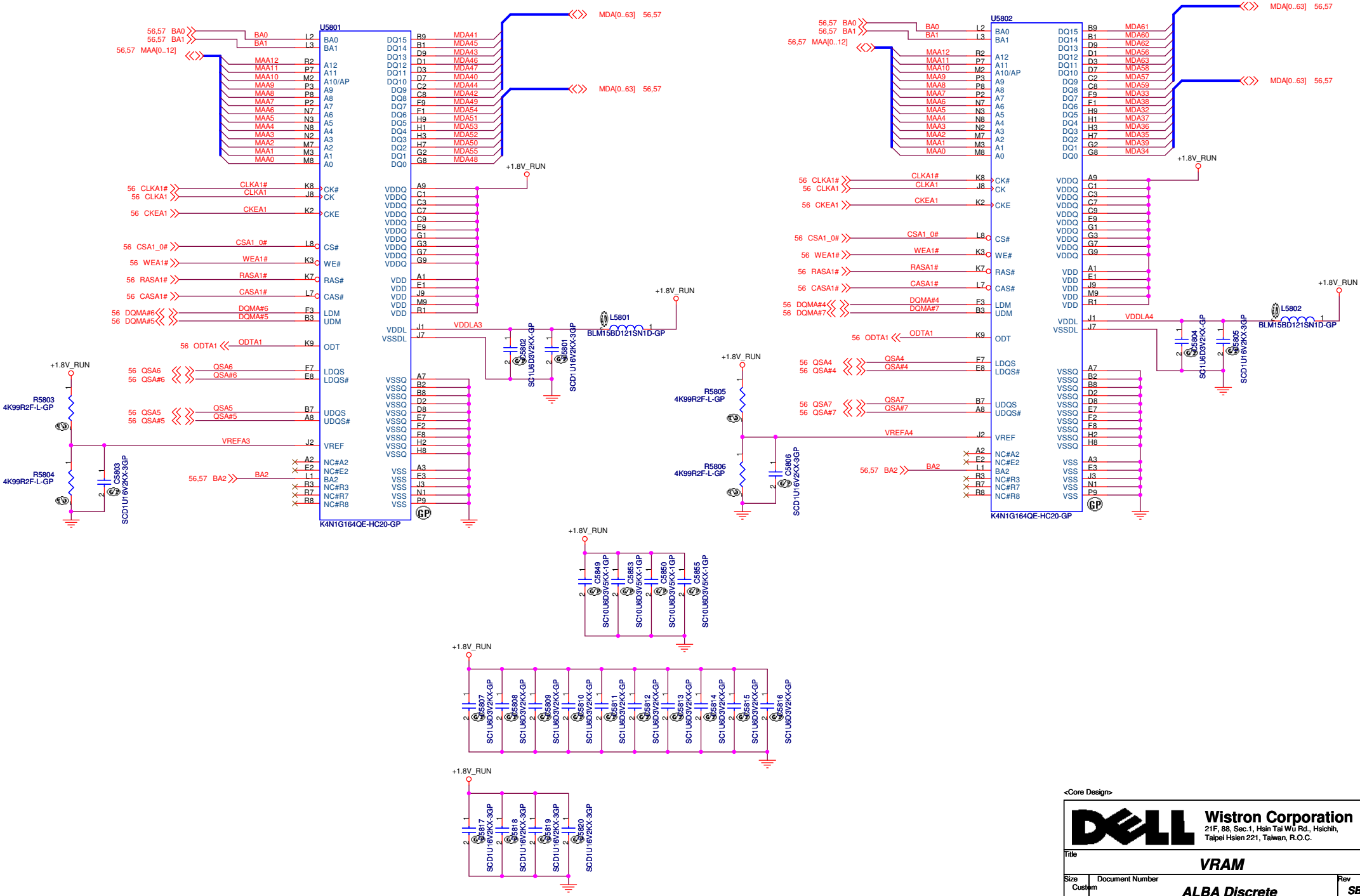
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM(1/2)

Size: Custom | Document Number: ALBA Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 57 of 60

SSID = VIDEO


U5801
K4N1G164QE-HC20-GP
U5802
K4N1G164QE-HC20-GP
MDA[0..63] 56,57
+1.8V_RUN
VDDLA3
VDDLA4
L5801
BLM15BD121SN1D-GP
L5802
BLM15BD121SN1D-GP
R5803 4K99R2F-L-GP
R5804 4K99R2F-L-GP
R5805 4K99R2F-L-GP
R5806 4K99R2F-L-GP
C5803 SCD1U16V2KX-3GP
C5806 SCD1U16V2KX-3GP
SC1U6D3V2KX-GP
SCD1U16V2KX-3GP
SC10U6D3V5KX-1GP
VREFA3
VREFA4
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM
Size Custom
Document Number
ALBA Discrete
Rev SB
Date: Monday, March 23, 2009
Sheet 58 of 60

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	18,46 52,42	2008/12/08	DELL	Remove Modem function.	Remove MDC schematics,holding,stand off.	X01
2	19,53	2008/12/08	Wistron	Reserve PLT_RST# for GPU PCIE reset.	Add R1913(DY),R5305(DY).	X01
3	25	2008/11/26	Realtek	Power down sequence issue, request by vendor.	Change R2506 to 1K ohm.	X01
4	25	2008/12/18	KDS	Follow crystal vendor test report.	Change C2501 to 18pF. C2502 to 15pF.	X01
5	26	2008/12/08	Wistron	MB version ID change.	Pop R2609,depop R2608.	X01
6	38	2008/12/08	Wistron	AMD power regulator issue.	Change 1.8V,0.9V power regulator.	X01
7	42	2008/12/08	Wistron	Follow ME connector list for touch pad connector.	Change TPAD1.	X01
8	46,51	2008/12/08	Wistron	Follow ME connector list for USB connector.	Change USB1, USB2 and CON4.	X01
9	30,33	2008/12/15	Wistron	MOSFET can not fully trun on issue.	Add +15V_ALW power circuits. And modify 3.3V_RUN, 5V_RUN enable circuits.	X01
10	8,28	2008/12/15	Wistron	Thermal sensor order changed because DTS still have accuracy problem.	Change EMC2102 first channel to CPU internal diode. Change channel to GPU inernal diode.	X01
11	15	2008/12/15	Wistron	Cantiga power rating issue.	Add R1507.	X01
12	26,54	2008/12/15	Wistron	AMD CTF glitch issue.	Reserve KBC GPIO27, Add R2639.	X01
13	40	2008/12/15	Wistron	Add panel self test for factory.	Add D4002,Pop R2638.	X01
14	32	2008/12/15	Wistron	Prevent leakage from KBC.	Change PR3203 pull high from +3.3V_ALW to +3.3V_RTC_LDO.	X01
15	44,52 51,47	2008/12/15	Wistron	Modify based on EMI test result.	POP EC5203 C5212 EC5202 C5211 C5213 EC5206 EC5201 EC5208 and POP EC4701 EC4702 EC4401 EC4402 EC4403 EC4404 EC5101 with 22P-Varistor	X01
16	41	2008/12/18	Wistron	LCD power sequence issue.	Change +LCD_VDD power produce solution.	X01
17	41	2008/12/19	Wistron	CMO LCD white screen issue.	Add R4108(DY).	X01
18	46,51	2008/12/19	Wistron	Add ESD diode for USB Port.	Add D4601,D4602,D5101.	X01
19	39	2008/12/29	Wistron	GFX CORE glitch issue.	Add PD3902,PD3903,PR3910,PR3915. Change PC3915,PC3916 to 0.047uF.	X01
20	50	2008/12/29	Wistron	Follow ME connector list for Express card board.	Change CON2 to 20.F1400.050.	X01

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List

Size: A3 | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 59 of 60

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
21	9	2009/01/06	Wistron	Power team request for CPU core measurement.	Add PG901,PG902. Pop C901 and depot C902.	X01
22	26	2009/01/08	Wistron	Keyboard detect issue.	Pop R2625.	X01
23	44,51	2009/01/08	Wistron	Change new connector.	Change HDD1 and CON5.	X01
24	8	2009/01/12	Wistron	For better GTL reference voltage.	Pop C802.	X01
25	30,36 37,38	2009/01/12	Wistron	Add discharge circuit for GPU powers.	Add R3016,Q3006,R3015,Q3003,Q3702,R3702 R3703,D3802,R3802,C3802.	X01
26	22,26	2009/01/13	IDT	For pop noise on YC version codec.	Add Q2201,Q2202,R2219. Add GPIO33 for HP_MUTE.	X01
27	33	2009/01/13	Wistron	For +15V_ALW issue. Prevent higher than 20V.	Add PD3303,PC3301.	X01
28	51	2009/01/30	Wistron	ESD protection concern.	Change R5106 to 33ohm.	X01
29	39	2009/01/30	Wistron	For GFX_CORE overshoot and undershoot issue.	Pop R3921,R3922. Depop R3920,R3923.	X01
30	18,26	2009/02/19	Wistron	Prevent 32768Hz crystal no oscillation from flux.	Change C1807,C1806,C2607,C2608 to 0603 size.	X02
31	22	2009/02/26	IDT	For codec pop noise issue.	Change C2204 to 2.2uf. Add Q2201,Q2202,Q2203, Q2204,Q2205. Move R2218,R2220 to main board.	X02
32	26	2009/02/26	Wistron	Change Board ID and add VRAM type select pin.	Change board ID to 010,Add GPIO5 for VRAM type	X02
33	30	2009/03/02	Wistron	+3.3V_ALW drop issue.	Add C3005.	X02
34	31,42, 44,45	2009/02/19	Wistron	Connector change request by ME.	Change RJ45,DCIN,FAN,SPEAKER connectors.	X02
35	41	2009/02/19	Wistron	LCD white screen issue.	Pop R4108.	X02
36	31,32	2009/03/02	Wistron	Power team request.	Change PD3107 to 1SMB22AT3G. Change PC3208, PC3209 to X7R.	X02
37	52	2009/03/05	Wistron	Reserve capacitors and springs for EMI.	Add location for SPR5206~SPR5209 and EC5210~EC5213.	X02
38	26	2009/03/09	Wistron	No need to support keyboard detect function.	Depop R2625.	X02
39	22	2009/03/09	Wistron	For PC_BEEP sound volume issue.	Modify R2203 to 120Kohm.	X02
40	33	2009/03/10	Wistron	+15V_ALW issue.	Depop PD3303.	X02

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List

Size: A3 | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 60 of 60