Alba UMA Schematics

uFCPGA Mobile Penryn

Intel Cantiga-GM + ICH9M

2009-04-06

REV : -1

DY : Nopop Component

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Title: *Cover Page*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

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ALBA UMA Block Diagram

Project code : 91.4BK01.001
Part Number : 48.4BK04.0SA
PCB P/N : 08243
Revision : SA

PCB LAYER

L1: Top
L2: GND
L3: Signal
L4: Signal
L5: VCC
L6: Signal
L7: GND
L8: Bottom

ISL6266A/CPU_CORE 34,35	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

TPS51117/1.05V 36	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

TPS51125/3V,5V 33	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

TPS51116/1.8V,0.9V 38	
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS +0.9V_DDR_VTT +V_DDR_MCH_REF

L6935TR/1.5V 37	
INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN

MAX8731A/CHARGER 32	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

RUN PWR/3V,5V 30	
INPUTS	OUTPUTS
+5V_ALW +3.3V_ALW	+5V_RUN +3.3V_RUN

Clock Generator
SLG8SP513VTR 7

Intel Mobile CPU
Penryn
Socket P 8,9

FSB
800/1066MHz

Intel
Cantiga-GM
AGTL+ CPU I/F
DDR Memory I/F
External Graphics
10,11,12,13,14,15

CRT 42 — RGB CRT
LCD 41 — LVDS(Dual Channel)

DDRII 800 Channel A
DDR II 800 Channel B

DDRII 800 Slot 0 16
DDRII 800 Slot 1 17

DMIx4
CONTROL-LINK

Intel
ICH9-M
USB 2.0/1.1 ports (12)
PCI Express ports (6)
High Definition Audio
SATA ports (4)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
18,19,20,21

Power SW
TPS2231RGP 50

New Card
(On Express Card board) 50
PCIE x 1 & USB 2.0 x 1

10/100 LOM
RTL8103EL 25
PCIE x 1

RJ45
CONN 42

Left Side:
USB x 2 46
USB 2.0 x 2

PCIE

Mini-Card
802.11a/b/g/n 43
PCIE x 1

CAMERA
(Option) 47
USB 2.0 x 1

USB 2.0

Bluetooth 45
USB 2.0 x 1

Right Side:
USB x 1 51
USB 2.0 x 1

LPC Bus

CardReader
Realtek
RTS5159 50
USB2.0

(7 in 1)SD/MMC
MS/MS Pro/xD
(On Express Card board)

RJ11 42
MDC MODEM 46
AZALIA

Digital Mic Array
(Option) 47
Internal Mic 44

Azalia
CODEC
OP AMP
IDT
92HD81 22
AZALIA

MIC IN
HP OUT
(On Express Card board)

2CH SPEAKER 44

SATA
SATA

HDD 44
ODD 44

SPI

KBC
WINBOND
WPCE773L 26

Flash ROM
2MB 47
Touch
PAD 45
Int.
KB 45
Thermal
& Fan
EMC2102 28,44

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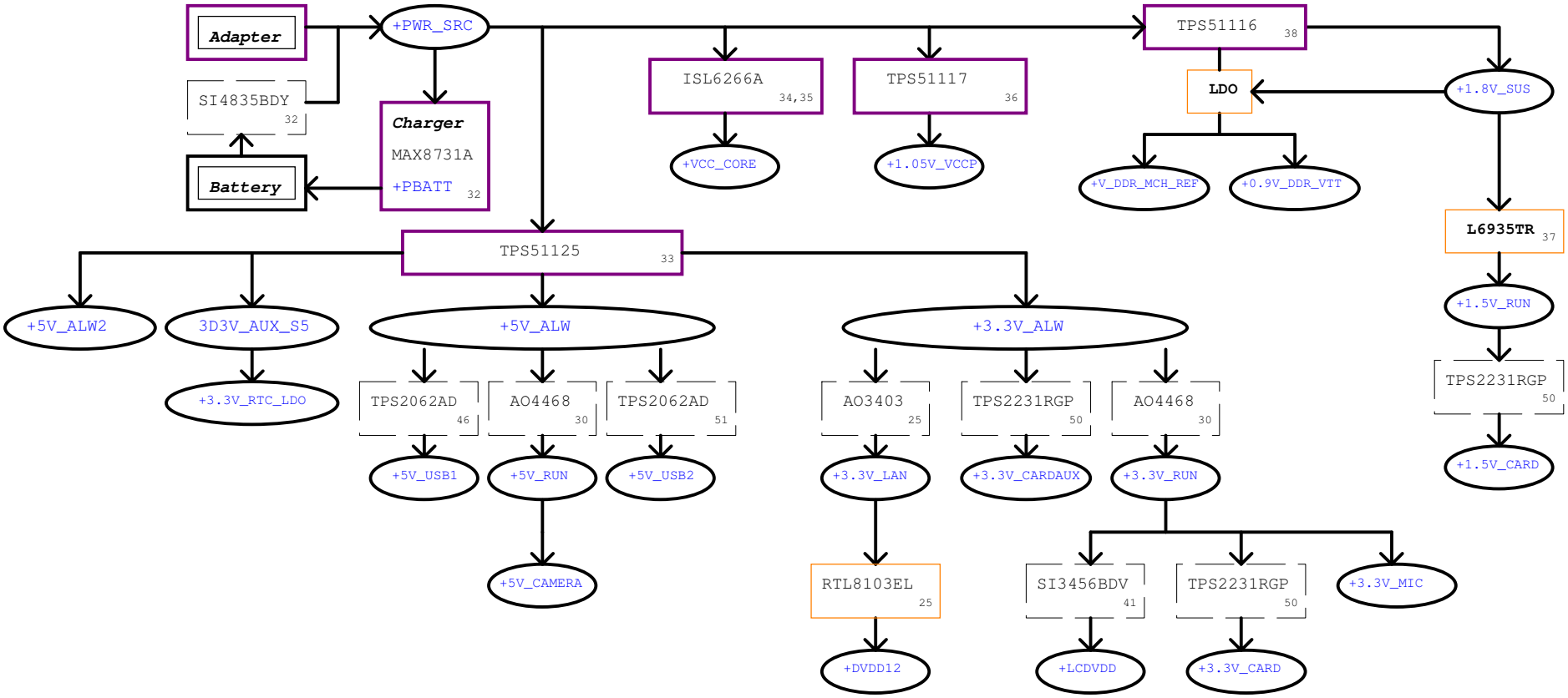

Power Shape

Regulator	LDO	Switch

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Title: ***Power Block Diagram***

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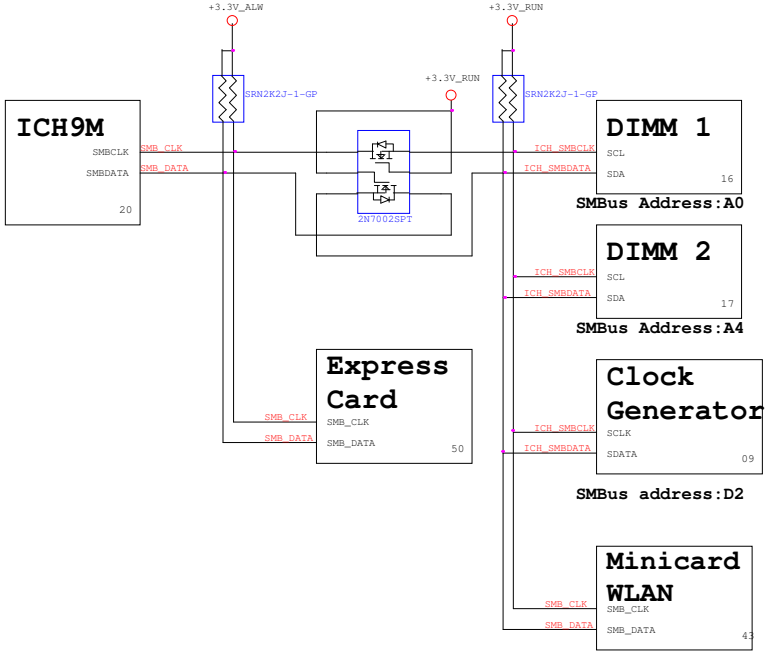
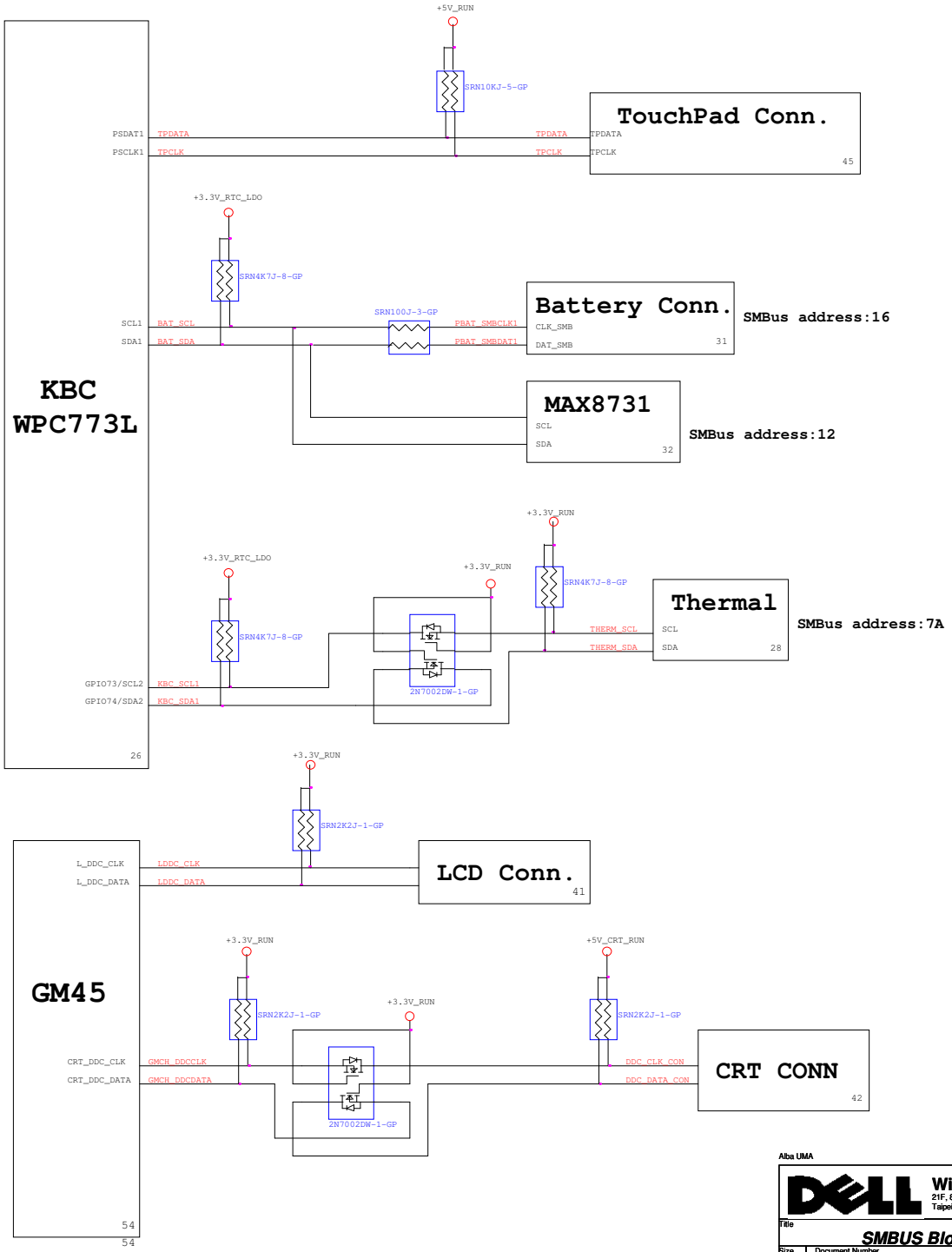
ICH9M SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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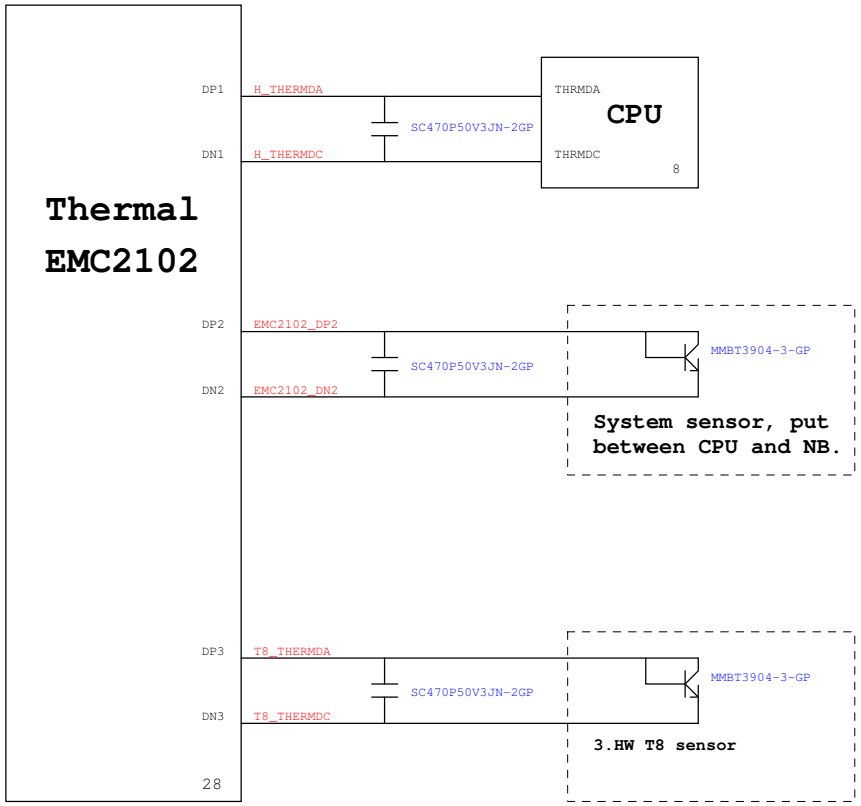
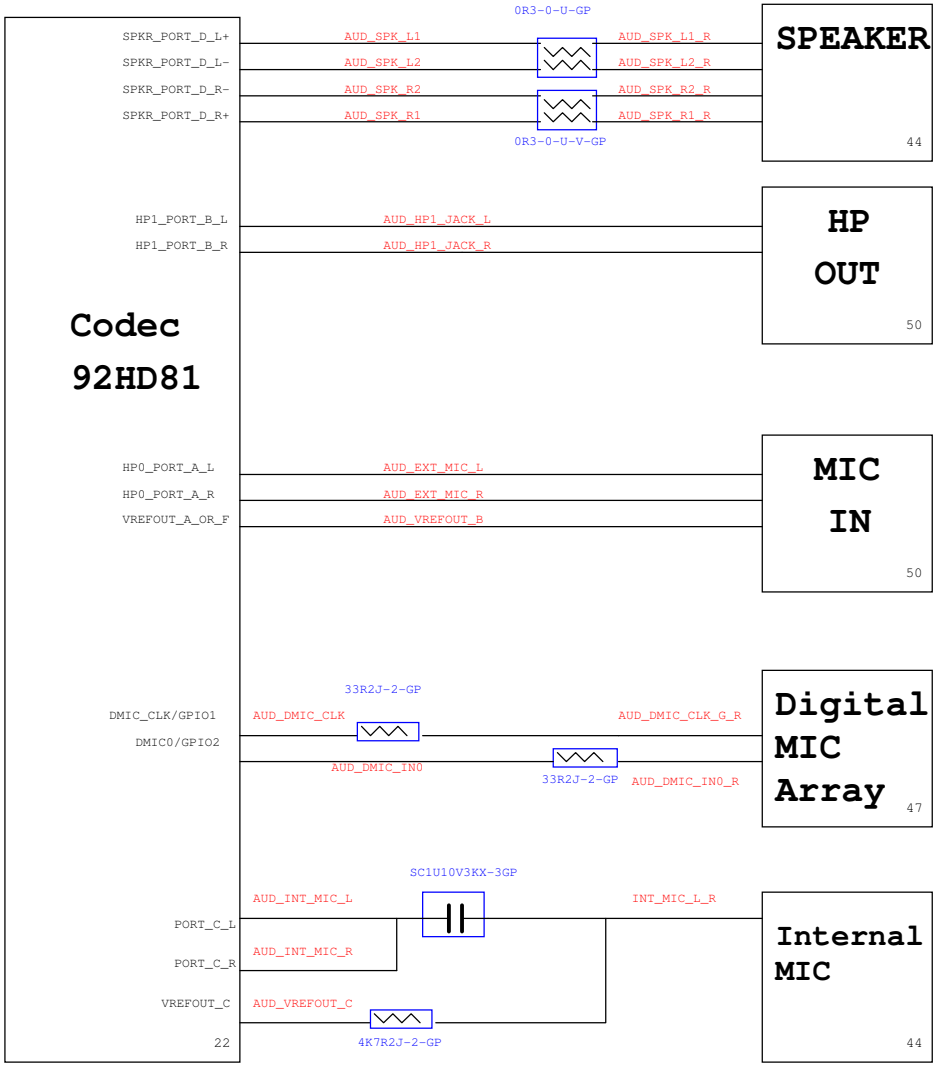
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

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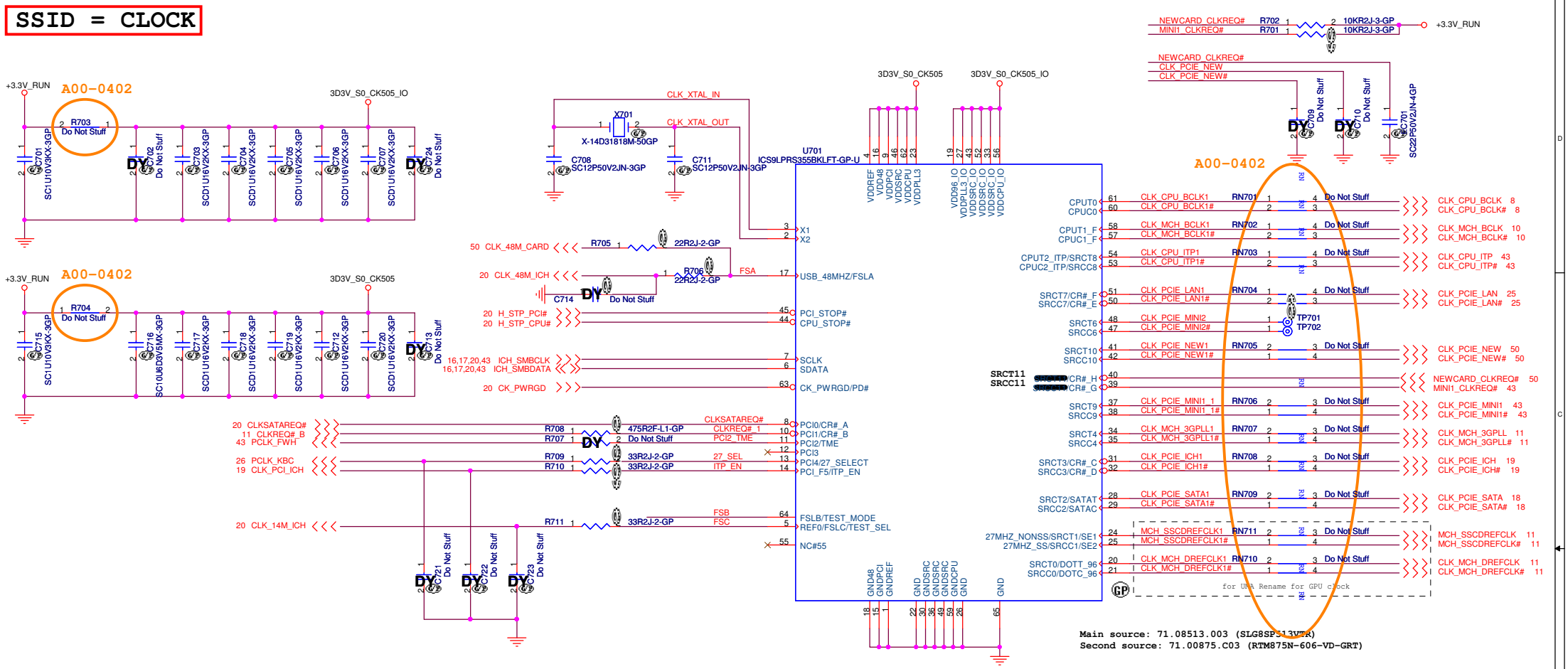
SSID = CLOCK



ITP_EN	Output
0	SRC8
1	CPU_ITP

PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

for UMA

27_SEL	PIN 20	PIN 21	
0	DOT96T	DOT96C	UMA
1	SRCT0	SRCC0	Discrete

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

8 CPU_BSEL2
8 CPU_BSEL1
8 CPU_BSEL0
R718 10KR2J-3-GP FSC
R719 0R2J-2-GP FSB
R720 2K2R2J-2-GP FSA
R721 1KR2J-1-GP MCH_CLKSEL0 11
R722 1KR2J-1-GP MCH_CLKSEL1 11
R723 1KR2J-1-GP MCH_CLKSEL2 11

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Title: Clock Generator SLG8SP513VTR

Size	Document Number	Rev
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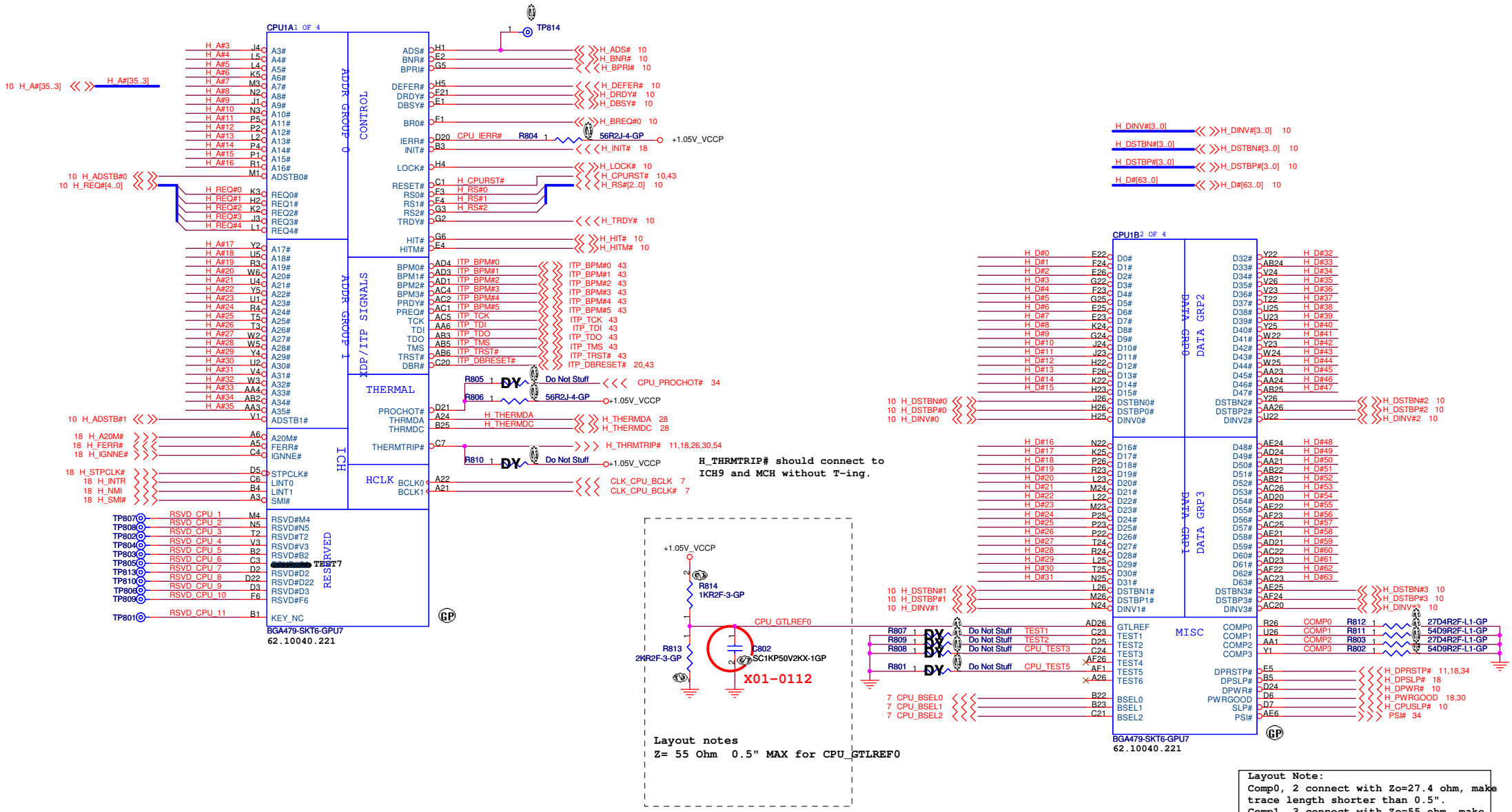
SSID = CPU



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Title: CPU-FSB(1/2)

Size	Document Number	Rev
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SSID = CPU

+VCC_CORE

X01-0106

C907 SC22U6D3V5MX-2GP

C914 SC22U6D3V5MX-2GP

X01-0106

C926 SC22U6D3V5MX-2GP

+1.05V_VCCP

CPU1C 3 OF 4

BGA479-SKT6-GPU7
62.10040.221

layout note: "+1.5V_VCCA" as short as possible

A00-0402

+1.5V_VCCA R903 Do Not Stuff +1.5V_RUN

C939 SCD01U16V2KX-3GP

C940 SC10U6D3V5MX-3GP

Layout Note:
Place as close as possible to the CPU VCCA pin.

CPU_VID[6..0] 34

R902 100R2F-L1-GP-U VCC_SENSE_1 PG902 Do Not Stuff +VCC_CORE

VCC_SENSE 34

R901 100R2F-L1-GP-U VSS_SENSE_1 PG901 Do Not Stuff

VSS_SENSE 34

VCC_SENSE and VSS_SENSE lines should be of equal length.

X01-0106

CPU1D 4 OF 4

BGA479-SKT6-GPU7
62.10040.221

NCTF PIN

CPU_GND1 TP902

CPU_GND2 TP901

CPU_GND3 TP903

CPU_GND4 TP904

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Title: CPU-Power(2/2)

Size: Custom | Document Number: Alba UMA | Rev: -1

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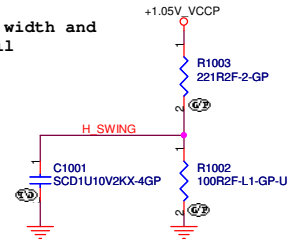
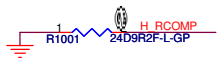
SSID = MCH

H_SWING routing Trace width and Spacing use 10 / 20 mil

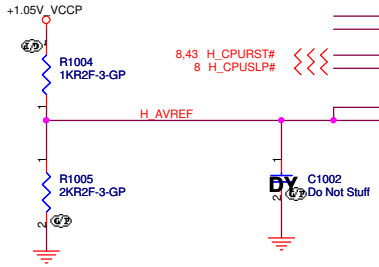
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)

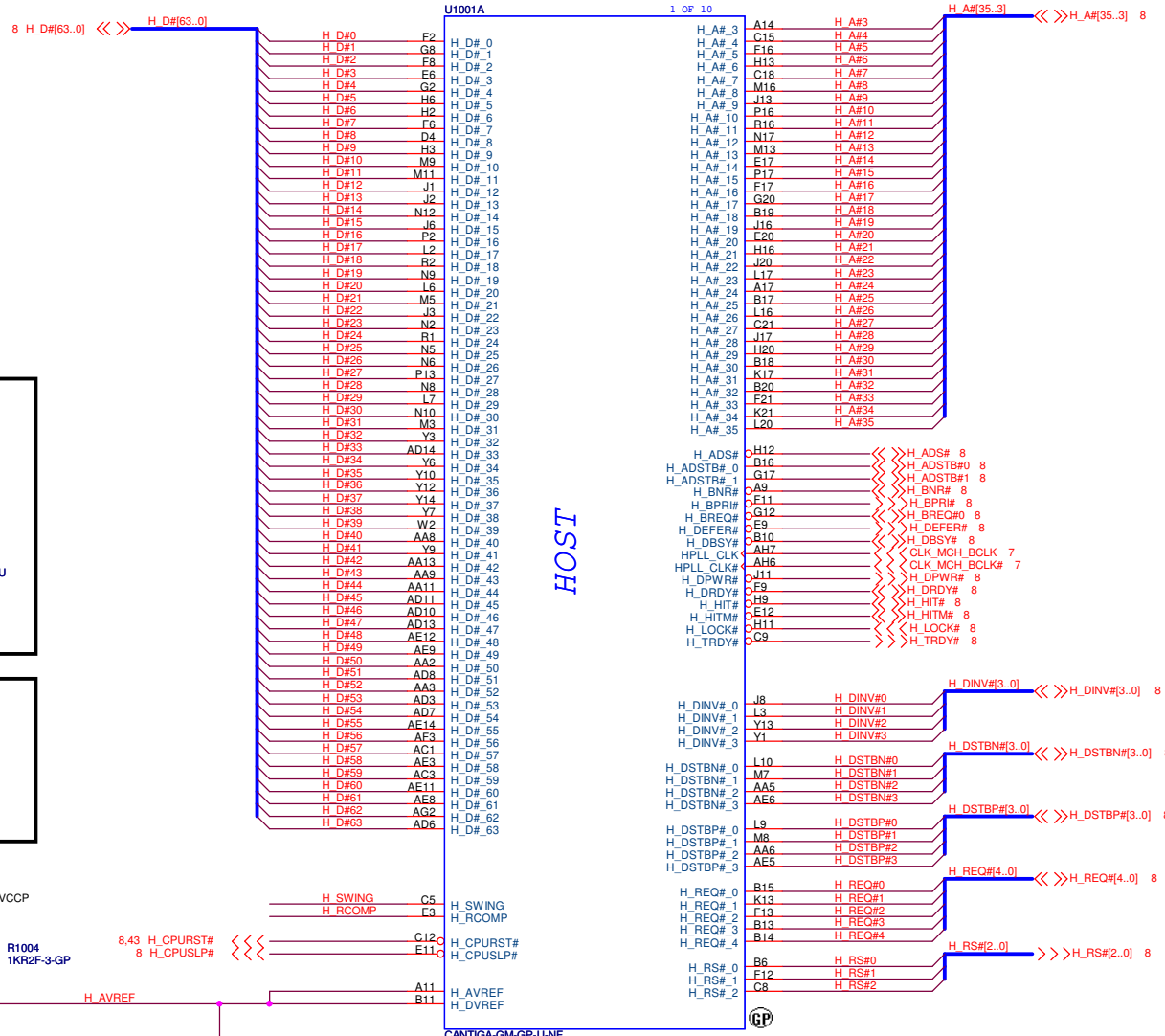


H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place R1001 near to the chip (< 0.5")





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Title: ***Cantiga-HOST(1/6)***

Size	Document Number	Rev
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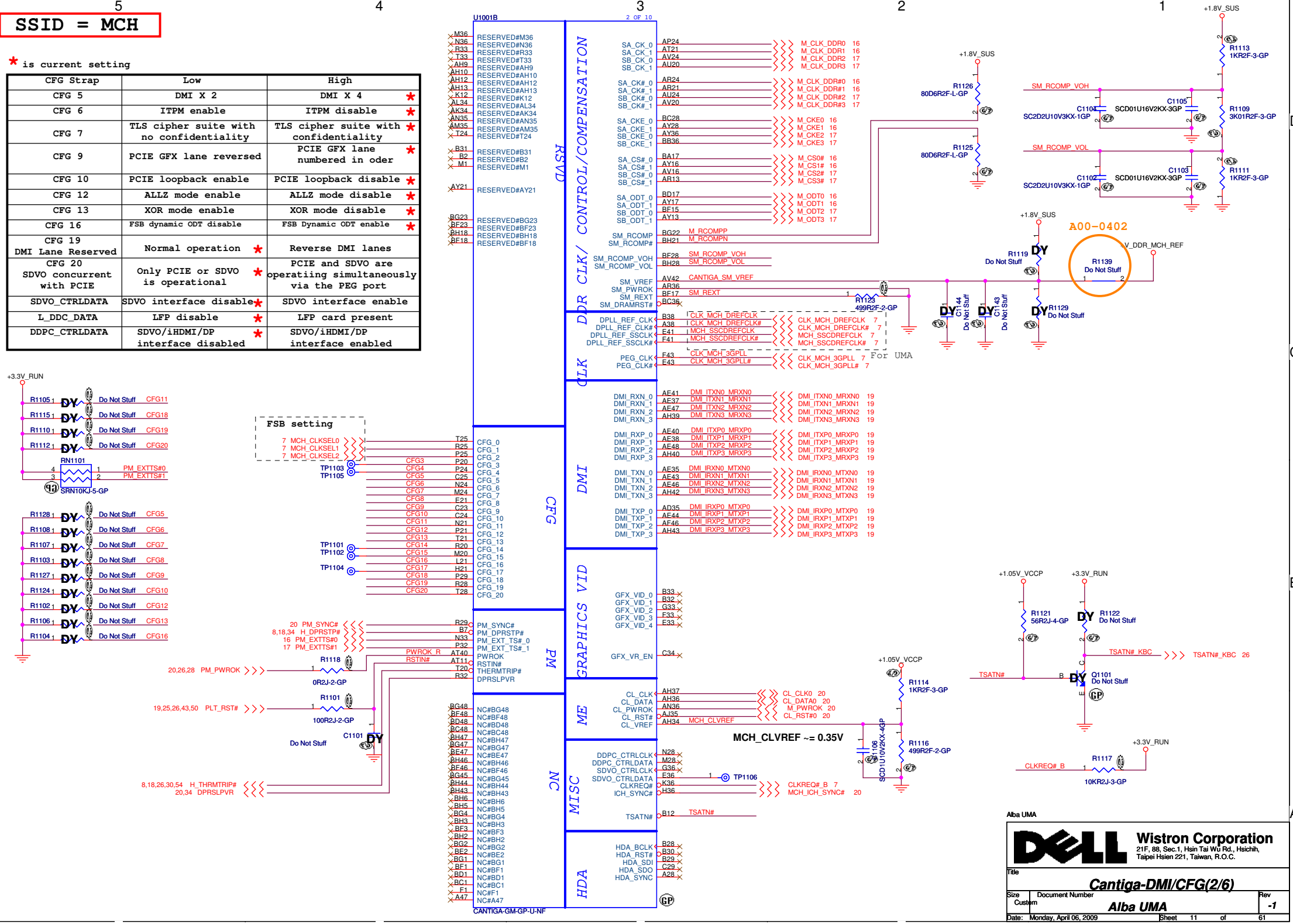
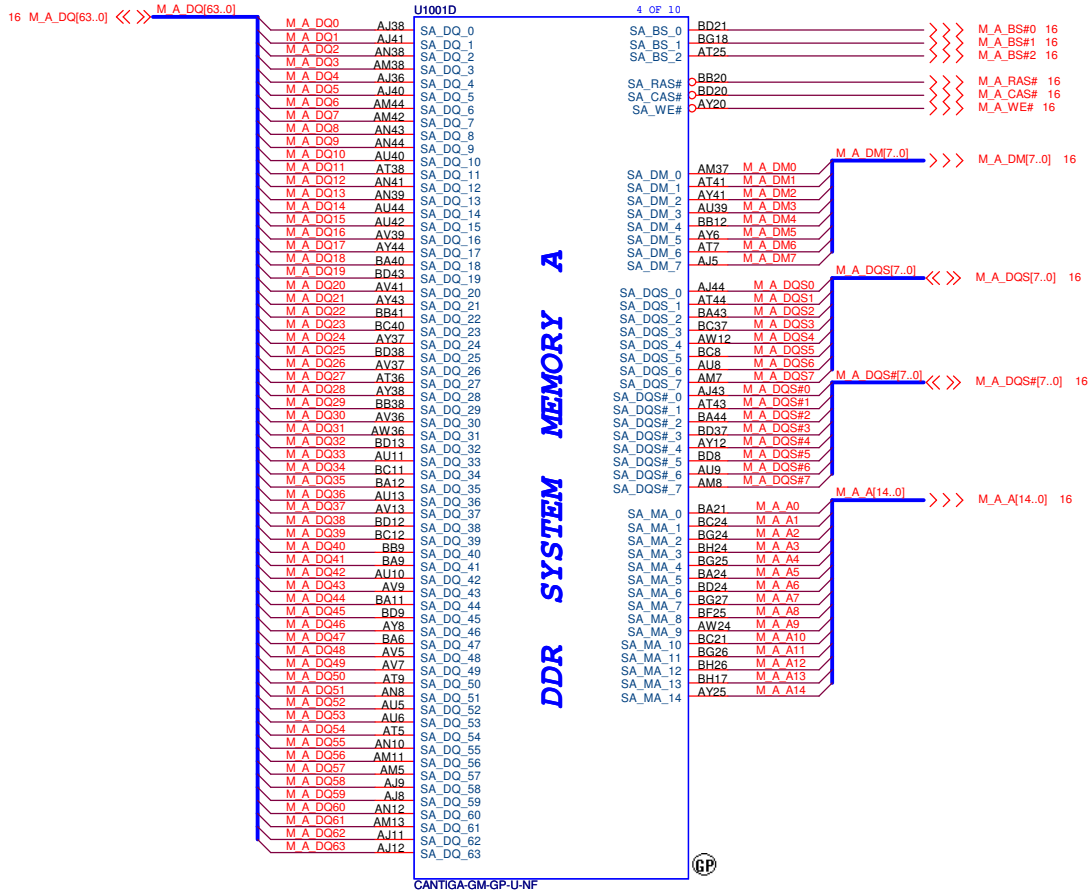
SSID = MCH

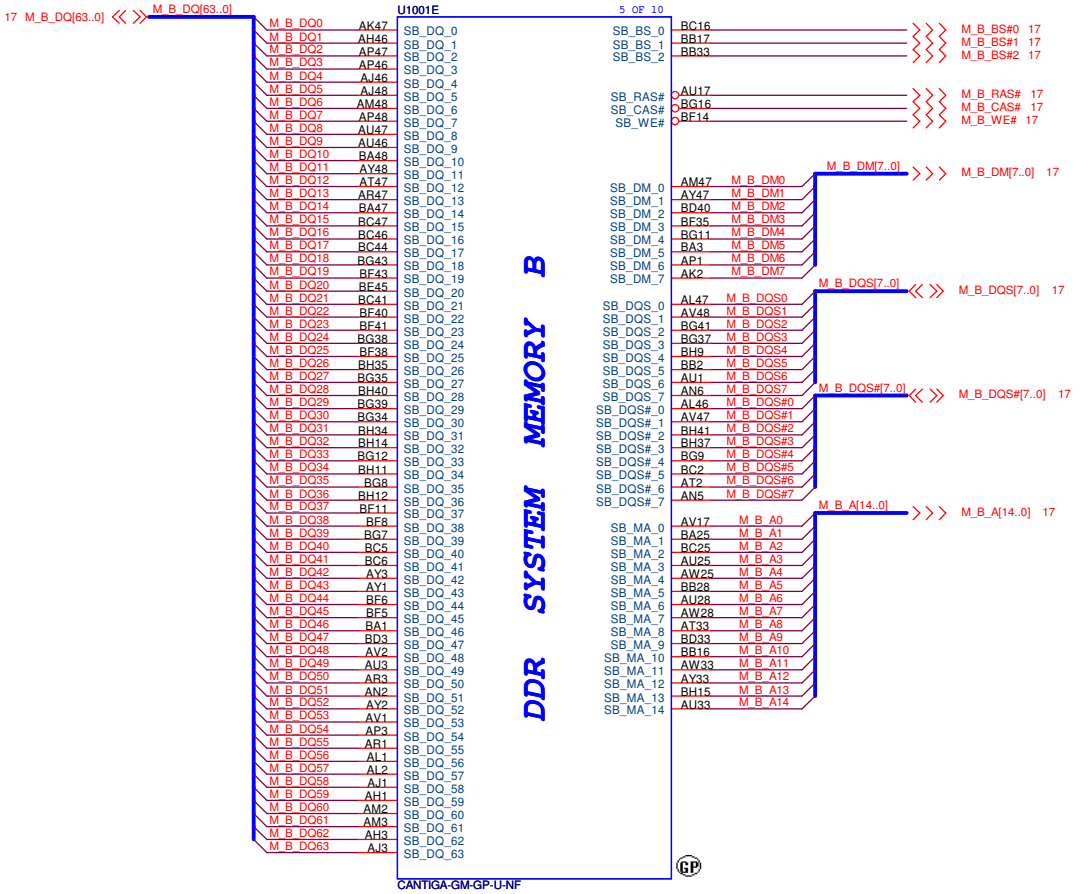
★ is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 ★
CFG 6	ITPM enable	ITPM disable ★
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality ★
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in oder ★
CFG 10	PCIE loopback enable	PCIE loopback disable ★
CFG 12	ALLZ mode enable	ALLZ mode disable ★
CFG 13	XOR mode enable	XOR mode disable ★
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable ★
CFG 19 DMI Lane Reserved	Normal operation ★	Reverse DMI lanes
CFG 20 SDVO concurrent with PCIE	Only PCIE or SDVO is operational ★	PCIE and SDVO are operatiing simultaneously via the PEG port
SDVO_CTRLDATA	SDVO interface disable ★	SDVO interface enable
L_DDC_DATA	LFP disable ★	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled ★	SDVO/iHDMI/DP interface enabled



SSID = MCH





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Title: Cantiga-DDR(3/6)

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SSID = MCH

U1001I — 9 OF 10 — CANTIGA-GM-GP-U-NF

U1001J — 10 OF 10 — CANTIGA-GM-GP-U-NF

VSS

VSS NCTF

VSS SCB

NC

NCTF PIN

U1001C — 3 OF 10 — CANTIGA-GM-GP-U-NF

PCI-EXPRESS GRAPHICS

LVDS

TV

VGA

UMA-SA

Place R1301 close to MCH within 500 mils.

CRT_IREF routing Trace width use 20 mil.

5V @ ext. CRT side

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Title: Cantiga-GND/LVDS/VGA(6/6)

Size: C | Document Number: Alba UMA | Rev: -1

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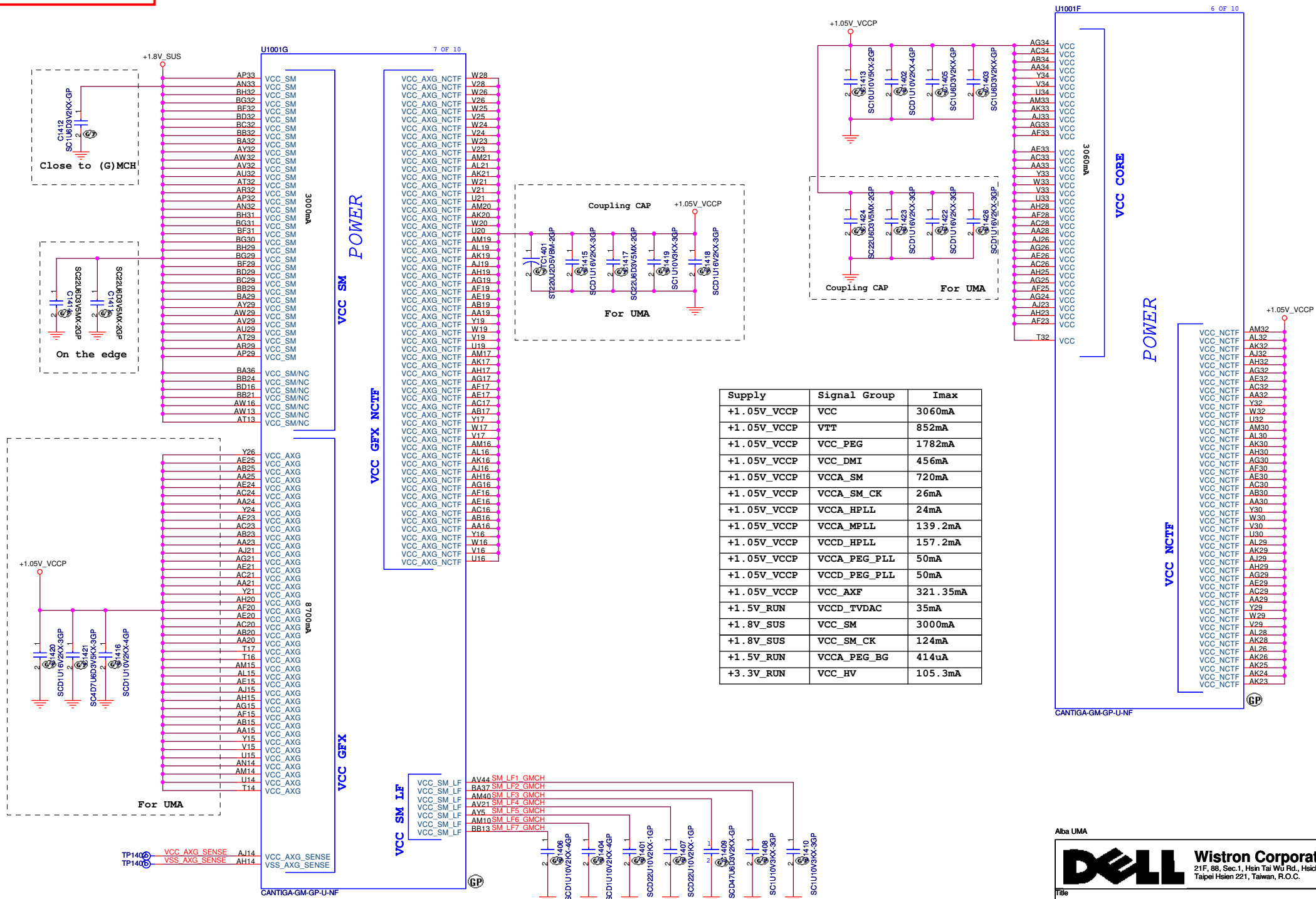
SSID = MCH



Supply	Signal Group	Imax
+1.05V_VCCP	VCC	3060mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

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Title: Cantiga-Power(4/6)

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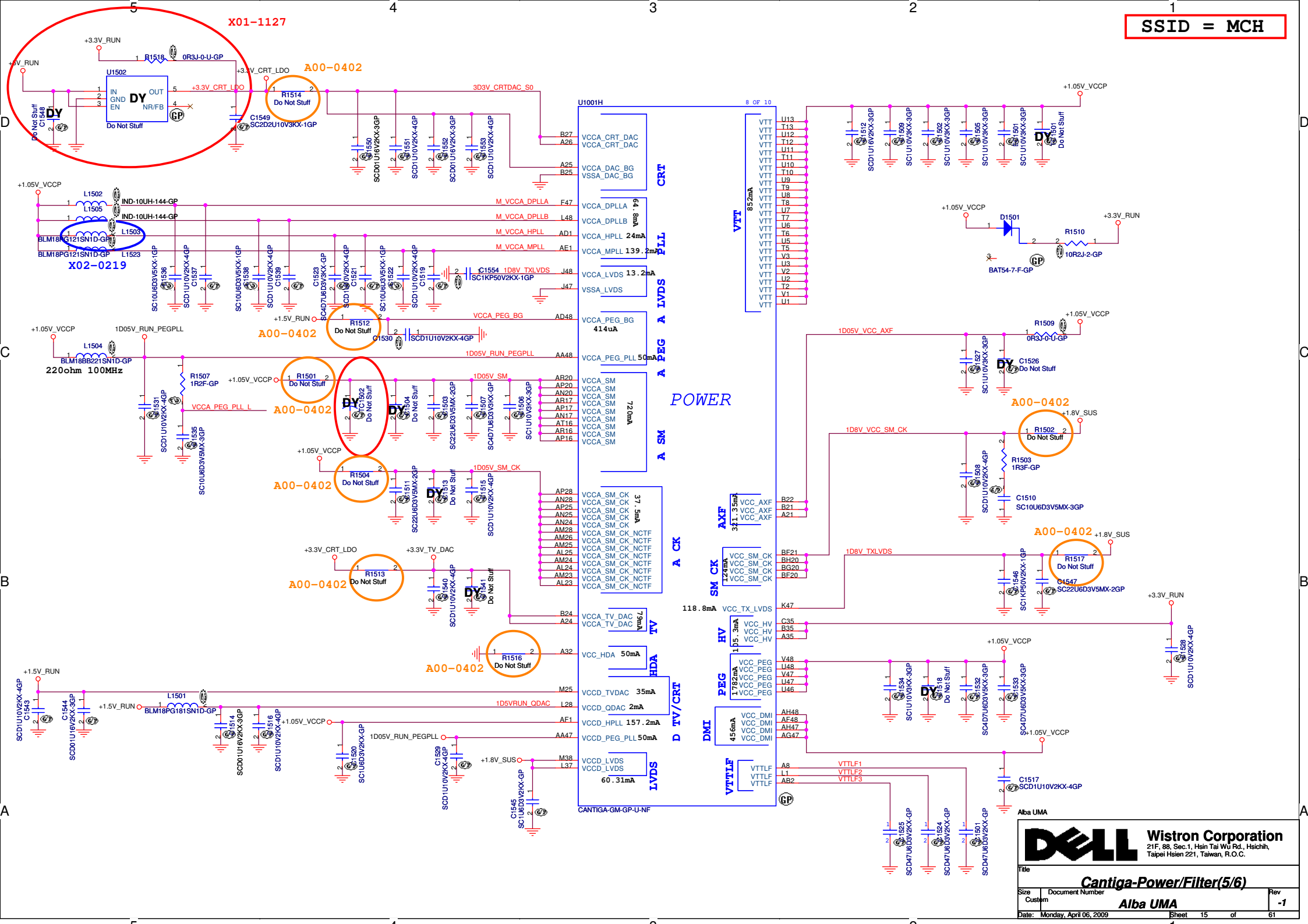
SSID = MCH
X01-1127
X02-0219
POWER
CANTIGA-GM-GP-U-NF
U1001H
8 OF 10
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
A00-0402
Do Not Stuff
DY
GP
Alba UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Cantiga-Power/Filter(5/6)
Size
Custom
Document Number
Alba UMA
Rev
-1
Date: Monday, April 06, 2009
Sheet 15 of 61

SSID = MEMORY

12 M_A_DQS#[7..0]
12 M_A_DQ[63..0]
12 M_A_DM[7..0]
12 M_A_DQS[7..0]
12 M_A_A[14..0]

DM1

12 M_A_BS#2
12 M_A_BS#0
12 M_A_BS#1

M_A_A0	102	A0	/RAS	108	M_A_RAS# 12
M_A_A1	101	A1	/WE	109	M_A_WE# 12
M_A_A2	100	A2	/CAS	113	M_A_CAS# 12
M_A_A3	99	A3	/CS0	110	M_CS0# 11
M_A_A4	98	A4	/CS1	115	M_CS1# 11
M_A_A5	97	A5	CKE0	79	M_CKE0 11
M_A_A6	94	A6	CKE1	80	M_CKE1 11
M_A_A7	92	A7	CK0	30	M_CLK_DDR0 11
M_A_A8	93	A8	/CK0	32	M_CLK_DDR#0 11
M_A_A9	91	A9	CK1	164	M_CLK_DDR1 11
M_A_A10	105	A10/AP	/CK1	166	M_CLK_DDR#1 11
M_A_A11	90	A11	DM0	10	M_A_DM0
M_A_A12	89	A12	DM1	26	M_A_DM1
M_A_A13	116	A13	DM2	52	M_A_DM2
M_A_A14	86	A14	DM3	67	M_A_DM3
	84	A15	DM4	130	M_A_DM4
M_A_BS#2	85	A16/BA2	DM5	147	M_A_DM5
M_A_BS#0	107	BA0	DM6	170	M_A_DM6
M_A_BS#1	106	BA1	DM7	185	M_A_DM7
M_A_DQ0	5	DQ0	SDA	195	ICH_SMBDATA
M_A_DQ1	7	DQ1	SCL	197	ICH_SMBCLK
M_A_DQ2	17	DQ2	VDDSPD	199	
M_A_DQ3	19	DQ3	SA0	198	
M_A_DQ4	4	DQ4	SA1	200	
M_A_DQ5	6	DQ5	NC#50	50	PM_EXTTS#0 11
M_A_DQ6	14	DQ6	NC#69	69	
M_A_DQ7	16	DQ7	NC#83	83	
M_A_DQ8	23	DQ8	NC#120	120	
M_A_DQ9	25	DQ9	NC#163/TEST	163	
M_A_DQ10	35	DQ10	VDD	81	
M_A_DQ11	37	DQ11	VDD	82	
M_A_DQ12	20	DQ12	VDD	87	
M_A_DQ13	22	DQ13	VDD	88	
M_A_DQ14	36	DQ14	VDD	95	
M_A_DQ15	38	DQ15	VDD	96	
M_A_DQ16	43	DQ16	VDD	103	
M_A_DQ17	45	DQ17	VDD	104	
M_A_DQ18	55	DQ18	VDD	111	
M_A_DQ19	57	DQ19	VDD	112	
M_A_DQ20	44	DQ20	VDD	117	
M_A_DQ21	46	DQ21	VDD	118	
M_A_DQ22	56	DQ22	VSS	3	
M_A_DQ23	58	DQ23	VSS	8	
M_A_DQ24	61	DQ24	VSS	9	
M_A_DQ25	63	DQ25	VSS	12	
M_A_DQ26	73	DQ26	VSS	15	
M_A_DQ27	75	DQ27	VSS	18	
M_A_DQ28	62	DQ28	VSS	21	
M_A_DQ29	64	DQ29	VSS	24	
M_A_DQ30	74	DQ30	VSS	27	
M_A_DQ31	76	DQ31	VSS	28	
M_A_DQ32	123	DQ32	VSS	33	
M_A_DQ33	125	DQ33	VSS	34	
M_A_DQ34	135	DQ34	VSS	39	
M_A_DQ35	137	DQ35	VSS	40	
M_A_DQ36	124	DQ36	VSS	41	
M_A_DQ37	126	DQ37	VSS	42	
M_A_DQ38	134	DQ38	VSS	47	
M_A_DQ39	136	DQ39	VSS	48	
M_A_DQ40	141	DQ40	VSS	53	
M_A_DQ41	143	DQ41	VSS	54	
M_A_DQ42	151	DQ42	VSS	59	
M_A_DQ43	153	DQ43	VSS	60	
M_A_DQ44	140	DQ44	VSS	65	
M_A_DQ45	142	DQ45	VSS	66	
M_A_DQ46	152	DQ46	VSS	71	
M_A_DQ47	154	DQ47	VSS	72	
M_A_DQ48	157	DQ48	VSS	77	
M_A_DQ49	159	DQ49	VSS	78	
M_A_DQ50	173	DQ50	VSS	121	
M_A_DQ51	175	DQ51	VSS	122	
M_A_DQ52	158	DQ52	VSS	127	
M_A_DQ53	160	DQ53	VSS	128	
M_A_DQ54	174	DQ54	VSS	132	
M_A_DQ55	176	DQ55	VSS	133	
M_A_DQ56	179	DQ56	VSS	138	
M_A_DQ57	181	DQ57	VSS	139	
M_A_DQ58	189	DQ58	VSS	144	
M_A_DQ59	191	DQ59	VSS	145	
M_A_DQ60	180	DQ60	VSS	149	
M_A_DQ61	182	DQ61	VSS	150	
M_A_DQ62	192	DQ62	VSS	155	
M_A_DQ63	194	DQ63	VSS	156	
M_A_DQS#0	11	/DQS0	VSS	161	
M_A_DQS#1	29	/DQS1	VSS	162	
M_A_DQS#2	49	/DQS2	VSS	165	
M_A_DQS#3	68	/DQS3	VSS	168	
M_A_DQS#4	129	/DQS4	VSS	171	
M_A_DQS#5	146	/DQS5	VSS	172	
M_A_DQS#6	167	/DQS6	VSS	177	
M_A_DQS#7	186	/DQS7	VSS	178	
M_A_DQS0	13	DQS0	VSS	183	
M_A_DQS1	31	DQS1	VSS	184	
M_A_DQS2	51	DQS2	VSS	187	
M_A_DQS3	70	DQS3	VSS	190	
M_A_DQS4	131	DQS4	VSS	193	
M_A_DQS5	148	DQS5	VSS	196	
M_A_DQS6	169	DQS6	VSS	201	
M_A_DQS7	188	DQS7			
M_ODT0	114	ODT0			
M_ODT1	119	ODT1			
	1	VREF			
	2	VSS			
	202	GND			

11 M_ODT0
11 M_ODT1

DDR2-200P-10-U1
62.10017.881

Height 6.5mm

ALBA X00

+3.3V_RUN
+1.8V_SUS
+0.9V_DDR_VTT
+V_DDR_MCH_REF

C1602 SCD1U16V2KX-3GP
DY C1601 Do Not Stuff

C1626 SCD1U16V2KX-3GP
DY C1625 Do Not Stuff

put near connector

M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1

DY C1603 Do Not Stuff
DY C1604 Do Not Stuff
DY C1623 Do Not Stuff
DY C1624 Do Not Stuff

Layout Note:
Place near SKT1

+1.8V_SUS

DY C1620 SC1U10V3KX-3GP
C1619 SC1U10V3KX-3GP
DY C1622 Do Not Stuff
DY C1621 Do Not Stuff
C1616 SC1U10V3KX-3GP
DY C1607 Do Not Stuff
C1613 SCD1U16V2KX-3GP
C1609 SC1U6D3V2KX-GP
C1612 SCD1U16V2KX-3GP
DY C1601 Do Not Stuff

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT.

+0.9V_DDR_VTT

DY C1610 Do Not Stuff
C1627 SCD1U16V2KX-3GP
DY C1611 Do Not Stuff
C1608 SCD1U16V2KX-3GP
DY C1605 Do Not Stuff
DY C1630 Do Not Stuff
C1606 SCD1U16V2KX-3GP
DY C1614 Do Not Stuff
DY C1617 Do Not Stuff
C1618 SCD1U16V2KX-3GP
C1615 SCD1U16V2KX-3GP
C1629 SCD1U16V2KX-3GP
C1628 SCD1U16V2KX-3GP

Layout Note:
Place these resistors close to DM1,
all trace length Max=1.5".

+0.9V_DDR_VTT

RN1601 SRN56J-5-GP
M_A_A5
M_A_A8
M_A_A9
M_A_A12

RN1605 SRN56J-4-GP
M_CKE0
M_A_BS#2

R1663 56R2J-4-GP
M_A_A13

RN1602 SRN56J-5-GP
M_ODT0
M_CS0#
M_A_BS#1
M_A_RAS#

RN1606 SRN56J-5-GP
M_A_A3
M_A_A1
M_A_A10
M_A_BS#0

RN1603 SRN56J-5-GP
M_ODT1
M_CS1#
M_A_CAS#
M_A_WE#

RN1607 SRN56J-5-GP
M_A_A7
M_A_A11
M_A_A14
M_CKE1

RN1604 SRN56J-5-GP
M_A_A0
M_A_A2
M_A_A4
M_A_A6

Alba UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT1

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 16 of 61

SSID = MEMORY

12 M_B_DQS#[7..0]
12 M_B_DQ[63..0]
12 M_B_DM[7..0]
12 M_B_DQS[7..0]
12 M_B_A[14..0]

DM2

DDR2-200P-33-GP

Height 11mm

put near connector
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3
C1703 Do Not Stuff
C1704 Do Not Stuff
C1718 Do Not Stuff
C1719 Do Not Stuff

ALBA X00

Layout Note:
Place near SKT2
+1.8V_SUS
C1716 SCU10V3KX-3GP
DY C1707 Do Not Stuff
C1711 SCU10V3KX-3GP
C1712 SCU10V3KX-3GP
C1710 SCU10V3KX-3GP
C1714 SCD1U10V2KX-4GP
DY C1717 Do Not Stuff
C1709 SC1U6D3V2KX-GP
C1715 SC1U6D3V2KX-GP
DY C1701 Do Not Stuff

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT.
+0.9V_DDR_VTT
DY C1729 Do Not Stuff
C1726 SCD1U16V2KX-3GP
C1728 SCD1U16V2KX-3GP
DY C1727 Do Not Stuff
C1725 SCD1U16V2KX-3GP
C1723 SCD1U16V2KX-3GP
C1722 SCD1U16V2KX-3GP
C1706 SCD1U16V2KX-3GP
C1724 SCD1U16V2KX-3GP
DY C1713 Do Not Stuff
C1705 SCD1U16V2KX-3GP
DY C1721 Do Not Stuff
C1708 SCD1U16V2KX-3GP

Layout Note:
Place these resistors close to DM2,
all trace length Max=1.5".
+0.9V_DDR_VTT
RN1701 SRN56J-3-GP
RN1702 SRN56J-3-GP
RN1703 SRN56J-3-GP
RN1704 SRN56J-3-GP
RN1705 SRN56J-3-GP
RN1706 SRN56J-3-GP
RN1707 SRN56J-3-GP

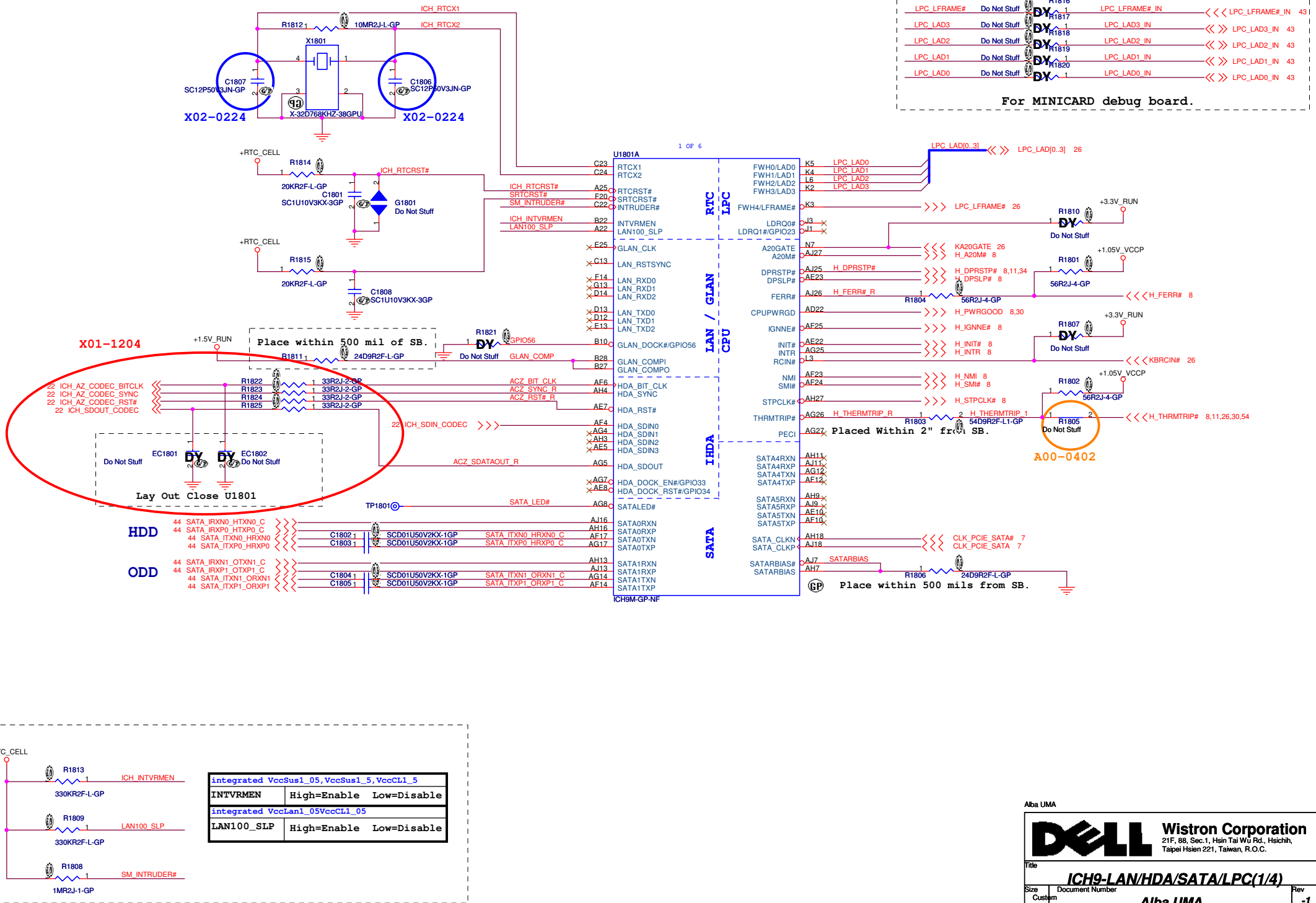
+V_DDR_MCH_REF
C1730 SCD1U16V2KX-3GP
C1720 SC2D2U10V3KX-1GP

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT2
Size: Custom | Document Number: Alba UMA | Rev: -1
Date: Monday, April 06, 2009 | Sheet 17 of 61

SSID = ICH



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-LAN/HDA/SATA/LPC(1/4)

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 18 of 61

SSID = ICH

U1801E — 5 OF 6 — ICH9M-GP-NF

U1902 — DY — Do Not Stuff — R1907 — A00-0402

U1801B — 2 OF 6 — PCI / Interrupt I/F — ICH9M-GP-NF

RN1905 / RN1901 / RN1902 / RN1906 / RN1904 — SRN8K2J-4-GP

RP1901 — SRN10KJ-L3-GP

RN1903 — SRN8K2J-4-GP

R1910 / R1911 / R1909 — DY — Do Not Stuff

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	

U1801D — 4 OF 6 — PCI-Express / Direct Media Interface / SPI / USB — ICH9M-GP-NF

Mini Card — LAN — New Card

R1908 24D9R2F-L-GP (+1.5V_RUN)

R1912 22D6R2F-L-GP

NCTF PIN

USB Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Alba UMA

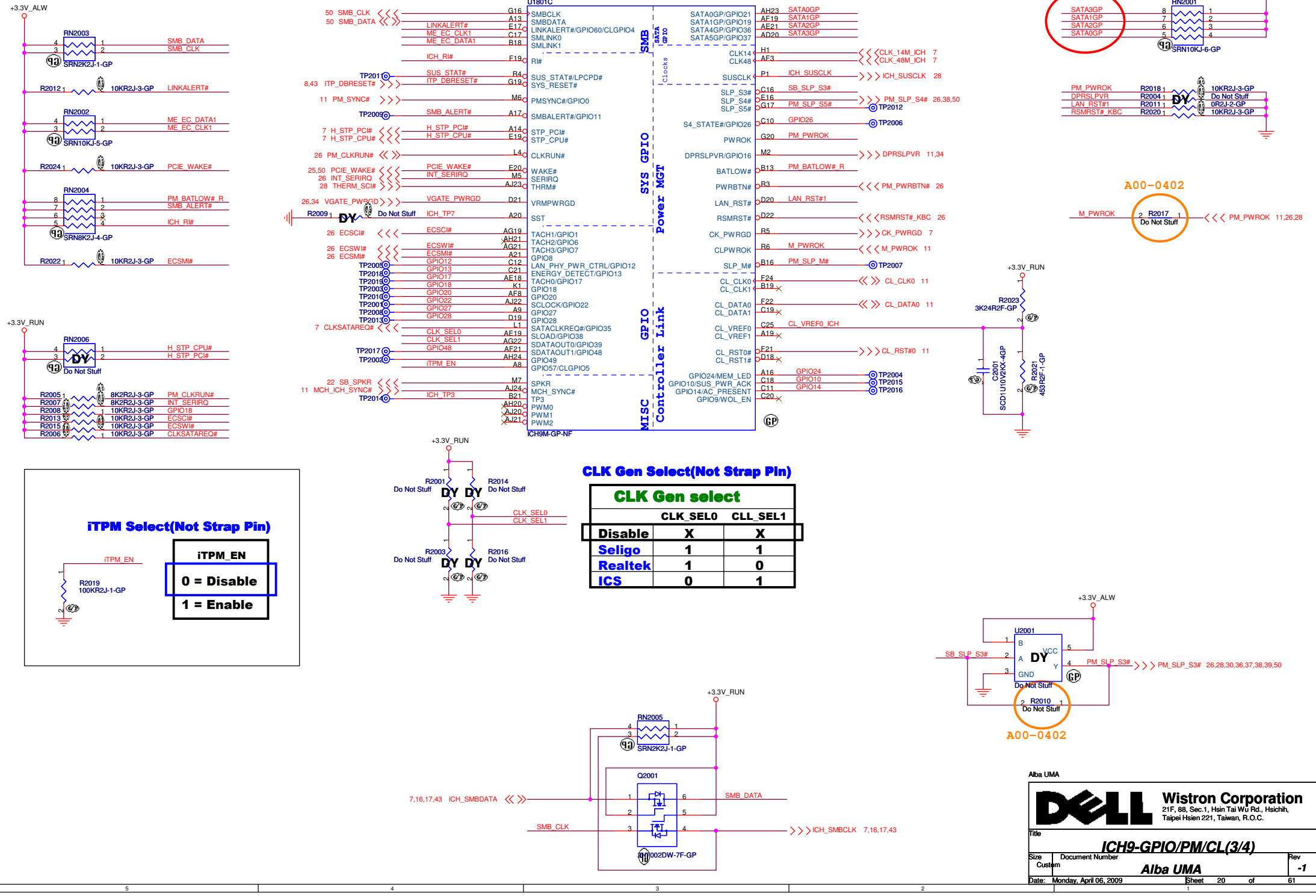
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-PCI/PCIE/DMI/USB/GND(2/4)

Size: Custom | Document Number: Alba UMA | Rev: -1

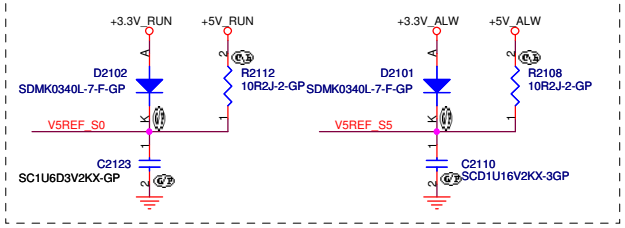
Date: Monday, April 06, 2009 | Sheet 19 of 61

SSID = ICH


X01-1223
A00-0402
A00-0402
3 OF 6
U1801C
ICH9M-GP-NF
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
RN2003
SMB_DATA
SMB_CLK
SRN2K2J-1-GP
R2012 10KR2J-3-GP LINKALERT#
RN2002
ME_EC_DATA1
ME_EC_CLK1
SRN10KJ-5-GP
R2024 10KR2J-3-GP PCIE_WAKE#
RN2004
PM_BATLOW#_R
SMB_ALERT#
ICH_RI#
SRN8K2J-4-GP
R2022 10KR2J-3-GP ECSMI#
RN2006
H_STP_CPU#
H_STP_PCI#
Do Not Stuff
R2005 8K2R2J-3-GP PM_CLKRUN#
R2007 8K2R2J-3-GP INT_SERIRQ
R2008 10KR2J-3-GP GPIO18
R2013 10KR2J-3-GP ECSCI#
R2015 10KR2J-3-GP ECSWI#
R2006 10KR2J-3-GP CLKSATAREQ#
RN2001
SRN10KJ-6-GP
R2018 10KR2J-3-GP PM_PWROK
R2004 Do Not Stuff DPRSLPVR
R2011 0R2J-2-GP LAN_RST#1
R2020 10KR2J-3-GP RSMRST#_KBC
R2017 Do Not Stuff M_PWROK
R2023 3K24R2F-GP
C2001 SCD1U10V2KX-4GP
R2021 453R2F-1-GP
R2001 Do Not Stuff
R2014 Do Not Stuff
R2003 Do Not Stuff
R2016 Do Not Stuff
CLK_SEL0
CLK_SEL1
iTPM Select(Not Strap Pin)
iTPM_EN
R2019 100KR2J-1-GP
iTPM_EN
0 = Disable
1 = Enable
CLK Gen Select(Not Strap Pin)
CLK Gen select
Disable X X
Seligo 1 1
Realtek 1 0
ICS 0 1
U2001
SB_SLP_S3#
PM_SLP_S3#
Do Not Stuff
R2010 Do Not Stuff
RN2005
SRN2K2J-1-GP
Q2001
2002DW-7F-GP
7,16,17,43 ICH_SMBDATA
SMB_DATA
SMB_CLK
ICH_SMBCLK 7,16,17,43
Alba UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-GPIO/PM/CL(3/4)
Size Custom
Document Number Alba UMA
Rev -1
Date: Monday, April 06, 2009
Sheet 20 of 61

SSID = ICH

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail



U1801F
6 OF 6
ICH9M-GP-NF

+RTC_CELL
C2155 SCD1U10V2KX-4GP
C2156 SCD1U10V2KX-4GP
V5REF_S0
V5REF_S5
A23 VCCRTC
A6 V5REF 2mA
AE1 V5REF_SUS 2mA

AA24 AA25 AB24 AB25 AC24 AC25 AD24 AD25 AE25 AE26 AE27 AE28 AE29 F25 G25 H24 H25 J24 J25 K24 K25 L23 L24 L25 M24 M25 N23 N24 N25 P24 P25 R24 R25 R26 R27 T24 T27 T28 T29 U24 U25 V24 V25 U23 W24 W25 K23 Y24 Y25 VCC1_5_B

646mA

+1.5V_RUN
+1.5V_PCIE_ICH
R2109 Do Not Stuff
A00-0402
C2137 Do Not Stuff
C2149 Do Not Stuff
C2101 Do Not Stuff
C2112 SC1U6D3V5MX-3GP
C2111 SC1U6D3V5MX-3GP
C2113 SC2D2U10V3KX-1GP

+3.3V_RUN
R2110 Do Not Stuff
SB_VCCLAN3_3
A00-0402
C2124 SCD1U10V2KX-4GP
C2120 Do Not Stuff

+1.5V_RUN
R2121 Do Not Stuff
VCC_GLAN_PLL
A00-0402
C2122 SC2D2U10V3KX-1GP
C2126 SC1U6D3V5MX-3GP

+1.5V_RUN
+VCCSATAPLL
L2101 L-10UH-11-GP
C2101 SC1U6D3V5MX-3GP
C2103 SC1U10V3KX-3GP

AJ19 VCCSATAPLL 47mA
AC16 AD15 AD16 AE15 AF15 AG15 AH15 AJ15 VCC1_5_A

+1.5V_RUN
C2132 SC1U6D3V2KX-GP
C2104 SC1U6D3V2KX-GP

AC11 AD11 AE11 AF11 AG10 AH10 AJ10 AC9 AC18 AC19 AC21 G10 G9 AC12 AC13 AC14 VCC1_5_A

1424mA

+1.5V_RUN
R2105 Do Not Stuff
A00-0402
1D5V_USB_S0
C2106 Do Not Stuff
C2133 SCD1U10V2KX-4GP
C2134 SCD1U10V2KX-4GP

AJ5 VCCUSBPLL 11mA
AA7 AB6 AB7 AC6 AC7 VCC1_5_A

VCCLAN1D05
C2154 Do Not Stuff
A10 A11 VCCLAN1_05
A12 B12 VCCLAN3_3 78mA
SB_VCCLAN3_3
A27 VCCGLANPLL 23mA
VCC_GLAN_PLL

+1.5V_RUN
C2118 SC4D7U6D3V3KX-GP
C2119 Do Not Stuff
+3.3V_RUN
D28 D29 E26 E27 VCCGLAN1_5
A26 VCCGLAN3_3 1mA

VCCRTC
V5REF 2mA
V5REF_SUS 2mA
CORE
1634mA
23mA VCCDMIPLL
50mA VCCDMI
2mA V_CPU_IO
VCC3_3
AD19 AF20 AG24 AC20
VCCP_CORE
308mA
PCI
11mA VCCHDA
11mA VCCSUSHDA
AREK
VCCSUS1_05
VCCSUS1_5
VCCSUS3_3
VCCSUS3_3_ALK
VCCP_USB
212mA
VCCCL1_05
VCCCL1_5
VCCCL3_3
73mA
USB CORE
80mA
GLAN POWER

A15 B15 C15 D15 E15 F15 L11 L12 L14 L16 L17 L18 M11 M18 P11 P18 T11 T18 U11 U18 V11 V12 V14 V16 V17 V18 VCC1_05

SB_VCC1_05
C2143 Do Not Stuff
C2144 SC1U10V2KX-1GP
C2142 SC1U10V2KX-1GP
C2140 Do Not Stuff
C2145 SC1U6D3V2KX-GP
R2115 Do Not Stuff
R2116 Do Not Stuff
+1.05V_VCCP
A00-0402

1D5V_DMIPLL_ICH_S0
C2116 SCD01U16V2KX-3GP
C2117 SC10U6D3V5MX-3GP
L2102 COIL-1UH-31-GP
+1.5V_RUN

VCCDMI
C2136 SCD1U10V2KX-4GP
C2114 SC10U6D3V5MX-3GP
C2115 SC4D7U6D3V3KX-GP
R2117 Do Not Stuff
+1.05V_VCCP
A00-0402

AB23 AC23 SB_V_CPU_IO

AG29 AJ6 AC10 AD19 AF20 AG24 AC20 VCC3_3

C2131 SCD1U10V2KX-4GP
C2107 SCD1U10V2KX-4GP
C2128 SCD1U10V2KX-4GP
+3.3V_RUN

B9 F9 G3 G6 J2 J7 K7 VCC3_3

C2105 SCD1U10V2KX-4GP
+3.3V_RUN
C2146 SCD1U10V2KX-4GP
C2147 SCD1U10V2KX-4GP
C2153 SCD1U10V2KX-4GP
+3.3V_RUN

AJ4 VCCHDA
AJ3 VCCSUSHDA
AC8 VCCSUS1_05[1]
F17 VCCSUS1_05[2]
TP2101
TP2102
R2101 Do Not Stuff
AD8 VCCSUS1_5[1]
F18 VCCSUS1_5[2]
R2107 Do Not Stuff
A00-0402
+1.5V_RUN
+3.3V_ALW
C2102 SCD1U10V2KX-4GP
C2152 SCD1U10V2KX-4GP

A18 D16 D17 E22 AF1 T1 T2 T3 T4 T5 T6 U6 U7 V6 V7 W6 W7 Y6 Y7 T7 VCCSUS3_3

SB_VCCSUS3_3
C2125 SCD1U10V2KX-4GP
C2127 Do Not Stuff
C2121 Do Not Stuff
R2111 Do Not Stuff
A00-0402
+3.3V_ALW

ICH9_SUS3_3
C2141 SCD1U10V2KX-4GP
C2139 SCD1U16V2KX-3GP
C2138 SCD022U16V2KX-3GP
R2118 Do Not Stuff
A00-0402
+3.3V_ALW

G22 G23 A24 B24 VCCCL1_5

VCCSUS1_05[3]
VCCSUS1_5[3]
C2150 Do Not Stuff
C2148 SCD1U10V2KX-4GP
C2151 SCD1U10V2KX-4GP
R2120 Do Not Stuff
A00-0402
+3.3V_RUN
SB_VCCCL3_3

+1.05V_VCCP
SB_V_CPU_IO
C2129 SCD1U10V2KX-4GP
C2130 Do Not Stuff
C2108 SC4D7U6D3V3KX-GP
R2114 Do Not Stuff
A00-0402

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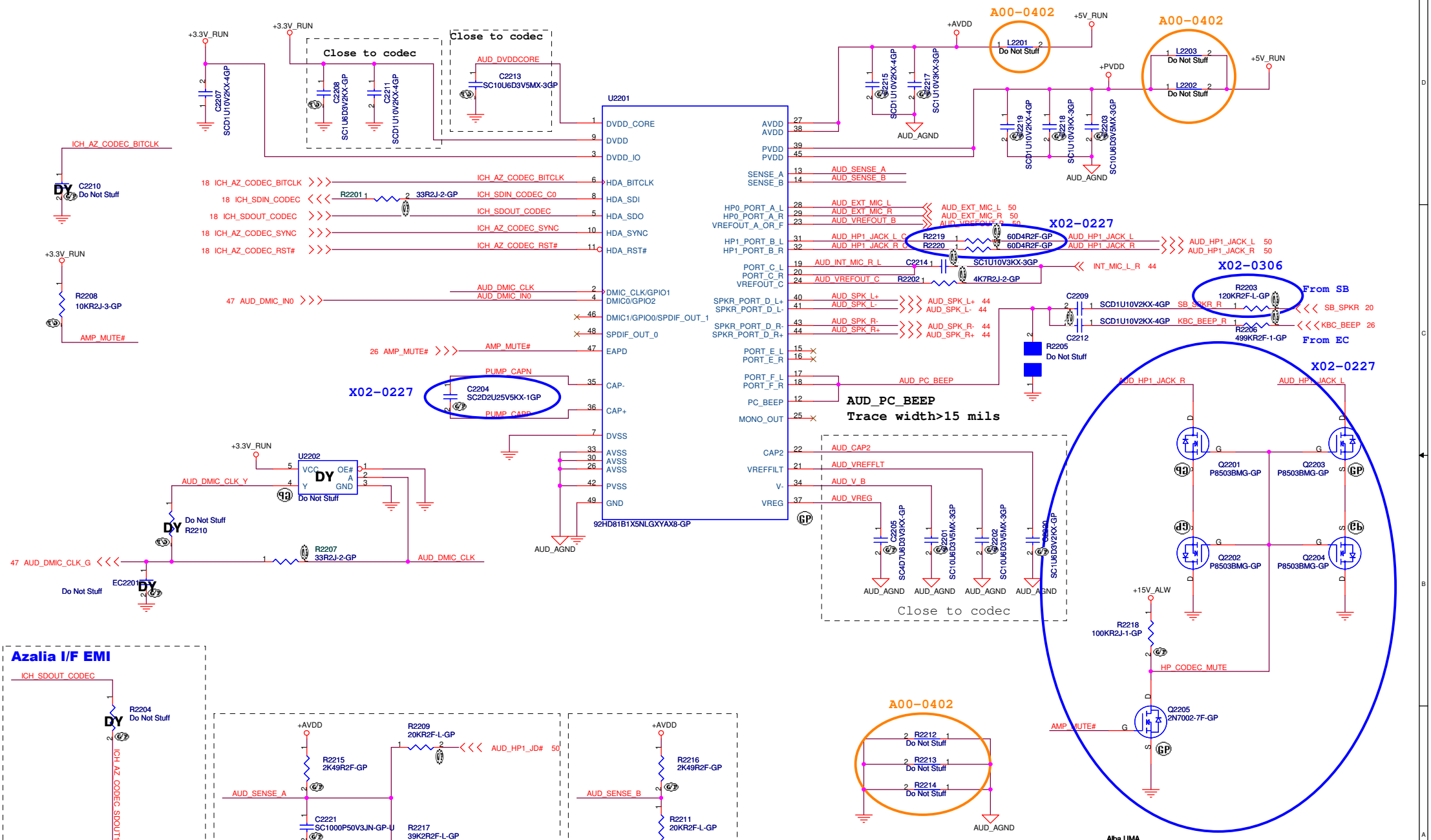
Title: ICH9-POWER(4/4)
Size: Custom
Document Number: Alba UMA
Rev: -1
Date: Monday, April 06, 2009
Sheet 21 of 61

SSID = AUDIO



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC 92HD81**

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 22 of 61

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Title: *(Reserve)*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 23 of 61

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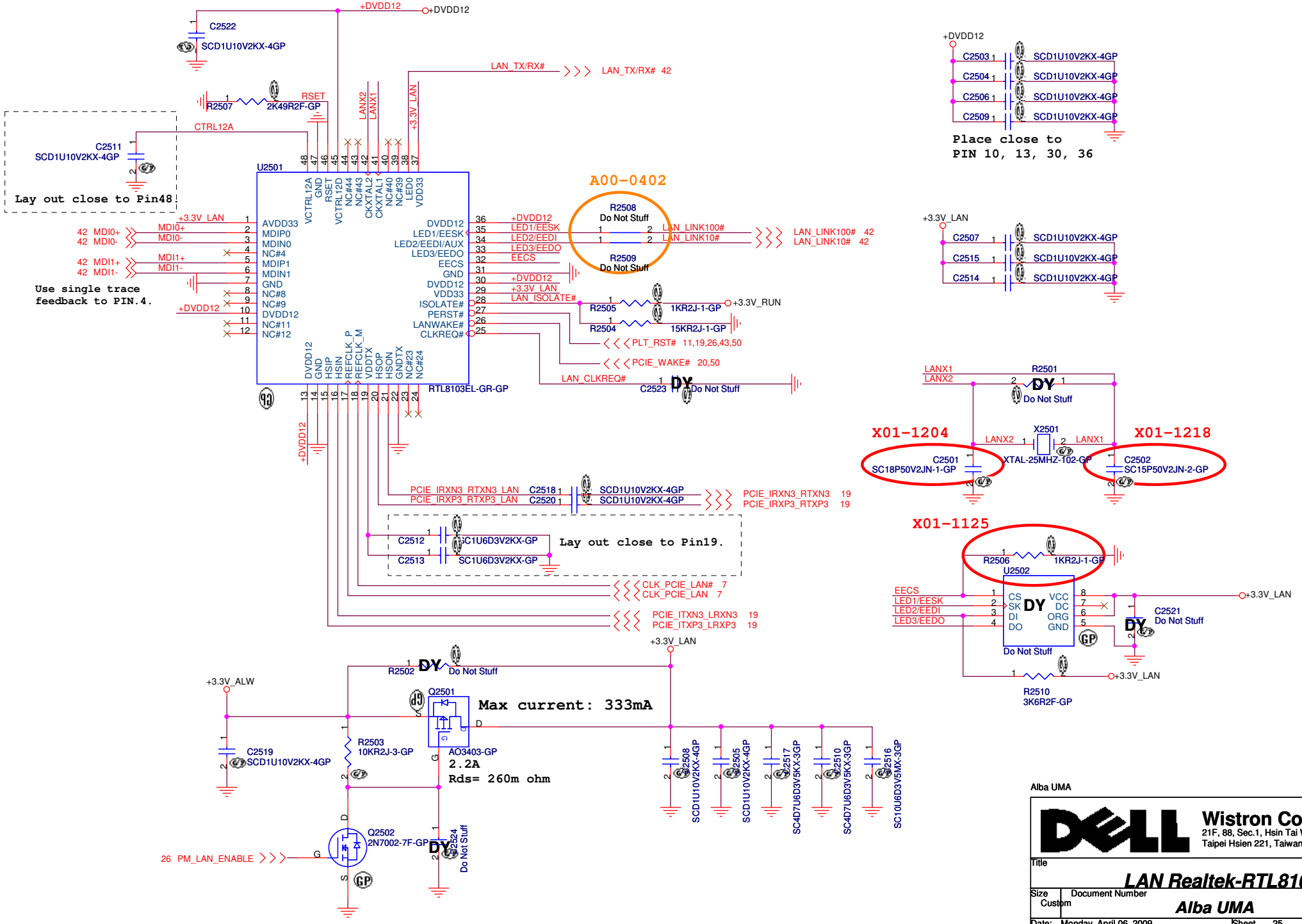
Title: *(Reserve)*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 24 of 61

SSID = LOM



Alba UMA

DELL

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **LAN Realtek-RTL8102EL**

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 25 of 61

SSID = KBC

Put 0.1uf close to VCC-GND pin pair.

Pull High : Discrete
internal Pull Low for UMA

X01-0113

A00-0402

X02-0227

X02-0225

X02-0303

X02-0219

X01-1215

X02-0224

MB VERSION ID

MB VERSION ID	VER2	VER1	VER0
SA	0	0	1
SB	0	1	0
SC	0	1	0
-1	0	1	1

ALBA X00

KBC CLK EMI

KBC

PS/2

FIU

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Alba UMA

Title: KBC Winbond WPC773L

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 26 of 61

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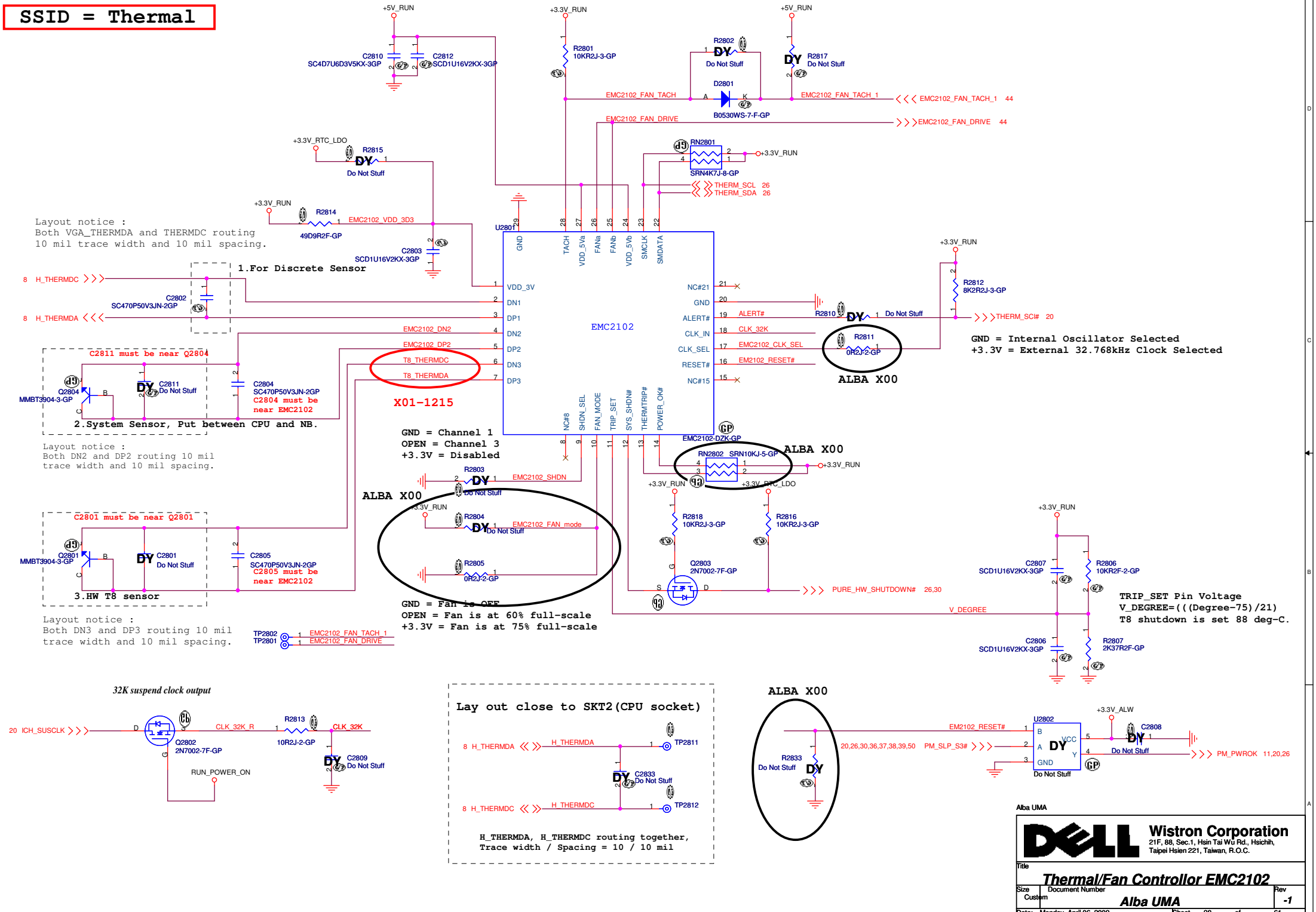
Title: *(Reserve)*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 27 of 61

SSID = Thermal



Alba UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 28 of 61

(Blank)

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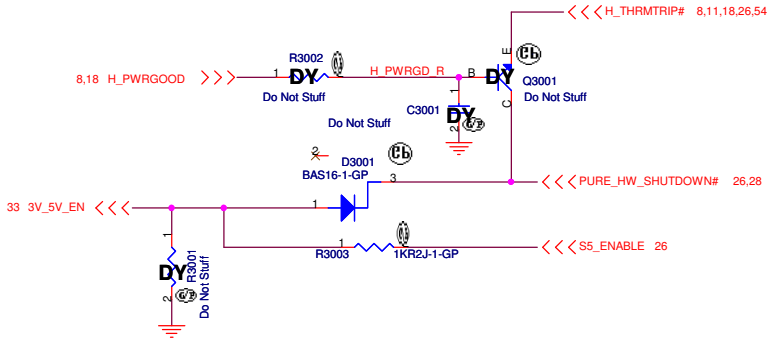
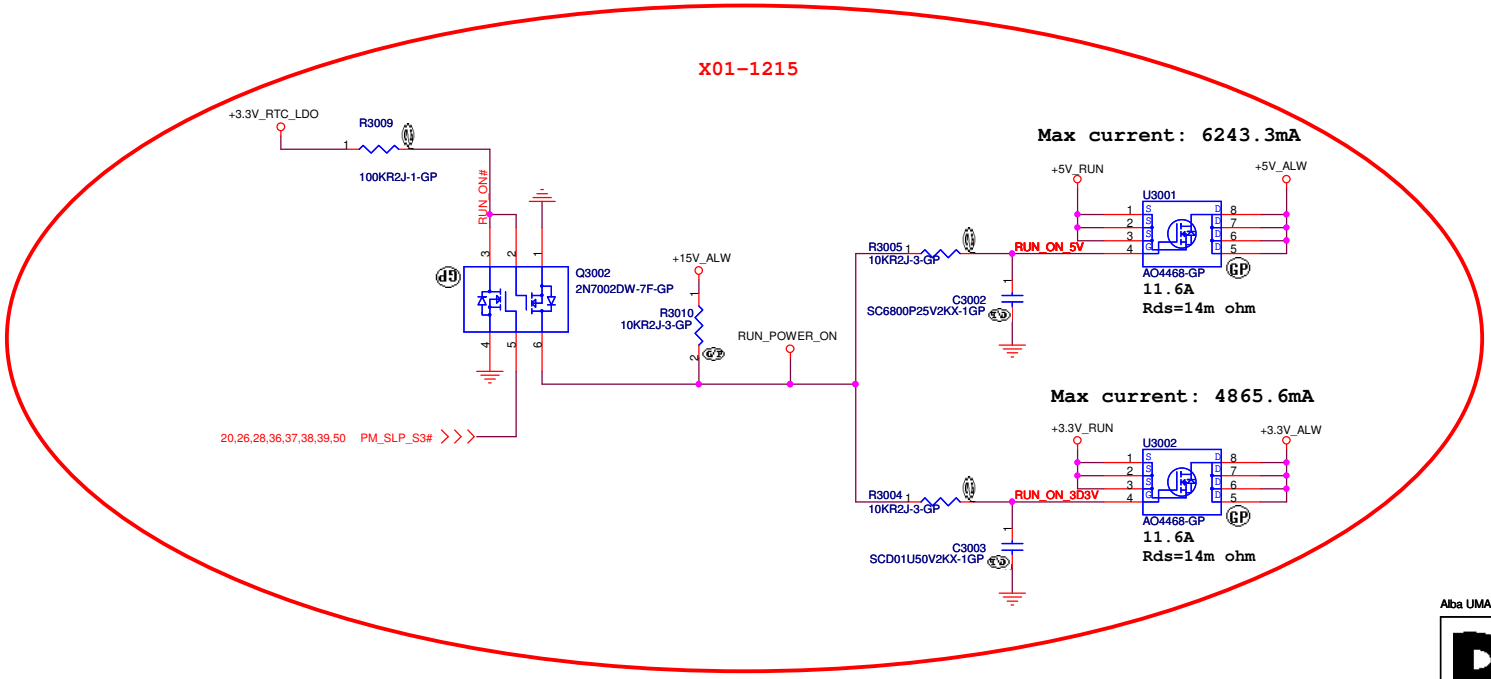
Title: *(Reserve)*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 29 of 61

SSID = Reset.Suspend





Alba UMA

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Taipei Hsien 221, Taiwan, R.O.C.

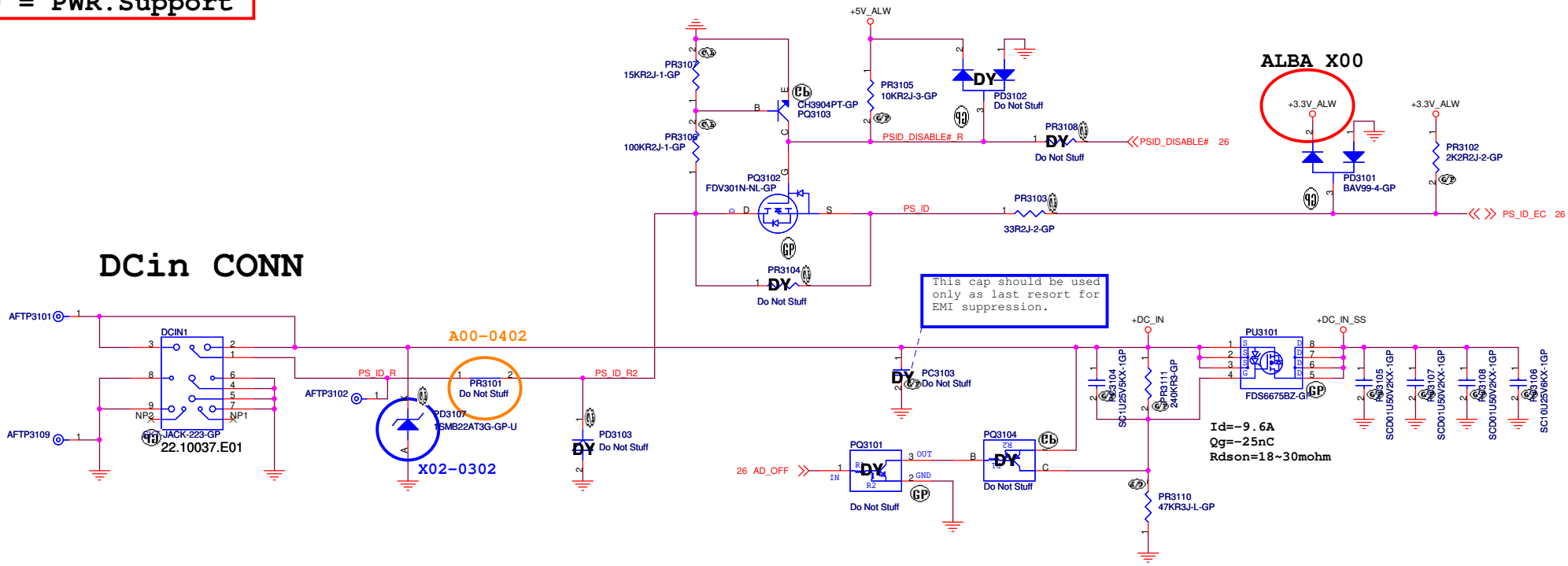
Title: ***Power Plane Enable***

Size	Document Number	Rev
Custom	***Alba UMA***	*-1*

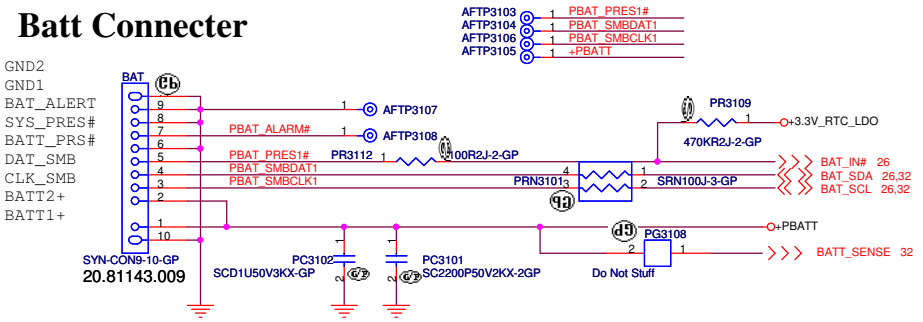
Date: Monday, April 06, 2009 Sheet 30 of 61

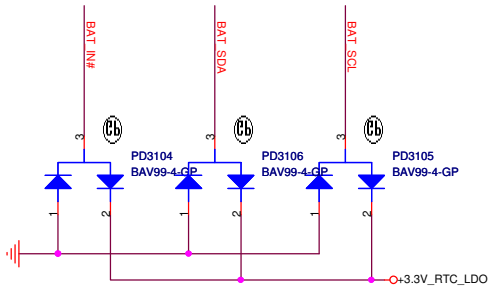
SSID = PWR.Support

DCin CONN



Batt Connecter





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Taipei Hsien 221, Taiwan, R.O.C.

Title: DC IN/BATT CONN/USB CONN

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 31 of 61

SSID = Charger

Adaptor In Soft-Start Circuit

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm
Layout Trace 250mil

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm
Layout Trace 300mil

Layout Trace 300mil

Layout Trace 300mil

X02-0302

X02-0302

A00-0402

A00-0402

A00-0402

A00-0402

A00-0402

A00-0402

X01-1219

TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR3202	PR3205	PR3207	PR3208
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR6326 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor

ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor

Note 2: 24.9K at PR6326 allows the 65W adaptor setting to switch down to 45W. (now is 33.2K for 90W)

Note 3: PR6302 must be 5m ohm instead of 10m ohm for the 230W adaptor

ADAPT_TRIP_SEL=1 Adapter is 90w

ADAPT_TRIP_SEL=0 Adapter is 65w

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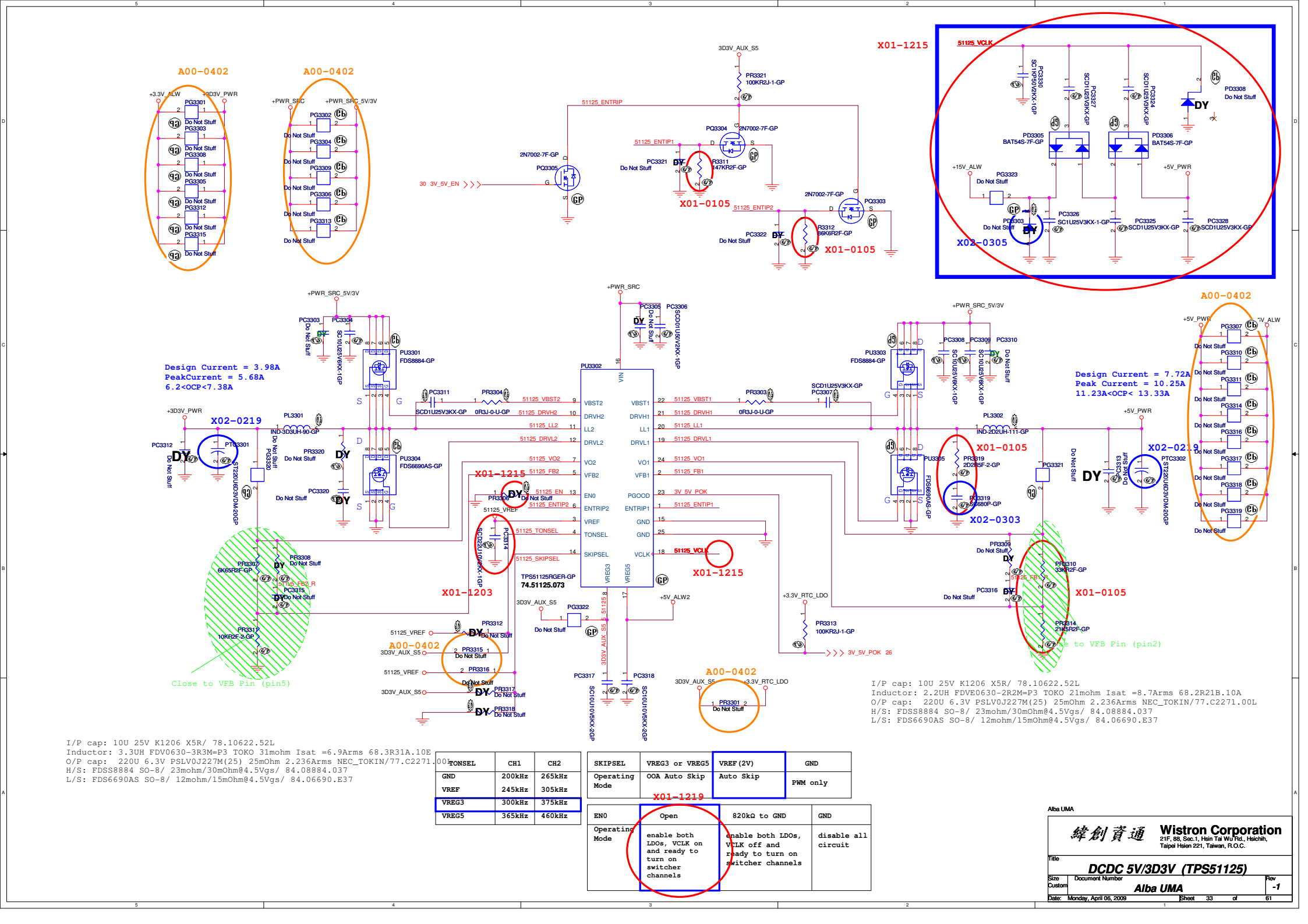
Title: CHARGER MAX8731

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 32 of 61



TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

Alba UMA

Wistron Corporation
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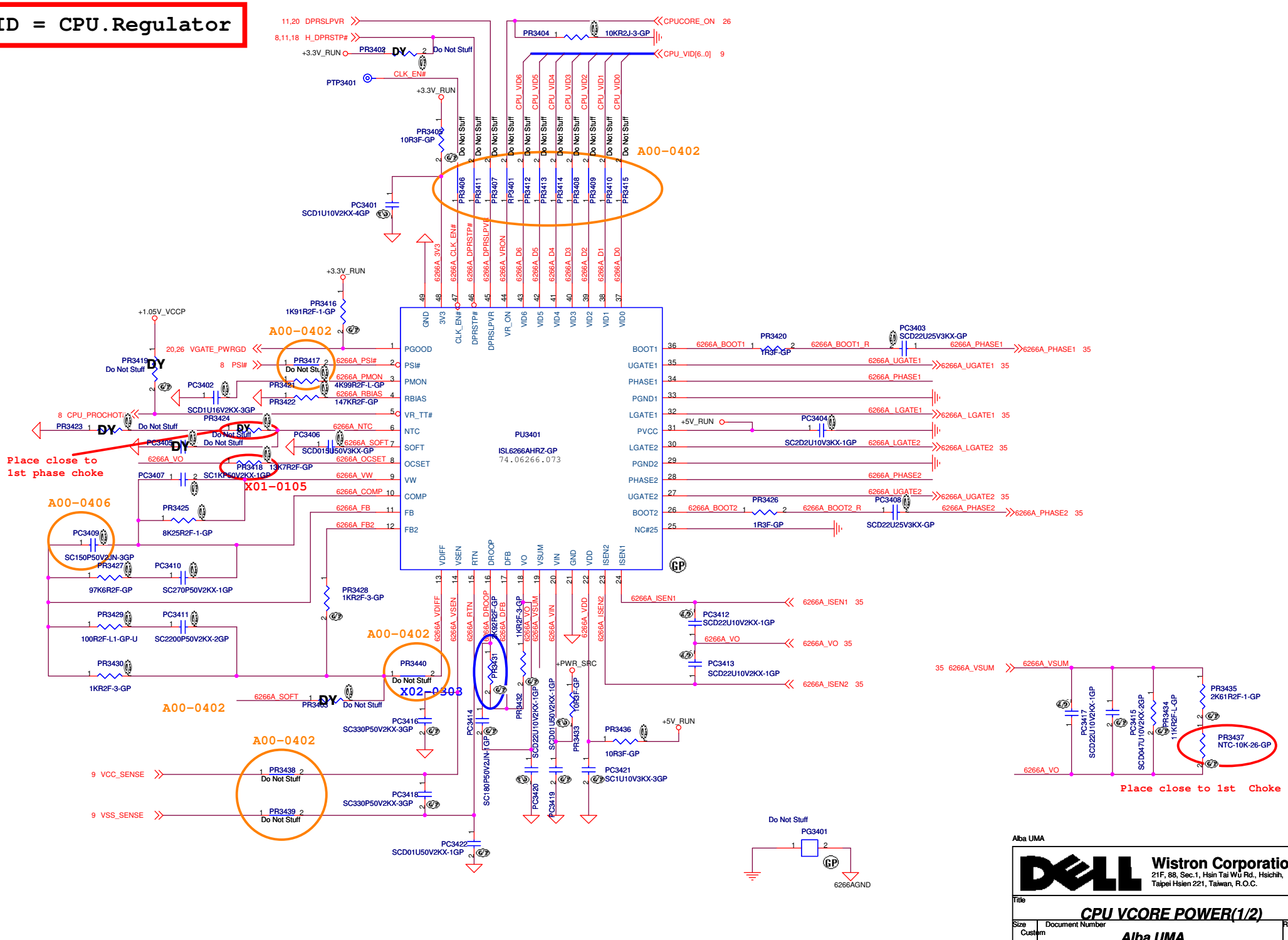
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 5V/3D3V (TPS51125)

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 33 of 61

SSID = CPU.Regulator



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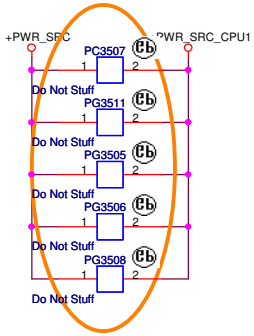
Taipei Hsien 221, Taiwan, R.O.C.

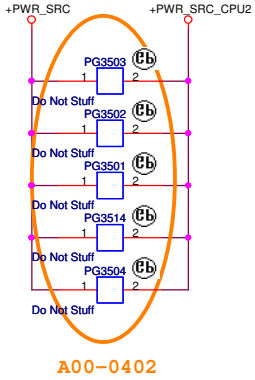
Title: CPU VCORE POWER(1/2)

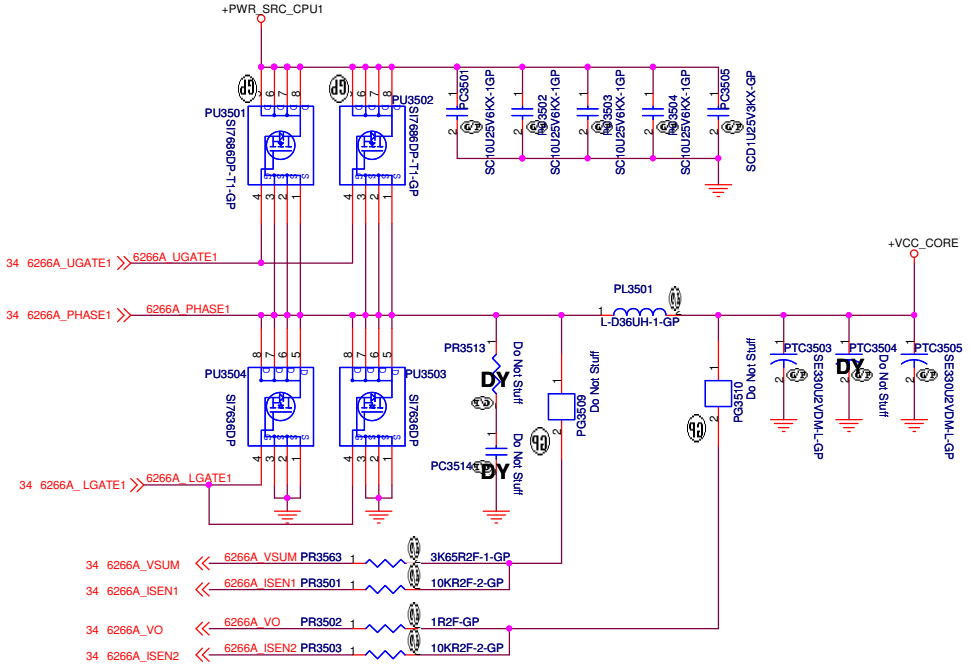
Size: Custom | Document Number: Alba UMA | Rev: -1

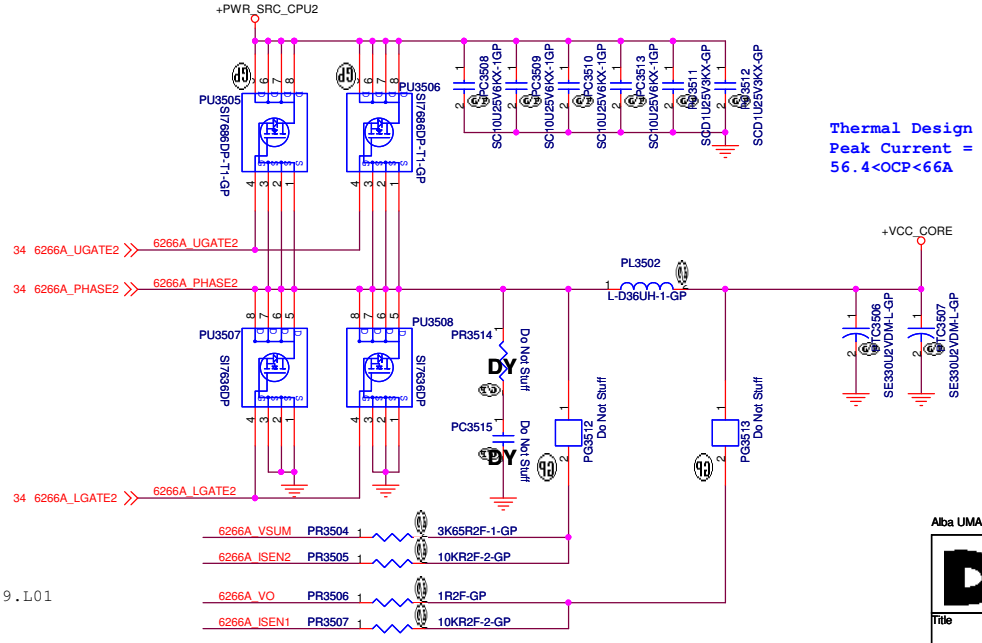
Date: Monday, April 06, 2009 | Sheet 34 of 61

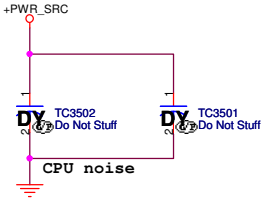
SSID = CPU.Regulator











Thermal Design Current = 36A(IMVP6+ Rev:1.35)
Peak Current = 47A
56.4<OCP<66A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: SI7686DP/ POWERPAK-8/ 14mOhm/ 4.5Vgs/ 84.07686.037
L/S: SI7636ADP/ POWERPAK-8/ 4.8mOhm/ 4.5Vgs/ 84.07636.037

Alba UMA

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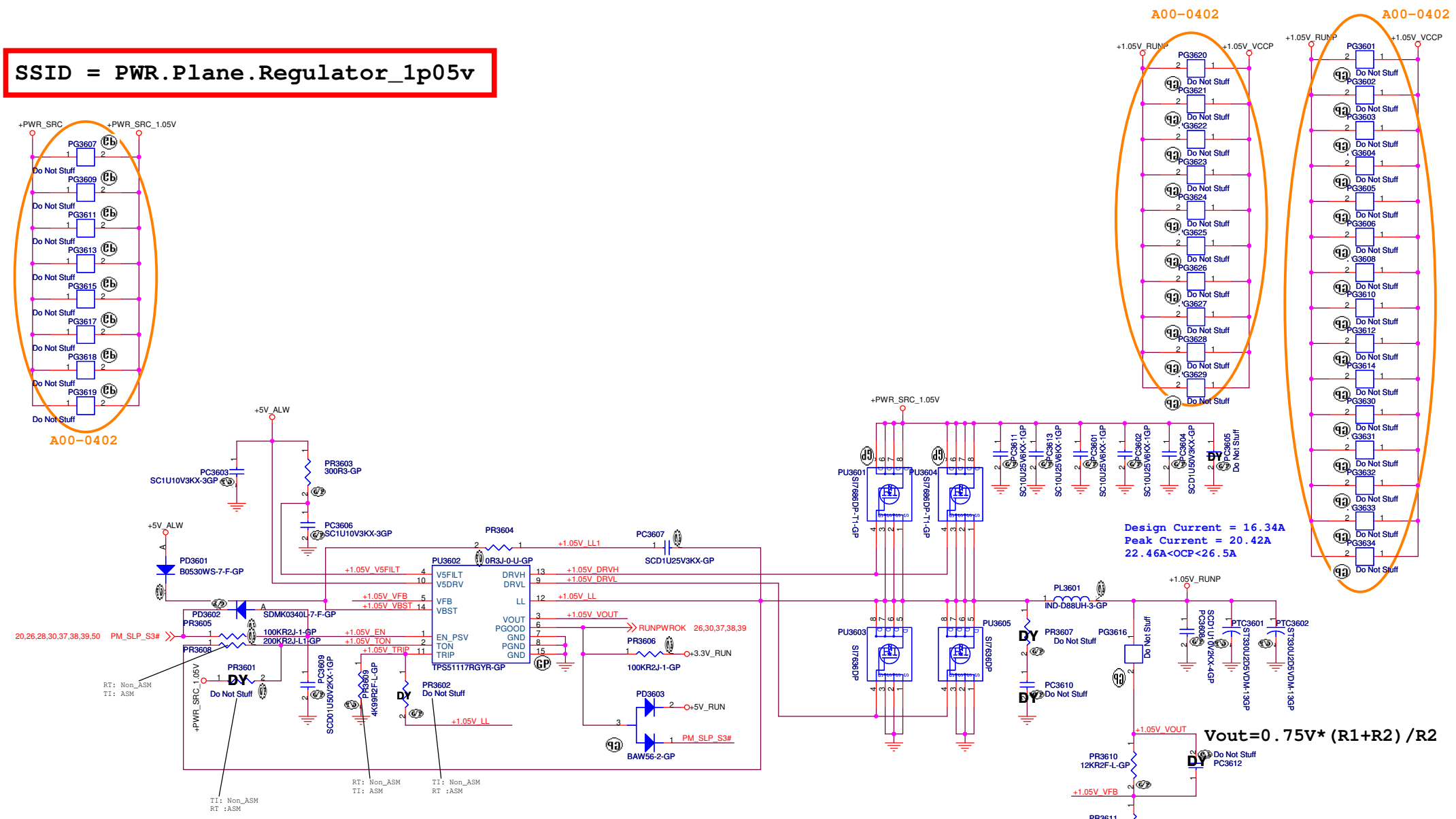
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU VCORE POWER(2/2)

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 35 of 61

SSID = PWR.Plane.Regulator_1p05v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.88UH FDU1040D-R88M=P3 TOKO DCR:2.3mohm Isat =22.2Arms 68.R8810.10B
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/ 14mOhm/ 4.5Vgs/ 84.07686.037
L/S: SI7636ADP/ POWERPAK-8/ 4.8mOhm/ 4.5Vgs/ 84.07636.037
Switching freq-->350KHz

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Title: DC to DC 1.05V		
Size: Custom	Document Number: Alba UMA	Rev: -1
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SSID = PWR.Plane.Regulator_1p5v/1p1v

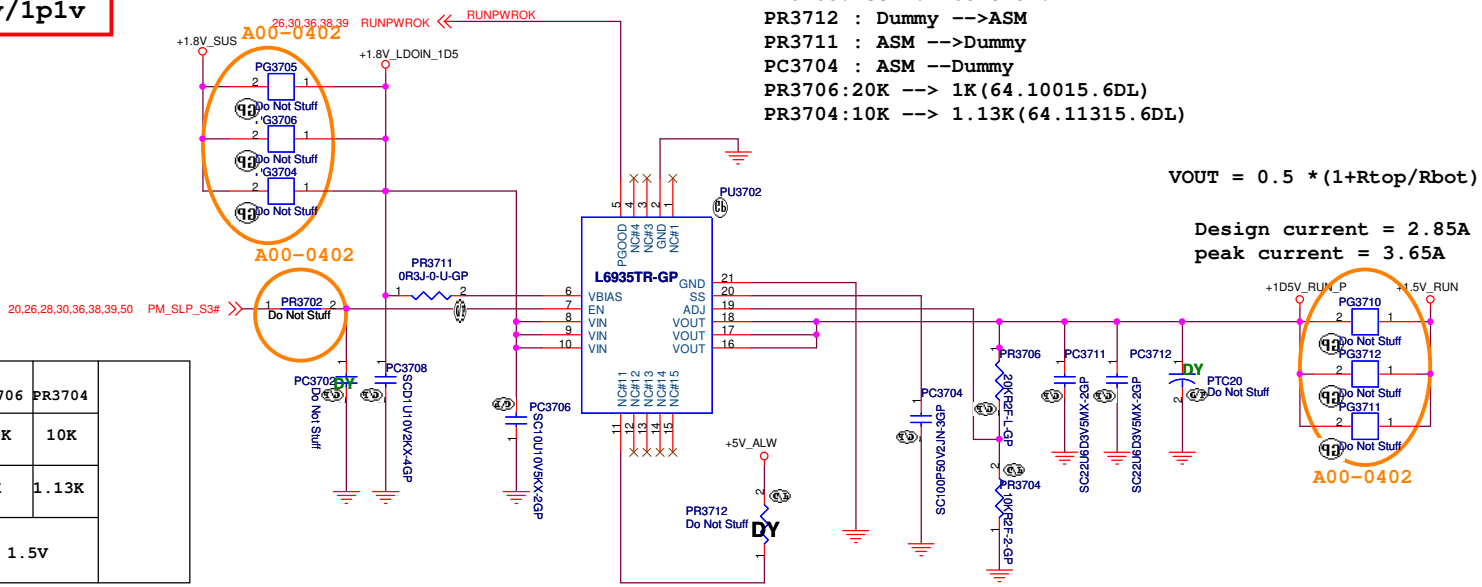
2nd Source BOM Control:
PR3712 : Dummy -->ASM
PR3711 : ASM -->Dummy
PC3704 : ASM --Dummy
PR3706:20K --> 1K(64.10015.6DL)
PR3704:10K --> 1.13K(64.11315.6DL)

VOUT = 0.5 *(1+Rtop/Rbot)

Design current = 2.85A
peak current = 3.65A

Vendor	PIN6	PIN11	PIN20
L6935	VBIAS	N.C.	SS
RTXX35	N.C.	VBIAS	N.C.

Vendor	PR3712	PR3711	PR3706	PR3704
L6935	DY	ASM	20K	10K
RTXX35	ASM	DY	1K	1.13K
			1.5V	



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Title: DC to DC L6935_1.5V / L6935_1.1V

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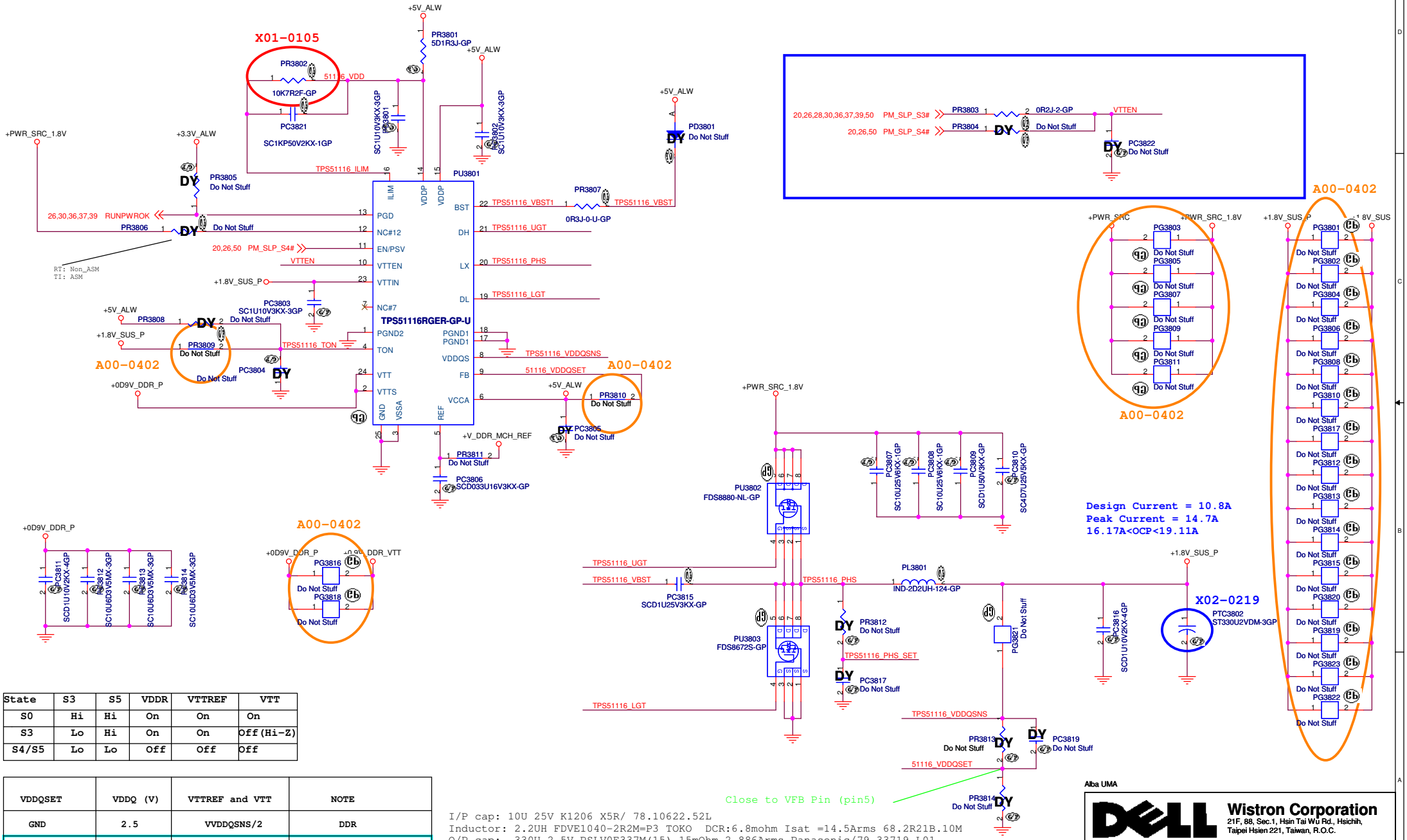
Date: Monday, April 06, 2009 | Sheet 37 of 61

SSID = PWR.Plane.Regulator_1p8v0p9v

TI TPS51116 for 1.8V and 0.9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE1040-2R2M=P3 TOKO DCR:6.8mohm Isat =14.5Arms 68.2R21B.10M
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms Panasonic/79.33719.L01
H/S: FDS8880 SO-8/ 9.6mOhm/12mOhm @4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A3784.07636.037

Alba UMA

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Title: DC to DC 1.8V/0.9V

Size: Custom | Document Number: Alba UMA | Rev: -1

Date: Monday, April 06, 2009 | Sheet 38 of 61

SSID = PWR.Plane.Regulator_gfx

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Title: VGA_CORE

Size: A3 | Document Number: Alba UMA | Rev: -1

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Alba UMA

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Taipei Hsien 221, Taiwan, R.O.C.

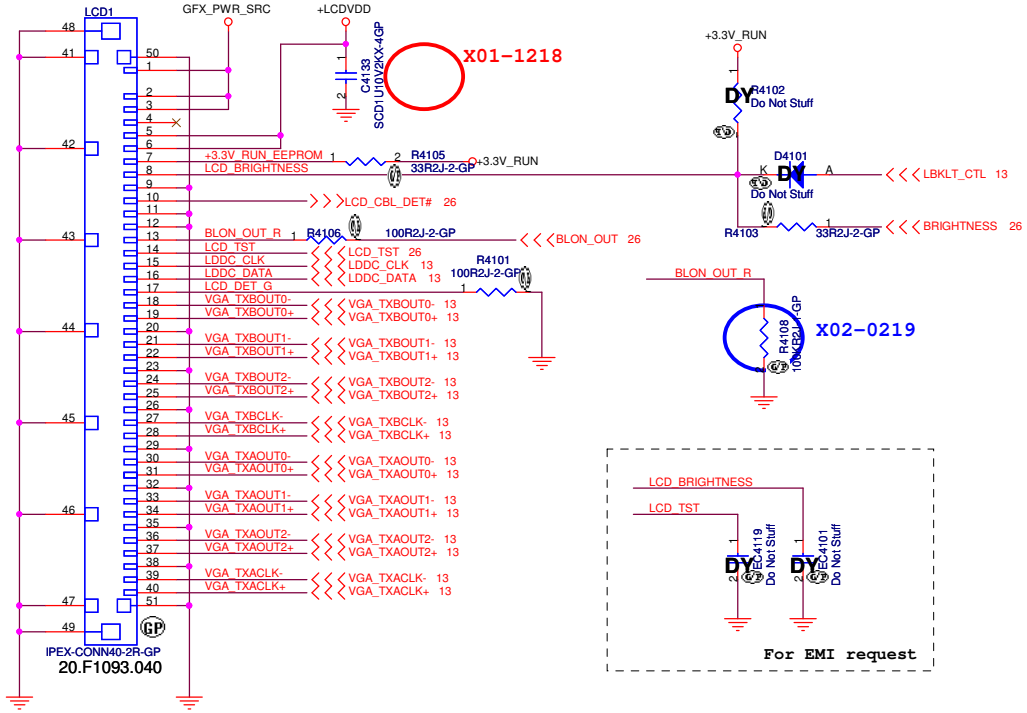
Title: *(Reserve)*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 40 of 61

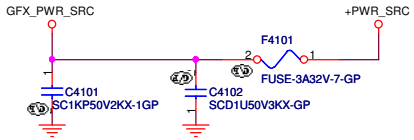
SSID = VIDEO

LVDS CONNECTOR

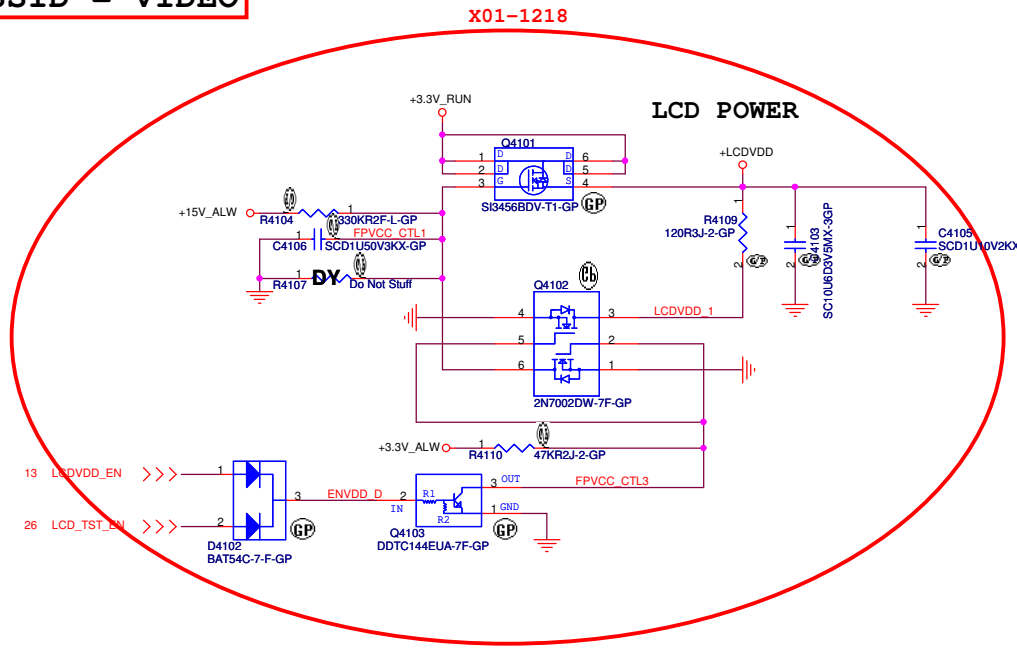


SSID = Inverter

INVERTER POWER



SSID = VIDEO



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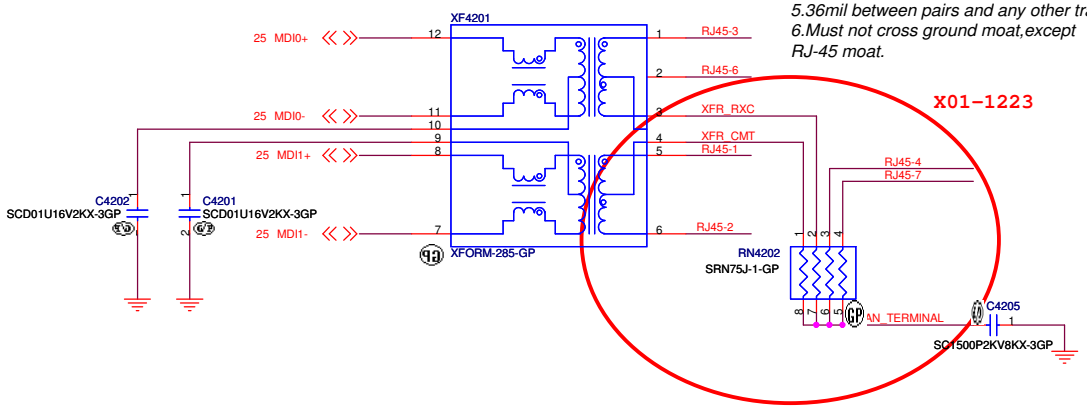
Title	LCD/Inverter Connector	
Size: Custom	Document Number: Alba UMA	Rev: -1
Date: Monday, April 06, 2009	Sheet 41 of 61	

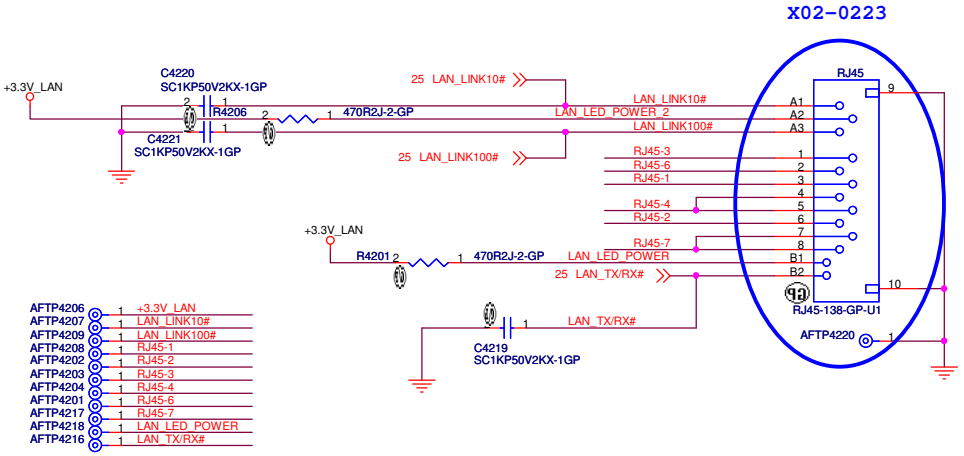
SSID = LOM

1.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
2.No vias, No 90 degree bends.
3.pairs must be equal lengths.
4.6mil trace width,12mil separation.
5.36mil between pairs and any other trace.
6.Must not cross ground moat,except RJ-45 moat.

10/100M Lan Transformer

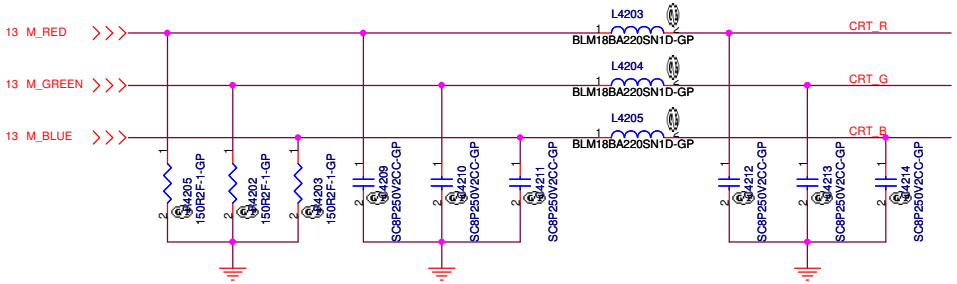


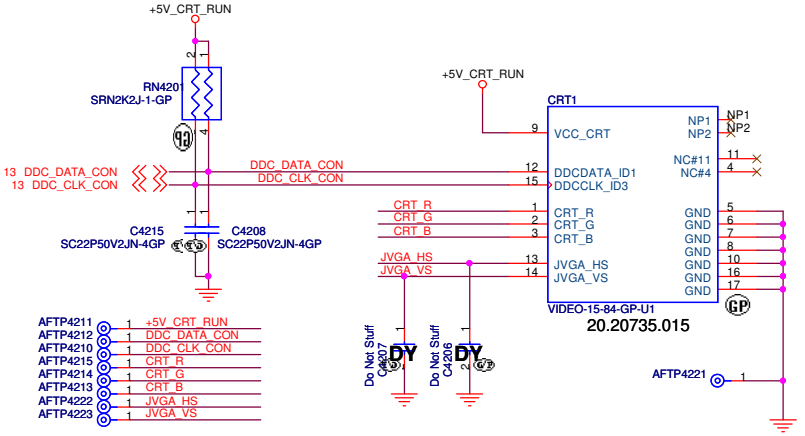
RJ45 Connector



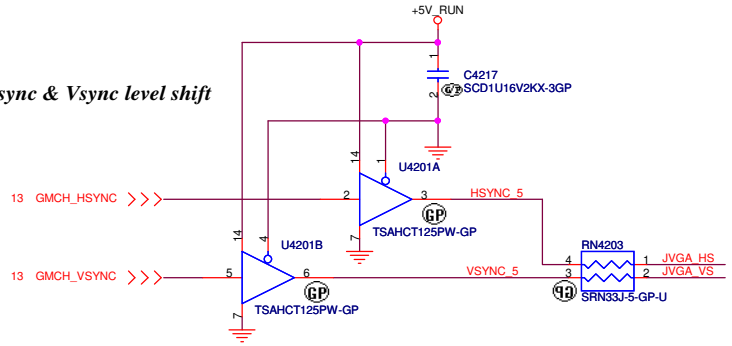
SSID = VIDEO

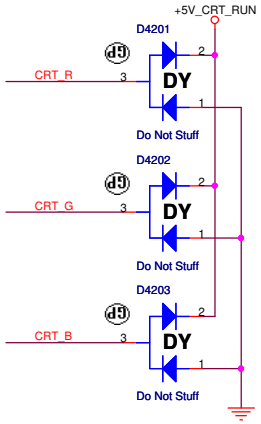
```
Layout Note:

*Pi-filter & 150 Ohm pull-down
  resistors should be as close
  as to CRT CONN.
* RGB signal will hit 75 Ohm
   first, then pi-filter, finally
   CRT CONN.
```

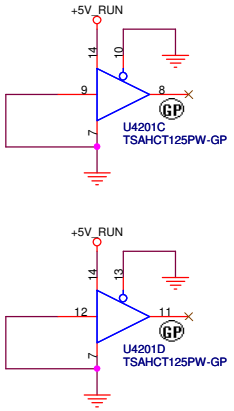


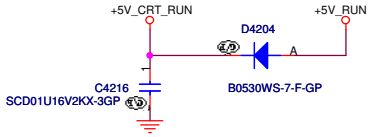


Hsync & Vsync level shift









Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

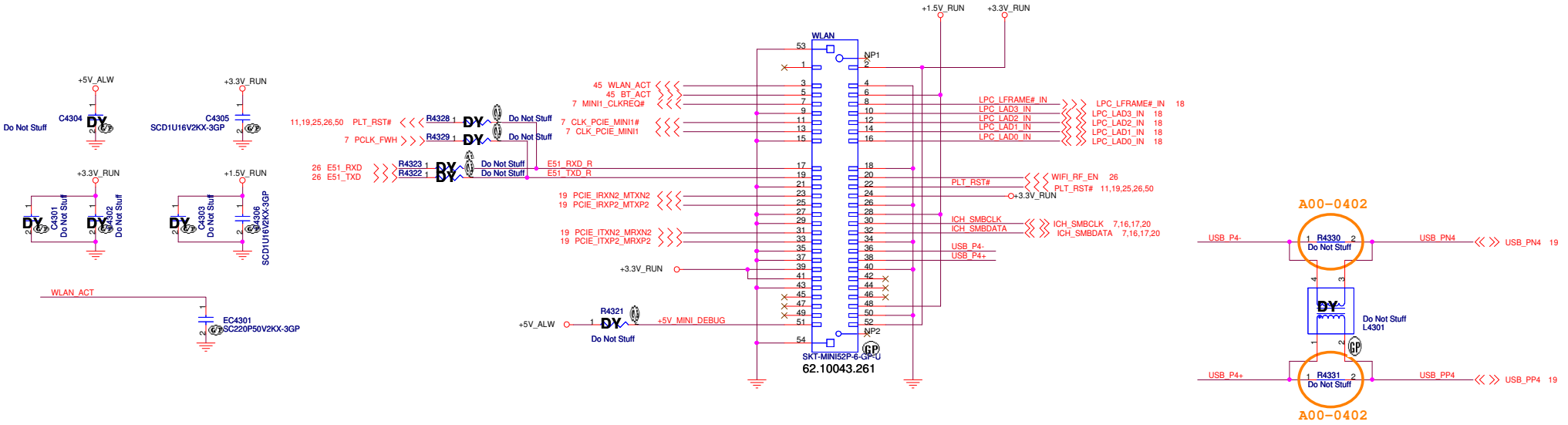
Title: **LAN/CRT Connector**

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 42 of 61

SSID = Wireless

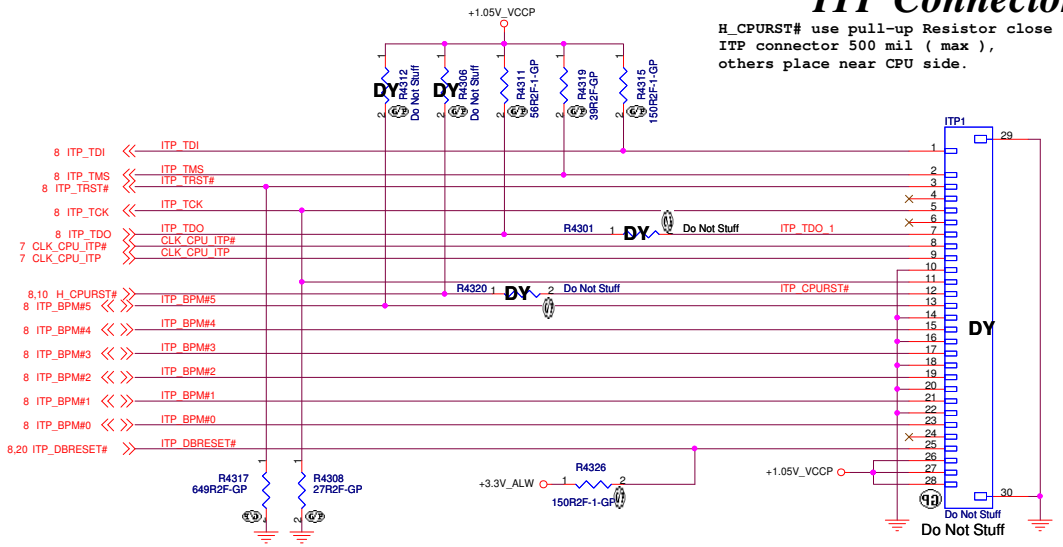
Mini Card Connector(802.11a/b/g/n)



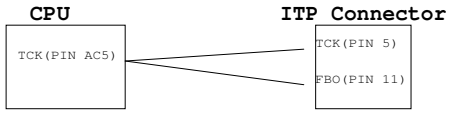
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



+1.05V_VCCP use Decoupling Capacitor close
ITP connector 100 mil (max)



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

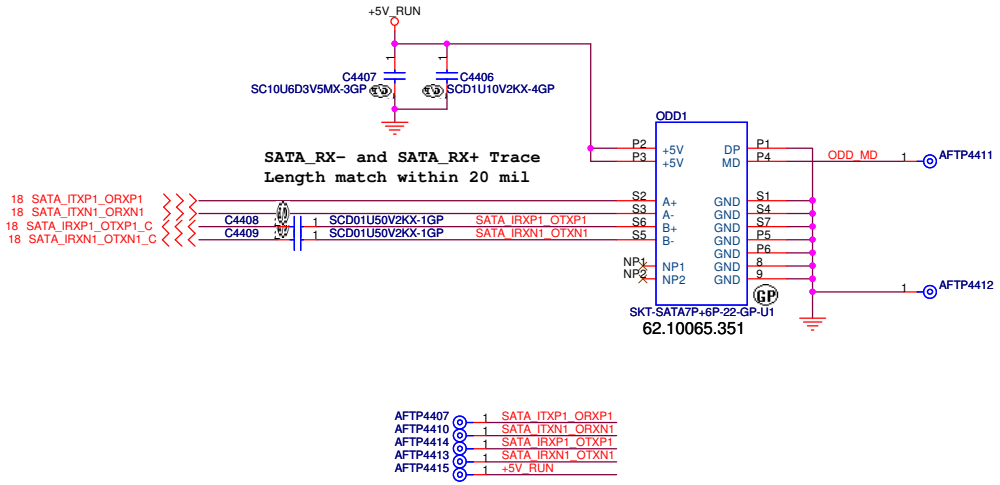
Title: MINICARD(WLAN)/ITP CONN

Size	Document Number	Rev
Custom	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 43 of 61

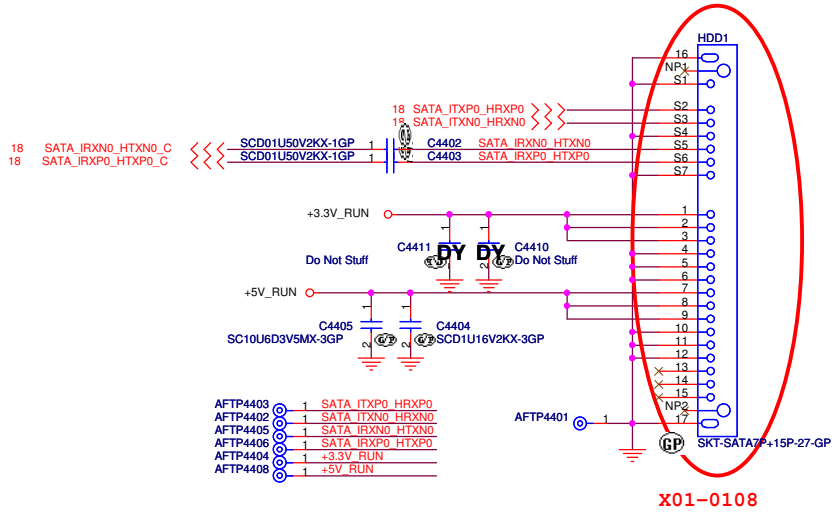
SSID = SATA

ODD Connector



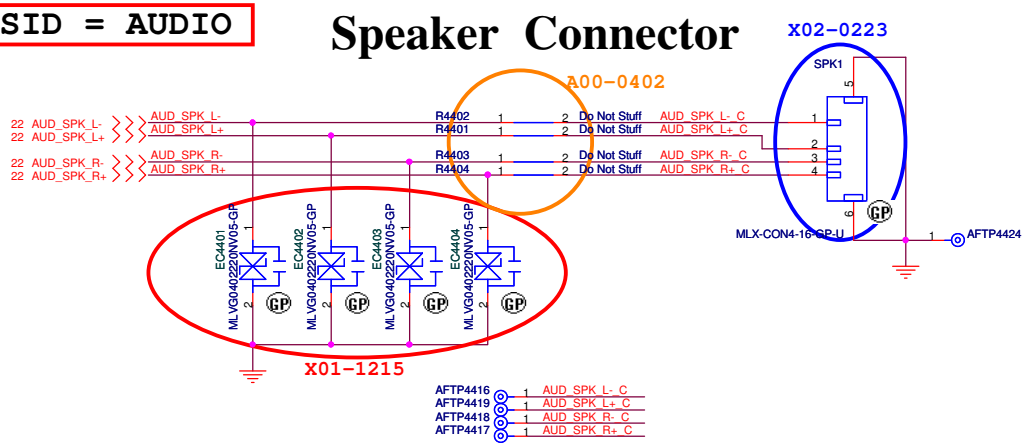
SSID = SATA

SATA HDD Connector



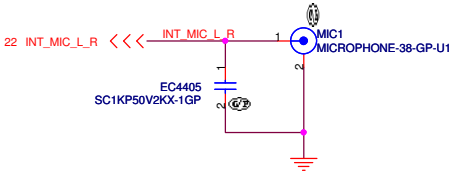
SSID = AUDIO

Speaker Connector



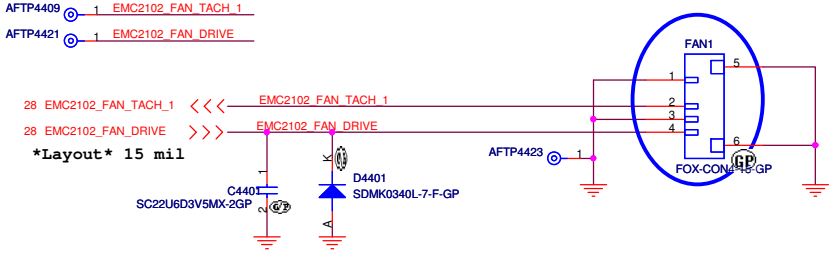
SSID = AUDIO

Internal MIC



SSID = Thermal

Fan Connector



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

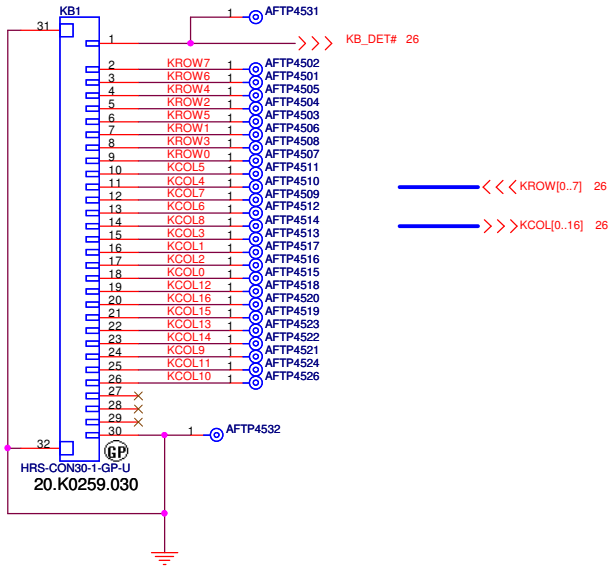
Title: HDD/ODD/FAN/SPEAKER/MIC

Size	Document Number	Rev
Custom	Alba UMA	-1

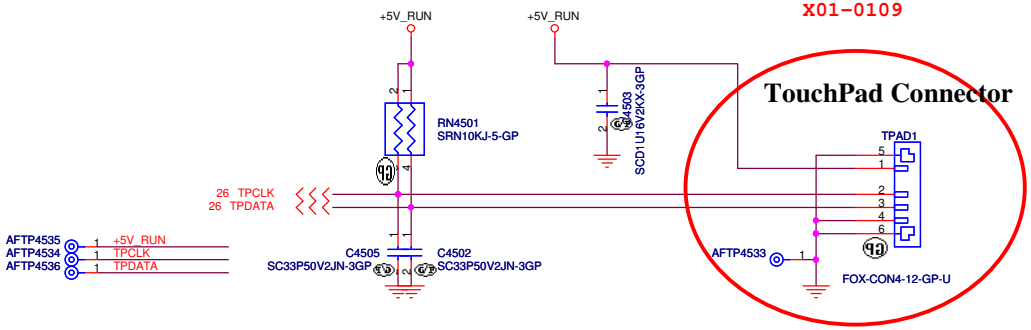
Date: Monday, April 06, 2009 Sheet 44 of 61

SSID = KBC

Internal KeyBoard Connector

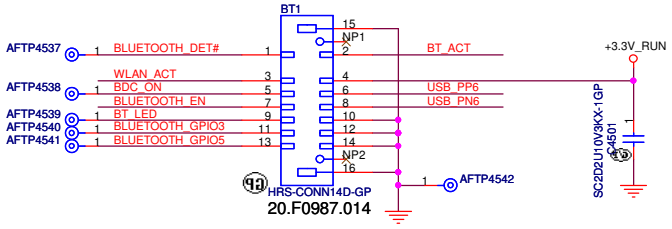


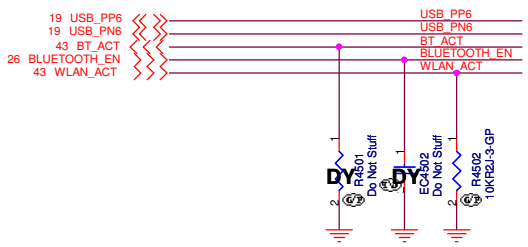
SSID = Touch.Pad

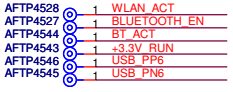


SSID = User.Interface

Bluetooth Module conn.







Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KeyBoard/TouchPad/BT

Size: Custom | Document Number: Alba UMA | Rev: -1

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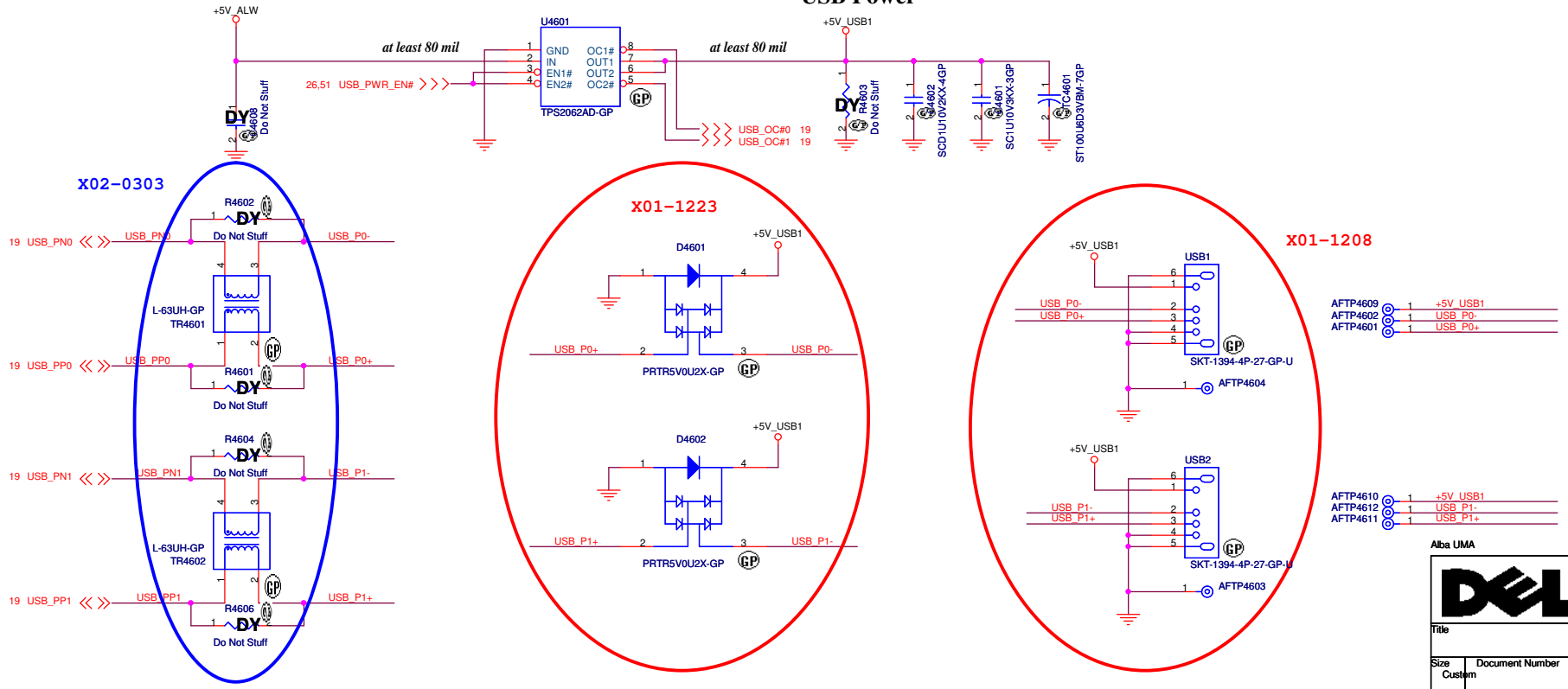
SSID = Modem

X01-1204

USB Power



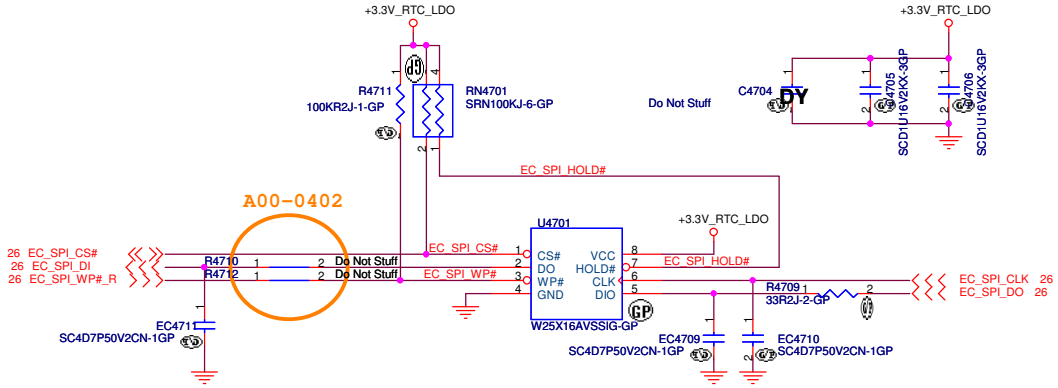
Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MDC CONN	
Size: Custom	Document Number: Alba UMA	Rev: -1
Date: Monday, April 06, 2009	Sheet 46 of 61	

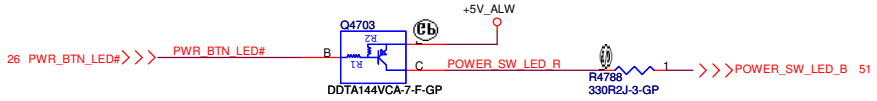
SSID = Flash.ROM

SPI FLASH ROM (16M bits)

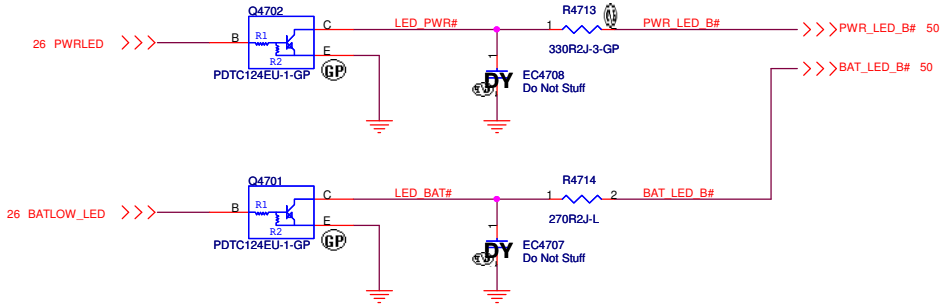


SSID = User.Interface

Power Button LED

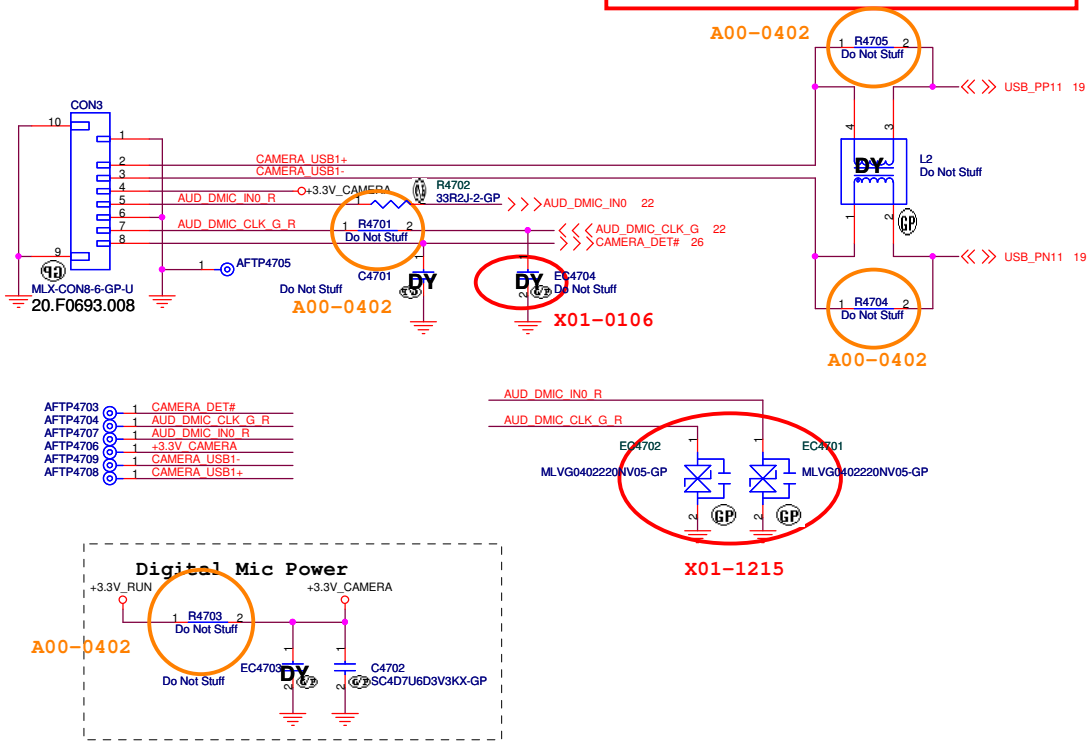


Power/Battery LED



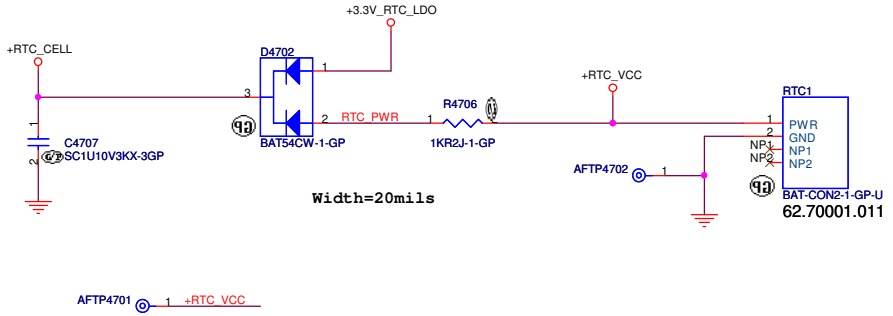
Camera Connector

SSID = User.Interface



SSID = RBATT

RTC Connector



Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	SPI Flash/LED/Camera/RTC	
Size: Custom	Document Number: Alba UMA	Rev: -1
Date: Monday, April 06, 2009	Sheet 47 of 61	

(Blank)

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

Size: Custom | Document Number: *Alba UMA* | Rev: *-1*

Date: Monday, April 06, 2009 | Sheet 48 of 61

(Blank)

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Alba UMA*	*-1*

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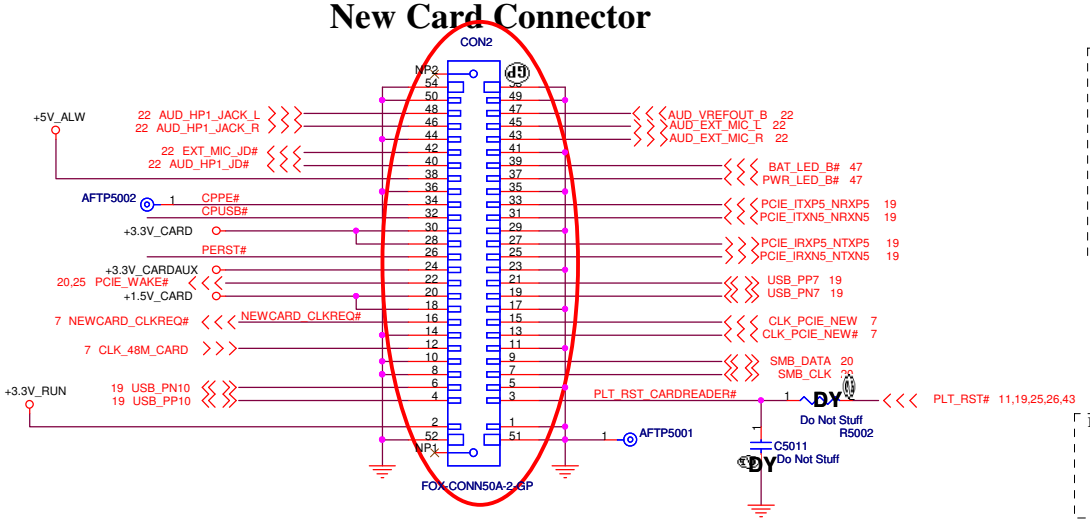
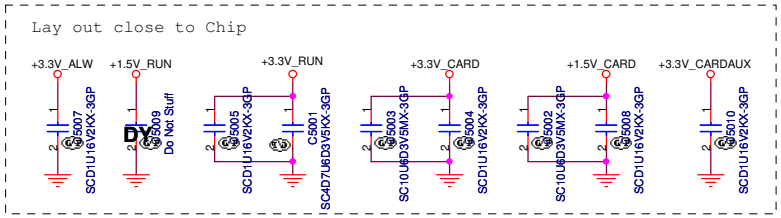
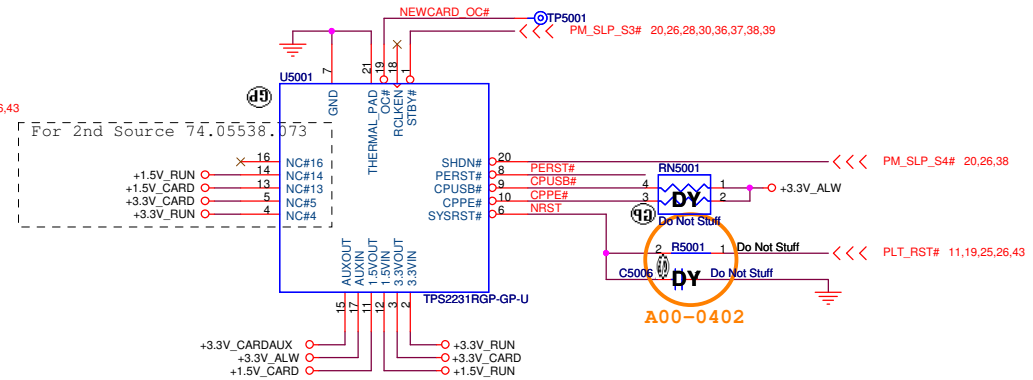
SSID = ExpressCard

New Card Connector



X01-0106





A00-0402

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

AFTP5029 PWR_LED_B#
AFTP5032 BAT_LED_B#
AFTP5031 +5V_ALW
AFTP5030 PLT_RST_CARDREADER#
AFTP5020 PCIE_ITXP5_NRXP5
AFTP5025 PCIE_ITXN5_NRXN5
AFTP5023 PCIE_IRXP5_NTXP5
AFTP5024 PCIE_IRXN5_NTXN5
AFTP5026 AUD_VREFOUT_B
AFTP5004 AUD_HP1_JACK_L
AFTP5006 AUD_HP1_JACK_R
AFTP5007 +3.3V_RUN
AFTP5009 CPUSB#
AFTP5005 USB_PP7
AFTP5008 USB_PN7
AFTP5011 AUD_EXT_MIC_L
AFTP5010 AUD_EXT_MIC_R
AFTP5017 EXT_MIC_JD#
AFTP5013 AUD_HP1_JD#
AFTP5014 CLK_48M_CARD
AFTP5012 NEWCARD_CLKREQ#
AFTP5019 +3.3V_CARD
AFTP5015 PERST#
AFTP5022 +3.3V_CARDAUX
AFTP5021 PCIE_WAKE#
AFTP5016 +1.5V_CARD
AFTP5018 SMB_DATA
AFTP5003 SMB_CLK
AFTP5027 USB_PN10
AFTP5028 USB_PP10

Alba UMA

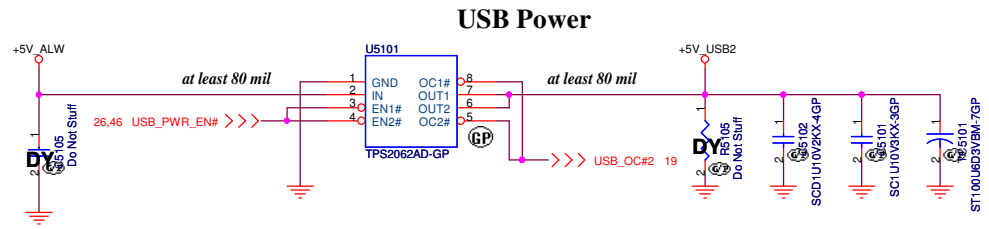
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

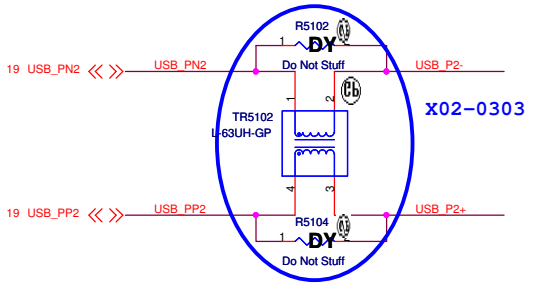
Title: Express Card Board CONN

Size: Custom | Document Number: Alba UMA | Rev: -1

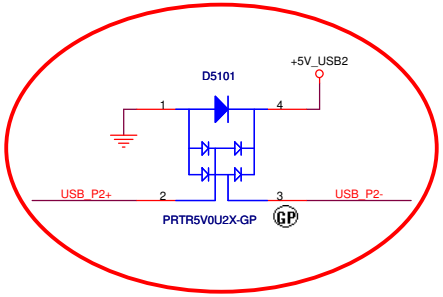
Date: Monday, April 06, 2009 | Sheet 50 of 61

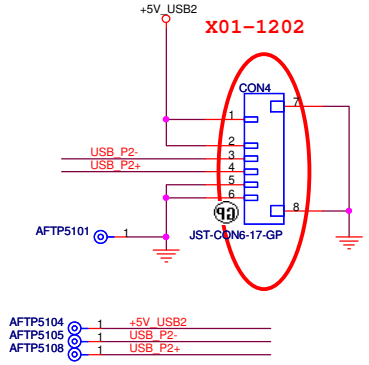
SSID = USB



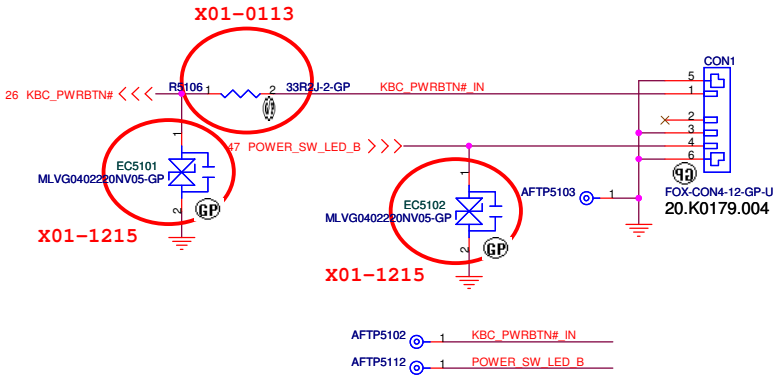


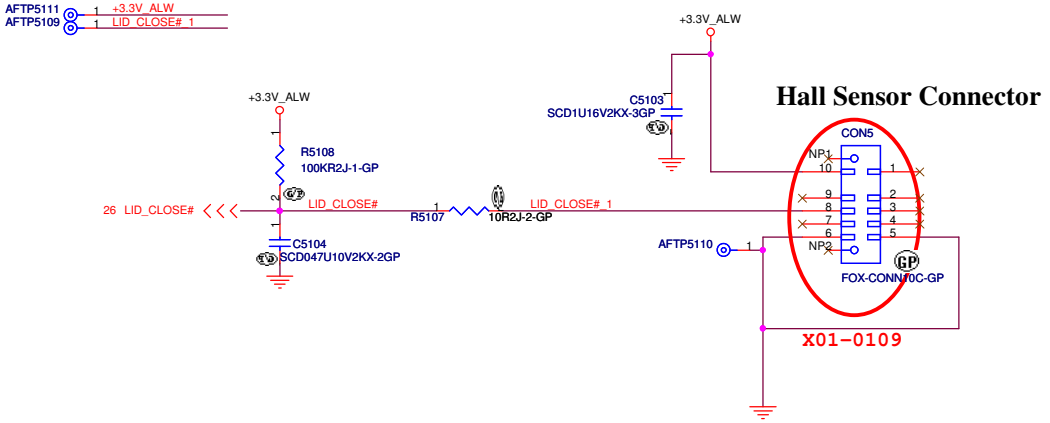
X01-1223





SSID = User.Interface

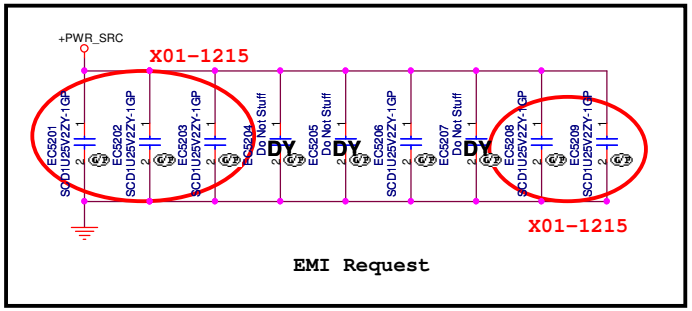


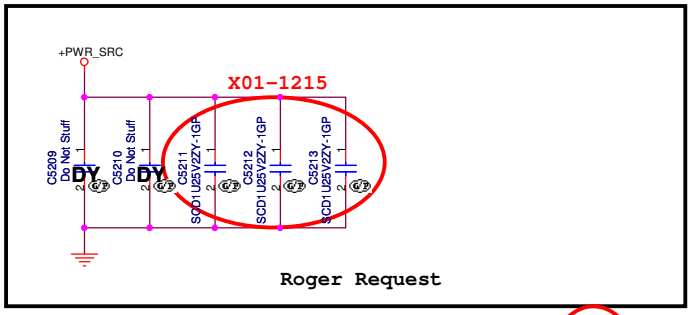


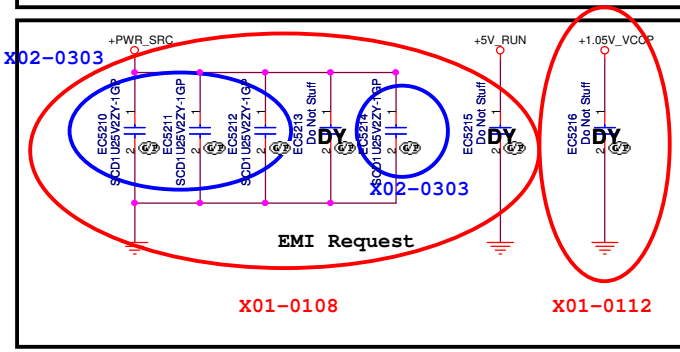
Alba UMA

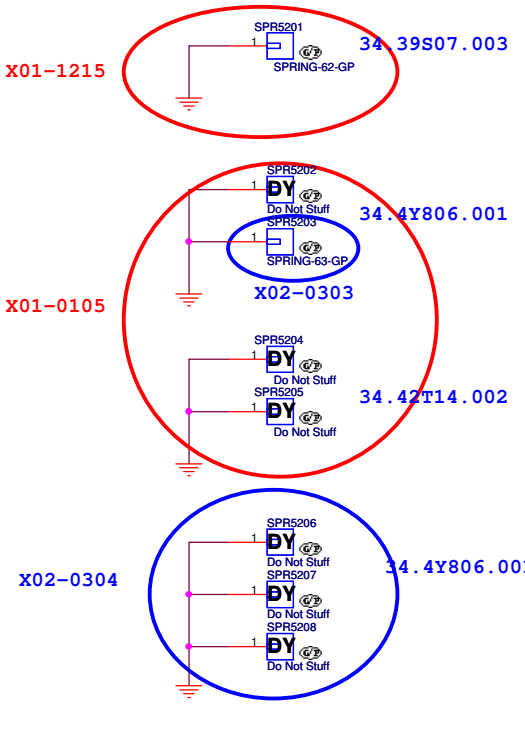
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Power Button/Hall Sensor/USB Board		
Size: Custom	Document Number: Alba UMA	Rev: -1
Date: Monday, April 06, 2009	Sheet 51 of 61	

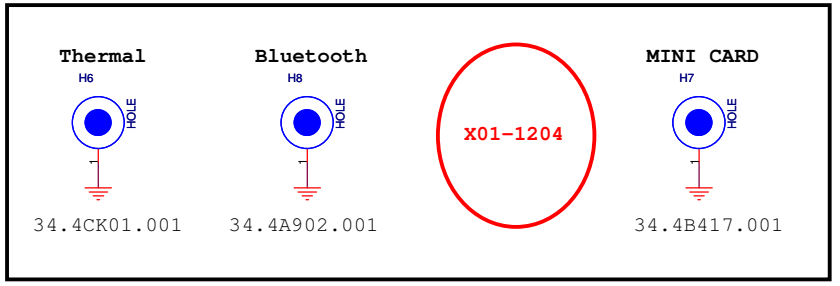
SSID = Mechanical











Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Miscellaneous Components

Size	Document Number	Rev
Custom	Alba UMA	-1

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SSID = VIDEO

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-PCIE/LVDS(1/4)

Size	Document Number	Rev
Custom	Alba UMA	-1

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SSID = VIDEO

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-TV/CRT/DP PORT

Size	Document Number	Rev
C	Alba UMA	-1

Date: Monday, April 06, 2009 Sheet 54 of 61

SSID = VIDEO

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-POWER/GND(3/4)

Size	Document Number	Rev
A2	Alba UMA	-1

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SSID = VIDEO

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-MEMORY/STRAPS(4/4)

Size: A2 | Document Number: Alba UMA | Rev: -1

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SSID = VIDEO

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM

Size: Custom | Document Number: Alba UMA | Rev: -1

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	20,26	2008/11/03	Wistron	UMA no need.	ICH gpio6 NC,KBC gpio45 NC,Remove R2030,R2635	X01
2	34	2008/11/19	Wistron	LoadLine is too low.	Change PR3431 to 3.48K ohm.	X01
3	25	2008/11/25	Realtek	Prevent for capacitance effect.	Change R2506 to 1K ohm.	X01
~~4~~	~~22~~	~~2008/11/27~~	~~IDT~~	~~PC beep issue.~~	~~Change R2203,R2206 to 10K ohm. Add R2218,R2219.~~	~~X01~~
5	26	2008/11/27	Wistron	MB version changed.	Change R2609 pop,R2608 dummy.	X01
6	15	2008/11/27	Wistron	Reserve +3.3V_RUN trace.	Add R1518.	X01
7	25	2008/12/18	KDS	Follow crystal vendor test result.	Change C2501 to 18pF,C2502 to 15pF	X01
8	18,46,52	2008/12/04	Dell	Remove MDC function.	Remove MDC schematics,holding,stand off.	X01
9	46	2008/12/04	Wistron	ID modify,Change USB connector.	Change USB connector from one dual port to two single port.(22.10218.T51)	X01
10	45	2008/12/04	Wistron	Change touch pad connector.	Change touch pad connector to 20.K0179.004	X01
11	42	2008/12/08	Wistron	Change RJ45 connector.	Change RJ45 connector to 22.10177.C81	X01
12	33	2008/12/15	Wistron	Add 15_ALW Schematics.	Add 15_ALW Schematics.	X01
13	30	2008/12/15	Wistron	Modify 3V 5V schematics.	Modify 3V 5V schematics.	X01
~~14~~	~~22~~	~~2008/12/15~~	~~Wistron~~	~~Diancetic mode sound is too slow.~~	~~Modify PC Beep schematcis.~~	~~X01~~
15	26,41	2008/12/15	Wistron	For Panel Test.	Add LCD_TST_EN for panel test. R2638 POP.	X01
16	52	2008/12/15	Wistron	EMI issue.	Add SPR5201.	X01
17	28	2008/12/15	Wistron	Rename trace name.	Rename T8_THERMDC and T8_THERMDA.	X01
18	41	2008/12/17	Wistron	CMO panel white screen issue.	Reseve R4108.	X01
19	41	2008/12/18	Wistron	LCD Power Sequence Issue.	Modify LCD Power schematics.~~Change LCD CONN part.~~	X01
20	52	2008/12/18	Wistron	EMI Issue.	Add SPR5202.	X01
~~21~~	~~42~~	~~2008/12/19~~	~~Wistron~~	~~CRT R.G.B EA test issue.~~	Change bead to 47ohm and depop capacitors for π filter.	~~X01~~
22	32	2008/12/10	Wistron	Prevent leakage from KBC.	Change PR3203 pull high from +3.3V_ALW to +3.3V_RTC_LDO.	X01

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23	44,52 51,47	2008/12/15	Wistron	Modify based on EMI test result.	EC5203/C5212/EC5202/C5211/C5213/EC5206/EC5201/EC5208 use 0.1u-Cap EC4701/EC4702/EC4401/EC4402/EC4403/EC4404/EC5101 use 22P5V-Varistor POWER_SW_LED_B add one 22P5V-Varistor Add EC5209 0.1uF cap.	X01
24	20,42,46	2008/12/23	Wistron	Layout request.	Swap TR4602,RN2001,RN4202,TR4601 net.	X01
25	46,51	2008/12/23	Wistron	For EMI request.	Add D4601,D4602,D5101	X01
26	52	2009/01/05	Wistron	Reserve 3 Spring.	Add SPR5203,SPR5204,SPR5205.Dummy SPR5202.	X01
27	15	2008/12/30	Wistron	Remove R1515.For layout get good performance.	Remove R1515,change R1549 to 2.2uF.	X01
28	50	2009/01/06	Wistron	Change CON2 connector.	Change CON2 connector to 20.F1400.050.	X01
29	9	2009/01/06	Wistron	For VCC_CORE sense.	Add PG901,PG902. Dummy C925,Pop C901	X01
30	47,52	2009/01/06	Wistron	For EMI request.	Reserve EC4704,EC5210,EC5211,EC5212,EC5213,EC5214	X01
31	26	2009/01/06	Wistron	Keyboard detect.	Pop R2625.	X01
32	52	2009/01/08	Wistron	For EMI request.	Reserve EC5215 for +5V_RUN	X01
33	44,51	2009/01/08	Wistron	Change HDD1,CON5 connector.	Modify HDD1,CON5 symbol.	X01
34	51	2009/01/09	Wistron	CON5 symbol layout concern.	Change CON5 pin5 to GND,pin7 to NC.	X01
35	45	2009/01/09	Wistron	Touch pad cable change.	Modify TPAD1 pin define.	X01
36	52	2009/01/12	Wistron	For EMI request.	Reserve EC5216.	X01
37	8	2009/01/12	Wistron	GTL issue.	Pop C802.	X01
38	22	2009/01/13	Wistron	Pop noise.	Add KBC GPIO33.	X01
39	51	2009/01/13	Wistron	KBC burn issue.	Change R5106 to 33 ohm.	X01
40	41	2009/02/19	Wistron	CMO panel white screen issue.	Pop R4108.	X02
41	26	2009/02/19	Wistron	Change board ID.	Pop R2601,R2608.Dummy R2602,R2609.	X02
42	31,42,44	2009/02/23	Wistron	Change connector.	Change SPK1,FAN1,RJ45 connector.	X02
43	18,26	2009/02/24	Wistron	Change 32.768K crystal cap size.	Change C1806,C1807,C2607,C2608 to 0603 size.	X02

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44	22	2009/02/27	Wistron	Codec pop noise.	Add Q2201~Q2205. Change C2204 to 2.2uF. Move 60.4 ohm from small board to MB.	X02
45	46,51,52	2009/03/03	Wistron	Modify based on EMI test result.	EC5212,EC5211,EC5210,EC5214 -- 0.1u cap on board TR4602,TR4601,TR5102 -- 67ohm common mode on board spr5203--spring on board	X02
46	26	2009/03/03	Wistron	Remove PAID for KB detection	Dummy R2625.	X02
47	52	2009/03/04	Wistron	For EMI request.	Add SPR5206,SPR5207,SPR5208.	X02
48	26	2009/04/02	Wistron	Board ID Changed.	Pop R2604,Dummy R2603.	X02

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1	33	2008/12/15	Wistron	3D3V OCP over spec.	Change R3312 from 160K to 86.6K ohm.	X01
2	33	2009/01/05	Wistron	5V output voltage is too high.	Change PR3310 from 30.9K to 33K ohm. Change PR3314 from 20K to 21.5K ohm.	X01
3	33	2009/01/05	Wistron	5V H/S MOSFET VDS over spec.	Add Snubber PR3319 to 2.2K ohm, PC3319 to 560pF.	X01
4	33	2009/01/05	Wistron	5V OCP over spec.	Change R3311 from 160K to 147K ohm.	X01
5	33	2008/12/15	Wistron	Add 15V_ALW schematics	Add 15V_ALW schematics. DY PR3306	X01
6	34	2008/11/27	Wistron	LoadLine is too low.	Change PR3431 from 3.92K to 3.48K ohm.	X01
7	34	2009/01/05	Wistron	CPU_CORE OCP is too low.	Change PR3418 from 12.1K to 13.7K ohm.	X01
8	38	2009/01/05	Wistron	UMA 1D8V OCP is too low.	Change PR3802 from 8.06K to 10.7K ohm.	X01
9	39	2009/02/19	Wistron	Change main source.	Change PTC3301,PTC3302 to 77.22271.27L.	X02
10	38	2009/02/19	Wistron	Change main source.	Change PTC3802 to 79.33719.20D.	X02
11	32	2009/03/02	Wistron	Change cap from 25V to 50V.	Change PC3208,PC3209 to 78.10424.2BL	X02
12	31	2009/03/02	Wistron	Change main source.	Change PD3107 to 83.22R03.03G.	X02
13	33	2009/03/03	Wistron	Phase voltage is too high.	PC3319 change from 560pF to 680pF	X02
14	34	2009/03/03	Wistron	LoadLine is too high.	PR3431 change from 3.48K ohm to 3.92K ohm.	X02
15	33	2009/03/05	Wistron	15_ALW no need to install PD3303.	Dummy PD3303.	X02
16	32	2009/04/02	Wistron	Sequence issue.	Change PC3207 from 1uF to 0.1uF.	A00
17	32	2009/04/06	Wistron	For CPU transition response.	Change PC3409 from 100p to 150p.	A00

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