

UM3/UM6 SYSTEM BLOCK DIAGRAM

POWER

AC/BATT CONNECTOR
PG 53

SYSTEM RESET CIRCUIT PG 42

BATT CHARGER PG 45

RUN POWER SW
+3.3V_SUS/+5V_SUS
+5V/+3.3V/+1.8V PG 52

CPU VR PG 51

DC/DC
+3.3V_ALW/+5V_ALW/
+15V_ALW PG 46

REGULATOR
+1.5V_SUS/+0.75V_DDR_VTT PG 47
+1.05V_PCH PG 48
+1.05V_VTT PG 49

THERMAL
SMSC1422 PG 38

CLOCK
SLG8SP585VTR
(QFN-32) PG 15

DDR3-SODIMM1
RVS Type PG 13

Dual Channel DDR3
800/1066 1.5V

DDR3-SODIMM2
RVS Type PG 14

Arrandale

(rPGA 989)
PG 3,4,5,6

PCIEx16

DDR3 x 4
(512M 64bits)
PG 22

ATI M92-LP S2
PCI EXPRESS GFX
631 uFCBGA 23mm*23mm
PG 16,17,18,19,20,21,22

LVDS

HDMI

VGA

Panel Connector PG 24

HDMI CONN. PG 24

CRT CONN. PG 25

DMI X 4

PCH
(HM55)
PG 7,8,9,10,11,12

SATA-ODD PG 35 SATA

SATA-HDD PG 35 SATA

USB conn x 1 PG 33 USB2.0

Bluetooth BTB Conn
BT365 PG 32 USB2.0

Camera PG 24 USB2.0
To LCD Conn

IHDA

PCI E 2.0

PCI E 2.0

USB2.0

PCI E 2.0

USB2.0

LOM
RTL8103E PG 41

MINI-CARD
WLAN PG 32

MINI-CARD
WWAN PG 31

USB2.0

USB2.0

DB CONN

USB2.0

USB2.0

USB conn x 2

CARD READER
RTS5159

IO Board PG 26

AUDIO/AMP
ALC269Q-GR PG 39

A- MIC conn PG 39

Audio SPK conn PG 39

DB CONN

Audio Jacks x2 PG 26

IO Board

USER INTERFACE PG 37

LPC

KBC
ITE8502 PG 29

FLASH
1Mbytes PG 30

Touchpad PG 36

SPI

FLASH
4Mbytes PG 30

Keyboard PG 36

PS/2

VER :C3B
PWA:
PWB:



Title Schematic Block Diagram		
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25	CRT CONN
26	DB CONN / R5U230
27	BLANK PAGE
28	BLANK PAGE
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32	MINI-Card (WLANWPAN)
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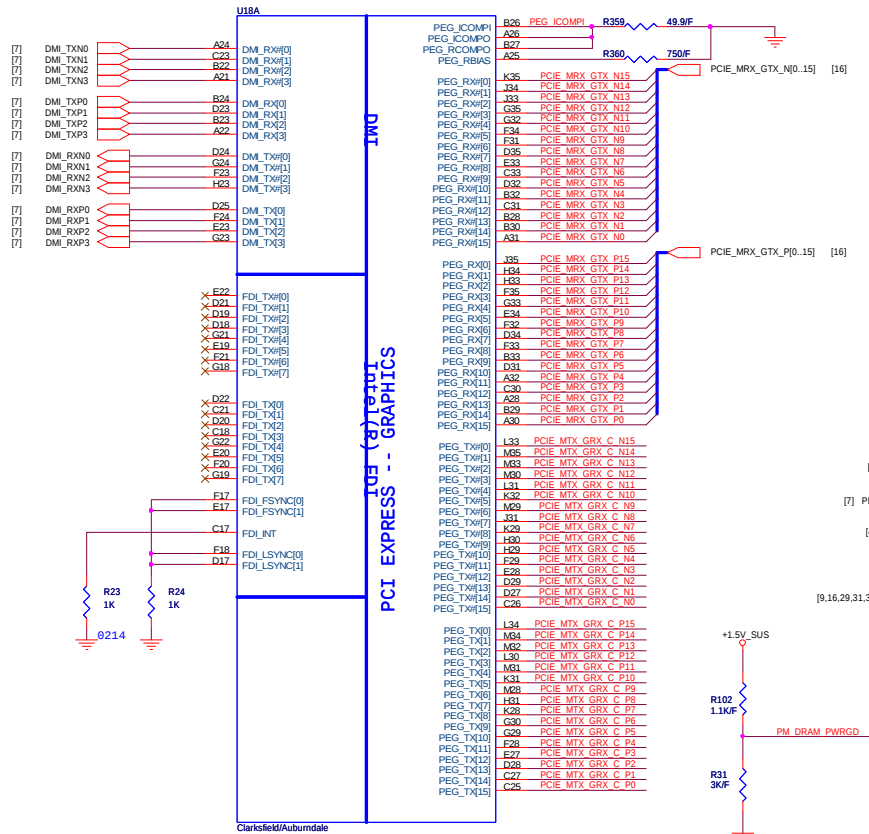
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,45,46,47,48,49,50,51	MAIN POWER		S0-S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0-S5
+5V_ALW	+5V	37,44,46,47,49,50,53	LARGE POWER	ALW_ON	S0-S5
+3.3V_ALW	+3.3V	29,30,37,44,45,46,51,52,53	8051 POWER	3.3V_ALW_ON	S0-S5
+5V_SUS	+5V	11,26,33,37,46,48,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,,24,36,37,41,42,44,47,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,37,38,39,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,19,24,25,26,29,30,31,32,35,38,39,41,42,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	GFX_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_+1.1_EN	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44	VGA POWER	GFX_+1.8_EN	
+1.05V_PCH	+1.05V	07,08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+1.05V_VTT	+1.1V	03,05,10,11,49	CPU POWER	RUN_ON	

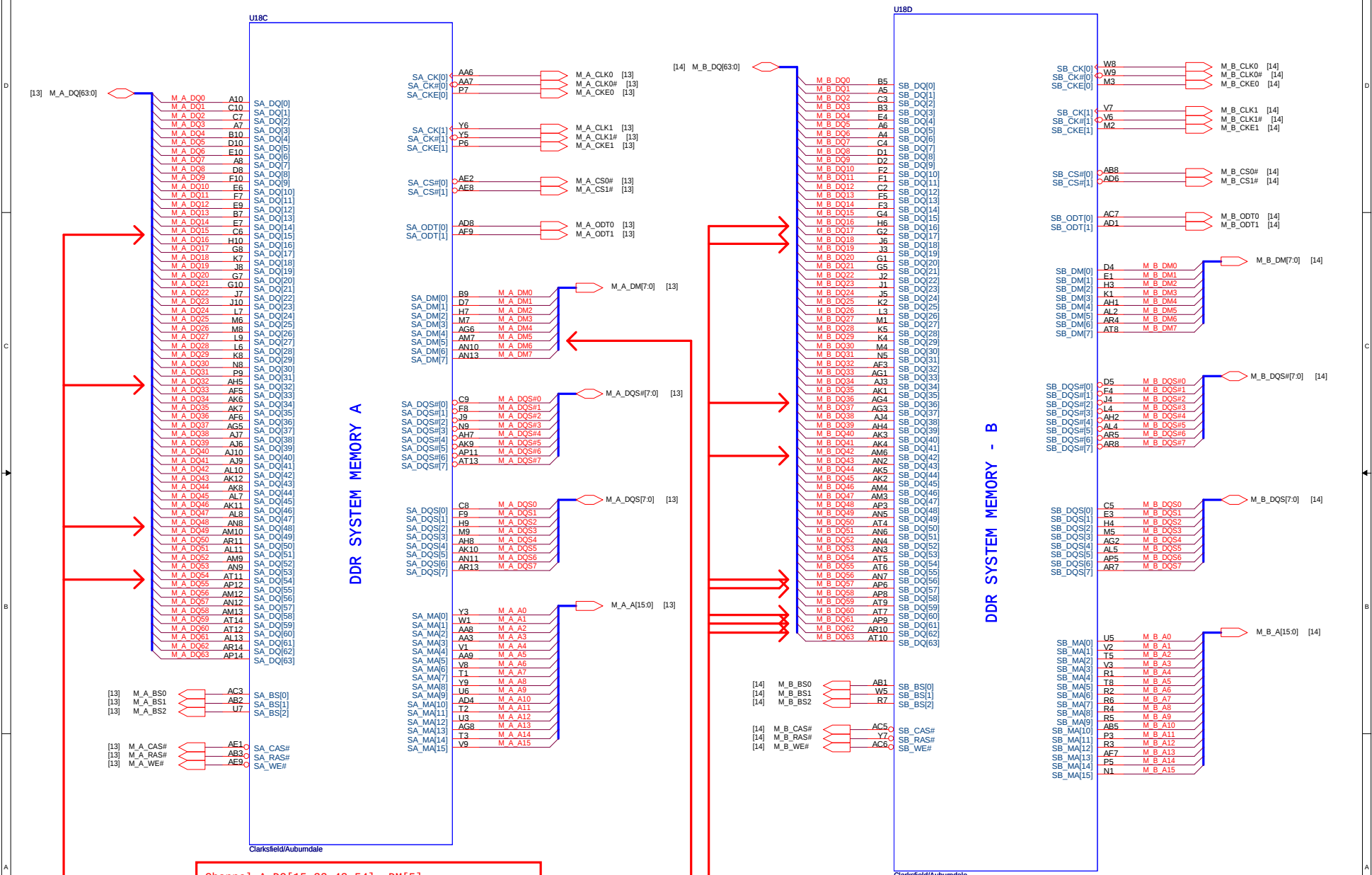
GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI, PEG, FDI)

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK, MISC, JTAG)



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

QUANTA
COMPUTER

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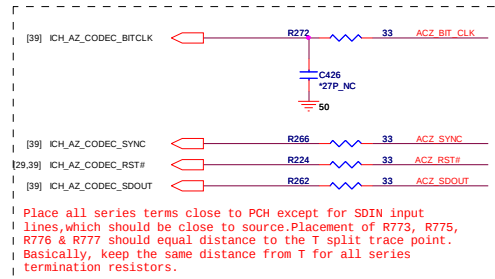
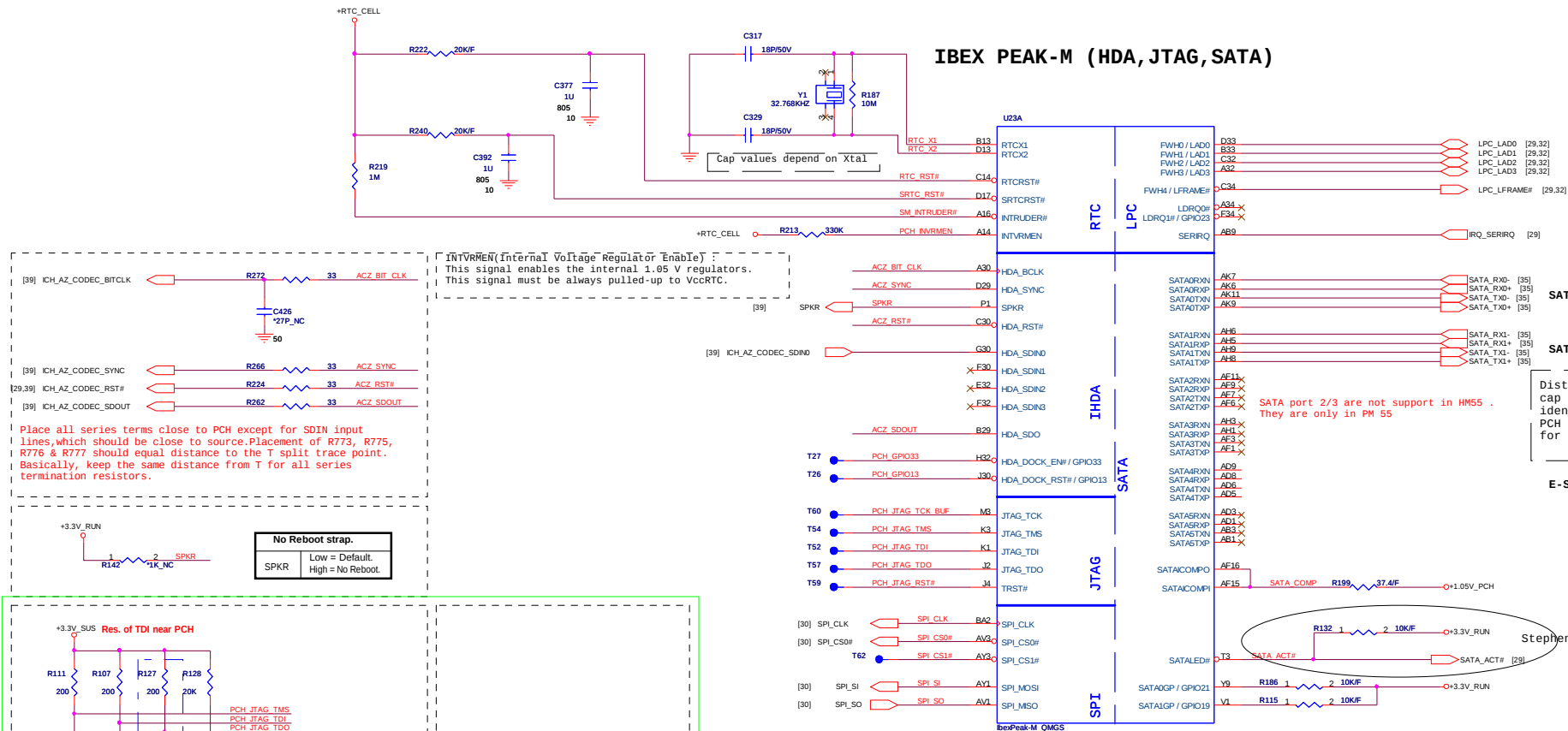
AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

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Title: AUBURNDA A/4			
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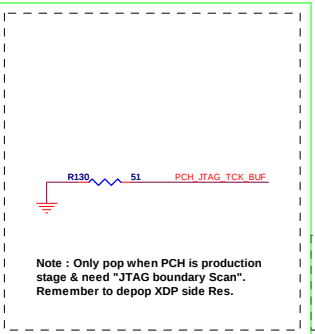
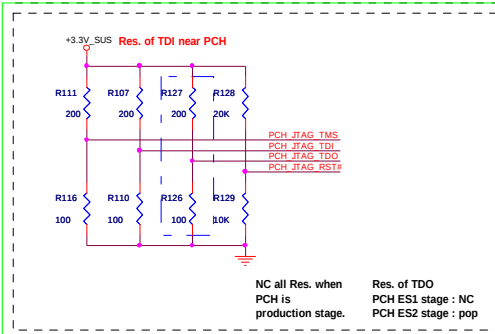


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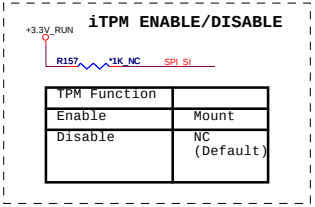
IBEX PEAK-M (HDA, JTAG, SATA)



INTRUDER(Internal Voltage Regulator Enable) : This signal enables the internal 1.05 V regulators. This signal must be always pulled-up to VccRTC.



JTAG Test Pads are need to put on the same side of mother board.



TPM Function	
Enable	Mount
Disable	NC (Default)

SATA port 2/3 are not support in HM55 . They are only in PM 55

Distance between the PCH and cap on the "P" signal should be identical distance between the PCH and cap on the "N" signal for the same pair.

QUANTA COMPUTER

File: IBEX PEAK-M 216

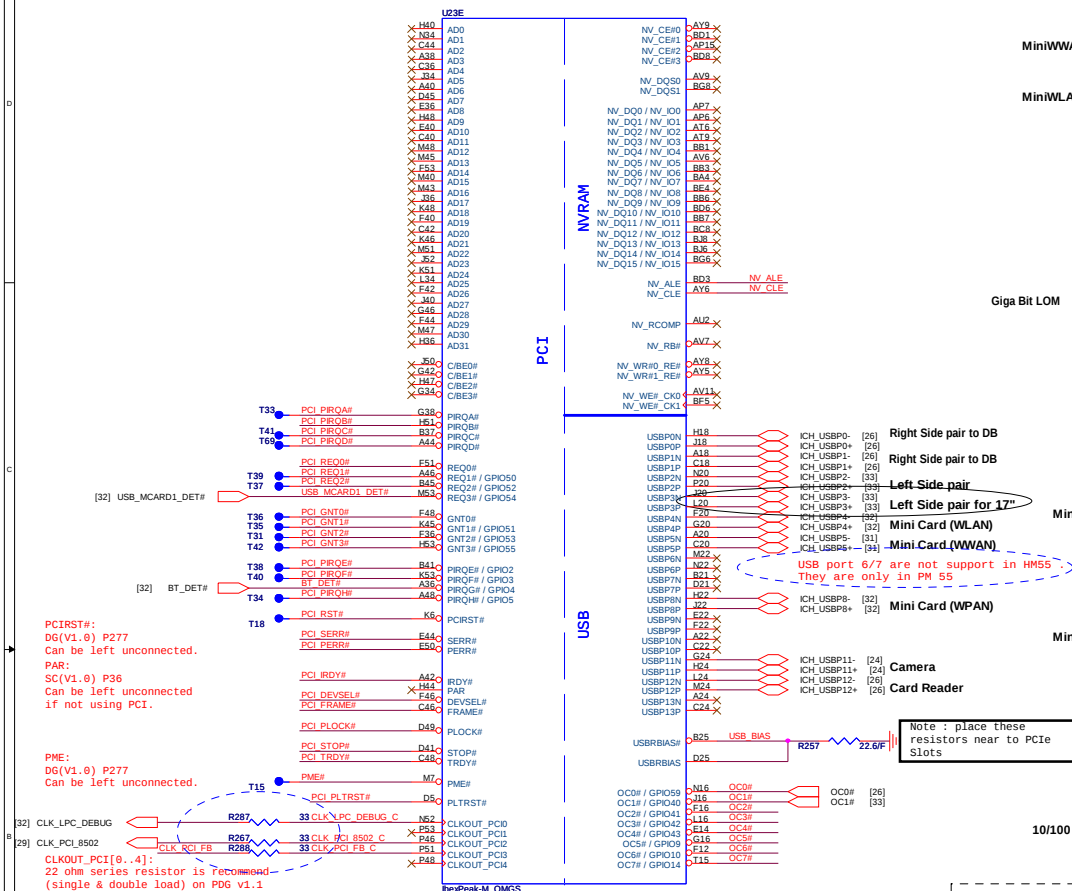
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Date: Thursday, October 15, 2009

Rev: 1A

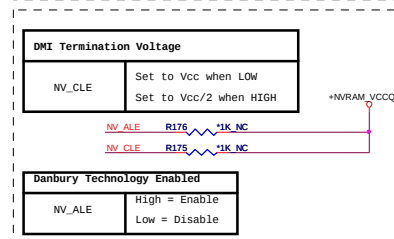
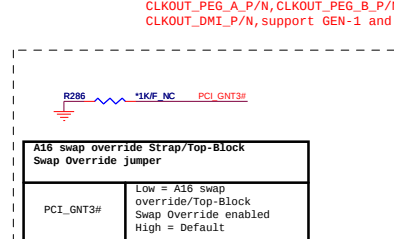
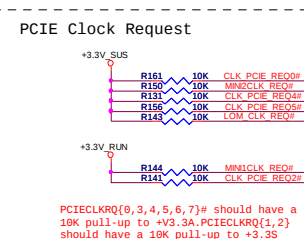
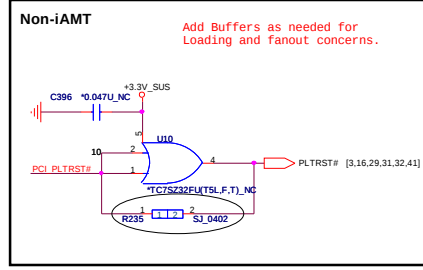
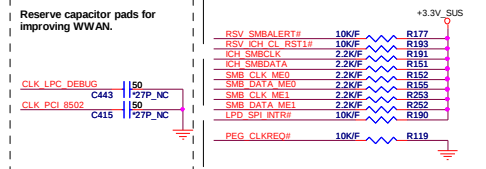
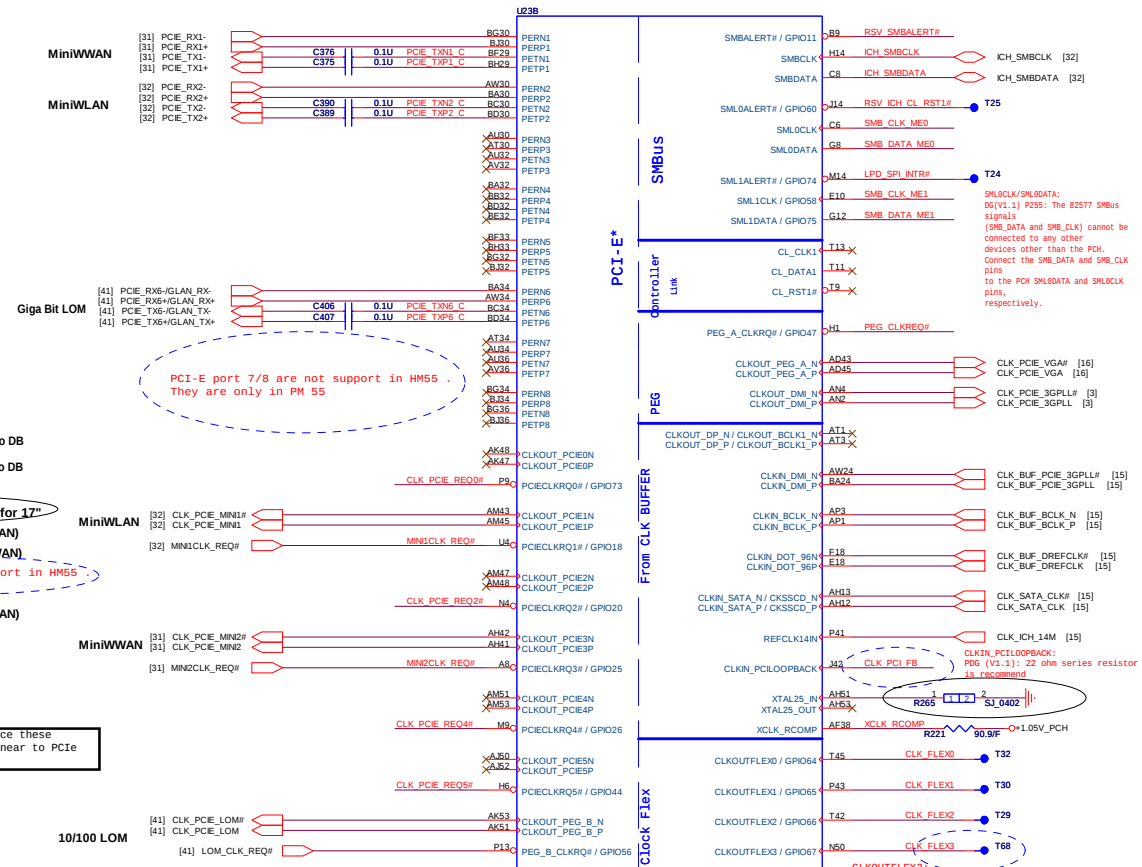
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IBEX PEAK-M (PCI, USB, NVRAM)

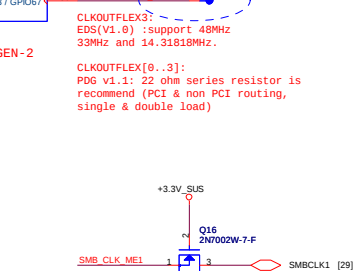


IBEX PEAK-M (PCI-E, SMBUS, CLK)

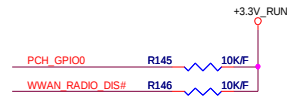
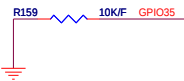
Place TX DC blocking caps close PCH.



Boot BIOS Strap		
PCI_GNT0#	PCI_GNT1#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

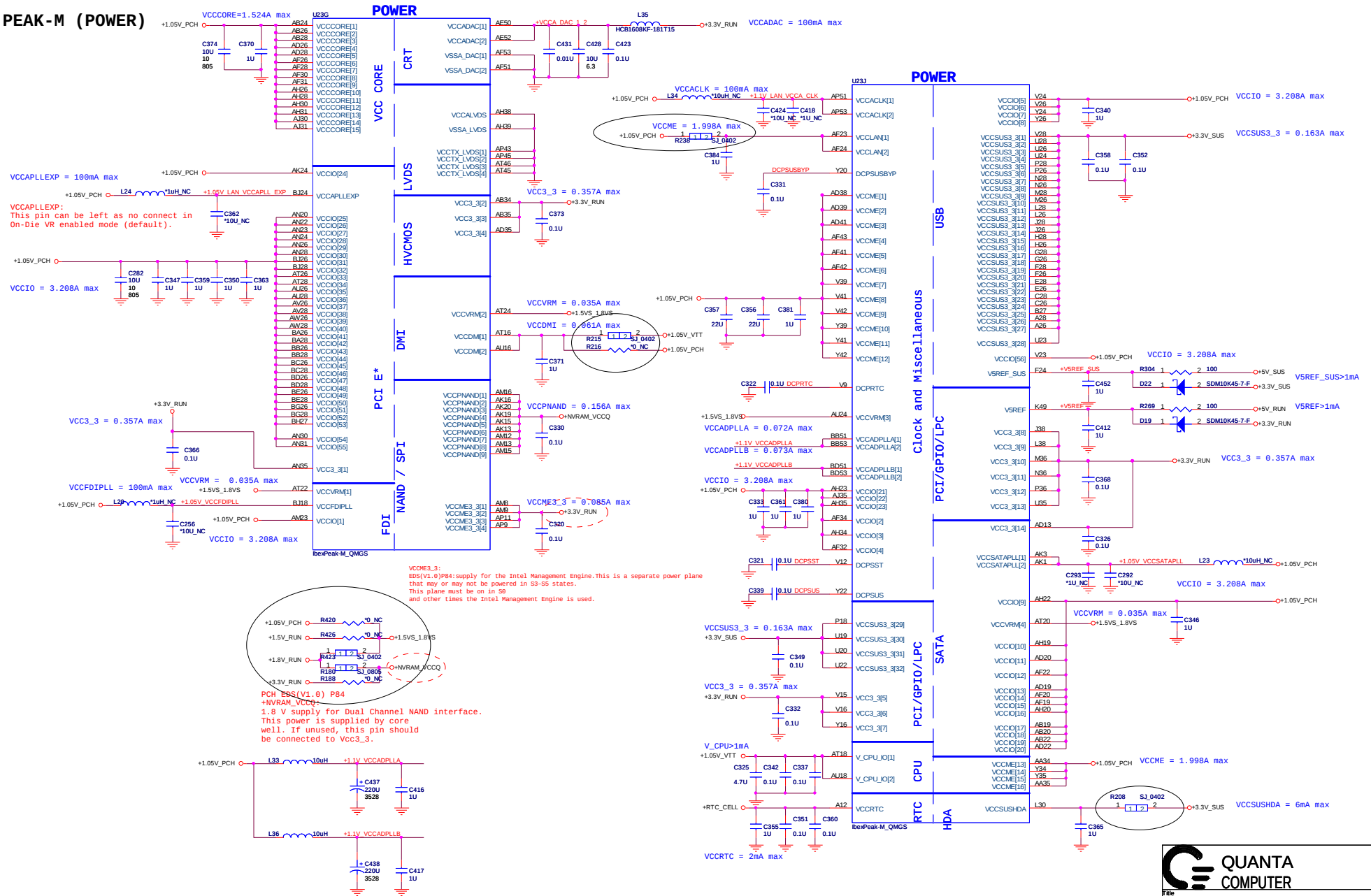
BMBUSY#:
If not used, require a weak pull-up
(8.2- K Ω to 10 k Ω) to Vcc3.3.
CRB(V1.0)P28: It has 1K PU and
100 ohm on this net for validation purpose.

WWAN_RADIO_DIS# 1-X High = Strong (Default)



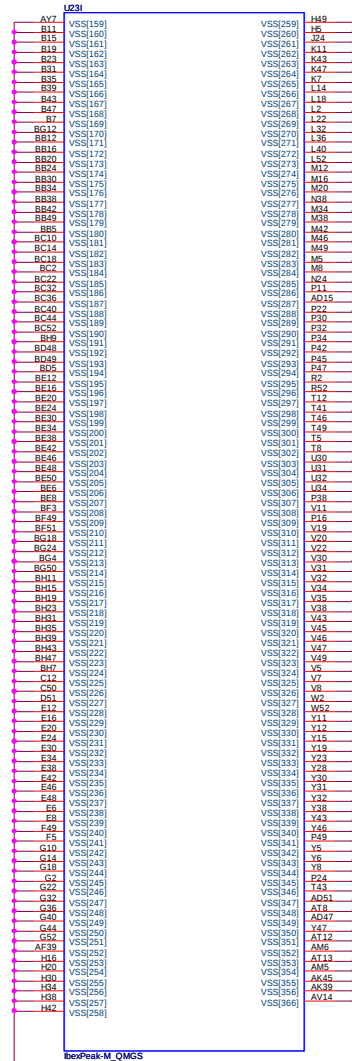
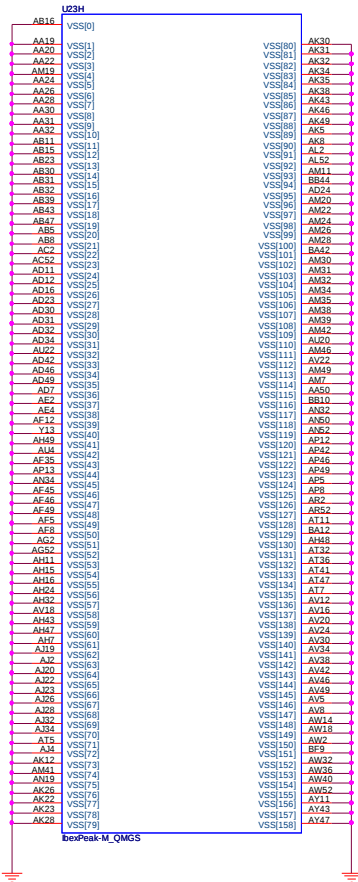
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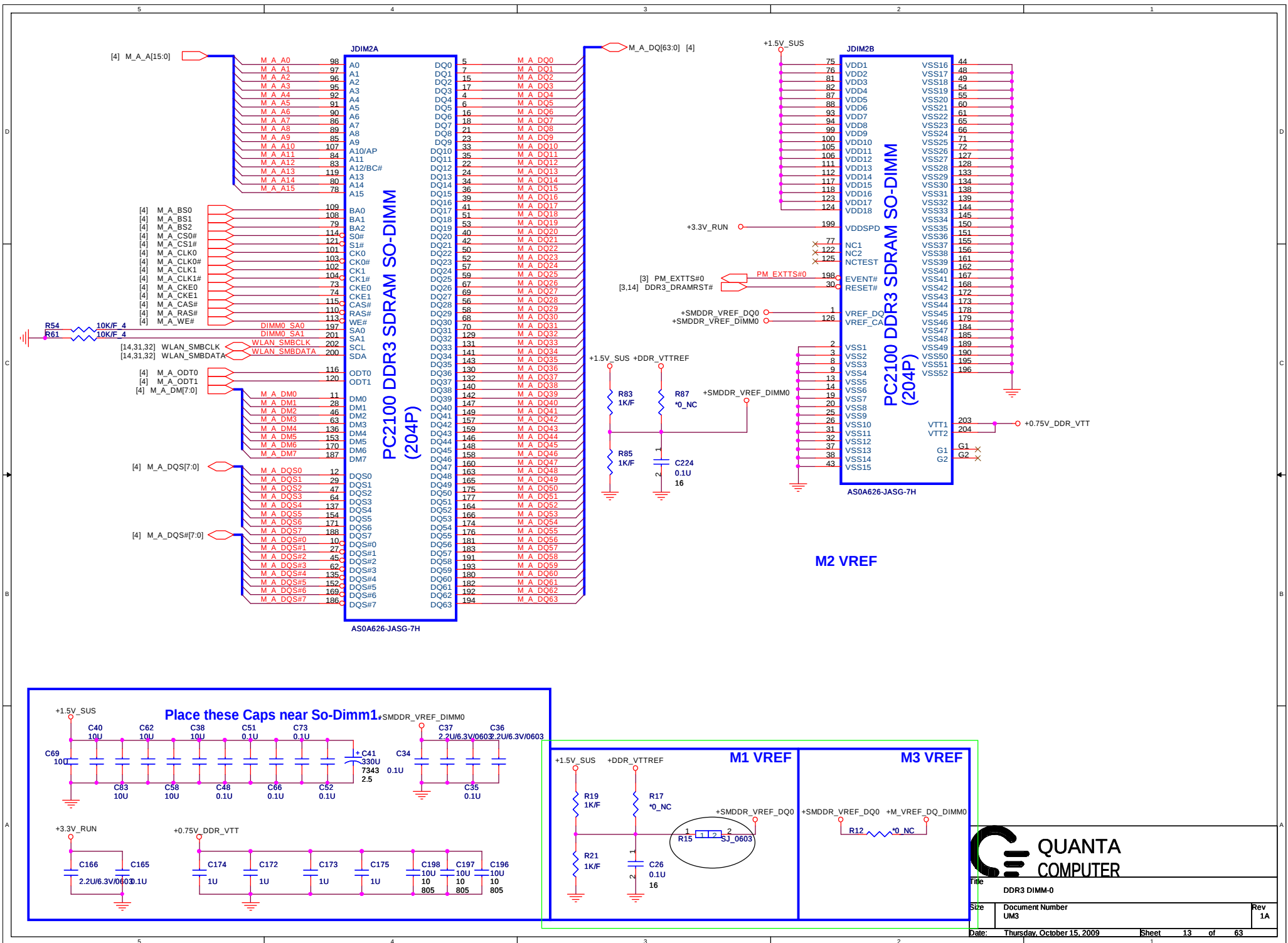
IBEX PEAK-M (POWER)

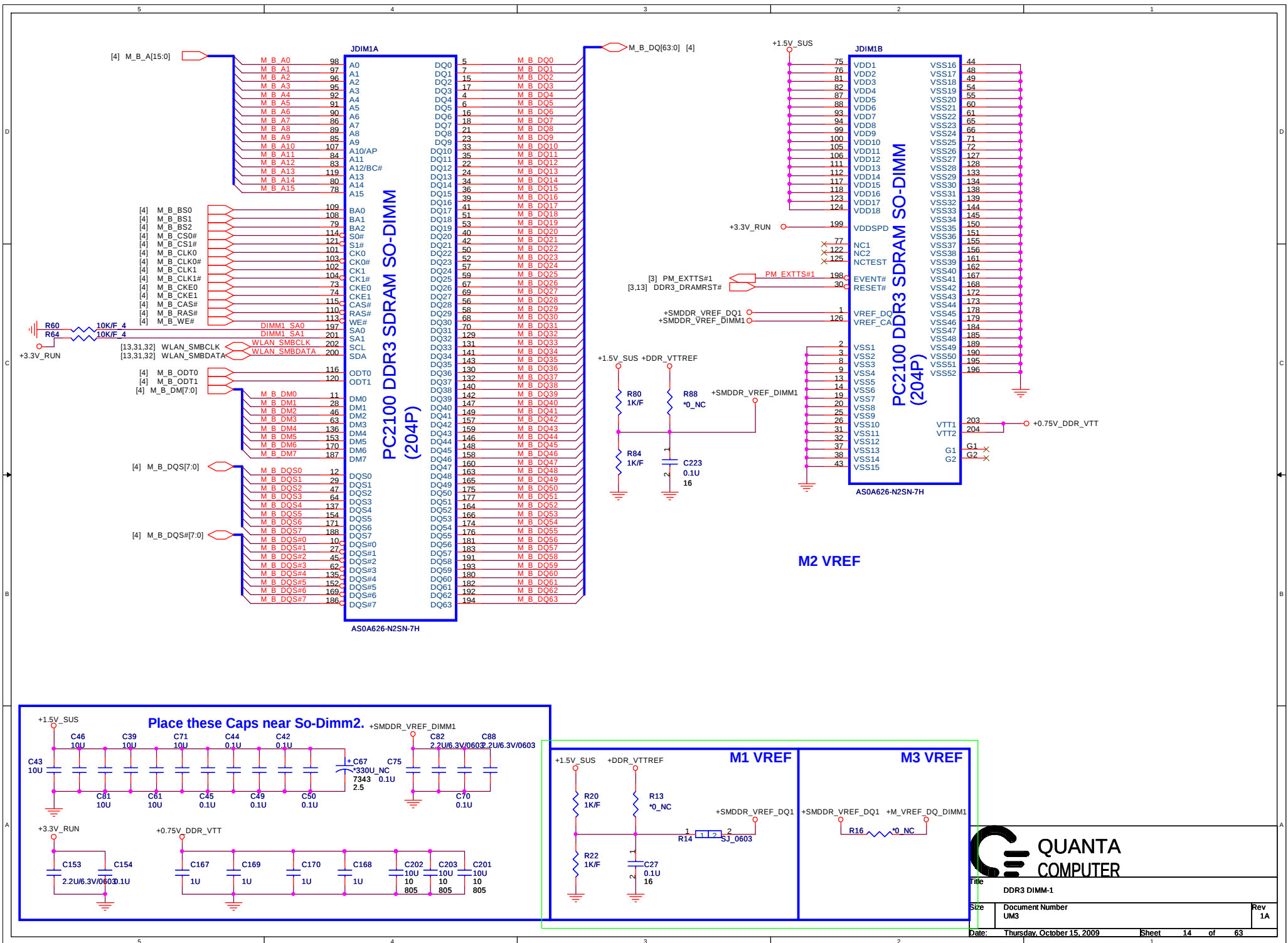


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IBEX PEAK-M 5/6			
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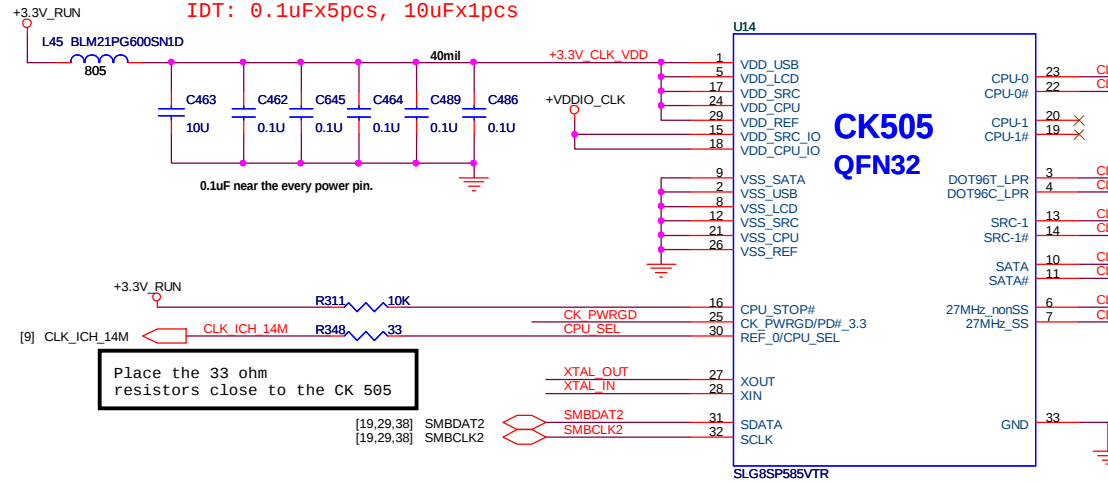
IBEX PEAK-M (GND)



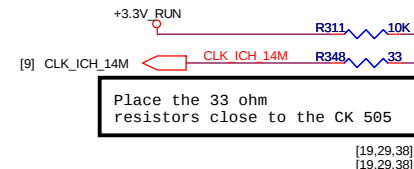




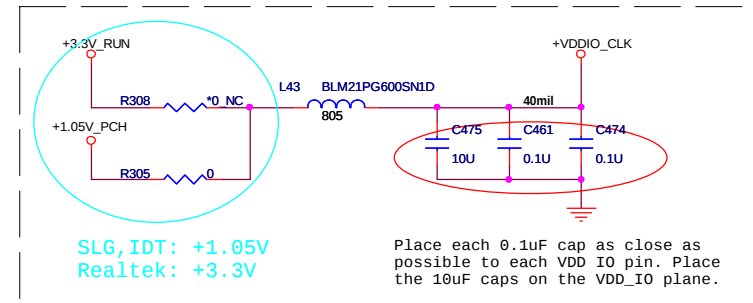
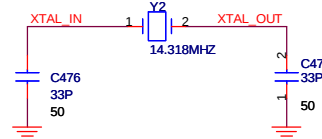
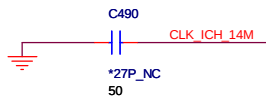
Realtek: 0.1uFx6pcs, 22uFx1pcs
IDT: 0.1uFx5pcs, 10uFx1pcs



Place within 0.5" of CLKGEN

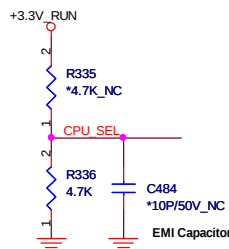


Add capacitor pads for improving WWAN.



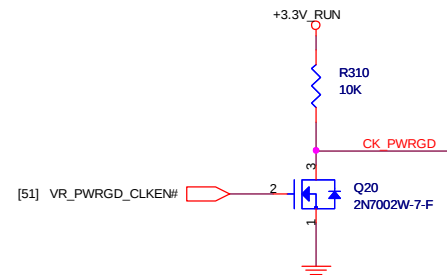
SLG, IDT: +1.05V
Realtek: +3.3V

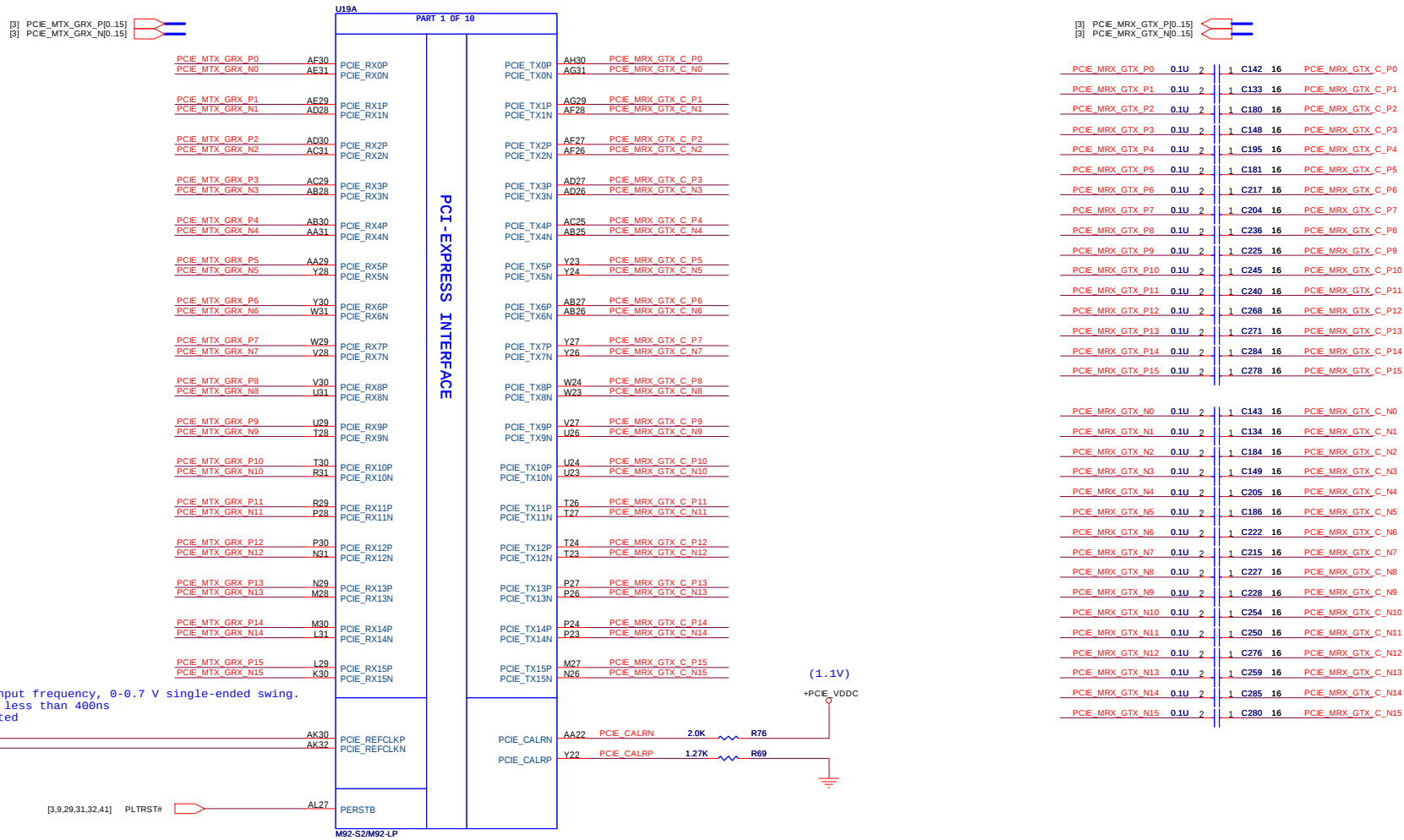
+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.
Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V.
IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.



PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet (V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet (V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.



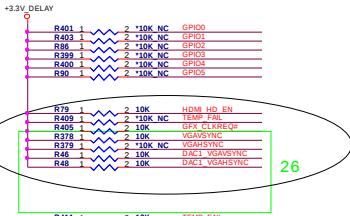


M92-S2 XT AJ072800T04 100-C61675(216-0728004)
M92-S2 AJ072800T03 100-C61643(216-0728003)

MEMORY APERTURE SIZE SELECT					
MEMORY SIZE	CFG3 GP109	CFG2 GP1013	CFG1 GP1012	CFG0 GP1011	
128MB		0	0	0	
256MB		0	0	1	
512MB		0	1	0	
512MB		1	0	0	



GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	FW setting
GPIO0	GPIO0: TL PWM5 ENB (Transceiver Power Savings Enable) 0: 50% Tx output swing for enable mode 1: Full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO1: TL_DEEMPH_EN (Transceiver De-emphasis Enable) 0: 1 to de-emphasis disabled for enable mode 1: 1 to de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO2: BIF_GBN2_EN (5.0 GT/s Enable) 0: 5.0 Gbps (Default setting for Desktop) 1: 5.0 Gbps (Default setting for Desktop)	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO5: AC_BATT 0: Battery saving mode = 0.0 V 1: AC (Performance mode) = 0.0 V	0
GPIO6	ATI Internal use only	0
HSYNC (A426)	00: No Audio function 01: Audio for DisplayPort only 10: Audio for DisplayPort only and HDMI if dongle is detected 11: Audio for both DisplayPort and HDMI. HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	
VSYNC (A327)		

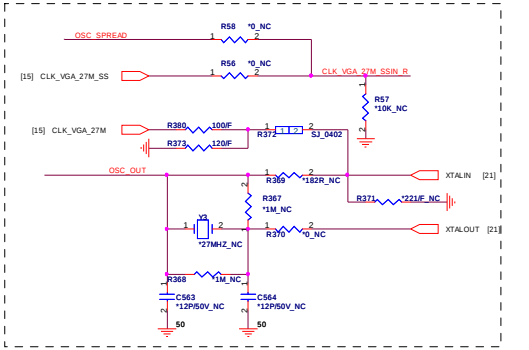
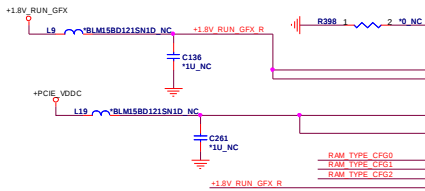


Memory Straps	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Quanta PN (winBuy)	Vendor PN	31 level PN
800MHz	0	0	0	AKD5LGGT582		K4W1G1646E-HC12	
512MB(64M*16) Samsung	0	0	1	AKD5LGGT582		K4W1G1646E-HC12	
800MHz	0	1	0	AKD5LZGTW00		H5TQ1663BFR-12C	
512MB(64M*16) Hynix	0	1	0	AKD5LZGTW00		H5TQ1663BFR-12C	



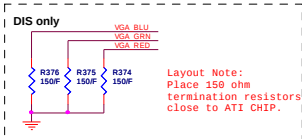
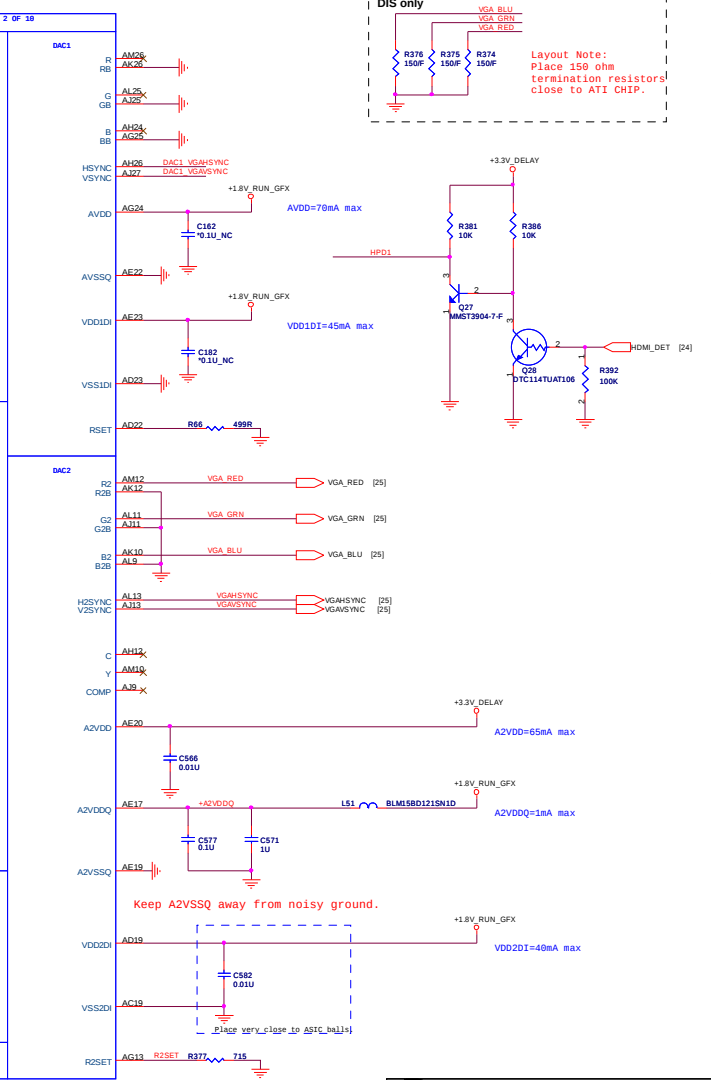
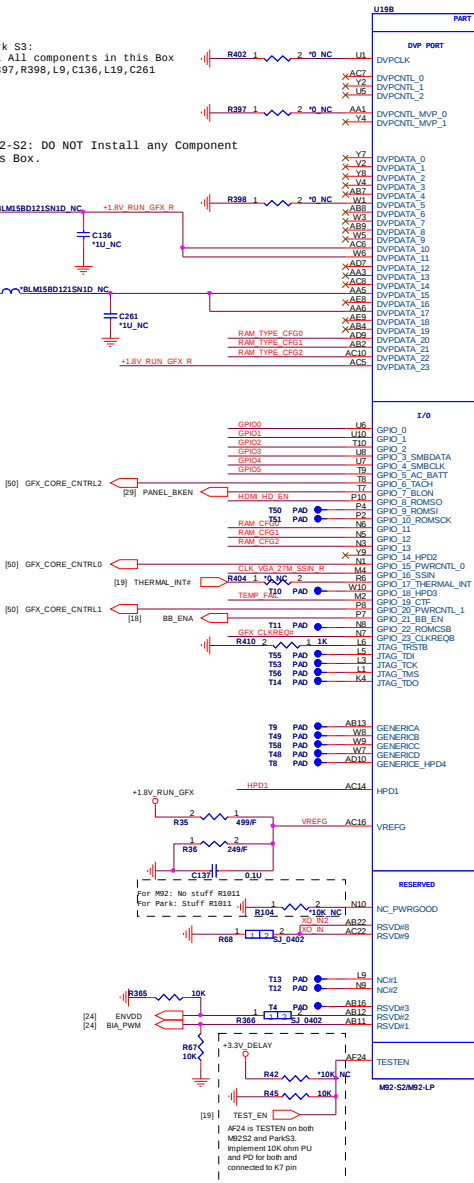
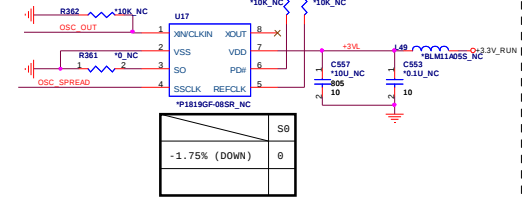
For Park S3:
Install All components in this Box
R402, R397, R398, L9, C136, L19, C261

For M92-S2: DO NOT Install any Component in this Box.



Spread Spectrum

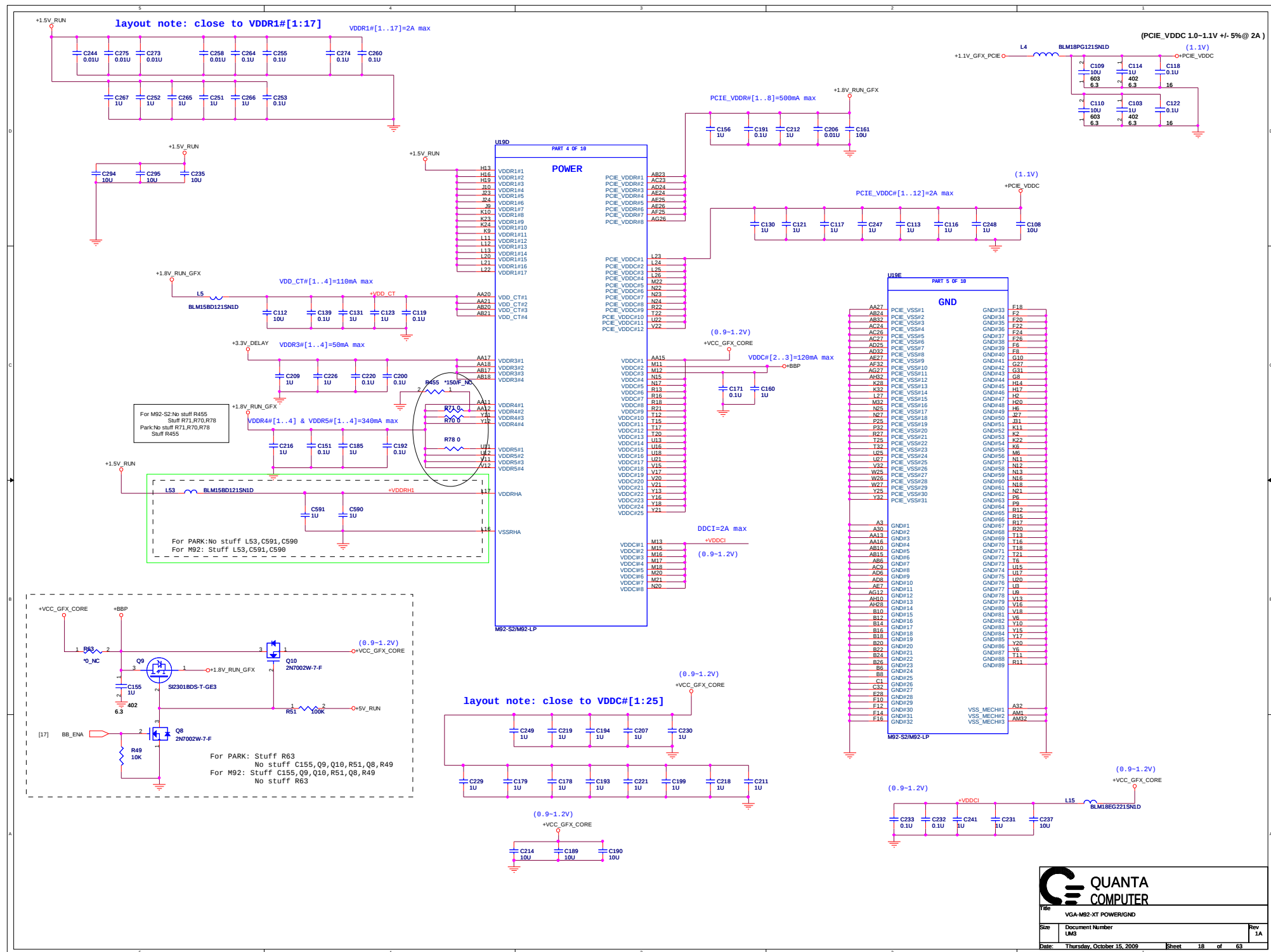
If U4, the discrete spread spectrum chip is not used, then pop R48 in order to pull-down BXTALOUT for EMI reasons.

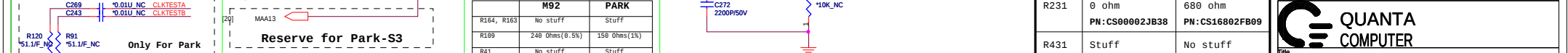
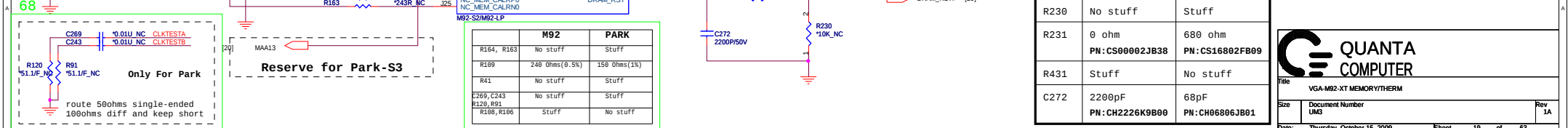


Layout Note:
Place 150 ohm termination resistors close to ATI CHIP.

QUANTA COMPUTER

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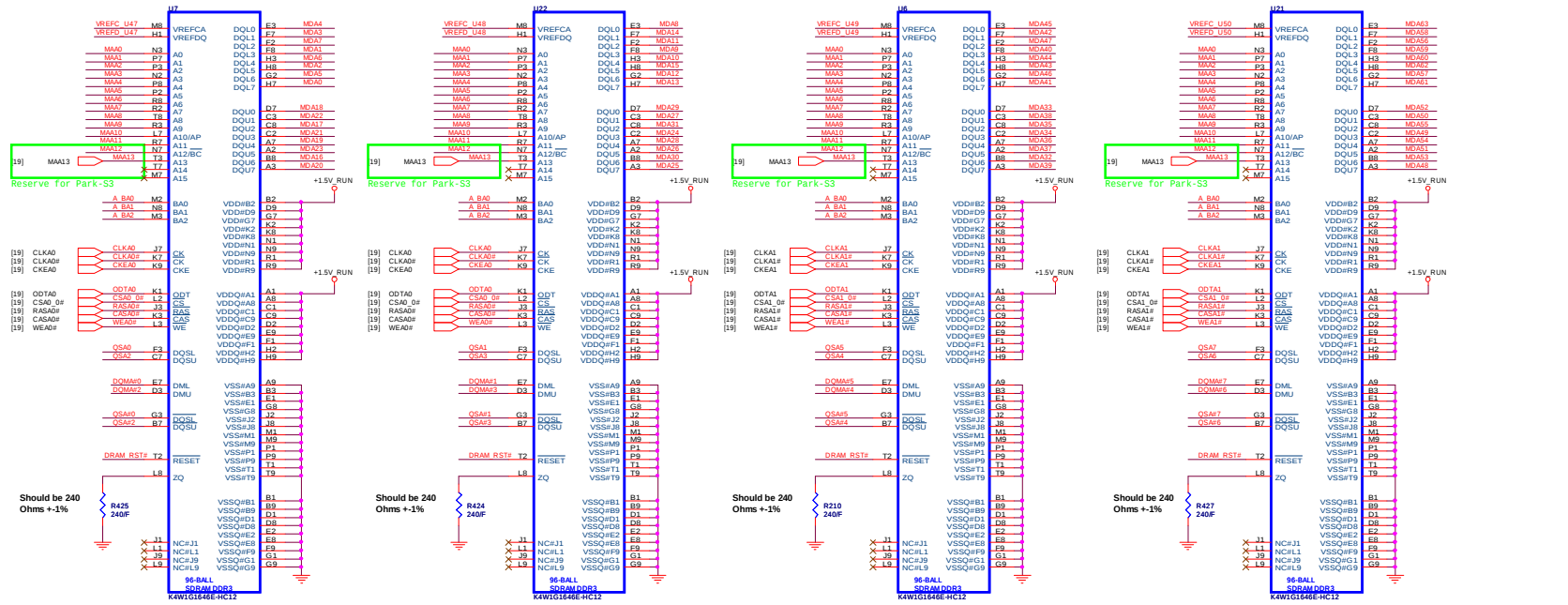


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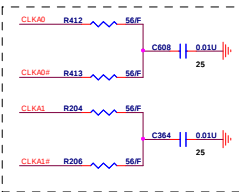
 route 50ohms single-ended 100ohms diff and keep short		<table border="1"> <tr> <td>C269, C243</td> <td>No stuff</td> <td>Stuff</td> </tr> <tr> <td>R120, R91</td> <td></td> <td></td> </tr> <tr> <td>R108, R106</td> <td>Stuff</td> <td>No stuff</td> </tr> </table>	C269, C243	No stuff	Stuff	R120, R91			R108, R106	Stuff	No stuff			<table border="1"> <tr> <td>C272</td> <td>2200pF</td> <td>68pF</td> </tr> <tr> <td>PN: CH2226K9B00</td> <td></td> <td>PN: CH06806JB01</td> </tr> </table>	C272	2200pF	68pF	PN: CH2226K9B00		PN: CH06806JB01	<table border="1"> <tr> <td colspan="3">VGA-M02-KT MEMORY/THERM</td> </tr> <tr> <td>Size</td> <td>Document Number</td> <td>Rev</td> </tr> <tr> <td></td> <td>UM3</td> <td>1A</td> </tr> <tr> <td colspan="3">Date: Thursday, October 15, 2009</td> </tr> <tr> <td></td> <td>Sheet</td> <td>19 of 63</td> </tr> </table>	VGA-M02-KT MEMORY/THERM			Size	Document Number	Rev		UM3	1A	Date: Thursday, October 15, 2009				Sheet	19 of 63
C269, C243	No stuff	Stuff																																		
R120, R91																																				
R108, R106	Stuff	No stuff																																		
C272	2200pF	68pF																																		
PN: CH2226K9B00		PN: CH06806JB01																																		
VGA-M02-KT MEMORY/THERM																																				
Size	Document Number	Rev																																		
	UM3	1A																																		
Date: Thursday, October 15, 2009																																				
	Sheet	19 of 63																																		
5		4	3	2	1																															

- [19] MD4[3..0]
- [19] MA4[12..0]
- [19] Q5A[7..0]
- [19] Q5A[7..0]
- [19] QDMA[7..0]
- [19] DRAM_RSTn
- [19] A_BA2[0]

DDR3



Placement has to be close to VRAM

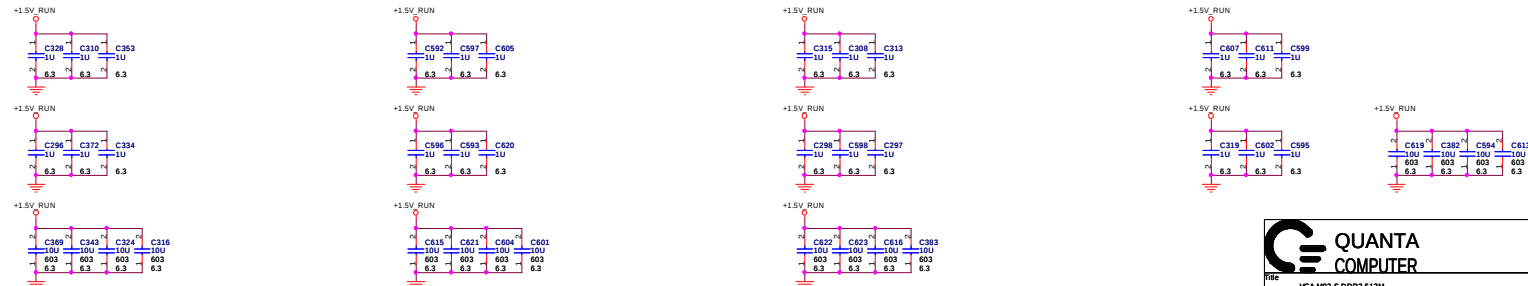


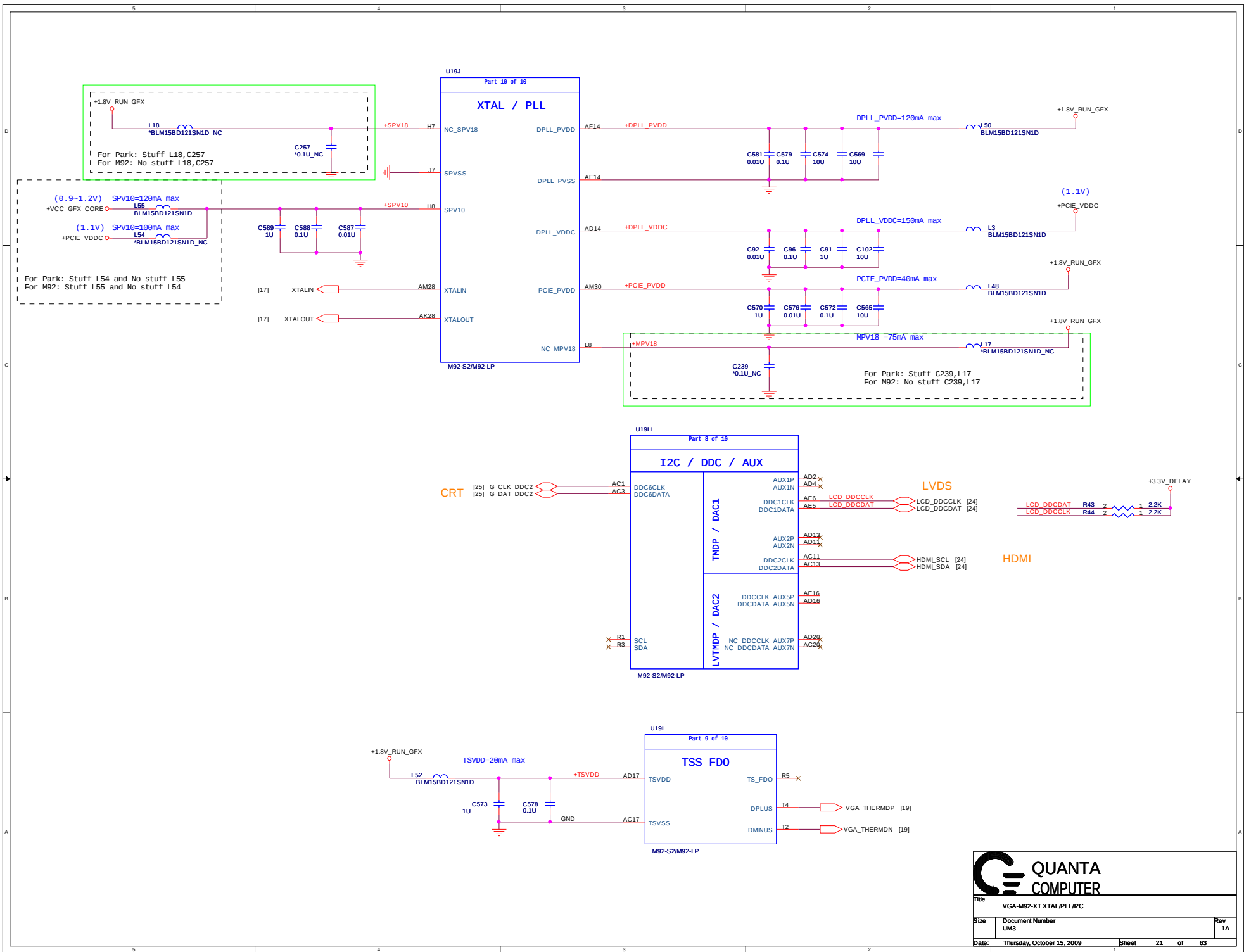
close to U47

close to U48

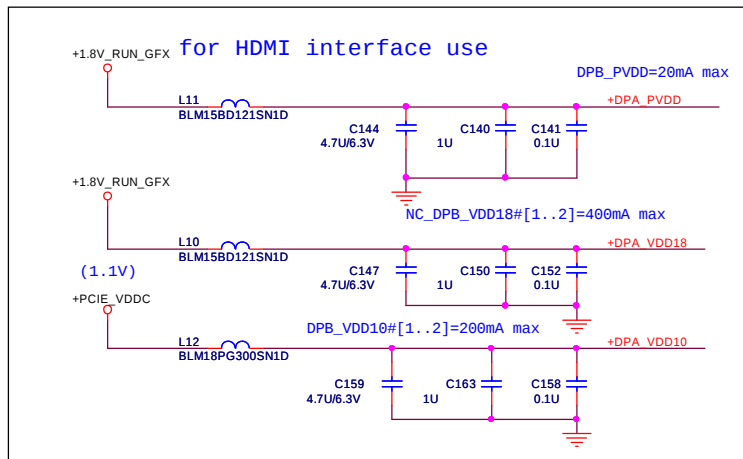
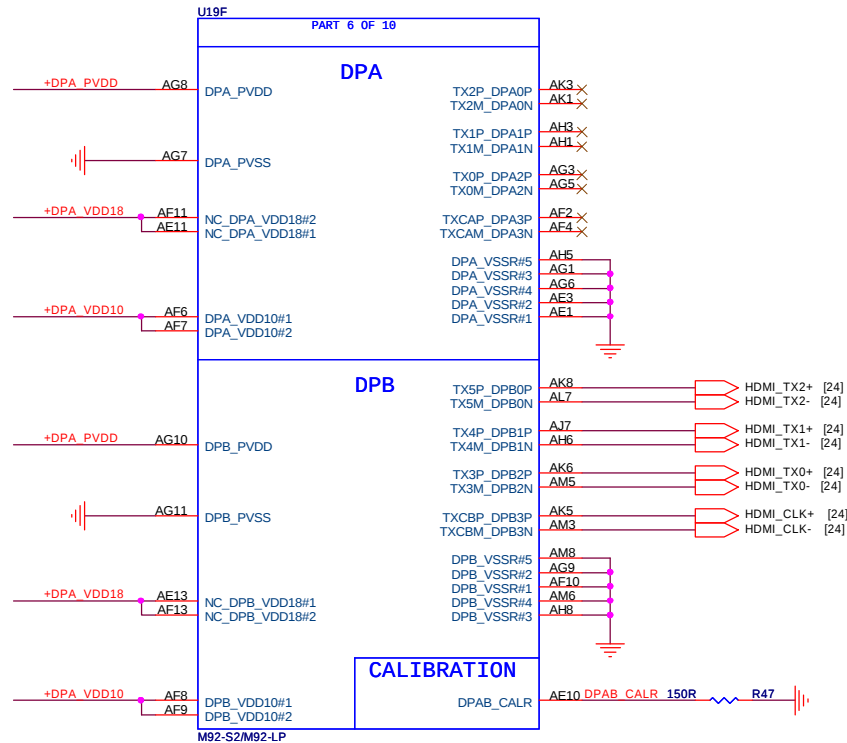
close to U49

close to U50

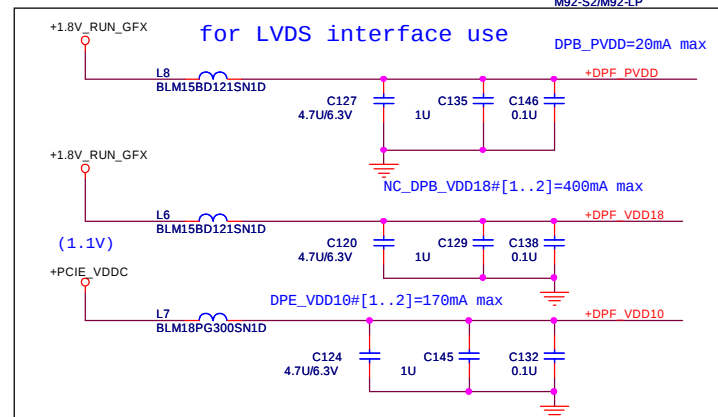
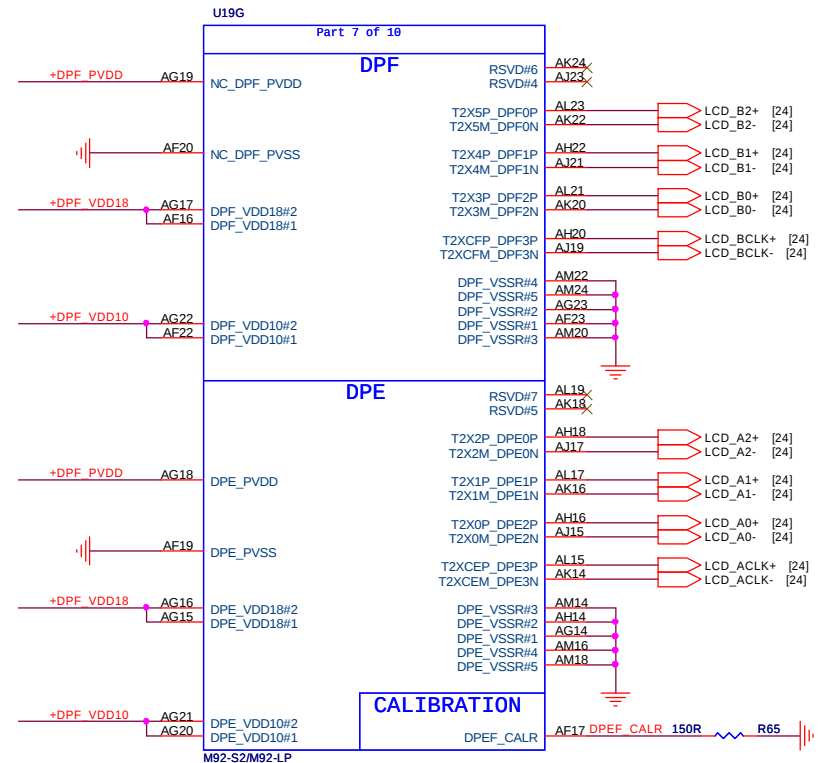




TMDP(HDMI) INTERFACE



LVDS INTERFACE



D

D

C

C

B

8

A

A

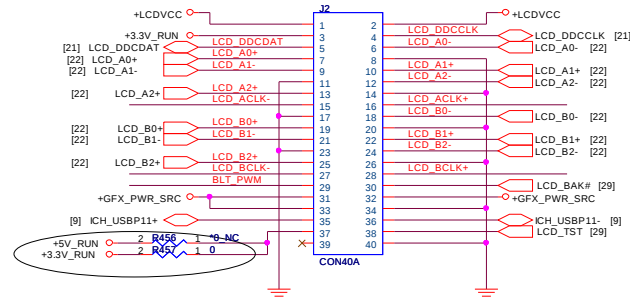
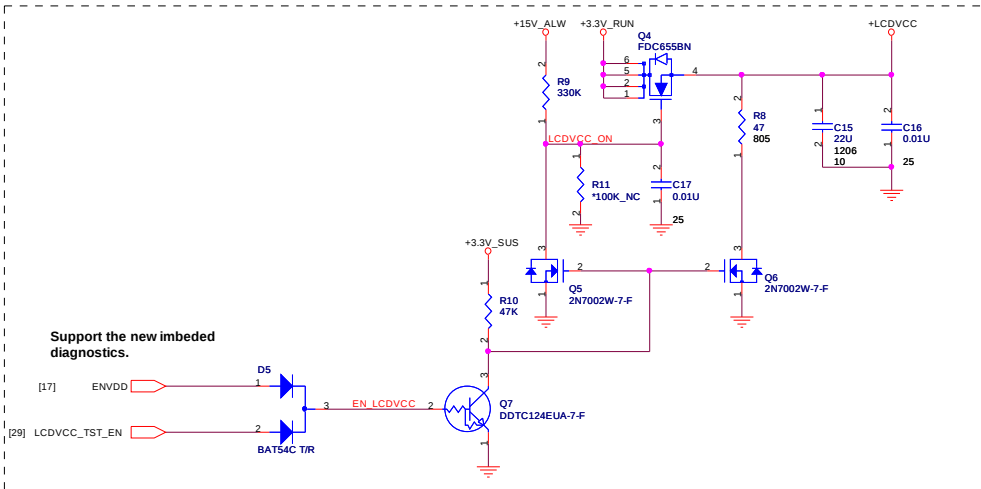


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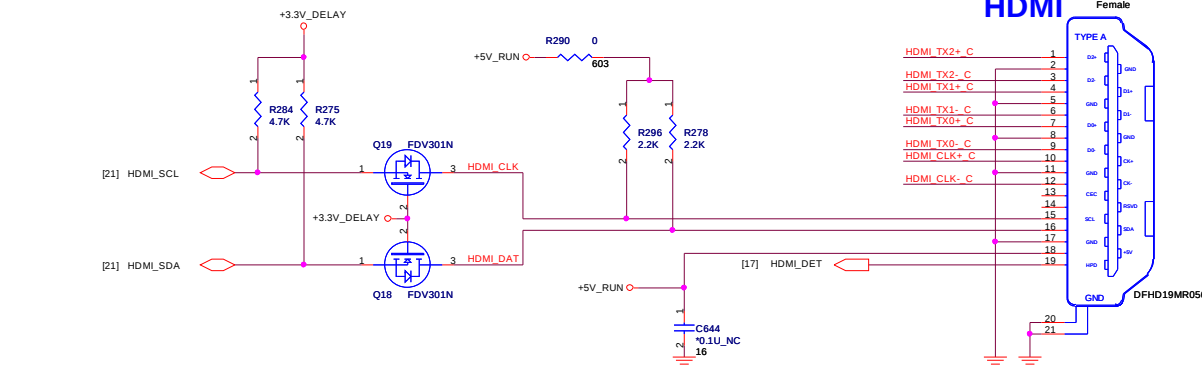
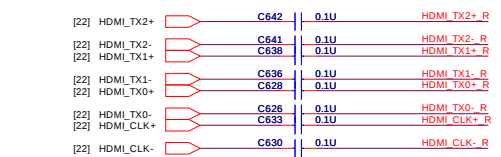
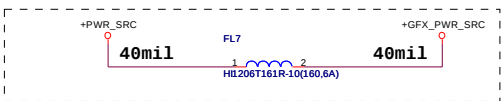
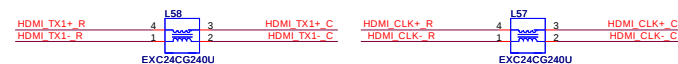
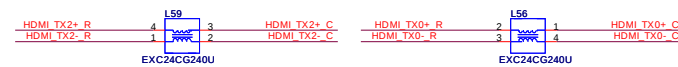
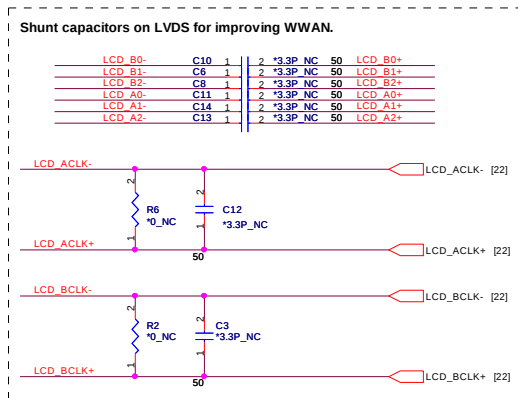
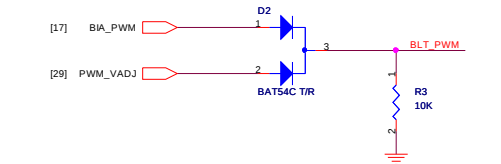
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Rev	
1A	

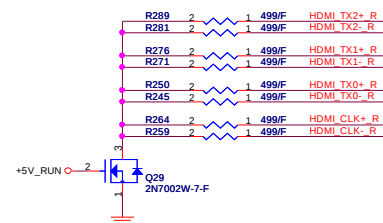
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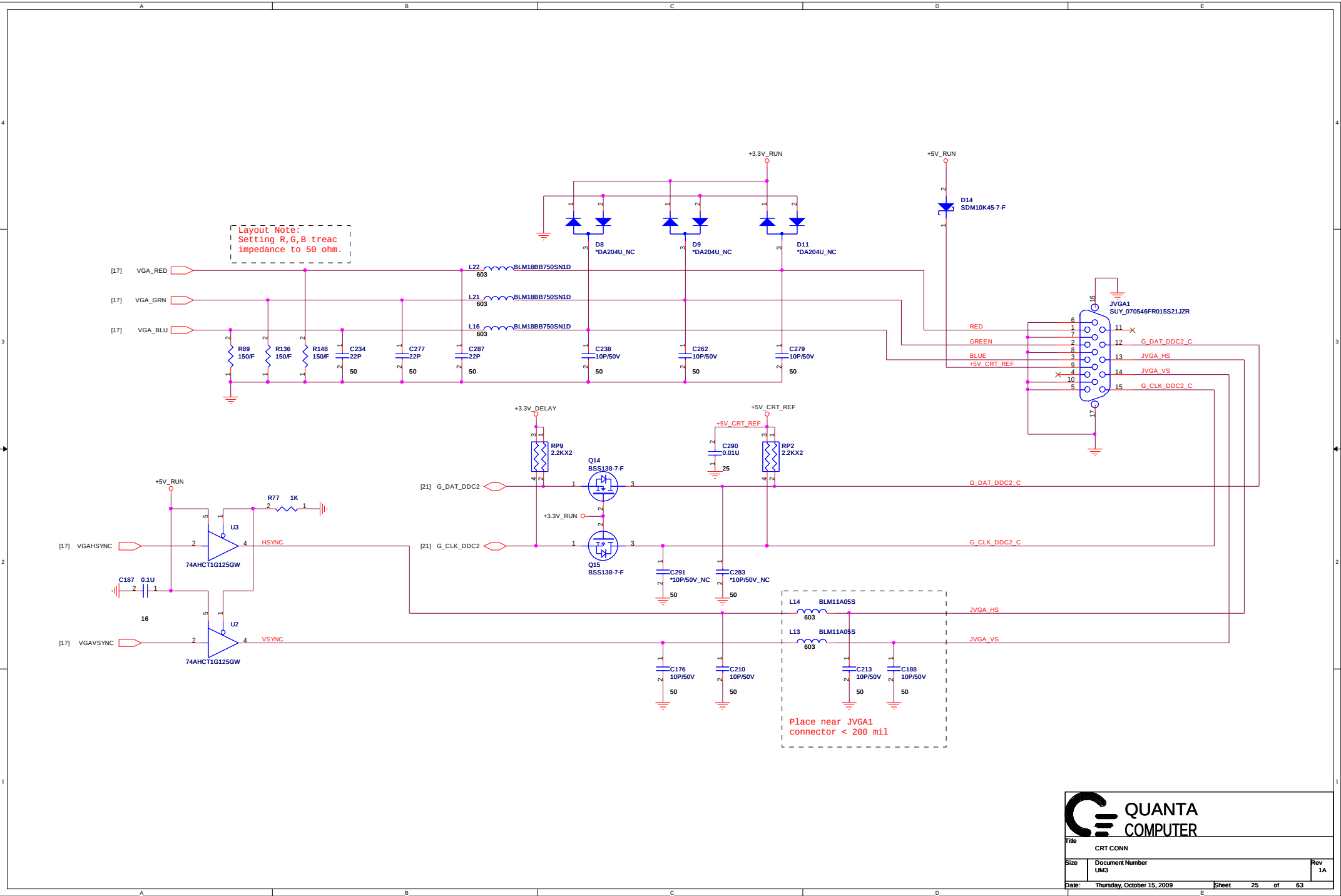


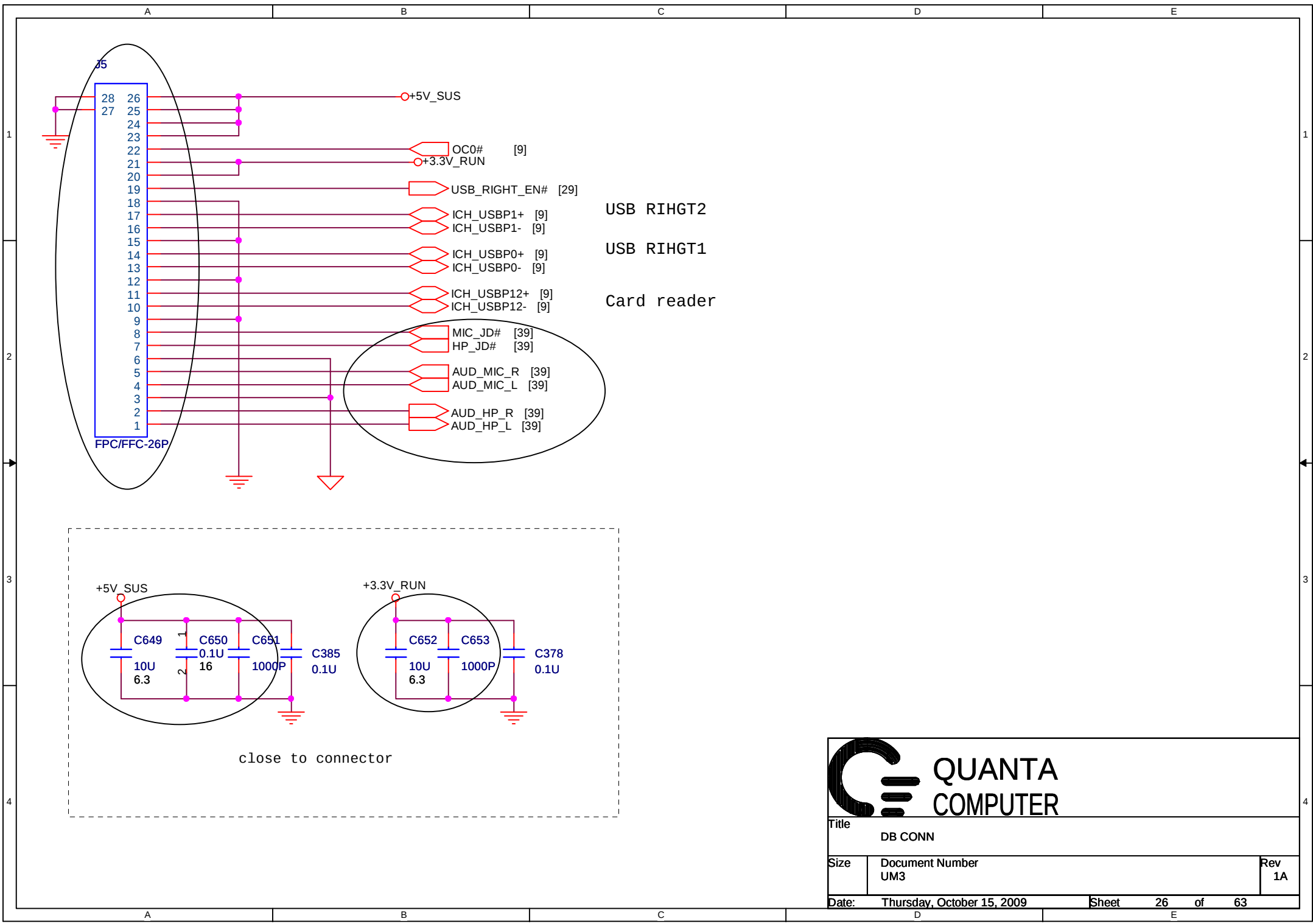
Need to check DFWF40MR000



DFHD19MR056







	A	B	C	D	E
1					
2					
3					
4					

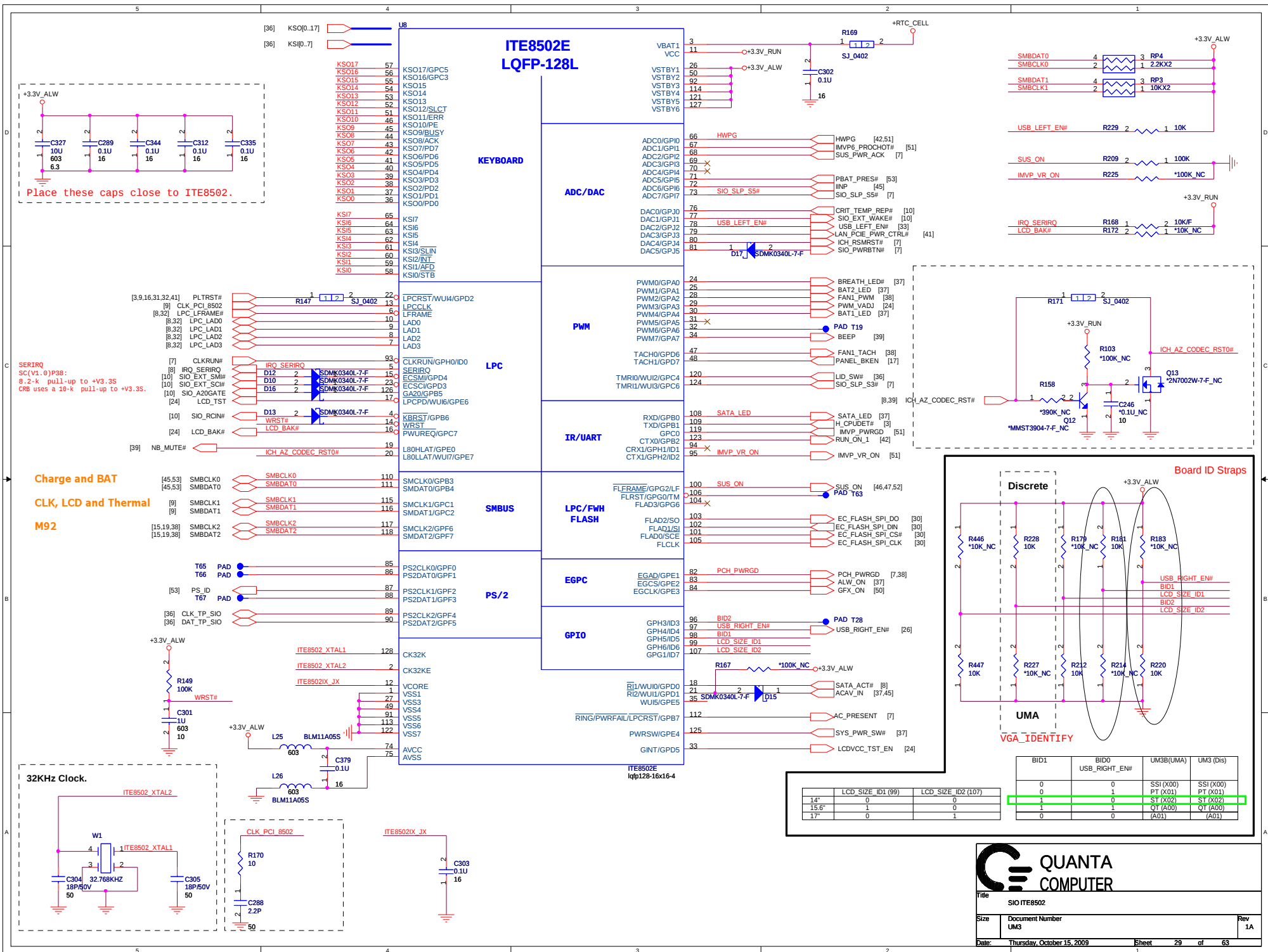
 QUANTA COMPUTER			
Title Blank Page			
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	1	2	3	4	5	6	7	8
A								
B								
C								
D								
	1	2	3	4	5	6	7	8



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COMPUTER

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	LCD_SIZE_ID1 (99)	LCD_SIZE_ID2 (107)
14"	0	0
15.6"	1	0
17"	0	1

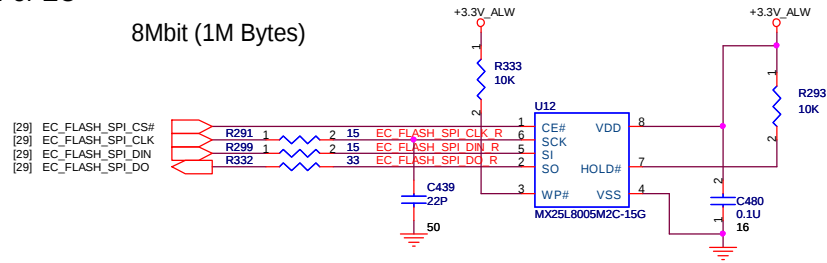
BID1	BID0	UM3B(UMA)	UM3 (Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	QT (A00)	QT (A00)
0	0	A01	A01



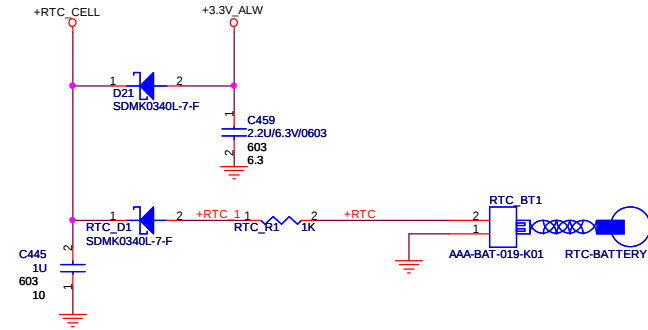
Title	SIO ITE8502		
Size	Document Number	Rev	1A
	UM3		
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For EC

8Mbit (1M Bytes)

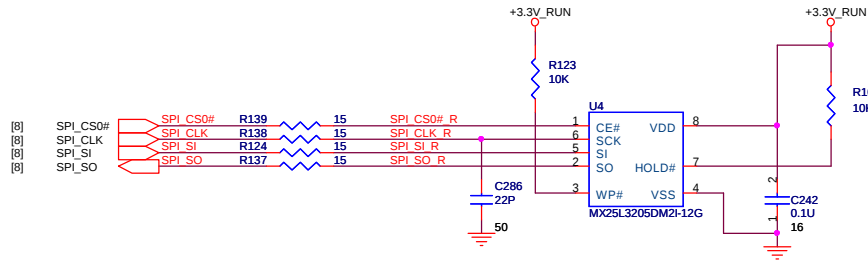


RTC BATTERY



For PCH

32Mbit (4M Bytes)



Title
FLASH/RTC

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Document Number
UM3

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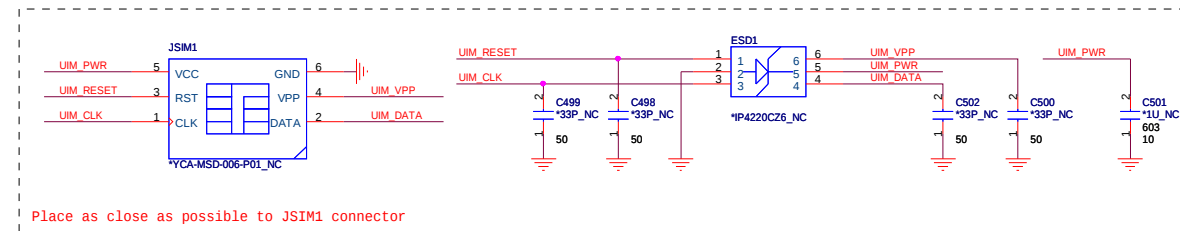
Rev
1A

Diagram illustrating the J11 connector pin connections for the LTS_AAA-PCI-092-K01_NC module. The diagram shows the internal wiring of the J11 connector, including power supply connections (+3.3V_RUN, +1.5V_RUN), signal connections (MINI2CLK_REQ#, CLK_PCIE_MINI2#, PCIE_RX1, PCIE_RX1+, PCIE_TX1, PCIE_TX1+, PCIE_MCARD2_DET#), and various peripheral signals (UIM_PWR, UIM_DATA, UIM_CLK, UIM_RESET, UIM_VPP, W_WAN_RADIO_DIS#, PLTRST#, WLAN_SMBCLK, WLAN_SMBDATA, USBP5_D-, USBP5_D+, USB_MCARD2_DET#).

Key connections include:

- Power:** +3.3V_RUN and +1.5V_RUN connections to pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51.
- Signal:** MINI2CLK_REQ# (pins 1, 3), CLK_PCIE_MINI2# (pins 5, 7), PCIE_RX1 (pins 9, 11), PCIE_RX1+ (pins 13, 15), PCIE_TX1 (pins 17, 19), PCIE_TX1+ (pins 21, 23), PCIE_MCARD2_DET# (pins 25, 27).
- Peripheral:** UIM_PWR (pins 29, 31), UIM_DATA (pins 33, 35), UIM_CLK (pins 37, 39), UIM_RESET (pins 41, 43), UIM_VPP (pins 45, 47), W_WAN_RADIO_DIS# (pins 49, 51), PLTRST# (pins 53, 55), WLAN_SMBCLK (pins 59, 61), WLAN_SMBDATA (pins 63, 65), USBP5_D- (pins 69, 71), USBP5_D+ (pins 73, 75), USB_MCARD2_DET# (pins 79, 81).

The diagram is labeled "LTS_AAA-PCI-092-K01_NC" at the bottom.

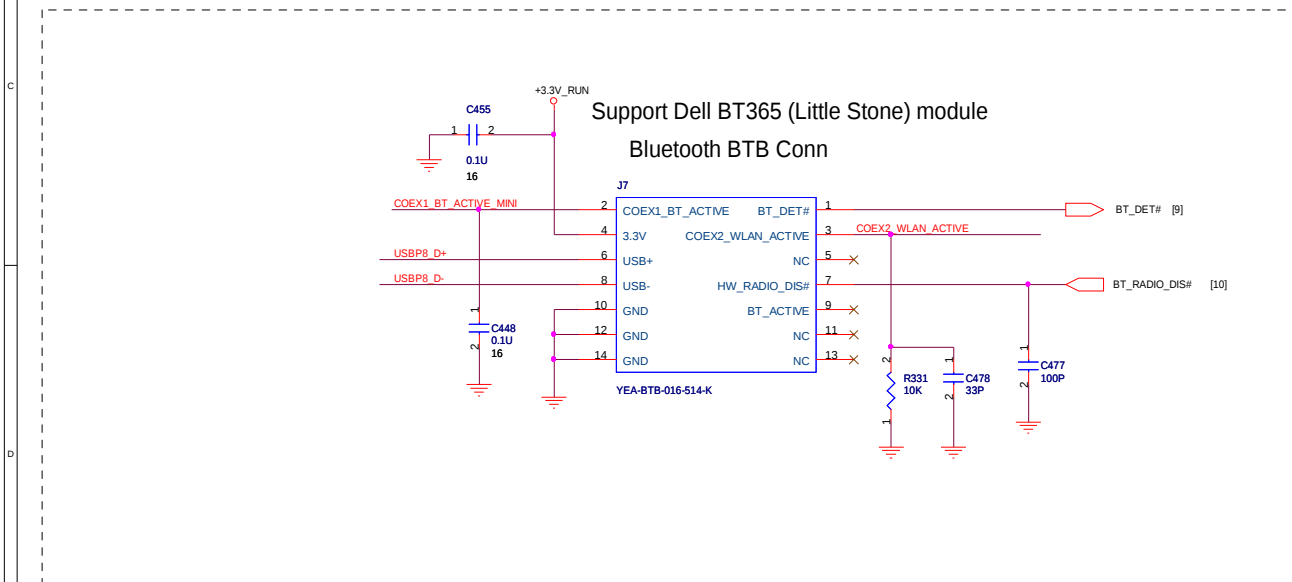
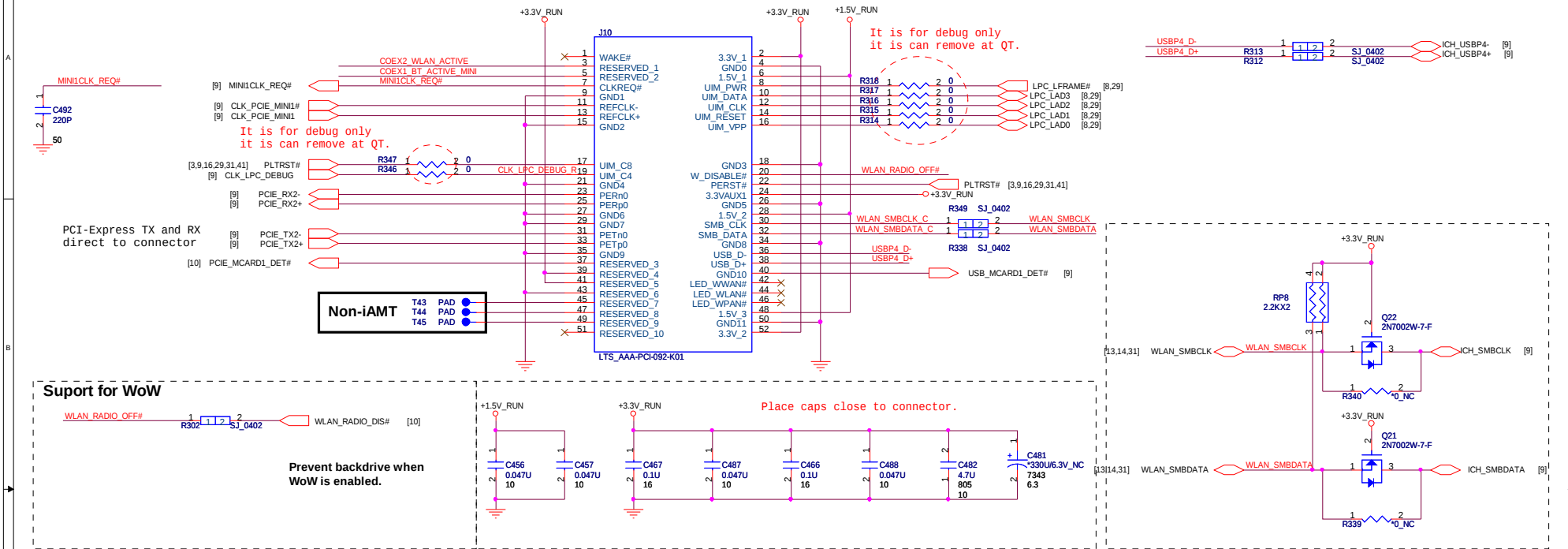


Place caps close to connector.

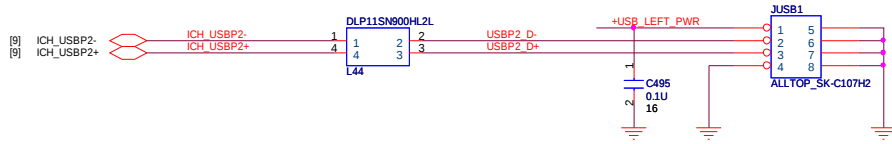
Capacitor values and footprints for the +1.5V_RUN and +3.3V_RUN rails:

- +1.5V_RUN: C468 (0.047uF, 10), C470 (33pF, 50)
- +3.3V_RUN: C465 (33pF, 50), C471 (0.047uF, 10), C472 (33pF, 50), C469 (0.047uF, 10), C483 (100uF, 6.3), C485 (330uF, 6.3)

MiniCard WLAN connector

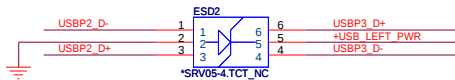


External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

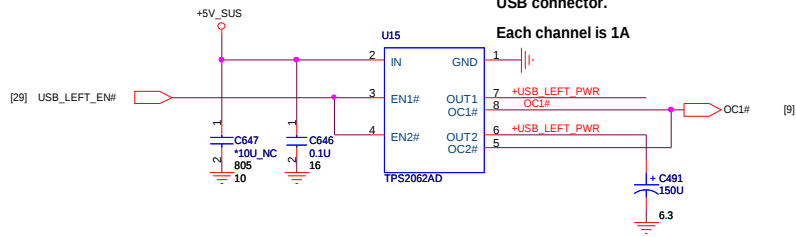


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.

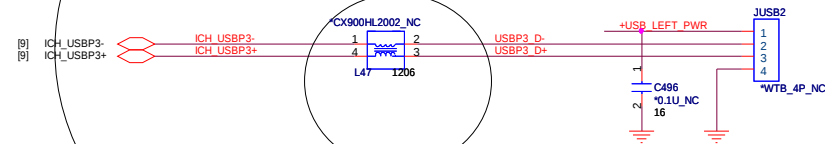


Place one 150uF cap by each USB connector.
Each channel is 1A



REV FOR 17"

Add L47 ,C496 , JUSB2 for UM5



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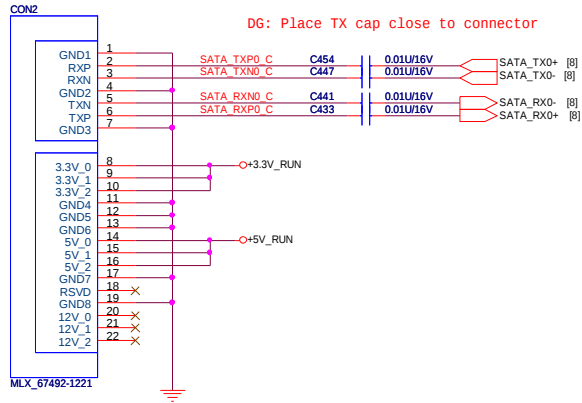
Document Number UM3

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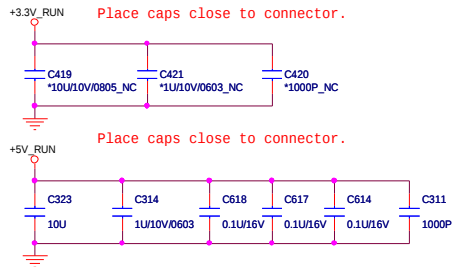
SATA Connector.



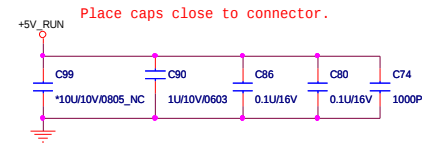
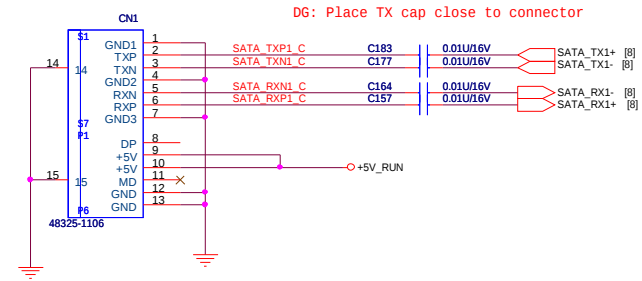
UM5與UM3/6不同，只差在高度，footprint沒變

UM5/UM5B
PN:DFHS22FR137
Mfr:67492-1224

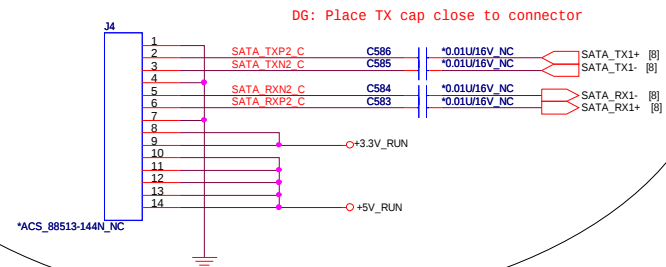
UM3/UM3B/UM6/UM6B
PN:DFHS22FR0B2
Mfr:67492-1921



ODD Connector

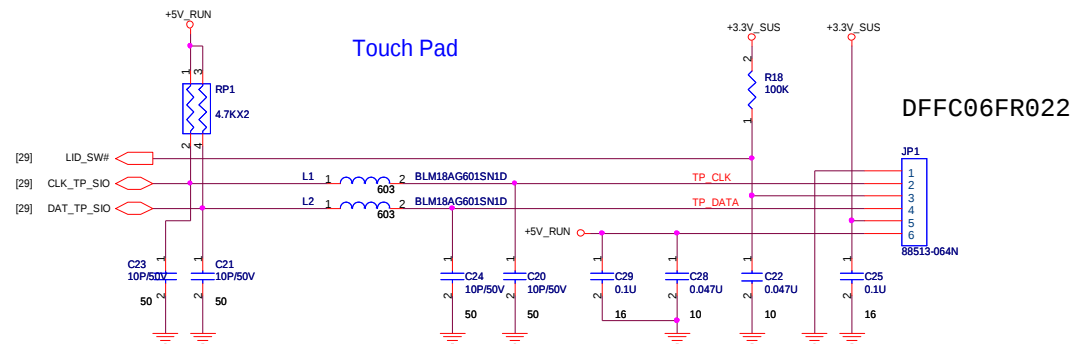


REV FOR 15.6"



Title	SATA (HDD&CD_ROM)		
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Touch Pad

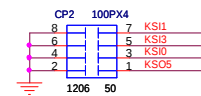
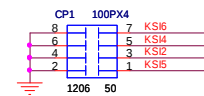
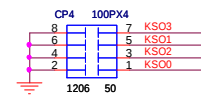
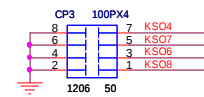
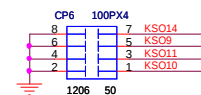
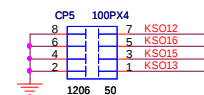
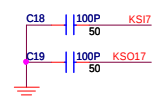
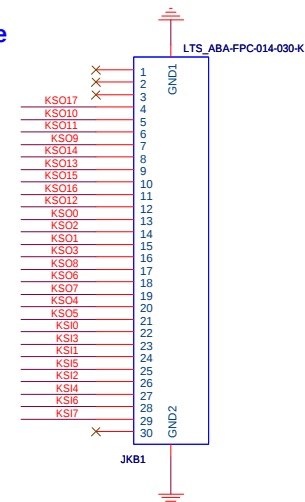


KEYBOARD CONNECTOR

Top side

[29] KSO[0..17]

[29] KSI[0..7]

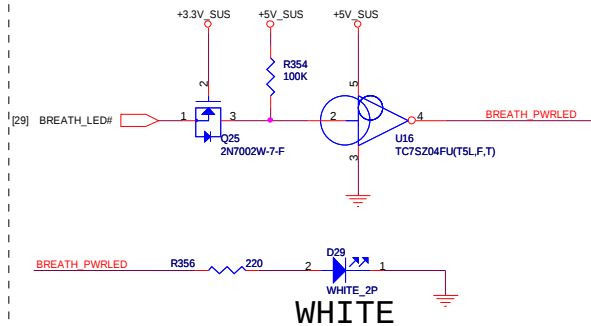


100P CAPS CLOSE TO JKB1

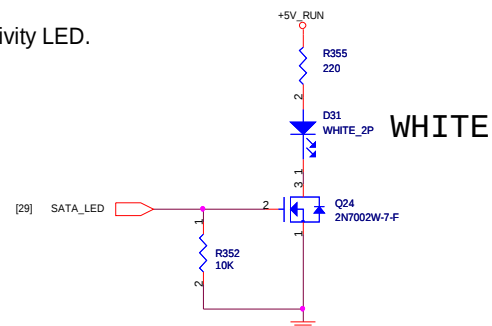


Title			TOUCH PAD, KB
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Power

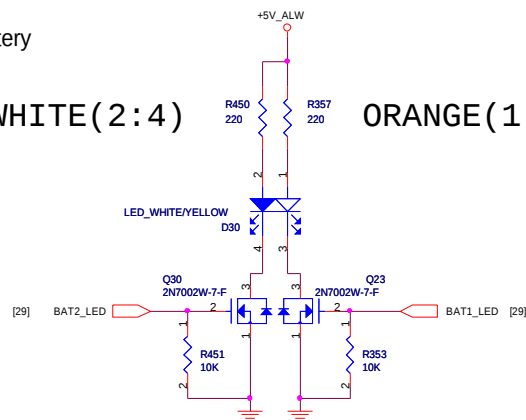


HDD activity LED.

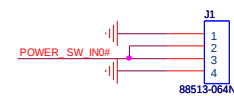


Battery

WHITE(2:4) ORANGE(1:3)



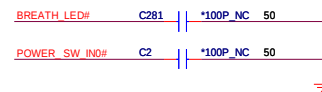
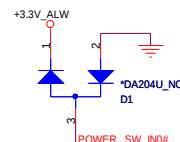
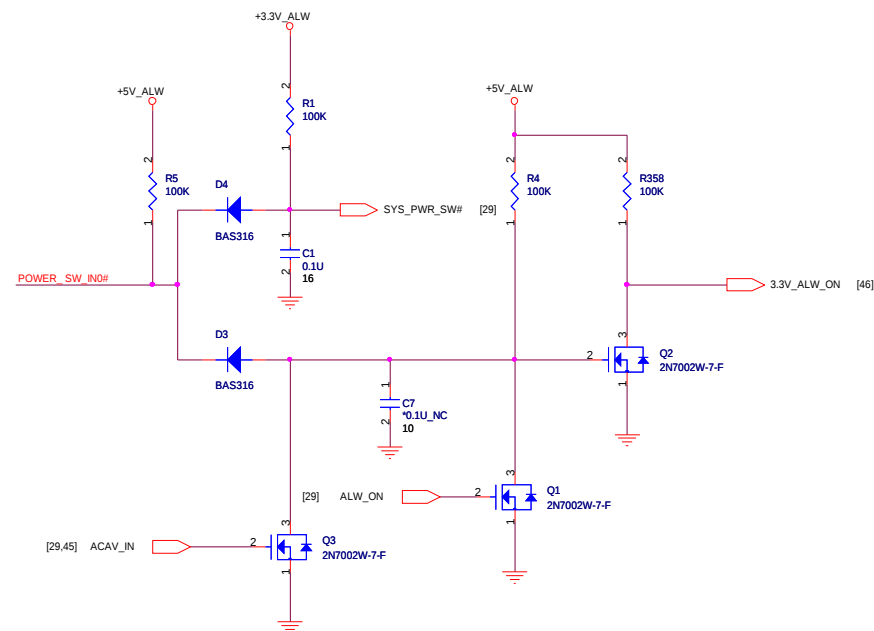
Power button Cable



Stephen 7/31

DFFC04FR014

3VALW ON POWER LOGIC



Title SWITCH, LED

Size Document Number UM3

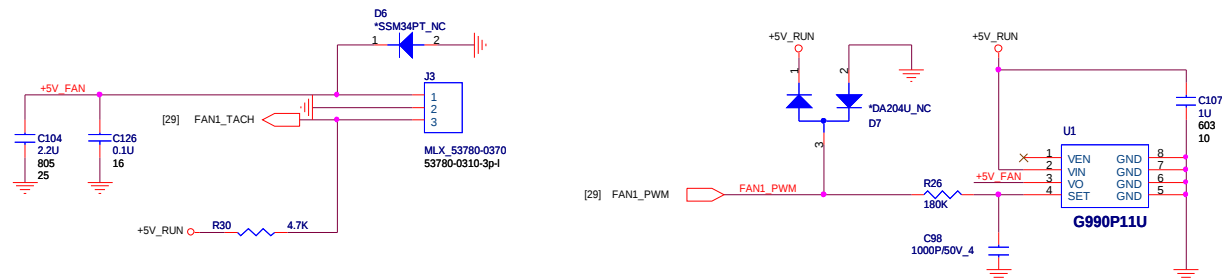
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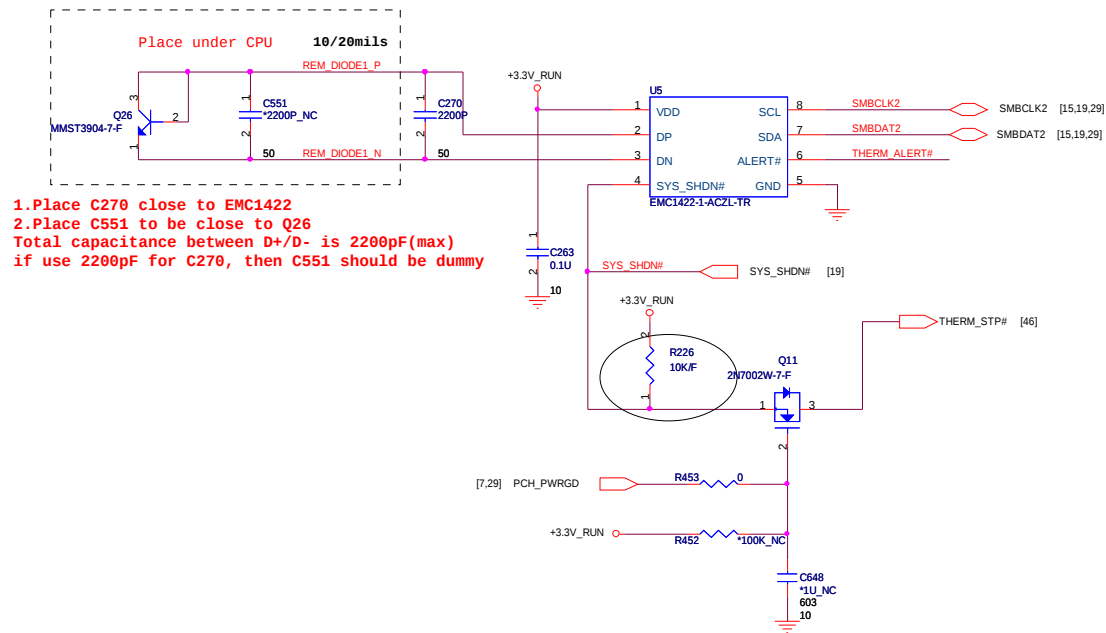
Rev 1A

FAN CONTROL

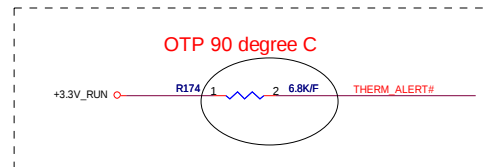
6/23 COPY FROM RM6

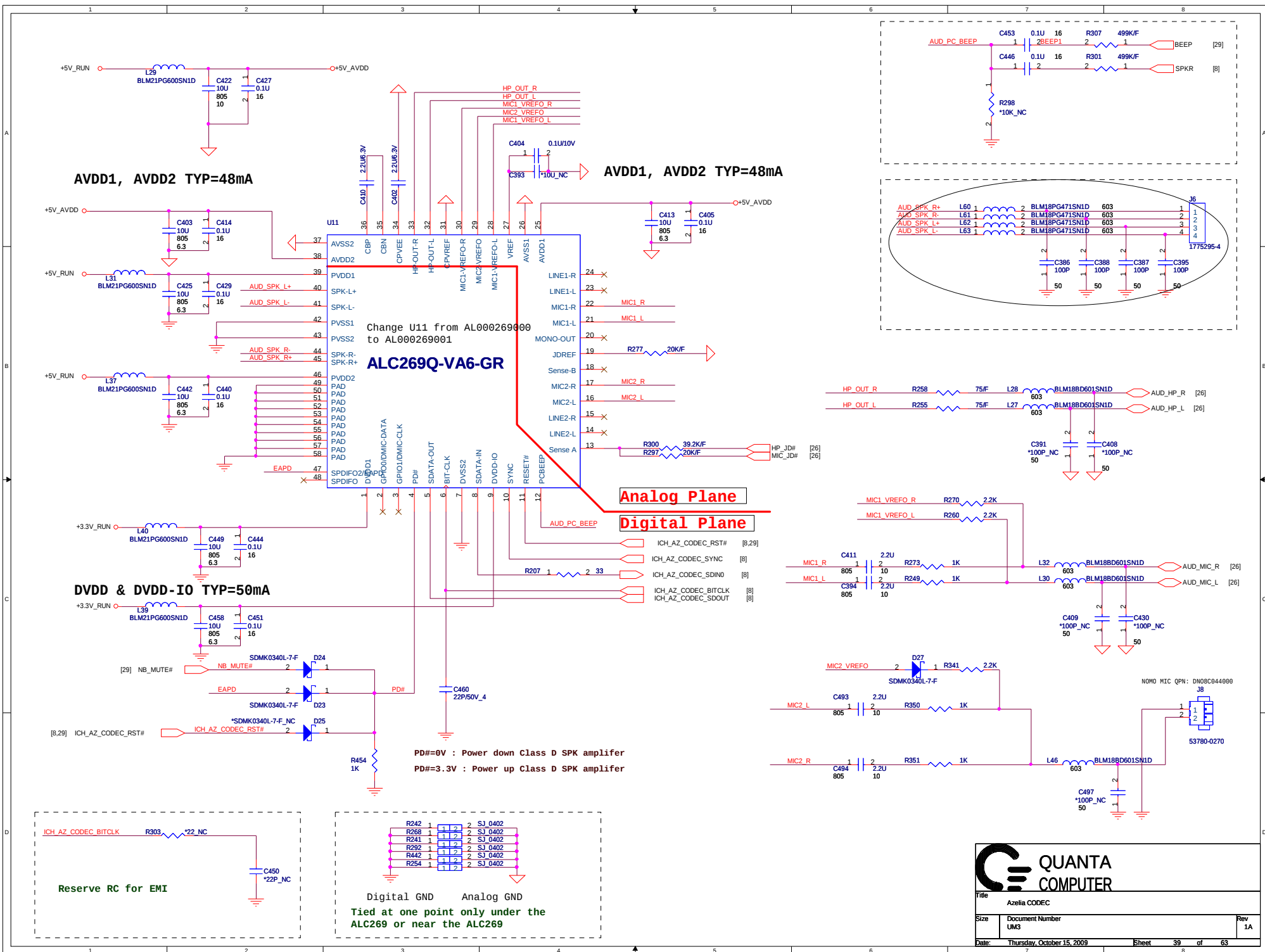


Thermal sensor

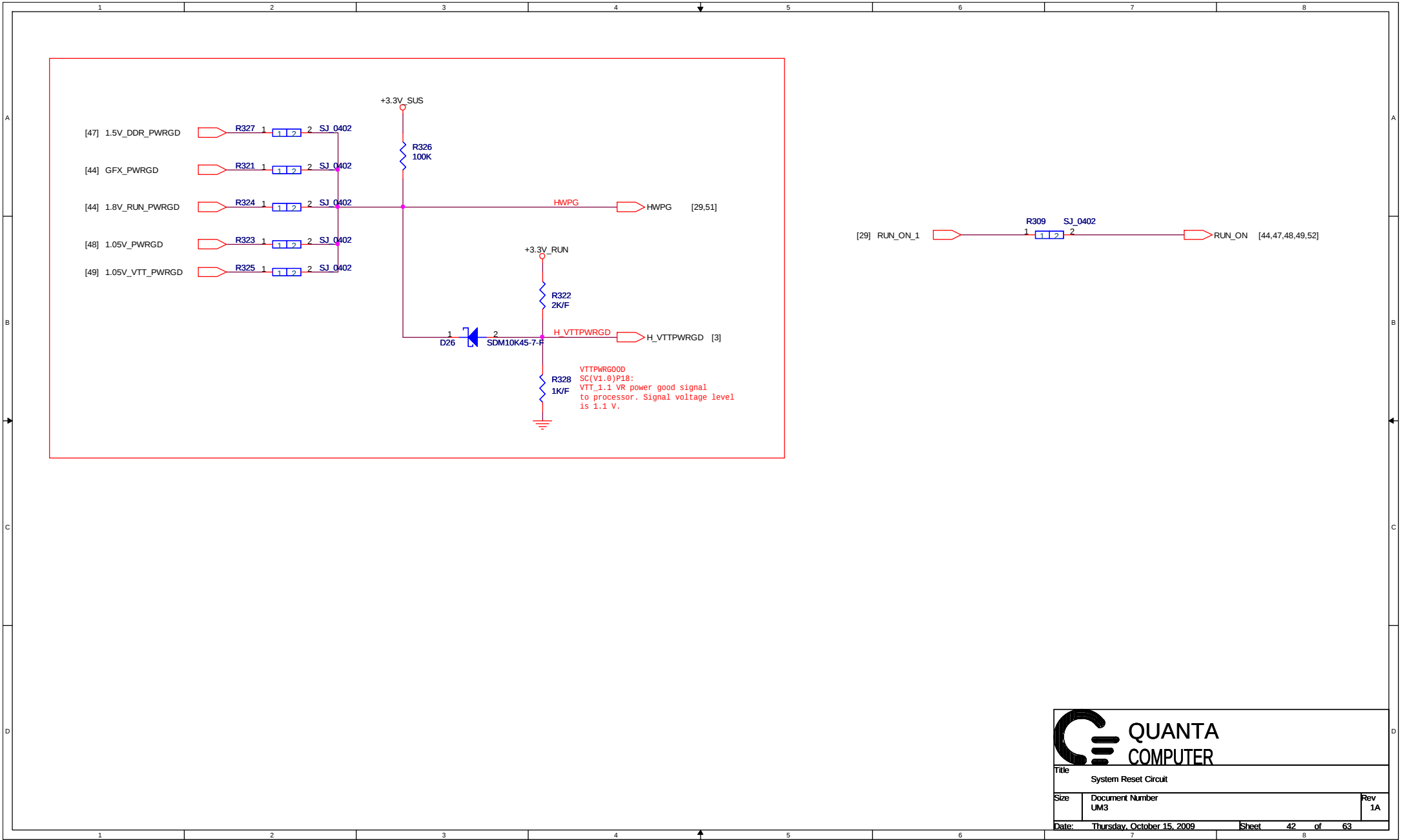


1. Place C270 close to EMC1422
 2. Place C551 to be close to Q26
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C270, then C551 should be dummy





	1	2	3	4	5	6	7	8
A								
B								
C								
D								
	1	2	3	4	5	6	7	8



Title			System Reset Circuit	
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1

2

3

4

5

A

B

C

D

A

B

C

D



QUANTA
COMPUTER

Title

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Size

Document Number
UM3

Rev

1A

Date:

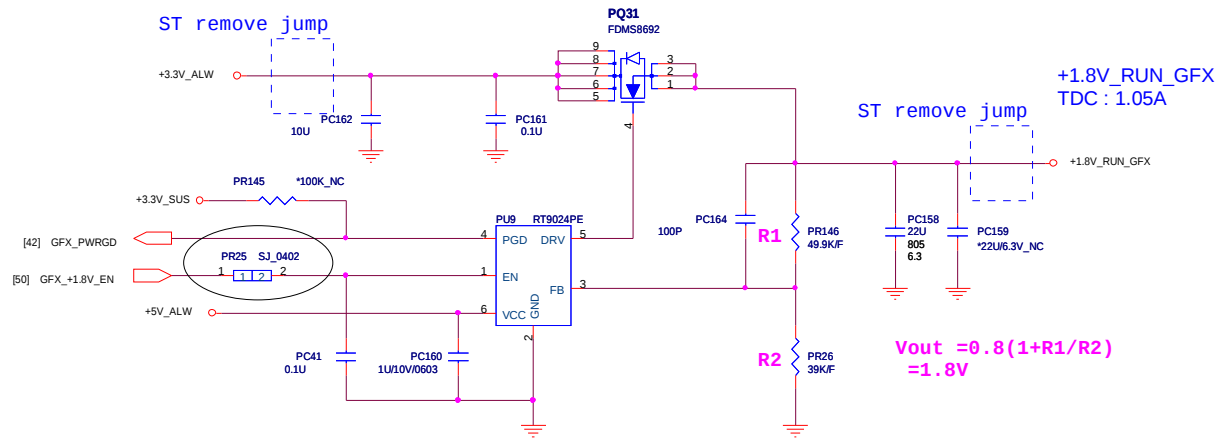
Thursday, October 15, 2009

Sheet

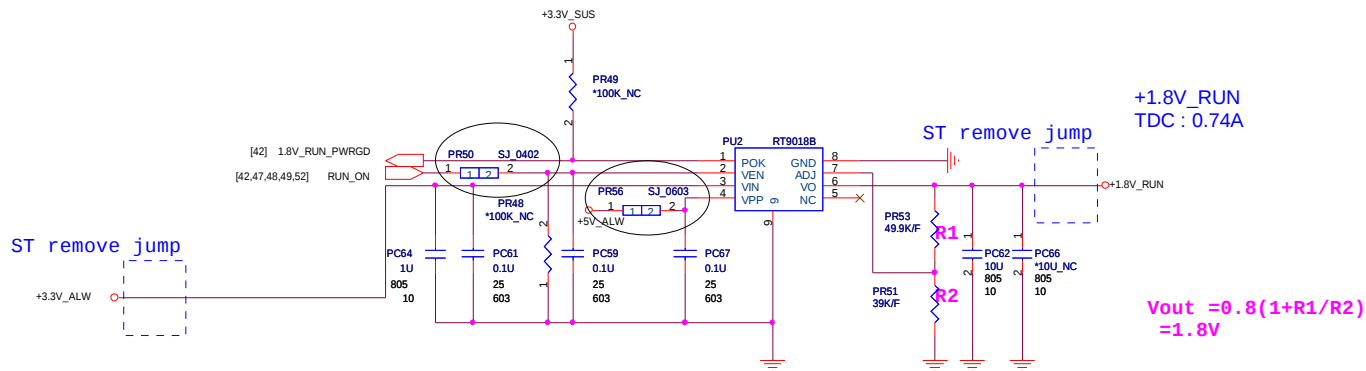
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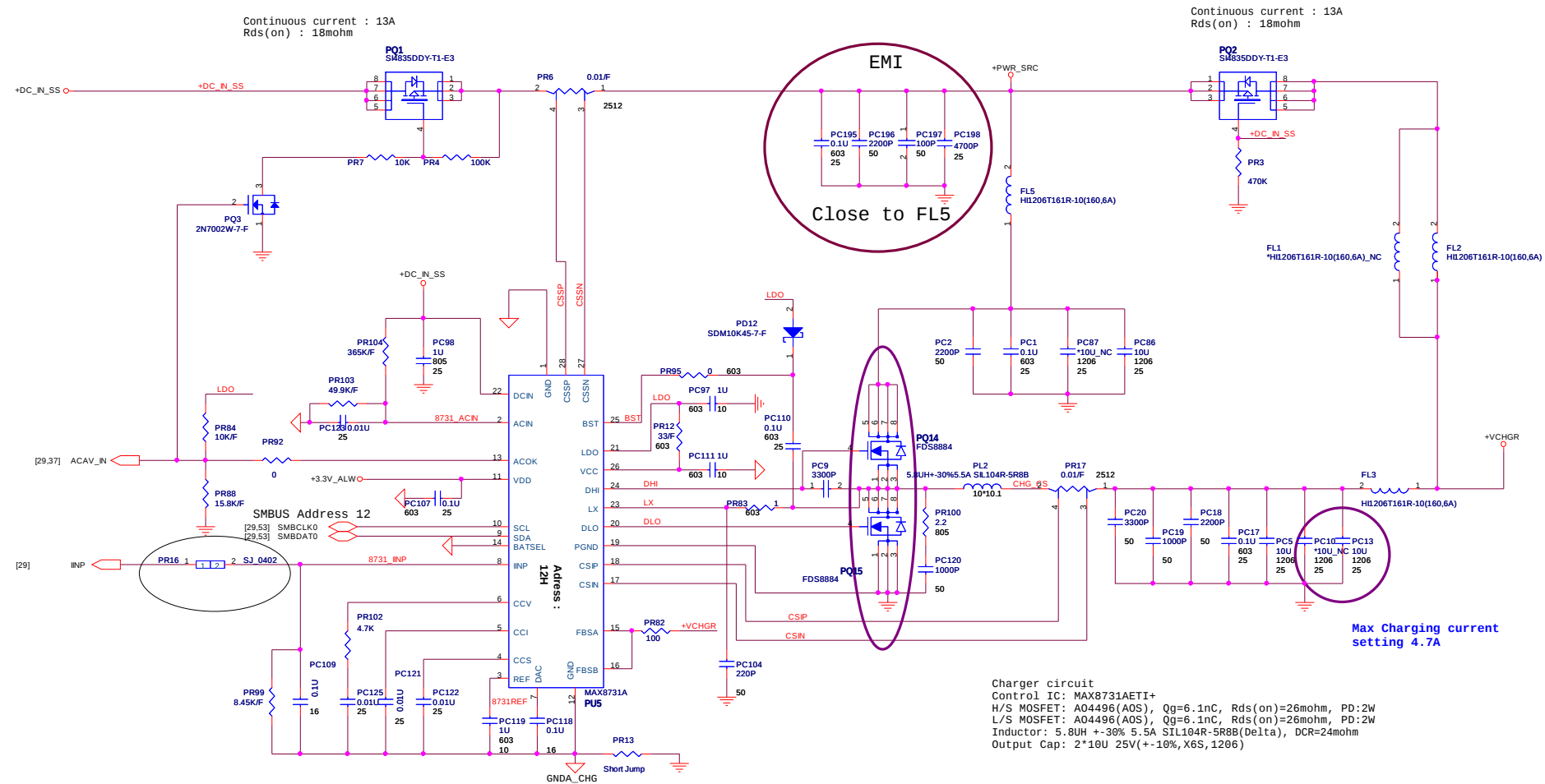
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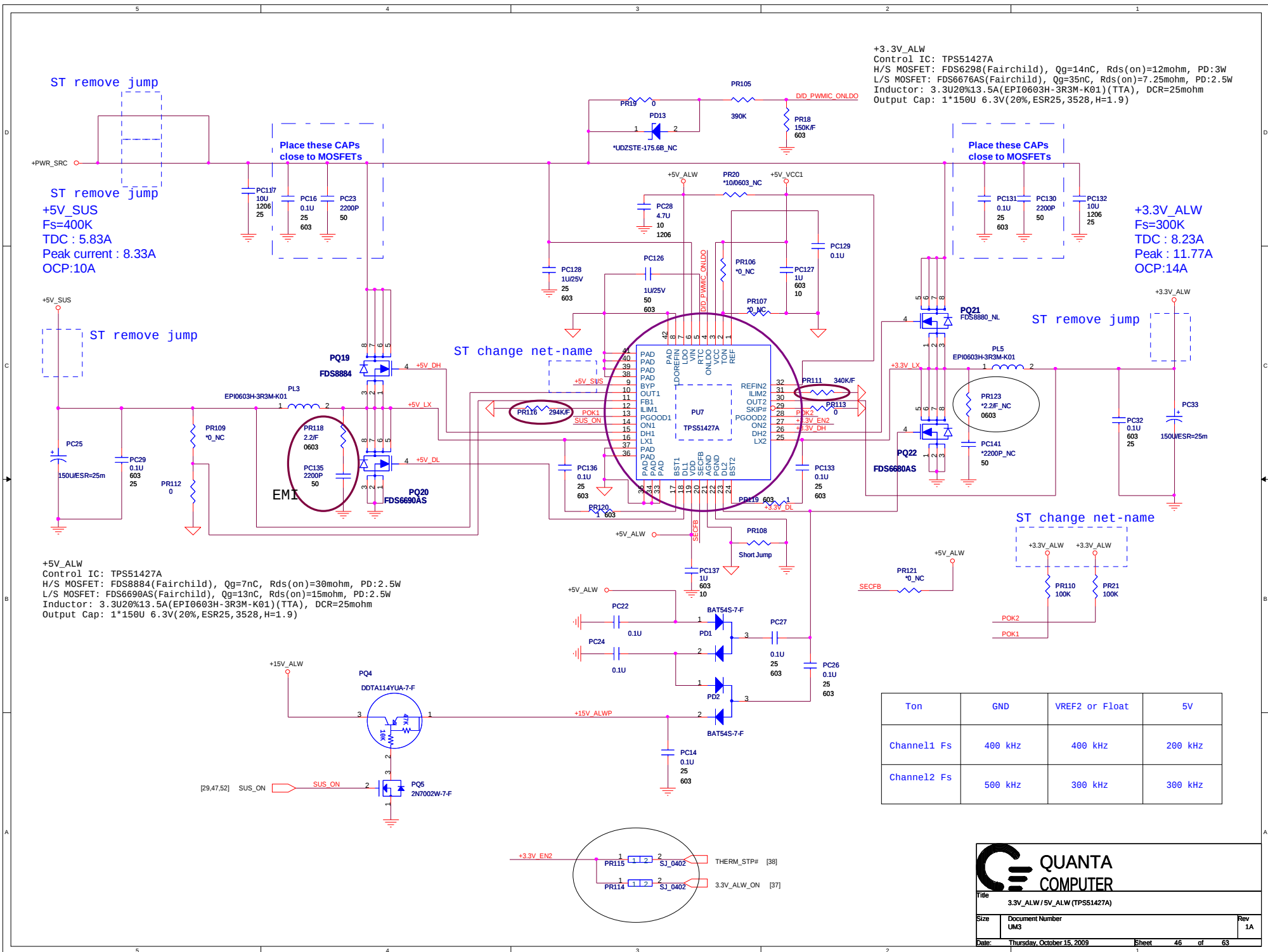
63



+1.8V_RUN_GFX for VGA 1.8V
+1.8V_RUN for CPU and PCH 1.8V







+3.3V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
L/S MOSFET: FDS6676AS(Fairchild), Qg=35nC, Rds(on)=7.25mohm, PD:2.5W
Inductor: 3.3U20%13.5A(EPI0603H-3R3M-K01)(TTA), DCR=25mohm
Output Cap: 1*150U 6.3V(20%,ESR25,3528,H=1.9)

ST remove jump

ST remove jump

+5V_SUS
Fs=400K
TDC : 5.83A
Peak current : 8.33A
OCP:10A

ST remove jump

ST change net-name

ST remove jump

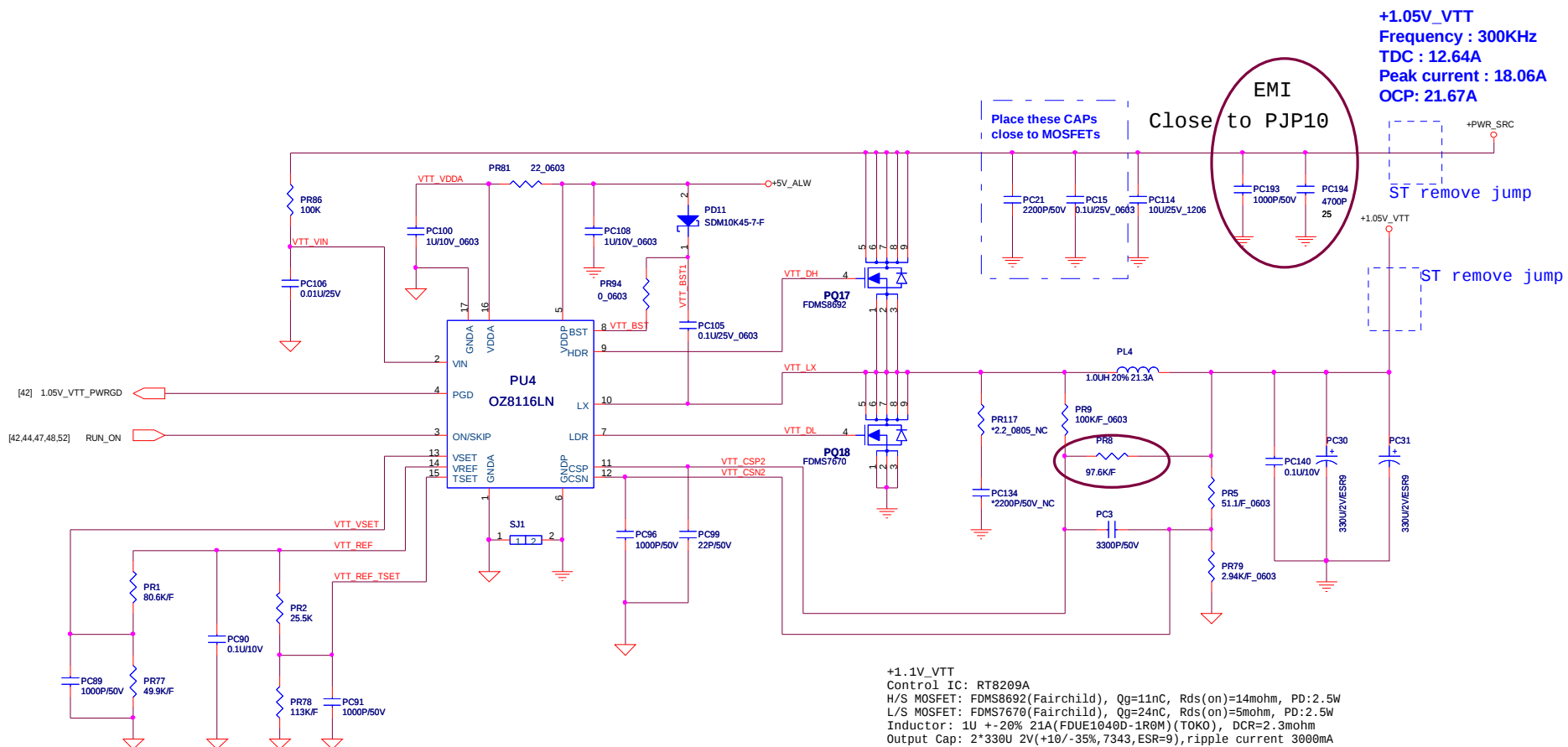
ST change net-name

+5V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS(Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W
Inductor: 3.3U20%13.5A(EPI0603H-3R3M-K01)(TTA), DCR=25mohm
Output Cap: 1*150U 6.3V(20%,ESR25,3528,H=1.9)

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz



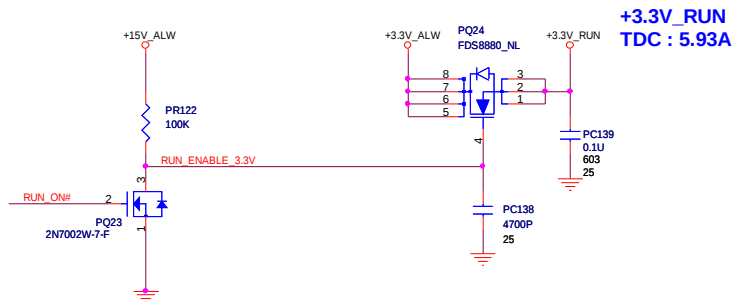
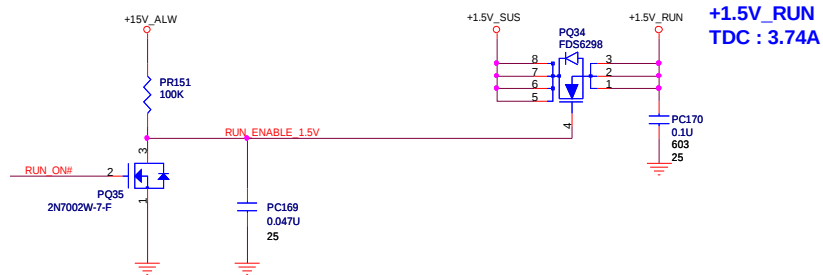
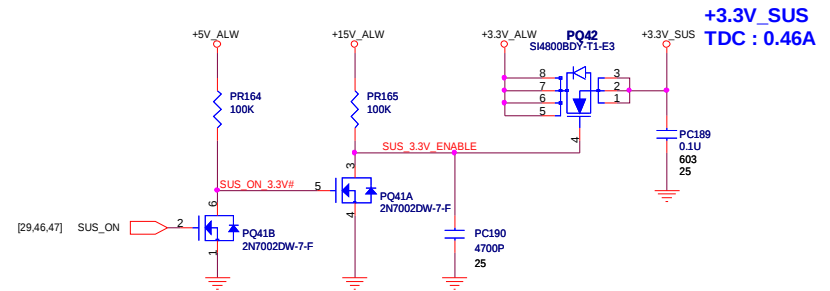
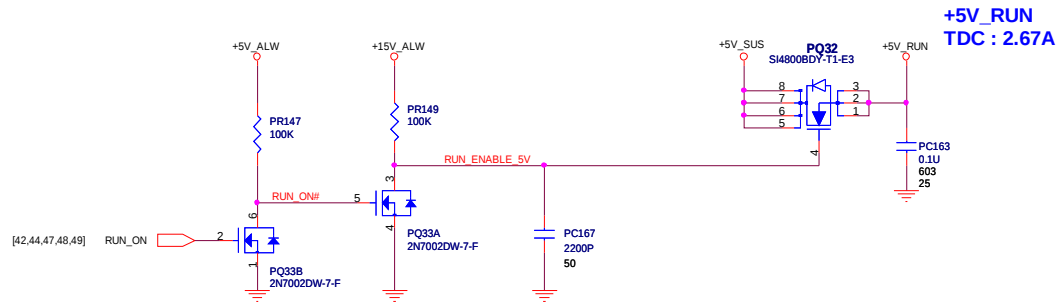
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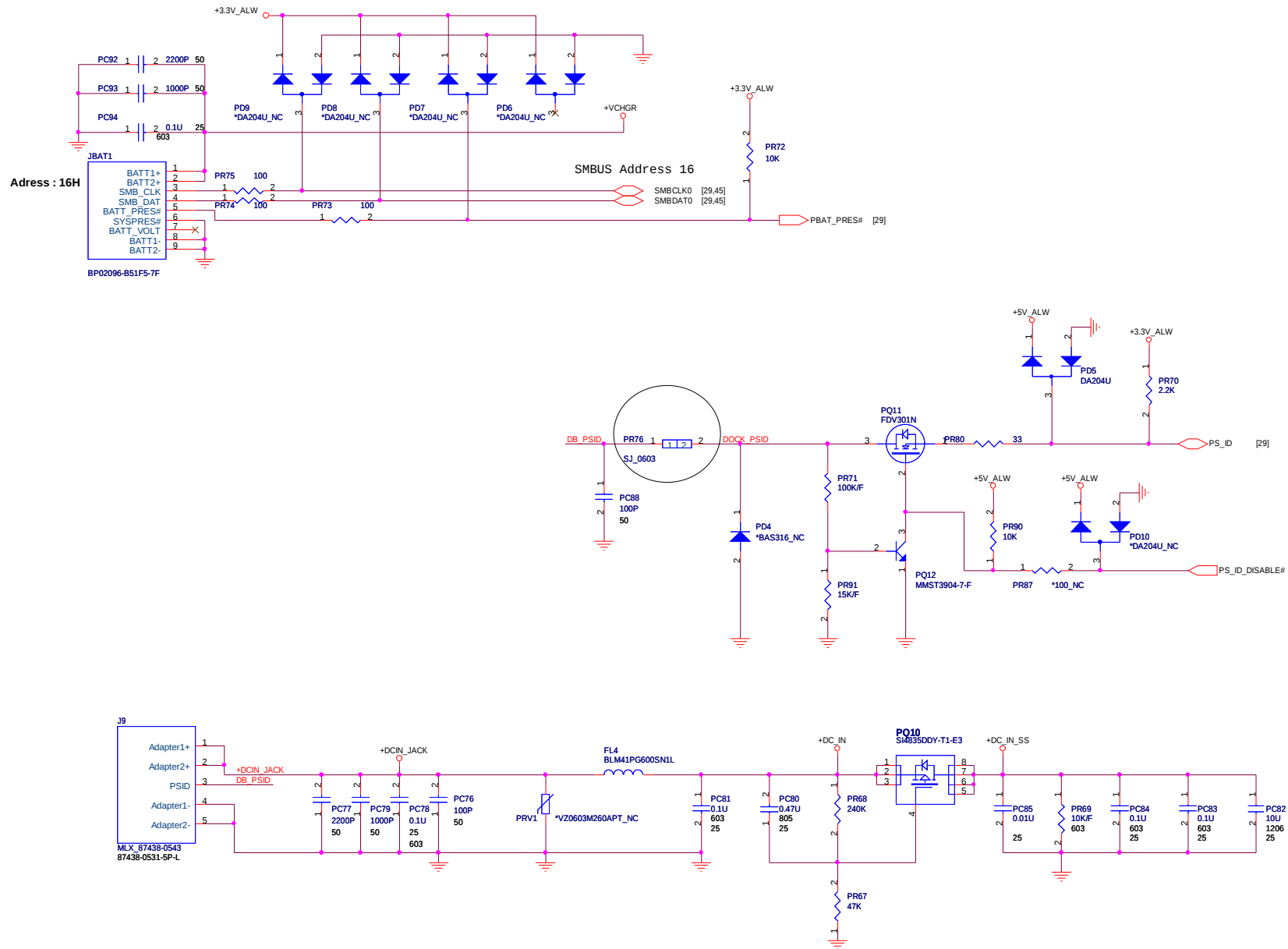


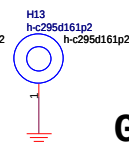
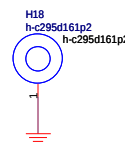
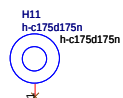
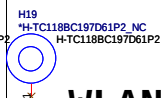
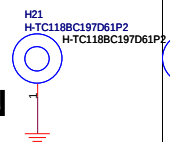
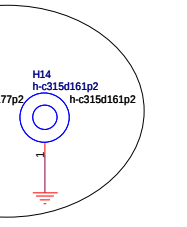
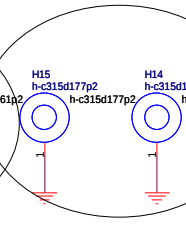
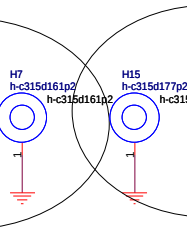
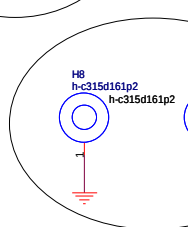
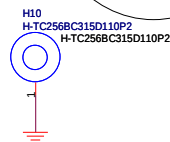
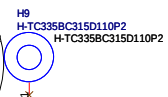
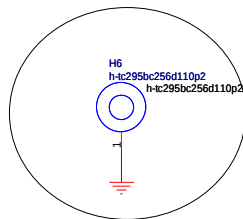
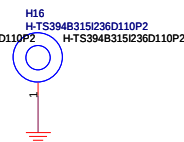
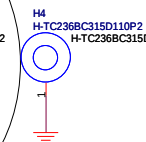
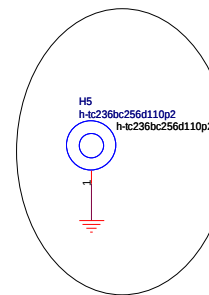
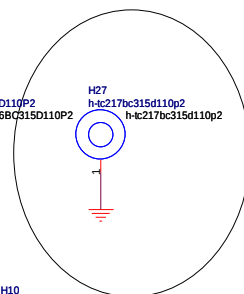
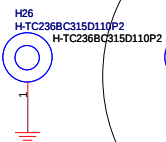
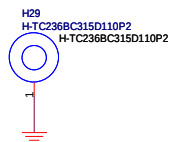
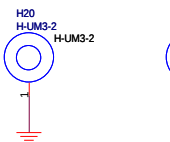
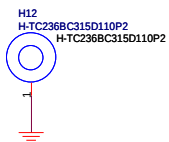
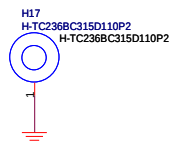
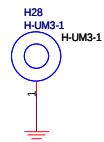
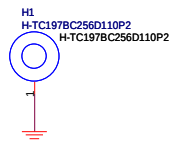


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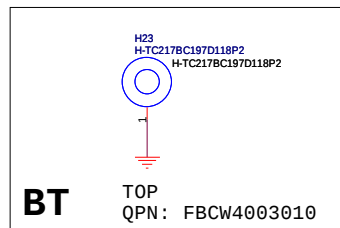
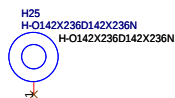


WWAN

BOT
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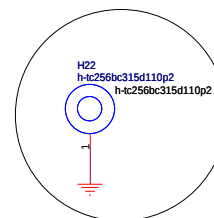
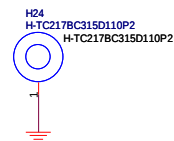
WLAN

GPU



BT

TOP
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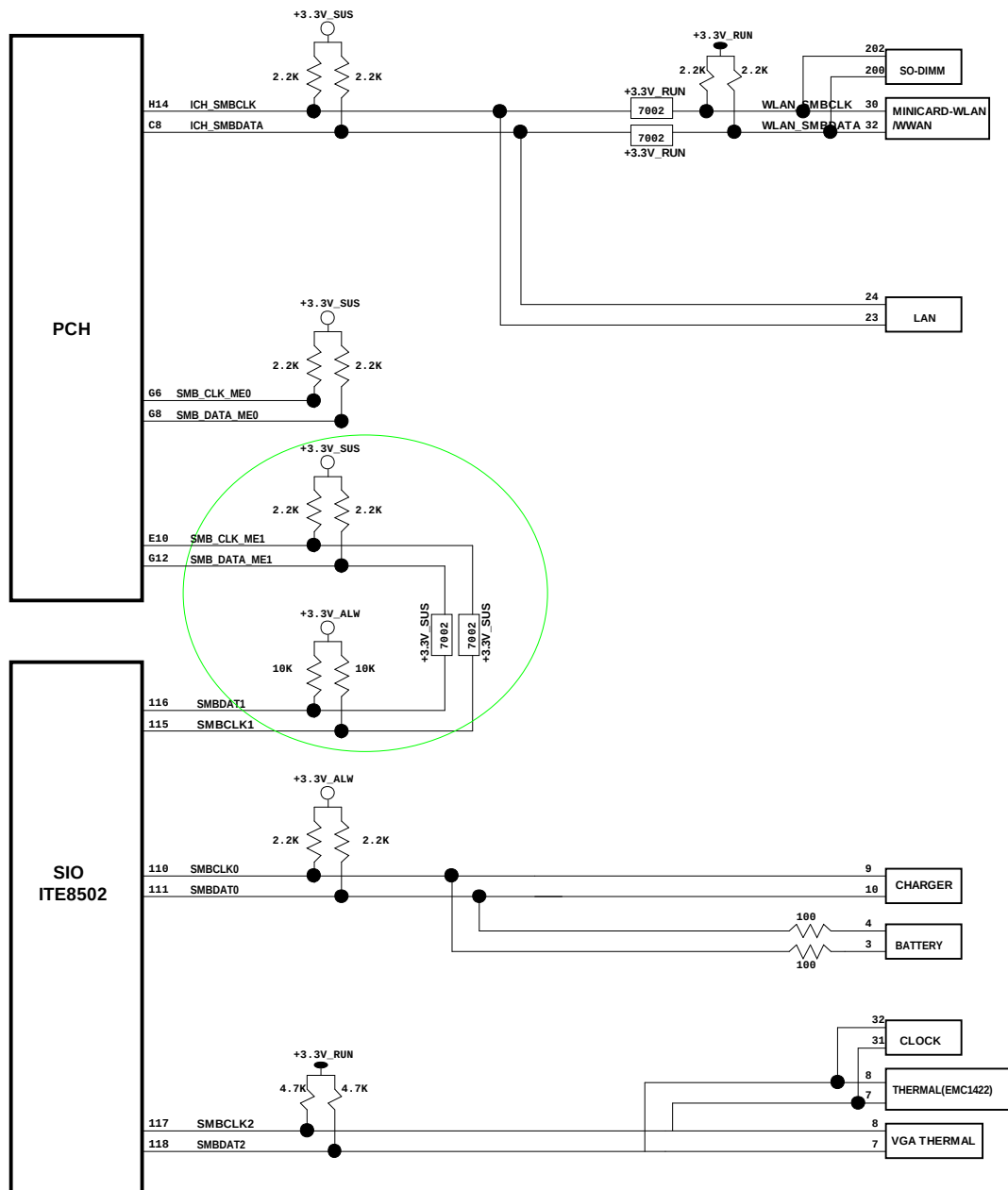
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Title: SCREW PAD			
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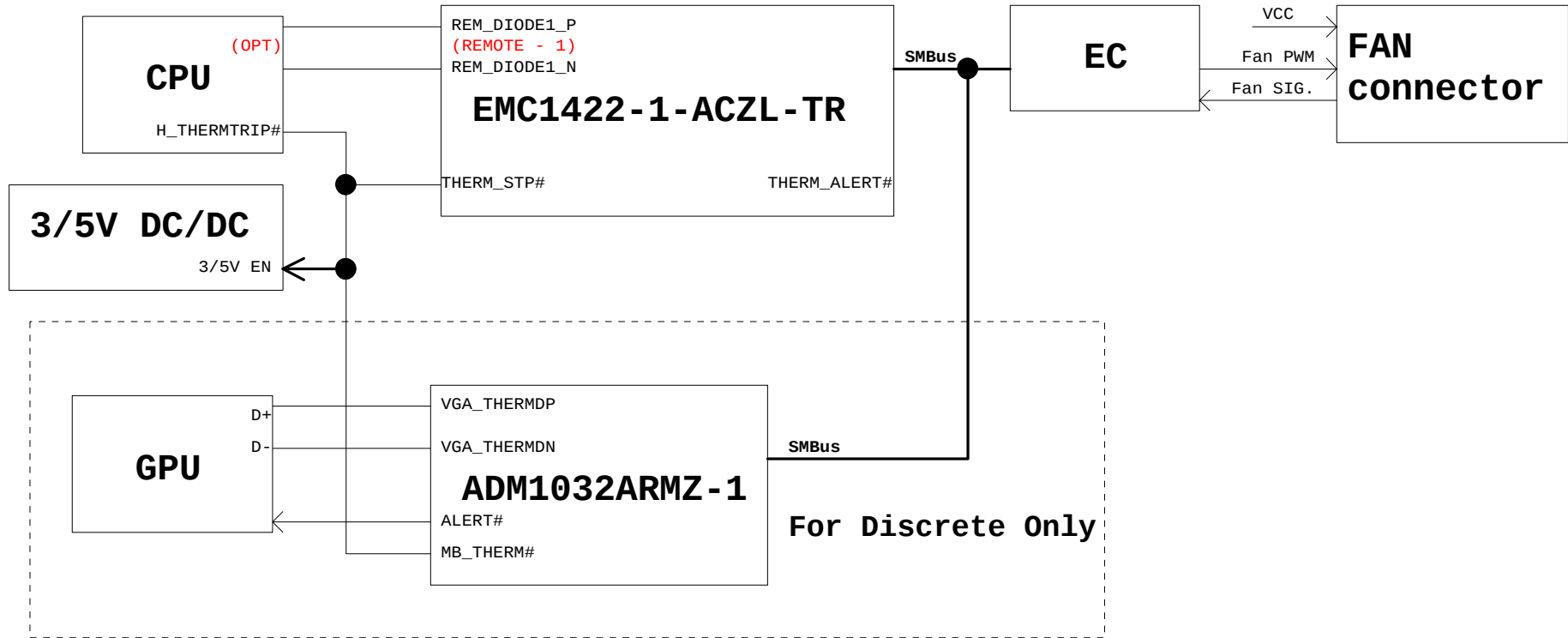
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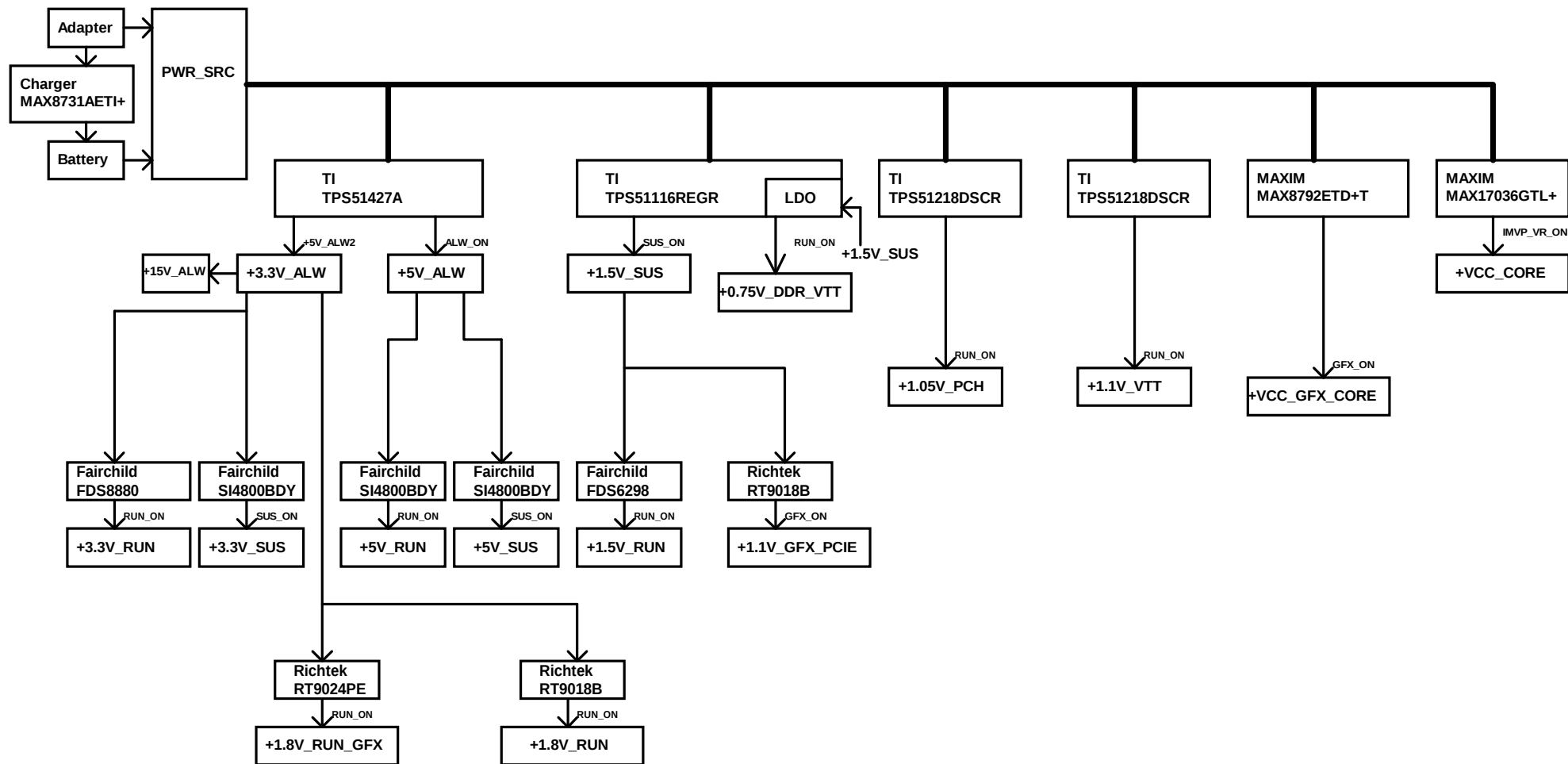


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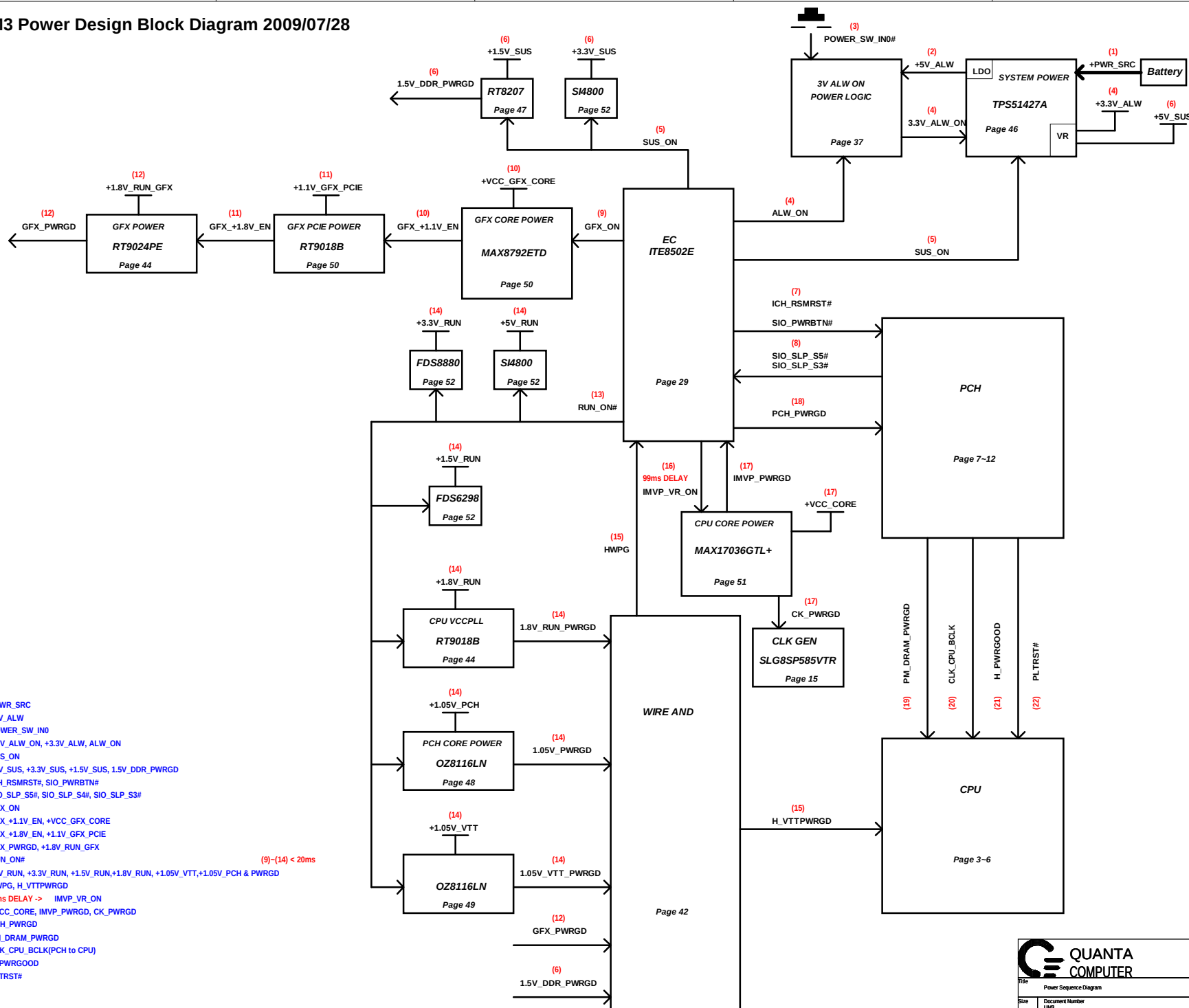
Title EMI CAP		
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