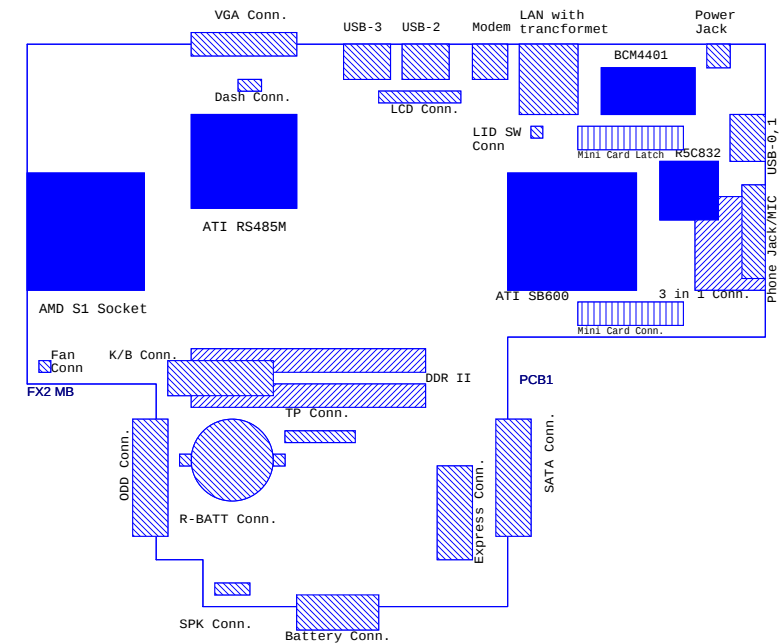
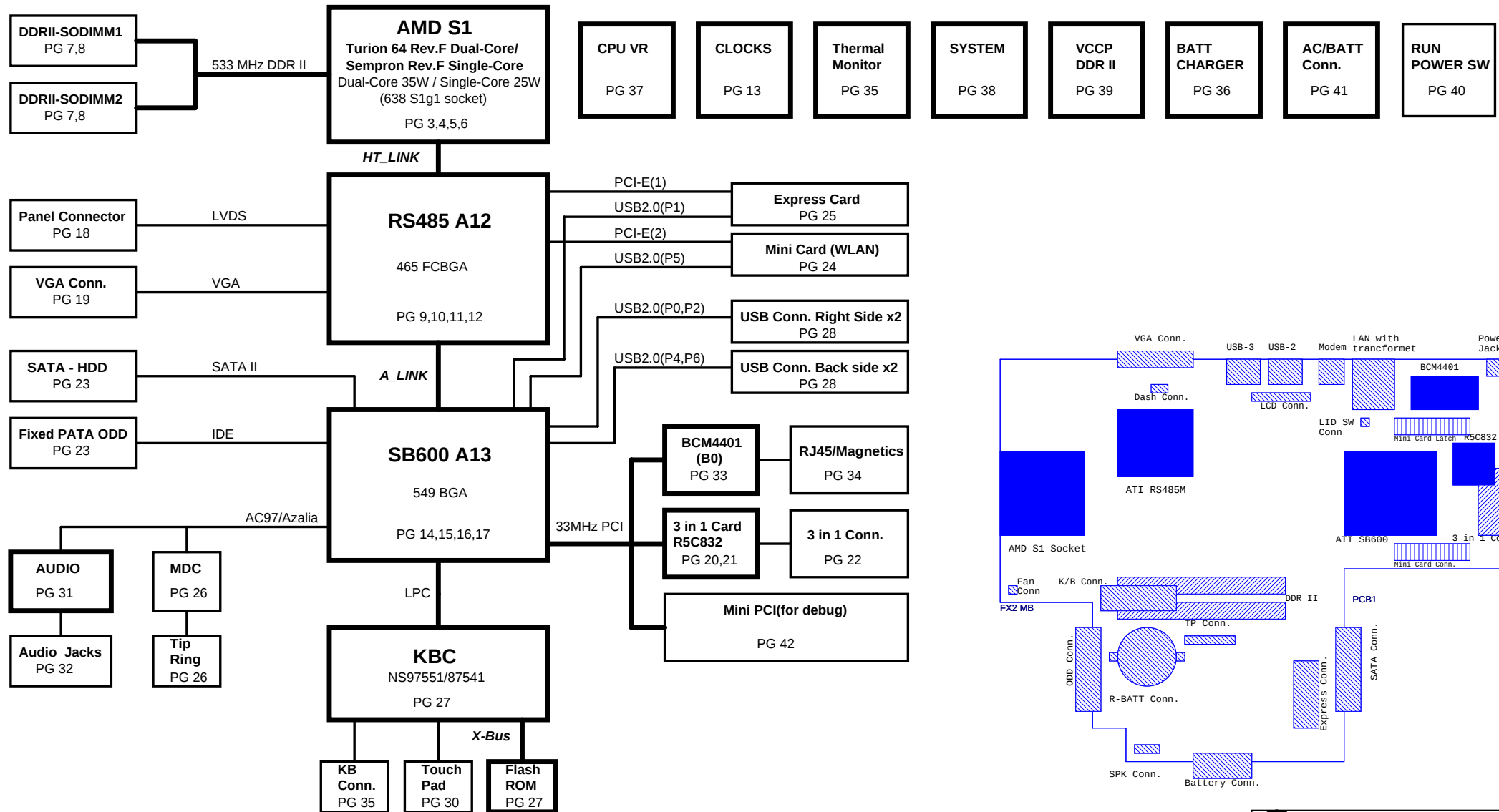


Kirin (FX2 with NS) VER : 1A



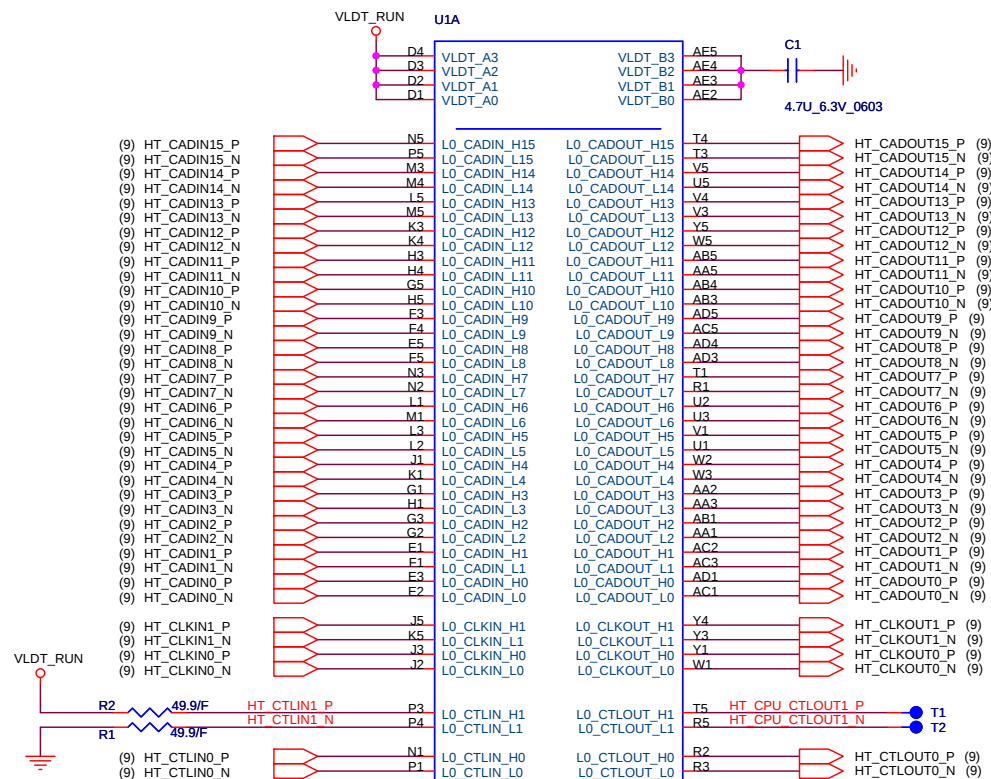
INDEX

Page	Description
1	BLOCK DIAGRAM
2	FRONT PAGE
3	ATHLON64 HT I/F
4	ATHLON64 DDRII MEMORY
5	ATHLON64 CTRL & DEBUG
6	ATHLON64 PWR & GND
7	DDRII SODIMMX2
8	DDRII TERMINATION
9	RS485-HT LINK0 I/F
10	RS485-PCIE LINK I/F
11	RS485-LVDS
12	RS485-POWER
13	CLOCK GENERATOR
14	SB600M-PCIE/PCI/LPC
15	SB600M ACPI/USB/AC97
16	SB600M HDD/POWER
17	SB600M STRAPS
18	LCD CONN
19	CRT
20	5C832/PCI
21	CARD READER
22	CARD READER CONN
23	SATA HDD & PATA ODD
24	MINI Card
25	MINI Card
26	MDC CONN
27	PC97551 & FLASH
28	USB
29	EMI & Screw hole
30	SWITCH & TP & LED
31	Azelia CODEC
32	AUDIO CONN
33	LAN(BCM4401)
34	LAN JACK
35	KB & THERMAL & FAN
36	CHARGER (MAX8731)
37	VHCORE (MAX8774)
38	SYSTEM (MAX8734)
39	VCCP & DDR2 (MAX8743)
40	RUN POWER SW
41	DCIN,Batt
42	MINI PCI(for debug)
43	Power On Sequence
44	Power On Diagram
45	SMBUS BLOCK

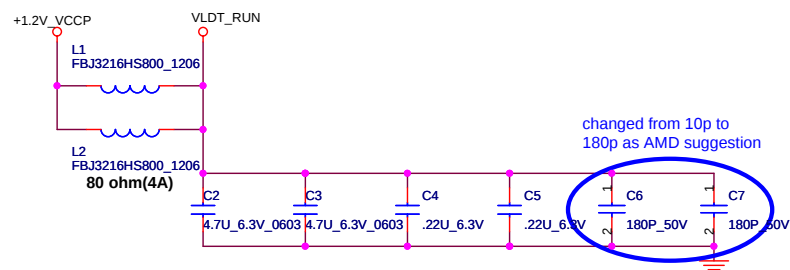


PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1
Processor Socket



LAYOUT: Place bypass cap on topside of board



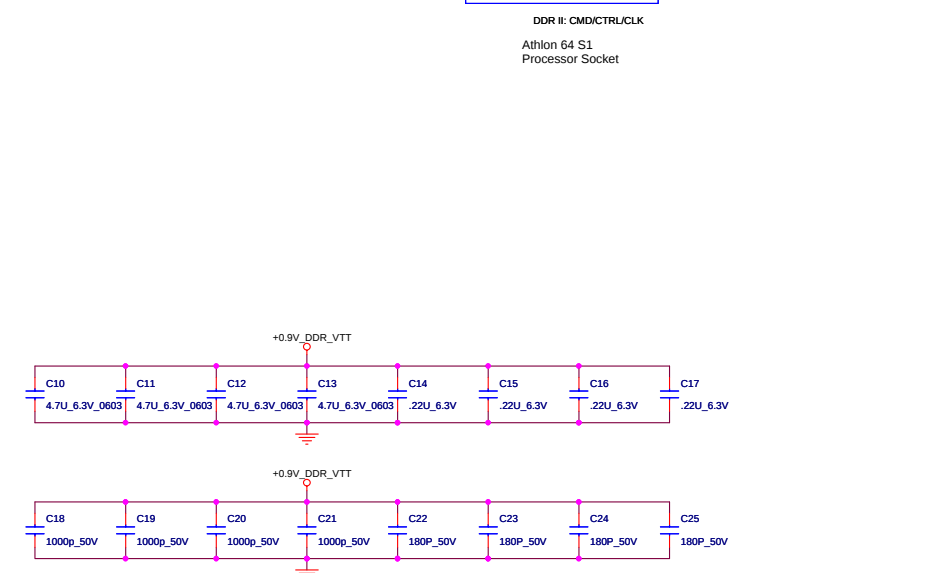
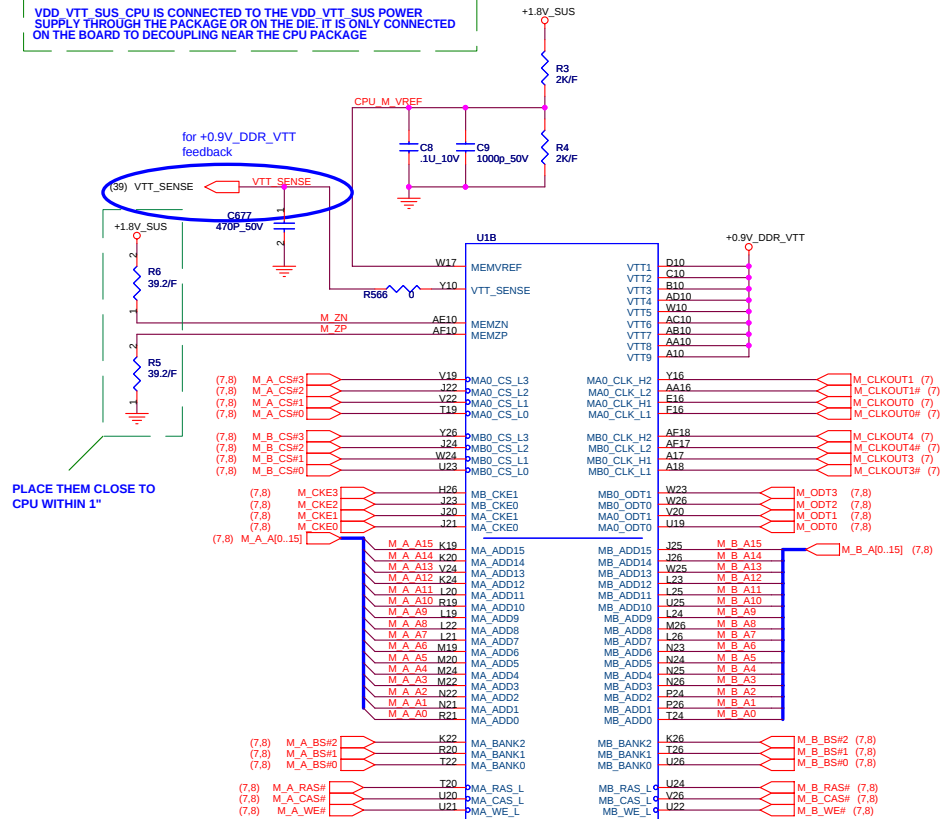
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



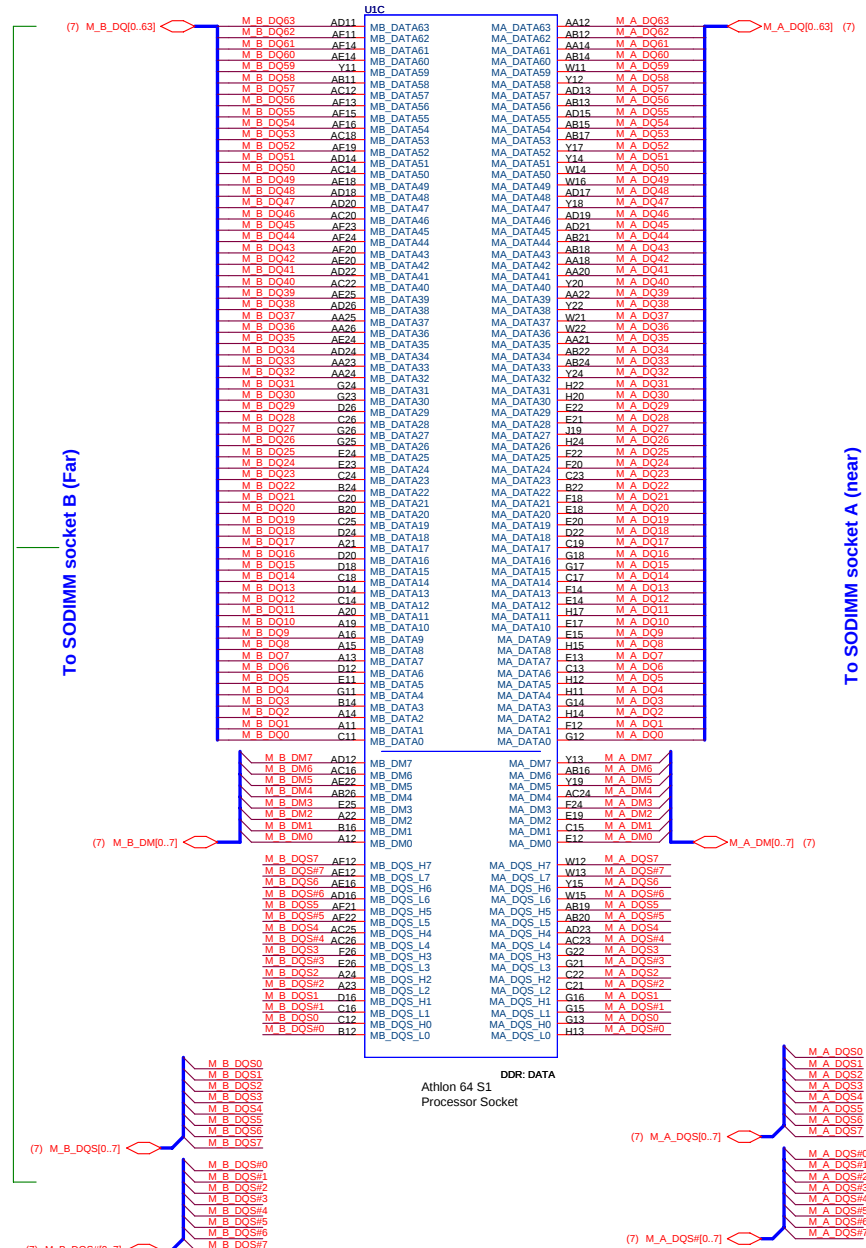
QUANTA
COMPUTER

Title			
ATHLON64 HT I/F			
Size	Document Number		Rev
	FX2		1A
Date:	Friday, May 05, 2006	Sheet	3 of 47

VDD, VTT, SUS, CPU, IS CONNECTED TO THE VDD, VTT, SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



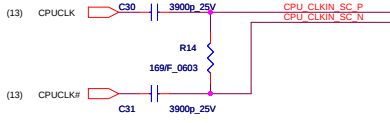
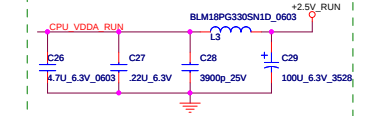
Processor DDR2 Memory Interface



ATHLON Control and Debug

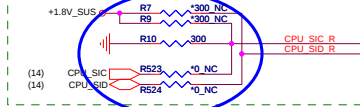
LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN



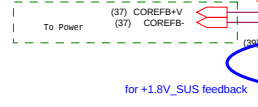
R14 close U1 within 600 mil, C30 & C31 close U1 within 1250 mil

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pull-down to VSS.

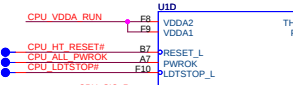


for CPU rev.F; if for rev.G, populate R7,R9,R523,R524 and depopulate R10

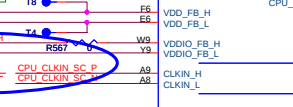
place them to CPU within 1"



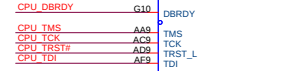
for +1.8V_SUS feedback



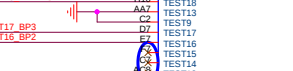
place them to CPU within 1"



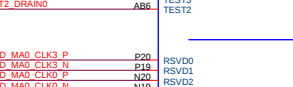
for +1.8V_SUS feedback



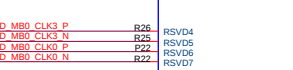
change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down



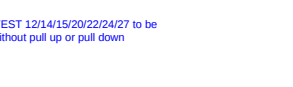
add port to Page 35 U36 Thermal IC



change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down



change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down



delete ED5 H_THERMTRIP# circuit



delete ED5 thermal sensor



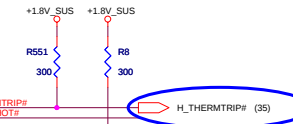
delete ED5 thermal sensor



delete ED5 thermal sensor

delete ED5 thermal sensor

delete ED5 thermal sensor



change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down



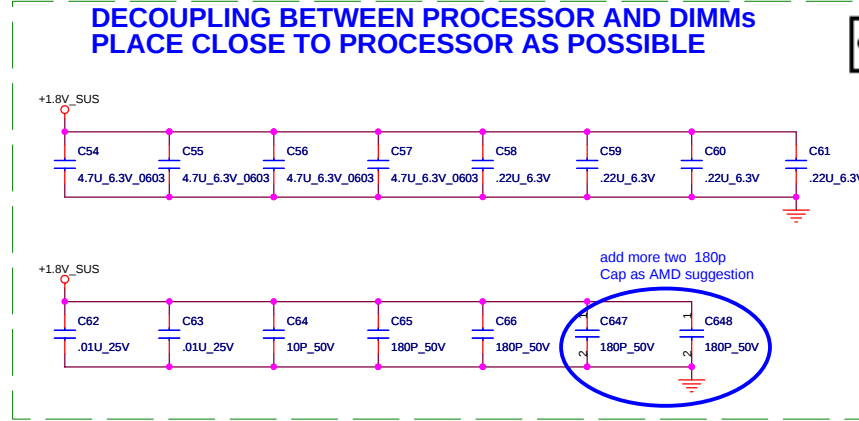
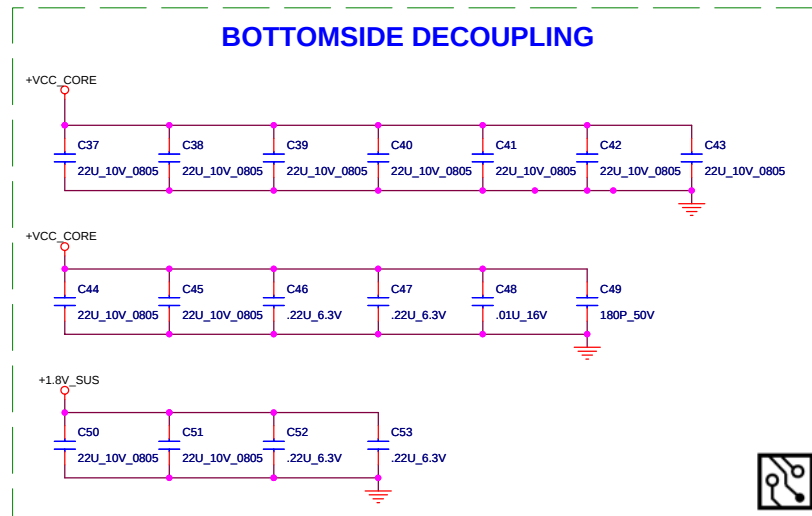
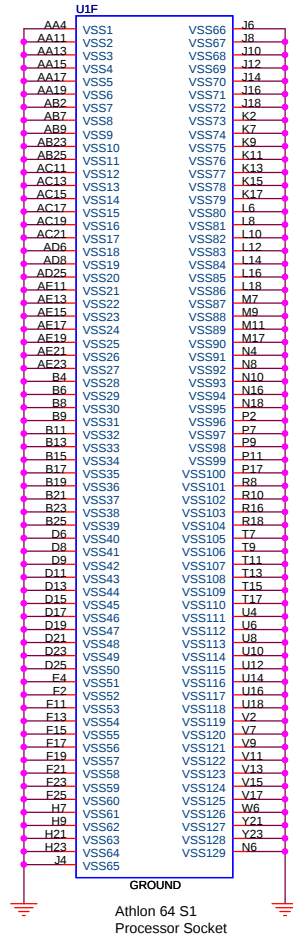
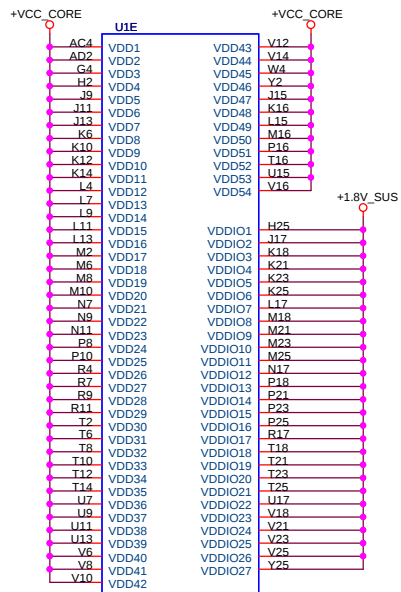
ATHLON64 CTRL & DEBUG

Size Document Number FX2

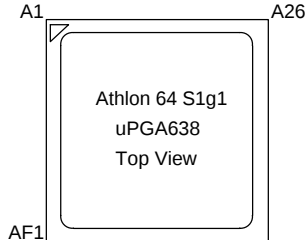
Date: Friday, May 05, 2006

Sheet 5 of 47

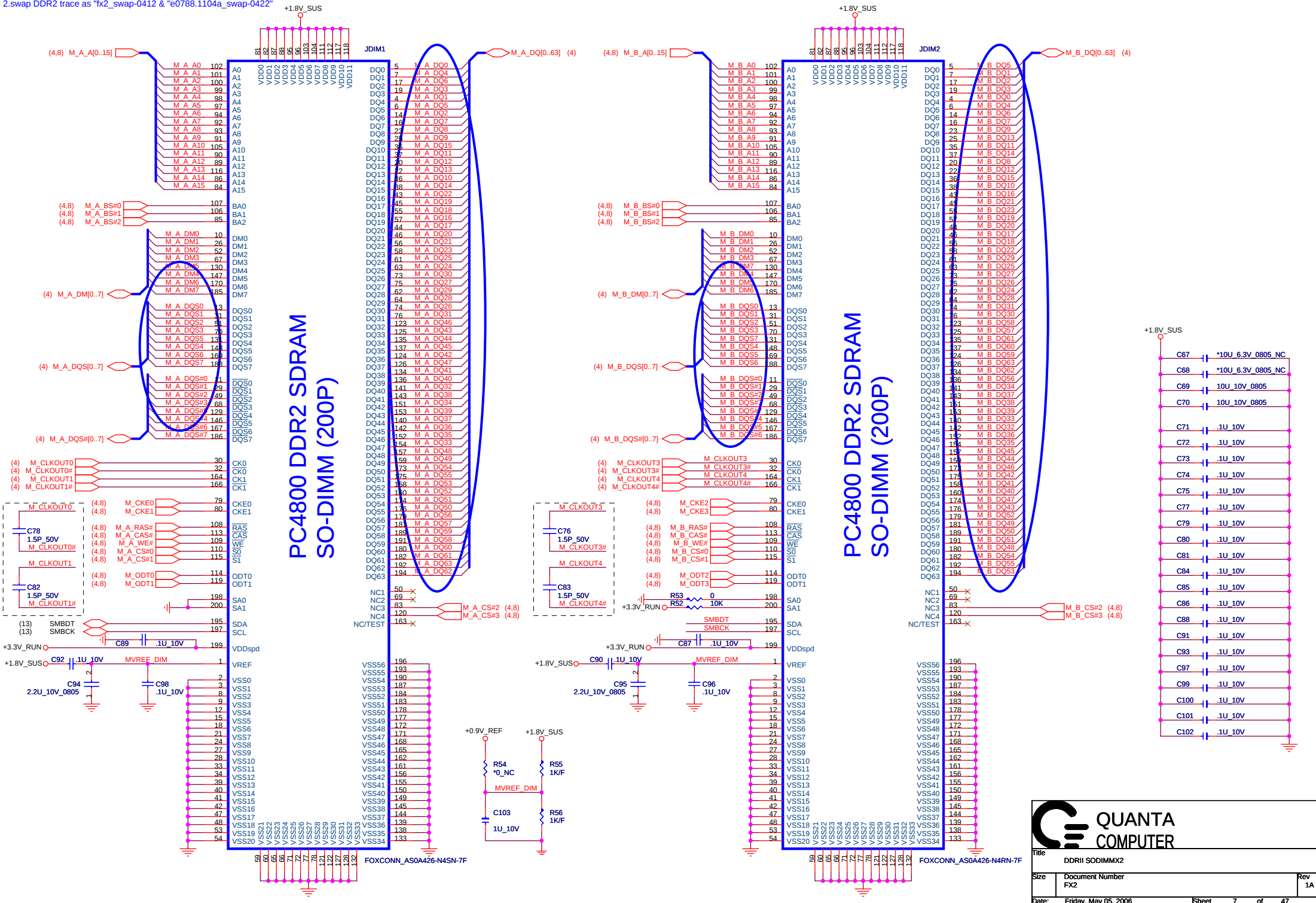
Rev 1A



PROCESSOR POWER AND GROUND



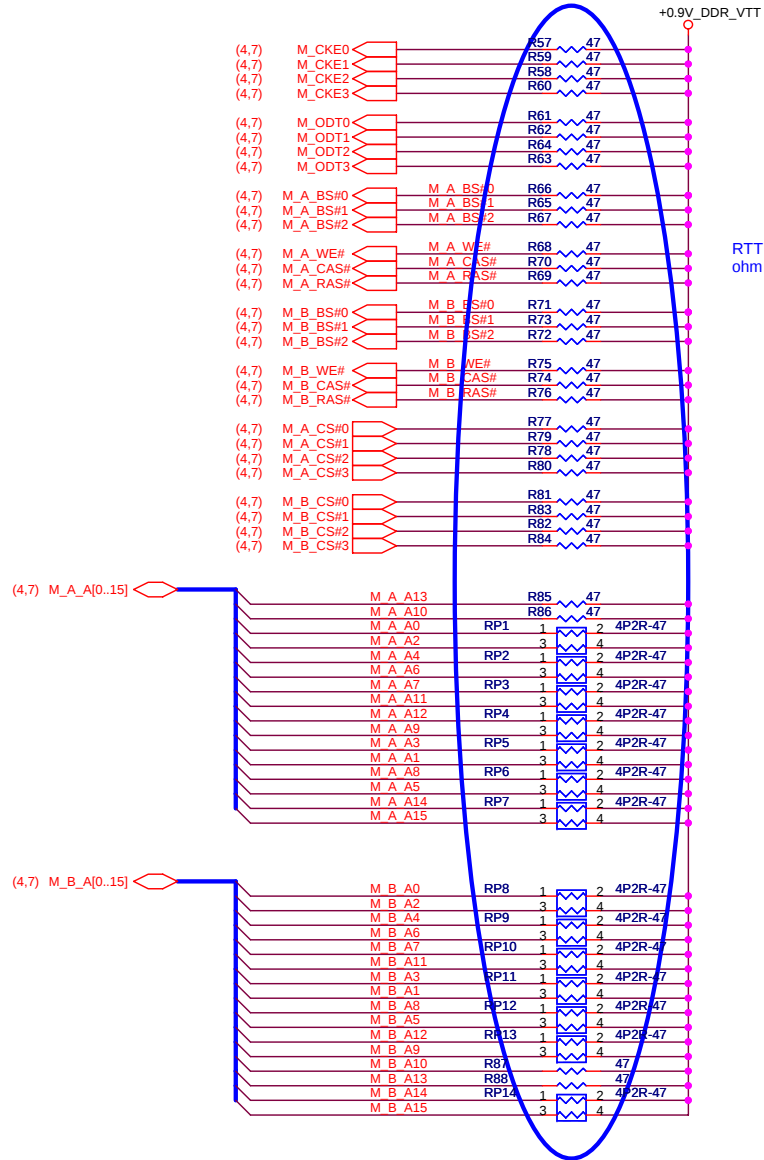
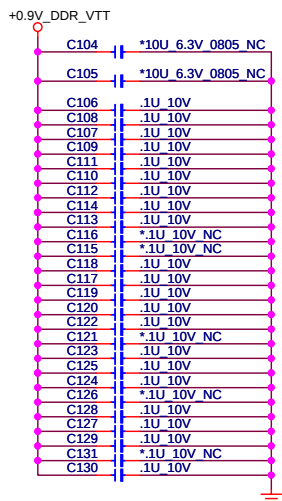
1.Change DDR2 socket(P/N, Description, footprint, part reference, value)
2.swap DDR2 trace as "fx2_swap-0412 & "e0788.1104a_swap-0422"

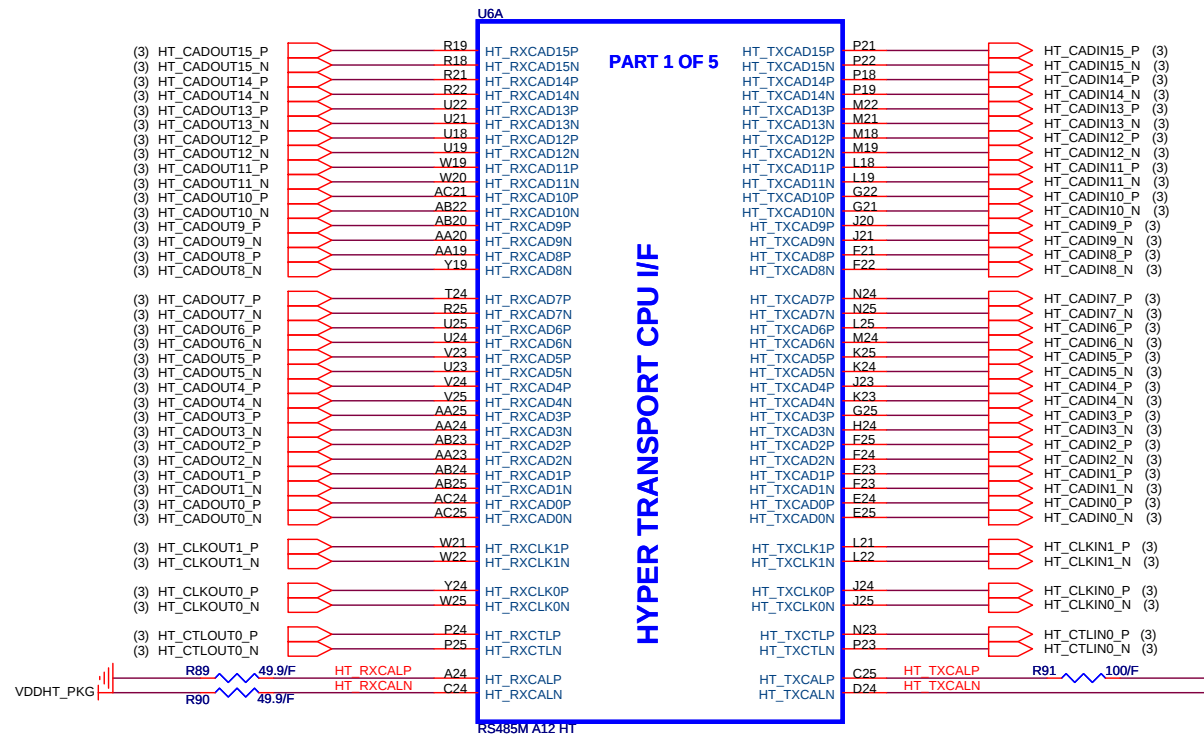


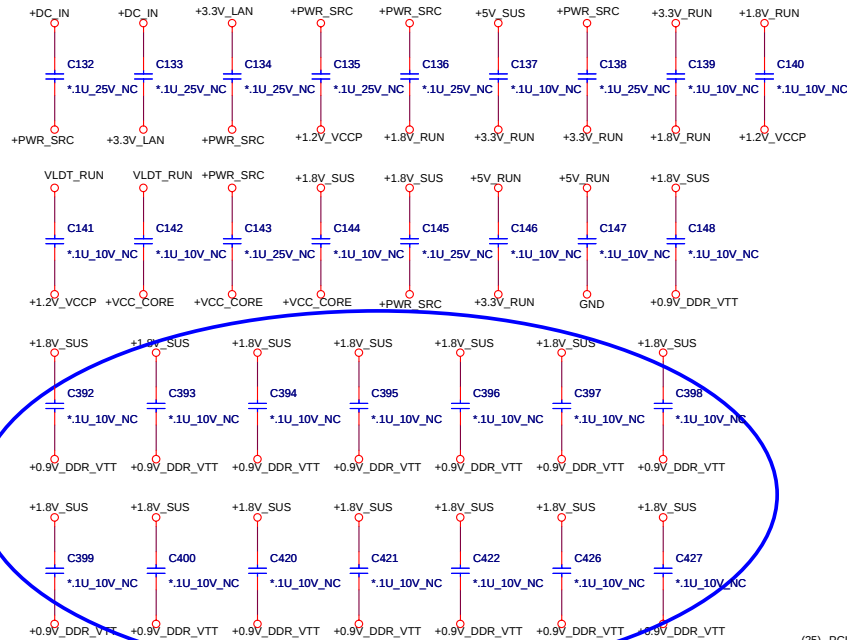


QUANTA
COMPUTER

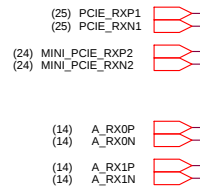
Title		
DDR2 SO-DIMM X2		
Size	Document Number	Rev
FX2		1A
Date		Sheet
Friday, May 05, 2006		7 of 47



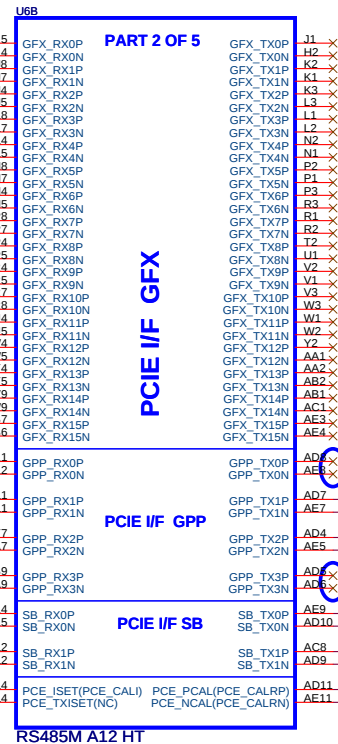




delete PCIE signal , original LAN & Mini Card of ED5



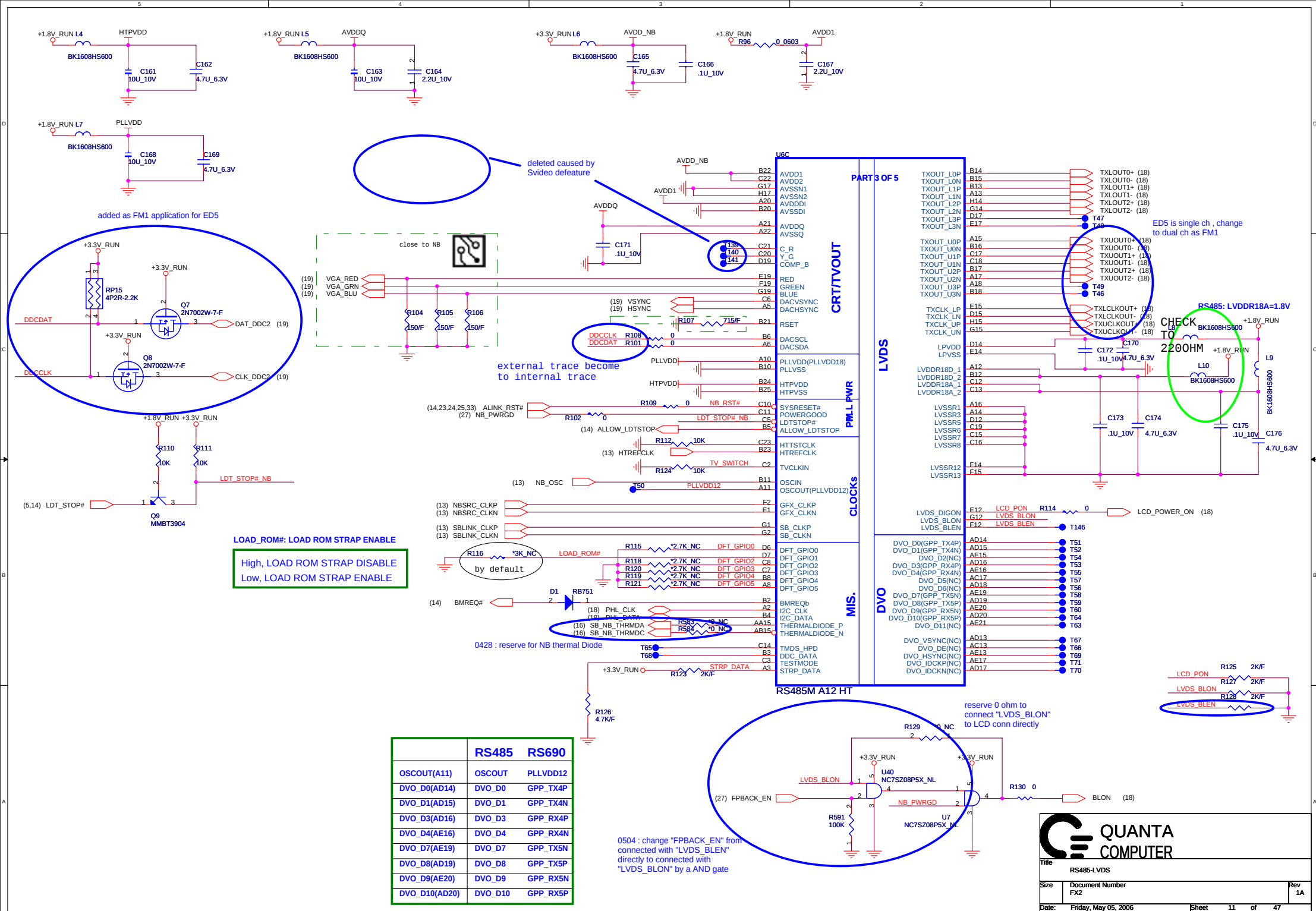
R93: 10KOhm FOR RS485
1.47KOhm FOR RS690
R92: 8.25KOhm FOR RS485
DNI FOR RS690

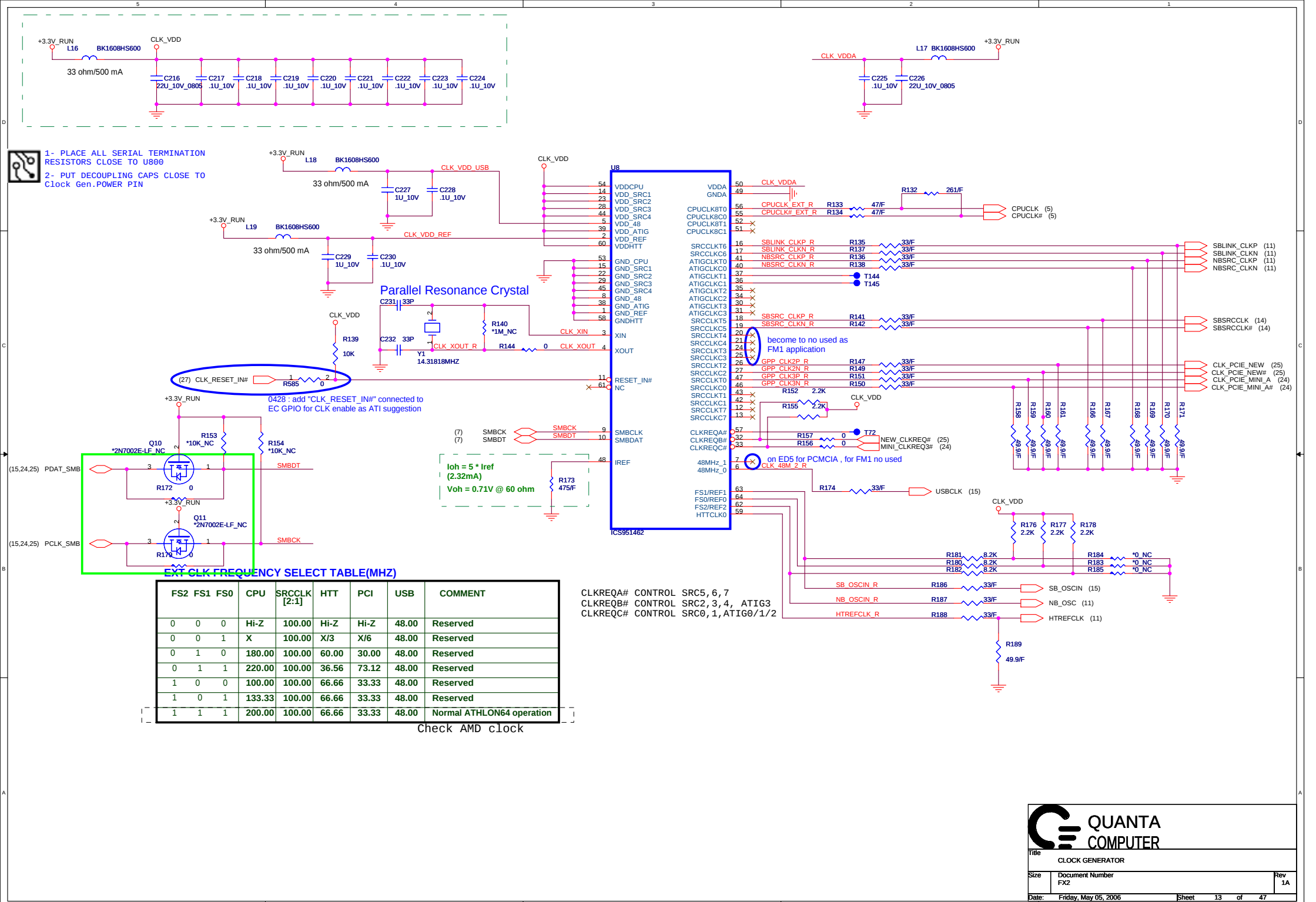


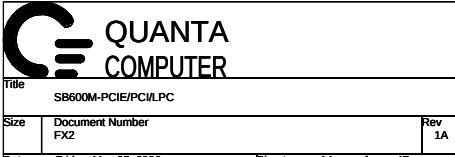
R95: 150 Ohm FOR RS485
562 Ohm FOR RS690
R94: Ward update to 100 Ohm FOR RS485
2KOhm FOR RS690



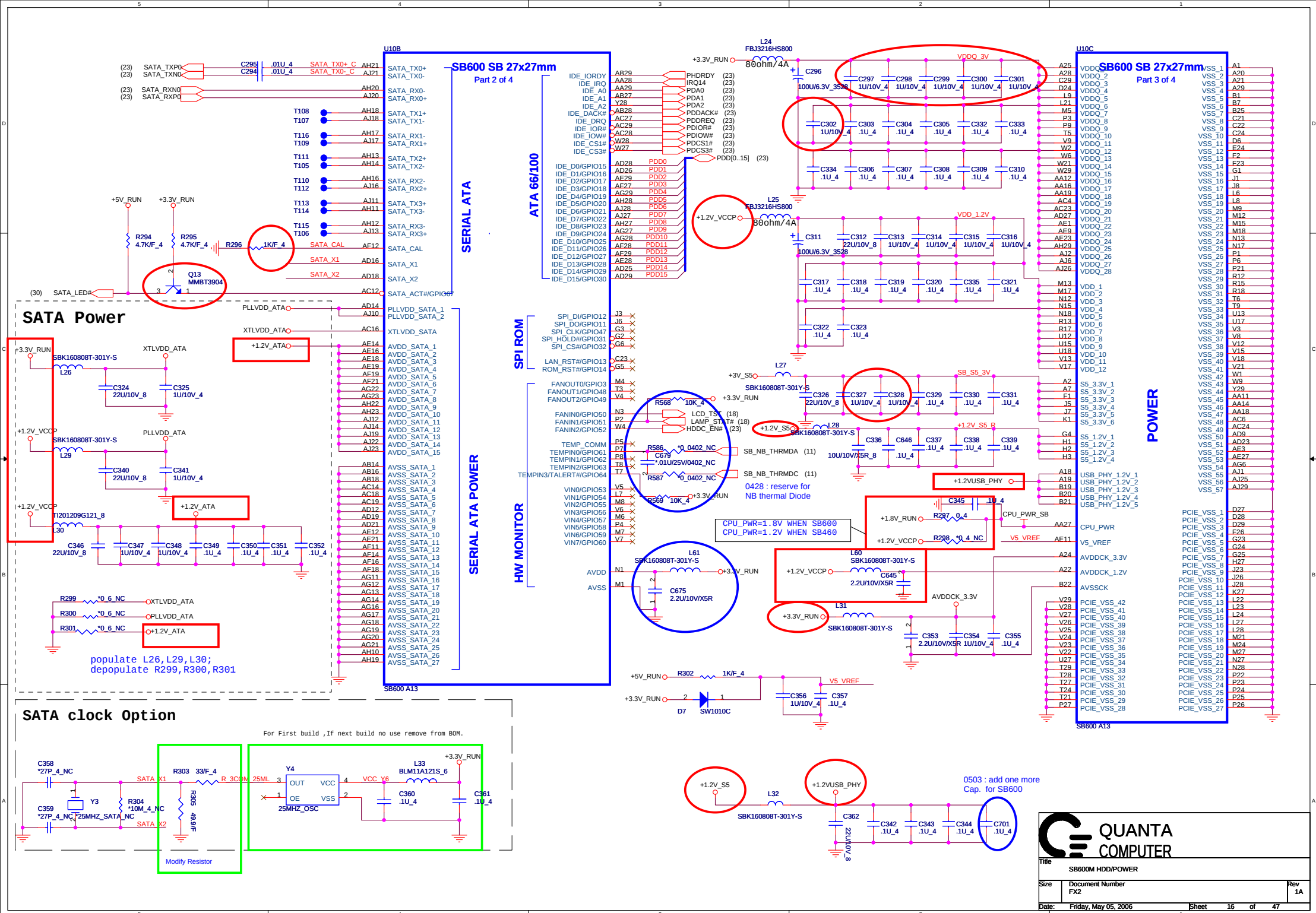
Place these caps close to connector



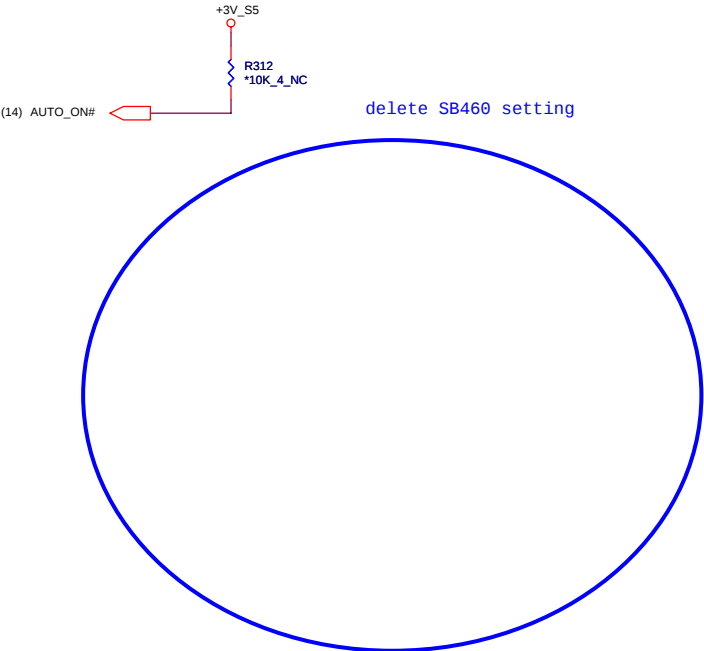
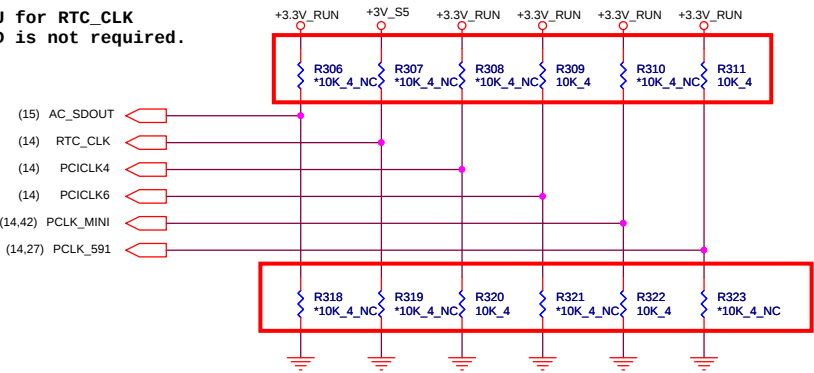




1

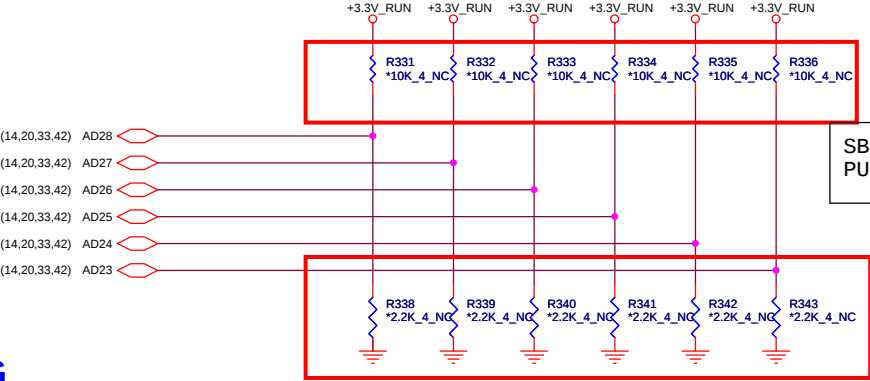


SB600 has 15K internal PD for AC_SDOUT
15K internal PU for RTC_CLK
,External PU/PD is not required.



REQUIRED STRAPS

		PCLK_MINI PCLK_591	
		PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48
PULL LOW	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ



SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET	Use Long Reset	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	boot fail time disabled
PULL LOW	USE SHORT RESET	Use Short Reset	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	boot fail time enabled



QUANTA
COMPUTER

TitleSB600M STRAPS

SizeDocument NumberFX2Rev1A

Date:Friday, May 05, 2006Sheet17 of 47



LID_CL# is connected to pull high circuit , then EC , as Page of EC.



as Tom suggestion , connect
to EC "MBCLK" & "MBDATA".

LD0C_CLK/DATA change to PHL_CLK/DATA
that connected to ATI NB

Address : A9H --Contrast
AAH --Backlight

M'07 inverter support - De-populate D16.
D'05 inverter support - Populate D16

as Tom suggestion , connect to EC "MBCLK" & "MBDATA".

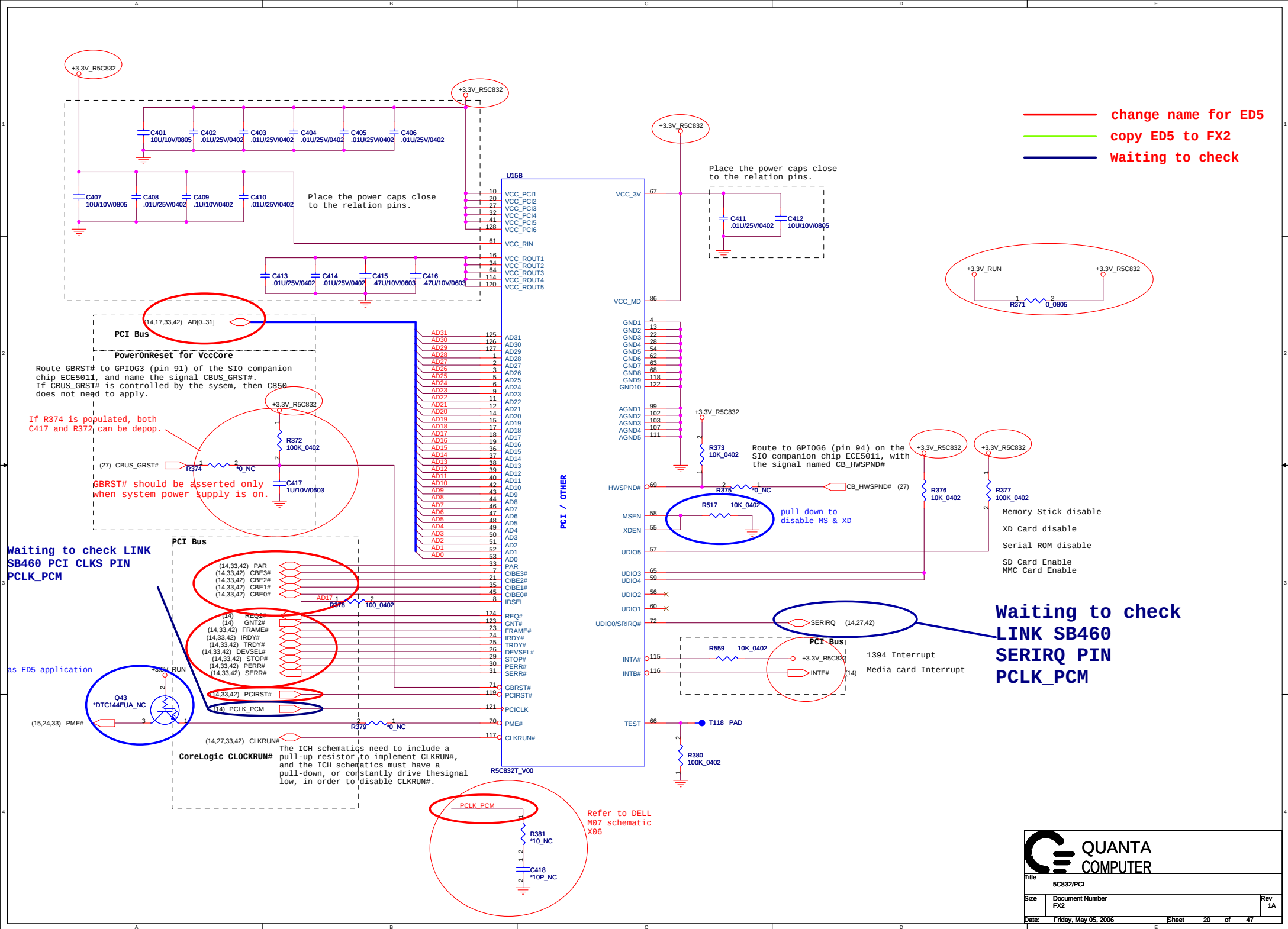
On FM1, LCD_TST & LAMP_STAT
connect to SB ; on FX2 ??.

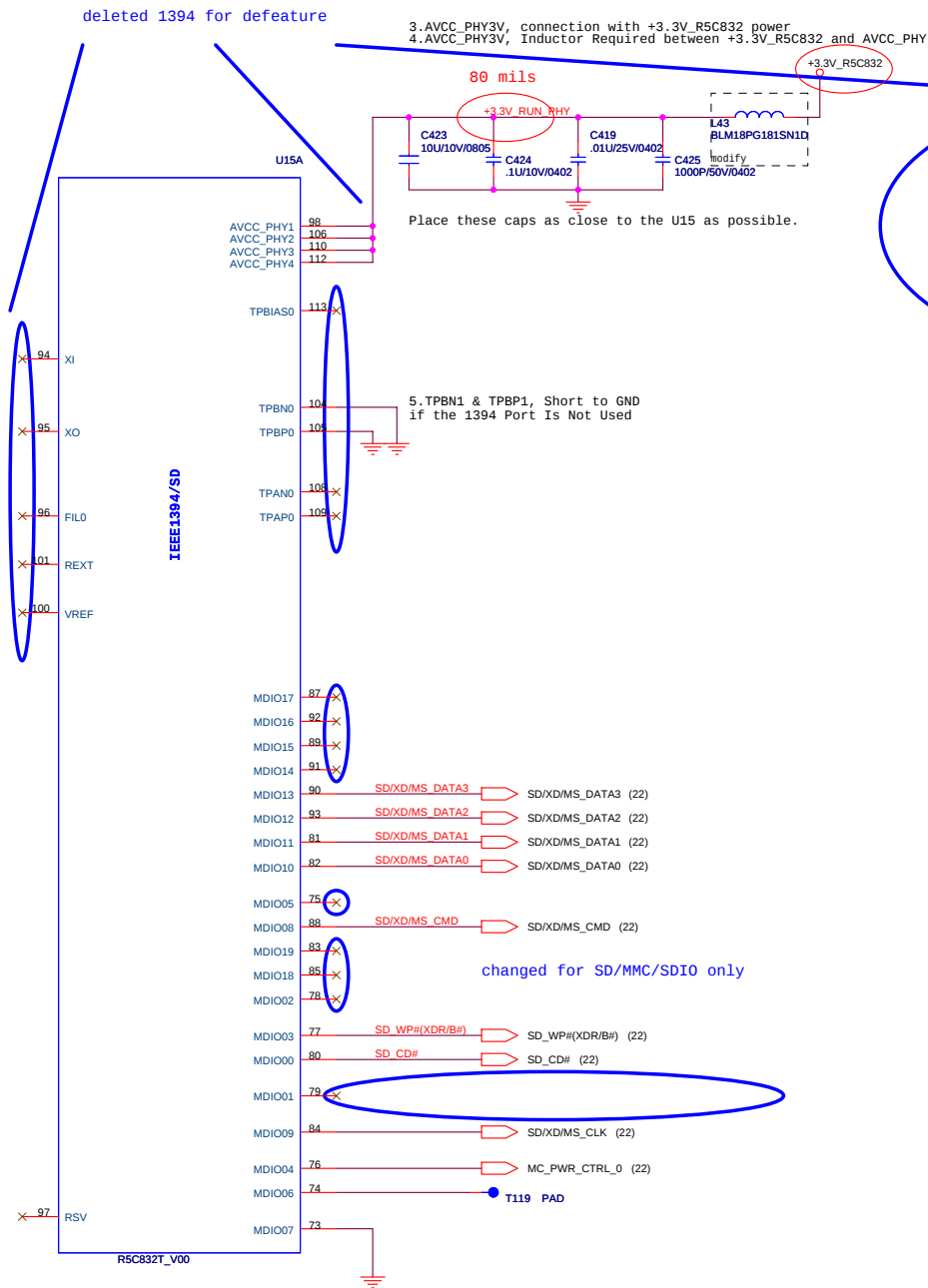
For Discrete:
De-populate J1, R230, C311, C331, C332,
D16, C333, C329, C341, C324, C326



Place All of those
Inductors Caps close
to JVGA1 <200 mils

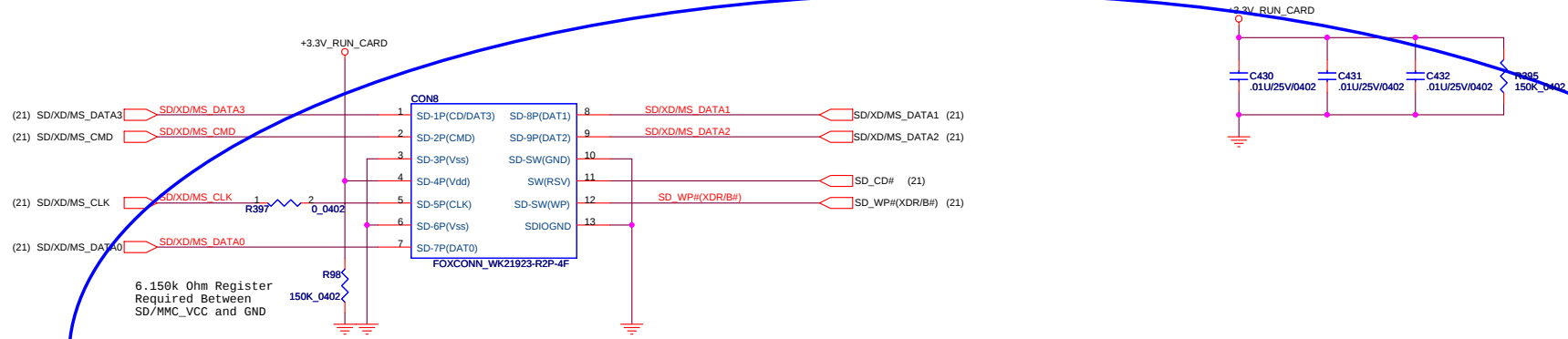




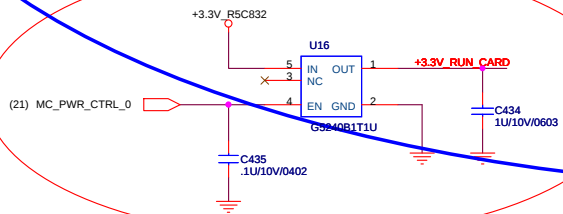


DO NOT INSERT SD/MMC SIMULTANEOUSLY.

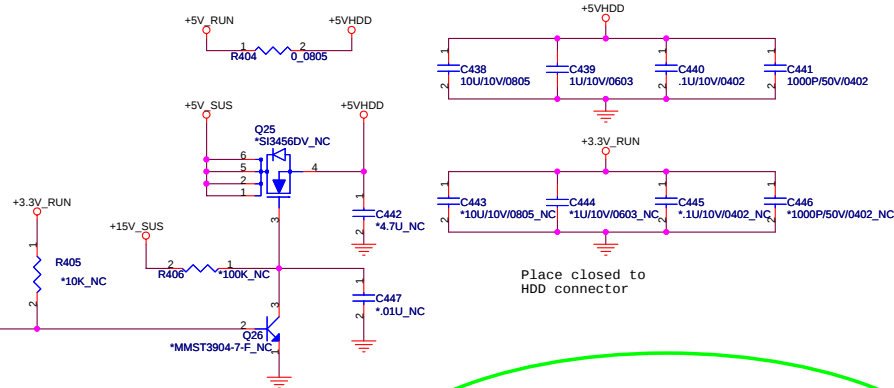
changed for SD/MMC/SDIO only



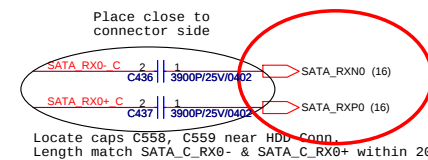
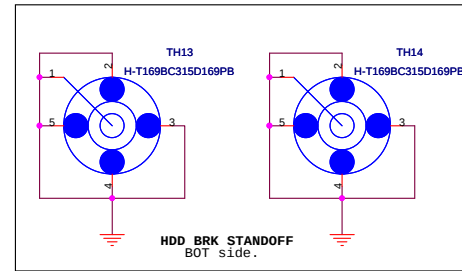
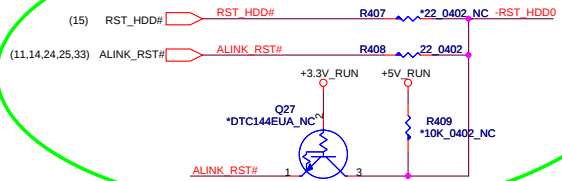
For SD/MS power



SATA HDD



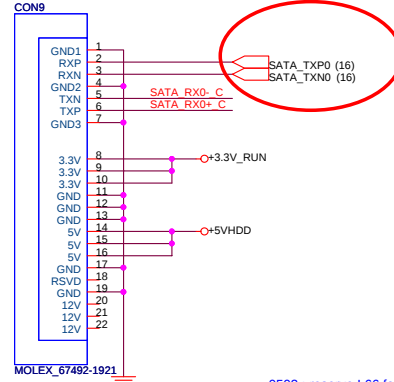
Place closed to HDD connector



Locate caps C558, C559 near HDD Conn. Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.

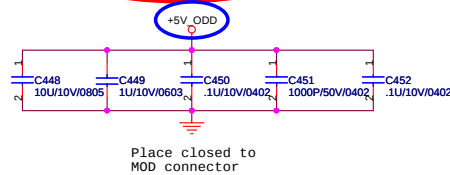
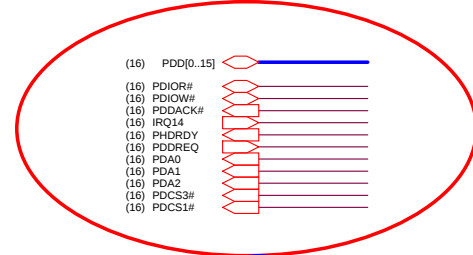
SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

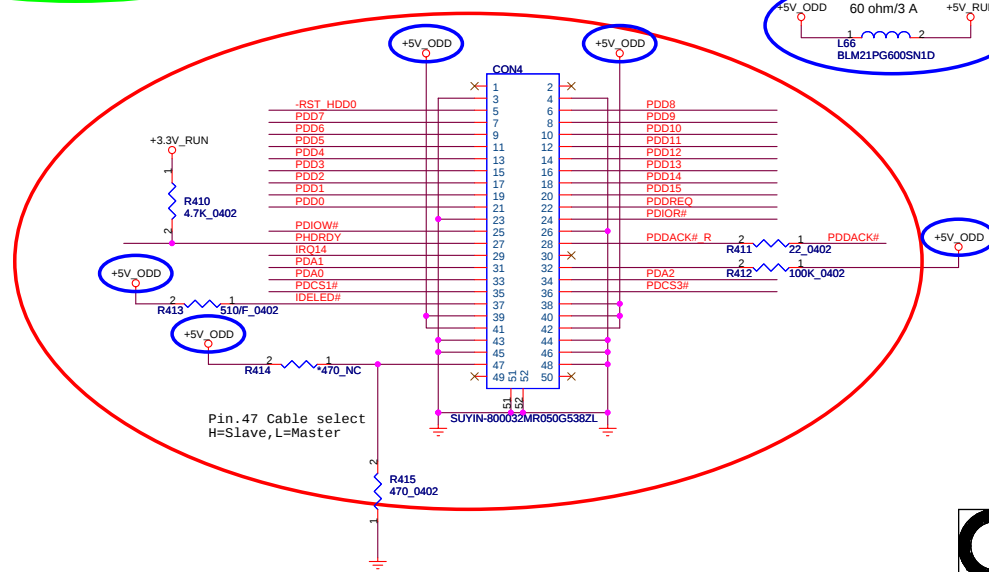


- change name for ED5
- copy ED5 to FX2
- Waiting to check

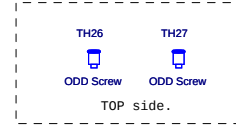
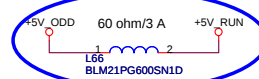
PATA ODD



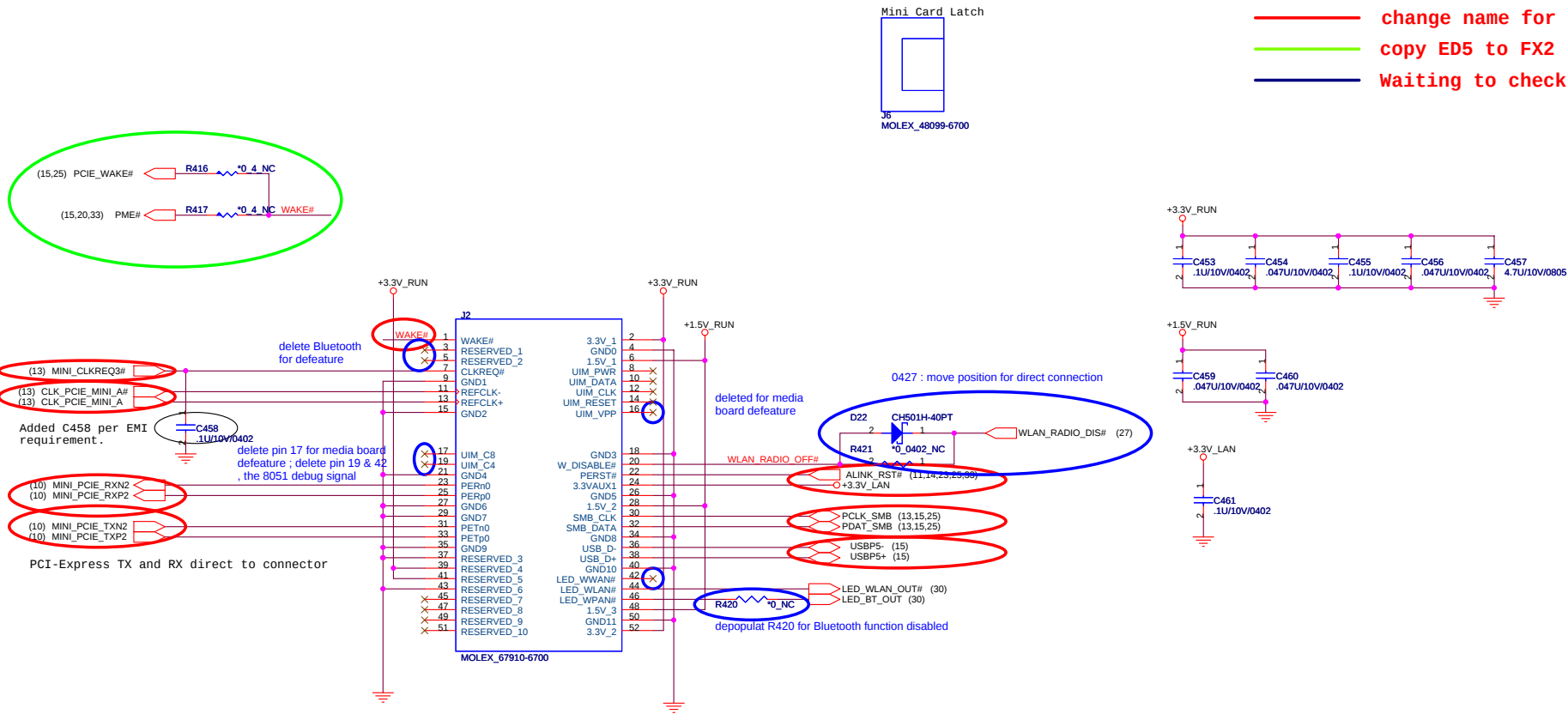
Place closed to MOD connector



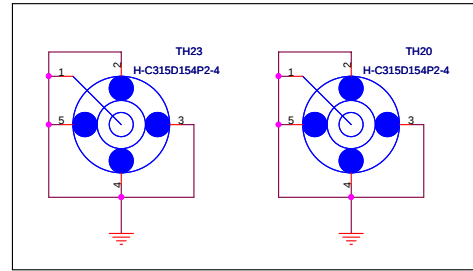
Pin.47 Cable select
H=Slave, L=Master



MINI CARD



Express Card



- change name for ED5
- copy ED5 to FX2
- Waiting to check

NEW CARD GUIDE POST
TOP side.

swap traces as "fx2_swap-0412"

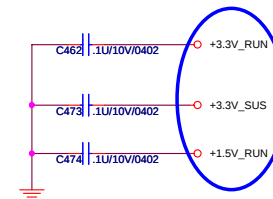
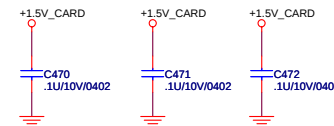
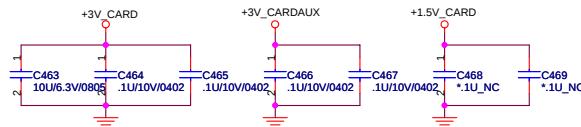
as ED5 application

reserve for pull up

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

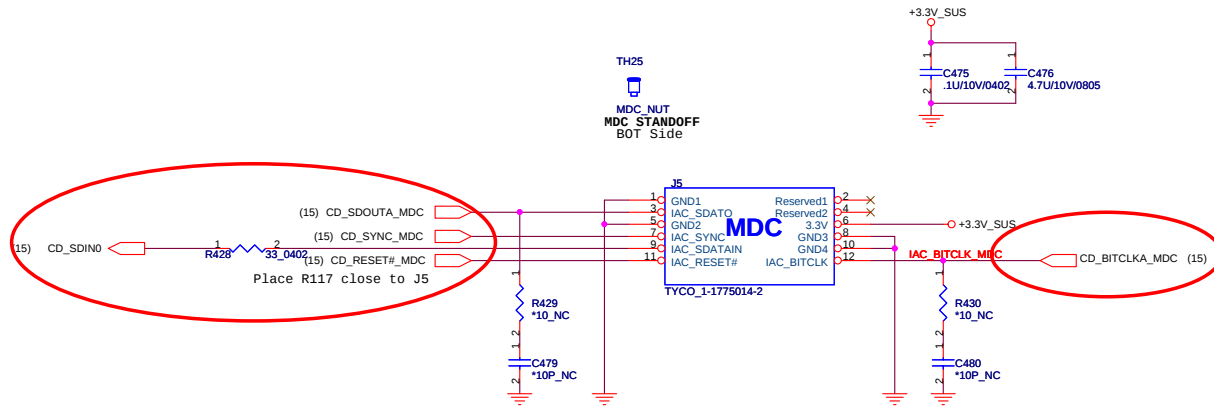
0427 : change from only net
name to symbol "power point"



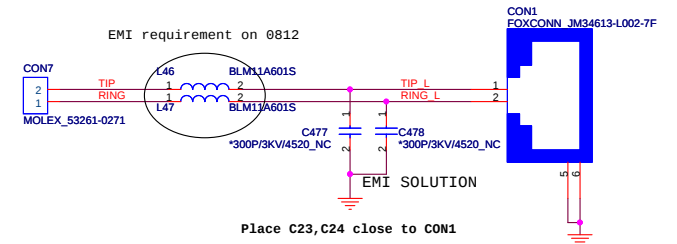
MDC INTERFACE

MDC Layout Notes

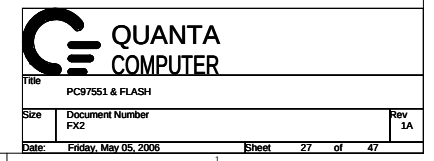
1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG (stranded or twisted pair wire)



- change name for ED5
- copy ED5 to FX2
- Waiting to check

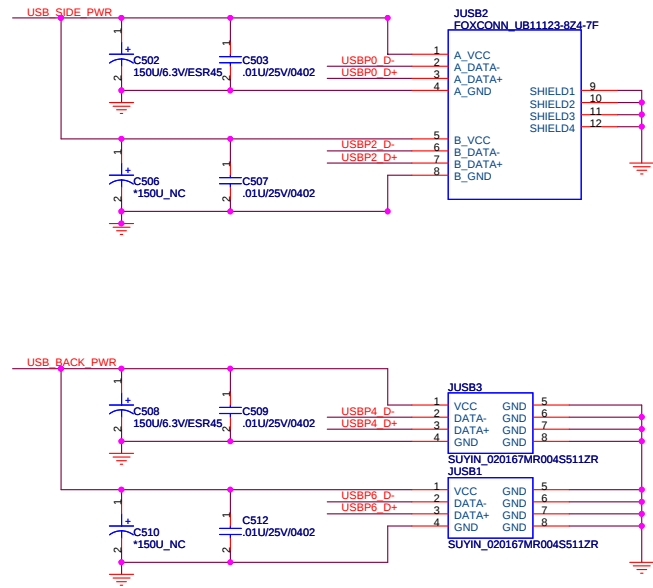
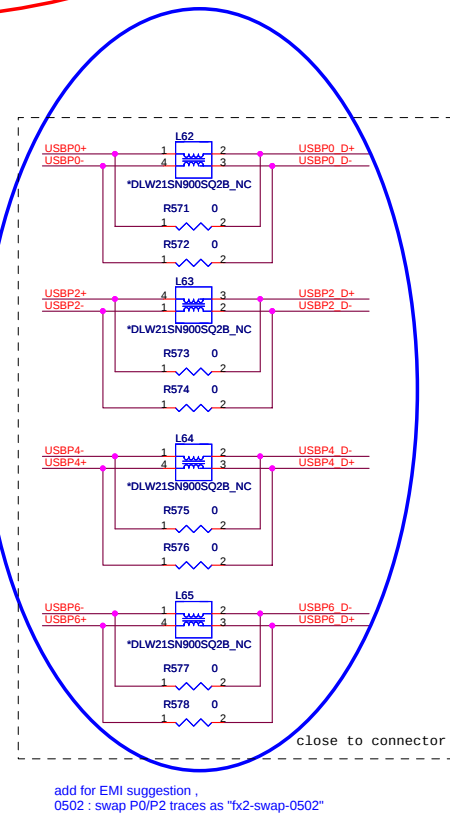
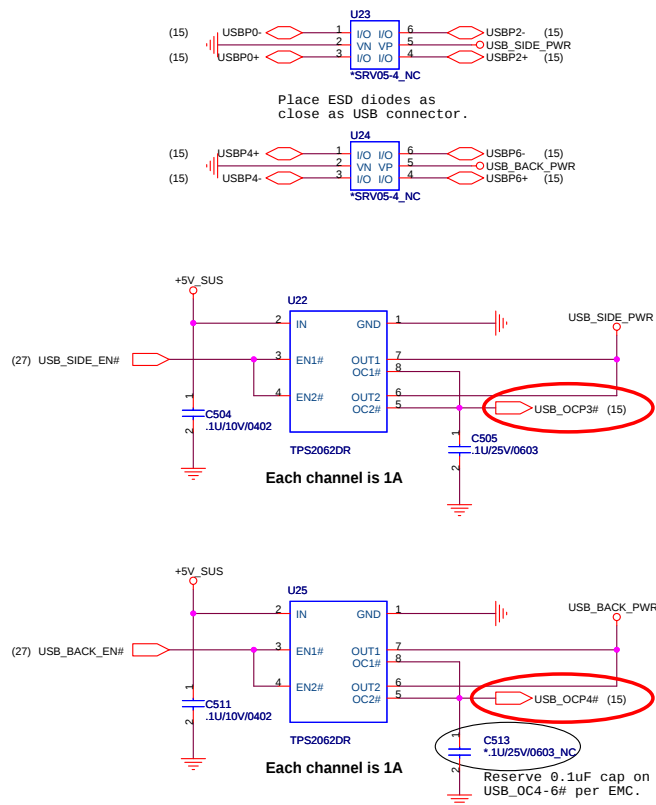


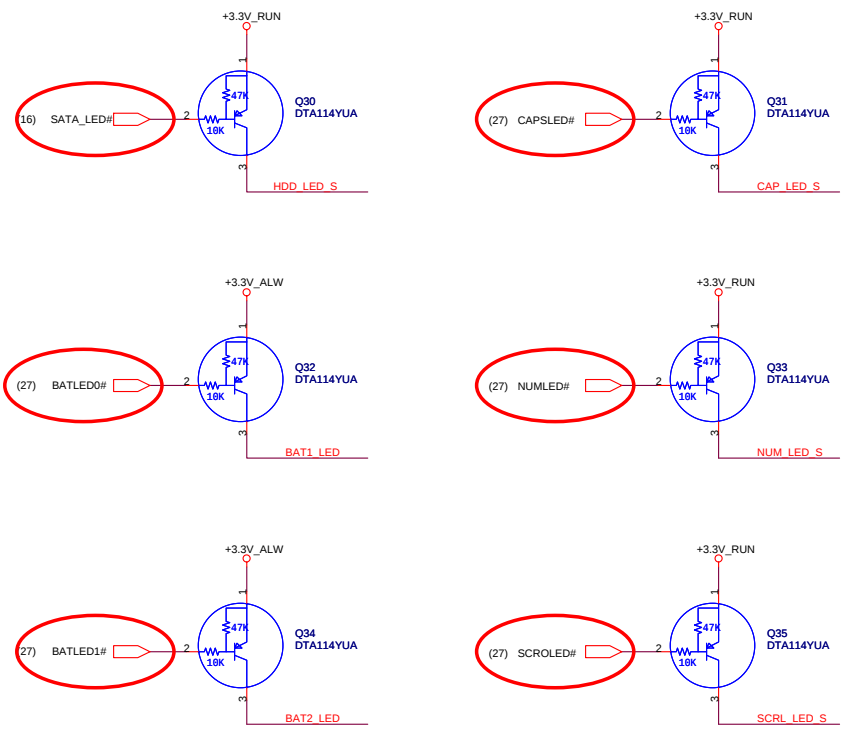
delete Bluetooth
for defeature



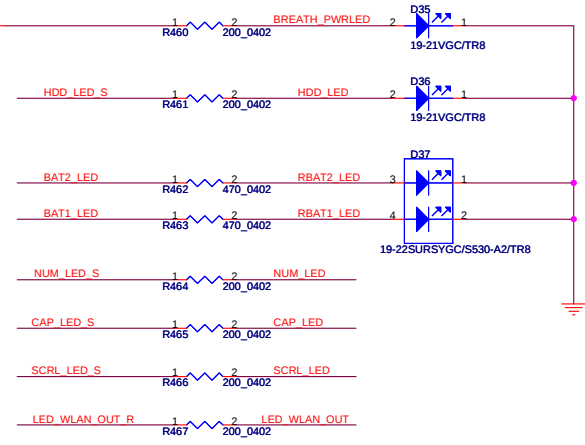
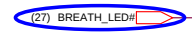
8Mbit (1M Byte), SPI

- change name for ED5
- copy ED5 to FX2
- Waiting to check

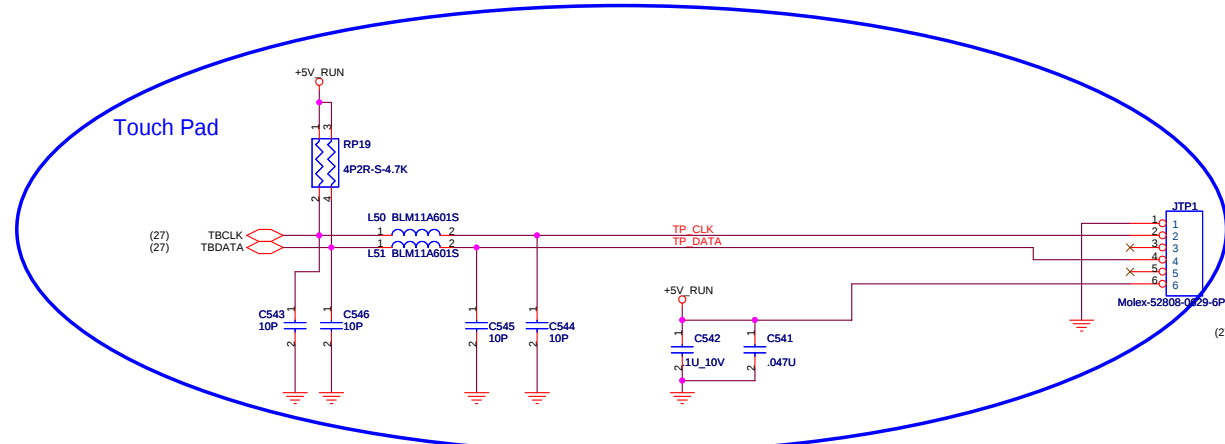




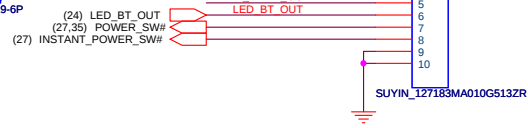
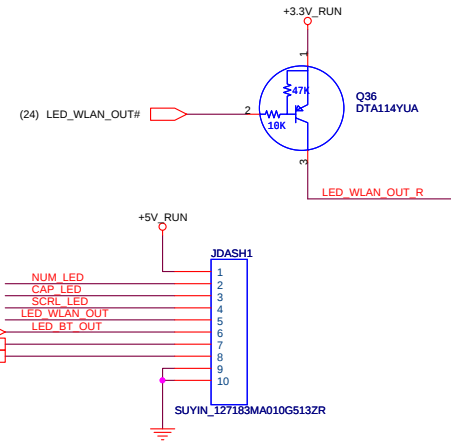
0427 : change from
BREATH_LED to BREATH_LED#

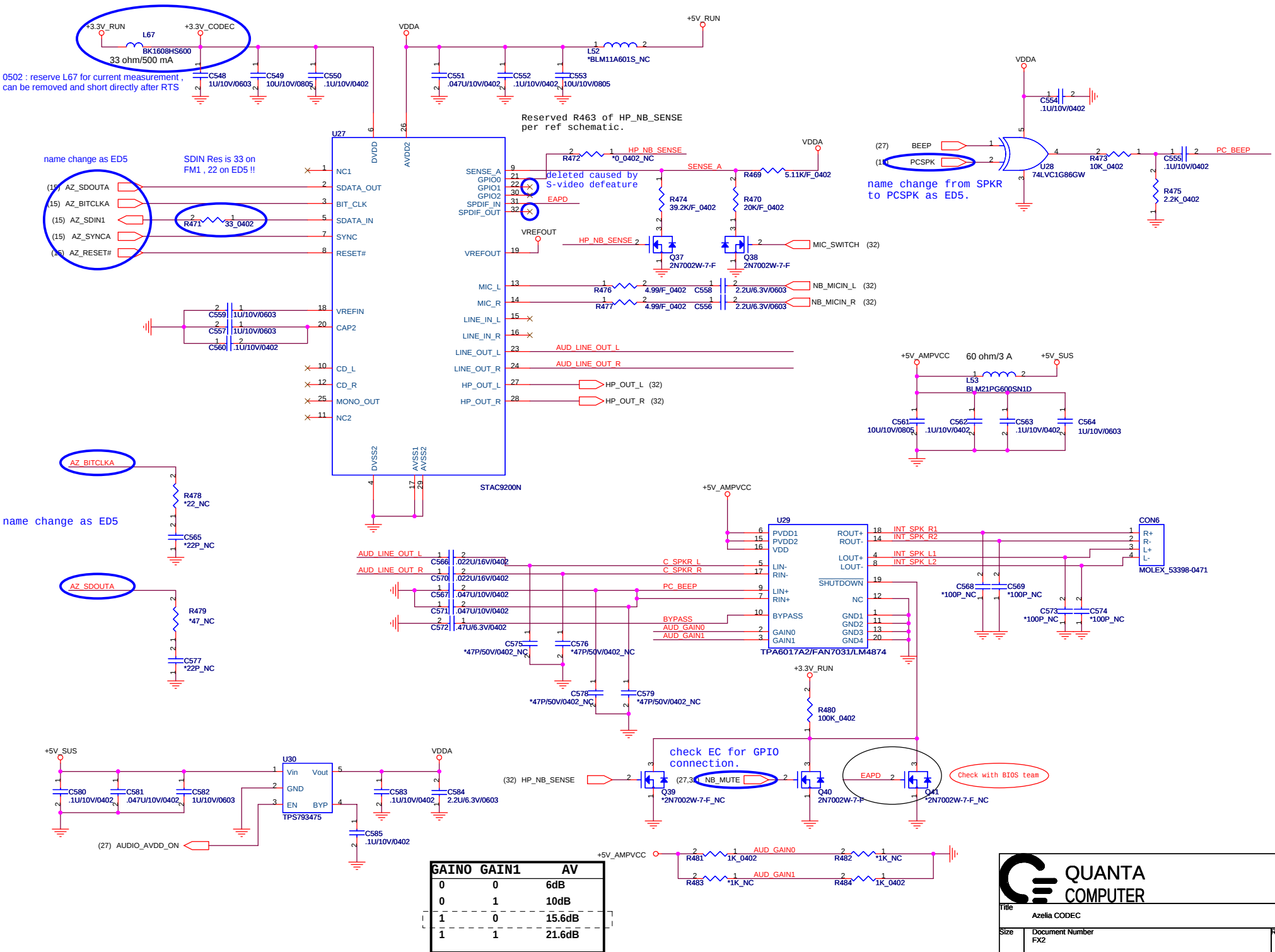


- change name for ED5
- copy ED5 to FX2
- Waiting to check



FM1 media board changed to TP only as DM5





0502 : reserve L67 for current measurement , can be removed and short directly after RTS

name change as ED5
SDIN Res is 33 on FM1 , 22 on ED5 !!

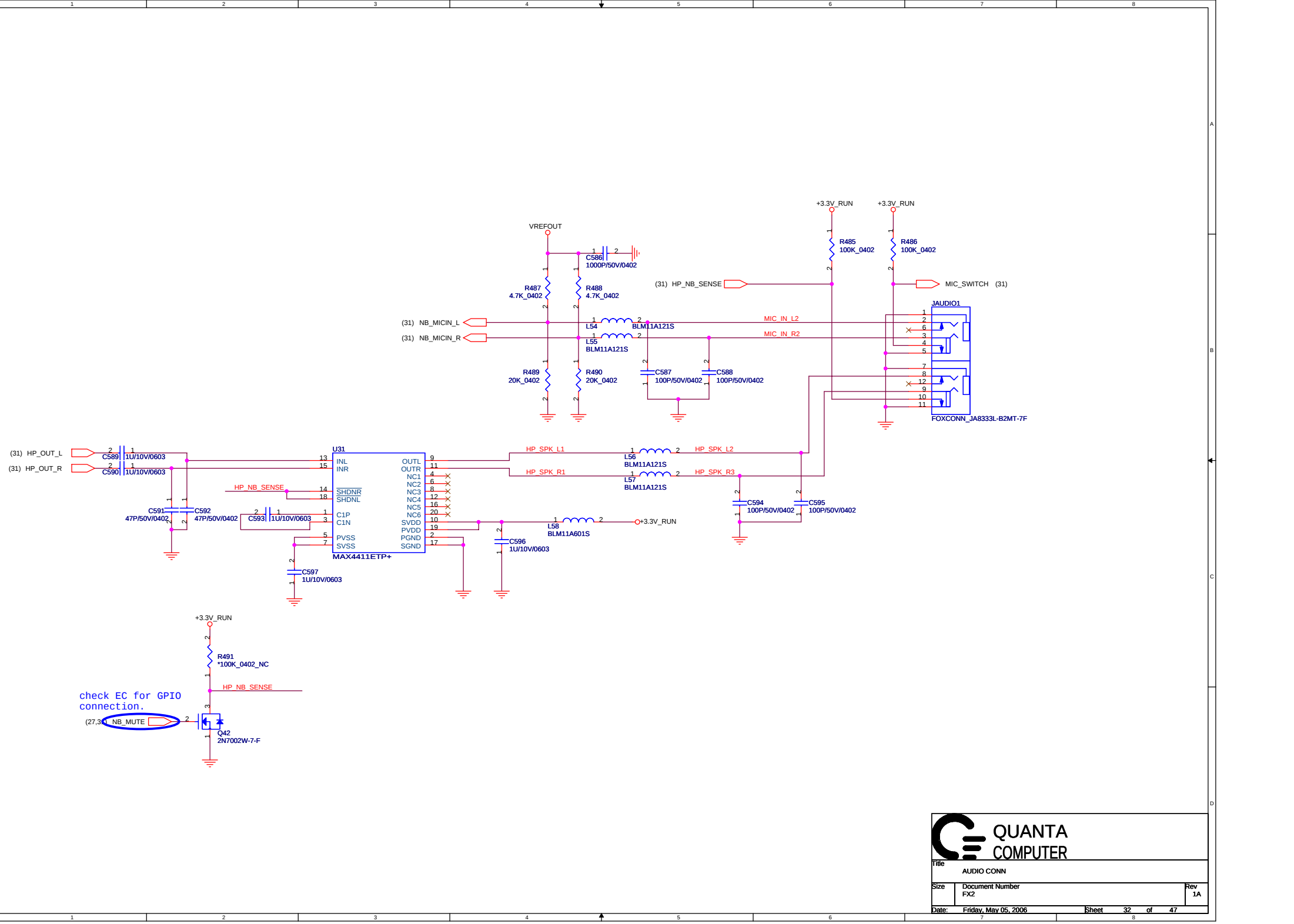
name change as ED5

check EC for GPIO connection.

Check with BIOS team

GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

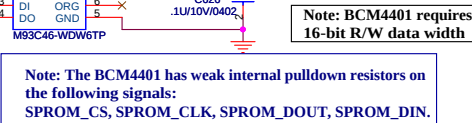




Place C607 close to pin65

EMI requirement on 0812

change name for ED5
copy ED5 to FX2
Waiting to check

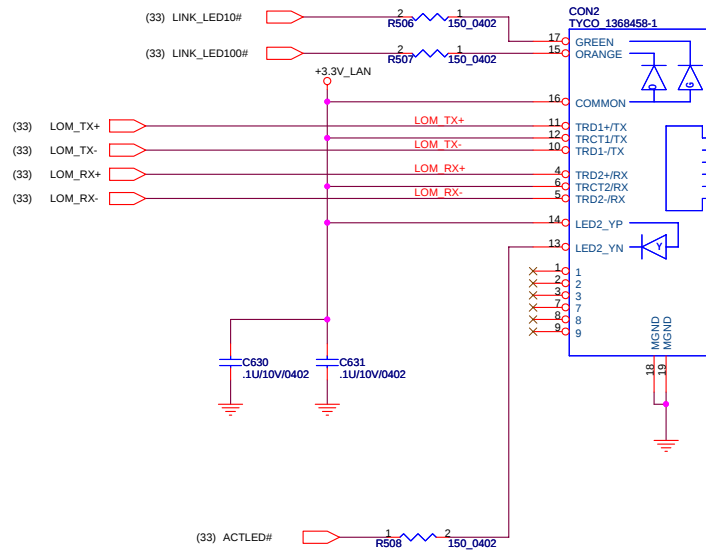


Note: The BCM4401 has weak internal pulldown resistors on the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.

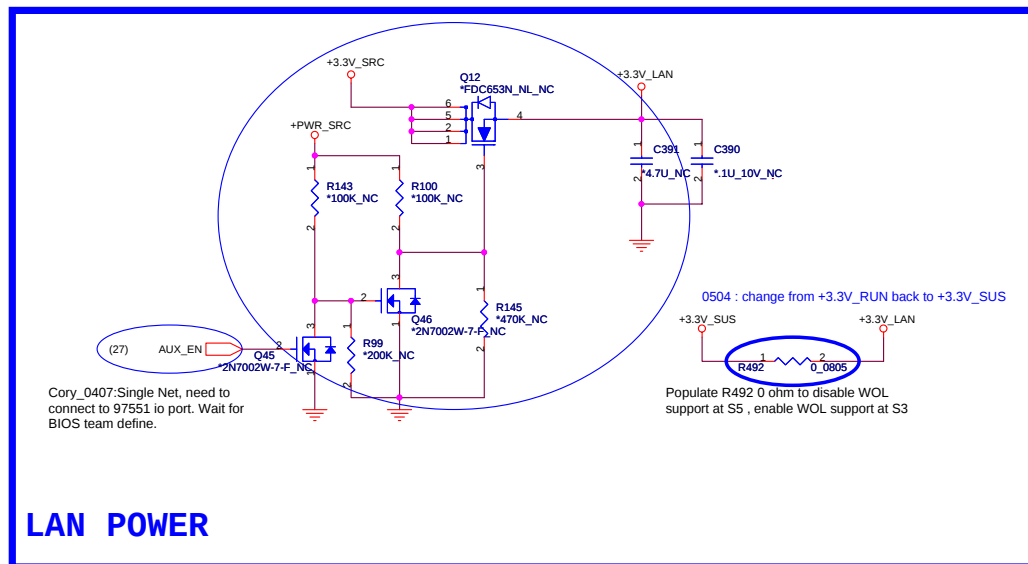
Note: BCM4401 requires 16-bit B/W data width.

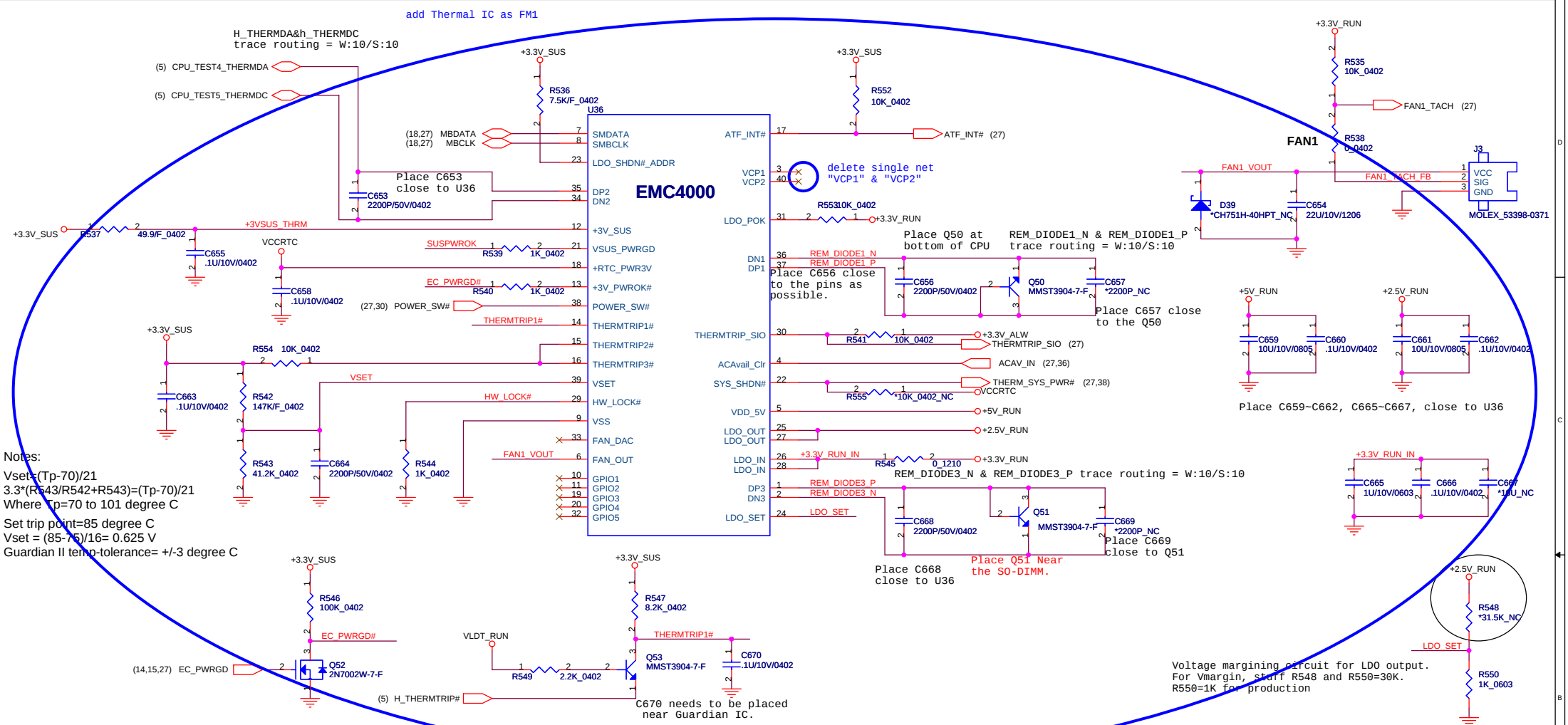


Title			
LAN(BCM4401)			
Size	Document Number	Rev	
	FX2	1A	
Date:	Friday, May 05, 2006	Sheet	33 of 47



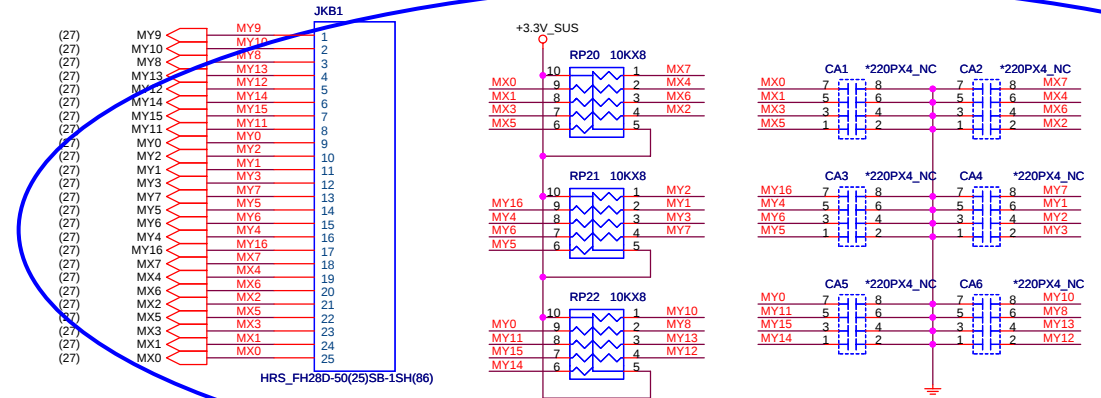
- change name for ED5
- copy ED5 to FX2
- Waiting to check
- copy DM5 to FX2





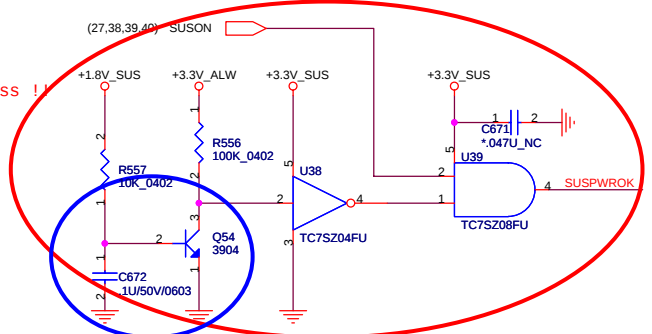
Notes:
Vset=(Tp-70)/21
3.3*(R543/R542+R543)=(Tp-70)/21
Where Tp=70 to 101 degree C
Set trip point=85 degree C
Vset = (85-76)/16= 0.625 V
Guardian II temp-tolerance= +/-3 degree C

as FM1 keyboard matrix & "e0788.1104a_swap-0422"



KBC

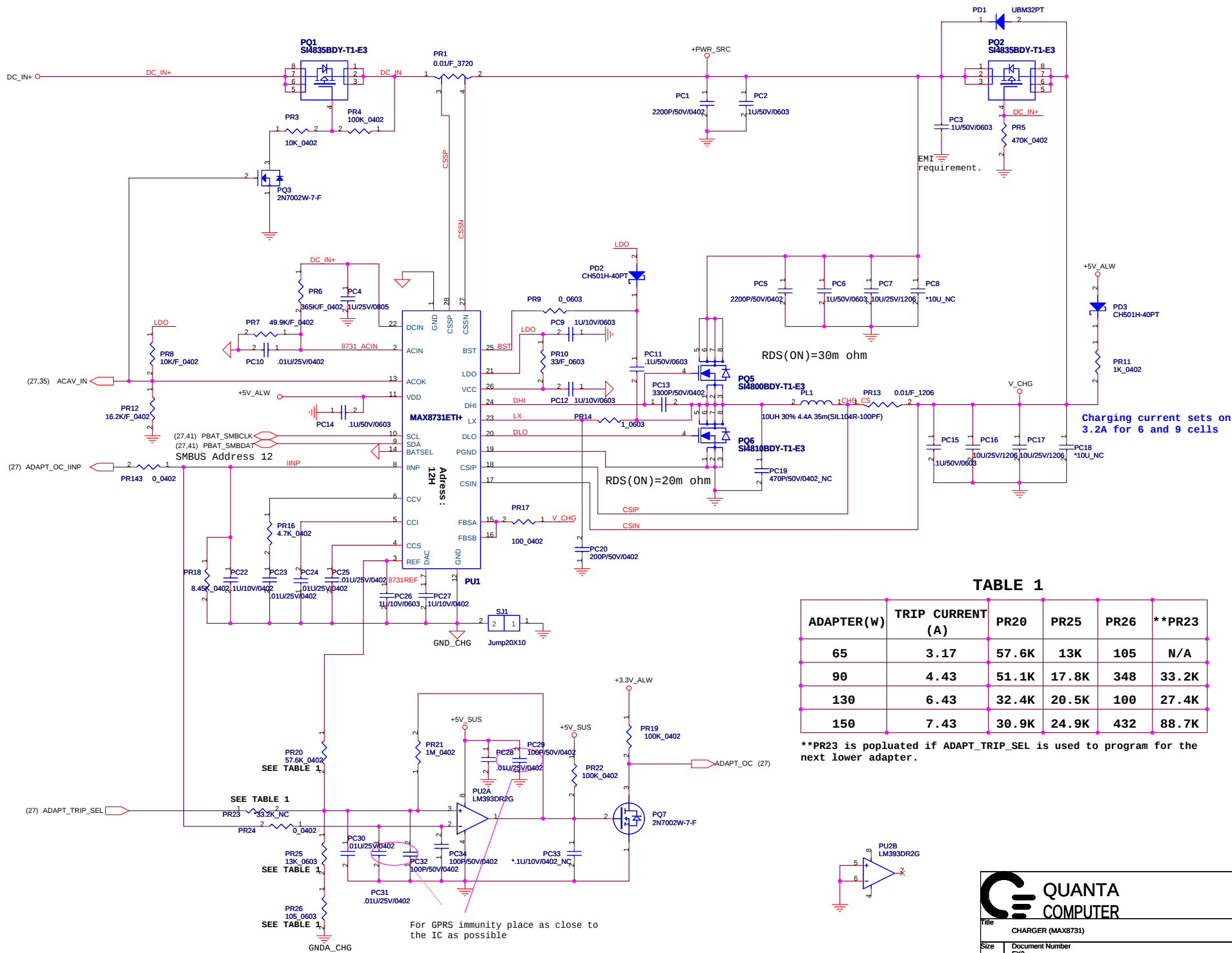
wait to discuss !!

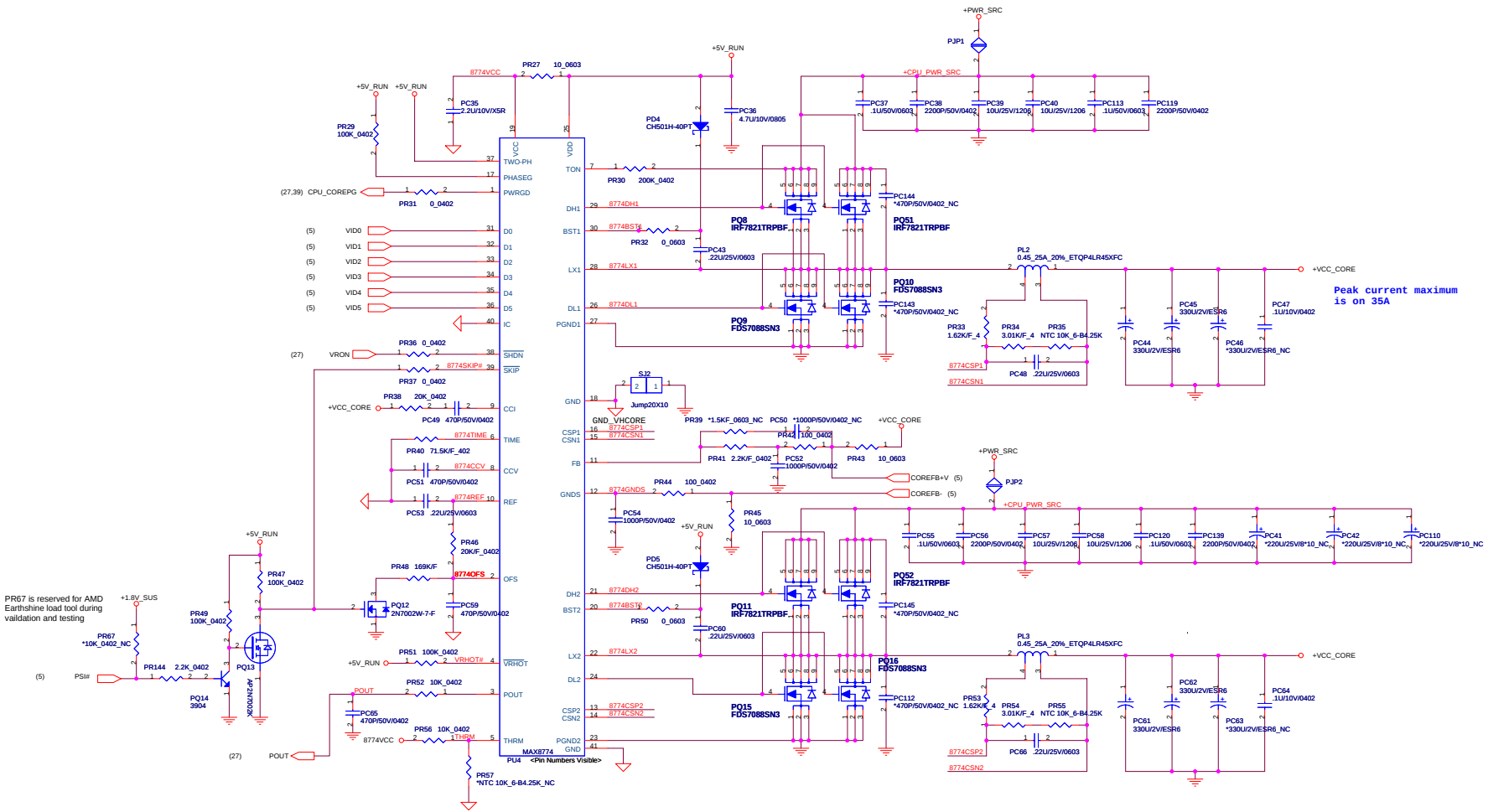




QUANTA
COMPUTER

Title		
KB & THERMAL & FAN		
Size	Document Number	Rev
FX2		1A
Date:	Friday, May 05, 2006	Sheet 35 of 47



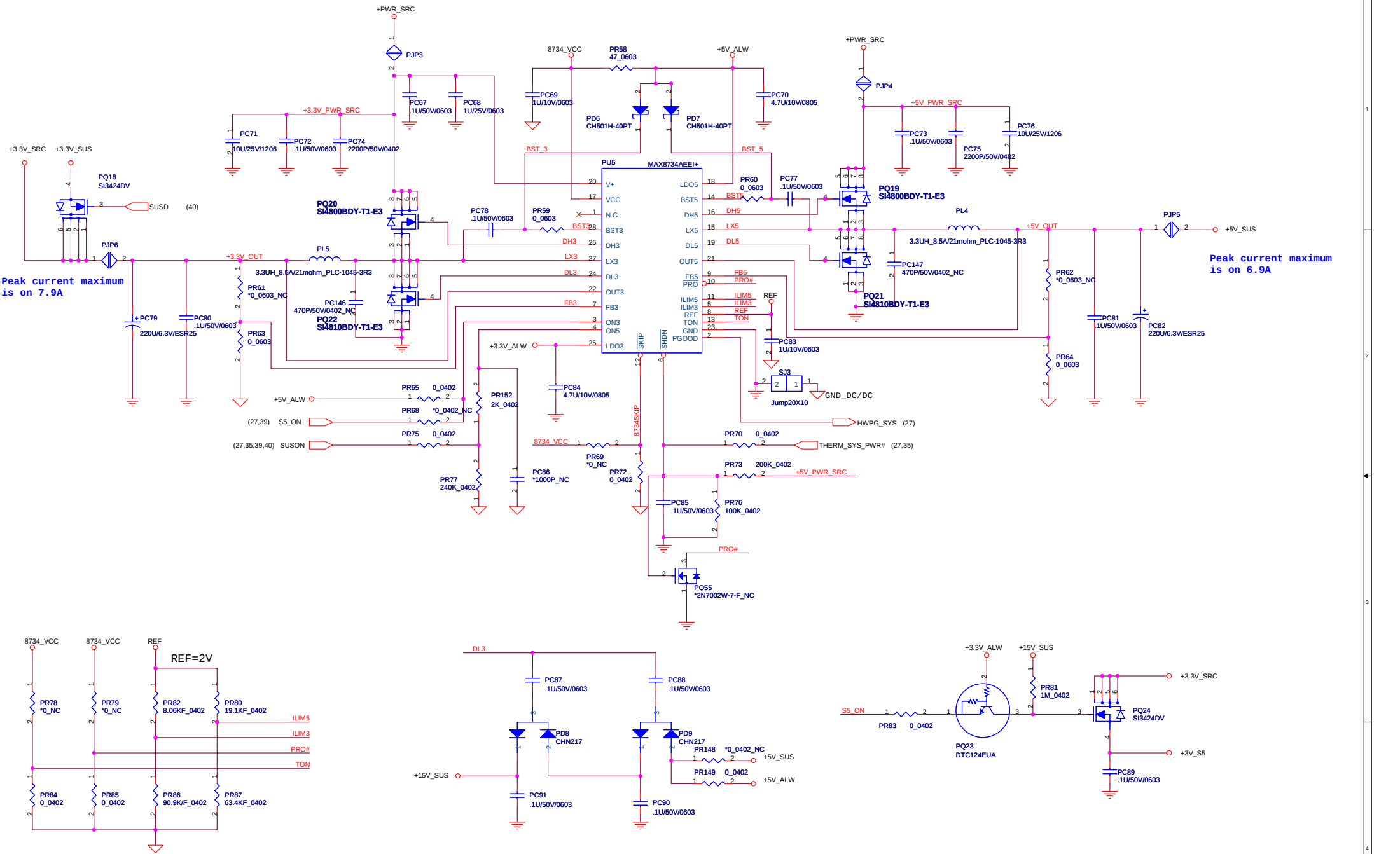


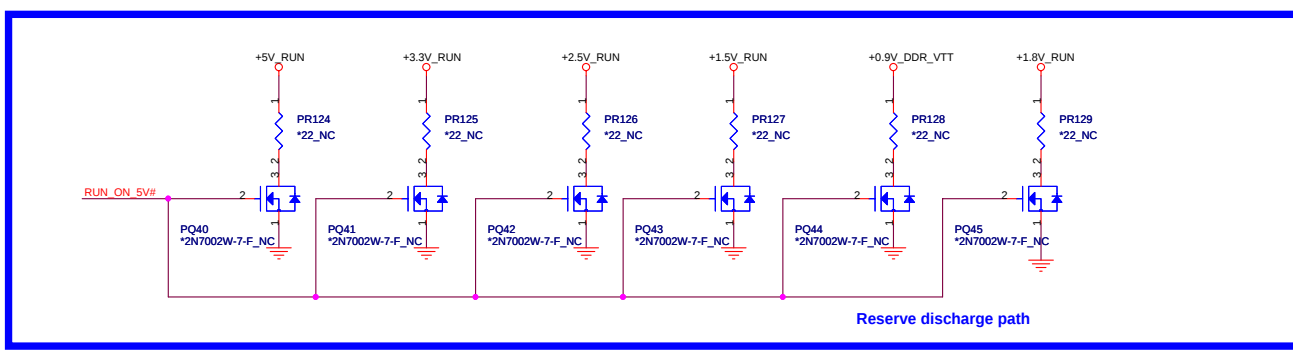
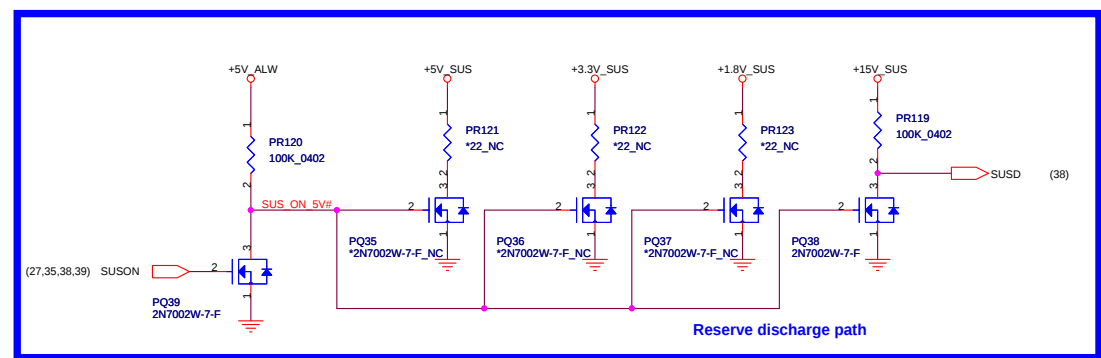
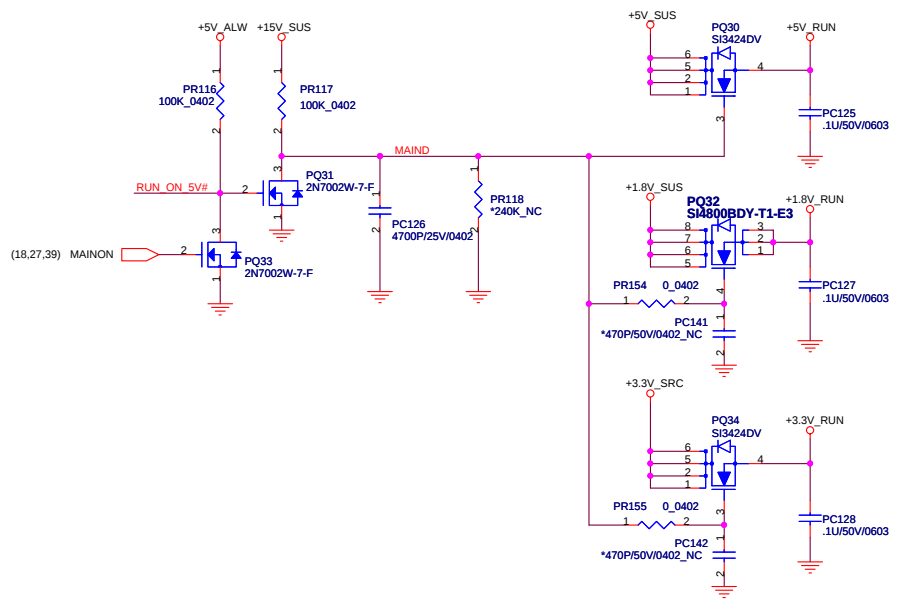
PR67 is reserved for AMD Earthshine load tool during validation and testing

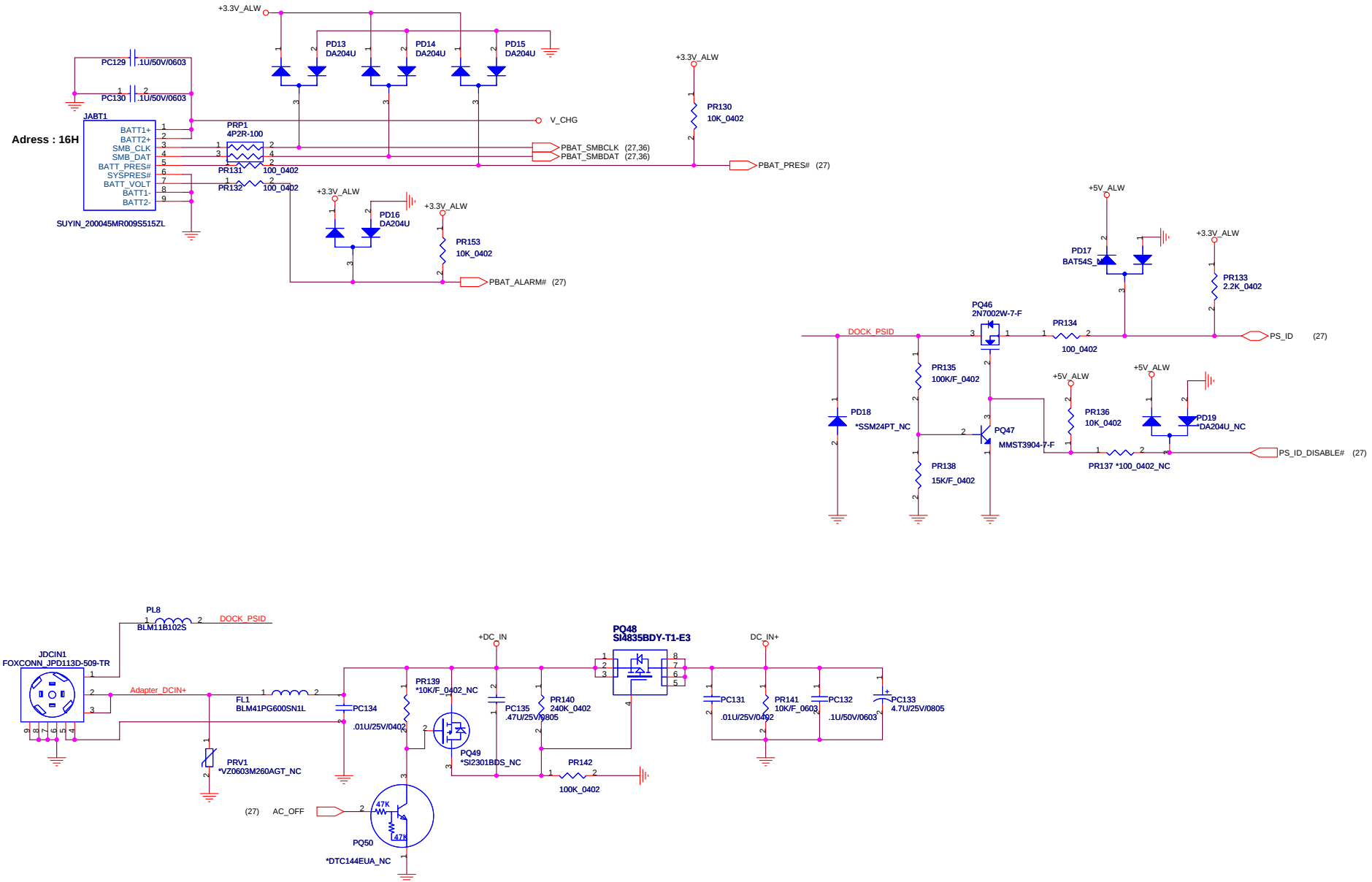
Peak current maximum is on 35A

D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V
0	0	0	0	0	1	1.5250V
0	0	0	0	1	0	1.5000V
0	0	0	0	1	1	1.4750V
0	0	0	1	0	0	1.4500V
0	0	0	1	0	1	1.4250V
0	0	0	1	1	0	1.4000V
0	0	1	0	0	0	1.3750V
0	0	1	0	0	1	1.3500V
0	0	1	0	1	0	1.3250V
0	0	1	0	1	1	1.3000V
0	0	1	1	0	0	1.2750V
0	0	1	1	0	1	1.2500V
0	0	1	1	1	0	1.2250V
0	0	1	1	1	1	1.2000V
0	1	0	0	0	0	1.1750V
0	1	0	0	0	1	1.1500V
0	1	0	0	1	0	1.1250V
0	1	0	0	1	1	1.1000V
0	1	0	1	0	0	1.0750V
0	1	0	1	0	1	1.0500V
0	1	0	1	1	0	1.0250V
0	1	0	1	1	1	1.0000V
0	1	1	0	0	0	0.9750V
0	1	1	0	0	1	0.9500V
0	1	1	0	1	0	0.9250V
0	1	1	0	1	1	0.9000V
0	1	1	1	0	0	0.8750V
0	1	1	1	0	1	0.8500V
0	1	1	1	1	0	0.8250V
0	1	1	1	1	1	0.8000V
0	1	1	1	1	1	0.7750V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	0.7500V
1	0	0	0	0	1	0.7375V
1	0	0	0	1	0	0.7250V
1	0	0	0	1	1	0.7125V
1	0	0	1	0	0	0.7000V
1	0	0	1	0	1	0.6875V
1	0	0	1	1	0	0.6750V
1	0	1	0	0	0	0.6625V
1	0	1	0	0	1	0.6500V
1	0	1	0	1	0	0.6375V
1	0	1	0	1	1	0.6250V
1	0	1	1	0	0	0.6125V
1	0	1	1	0	1	0.6000V
1	0	1	1	1	0	0.5875V
1	0	1	1	1	1	0.5750V
1	1	0	0	0	0	0.5625V
1	1	0	0	0	1	0.5500V
1	1	0	0	1	0	0.5375V
1	1	0	0	1	1	0.5250V
1	1	0	1	0	0	0.5125V
1	1	0	1	0	1	0.5000V
1	1	0	1	1	0	0.4875V
1	1	0	1	1	1	0.4750V
1	1	1	0	0	0	0.4625V
1	1	1	0	0	1	0.4500V
1	1	1	0	1	0	0.4375V
1	1	1	0	1	1	0.4250V
1	1	1	1	0	0	0.4125V
1	1	1	1	0	1	0.4000V
1	1	1	1	1	0	0.3875V
1	1	1	1	1	1	0.3750V



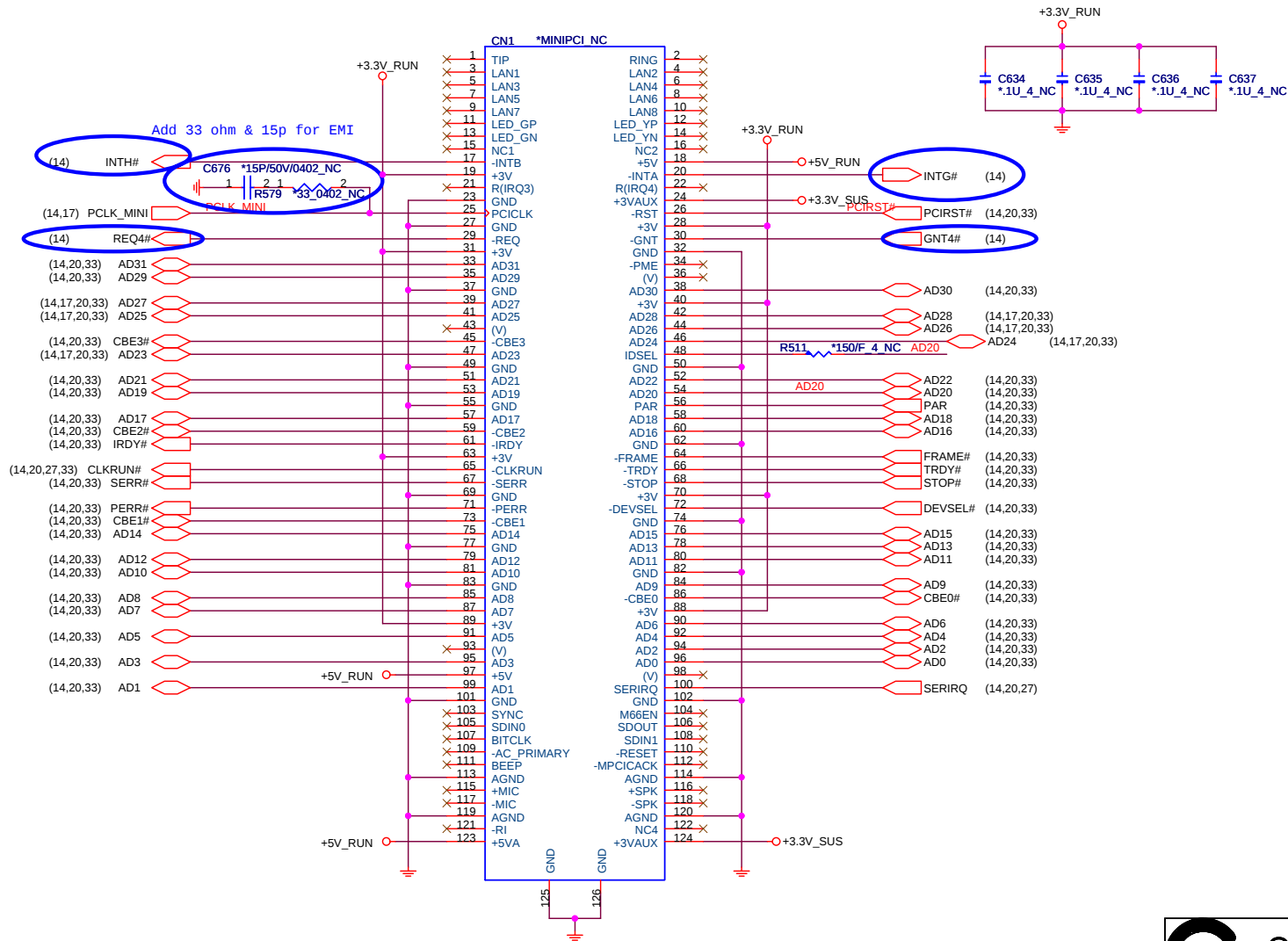




Title			DCIN,Batt
Size	Document Number	Rev	
FX2		1A	
Date:	Friday, May 05, 2006	Sheet	41 of 47

ID Select : AD20
Interrupt Pin : INTG# , INT#
Request Indicate : REQ4#
Grant Indicate : GNT4#

DEBUG PURPOSE ONLY



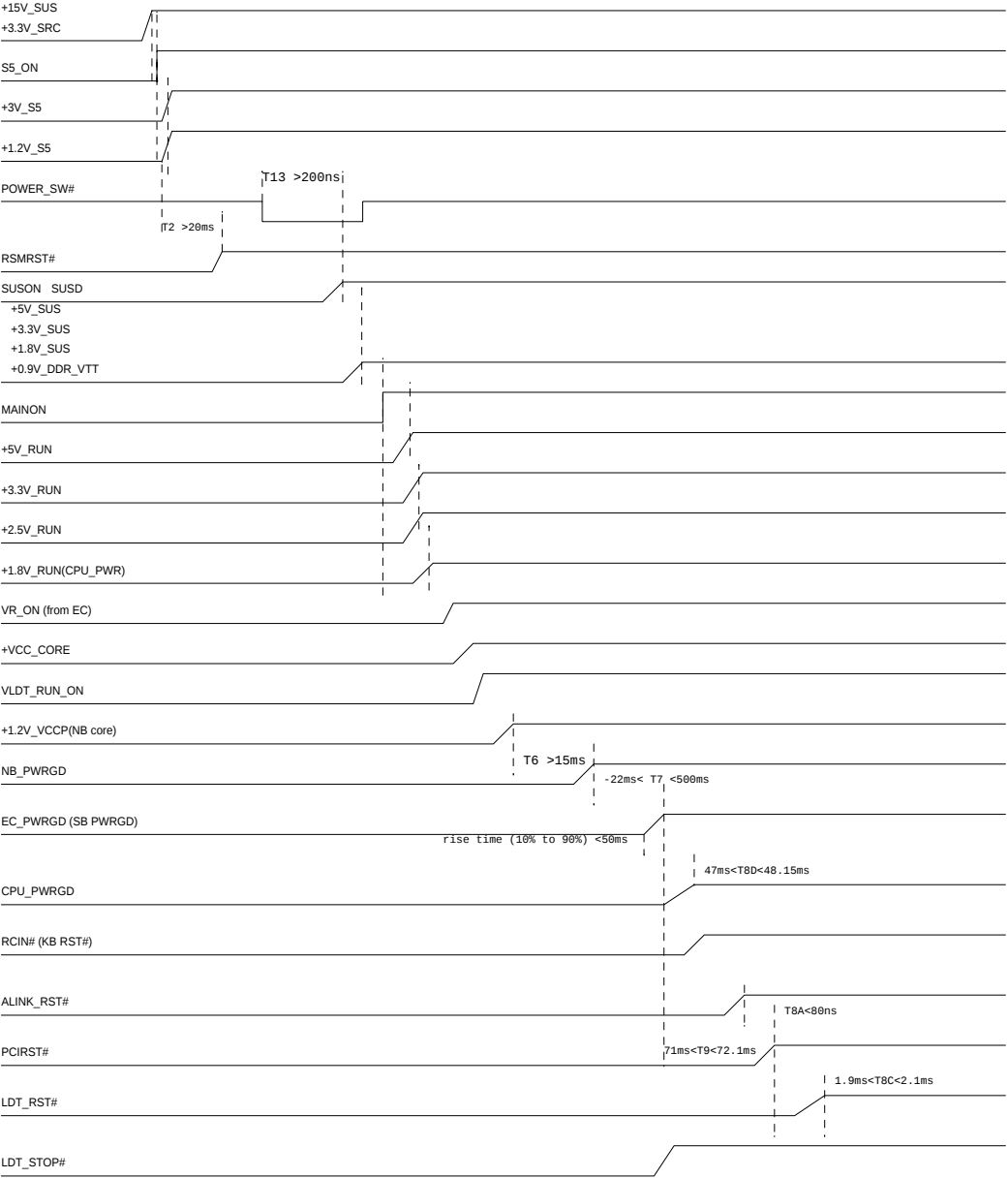
MPC



QUANTA
COMPUTER

Title MINI PCI(for debug)		
Size	Document Number FX2	Rev 1A
Date	Friday, May 05, 2006	Sheet 42 of 47

Power On Sequence



T6: NB core voltage to NB_PWRGD
T7: NB_PWRGD to SB_PWRGD
T8D: SB_PWRGD to CPU_PWRGD
T8A: ALINK_RST# to PCIRST#
T9: SB_PWRGD to PCIRST#
T8C: PCIRST# to LDT_RST#

