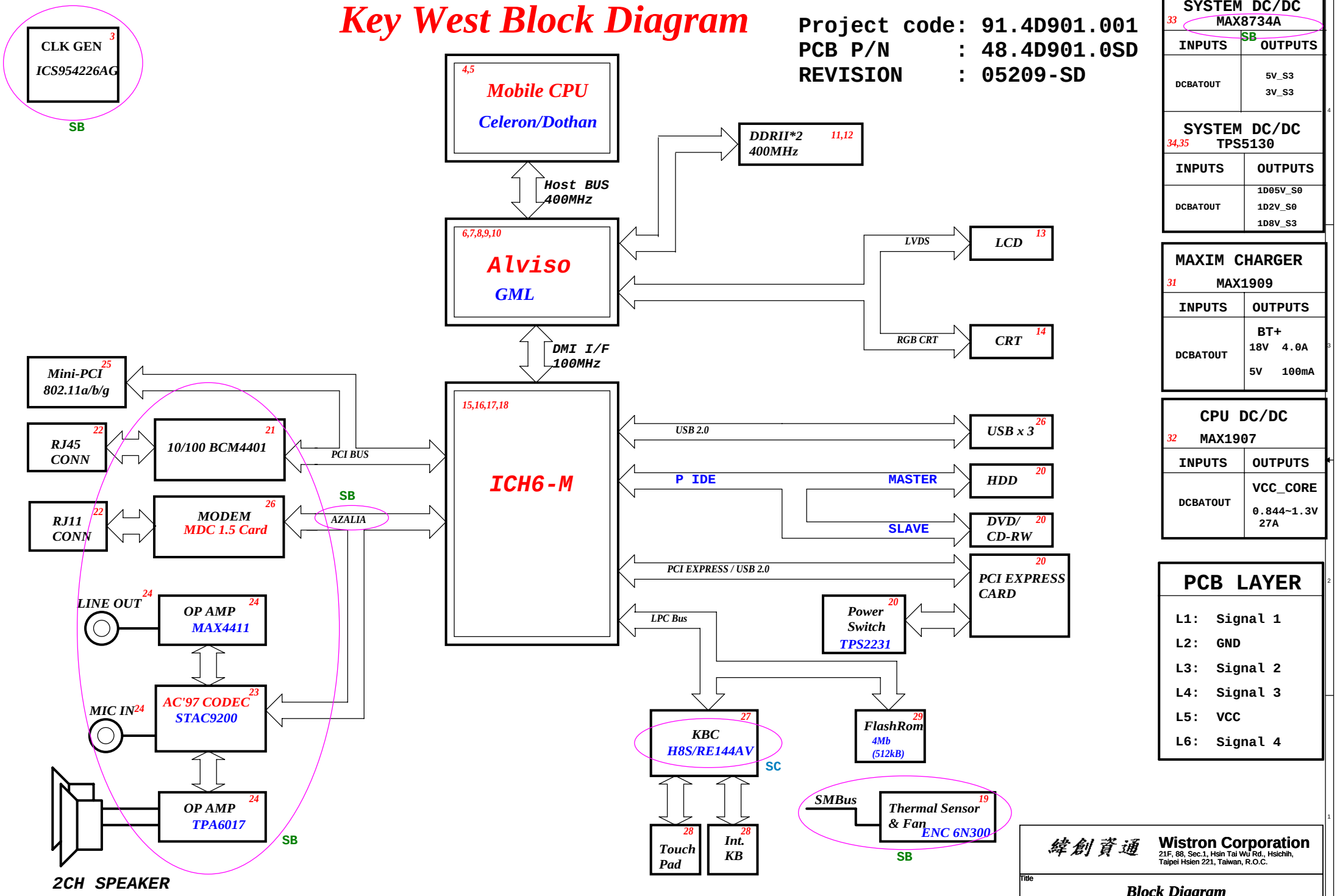
Key West Block Diagram

Project code: 91.4D901.001
PCB P/N : 48.4D901.0SD
REVISION : 05209-SD



SYSTEM DC/DC 33 MAX8734A SB	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S3

SYSTEM DC/DC 34,35 TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 1D8V_S3

MAXIM CHARGER 31 MAX1909	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC 32 MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 | Document Number: KeyWest | Rev: SD
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ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

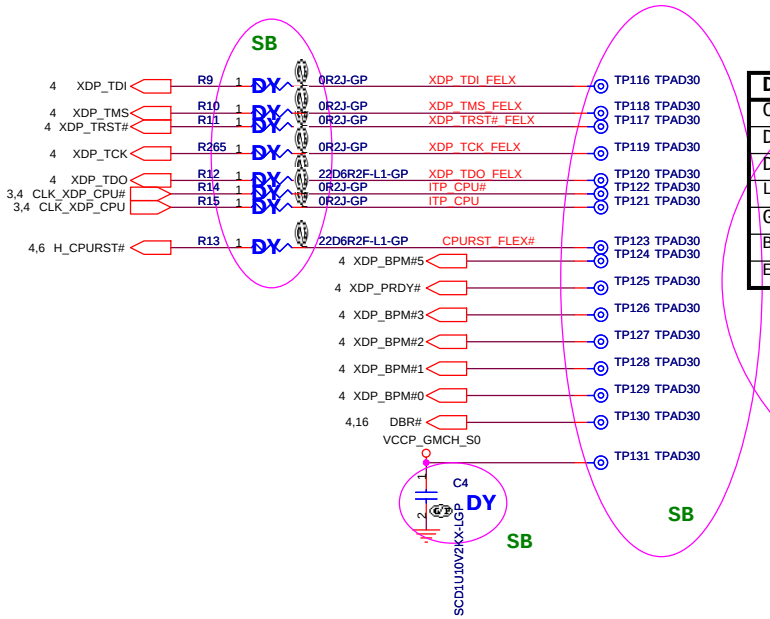
DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_2D5V= 2.5 Voltage power up on system work(S0 state)
1D8V_S3= 1.8 Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF_S3= 0.9 Voltage suspend to RAM(S3 state)
0D9V_S0= 0.9 Voltage power up on system work(S0 state)
1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

10,34,35,36,37 1D05V_S0 — 1D05V_S0
4,5,6,7,9,10,15,17,19,32,37 VCCP_GMCH_S0 — VCCP_GMCH_S0
6,9,10,37 CORE_GMCH_S0 — CORE_GMCH_S0
12,35,36 0D9V_S0 — 0D9V_S0
7,11,35 DDR_VREF_S3 — DDR_VREF_S3
5,7,9,16,17,20,36,37 1D5V_S0 — 1D5V_S0
17,34,35,36 1D5V_S3 — 1D5V_S3
5 1D5V_VCCA_S0 — 1D5V_VCCA_S0
5,32,36 VCC_CORE_S0 — VCC_CORE_S0
7,9,10,11,12,16,34,35,36,37 1D8V_S3 — 1D8V_S3
7,9,14,17,34,36 2D5V_S0 — 2D5V_S0
9 2D5V_CRTDAC_S0 — 2D5V_CRTDAC_S0
13 3D3V_LCD_S0 — 3D3V_LCD_S0
3,4,5,7,9,11,13,15,16,17,18,19,20,23,24,25,27,29,32,34,36,37 3D3V_S0 — 3D3V_S0
16,17,18,19,20,25,26,33,37 3D3V_S3 — 3D3V_S3
4,13,16,19,27,28,29,30,31,32,33,34,35,36 3D3V_S5 — 3D3V_S5
21,22,36,37 3D3V_LAN_S5 — 3D3V_LAN_S5
33,36 +3V_SRC — +3V_SRC
15,19,28,33,36 +3D3VRTC — +3D3VRTC
15,17 RTC_AUX_S5 — RTC_AUX_S5
23 VDDA — VDDA
13,14,17,18,19,20,24,25,27,28,32,35,36,37 5V_S0 — 5V_S0
13,17,19,23,24,26,33,34,35,36,37 5V_S3 — 5V_S3
13,32,33,34,36 5V_S5 — 5V_S5
14 5V_CRT_S0 — 5V_CRT_S0
13,19,33,36,37 +15V — +15V
13,31,33,34,35,36,37 DCBATOUT — DCBATOUT
30,31,37 BT+ — BT+
30,31,37 AD+ — AD+



Device	SMBus addr.
Clock Gen.	D2
DDR Module 1	A0
DDR Module 2	A4
LCD	58
Guardian	5E
Battery	16
EEPROM	A2

USB Port	Key West Define
USBP[0]	USB1 Up connector
USBP[1]	New card used
USBP[2]	USB1 Down connector
USBP[3]	NC
USBP[4]	USB2 connector
USBP[5]	NC
USBP[6]	NC
USBP[7]	NC

PCIE Port	Key West Define
PE[1]	NC
PE[2]	NC
PE[3]	NC
PE[4]	New card used

SB

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ#/GNT#
Mini-PCI	AD19	P_INTB# / P_INTD#	REQ3#/GNT3#
LAN	AD16	P_INTC#	REQ4#/GNT4#

SB

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Title: ITP
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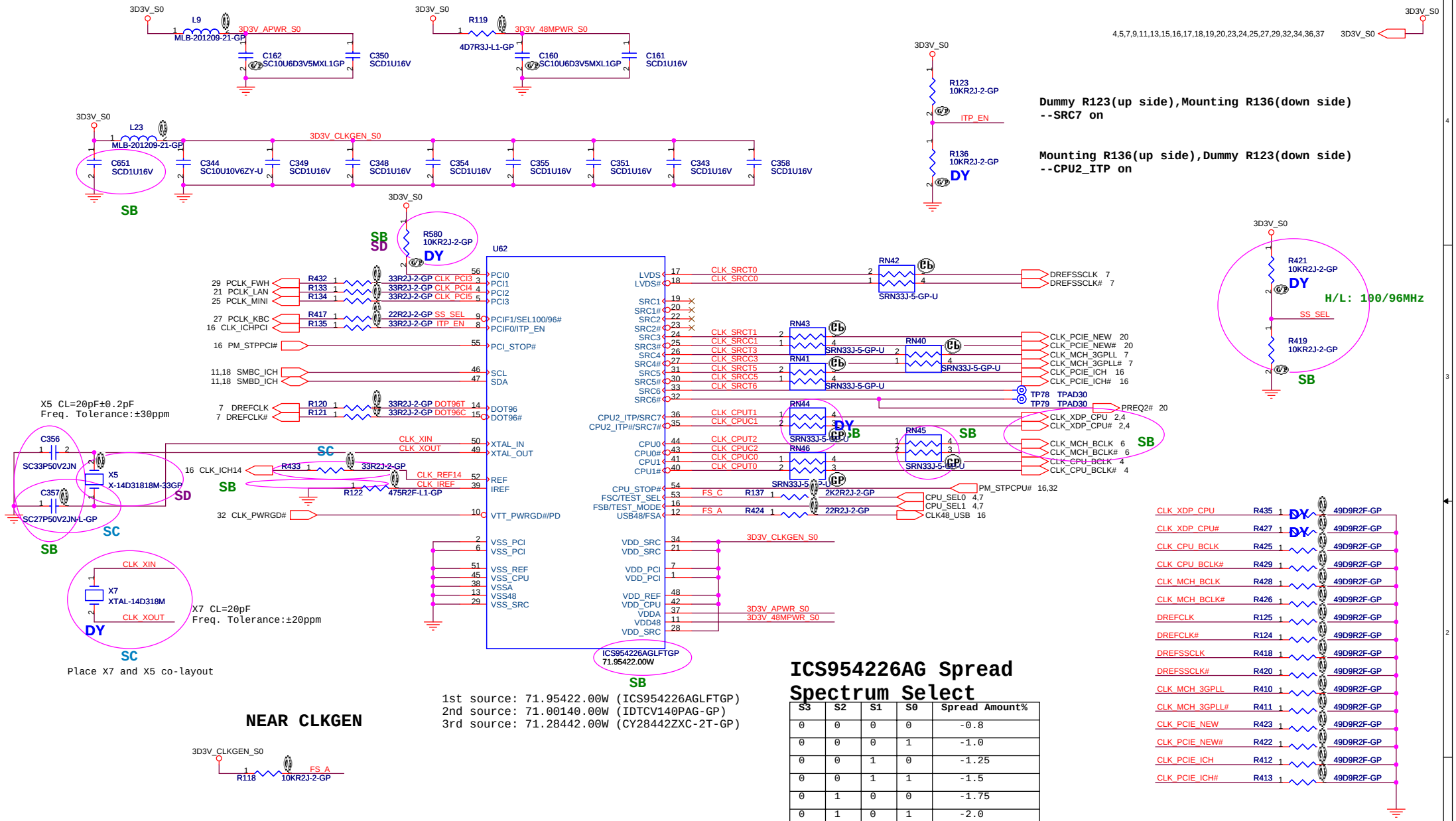

NEAR CLKGEN

1st source: 71.95422.00W (ICS954226AGLFTGP)
2nd source: 71.00140.00W (IDTCV140PAG-GP)
3rd source: 71.28442.00W (CY28442ZXC-2T-GP)

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

ICS954226AG Spread Spectrum Select

S3	S2	S1	S0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+/-0.3
1	0	0	1	+/-0.4
1	0	1	0	+/-0.5
1	0	1	1	+/-0.6
1	1	0	0	+/-0.8
1	1	0	1	+/-1.0
1	1	1	0	+/-1.25
1	1	1	1	+/-1.5

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator (ICS954226AG)

Size: A3 | Document Number: KeyWest | Rev: SD

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VCCP_GMCH_S0

2,5,6,7,9,10,15,17,19,32,37 VCCP_GMCH_S0

6 H_A#[31..3]

U46A 62.10055.011

ADDR GROUP 0 / CONTROL

H_A#3	P4	A3#	
H_A#4	U4	A4#	
H_A#5	V3	A5#	
H_A#6	R3	A6#	
H_A#7	V2	A7#	
H_A#8	W1	A8#	
H_A#9	T4	A9#	
H_A#10	W2	A10#	
H_A#11	Y4	A11#	
H_A#12	Y1	A12#	
H_A#13	U1	A13#	
H_A#14	AA3	A14#	
H_A#15	Y3	A15#	
H_A#16	AA2	A16#	
	U3	ADSTB#0	

6 H_ADSTB#0
6 H_REQ#[4..0]

H_REQ#0	R2	REQ0#	
H_REQ#1	P3	REQ1#	
H_REQ#2	T2	REQ2#	
H_REQ#3	P1	REQ3#	
H_REQ#4	T1	REQ4#	

ADDR GROUP 1 / XTP/ITP SIGNALS

H_A#17	AE4	A17#	
H_A#18	AC4	A18#	
H_A#19	AC7	A19#	
H_A#20	AC3	A20#	
H_A#21	AD3	A21#	
H_A#22	AE4	A22#	
H_A#23	AD2	A23#	
H_A#24	AB4	A24#	
H_A#25	AC6	A25#	
H_A#26	AD5	A26#	
H_A#27	AE2	A27#	
H_A#28	AD6	A28#	
H_A#29	AF3	A29#	
H_A#30	AE1	A30#	
H_A#31	AE1	A31#	
	AE5	ADSTB#1	

6 H_ADSTB#1

15 H_A20M#	C2	A20M#	
15 H_FERR#	D3	FERR#	
15 H_IGNNE#	A3	IGNNE#	

HCLK / THERM

15 H_STPCLK#	C6	STPCLK#	
15 H_INTR	D1	LINT0	
15 H_NMI	D4	LINT1	
15 H_SMI#	B4	SMI#	

	N2	ADS#	H_ADS# 6
	L1	BNR#	H_BNR# 6
	J3	BPRI#	H_BPRI# 6
	L4	DEFER#	H_DEFER# 6
	H2	DRDY#	H_DRDY# 6
	M2	DBSY#	H_DBSY# 6
	N4	BR0#	H_BREQ#0 6
H_IERR#	A4	IERR#	
	B5	INIT#	H_INIT# 15
	J2	LOCK#	H_LOCK# 6
	B11	RESET#	H_CPURST# 2,6
H_RS#0	H1	RS0#	H_RS#[2..0] 6
H_RS#1	K1	RS1#	
H_RS#2	L2	RS2#	
	M3	TRDY#	H_TRDY# 6
	K3	HIT#	H_HIT# 6
	K4	HITM#	H_HITM# 6

	C8	BPM#0	XDP_BPM#0 2
	B8	BPM#1	XDP_BPM#1 2
	A9	BPM#2	XDP_BPM#2 2
	C9	BPM#3	XDP_BPM#3 2
	A10	PRDY#	XDP_PRDY# 2
XDP_BPM#5	B10	PREQ#	XDP_BPM#5 2
XDP_TCK	A13	TCK	XDP_TCK 2
XDP_TDI	C12	TDI	XDP_TDI 2
XDP_TDO	A12	TDO	XDP_TDO 2
XDP_TMS	C11	TMS	XDP_TMS 2
XDP_TRST#	B13	TRST#	XDP_TRST# 2
DBR#	A7	DBR#	DBR# 2,16

CPU_PROCHOT#	B17	PROCHOT#	
	B18	THERMDA	THERMDP1 19
	A18	THERMDC	THERMDN 19
	C17	THERMTRIP#	PM_THRMTRIP-A# 19
	A15	ITP_CLK1	CLK_XDP_CPU# 2,3
	A16	ITP_CLK0	CLK_XDP_CPU 2,3
	B14	BCLK1	CLK_CPU_BCLK# 3
	B15	BCLK0	CLK_CPU_BCLK 3

PZ47903

R274 56R2J-4-GP

Place testpoint on H_IERR# with a GND 0.1" away

PM_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)

SB

1st source:62.10079.001
2nd source:62.10053.341

U46B 62.10055.011

H_D#[63..0] 6

DATA GRP 0 / DATA GRP 2

H_D#0	A19	D0#	
H_D#1	A25	D1#	
H_D#2	A22	D2#	
H_D#3	B21	D3#	
H_D#4	A24	D4#	
H_D#5	B26	D5#	
H_D#6	A21	D6#	
H_D#7	B20	D7#	
H_D#8	C20	D8#	
H_D#9	B24	D9#	
H_D#10	D24	D10#	
H_D#11	E24	D11#	
H_D#12	C26	D12#	
H_D#13	B23	D13#	
H_D#14	E23	D14#	
H_D#15	C25	D15#	
	Y26	D32#	H_D#32
	AA24	D33#	H_D#33
	T25	D34#	H_D#34
	U23	D35#	H_D#35
	V23	D36#	H_D#36
	R24	D37#	H_D#37
	R26	D38#	H_D#38
	R23	D39#	H_D#39
	AA23	D40#	H_D#40
	U26	D41#	H_D#41
	V24	D42#	H_D#42
	U25	D43#	H_D#43
	V26	D44#	H_D#44
	Y23	D45#	H_D#45
	AA26	D46#	H_D#46
	Y25	D47#	H_D#47

6 H_DSTBN#0
6 H_DSTBP#0
6 H_DINV#0

	C23	DSTBN0#	
	C22	DSTBP0#	
	D25	DINV0#	
	W25	DSTBN2#	H_DSTBN#2 6
	W24	DSTBP2#	H_DSTBP#2 6
	T24	DINV2#	H_DINV#2 6

DATA GRP 1 / DATA GRP 3

H_D#16	H23	D16#	
H_D#17	G25	D17#	
H_D#18	L23	D18#	
H_D#19	M26	D19#	
H_D#20	H24	D20#	
H_D#21	E25	D21#	
H_D#22	G24	D22#	
H_D#23	J23	D23#	
H_D#24	M23	D24#	
H_D#25	J25	D25#	
H_D#26	L26	D26#	
H_D#27	N24	D27#	
H_D#28	M25	D28#	
H_D#29	H26	D29#	
H_D#30	N25	D30#	
H_D#31	K25	D31#	
	AB25	D48#	H_D#48
	AC23	D49#	H_D#49
	AB24	D50#	H_D#50
	AC20	D51#	H_D#51
	AC22	D52#	H_D#52
	AC25	D53#	H_D#53
	AD23	D54#	H_D#54
	AE22	D55#	H_D#55
	AF23	D56#	H_D#56
	AD24	D57#	H_D#57
	AE20	D58#	H_D#58
	AE21	D59#	H_D#59
	AD21	D60#	H_D#60
	AF25	D61#	H_D#61
	AF22	D62#	H_D#62
	AF26	D63#	H_D#63

6 H_DSTBN#1
6 H_DSTBP#1
6 H_DINV#1

	K24	DSTBN1#	
	L24	DSTBP1#	
	J26	DINV1#	
	AE24	DSTBN3#	H_DSTBN#3 6
	AE25	DSTBP3#	H_DSTBP#3 6
	AD20	DINV3#	H_DINV#3 6

MISC

PSI#	E1	PSI#	
	P25	COMP0	R286 1 27D4R2F-L1-GP VCCP_GMCH_S0
	P26	COMP1	R287 1 54D9R2F-L1-GP
	AB2	COMP2	R40 1 27D4R2F-L1-GP
	AB1	COMP3	R39 1 54D9R2F-L1-GP
	C16	BSEL0	
	C14	BSEL1	
	G1	RSVD2	DPRSTP# H_DPRSLP# 15
	B7	RSVD3	DPSLP# H_DPSLP# 15
	C19	RSVD4	DPWR# H_DPWR# 6
	E4	RSVD5	PWRGOOD H_PWRGD 15
	A6	GTLREF0	SLP# H_CPUSLP# 6,15
	C5	TEST1	
	F23	TEST2	
	AD26	GTLREF	

PZ47903

R272 200R2F-L-GP

3,7 CPU_SEL0
3,7 CPU_SEL1

R256 1 0R2J-GP CPU_SEL0_CPU
R257 1 0R2J-GP CPU_SEL1_CPU

SD

Only support 400MHz (GML)

TPAD30 TP3

TPAD30 TP1
TPAD30 TP5
TPAD30 TP6
TPAD30 TP60

CPU_TP3 C3
CPU_TP4 AE7
CPU_TP5 AC1
CPU_TP6 E26

VCCP_GMCH_S0 R37 1 1KR2F-3-GP

R38 2KR2F-3-GP

Layout Note: 0.5" max length.

BSEL[1:0]	Freq.(MHz)
L H	100
L L	133

R31 1KR2J-1-GP DY

R268 1KR2J-1-GP DY

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .

CPU

TCK(PIN A13)

ITP Conn.

TCK(PIN 5)

FBO(PIN 11)

VCCP_GMCH_S0 R608 56R2J-4-GP

PM_THRMTRIP-A#

SB

VCCP_GMCH_S0

H_CPURST#	R267	54D9R2F-L1-GP	SB
XDP_TDO	R260	54D9R2F-L1-GP	DY
CPU_PROCHOT#	R258	56R2J-4-GP	
XDP_TDI	R261	150R2F-1-GP	
XDP_TMS	R263	39D2R2F-L-GP	
XDP_TRST#	R259	680R2J-3-GP	
XDP_TCK	R262	27D4R2F-L1-GP	

3D3V_S0 R532 150R2F-1-GP DBR#

SB

VCCP_GMCH_S0 R513 56R2J-4-GP DY

3D3V_S5 R514 330R2J-3-GP

CPU_PROCHOT# Q54 MMBT3904LT1-2-GP DY

PROCHOT# 27

SB

All place within 2" to CPU

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (1 of 2)

Size	Document Number	Rev
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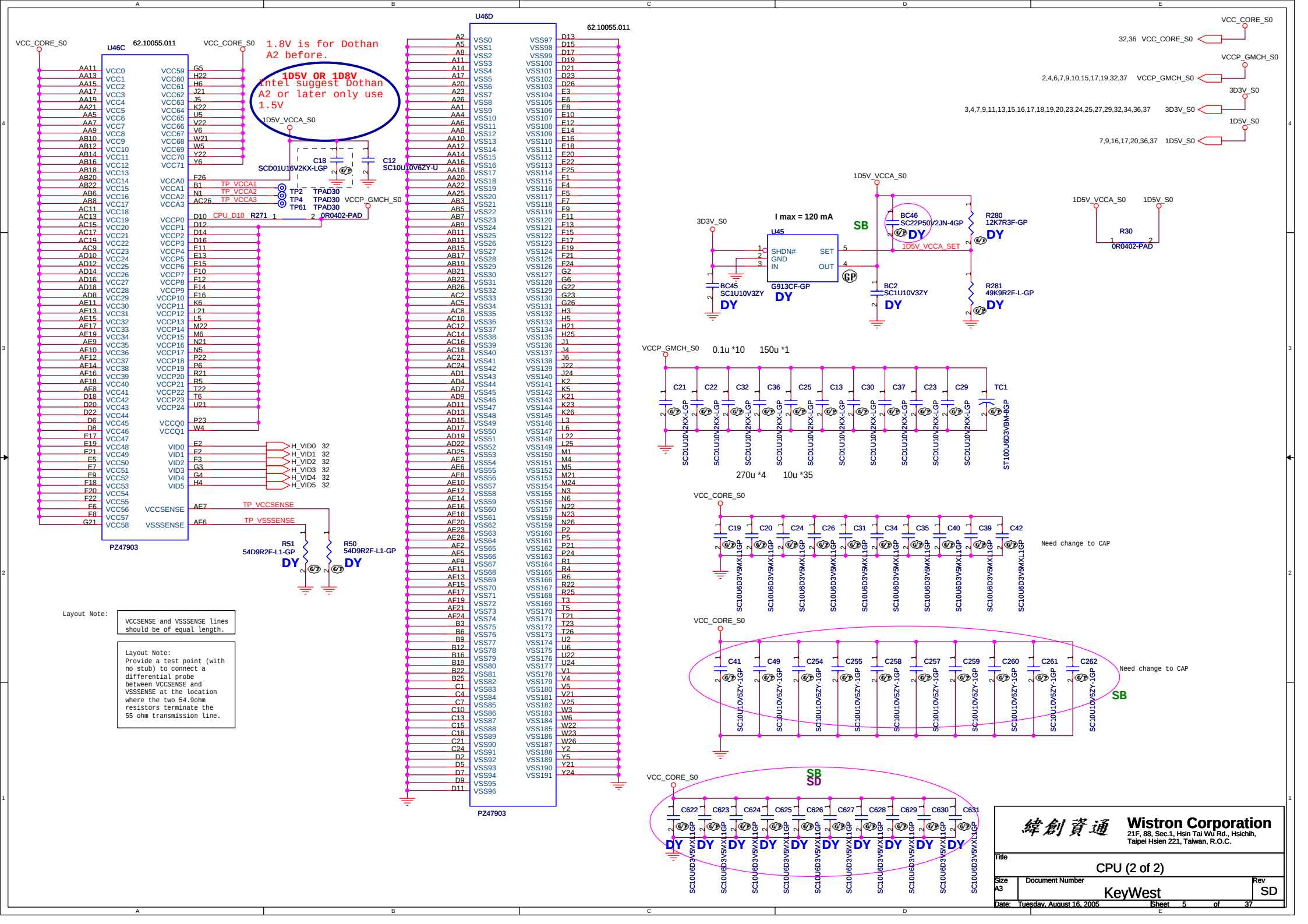
U46C
62.10055.011
PZ47903
VCC_CORE_S0
1.8V is for Dothan A2 before.
1D5V OR 1D8V
Intel suggest Dothan A2 or later only use 1.5V
1D5V_VCCA_S0
SCD01U16V2KX-LGP
C18
C12
SC10U10V6ZY-U
TP_VCCA1
TP_VCCA2
TP_VCCA3
TP2
TP4
TP61
TPAD30
0R0402-PAD
VCCP_GMCH_S0
CPU_D10
R271
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
TP_VCCSENSE
TP_VSSSENSE
R51
R50
54D9R2F-L1-GP
DY
U46D
62.10055.011
PZ47903
3D3V_S0
I max = 120 mA
U45
SHDN#
GND
IN
SET
OUT
G913CF-GP
BC45
SC1U10V3ZY
BC46
SC22P50V2JN-4GP
BC2
R280
12K7R3F-GP
R281
49K9R2F-L-GP
1D5V_VCCA_SET
SB
1D5V_S0
R30
0R0402-PAD
VCCP_GMCH_S0
0.1u *10
150u *1
270u *4
10u *35
C21
C22
C32
C36
C25
C13
C30
C37
C23
C29
TC1
SCD1U10V2KX-LGP
ST100U6D3VBM-8GP
Need change to CAP
SC10U6D3V5MXL1GP
C19
C20
C24
C26
C31
C34
C35
C40
C39
C42
C41
C49
C254
C255
C258
C257
C259
C260
C261
C262
SC10U10V5ZY-1GP
C622
C623
C624
C625
C626
C627
C628
C629
C630
C631
SD
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
32,36 VCC_CORE_S0
2,4,6,7,9,10,15,17,19,32,37 VCCP_GMCH_S0
3,4,7,9,11,13,15,16,17,18,19,20,23,24,25,27,29,32,34,36,37 3D3V_S0
7,9,16,17,20,36,37 1D5V_S0
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (2 of 2)
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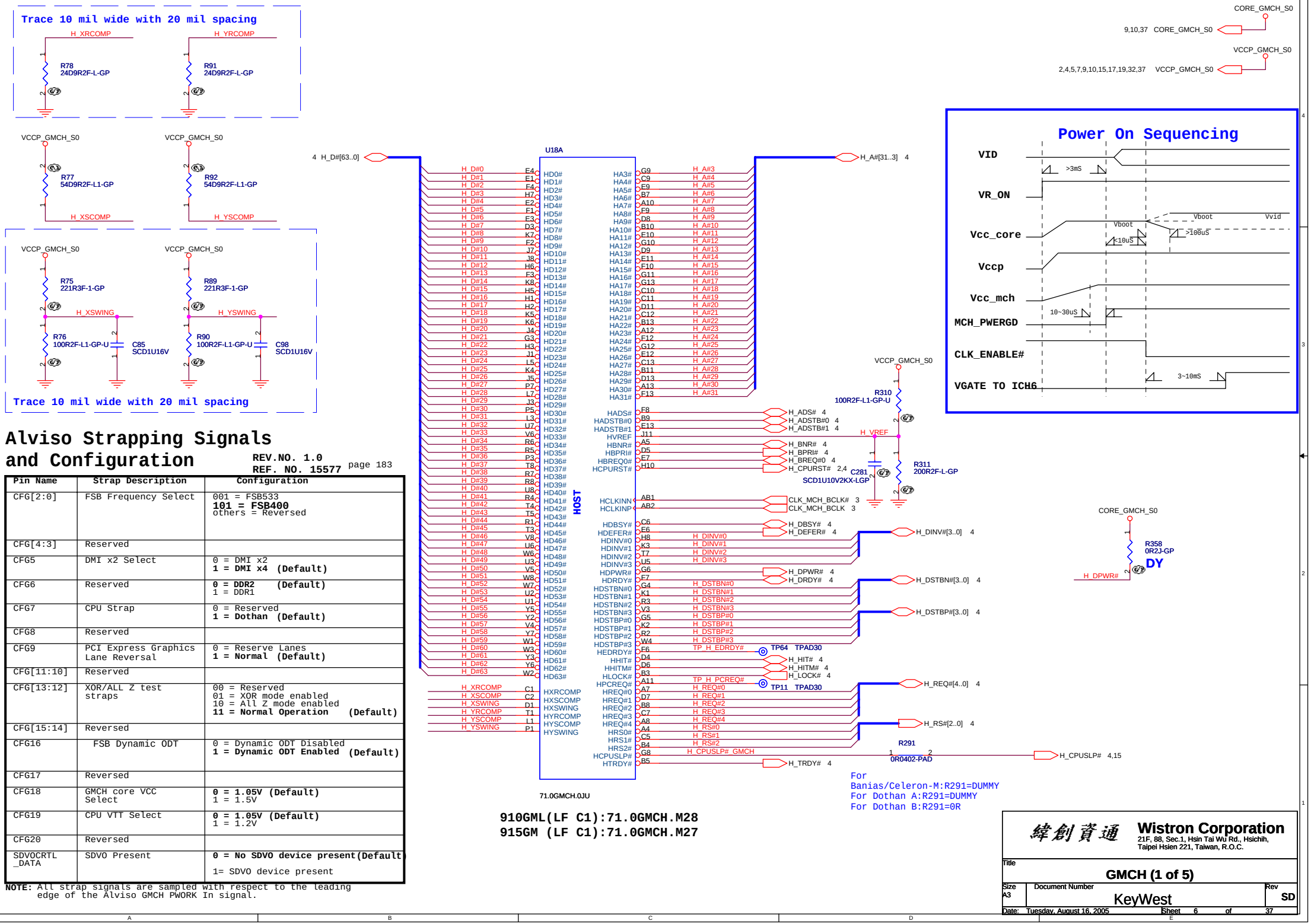

Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 **101 = FSB400** others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	Reserved	**0 = DDR2 (Default)** 1 = DDR1
CFG7	CPU Strap	0 = Reserved **1 = Dothan (Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes **1 = Normal (Default)**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation (Default)**
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Reversed	
CFG18	GMCH core VCC Select	**0 = 1.05V (Default)** 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V (Default)** 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present(Default)** 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

緯創資通 Wistron Corporation
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Title: GMCH (1 of 5)

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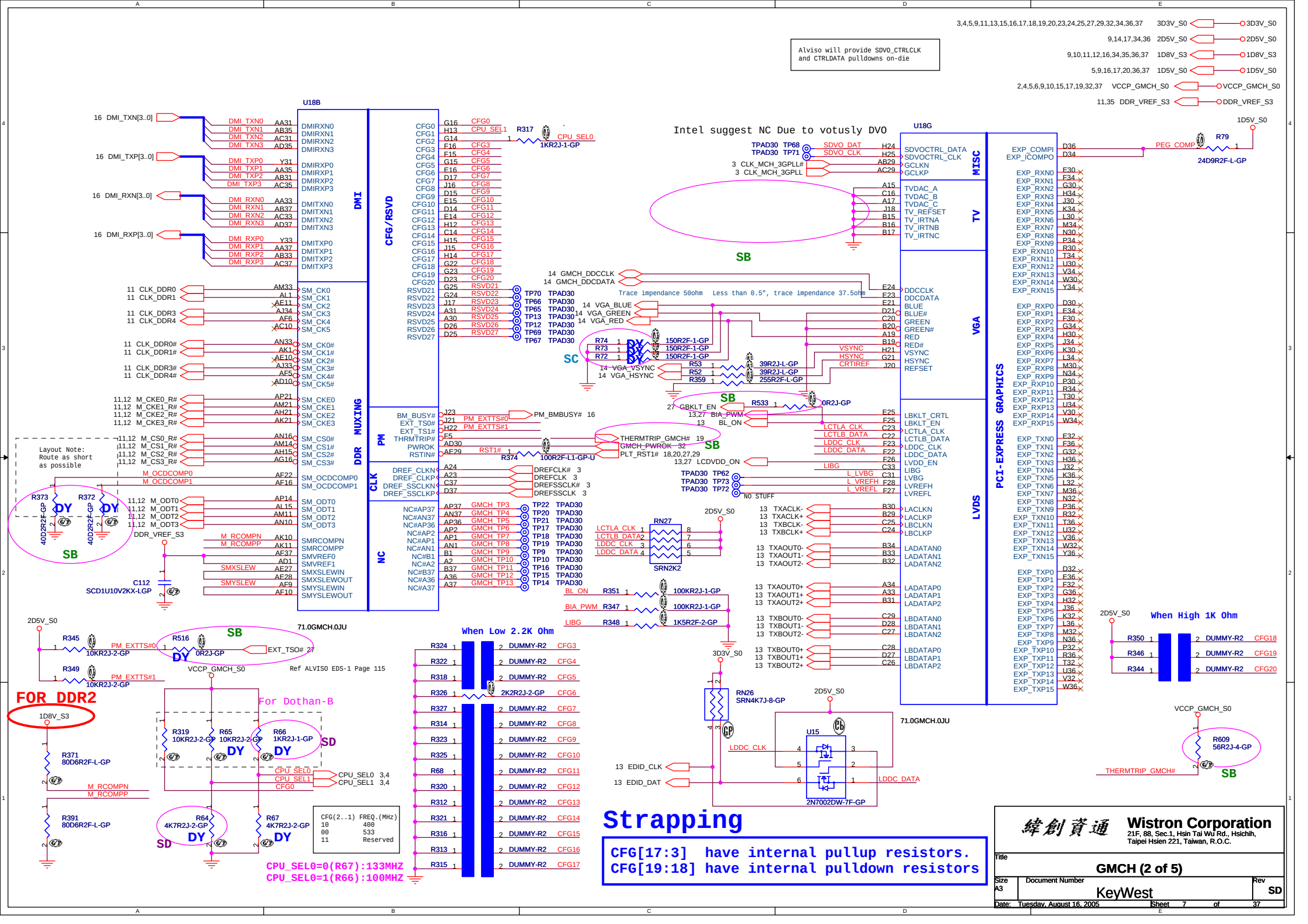
U18B
DMI
CFG/RSVD
DDR MUXING
PM
CLK
NC
U18G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
Intel suggest NC Due to votusly DVO
Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die
Layout Note: Route as short as possible
FOR DDR2
For Dothan-B
When Low 2.2K Ohm
When High 1K Ohm
Strapping
CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors
CPU_SEL0=0(R67):133MHZ
CPU_SEL0=1(R66):100MHZ
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GMCH (2 of 5)
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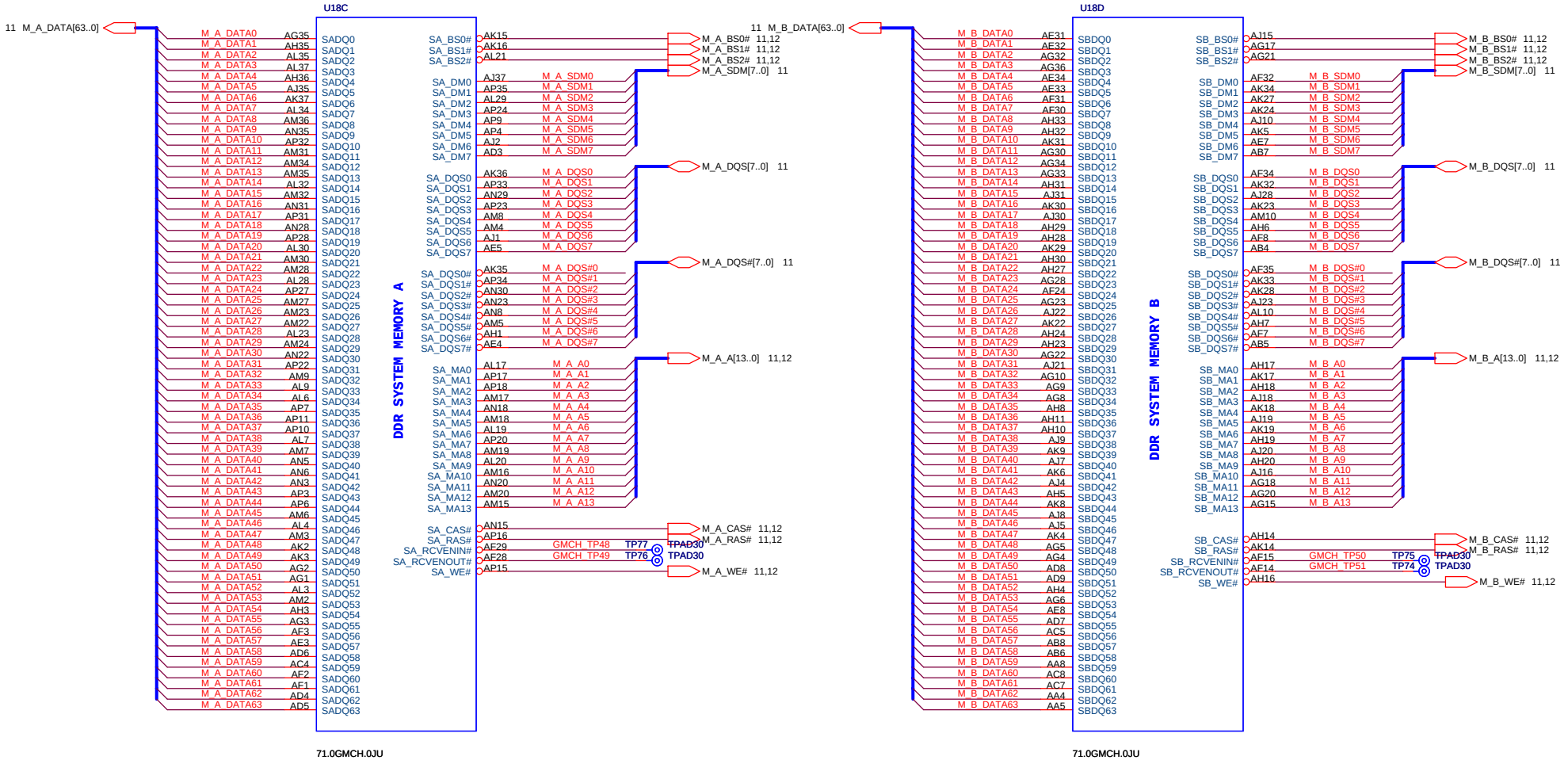
SUPPORT DDRII 400



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (3 of 5)

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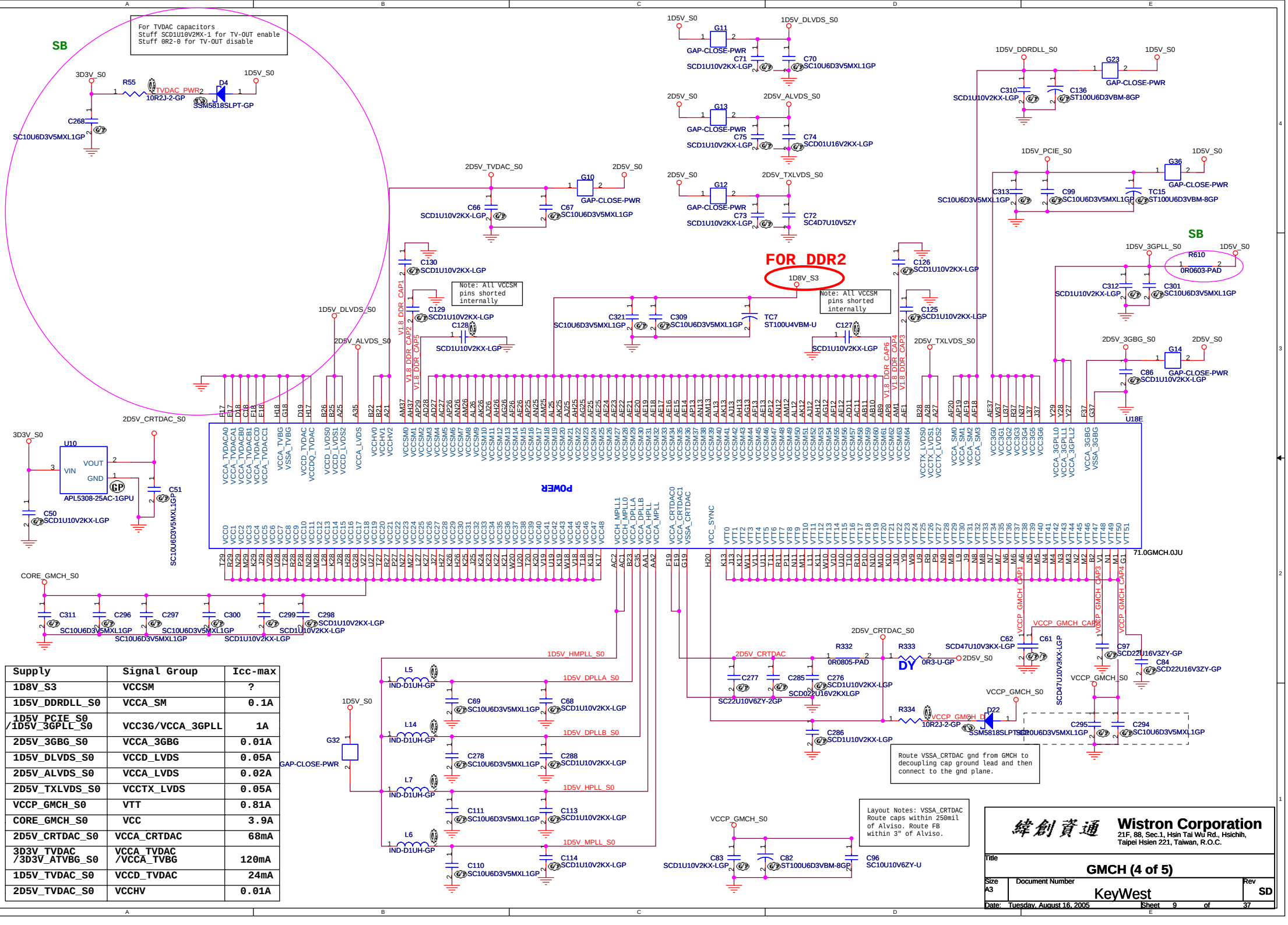

Supply	Signal Group	Icc-max
1D8V_S3	VCCSM	?
1D5V_DDRDLL_S0	VCCA_SM	0.1A
1D5V_PCIE_S0 /1D5V_3GPLL_S0	VCC3G/VCCA_3GPLL	1A
2D5V_3GBG_S0	VCCA_3GBG	0.01A
1D5V_DLVDS_S0	VCCD_LVDS	0.05A
2D5V_ALVDS_S0	VCCA_LVDS	0.02A
2D5V_TXLVDS_S0	VCCTX_LVDS	0.05A
VCCP_GMCH_S0	VTT	0.81A
CORE_GMCH_S0	VCC	3.9A
2D5V_CRTDAC_S0	VCCA_CRTDAC	68mA
3D3V_TVDAC /3D3V_ATVBG_S0	VCCA_TVDAC /VCCA_TVBG	120mA
1D5V_TVDAC_S0	VCCD_TVDAC	24mA
2D5V_TVDAC_S0	VCCHV	0.01A

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Title: GMCH (4 of 5)

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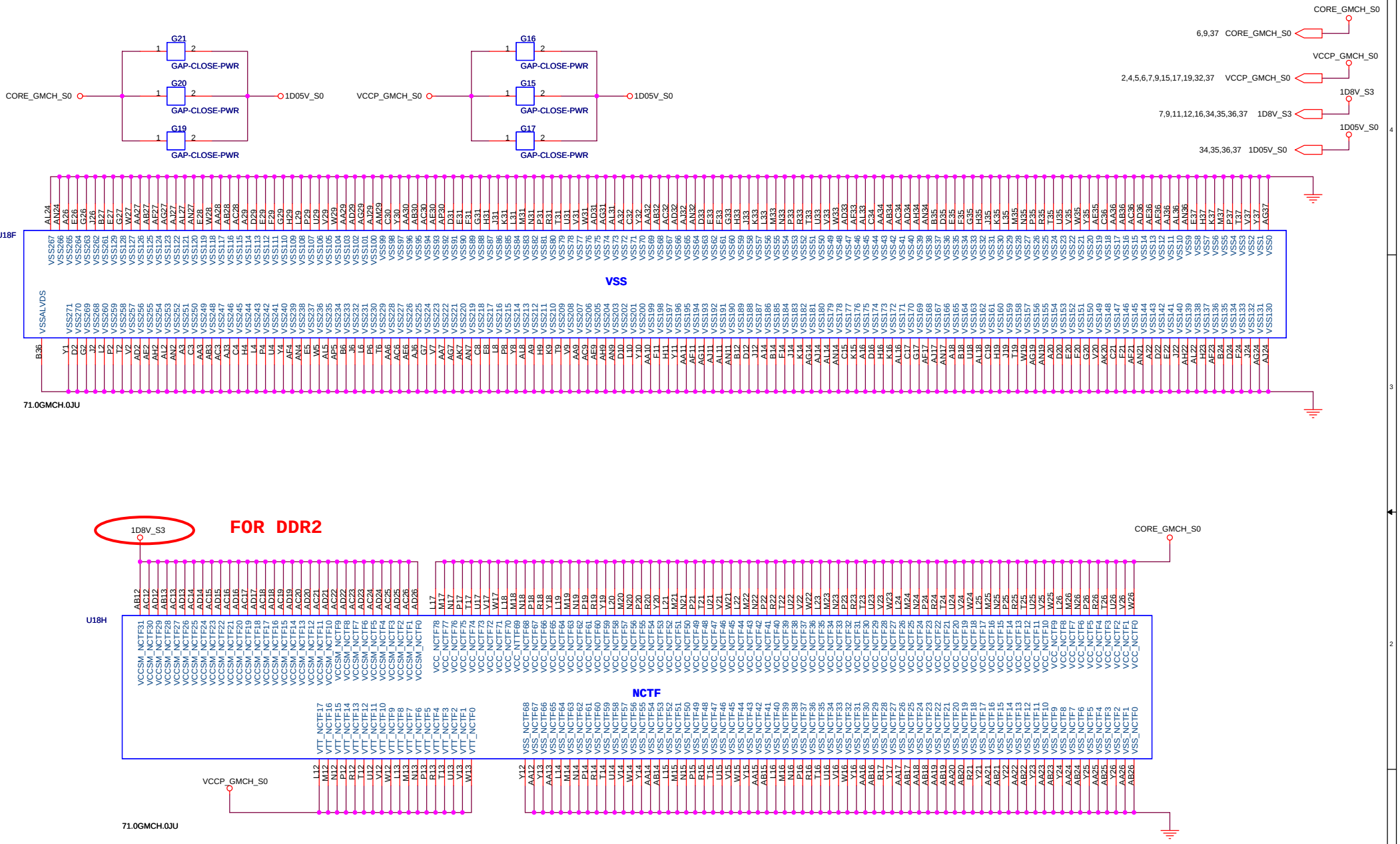

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	GMCH (5 of 5)	
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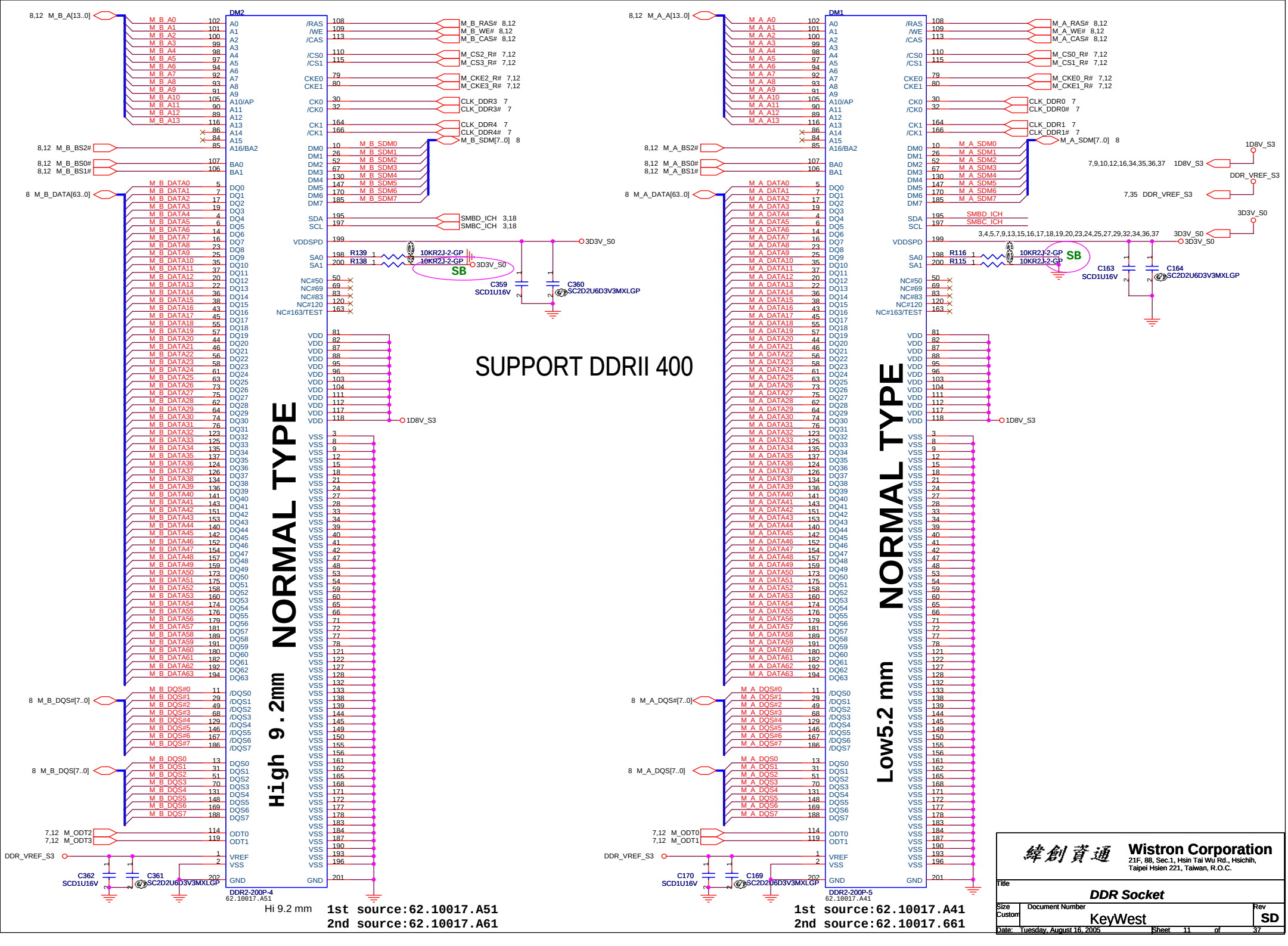
DM2
DDR2-200P-4
62.10017.A51
High 9.2mm NORMAL TYPE
Hi 9.2 mm
1st source:62.10017.A51
2nd source:62.10017.A61
SUPPORT DDRII 400
DM1
DDR2-200P-5
62.10017.A41
Low5.2 mm NORMAL TYPE
1st source:62.10017.A41
2nd source:62.10017.661
SB
SB
10KR2J-2-GP
C359 SCD1U16V
C360 SC2D2U6D3V3MXLGP
C361 SC2D2U6D3V3MXLGP
C362 SCD1U16V
C163 SCD1U16V
C164 SC2D2U6D3V3MXLGP
C169 SC2D2U6D3V3MXLGP
C170 SCD1U16V
3D3V_S0
1D8V_S3
DDR_VREF_S3
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Title
DDR Socket
Size Custom
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PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN

1D8V_S3

C152 SCD1U16V
C150 SCD1U16V
C151 SCD1U16V
C149 SCD1U16V
C183 SCD1U16V
C178 SCD1U16V
C168 SCD1U16V
C166 SCD1U16V

C167 SCD1U16V
C179 SCD1U16V
C180 SCD1U16V
C165 SCD1U16V
C184 SCD1U16V
C182 SCD1U16V
C181 SCD1U16V
C177 SCD1U16V

C176 SCD1U16V
C153 SC10U6D3V5MX-1GP
C185 SC10U6D3V5MX-1GP
EC30 SCD1U16V
EC38 SCD1U16V
EC23 SCD1U16V
EC24 SCD1U16V

Address / CommandControl

0D9V_S0

8,11 M_A_A1
8,11 M_A_A0
RN32 SRN56J-4-GP
C198 SCD1U16V
8,11 M_A_A3
8,11 M_A_A10
RN34 SRN56J-4-GP
C197 SCD1U16V

8,11 M_B_CAS#
8,11 M_B_RAS#
RN5 SRN56J-4-GP
C196 SCD1U16V
8,11 M_B_WE#
7,11 M_CS3_R#
RN7 SRN56J-4-GP
C195 SCD1U16V

8,11 M_A_A7
8,11 M_A_A6
RN35 SRN56J-4-GP
C191 SCD1U16V
8,11 M_A_A4
8,11 M_A_A2
RN33 SRN56J-4-GP
C194 SCD1U16V

8,11 M_B_BS0#
8,11 M_B_A2
RN8 SRN56J-4-GP
C193 SCD1U16V
8,11 M_B_A10
8,11 M_B_A4
RN9 SRN56J-4-GP
C192 SCD1U16V

7,11 M_CKE2_R#
8,11 M_B_A5
RN13 SRN56J-4-GP
C199 SCD1U16V
8,11 M_B_A11
8,11 M_B_A6
RN14 SRN56J-4-GP
C200 SCD1U16V

0D9V_S0

8,11 M_A_BS1#
8,11 M_A_RAS#
RN30 SRN56J-4-GP
C333 SCD1U16V
7,11 M_CS0_R#
8,11 M_A_A13
RN28 SRN56J-4-GP
C334 SCD1U16V

8,11 M_B_BS2#
8,11 M_B_A12
RN12 SRN56J-4-GP
C335 SCD1U16V
7,11 M_CKE3_R#
8,11 M_B_A7
RN15 SRN56J-4-GP
C336 SCD1U16V

7,11 M_CS2_R#
8,11 M_B_A13
RN4 SRN56J-4-GP
C337 SCD1U16V
8,11 M_B_A0
8,11 M_B_BS1#
RN6 SRN56J-4-GP
C338 SCD1U16V

8,11 M_A_WE#
8,11 M_A_BS0#
RN31 SRN56J-4-GP
C339 SCD1U16V
8,11 M_A_CAS#
7,11 M_CS1_R#
RN29 SRN56J-4-GP
C340 SCD1U16V

8,11 M_B_A3
8,11 M_B_A1
RN10 SRN56J-4-GP
C201 SCD1U16V
8,11 M_B_A9
8,11 M_B_A8
RN11 SRN56J-4-GP
C202 SCD1U16V

7,11 M_CKE0_R#
8,11 M_A_BS2#
RN39 SRN56J-4-GP
C330 SCD1U16V
8,11 M_A_A12
8,11 M_A_A9
RN38 SRN56J-4-GP
C331 SCD1U16V

7,11 M_CKE1_R#
8,11 M_A_A11
RN36 SRN56J-4-GP
C332 SCD1U16V
8,11 M_A_A8
8,11 M_A_A5
RN37 SRN56J-4-GP
C329 SCD1U16V

0D9V_S0

7,11 M_ODT0 R402 56R2J-4-GP
7,11 M_ODT1 R401 56R2J-4-GP
7,11 M_ODT2 R140 56R2J-4-GP
7,11 M_ODT3 R141 56R2J-4-GP

0D9V_S0
35,36 0D9V_S0

1D8V_S3
7,9,10,11,16,34,35,36,37 1D8V_S3

緯創資通 Wistron Corporation
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Title: DDR Serial/Terminator Resistor

Size	Document Number	Rev
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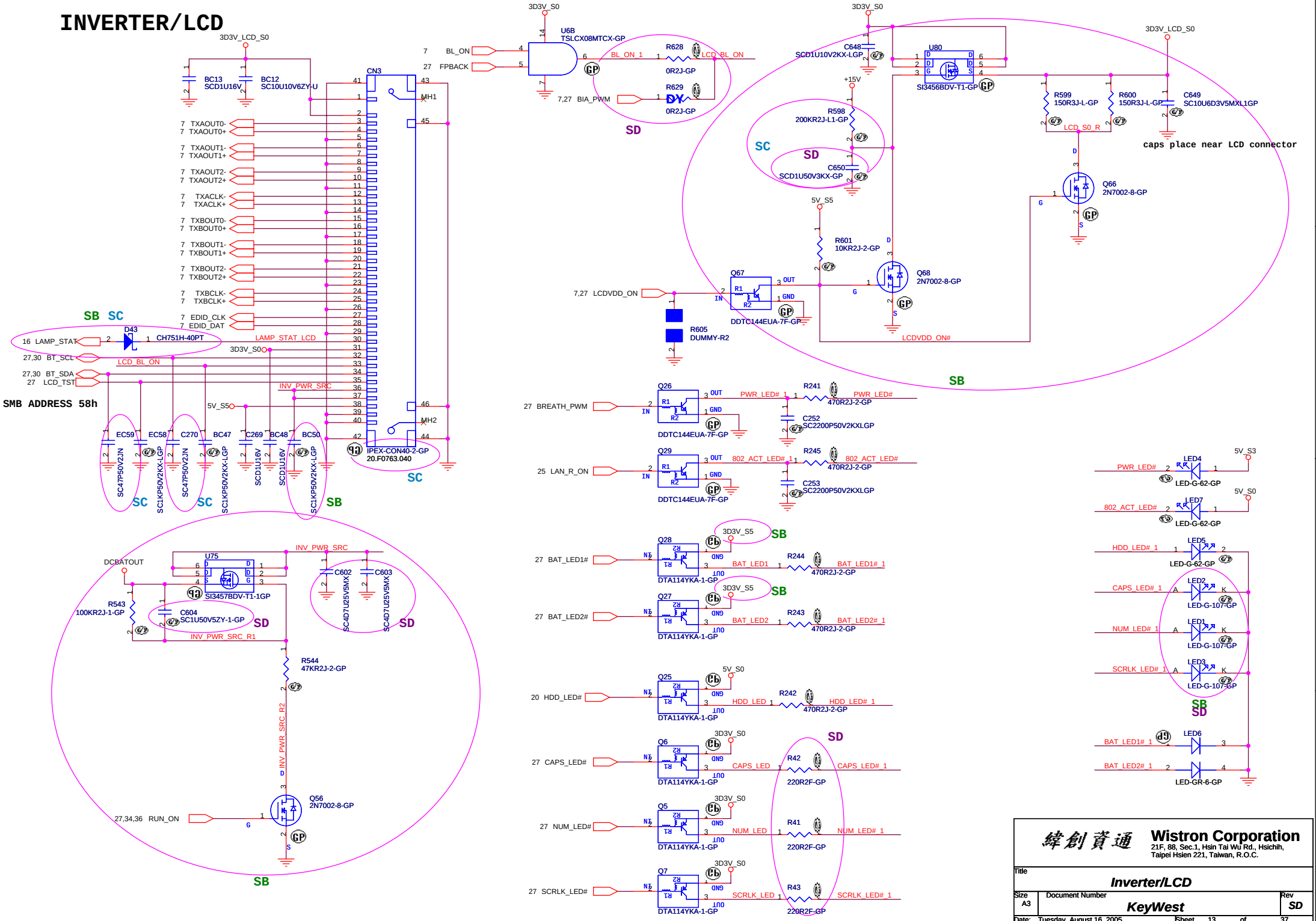
INVERTER/LCD



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Inverter/LCD*	
Size A3	Document Number *KeyWest*	Rev *SD*
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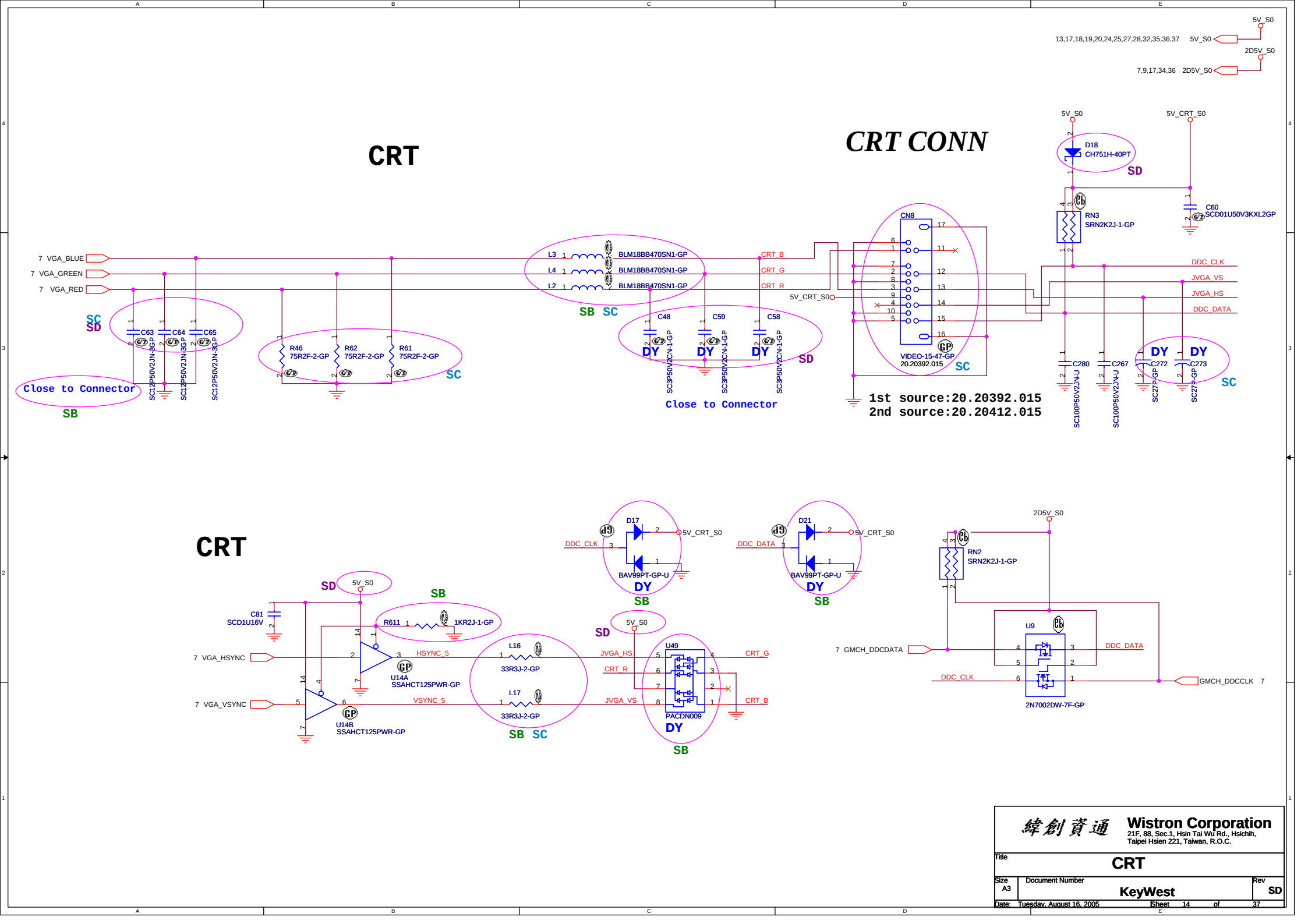
CRT
CRT CONN
CRT
7 VGA_BLUE
7 VGA_GREEN
7 VGA_RED
SC
SD
C63
C64
C65
SC12P50V2JN-3GP
Close to Connector
SB
R46
R62
R61
75R2F-2-GP
SC
L3
L4
L2
BLM18BB470SN1-GP
SB SC
CRT_B
CRT_G
CRT_R
C48
C59
C58
SC3P50V2CN-1-GP
DY
SD
Close to Connector
5V_CRT_S0
CN8
VIDEO-15-47-GP
20.20392.015
SC
1st source:20.20392.015
2nd source:20.20412.015
5V_S0
D18
CH751H-40PT
SD
5V_CRT_S0
RN3
SRN2K2J-1-GP
C60
SCD01U50V3KXL2GP
DDC_CLK
JVGA_VS
JVGA_HS
DDC_DATA
C280
C267
SC100P50V2JN-U
DY
C272
C273
SC27P-GP
SC
13,17,18,19,20,24,25,27,28,32,35,36,37 5V_S0
2D5V_S0
7,9,17,34,36 2D5V_S0
CRT
SD
5V_S0
SB
C81
SCD1U16V
R611
1KR2J-1-GP
7 VGA_HSYNC
HSYNC_5
U14A
SSAHCT125PWR-GP
7 VGA_VSYNC
VSYNC_5
U14B
SSAHCT125PWR-GP
L16
L17
33R3J-2-GP
SB SC
D17
BAV99PT-GP-U
DDC_CLK
5V_CRT_S0
DY
SB
D21
BAV99PT-GP-U
DDC_DATA
5V_CRT_S0
DY
SB
SD
5V_S0
JVGA_HS
CRT_R
JVGA_VS
U49
PACDN009
CRT_G
CRT_B
DY
SB
2D5V_S0
RN2
SRN2K2J-1-GP
U9
2N7002DW-7F-GP
7 GMCH_DDCDATA
DDC_DATA
DDC_CLK
GMCH_DDCCLK 7
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT
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A3
Document Number
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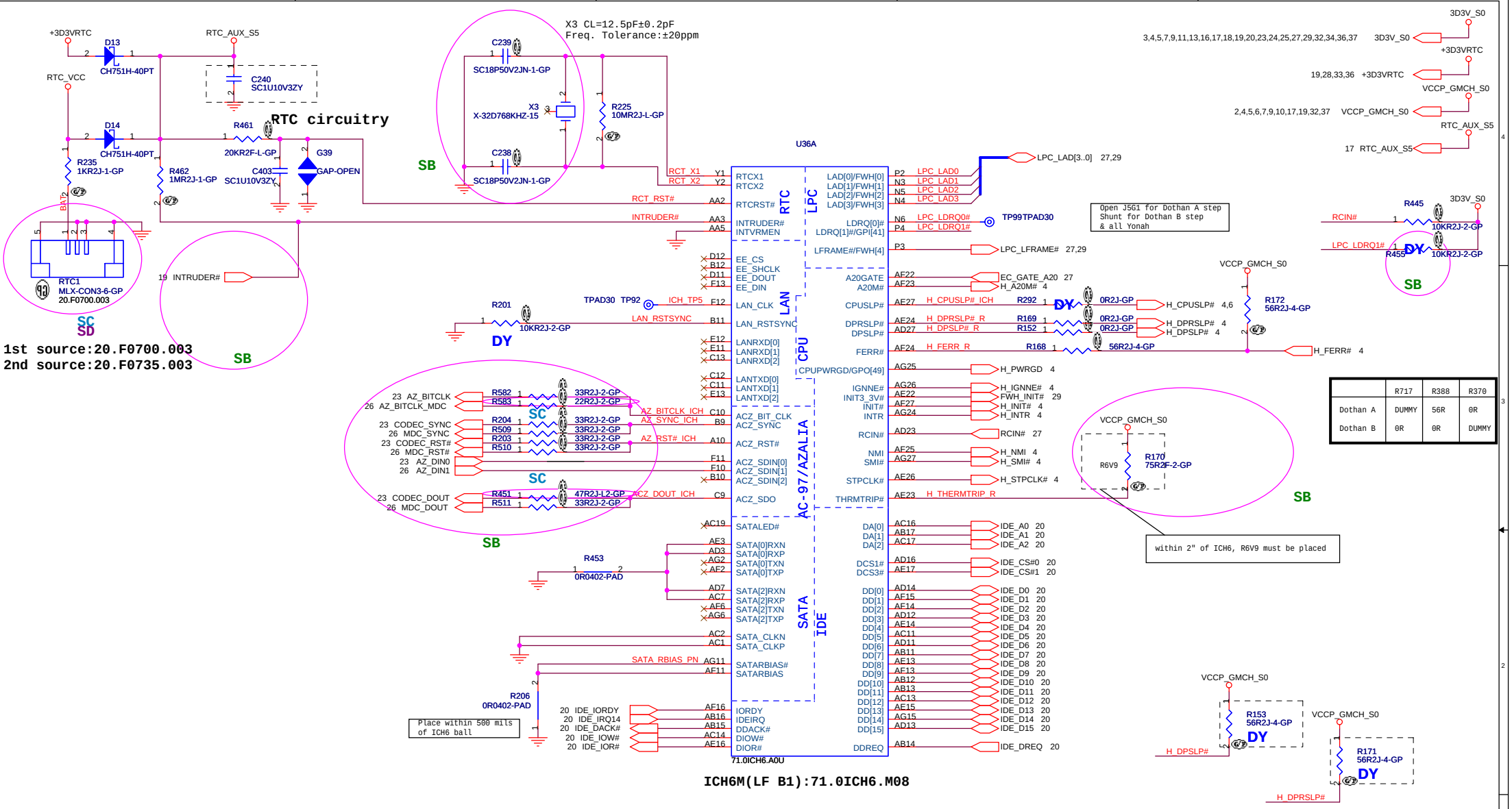
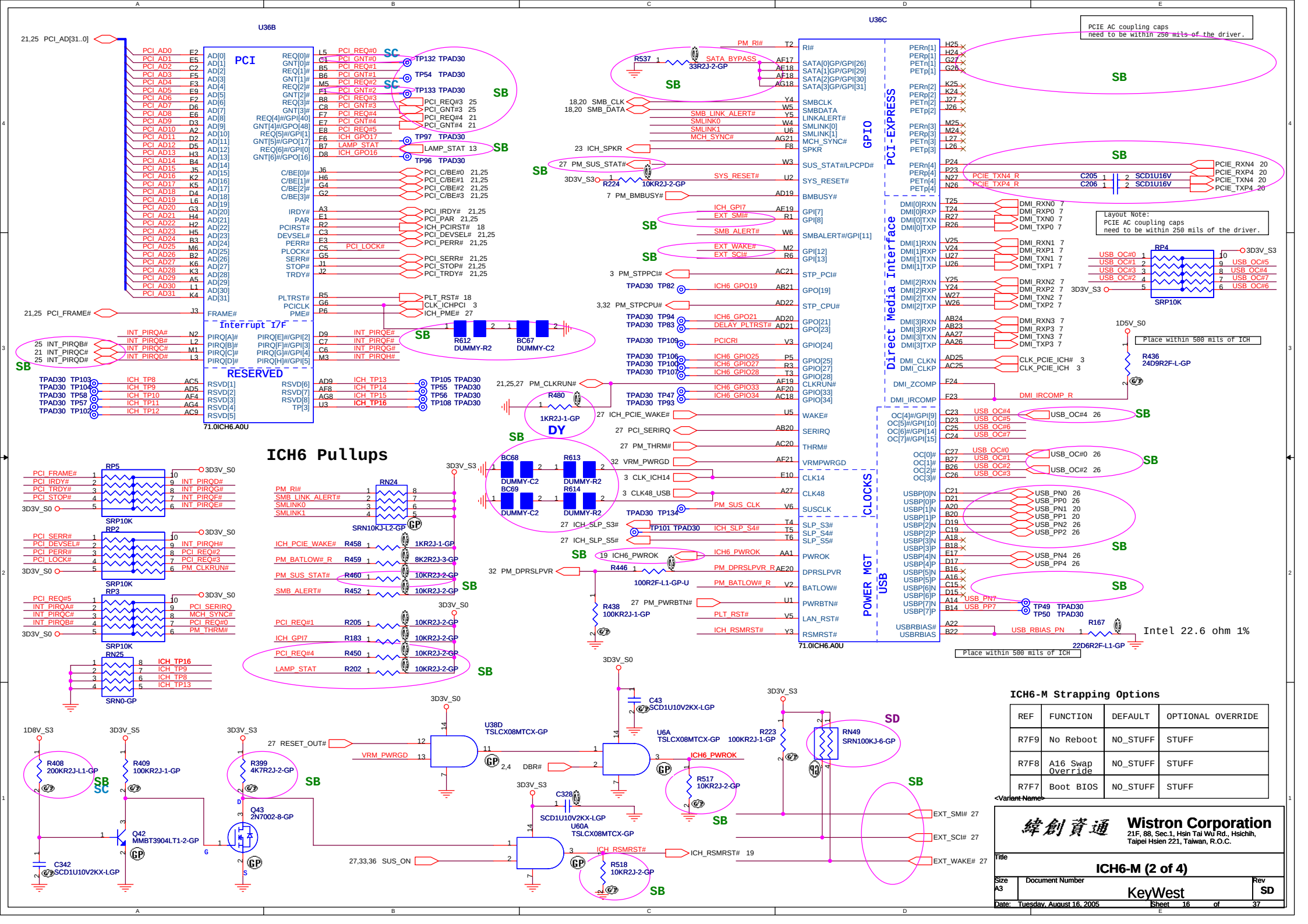


	R717	R388	R370
Dothan A	DUMMY	56R	0R
Dothan B	0R	0R	DUMMY


U36B
U36C
PCI
Interrupt I/F
RESERVED
GPIO
Direct Media Interface
PCI-EXPRESS
USB
CLOCKS
POWER MGT
ICH6 Pullups
SB
SC
DY
SD
PCIE AC coupling caps need to be within 250 mils of the driver.
Layout Note: PCIE AC coupling caps need to be within 250 mils of the driver.
Place within 500 mils of ICH
71.0ICH6.A0U
Intel 22.6 ohm 1%
ICH6-M Strapping Options
REF | FUNCTION | DEFAULT | OPTIONAL OVERRIDE
R7F9 | No Reboot | NO_STUFF | STUFF
R7F8 | A16 Swap Override | NO_STUFF | STUFF
R7F7 | Boot BIOS | NO_STUFF | STUFF
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (2 of 4)
Size A3
Document Number KeyWest
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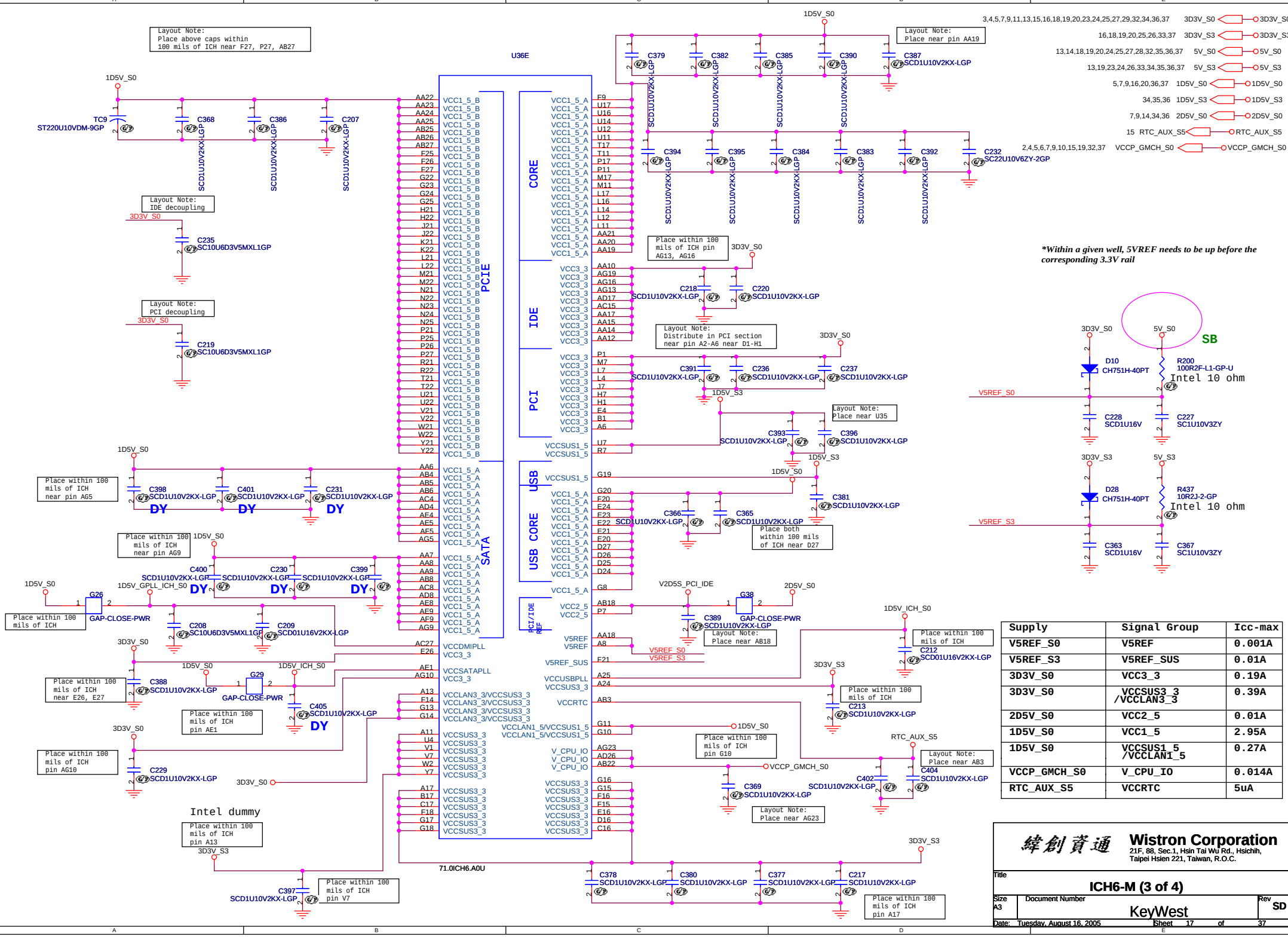

Supply	Signal Group	Icc-max
V5REF_S0	V5REF	0.001A
V5REF_S3	V5REF_SUS	0.01A
3D3V_S0	VCC3_3	0.19A
3D3V_S0	VCCSUS3_3 /VCCLAN3_3	0.39A
2D5V_S0	VCC2_5	0.01A
1D5V_S0	VCC1_5	2.95A
1D5V_S0	VCCSUS1_5 /VCCLAN1_5	0.27A
VCCP_GMCH_S0	V_CPU_IO	0.014A
RTC_AUX_S5	VCCRTC	5uA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH6-M (3 of 4)

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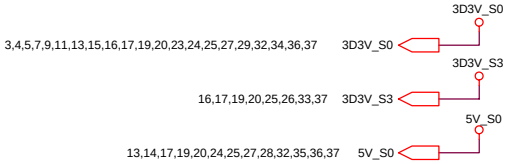
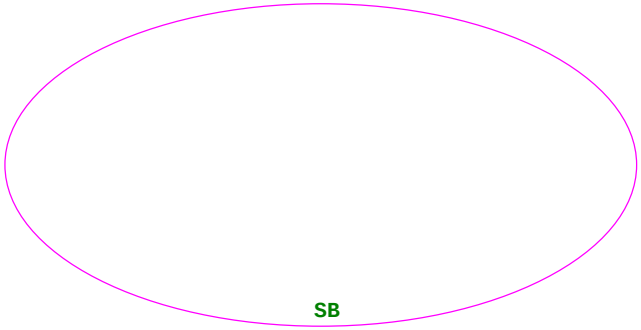
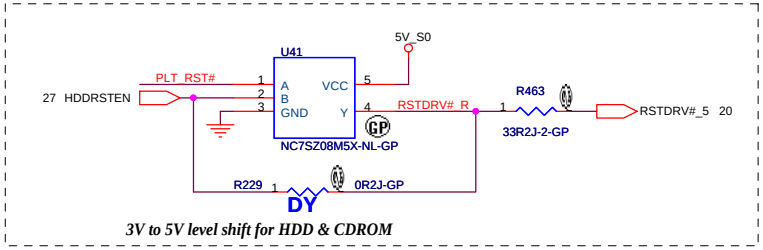
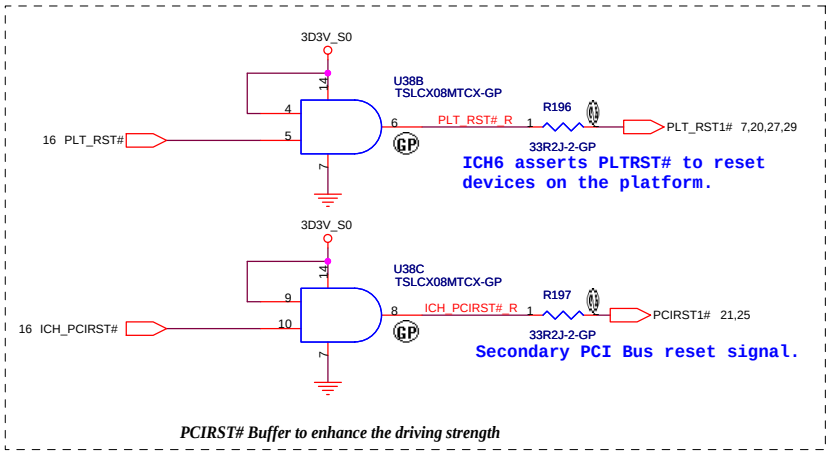
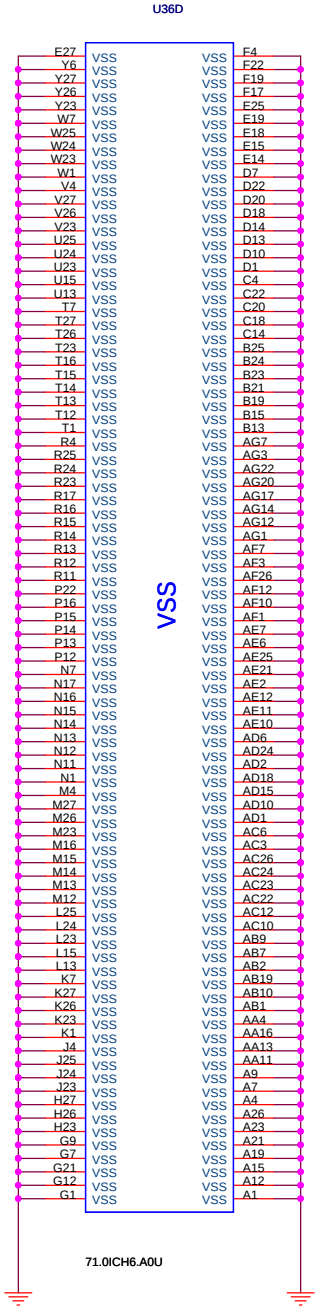


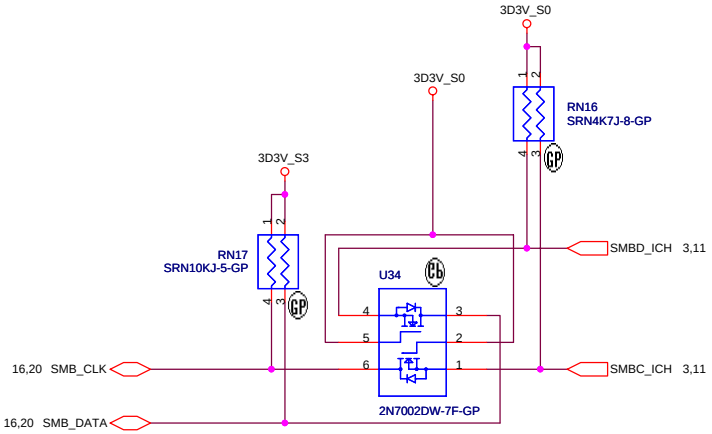








SMBUS(ICH6 ---> SODIMM,CLKGEN)



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ICH6-M (4 of 4)		
Size: A3	Document Number: KeyWest	Rev: SD
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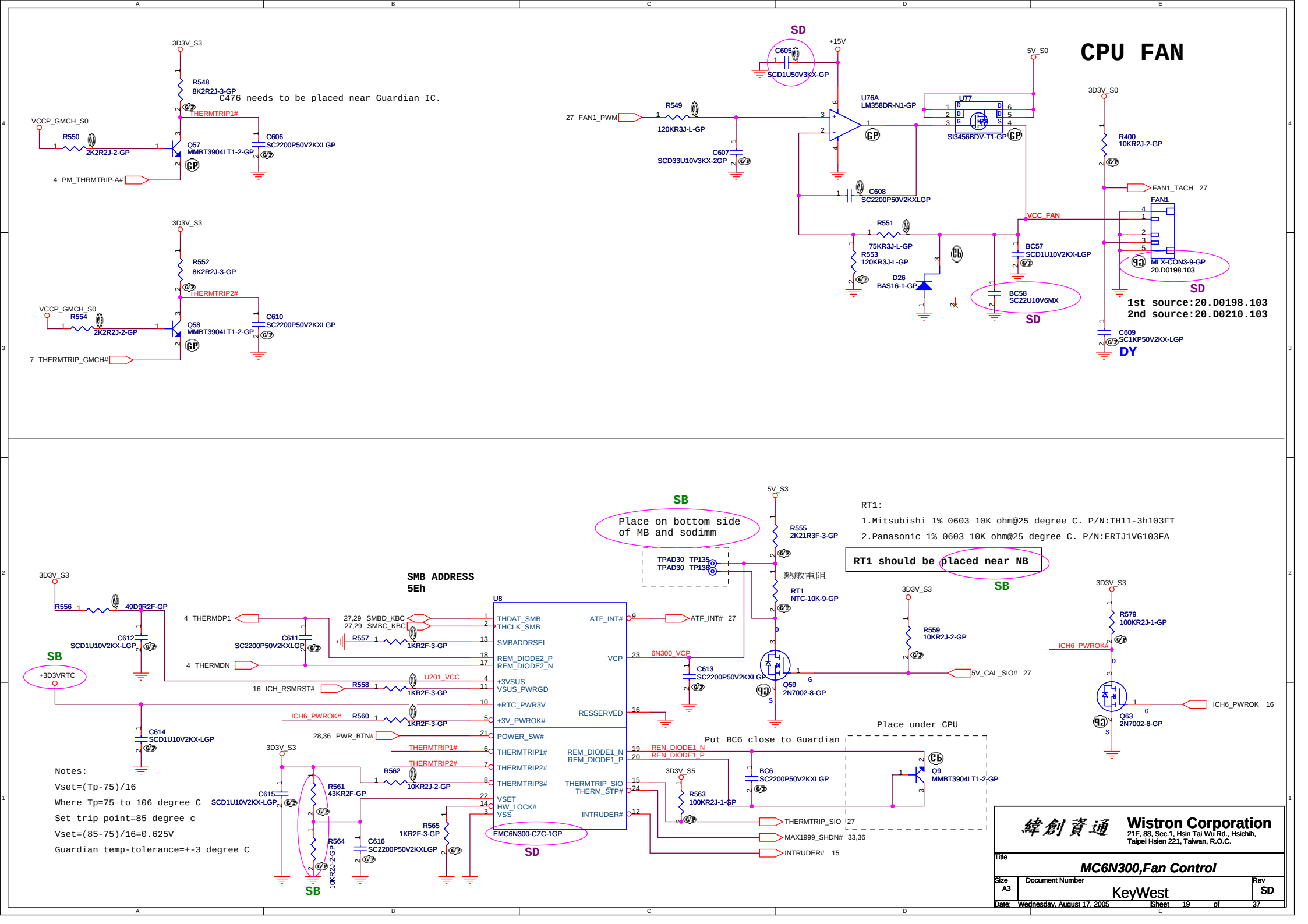
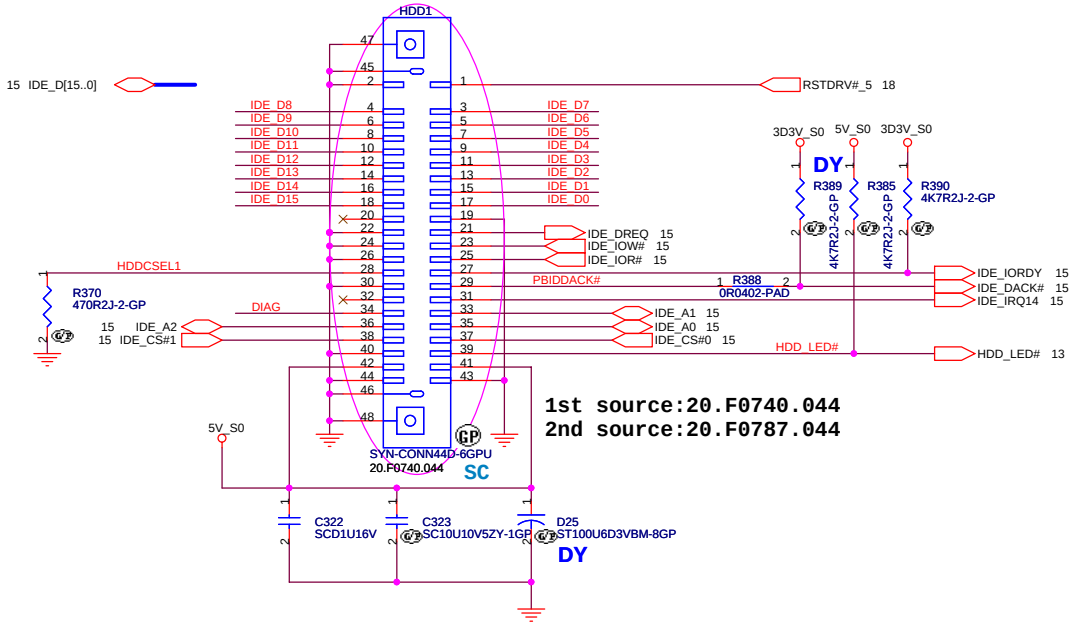

CPU FAN
C476 needs to be placed near Guardian IC.
3D3V_S3
R548
8K2R2J-3-GP
THERMTRIP1#
VCCP_GMCH_S0
R550
2K2R2J-2-GP
Q57
MMBT3904LT1-2-GP
C606
SC2200P50V2KXLGP
4 PM_THRMTRIP-A#
R552
8K2R2J-3-GP
THERMTRIP2#
R554
2K2R2J-2-GP
Q58
MMBT3904LT1-2-GP
C610
SC2200P50V2KXLGP
7 THERMTRIP_GMCH#
SD
C605
SCD1U50V3KX-GP
+15V
27 FAN1_PWM
R549
120KR3J-L-GP
C607
SCD33U10V3KX-2GP
U76A
LM358DR-N1-GP
U77
SI3456BDV-T1-GP
5V_S0
C608
SC2200P50V2KXLGP
R551
75KR3J-L-GP
R553
120KR3J-L-GP
D26
BAS16-1-GP
VCC_FAN
BC57
SCD1U10V2KX-LGP
BC58
SC22U10V6MX
3D3V_S0
R400
10KR2J-2-GP
FAN1_TACH 27
FAN1
MLX-CON3-9-GP
20.D0198.103
C609
SC1KP50V2KX-LGP
DY
1st source:20.D0198.103
2nd source:20.D0210.103
SB
Place on bottom side
of MB and sodimm
TPAD30 TP135
TPAD30 TP136
熱敏電阻
RT1
NTC-10K-9-GP
5V_S3
R555
2K21R3F-3-GP
RT1:
1.Mitsubishi 1% 0603 10K ohm@25 degree C. P/N:TH11-3h103FT
2.Panasonic 1% 0603 10K ohm@25 degree C. P/N:ERTJ1VG103FA
RT1 should be placed near NB
3D3V_S3
R556
49D9R2F-GP
C612
SCD1U10V2KX-LGP
+3D3VRTC
C614
SCD1U10V2KX-LGP
SMB ADDRESS
5Eh
U8
4 THERMDP1
4 THERMDN
27,29 SMBD_KBC
27,29 SMBC_KBC
C611
SC2200P50V2KXLGP
R557
1KR2F-3-GP
16 ICH_RSMRST#
U201_VCC
R558
1KR2F-3-GP
ICH6_PWROK#
R560
1KR2F-3-GP
28,36 PWR_BTN#
THERMTRIP1#
THERMTRIP2#
R562
10KR2J-2-GP
THDAT_SMB
THCLK_SMB
SMBADDRSEL
REM_DIODE2_P
REM_DIODE2_N
+3VSUS
VSUS_PWRGD
+RTC_PWR3V
+3V_PWROK#
POWER_SW#
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
VSET
HW_LOCK#
VSS
EMC6N300-CZC-1GP
ATF_INT#
VCP
RESSERVED
REM_DIODE1_N
REM_DIODE1_P
THERMTRIP_SIO
THERM_STP#
INTRUDER#
ATF_INT# 27
6N300_VCP
C613
SC2200P50V2KXLGP
Q59
2N7002-8-GP
5V_CAL_SIO# 27
R559
10KR2J-2-GP
3D3V_S3
R579
100KR2J-1-GP
ICH6_PWROK#
Q63
2N7002-8-GP
ICH6_PWROK 16
Place under CPU
Put BC6 close to Guardian
REN_DIODE1_N
REN_DIODE1_P
3D3V_S5
R563
100KR2J-1-GP
BC6
SC2200P50V2KXLGP
Q9
MMBT3904LT1-2-GP
THERMTRIP_SIO 27
MAX1999_SHDN# 33,36
INTRUDER# 15
3D3V_S3
C615
SCD1U10V2KX-LGP
R561
43KR2F-GP
R564
10KR2J-2-GP
C616
SC2200P50V2KXLGP
R565
1KR2F-3-GP
SB
Notes:
Vset=(Tp-75)/16
Where Tp=75 to 106 degree C
Set trip point=85 degree c
Vset=(85-75)/16=0.625V
Guardian temp-tolerance=+-3 degree C
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MC6N300,Fan Control
Size
A3
Document Number
KeyWest
Rev
SD
Date: Wednesday, August 17, 2005
Sheet 19 of 37

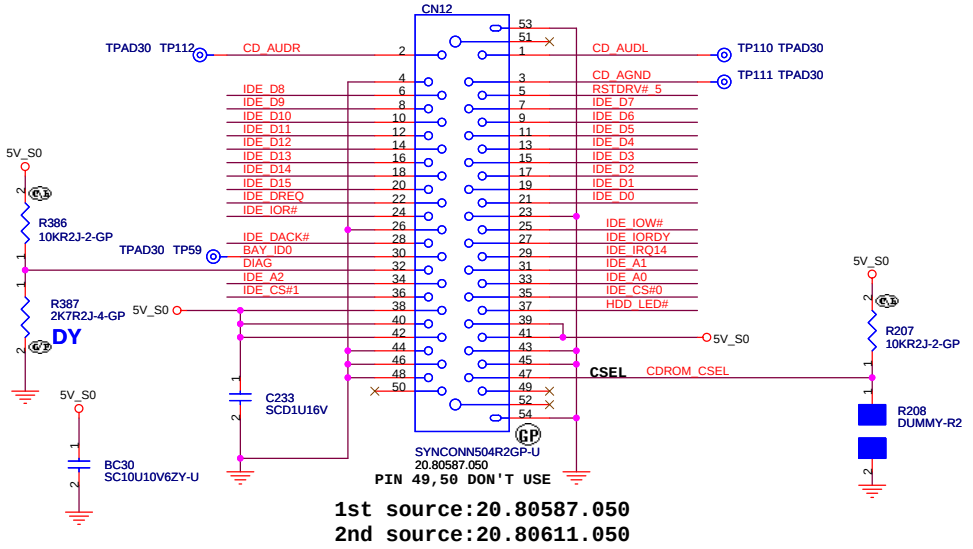
HDD Connector



1st source:20.F0740.044
2nd source:20.F0787.044

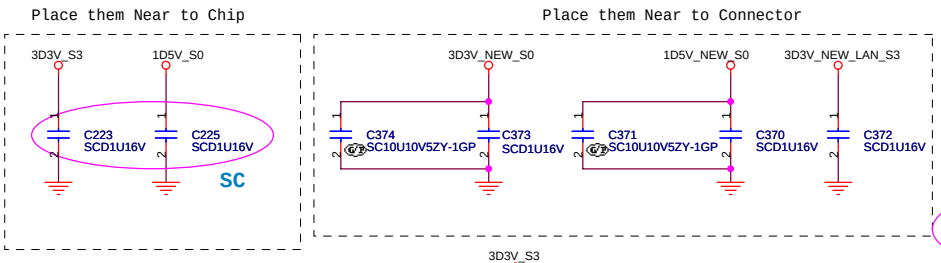
3,4,5,7,9,11,13,15,16,17,18,19,23,24,25,27,29,32,34,36,37 3D3V_S0 3D3V_S0
16,17,18,19,25,26,33,37 3D3V_S3 3D3V_S3
13,14,17,18,19,24,25,27,28,32,35,36,37 5V_S0 5V_S0
5,7,9,16,17,36,37 1D5V_S0 1D5V_S0

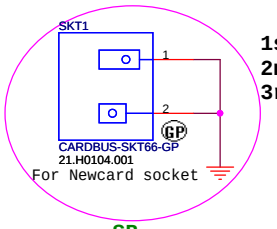
CDROM



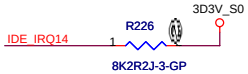
1st source:20.80587.050
2nd source:20.80611.050

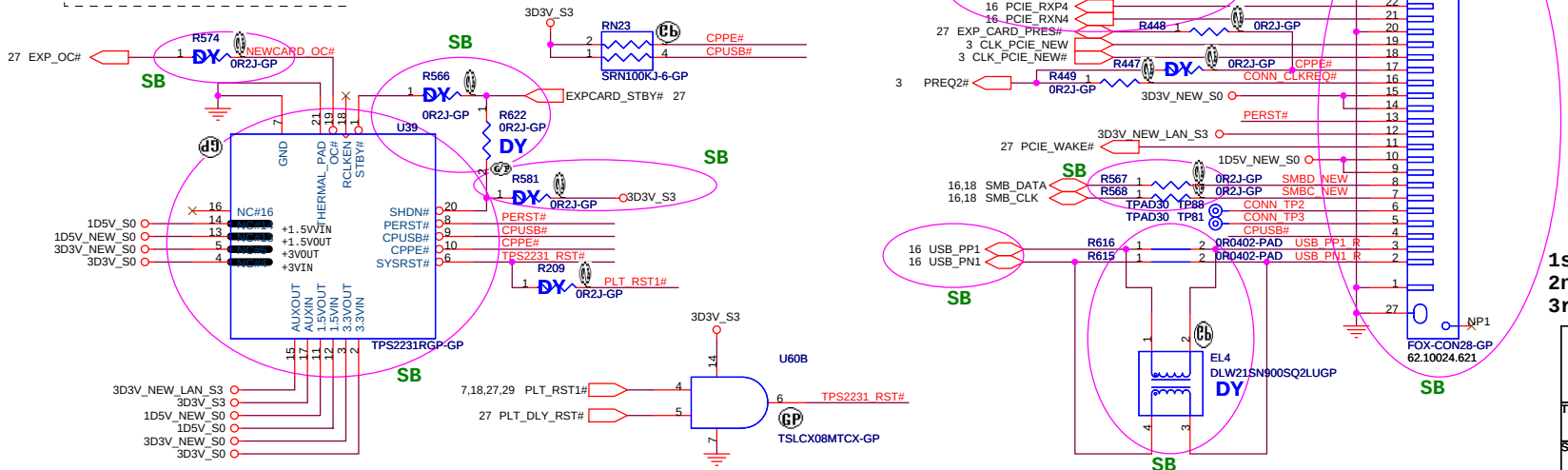
NEWCARD Connector





1st source:21.H0104.001
2nd source:21.H0103.011
3rd source:21.H0111.001





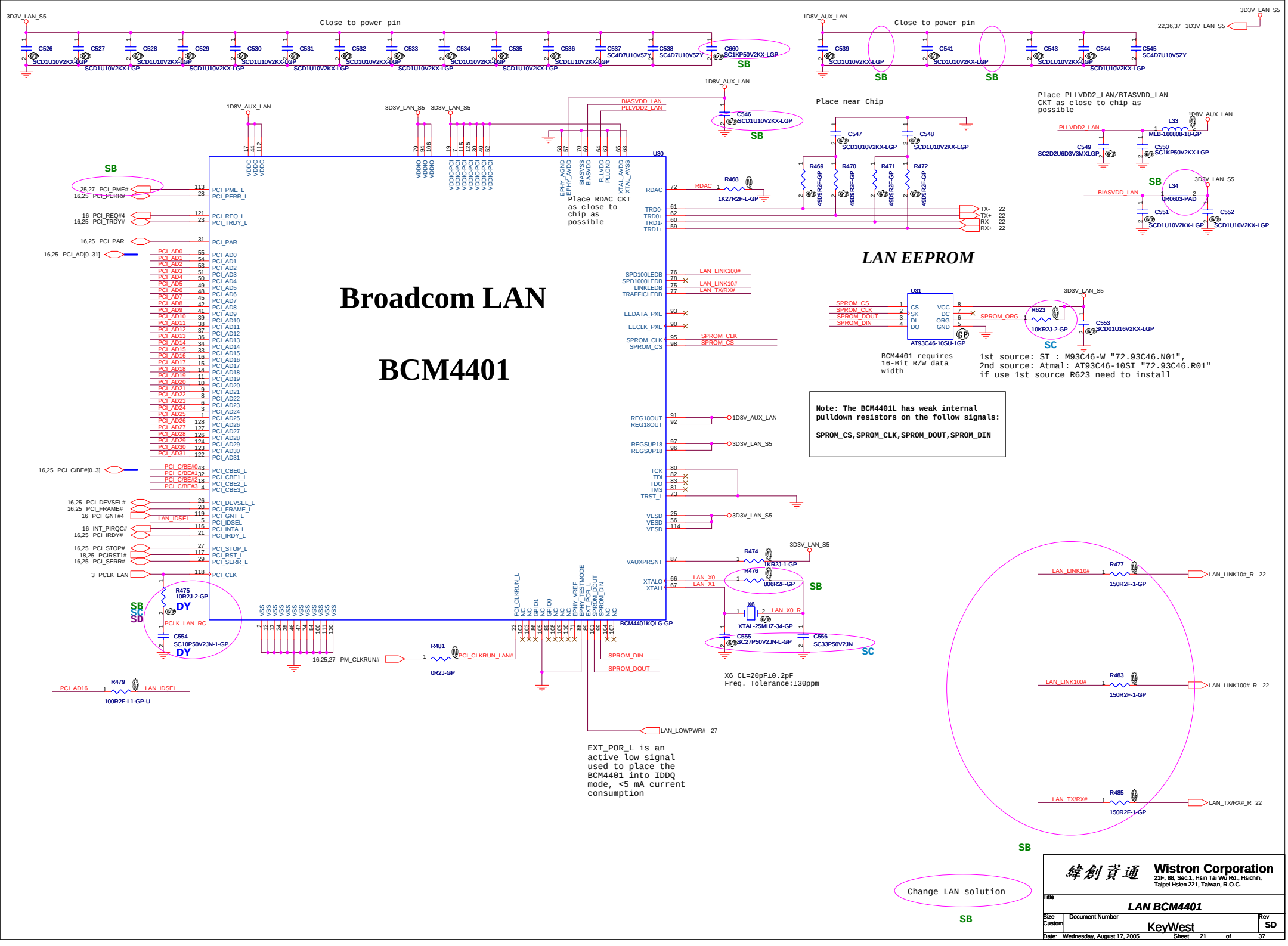
SMBUS(ICH6--NEWCARD,LAN)

1st source:62.10024.621
2nd source:62.10081.021
3rd source:20.F0782.026

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD / CDROM / NEW CARD	
Size A3	Document Number KeyWest	Rev SD
Date: Wednesday, August 17, 2005	Sheet 20 of 37	

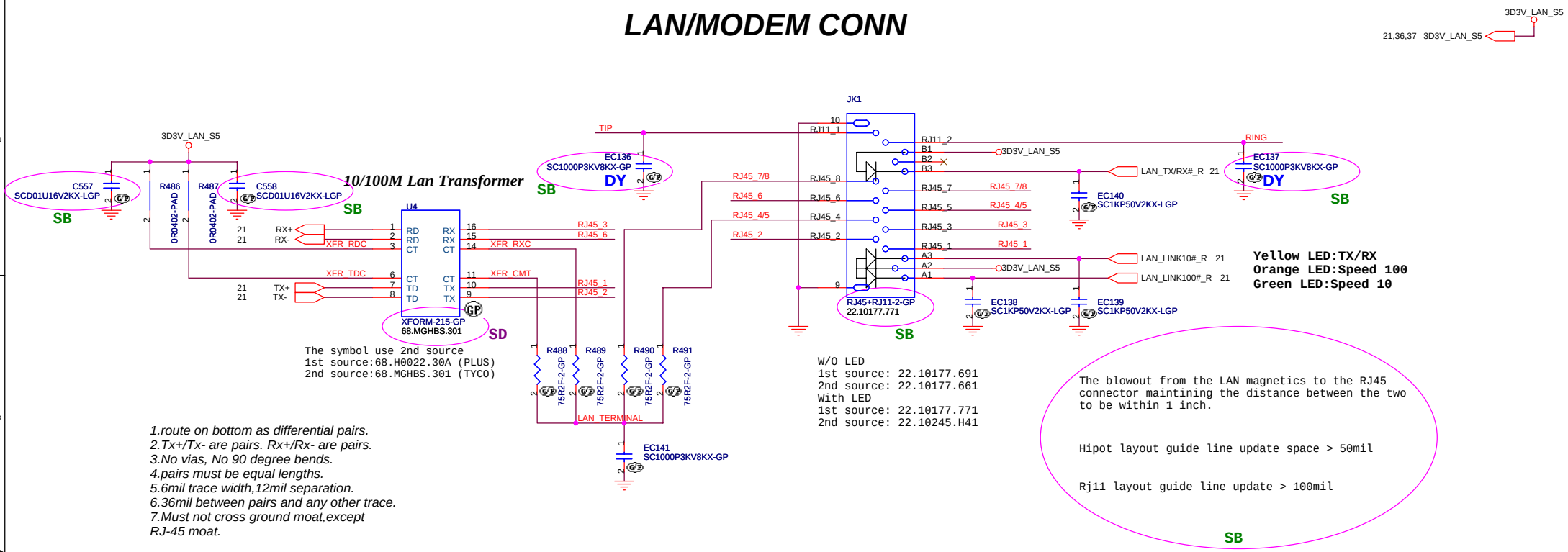
Broadcom LAN

BCM4401



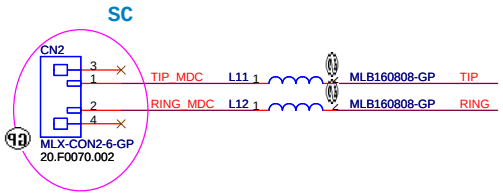
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LAN BCM4401	
Size: Custom	Document Number: KeyWest	Rev: SD
Date: Wednesday, August 17, 2005	Sheet 21 of 37

LAN/MODEM CONN



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



Change LAN solution

SB

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: LAN Connector			
Size: A3	Document Number: KeyWest		Rev: SD
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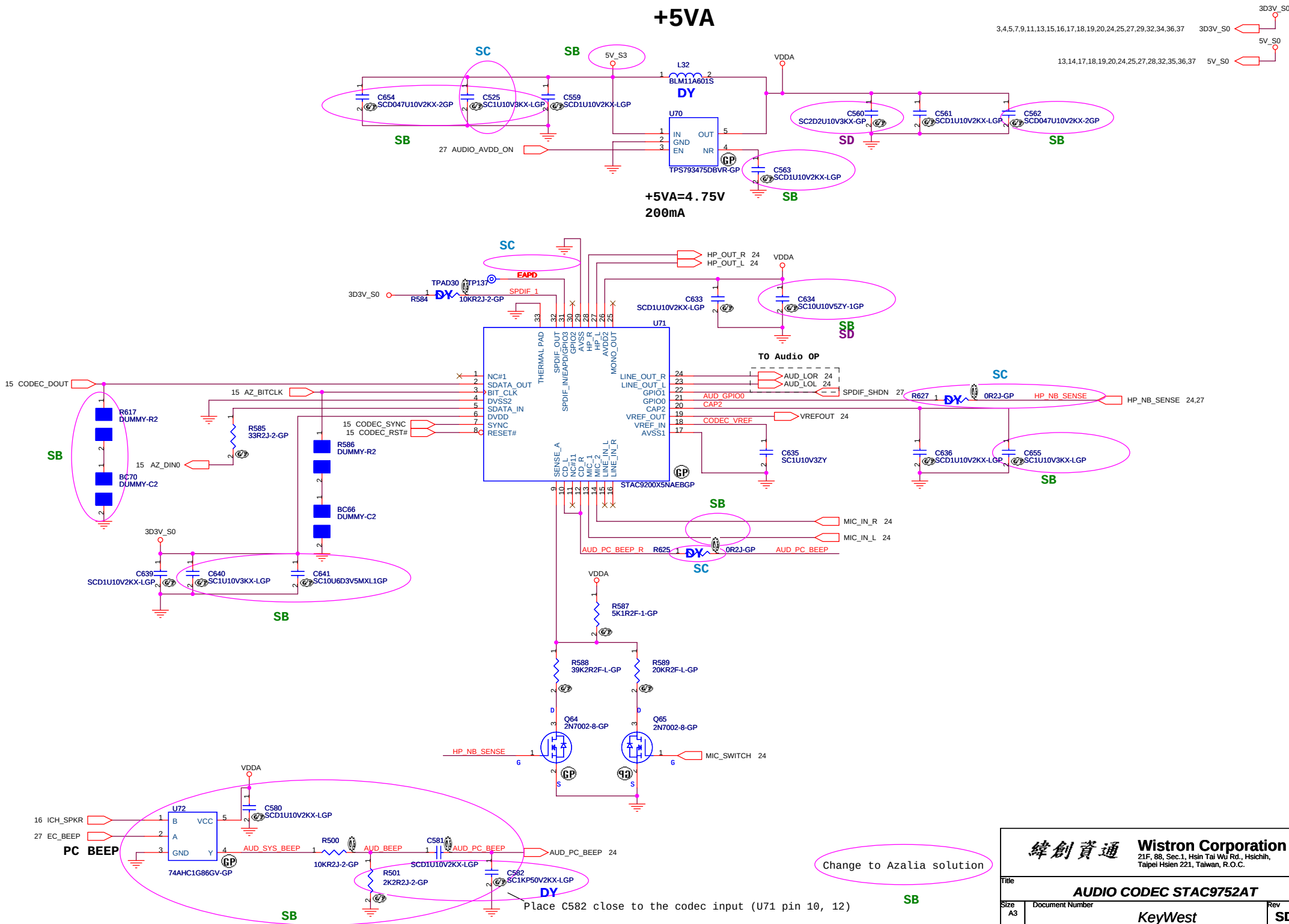
+5VA



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: AUDIO CODEC STAC9752AT		
Size: A3	Document Number: KeyWest	Rev: SD
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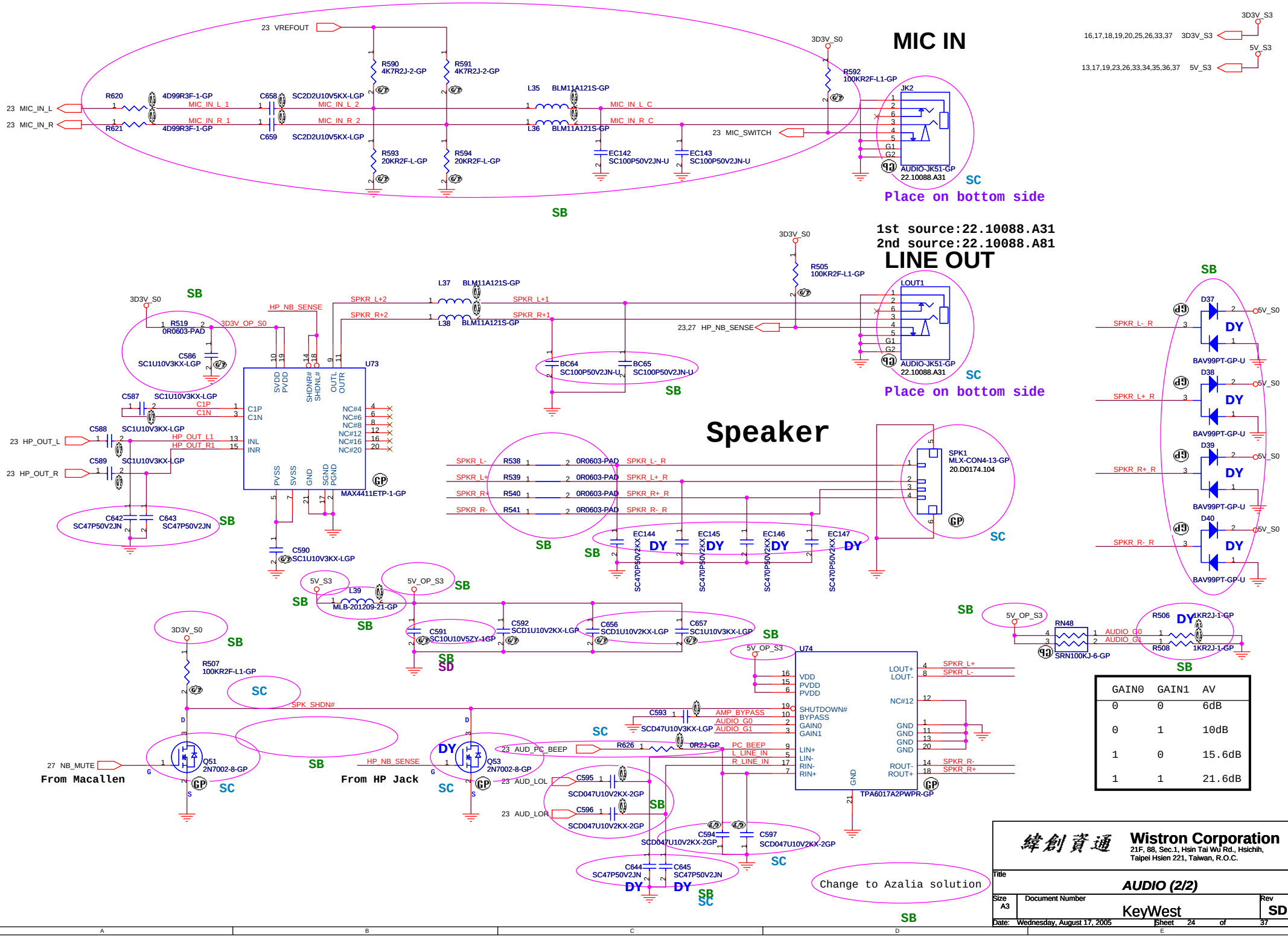
MIC IN
23 VREFOUT
R590 4K7R2J-2-GP
R591 4K7R2J-2-GP
23 MIC_IN_L
23 MIC_IN_R
R620 4D99R3F-1-GP
R621 4D99R3F-1-GP
C658 SC2D2U10V5KX-LGP
C659 SC2D2U10V5KX-LGP
MIC_IN_L_1
MIC_IN_R_1
MIC_IN_L_2
MIC_IN_R_2
R593 20KR2F-L-GP
R594 20KR2F-L-GP
L35 BLM11A121S-GP
L36 BLM11A121S-GP
MIC_IN_L_C
MIC_IN_R_C
EC142 SC100P50V2JN-U
EC143 SC100P50V2JN-U
23 MIC_SWITCH
3D3V_S0
R592 100KR2F-L1-GP
JK2
AUDIO-JK51-GP 22.10088.A31
SC
Place on bottom side
SB
3D3V_S3
16,17,18,19,20,25,26,33,37 3D3V_S3
5V_S3
13,17,19,23,26,33,34,35,36,37 5V_S3
1st source:22.10088.A31
2nd source:22.10088.A81
LINE OUT
3D3V_S0
R505 100KR2F-L1-GP
LOUT1
AUDIO-JK51-GP 22.10088.A31
SC
Place on bottom side
SB
L37 BLM11A121S-GP
L38 BLM11A121S-GP
SPKR_L+2
SPKR_R+2
SPKR_L+1
SPKR_R+1
23,27 HP_NB_SENSE
BC64 SC100P50V2JN-U
BC65 SC100P50V2JN-U
HP_NB_SENSE
R519 0R0603-PAD
3D3V_OP_S0
C586 SC1U10V3KX-LGP
U73
MAX4411ETP-1-GP
C587 SC1U10V3KX-LGP
C588 SC1U10V3KX-LGP
C589 SC1U10V3KX-LGP
23 HP_OUT_L
23 HP_OUT_R
HP_OUT_L1
HP_OUT_R1
C642 SC47P50V2JN
C643 SC47P50V2JN
C590 SC1U10V3KX-LGP
Speaker
SPKR_L- R538 0R0603-PAD SPKR_L- R
SPKR_L+ R539 0R0603-PAD SPKR_L+ R
SPKR_R+ R540 0R0603-PAD SPKR_R+ R
SPKR_R- R541 0R0603-PAD SPKR_R- R
SPK1 MLX-CON4-13-GP 20.D0174.104
EC144 DY
EC145 DY
EC146 DY
EC147 DY
SC470P50V2KX
D37 BAV99PT-GP-U
D38 BAV99PT-GP-U
D39 BAV99PT-GP-U
D40 BAV99PT-GP-U
5V_S0
5V_S3
L39 MLB-201209-21-GP
5V_OP_S3
C591 SC10U10V5ZY-1GP
C592 SCD1U10V2KX-LGP
C656 SCD1U10V2KX-LGP
C657 SC1U10V3KX-LGP
SD
RN48 SRN100KJ-6-GP
AUDIO_G0
AUDIO_G1
R506 1KR2J-1-GP
R508 1KR2J-1-GP
GAIN0 GAIN1 AV
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
3D3V_S0
R507 100KR2F-L-GP
SPK_SHDN#
27 NB_MUTE
From Macallen
Q51 2N7002-8-GP
HP_NB_SENSE
From HP Jack
Q53 2N7002-8-GP
U74
TPA6017A2PWPR-GP
C593 SCD47U10V3KX-LGP
R626 0R2J-GP
23 AUD_PC_BEEP
23 AUD_LOL
23 AUD_LOR
C595 SCD047U10V2KX-2GP
C596 SCD047U10V2KX-2GP
C594 SCD047U10V2KX-2GP
C597 SCD047U10V2KX-2GP
C644 SC47P50V2JN
C645 SC47P50V2JN
Change to Azalia solution
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO (2/2)
Size A3
Document Number KeyWest
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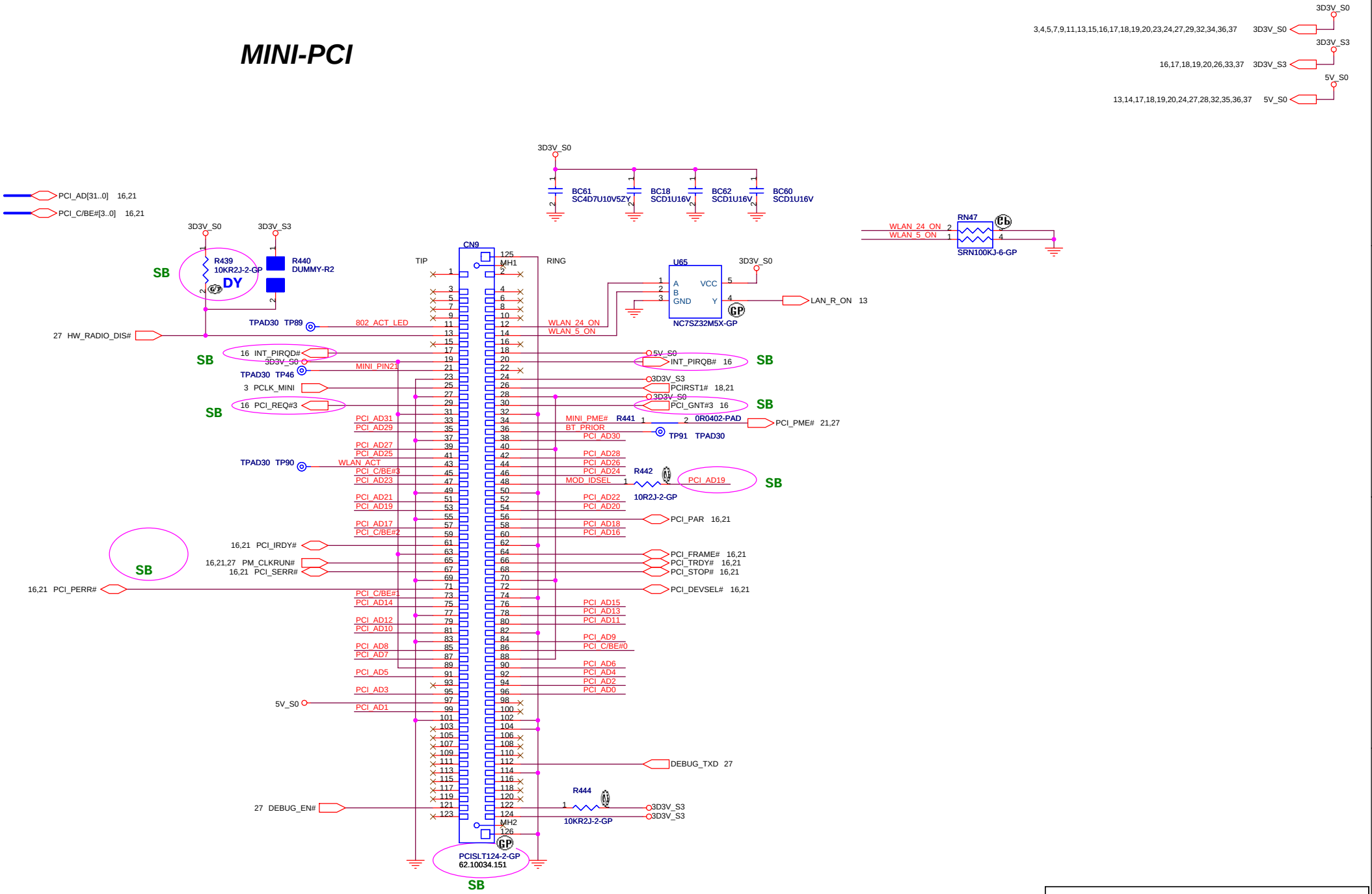
MINI-PCI



1st source:62.10034.151
2nd source:62.10043.151

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MINI-PCI	
Size A3	Document Number KeyWest	Rev SD
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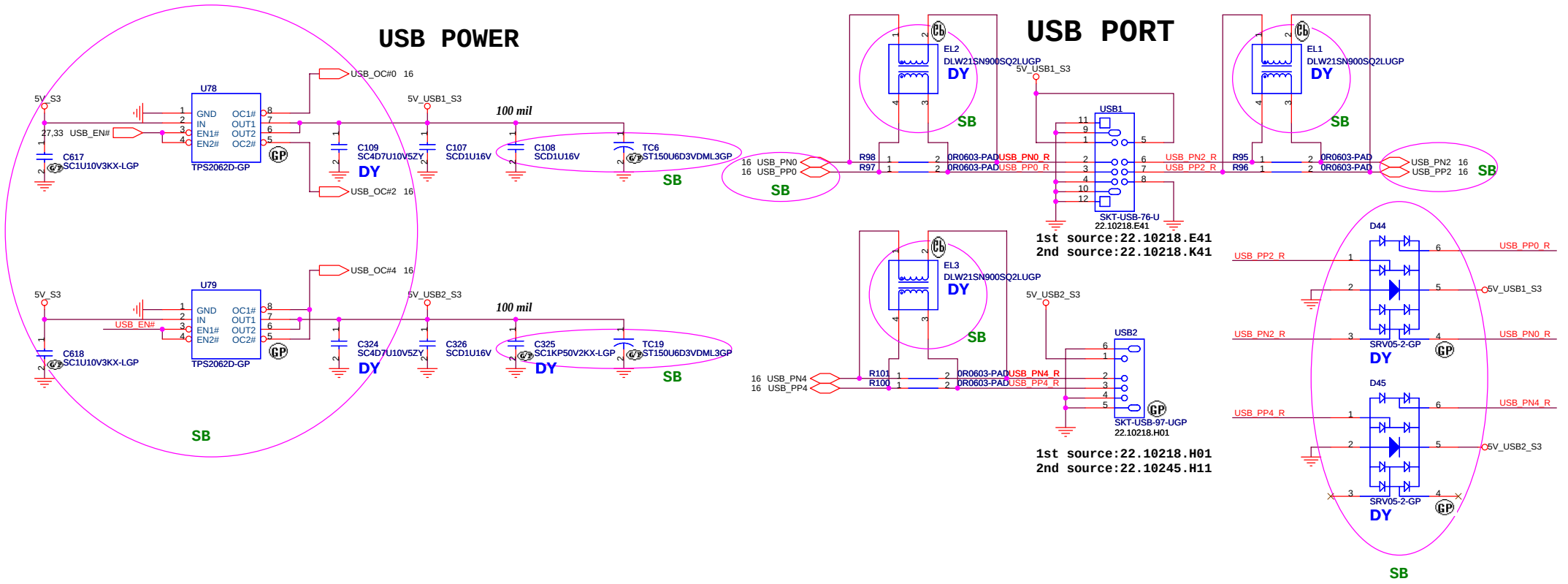
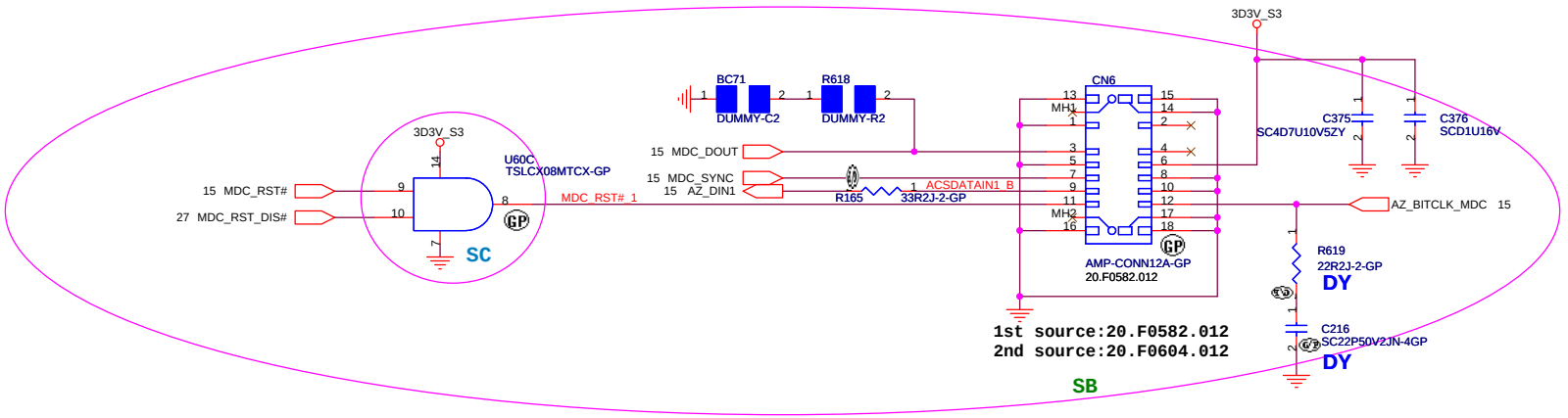
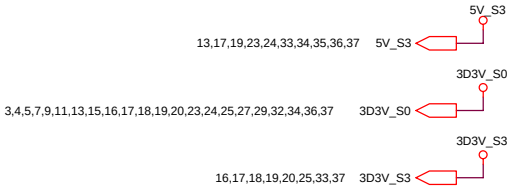
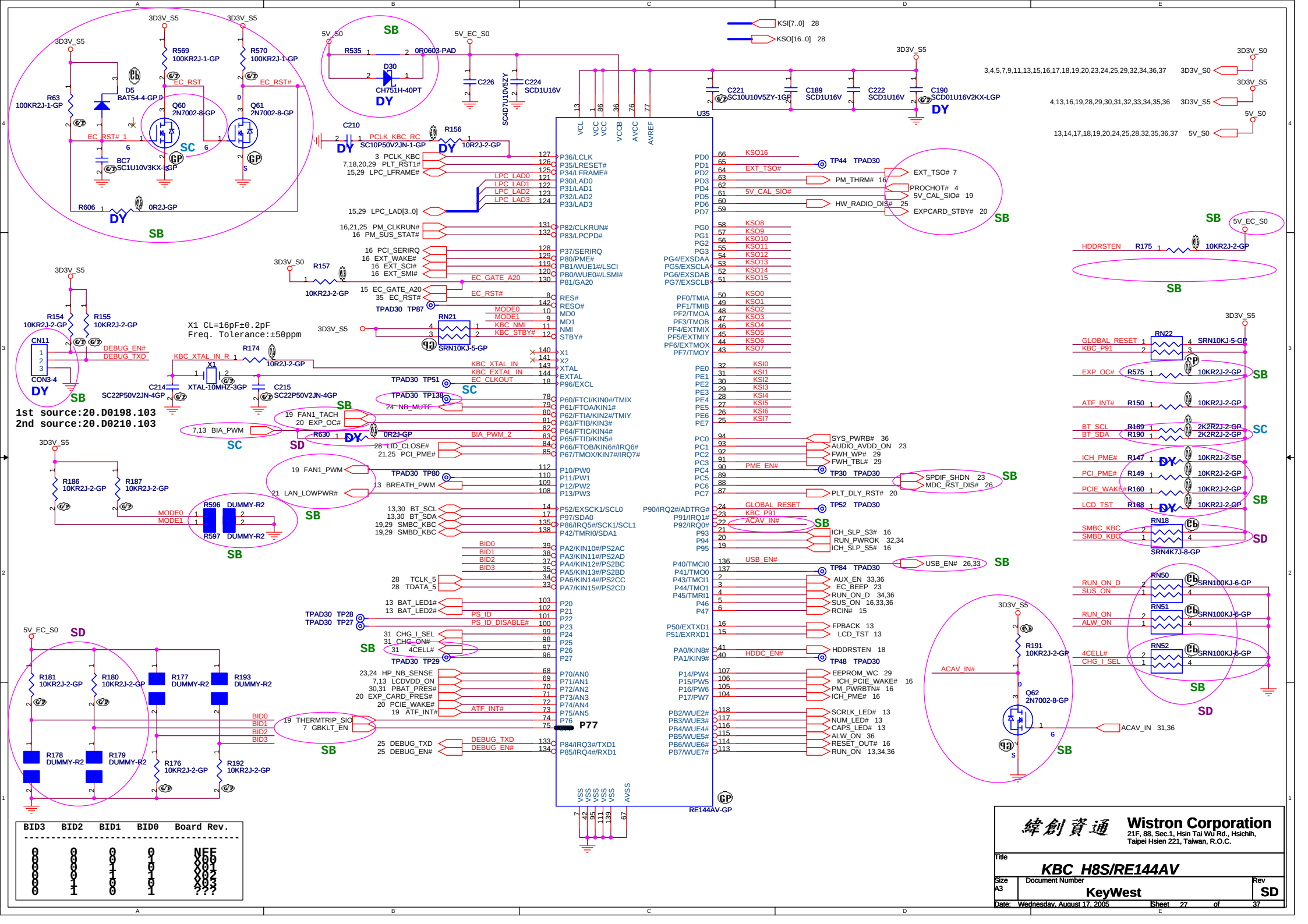






緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***USB / MDC CONN.***	
Size A3	Document Number KeyWest	Rev SD
Date: Wednesday, August 17, 2005	Sheet 26 of 37	


1st source:20.D0198.103
2nd source:20.D0210.103
X1 CL=16pF±0.2pF
Freq. Tolerance:±50ppm
U35
RE144AV-GP
P77
KSI[7..0] 28
KSO[16..0] 28
3,4,5,7,9,11,13,15,16,17,18,19,20,23,24,25,29,32,34,36,37 3D3V_S0
4,13,16,19,28,29,30,31,32,33,34,35,36 3D3V_S5
13,14,17,18,19,20,24,25,28,32,35,36,37 5V_S0
BID3 BID2 BID1 BID0 Board Rev.
0 0 0 0 NEE
0 0 0 1 X00
0 0 1 0 X01
0 1 0 1 X02
0 1 0 0 X03
0 1 0 1 ???
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC_H8S/RE144AV
Size A3
Document Number KeyWest
Rev SD
Date: Wednesday, August 17, 2005
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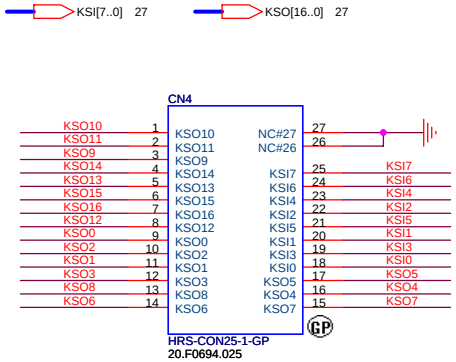
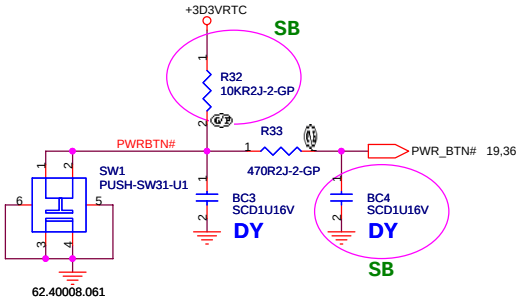
INTERNAL KEYBOARD CONNECTOR



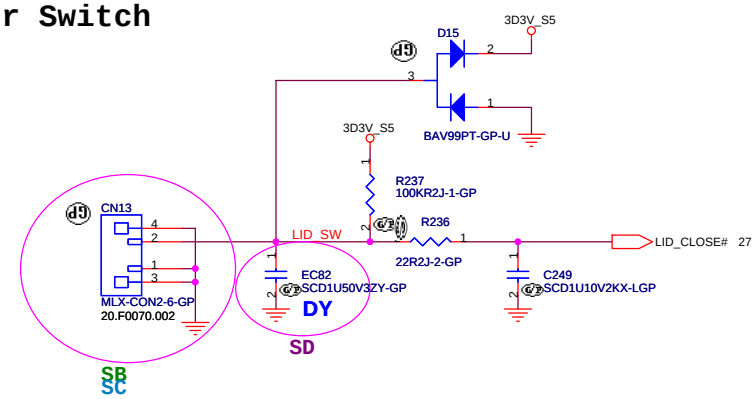
1st source : 20.F0694.025
2nd source : 20.F0642.025

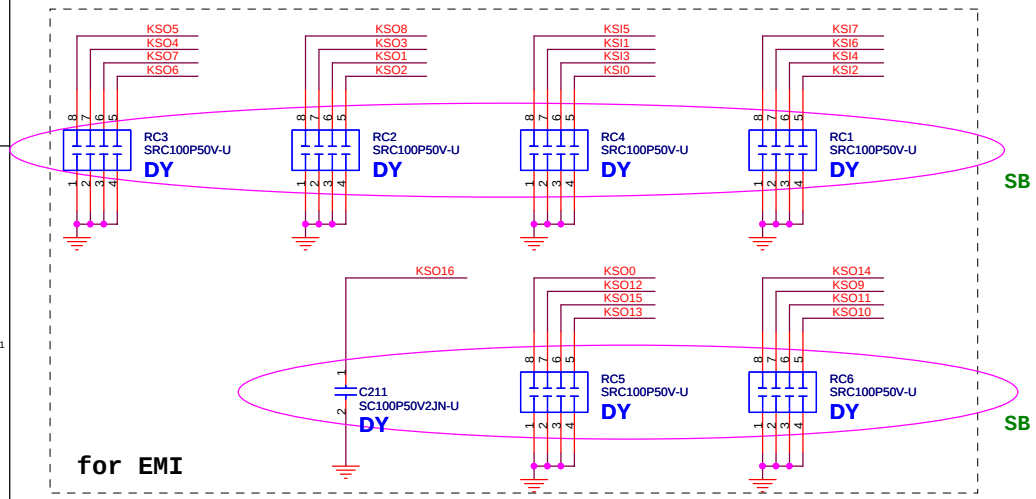
POWER BUTTON



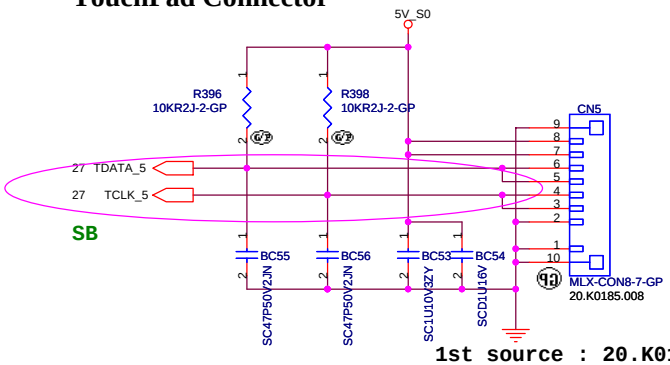
1st source : 62.40008.061
2nd source : 62.40009.191

Cover Switch





TouchPad Connector



1st source : 20.K0185.008
2nd source : 20.K0212.008

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***KB / TPAD / LID SW / PWR BTN***	
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3D3V_S5

4,13,16,19,27,28,30,31,32,33,34,35,36 3D3V_S5

512KB Flash

Unused FGPI pins must not be float

RP1
SELECT_FWH 1
FWH_FGPI4 2
FWH_FGPI3 3
FWH_FGPI2 4
5
10
9
8
7 FWH_FGPI1
6 FWH_FGPI0
SRP10K

LPC_LAD[3..0] 15,27

SB
3D3V_S0
C242 SCD1U16V
C241 SC1U10V3ZY

LPC_LFRAME# 15,27
FWH_INIT# 15
PLT_RST1# 7,18,20,27
SELECT_FWH
PCLK_FWH 3
R227 DUMMY-R3
PCLK_FWH_RC
C243 DUMMY-C3

SB
3D3V_S0
RN20
SRN10KJ-5-GP
27 FWH_TBL#
27 FWH_WP#

U40
VDD 25
VDD 32
WE#/FWH4 23
OE#/INIT# 24
R/C#/CLK 31
RST# 2
IC 29

A0/ID0 12
A1/ID1 11
A2/ID2 10
A3/ID3 9
A4/TBL# 8
A5/WP# 7
A6/FGPI0 6
A7/FGPI1 5
A8/FGPI2 4
A9/FGPI3 3
A10/FGPI4 30

DQ0/FWH0 13 LPC_LAD0
DQ1/FWH1 14 LPC_LAD1
DQ2/FWH2 15 LPC_LAD2
DQ3/FWH3 17 LPC_LAD3
DQ4/RES 18
DQ5/RES 19
DQ6/RES 20
DQ7/RES 21

FWH_FGPI0
FWH_FGPI1
FWH_FGPI2
FWH_FGPI3
FWH_FGPI4

VSS 28
VSS 16
NC#27 27
NC#26 26
NC#22 22
NC#1 1

49LF004B334C-GP
72.49004.F03
3D3V_S0
SB

SCOKET:
62.10002.032
62.10005.032

1st source:72.49004.F03 (SST)
2nd source:72.49004.G03 (PMC)
3rd source:72.39040.J03 (Winbond)

SMBus address A2

User Password

3D3V_S5
U32
A0 1
A1 2
A2 3
GND 4
VCC 8
WP 7
SCL 6
SDA 5
AT24C04N-10SU-GP
72.24C04.E01

3D3V_S5
C188
SCD1U10V2KX-LGP
EEPROM_WC 27
SMBC_KBC 19,27
SMBD_KBC 19,27

The symbol use 2nd source
1st source:72.24C04.G01 (ST)
2nd source:72.24C04.E01 (ATMEL)

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**BIOS**	
Size A3	Document Number **KeyWest**	Rev **SD**
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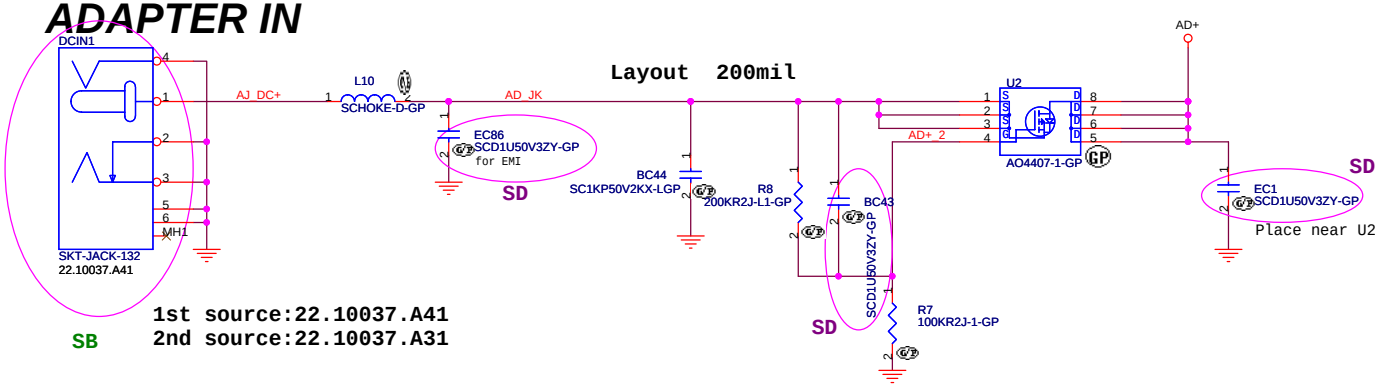
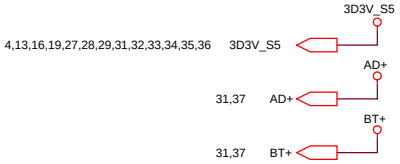
Adaptor in to generate DCBATOUT

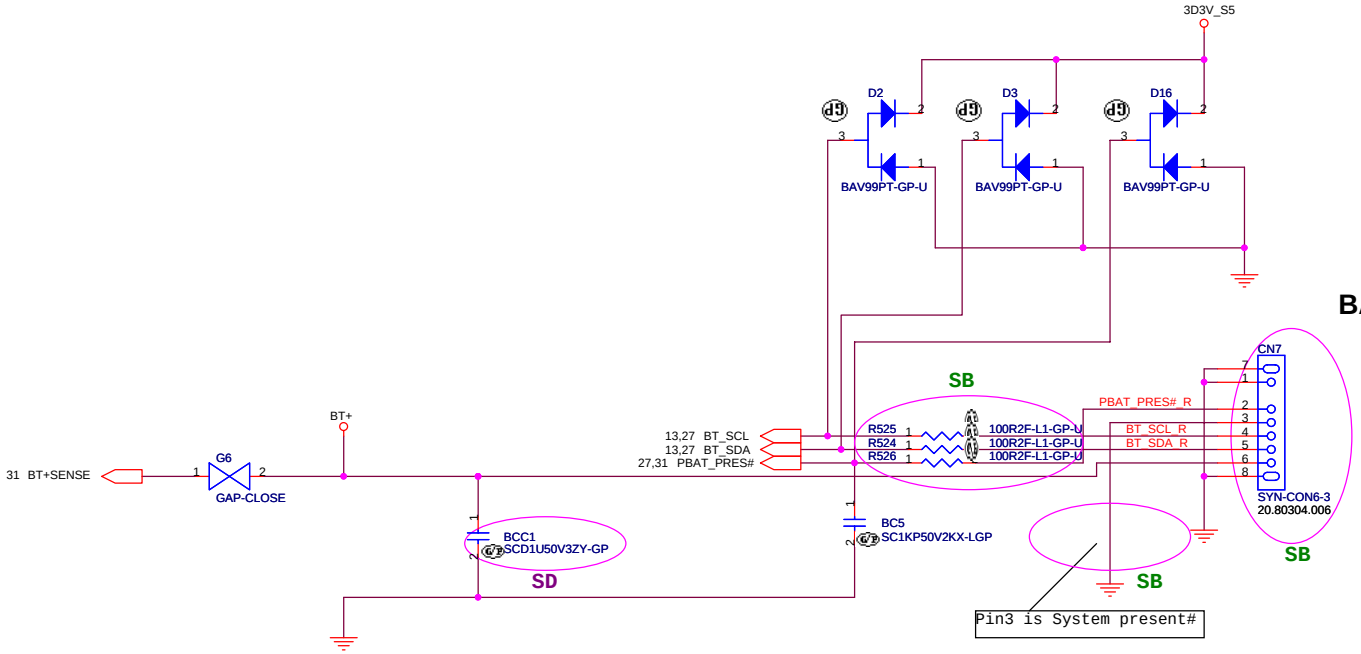
ADAPTER IN



SB

1st source:22.10037.A41
2nd source:22.10037.A31





BATTERY CONNECTOR

1st source:20.80304.006
2nd source:20.80385.006

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Title	***Adaptor/ Bettery conn.***	
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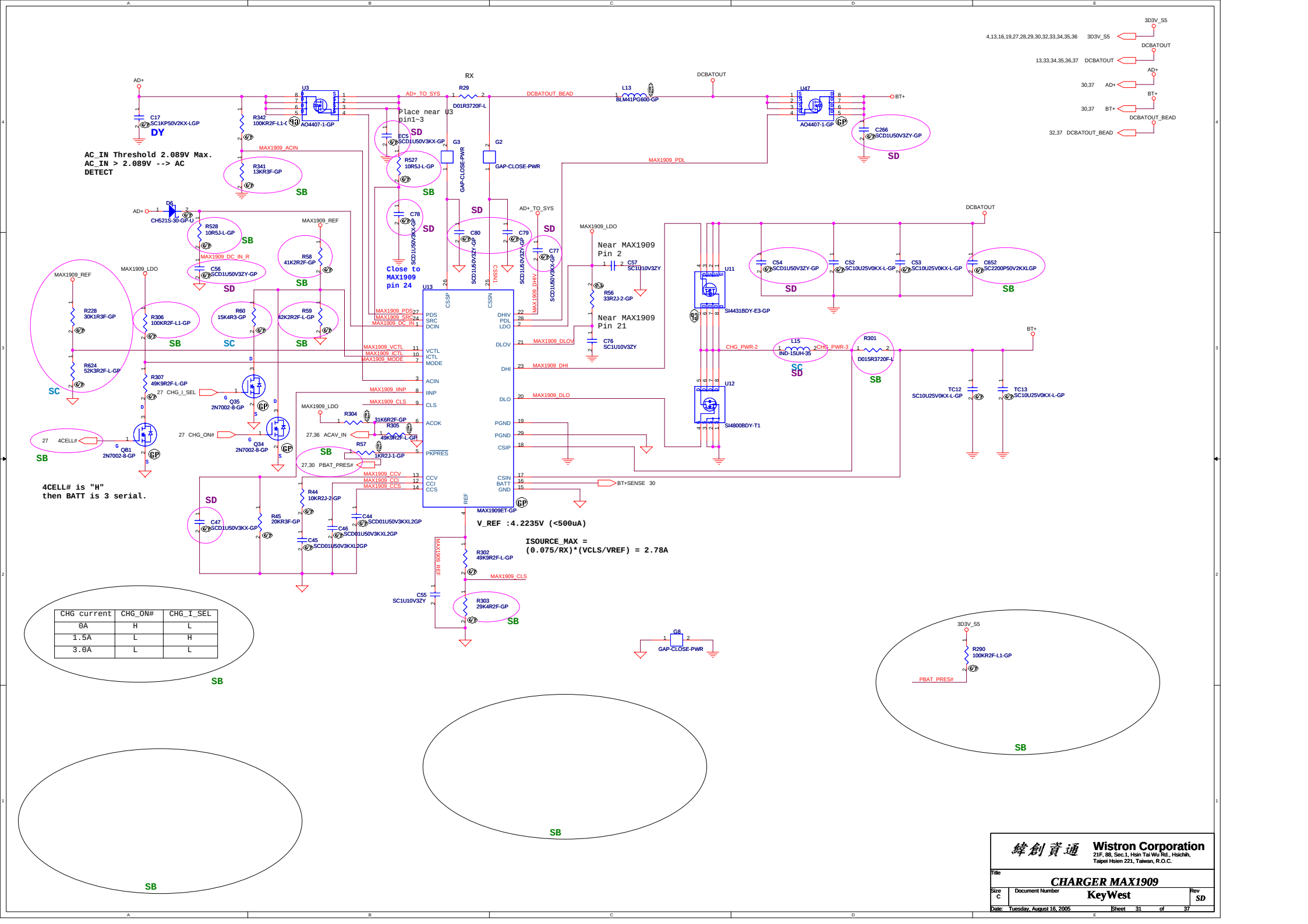
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
4CELL# is "H"
then BATT is 3 serial.
Place near U3 pin1~3
Close to MAX1909 pin 24
Near MAX1909 Pin 2
Near MAX1909 Pin 21
V_REF :4.2235V (<500uA)
ISOURCE_MAX = (0.075/RX)*(VCLS/VREF) = 2.78A
RX
CHG current | CHG_ON# | CHG_I_SEL
0A | H | L
1.5A | L | H
3.0A | L | L
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CHARGER MAX1909
KeyWest
Date: Tuesday, August 16, 2005
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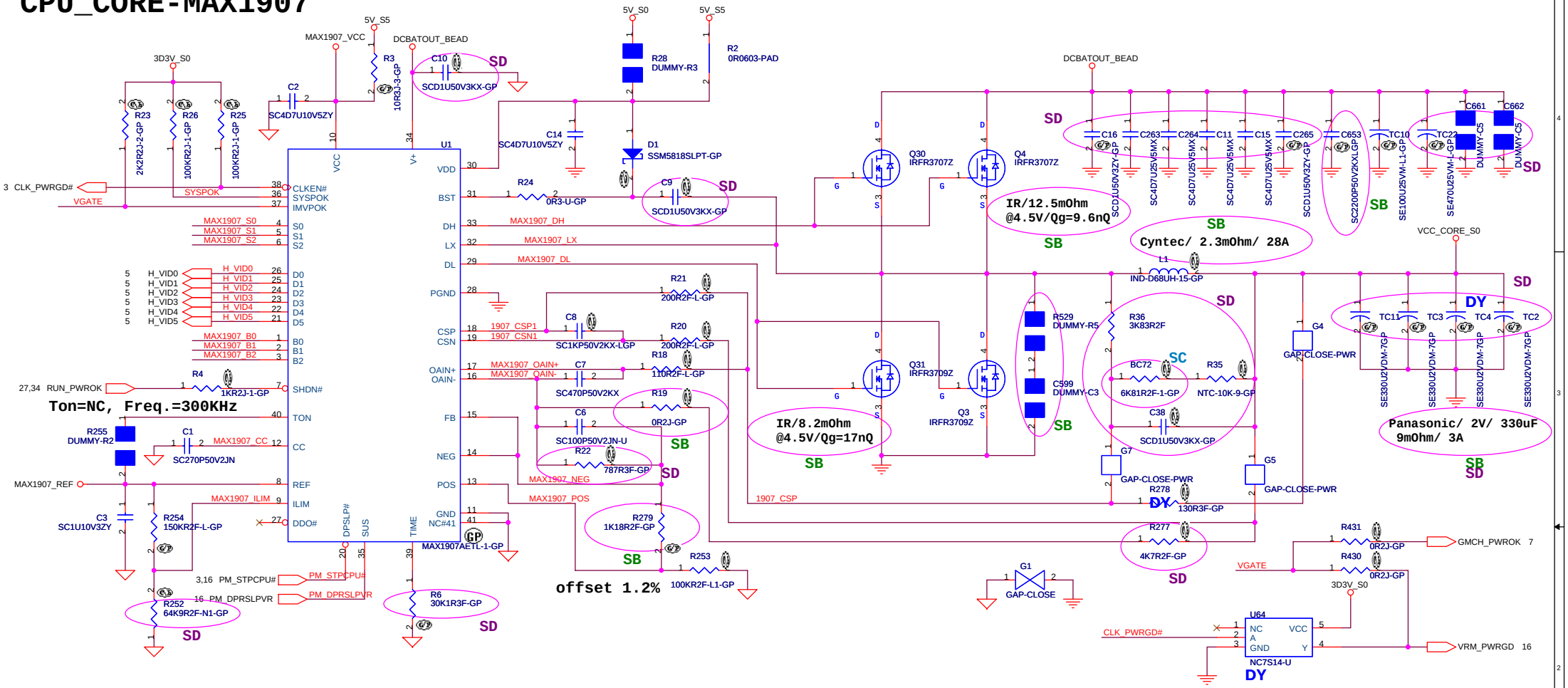
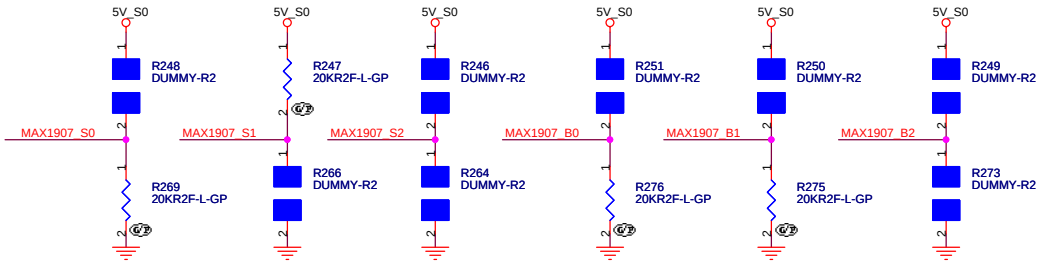
CPU_CORE-MAX1907



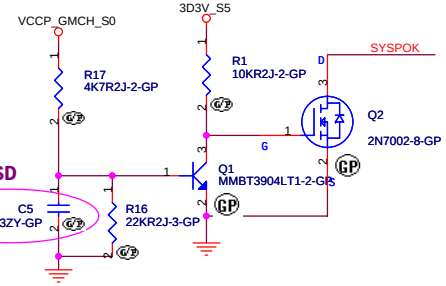
OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940



緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *IMVP IV-CPU POWER-MAX1907*

Size: A3 | Document Number: *KeyWest* | Rev: *SD*

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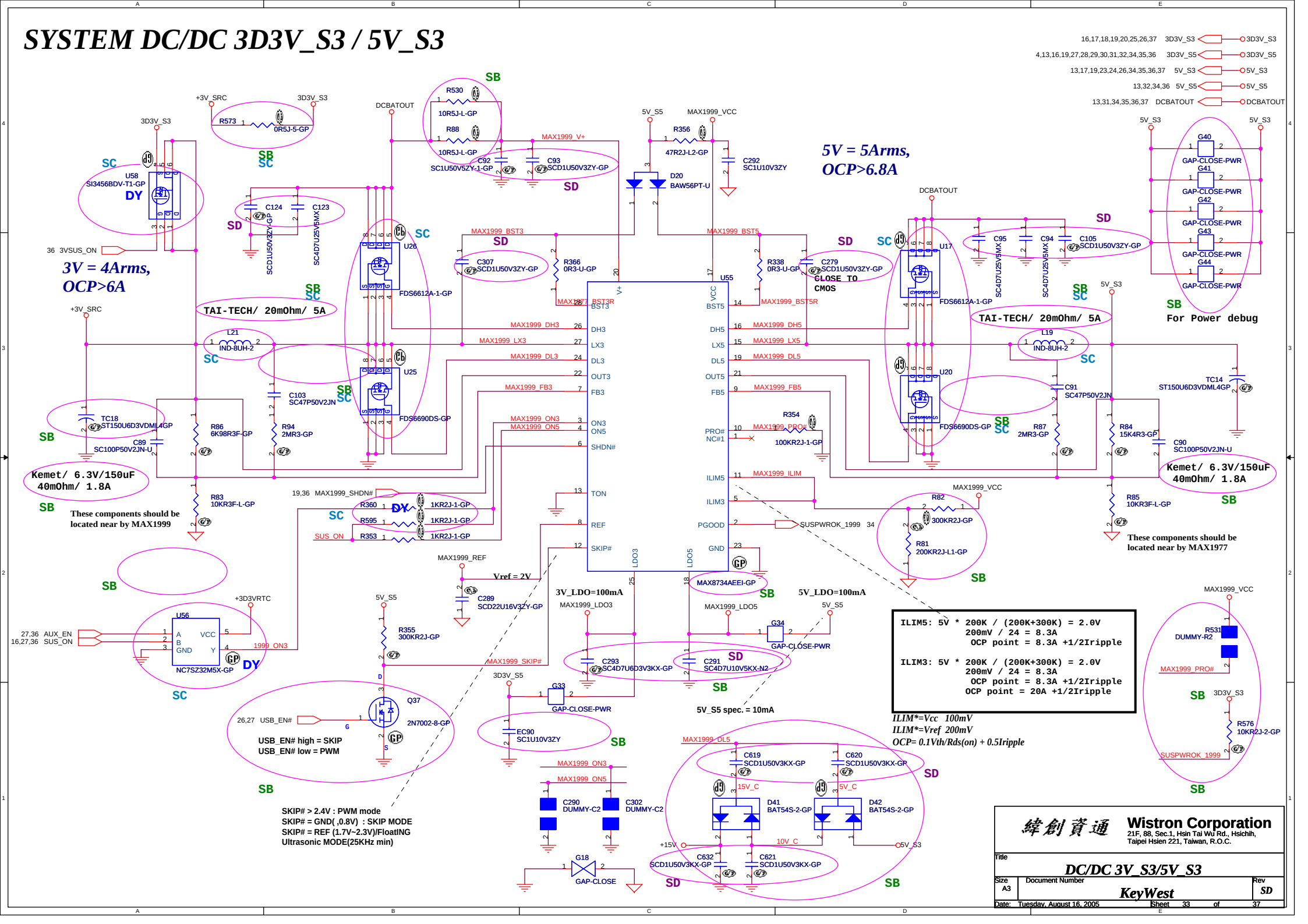
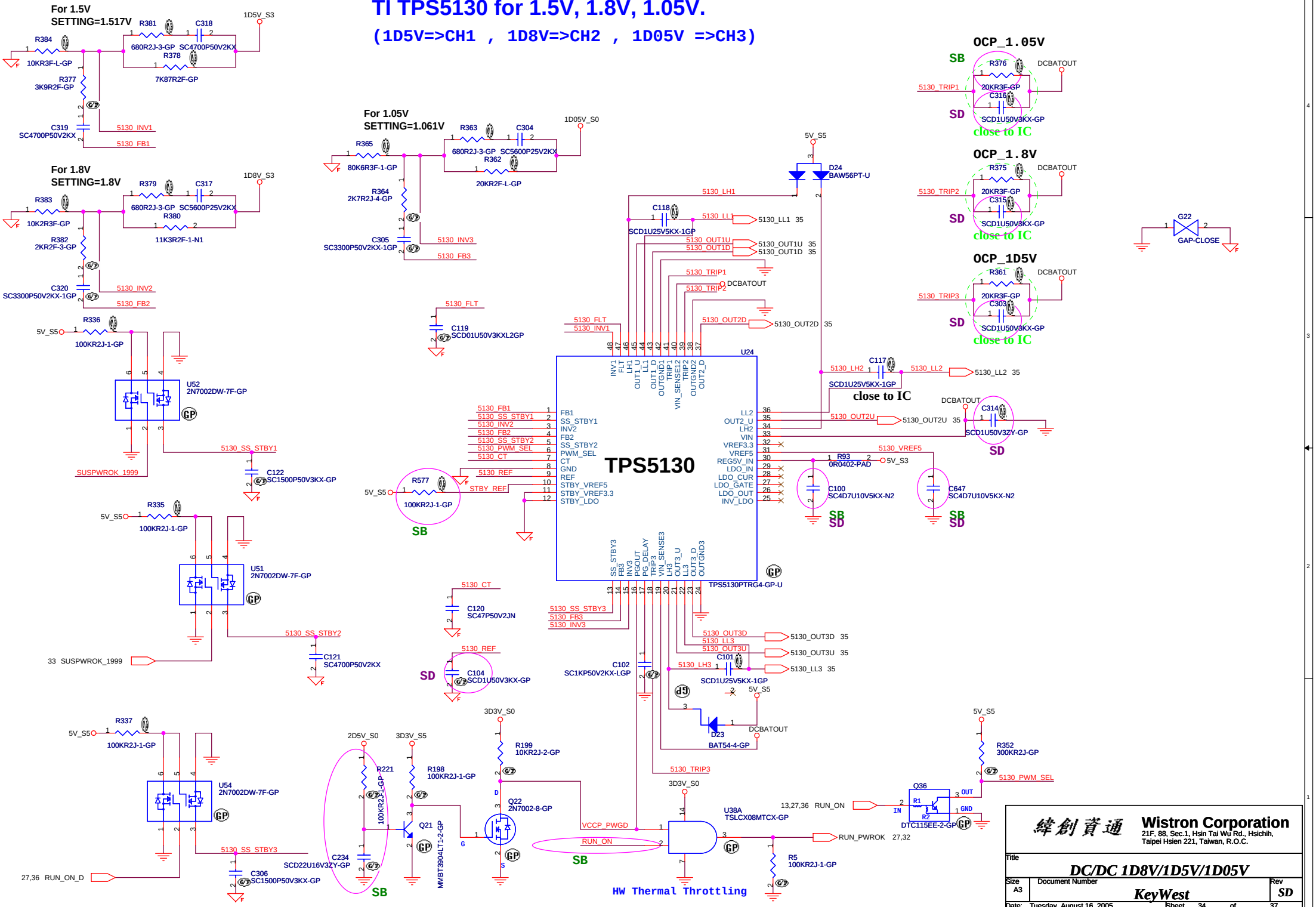
SYSTEM DC/DC 3D3V_S3 / 5V_S3



TI TPS5130 for 1.5V, 1.8V, 1.05V.

(1D5V=>CH1 , 1D8V=>CH2 , 1D05V =>CH3)

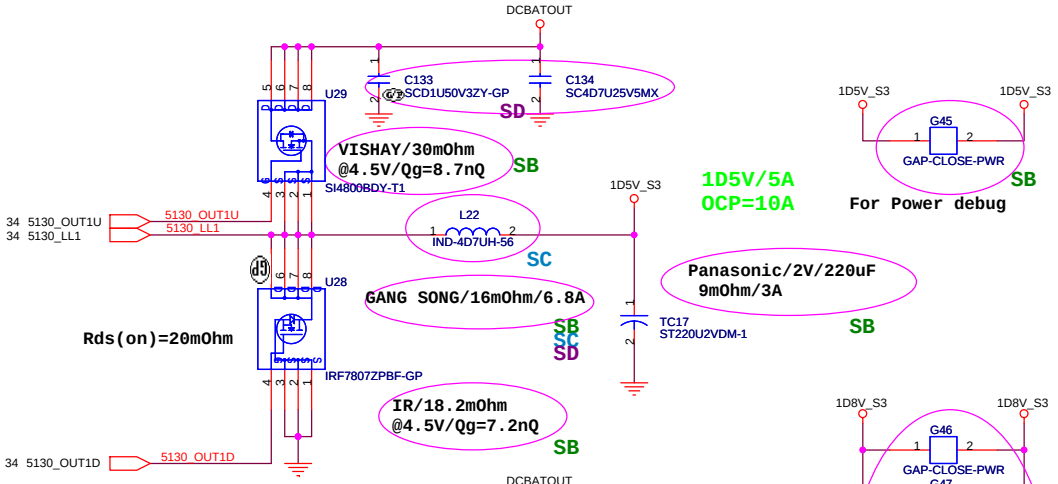


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***DC/DC 1D8V/1D5V/1D05V***		
Size A3	Document Number ***KeyWest***		Rev ***SD***
Date: Tuesday, August 16, 2005	Sheet 34 of 37		

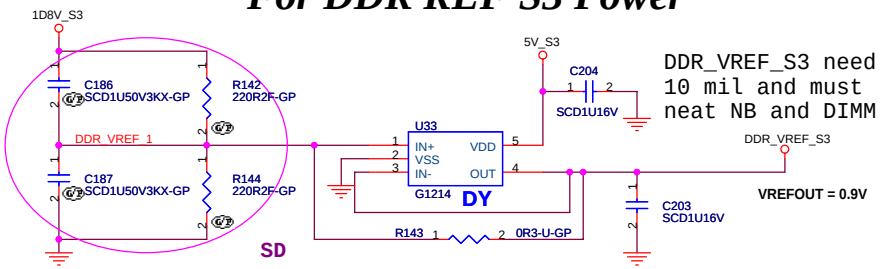
TI TPS5130 for 1.5V, 1.8V, 1.05V

(1D5V=>CH1 , 1D8V=>CH2 , 1D05V =>CH3)

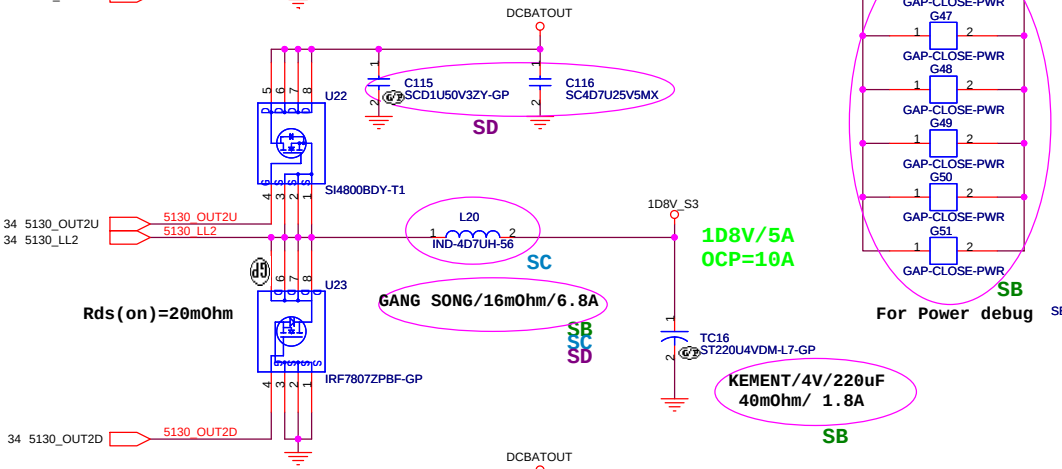
13,31,33,34,36,37 DCBATOUT
13,32,33,34,36 5V_S5
10,34,36,37 1D05V_S0
7,9,10,11,12,16,34,36,37 1D8V_S3
13,14,17,18,19,20,24,25,27,28,32,36,37 5V_S0
12,36 0D9V_S0
17,34,36 1D5V_S3



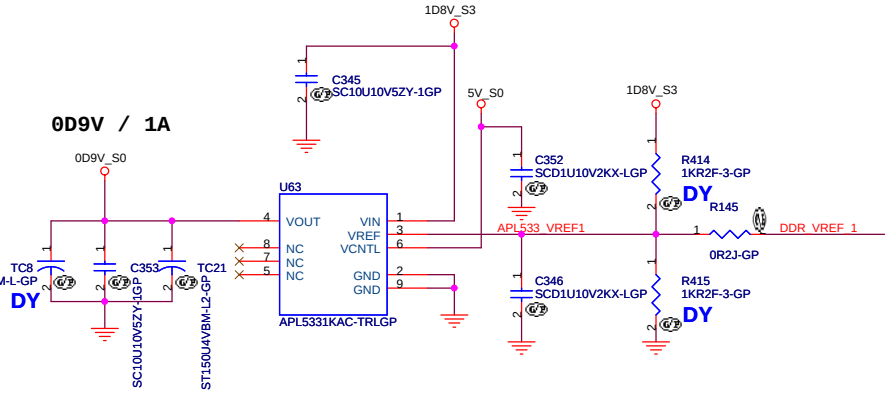
For DDR REF S3 Power



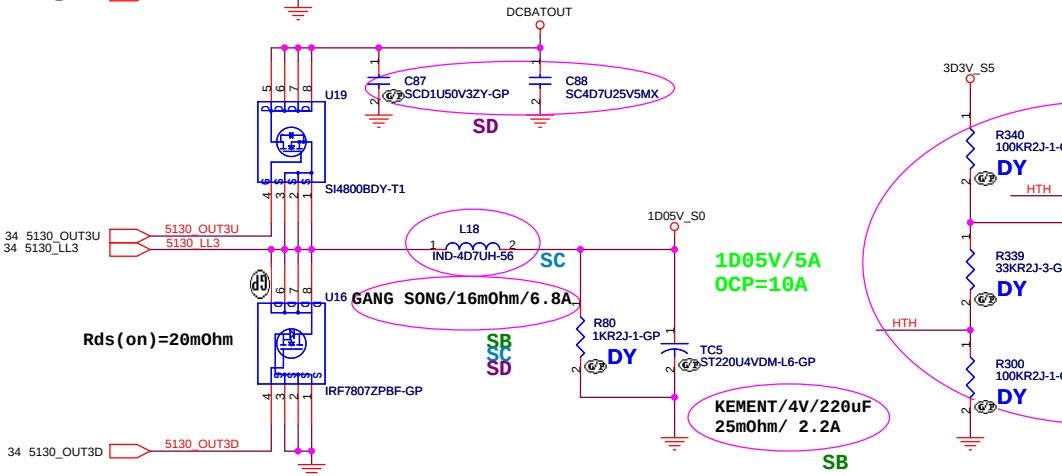
DDR_VREF_S3 need
10 mil and must
neat NB and DIMM

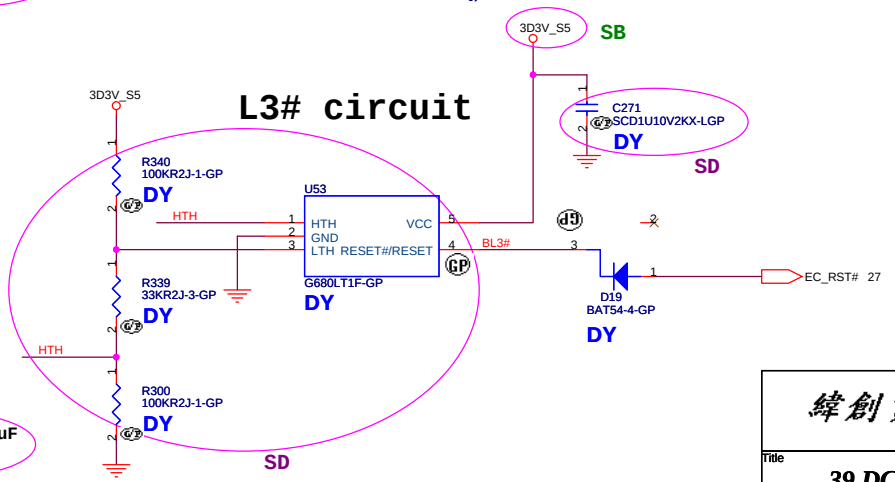


Power budget:0.9V/2.2Apeak (For DDR2_VTT)



L3# circuit





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Title: *39.DC/DC 1D8V/1D5V/1D05V-2*

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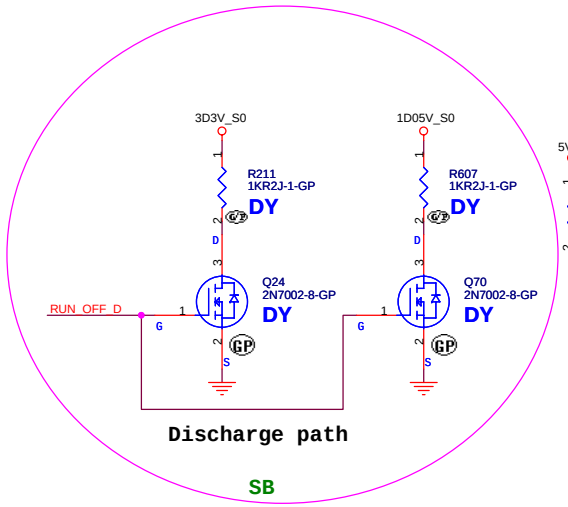
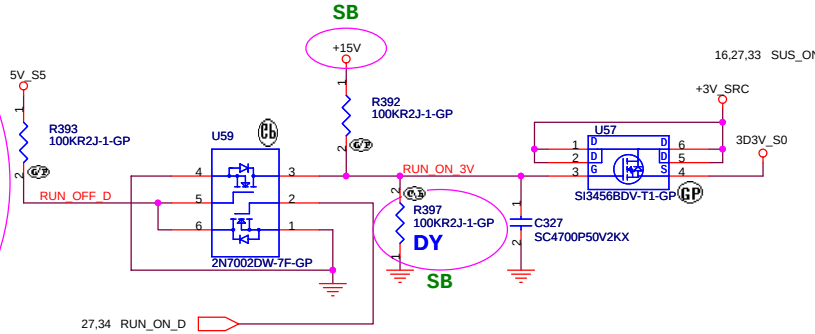
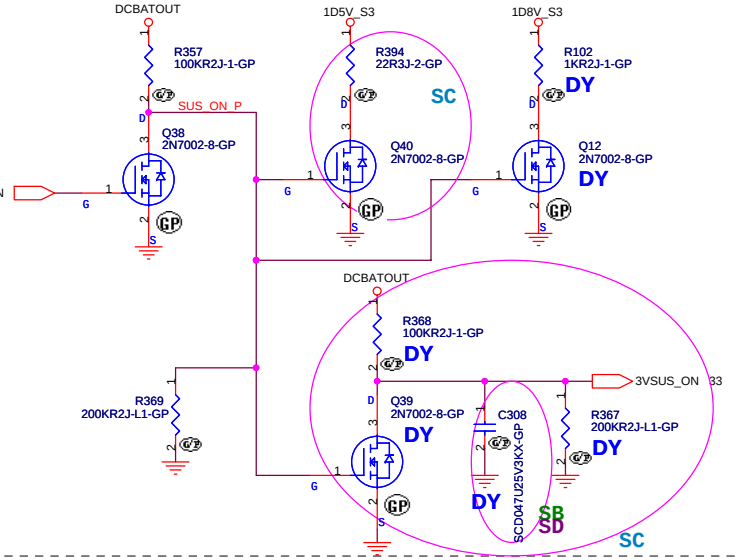
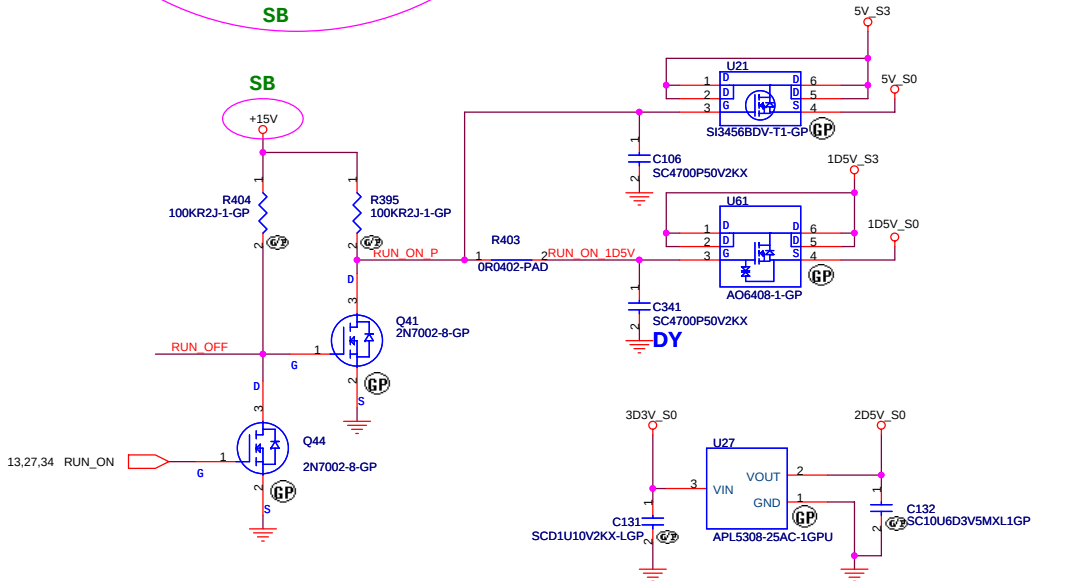
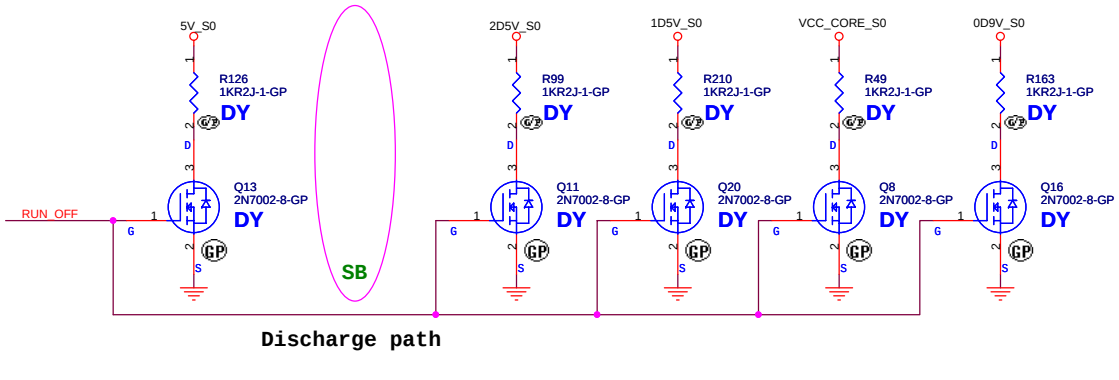
Run Power



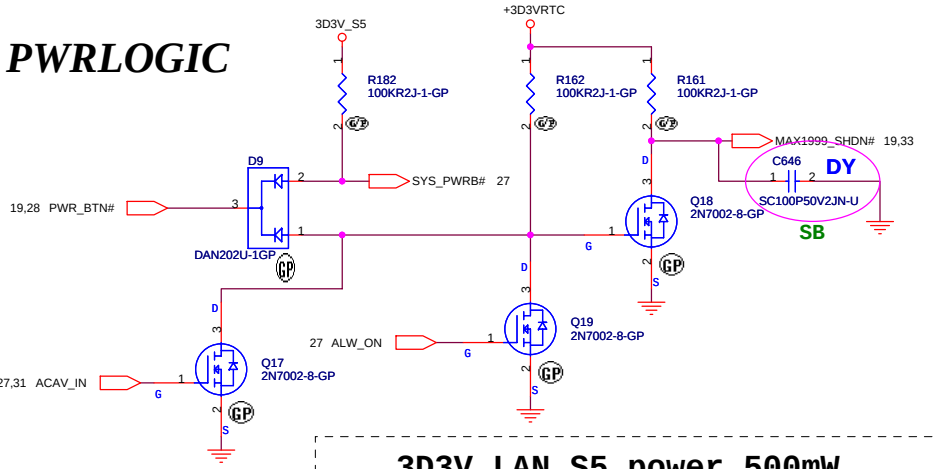




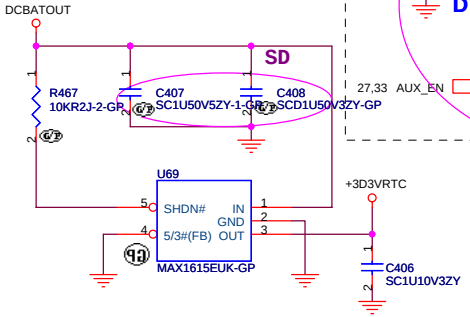




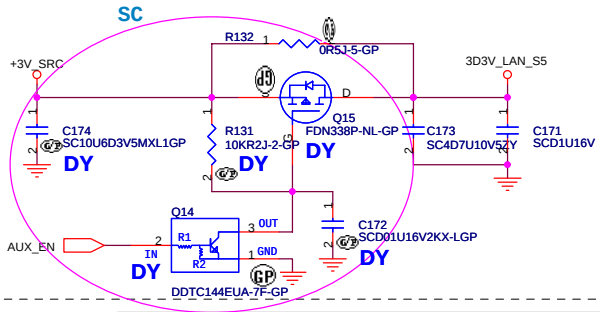
PWRLOGIC



+3D3VRTC



3D3V_LAN_S5 power 500mW



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Title	**PWRPLANE&PWRLOGIC**	
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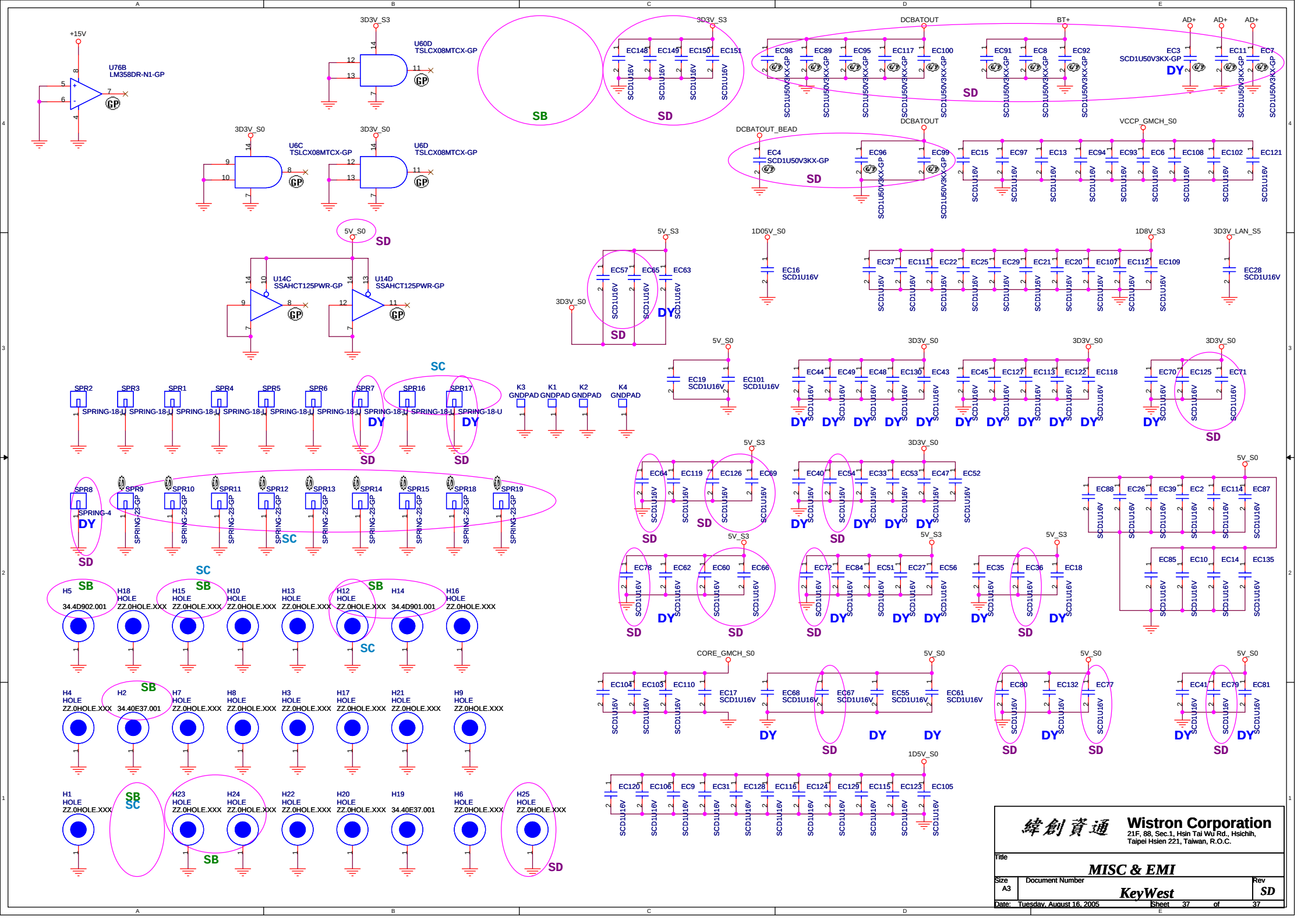
+15V
U76B
LM358DR-N1-GP
3D3V_S3
U60D
TSLCX08MTCX-GP
SB
EC148 EC149 EC150 EC151
SCD1U16V
SD
DCBATOUT
EC98 EC89 EC95 EC117 EC100
SCD1U50V3KX-GP
SD
BT+
EC91 EC8 EC92
AD+
EC3 EC11 EC7
SCD1U50V3KX-GP
DY
3D3V_S0
U6C
TSLCX08MTCX-GP
U6D
TSLCX08MTCX-GP
DCBATOUT_BEAD
EC4
SCD1U50V3KX-GP
SD
EC96 EC99
VCCP_GMCH_S0
EC15 EC97 EC13 EC94 EC93 EC6 EC108 EC102 EC121
SCD1U16V
5V_S0
SD
U14C
SSAHCT125PWR-GP
U14D
SSAHCT125PWR-GP
5V_S3
EC57 EC65 EC63
DY
1D05V_S0
EC16
SCD1U16V
1D8V_S3
EC37 EC111 EC22 EC25 EC29 EC21 EC20 EC107 EC112 EC109
3D3V_LAN_S5
EC28
SCD1U16V
SC
SPR2 SPR3 SPR1 SPR4 SPR5 SPR6 SPR7 SPR16 SPR17
SPRING-18-U
K3 K1 K2 K4
GNDPAD
EC19 EC101
SCD1U16V
EC44 EC49 EC48 EC130 EC43
EC45 EC127 EC113 EC122 EC118
EC70 EC125 EC71
SPR8
SPRING-4
SPR9 SPR10 SPR11 SPR12 SPR13 SPR14 SPR15 SPR18 SPR19
SPRING-23-GP
EC64 EC119 EC126 EC69
EC40 EC54 EC33 EC53 EC47 EC52
EC88 EC26 EC39 EC2 EC114 EC87
EC85 EC10 EC14 EC135
EC78 EC62 EC60 EC66
EC72 EC84 EC51 EC27 EC56
EC35 EC36 EC18
H5 34.4D902.001
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H2 34.40E37.001
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H25 HOLE ZZ.0HOLE.XXX
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EC68 EC67 EC55 EC61
EC80 EC132 EC77
EC41 EC79 EC81
1D5V_S0
EC120 EC106 EC9 EC31 EC128 EC116 EC124 EC129 EC115 EC123 EC105
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Taipei Hsien 221, Taiwan, R.O.C.
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MISC & EMI
Size A3
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KeyWest
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