

Compal Model Name: KAM01 (DIS)
KAM00 (UMA)
PCB NO: DA80000E800 LA-5162P R02 (X01) (DIS & UMA)
BOM P/N: 46170431L11 (DIS)
46170431L01 (UMA)

Liver-Pool 13.3"

Compal Confidential

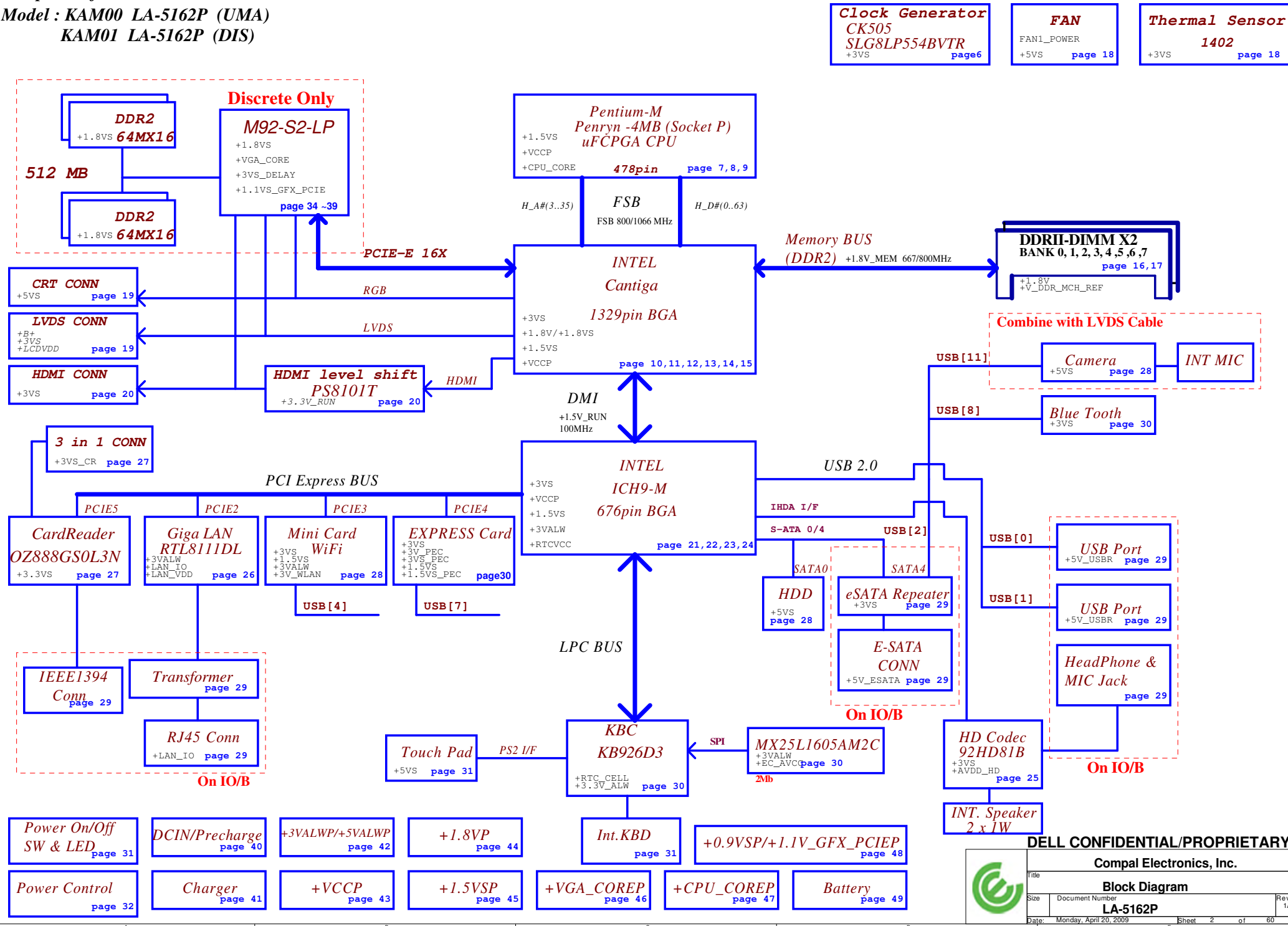
Schematic Document

Penryn + Cantiga(GM45) + ICH9-M

2009 / 04 / 20 Rev:0.2 (X01)

@ : Nopop Component
1@ : UMA Only
2@ : Discrete Only
ME@ : Mechanical Component

Main-Board TYPE	BOM P/N	BOM CONFIGURATION
DIS M/B	46170431L11	2@+ME@
UMA M/B	46170431L01	1@+ME@



Clock Generator
CK505
SLG8LP554BVTR
+3VS
page 6

FAN
FAN1_POWER
+5VS
page 18

Thermal Sensor
1402
+3VS
page 18

Voltage Rails O MEANS ON X MEANS OFF

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +GPU_CORE +1.8VS +1.1VS_GFX_PCIE +0.9VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

ID	BOARD ID	Ra	Rb	Vab
0	0.1(X00)	NC	0	0V
1	0.2(X01)	100K	9.09K	0.25V
2	0.3(X02)	100K	20K	0.50V
3	1.0(A00)	100K	37.4K	0.82V

Symbol Note :

 : means Digital Ground

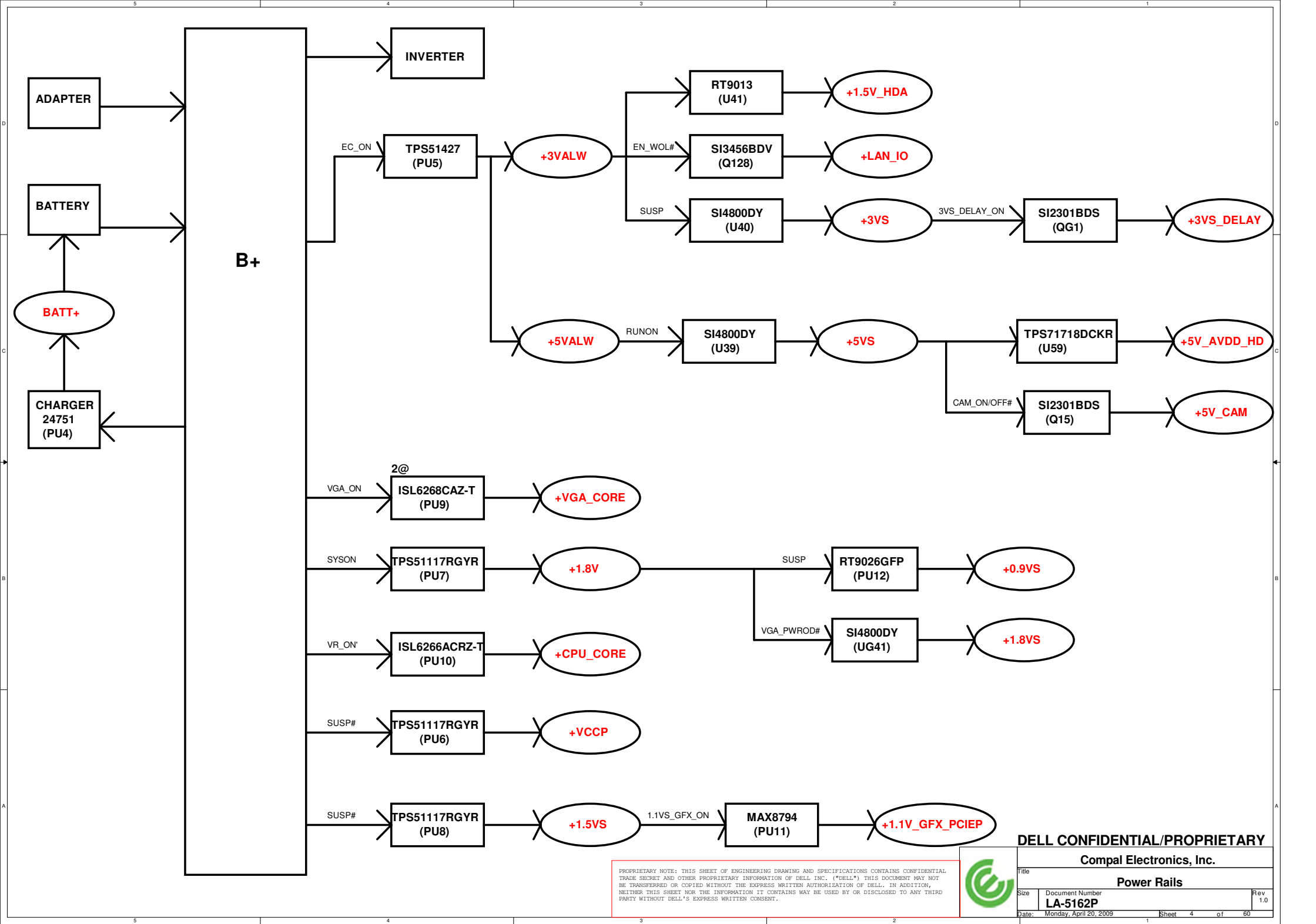
 : means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

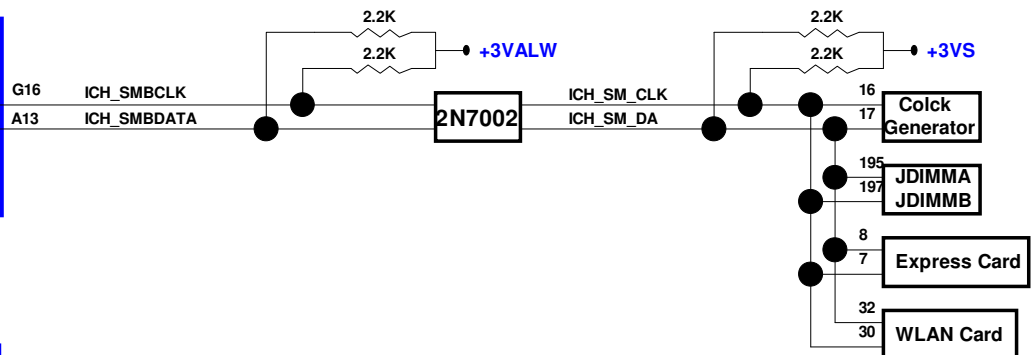
SATA	DESTINATION
Lane 0	HDD
Lane 1	NONE
Lane 4	ESATA
Lane 5	NONE

PCI EXPRESS	DESTINATION
Lane 1	NONE
Lane 2	GIGA LAN
Lane 3	WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER
Lane 6	NONE

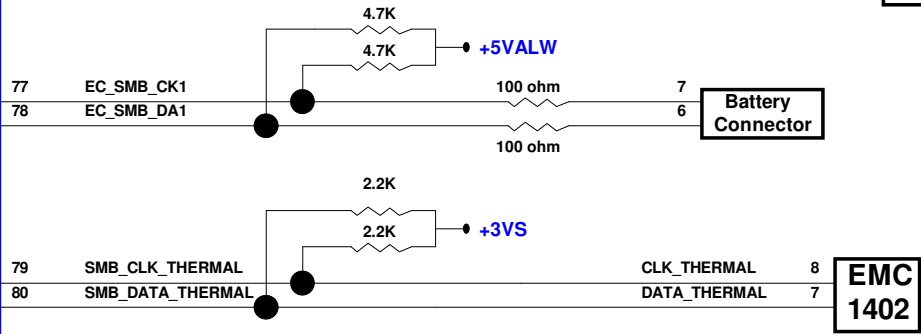
ICH9-M	USB PORT#	DESTINATION
	0	JUSBR1
	1	JUSBR2
	2	JUSBR3(E-SATA)
	3	NONE
	4	WLAN
	5	NONE
	6	NONE
	7	Express card
	8	Bluetooth
	9	NONE
	10	NONE
	11	CAMERA



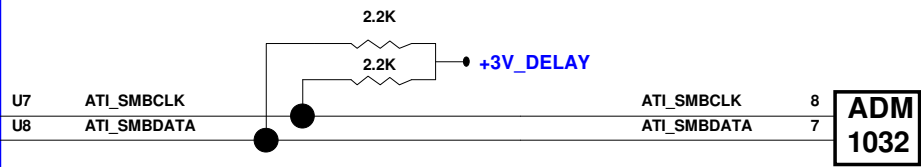
ICH9-M



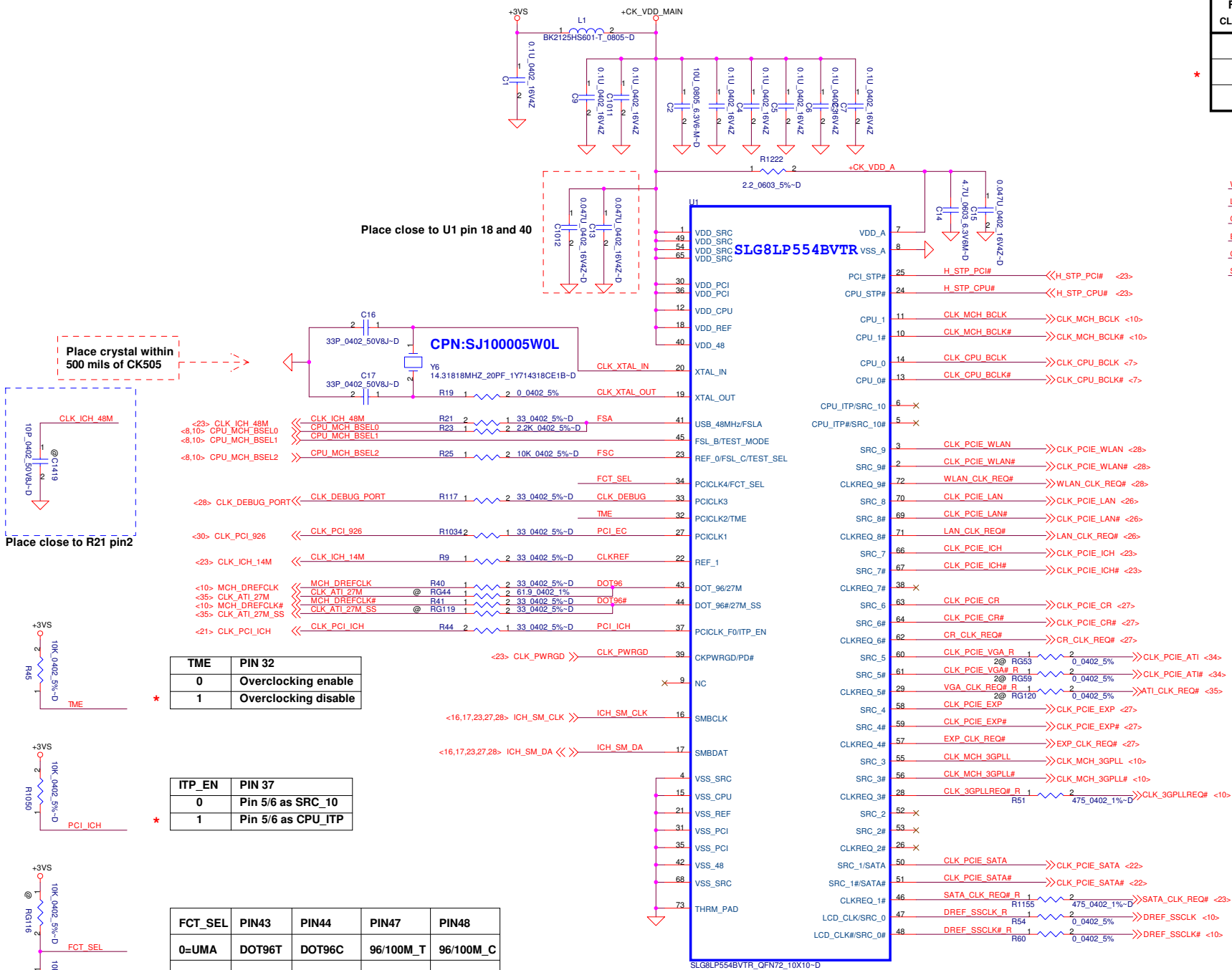
ENE KB926



ATI M92-S2



FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3



CIS Link:OK
CPN:SA000026T0L

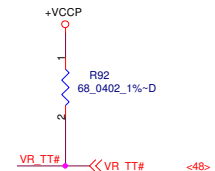
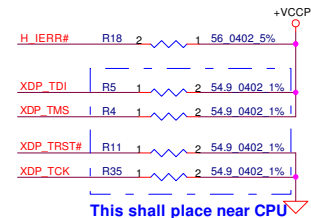
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Compal Electronics, Inc.



Title		Clock GEN. with internal terminations	
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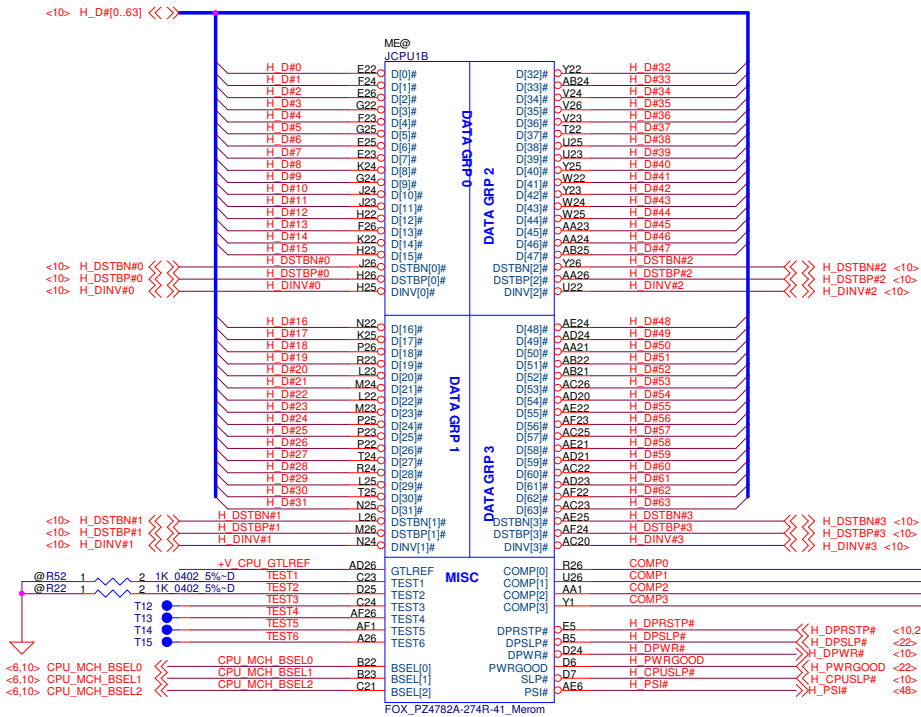


H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

FOX_PZ4782A-274R-41_Merom

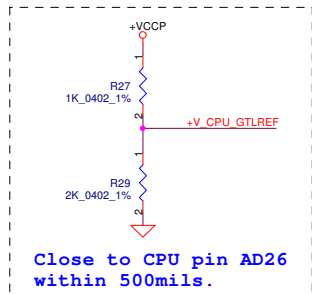
CIS Link:OK
12/29

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Size	Document Number	Rev		0.2	
Custor	LA-5162P	Date		Monday, April 20, 2009	
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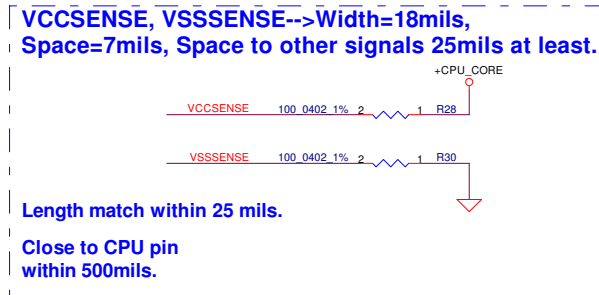
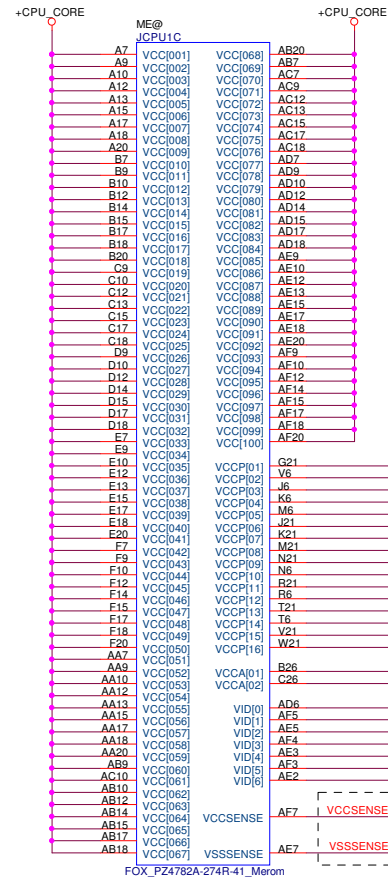


layout note: Rout H_DPRSTP# from ICH9 to IMPV6 then to GMCH & CPU
 layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TP's

FSB Frequency	BSEL[2]	BSEL[1]	BSEL[0]
667MHz	0	1	1
800MHz	0	1	0
1066MHz	0	0	0



Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils

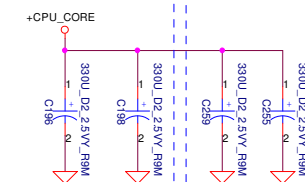
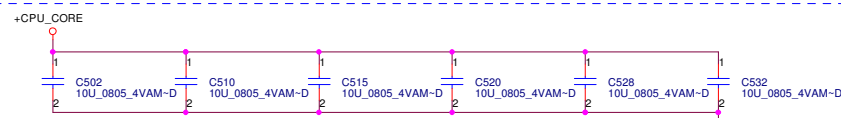
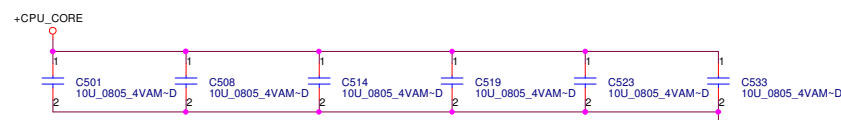
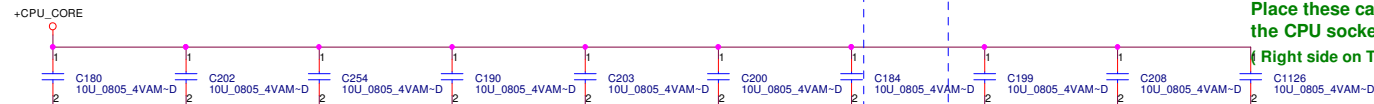
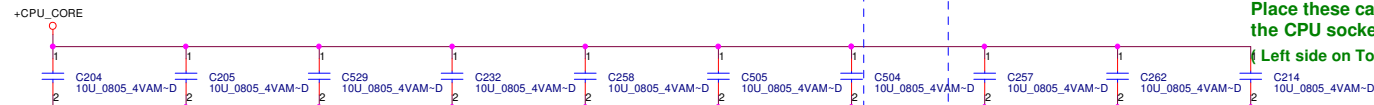


ME@	ICPU1D		
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R5
A16	VSS[005]	VSS[086]	R22
A19	VSS[006]	VSS[087]	R25
A23	VSS[007]	VSS[088]	T1
AF2	VSS[008]	VSS[089]	T4
B6	VSS[009]	VSS[090]	T23
B8	VSS[010]	VSS[091]	T26
B11	VSS[011]	VSS[092]	U3
B13	VSS[012]	VSS[093]	U6
B16	VSS[013]	VSS[094]	U21
B19	VSS[014]	VSS[095]	U24
B21	VSS[015]	VSS[096]	V2
B24	VSS[016]	VSS[097]	V5
C5	VSS[017]	VSS[098]	V22
C8	VSS[018]	VSS[099]	V25
C11	VSS[019]	VSS[100]	W1
C14	VSS[020]	VSS[101]	W4
C16	VSS[021]	VSS[102]	W23
C19	VSS[022]	VSS[103]	W26
C22	VSS[023]	VSS[104]	V3
C25	VSS[024]	VSS[105]	V6
D1	VSS[025]	VSS[106]	Y21
D4	VSS[026]	VSS[107]	Y24
D8	VSS[027]	VSS[108]	AA2
D11	VSS[028]	VSS[109]	AA5
D13	VSS[029]	VSS[110]	AA8
D16	VSS[030]	VSS[111]	AA11
D19	VSS[031]	VSS[112]	AA14
D23	VSS[032]	VSS[113]	AA16
D26	VSS[033]	VSS[114]	AA19
E3	VSS[034]	VSS[115]	AA22
E6	VSS[035]	VSS[116]	AA25
E8	VSS[036]	VSS[117]	AB1
E11	VSS[037]	VSS[118]	AB4
E14	VSS[038]	VSS[119]	AB8
E16	VSS[039]	VSS[120]	AB11
E19	VSS[040]	VSS[121]	AB13
E21	VSS[041]	VSS[122]	AB16
E24	VSS[042]	VSS[123]	AB19
F5	VSS[043]	VSS[124]	AB23
F8	VSS[044]	VSS[125]	AB26
F11	VSS[045]	VSS[126]	AC3
F13	VSS[046]	VSS[127]	AC6
F16	VSS[047]	VSS[128]	AC8
F19	VSS[048]	VSS[129]	AC11
F2	VSS[049]	VSS[130]	AC14
F22	VSS[050]	VSS[131]	AC16
F25	VSS[051]	VSS[132]	AC19
G4	VSS[052]	VSS[133]	AC21
G11	VSS[053]	VSS[134]	AC24
G23	VSS[054]	VSS[135]	AD2
G26	VSS[055]	VSS[136]	AD5
H3	VSS[056]	VSS[137]	AD8
H6	VSS[057]	VSS[138]	AD11
H21	VSS[058]	VSS[139]	AD13
H24	VSS[059]	VSS[140]	AD16
J2	VSS[060]	VSS[141]	AD19
J5	VSS[061]	VSS[142]	AD22
J22	VSS[062]	VSS[143]	AD25
J25	VSS[063]	VSS[144]	AE1
K1	VSS[064]	VSS[145]	AE4
K4	VSS[065]	VSS[146]	AE8
K23	VSS[066]	VSS[147]	AE11
K26	VSS[067]	VSS[148]	AE14
L3	VSS[068]	VSS[149]	AE16
L6	VSS[069]	VSS[150]	AE19
L21	VSS[070]	VSS[151]	AE23
L24	VSS[071]	VSS[152]	AE26
M2	VSS[072]	VSS[153]	A2
M5	VSS[073]	VSS[154]	AF6
M22	VSS[074]	VSS[155]	AF8
M25	VSS[075]	VSS[156]	AF11
N1	VSS[076]	VSS[157]	AF13
N4	VSS[077]	VSS[158]	AF16
N23	VSS[078]	VSS[159]	AF19
N26	VSS[079]	VSS[160]	AF21
P3	VSS[080]	VSS[161]	A25
	VSS[081]	VSS[162]	AF25
		VSS[163]	

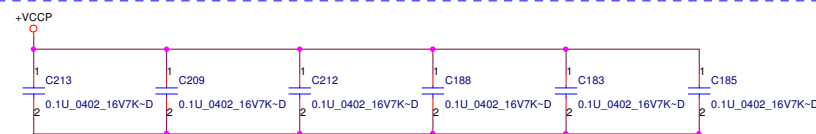
FOX_PZ4782A-274R-41_Merom

High Frequency Decoupling

10uF 0805 X5R -> 85 degree.

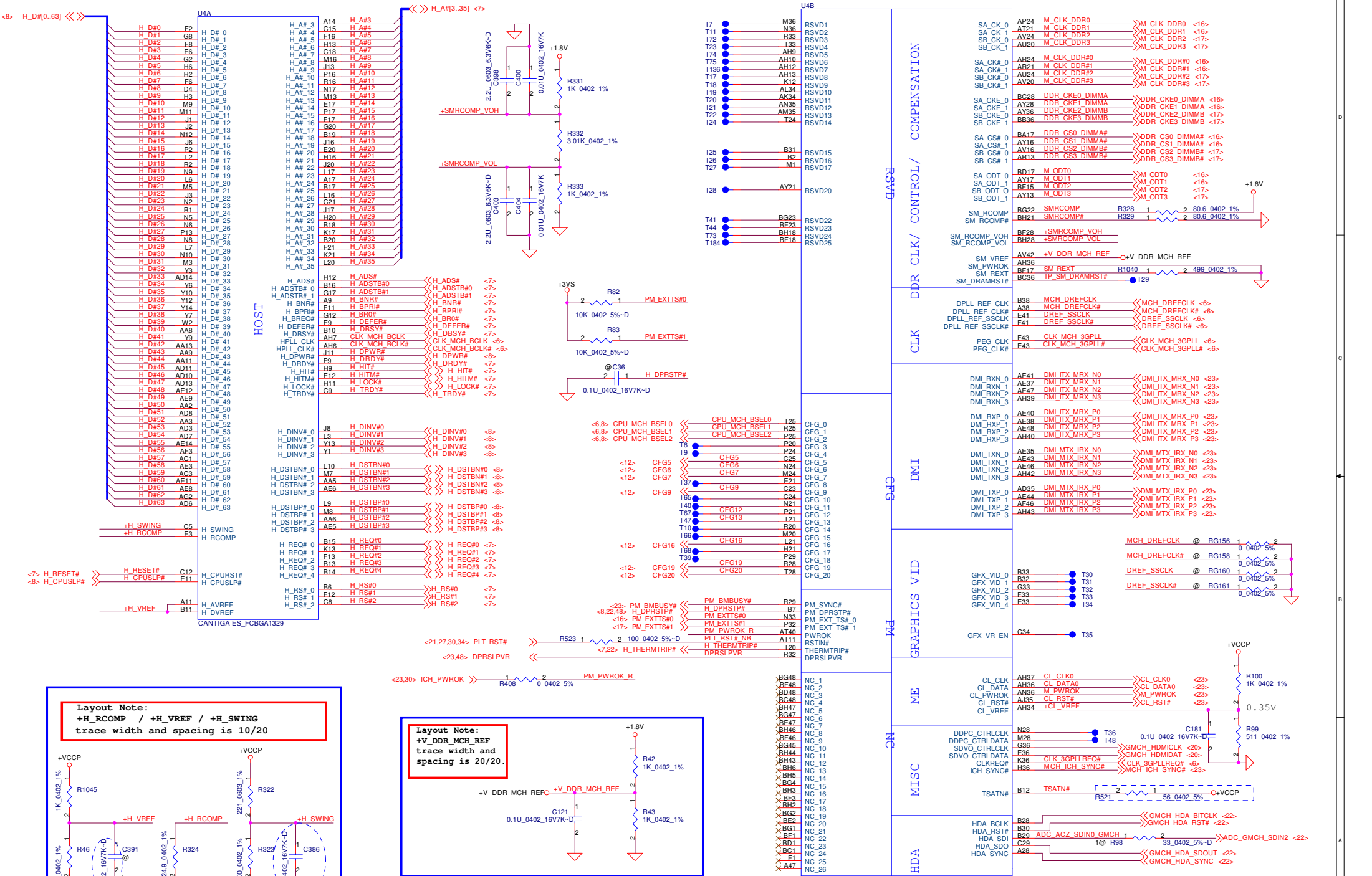


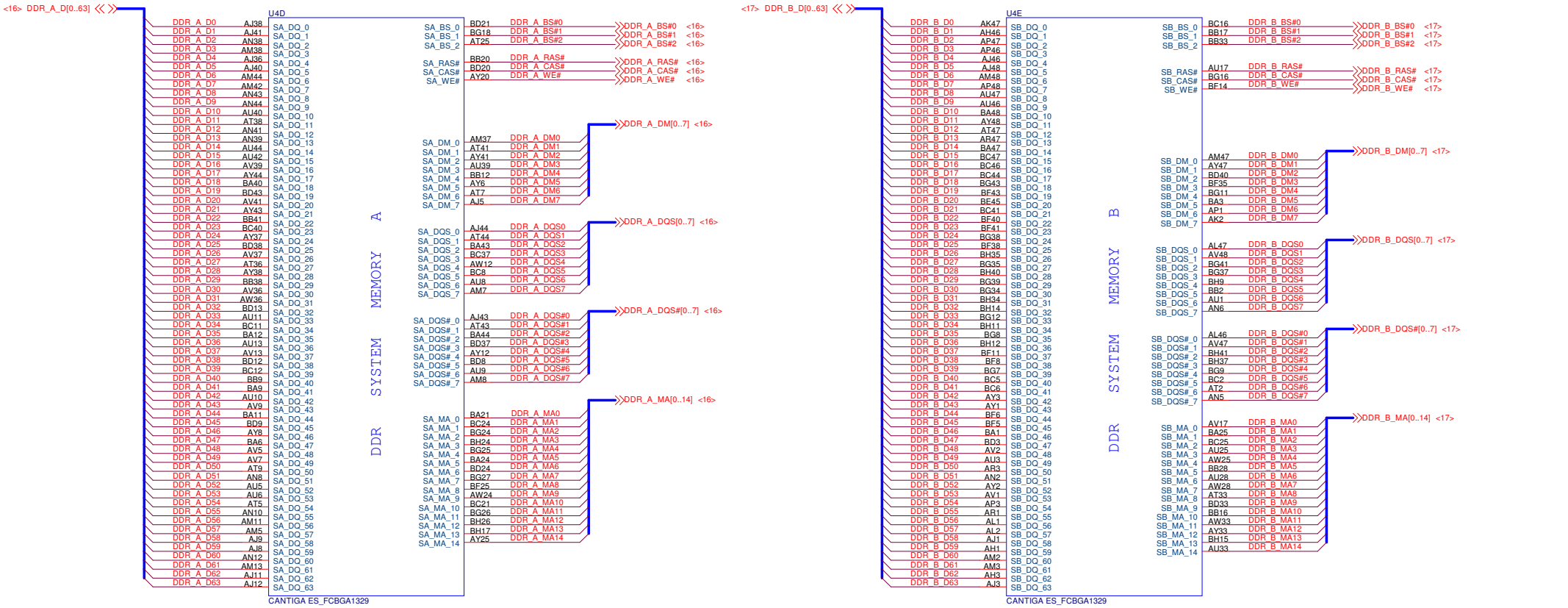
ESR <= 1.5m ohm
Capacitor > 880 uF



Place these inside
socket cavity on L8
(North side
Secondary)

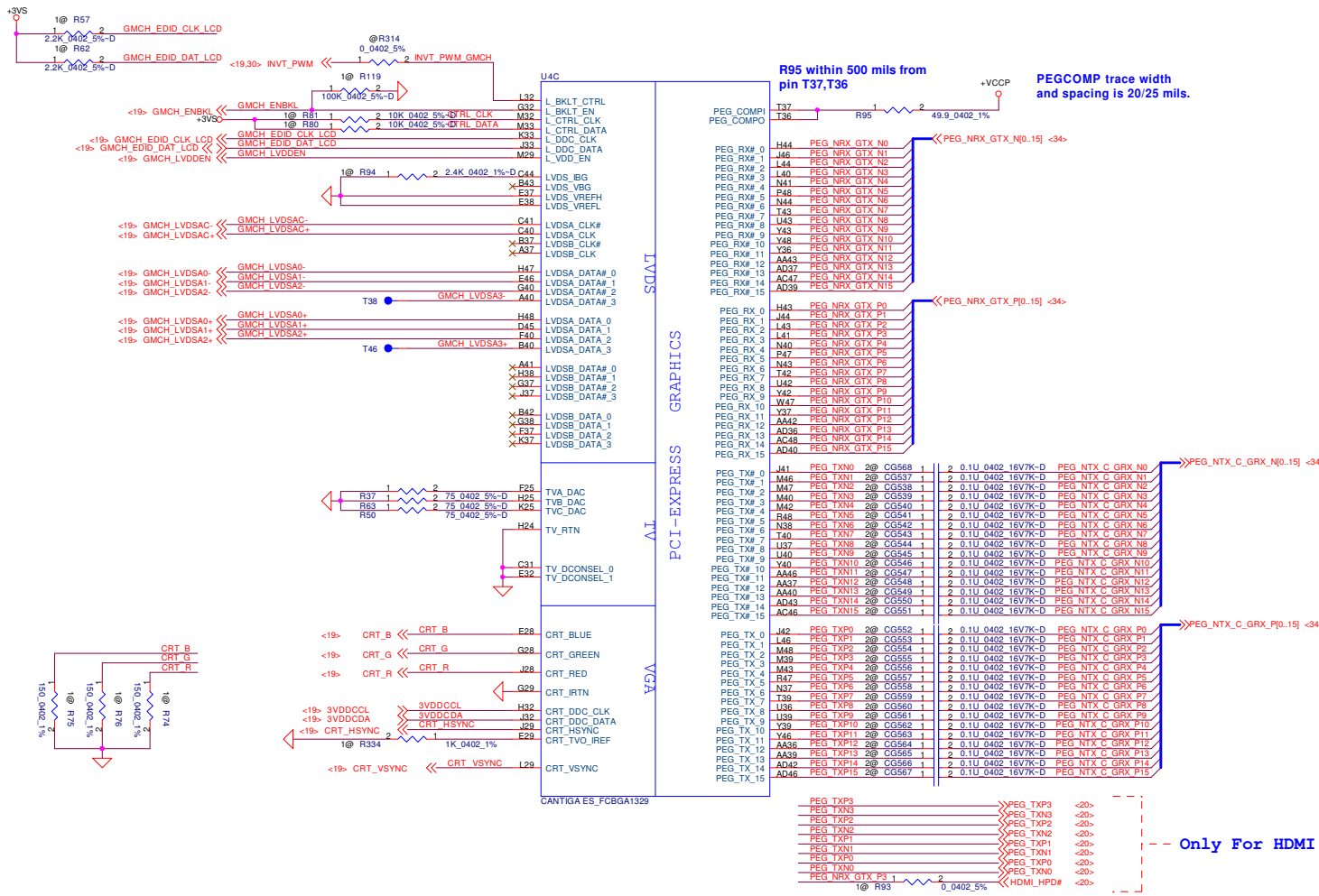
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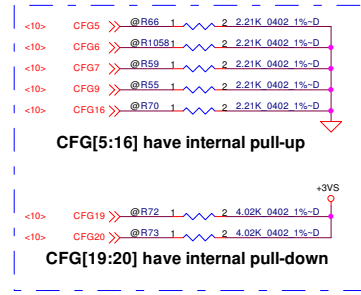
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Size	Document Number	Rev		0.2	
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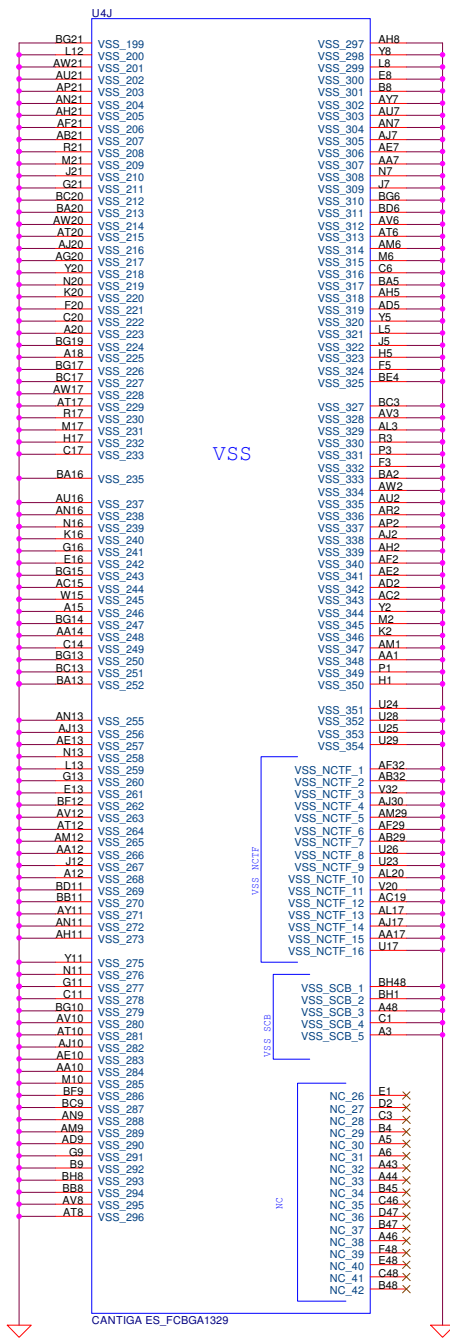
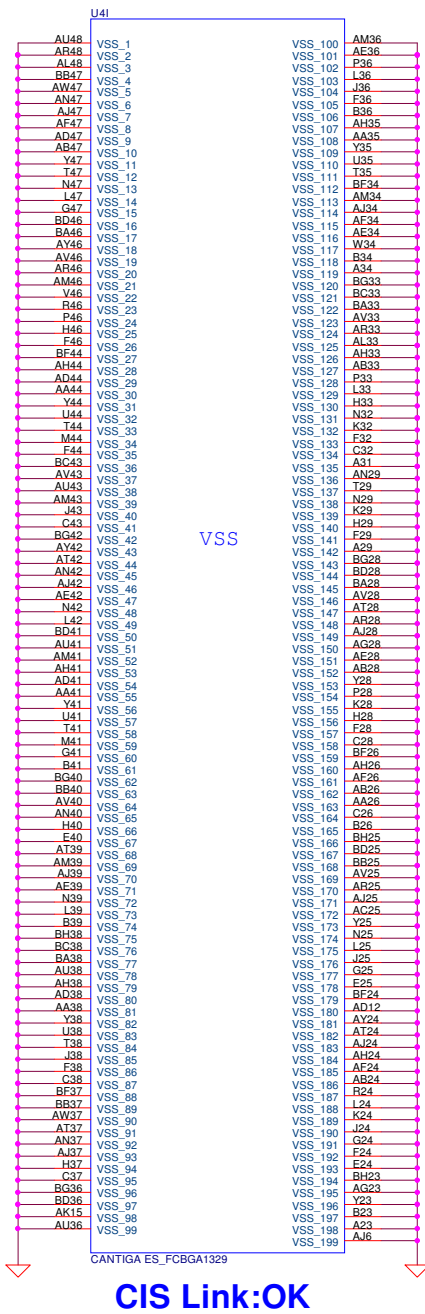


Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz * 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chiper suite with no confidentiality 1=(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu. *

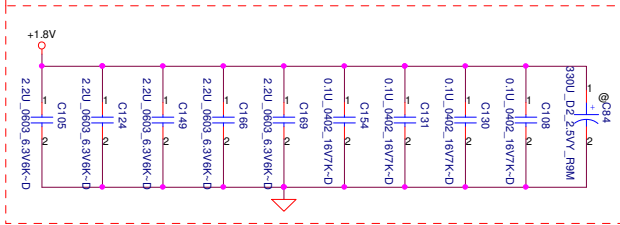


Only For HDMI

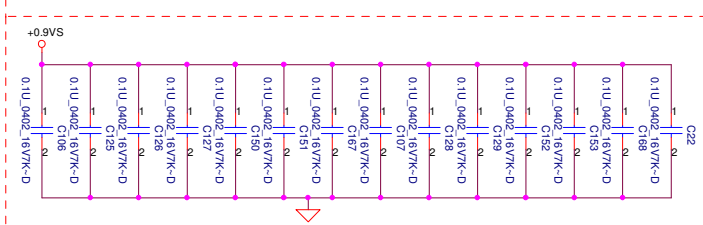


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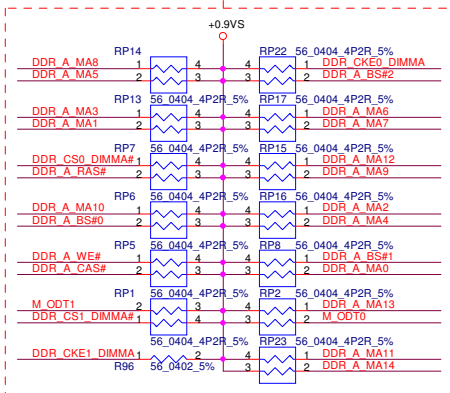
Layout Note:
Place near JDIMMA



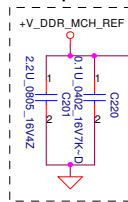
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V



Layout Note:
Place these resistor
closely JDIMMA, all
trace length Max=1.5"



Close to VREF pins of SO-DIMM



<10> DDR_CKE0_DIMMA

<11> DDR_BS#2

<11> DDR_A_BS#0

<11> DDR_A_WE#

<11> DDR_A_CAS#

<10> DDR_CS1_DIMMA#

<10> M_ODT1

<6,17,23,27,28> ICH_SM_DA

<6,17,23,27,28> ICH_SM_CLK

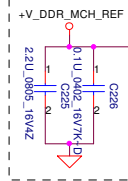
+3VSO

0.1uF 0402 16V7K-D

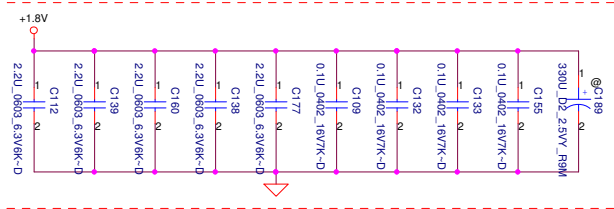
SO-DIMM A
STANDARD TYPE
CIS Link:OK 12/29

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				DDR2 SO-DIMM A	
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				Date	Monday, April 20, 2009
				Sheet	16 of 60
				Rev	0.2

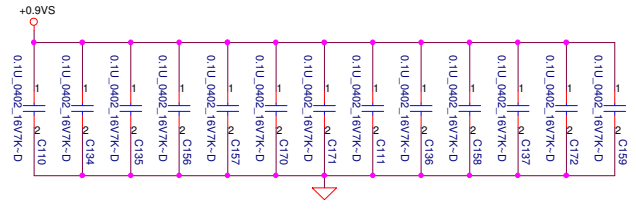
Close to VREF pins of SO-DIMM



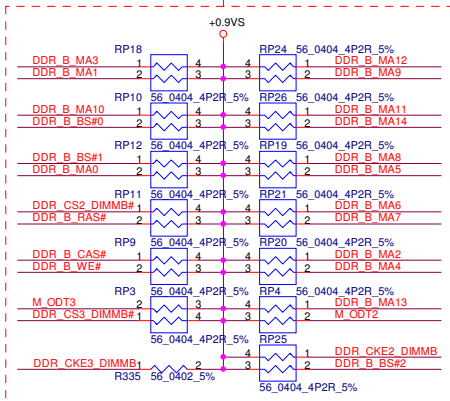
Layout Note:
Place near JDIMMB



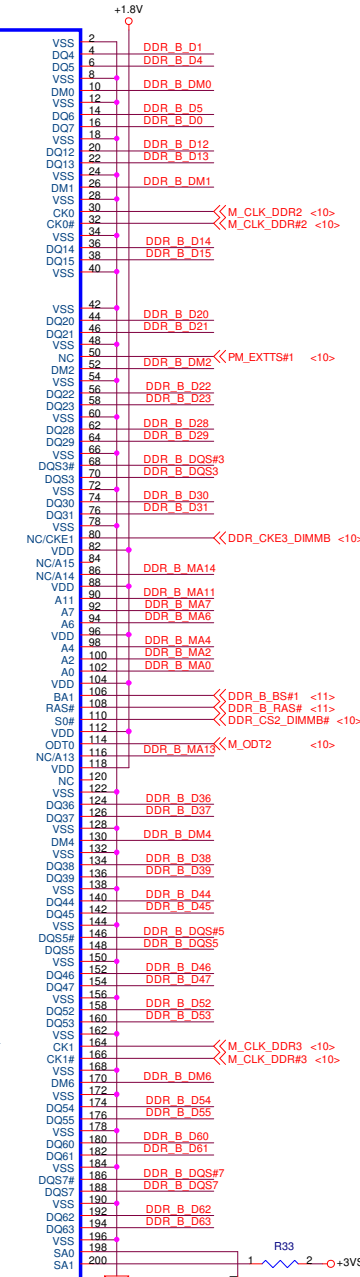
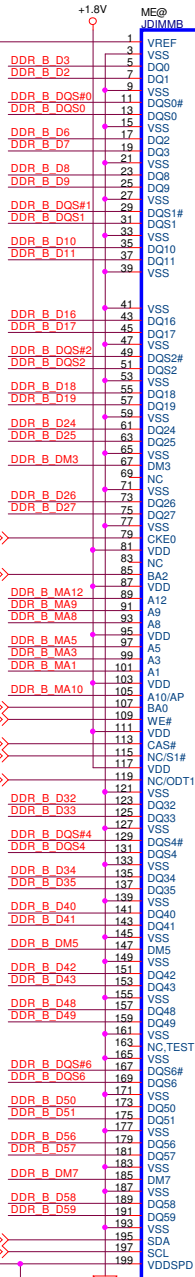
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely JDIMMB,all
trace length Max=1.5"



<10> DDR_CKE2_DIMMB
<11> DDR_BS#2
<11> DDR_BS#0
<11> DDR_BS#1
<11> DDR_BS#2
<11> DDR_BS#3
<10> M_ODT3

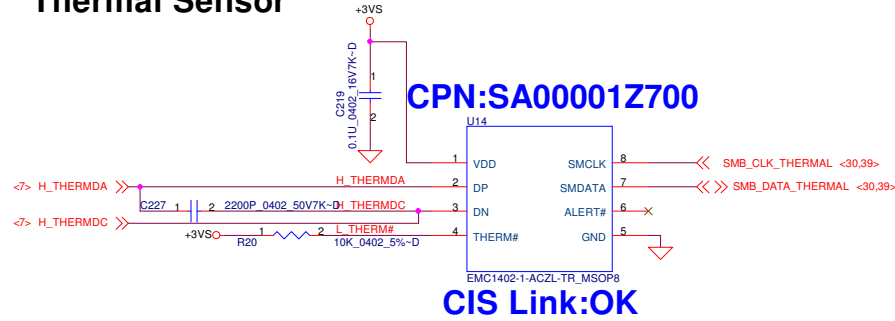


<<>> DDR_B_DQS[0..7] <11>
<<>> DDR_B_DQ[0..63] <11>
<<>> DDR_B_DM[0..7] <11>
<<>> DDR_B_DQS[0..7] <11>
<<>> DDR_B_MA[0..14] <11>

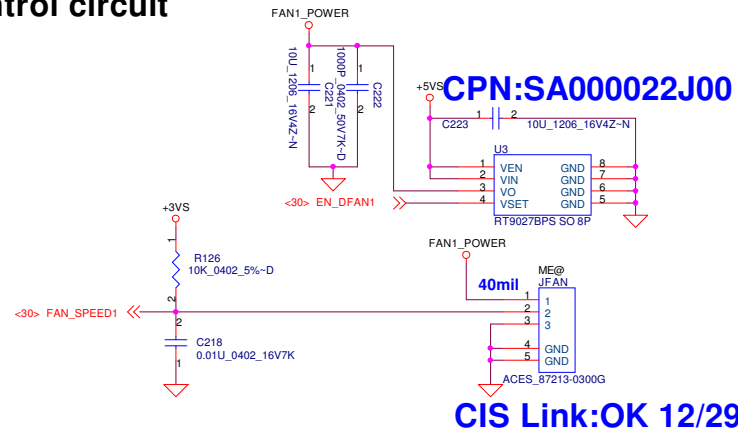
SO-DIMM B
STANDARD TYPE
CIS Link:OK 12/29

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Thermal Sensor



FAN Control circuit



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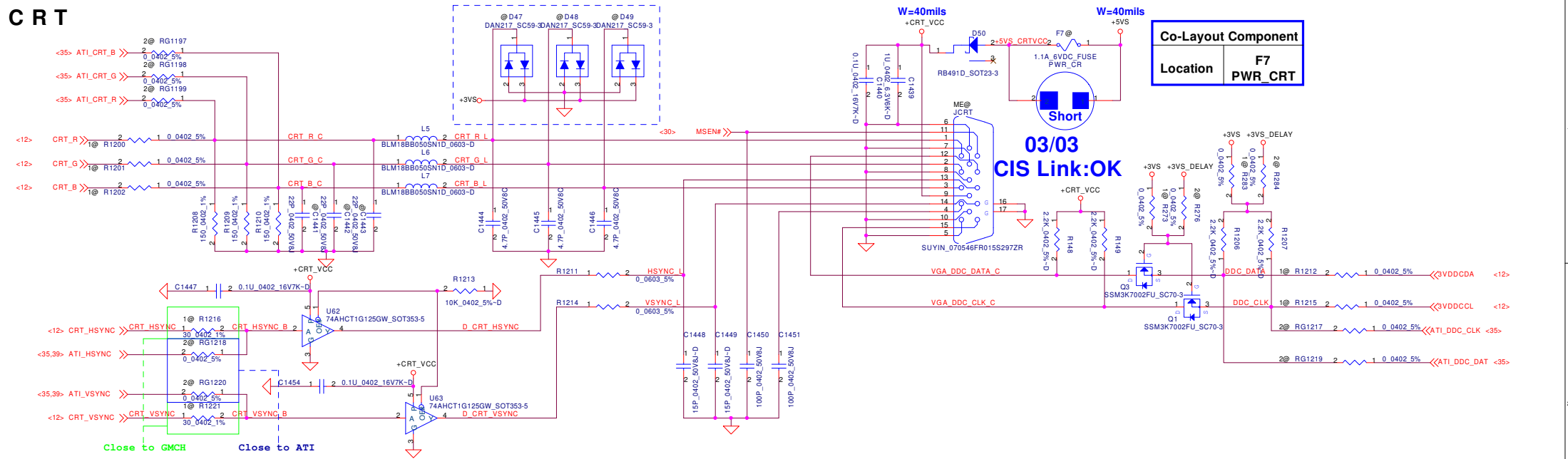


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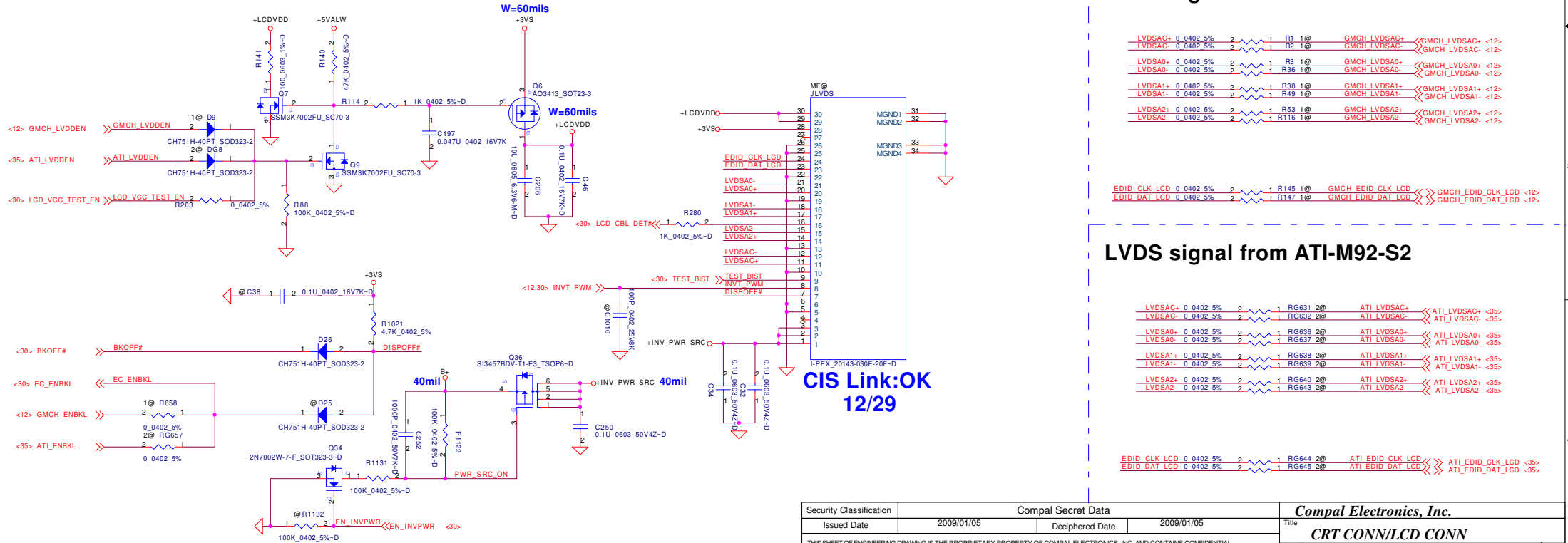
Compal Electronics, Inc.

Title			
FAN & Thermal Sensor			
Size	Document Number		Rev
	LA-5162P		1A
Date:	Monday, April 20, 2009	Sheet 18 of 60	

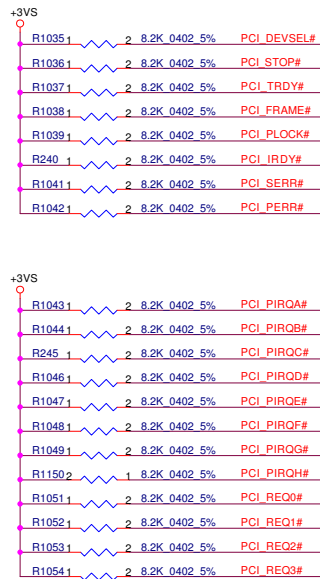
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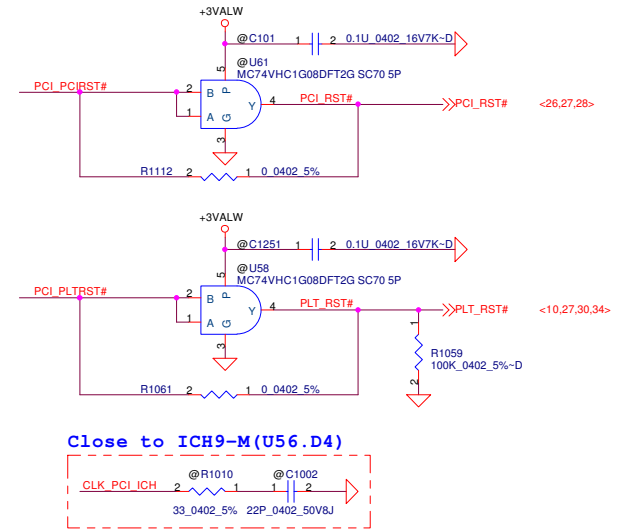
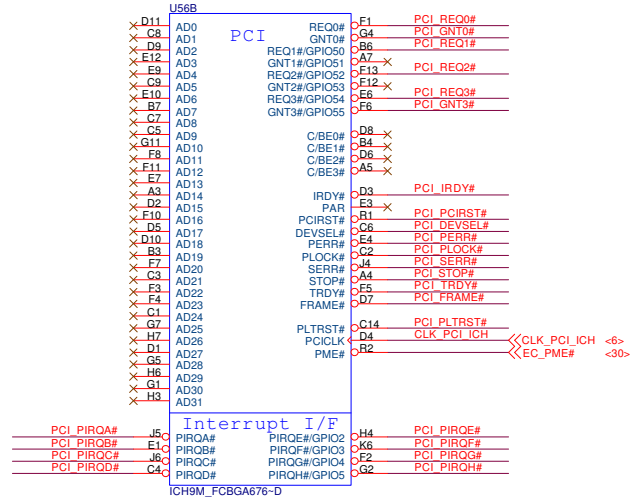
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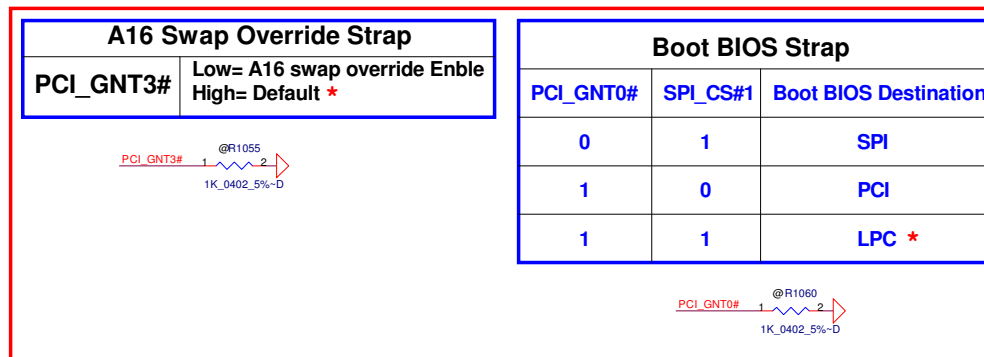
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Issued Date	2009/01/05	Deciphered Date	2009/01/05	Title	
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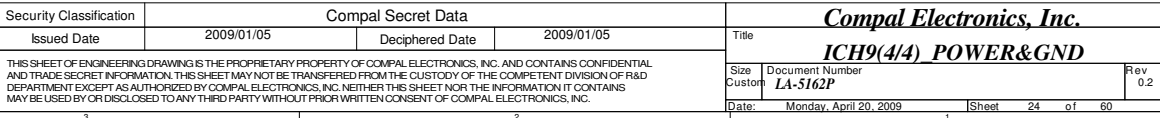


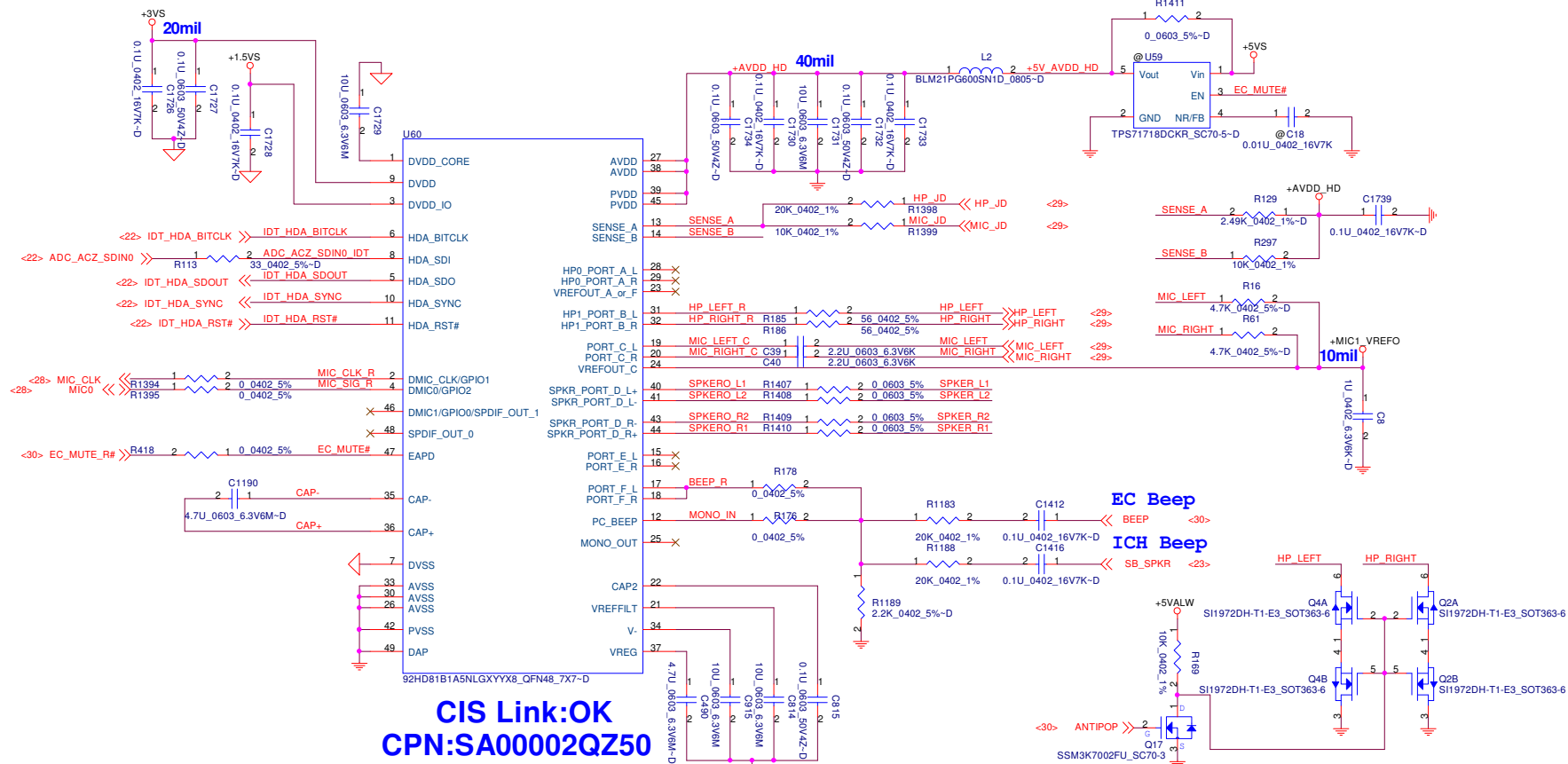
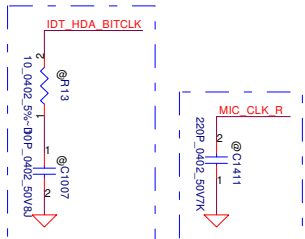
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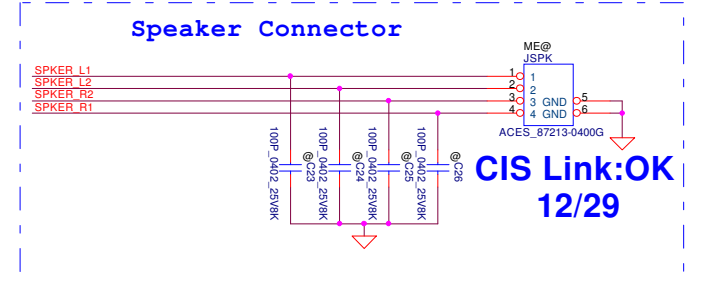
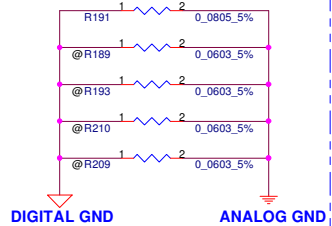






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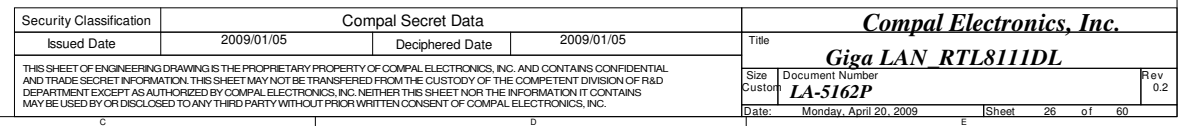
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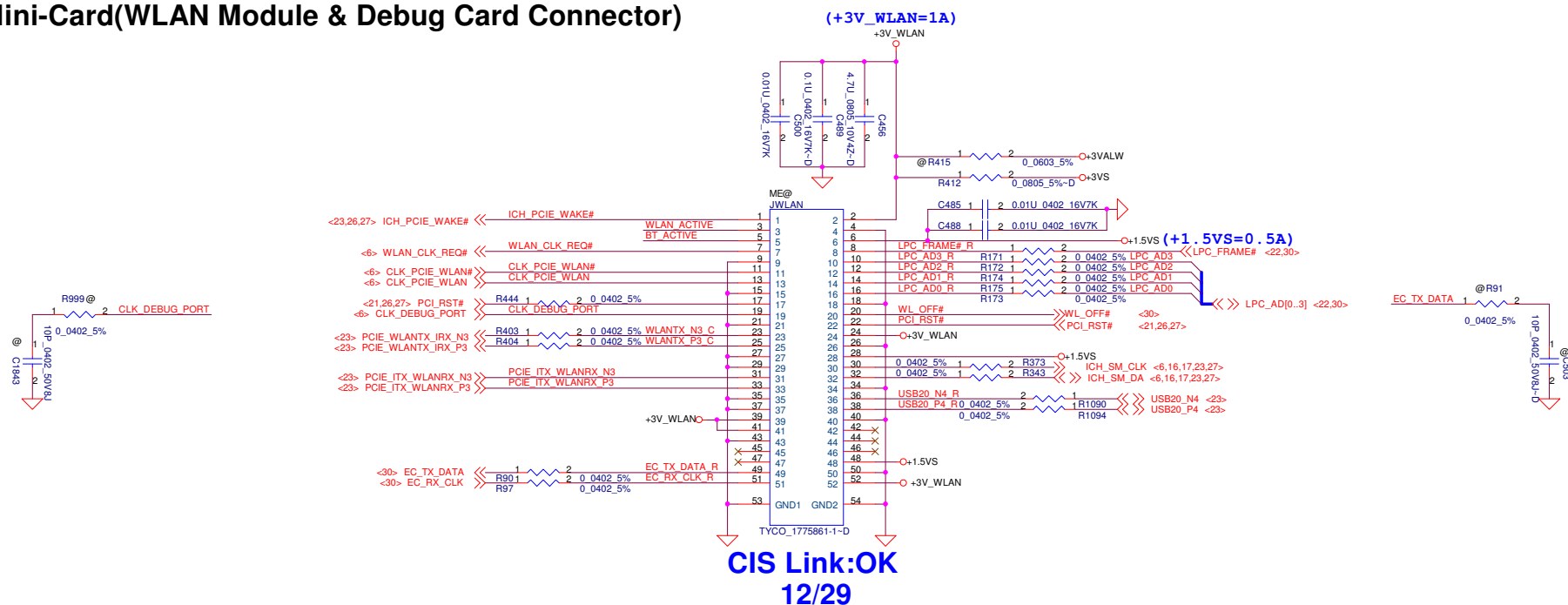
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Issued Date	2009/01/05	Deciphered Date	2009/01/05	Title	P24-Codex 92HD81B / Speaker
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LED[S1-S0]	00	01	10	11
LED0	TX/RX	TX/RX	TX	LINK 10/ACT
LED1	LINK 100	LINK 10/100/1000	LINK	LINK 100/ACT
LED2	LINK 10	LINK 10/100	RX	FULL
LED3	LINK 1000	LINK 1000	FULL	LINK 1000/ACT

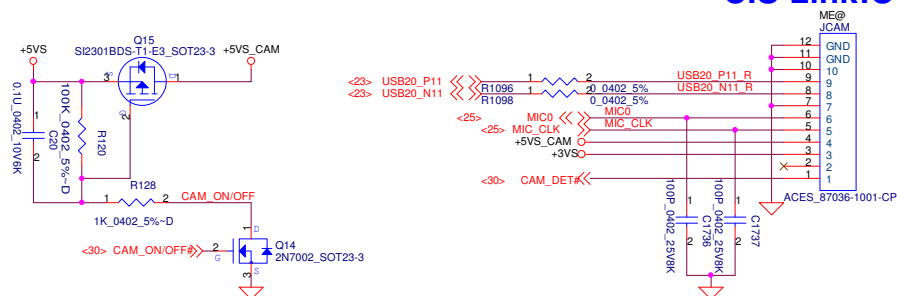
If there is no 93C46, the default value is [1:1].



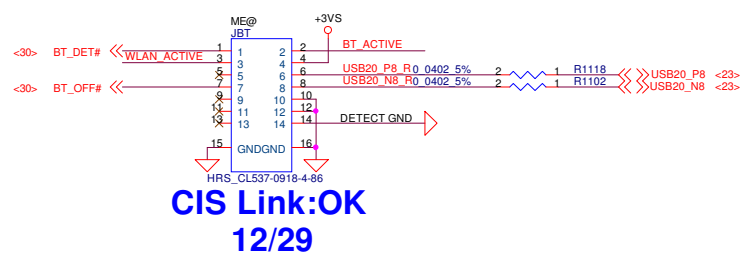
Mini-Card(WLAN Module & Debug Card Connector)



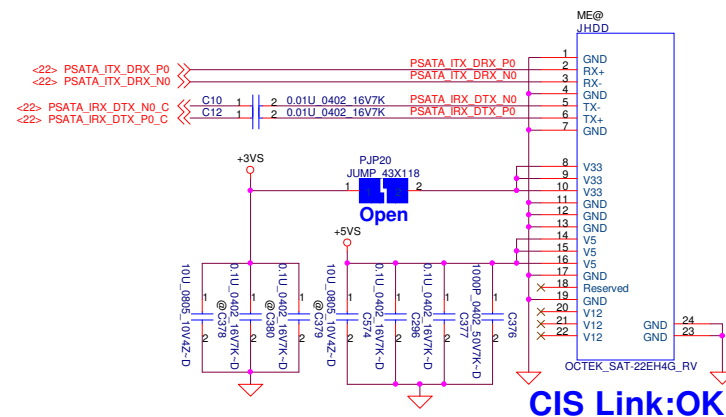
Camera Module Connector



Bluetooth Module Connector

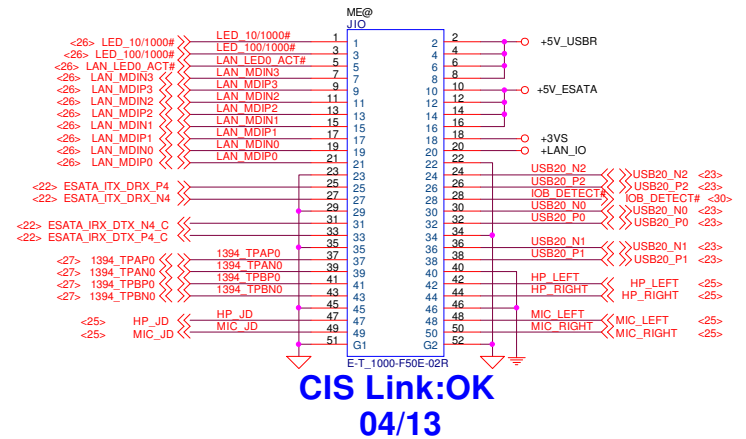


SATA Hard-Disk Connector



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I/O Board Connector
Type : Board to Board(50 Pin)



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Issued Date	2009/01/05	Deciphered Date	2009/01/05	Title	USB Port / IO connector	
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				Custom	LA-5162P	0.2
				Date	Monday April 20, 2009	Sheet 29 of 60

1



4



1



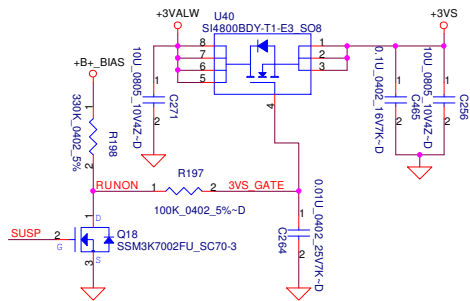
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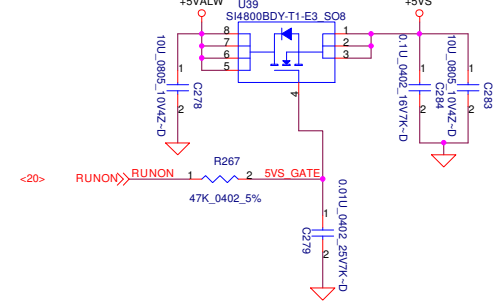
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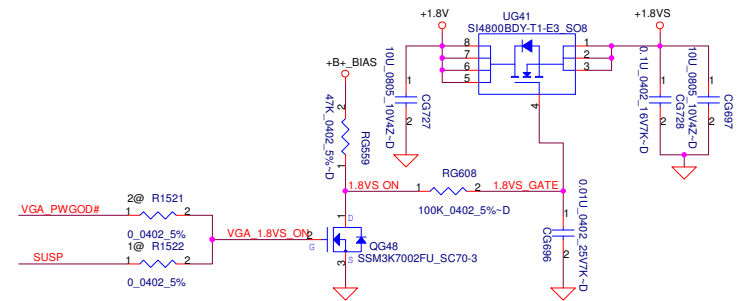
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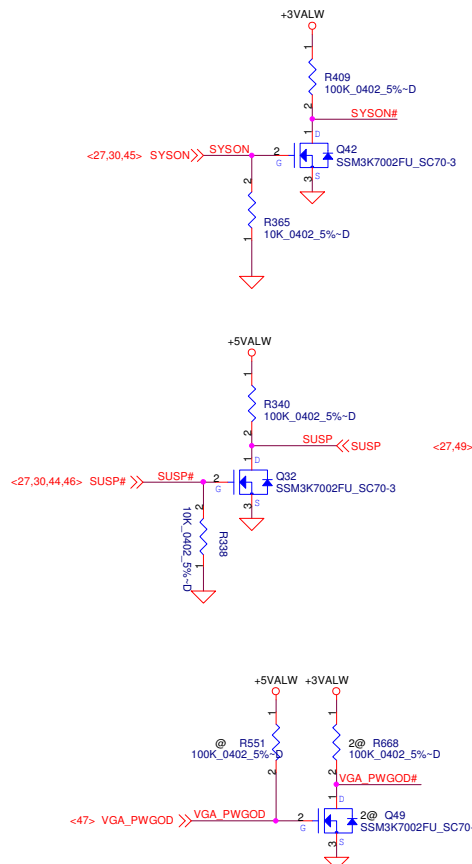
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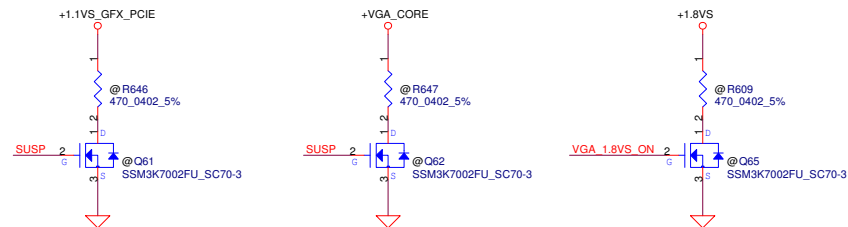
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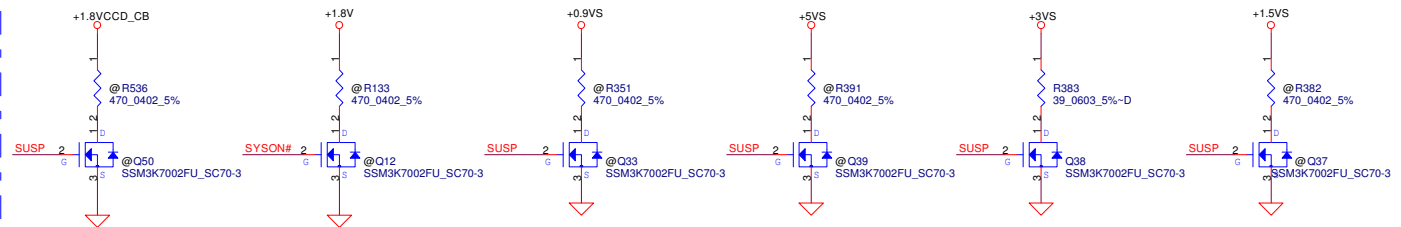
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VGA_ON>>>VGA_PWGOD**



VGA Discharge circuit

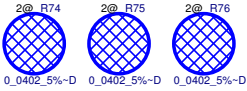


Discharge circuit



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				Customer	LA-5162P
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Dual BOM Component	
Location	R74 SD03415008L-1@ SD028000080-2@
	R75 SD03415008L-1@ SD028000080-2@
	R76 SD03415008L-1@ SD028000080-2@



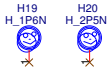
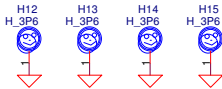
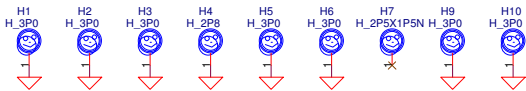
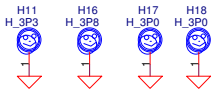
Dual BOM Component	
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	R138 SD03415008L-1@ SD02815018L-@
	R165 SD028000080-1@ SD028000080-@



Dual BOM Component	
Location	R39 SD02800008L-1@ SD034470180-@
	R334 SD03410018L-1@ SD028000080-@
	R568 SD034470180-1@ SD034470180-X76@



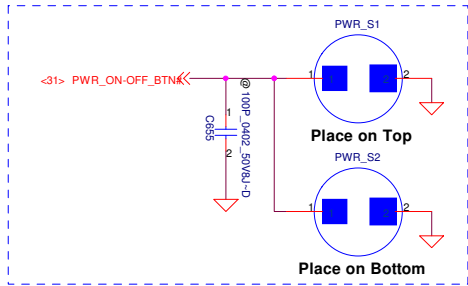
Dual BOM Component	
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	C1280 SE00000888L-1@ SD028000080-X76@
	U10 SA00002D700-1@ SA00002C610-X76@



Fiducial Mark



Power button switch for debug



Main Board PCB



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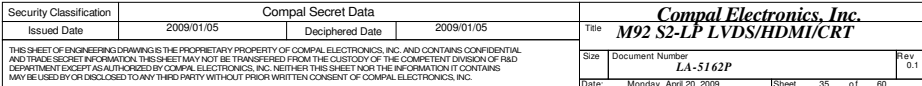
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Size	Document Number	Rev	1.0
Date	Monday, April 20, 2009	Sheet	33 of 60

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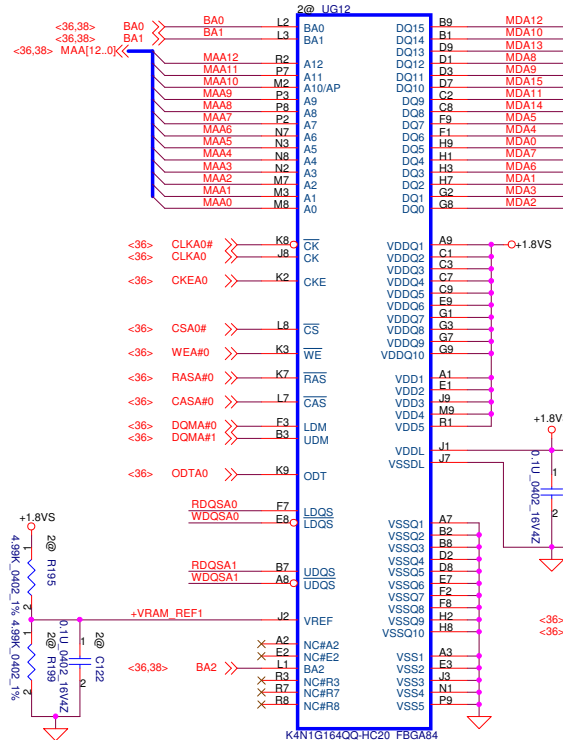


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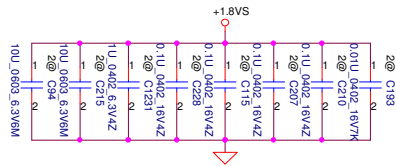
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Issued Date				2009/01/05				Title			
				Deciphered Date				M92 S2-LP PCIE interface			
				2009/01/05				LA-5162P			
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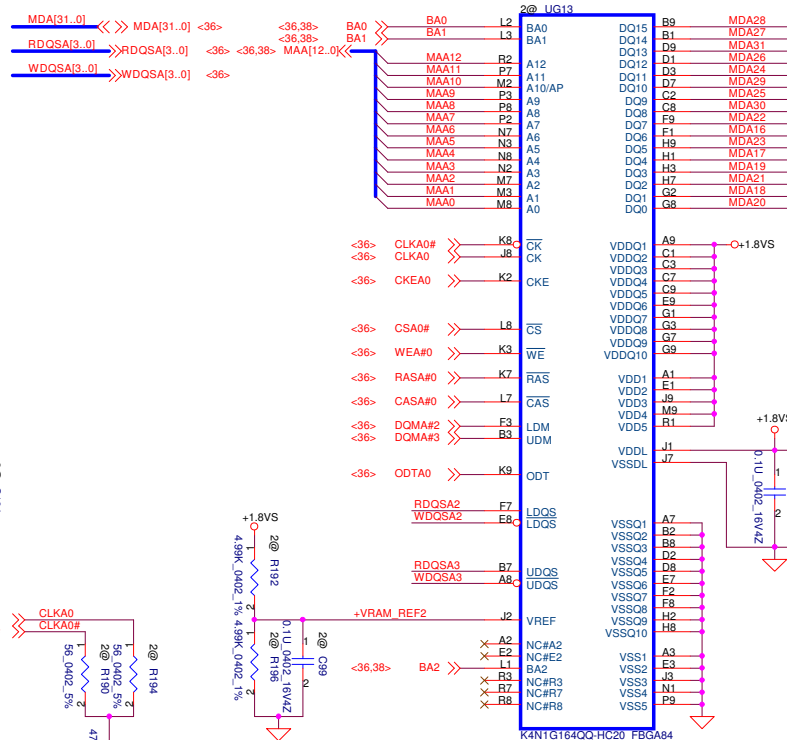
DDR2 64MX16(128MB)



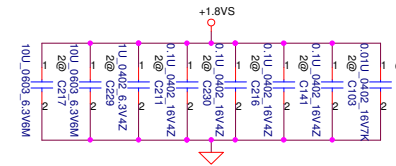
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DDR2 64MX16(128MB)



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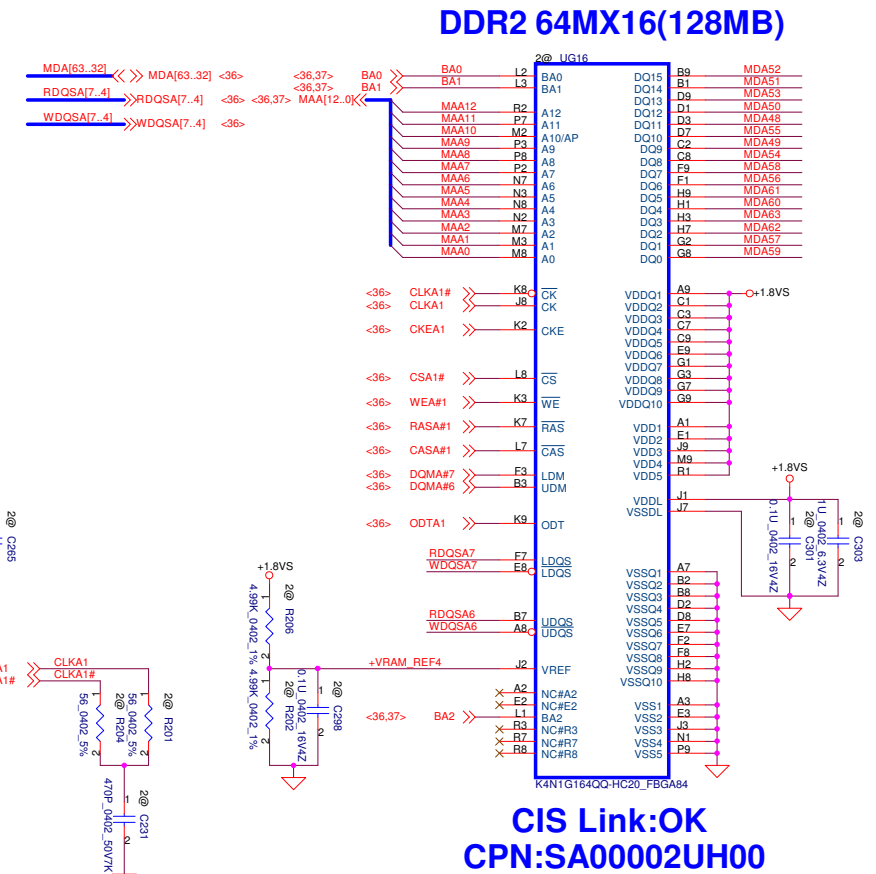
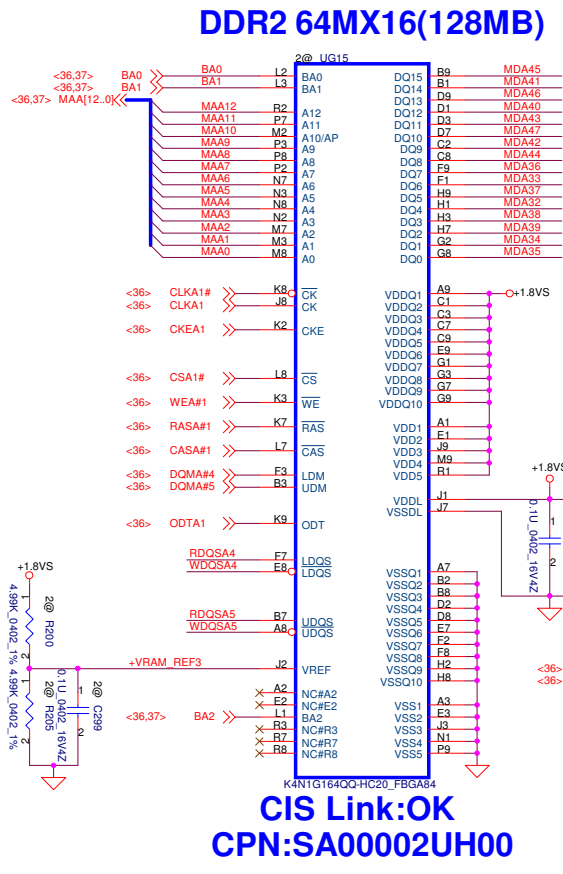
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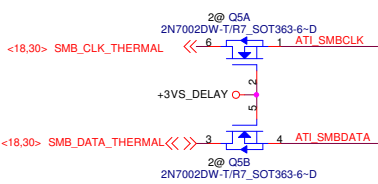
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LA-5162P

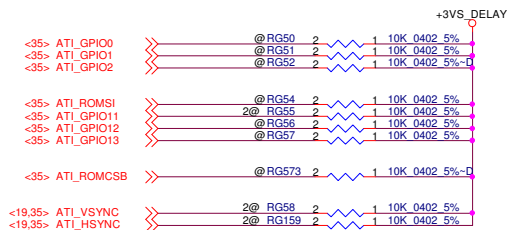
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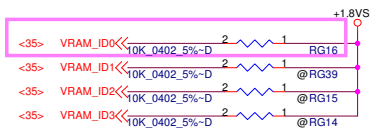
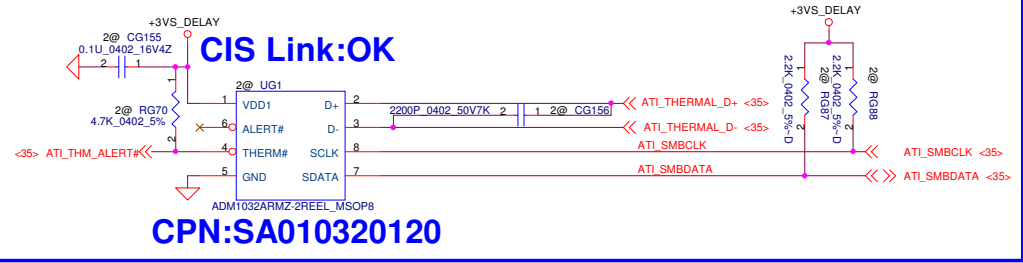
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Configuration Straps



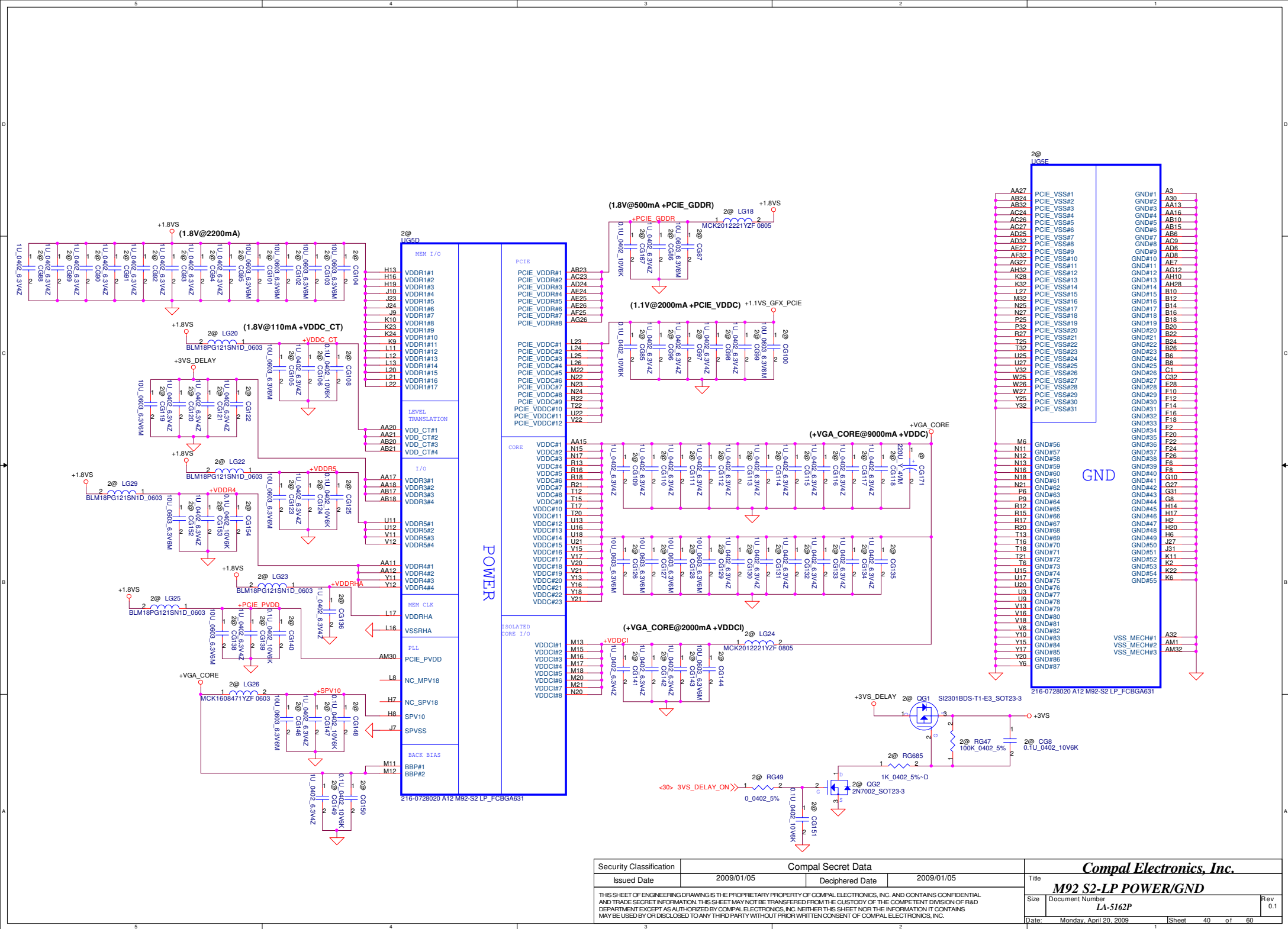
VGA Thermal Sensor ADM1032ARMZ



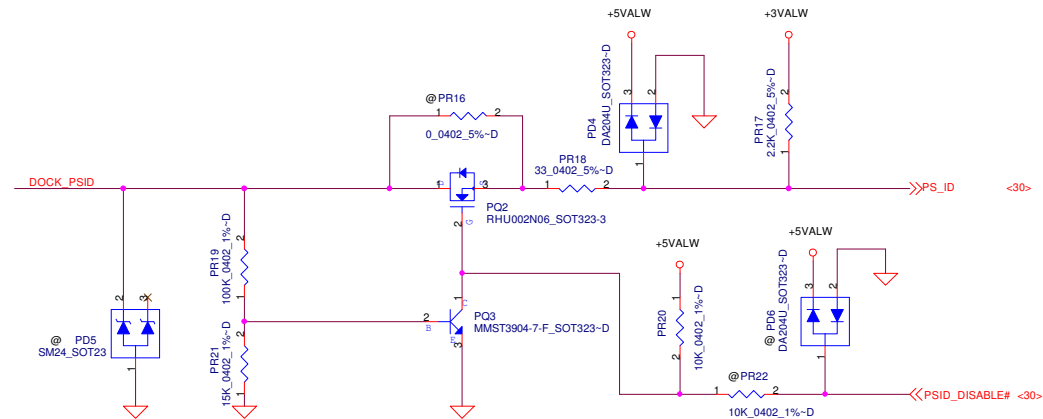
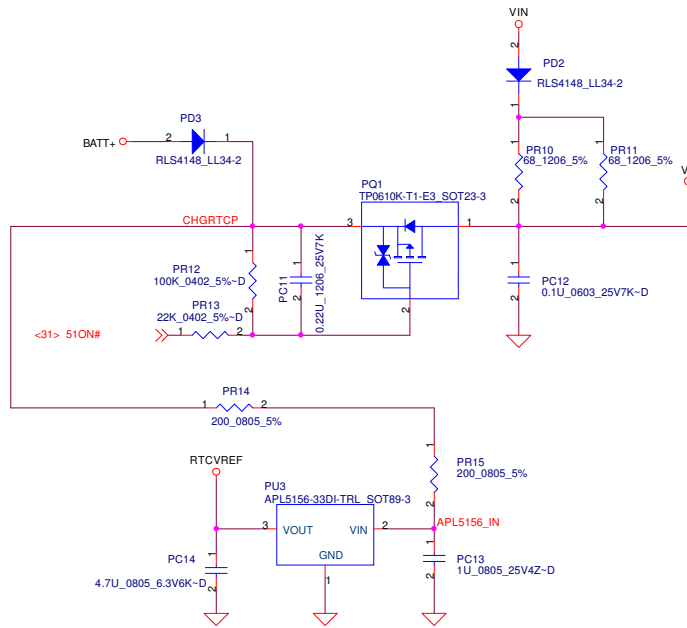
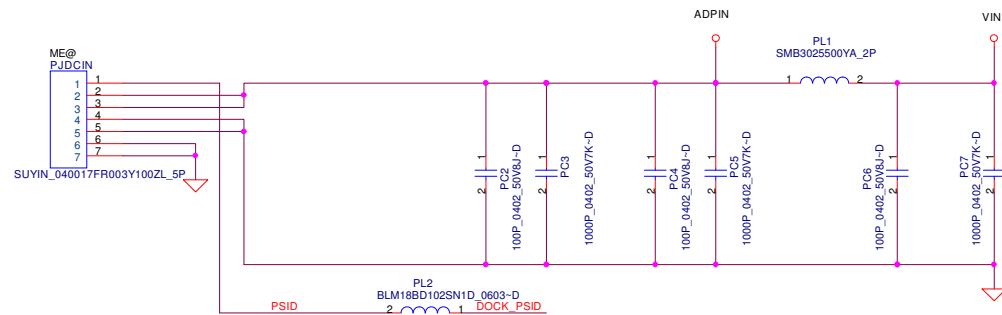
ATI-M92-S2 Strap Pin Table

Strap Name	Pin Name	Description	Setting
VIP_DEVICE_STRAP_EN	V2SYNC	0 --> Driver would ignore the value sampled on DVPDATA_20 during reset. 1 --> Driver would use the sampled value sampled at reset from DVPDATA_20 to determine whether or not.	0 *
VGA_DIS	GPIO_9_ROMSI	0 --> VGA Controller capacity enabled. 1 --> The device will not be recognized as the system's VGA controller.	0 *
TX_PWRS_ENB	GPIO_0	Transmitter Power Savings Enable 0 --> 50% Tx output swing 1 --> Full Tx output swing	0 *
TX_DEEMPH_EN	GPIO_1	PCI-Express Transmitter De-emphasis Enable 0 --> Tx de-emphasis disabled 1 --> Tx de-emphasis enable	0 *
CONFIG[2:0]	GPIO_[13:11]	GDDR3 memory capacity : 128MB --> 000 256MB --> 001 64MB --> 010 BIOS_ROM_EN=0	001 *
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 --> Disable external BIOS ROM device 1 --> Enable external BIOS ROM device	0 *
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] --> [HSYNC:VSYNC] 00 --> No Audio function 01 --> Audio for Display-Port and HDMI if adapter is detected 10 --> Audio for Display-Port only 11 --> Audio for both Display-Port and HDMI	11 *
BIF_GEN2_EN_A	GPIO_2	0 --> Advertises the PCIe device as 2.5GT/s capable at power-on. 1 --> Advertises the PCIe device as 5.0GT/s capable at power-on.	0 *
RESERVED	H2SYNC	Internal use only. This pad has an internal pull-down and must be 0V at reset.	0 *
RESERVED	GPIO_21_BB_EN GENERICC	Internal use only. This pad has an internal pull-down and must be 0V at reset.	0 *

Strap Name	Pin Name	GPU	Project	GDDR3 Size	Vendor Part Number	Compal Part Number	VRAM_ID[3:0]
VRAM_ID[3:0]	DVPDATA[23:20]	ATI M92-S2-LP	KAM01	512M	Samsung - K4N1G164QE-HC20	SA000031O00(2nd)	0 0 0 0
				512M	Hynix - H5PS1G63EFR-20L	SA00002UH00(main)	0 0 0 1



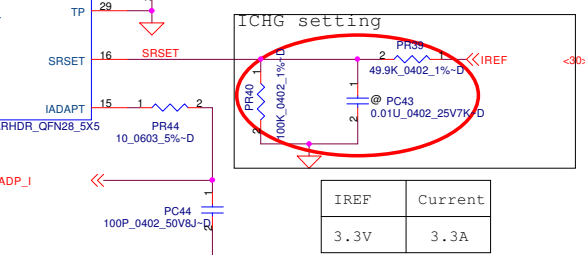
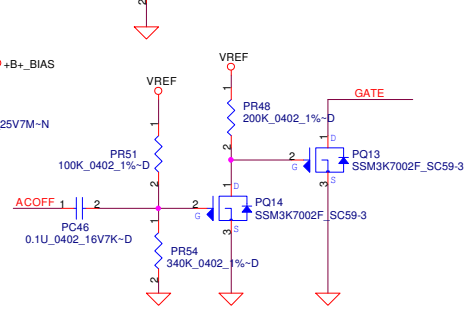
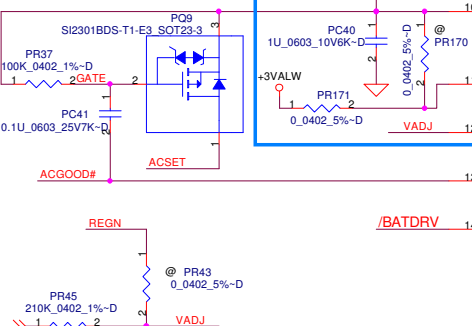
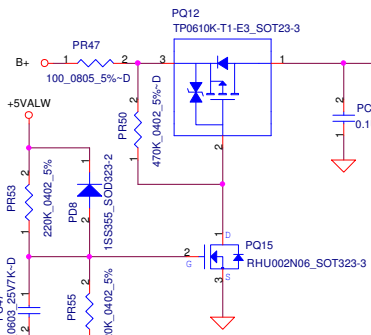
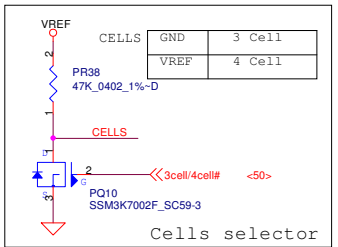
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Issued Date	2009/01/05	Deciphered Date	2009/01/05	Title	M92 S2-LP POWER/GND	
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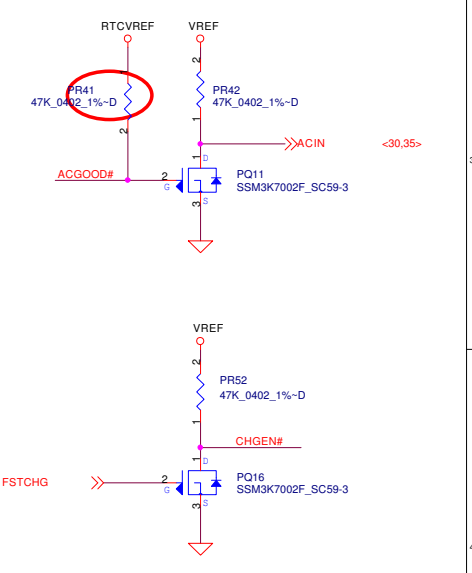
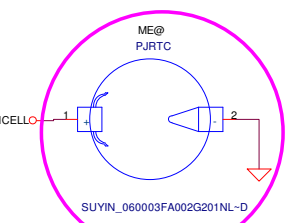
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90W adapter
 $I_{charge} = (V_{srset}/V_{dac}) * (0.1/PR30) = 3.3A$
 $I_{adapter} = (V_{acset}/V_{dac}) * (0.1/PR23) = 4.16A$
 Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

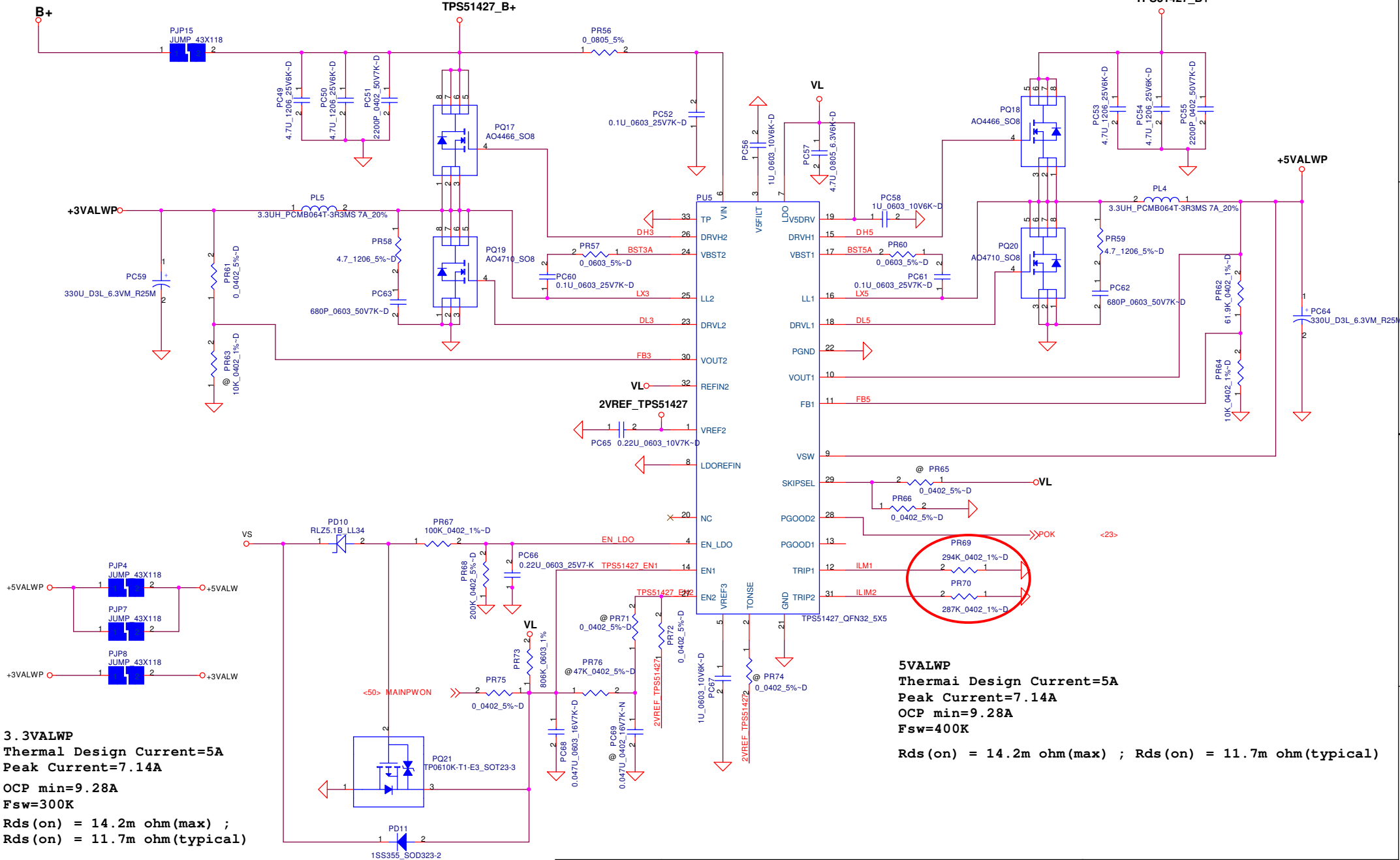
65W adapter(CP_SEL high)
 $I_{adapter} = (V_{acset}/V_{dac}) * (0.1/PR23) = 3A$



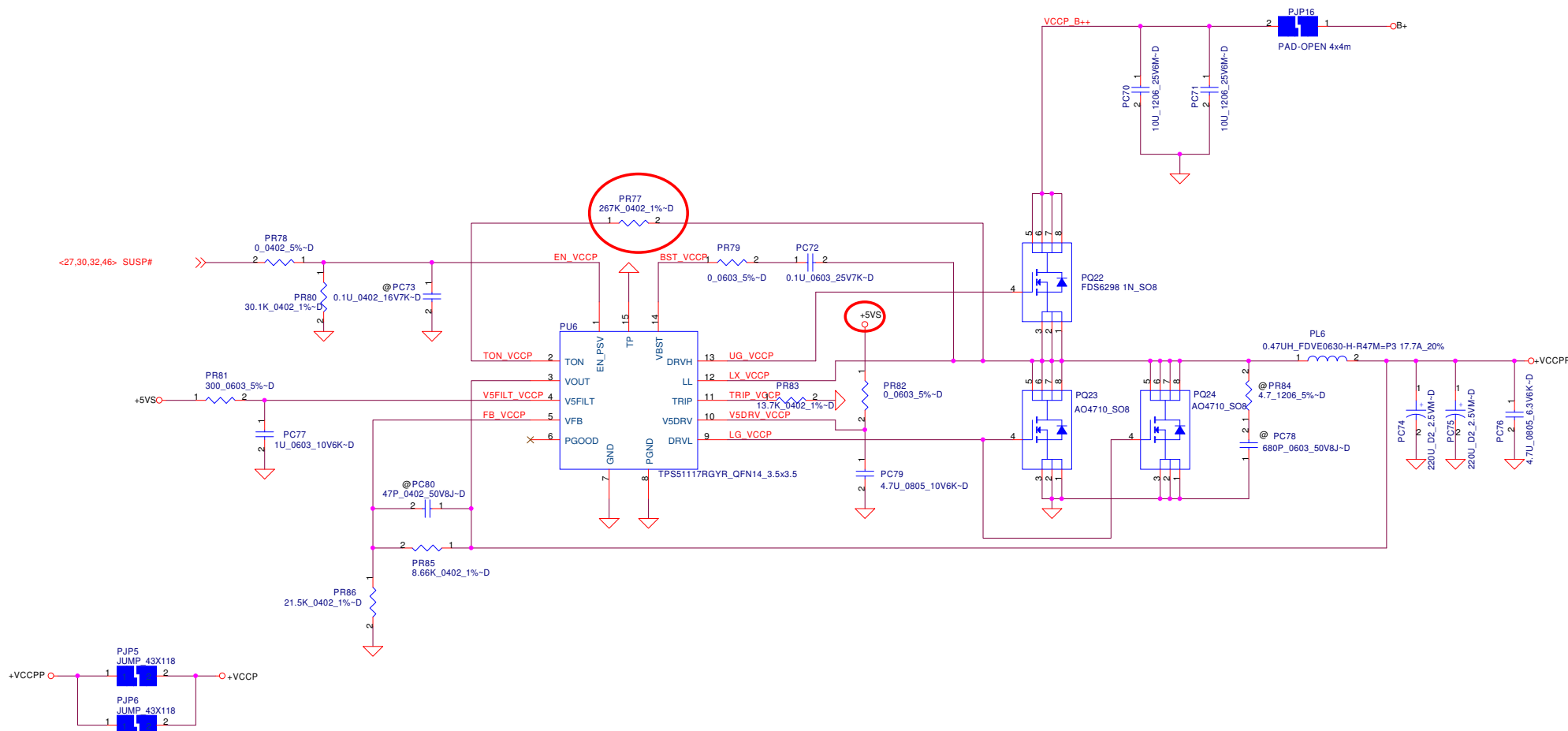
COIN RTC Battery



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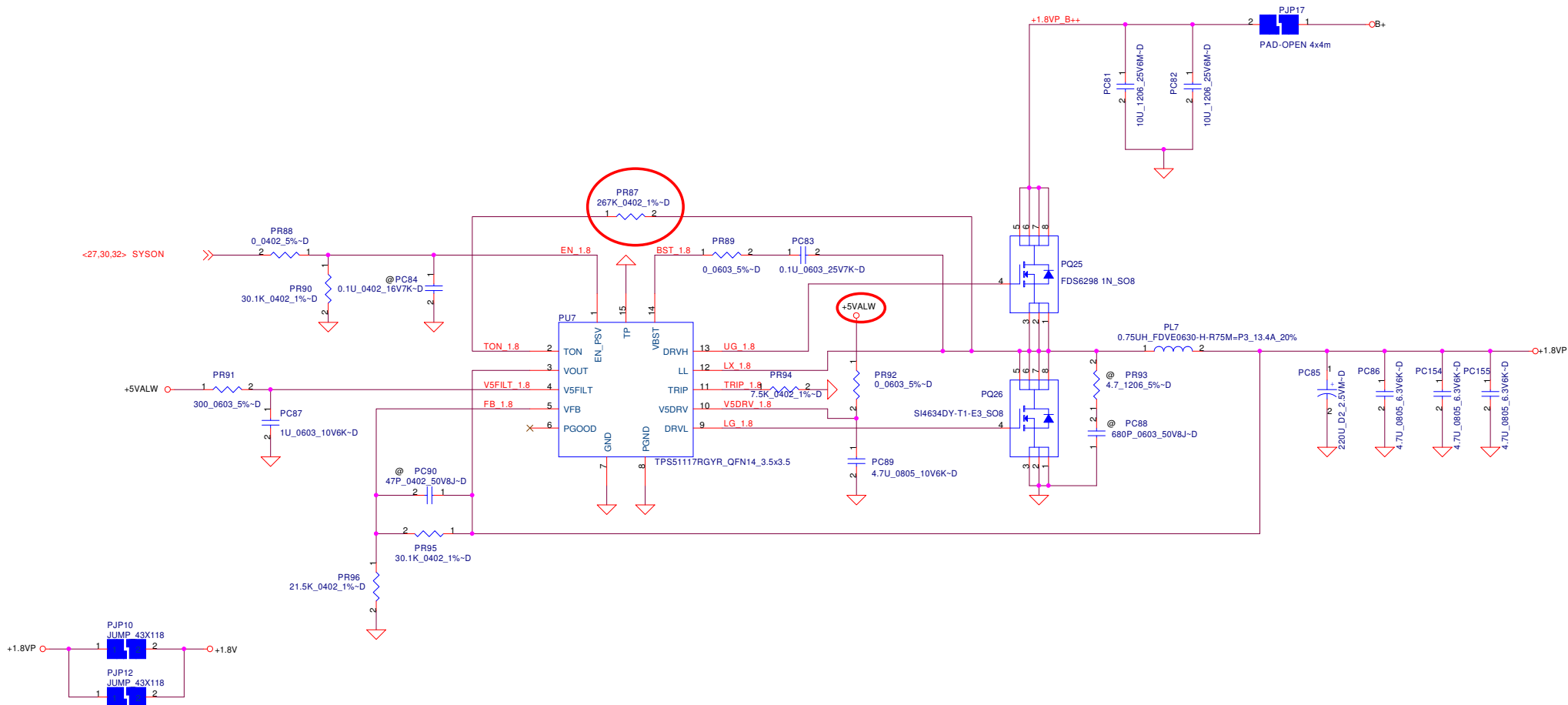


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VCCP
 Thermal Desig Current=14A
 Peak Current=20A
 OCP min=26A
 Fsw=298KHz
 $<V_o=1.05V>$ $V_{FB}=0.75V$
 $V_o=V_{FB} \cdot (1+PR85/PR86)=0.75 \cdot (1+8.66K/21.5K)=1.052V$

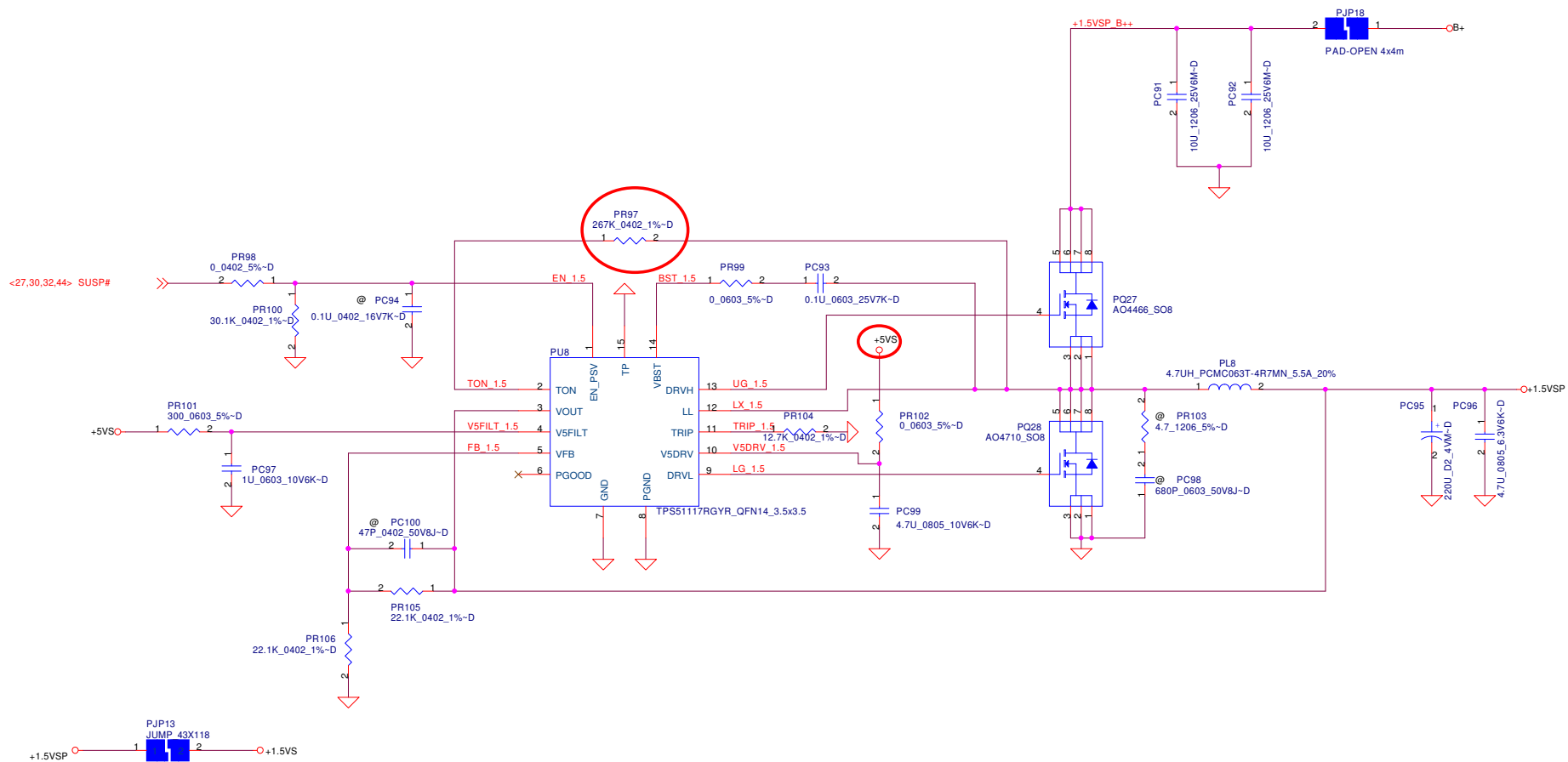
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1.8V
 Thermal Design Current=9A
 Peak Currnet=12.9A
 OCP min=16.77A
 Fsw=297KHz

<Vo=1.8V> VFB=0.75V
 $V_o = V_{FB} * (1 + PR95/PR96) = 0.75 * (1 + 30.1K/21.5K) = 1.8V$
 Fsw=297KHz

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1.5V

Thermal Design Current=3.9A

Peak Current=5.57A

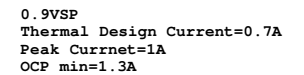
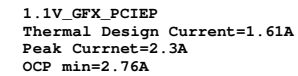
OCP_min=7.24A

Fsw=298KHz

<Vo=1.5V> VFB=0.75V

Vo=VFB*(1+PR105/PR106)=0.75*(1+22.1K/22.1K)=1.5V

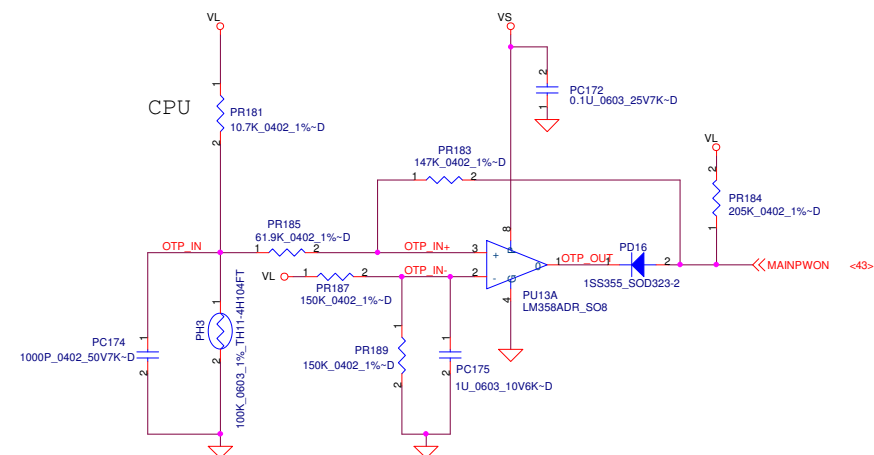
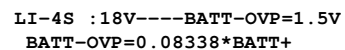
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CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
01	30	Board ID	2009-02-11	Compal	Change Board ID from 0.1(X00) to 0.2(X01)	Change R232 to 100K, R84 to 9.09K.	X01
02	20	HDMI Level Shifter	2009-02-19	Compal	Add U10 2nd source ST HDMI Level Shifter and support component	Add R165,R166,R161,R162,R163,R164, Change R560 to 4.3K ohm, C1280 to 0 ohm when use ST HDMI Level Shifter.	X01
03	22	ICH HDA Bus	2009-02-19	Compal	HDMI no Audio issue	ICH HDA_SDIN0(Pin AF4) for Codec ICH HDA_SDIN2(Pin AH3) for GMCH.	X01
04	25	MIC Record	2009-02-24	Compal	MIC can't Record ssue	Add C39,C40 for Mic signal, follow IDT schematic connect.	X01
05	31	EMI&ESD	2009-02-24	Compal	EMI&ESD requirement.	Add D52, Pop D24	X01
06	23	Audio	2009-02-27	IDT	Vendor recommandation after review X00 schematic.	Add R185,R186,Q2,Q4,Q17	X01
07	10,22	Audio	2009-03-03	Compal	HDA Bus with HDCP only on UMA.	Change R98,R103,R104,R105,R106 to 1@(UMA only).	X01
08	12,30	DPST	2009-03-04	Compal	Power Saving DPST for Intel UMA Platform	Add R295, R314	X01
09	19	LVDS	2009-03-05	Compal	Panel power up sequence timing too fast.	Change C206 value to 10uF, D22 to 0 ohm resistor.	X01
10	6,14,35	GMCH	2009-03-05	Compal	GM45 for DIS use.	R40,R41,R54,R60 always pop, RG44,RG119,RG163,RG103 de-pop PJP21,PJP24 always short, RG30,YG1,CG53,CG52 always pop.	X01
11	19	CRT	2009-03-05	Compal	R,G,B EA fail.	Change L5,L6,L7 to BLM18BB050SN1D and D50 to RB491D.	X01
12	20	HDMI	2009-03-05	Compal	HDMI test requirement.	Add Q16,C747,RG20.	X01
13	27	Card Reader	2009-03-05	O2	OZ888GS0L3N sequence requirement.	Add Q57,R170,C41.	X01
14	30	Battery LED	2009-03-05	Compal	Battery LED issue.	Change BATT_CHG_LED# to pin 25 of U29.	X01
15	31	Keyboard Connector	2009-03-05	Compal	Keyboard Connector issue.	JKBD change type to JAE_FL4S030HB3R3000.	X01
16	35,36	GPU change	2009-03-05	ATI	GPU schematic change after ATI review.	CG44,CG43,CG159CG48,CG49,CG161,RG37,CG266,CG71,CG72,CG68 CG69,CG70 de-pop, LG5,LG7 change to 0 ohm.	X01
17	36,37,38	VRAM change	2009-03-05	Dell	Change VRAM to DDR2(512MB).	Add UG12,UG13,UG15,UG16, change RG71, RG63 change to 100 ohm.	X01
18	12,30	DPST	2009-04-20	Compal	GM45 driver not implement this function.	Delete R314 and add R295 for UMA MB.	X02
19	21,22 23,24	ICH9 change	2009-04-20	Compal	ICH9ME-->Support IAMT, ICH9M-->Didn't support IAMT.	Change ICH9ME to ICH9M, because we didn't support IAMT.	X02
20	25	Codec change	2009-04-20	Compal	We need support Aux mode function.	Change U60 from SA00002QZ40(B5) to SA00002QZ50(A5).	X02
21	27	Carder Reader chip change	2009-04-20	O2	O2 vendor change version because 1394 and SD card issue.	Change U46 from SA000036M00(C) to SA000036M10(C1).	X02
21	27	Carder Reader	2009-04-20	O2	U46 need 1.8V source power from LDO(U2).	Add U2, C42, C43, R229, R230, R231.	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	Charger	2/10	Compal	can't not boot	Add net ACGOOD# and connect from PC41_pin2 to PQ11_pin2	X01
2	43	VCCPP	2/28	Compal	HW update PWR Budget	1.Change TDC from 5.85A to 14A Peak Current from 8.35A to 20A OCP min from 10.86A to 26A 2. Change PL6 from SH000003Y80(S COIL 1UH +-20% MPLC0730L1R0 10.6A) to SH00000GQ00 (S COIL 0.47UH +-20% FDVE0630-H-R47M=P3 17.7A)	X01
3	44	+1.8VP	2/28	Compal	HW update PWR Budget	1. Change TDC from 5.85A to 9A Peak Current from 8.35A to 12.9A OCP min from 10.86A to 16.77A 2. Change PL7 from SH000003Y80(S COIL 1UH +-20% MPLC0730L1R0 10.6A) to SH00000F40L (S COIL .75U 20% FDVE0630-H-R75M=P3 13.4A)	X01
4	46	+VGA_CORE	3/06	Compal	HW to meet the properly power sequence	change PR114 from SD03422028L(S RES 1/16W 22K +-1% 0402) to SD02800008L(S RES 1/16W 0 +-5% 0402)	X01
5	48	+1.1V_GFX_PCIEP	3/06	Compal	HW to meet the properly power sequence	change PR191 from SD02800008L(S RES 1/16W 0 +-5% 0402) to SD03447018L(S RES 1/16W 4.7K +-1% 0402)	X01
6	48	+1.1V_GFX_PCIEP	3/06	Compal	HW to meet the properly power sequence	change PC176 from SE076104K8L(S CER CAP .1U 16V K X7R 0402) to SE00000888L(S CER CAP 2.2U 6.3V M X5R 0402)	X01
7	40	DCIN	3/09	Compal	ME DCIN connector change	Modify DCIN connector PCB footprint and pin define Change from (P/N :DC231000B00) FOX_JPD113E-LB103-7F_5P to (P/N :DC231000L0L)SUYIN_040017FR003Y100ZL_5P	X01
8	43	VCCPP	03/13	Compal	modify ocp setting	Change PR83 from SD00000068L(S RES 1/16W 8.45K +-1% 0402) to SD03413728L (S RES 1/16W 13.7K +-1% 0402)	X02
9	44	+1.8VP	03/13	Compal	modify ocp setting	1.Change PQ26 from SB00000DU00(S TR AO4710 1N SO8) to SB00000DA00 (S TR SI4634DY-T1-E3 1N SO8) 2.Change PR94 from SD03415028L(S RES 1/16W 15K +-1% 0402) to SD034750180 (S RES 1/16W 7.5K +-1% 0402)	X02
10	41	Charger	03/31	Compal	Change 90W CP setting from 4.4A to 4.16A	Change PR32 from SD03451128L(S RES 1/16W 51.1K +-1% 0402) to SD034604280 (S RES 1/16W 60.4K +-1% 0402)	X02
11	41	Charger	03/31	Compal	Add support 65W CP setting circuit :3A (3.34A*0.9)	Add @PC191 SE102104K8L (S CER CAP .1U 10V +-10% X7R 0402) Add PR116 SD03497628L (S RES 1/16W 97.6K +-1% 0402) Add PQ38 SB000009080 (S TR SSM3K7002F 1N SC59-3)	X02
12	43 44	VCCPP +1.8VP	03/31	Compal	H/S mosfet current rating not enough (AO4466L Continuous Drain Current =9.4A)	Change PQ22, PQ25 from SB00000CG00 (S TR AO4466L 1N SO8) to SB000006D8L (S TR FDS6298 1N SO8)	X02

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