

Compal Confidential

KBYF0 Schematics Document

AMD Griffin Processor with RS780M+SB700

(With ATI MXM/B)

2009-01-22

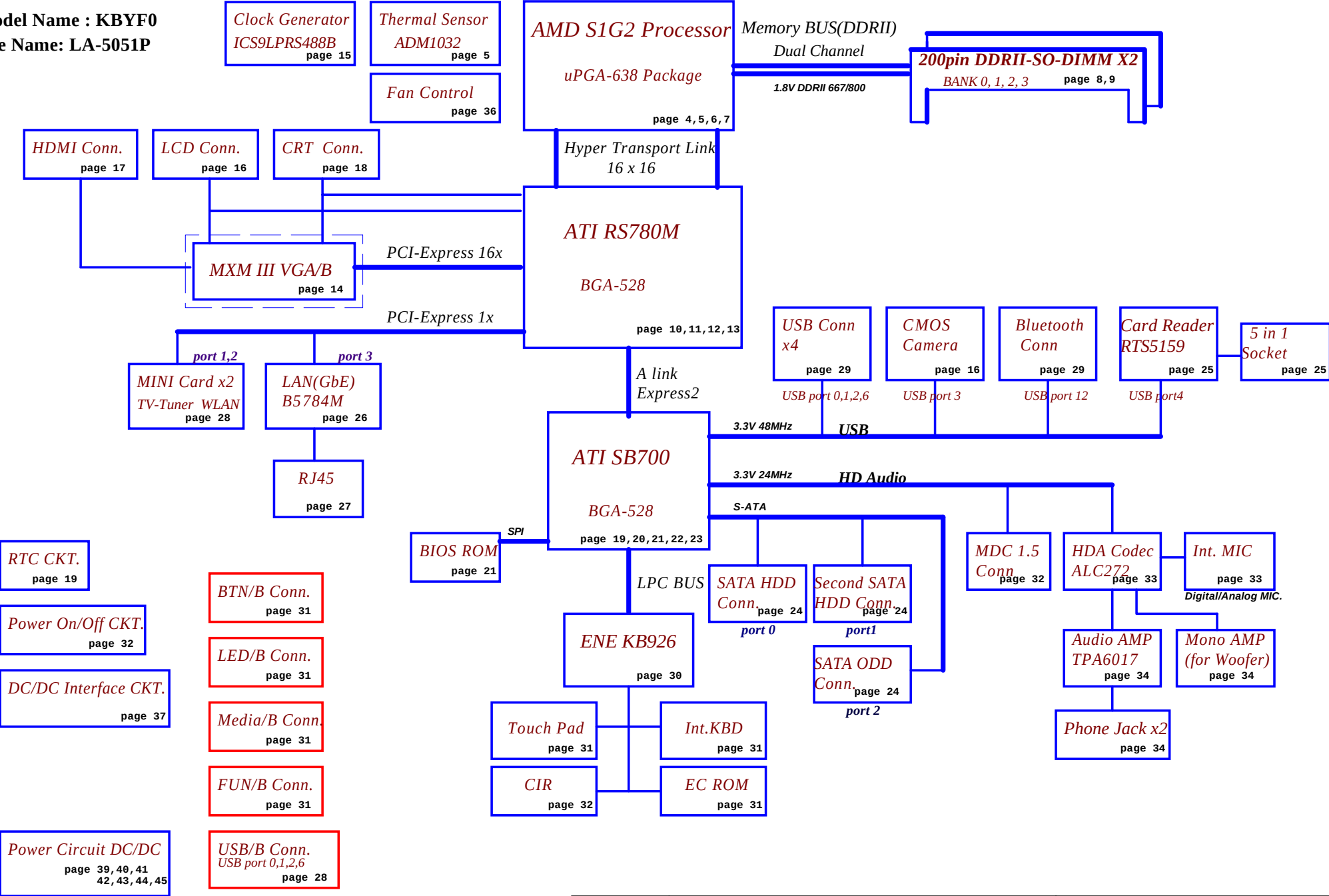
REV: 0.3

ZZZ1
PCB
DA60000B600-*

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Model Name : KBYF0
File Name: LA-5051P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE_0	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.05V switched power rail	ON	OFF	OFF
+1.2V_HT	1.25V switched power rail	ON	OFF	OFF
+NB_CORE	1.0V~1.1V switched power rail for NB VDDC	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA and MXM/B	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
No PCI device			

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	CPU SB	1001 101X b
MXM GMT G781-1	1001 101X b		

SB700 SM Bus 0 address

Device	Address	Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb	Lan	
DDR DIMM0	1001 000Xb		
DDR DIMM2	1001 010Xb		
Minicard			
Minicard			

EC SM Bus2 address

SB700 SM Bus 1 address

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

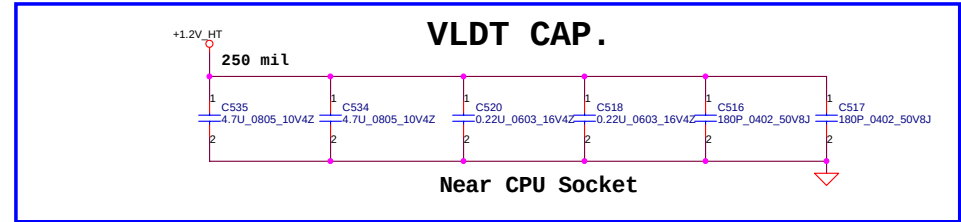
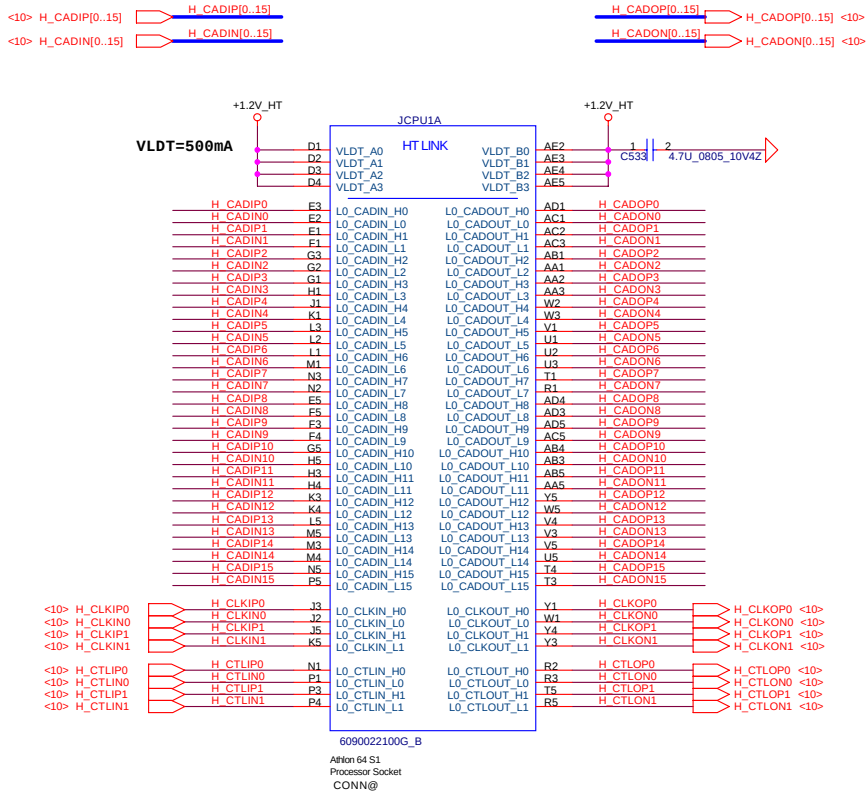
Board ID	PCB Revision
0	0.1
1	0.2
* 2	0.3 0.4 1.0
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@

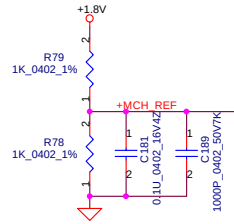
PROJECT ID Table

Board ID	PROJECT
0	KBKC0 (SJM70)
1	KBYF0 (SJV70)
2	
3	
4	
5	
6	
7	

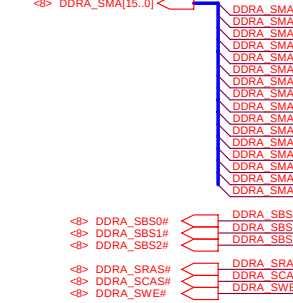
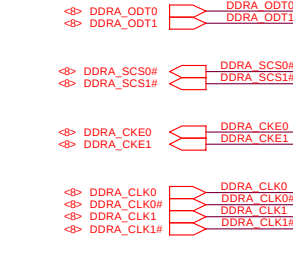
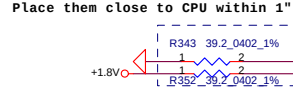
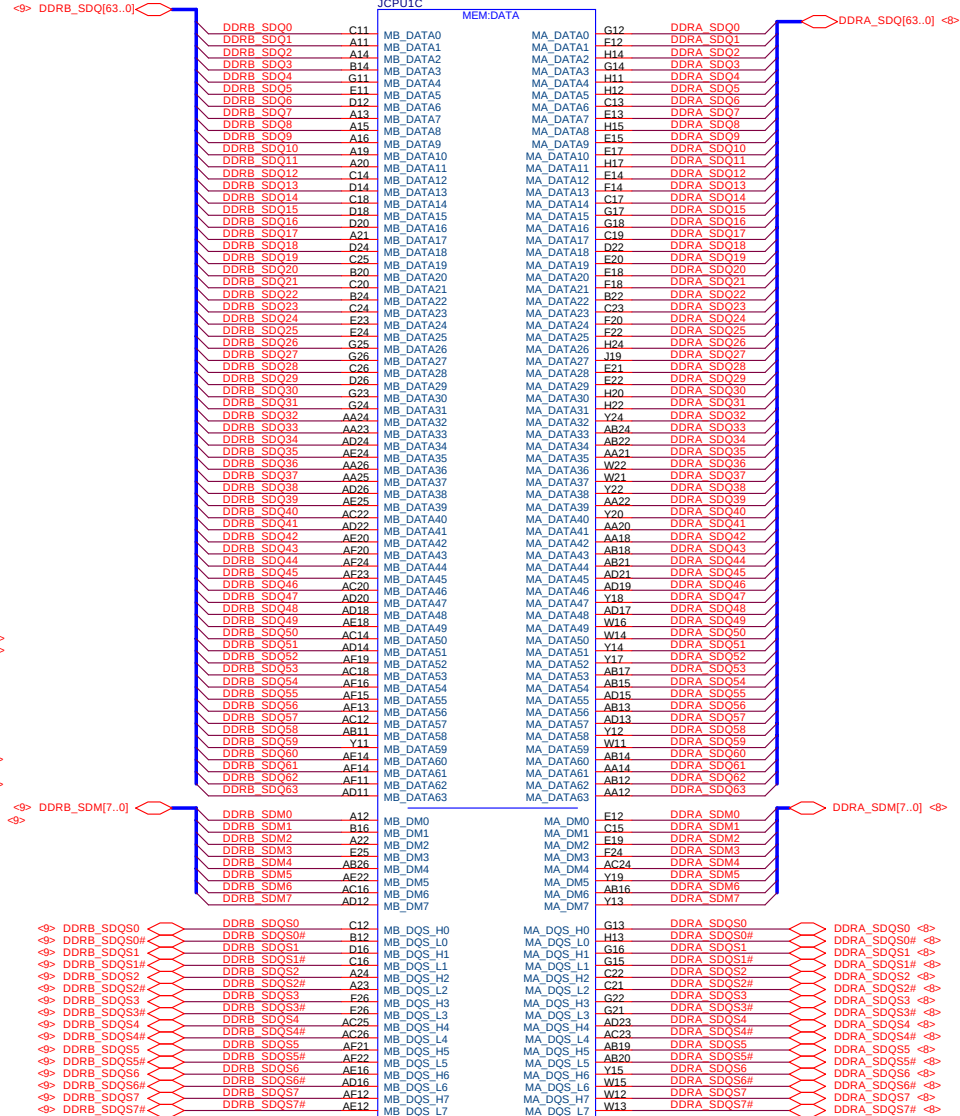
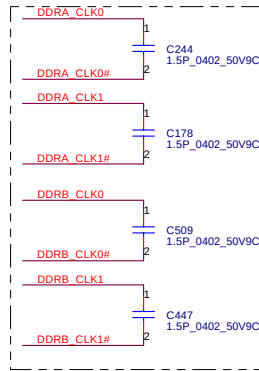


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2009/11/03				Title				AMD CPU S1G2 HT I/F			
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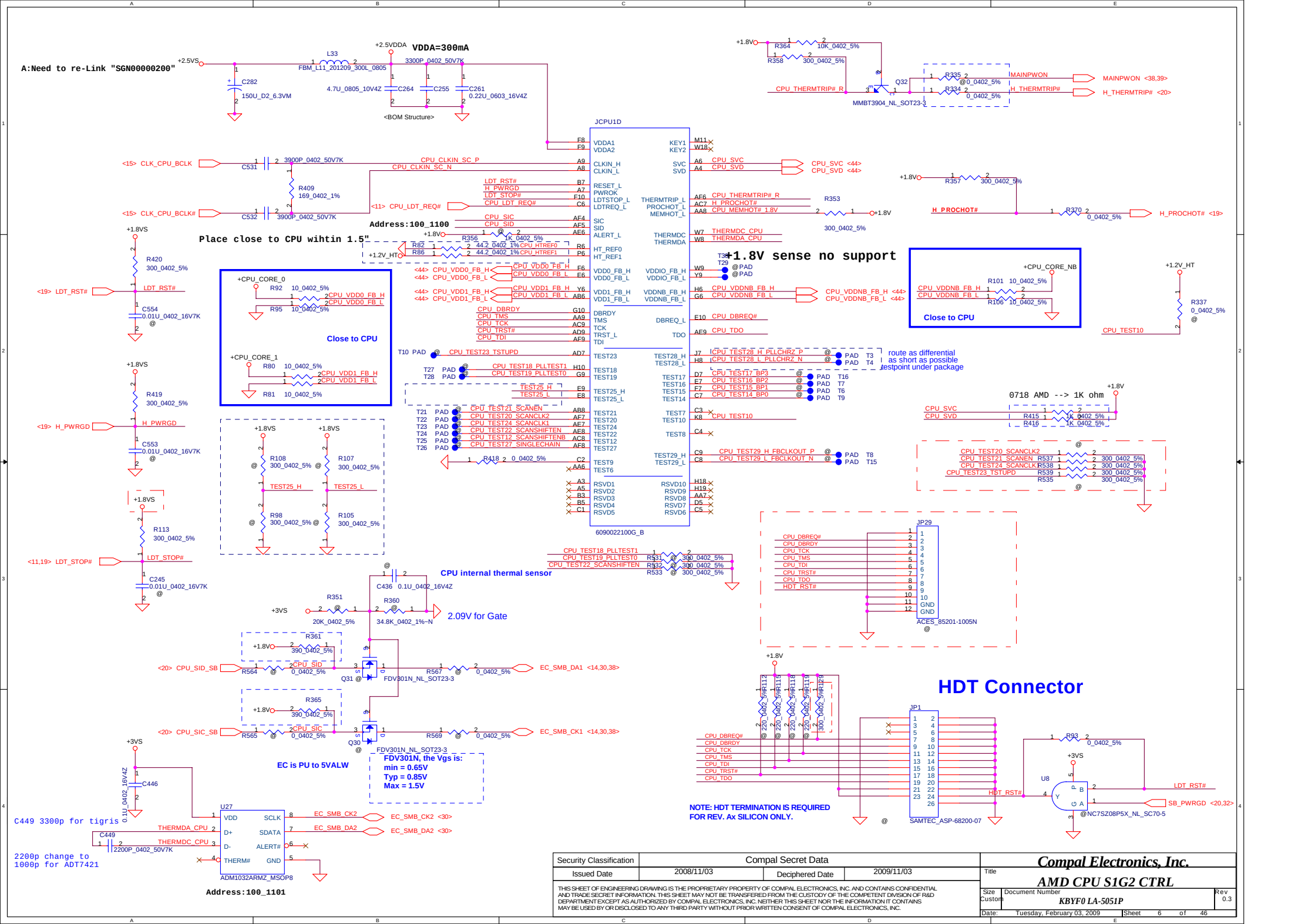
Processor DDR2 Memory Interface



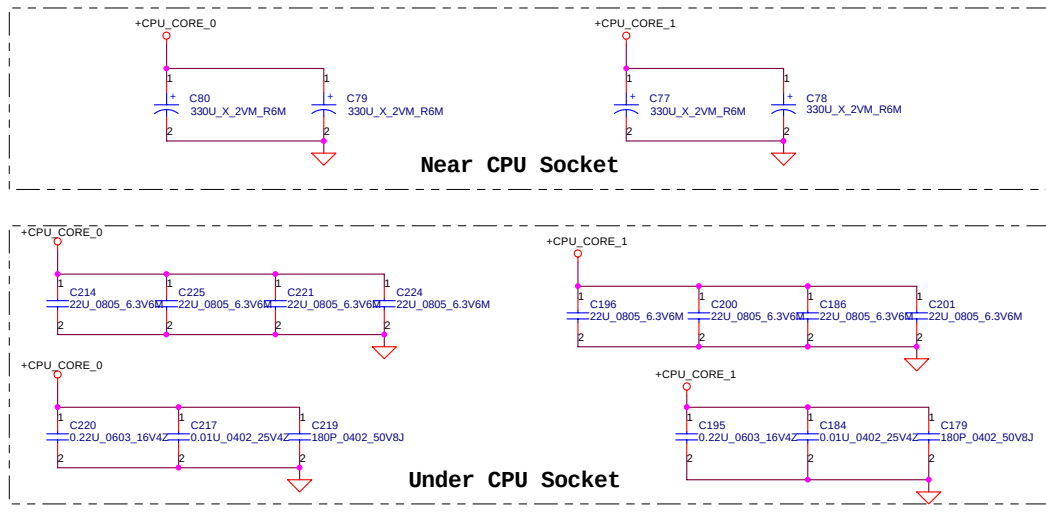
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



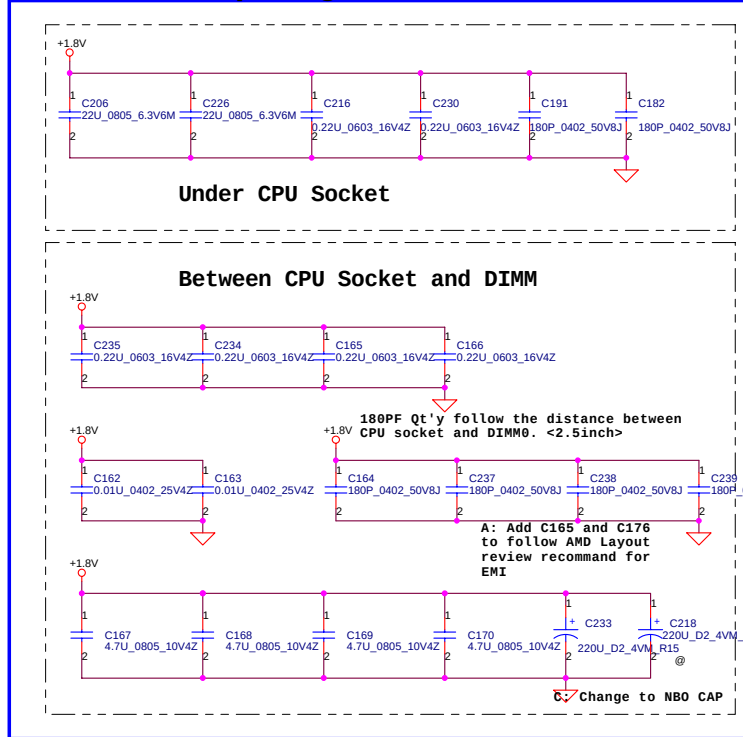
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2009/11/03				2009/11/03				AMD CPU S1G2 DDR2 I/F			
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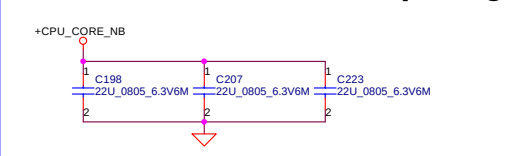
VDD(+CPU_CORE) decoupling.



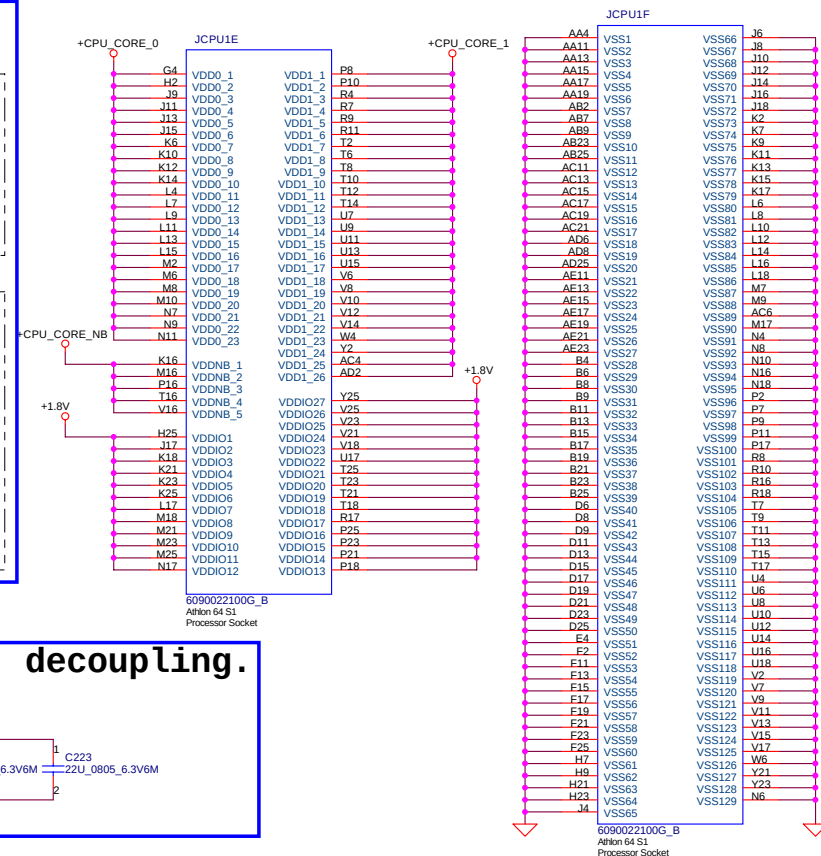
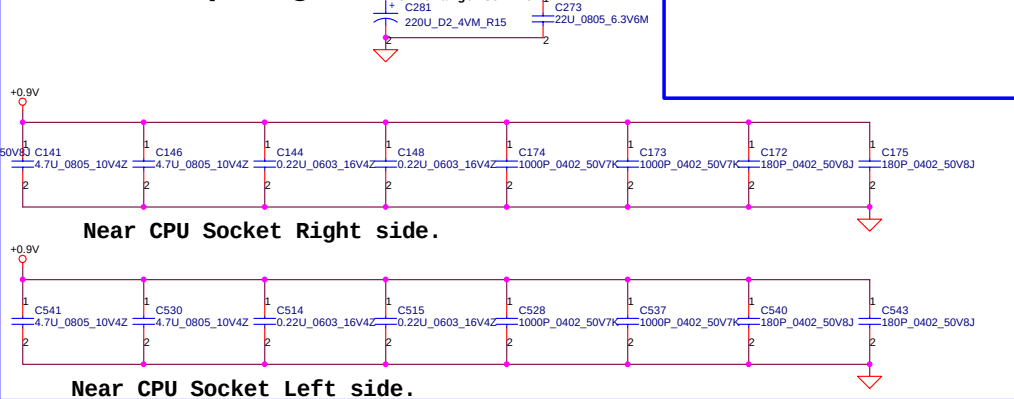
VDDIO decoupling.



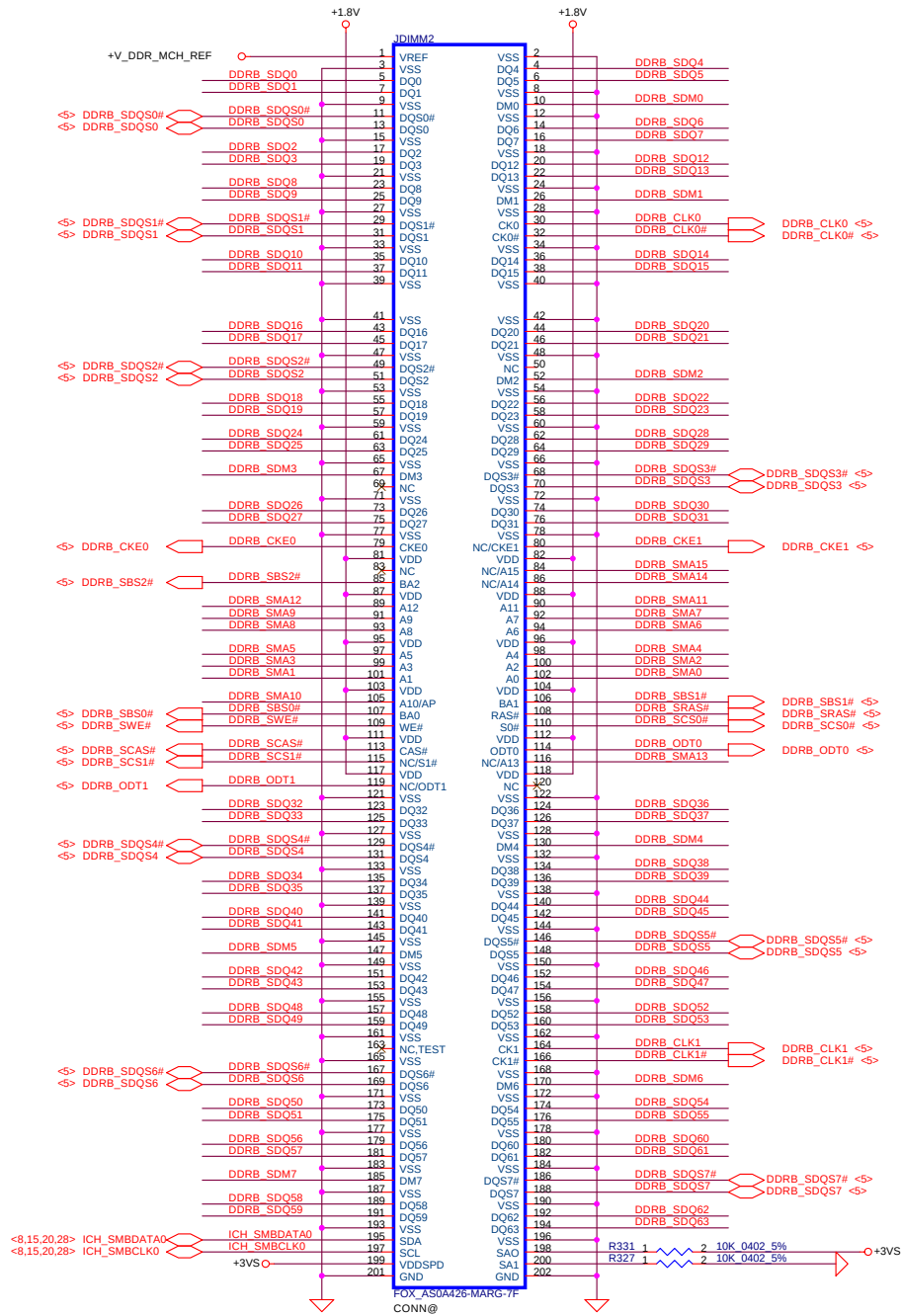
+CPU_CORE_NB decoupling.



VTT decoupling.

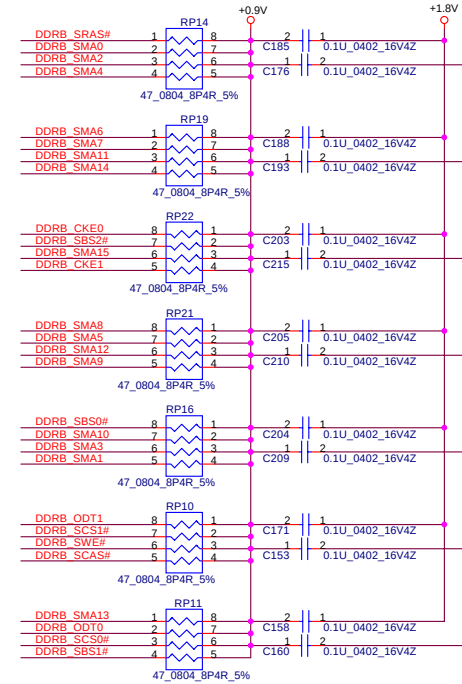
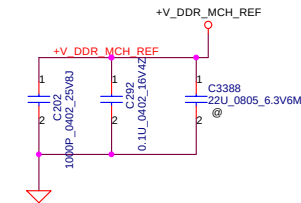


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DIMM1 REV H:9.2mm (BOT)

DDR_B_SQ[63..0] <=> DDRB_SQ[63..0] <=>
DDR_B_SDM[7..0] <=> DDRB_SDM[7..0] <=>
DDR_B_SMA[15..0] <=> DDRB_SMA[15..0] <=>



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<14> PCIE_GTX_C_MRX_P0[0..15] <PCIE GTX_C_MRX_P0[0..15]>
<14> PCIE_GTX_C_MRX_N0[0..15] <PCIE GTX_C_MRX_N0[0..15]>

PCIE_MTX_C_GRX_P0[0..15] <PCIE_MTX_C_GRX_P0[0..15]> <14>
PCIE_MTX_C_GRX_N0[0..15] <PCIE_MTX_C_GRX_N0[0..15]> <14>

PCIE GTX C MRX P0	C680	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P0 D4	GFX_RX0P
PCIE GTX C MRX N0	C681	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N0 C4	GFX_RX0N
PCIE GTX C MRX P1	C682	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P1 A3	GFX_RX1P
PCIE GTX C MRX N1	C683	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N1 B3	GFX_RX1N
PCIE GTX C MRX P2	C684	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P2 C2	GFX_RX2P
PCIE GTX C MRX N2	C685	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N2 C1	GFX_RX2N
PCIE GTX C MRX P3	C686	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P3 E5	GFX_RX3P
PCIE GTX C MRX N3	C687	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N3 F5	GFX_RX3N
PCIE GTX C MRX P4	C688	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P4 G5	GFX_RX4P
PCIE GTX C MRX N4	C689	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N4 G6	GFX_RX4N
PCIE GTX C MRX P5	C690	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P5 H5	GFX_RX5P
PCIE GTX C MRX N5	C691	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N5 H6	GFX_RX5N
PCIE GTX C MRX P6	C692	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P6 J5	GFX_RX6P
PCIE GTX C MRX N6	C693	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N6 J6	GFX_RX6N
PCIE GTX C MRX P7	C694	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P7 J7	GFX_RX7P
PCIE GTX C MRX N7	C695	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N7 J8	GFX_RX7N
PCIE GTX C MRX P8	C696	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P8 L5	GFX_RX8P
PCIE GTX C MRX N8	C697	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N8 L6	GFX_RX8N
PCIE GTX C MRX P9	C698	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P9 M8	GFX_RX9P
PCIE GTX C MRX N9	C699	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N9 L8	GFX_RX9N
PCIE GTX C MRX P10	C700	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P10 P7	GFX_RX10P
PCIE GTX C MRX N10	C701	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N10 M7	GFX_RX10N
PCIE GTX C MRX P11	C702	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P11 P5	GFX_RX11P
PCIE GTX C MRX N11	C703	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N11 M5	GFX_RX11N
PCIE GTX C MRX P12	C704	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P12 R8	GFX_RX12P
PCIE GTX C MRX N12	C705	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N12 P8	GFX_RX12N
PCIE GTX C MRX P13	C706	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P13 R6	GFX_RX13P
PCIE GTX C MRX N13	C707	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N13 R5	GFX_RX13N
PCIE GTX C MRX P14	C708	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P14 P4	GFX_RX14P
PCIE GTX C MRX N14	C709	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N14 P3	GFX_RX14N
PCIE GTX C MRX P15	C710	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX P15 T4	GFX_RX15P
PCIE GTX C MRX N15	C711	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX MRX N15 T3	GFX_RX15N

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

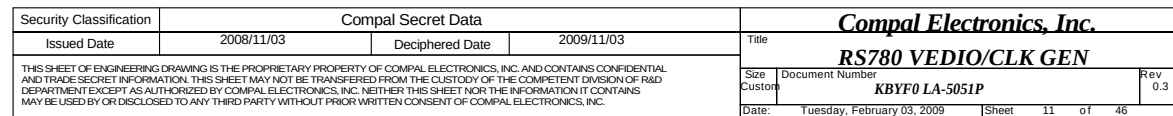
PCIE I/F SB

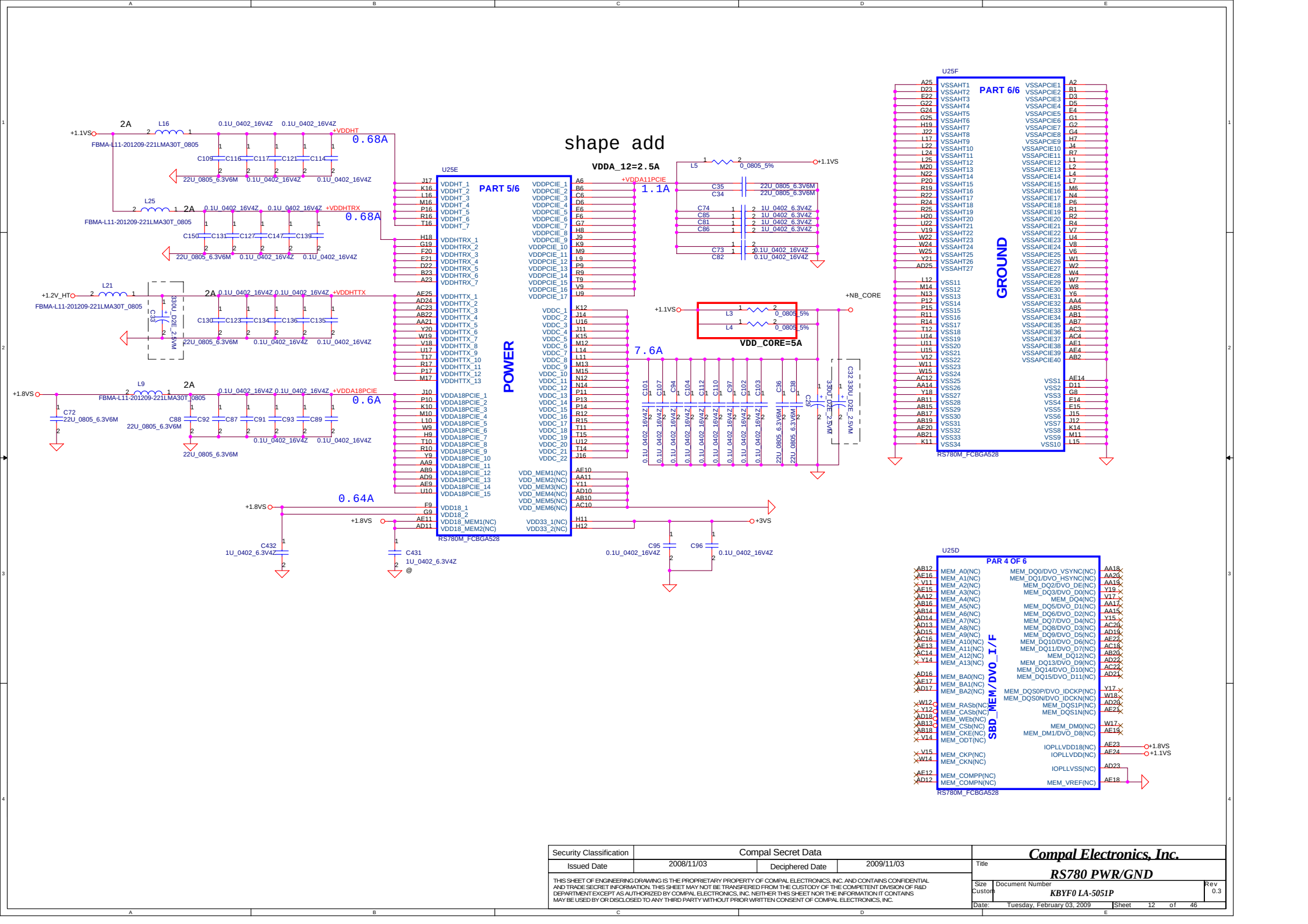
RS780M_FCBGA528

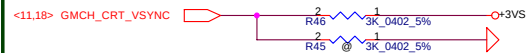
RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PCIE_MTX_GRX_P0	C897	1	2	UMA@0.1U 0402 10V7K HDMI TX2+ UMA	HDMI_TX2+_UMA <17>
PCIE_MTX_GRX_N0	C898	1	2	UMA@0.1U 0402 10V7K HDMI TX2- UMA	HDMI_TX2-_UMA <17>
PCIE_MTX_GRX_P1	C899	1	2	UMA@0.1U 0402 10V7K HDMI TX1+ UMA	HDMI_TX1+_UMA <17>
PCIE_MTX_GRX_N1	C900	1	2	UMA@0.1U 0402 10V7K HDMI TX1- UMA	HDMI_TX1-_UMA <17>
PCIE_MTX_GRX_P2	C901	1	2	UMA@0.1U 0402 10V7K HDMI TX0+ UMA	HDMI_TX0+_UMA <17>
PCIE_MTX_GRX_N2	C902	1	2	UMA@0.1U 0402 10V7K HDMI TX0- UMA	HDMI_TX0-_UMA <17>
PCIE_MTX_GRX_P3	C903	1	2	UMA@0.1U 0402 10V7K HDMI CLK+ UMA	HDMI_CLK+_UMA <17>
PCIE_MTX_GRX_N3	C904	1	2	UMA@0.1U 0402 10V7K HDMI CLK- UMA	HDMI_CLK-_UMA <17>







DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)

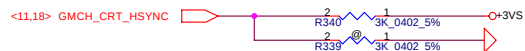


RS780 DFT_GPIO1 <11> SUS_STAT_R# PLT_RST# <11,19,26,28,30>

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

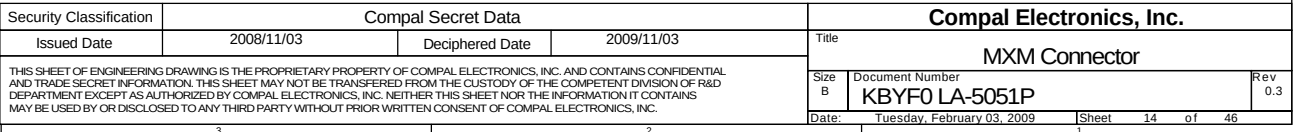
RS780 use HSYNC to enable SIDE PORT

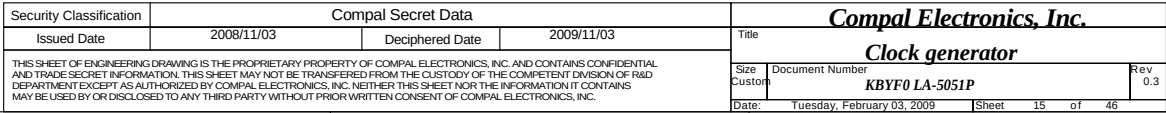


RS780 use HSYNC to enable SIDE PORT

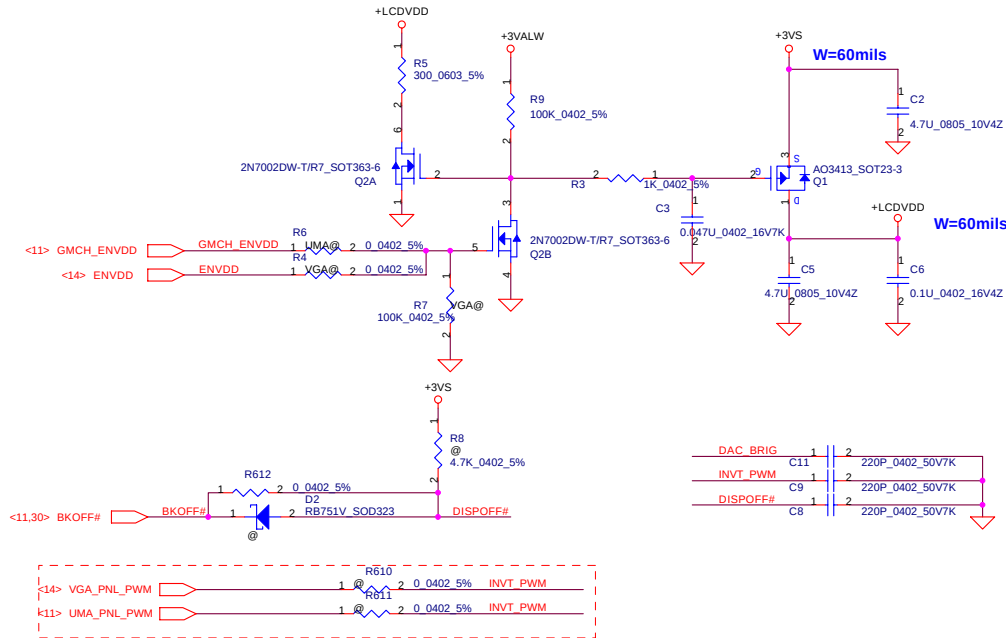
RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
0. Enable (RS780)
1 : Disable(RS780)

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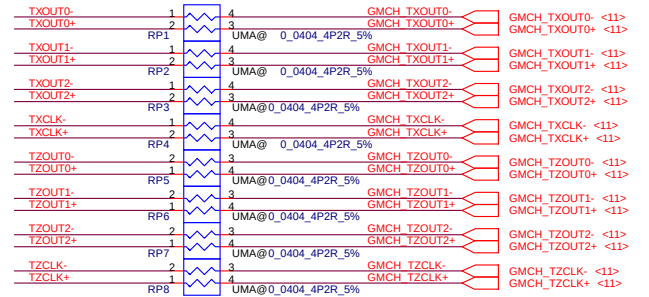
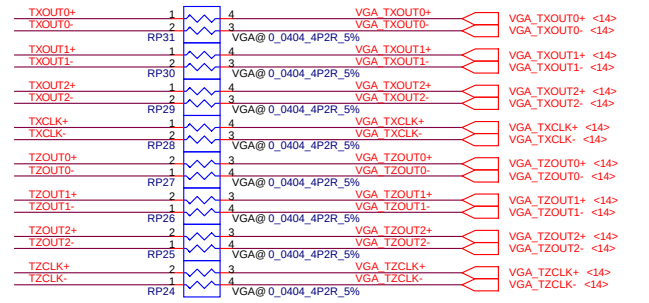
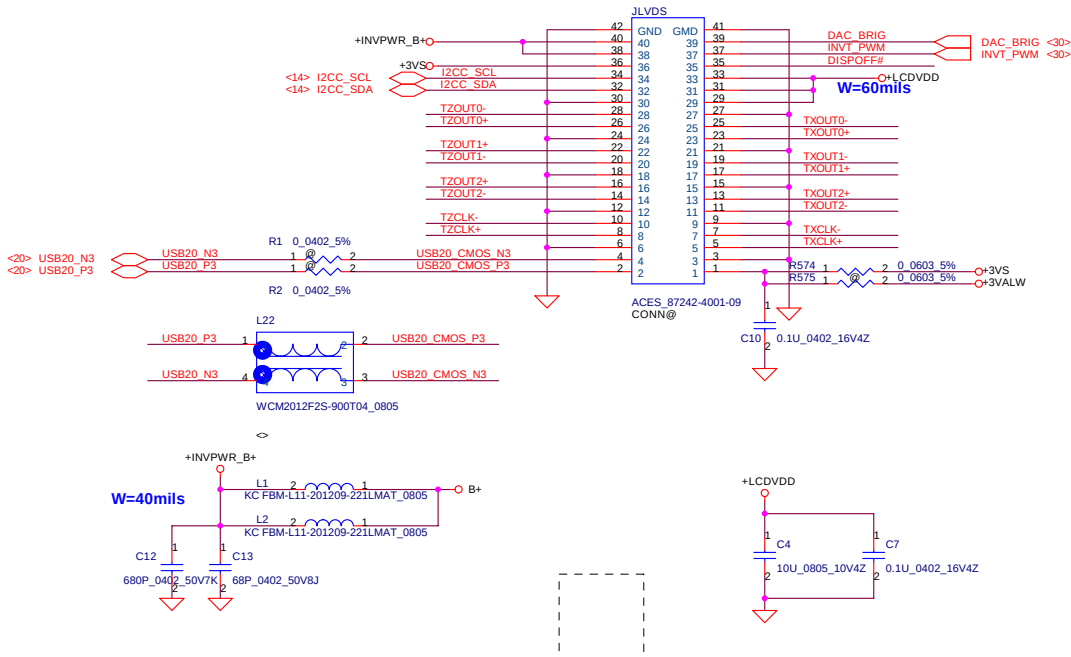




LCD POWER CIRCUIT

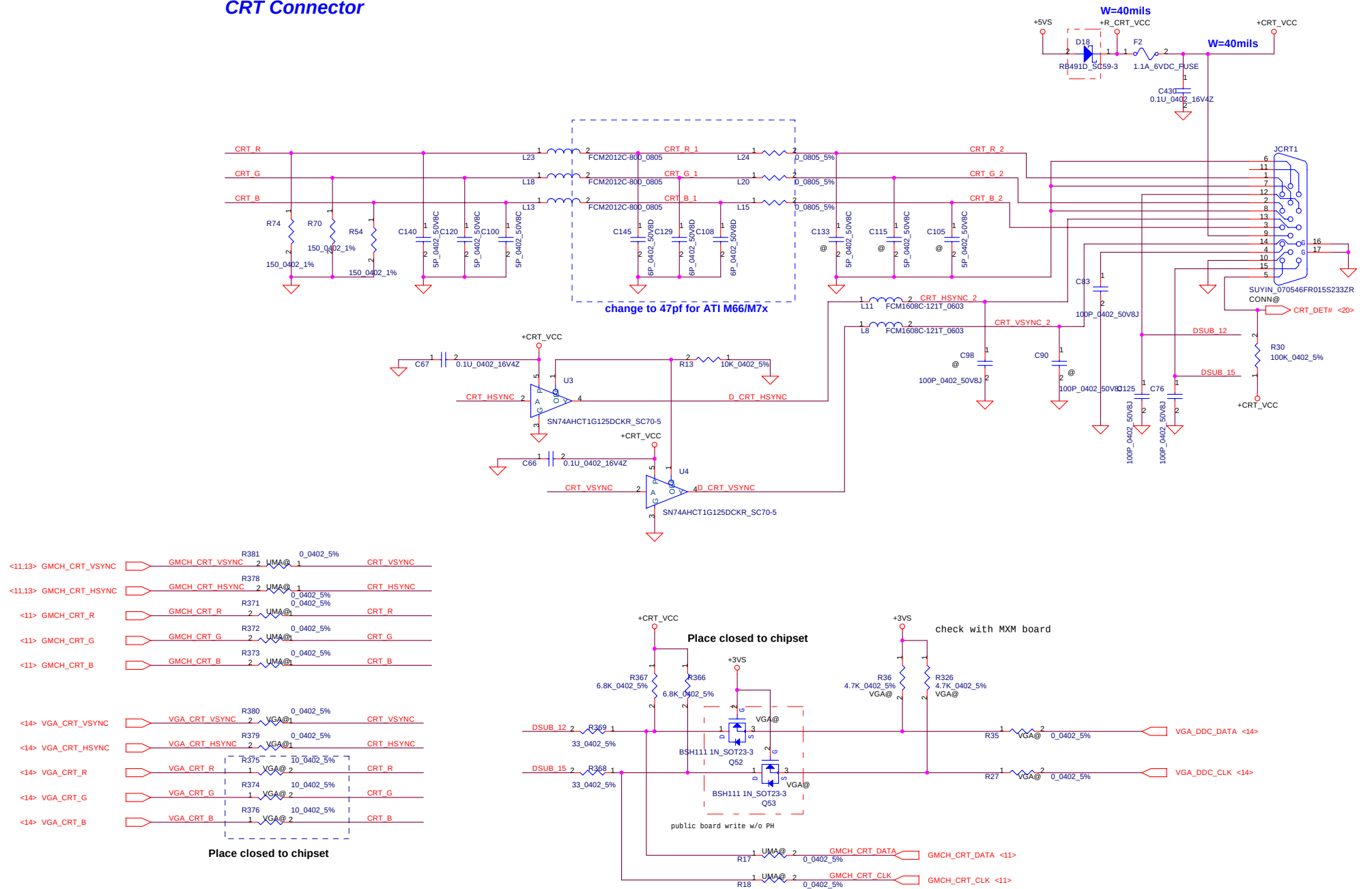


LCD/PANEL BD. Conn.



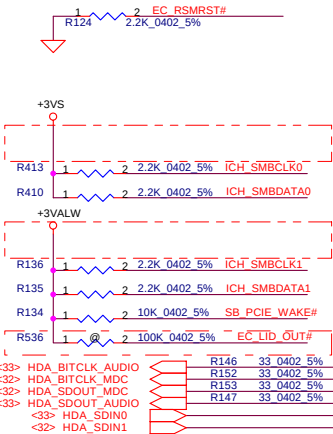
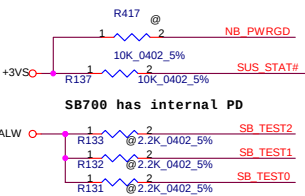
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2008/11/03				Title			
Deciphered Date				2009/11/03				LVDS & DVI Connector			
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								KBYFO LA-5051P			
								Rev 0.3			
								Date: Tuesday, February 03, 2009			
								Sheet 16 of 46			

CRT Connector

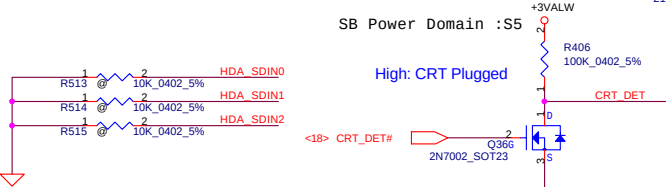


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/11/03	Deciphered Date	2009/11/03	Title CRT Connector		
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					KBYF0 LA-5051P	0.3
				Date	Tuesday, February 03, 2009	Sheet 18 of 46

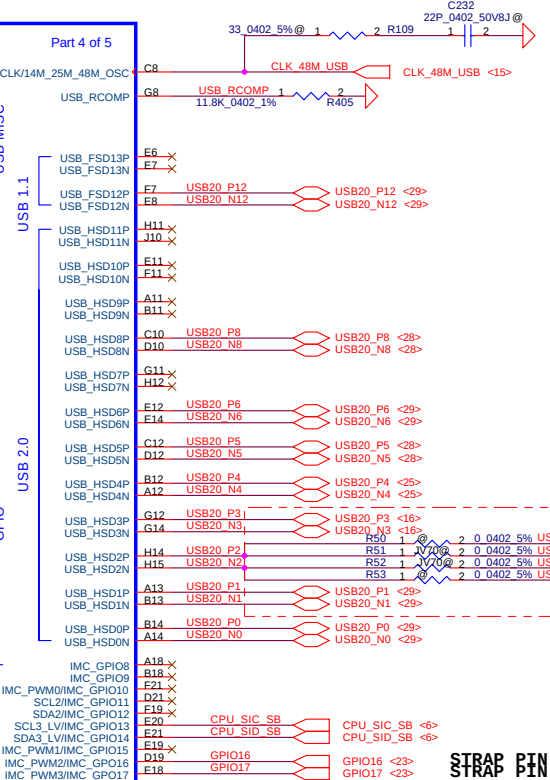
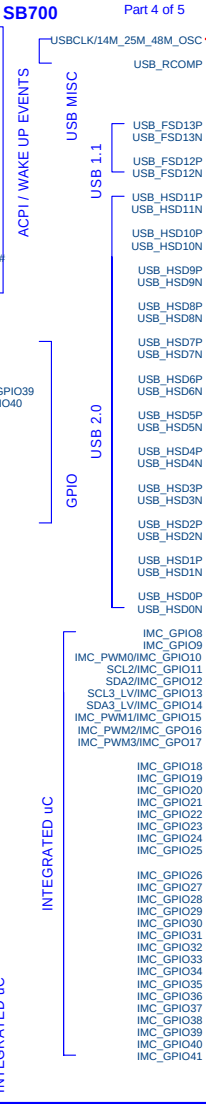
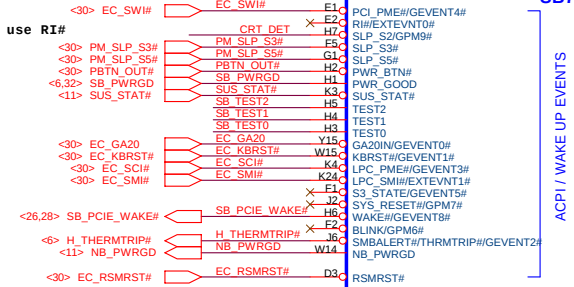
SKU-ID	R509	R510
UMA		POP
DIS	POP	



STRAP PIN <23> HDARST#



demo circuit LID use RI#



USB-12 Bluetooth

USB-8 MiniCard(WLAN)

USB-6 HS-USB

USB-5 MiniCard(TV)

USB-4 Card Reader

USB-3 USB Camera

USB-2 USB (eSATA) for SJM70
Ext.USB/B for SJV70

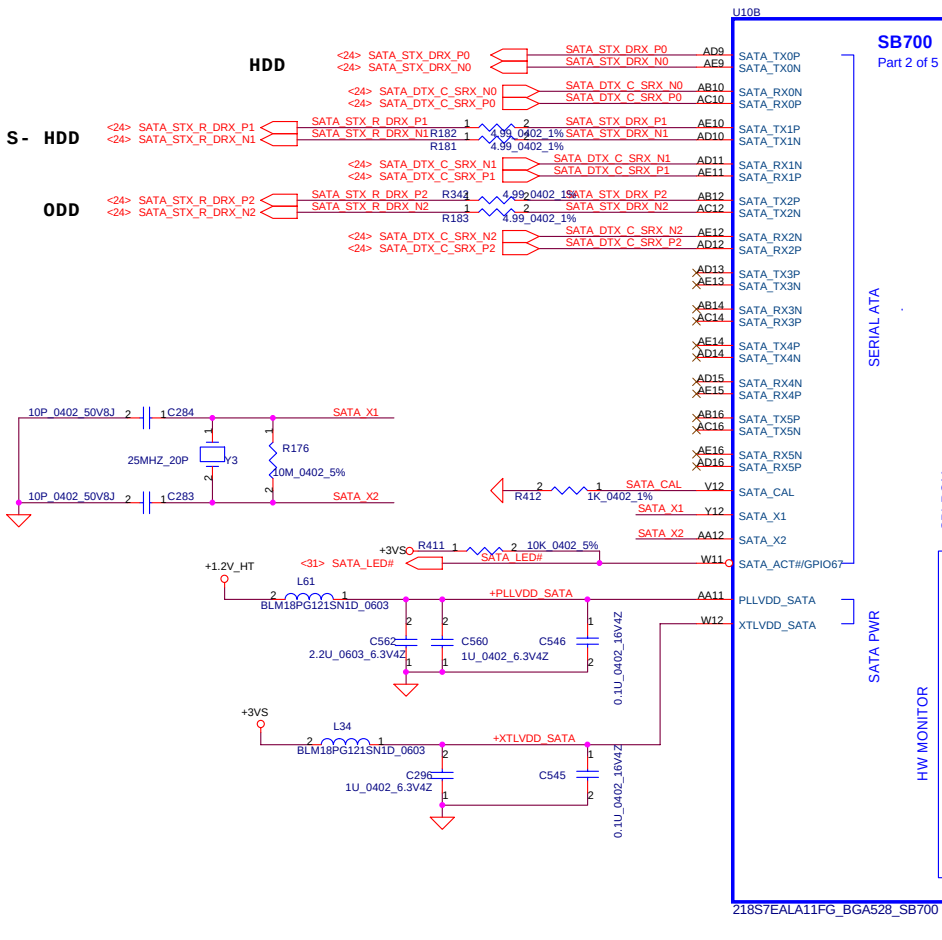
USB-1 Ext.USB/B

USB-0 Ext.USB/B

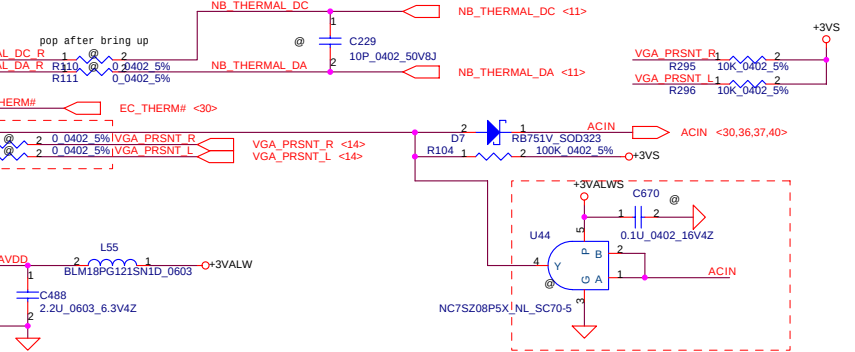
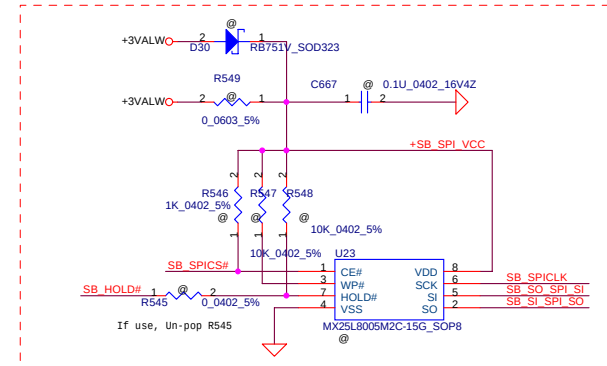
STRAP PIN

Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/03	Deciphered Date	2009/11/03	Compal Electronics, Inc.	
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Size	Document Number	Rev		0.3	
Custom	KBYP0 LA-5051P				
Date:	Tuesday, February 03, 2009	Sheet	20	of	46

S - HDD
ODD



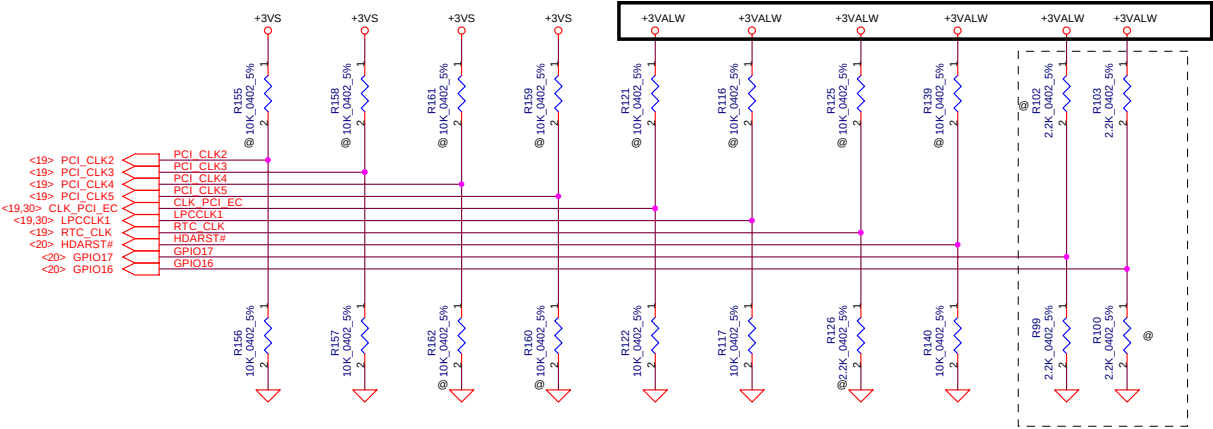
Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller



REQUIRED STRAPS

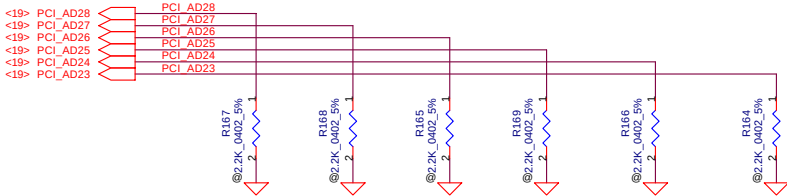
NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

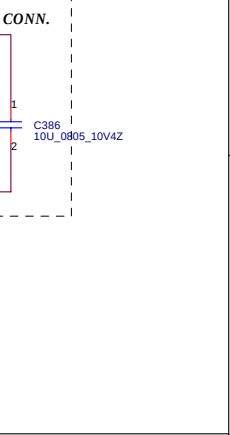
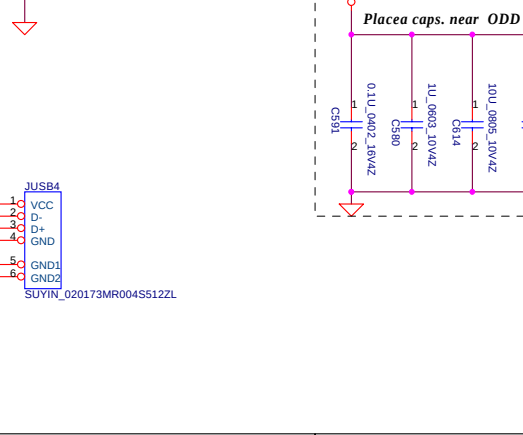
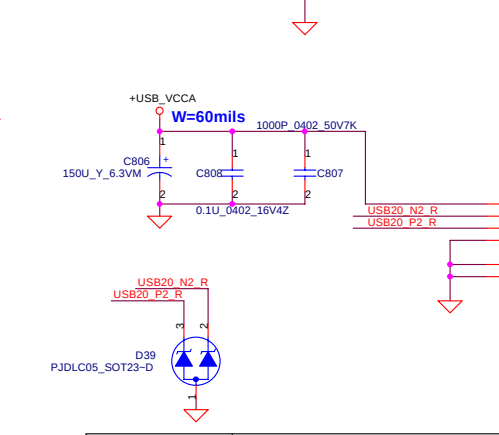
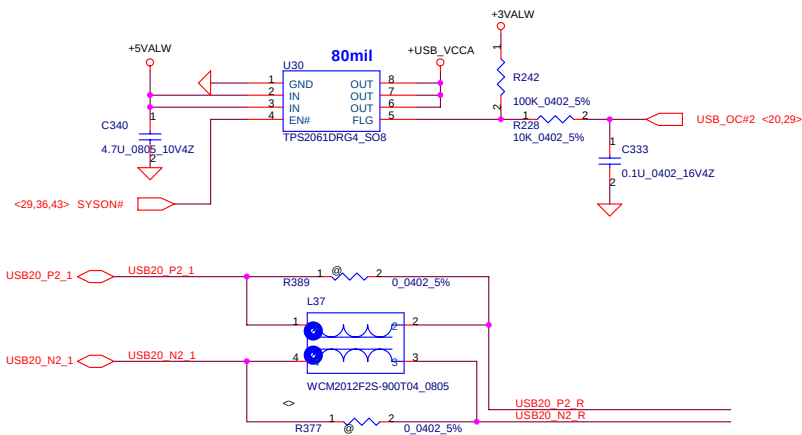
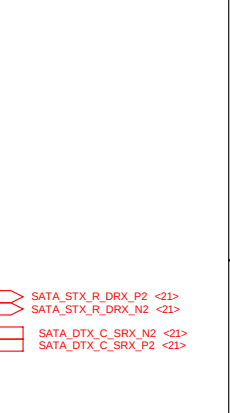
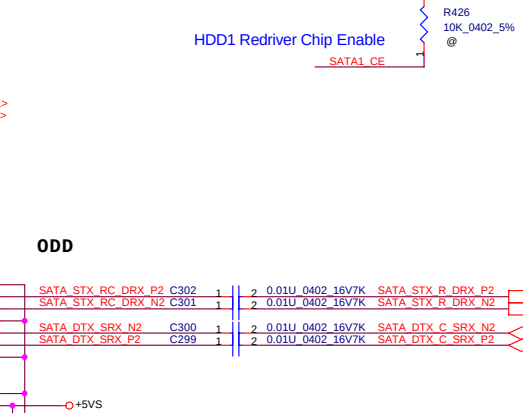
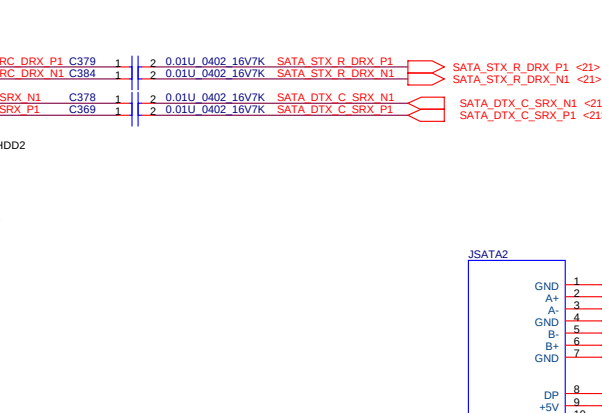
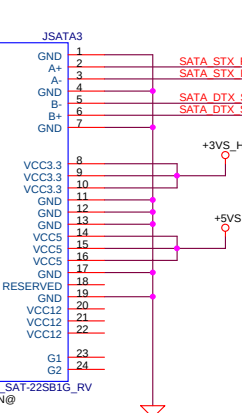
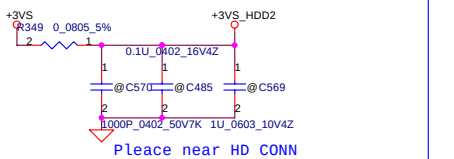
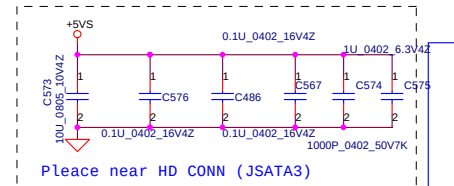
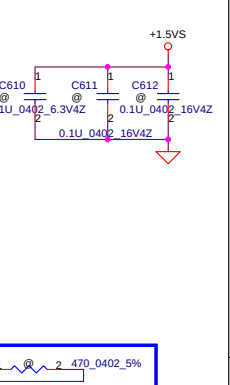
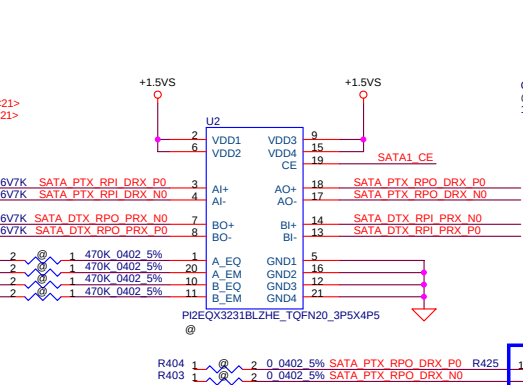
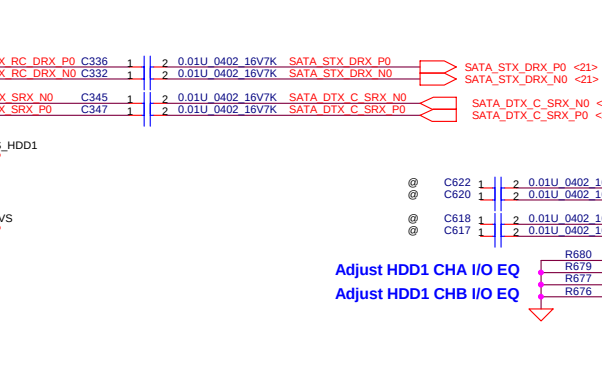
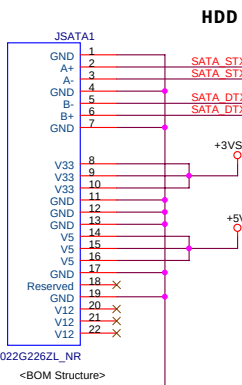
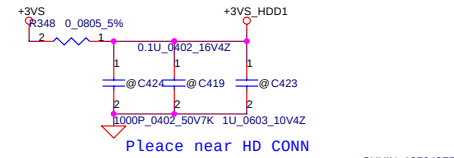
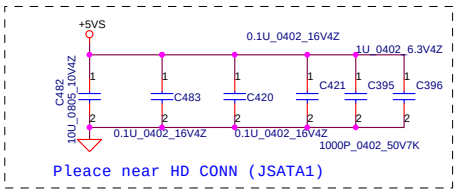
	PCI_CLK2 CLK_PCI_PCM	PCI_CLK3 CLK_PCI_DBG	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default L,NC) L,L = FWH ROM



DEBUG STRAPS
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

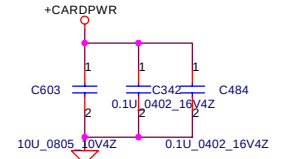
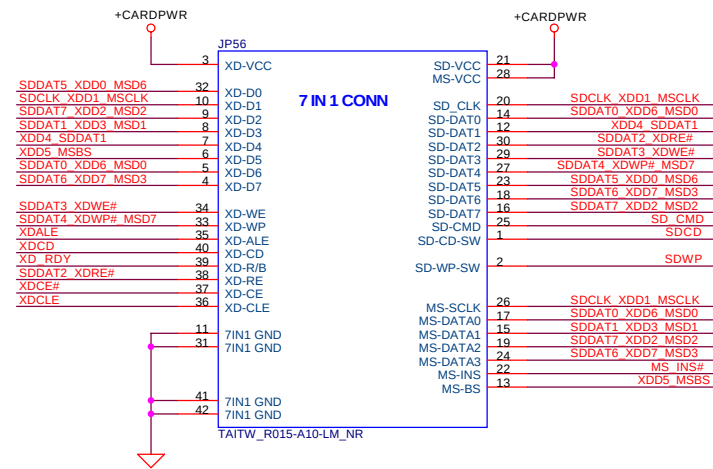
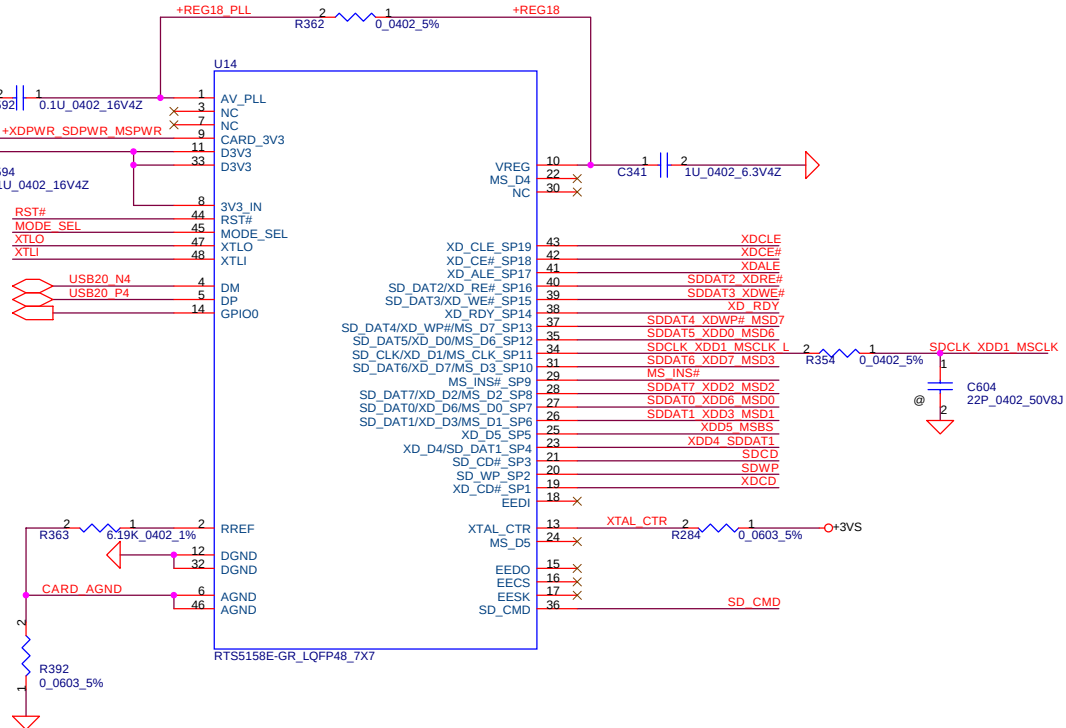
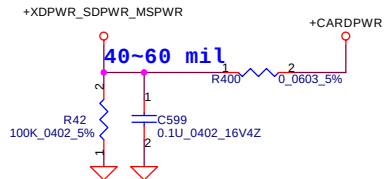
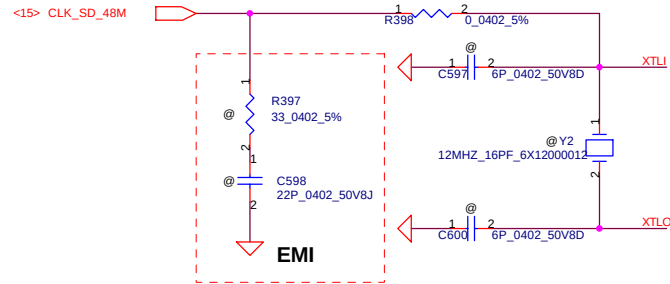
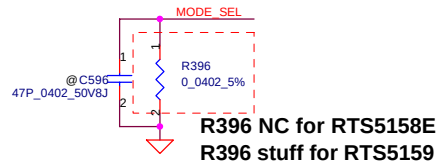
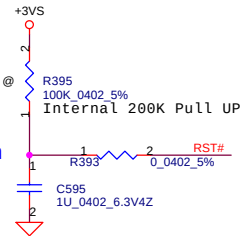
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



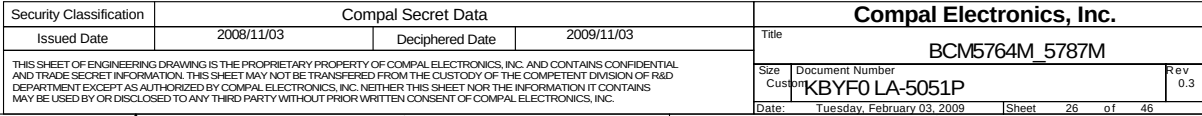


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Issued Date				2008/11/03				Deciphered Date			
								2009/11/03			
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Title				HDD & ODD Connector				Document Number			
Size				B				KBYFO LA-5051P			
Date:				Tuesday, February 03, 2009				Sheet 24 of 46			
Rev				0.3							

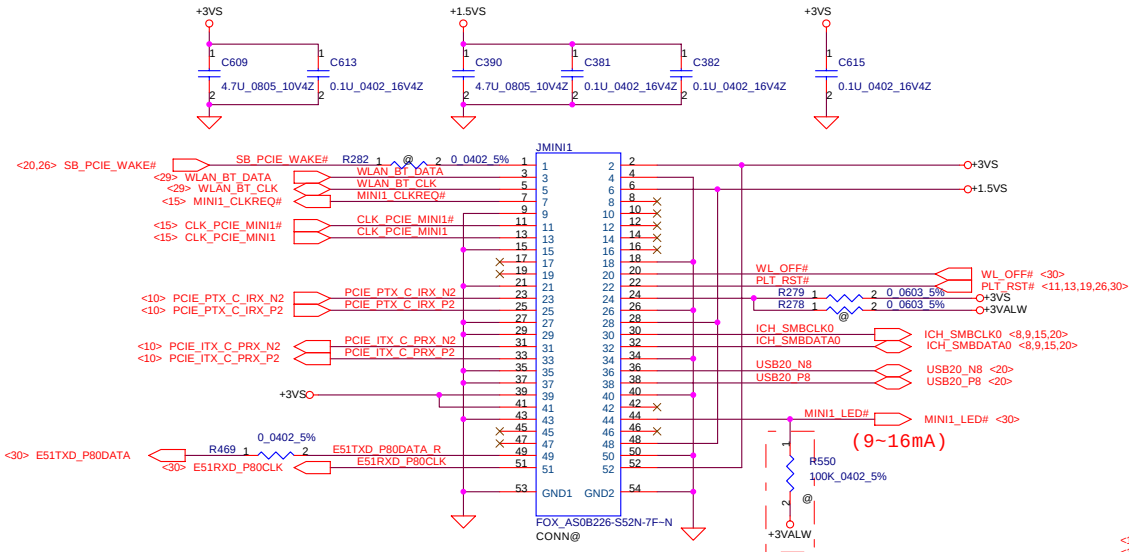
Vender suggestion



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Issued Date	2008/11/03	Deciphered Date	2009/11/03	Title	
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Size	Document Number	Rev		0.3	
Cust	KBYFO LA-5051P	Date		Tuesday, February 03, 2009	
Sheet		25		of 46	



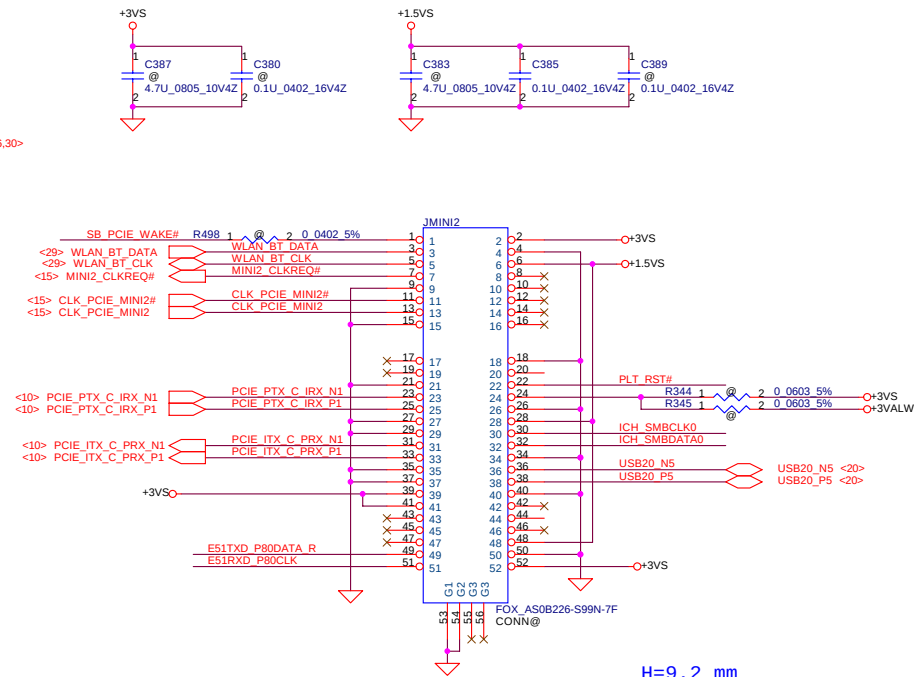
For Wireless LAN



H=5.2 mm

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

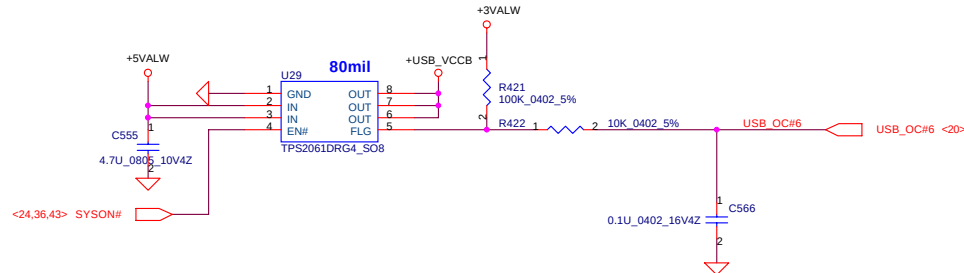
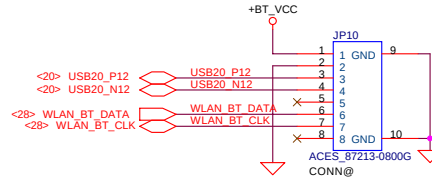
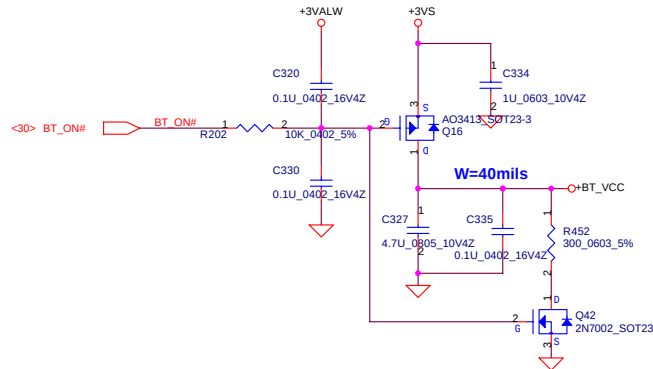
For TV-Tuner/HW MPEG



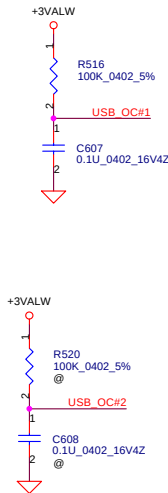
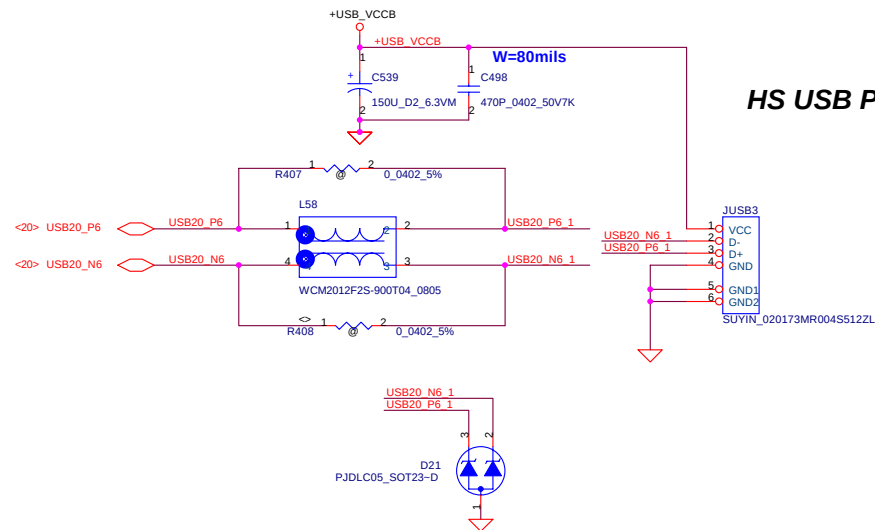
H=9.2 mm

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								2009/11/03			
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Title				MINI CARD (WLAN & TV-Tuner)				Document Number			
Size B				KBYF0 LA-5051P				Rev 0.3			
Date:				Tuesday, February 03, 2009				Sheet 28 of 46			

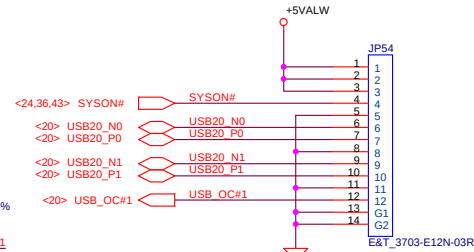
Bluetooth Conn.



HS USB PORT

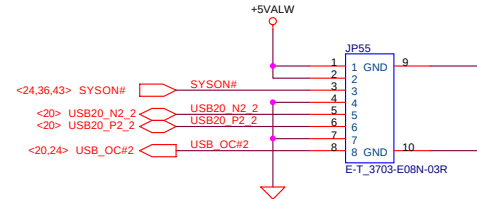


2 PORT



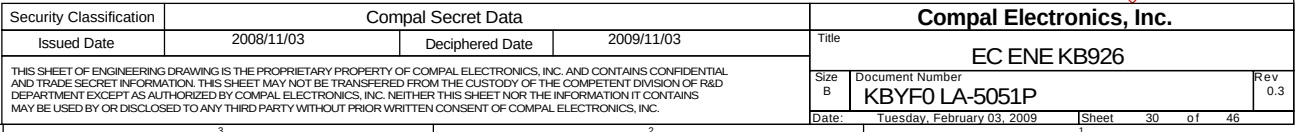
right

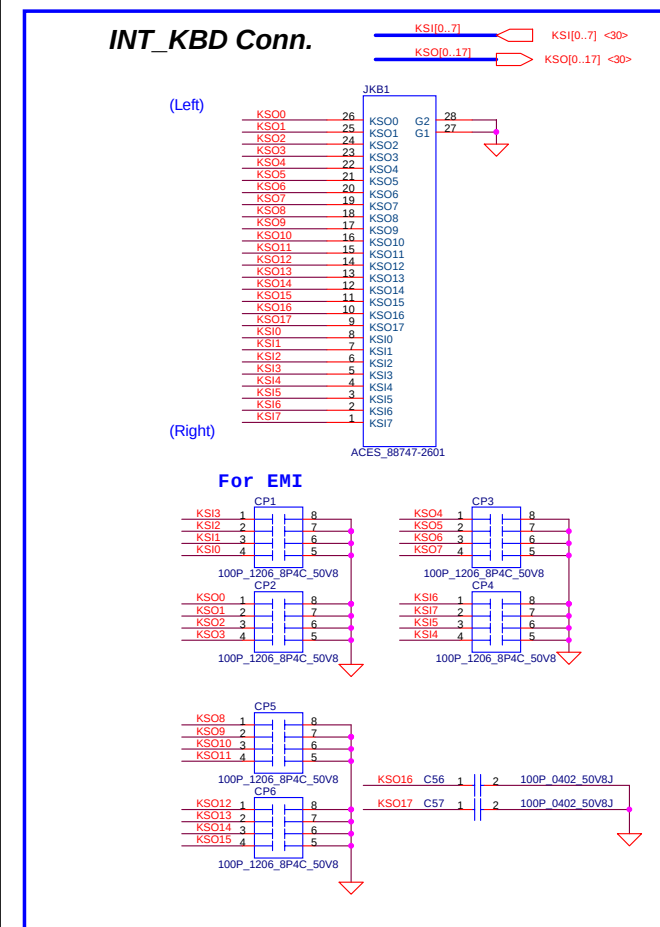
1 PORT FOR JV70



Right Up

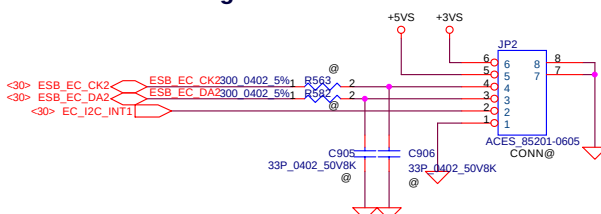
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2008/11/03	Deciphered Date	2009/11/03	Title	
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				Date: Tuesday, February 03, 2009	Rev 0.3
				Sheet 29	of 46



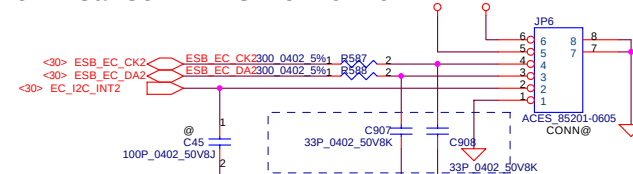


To Media/B Conn.

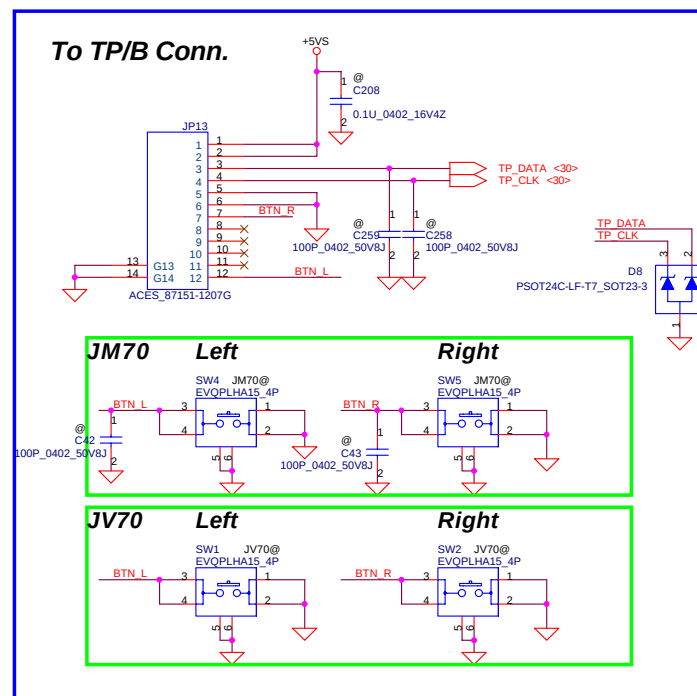
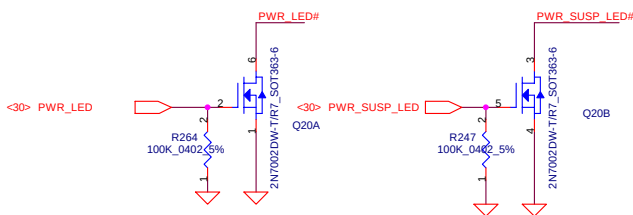
CAP Sansor right JM70



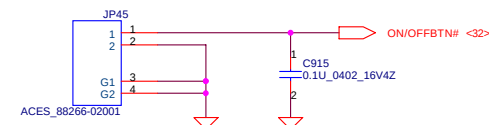
CAP Sansor lift for JM70



CAP Sensor up for JV70

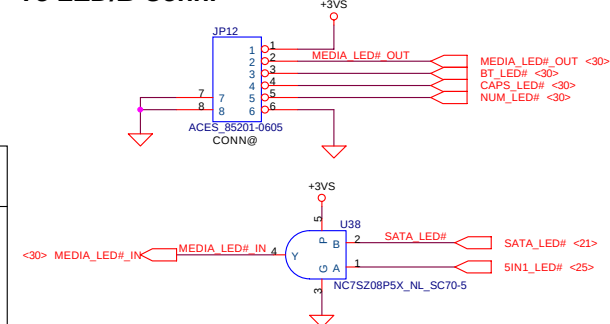


TO POWER BTN/B for JV70

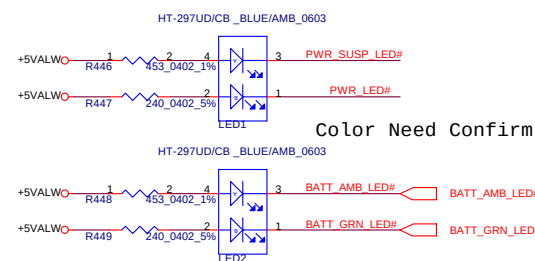


Need Check

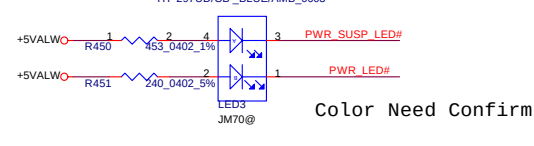
To LED/B Conn.



JM70



HT-297UD/CB BLUE/AMB 0603

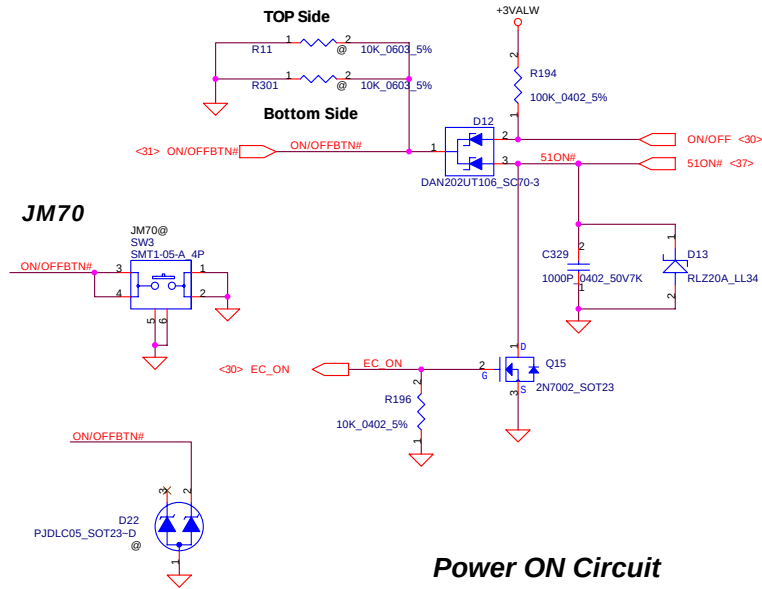


JM70	JV70
1.HDD	1.HDD
2.BT_LED	2.BT_LED
3.CAP_LED	4.NUM_LED
4.NUM_LED	3.CAP_LED

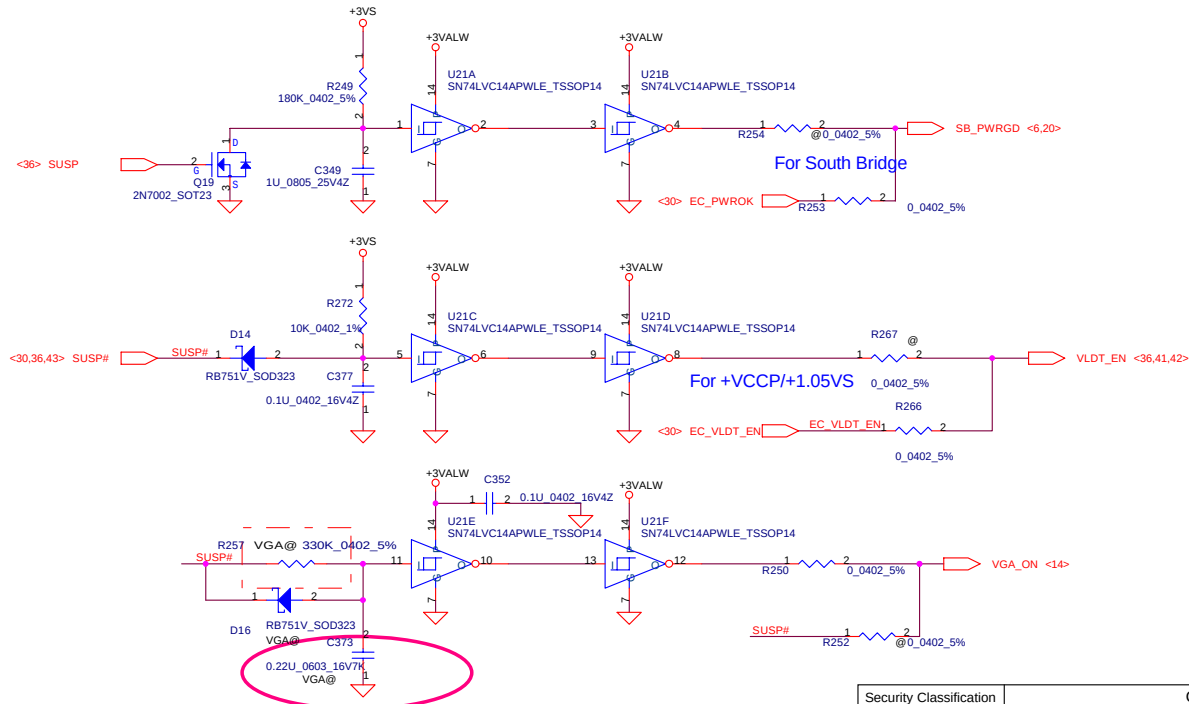
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2008/11/03	Deciphered Date	2009/11/03	Title	BIOS, I/O Port & K/B Connector		
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					KBYFO LA-5051P	0	
				Date	Tuesday, February 03, 2009	Sheet	31 of 46

Power Button

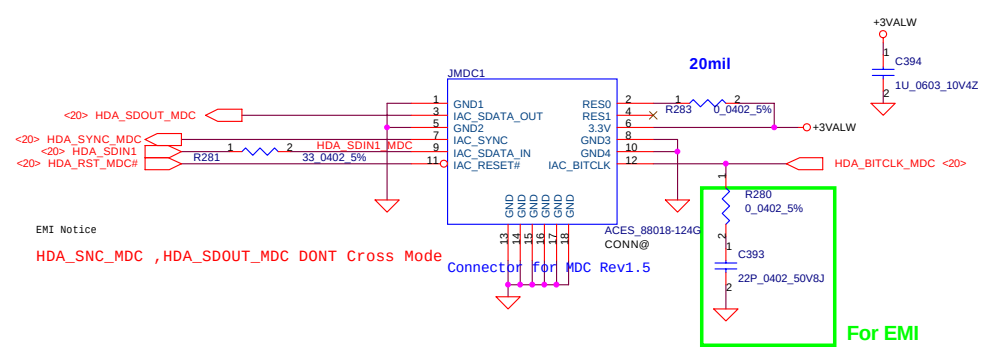
ON/OFF switch



Power ON Circuit

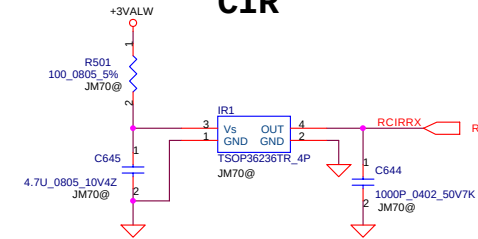


HDA MDC Conn.



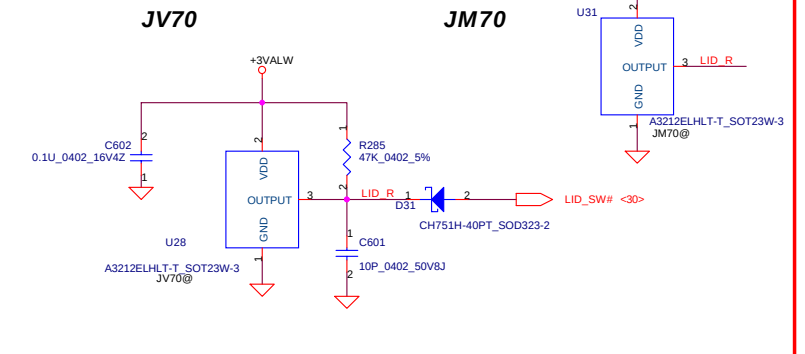
JM70

CIR



Lid Switch

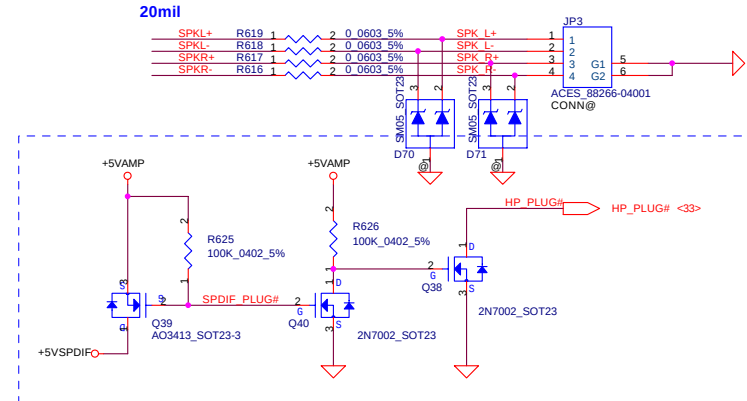
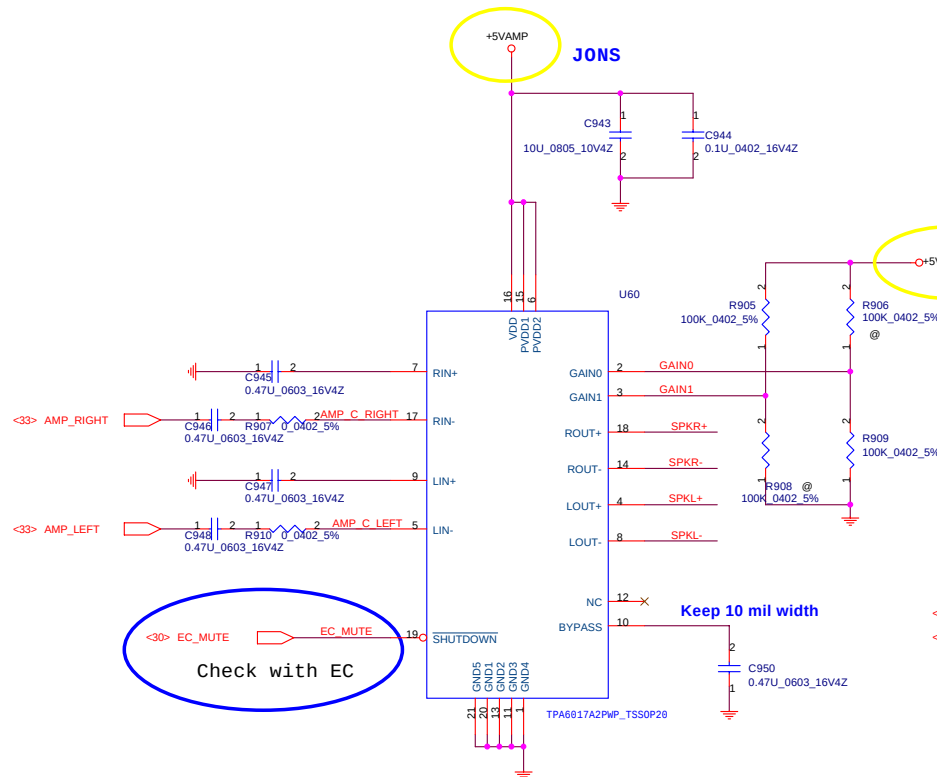
(Hall Effect Switch)



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Issued Date	2008/11/03	Deciphered Date	2009/11/03	Title	Power OK, Reset and RTC Circuit, TP
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				KBYF0 LA-5051P	
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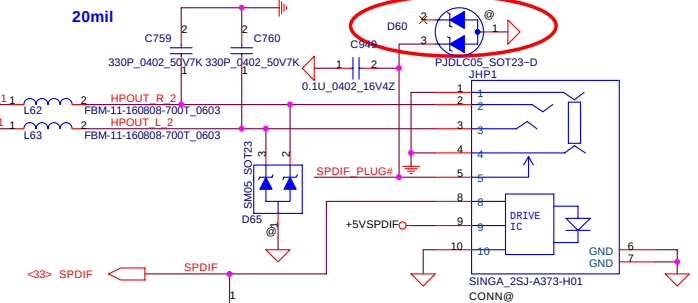
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				HD Audio Codec ALC268				
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Int. Speaker Conn.

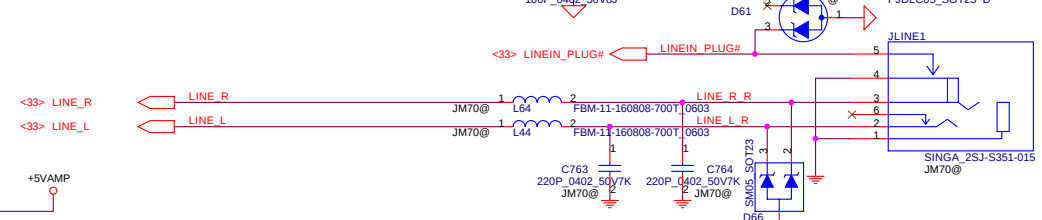


LINE Out/Headphone Out

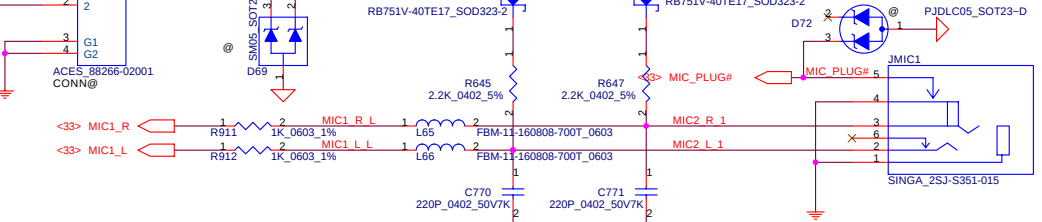
2007/12/07 S/PDIF Out JACK



JM70 LINE-IN JACK



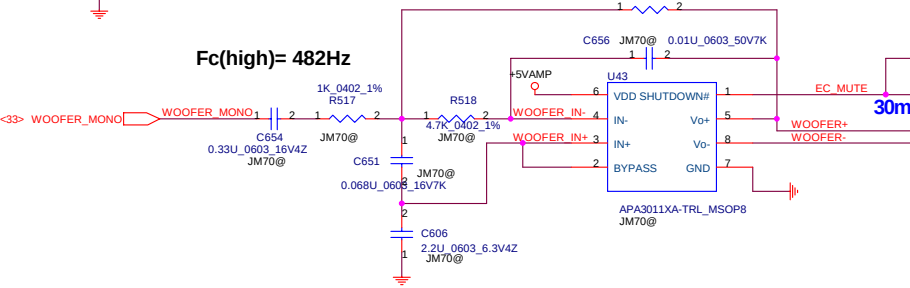
MIC JACK



JM70 Gain = 5.1dB(BTL Mode)

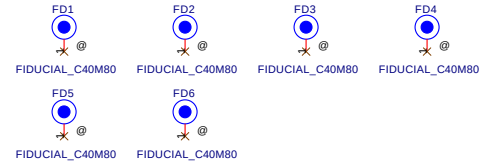
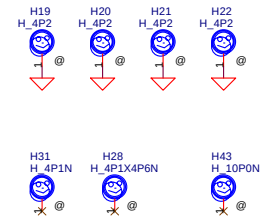
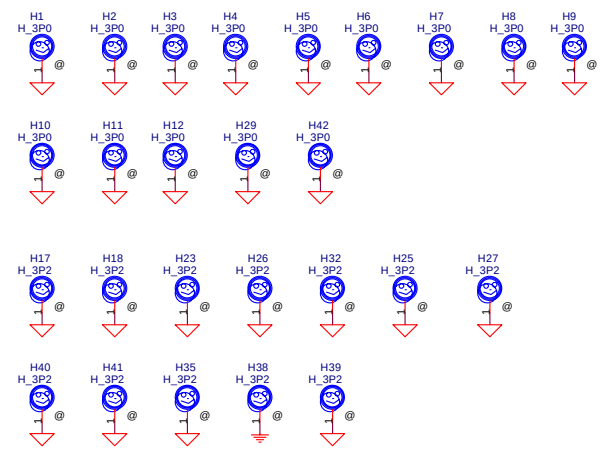
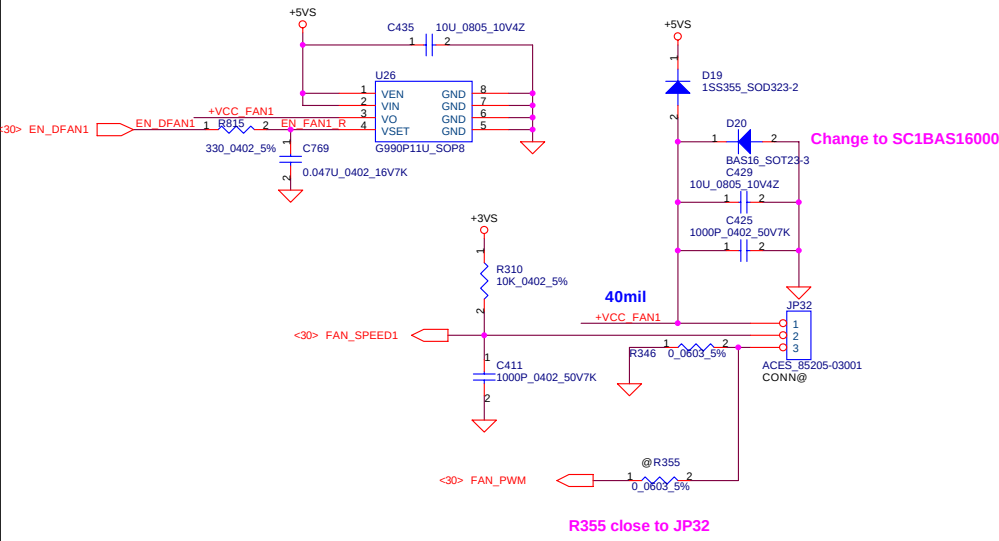
Fc(low)= 2KHz

Fc(high)= 482Hz

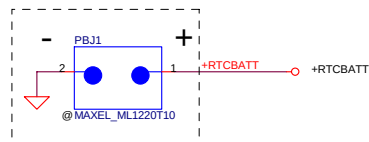
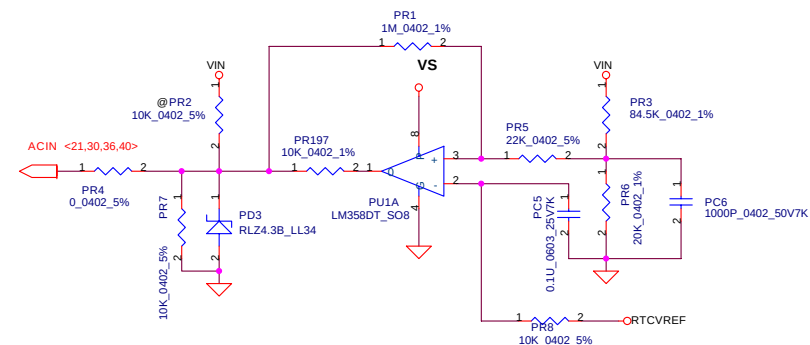


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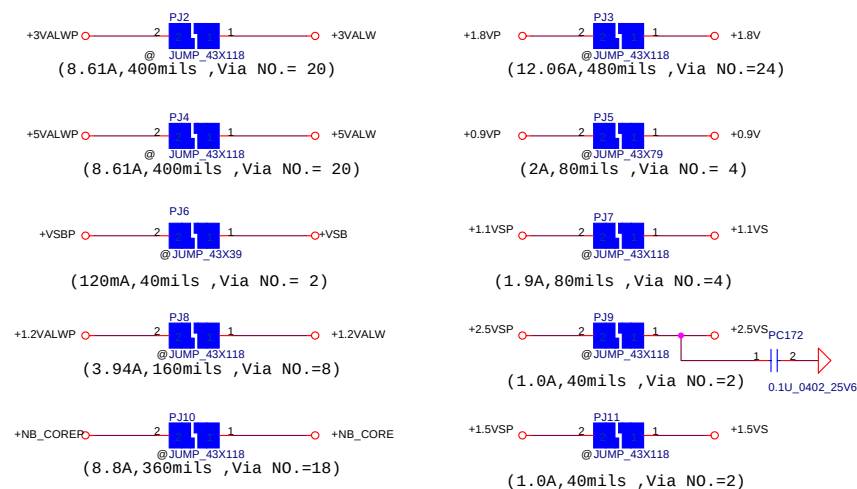
FAN1 Conn



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				0.3	

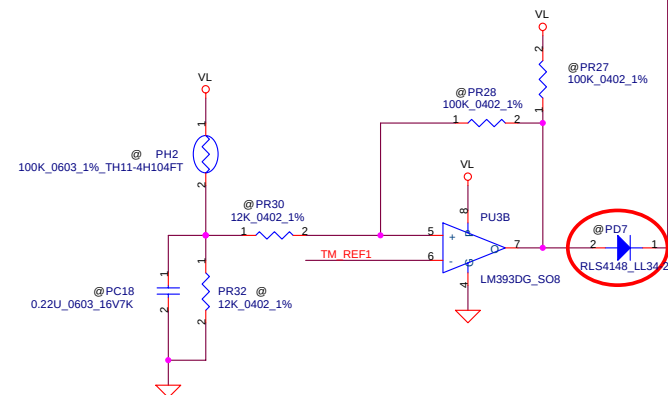
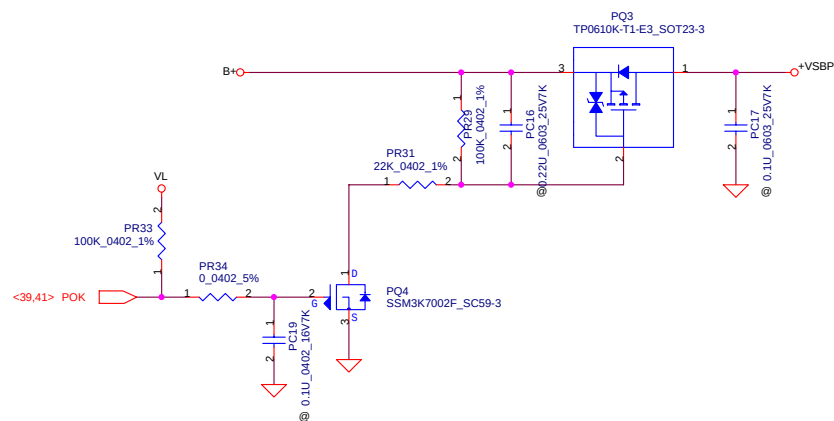
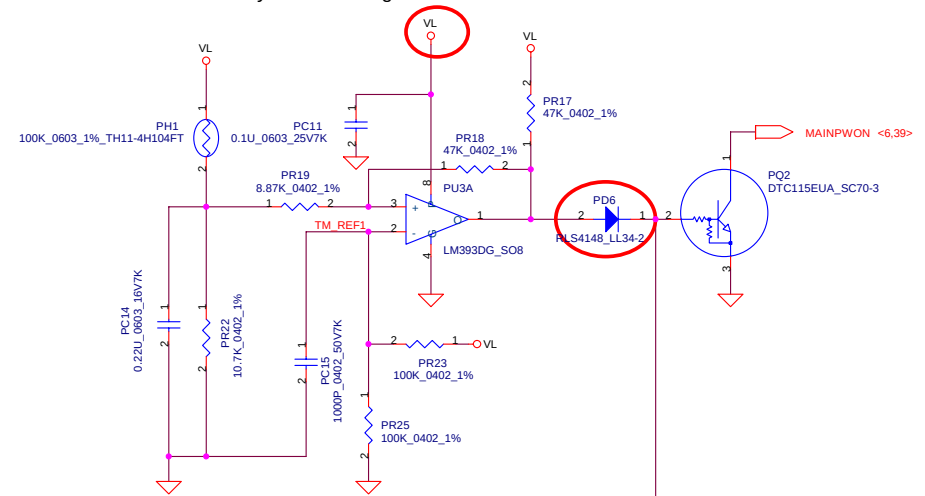
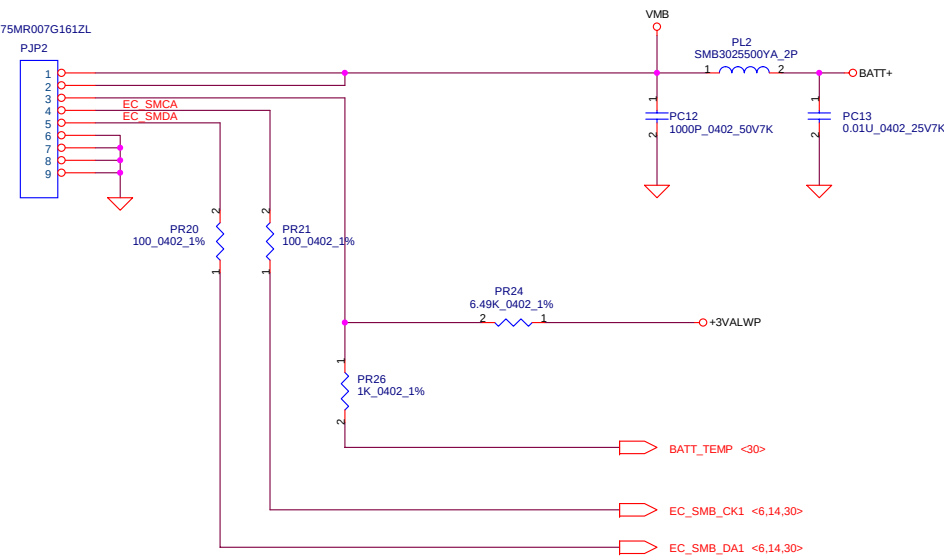


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

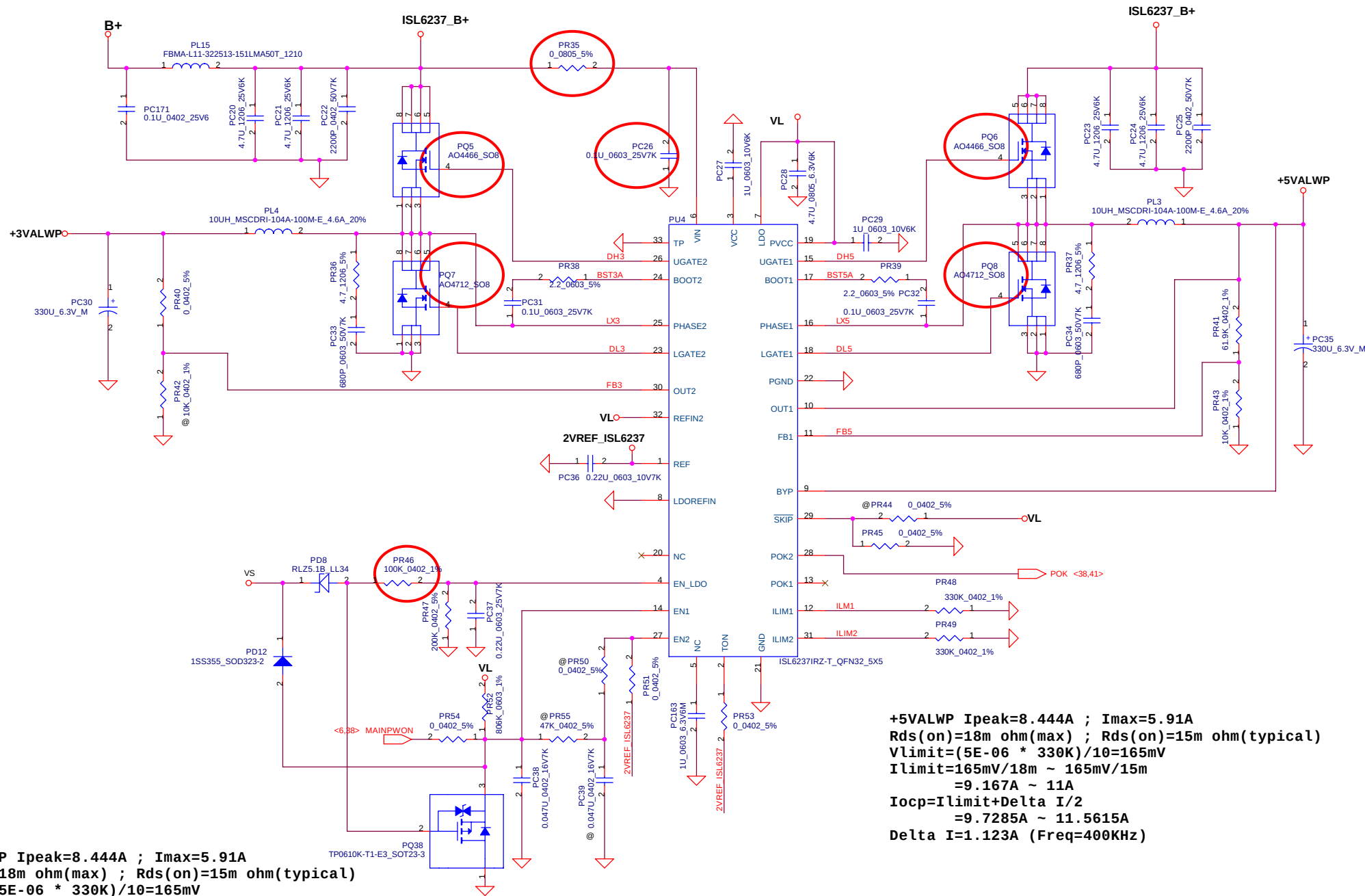


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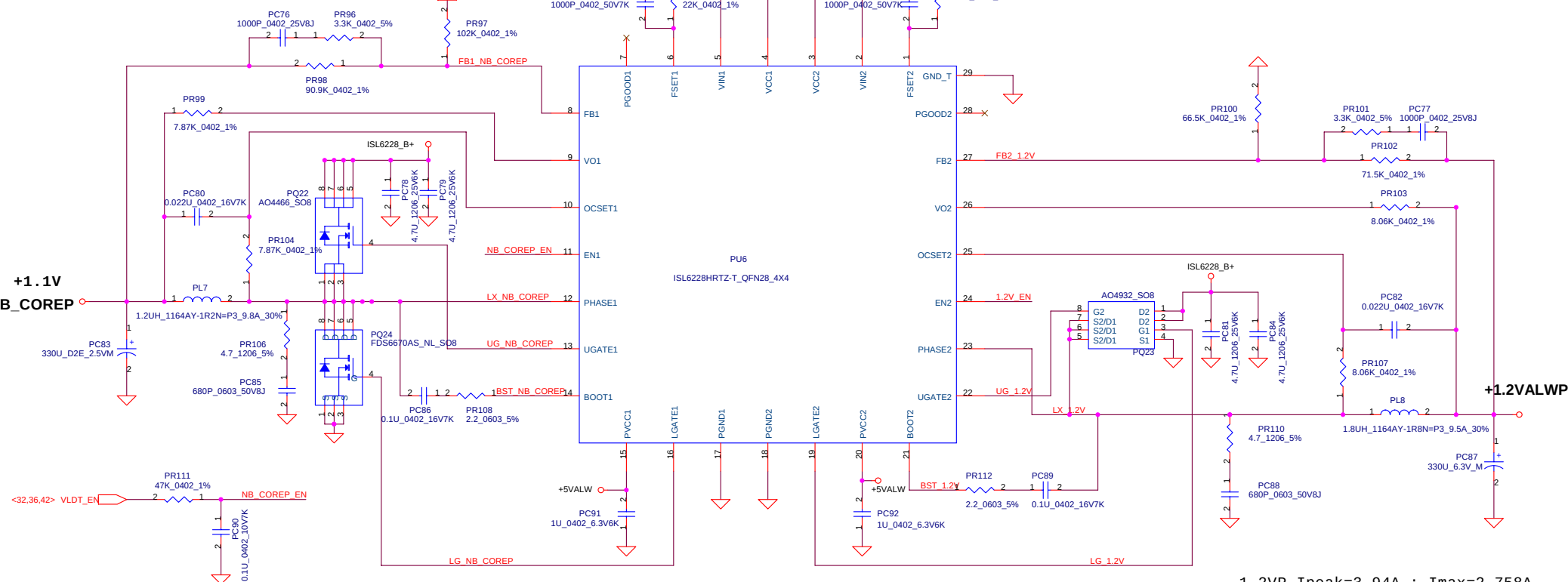


+5VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.7285A ~ 11.5615A
Delta I=1.123A (Freq=400KHz)

+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.721A ~ 11.554A
Delta I=1.108A (Freq=300KHz)

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POWER_SEL	
HIGH	1.0V
LOW	1.1V



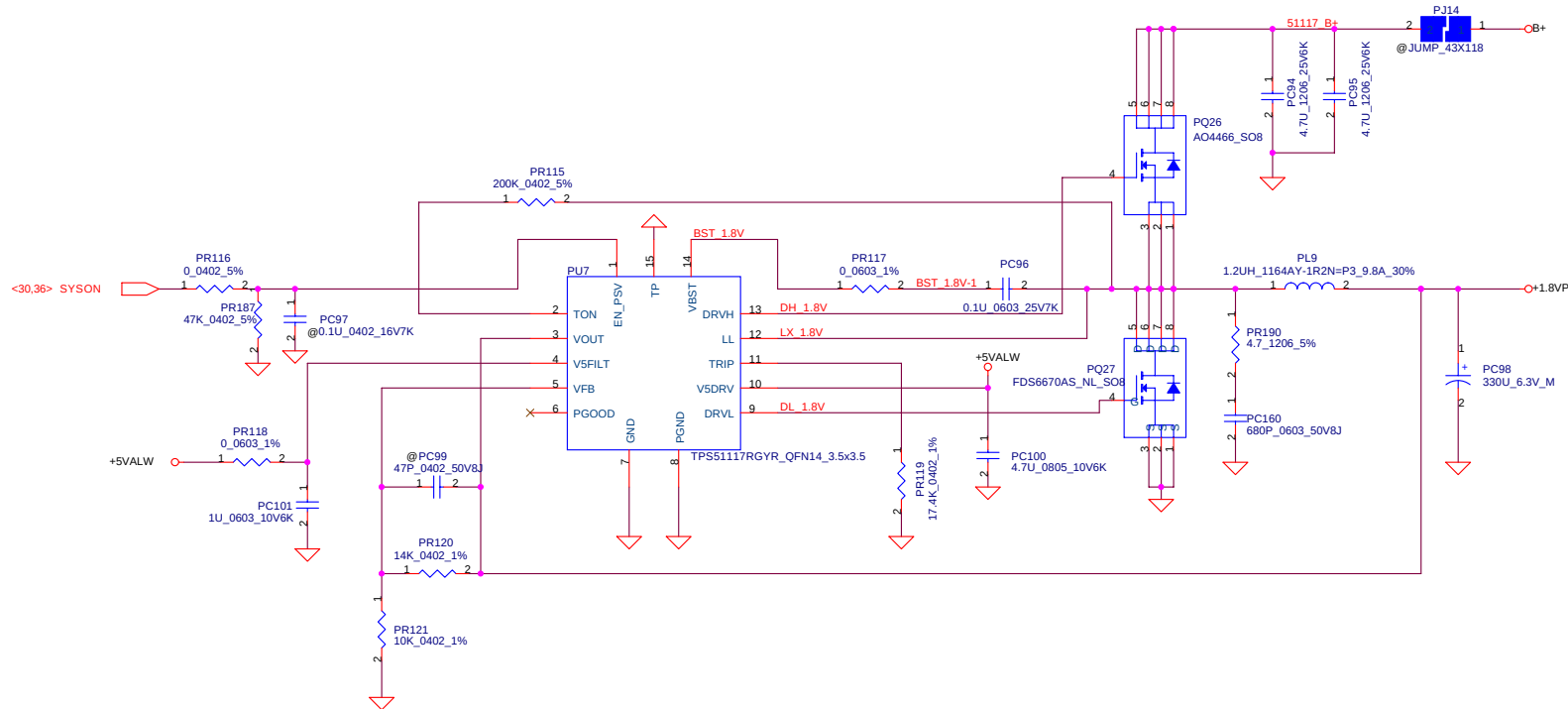
1.1VP Ipeak=8.9A ; Imax=6.23A
DCR=6m ohm (max)
Rocset=(Iocp*DCR)/10E-06=7.68K ohm
Iocp=9.846A(1.3*DCR)
Csen=L/(Rocset*DCR)=0.022uF

Freq=303KHz
Rfset=1/(1.5E-10 * Freq)=22K

1.2VP Ipeak=3.94A ; I_{max}=2.758A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=6.65K ohm
Iocp=5.542A(1.2*DCR)
Csen=L/(Rocset*DCR)=0.027uF

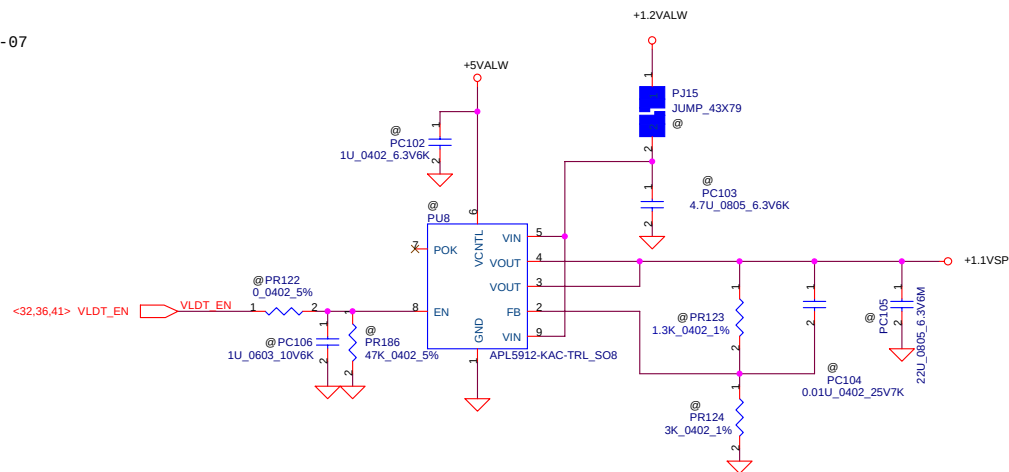
Freq=366KHz
Rfset=1/(1.5E-10 * Freq)=18.2K

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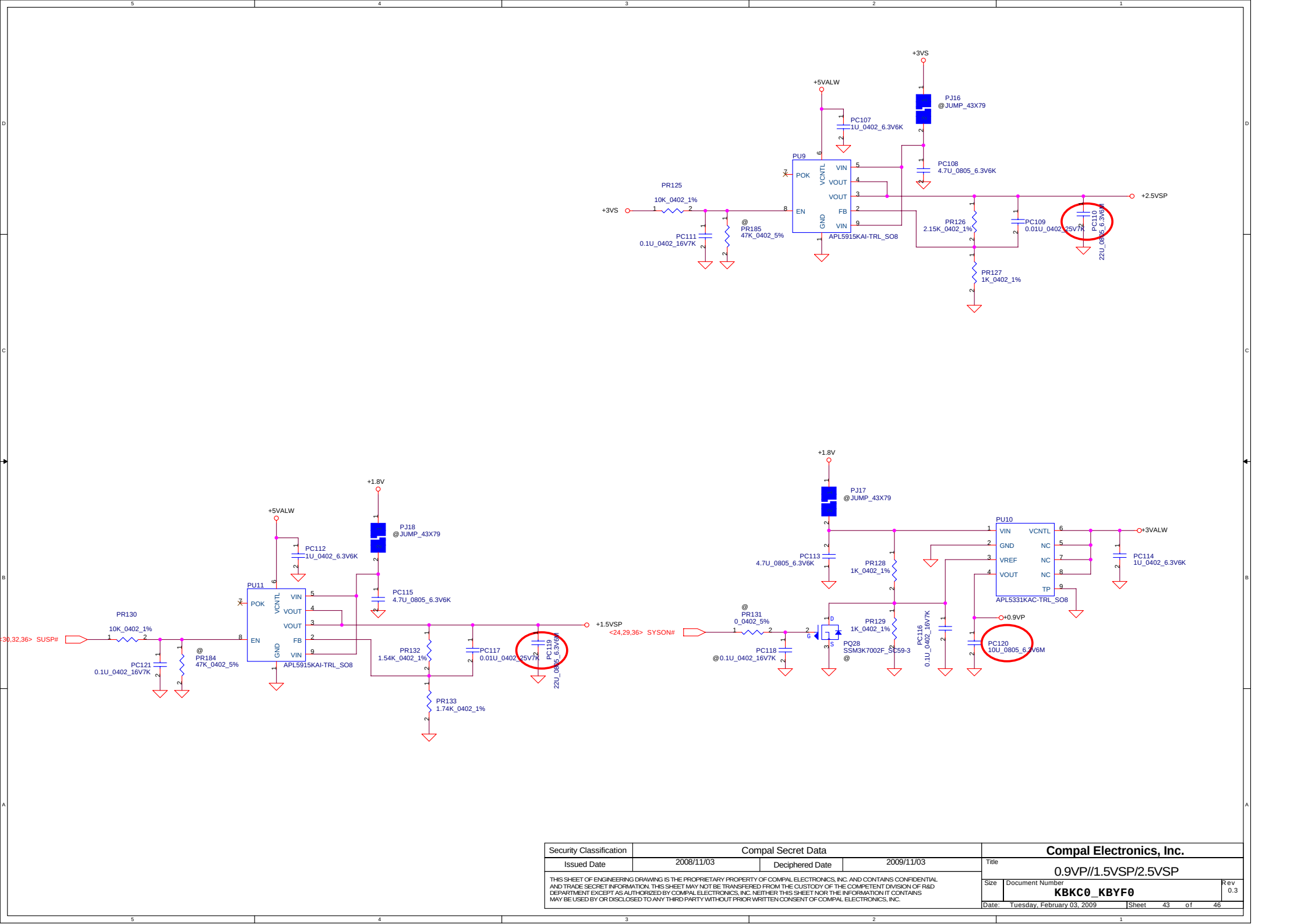


VFB=0.75V
 $V_o = VFB \cdot (1 + PR120/PR121) = 1.8V$
 $Ton = 19E-12 \cdot Ron \cdot ((2/3) \cdot V_o + 100mV) / (Vin) + 50ns = 3.1E-07$
 Freq=305KHz

Cesr=15m ohm
 $I_{peak} = 12.6A$ $I_{max} = 8.82A$
 $\Delta I = ((19-1.8) \cdot (1.8/19)) / (L \cdot Freq) = 5.332A$
 $V_{trip} = R_{trip} \cdot I_{0uA} = 0.24V$
 $I_{ocp_min} = V_{trip} / R_{dsonmax} \cdot 1.4 + 2.666 = 17.573A$
 $I_{ocp_max} = V_{trip} / R_{dsonmax} \cdot 1.2 + 2.666 = 26.908A$
 $I_{ocp} = 17.573-26.908A$



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	EMI request.	EMI request.	0.1	40	Change PR38, PR39, PR108, PR112, PR136, PR150, PR163 from SD0130000080 to SD013220B80.	08, 12/24	to DVT
2	EMI request.	EMI request.	0.1	40	Add PC170, PC171, PC172, PC173, PC174 SE00000G880 S CER CAP 0.1U 25V K X5R 0402	08, 12/24	to DVT
3	EMI request.	EMI request.	0.1	39	Add PL15 SM010016410 S SUPPRE_ KC FBMA-L11-322513-151LMA50T	08, 12/24	to DVT
4	EMI request.	EMI request.	0.1	41	Add PL14 SM010018210 S SUPPRE_ TAI-TECH HCB4532KF -800T90 1812	08, 12/24	to DVT
5	Link CIS error.	Link CIS error.	0.1	40	Change PQ9, PQ10, PQ12 from SB944070000 S TR A04407 1P S08 W/D to SB00000DL00 S TR A04407A 1P S08	08, 12/24	to DVT
6	cost down	cost down	0.1	40	Change PC30 from SGA19331360 S POLY C 330U 6.3V M D3L ESR25M TPE H2.8 to SF000001G00 S_A-P_CAP 330U 6.3V M 6.3X5.7 LESR14M ME	08, 12/24	to DVT
7	cost down	cost down	0.1	40	Change PC35 from SGA20151320 S POLY C 150U 6.3V M D2E TPE ESR18 H1.8 to SF000001G00 S_A-P_CAP 330U 6.3V M 6.3X5.7 LESR14M ME	08, 12/24	to DVT
8	cost down	cost down	0.1	41, 42	Change PC87, PC98 from SGA19331D00 S POLY C 330U 2.5V M D2 TPE LESR15M H1.8 to SF000001G00 S_A-P_CAP 330U 6.3V M 6.3X5.7 LESR14M ME	08, 12/24	to DVT
9	schematic update.	schematic update.	0.1	44	Delete PR198 SD028100380 S RES 1/16W 100K +-5% 0402	08, 12/24	to DVT
10	layout space too small.	layout space too small.	0.1	41	Change PQ23 from SB00000CG00 S TR A04466 1N S08 to SB00000BG00 S TR A04932 2N S08 Delete PQ25 SB00000AJ00 S TR A04712 1N S08	08, 12/24	to DVT
11							
12							
13							
14							
15							
16							
17							
18							

NO DATE		PAGE	MODIFICATION LIST	PURPOSE
12/17	p.12		L3,L4 change from bead to 0 Ohm	
12/17	P.17		Add R858~R865 for VGA HDMI	
12/17	P.18		R374,R375,R376 change from 0 ohm to 10 ohm	
12/17	P.20		R50 ,R53 change from JV70@ to @	
12/17	P.20		R51 ,R52 change from JM70@ to JV70@	
12/17	P.24		JP18 change from ESATA to USB port	
12/17	P.25		R396 change from 10K to 0 Ohm	
12/17	P.31		C905~C907 change from 0.1u to 33P	
12/17	P.31		U19 change from mount to @ ; U18 change from @ to mount	
12/17	P.32		D22 change from mount to @	
12/18	P.24		SATA re-driver IC reserved	
12/22	P.8		Add c124,c128,c151,c155,c55,c119,c113,c197 0.1uF	EMI request
12/22	P.30		Add c40 c41 100P	EMI request
12/22	P.30		Add c42,c43,c45	EMI request
12/22	P.37~p.45		upgrade PWR schematic	
12/22	P.30		Add C65 22uF for CRT flicker	
12/23	P.21		Delete R174,R175	
01/16	P.16		Add r611,r612 connect to INVT_PWM	Vari-Bright reserved
01/16	P.11		Add r347 connect to BKOFF#	Vari-Bright reserved
01/16	P.30		add r288 BKOFF# 4.7k pull low	

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