MOLOKAI Block Diagram

SPR.01.2004

Project Code:91.43E01.001

03249-SC

DC/DC IMVP4 Switching Power ISL6218 32	
INPUTS	OUTPUT
DCBATOUT	VCC_CORE

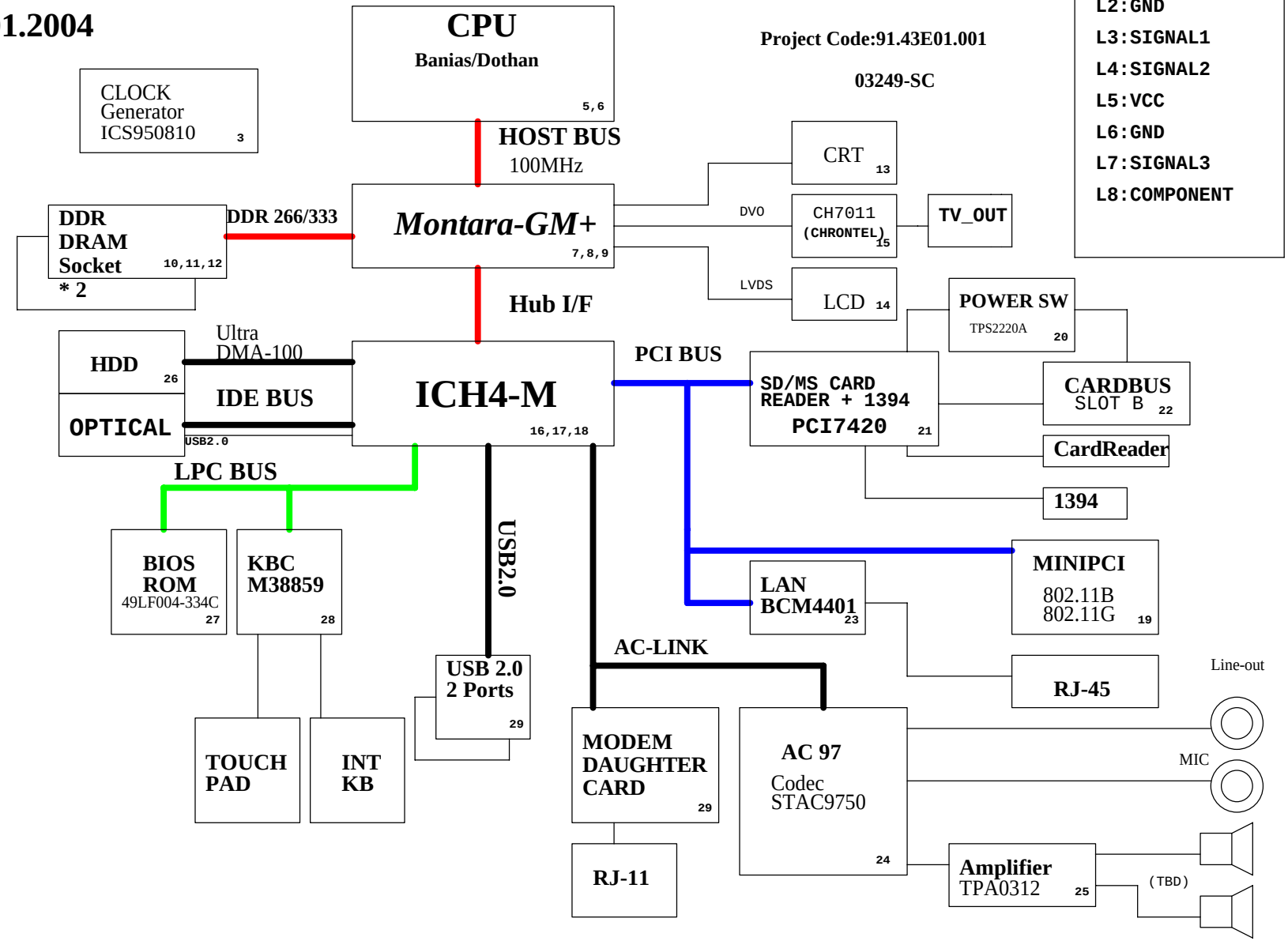
SYSTEM DC/DC MAX1715 34	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S0 2D5V_S3

DC/DC&CHARGER MAX1645 35	
INPUTS	OUTPUTS
AD+	BT+

DC/DC MAX1999 33	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

G913C/APL1085 APL5331kAC/G1211X 38	
INPUTS	OUTPUTS
3D3V_S0	1D8V_VCCA_S0
3D3V_S5	1D5V_S5
3D3V_S0	1D5V_S0
2D5V_S3	1D25V_S0
1D35V_S0	VCC_IO_S0

PCB LAYER
L1:COMPONENT
L2:GND
L3:SIGNAL1
L4:SIGNAL2
L5:VCC
L6:GND
L7:SIGNAL3
L8:COMPONENT



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Title		
BLOCK DIAGRAM		
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S5

5V_S5 — 5V_S5 18,33,34,36
3D3V_S5 — 3D3V_S5 4,16,17,18,28,30,31,33,36,38,39
1D5V_S5 — 1D5V_S5 18,38
VCC_RTC_S5 — VCC_RTC_S5 17

S3

3D3V_S3 — 3D3V_S3 14,25,28,30,34,36,39
2D5V_S3 — 2D5V_S3 7,9,10,11,34,38,39
1D25V_DDRVREF_S3 — 1D25V_DDRVREF_S3 7,10,34

S0

5V_S0 — 5V_S0 13,14,17,18,19,20,24,26,28,30,32,34,36,38,39
3D3V_S0 — 3D3V_S0 3,7,8,9,10,13,14,15,16,17,18,19,20,21,22,24,25,26,27,29,30,31,32,36,38,39

1D5V_S0 — 1D5V_S0 7,8,9,15,16,18,27,38,39
1D25V_S0 — 1D25V_S0 11,12,38
1D35V_S0 — 1D35V_S0 7,9,34,38,39
VCC_CORE_S0 — VCC_CORE_S0 6,32,39
VCC_IO_S0 — VCC_IO_S0 4,5,6,7,9,17,18,32,38,39
1D8V_VCCA_S0 — 1D8V_VCCA_S0 5,38

AC-IN / BAT.-IN

AD+ — AD+ 35,37,39
DCBATOUT — DCBATOUT 14,32,33,34,35,36,38,39

LAN-AC

3D3V_LAN_S5AC — 3D3V_LAN_S5AC 23,29,36,37

5VA_AUD_S3 — 5VA_AUD_S3 24 → **AUDIO**

3D3V_LCD_S0 — 3D3V_LCD_S0 14 → **LCD**

CRT_VCC_S0 — CRT_VCC_S0 13 → **CRT**

TV3D3V1_S0 — TV3D3V1_S0 15
TV3D3VA_S0 — TV3D3VA_S0 15
TV3D3V2_S0 — TV3D3V2_S0 15
TV1D5V_S0 — TV1D5V_S0 15
→ **TV-OUT**

OTHERS

5V_AUX — 5V_AUX 30,31,33,35,37,38,39
3D3V_AUX — 3D3V_AUX 14,17,33

3D3V_RTC — 3D3V_RTC 17,28
ICH_VBIAS — ICH_VBIAS 17
MAX1999_REF — MAX1999_REF 33,38

MAX1999_VCC — MAX1999_VCC 33

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
SD/MS CARD READER+1394 PCI7420	AD20	PIRQB# PIRQC# PIRQF#	REQ#1 / GNT#1
MINI PCI 802.11B/G	AD17	PIRQE# PIRQG#	REQ#0 / GNT#0
LAN BCM4401	AD21	PIRQD#	REQ#4 / GNT#4

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Title: *Table of Content*
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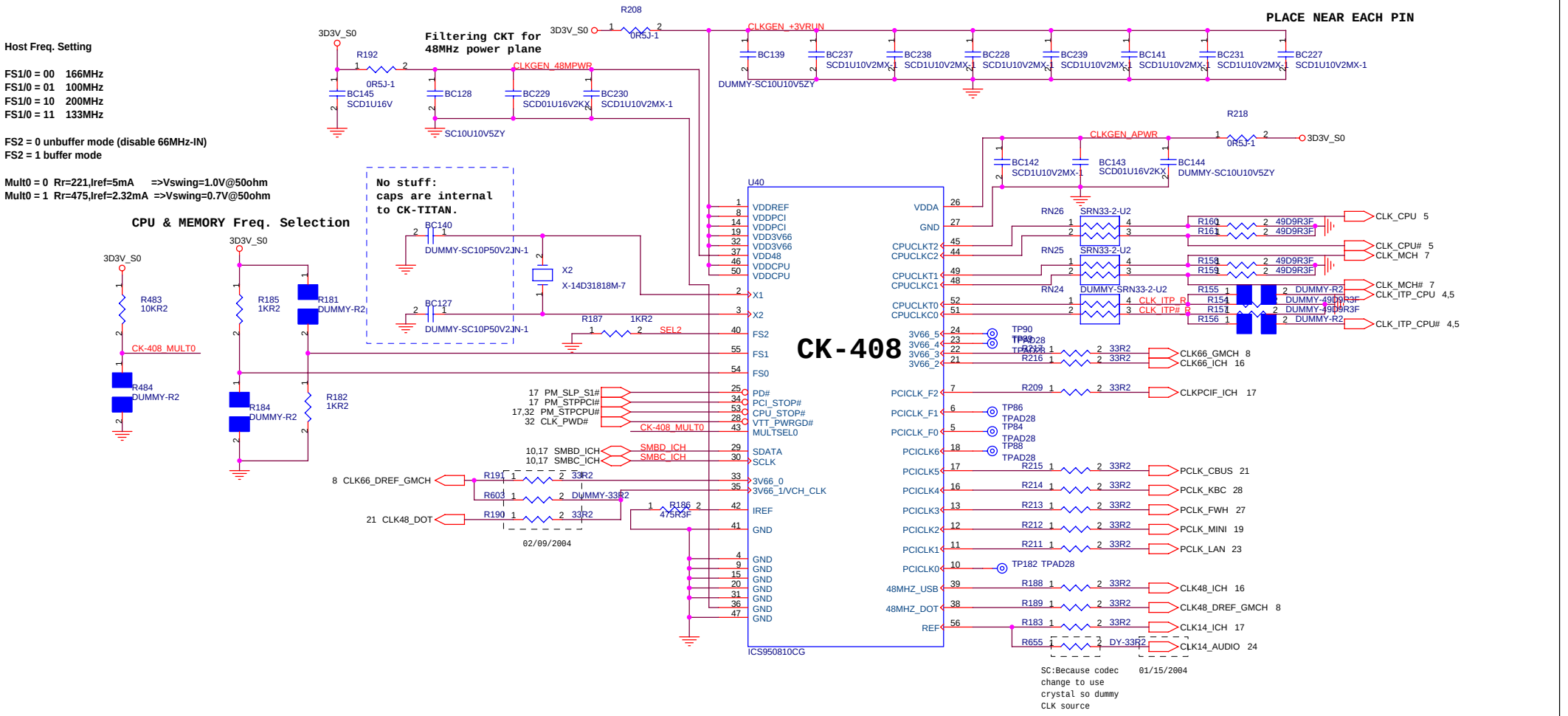

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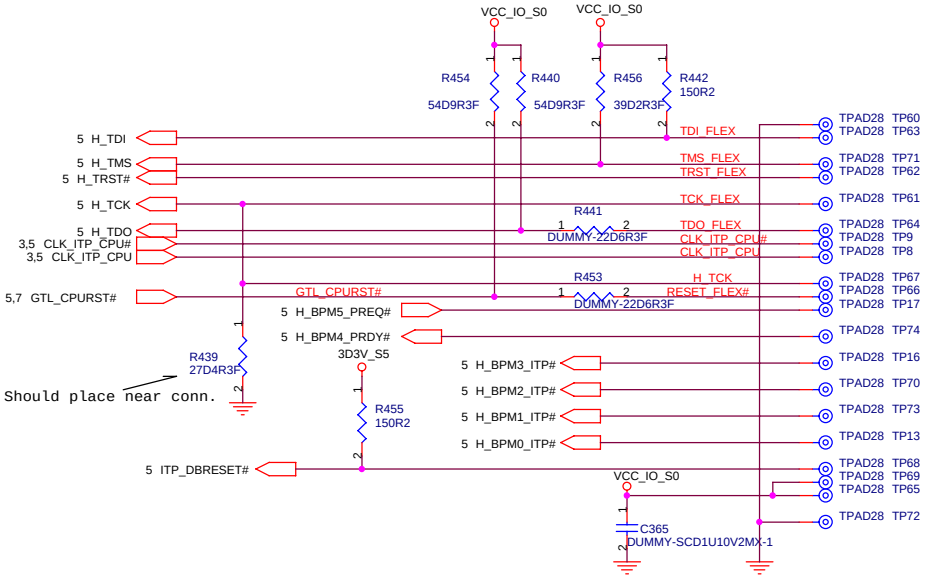
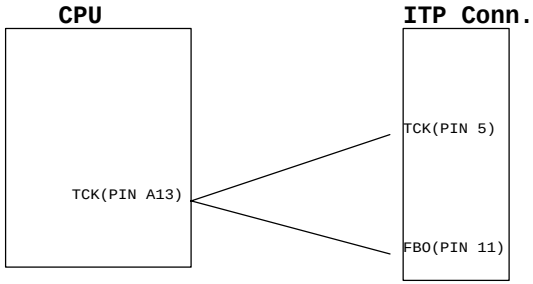
ITP Debug Pad





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Title: ITP		
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CPU VCCA POWER:

At Dothan CPU application, POWER is 1.5V or 1.8V.

For CPU VCCA[0:3] PLL place one 0.01u & 10u for each VCCA pin

1D8V_VCCA_S0

BC87 DY-SC10U6D3V5MX
BC75 SC10U6D3V5MX
BC108 DY-SC10U6D3V5MX
BC104 DY-SC10U6D3V5MX
BC106 SCD01U16V2KX
BC105 SCD01U16V2KX
BC86 SCD01U16V2KX
BC90 SCD01U16V2KX

Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
COMP1 and COMP3 should be routed asx Zo=54.9ohm, traces shorter than 0.5".

U68D

3 CLK_CPU → BCLK0 B15
3 CLK_CPU# → BCLK1 B14
3,4 CLK_ITP_CPU → ITP_CLK0 A16
3,4 CLK_ITP_CPU# → ITP_CLK1 A15

17 CC_A20M# → A20M# C2
17 CC_FERR# → CC_FERR# → FERR# D3
17 CC_IGNNE# → IGNNE# A3

17 CC_INTR → LINT0 D1
17 CC_NMI → LINT1 D4

17 CC_SMI# → SMI# B4
17 CC_STPCLK# → STPCLK# C6

1D8V_VCCA_S0 → VCCA3 AC26 **120mA**
VCCA2 N1
VCCA1 B1
VCCA0 F26

RSVD B2, AF7, C14, C3, C16, E1

TP20 TPAD28
TP10 TPAD28
TPAD28
TPAD28
TP19 TPAD28

VCC_IO_S0
R113 DUMMY-1KR2
R116 150R2
H_TDI
17 CC_CPUSLP# → 4 H_TCK → H_TCK → TCK A13 → SLP# A6
4 H_TDI → H_TDI → TDI C12
4 H_TDO → H_TDO → TDO A12

TP12 TPAD28
TP13 TPAD28
VCCSENSE AE7
VSSSENSE AF6

32 H_VID[5:0]
H_VID5 → VID5 H4
H_VID4 → VID4 G4
H_VID3 → VID3 G3
H_VID2 → VID2 F3
H_VID1 → VID1 F2
H_VID0 → VID0 E2
R131 DUMMY-54D9R3F
R132 DUMMY-54D9R3F

BPM3# C9 H_BPM3_ITP# → H_BPM3_ITP# 4
BPM2# A9 H_BPM2_ITP# → H_BPM2_ITP# 4
BPM1# B8 H_BPM1_ITP# → H_BPM1_ITP# 4
BPM0# C8 H_BPM0_ITP# → H_BPM0_ITP# 4

COMP3 AB1 27D4-3 R135 54D9R3F
COMP2 AB2 27D4-1 R136 27D4R3F
COMP1 P26 27D4-4 R110 54D9R3F
COMP0 P25 27D4-2 R109 27D4R3F

DPSLP# B7 → CC_DPSLP# 7,17

GTLREF3 AC1
GTLREF2 G1
GTLREF1 E26
GTLREF0 AD26

VCC_IO_S0
R108 1KR2F
H_GTLREF_0 → 2/3 RATIO
R107 2KR3F
C134 DUMMY-SCD1U16V

SC: Change to 1KR2F for GTLREF pass

Voltage divider placed within 0.5" of CPU pin via a Zo=55ohm trace.

PROCHOT# B17 → CC_PROCHOT#
PWRGOOD E4 → CC_CPUPWRGD → CC_CPUPWRGD 7,17

THERMDP1 30
C165 SC1000P50V
THERMDN 30
PM_THERMTRIP# 17

TEST1 C5 TEST1 → TP6 TPAD28
TEST2 F23 TEST2 → TP15 TPAD28
THERMDA B18
THERMDC A18
THERMTRIP# C17
TMS C11 H_TMS → H_TMS 4
TRST# B13 → H_TRST# 4
R115 680R2

VCC_IO_S0
GTL_IERR# → R450 56R2J
CC_CPUPWRGD → R133 330R2
CC_PROCHOT# → R114 56R2J

7 GTL_D#[15..0]
GTL_D#15 C25 D15#
GTL_D#14 E23 D14#
GTL_D#13 B23 D13#
GTL_D#12 C26 D12#
GTL_D#11 E24 D11#
GTL_D#10 D24 D10#
GTL_D#9 B24 D9#
GTL_D#8 C20 D8#
GTL_D#7 B20 D7#
GTL_D#6 A21 D6#
GTL_D#5 B26 D5#
GTL_D#4 A24 D4#
GTL_D#3 B21 D3#
GTL_D#2 A22 D2#
GTL_D#1 A25 D1#
GTL_D#0 A19 D0#

U68C

D47# Y25 GTL_D#47
D46# AA26 GTL_D#46
D45# Y23 GTL_D#45
D44# V26 GTL_D#44
D43# U25 GTL_D#43
D42# V24 GTL_D#42
D41# U26 GTL_D#41
D40# AA23 GTL_D#40
D39# R23 GTL_D#39
D38# R26 GTL_D#38
D37# R24 GTL_D#37
D36# V23 GTL_D#36
D35# U23 GTL_D#35
D34# T25 GTL_D#34
D33# AA24 GTL_D#33
D32# Y26 GTL_D#32
GTL_D#[47..32] 7

7 GTL_DINV#0 → D25 DINV0#
7 GTL_DSTBN#0 → C23 DSTBN0#
7 GTL_DSTBP#0 → C22 DSTBP0#

DINV2# T24 → GTL_DINV#2 7
DSTBN2# W25 → GTL_DSTBN#2 7
DSTBP2# W24 → GTL_DSTBP#2 7

7 GTL_D#[31..16]
GTL_D#31 K25 D31#
GTL_D#30 N25 D30#
GTL_D#29 H26 D29#
GTL_D#28 M25 D28#
GTL_D#27 N24 D27#
GTL_D#26 L26 D26#
GTL_D#25 J25 D25#
GTL_D#24 M23 D24#
GTL_D#23 J23 D23#
GTL_D#22 G24 D22#
GTL_D#21 F25 D21#
GTL_D#20 H24 D20#
GTL_D#19 M26 D19#
GTL_D#18 L23 D18#
GTL_D#17 G25 D17#
GTL_D#16 H23 D16#

D63# AF26 GTL_D#63
D62# AF22 GTL_D#62
D61# AF25 GTL_D#61
D60# AD21 GTL_D#60
D59# AE21 GTL_D#59
D58# AF20 GTL_D#58
D57# AD24 GTL_D#57
D56# AF23 GTL_D#56
D55# AE22 GTL_D#55
D54# AD23 GTL_D#54
D53# AC25 GTL_D#53
D52# AC22 GTL_D#52
D51# AC20 GTL_D#51
D50# AB24 GTL_D#50
D49# AC23 GTL_D#49
D48# AB25 GTL_D#48
GTL_D#[63..48] 7

7 GTL_DINV#1 → J26 DINV1#
7 GTL_DSTBN#1 → K24 DSTBN1#
7 GTL_DSTBP#1 → L24 DSTBP1#

DINV3# AD20 → GTL_DINV#3 7
DSTBN3# AE24 → GTL_DSTBN#3 7
DSTBP3# AE25 → GTL_DSTBP#3 7

BGA479-SKT-2-U

U68B

7 GTL_A#[16..3]
GTL_A#16 AA2 A16#
GTL_A#15 Y3 A15#
GTL_A#14 AA3 A14#
GTL_A#13 U1 A13#
GTL_A#12 Y1 A12#
GTL_A#11 Y4 A11#
GTL_A#10 W2 A10#
GTL_A#9 T4 A9#
GTL_A#8 W1 A8#
GTL_A#7 V2 A7#
GTL_A#6 R3 A6#
GTL_A#5 V3 A5#
GTL_A#4 U4 A4#
GTL_A#3 P4 A3#

7 GTL_ADSTB#0 → U3 ADSTB0#

7 GTL_A#[31..17]
GTL_A#31 AF1 A31#
GTL_A#30 AE1 A30#
GTL_A#29 AF3 A29#
GTL_A#28 AD6 A28#
GTL_A#27 AE2 A27#
GTL_A#26 AD5 A26#
GTL_A#25 AC6 A25#
GTL_A#24 AB4 A24#
GTL_A#23 AD2 A23#
GTL_A#22 AE4 A22#
GTL_A#21 AD3 A21#
GTL_A#20 AC3 A20#
GTL_A#19 AC7 A19#
GTL_A#18 AC4 A18#
GTL_A#17 AF4 A17#

7 GTL_ADSTB#1 → AE5 ADSTB1#

BGA479-SKT-2-U

TP18 TPAD28

ADS# N2 → GTL_ADS# 7
BNR# L1 → GTL_BNR# 7
BPRI# J3 → GTL_BPRI# 7
BR0# N4 → GTL_BR0# 7
DBR# A7 → ITP_DBRESET# 4
DBSY# M2 → GTL_DBSY# 7
DEFER# L4 → GTL_DEFER# 7
DRDY# H2 → GTL_DRDY# 7
HIT# K3 → GTL_HIT# 7
HITM# K4 → GTL_HITM# 7
IERR# A4 → GTL_IERR#
INIT# B5 → CC_INIT# 17,27
LOCK# J2 → GTL_LOCK# 7
PRDY# A10 → H_BPM4_PRDY# 4
PREQ# B10 → H_BPM5_PREQ# 4
RESET# B11 → GTL_CPURST# 4,7

TRDY# M3 → GTL_TRDY# 7

RS2# L2 → GTL_RS#2 7
RS1# K1 → GTL_RS#1 7
RS0# H1 → GTL_RS#0 7

DPWR# C19 → GTL_DPWR# 7

REQ4# T1 → GTL_REQ#4
REQ3# P1 → GTL_REQ#3
REQ2# T2 → GTL_REQ#2
REQ1# P3 → GTL_REQ#1
REQ0# R2 → GTL_REQ#0
GTL_REQ#[0..4] 7

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Title: **Banias CPU (1 of 2)**

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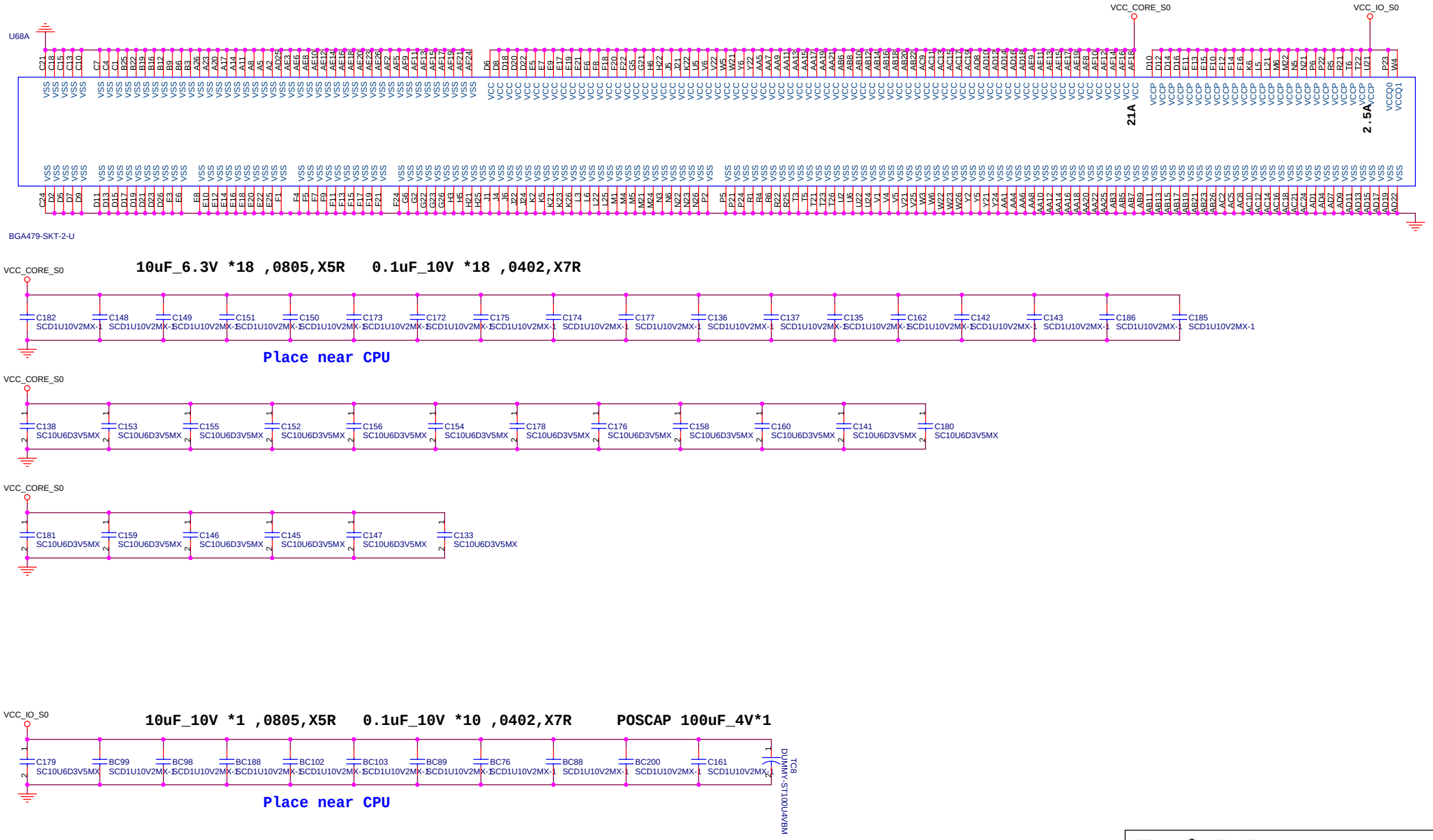

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Title: *Banias CPU (2 of 2)*		
Size: A3	Document Number: *MOLOKAI*	Rev: *SC*
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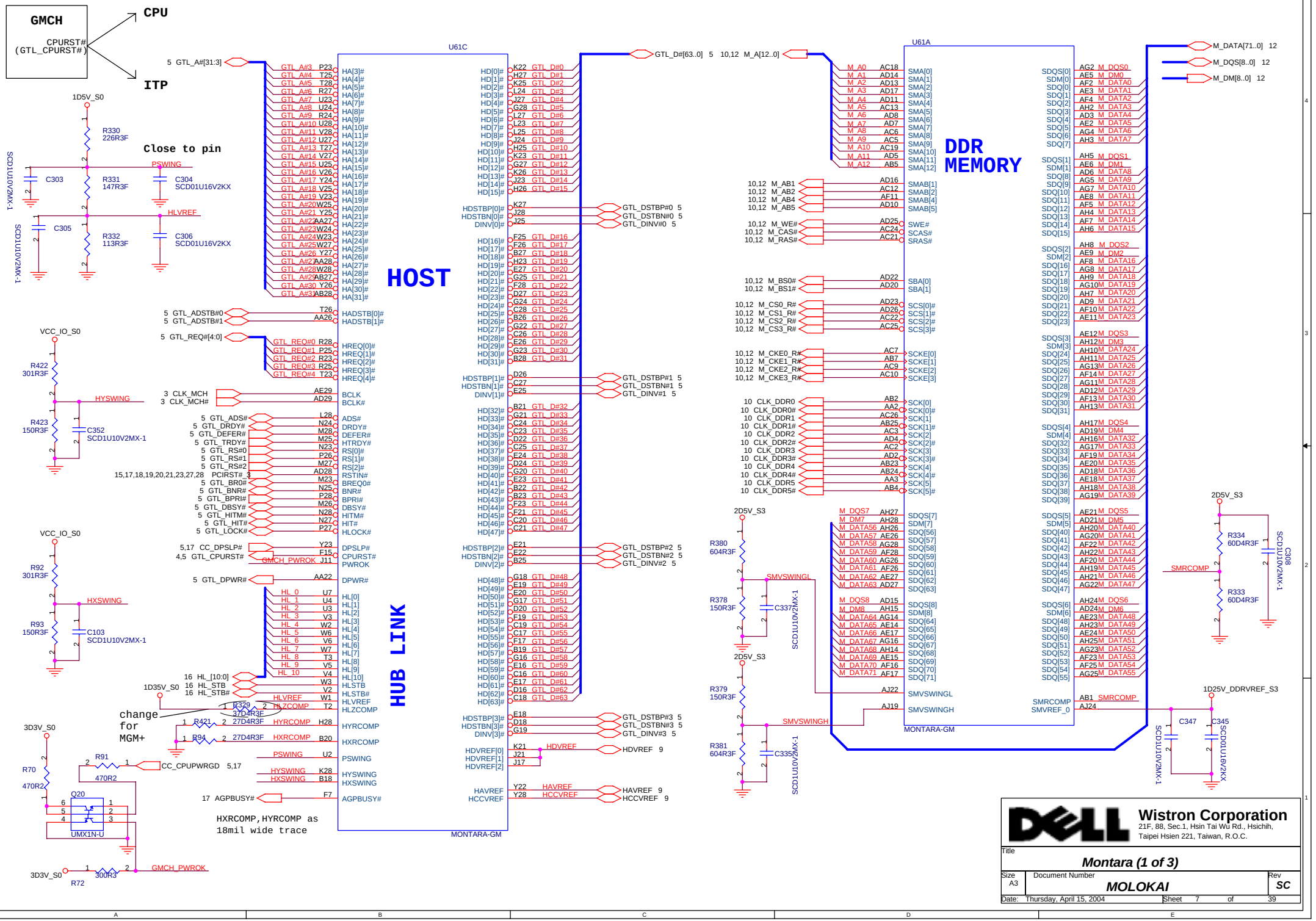
GMCH
CPURST#
(GTL_CPURST#)
CPU
ITP
HOST
HUB LINK
U61C
MONTARA-GM
U61A
DDR MEMORY
MONTARA-GM
Close to pin
change for MGM+
HXRCOMP,HYRCOMP as 18mil wide trace
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Montara (1 of 3)
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FOR MGM+ internal pull down

GST[2:0]	FSB	DDR	Gfx Core Clock Low	Gfx Core Clock High
000	400	266	133	200
001	400	200	100	200
010	400	200	100	133
111	400	333	166	250

DEFAULT NOT USE TV ENCODER

IF USE TV ENCODER ADD R63 ,REMOVE R76 AND R66

change for MGM+

short trace

DDR Feedback(inside the package) Route transitioned to buttom side with vias near ball

SB: for SIV pass

SB:03/03/2004

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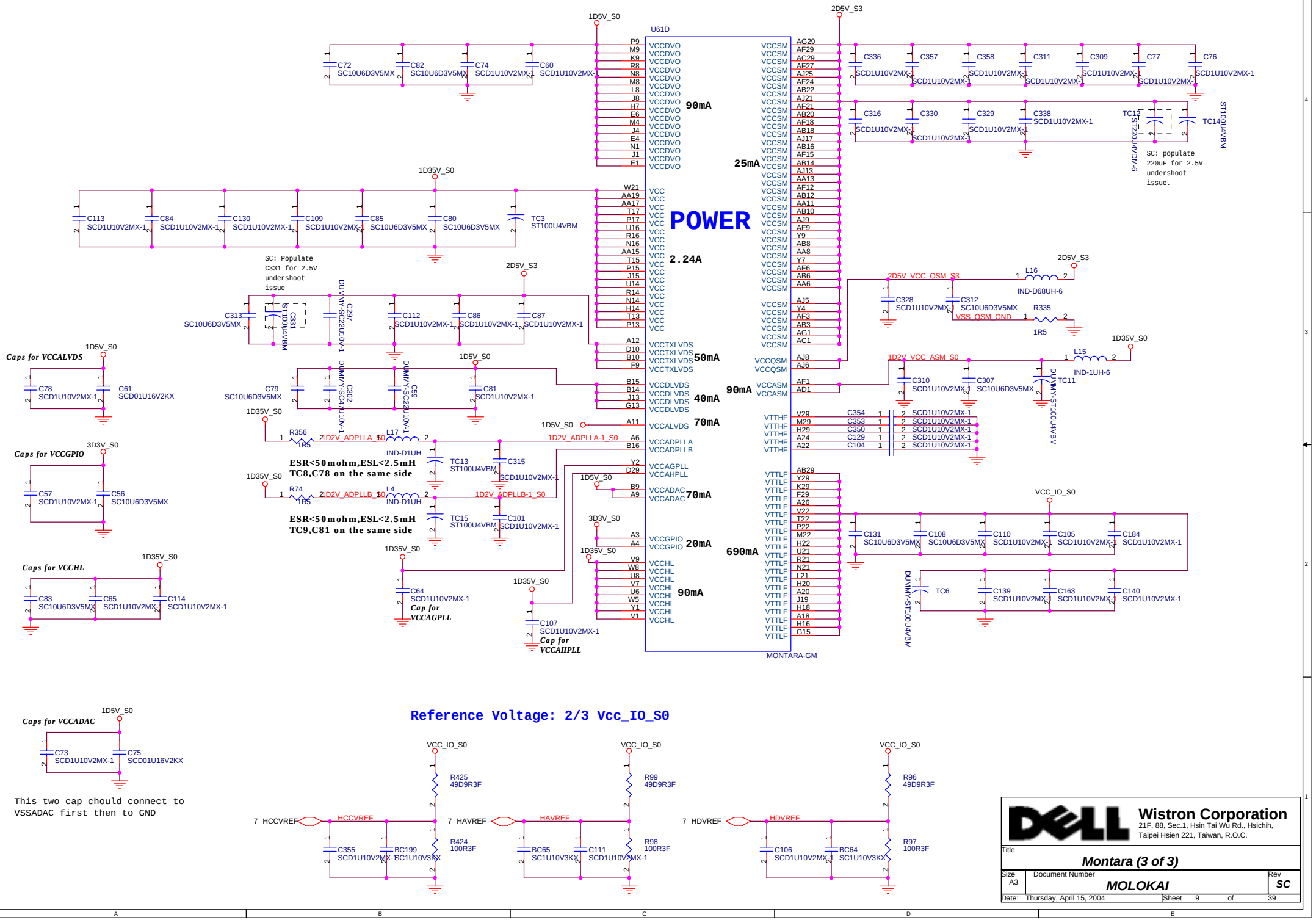
U61D
POWER
MONTARA-GM
1D5V_S0
2D5V_S3
1D35V_S0
3D3V_S0
90mA
25mA
2.24A
50mA
40mA
70mA
20mA
690mA
Caps for VCCALVDS
Caps for VCCGPIO
Caps for VCCHL
Caps for VCCADAC
ESR<50mohm,ESL<2.5mH
TC8,C78 on the same side
ESR<50mohm,ESL<2.5mH
TC9,C81 on the same side
Cap for
VCCAGPLL
Cap for
VCCAHPLL
SC: Populate
C331 for 2.5V
undershoot
issue
SC: populate
220uF for 2.5V
undershoot
issue.
This two cap chould connect to
VSSADAC first then to GND
Reference Voltage: 2/3 Vcc_IO_S0
VCC_IO_S0
HCCVREF
HAVREF
HDVREF
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DIMM1

DM1

REVERSE TYPE

Top Side

SKTSODIMM200-1U1
62.10017.311

DIMM2

Use old symbol change PN only

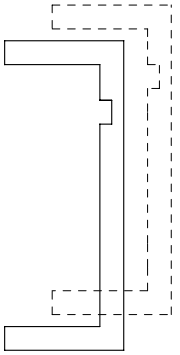
DM2

NORMAL TYPE

BOT side

SKT-SODIMM200-7U
62.10024.481

(Normal Type)
DIMM 2(BOT side)



Montara-GM+
(BOT side)

(REVERSE TYPE)
DIMM 1(Top side)

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Title: DDR Socket

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Title: ***DDR Decoupling CPA***

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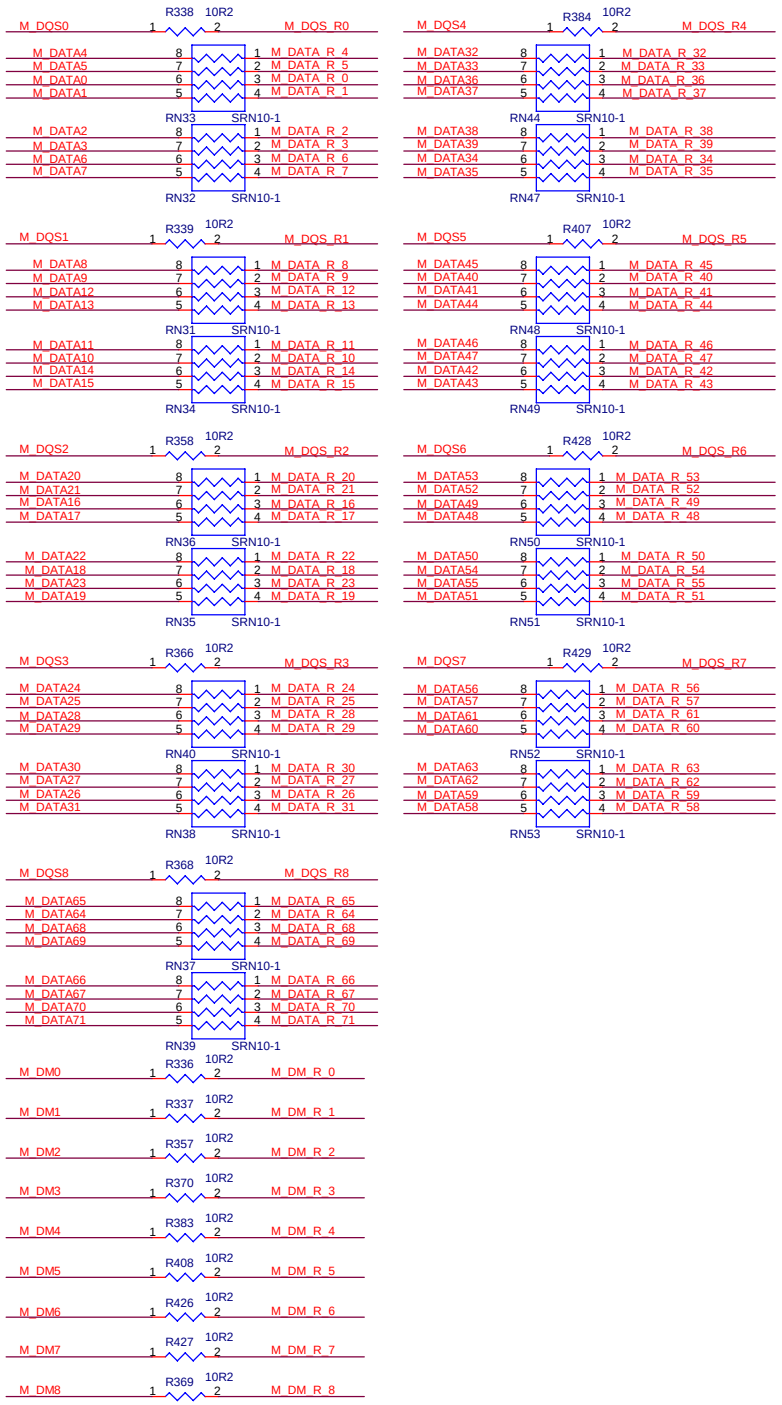
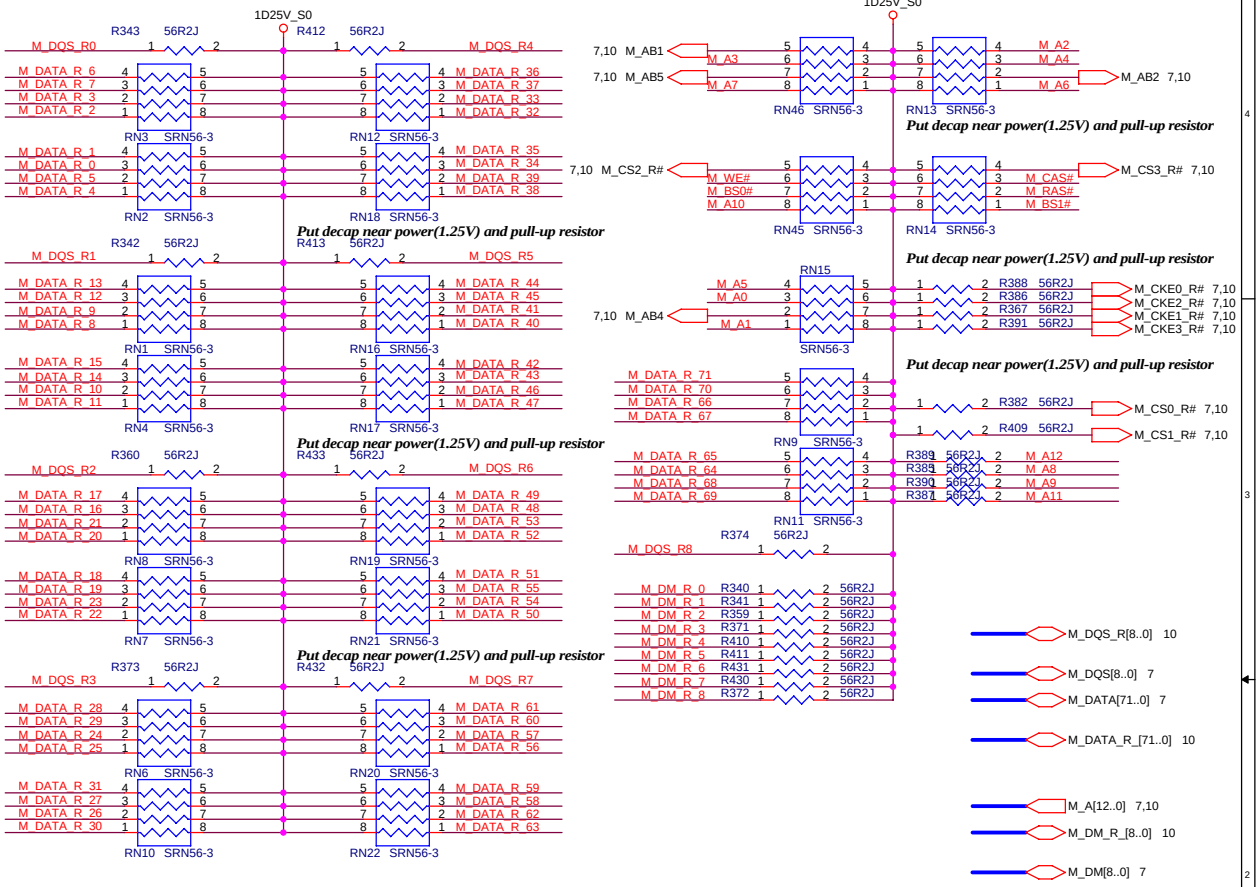
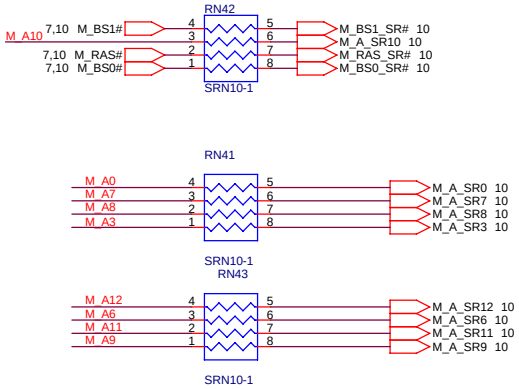
SERIES DAMPING



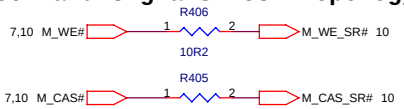
PARALLEL TERMINATION

Put decap near power(1.25V) and pull-up resistor





Command Signals USE Topology 2



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Title: ***DDR Serial/Terminator Resistor***

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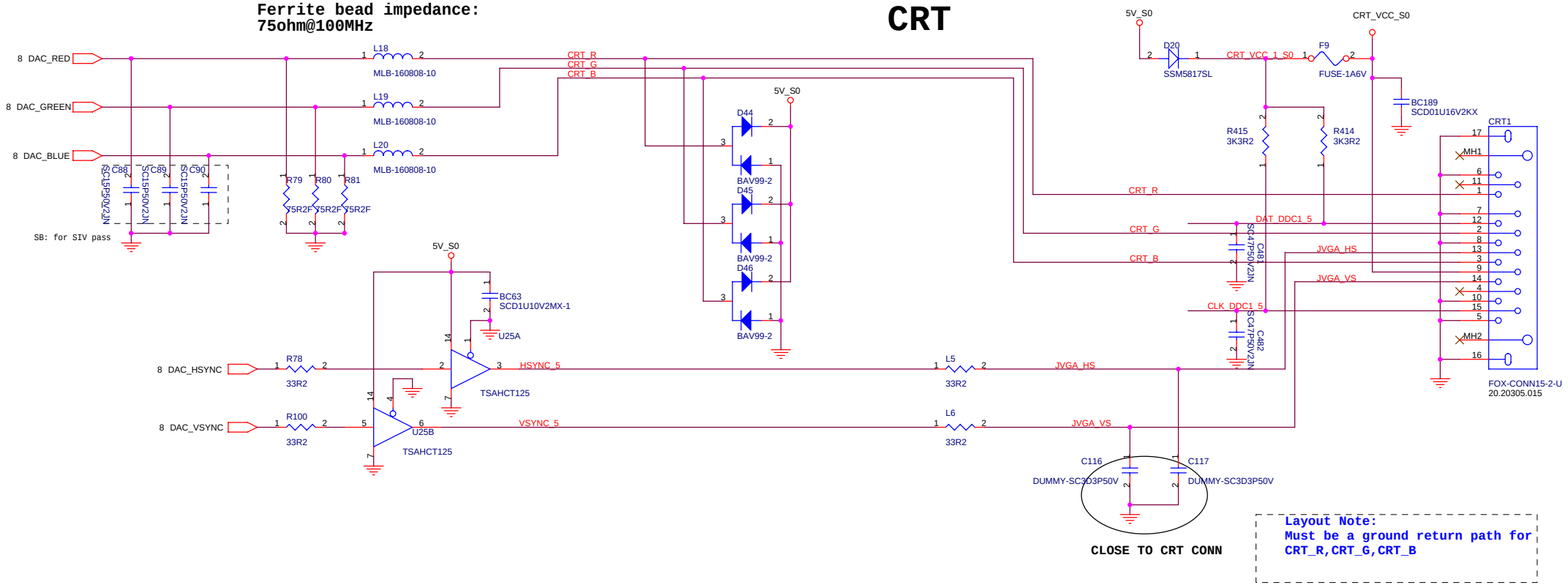
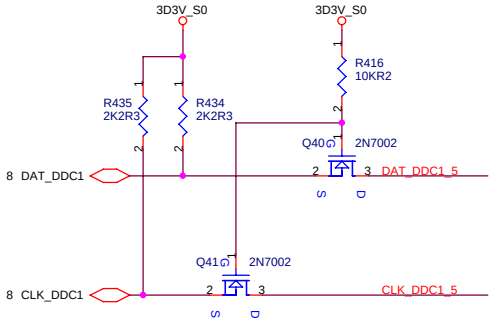
CRT

Ferrite bead impedance:
75ohm@100MHz



Layout Note:
Must be a ground return path for CRT_R,CRT_G,CRT_B

DDC_CLK & DATE LEVEL SHIFT



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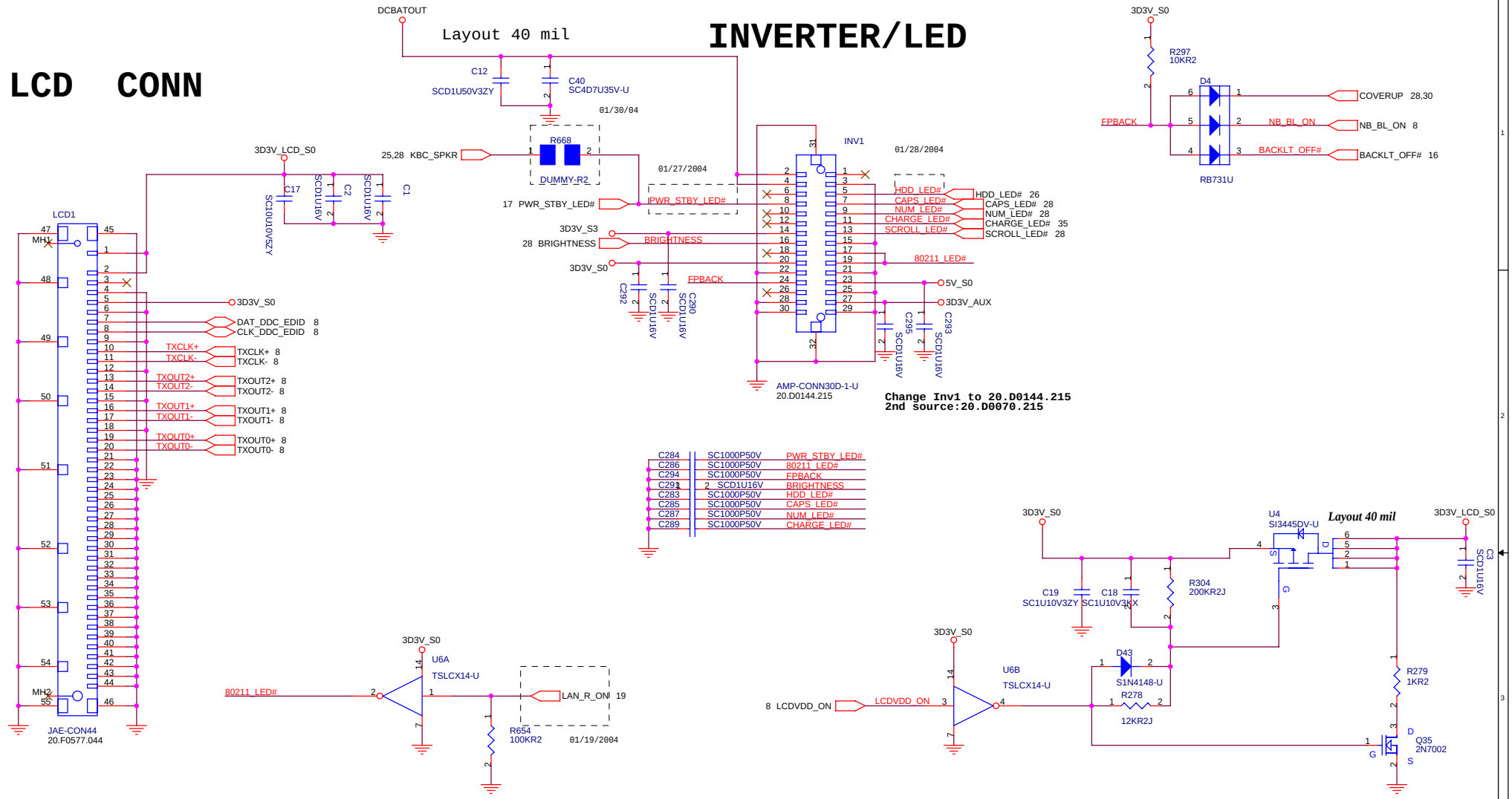
Title: *CRT CONN.*		
Size: A3	Document Number: *MOLOKAI*	Rev: *SC*
Date: Thursday, April 15, 2004	Sheet 13 of 39	

LCD CONN

INVERTER/LED



	S0/S1	S3	S4	S5	Functions	when LID is closed
Power On / Battery Low LED (PWR_LED#)	LOW	HIGH	HIGH	HIGH		readable
Sleep / Waking LED (STDBY_LED#)	HIGH	LOW	HIGH	HIGH	(Don't flash during waking)	readable
Disk Media (MEDIA_LED#)					HDD,ODD access indicator	not readable
Charging LED (CHARGE_LED#)					On when charging. Flashing when charging error is occured.	not readable
Wireless LED (80211_LED#)					On when wireless is On	not readable
NUM Lock (NUM_LED#)					On when Number key is locked	not readable
CAPS Lock (MEDIA_LED#)					On when Caps lock is On	not readable

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Title: LCD CONN & INVERTER

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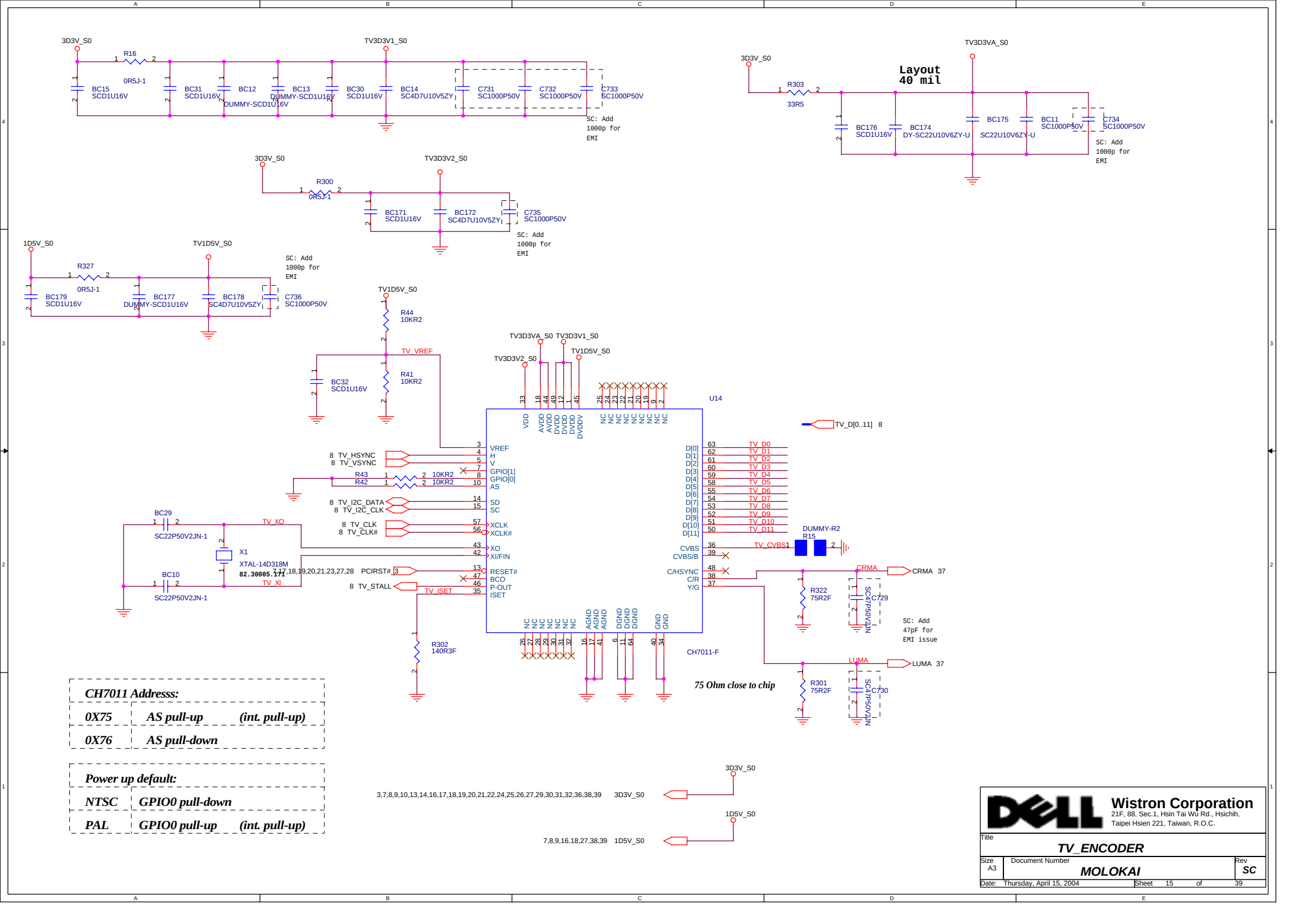
3D3V_S0
R16
0R5J-1
BC15 SCD1U16V
BC31 SCD1U16V
BC12 DUMMY-SCD1U16V
BC13 DUMMY-SCD1U16V
BC30 SCD1U16V
TV3D3V1_S0
BC14 SC4D7U10V5ZY
C731 SC1000P50V
C732 SC1000P50V
C733 SC1000P50V
SC: Add 1000p for EMI
TV3D3VA_S0
Layout 40 mil
R303
33R5
BC176 SCD1U16V
BC174 DY-SC22U10V6ZY-U
BC175 SC22U10V6ZY-U
BC11 SC1000P50V
C734 SC1000P50V
SC: Add 1000p for EMI
TV3D3V2_S0
R300
0R5J-1
BC171 SCD1U16V
BC172 SC4D7U10V5ZY
C735 SC1000P50V
SC: Add 1000p for EMI
1D5V_S0
TV1D5V_S0
R327
0R5J-1
BC179 SCD1U16V
BC177 DUMMY-SCD1U16V
BC178 SC4D7U10V5ZY
C736 SC1000P50V
SC: Add 1000p for EMI
R44 10KR2
TV_VREF
R41 10KR2
BC32 SCD1U16V
U14
VDD AVDD AVDD DVDD DVDD DVDD DVDDV
NC NC NC NC NC NC NC NC NC
VREF
H
V
GPIO[1]
GPIO[0]
AS
SD
SC
XCLK
XCLK#
XO
XI/FIN
RESET#
BCO
P-OUT
ISET
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7] D[8] D[9] D[10] D[11]
TV_D0 TV_D1 TV_D2 TV_D3 TV_D4 TV_D5 TV_D6 TV_D7 TV_D8 TV_D9 TV_D10 TV_D11
CVBS CVBS/B
C/HSYNC C/R Y/G
TV_D[0..11] 8
8 TV_HSYNC
8 TV_VSYNC
R43 10KR2
R42 10KR2
8 TV_I2C_DATA
8 TV_I2C_CLK
8 TV_CLK
8 TV_CLK#
8 TV_STALL
PCIRST# 3
TV_ISET
R302 140R3F
BC29 SC22P50V2JN-1
BC10 SC22P50V2JN-1
TV_XO
TV_XI
X1
XTAL-14D318M
82.30005.211
7,17,18,19,20,21,23,27,28
DUMMY-R2
R15
TV_CVBS1
CRMA
CRMA 37
R322 75R2F
C729 SC47P50V2JN
SC: Add 47pF for EMI issue
LUMA
LUMA 37
R301 75R2F
C730 SC47P50V2JN
CH7011-F
75 Ohm close to chip
CH7011 Addresss:
0X75 AS pull-up (int. pull-up)
0X76 AS pull-down
Power up default:
NTSC GPIO0 pull-down
PAL GPIO0 pull-up (int. pull-up)
3,7,8,9,10,13,14,16,17,18,19,20,21,22,24,25,26,27,29,30,31,32,36,38,39 3D3V_S0
7,8,9,16,18,27,38,39 1D5V_S0
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Title
TV_ENCODER
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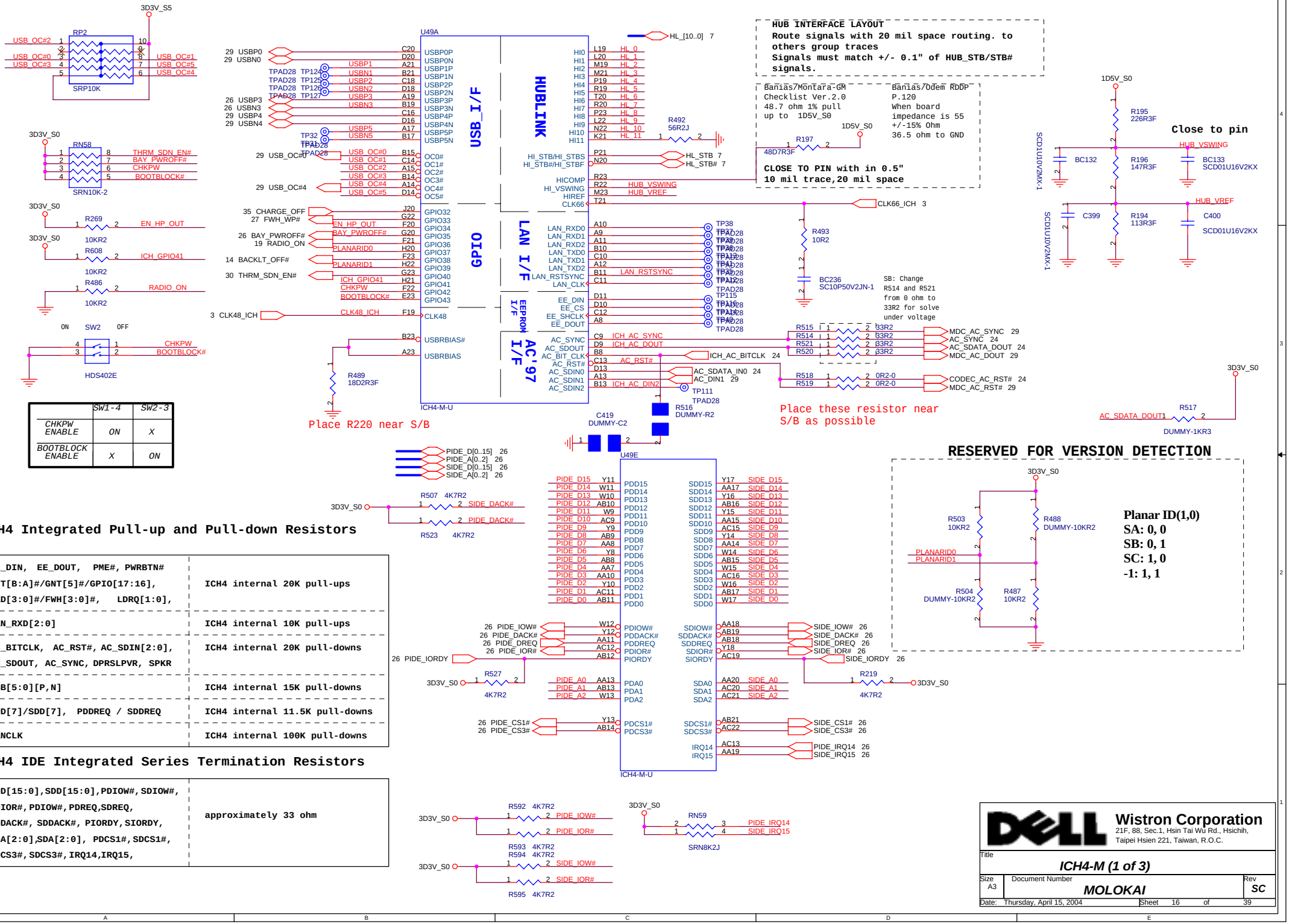
HUB INTERFACE LAYOUT
Route signals with 20 mil space routing. to others group traces
Signals must match +/- 0.1" of HUB_STB/STB# signals.
Banias/Montara-GM Checklist Ver.2.0 48.7 ohm 1% pull up to 1D5V_S0
Banias/Odem RDDP P.120 When board impedance is 55 +/-15% Ohm 36.5 ohm to GND
CLOSE TO PIN with in 0.5" 10 mil trace,20 mil space
Close to pin
SB: Change R514 and R521 from 0 ohm to 33R2 for solve under voltage
Place R220 near S/B
Place these resistor near S/B as possible
RESERVED FOR VERSION DETECTION
Planar ID(1,0)
SA: 0, 0
SB: 0, 1
SC: 1, 0
-1: 1, 1
ICH4 Integrated Pull-up and Pull-down Resistors
EE_DIN, EE_DOUT, PME#, PWRBTN#
GNT[B:A]#/GNT[5]#/GPIO[17:16],
LAD[3:0]#/FWH[3:0]#, LDRQ[1:0],
ICH4 internal 20K pull-ups
LAN_RXD[2:0]
ICH4 internal 10K pull-ups
AC_BITCLK, AC_RST#, AC_SDIN[2:0],
AC_SDOUT, AC_SYNC, DPRSLPVR, SPKR
ICH4 internal 20K pull-downs
USB[5:0][P,N]
ICH4 internal 15K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ
ICH4 internal 11.5K pull-downs
LANCLK
ICH4 internal 100K pull-downs
ICH4 IDE Integrated Series Termination Resistors
PDD[15:0],SDD[15:0],PDIOW#,SDIOW#,
PDIOR#,PDIOW#,PDREQ,SDREQ,
PDDACK#, SDDACK#, PIORDY,SIORDY,
PDA[2:0],SDA[2:0], PDCS1#,SDCS1#,
PDCS3#,SDCS3#,IRQ14,IRQ15,
approximately 33 ohm
SW1-4
SW2-3
CHKPW ENABLE
ON
X
BOOTBLOCK ENABLE
X
ON
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Title
ICH4-M (1 of 3)
Size A3
Document Number
MOLOKAI
Rev SC
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PCI/Interrupt I/F Pullups

3D3V_S0

RN65: PCI_STOP# PCI_TRDY# PCI_FRAME# PCI_SERR# — SRN8K2-U
RN66: PCI_PLOCK# PCI_DEVSEL# PCI_PERR# PCI_IRDY# — SRN8K2-U

RN62: PCI_REQA# PIRQF# PIRQC# PIRQD# — SRN8K2-U
RN63: PIRQA# PCI_REQ#0 PCI_REQ#1 PCI_REQ#2 — SRN8K2-U

RN64: PCIRST#_3 PIRQG# PCI_SERIRQ PIRQB# — SRN8K2-U
RN60: PIRQE# PCI_REQB# PCI_REQ#3 PCI_REQ#4 — SRN8K2-U

PCI_AD[31..0] 19,21,23
PCI_C/BE#[3..0] 19,21,23

U49D

21 PIRQB#	PIRQA#	D5	PIRQA#
21 PIRQC#		C2	PIRQB#
23 PIRQD#		B4	PIRQC#
19 PIRQE#		A3	PIRQD#
21 PIRQF#		C8	PIRQE#/GPIO2
19 PIRQG#		D7	PIRQF#/GPIO3
	ICH_GPIO5	C3	PIRQG#/GPIO4
		C4	PIRQH#/GPIO5
23 PCI_REQ#4		B6	REQ4#
	PCI_REQ#3	C7	REQ3#
	PCI_REQ#2	B3	REQ2#
		A2	REQ1#
21 PCI_REQ#1		B1	REQ0#
19 PCI_REQ#0		A6	REQB#/REQ5#/GPIO1
	PCI_REQB#	B5	REQA#/GPIO0
	PCI_REQA#	D6	GNT4#
23 PCI_GNT#4		B7	GNT3#
TPAD28 TP110	PCI_GNT#3	A7	GNT2#
TPAD28 TP109	PCI_GNT#2	E6	GNT1#
21 PCI_GNT#1		C1	GNT0#
19 PCI_GNT#0		C5	GNTB#/GNT5#/GPIO17
	PCI_GNTB#	E8	GNTA#/GPIO16
	PCI_GNTA#	F1	FRAME#
19,21,23 PCI_FRAME#		L5	IRDY#
19,21,23 PCI_IRDY#		F2	TRDY#
19,21,23 PCI_TRDY#		M3	DEVSEL#
19,21,23 PCI_DEVSEL#		F3	STOP#
19,21,23 PCI_STOP#		G1	PAR
19,21,23 PCI_PAR		L4	PERR#
19,21,23 PCI_PERR#	PCI_PLOCK#	M2	PLOCK#
21 PCI_PLOCK#		K5	SERR#
19,21,23 PCI_SERR#	ICH_PME#	W2	PME#
19,21,23 ICH_PME#	CLKPCIF_ICH	U5	PCIRST#
7,15,18,19,20,21,23,27,28 PCIRST#_3		P5	PCICLK
3 CLKPCIF_ICH			

AD31	P4	PCI_AD31	
AD30	D2	PCI_AD30	
AD29	R1	PCI_AD29	
AD28	D3	PCI_AD28	
AD27	P2	PCI_AD27	
AD26	E1	PCI_AD26	
AD25	P1	PCI_AD25	
AD24	E2	PCI_AD24	
AD23	M5	PCI_AD23	
AD22	E4	PCI_AD22	
AD21	N3	PCI_AD21	
AD20	E3	PCI_AD20	
AD19	N2	PCI_AD19	
AD18	E5	PCI_AD18	
AD17	N1	PCI_AD17	
AD16	F4	PCI_AD16	
AD15	F5	PCI_AD15	
AD14	L3	PCI_AD14	
AD13	H2	PCI_AD13	
AD12	L2	PCI_AD12	
AD11	G4	PCI_AD11	
AD10	L1	PCI_AD10	
AD9	G2	PCI_AD9	
AD8	K2	PCI_AD8	
AD7	J5	PCI_AD7	
AD6	H4	PCI_AD6	
AD5	J4	PCI_AD5	
AD4	G5	PCI_AD4	
AD3	K1	PCI_AD3	
AD2	H3	PCI_AD2	
AD1	J3	PCI_AD1	
AD0	H5	PCI_AD0	
C/BE3#	N4	PCI_C/BE#3	
C/BE2#	M4	PCI_C/BE#2	
C/BE1#	K4	PCI_C/BE#1	
C/BE0#	J2	PCI_C/BE#0	

ICH4-M-U

ICH_PME#
Internal
Pull-up

3D3V_S0
R539 1 — 2 8K2R2 ICH_GPIO5
R540 1 — 2 8K2R2 PM_THRM#

3D3V_S5
RN68 4 1 3 2 BATLOW# SYS_RESET# — SRN10KJ

3D3V_S0
RN69 4 1 3 2 PCI_CLKRUN# AGPBUSY# — SRN10KJ
1 2 MUTE
DUMMY-10KR2
R494 1 — 2 100KR2 VGATE
R526 1 — 2 100KR2 RSMRST#

TP117 TPAD28 PCI_GNTA#
TP118 TPAD28 PCI_GNTB#

R522 10R2
SC10P50V2JN-1
BC264

BIOS NOTE:
BIOS should disable PM_STPCPU# on CK_Titan.
(Use H_DPSLP# instead)

U49B

R506 1 — 2 10KR2

	APICCLK	J19	
	APICD0	H19	
	APICD1	K20	
5 CC_STPCLK#	STPCLK#	V23	
5 CC_A20M#	A20M#	AB23	
5 CC_CPUSLP#	CPUSLP#	U21	
5,7 CC_CPUPWRGD	CPUPWRGD	Y23	
5 CC_INTR	INTR	AB22	
5 CC_NMI	NMI	V21	
5 CC_SMI#	SMI#	W23	
5 CC_IGNNE#	IGNEE#	W21	
28 ICH_A20GATE	A20GATE	Y22	
28 RCIN#	RCIN#	U22	
5 CC_FERR#	FERR#	AA21	
5,27 CC_INIT#	INIT#	V22	
19,21,28 PCI_SERIRQ	SERIRQ	J22	
27,28 LPC_LFRAME#	LFRAME#/FWH4	T5	
TPAD28 TP121 LPC_LDRQ0#	LDRQ0#	U3	
TPAD28 TP120 LPC_LDRQ1#	LDRQ1#	U4	
27,28 LPC_LAD[3..0]	LAD0/FWH0	T2	
LPC_LAD1	LAD1/FWH1	R4	
LPC_LAD2	LAD2/FWH2	T4	
LPC_LAD3	LAD3/FWH3	U2	
8,30 PM_SUS_CLK	SUSCLK	AA4	
	INTRUDER#	W6	
RTCRST#	RTCRST#	W7	
25,30 G768D_PWROK	PWROK	AB6	
30 RSMRST#	RSMRST#	AA6	
	VCCRTC	AB5	
ICH_VBIAS	VBIAS	Y6	
RTCX1	RTCX1	AC7	
RTCX2	RTCX2	AC6	
32 DPRSLPVR	DPRSLPVR	V20	
5,7 CC_DPSLP#	DPSLP#	U23	

AGPBUSY#/GPIO6	AGPBUSY# 7	R2	
GPIO7	ECSMI 28	R3	
GPIO8	ECSWI 28	V4	
GPIO12	ECSCI 28	V5	
GPIO13	BAY_PWROK#	W3	BAY_PWROK# 26
STP_PCI#/GPIO18	PM_SLP_S1# G	Y21	
SLP_S1#/GPIO19		W18	PM_STPPCI# 3
STP_CPU#/GPIO20	PM_C3_STAT#	W19	PM_STPCPU# 3,32
C3_STAT#/GPIO21	PM_CPUPERF#	T3	TP119 TPAD28
CPUPERF#/GPIO22	ICH_GMUXSEL#	Y20	TP93 TPAD28
SSMUXSEL/GPIO23	PCI_CLKRUN#	J21	TP91
CLKRUN#/GPIO24	EXT_POR_L	AC2	PCI_CLKRUN# 19,21,23
GPIO25		V2	EXT_POR_L 23
GPIO27	PWR_LED# R673 1 — 2 0R2-0	W1	MUTE 25
GPIO28	01/30/04	W4	PWR_STBY_LED# 14
SLP_S3#	PM_SLP_S5#	Y4	PM_SLP_S3# 24,30,33,34,36
SLP_S4#	ICH_RI# R543 1 — 2 10KR2	Y2	PM_SLP_S4# 28,31,34,35,36
SLP_S5#		AA2	TP122
RI#		Y1	3D3V_S5 TPAD28
PWRBTN#	SYS_RESET#	AA1	SB_PWRBTN# 31
SYS_RESET#	BATLOW#	Y3	
LAN_RST#	PM_SUS_STAT#	V5	R542 1 — 2 10KR2
BATLOW#/TP0	VGATE	AB2	
SUS_STAT#/LPCPD#	THRMTRIP#	AB3	PM_SUS_STAT# 28
VGATE/VRMPWRGD	PM_THRM#	V19	VGATE 32
THRMTRIP#		W20	
THRM#	SMBD_SB	V1	PM_THRM# 8,30
SMLINK0	SMBC_SB	AC3	
SMLINK1	SMB_ALERT#	AB1	
SMBDATA		AB4	
SMBCLK		AC4	
SMBALERT#/GPIO11	SB_SPKR	AA5	
SPKR	CLK14_ICH	H23	SB_SPKR 25
CLK14		J23	CLK14_ICH 3

ICH4-M-U

R491 DUMMY-33R2
BC233 DUMMY-SC10P50V2JN-1

CLK termination close to ICH4

Should go high no sooner than 10mS after both +3VRUN and +1.5VRUN have reach their nominal voltage

Should go high no sooner than 10mS after both +3VSUS and +1.5VSUS have reach their nominal voltage

S5 OK

If ICH-4 LAN not used,10K ohm PD or connect directly to ----RSMRST#(SUSPWROK) But in Bon conncet to PWROK(DELAY_IMVP_PWRGD)

VCC_IO_S0 — R497 56R2J — THRMTRIP# — R498 56R2J — PM_THERMTRIP# 5

VCC_RTC_S5 — R525 100KR2

RTC Circuitry

VCC_RTC_S5 — BC155 SC1U10V3KX
3D3V_AUX — D25 RB751V-40-U — BC53 SC1U10V3KX
3D3V_RTC — RB751V-40-U

RTC1 — SCON3 21.D0010.103

LAYOUT: MAKE PAD ACCESSABLE

RTCRST# — R199 180KR2 — D26 RB751V-40-U — R68 1KR2 — RTBAT
GP1 GAP-OPEN — RTCRST#
BC136 SCD1U10V2MX-1
RTCRST# delay 18~25ms
BC146 SCD047U25V3KX

ICH_VBIAS — R233 10MR2J
RTCX1 — BC156 SC12P50V2JN-1
RTCX2 — R234 10MR2J — X4 X-32D768KHZ-12-U
BC154 SC12P50V2JN-1

3D3V_S5 — R541 10KR2

R165 0R2-0
PM_SLP_S1# G — PM_SLP_S1# 3
PM_SLP_S3# — U41 DUMMY-NC7SZ08-U — 3D3V_S5 — BC134 DUMMY-SCD1U16V3KX

3D3V_S5 — RN61 SRN4D7KJ — SMBC_SB — SMBC_ICH 3,10
5V_S0 — R528 0R2-0 — Q49 2N7002
3D3V_S0 — RN27 SRN10KJ — SMBD_SB — Q48 2N7002 — SMBD_ICH 3,10

3D3V_S5 — R524 10KR2 — SMB_ALERT#

H/W Strapping
SB_SPKR — R490 DUMMY-1KR2 — 3D3V_S0
Stuff for No Reboot

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Title: *ICH4-M (2 of 3)*
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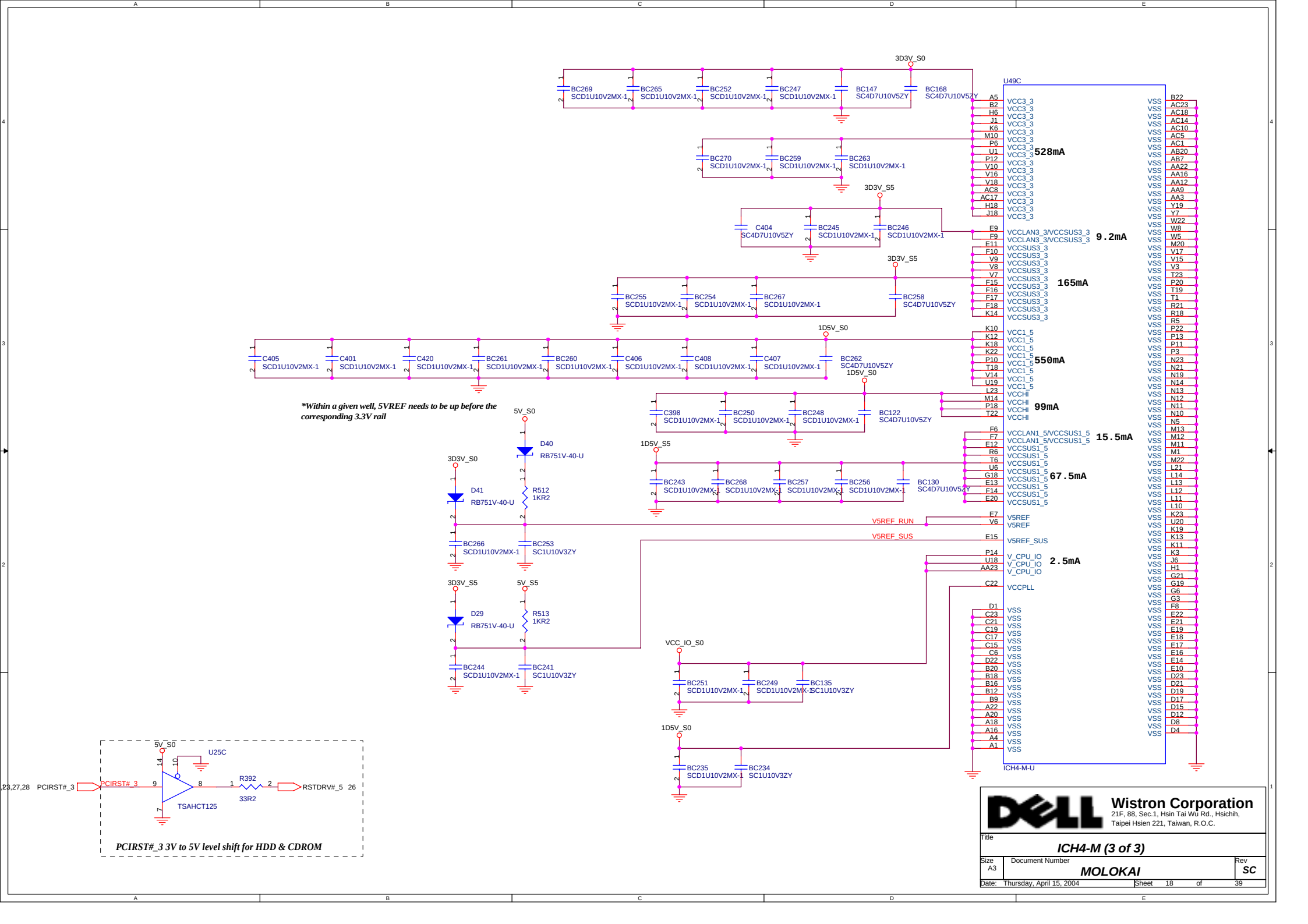
3D3V_S0
U49C
ICH4-M-U
528mA
9.2mA
165mA
1D5V_S0
550mA
99mA
15.5mA
67.5mA
2.5mA
5V_S0
3D3V_S5
5V_S5
1D5V_S5
VCC_IO_S0
V5REF_RUN
V5REF_SUS
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
U25C
TSAHCT125
PCIRST#_3
RSTDRV#_5
PCIRST#_3 3V to 5V level shift for HDD & CDROM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH4-M (3 of 3)
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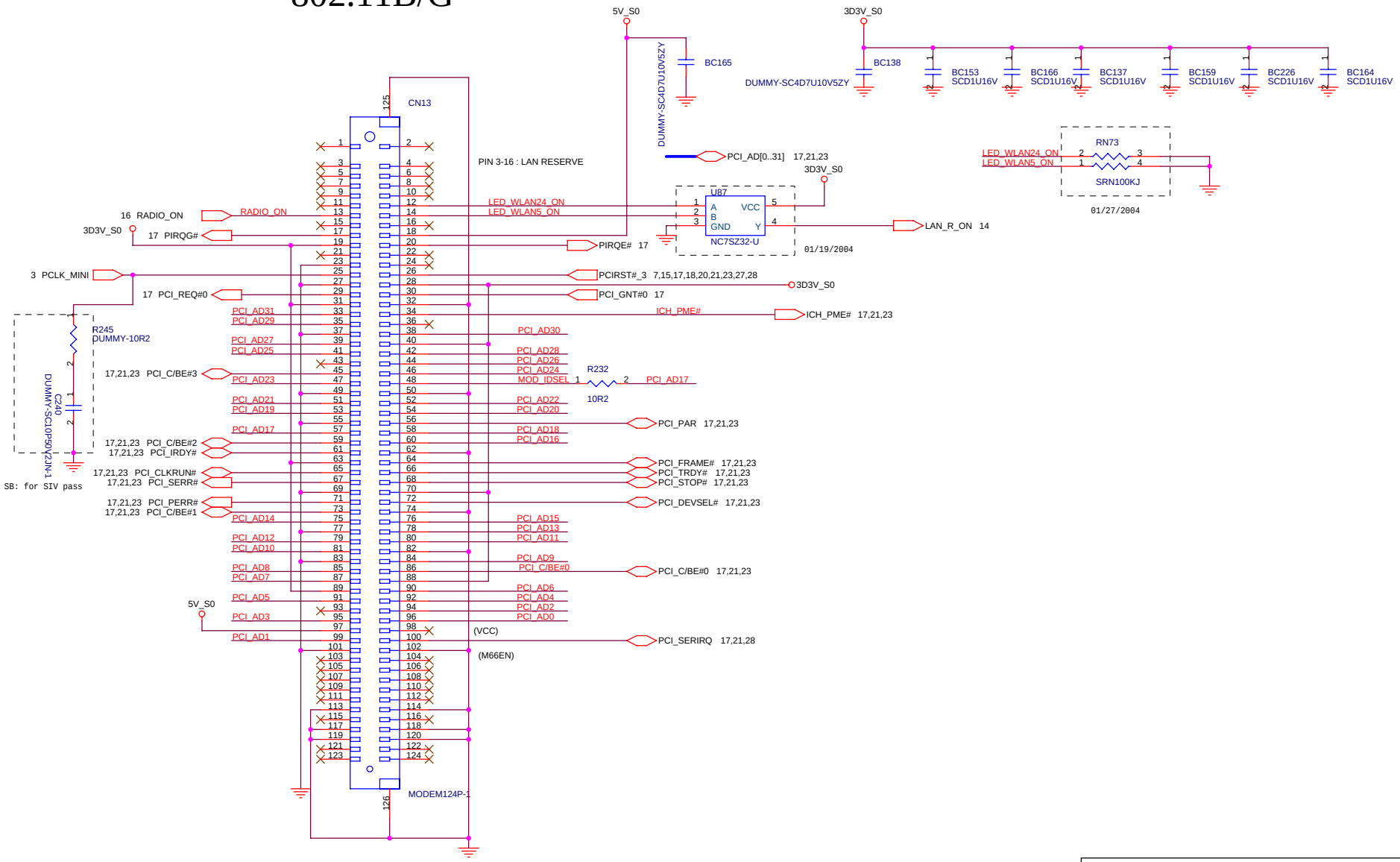
Mini PCI
802.11B/G



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Mini PCI Socket*		
Size: A3	Document Number: *MOLOKAI*	Rev: *SC*
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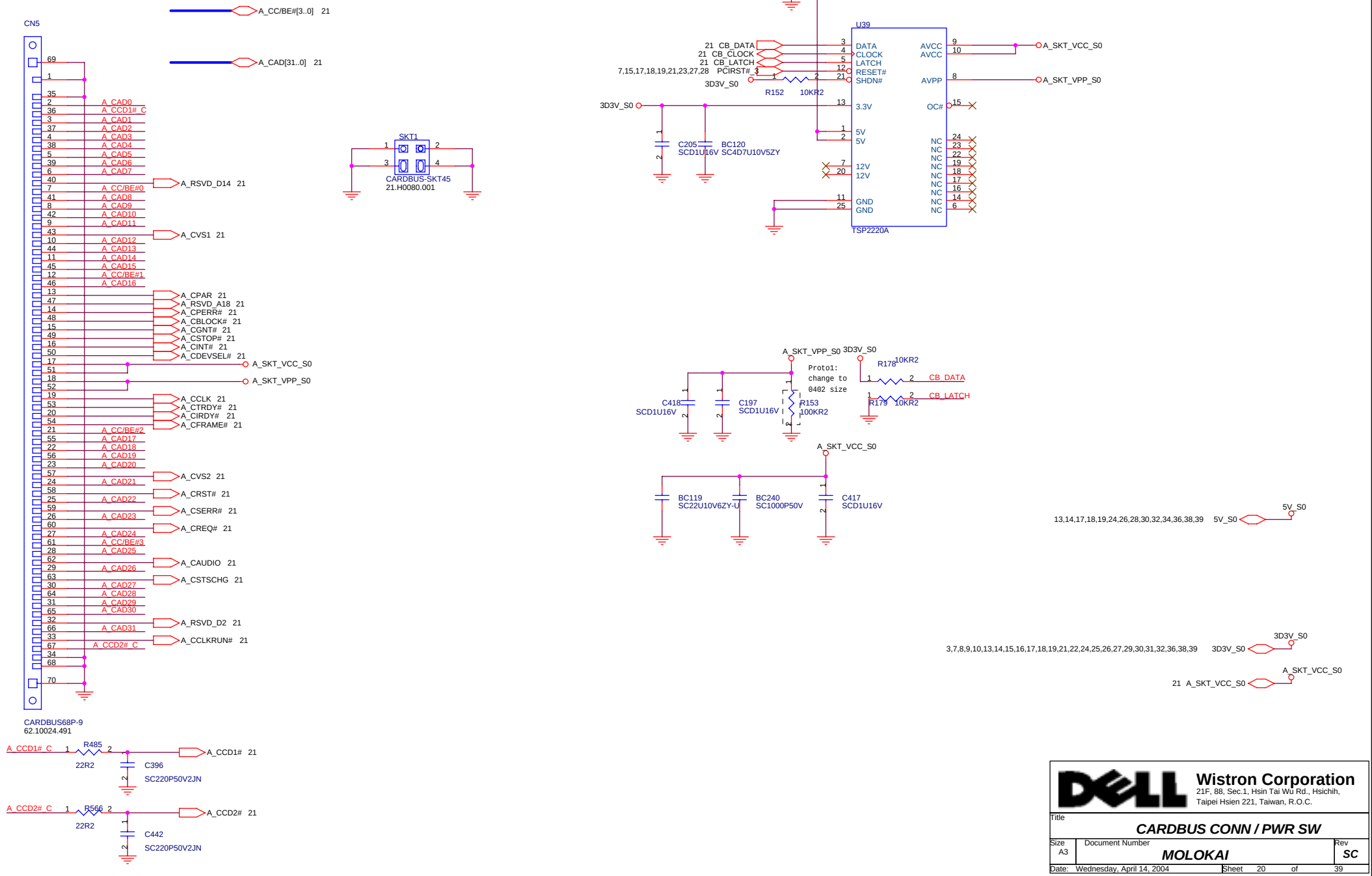
PCMCIA socket



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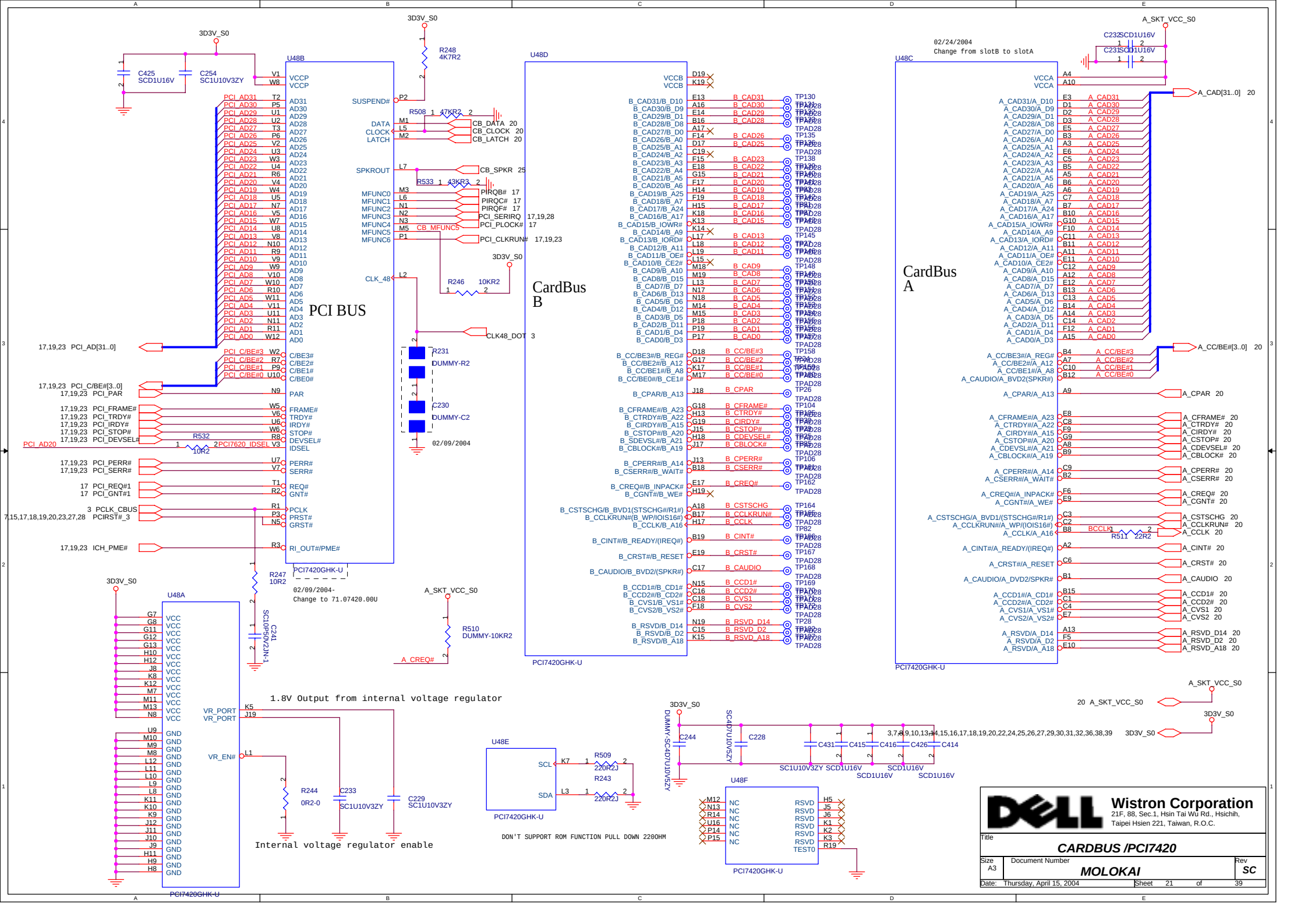
Title	CARDBUS CONN / PWR SW	
Size A3	Document Number MOLOKAI	Rev SC
Date: Wednesday, April 14, 2004	Sheet 20 of 39	


PCI BUS
CardBus B
CardBus A
U48B
U48D
U48C
U48A
U48E
U48F
PCI7420GHK-U
02/24/2004
Change from slotB to slotA
02/09/2004-
Change to 71.07420.00U
1.8V Output from internal voltage regulator
Internal voltage regulator enable
DON'T SUPPORT ROM FUNCTION PULL DOWN 220OHM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CARDBUS /PCI7420
Size A3
Document Number
MOLOKAI
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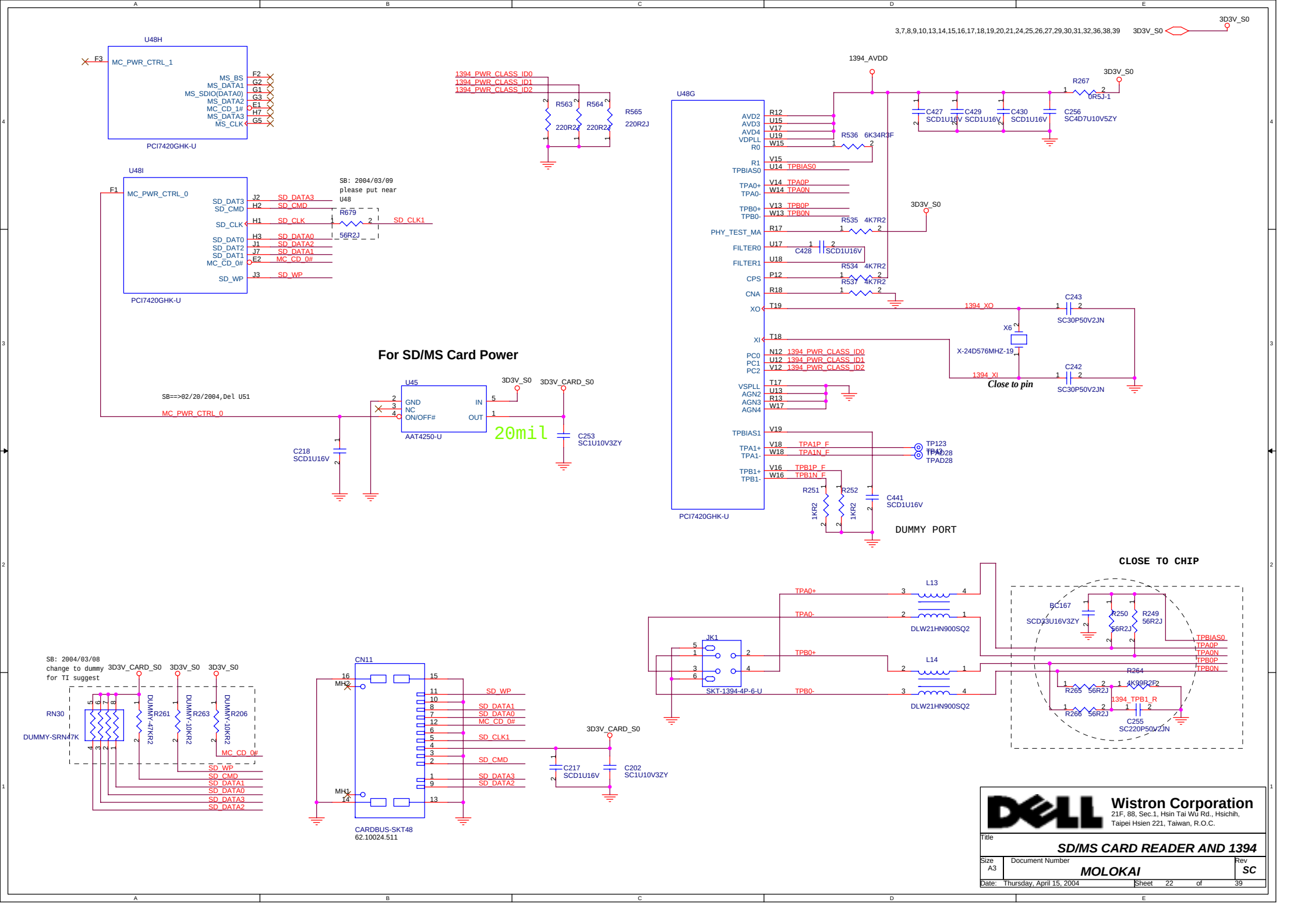

3D3V_S0
3,7,8,9,10,13,14,15,16,17,18,19,20,21,24,25,26,27,29,30,31,32,36,38,39
3D3V_S0
U48H
F3
MC_PWR_CTRL_1
MS_BS F2
MS_DATA1 G2
MS_SDIO(DATA0) G1
MS_DATA2 G3
MC_CD_1# E1
MS_DATA3 H7
MS_CLK G5
PCI7420GHK-U
1394_PWR_CLASS_ID0
1394_PWR_CLASS_ID1
1394_PWR_CLASS_ID2
R563 220R2J
R564 220R2J
R565 220R2J
1394_AVDD
3D3V_S0
R267 0R5J-1
U48G
AVD2 R12
AVD3 U15
AVD4 V17
VDPLL U19
R0 W15
R536 6K34R3F
C427 SCD1U16V
C429 SCD1U16V
C430 SCD1U16V
C256 SC4D7U10V5ZY
R1 V15
TPBIAS0 U14 TPBIAS0
TPA0+ V14 TPA0P
TPA0- W14 TPA0N
TPB0+ V13 TPB0P
TPB0- W13 TPB0N
R535 4K7R2
PHY_TEST_MA R17
3D3V_S0
FILTER0 U17
C428 SCD1U16V
FILTER1 U18
R534 4K7R2
CPS P12
R537 4K7R2
CNA R18
XO T19
1394_XO
C243 SC30P50V2JN
X6
X-24D576MHZ-19
XI T18
1394_XI
C242 SC30P50V2JN
Close to pin
PC0 N12 1394_PWR_CLASS_ID0
PC1 U12 1394_PWR_CLASS_ID1
PC2 V12 1394_PWR_CLASS_ID2
VSPLL T17
AGN2 U13
AGN3 R13
AGN4 W17
TPBIAS1 V19
TPA1+ V18 TPA1P_F
TPA1- W18 TPA1N_F
TP123 TPA2
TPAD28
TPB1+ V16 TPB1P_F
TPB1- W16 TPB1N_F
R251 1KR2
R252 1KR2
C441 SCD1U16V
PCI7420GHK-U
DUMMY PORT
U48I
F1
MC_PWR_CTRL_0
SD_DAT3 J2 SD_DATA3
SD_CMD H2 SD_CMD
SD_CLK H1 SD_CLK
R679 56R2J
SD_CLK1
SD_DAT0 H3 SD_DATA0
SD_DAT2 J1 SD_DATA2
SD_DAT1 J7 SD_DATA1
MC_CD_0# E2 MC_CD_0#
SD_WP J3 SD_WP
PCI7420GHK-U
SB: 2004/03/09
please put near
U48
For SD/MS Card Power
SB==>02/20/2004,Del U51
MC_PWR_CTRL_0
U45
GND
NC
ON/OFF#
IN
OUT
AAT4250-U
3D3V_S0
3D3V_CARD_S0
20mil
C218 SCD1U16V
C253 SC1U10V3ZY
CLOSE TO CHIP
TPA0+
TPA0-
TPB0+
TPB0-
L13
L14
DLW21HN900SQ2
DLW21HN900SQ2
JK1
SKT-1394-4P-6-U
BC167 SCD33U16V3ZY
R250 56R2J
R249 56R2J
R264 4K99R2F2
R265 56R2J
R266 56R2J
1394_TPB1_R
C255 SC220P50V2JN
TPBIAS0
TPA0P
TPA0N
TPB0P
TPB0N
SB: 2004/03/08
change to dummy
for TI suggest
3D3V_CARD_S0
3D3V_S0
3D3V_S0
RN30
DUMMY-SRN47K
DUMMY-47KR2
R261
DUMMY-10KR2
R263
DUMMY-10KR2
R206
MC_CD_0#
SD_WP
SD_CMD
SD_DATA1
SD_DATA0
SD_DATA3
SD_DATA2
CN11
MH2
MH1
CARDBUS-SKT48
62.10024.511
SD_WP
SD_DATA1
SD_DATA0
MC_CD_0#
SD_CLK1
SD_CMD
SD_DATA3
SD_DATA2
3D3V_CARD_S0
C217 SCD1U16V
C202 SC1U10V3ZY
DELL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SD/MS CARD READER AND 1394
Size A3
Document Number
MOLOKAI
Rev SC
Date: Thursday, April 15, 2004
Sheet 22 of 39

Broadcom LAN

BCM4401

LAN EEPROM

10/100M Lan Transformer

Close to power pin

Place near Chip

Place RDAC CKT as close to chip as possible

Place PLLVDD2_LAN/PLLVDD3_LAN CKT as close to chip as possible

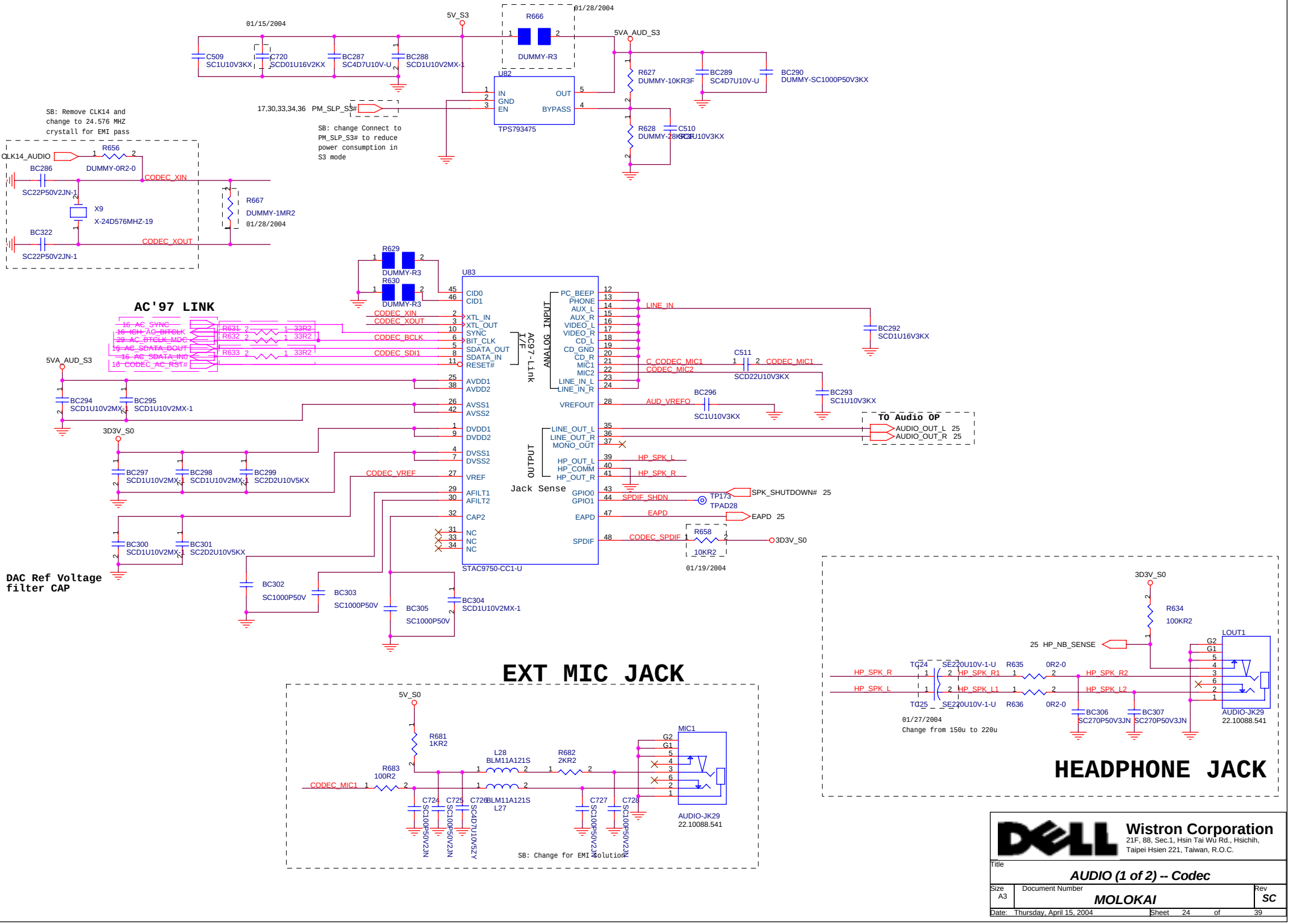
BCM4401 requires 16-Bit R/W data width

Note: The BCM4401L has weak internal pulldown resistors on the follow signals:

SPROM_CS,SPROM_CLK,SPROM_DOUT,SPROM_DIN

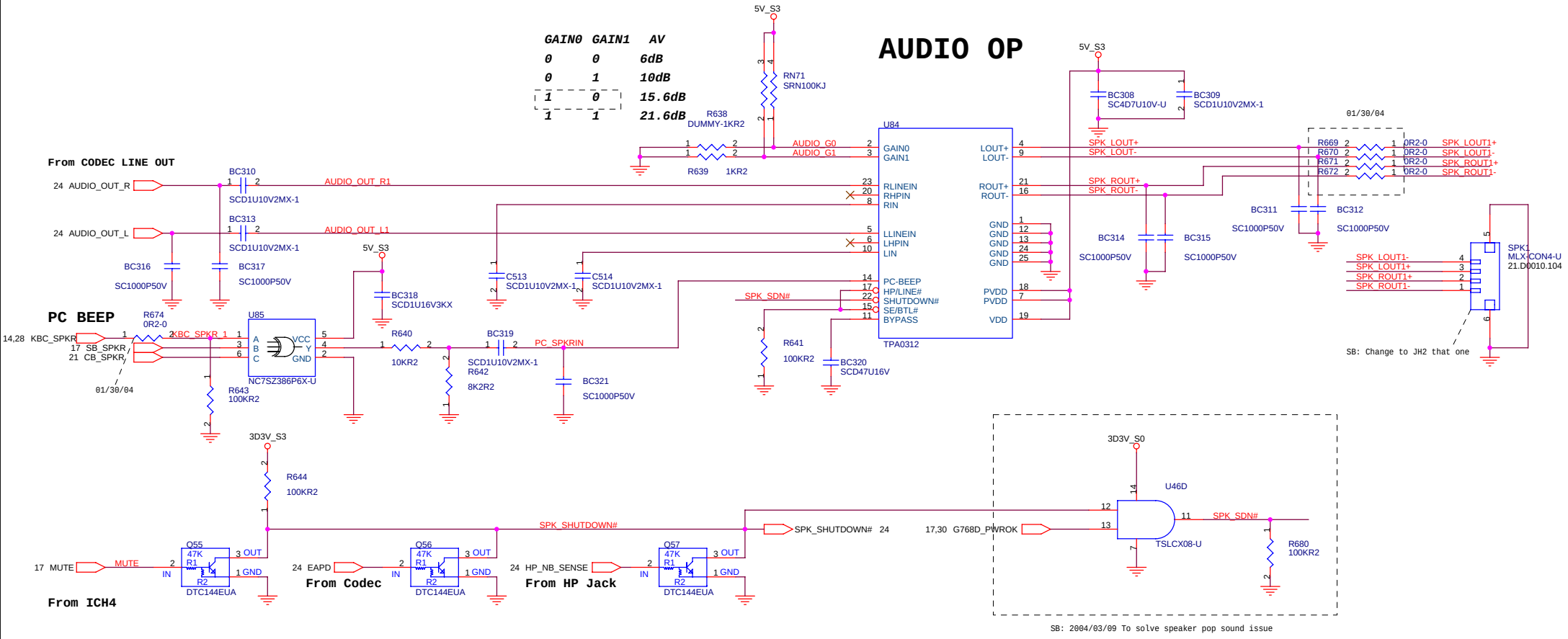
EXT_POR_L is an active low signal used to place the BCM4401 into IDDQ mode, <5 mA current consumption

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	10/100 LAN
Size: Custom	Document Number: MOLOKAI
Rev	SC
Date: Thursday, April 15, 2004	Sheet 23 of 39



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO (1 of 2) -- Codec*		
Size: A3	Document Number: *MOLOKAI*	Rev: *SC*
Date: Thursday, April 15, 2004	Sheet 24 of 39	

AUDIO OP



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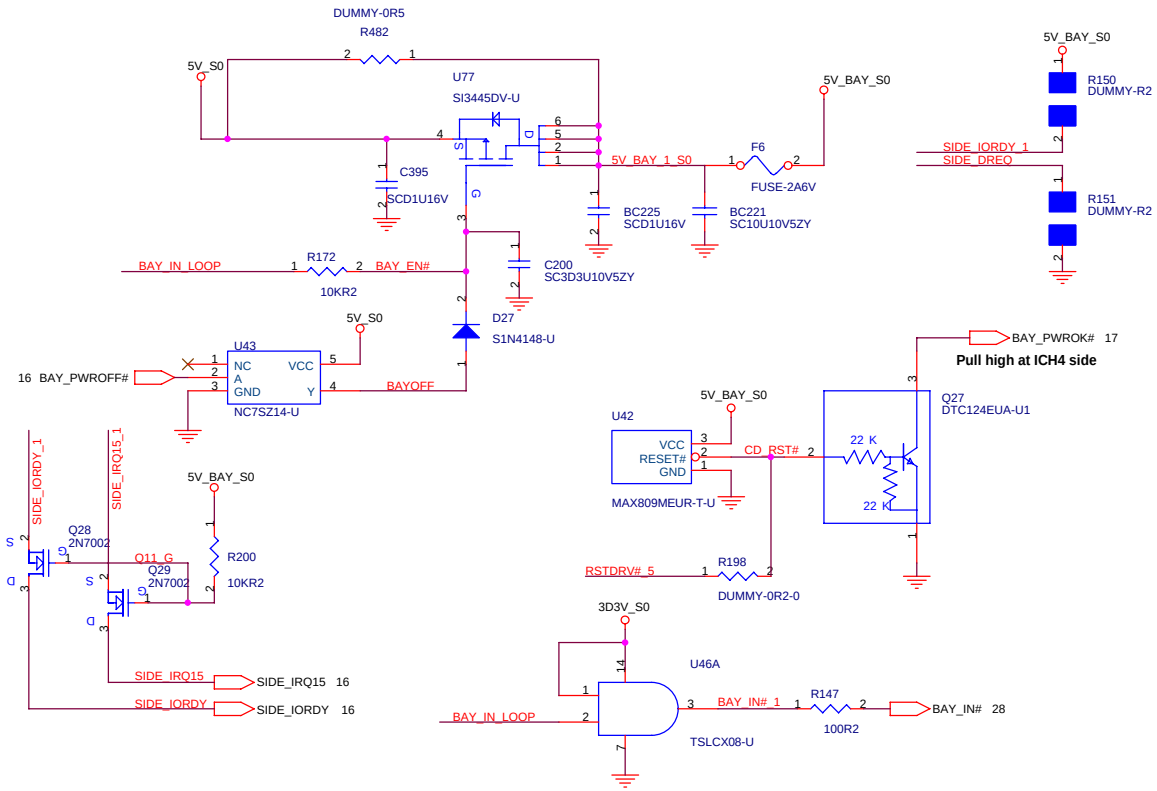
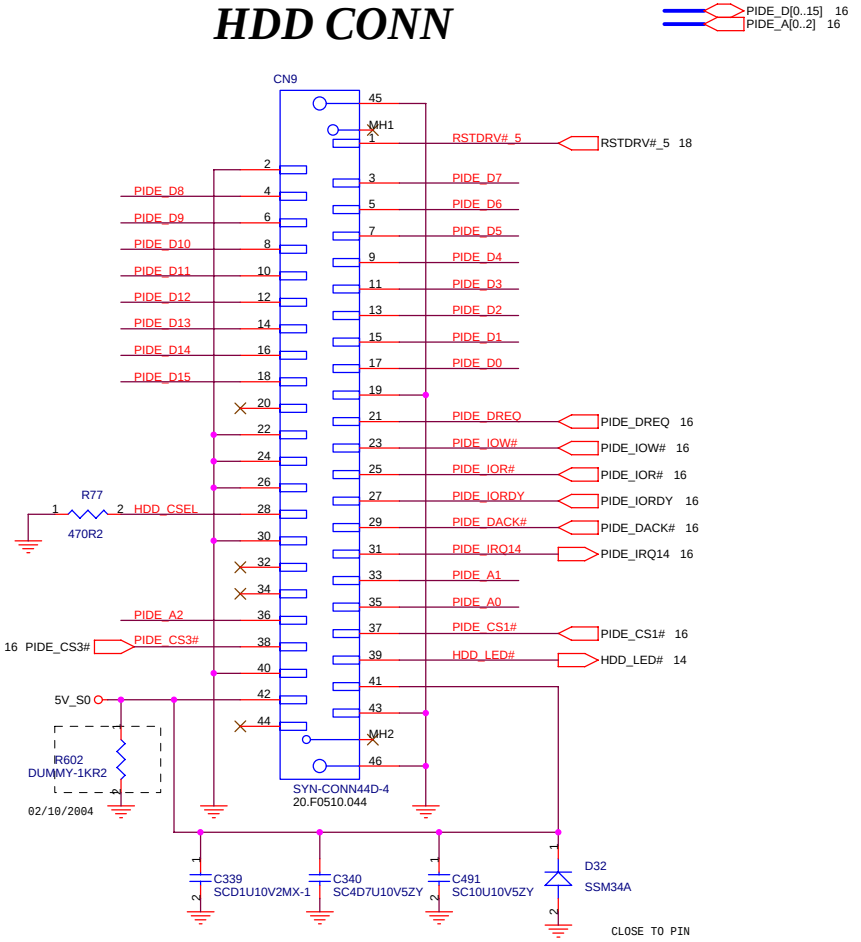
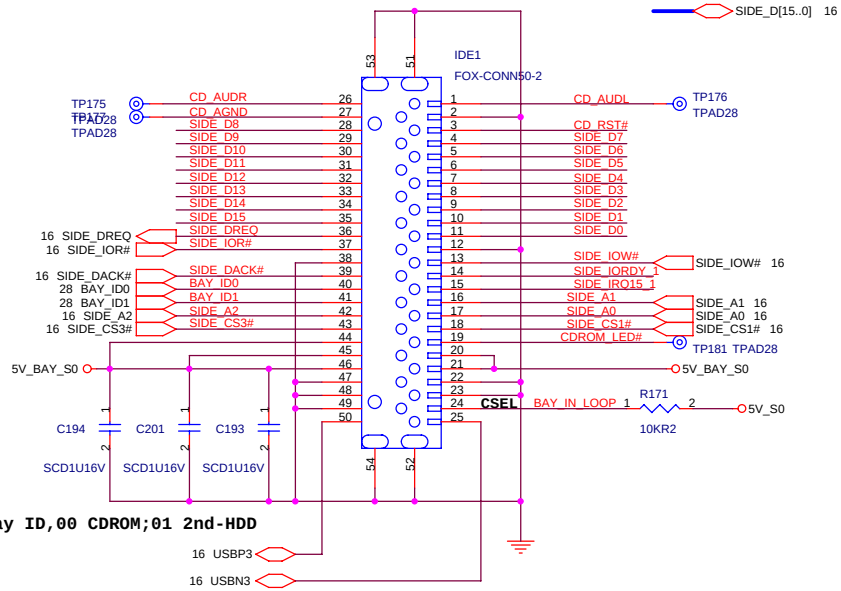
Title	AUDIO (2 of 2) --Phone Jack
Size: A3	Document Number: MOLOKAI
Rev: SC	
Date: Thursday, April 15, 2004	Sheet 25 of 39



HDD CONN



CDROM



Optical Bay ID,00 CDROM;01 2nd-HDD

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Title: **HDD/CD ROM**

Size	Document Number	Rev
A3	**MOLOKAI**	SC

Date: Thursday, April 15, 2004 Sheet 26 of 39

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

RN29
SELECT_FWH
FWH_FGPI4
SRN10K-2

RN28
FWH_FGPI3
FWH_FGPI2
FWH_FGPI1
FWH_FGPI0
SRN10K-2

Unused FGPI pins must not be float

7,15,17,18,19,20,21,23,28 PCIRST#_3

R585 68R2

SB: Because new add R684 is 330 ohm so need change R260 from 1K to 4.7K to make FWH_INIT# low level be correct

3D3V_S0
1D5V_S0
R260 4K7R2
R259 1K5R2
Q33
FWH_INT_Q
MMBT3904-1-U
84.03904.B11

CC_INIT1#
R684 330R2
CC_INIT# 5,17
SB: for SIV pass

U55
49LF004A-33

1	NC	OE#/INIT#	32
2	NC	WE#/FWH4	31
3	NC	NC	30
4	VSS	DQ7/RES	29
5	IC	DQ6/RES	28
6	A10/FGPI4	DQ5/RES	27
7	R/C#(CLK)	DQ4/RES	26
8	VDD	DQ3/LAD3	25
9	NC	VSS	24
10	RST#	DQ2/LAD2	23
11	A9(FGPI3)	DQ1/LAD1	22
12	A8(FGPI2)	DQ0/LAD0	21
13	A7(FGPI1)	A0/ID0	20
14	A6(FGPI0)	A1/ID1	19
15	A5(WP#)	A2/ID2	18
16	A4(TBL#)	A3/ID3	17

FWH_INIT#
LPC_LFRAME# 17,28
LPC_LAD3
LPC_LAD2
LPC_LAD1
LPC_LAD0
LPC_LAD[3..0] 17,28

3D3V_S0
3D3V_S0
SELECT_FWH
FWH_FGPI4
FWH_FGPI3
FWH_FGPI2
FWH_FGPI1
FWH_FGPI0

3 PCLK_FWH
R262 10R2
PCLK_FWH_2
R240 10KR2
63.10334.1D1
16 FWH_WP#
BC163 SC10P50V2JN-1

3D3V_S0
BC162 DUMMY-SC10U10V5ZY
BC149 SCD1U10V2MX-1 **78.10492.4B1**
BC158 SCD1U10V2MX-1 **78.10492.4B1**
BC157 SCD1U10V2MX-1 **78.10492.4B1**
BC150 SCD1U10V2MX-1 **78.10492.4B1**

3D3V_S0
3,7,8,9,10,13,14,15,16,17,18,19,20,21,22,24,25,26,29,30,31,32,36,38,39 3D3V_S0

5V_S0
13,14,17,18,19,20,24,26,28,30,32,34,36,38,39 5V_S0

1D5V_S0
7,8,9,15,16,18,38,39 1D5V_S0

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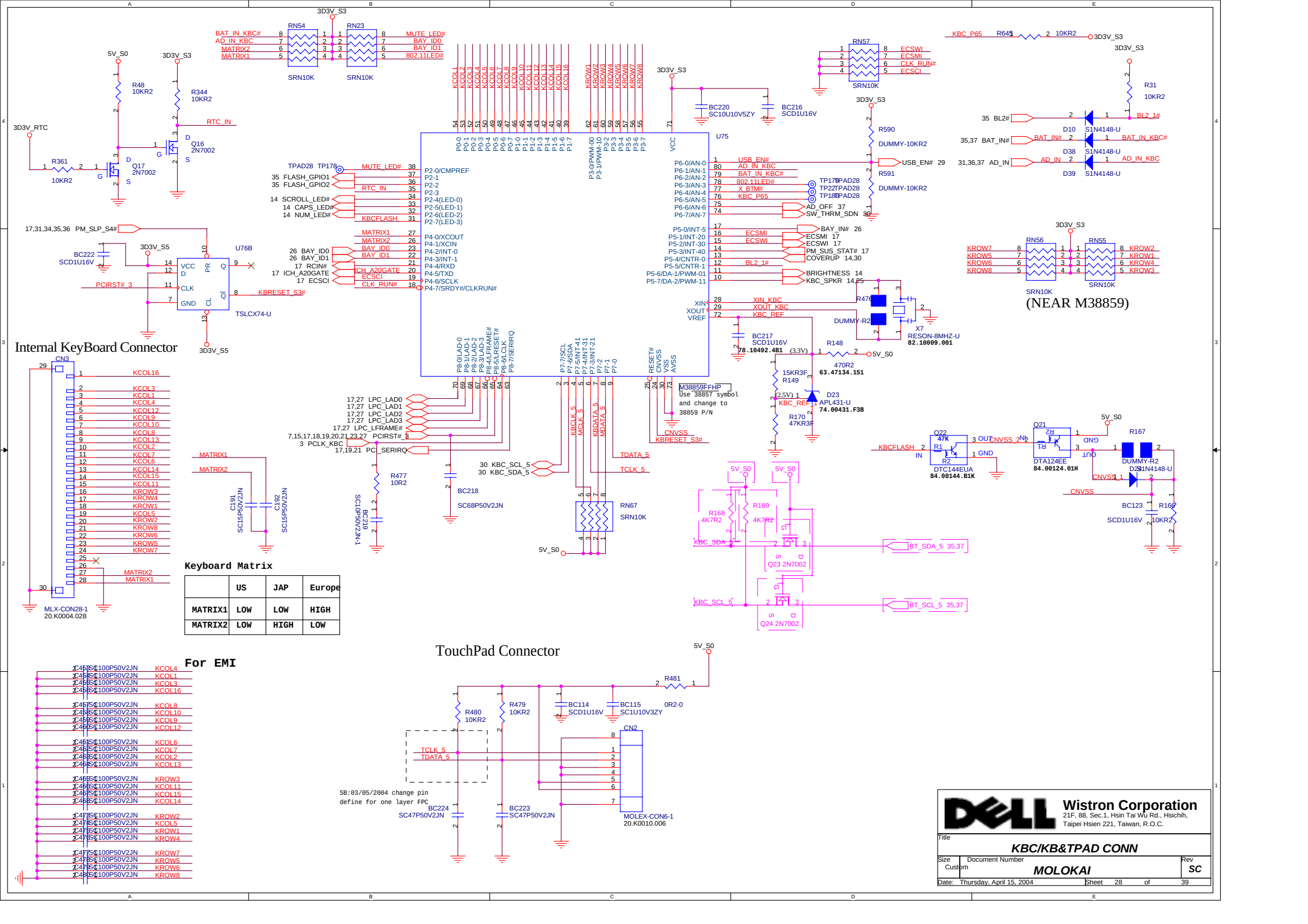
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***FWH/Debug Port***

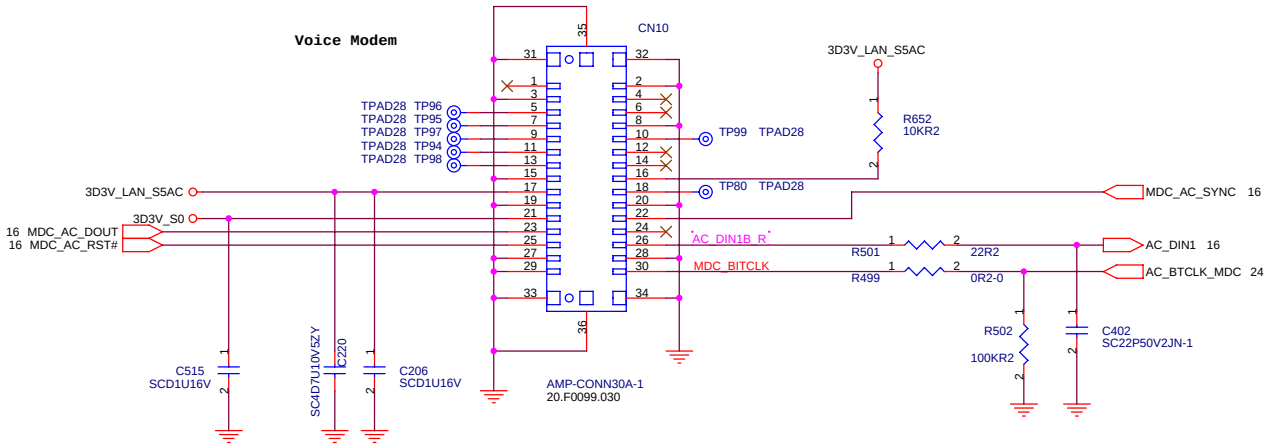
Size	Document Number	Rev
A3	***MOLOKAI***	***SC***

Date: Thursday, April 15, 2004 Sheet 27 of 39

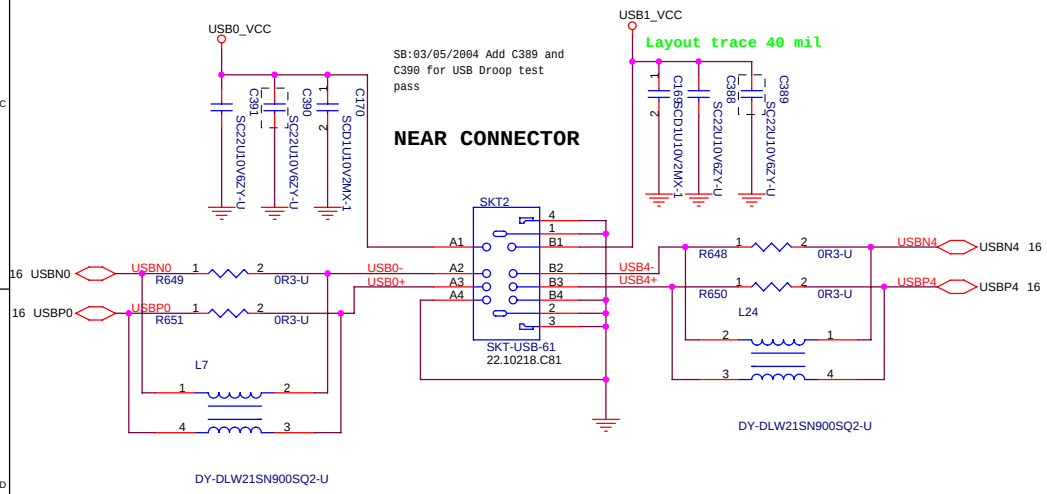


	US	JAP	Europe
MATRIX1	LOW	LOW	HIGH
MATRIX2	LOW	HIGH	LOW

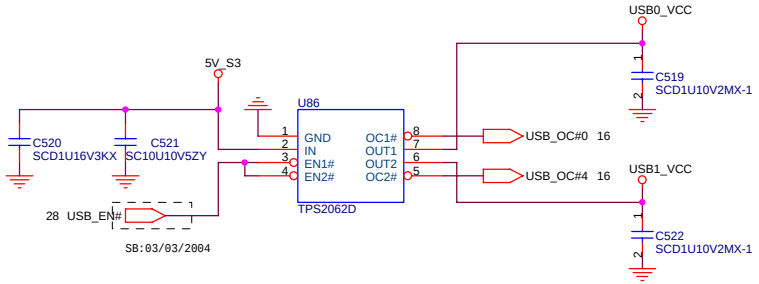
MDC CONN



USB PORT



Dual USB switch



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MDC CONN & USB CONN	
Size A3	Document Number MOLOKAI	Rev SC
Date: Thursday, April 15, 2004	Sheet 29 of 39	

240 ms after VCC_G768 > 4.38v

Check default setting, default enable is preferred

FAN Conn.

THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768D

SYSTEM SENSOR

put together

32K suspend clock output

SC:change TEMP setting from 85 to 105 degree.

HW thermal shut down tempature setting 105 degree . Put Near vent out .

COVER SWITCH

TO KBC

RESUME RESET

TO SB

RSMRST# is RTC power plane

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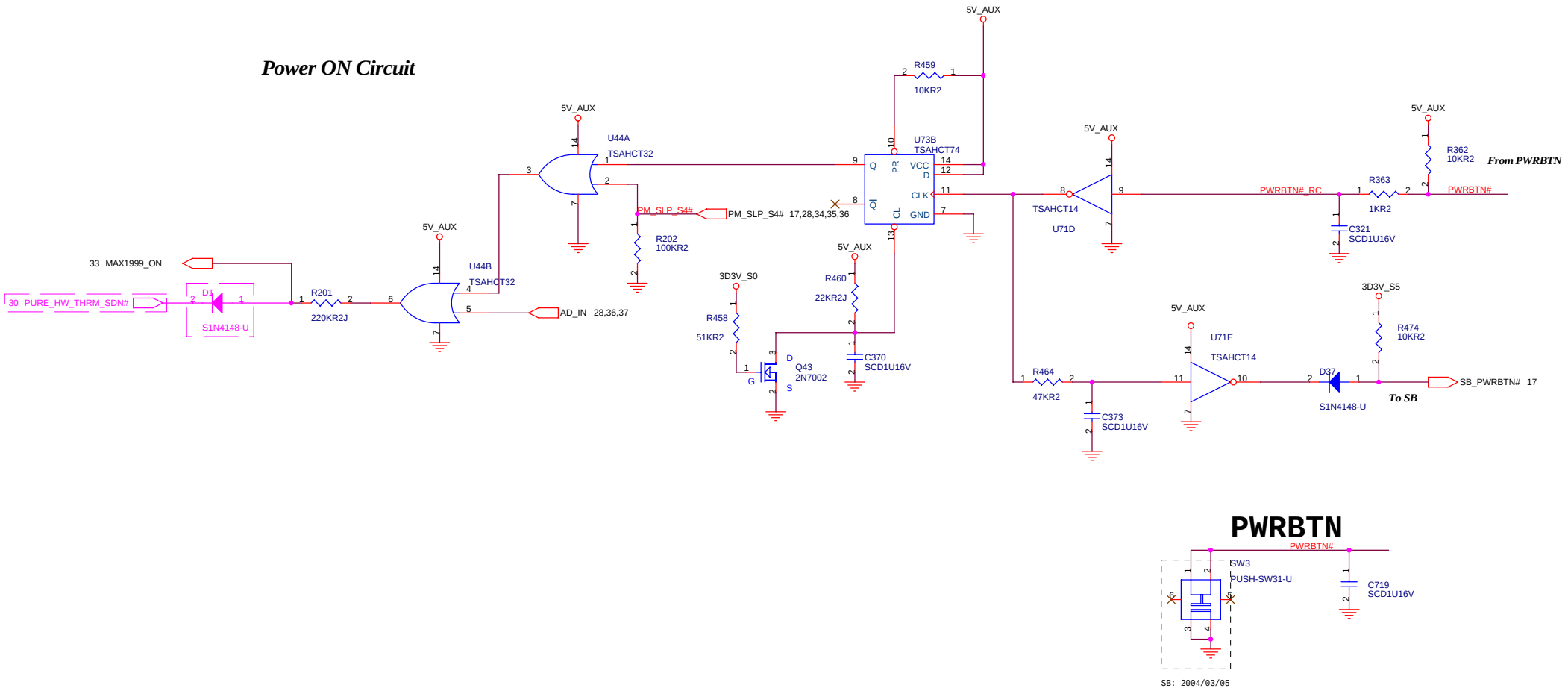
Title: G768D		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 30 of 39	



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: POWER ON CIRCUIT		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 31 of 39	

Deep Sleep
100k/(100k+1.21k)=98.79%
OffSet= 1.21%

	Active	Deep	Deeper
DPRSLPVR	0	0	1
STP_CPU#	1	0	0

IFL=(RISEN*32uA*n) / Rds(on)=
1.96k*32uA*2 / 5mR =25.157A
FDS7088N3 Rds(on)=5mR

MAX=14A

SC: populate C341 for VTT test pass

MAX=21A
Vf=0.7V

SC:Change for VTT test pass

SC: change for load line test pass

SC: populate TC10 for VTT test pass

PWRCH Low ==> One Phase

IMVP IV
Load Line Slope :3mR
32A=> 96mV
Rdroop = 96mV /
32uA

V_OCSET = 1.75V
V_DRSV = 0.75716V
V_BOOT =1.2611V
I_OCSET = 12.5uA =>
OCP =125% ~ 175%

For Banias/ULV CPU:

Active Mode:
1.Highest Frequency:
VID=1.484V/1.00V
2.Lowest Frequency:
VID=0.956V/0.85V
Deep Sleep Mode:
1.Highest Frequency: VID=1.484V,Offset=
-1.2%->VID=1.466
2.Lowest Frequency: VID=0.956V,Offset=
-1.2%->VID=0.945
Deeper Sleep Mode:
VID=0.748V

VCC_IO_S0-->Delay 3 mS-->CPUCORDE_ON_DELAY

SB: 2004/03/01

Wistron Corporation
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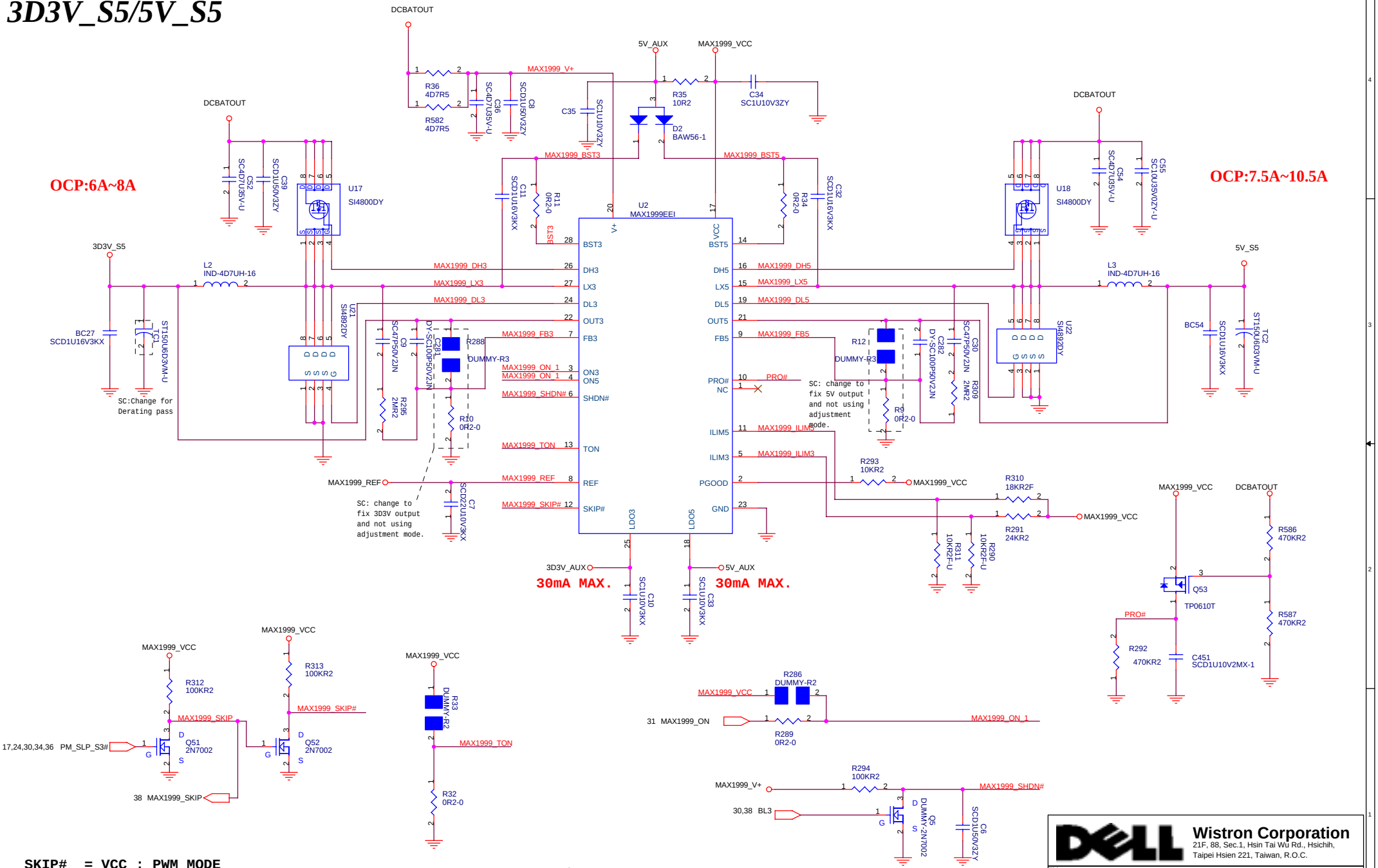
Taipei Hsien 221, Taiwan, R.O.C.

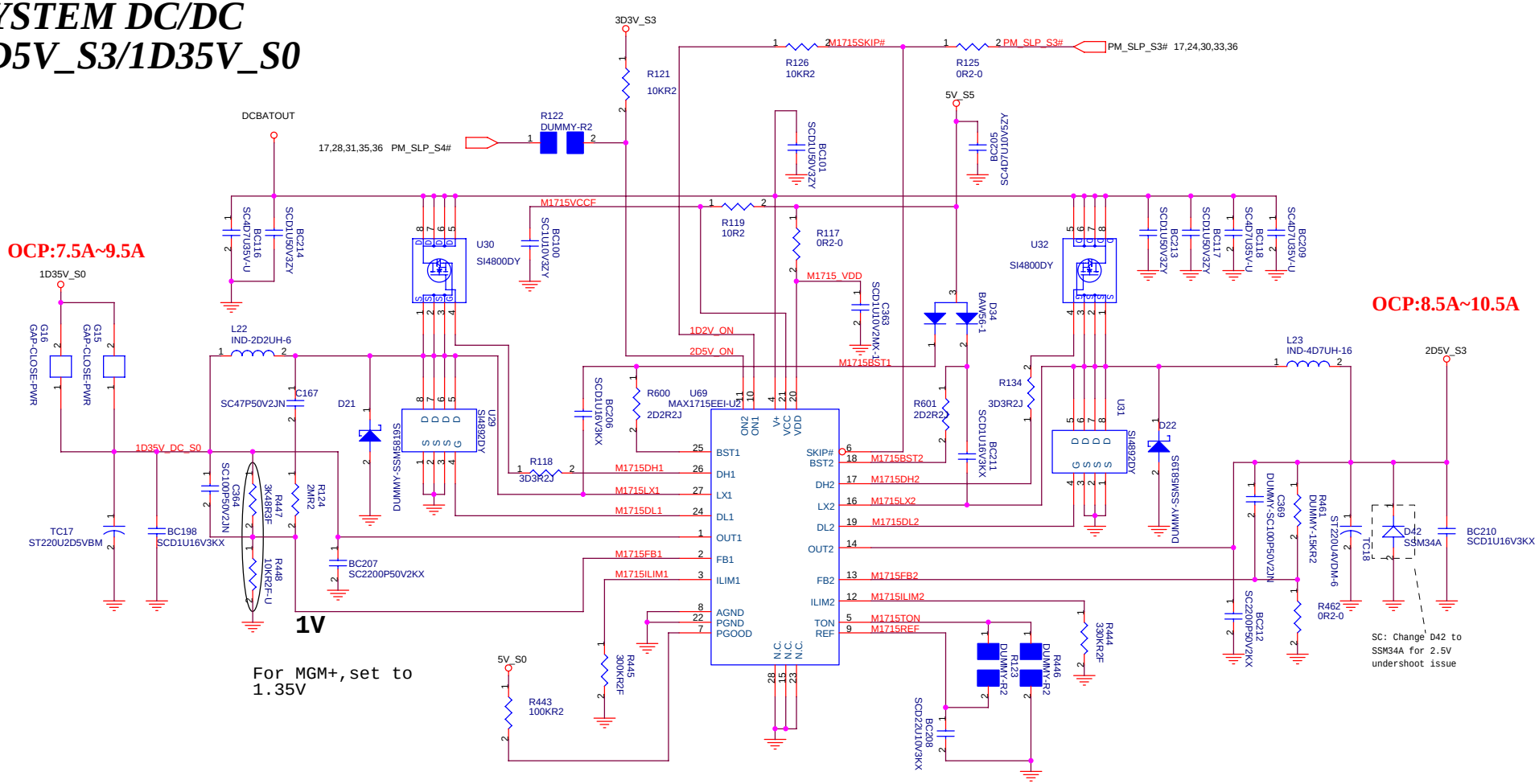
Title: *IMVP IV-CPU POWER-ISL6218*
Size: A3 | Document Number: *MOLOKAI* | Rev: *SC*
Date: Thursday, April 15, 2004 | Sheet 32 of 39

SYSTEM DC/DC
3D3V_S5/5V_S5

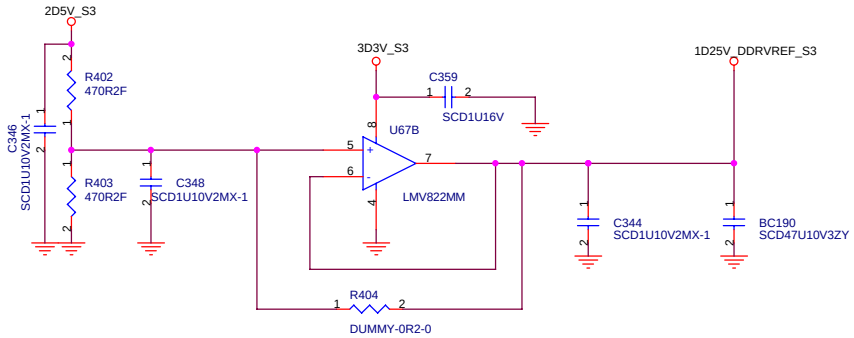


Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	MAX1999/3D3V_S5/5V_S5	
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 33 of 39	

SYSTEM DC/DC
2D5V_S3/1D35V_S0

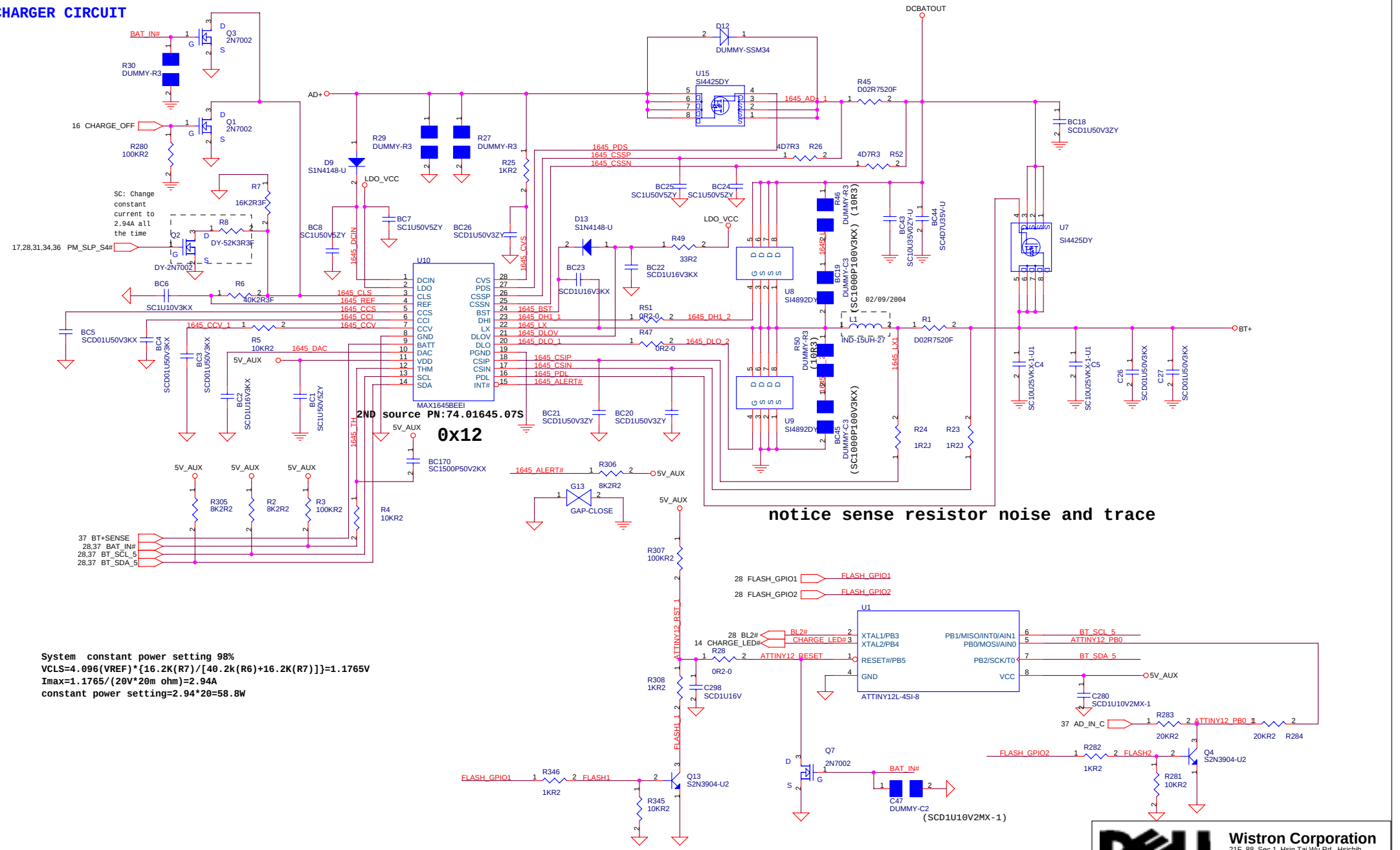


1D25V_DDRVREF_S3 need 10 mil and must near NB/DIMM



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MAX1715/2D5V_S3/1D35V_S0		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 34 of 39	

CHARGER CIRCUIT



System constant power setting 98%
VCLS=4.096(VREF)*{16.2K(R7)/[40.2k(R6)+16.2K(R7)]}=1.1765V
Imax=1.1765/(20V*20m ohm)=2.94A
constant power setting=2.94*20=58.8W

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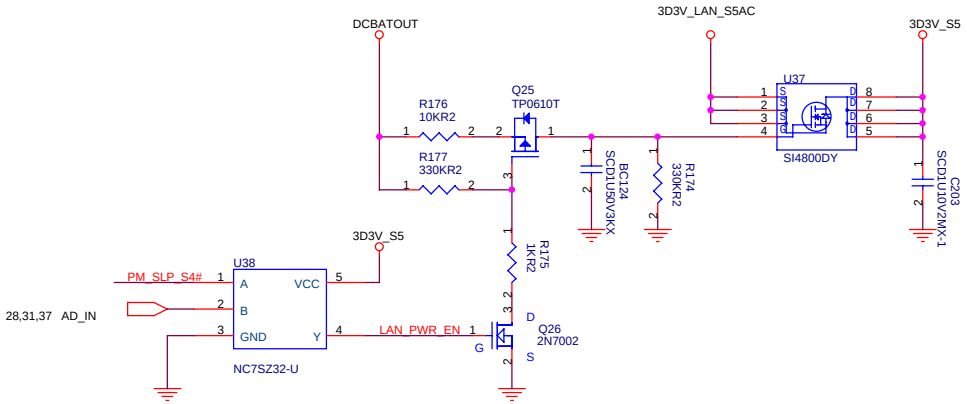
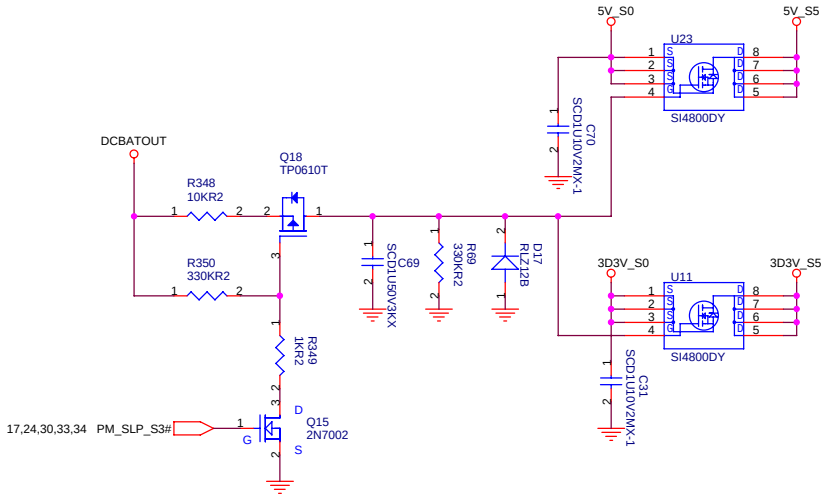
Taipei Hsien 221, Taiwan, R.O.C.

Title	CHARGER&MicroP	
Size: Custom	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 35 of 39	

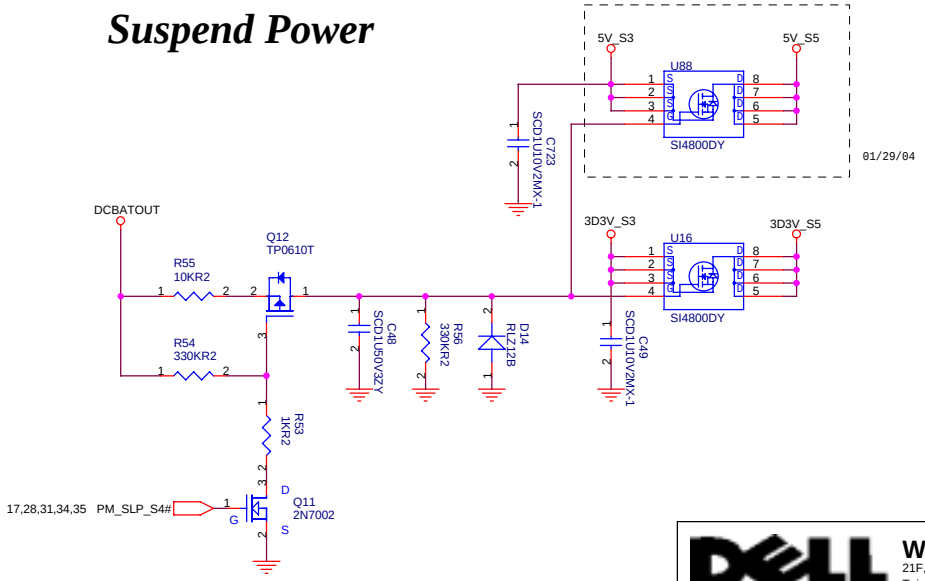
LAN Power



Run Power

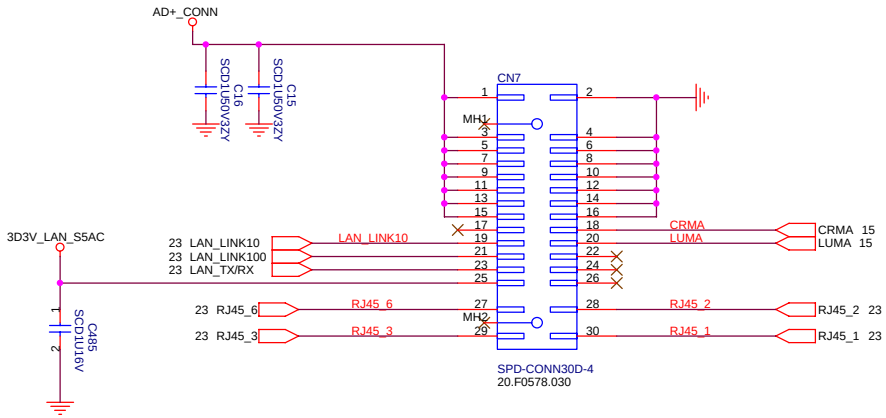


Suspend Power

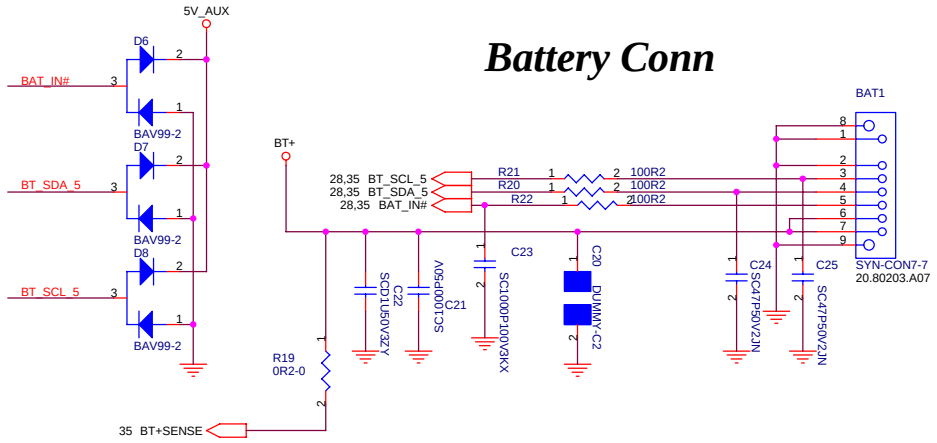


Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *PWR Plane SW / VCC_IO_S0*		
Size: A3	Document Number: *MOLOKAI*	Rev: *SC*
Date: Thursday, April 15, 2004	Sheet 36 of 39	

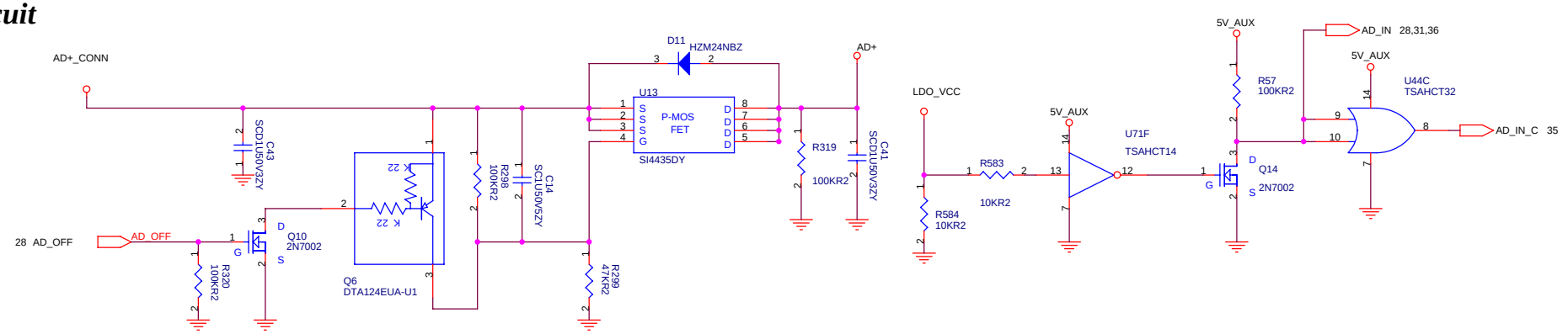
TV BD Conn



Battery Conn

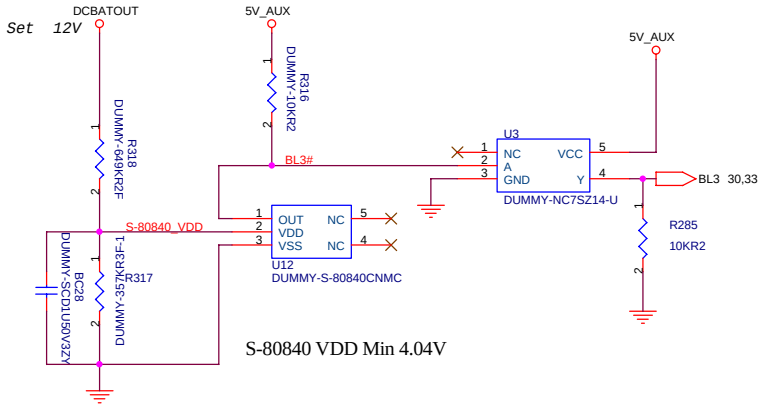


Adaptor In Circuit



DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Battery Conn/TV BD Conn/Adaptor In Circuit	
Size A3	Document Number MOLOKAI	Rev SC
Date: Thursday, April 15, 2004	Sheet 37 of 39	

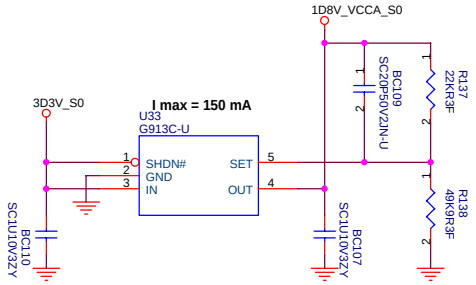
BATRERY LOW3 DETECTOR



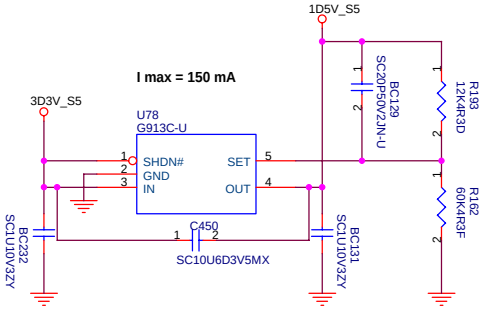
S-80840 VDD Min 4.04V

At Dothan CPU application, POWER is 1.5V or 1.8V.

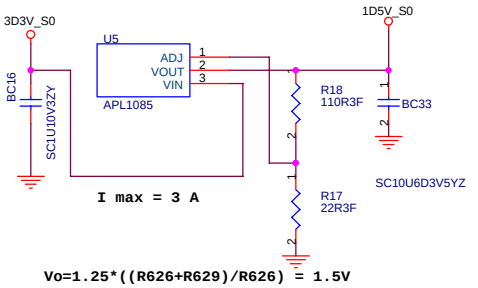
3D3V_S0 --> 1D8V_VCCA_S0 (For CPU VCCA)



3D3V_S5 --> 1D5V_S5

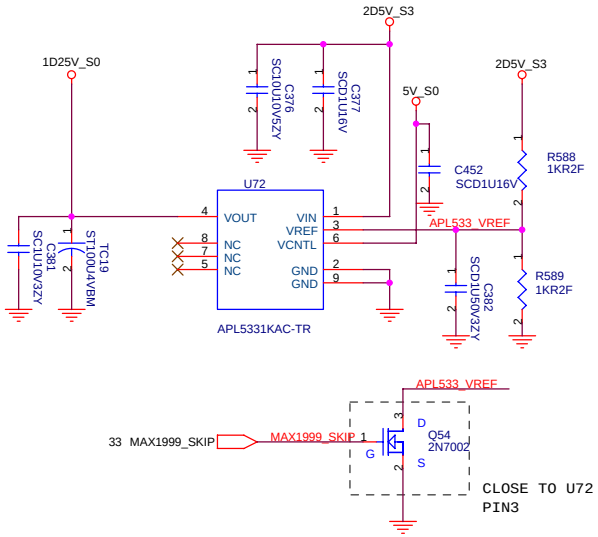


3D3V_S0 → 1D5V_S0

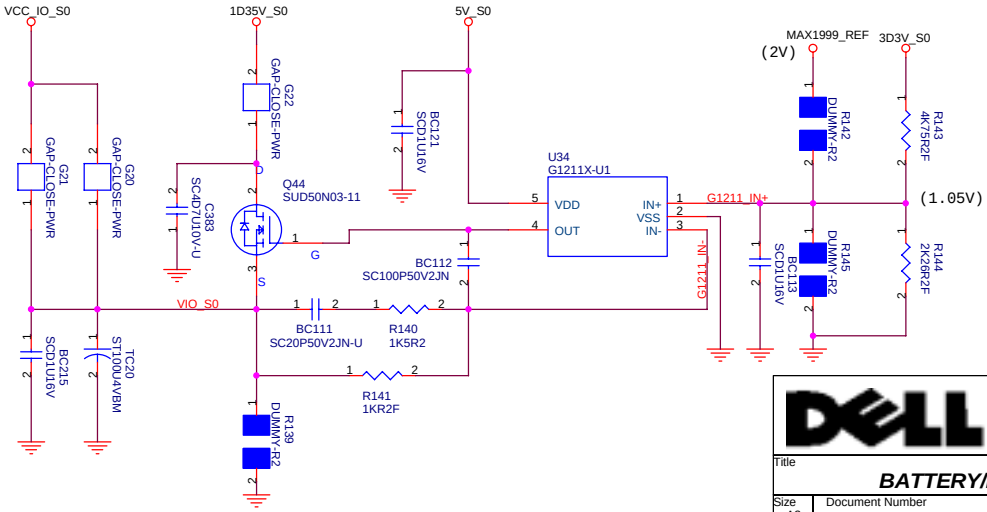


Vo=1.25*((R626+R629)/R626) = 1.5V

2D5V_S3 → 1D25V_S0



1D35V_S0 → VCC_IO_S0(1.05V)



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Title: BATTERY/LDO/Adaptor In		
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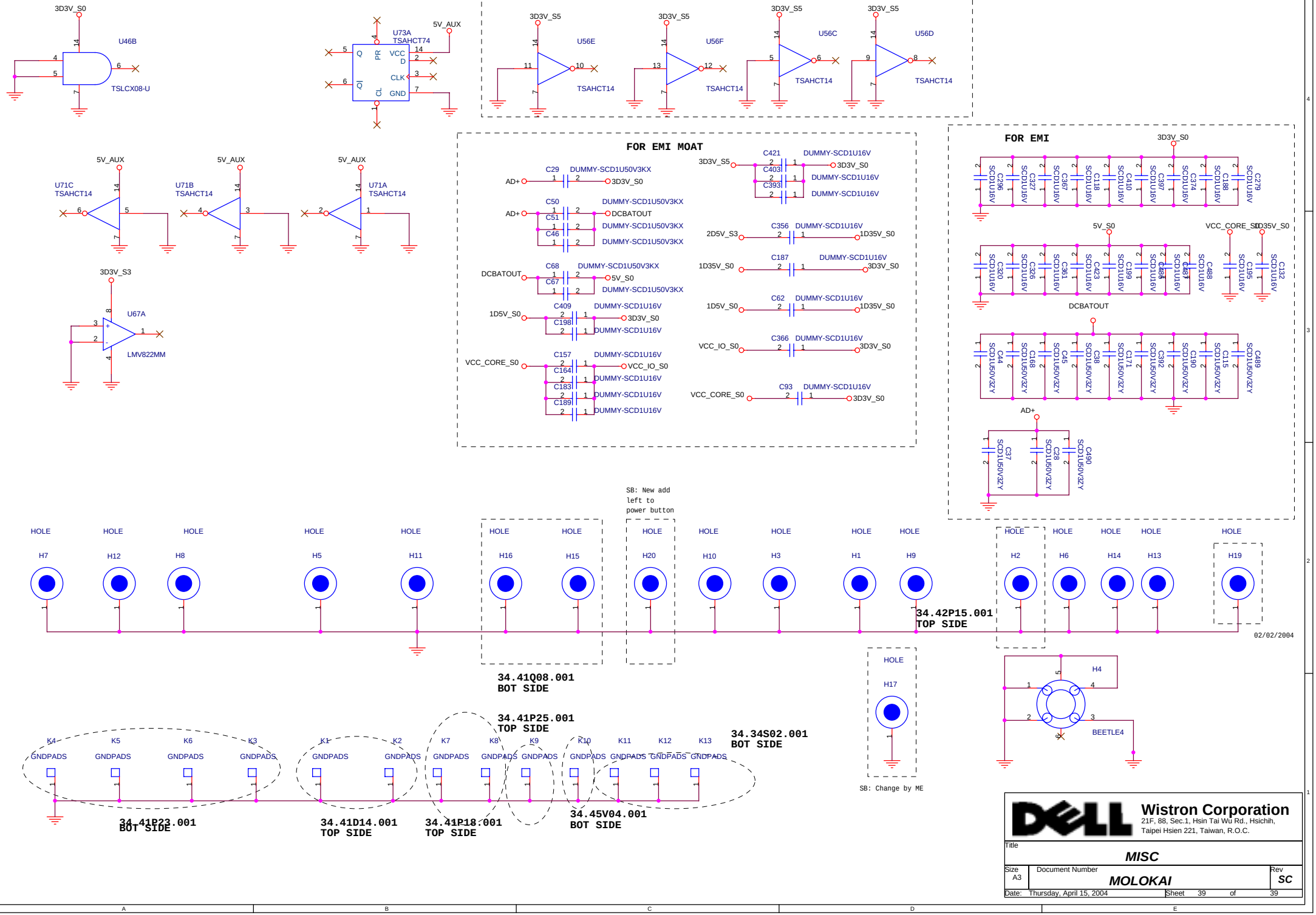

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