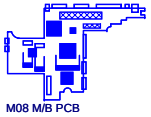
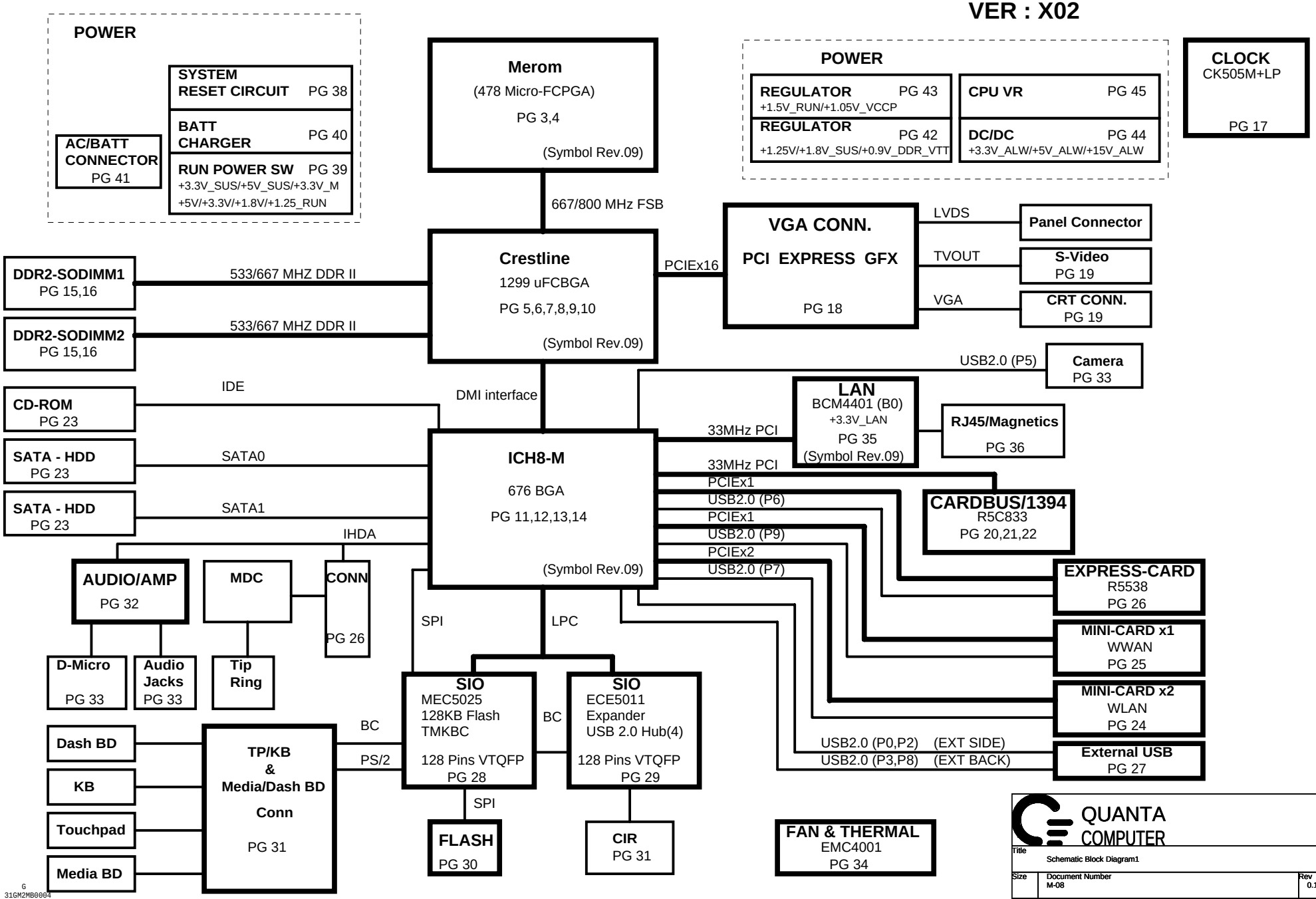
Kevin.Liou



Corsica\Gilligan - DISCRETE

VER : X02



QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number M-08	Rev 0.1
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C G
31FM5MB0011 31GM2MB0004
41FM5SS0017 41GM2SS0000

INDEX

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43-44	Battery Selector & Charger	
45	DDR2_1.8VSUS, 0.9V	
46	1.5VSUS,1.05V(VTT)	
47	1.25V,1.05VM	
48	CPU_MAX8786(3phase)	
49	D/D Power	
50	RUN Power Switch	
51	VGA DC/DC	
52	DCIN/Batt Conn.	
53	PAD& SCREW	
54	EMI CAP	

Power & Ground

Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (19V)	
PBATT+		MAIN BATTERY + (10~17V)	
PBATT+		SECOND BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~19V)	
RTC_PWR3_3V		RTC & +3.3V_RTC_LDO(3.3V)	
+VCC_CORE		CPU CORE POWER (1.5V)	RUNPWROK
+15V_ALW		LARGE POWER (15V)	SUS_ON
+3.3V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+3.3V_SUS		SLP_S5# CTRLD POWER	SUS_ENABLE
+3.3V_ALW		8051 POWER (3.3V)	ALWON/THERM_STP#
+5V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+5V_SUS		SLP_S5# CTRLD POWER	SUS_ON
+5V_HDD		HDD POWER (5V)	+5V_RUN
+5V_MOD		MODULE POWER (5V)	HDDC_EN
+5V_ALW		LCD/CHARGE POWER (5V)	
+VDDA		AUDIO ANALOG POWER (5V)	AUDIO_AVDD_ON
+1.5V_RUN		CALISTOGA/ICH7 POWER	RUN_ON
+1.05V_VCCP		CPU/CALISTOGA/ICH7 POWER	RUN_ON
+1_8V_SUS		SODIMM POWER	SUSPWROK_5V
+1.8V_RUN		SDVO POWER	RUN_ON
+0.9V_DDR_VTT		SODIMM POWER	RUN_ON
+3.3V_LAN		LAN POWER	AUX_EN
GND	ALL PAGES	DIGITAL GROUND	
AGND_ISL6260		CPU GND	
AGND_TPS51120		DC/DC POWER GND	
AGND1		VTT POWER GND	
AGND2		VTT POWER GND	
8731AGND		CHARGER GND	

QUANTA COMPUTER

Title	Index, DNI, Power & Ground	
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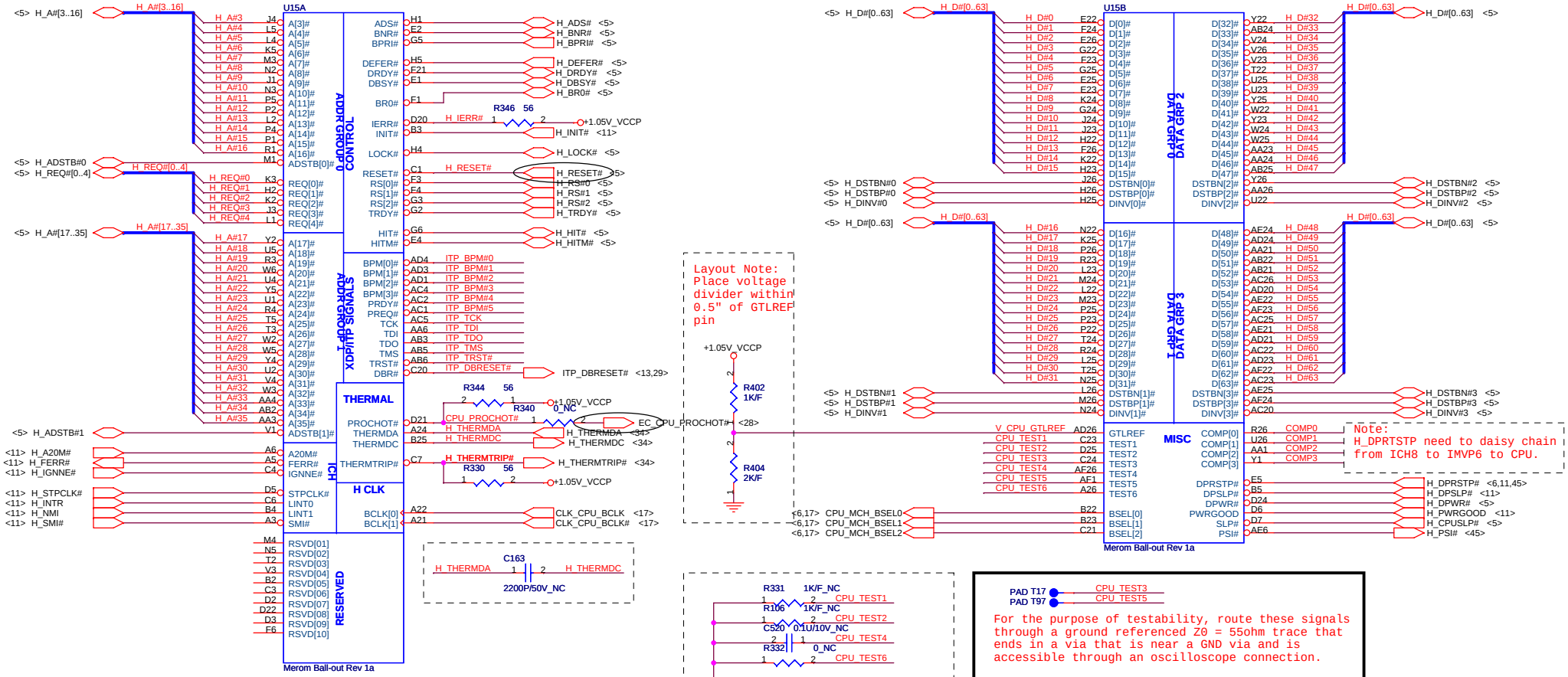
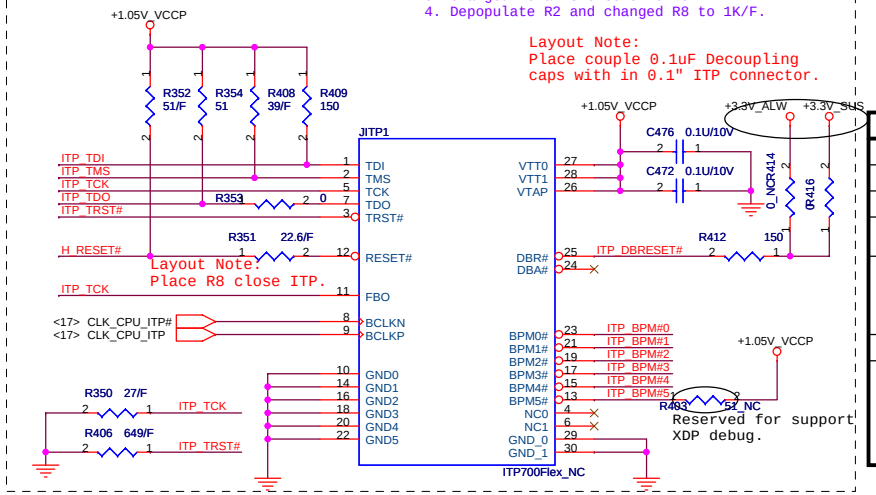


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

Populate ITP700Flex for bringup

For Support XDP:
1. ITP_BPM#5 need PU 51ohms to +1.05V_VCCP.
2. Change R4 & R361 to 51 ohms.
3. Changed R6 & R346 to 51 ohms.
4. Depopulate R2 and changed R8 to 1K/F.

Layout Note: Place couple 0.1uF Decoupling caps with in 0.1" ITP connector.



ITP700 layout guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-down near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near ITP
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

DELL CONFIDENTIAL/PROPRIETARY

Title: Merom Processor (HOST BUS)

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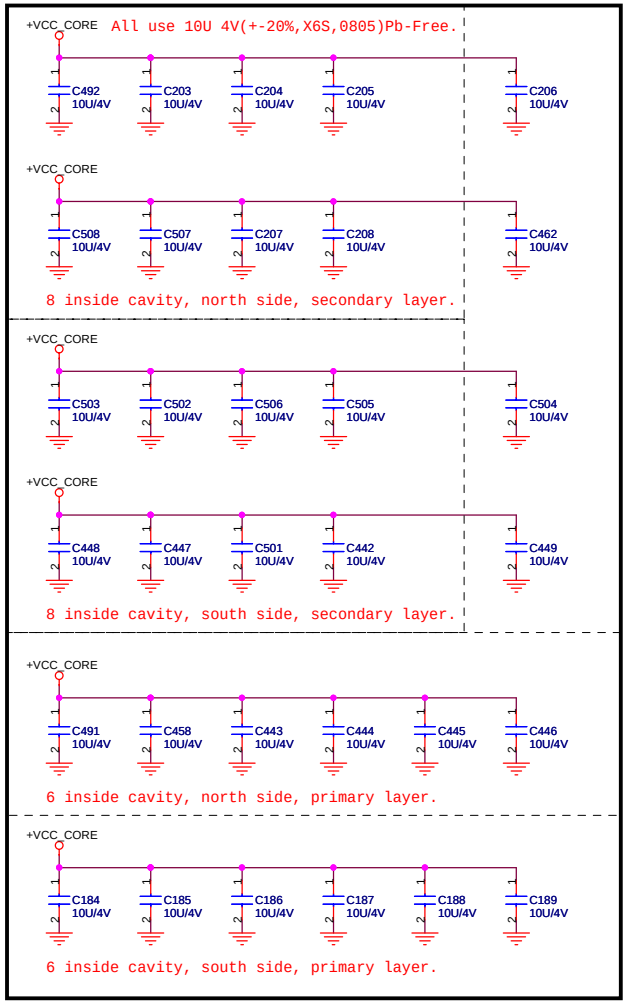

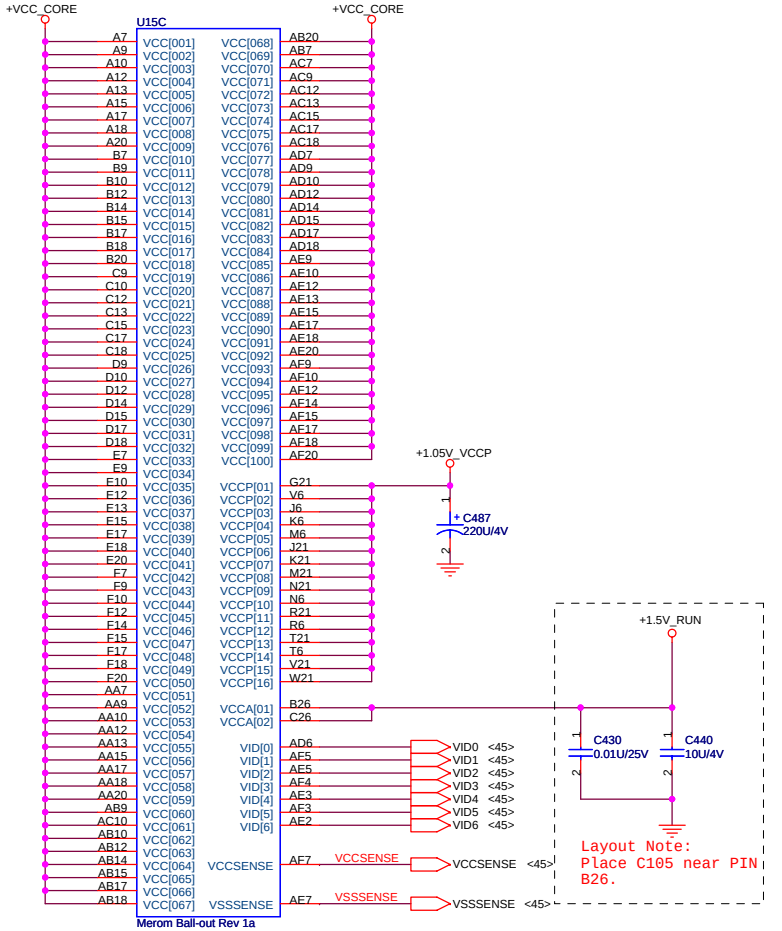

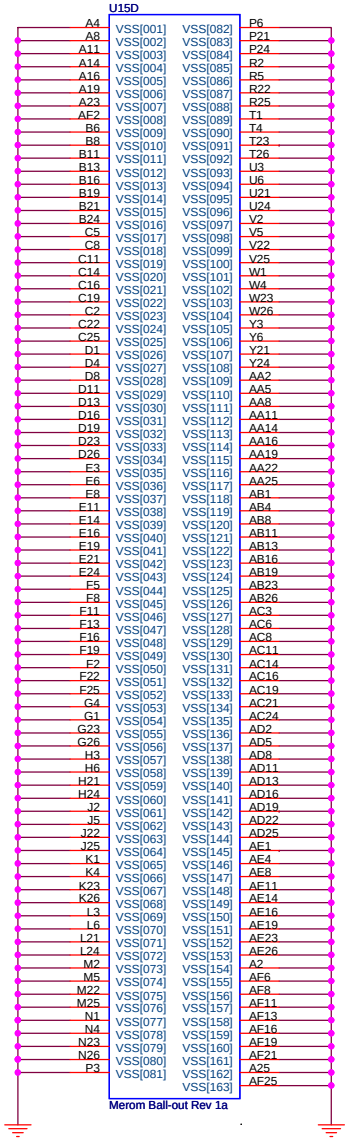

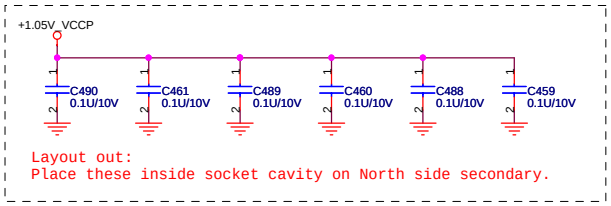

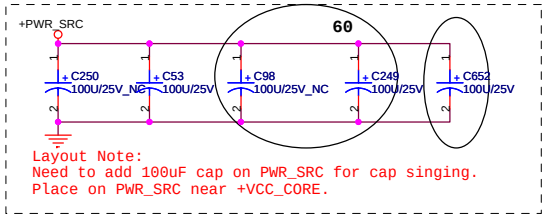

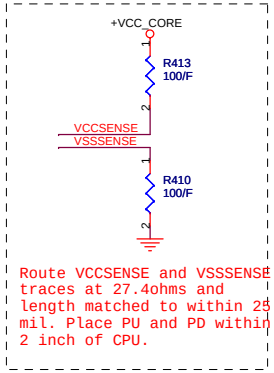

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Title	Merom Processor (POWER)	
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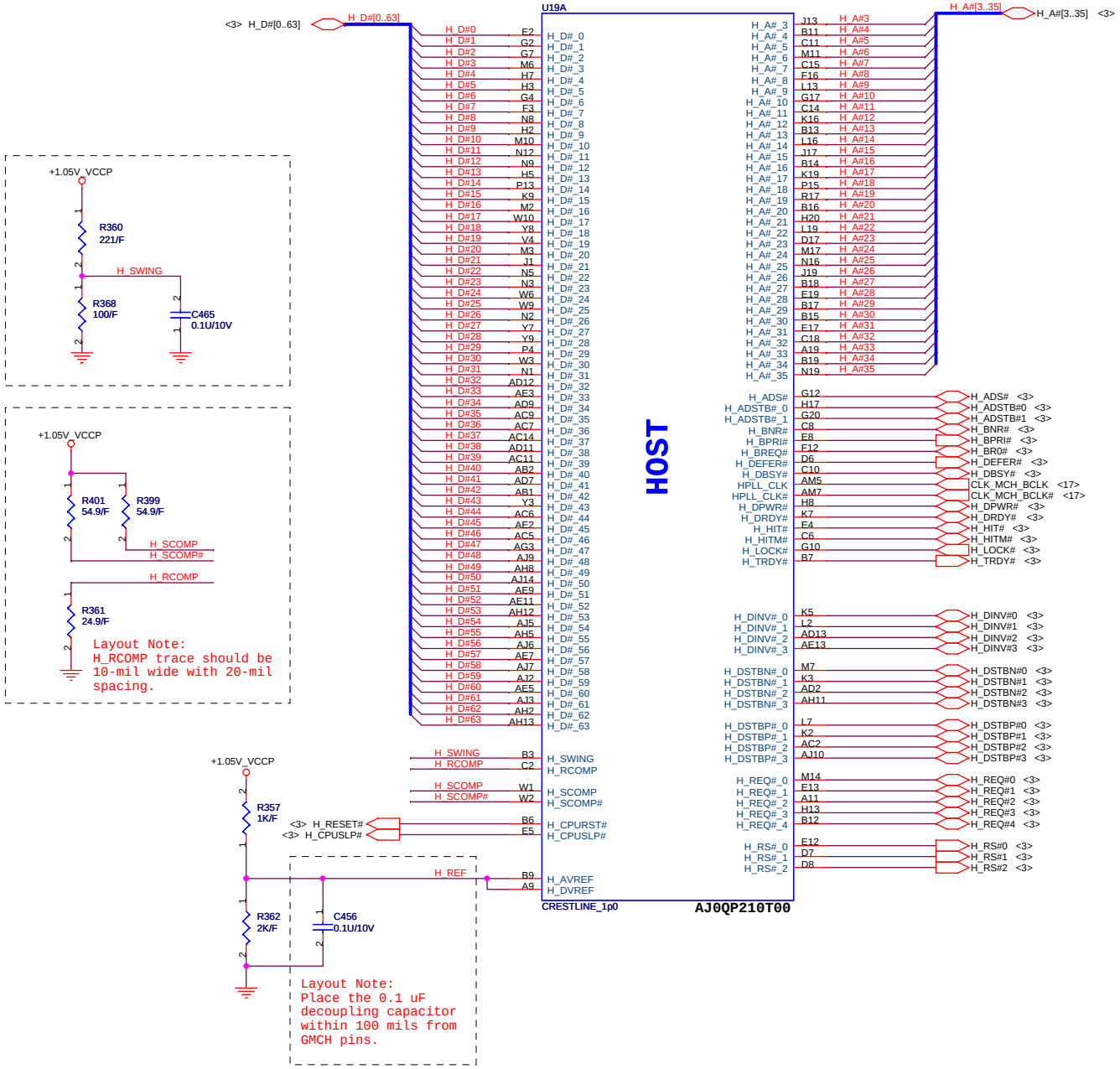

DELL CONFIDENTIAL/PROPRIETARY

Title	Crestline (HOST)		
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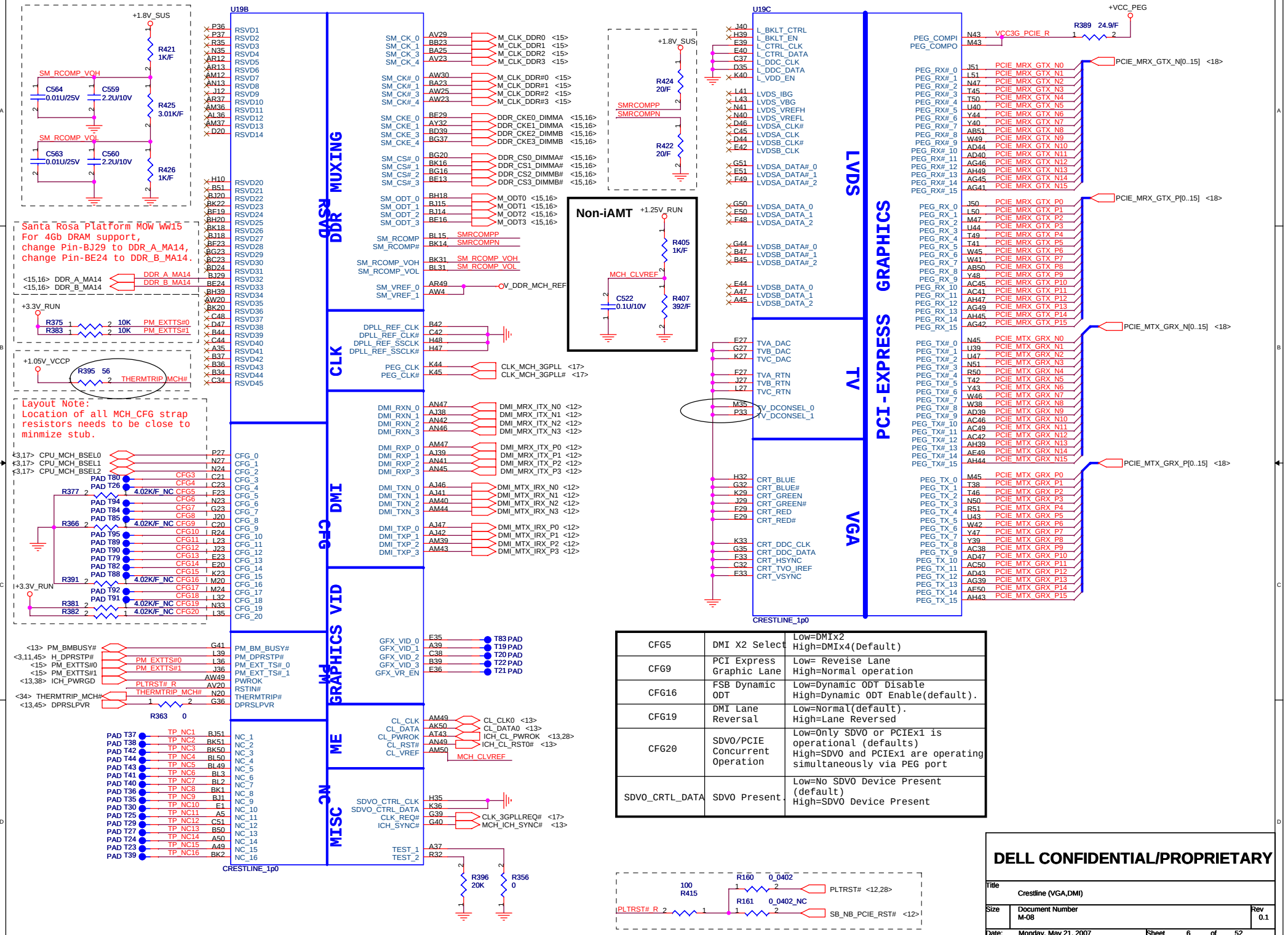

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

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Title: Crestline (VGA,DMI)

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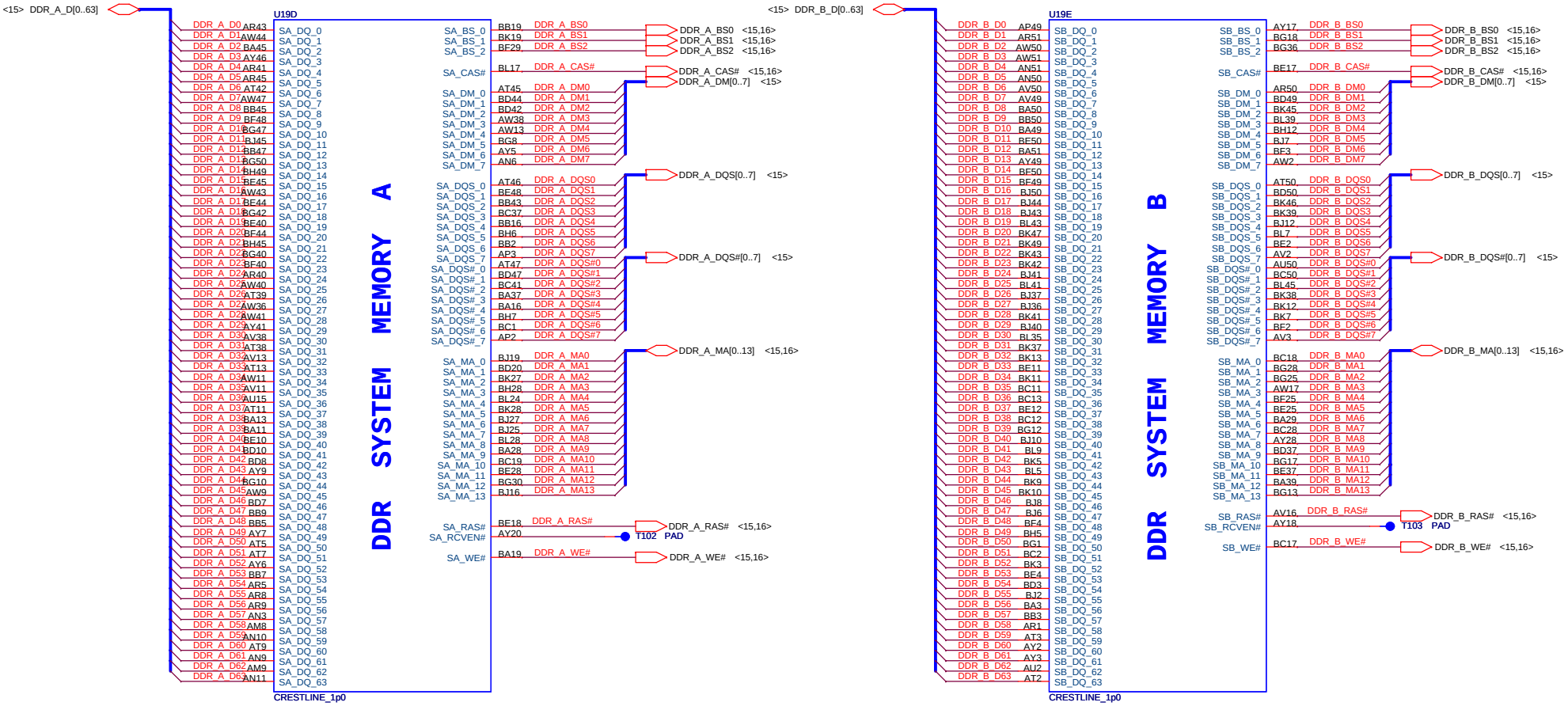

DELL CONFIDENTIAL/PROPRIETARY

Title	Crestline (DDR2)		
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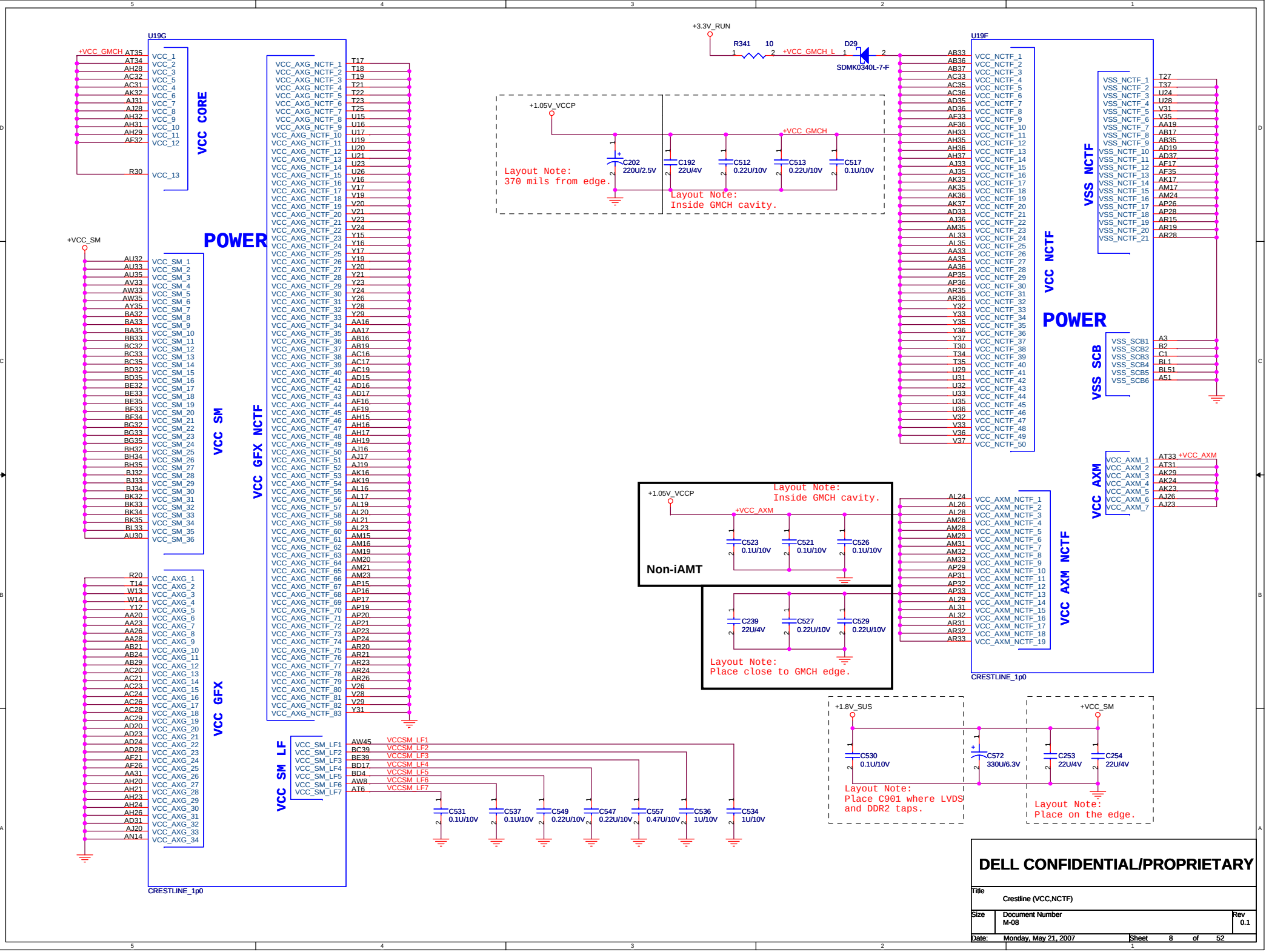

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Title	Crestline (VCC,NCTF)		
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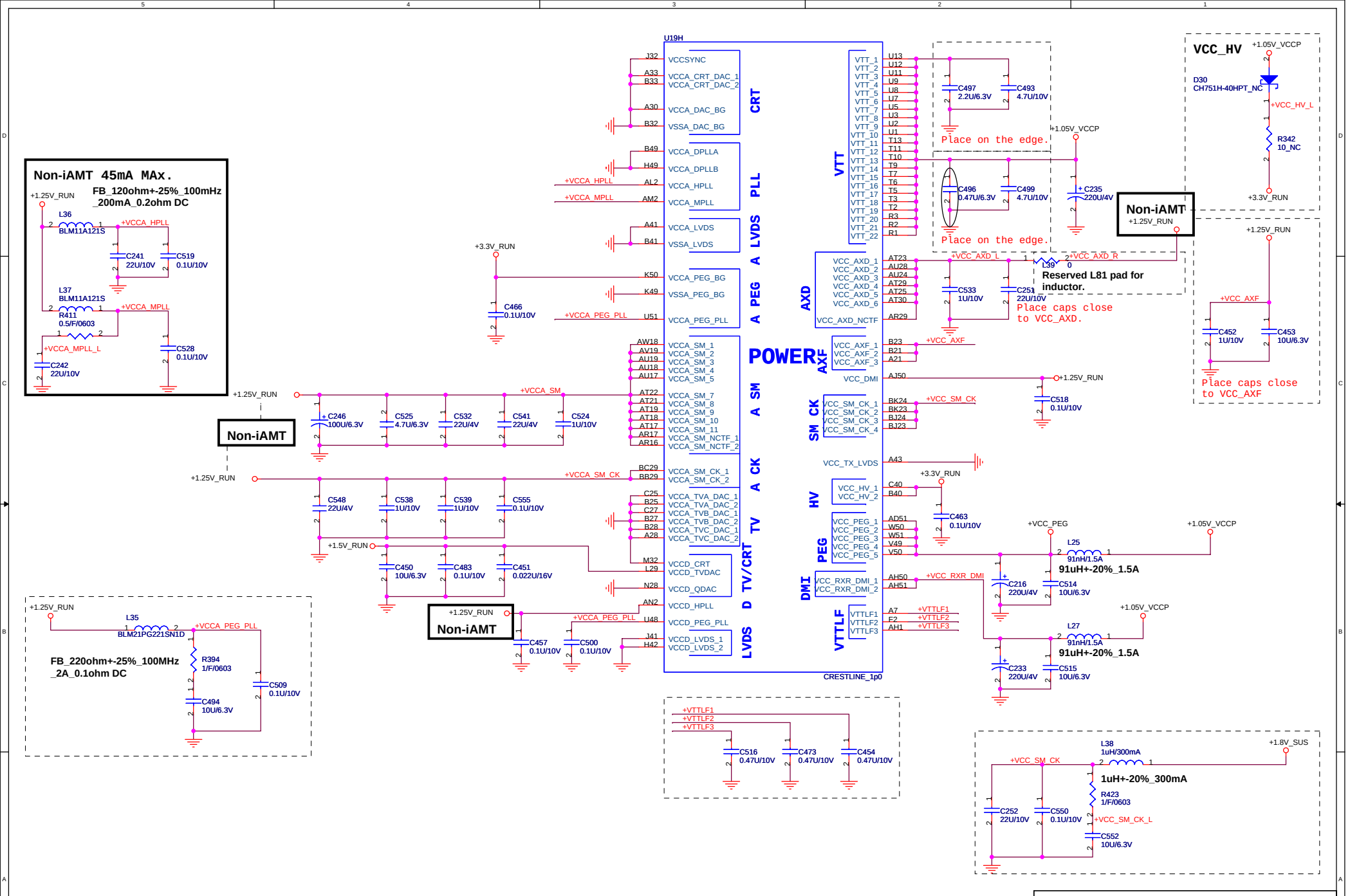

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Title	Crestline (POWER)	
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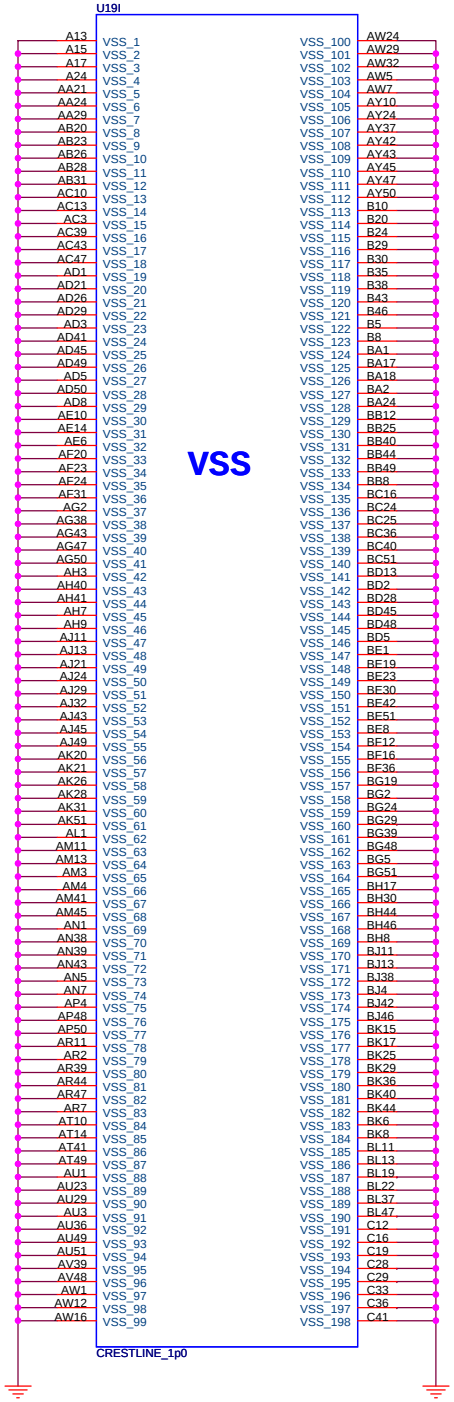

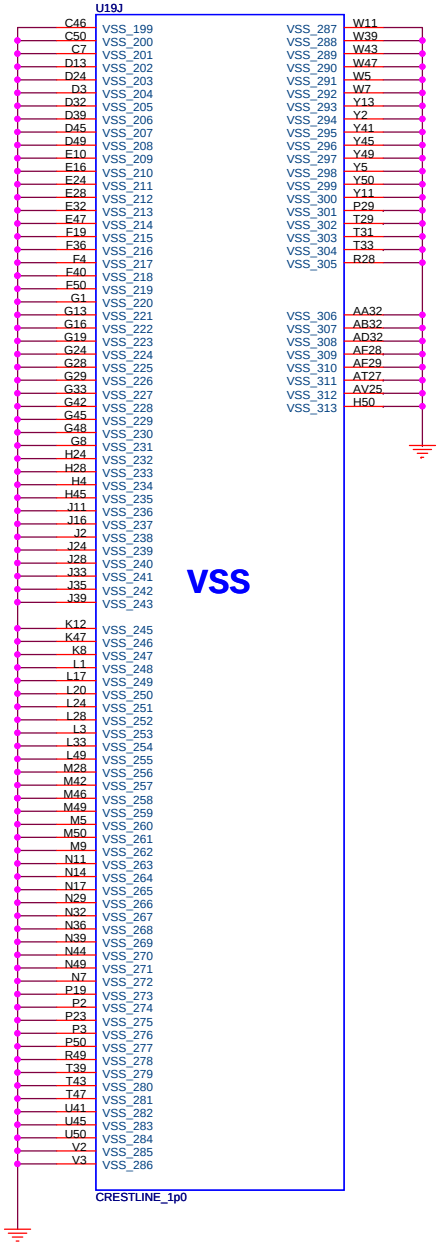

DELL CONFIDENTIAL/PROPRIETARY

Title	Crestline (VSS)		
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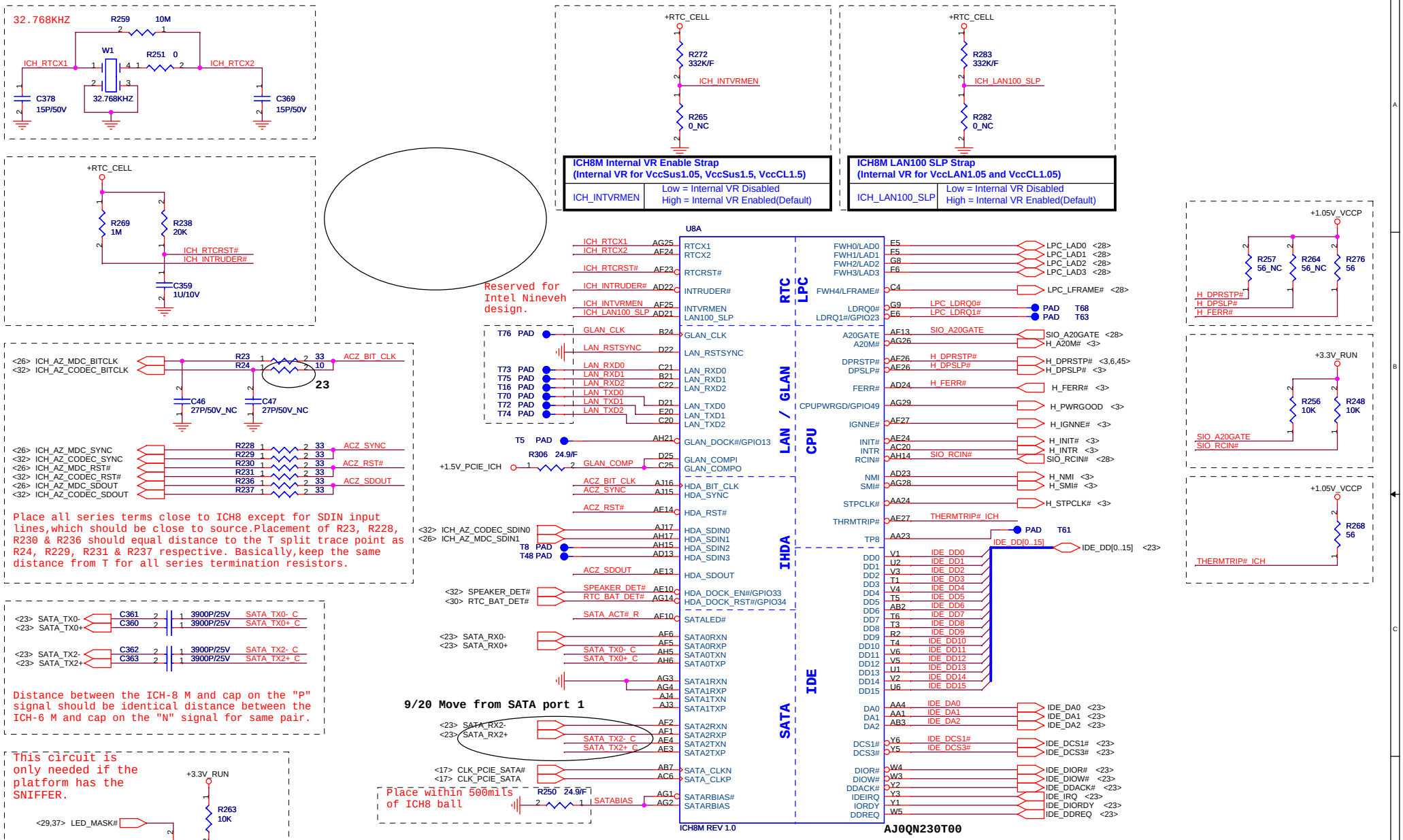

DELL CONFIDENTIAL/PROPRIETARY

Title	ICH8-M (CPU,IDE,SATA,LPC,AC97,LAN)
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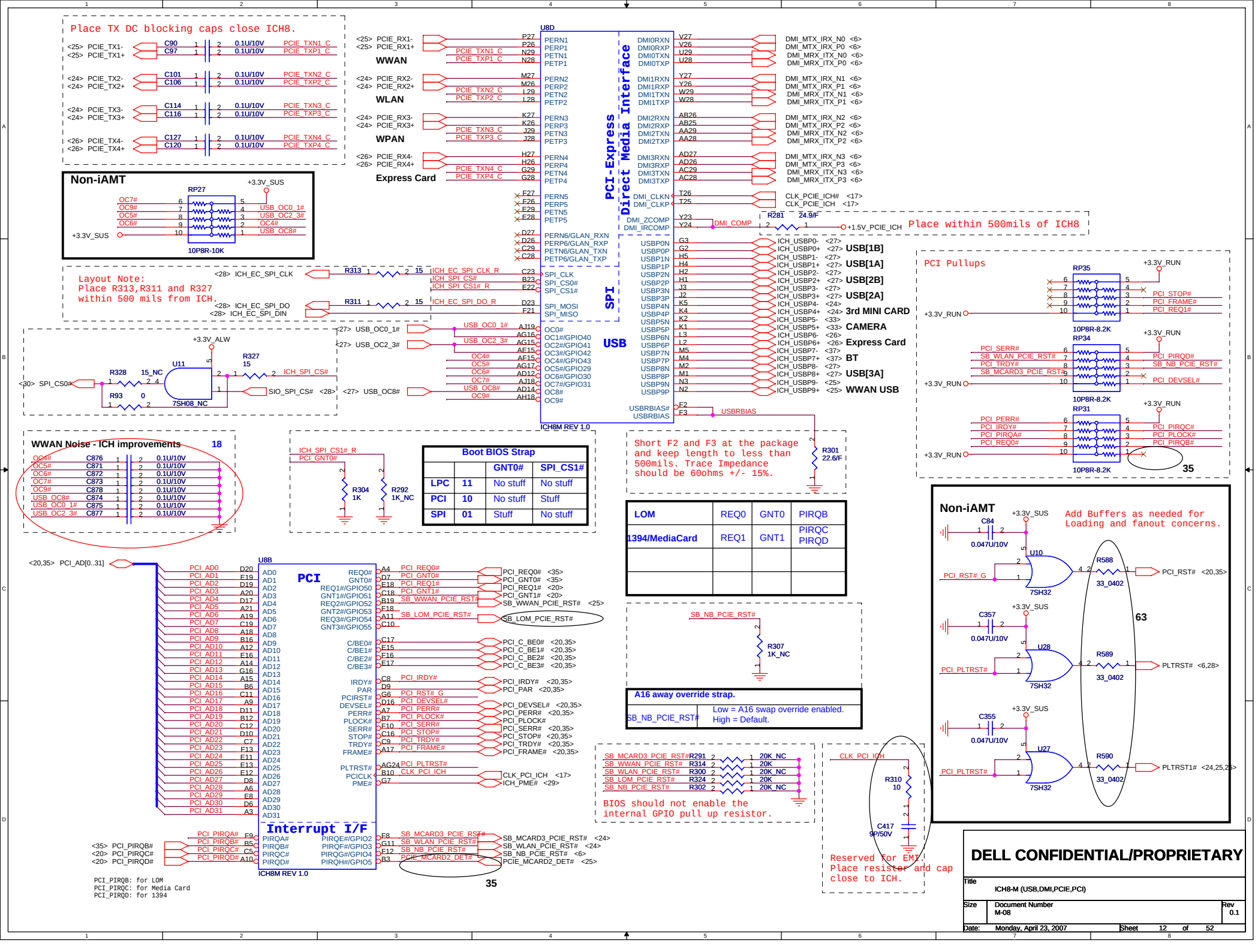
Place TX DC blocking caps close ICH8.
U8D
PCI-Express Direct Media Interface
WWAN
WLAN
WPAN
Express Card
Non-iAMT
RP27
10P8R-10K
Place within 500mils of ICH8
USB[1B]
USB[1A]
USB[2B]
USB[2A]
3rd MINI CARD
CAMERA
Express Card
BT
USB[3A]
WWAN USB
Layout Note:
Place R313,R311 and R327
within 500 mils from ICH.
SPI
USB
ICH8M REV 1.0
PCI Pullups
RP35
RP34
RP31
10P8R-8.2K
35
WWAN Noise - ICH improvements
18
Boot BIOS Strap
GNT0#
SPI_CS1#
LPC 11 No stuff No stuff
PCI 10 No stuff Stuff
SPI 01 Stuff No stuff
Short F2 and F3 at the package
and keep length to less than
500mils. Trace Impedance
should be 60ohms +/- 15%.
LOM REQ0 GNT0 PIRQB
1394/MediaCard REQ1 GNT1 PIRQC PIRQD
Non-iAMT
Add Buffers as needed for
Loading and fanout concerns.
63
PCI
Interrupt I/F
ICH8M REV 1.0
35
A16 away override strap.
SB_NB_PCIE_RST#
Low = A16 swap override enabled.
High = Default.
BIOS should not enable the
internal GPIO pull up resistor.
Reserved for EMI.
Place resister and cap
close to ICH.
PCI_PIRQB: for LOM
PCI_PIRQC: for Media Card
PCI_PIRQD: for 1394
DELL CONFIDENTIAL/PROPRIETARY
Title
ICH8-M (USB,DMI,PCIE,PCI)
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0.1
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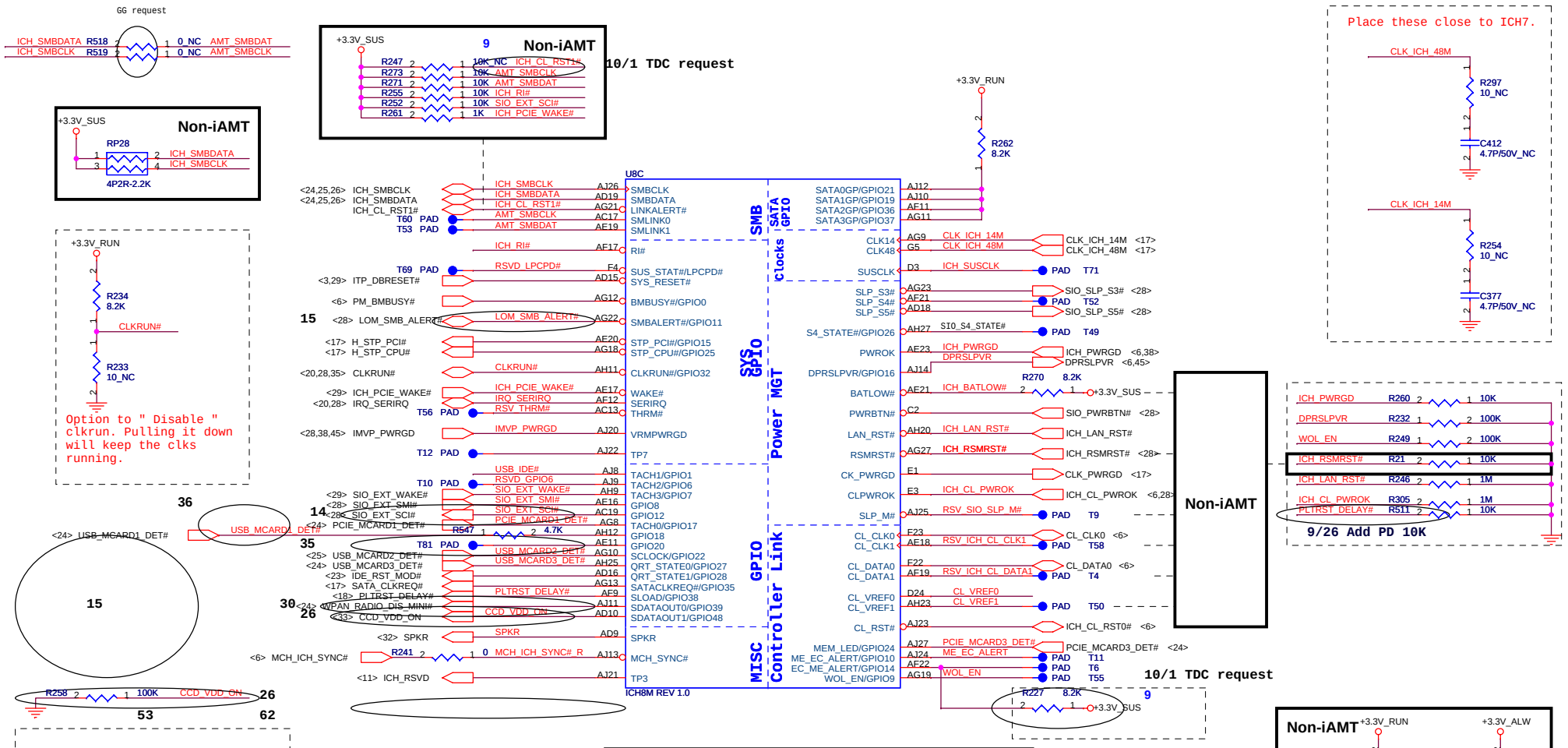

DELL CONFIDENTIAL/PROPRIETARY

Title	ICH8-M (PM,GPIO,SMB,CL)	
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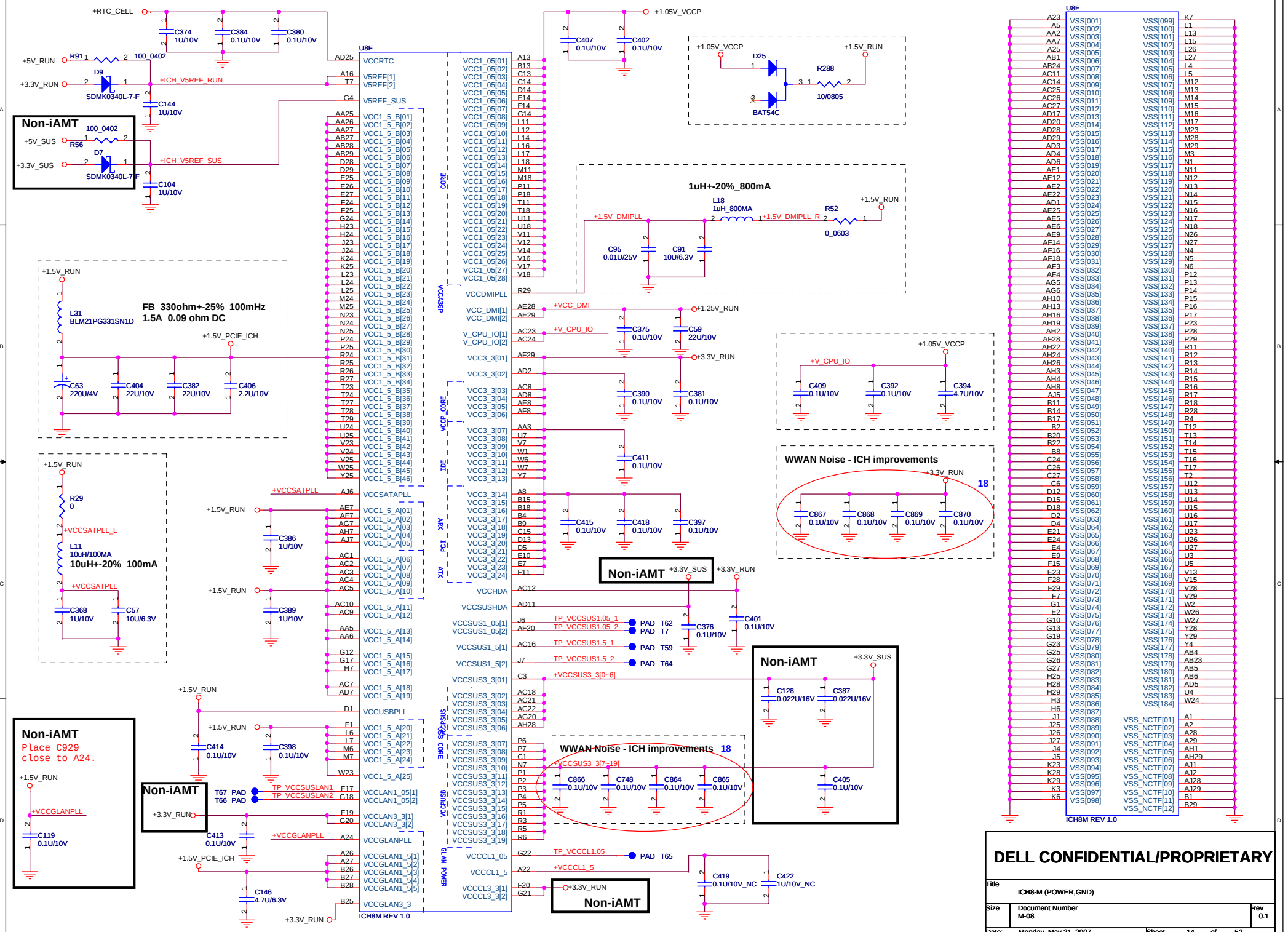
U8F
ICH8M REV 1.0
U8E
ICH8M REV 1.0
Non-iAMT
Place C929
close to A24.
WWAN Noise - ICH improvements
1uH+-20%_800mA
FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC
10uH+-20%_100mA
DELL CONFIDENTIAL/PROPRIETARY
Title
ICH8-M (POWER,GND)
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A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.

TOP

JDIM1

PC4800 DDR2 SDRAM SO-DIMM (200P)

+1.8V_SUS, V_DDR_MCH_REF

DDR_A_DM[0..7] <7>
DDR_A_D[0..63] <7>
DDR_A_DQS[0..7] <7>
DDR_A_DQS#[0..7] <7>
DDR_A_MA[0..14] <6,7,16>

V_DDR_MCH_REF: C277 0.1U/10V, C276 2.2U/6.3V

M_CLK_DDR0 <6>
M_CLK_DDR#0 <6>
PM_EXTTS#0 <6>
DDR_CKE1_DIMMA <6,16>
M_ODT0 <6,16>
M_CLK_DDR1 <6>
M_CLK_DDR#1 <6>

<6,16> DDR_CKE0_DIMMA
<7,16> DDR_A_BS2
<7,16> DDR_A_BS0
<7,16> DDR_A_WE#
<7,16> DDR_A_CAS#
<6,16> DDR_CS1_DIMMA#
<6,16> M_ODT1
<13> MEM_SDATA
<13> MEM_SCLK
+3.3V_RUN

FOX_AS0A426-N2RN-7F

Non-iAMT

SMbus address A0

CLOCK 0,1
CKE 0,1

R169 10K, R170 10K

+3.3V_RUN, Non-iAMT: C580 2.2U/6.3V, C579 0.1U/10V

Non-iAMT

BOT

JDIM2

PC4800 DDR2 SDRAM SO-DIMM (200P)

+1.8V_SUS, V_DDR_MCH_REF

DDR_B_DM[0..7] <7>
DDR_B_D[0..63] <7>
DDR_B_DQS[0..7] <7>
DDR_B_DQS#[0..7] <7>
DDR_B_MA[0..14] <6,7,16>

V_DDR_MCH_REF: C274 0.1U/10V, C275 2.2U/6.3V

M_CLK_DDR2 <6>
M_CLK_DDR#2 <6>
PM_EXTTS#1 <6>
DDR_CKE3_DIMMB <6,16>
M_ODT2 <6,16>
M_CLK_DDR3 <6>
M_CLK_DDR#3 <6>

<6,16> DDR_CKE2_DIMMB
<7,16> DDR_B_BS2
<7,16> DDR_B_BS0
<7,16> DDR_B_WE#
<7,16> DDR_B_CAS#
<6,16> DDR_CS3_DIMMB#
<6,16> M_ODT3
DDR_B_BS1 <7,16>
DDR_B_RAS# <7,16>
DDR_CS2_DIMMB# <6,16>
+3.3V_RUN

FOX_ AS0A426-N2SN-7F

SMbus address A4

CLOCK 2,3
CKE 2,3

R449 10K, R448 10K

Non-iAMT

Place these Caps near So-Dimm1.
C270 2.2U/6.3V, C269 2.2U/6.3V, C279 2.2U/6.3V, C280 2.2U/6.3V, C281 2.2U/6.3V

Place these Caps near So-Dimm2.
C588 2.2U/6.3V, C575 2.2U/6.3V, C586 2.2U/6.3V, C587 2.2U/6.3V, C576 2.2U/6.3V

Place these Caps near So-Dimm1.
C272 0.1U/10V, C278 0.1U/10V, C271 0.1U/10V, C273 0.1U/10V

Place these Caps near So-Dimm2.
C574 0.1U/10V, C584 0.1U/10V, C578 0.1U/10V, C577 0.1U/10V

+3.3V_RUN, Non-iAMT: C264 2.2U/6.3V, C268 0.1U/10V

DELL CONFIDENTIAL/PROPRIETARY

Title	DDR2 SO-DIMM (200P) X 2	
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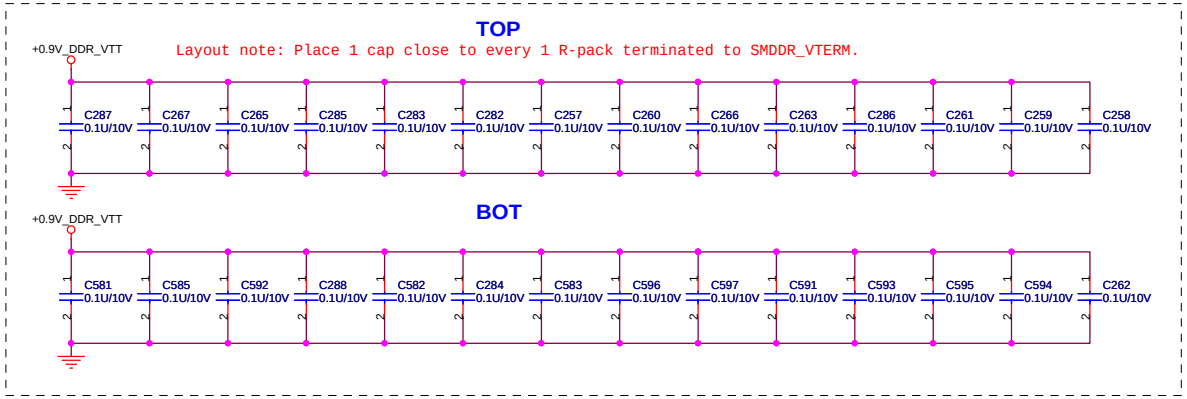

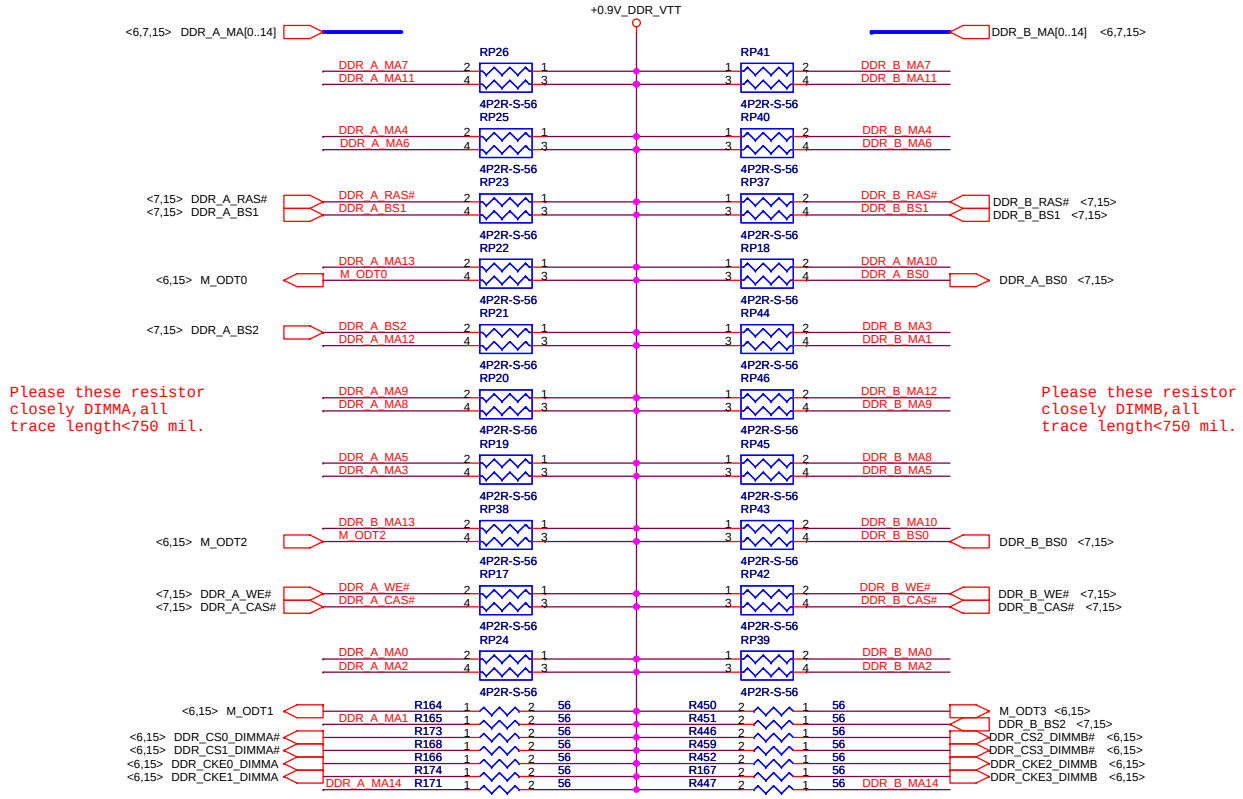

Please these resistor closely DIMMA,all trace length<750 mil.

Please these resistor closely DIMMB,all trace length<750 mil.

DELL CONFIDENTIAL/PROPRIETARY

Title	DDR2 RES ARRAY	
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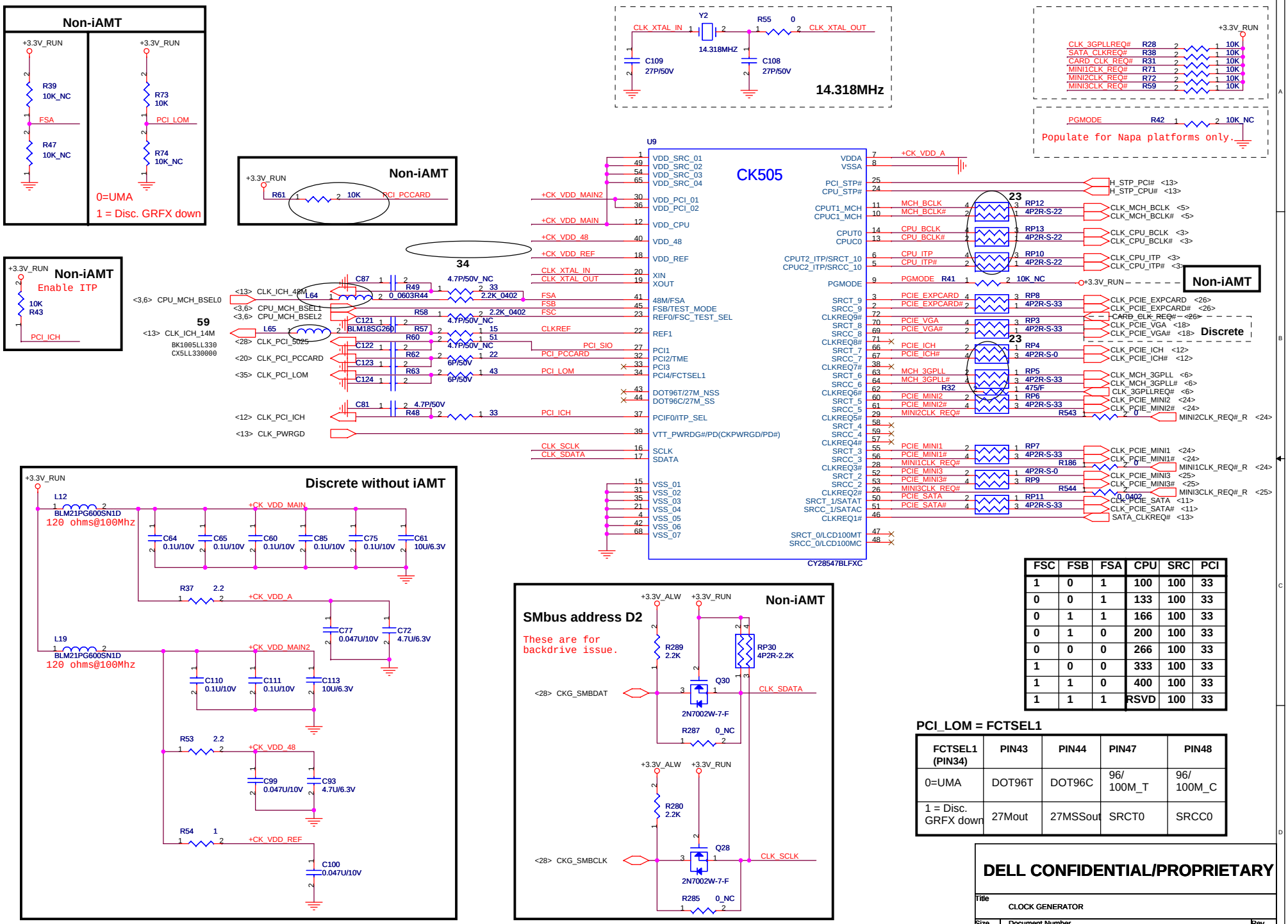

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0

DELL CONFIDENTIAL/PROPRIETARY

Title: CLOCK GENERATOR

Size: | Document Number: M-08 | Rev: 0.1

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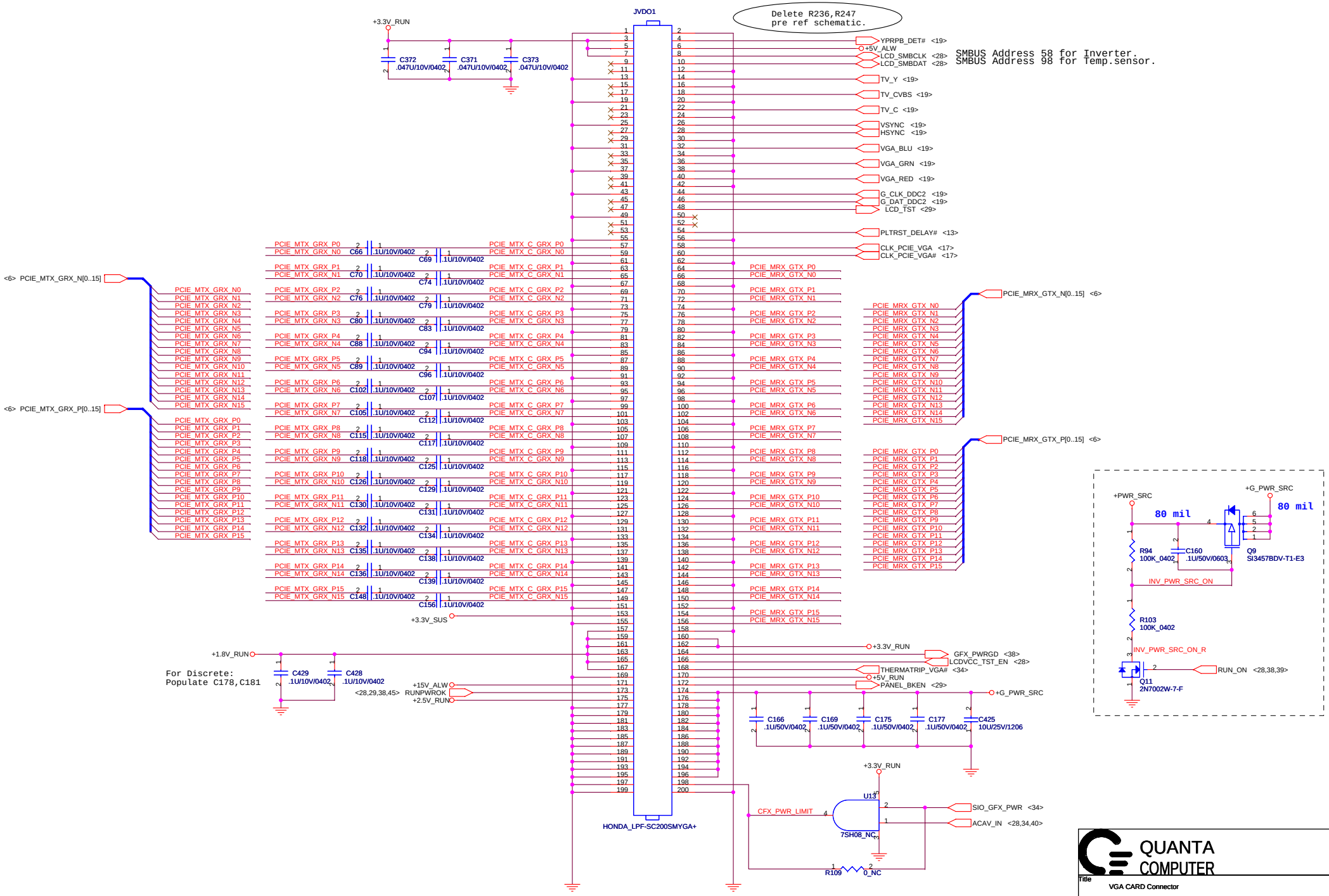
YPRPB_DET: SIGNAL FROM SVIDEO CONNECTOR,
TO SWICH TO COMPONENT OUT.

Delete R236,R247
pre ref schematic.

SMBUS Address 58 for Inverter.
SMBUS Address 98 for Temp.sensor.



QUANTA COMPUTER

Title	VGA CARD Connector	
Size	Document Number FM1	Rev 0.1
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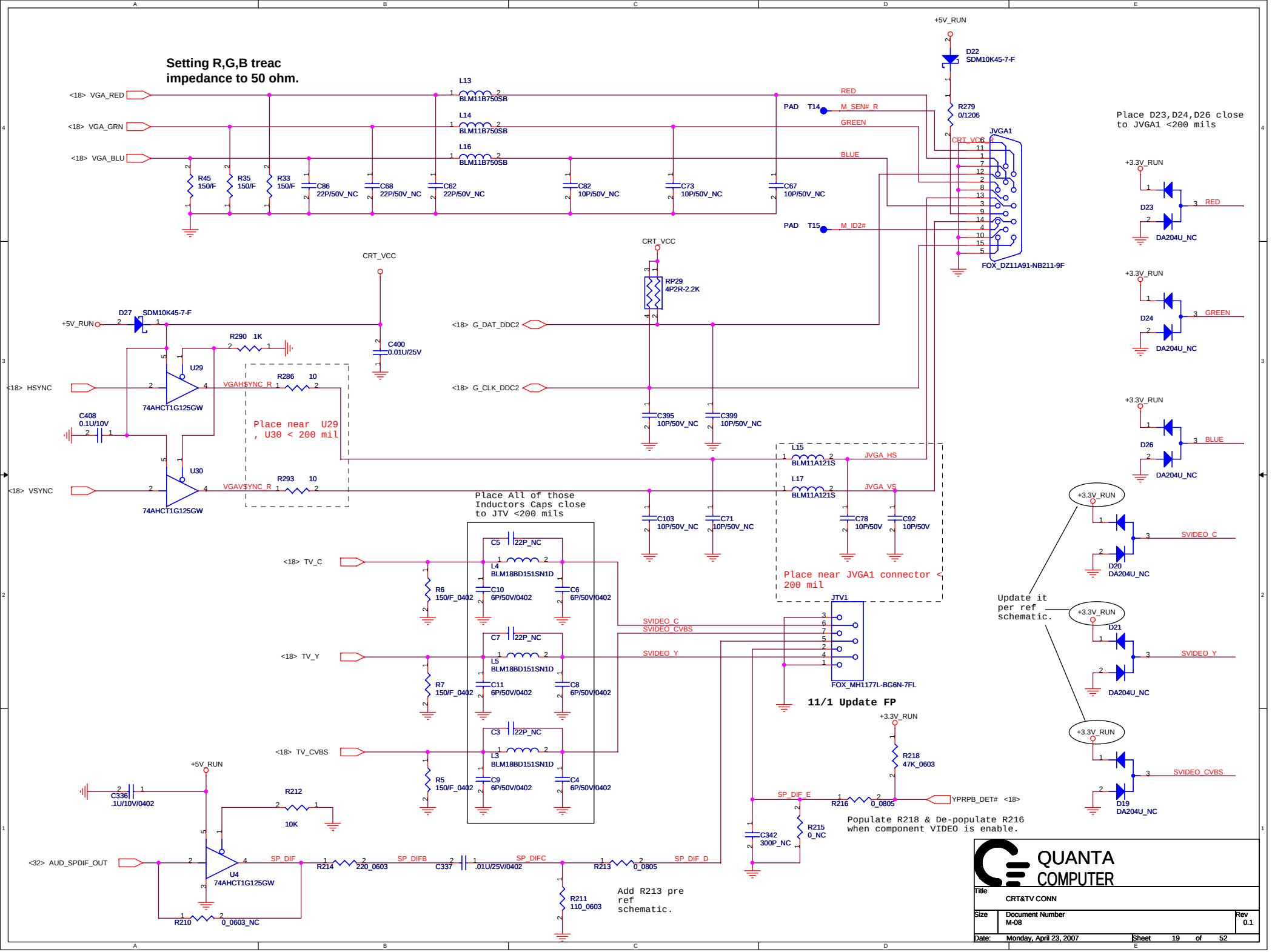
Setting R,G,B treac impedance to 50 ohm.
<18> VGA_RED
<18> VGA_GRN
<18> VGA_BLU
L13 BLM11B750SB
L14 BLM11B750SB
L16 BLM11B750SB
R45 150/F
R35 150/F
R33 150/F
C86 22P/50V_NC
C68 22P/50V_NC
C62 22P/50V_NC
C82 10P/50V_NC
C73 10P/50V_NC
C67 10P/50V_NC
RED
GREEN
BLUE
PAD T14
M_SEN# R
PAD T15
M_ID2#
+5V_RUN
D22 SDM10K45-7-F
R279 0/1206
JVGA1
CRT_VC6
FOX_DZ11A91-NB211-9F
Place D23,D24,D26 close to JVGA1 <200 mils
+3.3V_RUN
D23
DA204U_NC
D24
DA204U_NC
D26
DA204U_NC
CRT_VCC
RP29 4P2R-2.2K
<18> G_DAT_DDC2
<18> G_CLK_DDC2
C395 10P/50V_NC
C399 10P/50V_NC
C400 0.01U/25V
D27 SDM10K45-7-F
R290 1K
U29
74AHCT1G125GW
<18> HSYNC
VGAHSYNC_R
R286 10
C408 0.1U/10V
U30
74AHCT1G125GW
<18> VSYNC
VGAVSYNC_R
R293 10
Place near U29 , U30 < 200 mil
L15 BLM11A121S
L17 BLM11A121S
JVGA_HS
JVGA_VS
C78 10P/50V
C92 10P/50V
C103 10P/50V_NC
C71 10P/50V_NC
Place near JVGA1 connector < 200 mil
Place All of those Inductors Caps close to JTV <200 mils
<18> TV_C
<18> TV_Y
<18> TV_CVBS
C5 22P_NC
L4 BLM18BD151SN1D
C10 6P/50V/0402
C6 6P/50V/0402
R6 150/F_0402
C7 22P_NC
L5 BLM18BD151SN1D
C11 6P/50V/0402
C8 6P/50V/0402
R7 150/F_0402
C3 22P_NC
L3 BLM18BD151SN1D
C9 6P/50V/0402
C4 6P/50V/0402
R5 150/F_0402
SVIDEO_C
SVIDEO_CVBS
SVIDEO_Y
JTV1
FOX_MH1177L-BG6N-7FL
11/1 Update FP
Update it per ref schematic.
D20 DA204U_NC
D21
DA204U_NC
D19 DA204U_NC
SVIDEO_C
SVIDEO_Y
SVIDEO_CVBS
+3.3V_RUN
R218 47K_0603
SP_DIF_E
R216 0_0805
YPRPB_DET# <18>
R215 0_NC
C342 300P_NC
Populate R218 & De-populate R216 when component VIDEO is enable.
C336 .1U/10V/0402
R212 10K
<32> AUD_SPDIF_OUT
U4 74AHCT1G125GW
SP_DIF
R214 220_0603
SP_DIFB
C337 .01U/25V/0402
SP_DIFC
R213 0_0805
SP_DIF_D
R211 110_0603
Add R213 pre ref schematic.
R210 0_0603_NC
QUANTA COMPUTER
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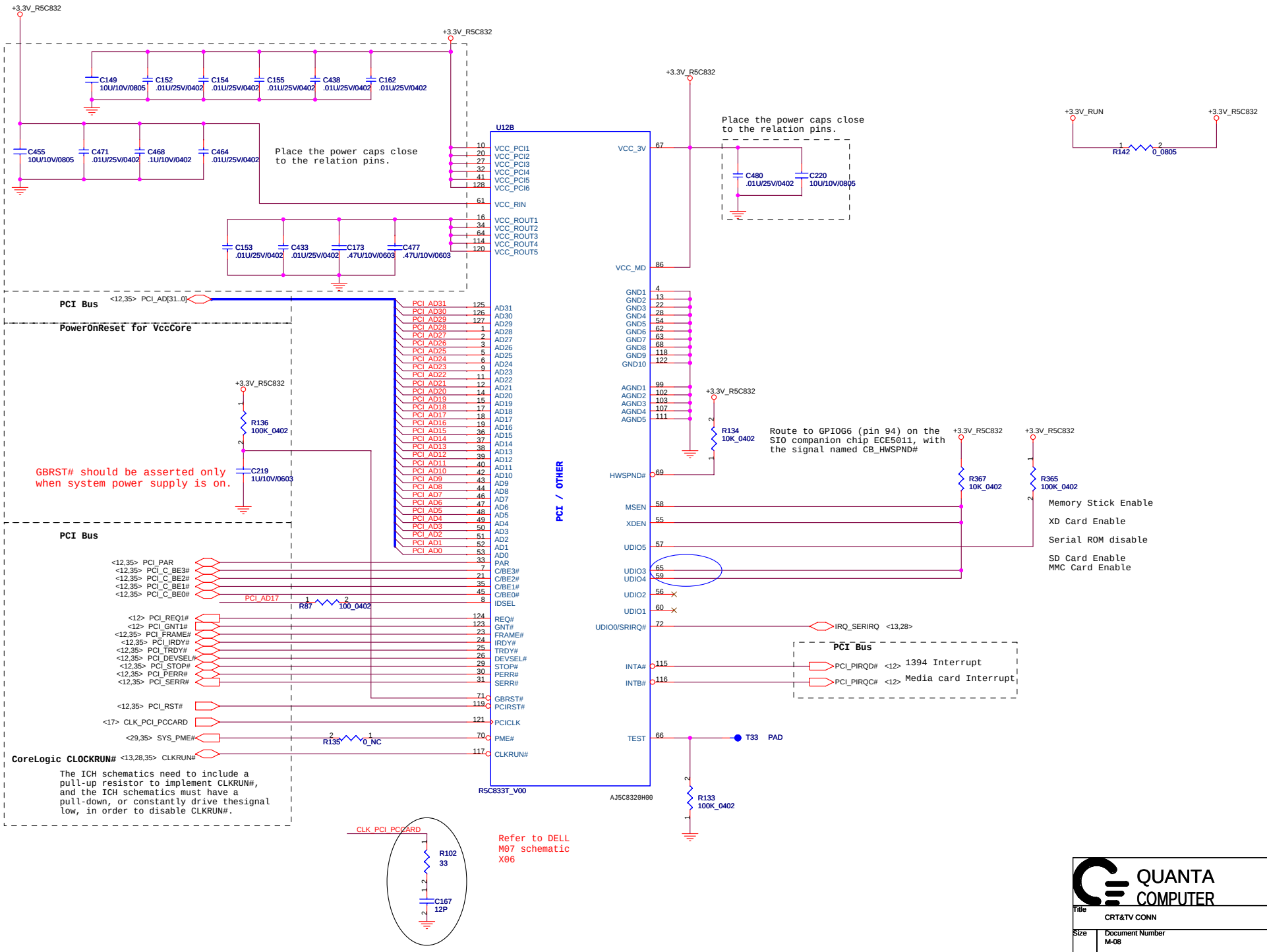

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Title	CRT&TV CONN	
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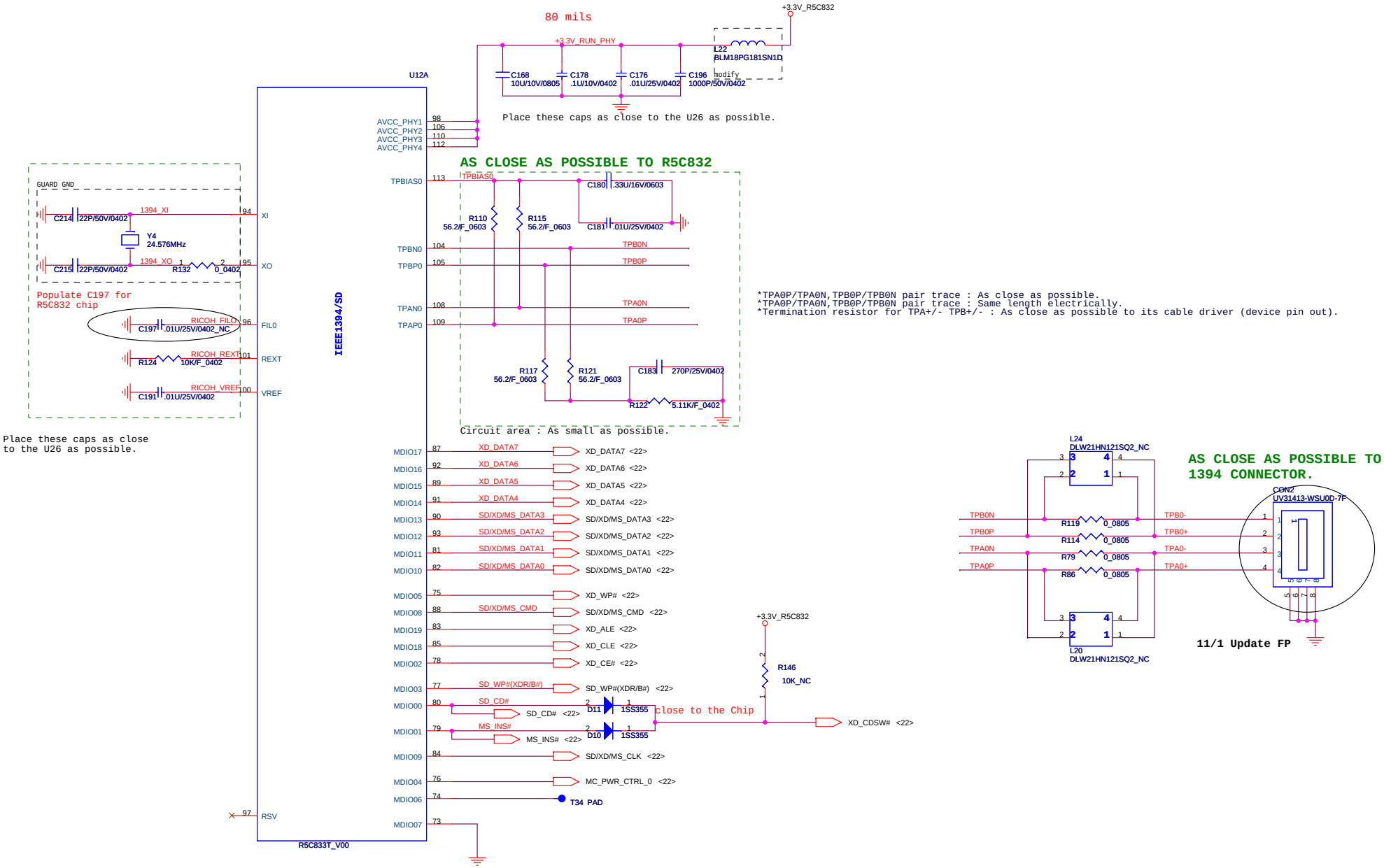

QUANTA COMPUTER

Title	CRT&TV CONN	
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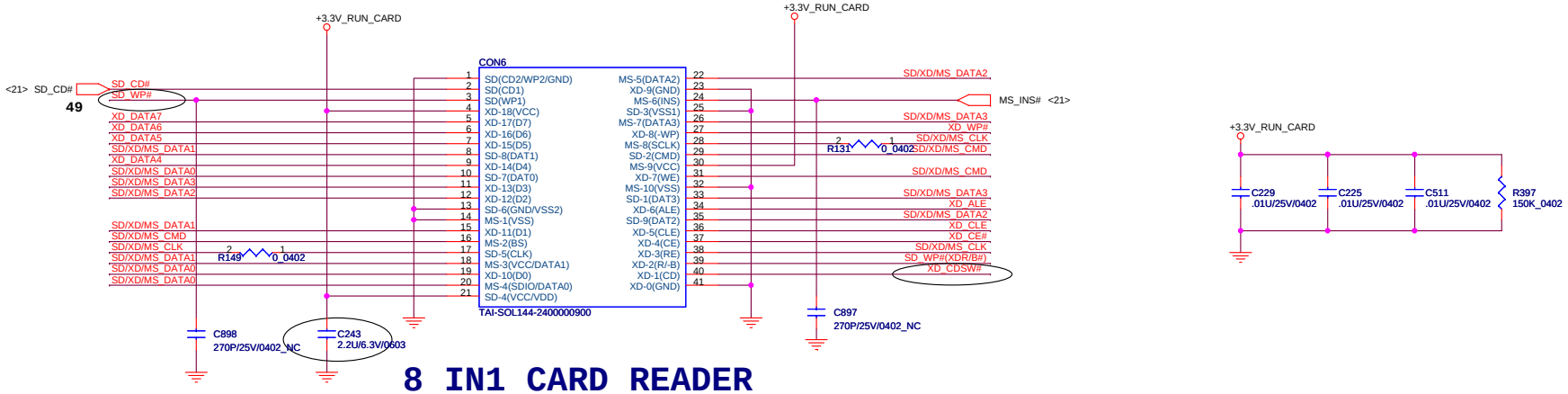
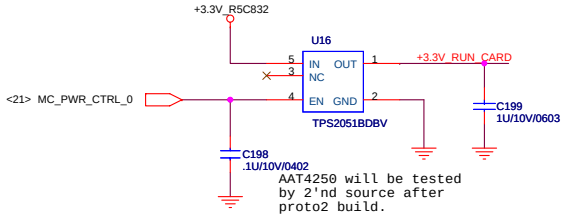
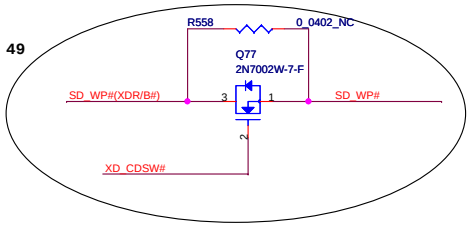


8 IN1 CARD READER



SD Protect



QUANTA COMPUTER

Title	CRT&TV CONN	
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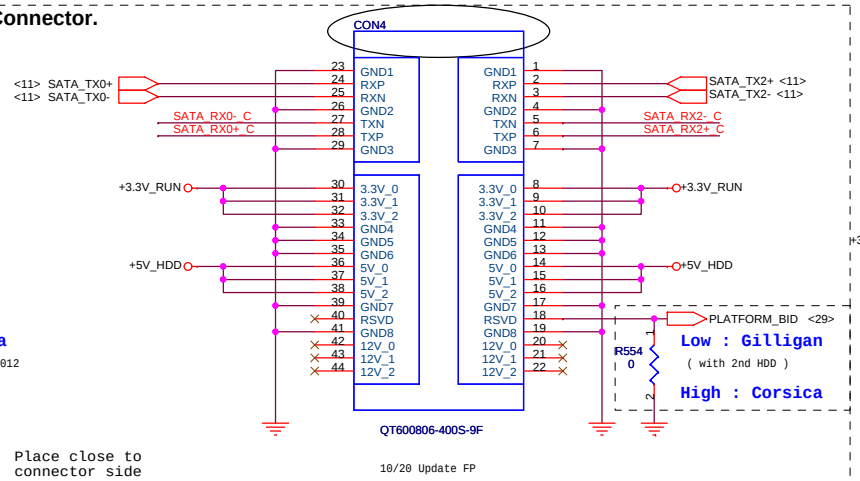
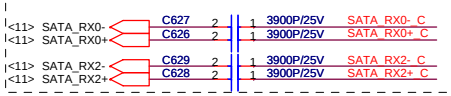
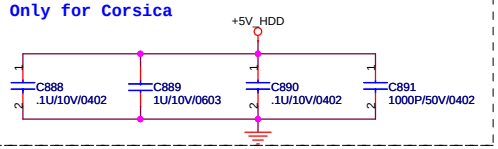
SATA 1 & 2 Connector.



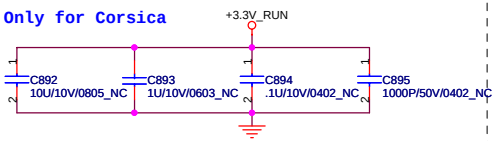
Locate caps C626, C627, C628, C629 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 0 mils.



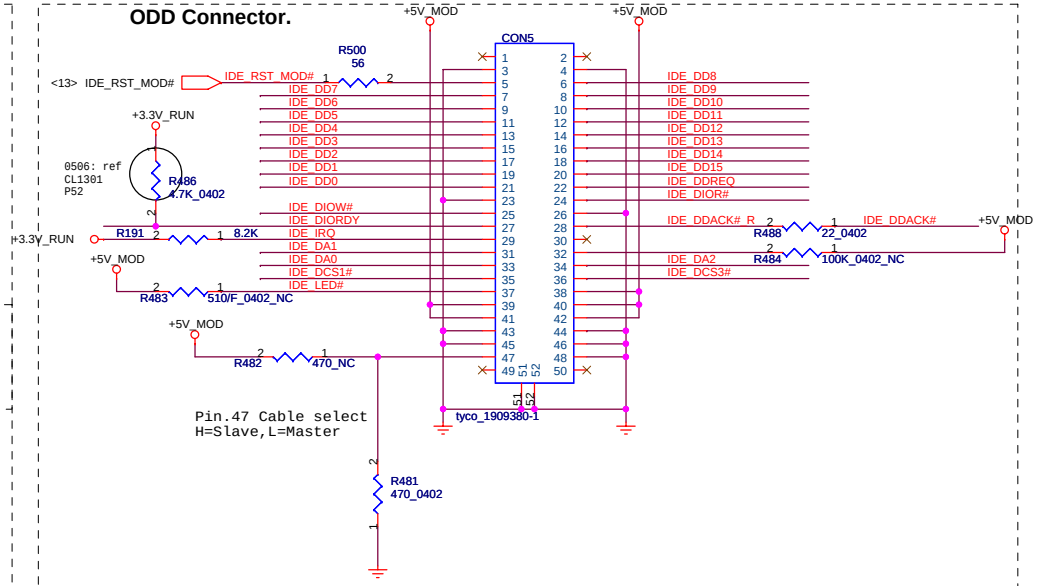
Only for Corsica

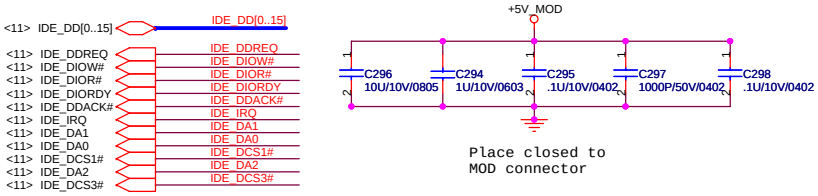


Only for Corsica

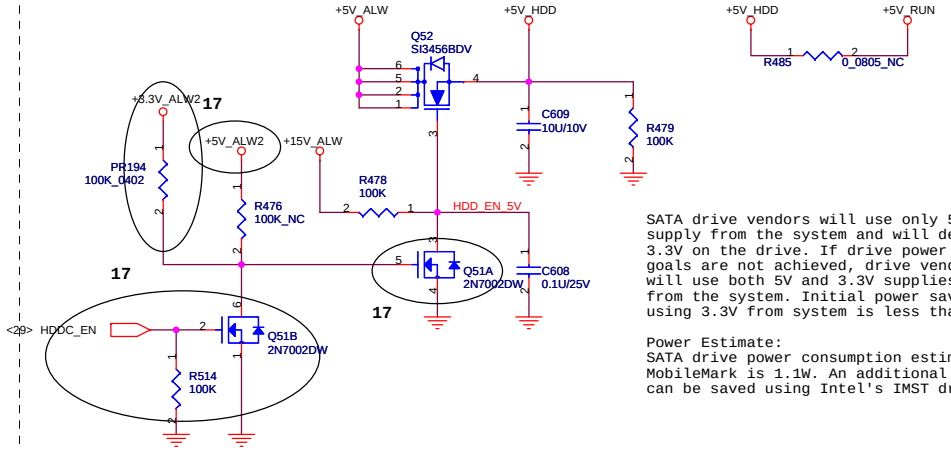


ODD Connector.





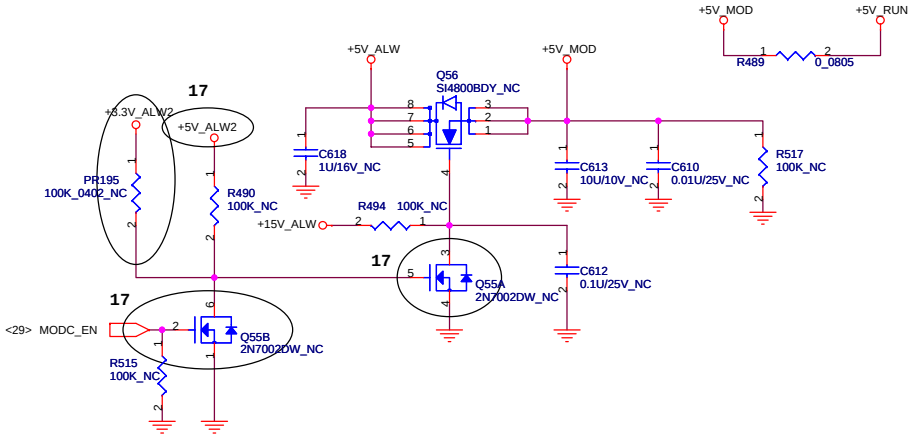
SATA PWR



SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

ODD PWR



QUANTA COMPUTER

Title	SATA (HDD&CD_ROM)	
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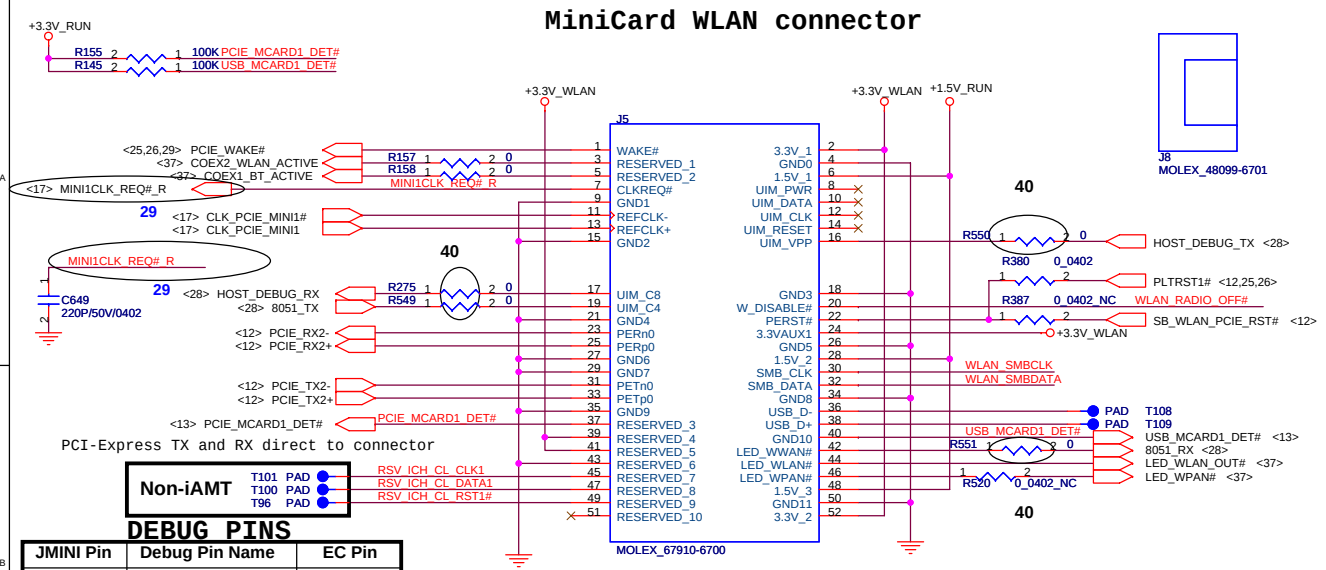
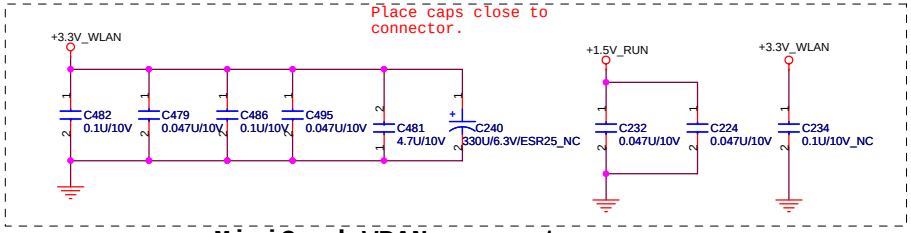
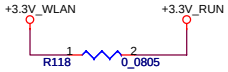
MiniCard WLAN connector

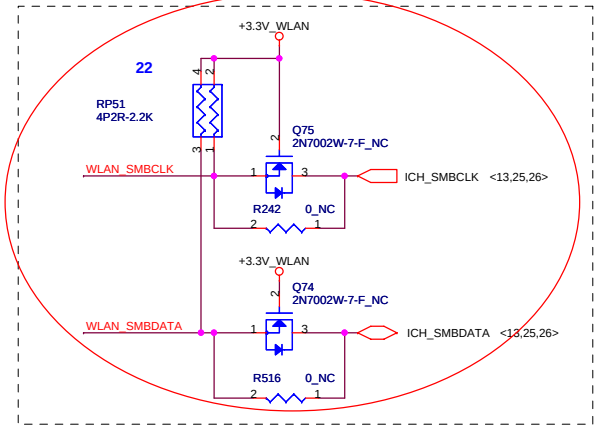


DEBUG PINS

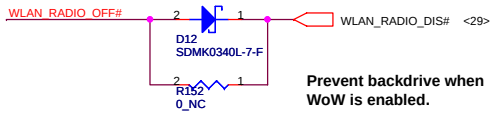
JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



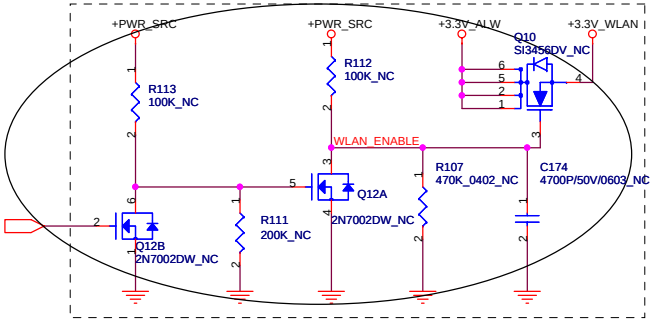




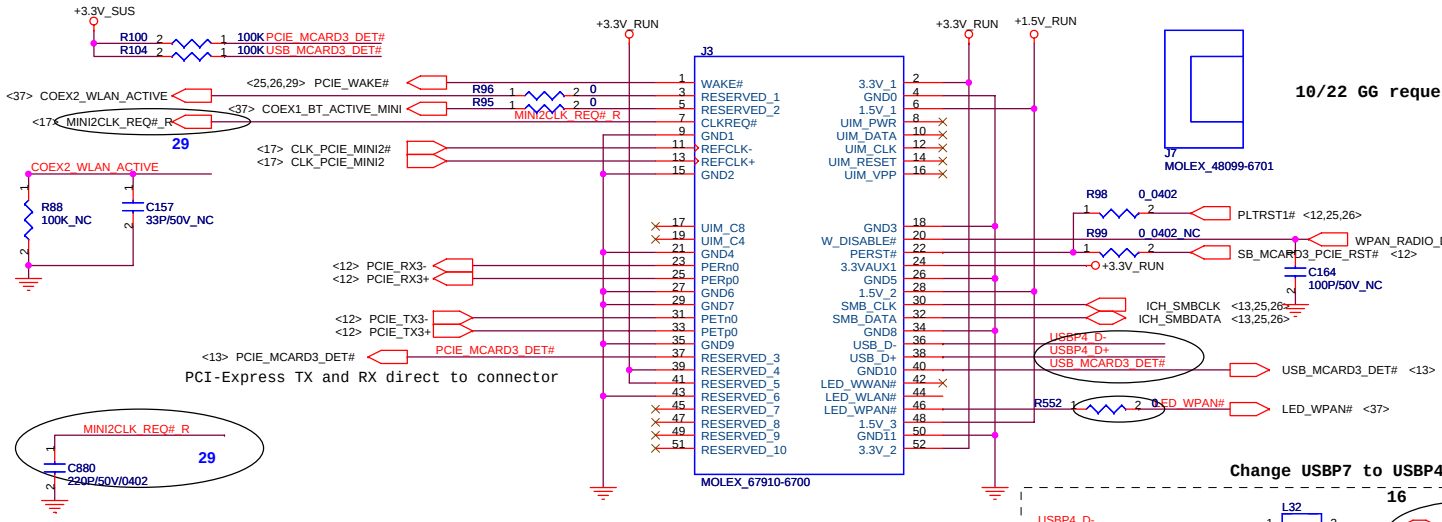
Suport for WoW



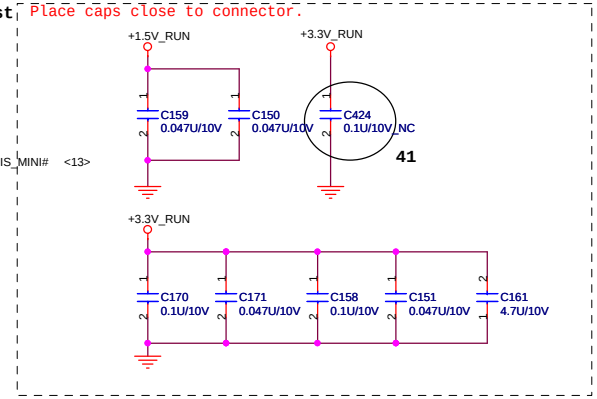
Prevent backdrive when WoW is enabled.



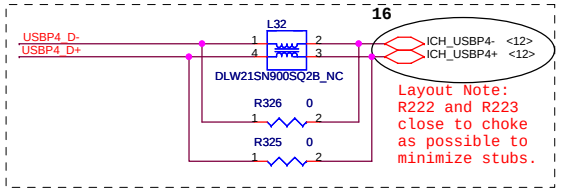
MiniCard WPAN connector



10/22 GG request



Change USBP7 to USBP4



Layout Note: R222 and R223 close to choke as possible to minimize stubs.

QUANTA COMPUTER

Title	MINI-PCI	
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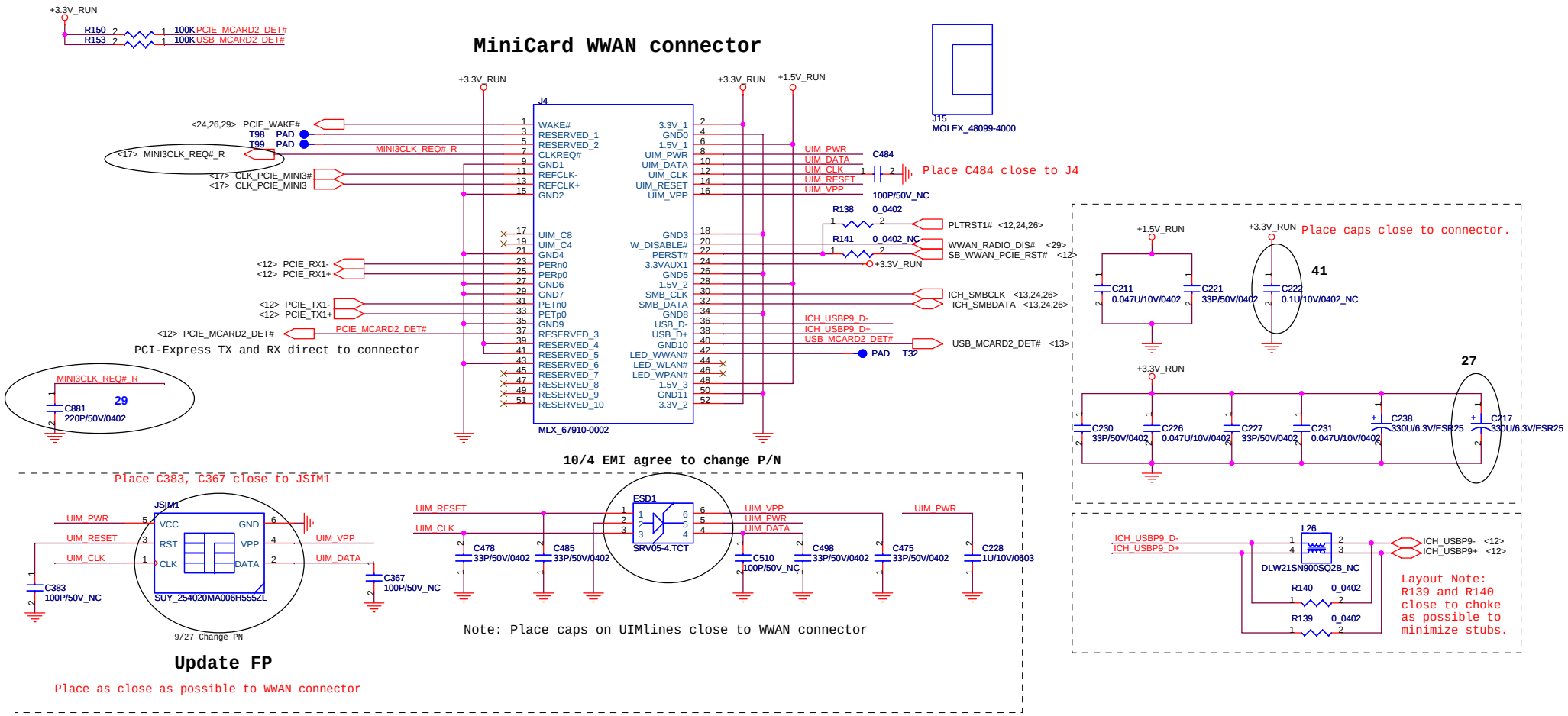

QUANTA COMPUTER

Title	WWAN	
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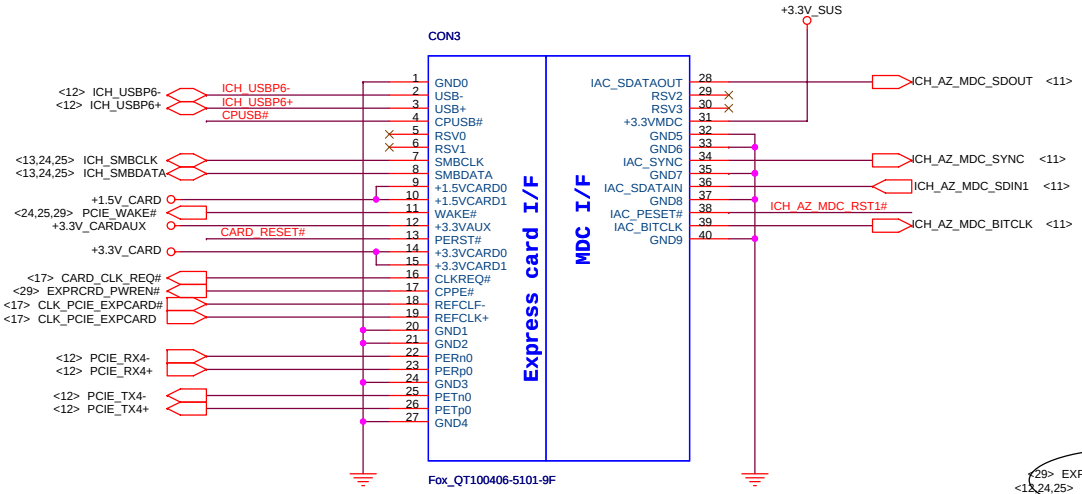
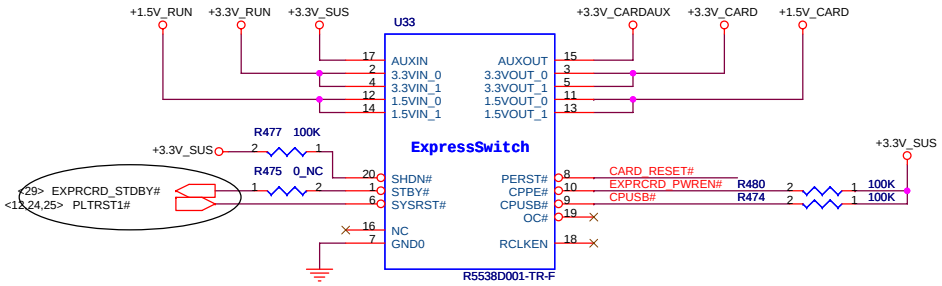
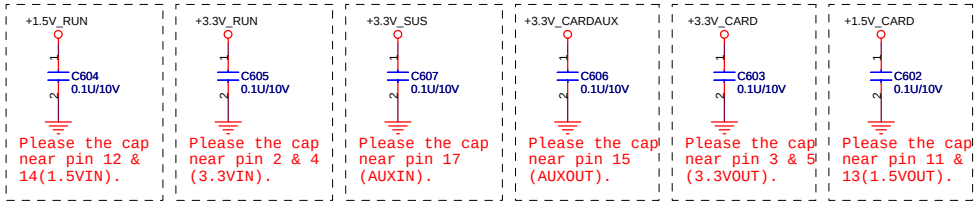
EXPRESS+MDC

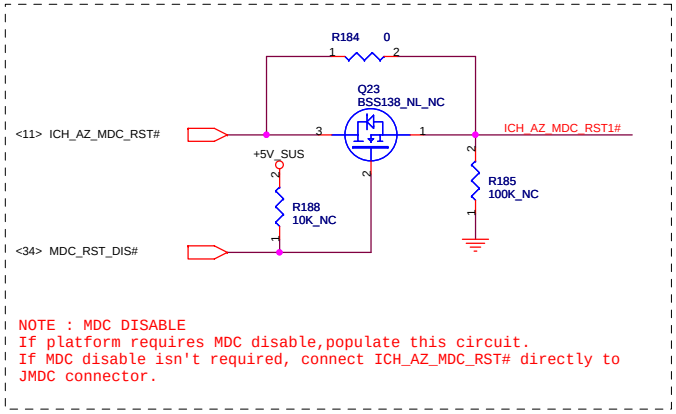


Update PN

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.







NOTE : MDC DISABLE
If platform requires MDC disable,populate this circuit.
If MDC disable isn't required, connect ICH_AZ_MDC_RST# directly to JMDC connector.

QUANTA COMPUTER

Title	ExpressCard/SmartCard	
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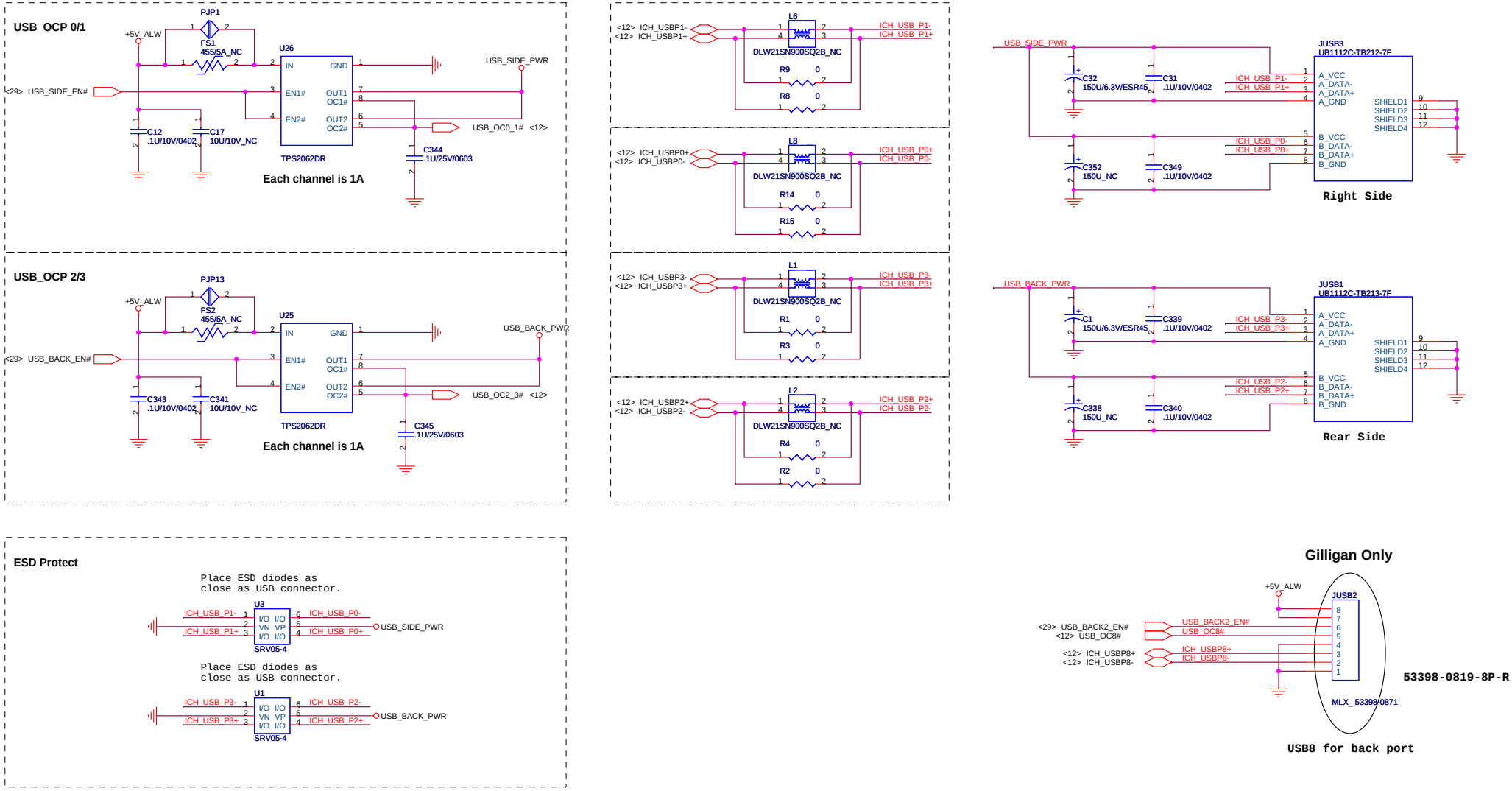
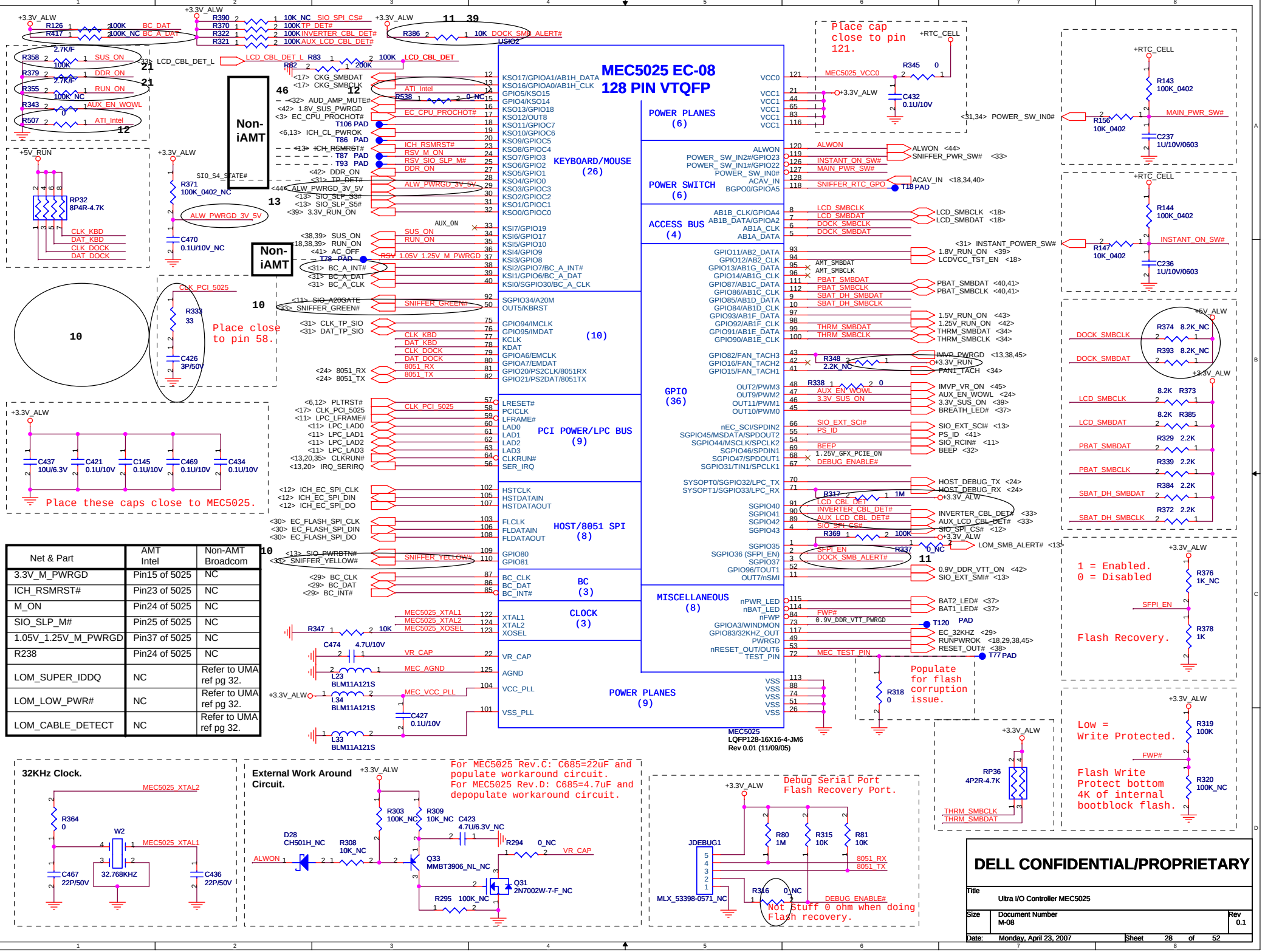


QUANTA COMPUTER

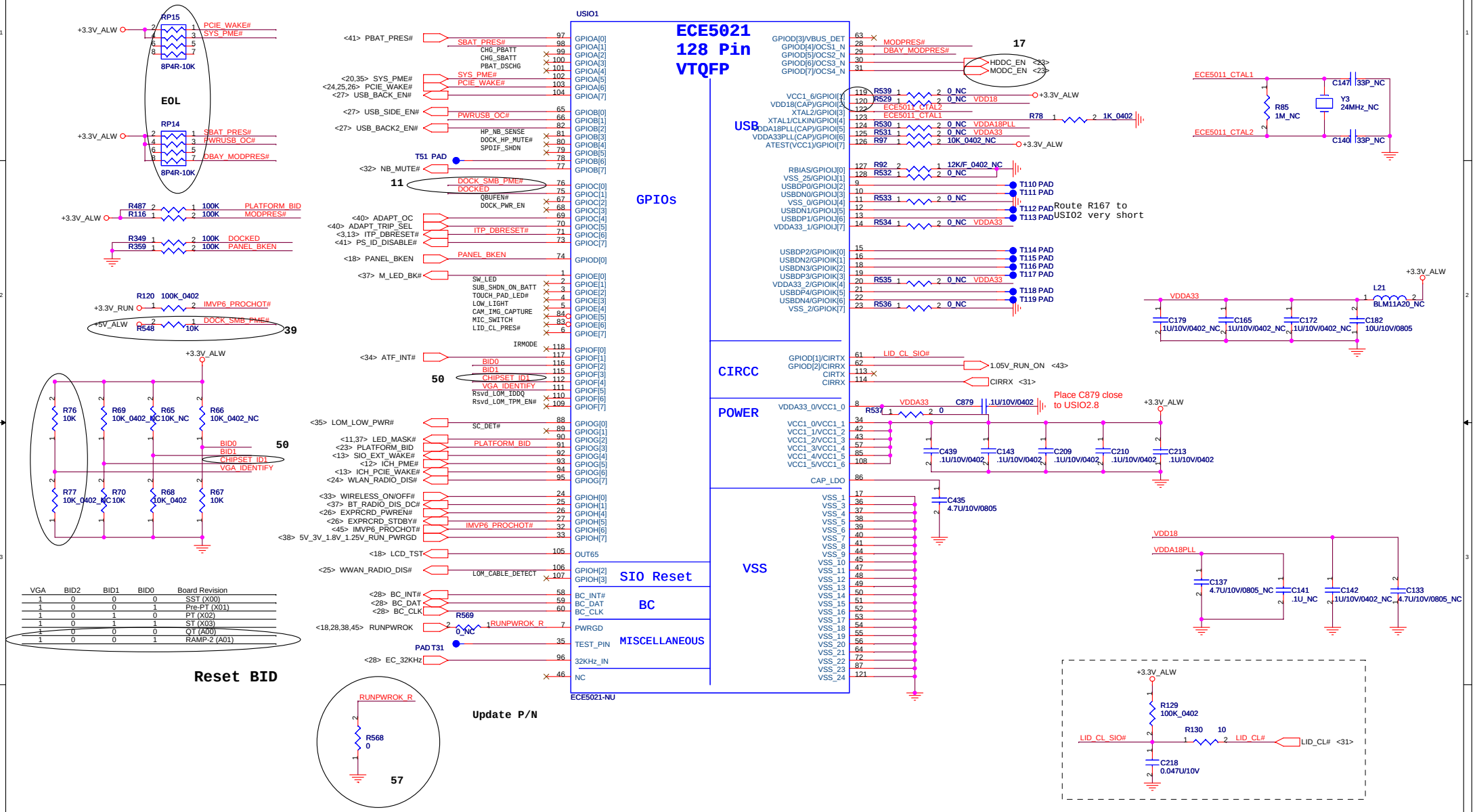
Title	USB & Flash	
Size	Document Number FM1	Rev 0.1
Date: Monday, April 23, 2007	Sheet 27 of 52	



Net & Part	AMT Intel	Non-AMT Broadcom
3.3V_M_PWRGD	Pin15 of 5025	NC
ICH_RSMRST#	Pin23 of 5025	NC
M_ON	Pin24 of 5025	NC
SIO_SLP_M#	Pin25 of 5025	NC
1.05V_1.25V_M_PWRGD	Pin37 of 5025	NC
R238	Pin24 of 5025	NC
LOM_SUPER_IDDQ	NC	Refer to UMA ref pg 32.
LOM_LOW_PWR#	NC	Refer to UMA ref pg 32.
LOM_CABLE_DETECT	NC	Refer to UMA ref pg 32.

Update to 5021

Depopulate R529, R530, R531, R532, R533, R534, R535, R536, R92, R97, C142, C133, C137, C141, C179, C165, C172, L21
Populate R537, C879.



VGA	BID2	BID1	BID0	Board Revision
1	0	0	0	SST (X00)
1	0	0	1	Pre-PT (X01)
1	0	1	0	PT (X02)
1	0	1	1	ST (X03)
1	0	0	0	QT (A00)
1	0	0	1	RAMP-2 (A01)

Reset BID

Update P/N

QUANTA COMPUTER

Title	SIO (GPIO/BC/USB/CIRR)	
Size	Document Number FM1	Rev 0.1
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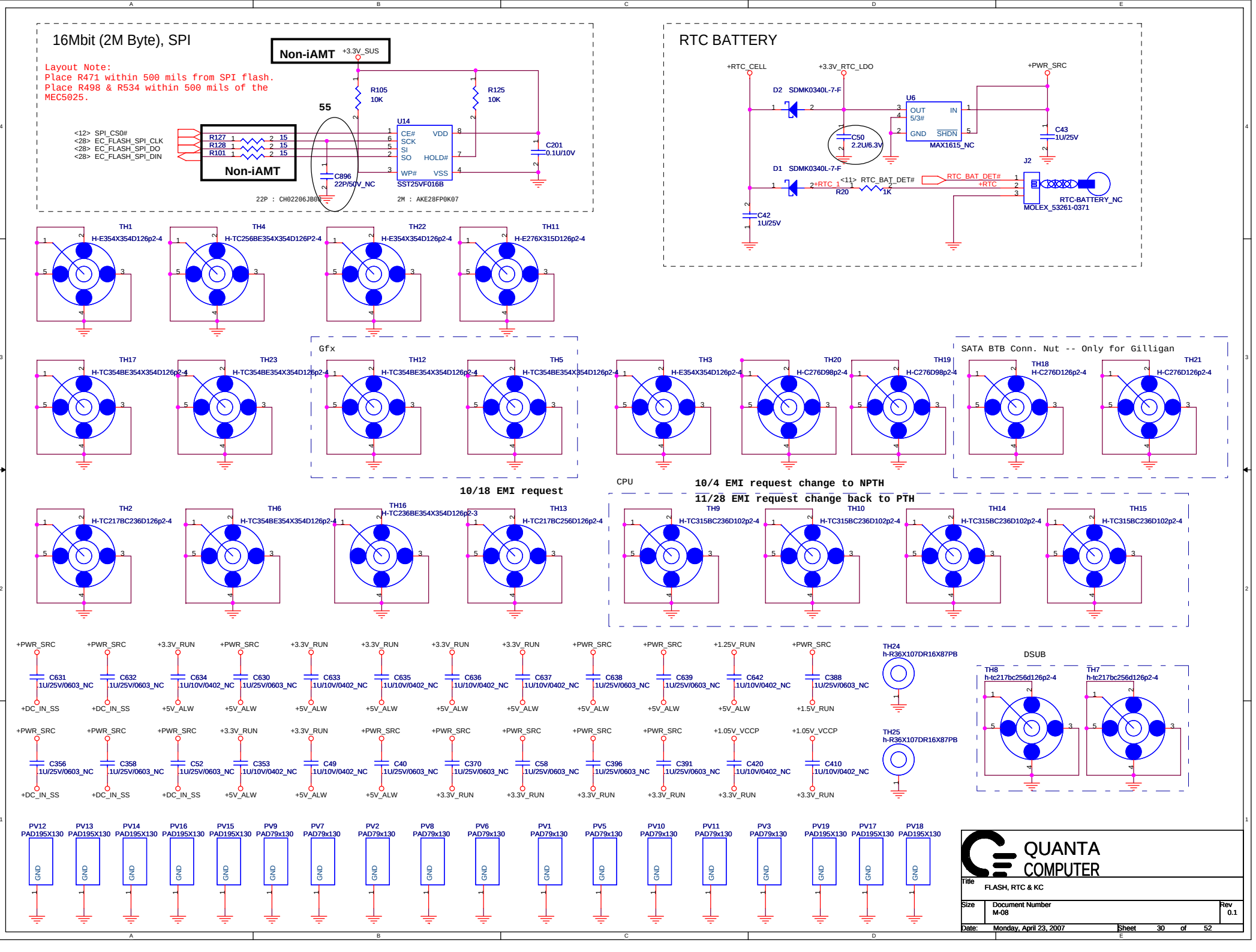
16Mbit (2M Byte), SPI
Non-iAMT
+3.3V_SUS
Layout Note:
Place R471 within 500 mils from SPI flash.
Place R498 & R534 within 500 mils of the MEC5025.
55
R105 10K
R125 10K
<12> SPI_CS0#
<28> EC_FLASH_SPI_CLK
<28> EC_FLASH_SPI_DO
<28> EC_FLASH_SPI_DIN
R127 15
R128 15
R101 15
Non-iAMT
U14
CE# VDD
SCK
SI
SO HOLD#
WP# VSS
SST25VF016B
C201 0.1U/10V
C896 22P/50V_NC
22P : CH02206JB08
2M : AKE28FP0K07
RTC BATTERY
+RTC_CELL
+3.3V_RTC_LDO
+PWR_SRC
D2 SDMK0340L-7-F
U6
OUT IN
5/3#
GND SHDN
MAX1615_NC
C50 2.2U/6.3V
C43 1U/25V
J2
D1 SDMK0340L-7-F
+RTC_1
<11> RTC_BAT_DET#
RTC_BAT_DET#
+RTC
R20 1K
RTC-BATTERY_NC
MOLEX_53261-0371
C42 1U/25V
TH1 H-E354X354D126p2-4
TH4 H-TC256BE354X354D126P2-4
TH22 H-E354X354D126p2-4
TH11 H-E276X315D126p2-4
Gfx
TH17 H-TC354BE354X354D126p2-4
TH23 H-TC354BE354X354D126p2-4
TH12 H-TC354BE354X354D126p2-4
TH5 H-TC354BE354X354D126p2-4
TH3 H-E354X354D126p2-4
TH20 H-C276D98p2-4
TH19 H-C276D98p2-4
SATA BTB Conn. Nut -- Only for Gilligan
TH18 H-C276D126p2-4
TH21 H-C276D126p2-4
10/18 EMI request
CPU
10/4 EMI request change to NPTH
11/28 EMI request change back to PTH
TH2 H-TC217BC236D126p2-4
TH6 H-TC354BE354X354D126p2-4
TH16 H-TC236BE354X354D126p2-3
TH13 H-TC217BC256D126p2-4
TH9 H-TC315BC236D102p2-4
TH10 H-TC315BC236D102p2-4
TH14 H-TC315BC236D102p2-4
TH15 H-TC315BC236D102p2-4
+PWR_SRC
+3.3V_RUN
+1.25V_RUN
C631 1U/25V/0603_NC
C632 1U/25V/0603_NC
C634 1U/10V/0402_NC
C630 1U/25V/0603_NC
C633 1U/10V/0402_NC
C635 1U/10V/0402_NC
C636 1U/10V/0402_NC
C637 1U/10V/0402_NC
C638 1U/25V/0603_NC
C639 1U/25V/0603_NC
C642 1U/10V/0402_NC
C388 1U/25V/0603_NC
+DC_IN_SS
+5V_ALW
+1.5V_RUN
TH24 h-R36X107DR16X87PB
TH25 h-R36X107DR16X87PB
DSUB
TH8 h-tc217bc256d126p2-4
TH7 h-tc217bc256d126p2-4
+1.05V_VCCP
C356 1U/25V/0603_NC
C358 1U/25V/0603_NC
C52 1U/25V/0603_NC
C353 1U/10V/0402_NC
C49 1U/10V/0402_NC
C40 1U/25V/0603_NC
C370 1U/25V/0603_NC
C58 1U/25V/0603_NC
C396 1U/25V/0603_NC
C391 1U/25V/0603_NC
C420 1U/10V/0402_NC
C410 1U/10V/0402_NC
PV12 PAD195X130
PV13 PAD195X130
PV14 PAD195X130
PV16 PAD195X130
PV15 PAD195X130
PV9 PAD79x130
PV7 PAD79x130
PV2 PAD79x130
PV8 PAD79x130
PV6 PAD79x130
PV1 PAD79x130
PV5 PAD79x130
PV10 PAD79x130
PV11 PAD79x130
PV3 PAD79x130
PV19 PAD195X130
PV17 PAD195X130
PV18 PAD195X130
GND
QUANTA COMPUTER
Title
FLASH, RTC & KC
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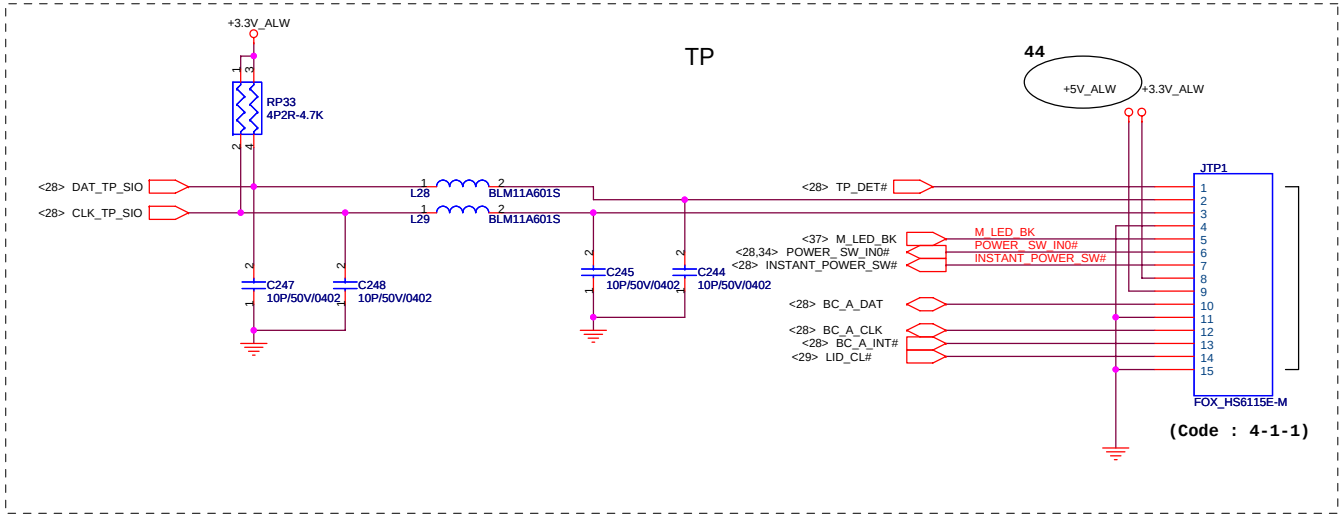

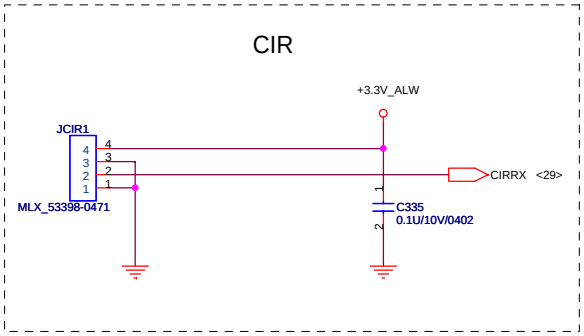

QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
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INTERNAL SPEAKER AMP

Update PN

52

Package 1206 for THD+N performance for Vista Logo requirements.

AUD_LINE_OUT_L C306 .033U/25V/X7R/1206
AUD_LINE_OUT_R C307 .033U/25V/X7R/1206
AUD_HP_OUT_L C326 1uF/25V/X7R/1206
AUD_HP_OUT_R C329 1uF/25V/X7R/1206

10/18 Change 2.2u if necessary

C330 47P/50V_NC C327 47P/50V_NC C312 47P/50V_NC C311 47P/50V_NC

31

C334 1U/10V

<28> AUD_AMP_MUTE# 32

U23 TPA6040A4 QFN 32PIN

SPKR_INL SPKR_INR HP_INL HP_INR BIAS SPKR_EN# HP_EN MUTE# GAIN1 GAIN2 HPVDD CPVDD C1P C1N CPGND PVSS CPVSS

OUTL+ OUTL- OUTR+ OUTR- HPL HPR REGEN SET VOUT VDD PVDD_8 PVDD_18 GND_28 PGND_5 PGND_21

LIN- SPKR_LIN+
RIN- SPKR_RIN+
HP_OUT_L
HP_OUT_R
AUD_SPK_ENABLE#
AMP_HP_EN
AUD_AMP_MUTE#
AUD_AMP_GAIN1
AUD_AMP_GAIN2
REG_EN

AUD_SPK_L1 AUD_SPK_L2 AUD_SPK_R1 AUD_SPK_R2
AUD_HP_JACK_L <33>
AUD_HP_JACK_R <33>
REGEN
SET
SPKR_LIN-
SPKR_RIN-
+VDDA
VDD
+5V_SPK_AMP

C616 1U/16V C328 1U/10V C318 10U/10V

10/18 Depop if not necessary

C324 1U/16V

TPA6040A4

JSPK1 MLX_53398-0671

R560 0_0603 R561 0_0603 R562 0_0603 R563 0_0603

<11> SPEAKER_DET#

C620 100P/50V_NC C621 100P/50V_NC C622 100P/50V_NC C623 100P/50V_NC

For MAX9789A,depop R505,pop R506.

+5V_SPK_AMP R506 100K_NC R505 0 AUDIO_AVDD_ON AUD_AMP_MUTE#

+5V_SPK_AMP C625 0.1U/10V U34 74AHCT1G08GW

NB_MUTE# AUD_HP_NB_SENSE AUD_HP_NB_SENSE_R CODEC_GPIO_PIN_4 AMP_HP_EN

AL01GT08011 R545 0

+5V_SPK_AMP U36 NC7SZ08P5X_NL_NC

L35 FB_600ohm+-25%_100MHz _200mA_0.6ohm DC

+5V_SPK_AMP VDD C316 1U/10V C615 1U/10V C319 0.1U/10V

Layout Note: Place close U22.

+VDDA C617 1U/10V C323 1U/10V

Layout Note: Place close U22.

AUDIO_AVDD_ON <34> R504 0_NC REGEN C619 0.033U/16V

C1425/C331 value need to match with C326/C290. This value be chosen in PT phase.

For MAX9789A,depop C619,pop R504.

+5V_SPK_AMP +5V_RUN +5V_SPK_AMP L30 BLM21PG600SN1D

C310 1U/10V C315 10U/10V

Layout Note: Place close to pin 8.

FB_60ohm+-25%_100MHz _3A_0.05ohm DC

C332 1U/10V C331 10U/10V C333 0.1U/10V

Layout Note: Place close to pin 18.

+5V_SPK_AMP R208 100K R209 100K AUD_SPK_ENABLE# AUD_EAPD# Q25 2N7002W-7-F

<29> NB_MUTE# Q24 2N7002W-7-F

+5V_SPK_AMP R496 100K_NC R499 100K AUD_AMP_GAIN1 AUD_AMP_GAIN2 R197 100K R199 100K_NC

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

For MAX9789A,depop C614,pop R497.

SET R498 2.2K_NC +VDDA C614 0.033U/16V R497 0_NC

R501 0_0805 R207 0_0603 R189 0_0603 R198 0_0603 R202 0_0603

EMI Request

AZALIA (HD) CODEC

ICH_AZ_CODEC_BITCLK R193 47_NC Close to pin 6. C305 0.1U/10V_NC

ICH_AZ_CODEC_SDOUT R195 47_NC Close to pin 5. C308 0.1U/10V_NC

<11> ICH_AZ_CODEC_BITCLK
<11> ICH_AZ_CODEC_SDIN0
<11> ICH_AZ_CODEC_SDOUT
<11> ICH_AZ_CODEC_SYNC
<11> ICH_AZ_CODEC_RST#

R192 33 SDIN

49

<33> AUD_DMIC_CLK
<33> AUD_DMIC_IN0

R555 0 R556 0 CODEC_GPIO_PIN_4

For tuning.

<19> AUD_SPDIF_OUT R204 0 AUD_EAPD# SPDIF_OUT

+3.3V_RUN C317 10U/10V_NC C301 0.1U/10V C313 1U/10V R203 0 R253 100K

+3.3V_RUN C325 4.7U/10V_NC C321 0.1U/10V_NC C643 1000P/50V C309 0.1U/10V

37

AUD_DMIC_CLK C647 4.7P/50V_NC 49 AUD_DMIC_IN0 C648 4.7P/50V_NC

+VDDA Depop R203 & pop C321 & C325 for AD1984.

C302 0.1U/16V C303 1U/10V C322 10U/10V_NC

U22 10/18 Check package STAC9205 LQFP 48PIN

HDA_BITCLK HDA_SDI_CODEC HDA_SDO HDA_SYNC HDA_RST# DMIC_CLK DMIC0/VOL_UP/GPIO1 DMIC1/VOL_DN/GPIO2 SPDIF_IN/EAPD#/GPIO0 SPDIF_OUT NC_43 NC_44 NC_45 DVDD_CORE_1 DVDD_CORE_9 DVDD_CORE_40 DVDD_IO AVDD_25 AVDD_38 DVSS AVSS_26 AVSS_42

SENSE_A SENSE_B PORT_A_L PORT_A_R VREFOUT_A PORT_B_L PORT_B_R VREFOUT_B PORT_C_L PORT_C_R VREFOUT_C PORT_D_L PORT_D_R PORT_E_L PORT_E_R GPIO4/VREFOUT_E PORT_F_L PORT_F_R GPIO3/VREFOUT_F CD_L CD_GND CD_R PC_BEEP MONO_OUT VREFFILT CAP2

AUD_SENSE_A AUD_SENSE_B AUD_HP_OUT_L AUD_HP_OUT_R AUD_EXT_MIC_L <33> AUD_EXT_MIC_R <33> AUD_VREFOUT_B <33> AUD_MIC_IN_L AUD_MIC_IN_R AUD_LINE_OUT_L AUD_LINE_OUT_R DOCK_HP_MUTE# AUD_SPDIF_SHDN AUD_PC_BEEP AC97VREFI CAP2

+VDDA R201 100K R196 10K R194 10K 10_NC R200

C314 10U/10V C304 10U/10V C320 0.1U/10V_NC

C304 must be 1U & Pop C320 & R200 for AD1984.

Layout Note: Close to U22 Pin 13.

R493 5.1K/F +VDDA AUD_SENSE_A R491 39.2K/F R492 20K/F C611 1000P/50V

<33> AUD_HP_NB_SENSE AUD_HP_NB_SENSE Q53 2N7002W-7-F Q54 2N7002W-7-F AUD_MIC_SWITCH <33>

Close to U22

+VDDA C300 0.1U/16V

AUD_PC_BEEP C299 0.1U/10V BEEP2 R187 20K BEEP1 R190 10K U21 74LVC1G86GW BEEP <28> SPKR <13>

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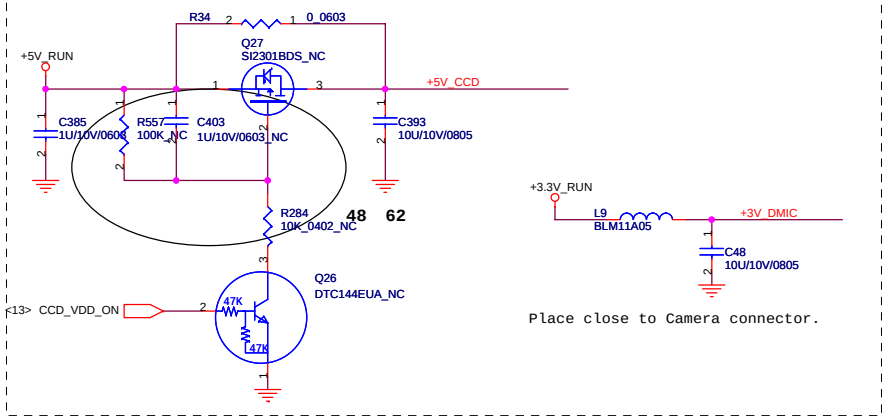
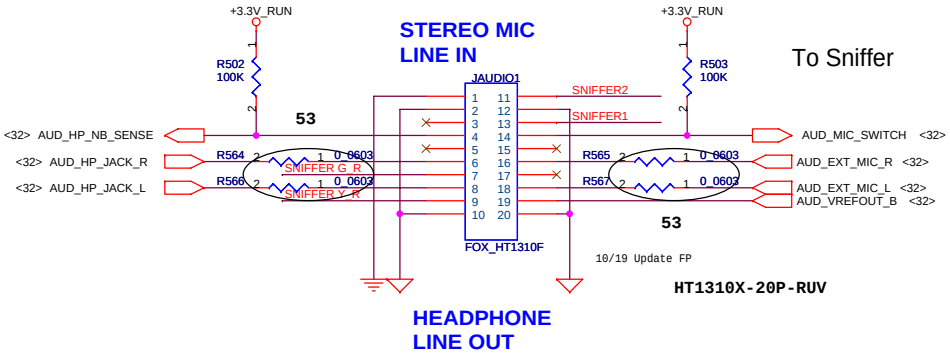
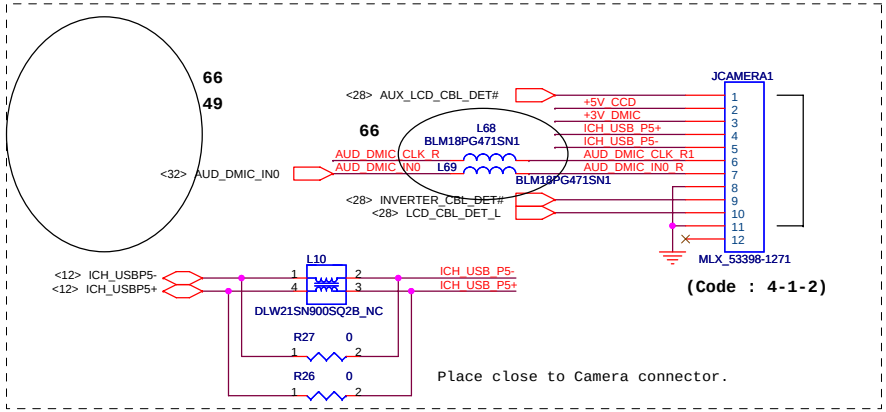
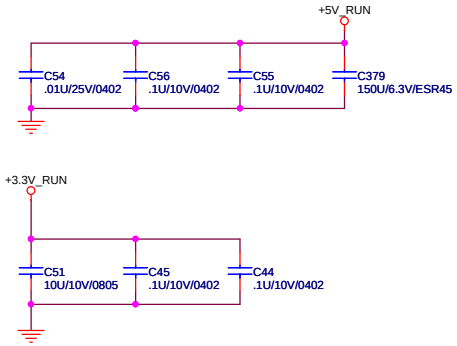
Digital Microphone & Camera

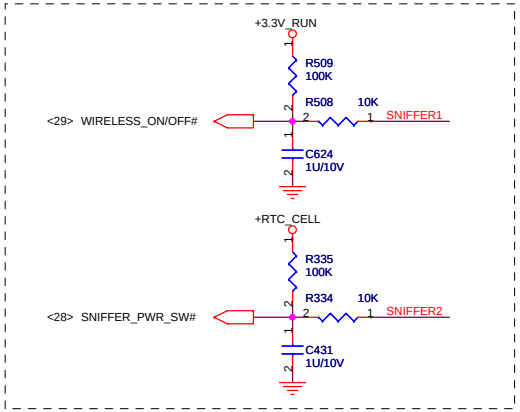


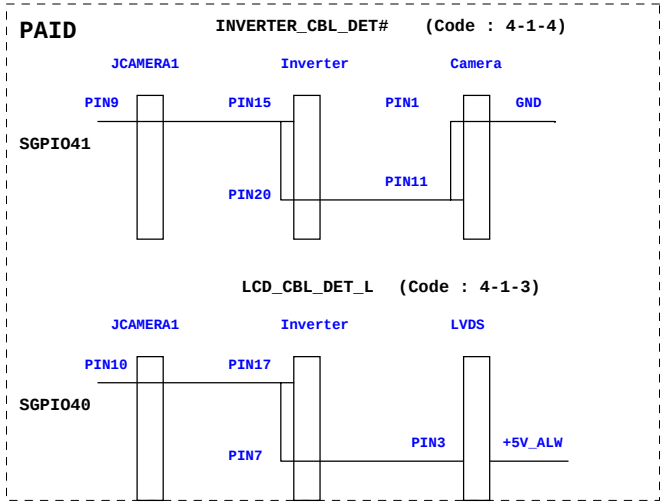
Update PN

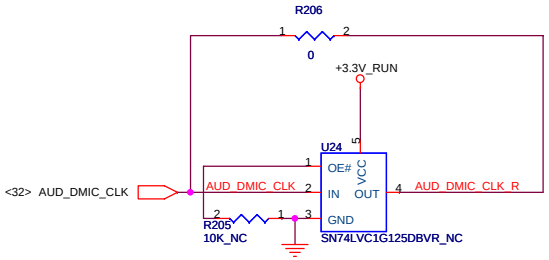


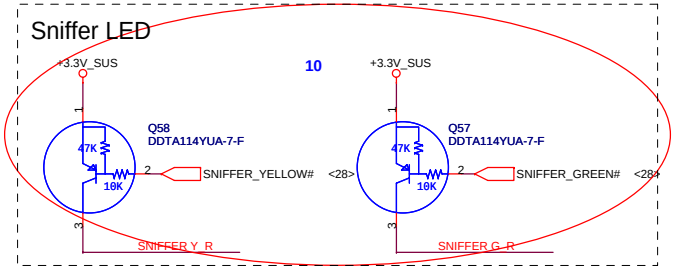












DELL CONFIDENTIAL/PROPRIETARY

Title	AUDIO CONN	
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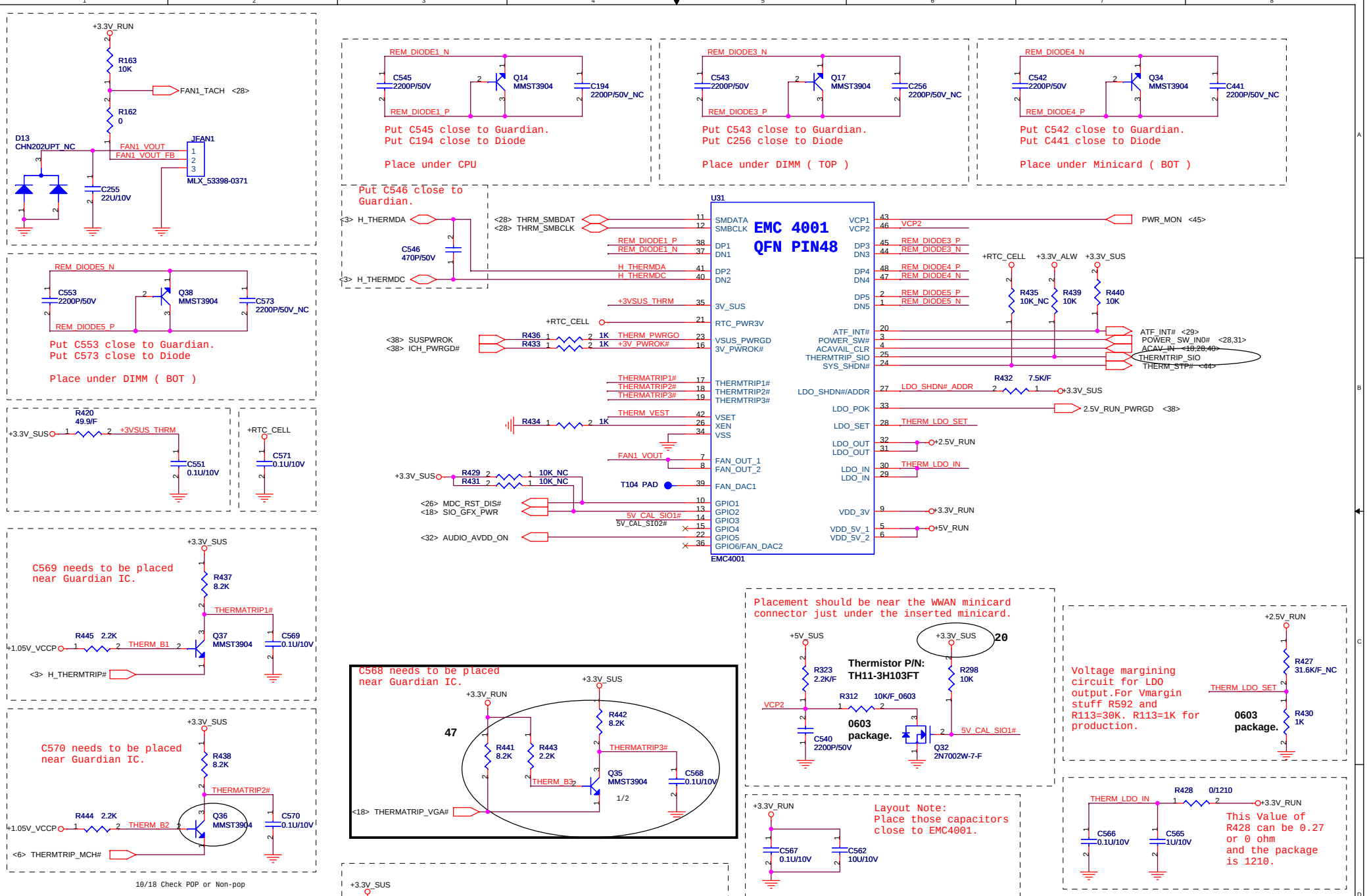

DELL CONFIDENTIAL/PROPRIETARY

Title	FAN & THERMAL	
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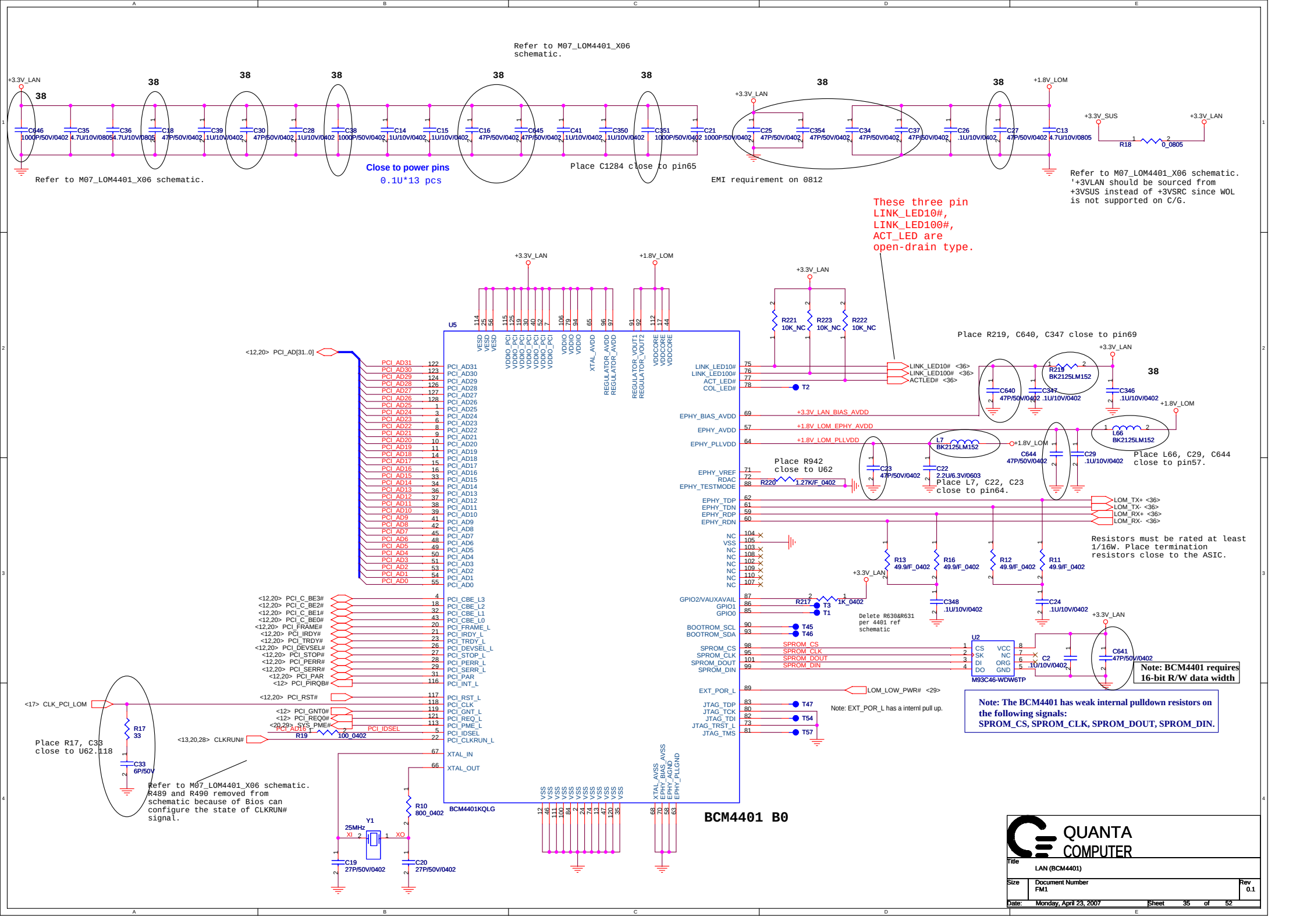
Refer to M07_LOM4401_X06 schematic.
+3.3V_LAN
38
C646 1000P/50V/0402
C35 4.7U/10V/0805
C36 4.7U/10V/0805
C18 47P/50V/0402
C39 1U/10V/0402
C30 47P/50V/0402
C28 1U/10V/0402
C38 1000P/50V/0402
C14 1U/10V/0402
C15 1U/10V/0402
C16 47P/50V/0402
C645 47P/50V/0402
C41 1U/10V/0402
C350 1U/10V/0402
C351 1000P/50V/0402
C21 1000P/50V/0402
Close to power pins
0.1U*13 pcs
Place C1284 close to pin65
Refer to M07_LOM4401_X06 schematic.
C25 47P/50V/0402
C354 47P/50V/0402
C34 47P/50V/0402
C37 47P/50V/0402
C26 .1U/10V/0402
C27 47P/50V/0402
C13 4.7U/10V/0805
+1.8V_LOM
EMI requirement on 0812
+3.3V_SUS
R18 0_0805
Refer to M07_LOM4401_X06 schematic.
'+3VLAN should be sourced from
+3VSUS instead of +3VSRC since WOL
is not supported on C/G.
These three pin
LINK_LED10#,
LINK_LED100#,
ACT_LED are
open-drain type.
U5
BCM4401KQLG
R221 10K_NC
R223 10K_NC
R222 10K_NC
Place R219, C640, C347 close to pin69
R219 BK2125LM152
C640 47P/50V/0402
C347 .1U/10V/0402
C346 .1U/10V/0402
LINK_LED10# <36>
LINK_LED100# <36>
ACTLED# <36>
+3.3V_LAN_BIAS_AVDD
+1.8V_LOM_EPHY_AVDD
+1.8V_LOM_PLLVDD
L7 BK2125LM152
L66 BK2125LM152
C644 47P/50V/0402
C29 .1U/10V/0402
Place L66, C29, C644
close to pin57.
Place R942
close to U62
R220 1.27K/F_0402
C23 47P/50V/0402
C22 2.2U/6.3V/0603
Place L7, C22, C23
close to pin64.
LOM_TX+ <36>
LOM_TX- <36>
LOM_RX+ <36>
LOM_RX- <36>
Resistors must be rated at least
1/16W. Place termination
resistors close to the ASIC.
R13 49.9/F_0402
R16 49.9/F_0402
R12 49.9/F_0402
R11 49.9/F_0402
C348 .1U/10V/0402
C24 .1U/10V/0402
R217 1K_0402
Delete R630&R631
per 4401 ref
schematic
U2
M93C46-WDW6TP
C2 .1U/10V/0402
C641 47P/50V/0402
Note: BCM4401 requires
16-bit R/W data width
LOM_LOW_PWR# <29>
Note: EXT_POR_L has a internl pull up.
Note: The BCM4401 has weak internal pulldown resistors on
the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.
<12,20> PCI_AD[31..0]
<12,20> PCI_C_BE3#
<12,20> PCI_C_BE2#
<12,20> PCI_C_BE1#
<12,20> PCI_C_BE0#
<12,20> PCI_FRAME#
<12,20> PCI_IRDY#
<12,20> PCI_TRDY#
<12,20> PCI_DEVSEL#
<12,20> PCI_STOP#
<12,20> PCI_PERR#
<12,20> PCI_SERR#
<12,20> PCI_PAR
<12> PCI_PIRQB#
<12,20> PCI_RST#
<17> CLK_PCI_LOM
<12> PCI_GNT0#
<12> PCI_REQ0#
<20,29> SYS_PME#
<13,20,28> CLKRUN#
R17 33
C33 6P/50V
R19 100_0402
Place R17, C33
close to U62.118
Refer to M07_LOM4401_X06 schematic.
R489 and R490 removed from
schematic because of Bios can
configure the state of CLKRUN#
signal.
R10 800_0402
Y1 25MHz
C19 27P/50V/0402
C20 27P/50V/0402
BCM4401 B0
QUANTA COMPUTER
Title
LAN (BCM4401)
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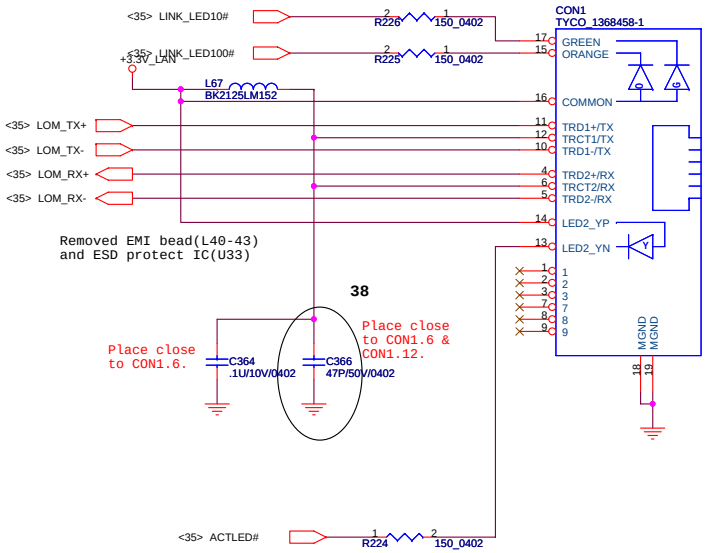

QUANTA COMPUTER

Title	LAN Jack	
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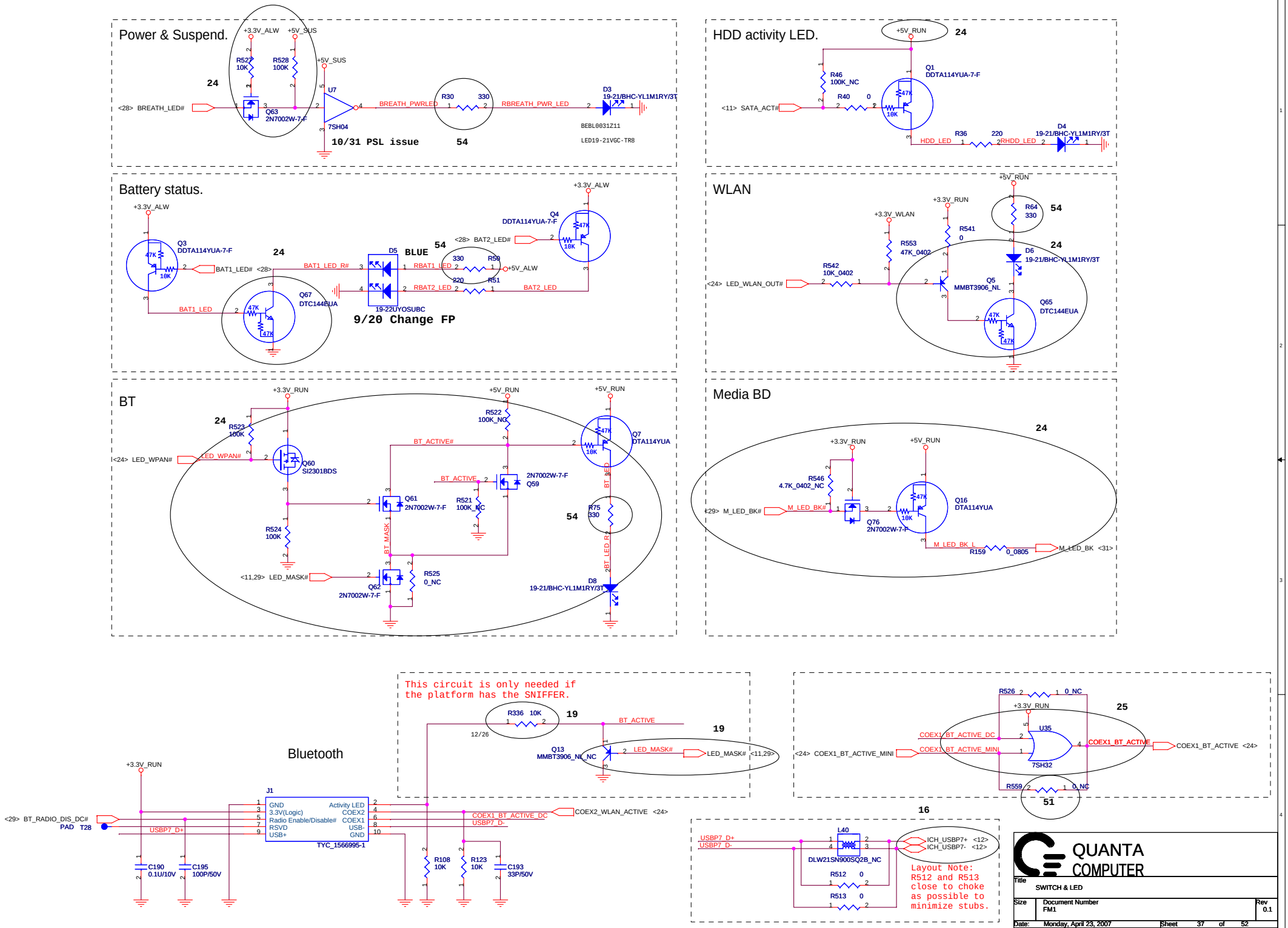
Power & Suspend.
+3.3V_ALW
+5V_SUS
R522 10K
R528 100K
24
<28> BREATH_LED#
Q63 2N7002W-7-F
U7
7SH04
BREATH_PWRLED
R30 330
RBREATH_PWR_LED
D3 19-21/BHC-YL1M1RY/3T
BEBL0031Z11
LED19-21VGC-TR8
10/31 PSL issue
54
HDD activity LED.
+5V_RUN
24
R46 100K_NC
R40 0
Q1 DDTA114YUA-7-F
<11> SATA_ACT#
HDD_LED
R36 220
RHDD_LED
D4 19-21/BHC-YL1M1RY/3T
Battery status.
+3.3V_ALW
Q3 DDTA114YUA-7-F
24
BAT1_LED# <28>
BAT1_LED_R#
D5 BLUE
54
RBAT1_LED
RBAT2_LED
19-22UYOSUBC
Q67 DTC144EUA
BAT1_LED
<28> BAT2_LED#
Q4 DDTA114YUA-7-F
R59 330
R51 220
+5V_ALW
BAT2_LED
9/20 Change FP
WLAN
+5V_RUN
+3.3V_RUN
+3.3V_WLAN
R64 330
54
R541 0
R553 47K_0402
24
D6 19-21/BHC-YL1M1RY/3T
R542 10K_0402
<24> LED_WLAN_OUT#
Q5 MMBT3906_NL
Q65 DTC144EUA
BT
+3.3V_RUN
+5V_RUN
24
R523 100K
R522 100K_NC
Q7 DTA114YUA
<24> LED_WPAN#
LED_WPAN#
Q60 SI2301BDS
BT_ACTIVE#
BT_ACTIVE
2N7002W-7-F Q59
Q61 2N7002W-7-F
R521 100K_NC
R75 330
54
R524 100K
BT_MASK
BT_LED
2BT_LED_R2
<11,29> LED_MASK#
Q62 2N7002W-7-F
R525 0_NC
D8 19-21/BHC-YL1M1RY/3T
Media BD
24
+3.3V_RUN
+5V_RUN
R546 4.7K_0402_NC
<29> M_LED_BK#
M_LED_BK#
Q76 2N7002W-7-F
Q16 DTA114YUA
M_LED_BK_L
R159 0_0805
M_LED_BK <31>
Bluetooth
This circuit is only needed if the platform has the SNIFFER.
R336 10K
19
12/26
BT_ACTIVE
19
Q13 MMBT3906_NL_NC
LED_MASK#
LED_MASK# <11,29>
R526 0_NC
+3.3V_RUN
25
U35
7SH32
COEX1_BT_ACTIVE_DC
COEX1_BT_ACTIVE_MINI
<24> COEX1_BT_ACTIVE_MINI
COEX1_BT_ACTIVE
COEX1_BT_ACTIVE <24>
R559 0_NC
51
+3.3V_RUN
J1
<29> BT_RADIO_DIS_DC#
PAD T28
USBP7_D+
GND
3.3V(Logic)
Radio Enable/Disable#
RSVD
USB+
Activity LED
COEX2
COEX1
USB-
GND
TYC_1566995-1
COEX1_BT_ACTIVE_DC
USBP7_D-
COEX2_WLAN_ACTIVE <24>
C190 0.1U/10V
C195 100P/50V
R108 10K
R123 10K
C193 33P/50V
16
USBP7_D+
USBP7_D-
L40
DLW21SN900SQ2B_NC
ICH_USBP7+ <12>
ICH_USBP7- <12>
R512 0
R513 0
Layout Note:
R512 and R513
close to choke
as possible to
minimize stubs.
QUANTA COMPUTER
Title
SWITCH & LED
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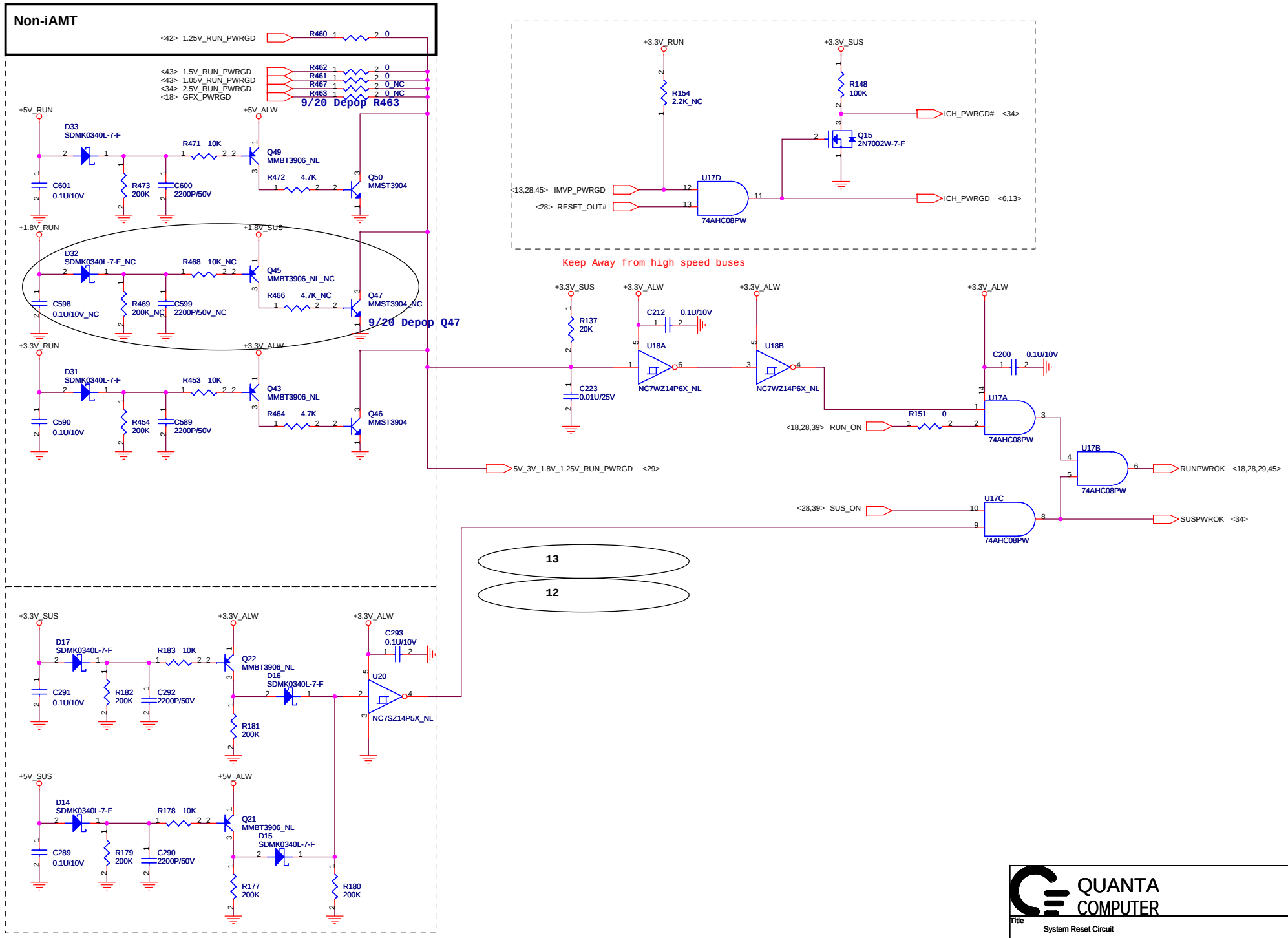
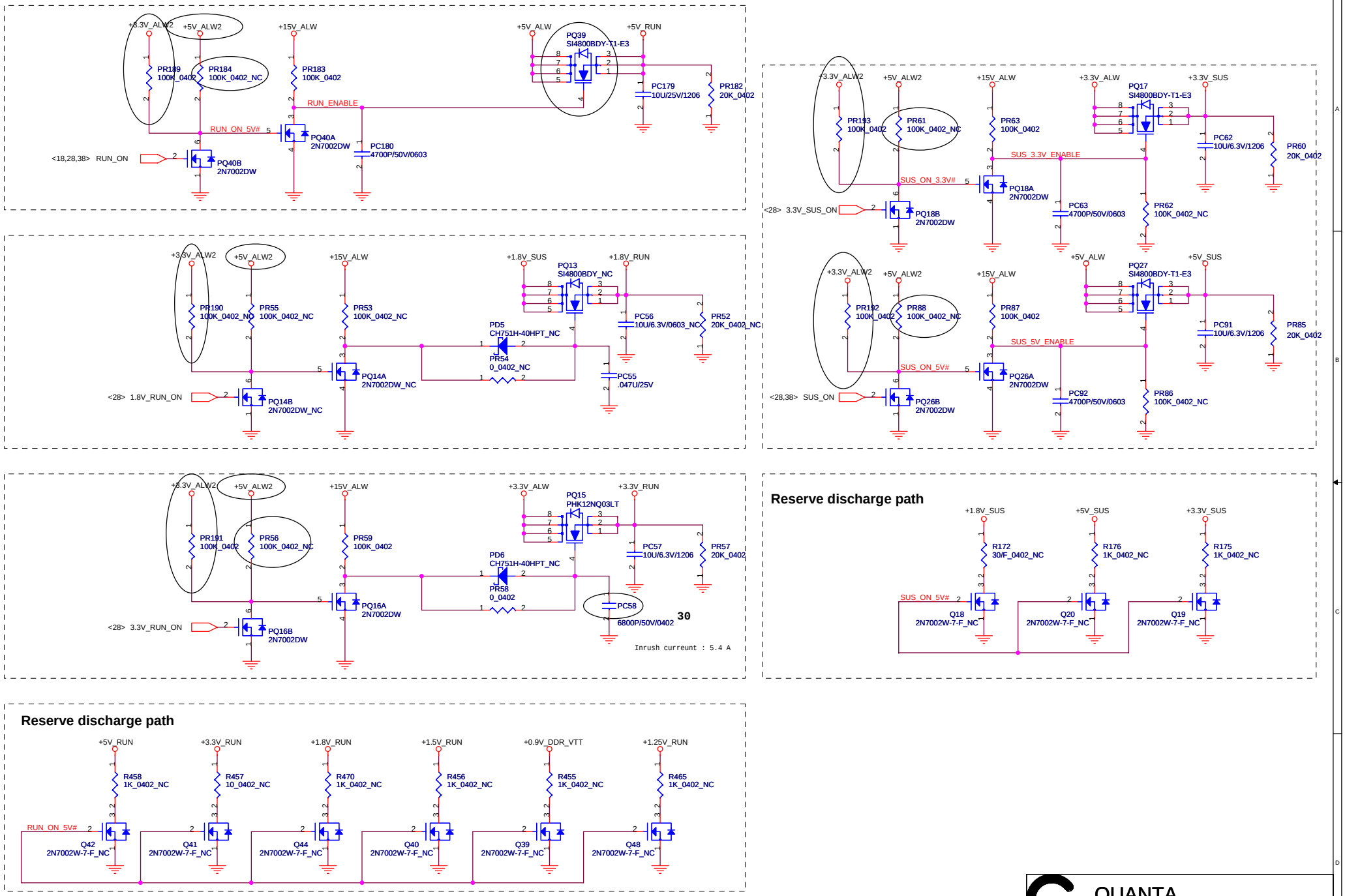


QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number M-08	Rev 0.1
Date: Monday, April 23, 2007	Sheet 38 of 52	



QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number M-08	Rev 0.1
Date: Monday, April 23, 2007	Sheet 39 of 52	

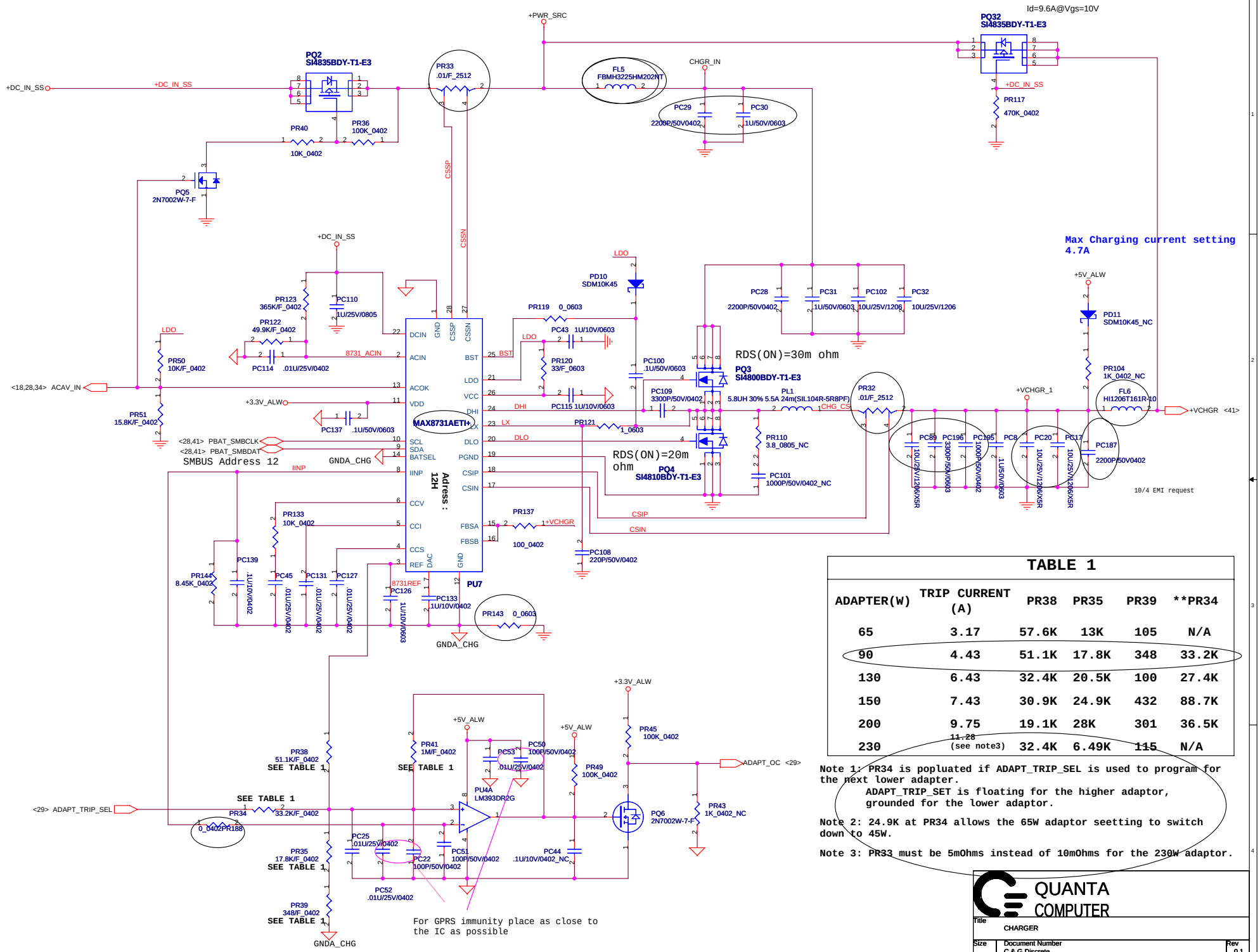


TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR38	PR35	PR39	**PR34
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

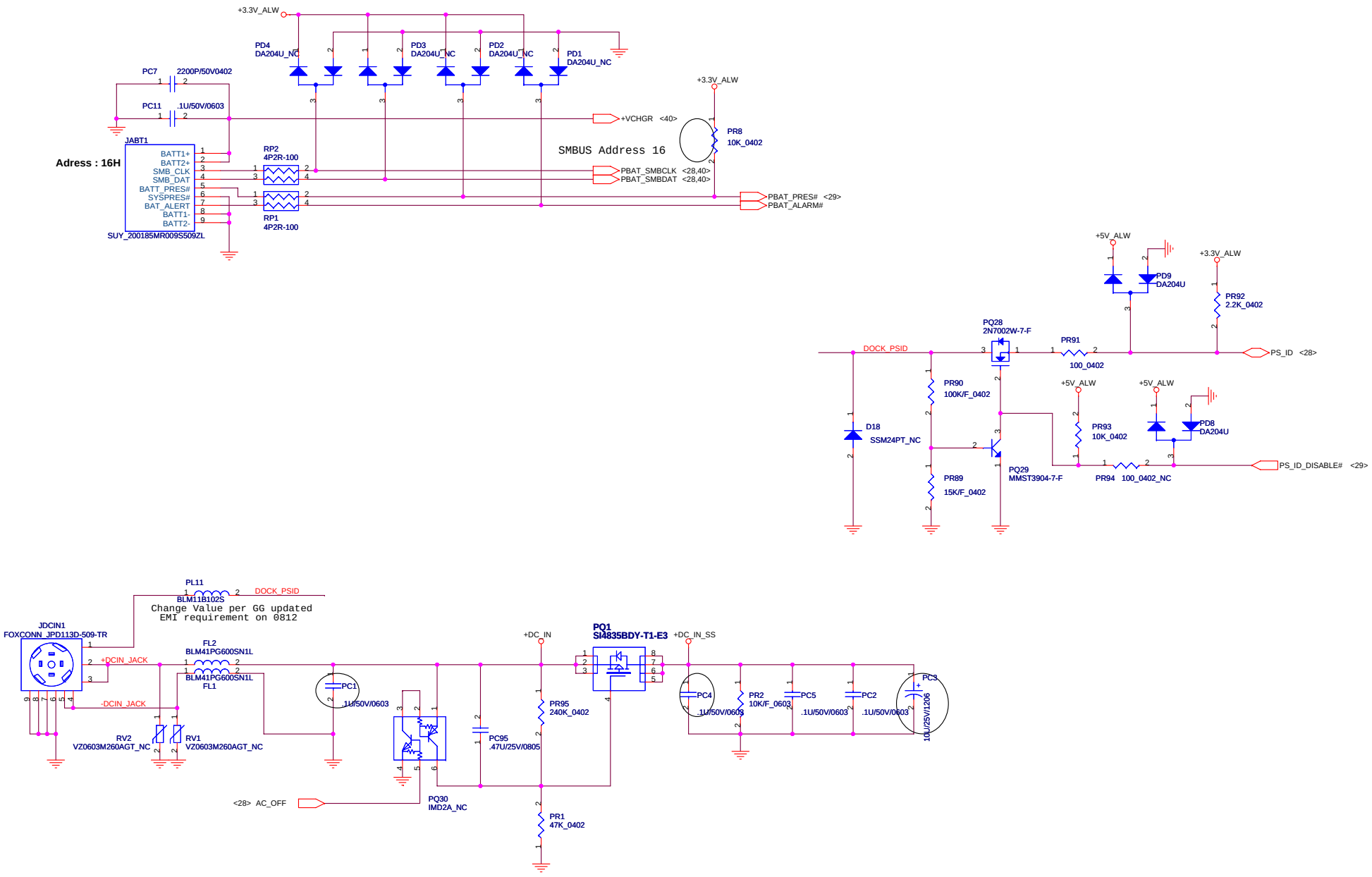
Note 1: PR34 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR34 allows the 65W adaptor seetting to switch down to 45W.

Note 3: PR33 must be 5mOhms instead of 10mOhms for the 230W adaptor.

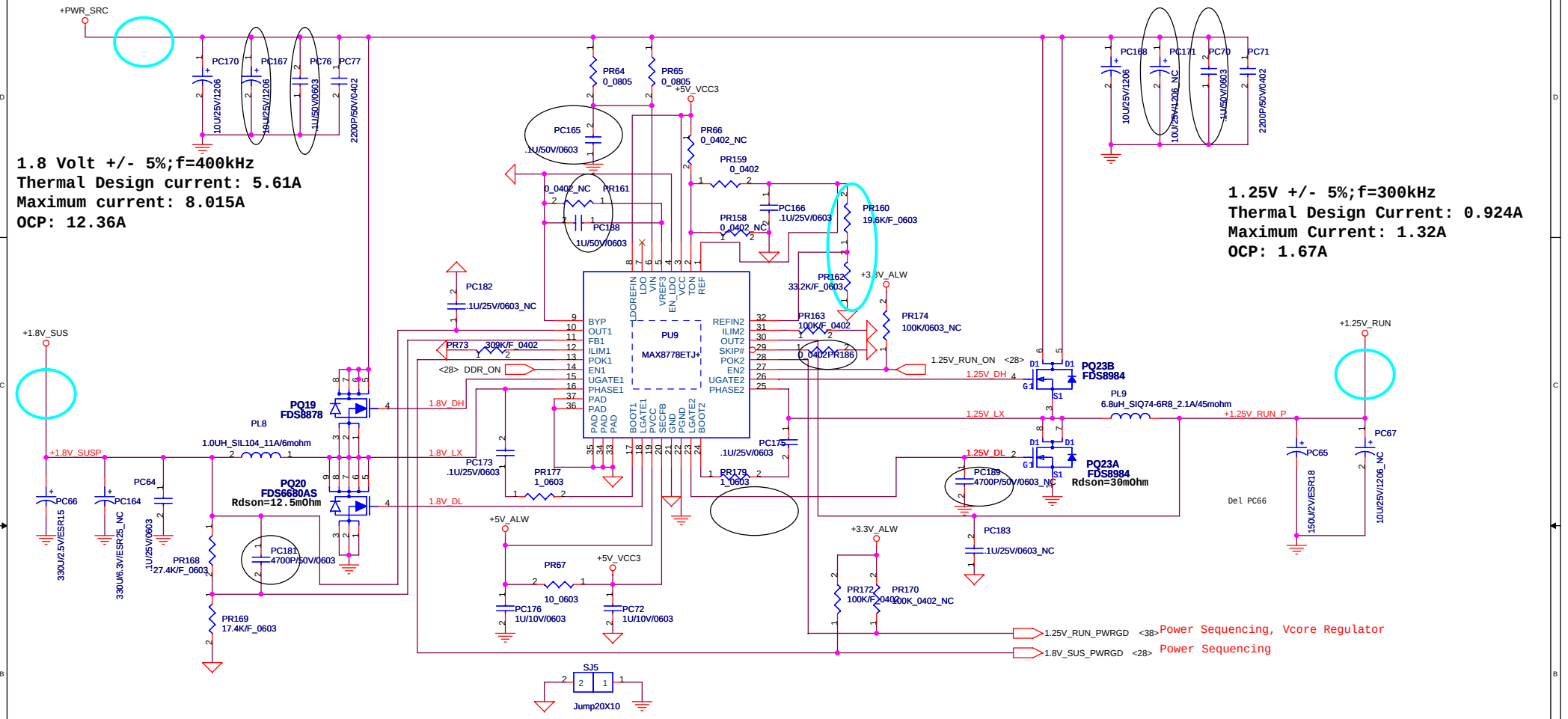
QUANTA COMPUTER

Title	CHARGER	
Size	Document Number C & G Discrete	Rev 0.1
Date: Monday, April 23, 2007	Sheet 40 of 52	

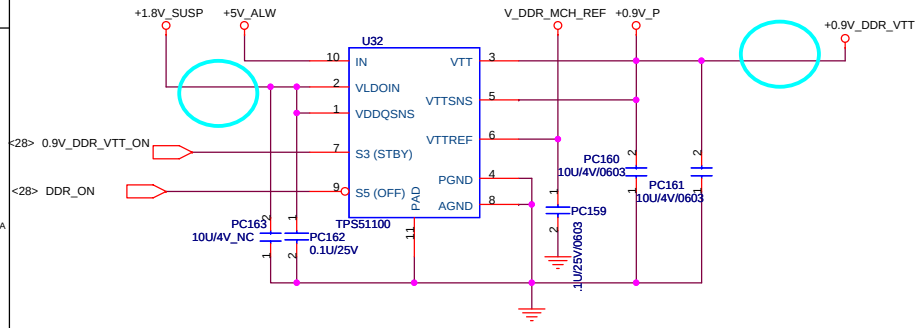


QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number C & G Discrete	Rev 0.1
Date: Monday, April 23, 2007	Sheet 41 of 52	



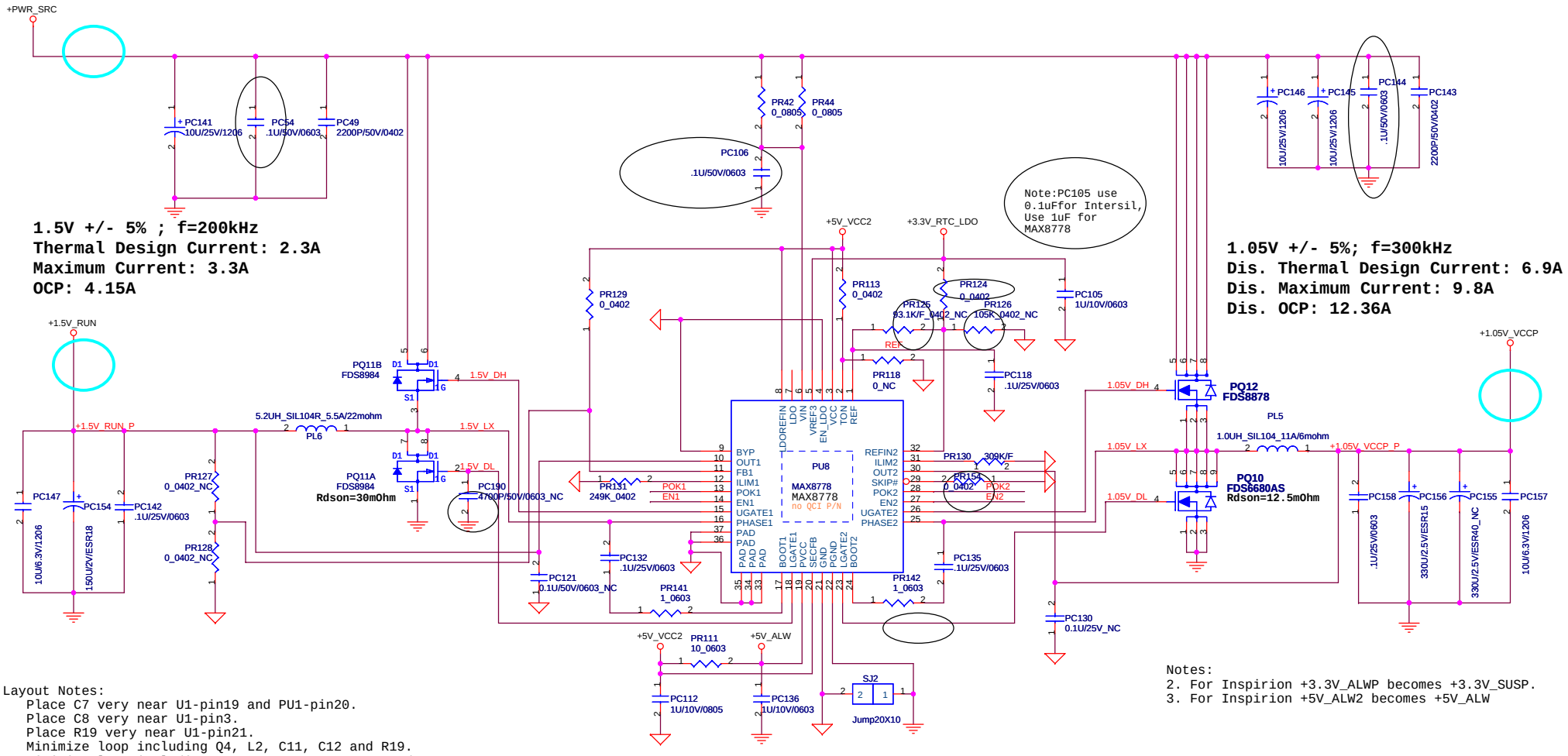
0.9V +/- 5%
Design current 1.05 A
Peak Current 1.5 A



QUANTA COMPUTER

Title	1.25V,1.05V,1.8V,0.9V	
Size	Document Number C & G Discrete	Rev 0.1
Date: Monday, April 23, 2007	Sheet 42 of 52	

+1.5V_RUN /+1.05V_VCCP /+3.3V_ALW /+3.3_RTC_LDO



Notes:
2. For Inspirion +3.3V_ALWP becomes +3.3V_SUSP.
3. For Inspirion +5V_ALW2 becomes +5V_ALW

Layout Notes:
- Place C7 very near U1-pin19 and PU1-pin20.
- Place C8 very near U1-pin3.
- Place R19 very near U1-pin21.
- Minimize loop including Q4, L2, C11, C12 and R19.
- Minimize loop including Q2, L3, C17, C18, C19 and R19.
- Route GNDA_DC2 using at least 25 mil trace width.
- Minimize GNDA_DC2 trace length.
- Place C15 near U1-pin7.
- Place C20 near U1-pin5.
- Place R7 near U1-pin11.
- Place R12 near U1-pin31.
- Place R3, C10 near U1-pins 24 and 25.
- Place R2, C9 near U1-pins 16 and 17.
- Route +1.05V_BOOT, +1.05V_BOOST, +1.5V_BOOT, +1.5V_BOOST using 25mil trace width and minimize lengths.
- Connect large copper fill areas to PQ1, PQ2, PQ3 and Q4 signals for thermal improvement.
- Minimize length of +1.5V_RUN_PL and +1.05V_VCCP_PL.
- Place C1, C2, C3, C22 very near Q3-pins 5, 6, 7, 8.
- Place C4, C5, C6, C23 very near Q1-pins 5, 6, 7, 8.
- Route +DC2_PWR_SRC using 50 mil trace width and minimize length.
- Route OUT1 and OUT2 away from inductor and switch-node. Sense Vout directly at output bulk cap.

QUANTA COMPUTER

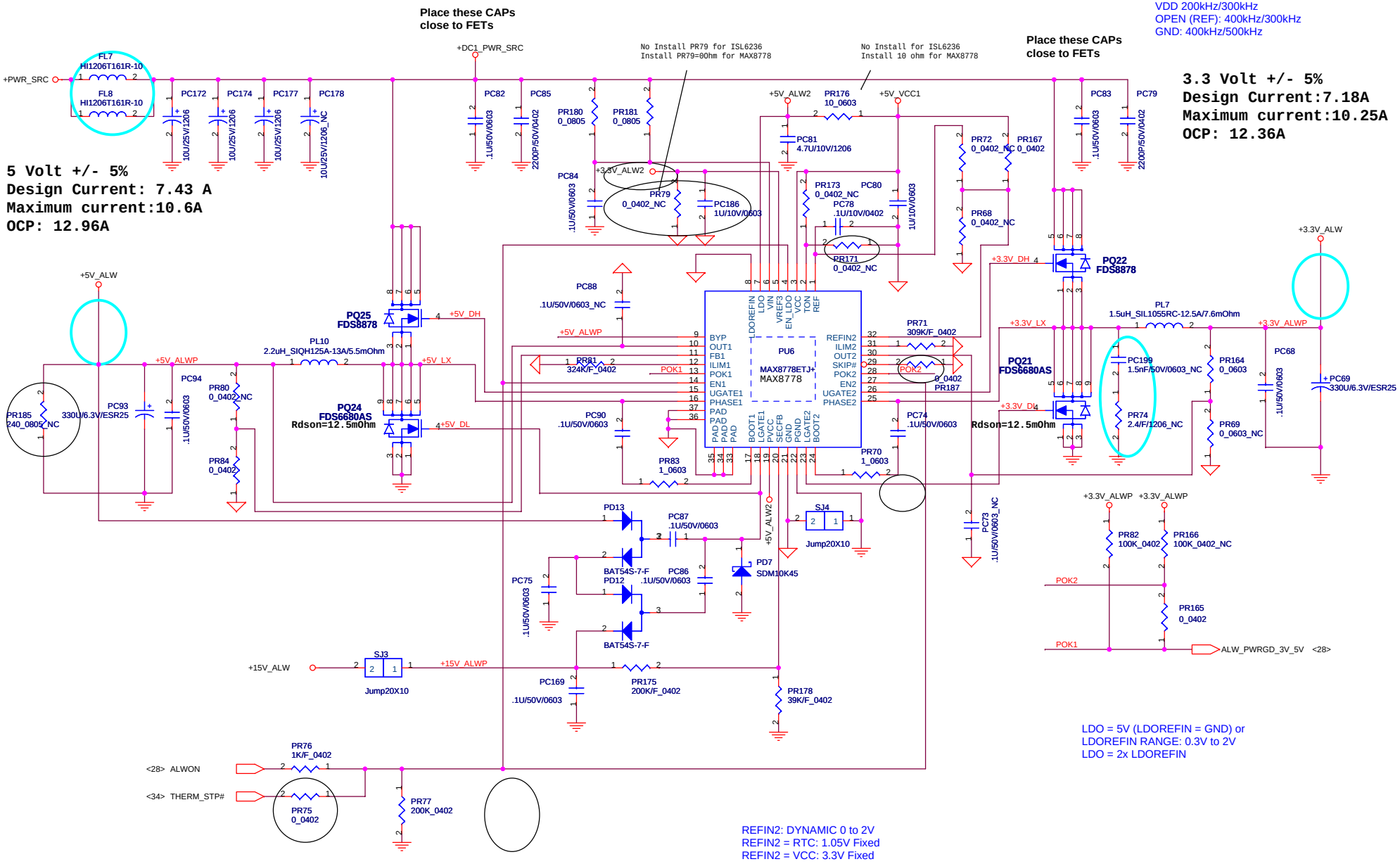
Title	1.5V,1.05V	
Size	Document Number C & G Discrete	Rev 1A
Date: Monday, April 23, 2007	Sheet 43 of 52	

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

Ton:OUT1/OUT2 Switching Frequency
VDD 200kHz/300kHz
OPEN (REF): 400kHz/300kHz
GND: 400kHz/500kHz

3.3 Volt +/- 5%
Design Current:7.18A
Maximum current:10.25A
OCP: 12.36A

5 Volt +/- 5%
Design Current: 7.43 A
Maximum current:10.6A
OCP: 12.96A

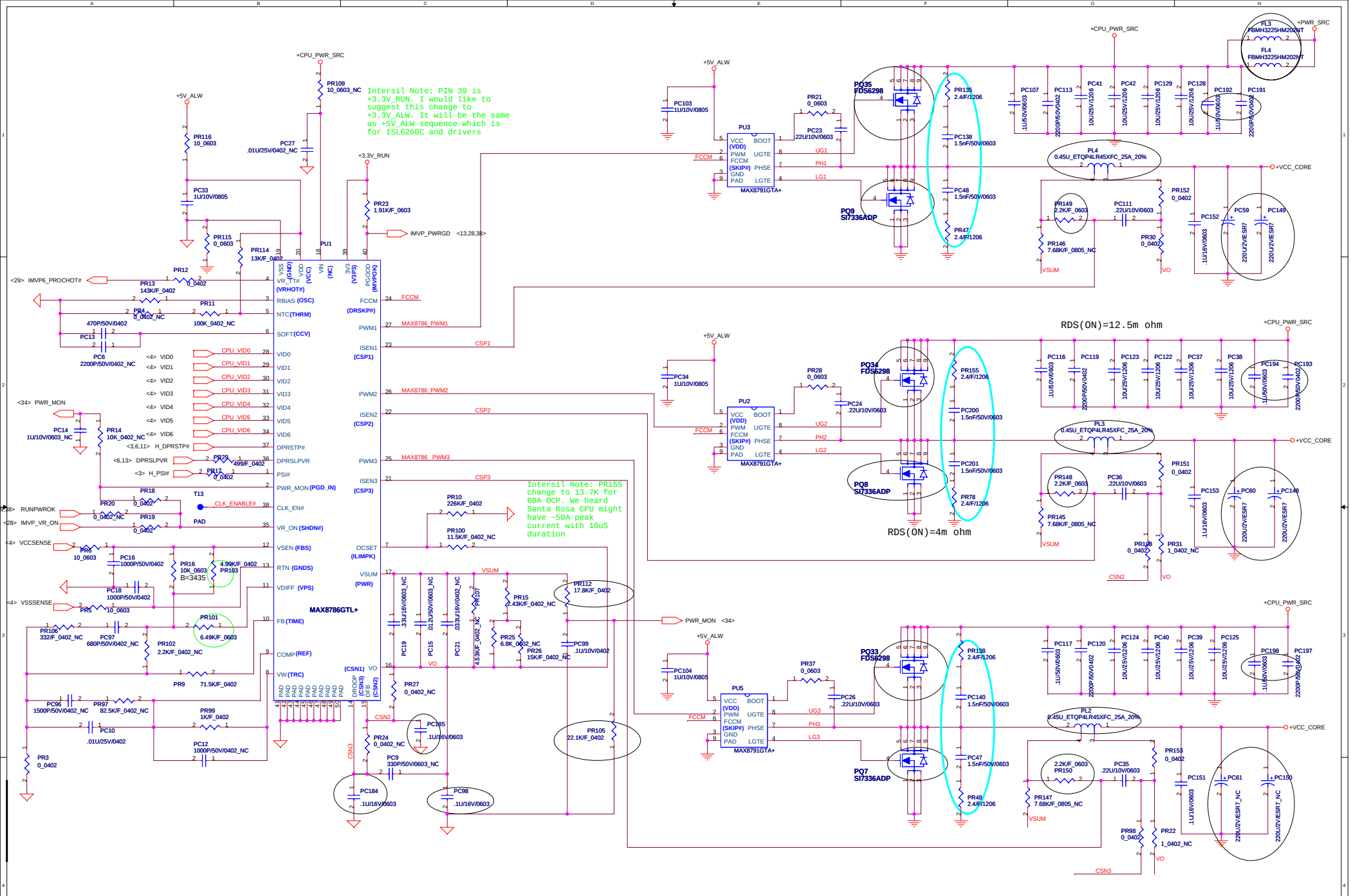


LDO = 5V (LDOREFIN = GND) or
LDOREFIN RANGE: 0.3V to 2V
LDO = 2x LDOREFIN

REFIN2: DYNAMIC 0 to 2V
REFIN2 = RTC: 1.05V Fixed
REFIN2 = VCC: 3.3V Fixed

QUANTA COMPUTER

Title	3VALW,5V,3V, power on	
Size	Document Number C & G Discrete	Rev 1A
Date: Monday, April 23, 2007	Sheet 44 of 52	



PHASE 3 populate

QUANTA COMPUTER

Title	CPU POWER		
Size	Document Number C & G Discrete		Rev 1A
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON		ON
S3	ON	ON	OFF		ON
S5 S4/AC	ON	OFF	OFF		ON
S5 S4/AC don't exist	OFF	OFF	OFF		ON

PCI TABLE

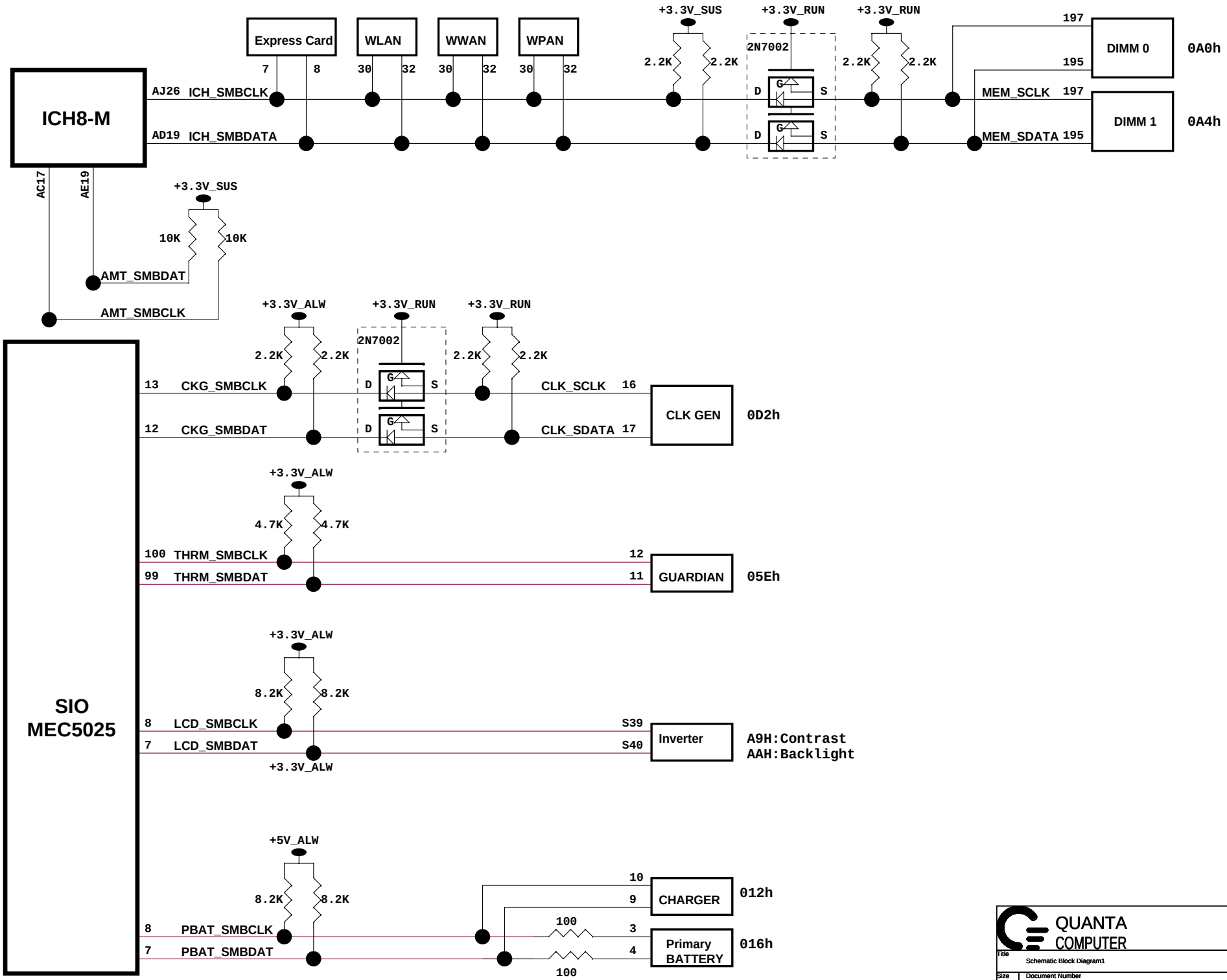
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
BCM4401B	AD16	REQ#0 / GNT#0	PIRQB
R5C833	AD17	REQ#1 / GNT#1	PIRQC: Card reader PIEQD: 1394

	USB PORT#	DESTINATION
ICH8-M	0	Right Top
	1	Right Bottom
	2	Side TOP
	3	Side Bottom
	4	Ext. USB TOP
	5	DIgital Camera
	6	Express Card
	7	WPAN/Bluetooth
	8	Ext. USB Bottom
	9	WWAN
ECE 5011	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None

QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number C & G UMA	Rev 1A
Date: Monday, April 23, 2007	Sheet 46 of 52	



QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number C & G UMA	Rev 1A
Date: Monday, April 23, 2007	Sheet 47 of 52	

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
C/G DISCRETE	1	39-45	7/13/2006					Update PWR schematics
	2	13,29	9/20/2006				S3 resume fail	Move PLTRST_DELAY# from EC to ICH8
	3	11	9/20/2006				2nd SATA HDD can't recognize	Move 2nd SATA from port 1 to port 2
	4	38	9/20/2006				Gfx card timing error	Disconnect GFX_PWRGD to system (Delete R463)
	5	38	9/20/2006				Gfx card timing error	Disconnect +1.8V_RUN detect circuit to system (Delete Q47)
	6	39-45	9/21/2006					Update PWR schematics
	7	23	9/21/2006					Add +1.8V_RUN for SATA buffer test (CON4.20-21-22-42-43-44)
	8	37	10/2/2006				Update WLAN LED implementation.With the current implementation, there is a possibility for backdrive from the WLAN LED control signal to +3.3V_RUN while in S3 / S4 / S5. With the voltage rail being +3.3V_WLAN, there is a high probability that the LED will be illuminated while in S3 / S4 / S5.	Please change the WLAN LED implementation to advice from Dell.
	9	13	10/2/2006				Intel has advised that the pull-up on LINKALERT# be depopulated and that the pull-up on GPIO14 be 8.2k. Please update.	Depop R247 & change R227 from 10K ohm to 8.2K ohm
	10	28,33	10/11/2006				In order to leverage the M07 implementation, the sniffer LED circuit needs to be modified. The MEC5025 pins are being changed from active high to active low.	Change back VC08 design, rename SNIFFER_YELLOW to SNIFFER_YELLOW#, SNIFFER_GREEN to SNIFFER_GREEN# and remove R507 and R510.
	11	28,29	10/11/2006				Move DOCK_SMB_PME from MEC5025 SGPIO37 to ECE5018/5011 GPIOC0.Move DOCK_SMB_ALERT# from ECE5018/5011 GPIOC0 to MEC5025 SGPIO37	DOCK_SMB_PME# should be pulled up to +3.3V_ALW DOCK_SMB_ALERT# should be pulled up to +5V_ALW
	12	28,38	10/11/2006				Add ATI_Intel to MEC5025 pin 14 and tie to GND.This connection should be labeled ATI_Intel.	Remove 3.3V_LAN_PWRGD circuit from page 38 Delete 3.3V_LAN_PWRGD from MEC5025 pin 14 Add a connection from the MEC5025 pin 14 and tie to GND.
	13	28	10/11/2006					Move ALW_PWRGD_3V_5V from MEC5025 pin 18 to pin 29
	14	13	10/11/2006					1) Move SIO_EXT_SCI# from ICH pin AG22 to ICH pin AC19 2) Delete R242 (delete DOCKED# signal)
	15	13	10/11/2006					Reserve LOM_SMBALERT# (ICH8 AG22) & PU resister
	16	24	10/16/2006					Change WPAN USB port from USBP7 to USBP4
	17	23,29	10/18/2006				Modify HDDC_EN and MODC_EN Circuits to Resolve Glitch Issue. unintentionally for a brief moment.With the current Dawson design, it has been shown that the +15V_ALW rail comes up before the +3V_ALW rail on the original HDDC_EN and MODC_EN circuits. This can cause a momentary glitch at the gate of the power FET, which may cause the FET to turn on unintentionally for a brief moment.	To resolve this issue, please use the HDDC_EN and MODC_EN circuits that are attached below. These new circuits resemble closely our other load switch circuits, but require an additional FET and changes the sense of the HDDC_EN and MODC_EN signals to active high. Please note the use of +5V_ALW2 on these circuits. The +5V_ALW2 voltage comes directly from the LDO output on the 3V/5V switcher in your M08 design.
	18	12,14	10/18/2006				WWAN Noise - ICH improvements. Add one .1 uF cap on each USB OC (over current) trace near the ICH. Add four .1uF caps in parellel to C813 close to the ICH pins. Add four .1uF caps in parellel to C825 close to the ICH pins.	Add C871~C878 for USB OC. Add C867~C870 in parellel to C825. Add C748,C864~C866 in parellel to C813.
	19	37	10/23/2006				Use LED_MASK# to control BT LED to prevent leakage	Add R336 & change Q13 to BJT
	20	34	10/23/2006				Change pull-up rail on 5V_CAL_SIO1# to +3.3V_SUS. Feedback from SMSC has indicated that the pull-up rail on 5V_CAL_SIO1# needs to change from +5V_SUS to +3.3V_SUS.This is necessary because the GPIO on the EMC4001 is 3V tolerant, not 5V.	Pullup is at reference designator R298.
	21	28	10/23/2006				Due to the power on defaults of the MEC5025, the pull-downs on the KSI lines of the MEC5025 need to be stronger, to avoid pulses from powering on certain power rails. Please do the following: 1. Change pull-down on SUS_ON to 2.7k 2. Change pull-down on RUN_ON to 2.7k	Change R355,R358 to 2.7K
	22	24	10/23/2006				Add SMBus isolation circuitry for WLAN.Add isolation circuitry for SMBus on WLAN.	

QUANTA COMPUTER

Title	Change List		
Size	Document Number JM7B		Rev 1A
Date:	Monday, April 23, 2007	Sheet 49 of 1	

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
C/G *DISCRETE*	23	17	10/26/2006				Chipset side spec. Differetial CLK raise/fall slew rate is 2.5~8 V/ns, only express card and mini card is 0.6~4V/ns. BITCLK rise/fall slew rate in 1-3 V/ns &	Change serial resistors (PR4,PR5,PR10,PR12,PR13) to meet the CLK SPEC
	24	37	10/26/2006				Change LED control method	
	25	37	10/26/2006				Add OR gate for BT_ACTIVE	
	26	13	10/26/2006				M08 GPIO A14 update. Original EC5011 pin66 CCD_VDD_ON move to IC8 pinAD10 GPIO48 and add 100K ohm pull down.	Move CCD_VDD_ON from EC5011 pin66to IC8 pin AD10 GPIO48 and add 100K ohm pull down.
	27	25	10/26/2006				For Comm team suggestion (GG list), pop C217 for WWAN	
	28	39 - 45	10/31/2006				PWR team updat schemtics - 10/23	

QUANTA COMPUTER

Title	Change List	
Size	Document Number JM7B	Rev 1A
Date: Monday, April 23, 2007	Sheet 50 of 1	

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	
C/G DISCRETE	29	24 - 25	11/1/2006				For EMI request, add RC circuit for Mini card clk request	Add R543, C880, R186, C649, R544, C181
	30	39	11/1/2006				For +3.3V_RUN inrush current, it may over OCP (12.36 A)	Change PC58 from 470 pF to 6800 pF
	31	32	11/3/2006				For AP - THN+D fail, change C306, 307 to 0.033uF/16V/X7R/1206 & C326, C329 to 1uF/16V/X7R/1206	Change C306, 307 to 0.033uF/16V/X7R/1206 & C326, C329 to 1uF/16V/X7R/1207
	32	32	11/3/2006				'PO' noise in resume from S3,S4,S5	Reserved the AUD_AMP_MUTE# for 'PO' noise
	33	39 - 45	11/09/2006				PWR team updat schemtics - 11/08	
	34	17	11/09/2006				Change R44 to 2.2K per Intel recommend value.	
	35	12 - 13	11/21/2006				Due to Intel-ICH8 uses GPIO20 pin AE11 as an Internal Strapping at power up	Move PCIE_MCARD2_DET# from GPIO20 to ICH8 GPIO5/PIRQH# pin B3.
	36	13	11/21/2006				GPIO18 is default as an output at power up, it will drive 1Hz output at power up. Per Intel this GPIO could not be connected to GND	Add 4.7K series - R547 resistor to separate it
	37	32	11/22/2006				There is potential back drive from the codec DVdd back to the AVdd supply due to an internal ESD diode	add 100kohm resistor (R253) between pin 40 and +3.3V_RUN and a 1000pF cap (C643 below) from Pin 40 to ground
	38	35 - 36	11/28/2006				GG list -- COMM team request	1.Change capacitor for U5 pin 79, 94,106 (VDDIO) (C18, C16, C25) to 47pF. 2.Change those three capacitors (C27, C37,C34) to 47pF 3.Add C644 - 47pF capacitor by the pin 57 of U5 4.Change L7 to 0805 package -BK2125LM152. & C23 to 47 pF 5.Add Ferrite Bead BK1608LM152 on 1.8V to EPHY_AVDD pin 57
	39	28-29	11/28/2006				Move DOCK_SMB_PME from MEC5025 SGPIO37 to ECE5018/5011 GPIOC0.Move DOCK_SMB_ALERT# from ECE5018/5011 GPIOC0 to MEC5025 SGPIO37	DOCK_SMB_PME# should be pulled up to +5V_ALW DOCK_SMB_ALERT# should be pulled up to +3.3V_ALW
	40	24	12/01/2006				GG list -- Seperate debug port with MINI-PCI if not necessary	Add 4 0ohm resistors for these pins
	41	24 - 25	12/01/2006				GG list -- Delete decoupling cap	Delete C222 & C424
	42	39 - 45	12/04/2006				PWR team updat schemtics - 12/04	
	43	32	12/08/2006				GG List -- Change audio AMP to TI solution	1.Change codec to TPA9040A4 2.Pop R505, C619 & C614; depop R506, R504 & R497
	44	31	12/13/2006				GG List -- Change power source for LED of dash board	Change JTP1.9 from +3.3V_RUN to +5V_ALW
	45	39 - 45	12/19/2006				PWR team updat schemtics - 12/19	
	46	28	12/25/2006				GG List -- Remove EC5025 pin15 GPIO4 AUD_AMP_MUTE# circuit.	NC R538
	47	34	12/25/2006				GG List -- Add THERMATRIP_VGA# function	Pop R441,442,443 and Q35, C568 for THERMATRIP_VGA# trip.
	48	33	12/28/2006				Modify CCD power control soft start function	Change C403 , R284 connect method

QUANTA COMPUTER

Title	EMI & Screw hole	
Size	Document Number C & G UMA	Rev 2A
Date: Monday, April 23, 2007	Sheet 50 of 52	

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
C/G DISCRETE	49	22	1/11/2006				XD card detect function error	
	50	29	1/11/2006				Base on A16 GPIO : Change net name from BID2 to CHIPSET_ID1	
	51	37	1/24/2007				Add 0ohm_NC(R571) resistor pad connected from Coex1_BT_Active_MINI to Coex1_BT_Active	
	52	32	1/24/2007				Audio solution for pass EMI 225MHz and 451MHz radiation emission test.	Added R560, R561, R562 and R563 on AUD_SPK_L1, AUD_SPK_L2, AUD_SPK_R1, AUD_SPK_R2 trace
	52	33	1/24/2007				Audio solution for pass EMI 225MHz and 451MHz radiation emission test.	Added R564, R565, R566 and R567 on AUD_LINE_OUT,AUD_HP_OUT
	53	13	1/24/2007				GG List -- CCD_ON pull down R258 100K NC.	
	54	37	2/5/2007				Blue LED brightness is too high	Change R30,R50,R75,R64 & R36 from 220 ohm to 330 ohm
	55	30	2/12/2007				Prevent SPI CLK overshoot/undershoot issue	Add C896 for RC circuit but not pop it
	56	39 - 45	2/12/2007				PWR team updat schemtics - 2/12	
	57	29	2/12/2007				GG List -- CIR function intermidiate issue	ECE5021 pin7 PWRGD need to pull-down to GND with 0 ohm - Add R568 PD resistor & R569 series resistor (NC)
	58	44	3/1/2007				PWR team updat schemtics - 3/1	
	59	17	3/2/2007				Per TDC COMM team request - Change L65 to BLM18SG260	Fine tune 14M CLK - Change R57 from 33 to 15 ohm & L65 to BLM18SG260
	60	04	3/2/2007				Per reliability issue - Move C98 to C249	De-pop C98 & pop C249

QUANTA COMPUTER

Title	EMI & Screw hole	
Size	Document Number C & G UMA	Rev 2A
Date: Monday, April 23, 2007	Sheet 51 of 52	

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
C/G *DISCRETE*	61	13	04/10/2007				M08 NBEE Issue/Change Alert: Unused ICH8M GPIO pullups when defaulting as inputs on power-up GPIO10 pullup to +3.3V_SUS.	Add PU resistor R591
	62	13,33	04/10/2007				Removed CCD_VDD_ON control circuit	Populate R258,R34. Depopulate R557,R284,C403,Q26,Q27.
	63	12	04/10/2007				Fine tune PLTRST#,PLTRST1#,PCI_RST# signals to reduce glitch	Add 33 ohm (R588, R589, R590)
	64	39 - 45	4/19/2007				PWR team updat schemtics - 4/19	
	65	14	4/19/2007				Reserve Al-cap for acoustics test	Add C652
	66	33	4/19/2007				Per EMI request - Add bead to get more tolerance for noise margin	Add L68 & L69; Remove C650 & C651 (for layout concern)

QUANTA COMPUTER

Title	EMI & Screw hole	
Size	Document Number C & G UMA	Rev 2A
Date: Monday, April 23, 2007	Sheet 52 of 52	

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
C/G *DISCRETE*	67	5-10	05/21/2007				Crestline chipset PM965 on discrete MM# will be changed.	Change U19 P/N to AJSLA5U0T11 from AJSLA5U0T01.
	68	14	05/21/2007				1. For Intel confirm the ICH8 5VREF_RUN & 5VREF_SUS waveform had swing. For solved this issue need change resistor from 10ohms to 100ohms and Cap change from 0.1uF to 1uF. 2. The original design not any function impact in C&G, but Dell wish QCI change design for follow up Intel request.	1. Change C104 & C144 to 1uF (P/N:CH5102M9B07) 2. Change R56 to 100 ohm (P/N:CS11002JB32)

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