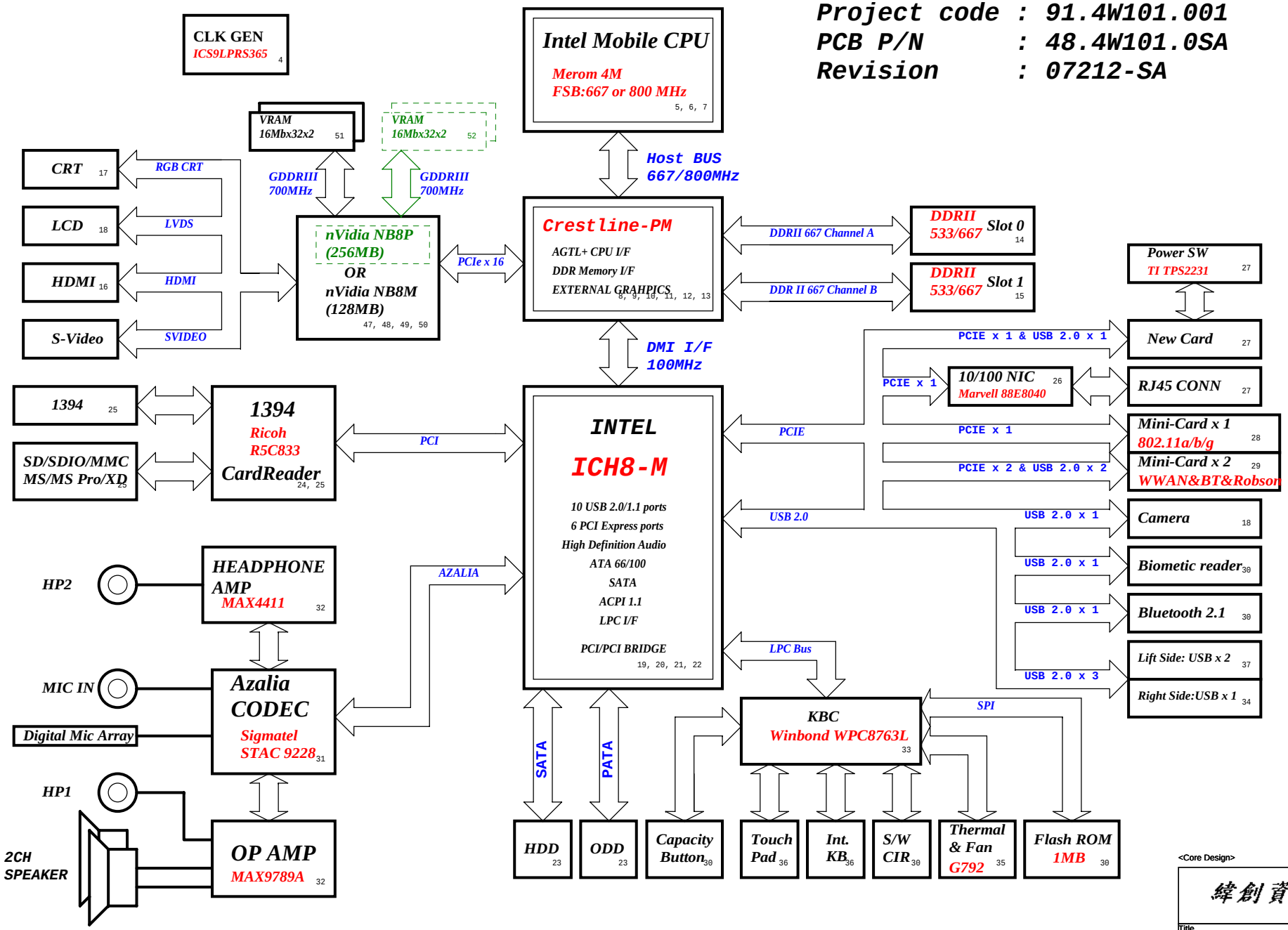
Hawke Intel Discrete Block Diagram

Project code : 91.4W101.001
PCB P/N : 48.4W101.0SA
Revision : 07212-SA



BATTERY CHARGER MAX8731A 38	
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC TPS51120 39	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS5117 42, 43	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC TPS51100 44	
INPUTS	OUTPUTS
1D8V_S3	0D9V_S3

SYSTEM DC/DC RT9018 44	
INPUTS	OUTPUTS
1D8V_S3 1D8V_S3	1D5V_S0 1D25V_S0

VGA DC/DC TPS5117 53	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFX_CORE_S0

CPU DC/DC ISL6262A 40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

PCB LAYER

L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Singal
L7:GND
L8:BOT

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **System Block Diagram**

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Date: Tuesday, May 08, 2007 Sheet 1 of 55

Adapter

Input Signal (I)	Output Signal (O)
AD_OFF	AD_IN
Input Power	**Output Power**
AD_JK	VCC(I)
5V_AUX_S5	VCC(I)
	VCC(O)
	AD+

Charger_ISL6255

Input Signal	Output Signal
CHARGE_OFF	CLS (I / 3.3V)
BT_TH	THM (I / 3.3V)
BAT+SENSE	BATT (I / 3.3V)
BT_SCL_5	SCL (IO / 5V)
BT_SDA_5	SDA (IO / 5V)
FLASH_GPIO1	RESET#/PB5 (I/5V)
FLASH_GPIO2	PB0/MOSI/AIN0
AC_IN	PB0/MOSI/AIN0
	LDO (O / 5.4V)
	XTAL2/PB4 (O/5V)
	XTAL1/PB3 (O/5V)
Input Power	**Output Power**
AD+	DCIN (I)
	VCC (O)
	VCC (O)
	AD_IN
	CHARGE_LED#
	BL2#
	DCBATOUT
	BT+

TI TPS51120 3D3V/5V

Input Signal	Output Signal
3V/5V_EN	51120_EN2 FOR 3.3V
3V/5V_EN	51120_EN1 FOR 5.0V
	PGOUT(OD / 5V)
	CPUCORE_ON
Input Power	**Output Power**
DCBATOUT	VIN
5V_AUX_S5	REG5V_IN(I / 5V)
	5V(O)
	3D3V(O)
	5V_AUX_S5
	3D3V_AUX_S5
	5V_S5 (6A)
	3D3V_S5 (5A)

TPS51117 1D8V

Input Signal	Output Signal
PM_SLP_S4#	EN_PSV(I / 5V)
	(O)
	CPUCORE_ON
Input Power	**Output Power**
5V_S5	VCC
DCBATOUT	VIN
	(O)
	1D8V_S3(19A)

TPS51117 1D05V

Input Signal	Output Signal
PM_SLP_S3#	EN_PSV(I / 5V)
	(O)
	CPUCORE_ON
Input Power	**Output Power**
5V_S5	VCC
DCBATOUT	VIN
	(O)
	1D05V_S0(5A)

TI TPS51100 0.9V/DDR_VREF_S3

Input Signal	
PM_SLP_S4#	S5
PM_SLP_S4#	S3
Input Power	**Output Power**
5V_S5	VCC(I)
1D8V_S3	VN(I)
	VCC(O)
	VCC(O)
	DDR_VREF_S3
	DDR_VERF_S0

RT9018A 1D5V

Input Signal	Output Signal
PM_SLP_S3#	EN(I / 5V)
	(O)
	CPUCORE_ON
Input Power	**Output Power**
5V_S5	VCC
1D8V_S3	VIN
	(O)
	1D5V_S0(2.2A)

RT9018A 1D25V

Input Signal	Output Signal
PM_SLP_S3#	EN(I / 5V)
	(O)
	CPUCORE_ON
Input Power	**Output Power**
5V_S5	VCC
1D8V_S3	VIN
	(O)
	1D25V_S0(2.7A)

TPS51117 VGA_CORE

Input Signal	Output Signal
PM_SLP_S3#	EN_PSV(I / 5V)
	(O)
	CPUCORE_ON
Input Power	**Output Power**
5V_S5	VCC
DCBATOUT	VIN
	(O)
	VCC_GFX_CORE_S0 (18.4A)

ISL6262A CPU_CORE

VID Setting	Output Signal
CPU_VID0	VID0(I / 3.3V)
CPU_VID1	VID1(I / 3.3V)
CPU_VID2	VID2(I / 3.3V)
CPU_VID3	VID3(I / 3.3V)
CPU_VID4	VID4(I / 3.3V)
CPU_VID5	VID5(I / 3.3V)
CPU_VID6	VID6(I / 3.3V)
	VROK()
	VGATE_PWRGD
Input Signal	**Output Power**
CPUCORE_ON	EN (I / 3.3V)
	VCC_CORE_PWR(O)
	VCC_CORE_S0 (Imax=47A)
Voltage Sense	
VCC_SENSE	VSEN(I / Vcore)
VSS_SENSE	RGND(I / Vcore)
Input Power	
DCBATOUT	VCC(I)
5V_S0	VCC(I)
3D3V_S0	VCC(I)

<Core Design>

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Title: **Power Block Diagram**

Size	Document Number	Rev
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INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD/tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3: low = A16 swap override enable
high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN: High=Enable Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP: High=Enable Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR: LOW = Defaule
High=No Reboot

8.2K PULL HIGH

20,22 +RTCVCC → +RTCVCC
5,6,7,8,10,11,12,20,22,33,42,46 1D05V_S0 → 1D05V_S0
8,11,22,44,47,48,49 1D25V_S0 → 1D25V_S0
26 1D2V_LAN_S5 → 1D2V_LAN_S5
27 1D5V_NEW_S0 → 1D5V_NEW_S0
6,11,20,21,22,27,28,29,44 1D5V_S0 → 1D5V_S0
8,11,12,14,15,43,44,45,46 1D8V_S3 → 1D8V_S3
26,27 2D5V_LAN_S5 → 2D5V_LAN_S5

20,30,33,35,38,39,46 3D3V_AUX_S5 → 3D3V_AUX_S5
26,27 3D3V_LAN_S5 → 3D3V_LAN_S5
4,8,11,14,15,16,18,19,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,40,42,45,46,47,49,50,53 3D3V_S0 → 3D3V_S0
19,21,22,26,27,30,37,39,45,46 3D3V_S5 → 3D3V_S5
18,38,39,46 5V_AUX_S5 → 5V_AUX_S5

16,17,18,22,23,30,32,34,35,36,40,44,45,46 5V_S0 → 5V_S0
22,29,30,34,36,37,39,42,43,44,45,53 5V_S5 → 5V_S5
37,38,46 AD+ → AD+
18,38,39,40,41,42,43,45,46,53 DCBATOUT → DCBATOUT
14,15,44,46 DDR_VREF_S0 → DDR_VREF_S0
8,14,15,44 DDR_VREF_S3 → DDR_VREF_S3

18 +LCDVDD → +LCDVDD
6,7,41 VCC_CORE_S0 → VCC_CORE_S0

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal ★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order) ★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation ★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

<Core Design>

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Title: Table of Content

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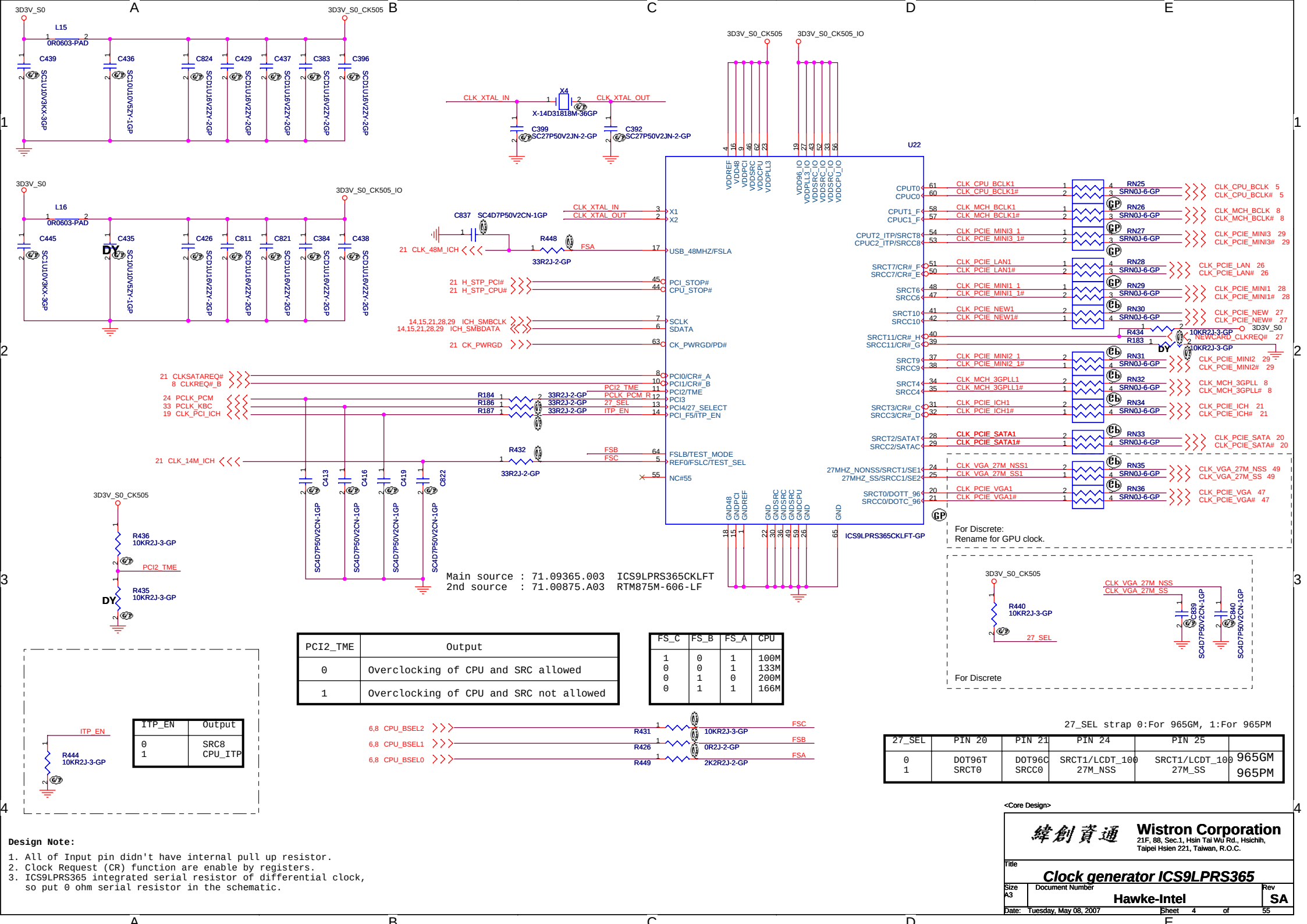

Main source : 71.09365.003 ICS9LPRS365CKLFT
2nd source : 71.00875.A03 RTM875M-606-LF

PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M

ITP_EN	Output
0	SRC8
1	CPU_ITP

27_SEL strap 0:For 965GM, 1:For 965PM

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25	
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100	965GM
1	SRCT0	SRCC0	27M_NSS	27M_SS	965PM

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. ICS9LPRS365 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Core Design>

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Title: Clock generator ICS9LPRS365

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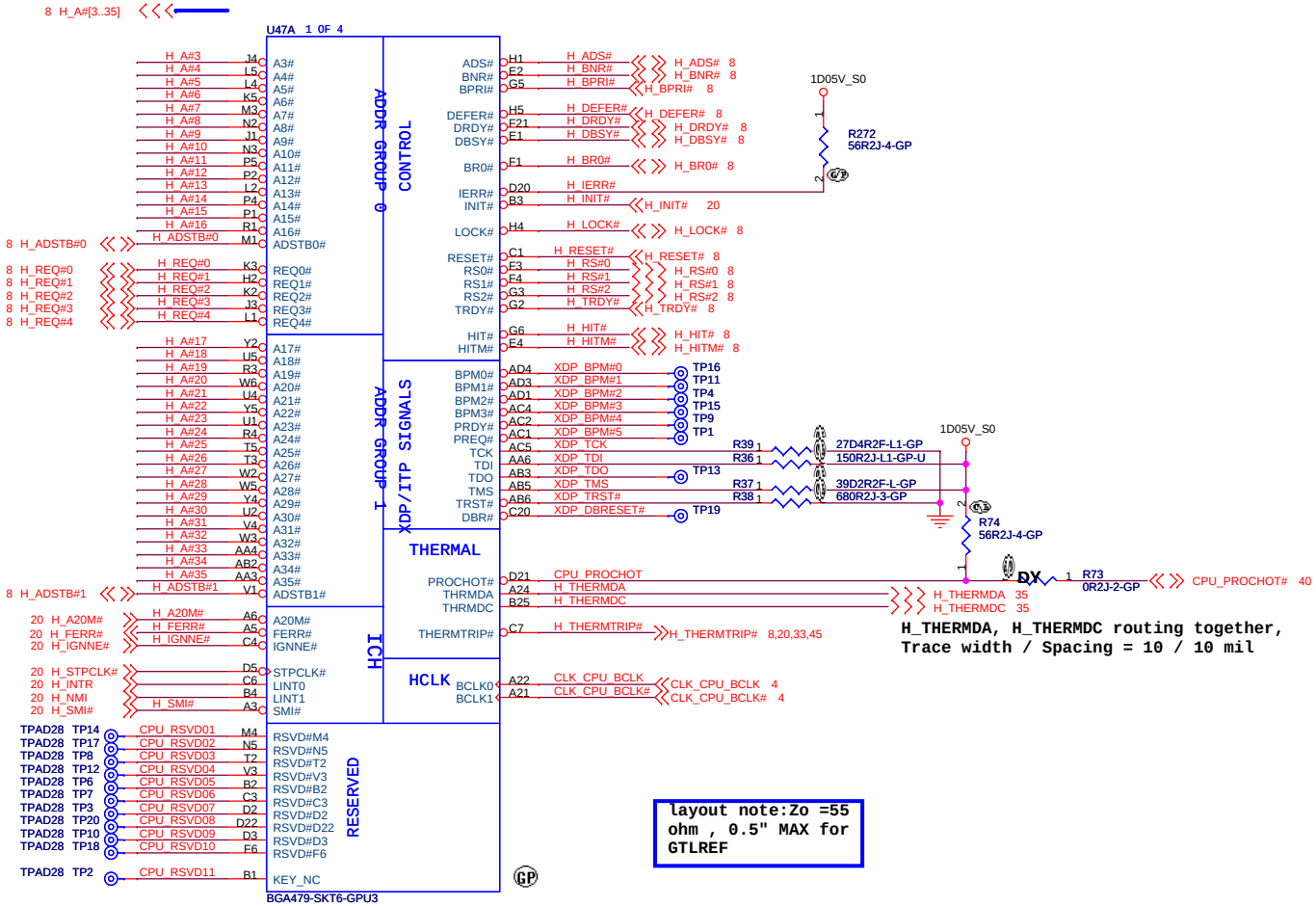

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Title: Meron(1/3)-AGTL+/XDP

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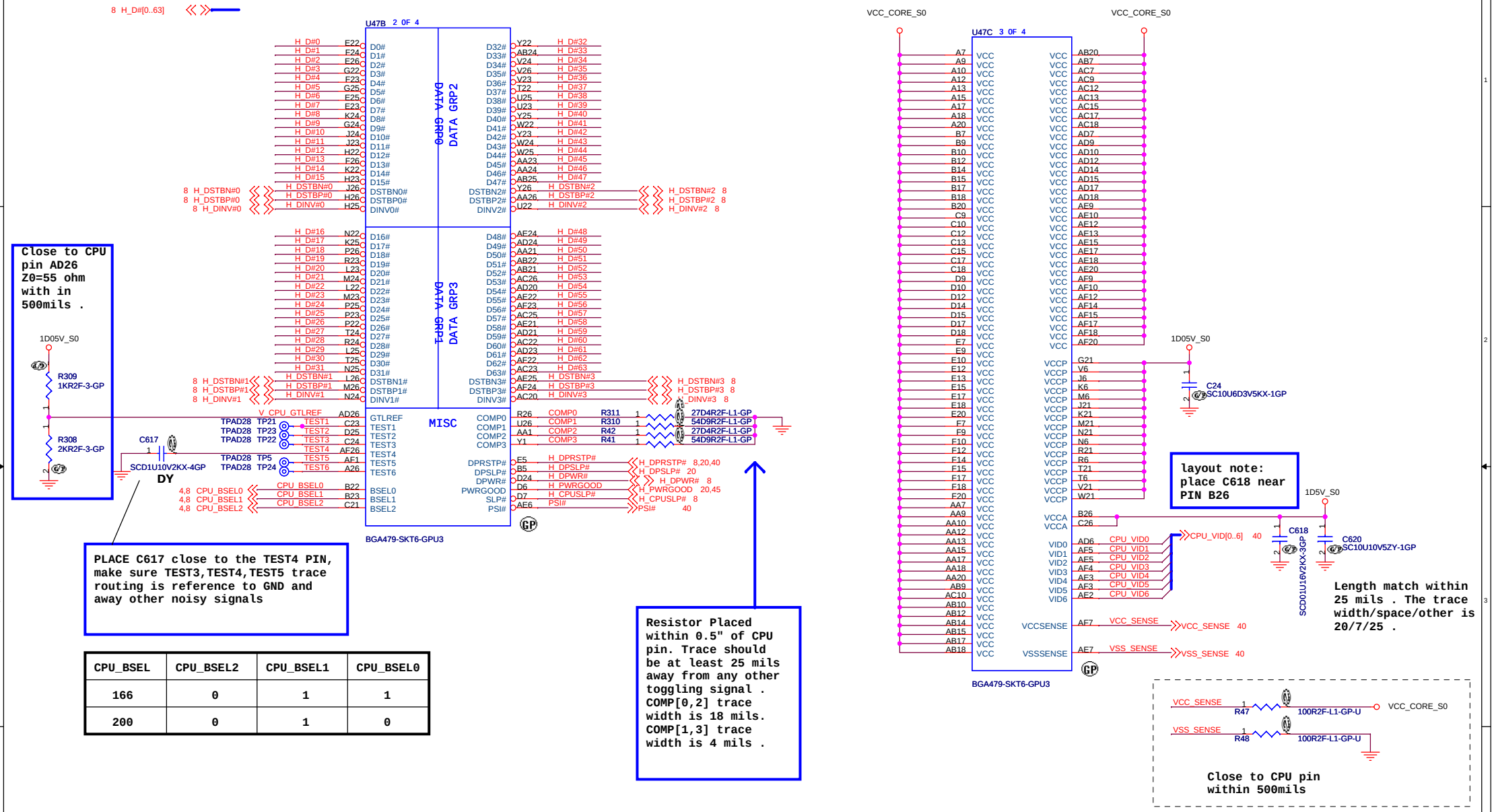

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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Title: ***Meron(2/3)-AGTL+/PWR***

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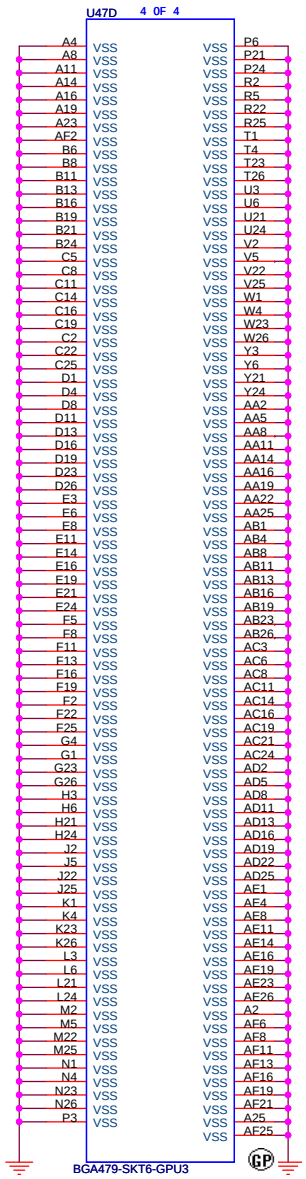

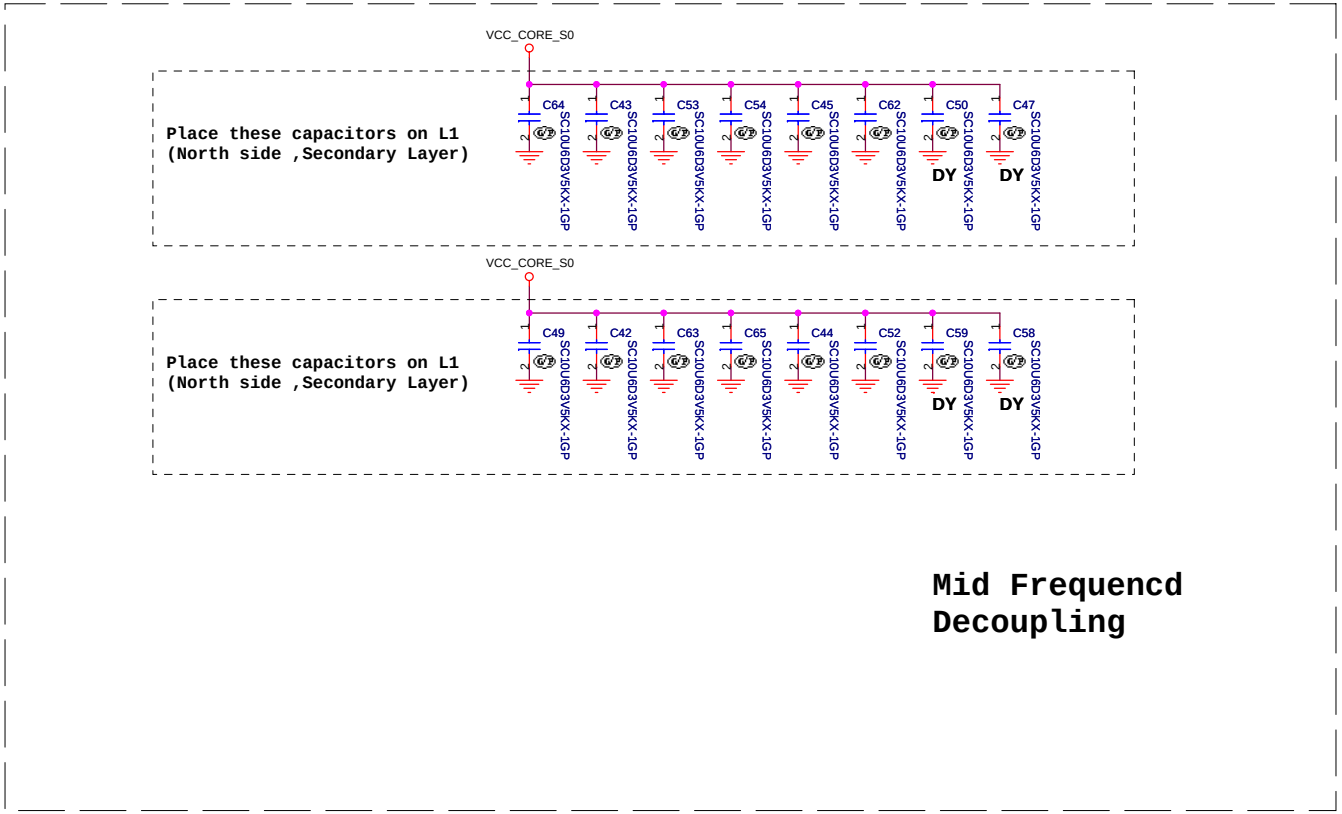

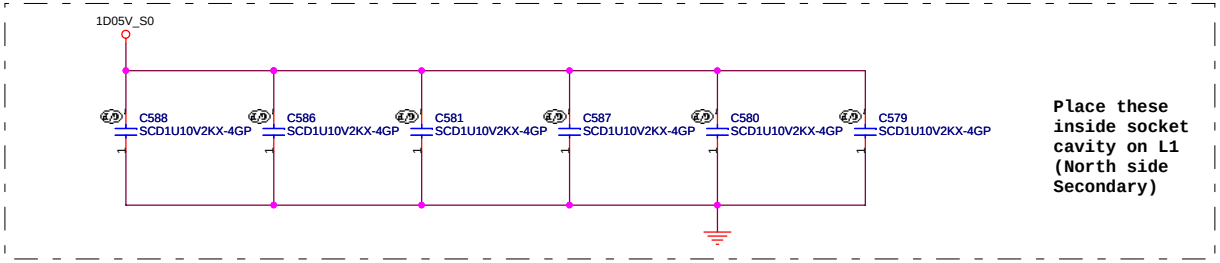

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Title: Meron(3/3)-GND&Bypass

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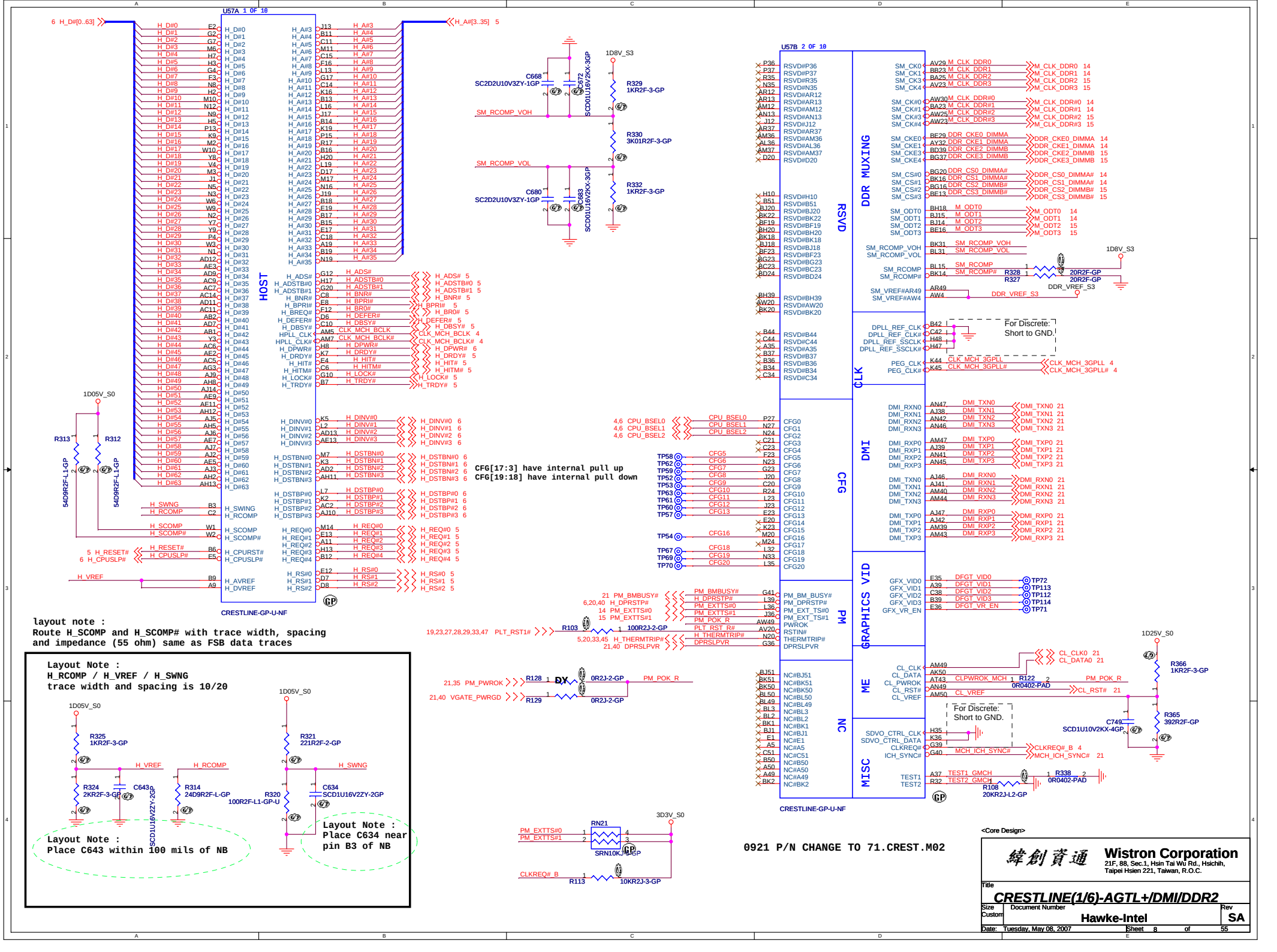
U57A 1 OF 10
HOST
U57B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down
layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing
and impedance (55 ohm) same as FSB data traces
Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20
Layout Note :
Place C643 within 100 mils of NB
Layout Note :
Place C634 near
pin B3 of NB
For Discrete:
Short to GND.
For Discrete:
Short to GND.
0921 P/N CHANGE TO 71.CREST.M02
CRESTLINE-GP-U-NF
CRESTLINE-GP-U-NF
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRESTLINE(1/6)-AGTL+/DMI/DDR2
Size
Custom
Document Number
Hawke-Intel
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SA
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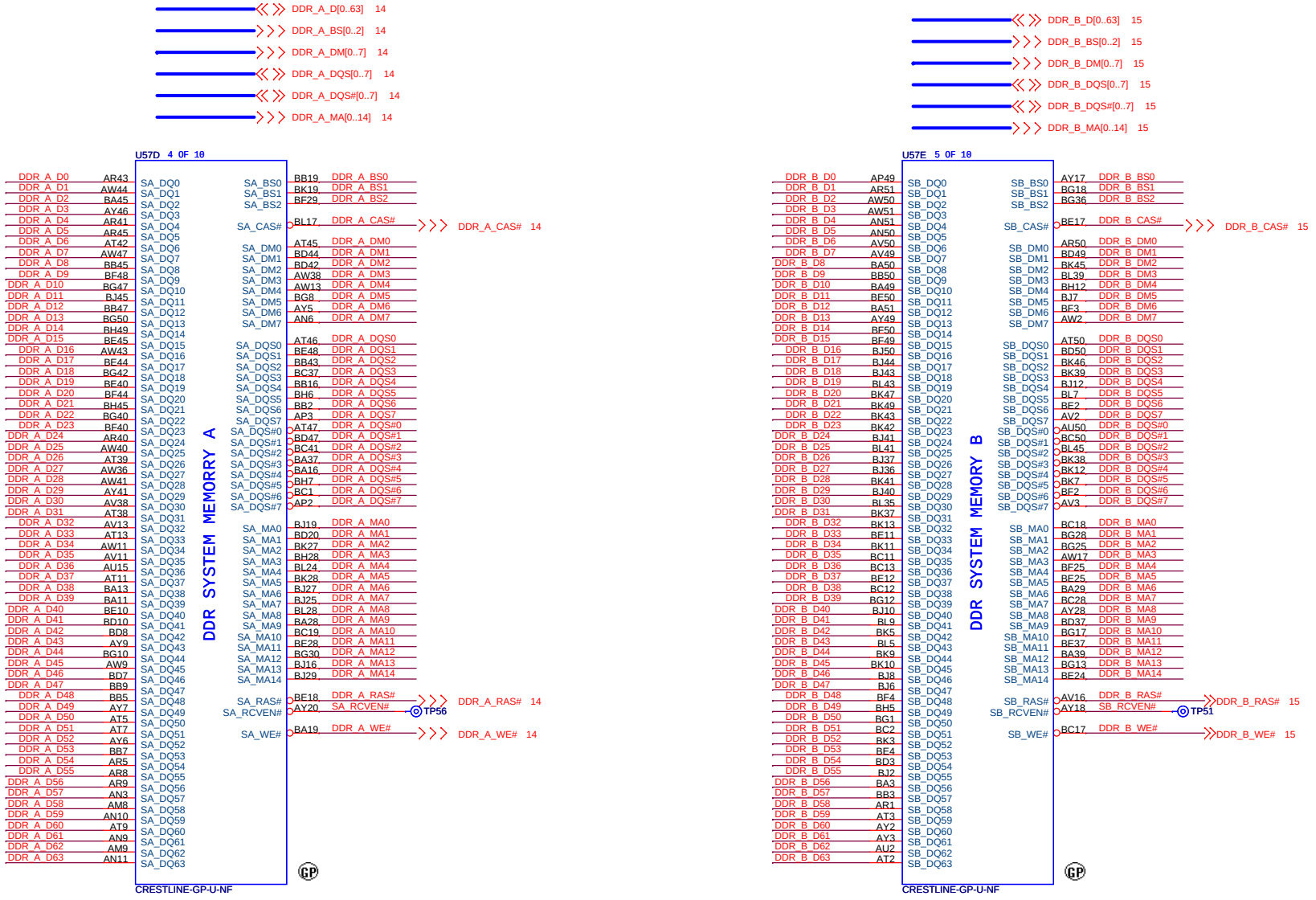

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Title
CRESTLINE(2/6)-DDR2 A/B CH

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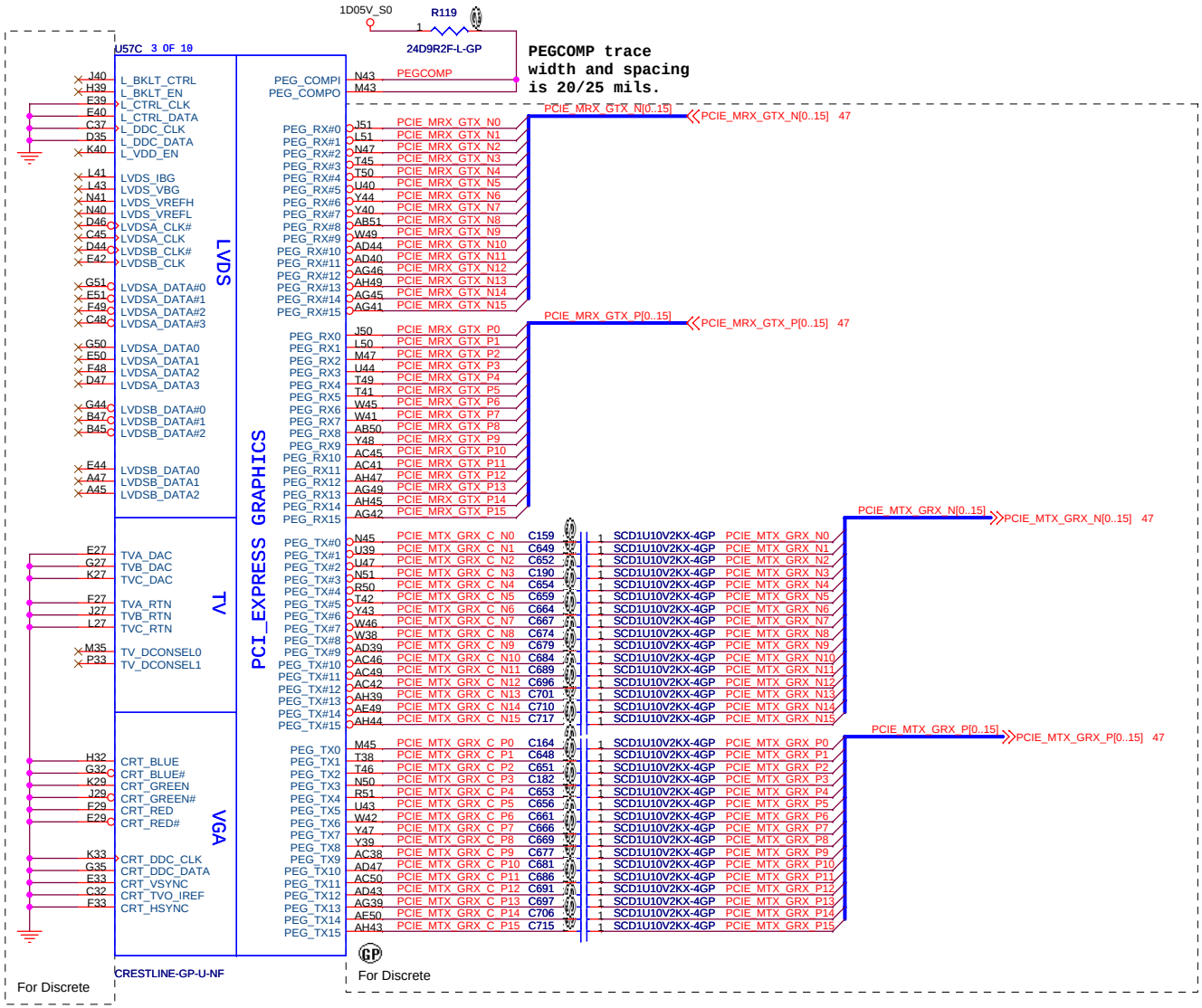

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

<Core Design>

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Title: CRESTLINE(3/6)-VGA/LVDS/TV

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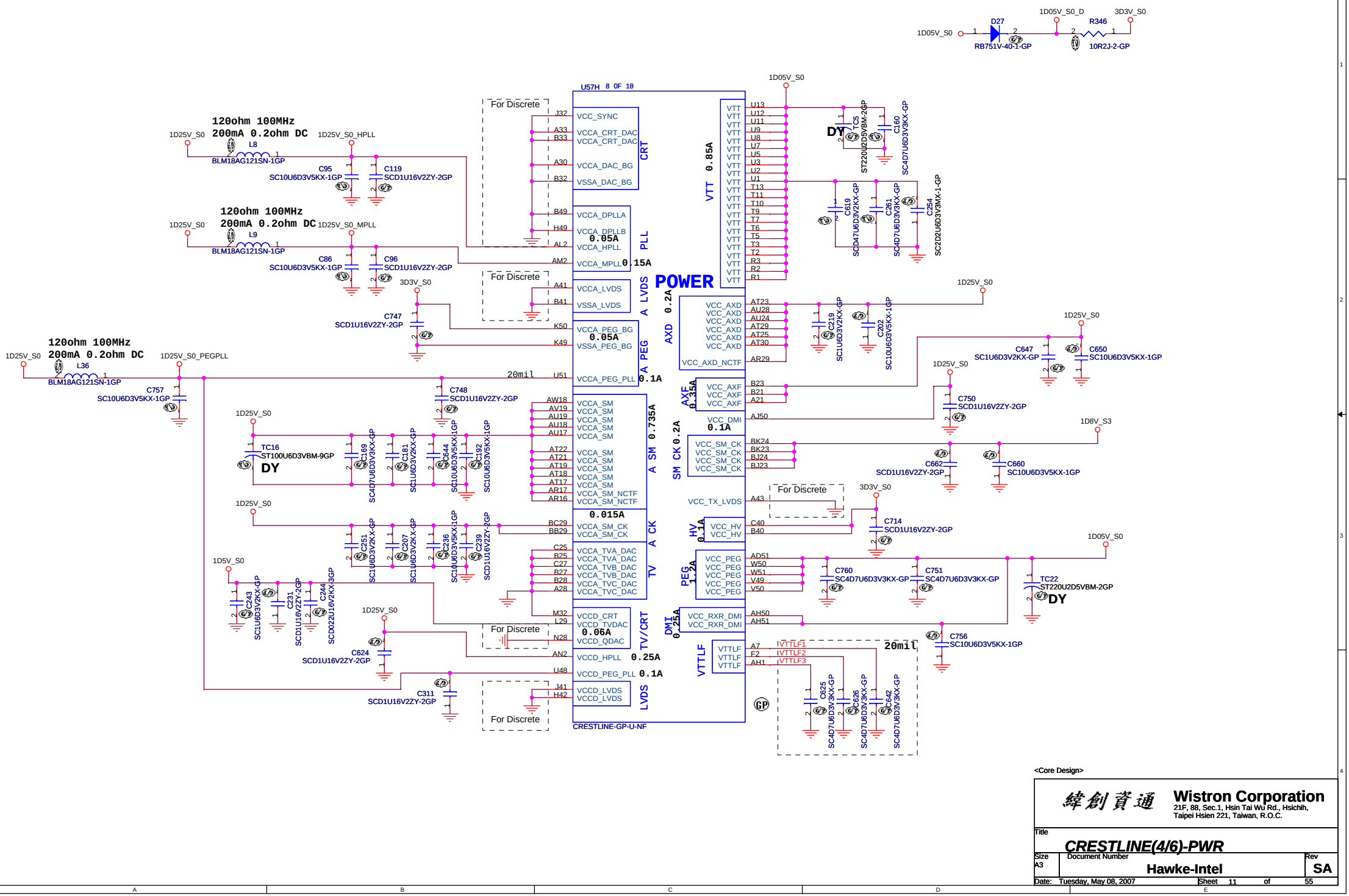
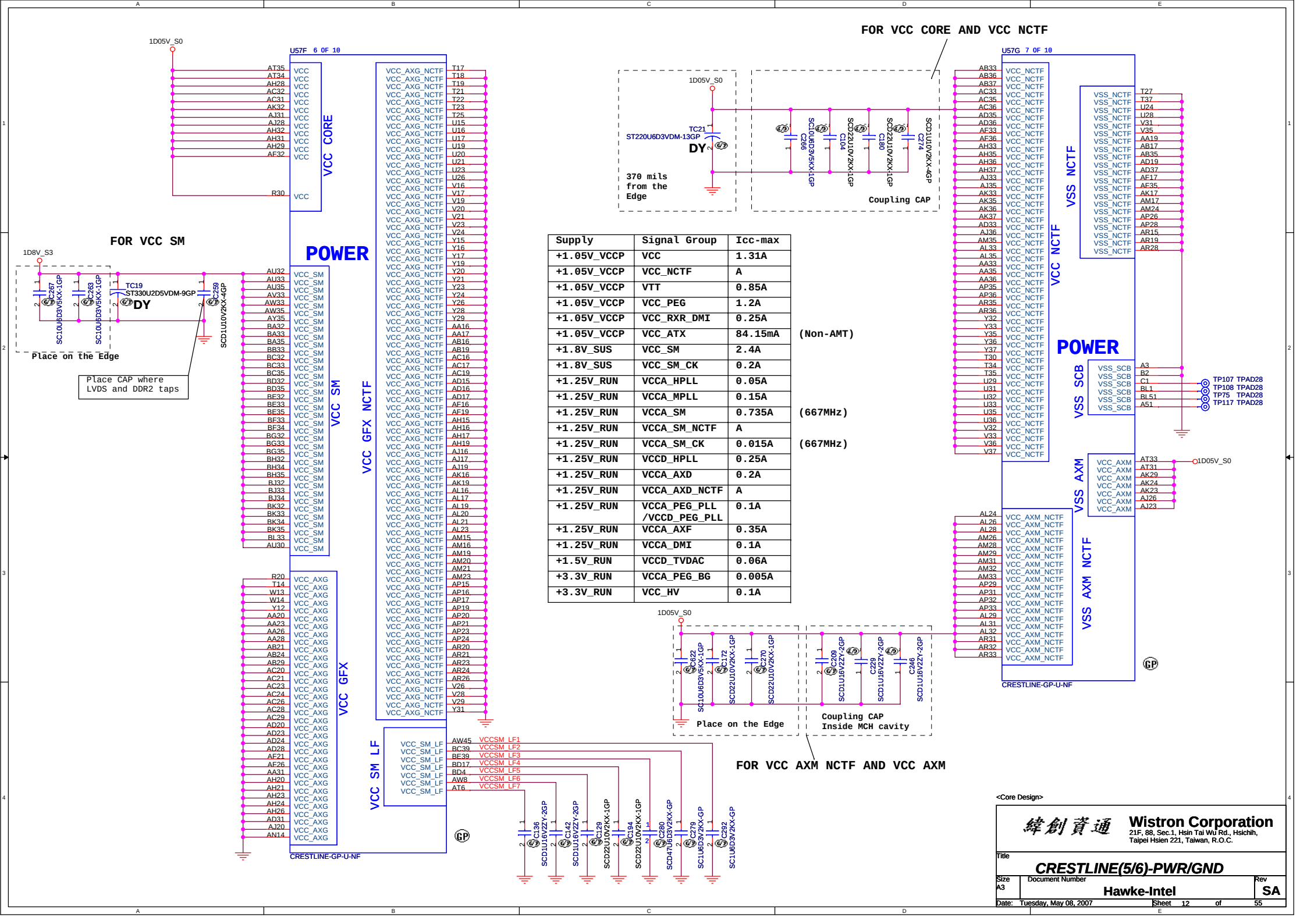

1D05V_S0_D
3D3V_S0
1D05V_S0
D27
R346
RB751V-40-1-GP
10R2J-2-GP
U57H 8 OF 10
POWER
CRESTLINE-GP-U-NF
120ohm 100MHz
200mA 0.2ohm DC
L8
BLM18AG121SN-1GP
1D25V_S0_HPLL
C95
SC10U6D3V5KX-1GP
C119
SCD1U16V2ZY-2GP
L9
1D25V_S0_MPLL
C86
C96
L36
1D25V_S0_PEGPLL
C757
C747
C748
20mil
For Discrete
DY
TC16
ST100U6D3VBM-9GP
TC5
ST220U2D5VBM-2GP
C160
SC4D7U6D3V3KX-GP
C619
SCD47U6D3V2KX-GP
C261
SC4D7U6D3V3KX-GP
C254
SC2D2U6D3V3MX-1-GP
C219
SC1U6D3V2KX-GP
C202
SC10U6D3V5KX-1GP
C647
SC1U6D3V2KX-GP
C650
SC10U6D3V5KX-1GP
C750
SCD1U16V2ZY-2GP
C662
C660
C714
C760
SC4D7U6D3V3KX-GP
C751
SC4D7U6D3V3KX-GP
TC22
ST220U2D5VBM-2GP
C756
SC10U6D3V5KX-1GP
C625
C626
C642
C624
C311
C169
C181
C644
C192
C251
C207
C236
C239
C243
C231
C244
SCD022U16V2KX3GP
VCC_SYNC
VCCA_CRT_DAC
VCCA_DAC_BG
VSSA_DAC_BG
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
0.15A
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG
VSSA_PEG_BG
VCCA_PEG_PLL
0.1A
VCCA_SM
VCCA_SM_NCTF
0.015A
VCCA_SM_CK
VCCA_TVA_DAC
VCCA_TVB_DAC
VCCA_TVC_DAC
VCCD_CRT
VCCD_TVDAC
0.06A
VCCD_QDAC
VCCD_HPLL
0.25A
VCCD_PEG_PLL
0.1A
VCCD_LVDS
CRT
PLL
LVDS
A LVDS
A PEG
A SM 0.735A
A CK
TV
TV/CRT
VTT 0.85A
VCC_AXD
VCC_AXD_NCTF
AXD 0.2A
VCC_AXF
AXF 0.35A
VCC_DMI
0.1A
VCC_SM_CK
SM CK 0.2A
VCC_TX_LVDS
VCC_HV
HV 0.1A
VCC_PEG
PEG 1.2A
VCC_RXR_DMI
DMI 0.25A
VTTLF
VTTLF1
VTTLF2
VTTLF3
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRESTLINE(4/6)-PWR
Size A3
Document Number
Hawke-Intel
Rev SA
Date: Tuesday, May 08, 2007
Sheet 11 of 55



Supply	Signal Group	Icc-max	
+1.05V_VCCP	VCC	1.31A	
+1.05V_VCCP	VCC_NCTF	A	
+1.05V_VCCP	VTT	0.85A	
+1.05V_VCCP	VCC_PEG	1.2A	
+1.05V_VCCP	VCC_RXR_DMI	0.25A	
+1.05V_VCCP	VCC_ATX	84.15mA	(Non-AMT)
+1.8V_SUS	VCC_SM	2.4A	
+1.8V_SUS	VCC_SM_CK	0.2A	
+1.25V_RUN	VCCA_HPLL	0.05A	
+1.25V_RUN	VCCA_MPLL	0.15A	
+1.25V_RUN	VCCA_SM	0.735A	(667MHz)
+1.25V_RUN	VCCA_SM_NCTF	A	
+1.25V_RUN	VCCA_SM_CK	0.015A	(667MHz)
+1.25V_RUN	VCCD_HPLL	0.25A	
+1.25V_RUN	VCCA_AXD	0.2A	
+1.25V_RUN	VCCA_AXD_NCTF	A	
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL	0.1A	
+1.25V_RUN	VCCA_AXF	0.35A	
+1.25V_RUN	VCCA_DMI	0.1A	
+1.5V_RUN	VCCD_TVDAC	0.06A	
+3.3V_RUN	VCCA_PEG_BG	0.005A	
+3.3V_RUN	VCC_HV	0.1A	

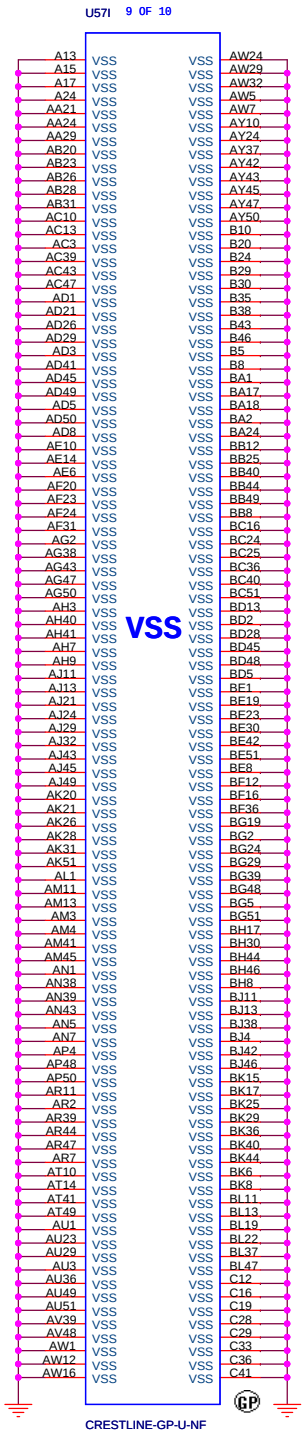
<Core Design>

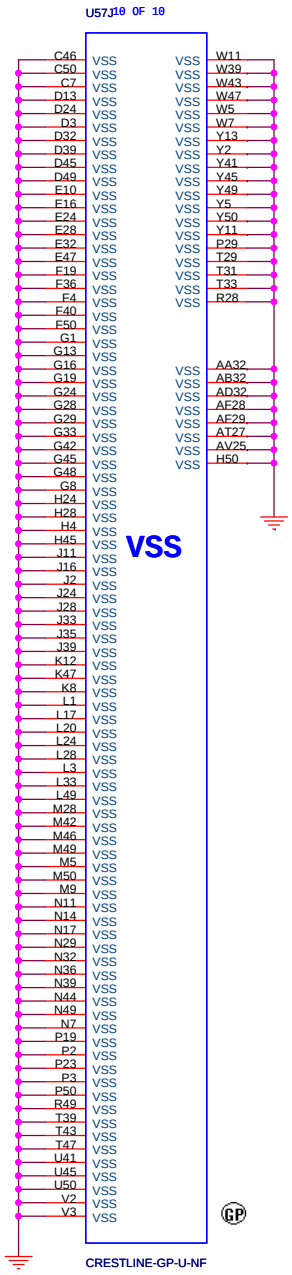
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(5/6)-PWR/GND

Size: A3 | Document Number: Hawke-Intel | Rev: SA

Date: Tuesday, May 08, 2007 | Sheet 12 of 55





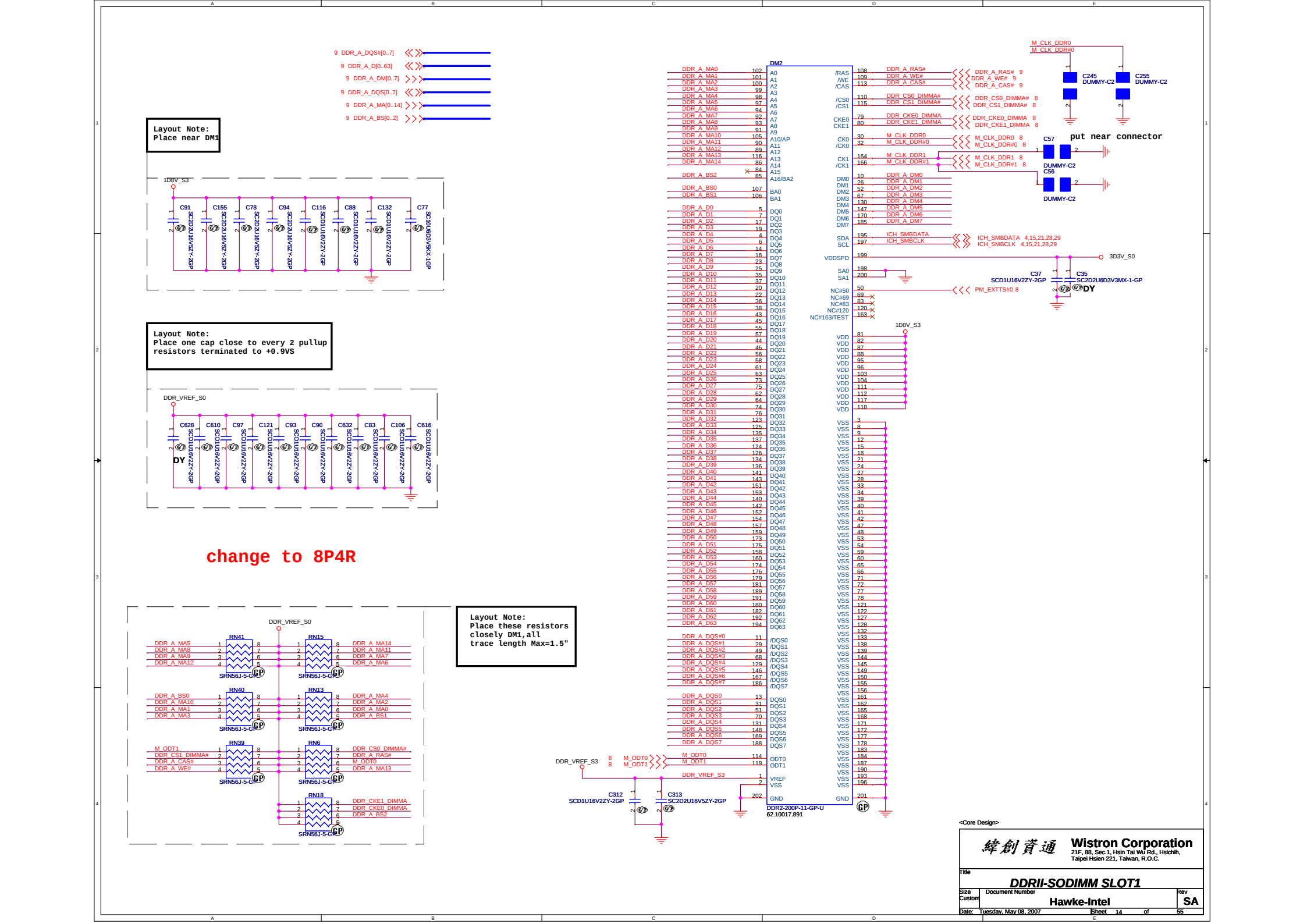
<Core Design>

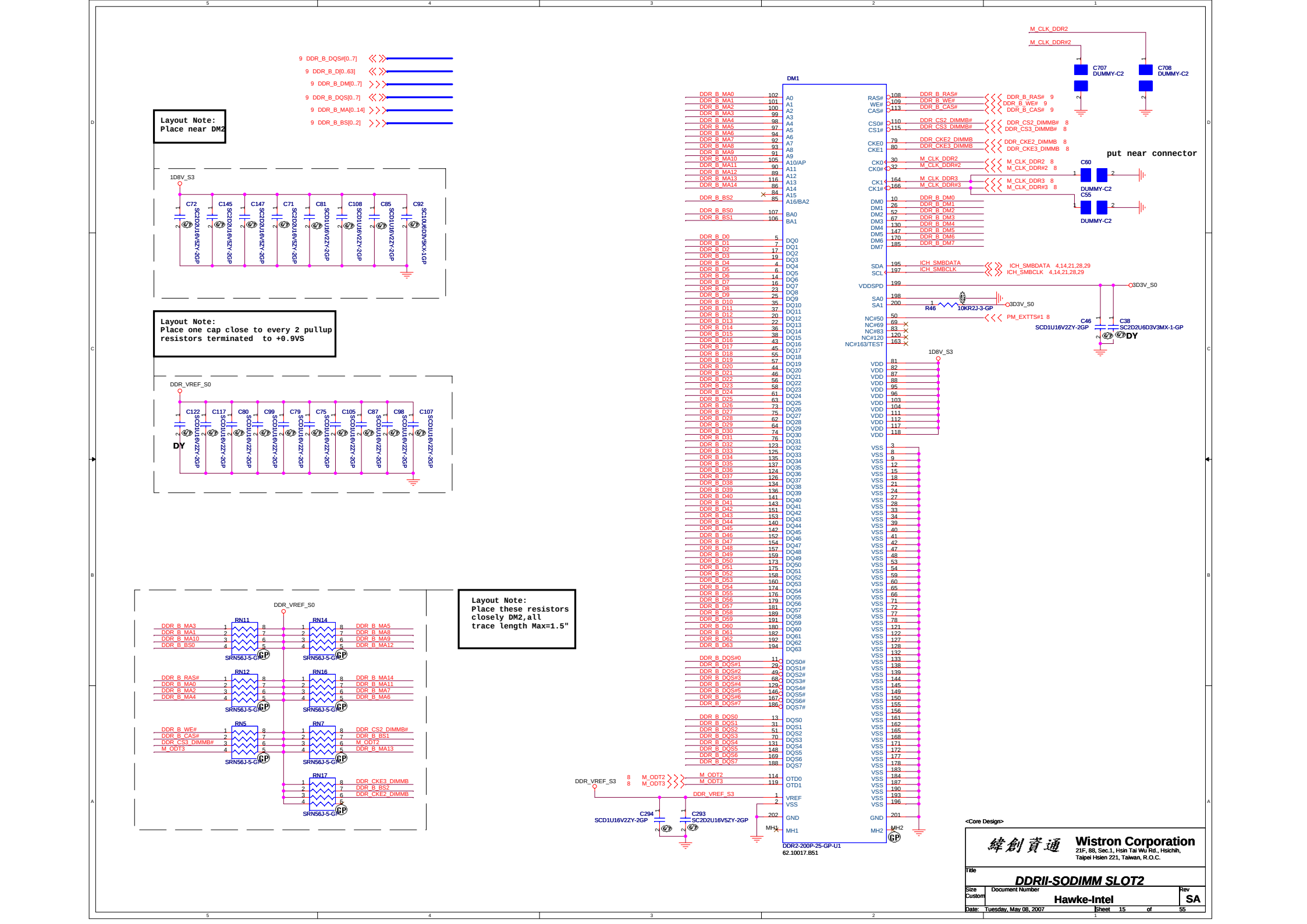
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(6/6)-PWR/GND

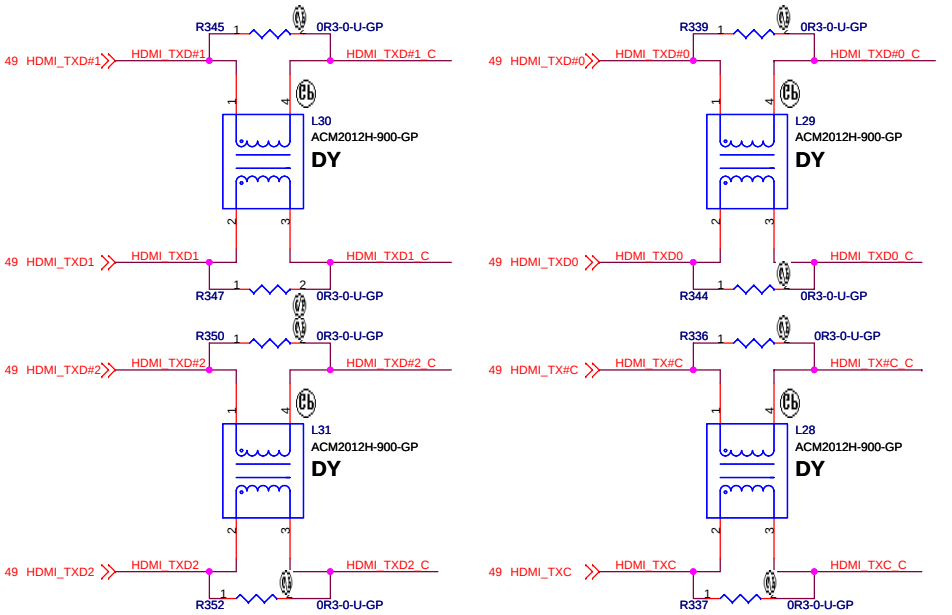
Size	Document Number	Rev
A3	Hawke-Intel	SA

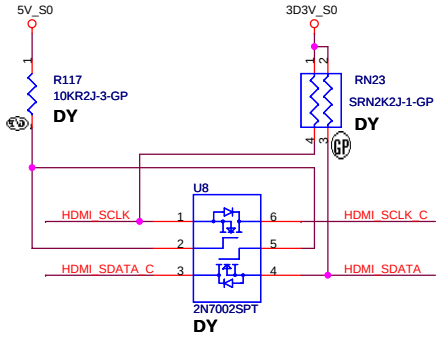
Date: Tuesday, May 08, 2007 Sheet 13 of 55


9 DDR_A_DQS#[0..7]
9 DDR_A_D[0..63]
9 DDR_A_DM[0..7]
9 DDR_A_DQS[0..7]
9 DDR_A_MA[0..14]
9 DDR_A_BS[0..2]
Layout Note:
Place near DM1
1D8V_S3
C91 SC2D2U16V5ZY-2GP
C155 SC2D2U16V5ZY-2GP
C78 SC2D2U16V5ZY-2GP
C94 SC2D2U16V5ZY-2GP
C116 SCD1U16V2ZY-2GP
C88 SCD1U16V2ZY-2GP
C132 SCD1U16V2ZY-2GP
C77 SC10U6D3V5KX-1GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C628 C610 C97 C121 C93 C90 C632 C83 C106 C616
SCD1U16V2ZY-2GP
DY
change to 8P4R
DDR_VREF_S0
RN41 RN15 RN40 RN13 RN39 RN6 RN18
SRN56J-5-GP
DDR_A_MA5 DDR_A_MA8 DDR_A_MA9 DDR_A_MA12
DDR_A_MA14 DDR_A_MA11 DDR_A_MA7 DDR_A_MA6
DDR_A_BS0 DDR_A_MA10 DDR_A_MA1 DDR_A_MA3
DDR_A_MA4 DDR_A_MA2 DDR_A_MA0 DDR_A_BS1
M_ODT1 DDR_CS1_DIMMA# DDR_A_CAS# DDR_A_WE#
DDR_CS0_DIMMA# DDR_A_RAS# M_ODT0 DDR_A_MA13
DDR_CKE1_DIMMA DDR_CKE0_DIMMA DDR_A_BS2
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
DM2
DDR_A_MA0 DDR_A_MA1 DDR_A_MA2 DDR_A_MA3 DDR_A_MA4 DDR_A_MA5 DDR_A_MA6 DDR_A_MA7 DDR_A_MA8 DDR_A_MA9 DDR_A_MA10 DDR_A_MA11 DDR_A_MA12 DDR_A_MA13 DDR_A_MA14
DDR_A_BS2 DDR_A_BS0 DDR_A_BS1
DDR_A_D0 DDR_A_D1 DDR_A_D2 DDR_A_D3 DDR_A_D4 DDR_A_D5 DDR_A_D6 DDR_A_D7 DDR_A_D8 DDR_A_D9 DDR_A_D10 DDR_A_D11 DDR_A_D12 DDR_A_D13 DDR_A_D14 DDR_A_D15 DDR_A_D16 DDR_A_D17 DDR_A_D18 DDR_A_D19 DDR_A_D20 DDR_A_D21 DDR_A_D22 DDR_A_D23 DDR_A_D24 DDR_A_D25 DDR_A_D26 DDR_A_D27 DDR_A_D28 DDR_A_D29 DDR_A_D30 DDR_A_D31 DDR_A_D32 DDR_A_D33 DDR_A_D34 DDR_A_D35 DDR_A_D36 DDR_A_D37 DDR_A_D38 DDR_A_D39 DDR_A_D40 DDR_A_D41 DDR_A_D42 DDR_A_D43 DDR_A_D44 DDR_A_D45 DDR_A_D46 DDR_A_D47 DDR_A_D48 DDR_A_D49 DDR_A_D50 DDR_A_D51 DDR_A_D52 DDR_A_D53 DDR_A_D54 DDR_A_D55 DDR_A_D56 DDR_A_D57 DDR_A_D58 DDR_A_D59 DDR_A_D60 DDR_A_D61 DDR_A_D62 DDR_A_D63
DDR_A_DQS#0 DDR_A_DQS#1 DDR_A_DQS#2 DDR_A_DQS#3 DDR_A_DQS#4 DDR_A_DQS#5 DDR_A_DQS#6 DDR_A_DQS#7
DDR_A_DQS0 DDR_A_DQS1 DDR_A_DQS2 DDR_A_DQS3 DDR_A_DQS4 DDR_A_DQS5 DDR_A_DQS6 DDR_A_DQS7
M_ODT0 M_ODT1
DDR_VREF_S3
GND
DDR2-200P-11-GP-U
62.10017.891
/RAS /WE /CAS /CS0 /CS1 CKE0 CKE1 CK0 /CK0 CK1 /CK1 DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7 SDA SCL VDDSPD SA0 SA1 NC#50 NC#69 NC#83 NC#120 NC#163/TEST
DDR_A_RAS# DDR_A_WE# DDR_A_CAS# DDR_CS0_DIMMA# DDR_CS1_DIMMA# DDR_CKE0_DIMMA DDR_CKE1_DIMMA M_CLK_DDR0 M_CLK_DDR#0 M_CLK_DDR1 M_CLK_DDR#1 DDR_A_DM0 DDR_A_DM1 DDR_A_DM2 DDR_A_DM3 DDR_A_DM4 DDR_A_DM5 DDR_A_DM6 DDR_A_DM7 ICH_SMBDATA ICH_SMBCLK PM_EXTTS#0
VDD VSS
M_CLK_DDR0 M_CLK_DDR#0
C245 DUMMY-C2 C255 DUMMY-C2
put near connector
C57 C56 DUMMY-C2
3D3V_S0
C37 SCD1U16V2ZY-2GP C35 SC2D2U6D3V3MX-1-GP DY
C312 SCD1U16V2ZY-2GP C313 SC2D2U16V5ZY-2GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT1
Size Custom
Document Number
Hawke-Intel
Rev
SA
Date: Tuesday, May 08, 2007
Sheet 14 of 55

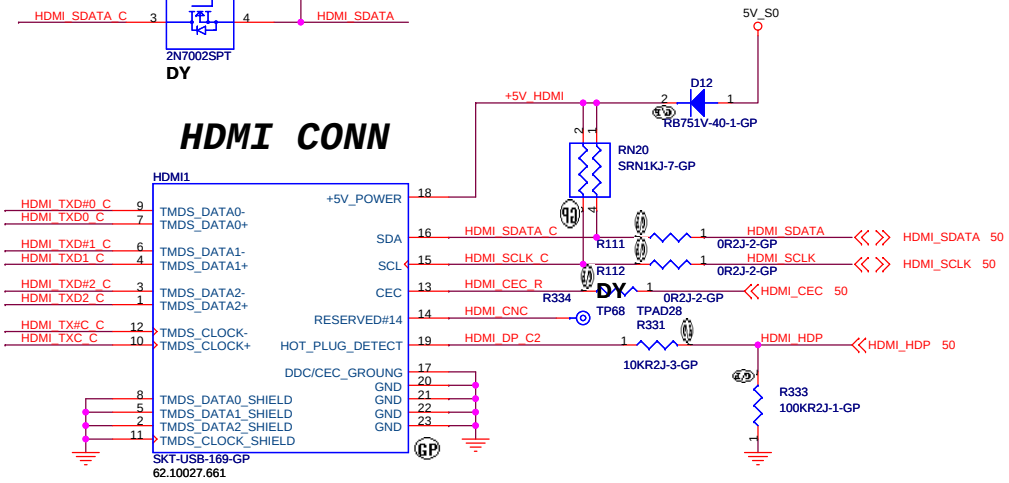

9 DDR_B_DQS#[0..7]
9 DDR_B_D[0..63]
9 DDR_B_DM[0..7]
9 DDR_B_DQS[0..7]
9 DDR_B_MA[0..14]
9 DDR_B_BS[0..2]
Layout Note:
Place near DM2
1D8V_S3
C72 C145 C147 C71 C81 C108 C85 C92
SC220U16V8ZY-26P
SCD1U16V2ZY-2GP
SC1U4D3V5KX-1GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C122 C117 C80 C99 C79 C75 C105 C87 C98 C107
SCD1U16V2ZY-2GP
DY
DDR_VREF_S0
RN11 RN14 RN12 RN16 RN5 RN7 RN17
SRN56J-5-GP
DDR_B_MA3 DDR_B_MA1 DDR_B_MA10 DDR_B_BS0
DDR_B_MA5 DDR_B_MA8 DDR_B_MA9 DDR_B_MA12
DDR_B_RAS# DDR_B_MA0 DDR_B_MA2 DDR_B_MA4
DDR_B_MA14 DDR_B_MA11 DDR_B_MA7 DDR_B_MA6
DDR_B_WE# DDR_B_CAS# DDR_CS3_DIMMB# M_ODT3
DDR_CS2_DIMMB# DDR_B_BS1 M_ODT2 DDR_B_MA13
DDR_CKE3_DIMMB DDR_B_BS2 DDR_CKE2_DIMMB
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
DM1
DDR_B_MA0 DDR_B_MA1 DDR_B_MA2 DDR_B_MA3 DDR_B_MA4 DDR_B_MA5 DDR_B_MA6 DDR_B_MA7 DDR_B_MA8 DDR_B_MA9 DDR_B_MA10 DDR_B_MA11 DDR_B_MA12 DDR_B_MA13 DDR_B_MA14
DDR_B_BS2
DDR_B_BS0 DDR_B_BS1
DDR_B_D0 DDR_B_D1 DDR_B_D2 DDR_B_D3 DDR_B_D4 DDR_B_D5 DDR_B_D6 DDR_B_D7 DDR_B_D8 DDR_B_D9 DDR_B_D10 DDR_B_D11 DDR_B_D12 DDR_B_D13 DDR_B_D14 DDR_B_D15 DDR_B_D16 DDR_B_D17 DDR_B_D18 DDR_B_D19 DDR_B_D20 DDR_B_D21 DDR_B_D22 DDR_B_D23 DDR_B_D24 DDR_B_D25 DDR_B_D26 DDR_B_D27 DDR_B_D28 DDR_B_D29 DDR_B_D30 DDR_B_D31 DDR_B_D32 DDR_B_D33 DDR_B_D34 DDR_B_D35 DDR_B_D36 DDR_B_D37 DDR_B_D38 DDR_B_D39 DDR_B_D40 DDR_B_D41 DDR_B_D42 DDR_B_D43 DDR_B_D44 DDR_B_D45 DDR_B_D46 DDR_B_D47 DDR_B_D48 DDR_B_D49 DDR_B_D50 DDR_B_D51 DDR_B_D52 DDR_B_D53 DDR_B_D54 DDR_B_D55 DDR_B_D56 DDR_B_D57 DDR_B_D58 DDR_B_D59 DDR_B_D60 DDR_B_D61 DDR_B_D62 DDR_B_D63
DDR_B_DQS#0 DDR_B_DQS#1 DDR_B_DQS#2 DDR_B_DQS#3 DDR_B_DQS#4 DDR_B_DQS#5 DDR_B_DQS#6 DDR_B_DQS#7
DDR_B_DQS0 DDR_B_DQS1 DDR_B_DQS2 DDR_B_DQS3 DDR_B_DQS4 DDR_B_DQS5 DDR_B_DQS6 DDR_B_DQS7
M_ODT2 M_ODT3
DDR_VREF_S3
DDR_B_RAS# DDR_B_WE# DDR_B_CAS#
DDR_CS2_DIMMB# DDR_CS3_DIMMB#
DDR_CKE2_DIMMB DDR_CKE3_DIMMB
M_CLK_DDR2 M_CLK_DDR#2 M_CLK_DDR3 M_CLK_DDR#3
DDR_B_DM0 DDR_B_DM1 DDR_B_DM2 DDR_B_DM3 DDR_B_DM4 DDR_B_DM5 DDR_B_DM6 DDR_B_DM7
ICH_SMBDATA ICH_SMBCLK
ICH_SMBDATA 4,14,21,28,29
ICH_SMBCLK 4,14,21,28,29
VDDSPD
SA0 SA1
R46 10KR2J-3-GP
3D3V_S0
PM_EXTTS#1 8
NC#50 NC#69 NC#83 NC#120 NC#163/TEST
1D8V_S3
VDD VSS GND MH1 MH2
DDR2-200P-25-GP-U1
62.10017.B51
C707 DUMMY-C2
C708 DUMMY-C2
put near connector
C60 DUMMY-C2
C55 DUMMY-C2
C46 SCD1U16V2ZY-2GP
C38 SC2D2U6D3V3MX-1-GP
DY
DDR_VREF_S3
C294 SCD1U16V2ZY-2GP
C293 SC2D2U16V5ZY-2GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT2
Size Custom
Document Number
Hawke-Intel
Rev SA
Date: Tuesday, May 08, 2007
Sheet 15 of 55

HDMI I/F & CONNECTOR





HDMI CONN

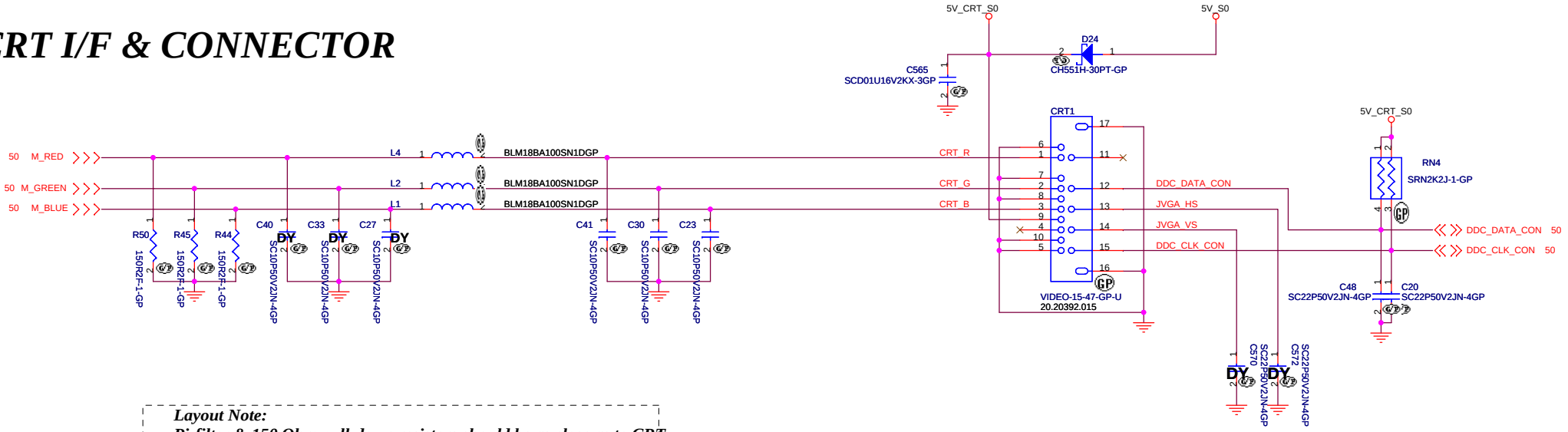


<Core Design>

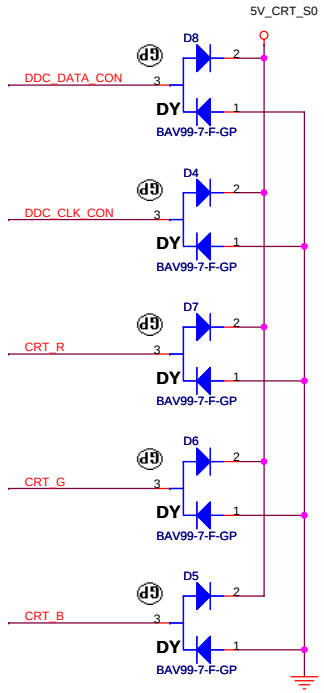
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI**		
Size: A3	Document Number: **Hawke-Intel**	Rev: **SA**
Date: Tuesday, May 08, 2007	Sheet 16 of 55	

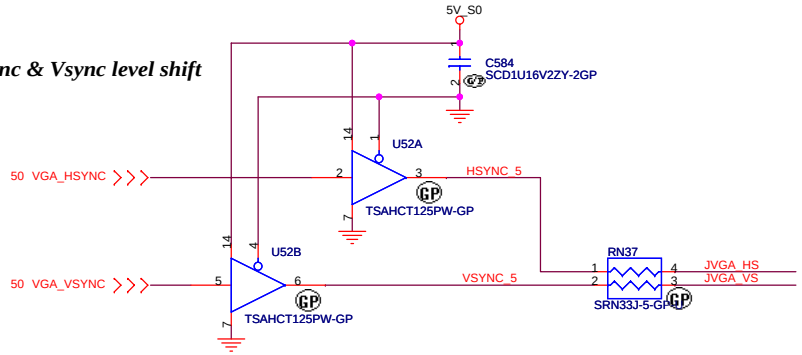
CRT I/F & CONNECTOR



Layout Note:
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

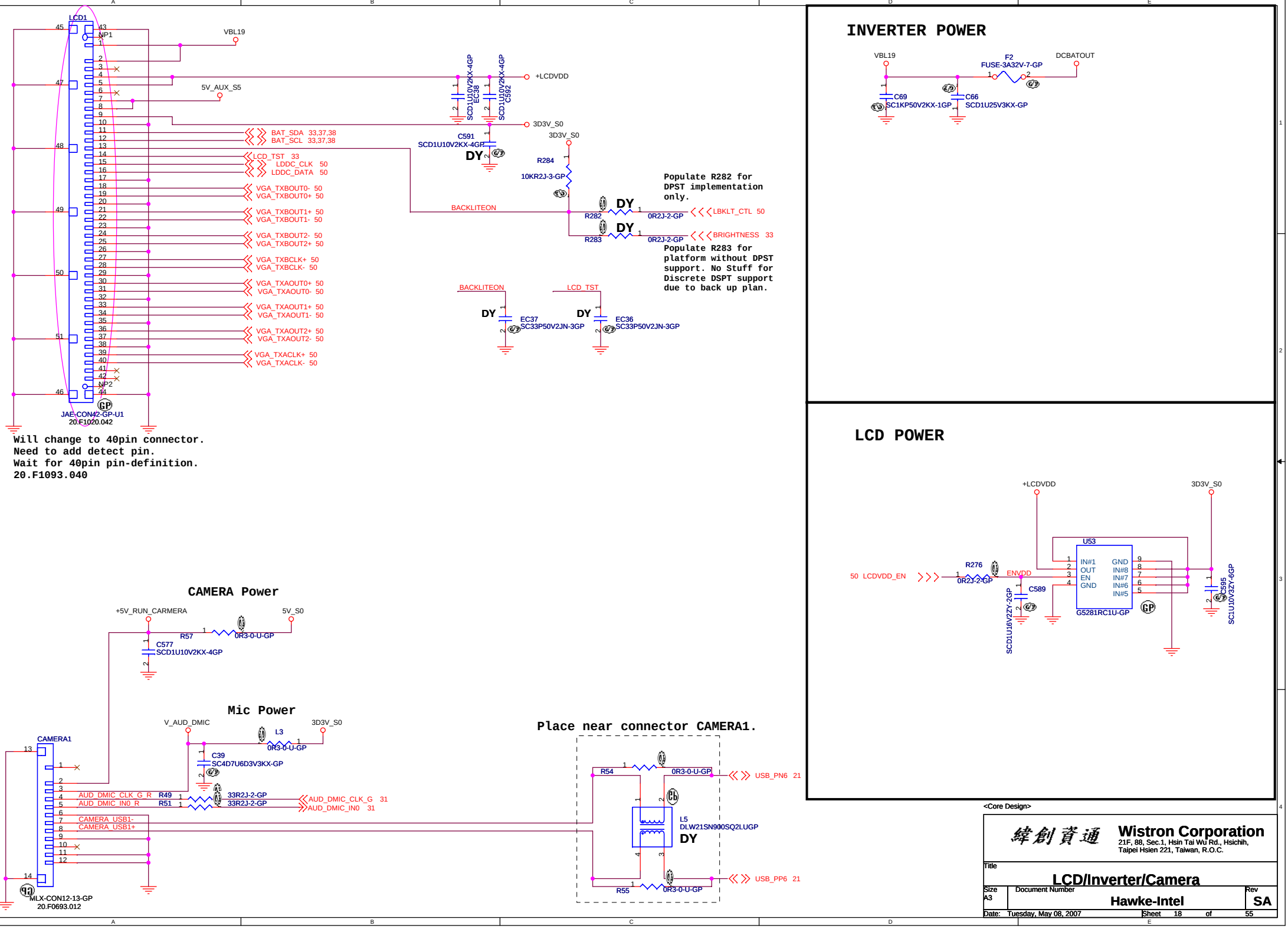


Hsync & Vsync level shift



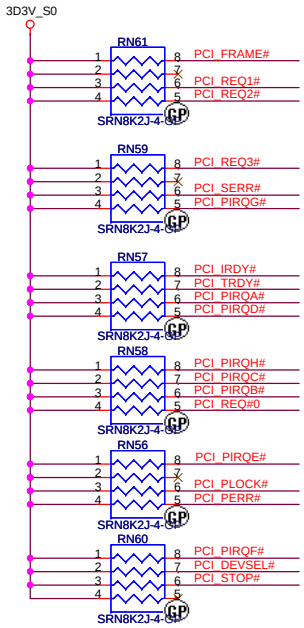
<Core Design>

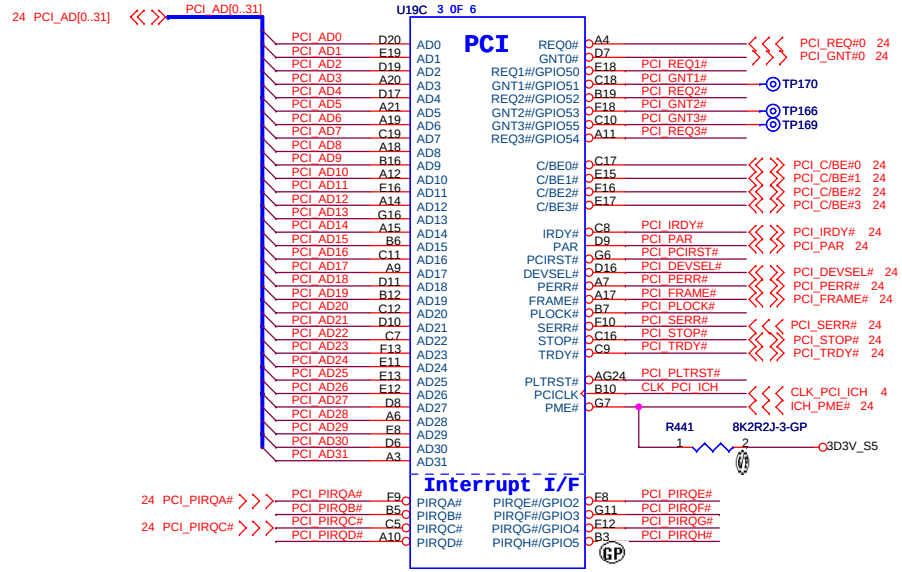
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***CRT Connector***		
Size: A3	Document Number: Hawke-Intel	Rev: SA
Date: Tuesday, May 08, 2007	Sheet 17 of 55	

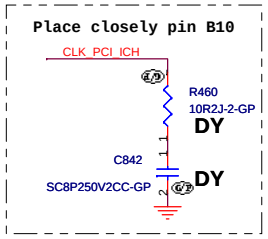

LCD1
JAE-CON42-GP-U1
20.F1020.042
VBL19
5V_AUX_S5
+LCDVDD
3D3V_S0
BAT_SDA 33,37,38
BAT_SCL 33,37,38
LCD_TST 33
LDDC_CLK 50
LDDC_DATA 50
VGA_TXBOUT0- 50
VGA_TXBOUT0+ 50
VGA_TXBOUT1+ 50
VGA_TXBOUT1- 50
VGA_TXBOUT2- 50
VGA_TXBOUT2+ 50
VGA_TXBCLK+ 50
VGA_TXBCLK- 50
VGA_TXAOUT0+ 50
VGA_TXAOUT0- 50
VGA_TXAOUT1+ 50
VGA_TXAOUT1- 50
VGA_TXAOUT2+ 50
VGA_TXAOUT2- 50
VGA_TXACLK+ 50
VGA_TXACLK- 50
C591
SCD1U10V2KX-4GP
DY
R284
10KR2J-3-GP
BACKLITEON
R282
R283
0R2J-2-GP
LBKLT_CTL 50
BRIGHTNESS 33
Populate R282 for DPST implementation only.
Populate R283 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.
EC37
EC36
SC33P50V2JN-3GP
LCD_TST
Will change to 40pin connector.
Need to add detect pin.
Wait for 40pin pin-definition.
20.F1093.040
INVERTER POWER
F2
FUSE-3A32V-7-GP
DCBATOUT
C69
SC1KP50V2KX-1GP
C66
SCD1U25V3KX-GP
LCD POWER
U53
G5281RC1U-GP
R276
ENVDD
C589
SCD1U16V2ZY-2GP
C595
SC1U10V3ZY-6GP
50 LCDVDD_EN
CAMERA Power
+5V_RUN_CARMERA
5V_S0
R57
0R3-0-U-GP
C577
SCD1U10V2KX-4GP
Mic Power
V_AUD_DMIC
L3
C39
SC4D7U6D3V3KX-GP
CAMERA1
MLX-CON12-13-GP
20.F0693.012
AUD_DMIC_CLK_G_R
AUD_DMIC_IN0_R
R49
R51
33R2J-2-GP
AUD_DMIC_CLK_G 31
AUD_DMIC_IN0 31
CAMERA_USB1-
CAMERA_USB1+
Place near connector CAMERA1.
R54
R55
L5
DLW21SN900SQ2LUGP
USB_PN6 21
USB_PP6 21
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LCD/Inverter/Camera
Size
A3
Document Number
Hawke-Intel
Rev
SA
Date: Tuesday, May 08, 2007
Sheet 18 of 55

PCI Interface Routing

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0





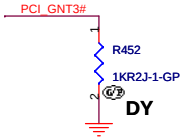


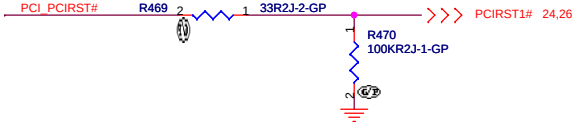
0504 P/N CHANGE TO 71.ICH8M.C0U

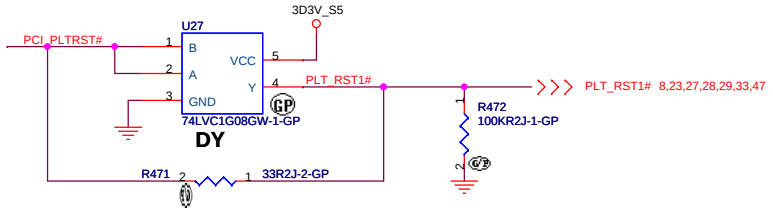
ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *







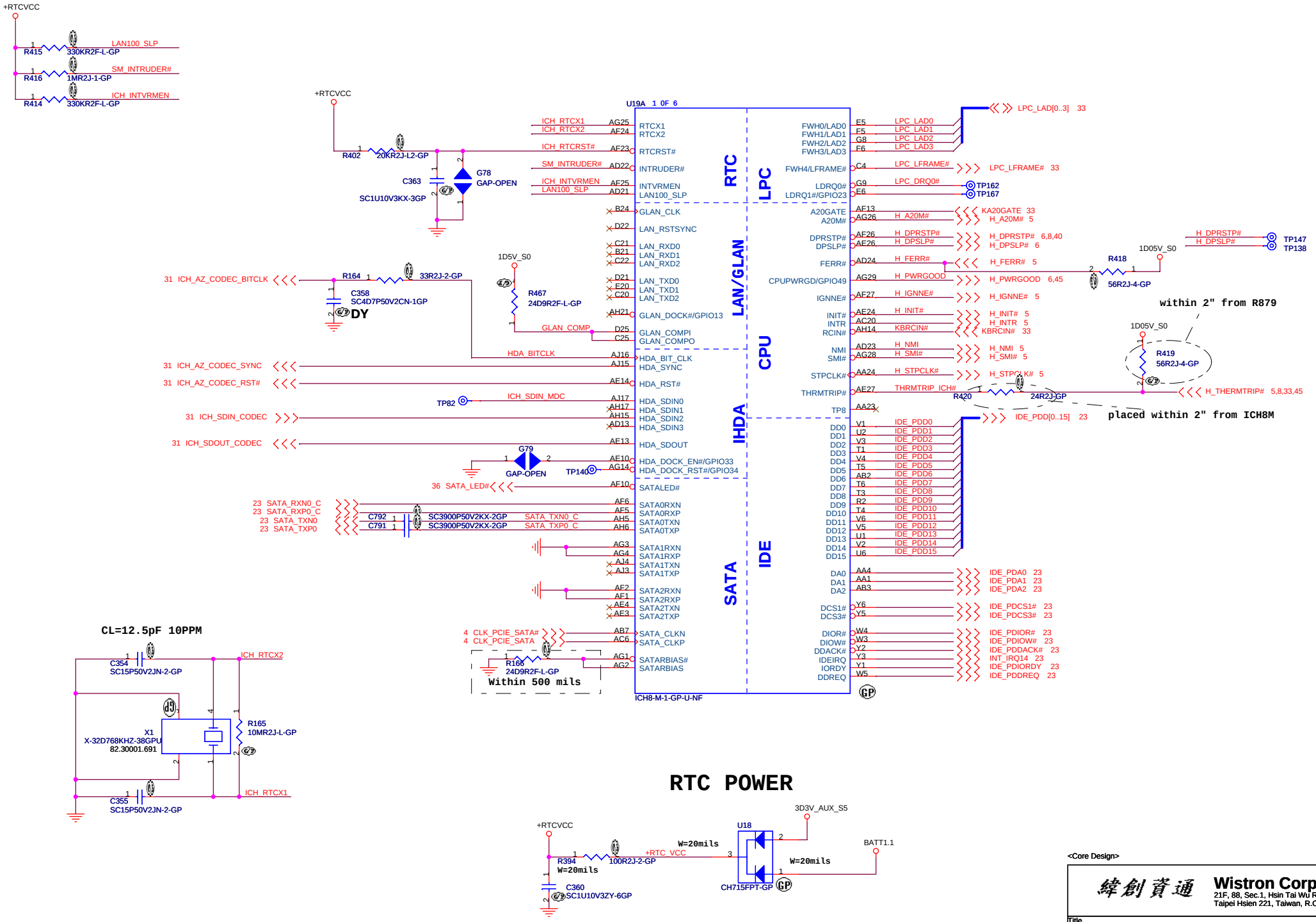
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(1/4)-PCI/INT

Size: A3 | Document Number: Hawke-Intel | Rev: SA

Date: Tuesday, May 08, 2007 | Sheet 19 of 55



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(2/4) LAN,HD,IDE,LPC

Size	Document Number	Rev
A3	Hawke-Intel	SA

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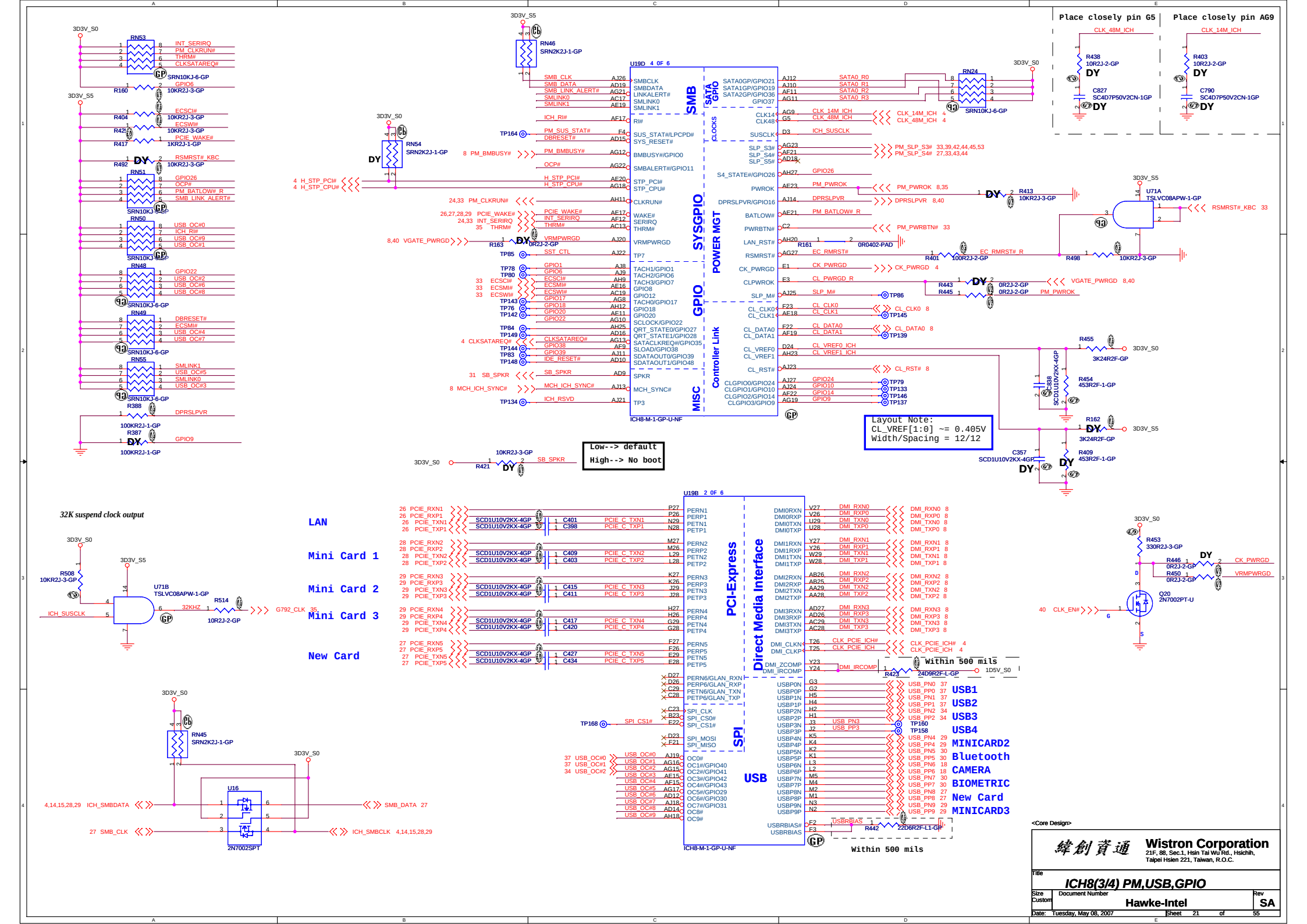
Place closely pin G5
Place closely pin AG9
U19D 4 OF 6
U19B 2 OF 6
ICH8-M-1-GP-U-NF
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
PCI-Express
Direct Media Interface
SPI
USB
LAN
Mini Card 1
Mini Card 2
Mini Card 3
New Card
USB1
USB2
USB3
USB4
MINICARD2
Bluetooth
CAMERA
BIOMETRIC
New Card
MINICARD3
Layout Note:
CL_VREF[1:0] ~= 0.405V
Width/Spacing = 12/12
Low--> default
High--> No boot
32K suspend clock output
Within 500 mils
Within 500 mils
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH8(3/4) PM,USB,GPIO
Hawke-Intel
SA
Tuesday, May 08, 2007
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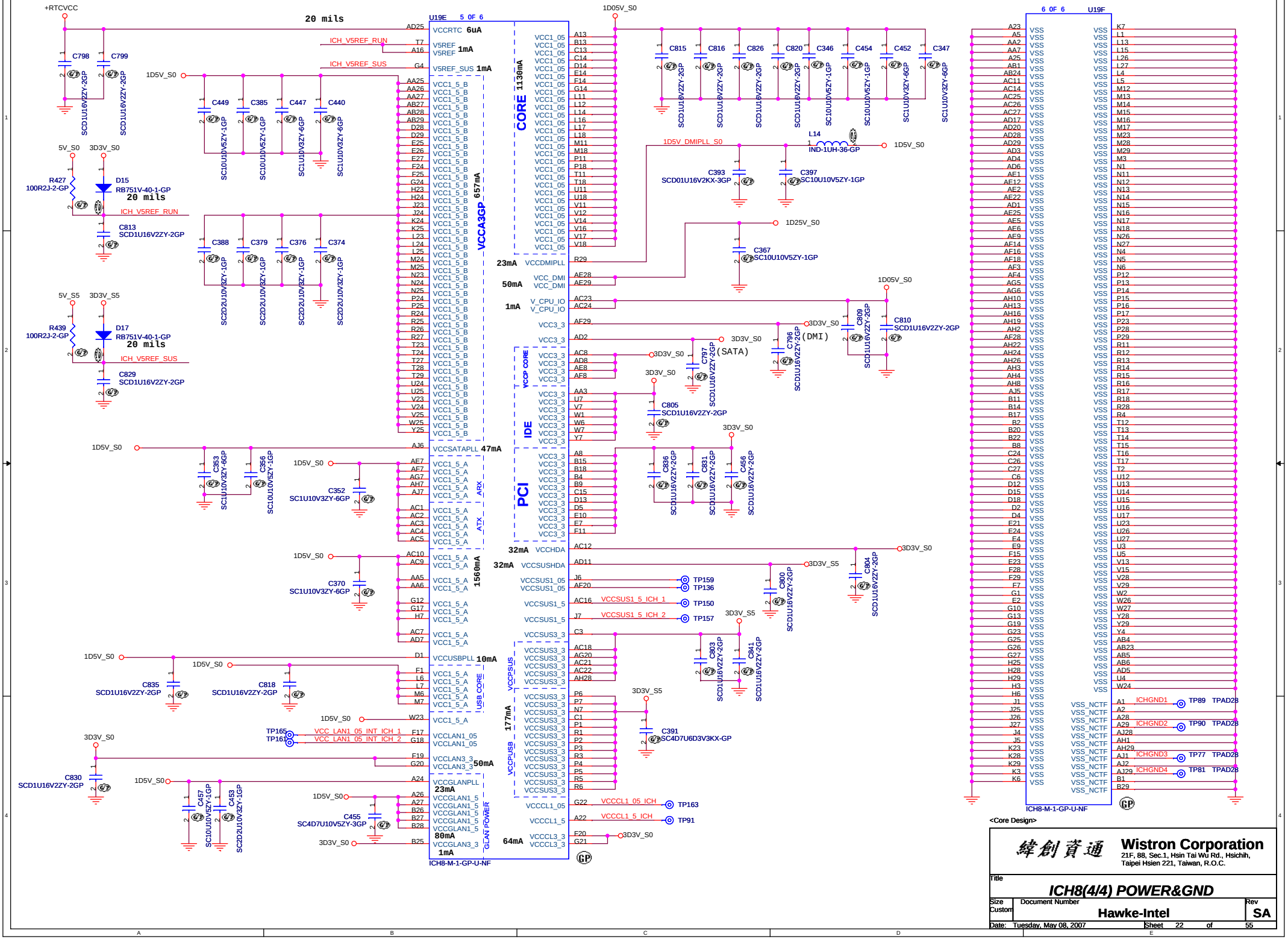
+RTCVCC
20 mils
U19E 5 OF 6
ICH_V5REF_RUN
ICH_V5REF_SUS
1D5V_S0
5V_S0
3D3V_S0
5V_S5
3D3V_S5
R427 100R2J-2-GP
D15 RB751V-40-1-GP
R439 100R2J-2-GP
D17 RB751V-40-1-GP
C798 C799 C813 C829
C449 C385 C447 C440
C388 C379 C376 C374
C353 C356 C352 C370
C835 C818 C830
C457 C453 C455
TP165 TP161
VCC_LAN1_05_INT_ICH_1
VCC_LAN1_05_INT_ICH_2
VCCRTC 6uA
V5REF 1mA
V5REF_SUS 1mA
VCCA3GP 657mA
VCCSATAPLL 47mA
VCCUSBPLL 10mA
VCCLAN3_3 50mA
VCCGLANPLL 23mA
VCCGLAN3_3 1mA
CORE 1130mA
VCCDMIPLL 23mA
VCC_DMI 50mA
V_CPU_IO 1mA
VCCHDA 32mA
VCCSUSHDA 32mA
VCCSUS1_05
VCCSUS1_5
VCCSUS3_3 177mA
VCCCL1_05
VCCCL1_5
VCCCL3_3 64mA
VCCP CORE
IDE
PCI
ARX
ATX
VCCPSUS
VCCPUSB
USB_CORE
GLAN POWER
ICH8-M-1-GP-U-NF
C815 C816 C826 C820 C346 C454 C452 C347
SCD1U16V2ZY-2GP
SC10U10V5ZY-1GP
SC1U10V3ZY-6GP
L14 IND-1UH-36-GP
1D5V_DMIPLL_S0
C393 SCD01U16V2KX-3GP
C397 SC10U10V5ZY-1GP
1D25V_S0
C367 SC10U10V5ZY-1GP
C809 C810
C796 (DMI)
C797 (SATA)
C805 C836 C831 C456
C800 C804
C803 C841
C391 SC4D7U6D3V3KX-GP
TP159 TP136 TP150 TP157 TP163 TP91
6 OF 6 U19F
VSS
VSS_NCTF
ICHGND1 TP89 TPAD28
ICHGND2 TP90 TPAD28
ICHGND3 TP77 TPAD28
ICHGND4 TP81 TPAD28
ICH8-M-1-GP-U-NF
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(4/4) POWER&GND
Size Custom
Document Number
Hawke-Intel
Rev
SA
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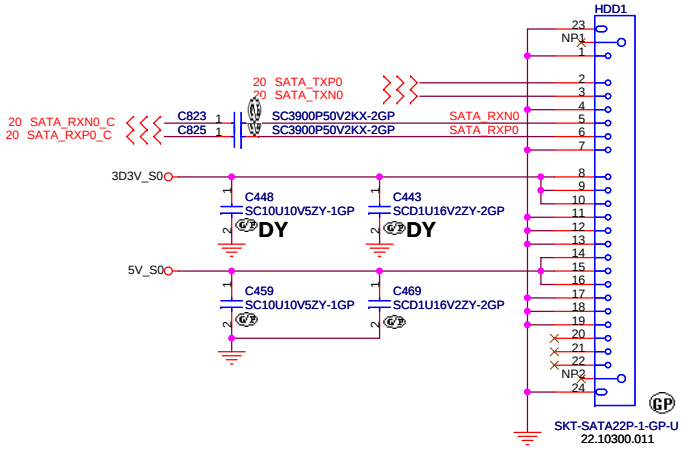
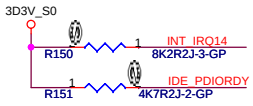
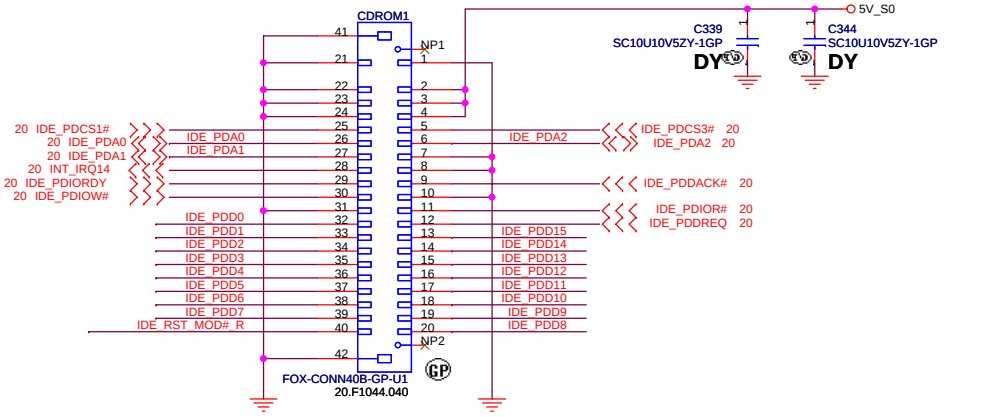
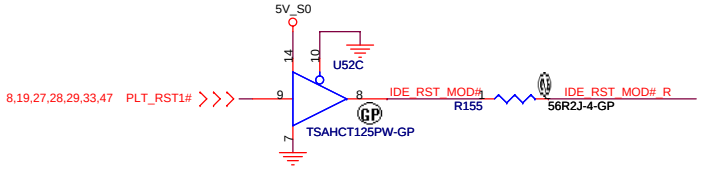
SATA HDD Connector



ODD Connector



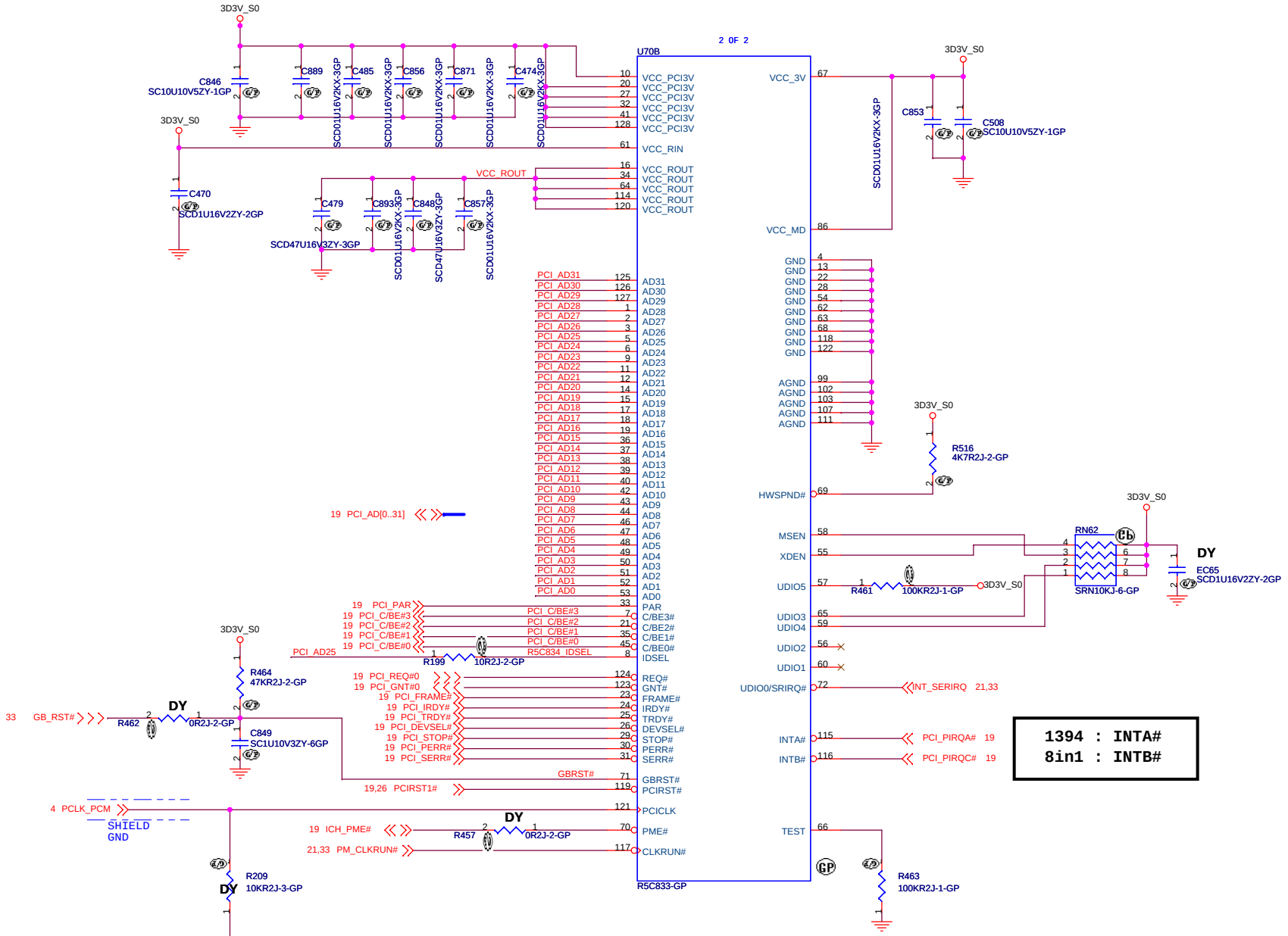




<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***HDD/ODD***	
Size A3	Document Number **Hawke-Intel**	Rev **SA**
Date: Tuesday, May 08, 2007	Sheet 23 of 55	



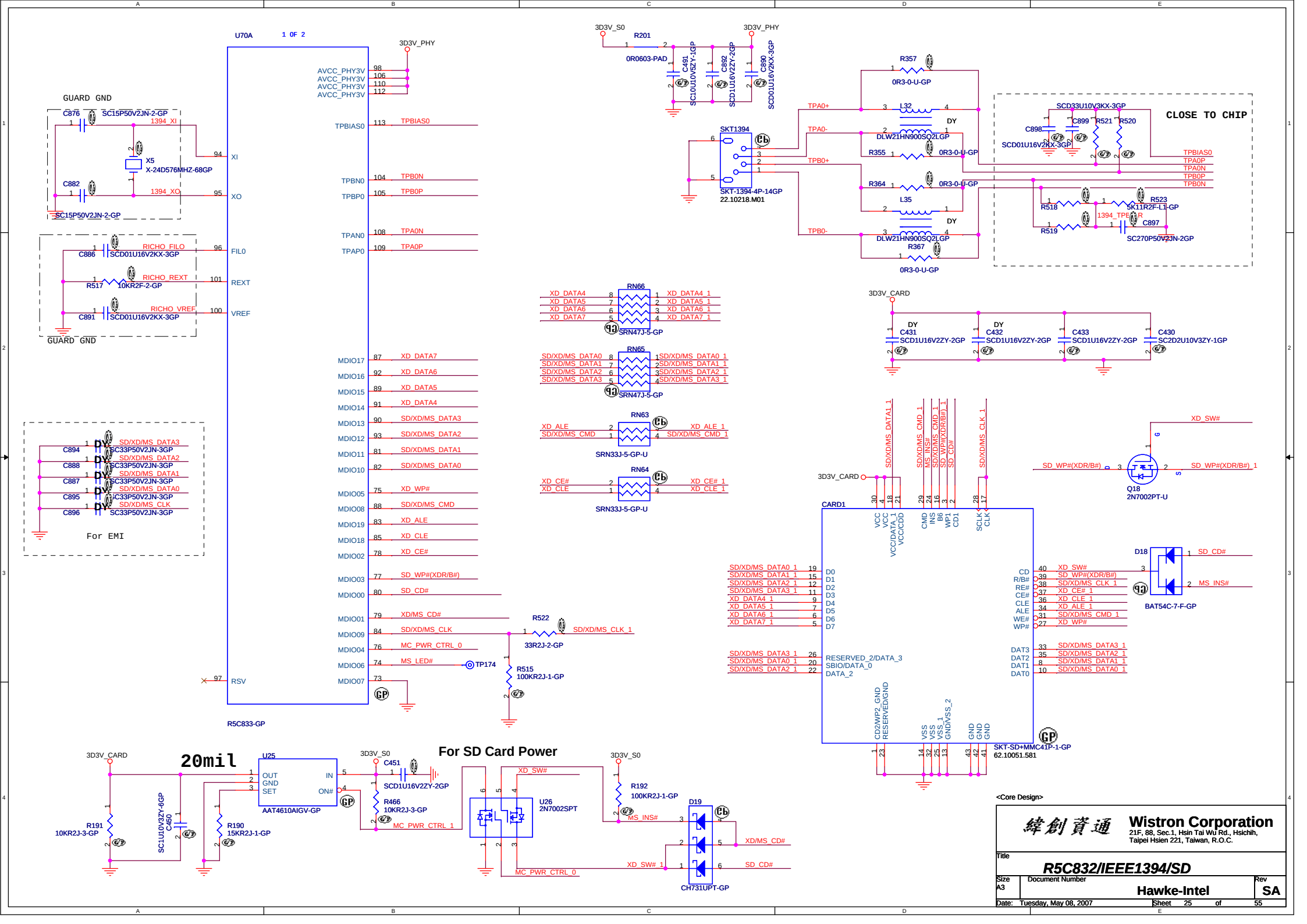
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***R5C833/PCI***

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Tuesday, May 08, 2007 Sheet 24 of 55


U70A
1 OF 2
R5C833-GP
GUARD GND
C876
SC15P50V2JN-2-GP
1394_XI
X5
X-24D576MHZ-68GP
C882
1394_XO
SC15P50V2JN-2-GP
RICHO_FILO
C886
SCD01U16V2KX-3GP
RICHO_REXT
R517
10KR2F-2-GP
RICHO_VREF
C891
SCD01U16V2KX-3GP
GUARD GND
For EMI
C894
C888
C887
C895
C896
SD/XD/MS_DATA3
SD/XD/MS_DATA2
SD/XD/MS_DATA1
SD/XD/MS_DATA0
SD/XD/MS_CLK
SC33P50V2JN-3GP
3D3V_PHY
AVCC_PHY3V
TPBIAS0
TPBN0
TPBP0
TPAN0
TPAP0
XI
XO
FIL0
REXT
VREF
RSV
MDIO17
MDIO16
MDIO15
MDIO14
MDIO13
MDIO12
MDIO11
MDIO10
MDIO05
MDIO08
MDIO19
MDIO18
MDIO02
MDIO03
MDIO00
MDIO01
MDIO09
MDIO04
MDIO06
MDIO07
XD_DATA7
XD_DATA6
XD_DATA5
XD_DATA4
SD/XD/MS_DATA3
SD/XD/MS_DATA2
SD/XD/MS_DATA1
SD/XD/MS_DATA0
XD_WP#
SD/XD/MS_CMD
XD_ALE
XD_CLE
XD_CE#
SD_WP#(XDR/B#)
SD_CD#
XD/MS_CD#
SD/XD/MS_CLK
MC_PWR_CTRL_0
MS_LED#
TP174
R522
33R2J-2-GP
R515
100KR2J-1-GP
3D3V_S0
R201
0R0603-PAD
C491
SC10U10V5ZY-1GP
C892
SCD1U16V2ZY-2GP
C890
SCD01U16V2KX-3GP
SKT1394
SKT-1394-4P-14GP
22.10218.M01
TPA0+
TPA0-
TPB0+
TPB0-
R357
R355
R364
R367
0R3-0-U-GP
L32
L35
DY
DLW21HN900SQ2LGP
CLOSE TO CHIP
SCD33U10V3KX-3GP
C898
C899
R521
R520
SCD01U16V2KX-3GP
TPBIAS0
TPA0P
TPA0N
TPB0P
TPB0N
R518
R519
R523
5K11R2F-L1-GP
1394_TPBR
C897
SC270P50V2JN-2GP
RN66
RN65
RN63
RN64
SRN47J-5-GP
SRN33J-5-GP-U
XD_DATA4_1
XD_DATA5_1
XD_DATA6_1
XD_DATA7_1
SD/XD/MS_DATA0_1
SD/XD/MS_DATA1_1
SD/XD/MS_DATA2_1
SD/XD/MS_DATA3_1
XD_ALE_1
SD/XD/MS_CMD_1
XD_CE#_1
XD_CLE_1
3D3V_CARD
C431
C432
C433
C430
SCD1U16V2ZY-2GP
SC2D2U10V3ZY-1GP
CARD1
SD/XD/MS_DATA1_1
SD/XD/MS_CMD_1
SD/XD/MS_INS#
SD/XD/MS_CLK_1
SD_WP#(XDR/B#)_1
SD_CD#
VCC
VCC
VCC/DATA_1
VCC/CDD
CMD
INS
B6
WP1
CD1
SCLK
CLK
D0
D1
D2
D3
D4
D5
D6
D7
RESERVED_2/DATA_3
SBIO/DATA_0
DATA_2
CD
R/B#
RE#
CE#
CLE
ALE
WE#
WP#
DAT3
DAT2
DAT1
DAT0
CD2/WP2_GND
RESERVED/GND
VSS
VSS_1
GND/VSS_2
GND
SKT-SD+MMC41P-1-GP
62.10051.581
XD_SW#
SD_WP#(XDR/B#)_1
Q18
2N7002PT-U
D18
BAT54C-7-F-GP
MS_INS#
20mil
U25
AAT4610AIGV-GP
OUT
GND
SET
IN
ON#
C451
SCD1U16V2ZY-2GP
R466
10KR2J-3-GP
R191
10KR2J-3-GP
R190
15KR2J-1-GP
C450
SC1U10V3ZY-6GP
For SD Card Power
U26
2N7002SPT
R192
100KR2J-1-GP
D19
CH731UPT-GP
XD/MS_CD#
SD_CD#
XD_SW#_1
MC_PWR_CTRL_0
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C832/IEEE1394/SD
Size
A3
Document Number
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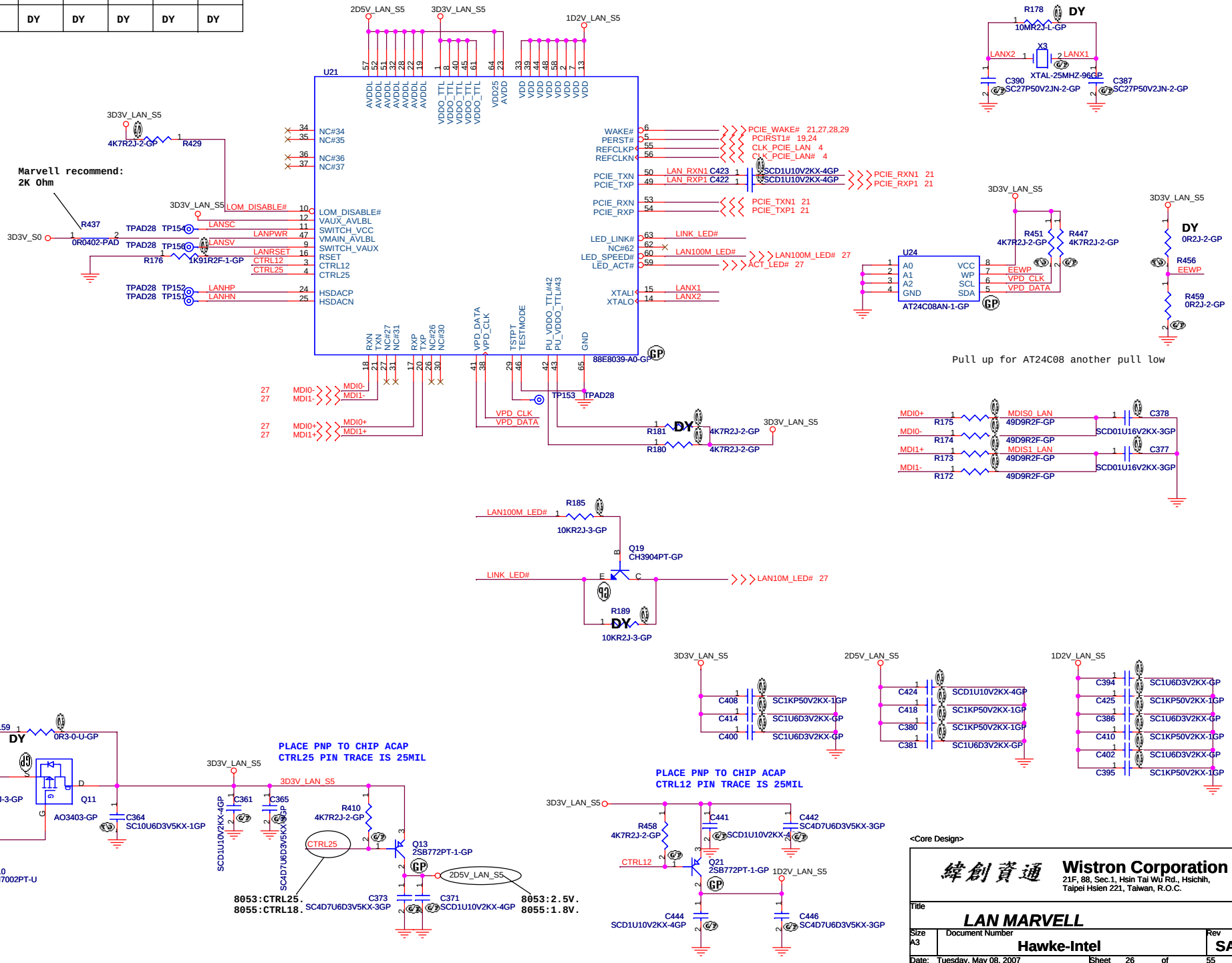
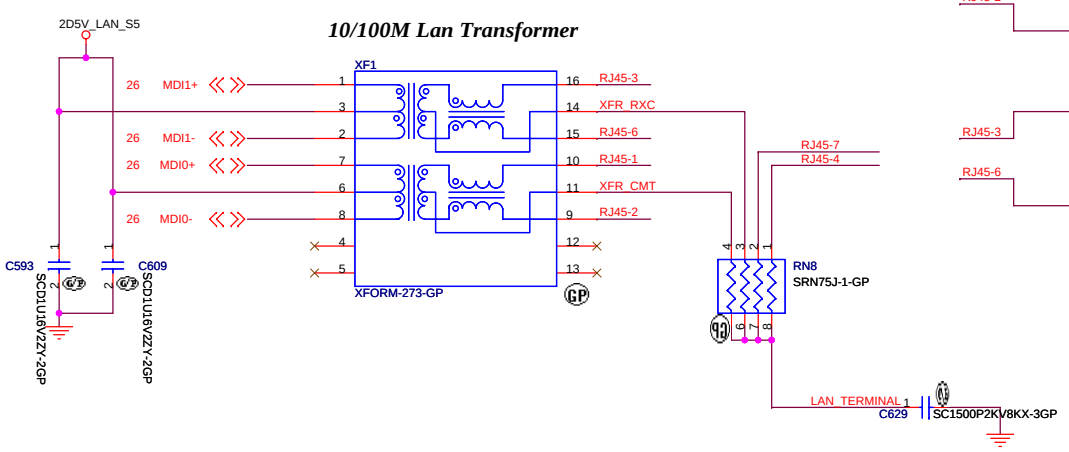
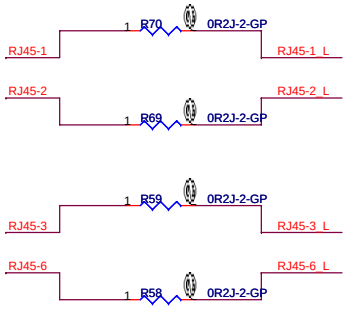
	R181	R176	R172	R173	R174	R175	C377	C378
88E8039	DY	1.91K	49.9	49.9	49.9	49.9	0.01u	0.01u
88E8040	4.7K	2K	DY	DY	DY	DY	DY	DY

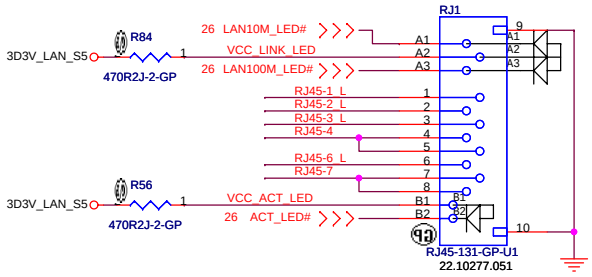


RJ45 Connector





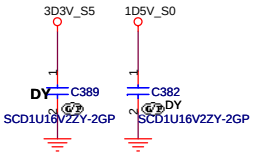
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



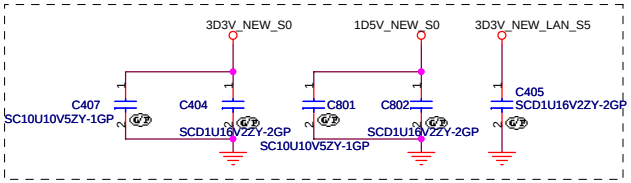
Yellow LED:TX/RX
Orange LED:Speed 100
Green LED:Speed 10

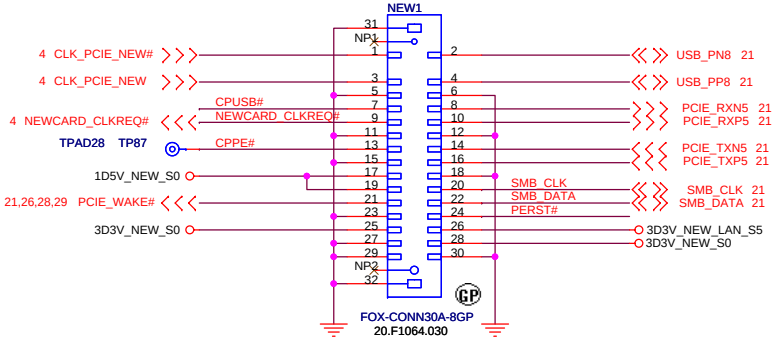
NEWCARD Connector

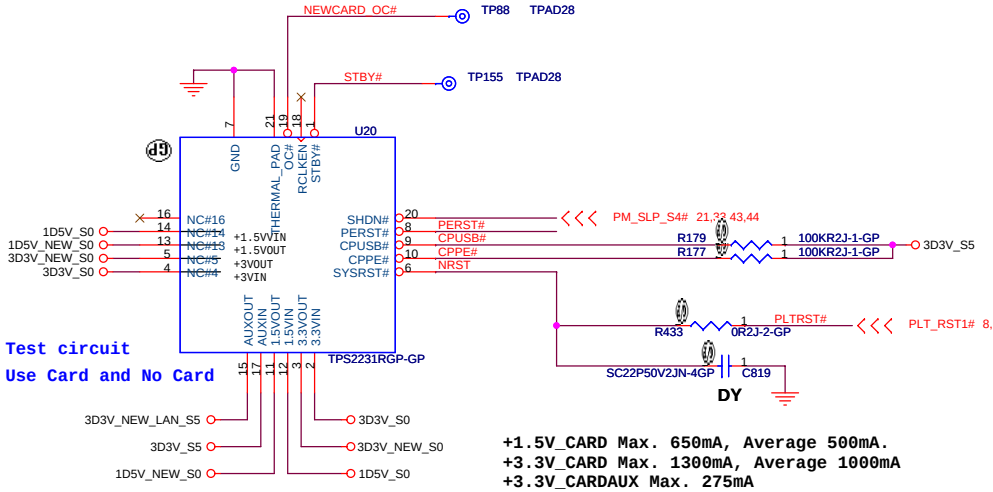
Place them Near to Chip



Place them Near to Connector

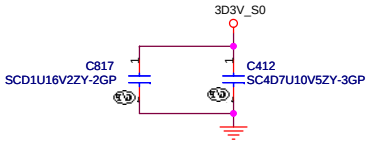






Test circuit
Use Card and No Card

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN connector/NEW CARD***

Size	Document Number	Rev
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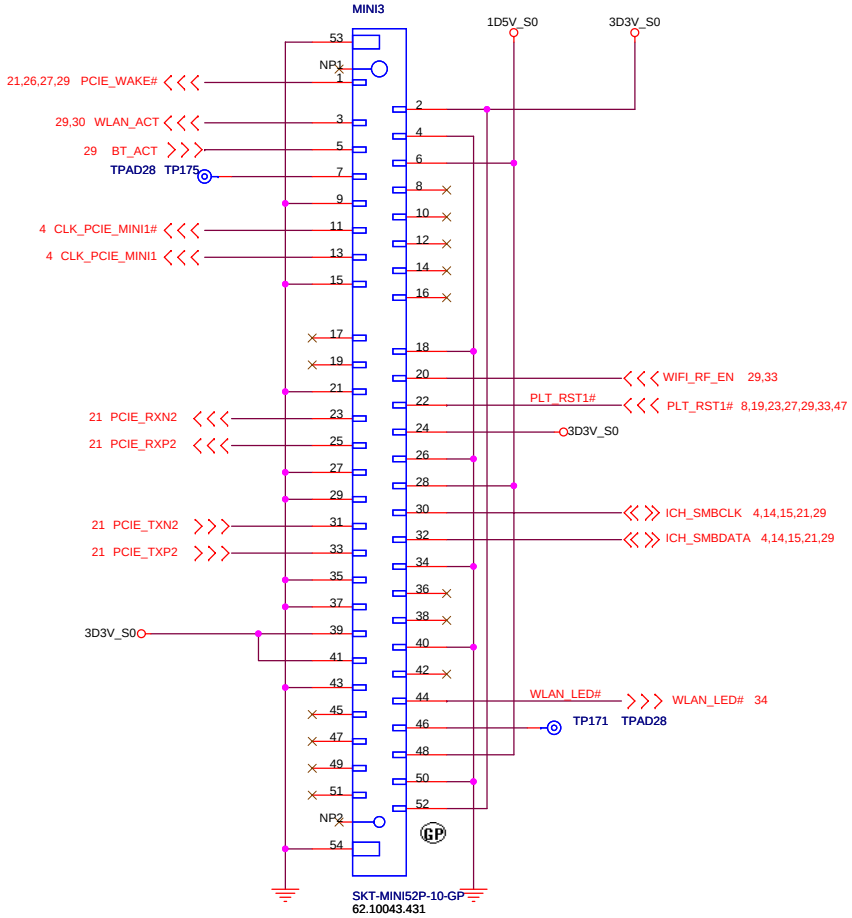
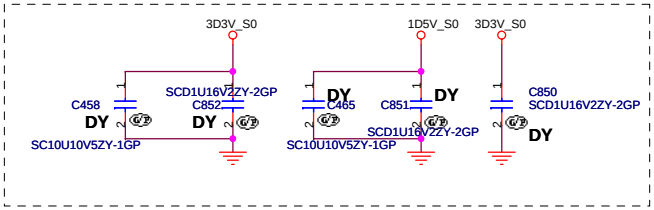
Mini Card Connector 2(802.11a/b/g)





<Core Design>

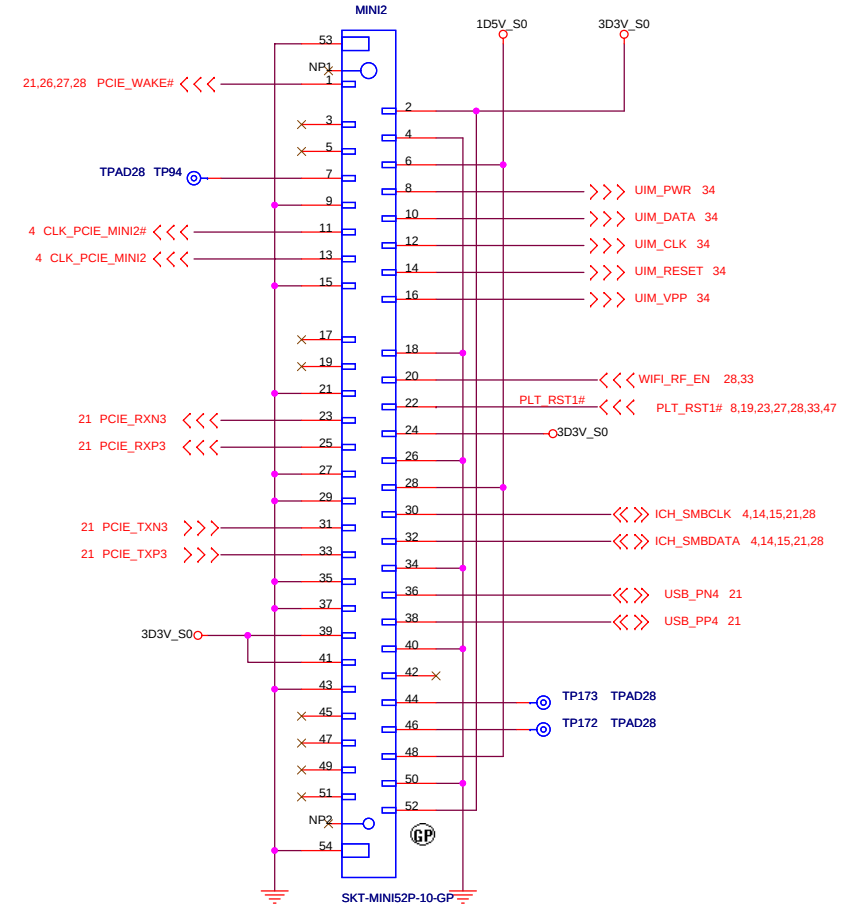
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

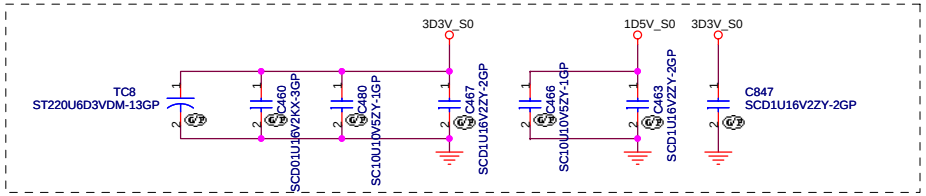
Title: MINI CARD CONN 1

Size	Document Number	Rev
A3	Hawke-Intel	SA

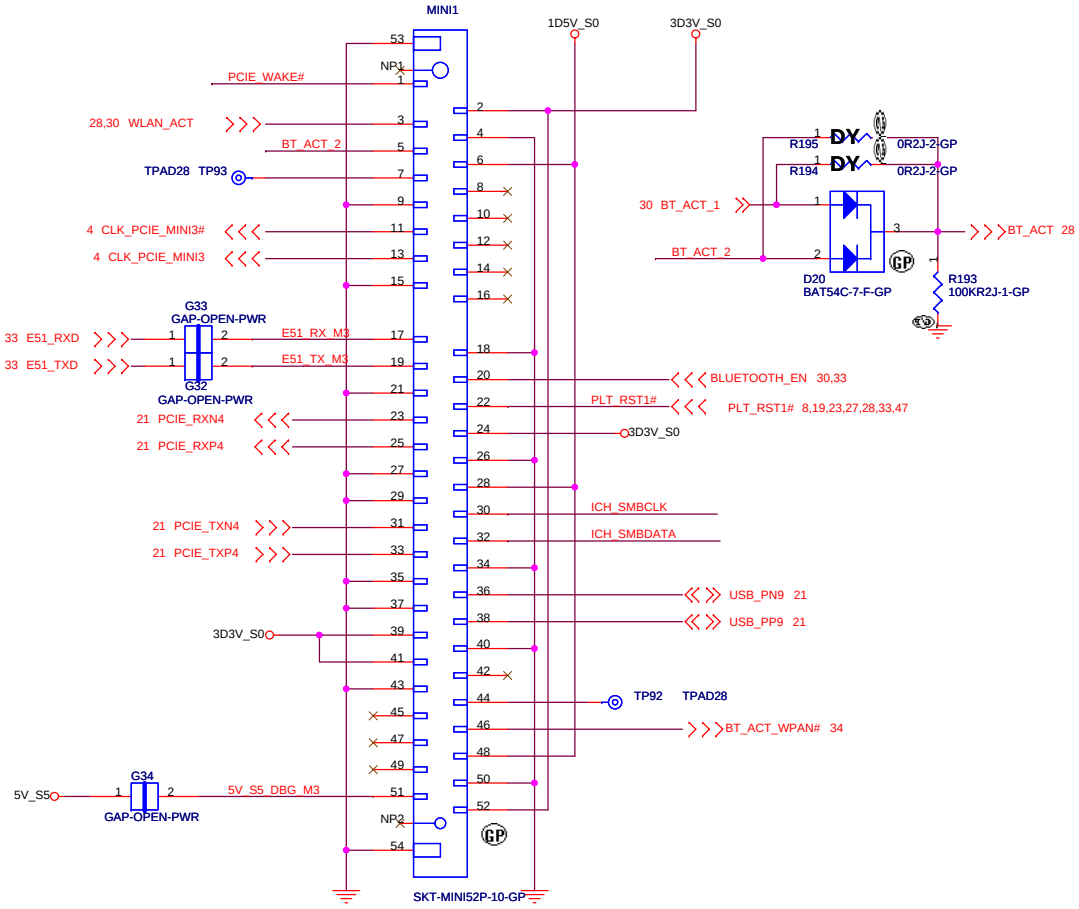
Date: Tuesday, May 08, 2007 Sheet 28 of 55

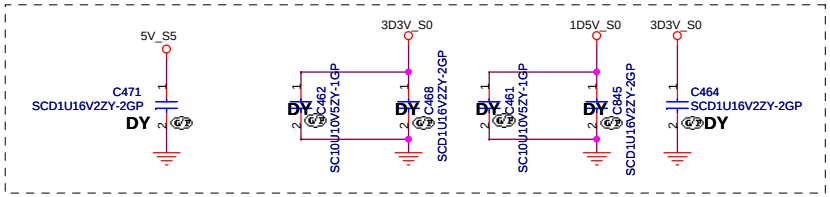
Mini Card Connector
Mini Card Connector 2(WWAN)





Mini Card Connector 3(Robson/BT)





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN 2 & 3

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SPI FLASH ROM

3D3V_AUX_S5

SRN10KJ-6-GP
RN43

SPI_HOLD#

C777
SC10U6D3V5KX-1GP
DY

C772
SCD1U16V2ZY-2GP

C771
SCD1U16V2ZY-2GP

8M Bits

U61
CS#
DO
WP#
GND
VCC
HOLD#
CLK
DIO
W25X80-VSSI-GP

33 SPICS#
33 SPIDI
R378
150R2J-L1-GP-U
EC49
SC4D7P50V2CN-1GP

SPICS#
SPI_SO0
SPI_WP#
SPI_HOLD#
SPI_CLK0
SPI_SI0

EMI REQUEST

R384
150R2J-L1-GP-U
SPIDO 33

R382
150R2J-L1-GP-U
SPICLK 33

EC55
SC4D7P50V2CN-1GP

EC51
SC4D7P50V2CN-1GP

Place close to EC

Switch Board

SNIFFER_BD1
MLX-CON10-6
20.D0174.110

33 WLAN/BT_BTN#
33 SNIFFER_PWR_SW#
33 SNIFFER_YELLOW#
33 SNIFFER_BLUE#
5V_S5

C872
SCD1U10V2KX-4GP

SC33P50V2JN-3GP
C864 SNIFFER_PWR_SW#
C867 SNIFFER_YELLOW#
C869 SNIFFER_BLUE#
C870
WLAN/BT_BTN#

CIR

3D3V_AUX_S5
3D3V_S5
R216
100R2J-2-GP
33 CIRRX
R220
10KR2J-3-GP
SIO_CIRRX_VS
U34
OUT
VS
GND
GND
TSOP36136-GP
SC4D7U6D3V5KX-3GP
C512
SCD1U10V2KX-4GP
C513

To Hall Switch

3D3V_S5
C500
SCD1U10V2KX-4GP
DY

R208
100KR2J-1-GP
R214
10R2J-2-GP
33 LID_CLOSE#
LID_CL#
C507
SCD047U10V2KX-2GP
CN3
FOX-CON4-12-GP
20.K0179.004

CAPACITY BUTTON

5V_S0
RN1
SRN10KJ-5-GP
DY
35 CAP_SCL
35 CAP_SDA
33 CAPA_INT#
CAP1
FOX-CON8-4-GP
20.K0178.008

Bluetooth Module conn.

BT1
FOX-CON10-GP
20.F0711.010

USB_P5+
USB_P5-
BT_LED
29 BT_ACT_1
29,33 BLUETOOTH_EN
28,29 WLAN_ACT

3D3V_S0
C627
SCD1U10V2KX-4GP
R316
10KR2J-3-GP

34 BT_ACT_K#
Q36
R1
R2
PDTC124EU-1-GP

21 USB_PP5
R322 0R2J-2-GP
USB_P5+
TR1
L-63UH-GP
DY
21 USB_PN5
USB_P5-
R319 0R2J-2-GP

Biometric Connector

21 USB_PN7
R127
0R3-0-U-GP
L13
DLW21SN900SQ2LUGP
DY
21 USB_PP7
R126
0R3-0-U-GP

3D3V_S0
C268
SCD1U10V2KX-4GP

Biometric_USBP-
Biometric_USBP+
CN2
ACES-CON6-8GP
20.K0228.006

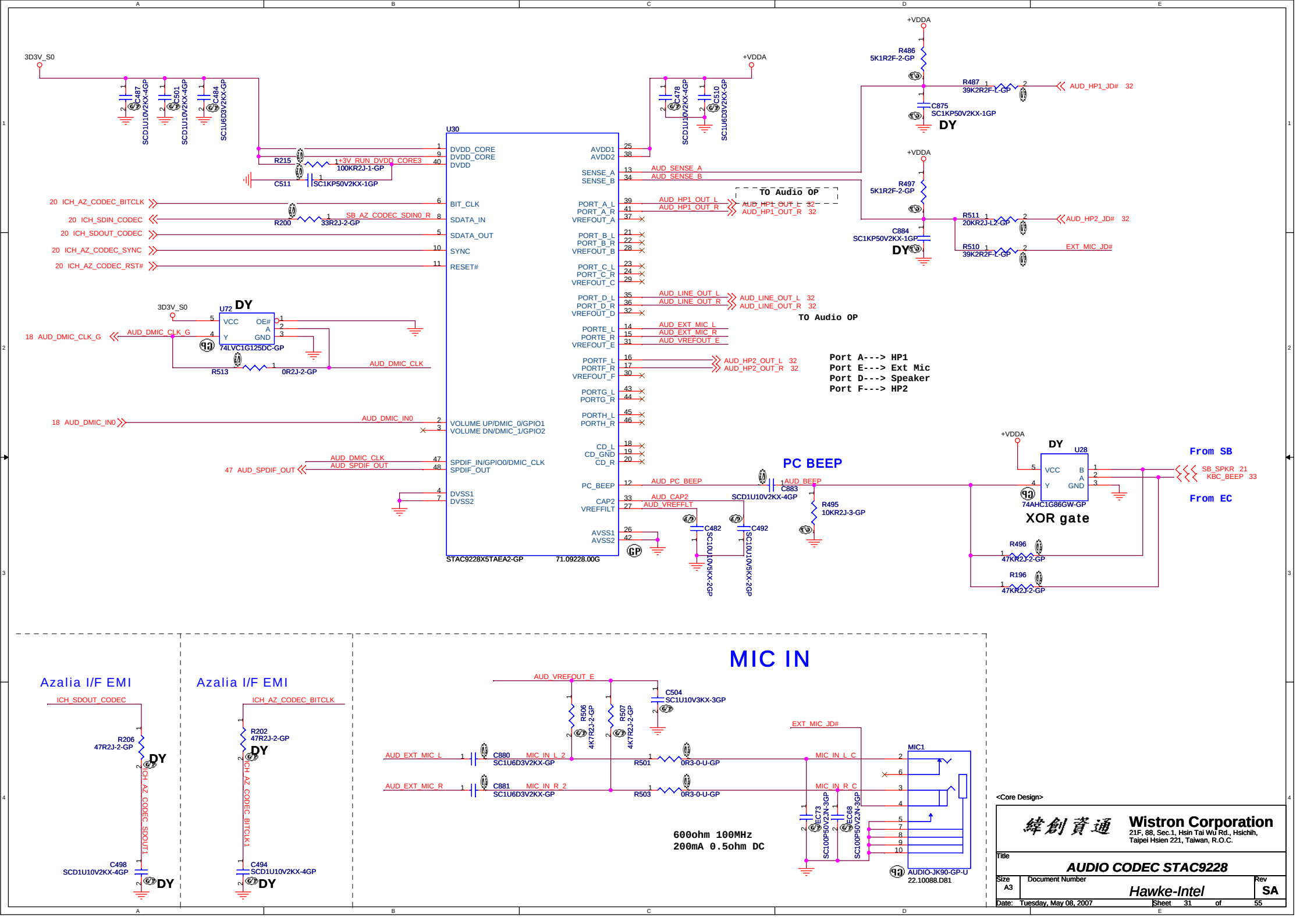
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPI/SNIFFER/CIR/BT/Biometric

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Tuesday, May 08, 2007 Sheet 30 of 55



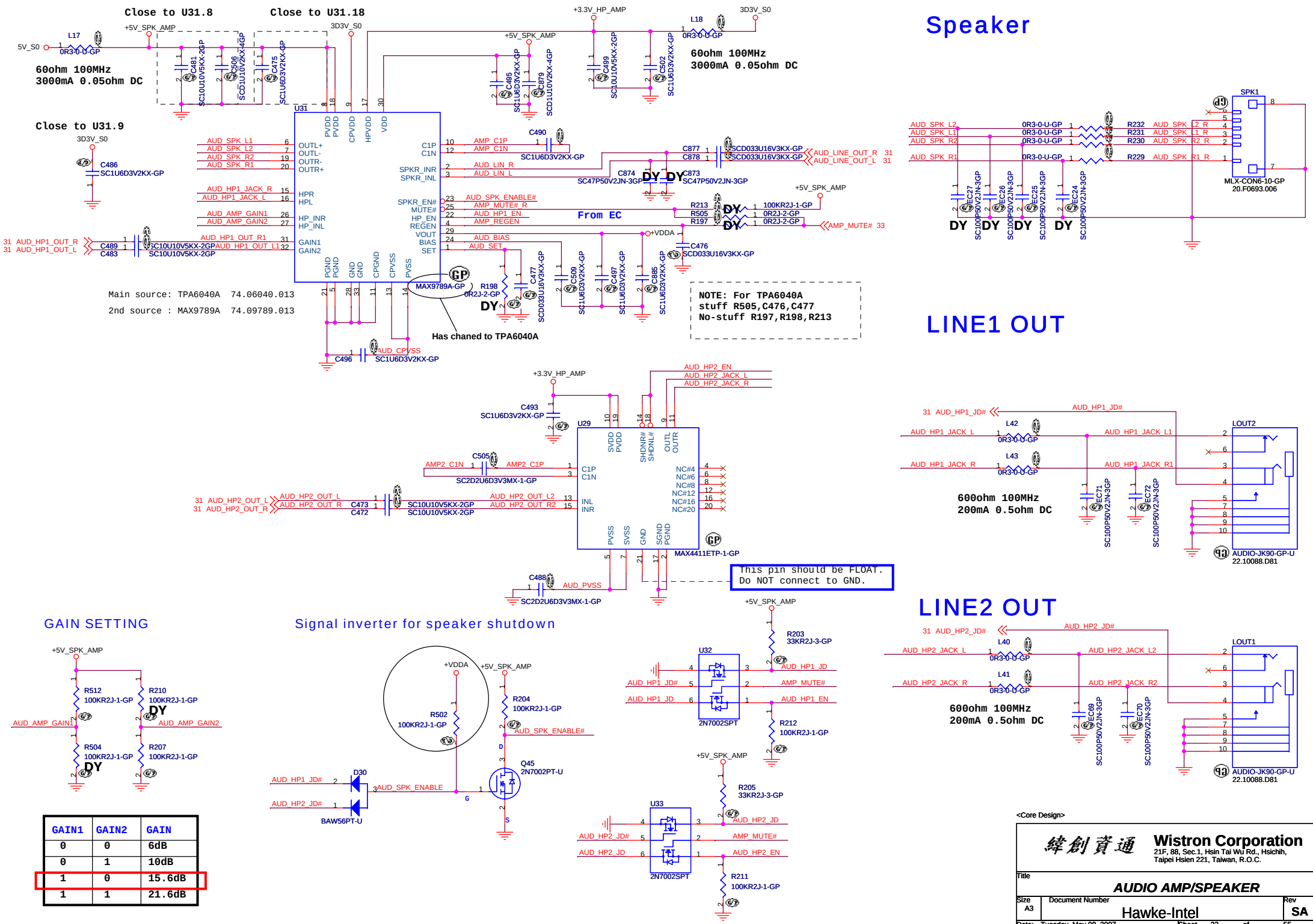
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC STAC9228

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Tuesday, May 08, 2007 Sheet 31 of 55


Close to U31.8
Close to U31.18
Close to U31.9
60ohm 100MHz
3000mA 0.05ohm DC
Main source: TPA6040A 74.06040.013
2nd source : MAX9789A 74.09789.013
Has chaned to TPA6040A
NOTE: For TPA6040A
stuff R505,C476,C477
No-stuff R197,R198,R213
From EC
MAX9789A-GP
Speaker
SPK1
MLX-CON6-10-GP
20.F0693.006
LINE1 OUT
LOUT2
AUDIO-JK90-GP-U
22.10088.D81
600ohm 100MHz
200mA 0.5ohm DC
LINE2 OUT
LOUT1
MAX4411ETP-1-GP
This pin should be FLOAT.
Do NOT connect to GND.
GAIN SETTING
Signal inverter for speaker shutdown
2N7002SPT
BAW56PT-U
GAIN1 GAIN2 GAIN
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO AMP/SPEAKER
Hawke-Intel
Size A3
Rev SA
Date: Tuesday, May 08, 2007
Sheet 32 of 55

PLACE CAP NEAR PIN80 AND PIN102

PLACE CAP NEAR PIN46,10,115,76,88

PLACE CAP NEAR PIN104

PLACE CAP Close to Pin 4

WPC8763L STRAP PIN

JEN0 (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES		GPIO Port	Keyboard Scan
10K PD	NO PD	JTAG signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

TRIS#(Pin 110) TRI-STATE

Forces the device to float all its output and I/O pins,if an external 10 KΩ pull-down resistor is conected.

BADDR1-0 (PIN 111, 112) I/O Base Address.
10KΩ external pull-down
resistor on BADDR1: Core defined

SHBM PIPN83 Shared Host BIOS Memory.
HIGH:NO SHARED(internal resistor)
LOW:SHARED BIOS memory.

FOR THERMAL AND VOLUME CONTROL THERMAL----->

KBC DEBUG POINT

<-----BATTERY

MB VERSION ID

	VER0	VER1
SA	0	0
SB	0	1
SC	1	0
SD	1	1

ADIA:to Charger
ACDC_ID:from Adapter Conn
KBC_PWRBTN#:from power button
BAT_IN#:from Battery Conn
DC_BATFULL#:for Battery charge LED 1
WLAN_TEST:for WKS test WLAN LED
AD_OFF:enable AC adapter power source
CHARGE_LED#:for Battery charge LED 2
WLAN/BT_BTN#:from Wlan on/off button
GMCH_BL_ON:Sense The Backlight On/Off Status from VGA Chip
WIRELESS_EN:Disable/Enable Wireless Module
BLUETOOTH_EN:Disable/Enable Bluetooth
USB_PWR_EN#:to on/off USB power switch
CCD_ON:Webcam power on/off
AC_IN#:From Charge

WPC8763L XTAL

KBC CLK EMI

<Core Design>

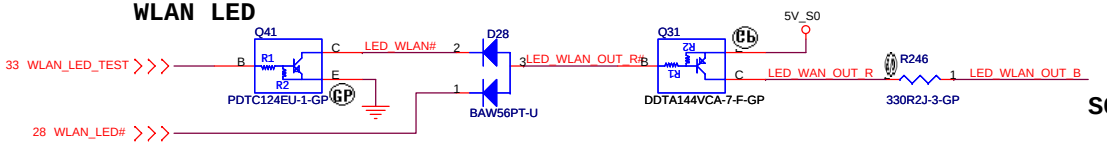
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_Winbond WPC8763L

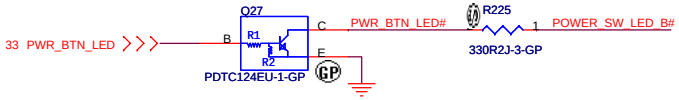
Size: A2 | Document Number: Hawke-Intel | Rev: SA

Date: Tuesday, May 08, 2007 | Sheet 33 of 55

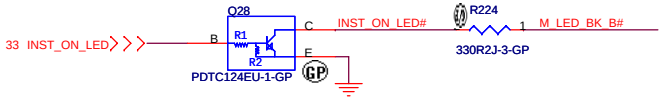
WLAN LED



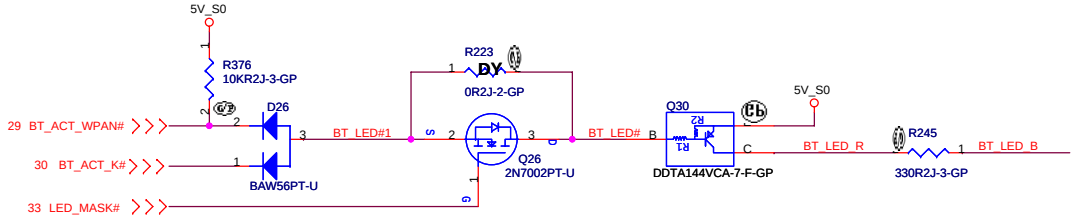
Power Button LED



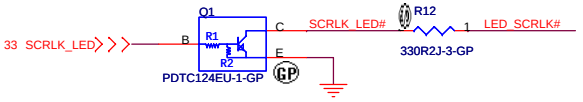
Instant Power Button LED



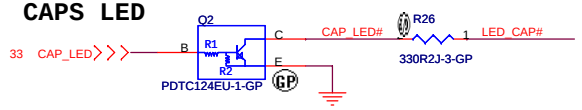
Bluetooth LED



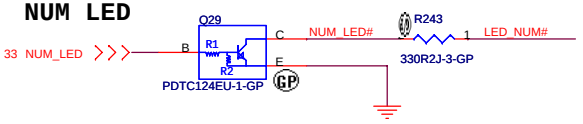
SCRLK LED

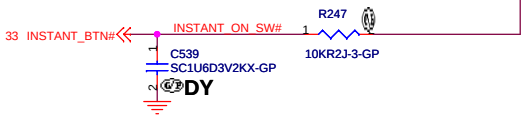


CAPS LED

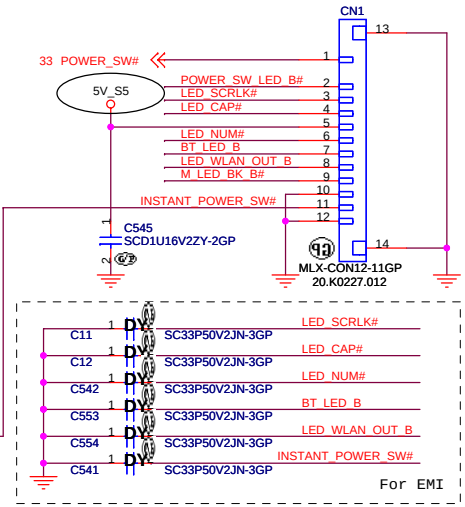


NUM LED

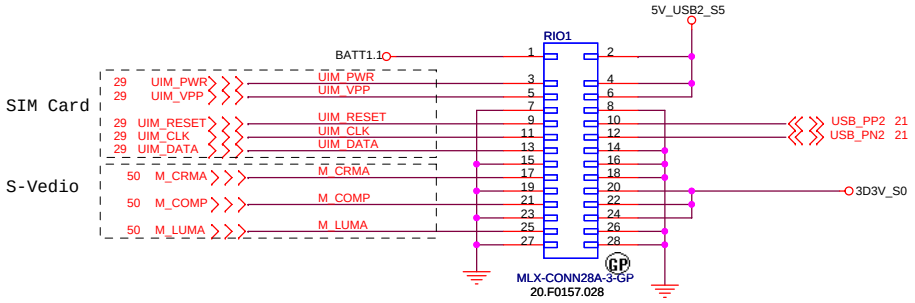




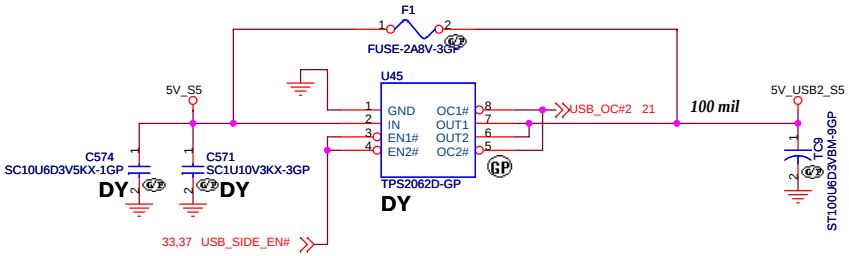
To LED Board

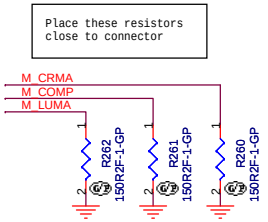


To Right I/O Board



USB POWER





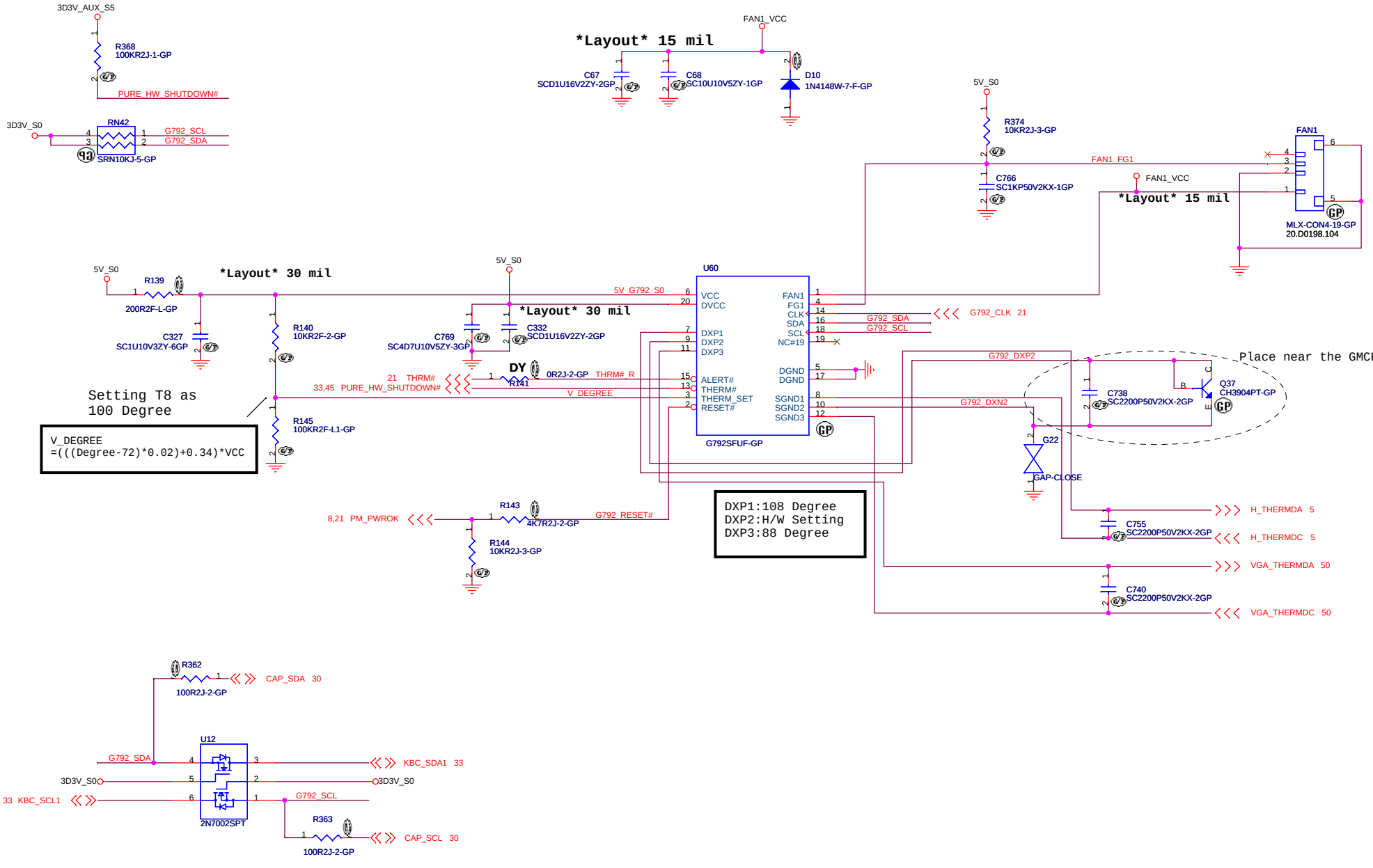
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Right I/O/ Power Dash***

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Tuesday, May 08, 2007 Sheet 34 of 55



<Core Design>

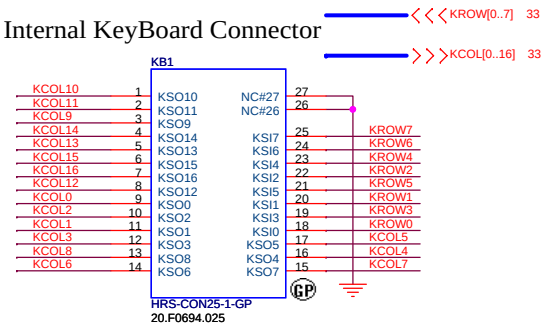
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

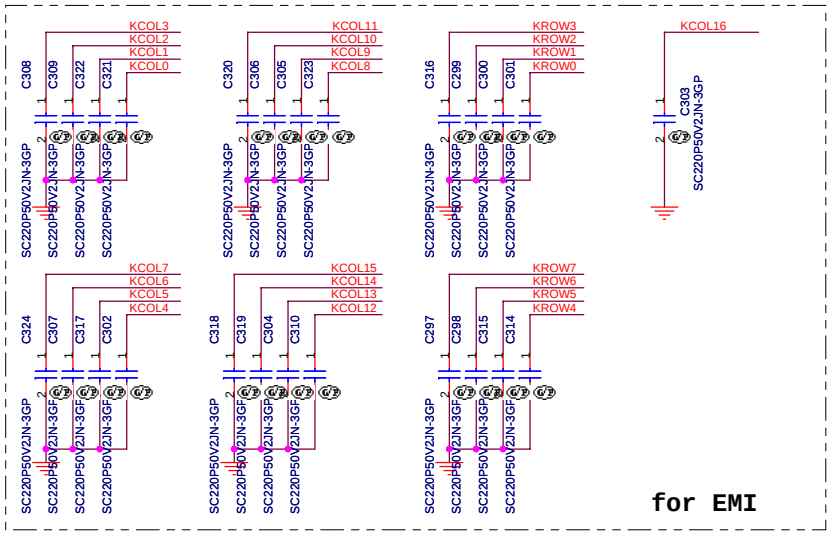
Title: Thermal/Fan Controllor G792

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Tuesday, May 08, 2007 Sheet 35 of 55

Internal KeyBoard Connector





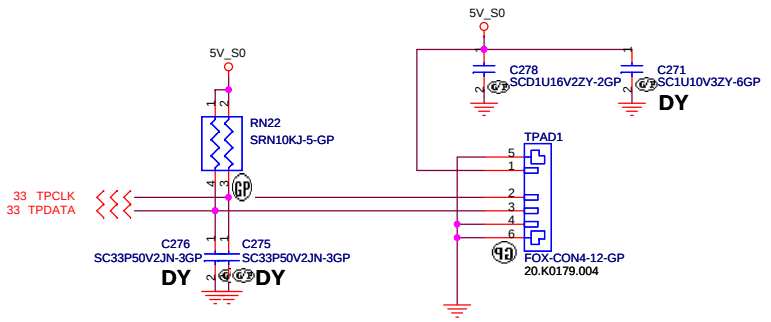
LED Board

LED NAME	ACTIVE SIGNAL	
Power Button LED	PWR_BTN_LED	*
Instant Power Button LED	INST_ON_LED	*
WLAN LED	WLAN_LED_TEST (from KBC) WLAN_LED# (from Mini)	
Bluetooth LED	BT_ACT_WPAN# (from Mini) BT_ACT_K# (from BT)	
NUM LED	NUM_LED (from KBC)	
SCRLK LED	SCRLK_LED (from KBC)	
CAPS LED	CAP_LED (from KBC)	

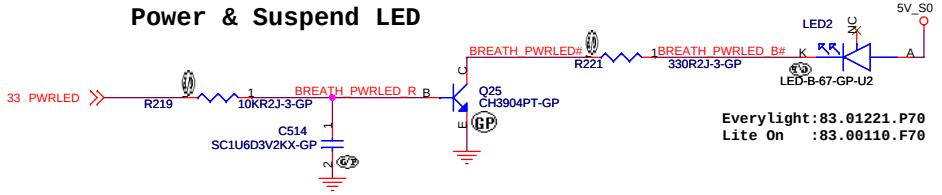
Main Board

Power & Suspend LED	PWRLED	(from KBC)
HDD LED	SATA_LED#	(from ICH)
Battery LED	BATFULL_LED CHARGE_LED	(from KBC)

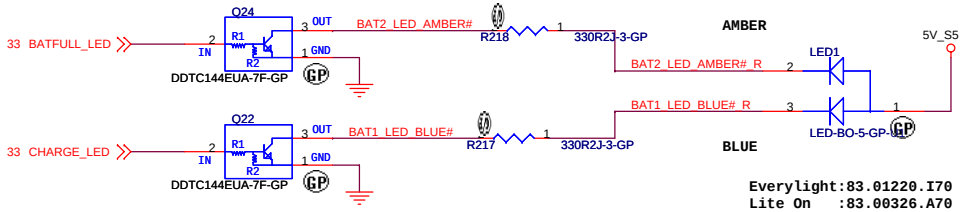
TouchPad Connector



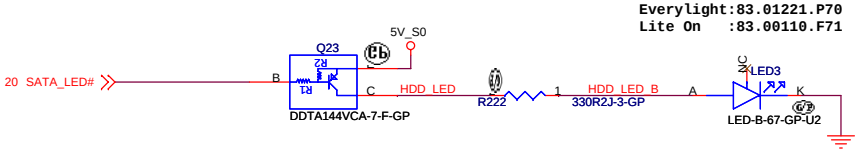
Power & Suspend LED



Battery LED



HDD LED



<Core Design>

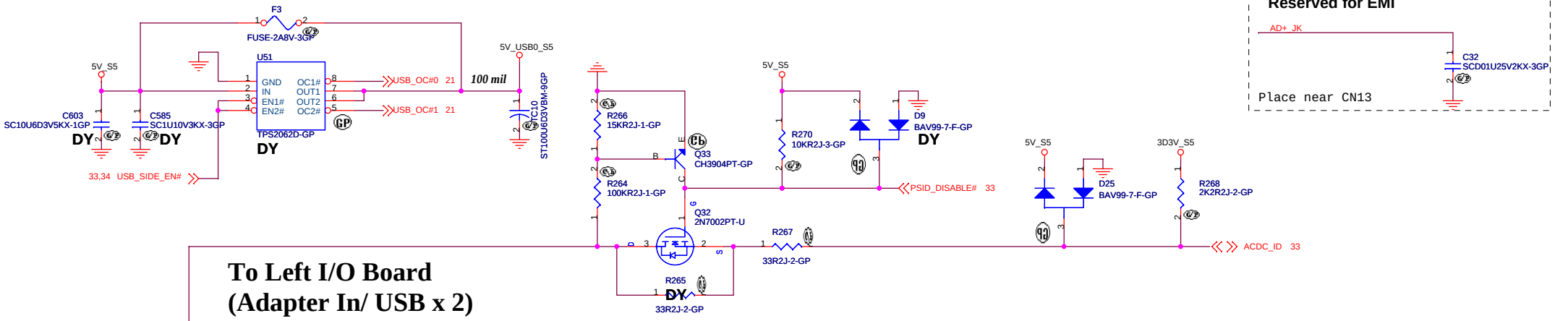
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KeyBoard/Touchpad

Size: A3 | Document Number: Hawke-Intel | Rev: SA

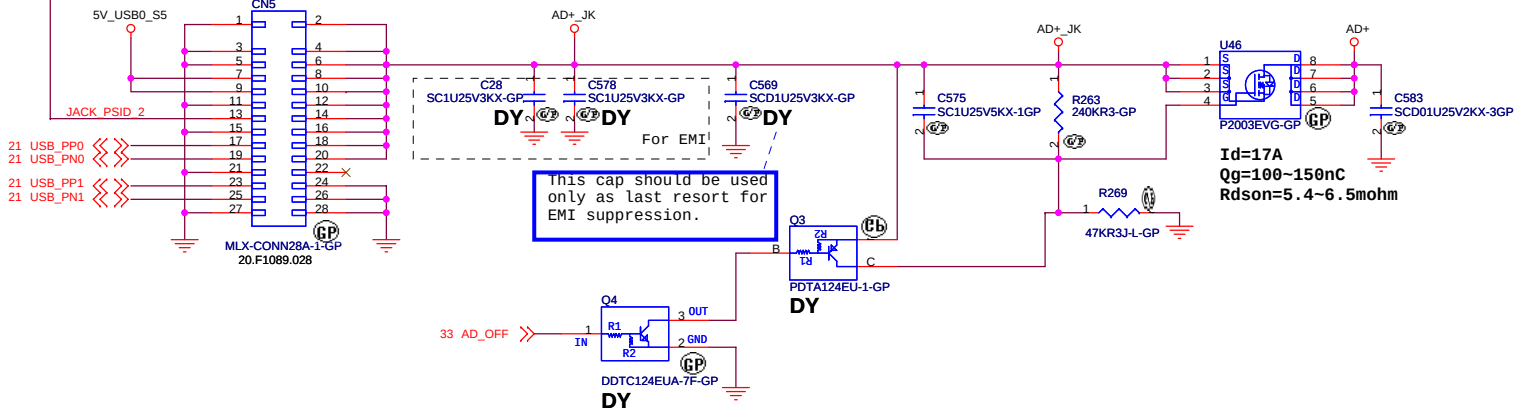
Date: Tuesday, May 08, 2007 | Sheet 36 of 55

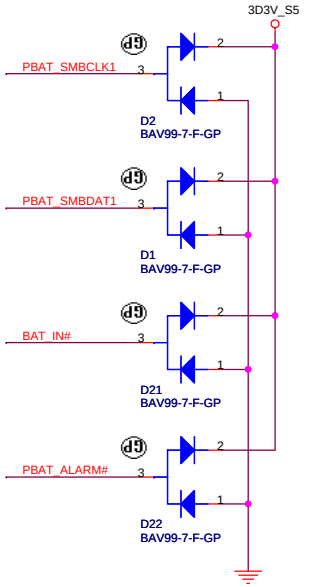
USB POWER



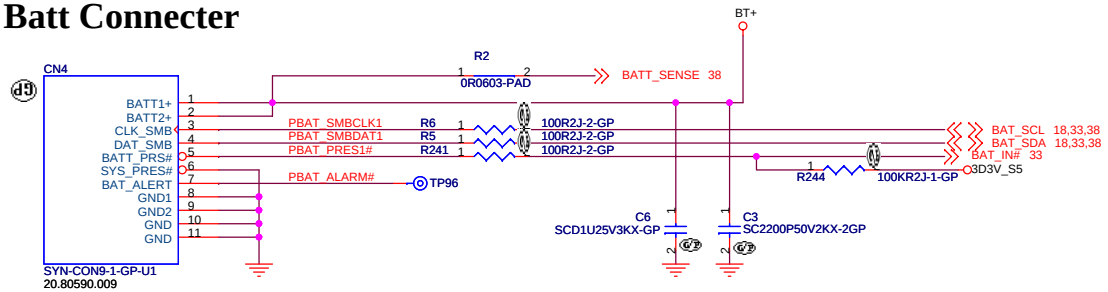
Reserved for EMI

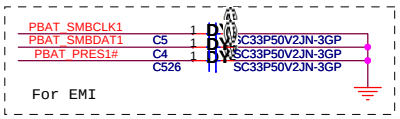
To Left I/O Board (Adapter In/ USB x 2)





Batt Connecter





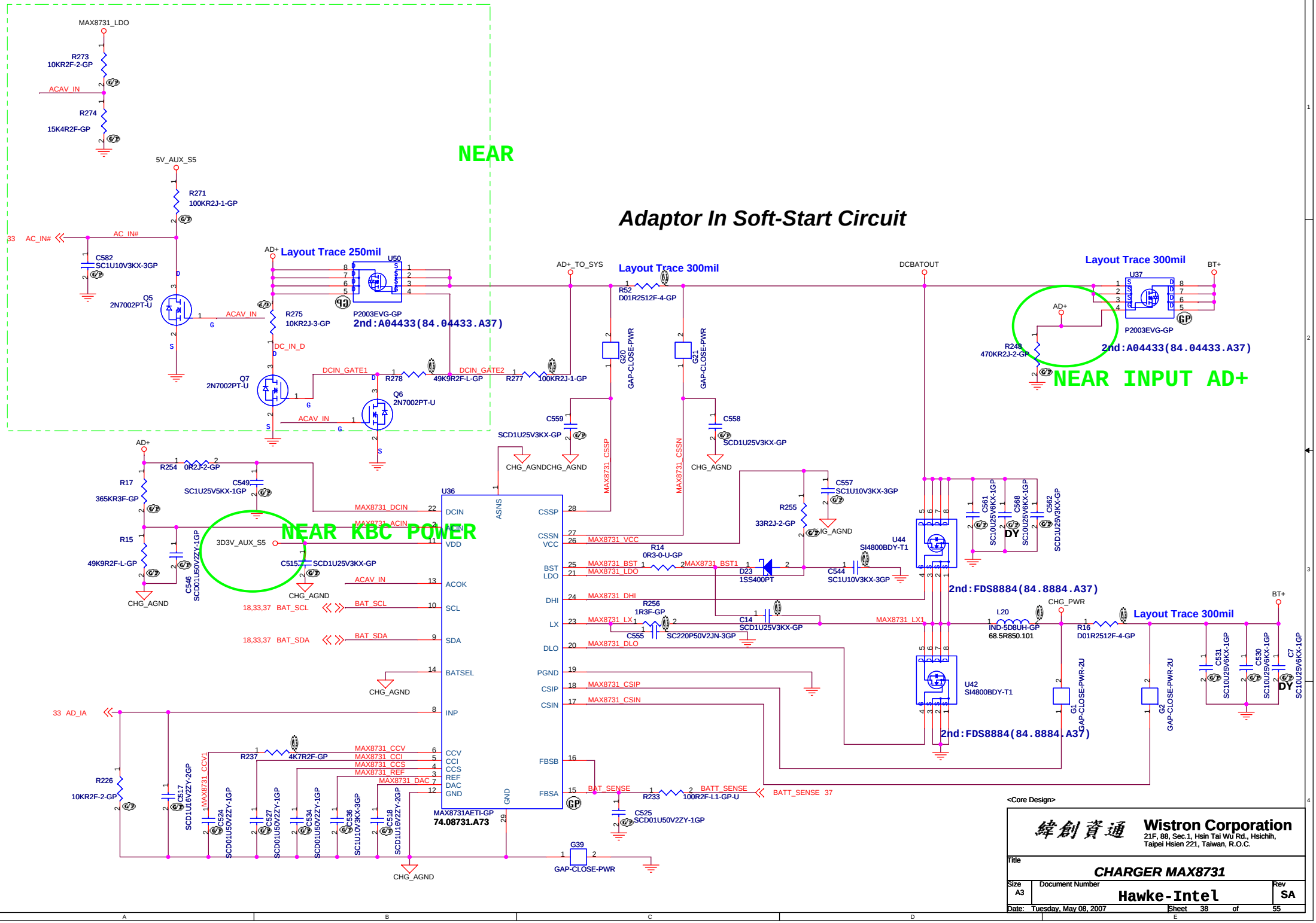
<Core Design>

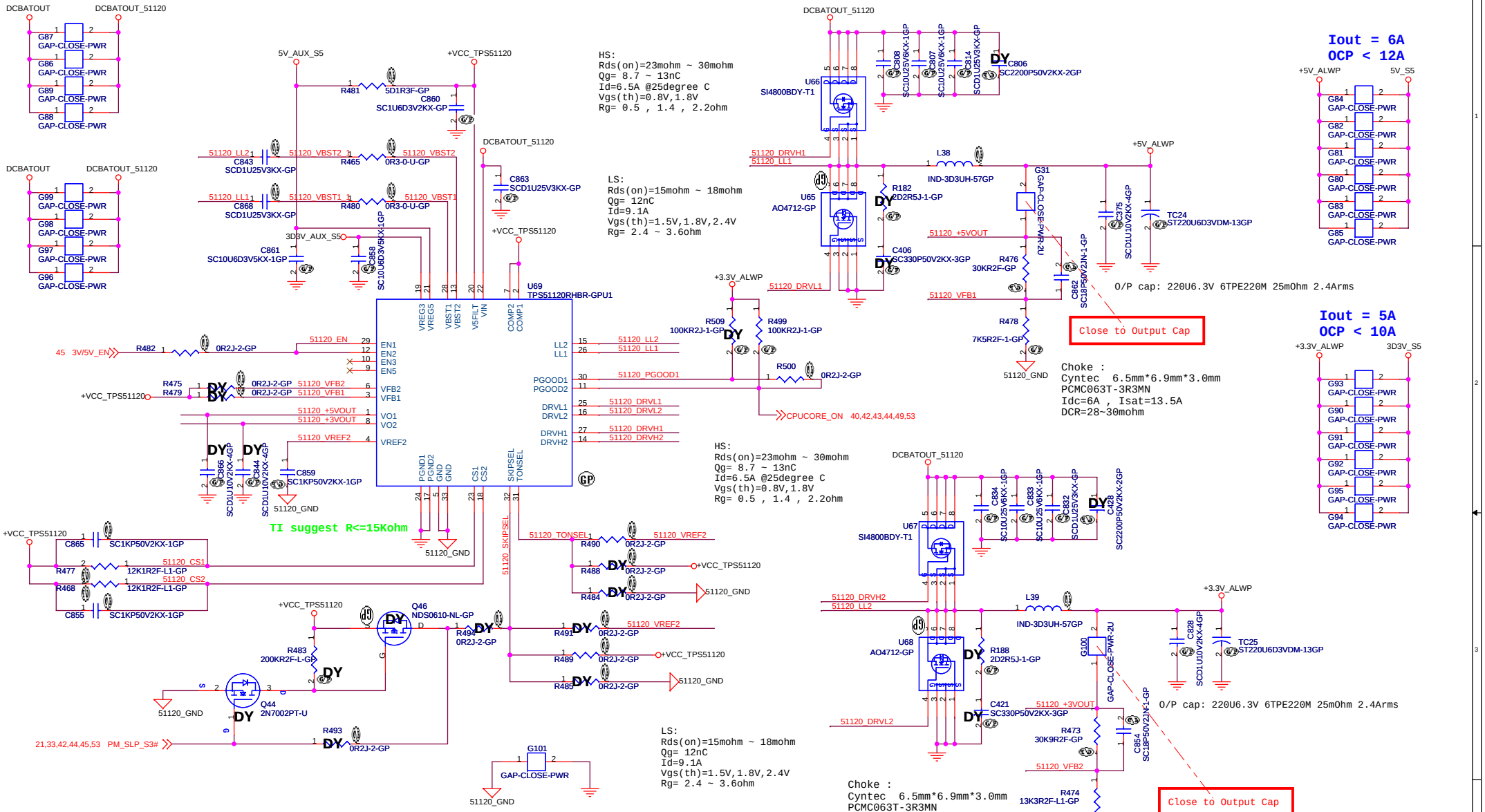
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

Size: A3 | Document Number: Hawke-Intel | Rev: SA

Date: Tuesday, May 08, 2007 | Sheet 37 of 55


Adaptor In Soft-Start Circuit
NEAR
NEAR KBC POWER
NEAR INPUT AD+
MAX8731_LDO
R273
10KR2F-2-GP
ACAV_IN
R274
15K4R2F-GP
5V_AUX_S5
R271
100KR2J-1-GP
33 AC_IN#
AC_IN#
C582
SC1U10V3KX-3GP
Q5
2N7002PT-U
AD+
Layout Trace 250mil
U50
P2003EVG-GP
2nd:A04433(84.04433.A37)
R275
10KR2J-3-GP
DC_IN_D
Q7
2N7002PT-U
DCIN_GATE1
R278
49K9R2F-L-GP
DCIN_GATE2
R277
100KR2J-1-GP
Q6
2N7002PT-U
AD+_TO_SYS
Layout Trace 300mil
R52
D01R2512F-4-GP
G20
GAP-CLOSE-PWR
G21
GAP-CLOSE-PWR
DCBATOUT
C559
SCD1U25V3KX-GP
C558
SCD1U25V3KX-GP
CHG_AGNDCHG_AGND
CHG_AGND
MAX8731_CSSP
MAX8731_CSSN
Layout Trace 300mil
U37
P2003EVG-GP
BT+
R248
470KR2J-2-GP
2nd:A04433(84.04433.A37)
AD+
R254
0R2J-2-GP
R17
365KR3F-GP
C549
SC1U25V5KX-1GP
R15
49K9R2F-L-GP
C546
SCD01U50V2ZY-1GP
3D3V_AUX_S5
C515
SCD1U25V3KX-GP
CHG_AGND
U36
MAX8731_DCIN
MAX8731_ACIN
VDD
ACAV_IN
ACOK
18,33,37 BAT_SCL
BAT_SCL
SCL
18,33,37 BAT_SDA
BAT_SDA
SDA
BATSEL
CHG_AGND
33 AD_IA
INP
R237
4K7R2F-GP
MAX8731_CCV
MAX8731_CCI
MAX8731_CCS
MAX8731_REF
MAX8731_DAC
CCV
CCI
CCS
REF
DAC
GND
R226
10KR2F-2-GP
C517
SCD1U16V2ZY-2GP
MAX8731_CCV1
C524
SCD01U50V2ZY-1GP
C527
SCD01U50V2ZY-1GP
C534
SCD01U50V2ZY-1GP
C536
SC1U10V3KX-3GP
C518
SCD1U16V2ZY-2GP
CHG_AGND
MAX8731AETI-GP
74.08731.A73
ASNS
CSSP
CSSN
VCC
BST
LDO
DHI
LX
DLO
PGND
CSIP
CSIN
FBSB
FBSA
GND
MAX8731_VCC
MAX8731_BST
MAX8731_BST1
MAX8731_LDO
MAX8731_DHI
MAX8731_LX
MAX8731_LX1
MAX8731_DLO
MAX8731_CSIP
MAX8731_CSIN
BAT_SENSE
BATT_SENSE
BATT_SENSE 37
R14
0R3-0-U-GP
R255
33R2J-2-GP
IG_AGND
C557
SC1U10V3KX-3GP
D23
1SS400PT
C544
SC1U10V3KX-3GP
U44
SI4800BDY-T1
R256
1R3F-GP
C555
SC220P50V2JN-3GP
C14
SCD1U25V3KX-GP
2nd:FDS8884(84.8884.A37)
U42
SI4800BDY-T1
2nd:FDS8884(84.8884.A37)
L20
IND-5D8UH-GP
68.5R850.101
CHG_PWR
R16
D01R2512F-4-GP
Layout Trace 300mil
BT+
C561
SC10U25V6KX-1GP
C568
SC10U25V6KX-1GP
C562
SCD1U25V3KX-GP
DY
C531
SC10U25V6KX-1GP
C530
SC10U25V6KX-1GP
C7
SC10U25V6KX-1GP
DY
G1
GAP-CLOSE-PWR-2U
G2
GAP-CLOSE-PWR-2U
C525
SCD01U50V2ZY-1GP
G39
GAP-CLOSE-PWR
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER MAX8731
Size
A3
Document Number
Hawke-Intel
Rev
SA
Date: Tuesday, May 08, 2007
Sheet 38 of 55



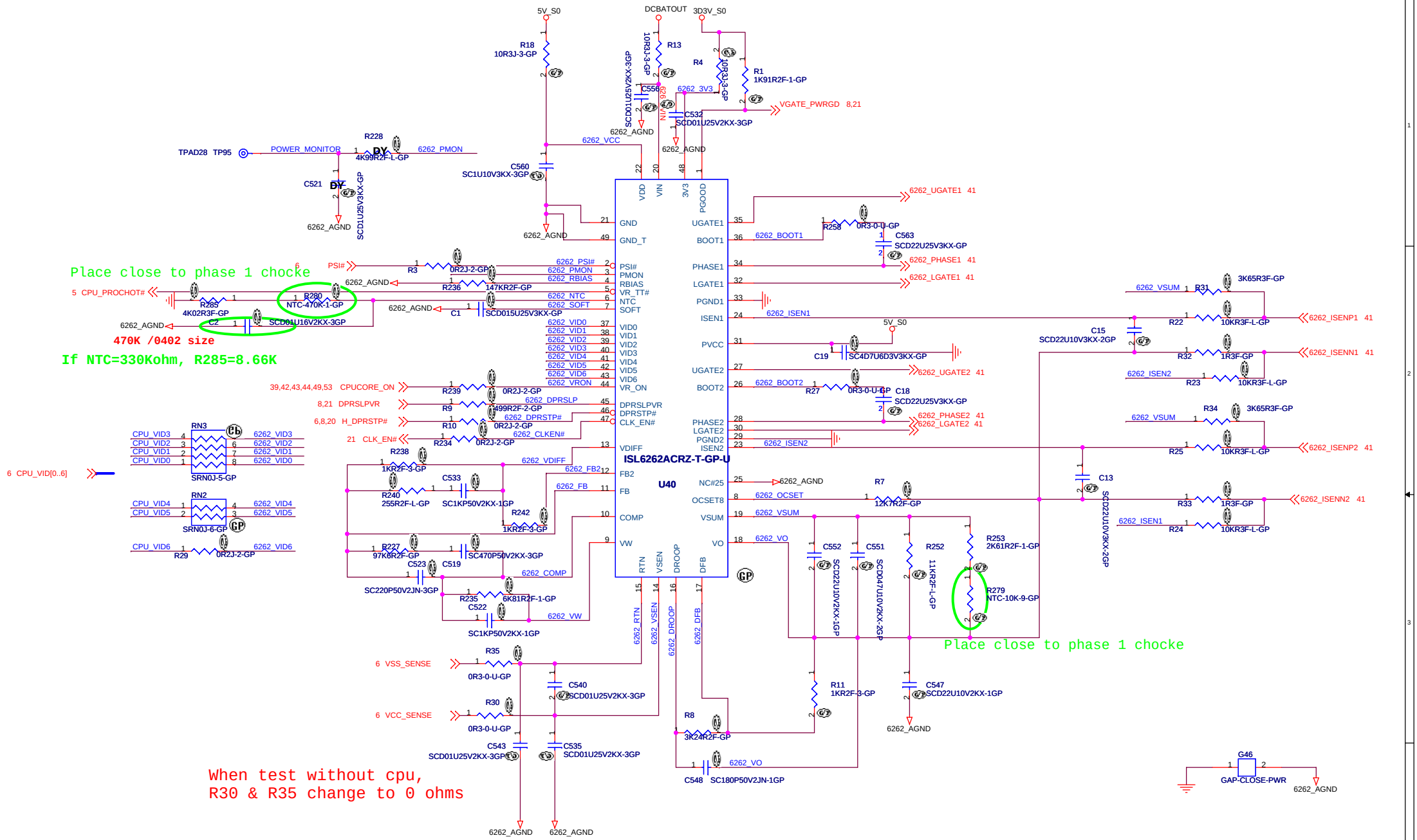
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 3.3V & 5V

Size: Custom | Document Number: Hawke-Intel | Rev: SA

Date: Tuesday, May 08, 2007 | Sheet 39 of 55



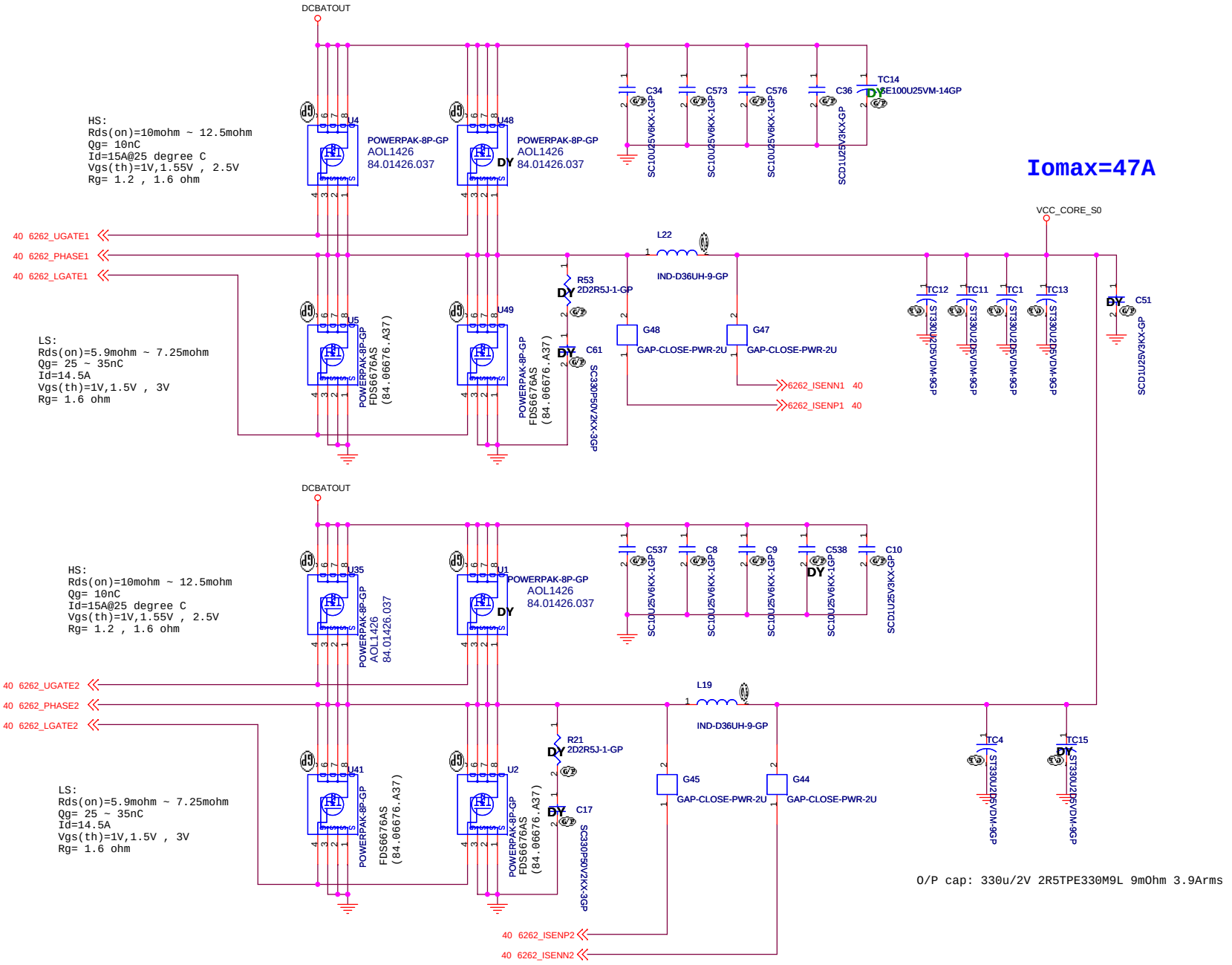
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC-DC VCCCPUCORE 1/2

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Tuesday, May 08, 2007 Sheet 40 of 55



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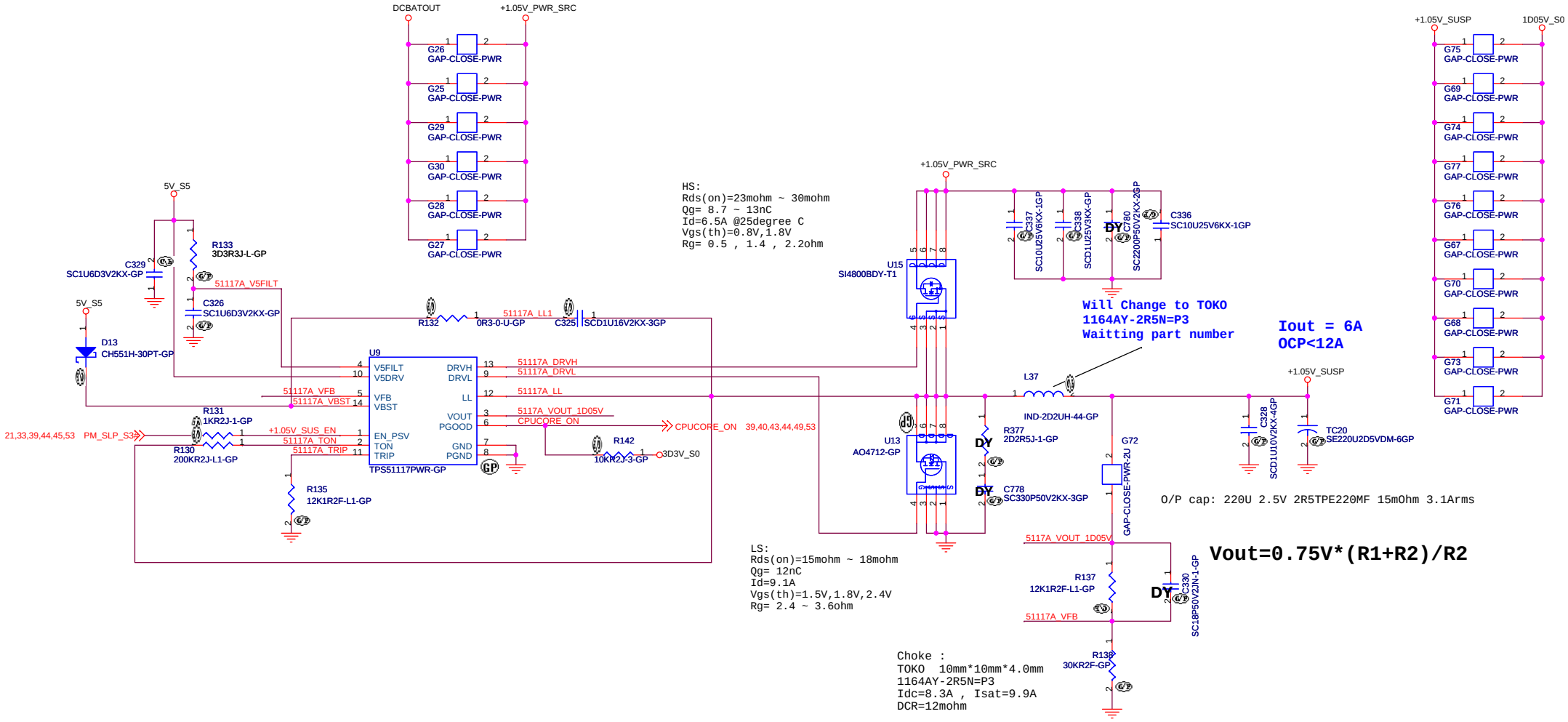
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DC-DC VCCCPUCORE 2/2***

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Tuesday, May 08, 2007 Sheet 41 of 55



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緯創資通 Wistron Corporation
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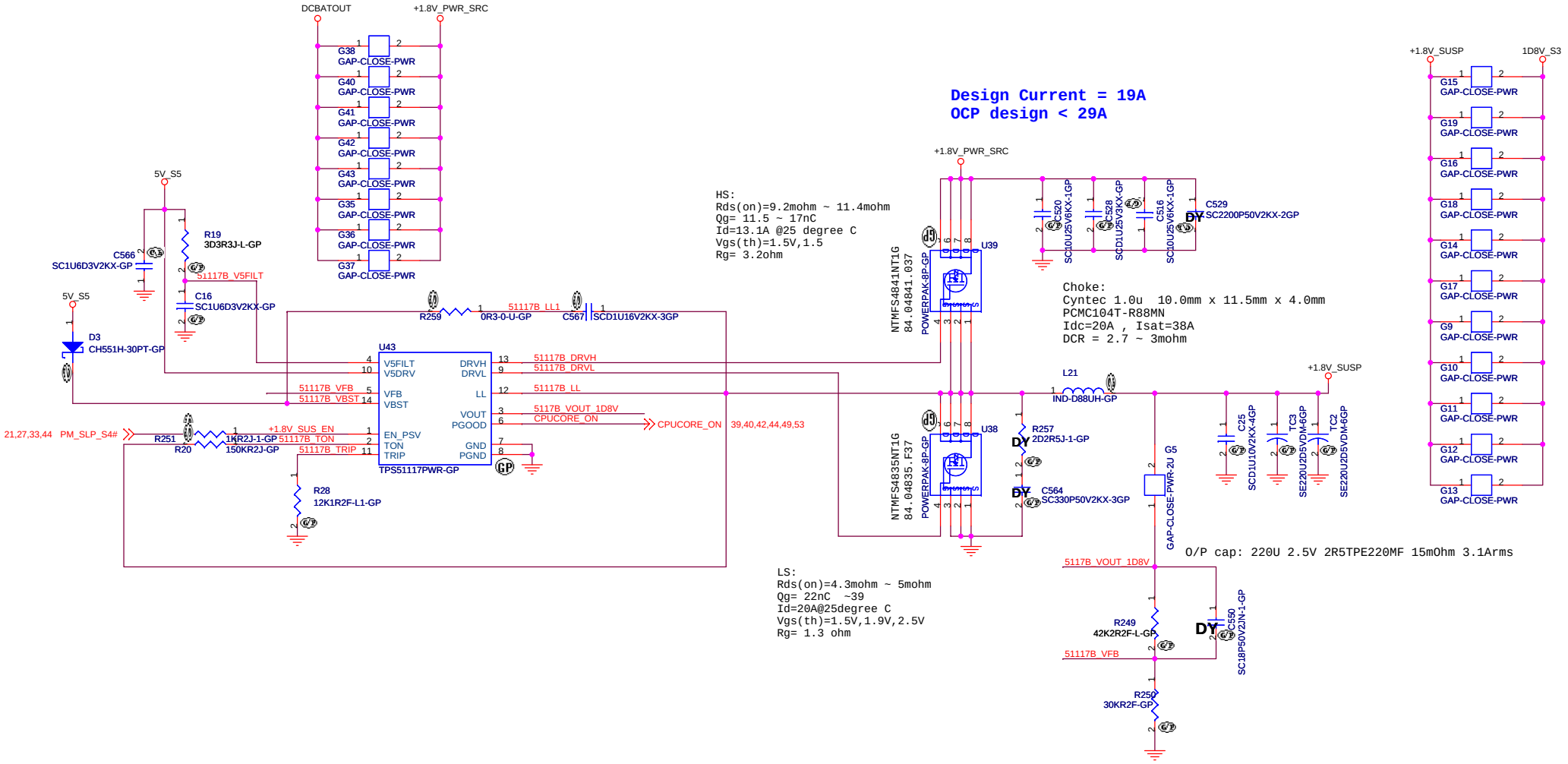
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 1.05V

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Tuesday, May 08, 2007 Sheet 42 of 55



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緯創資通 Wistron Corporation
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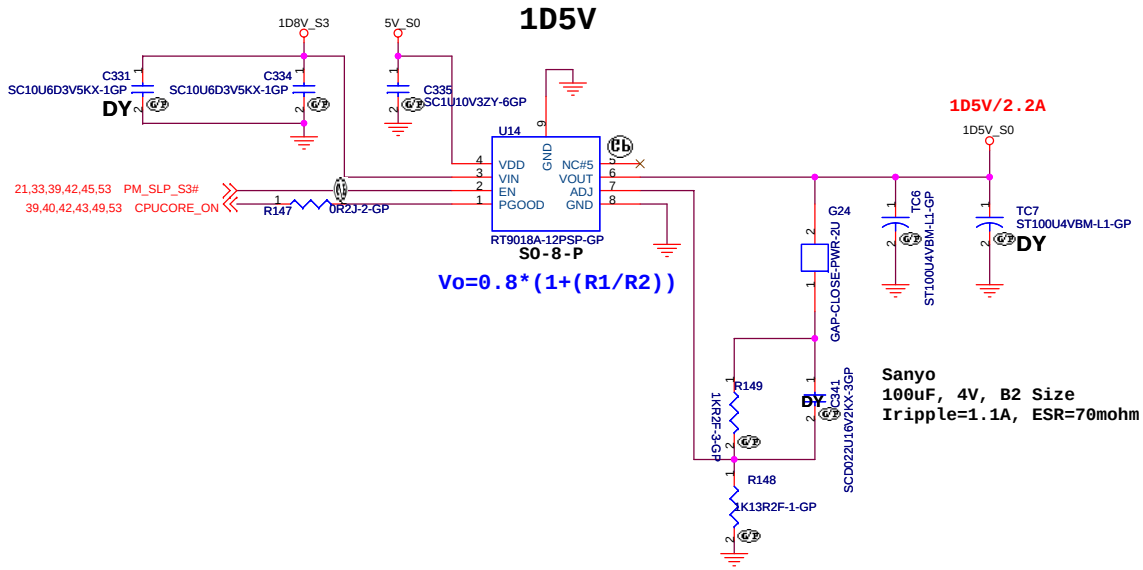
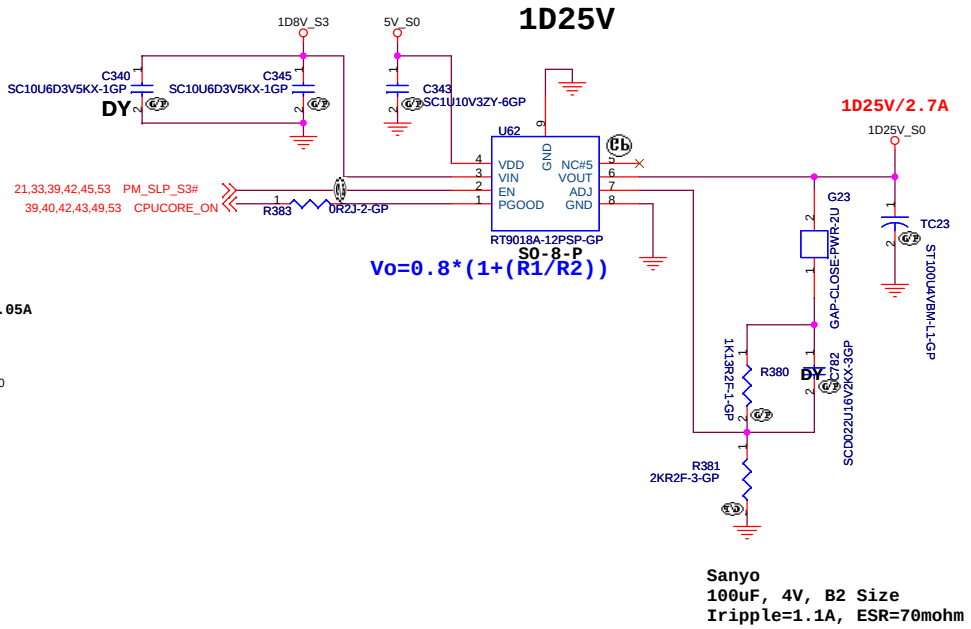
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC 1D8V(ISL6268)

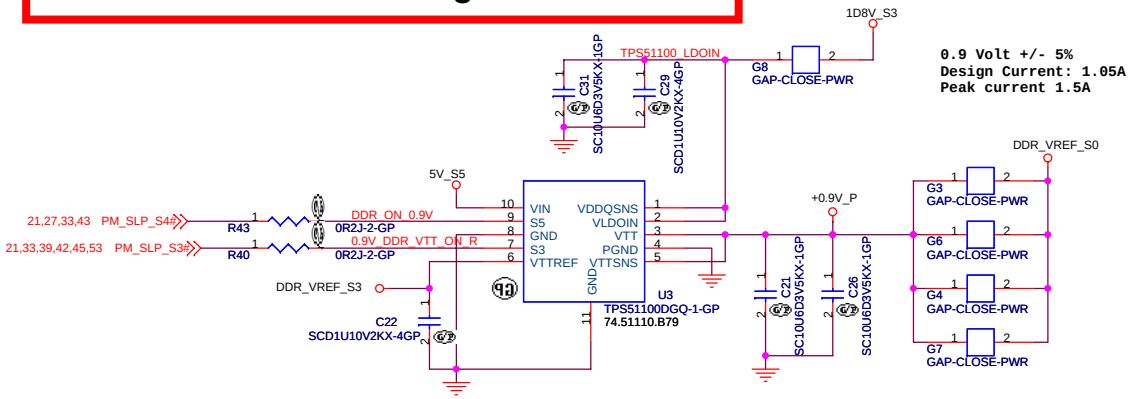
Size: A3 | Document Number: Hawke-Intel | Rev: SA

Date: Tuesday, May 08, 2007 | Sheet 43 of 55





SSID = PWR.Plane.Regulator_0.9V



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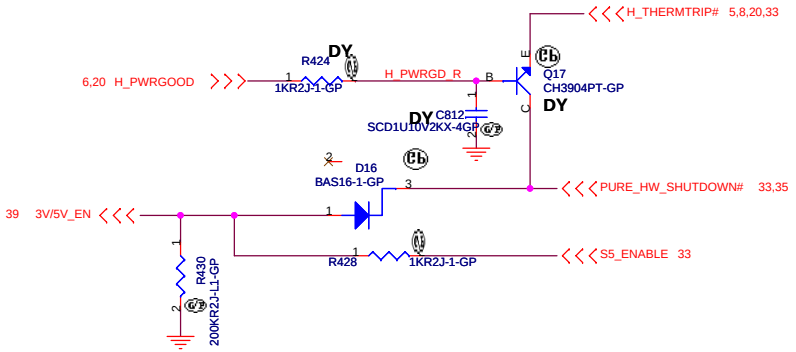
Taipei Hsien 221, Taiwan, R.O.C.

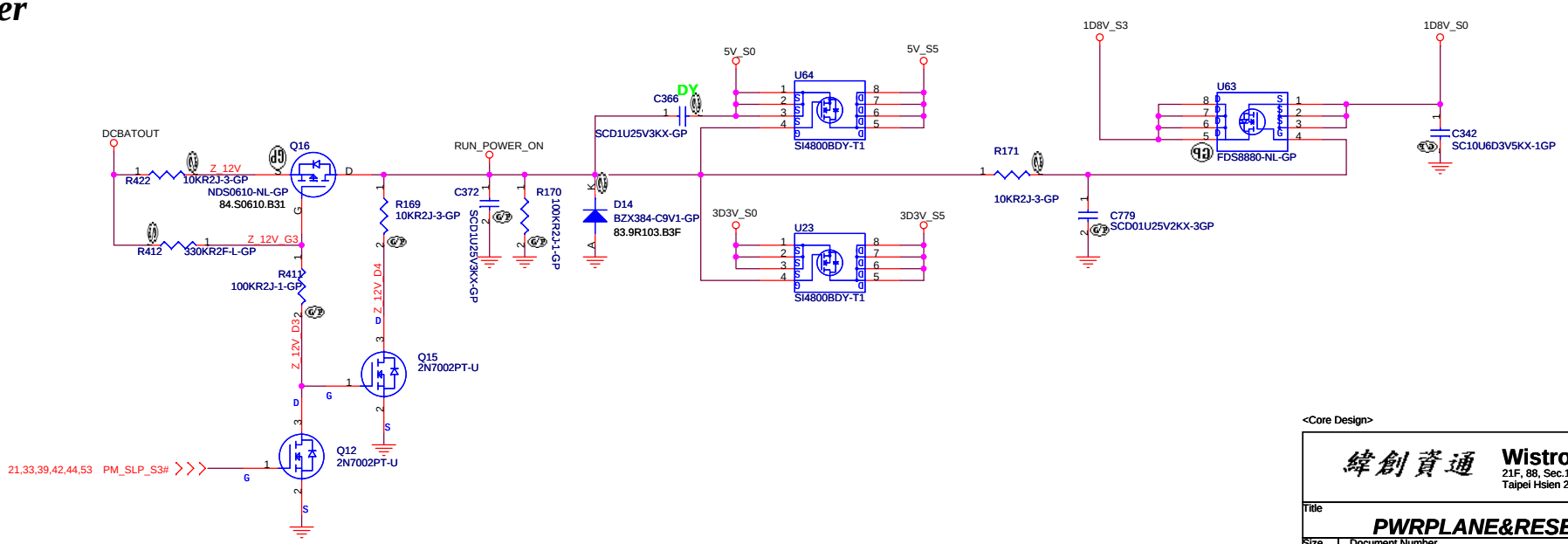
Title: **DC to DC 1D5V / 0D9V /1D25V**

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Tuesday, May 08, 2007 Sheet 44 of 55



Run Power



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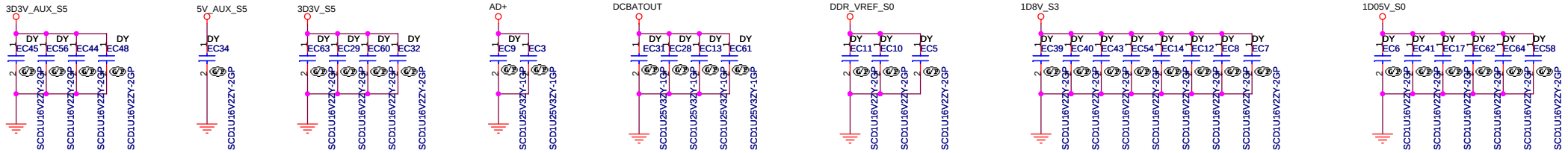
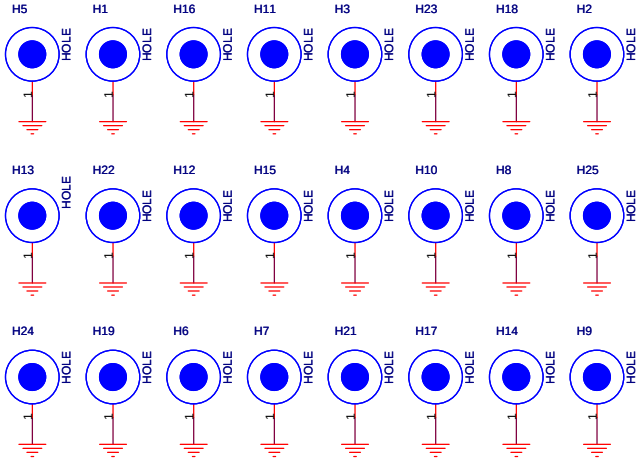
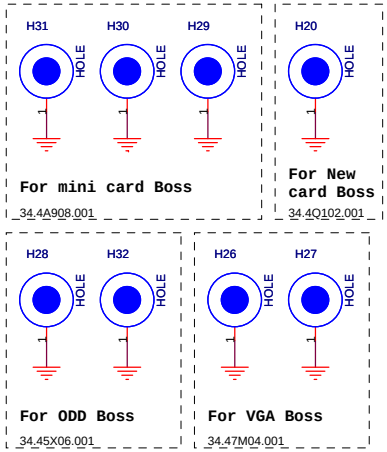
Title: ***PWRPLANE&RESETLOGIC***

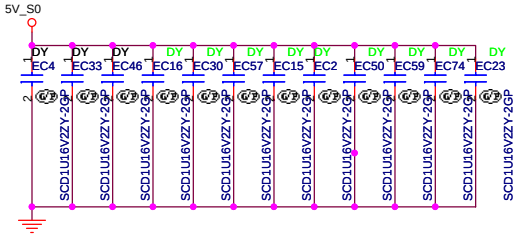
Size	Document Number	Rev
A3	Hawke-Intel	SA

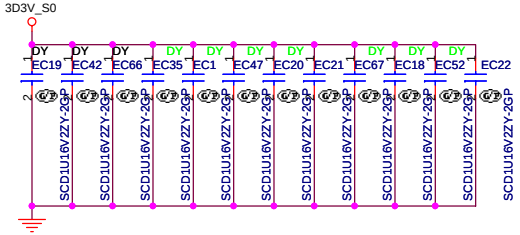
Date: Tuesday, May 08, 2007 Sheet 45 of 55

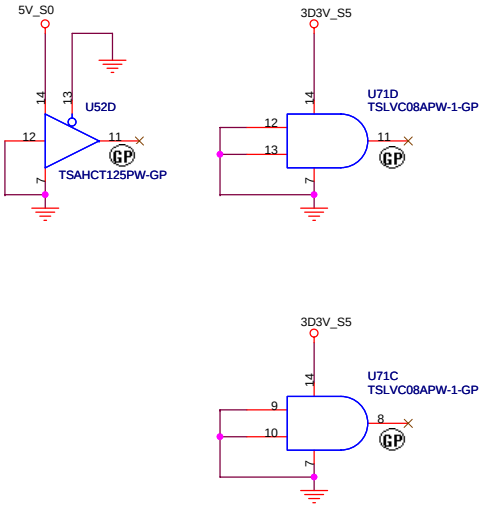


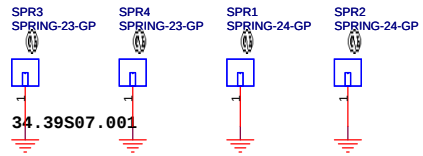












<Core Design>

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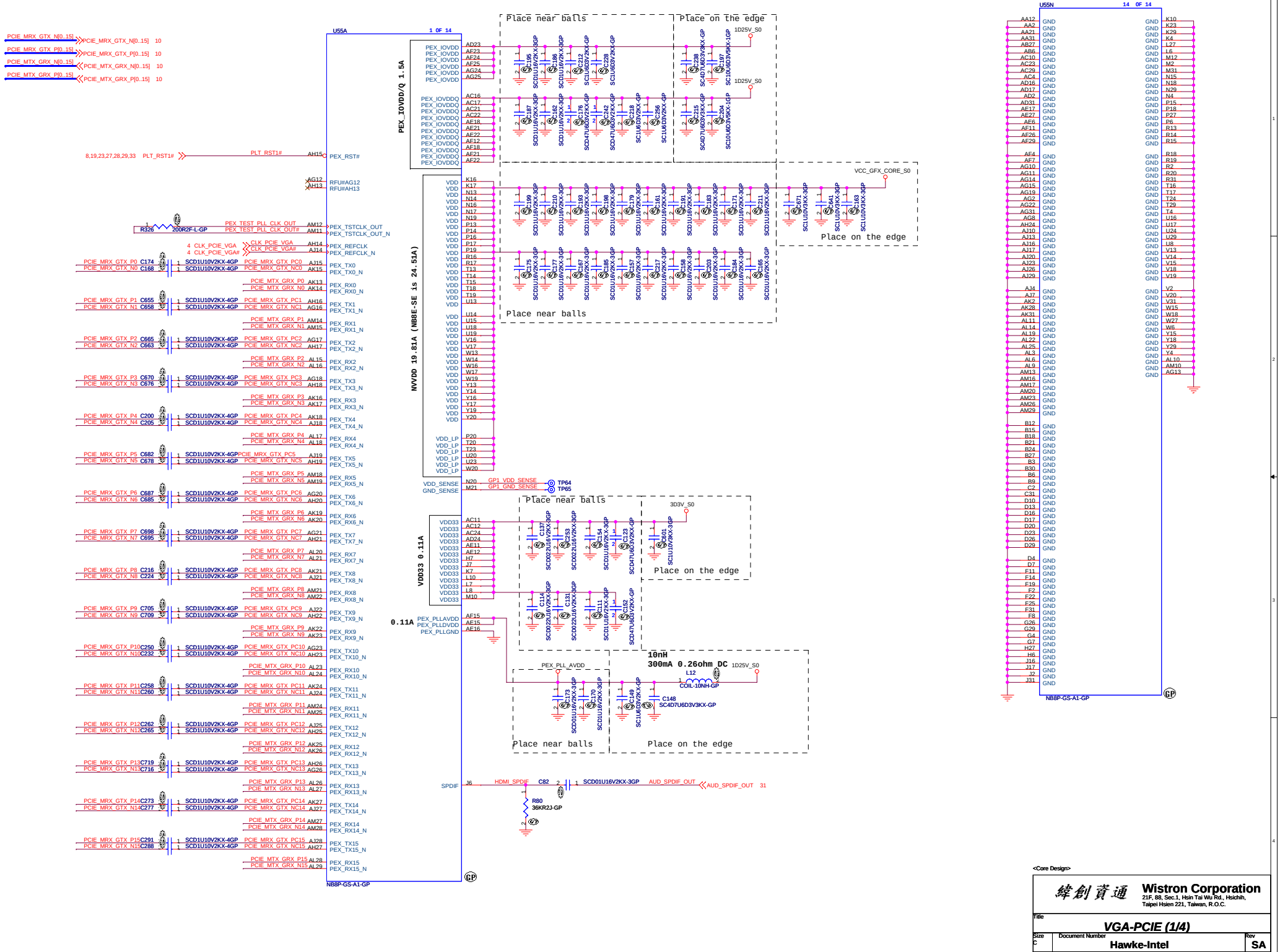
Title: ***MISC***

Size	Document Number	Rev
A3	Hawke-Intel	SA

Date: Tuesday, May 08, 2007 Sheet 46 of 55



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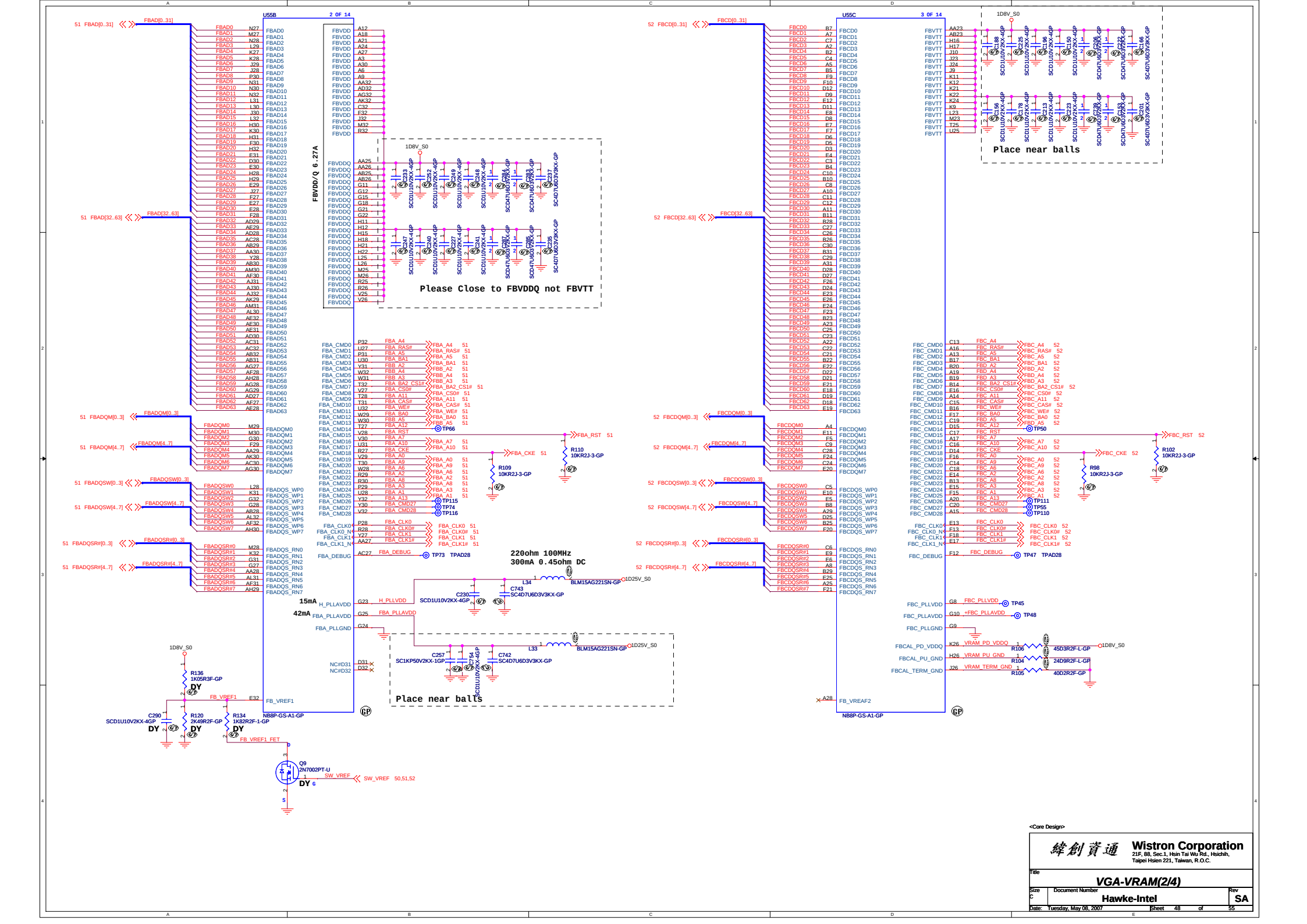
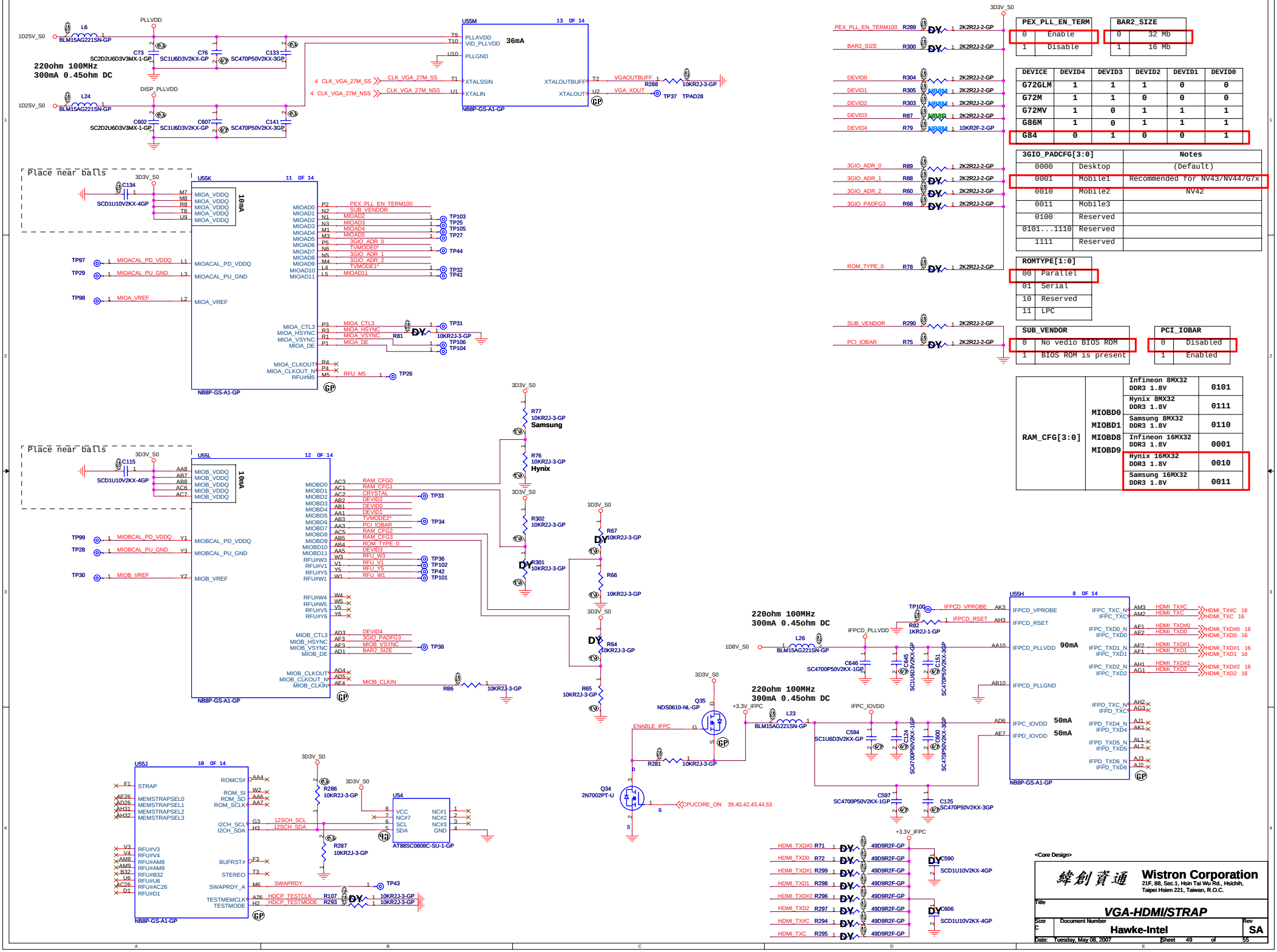
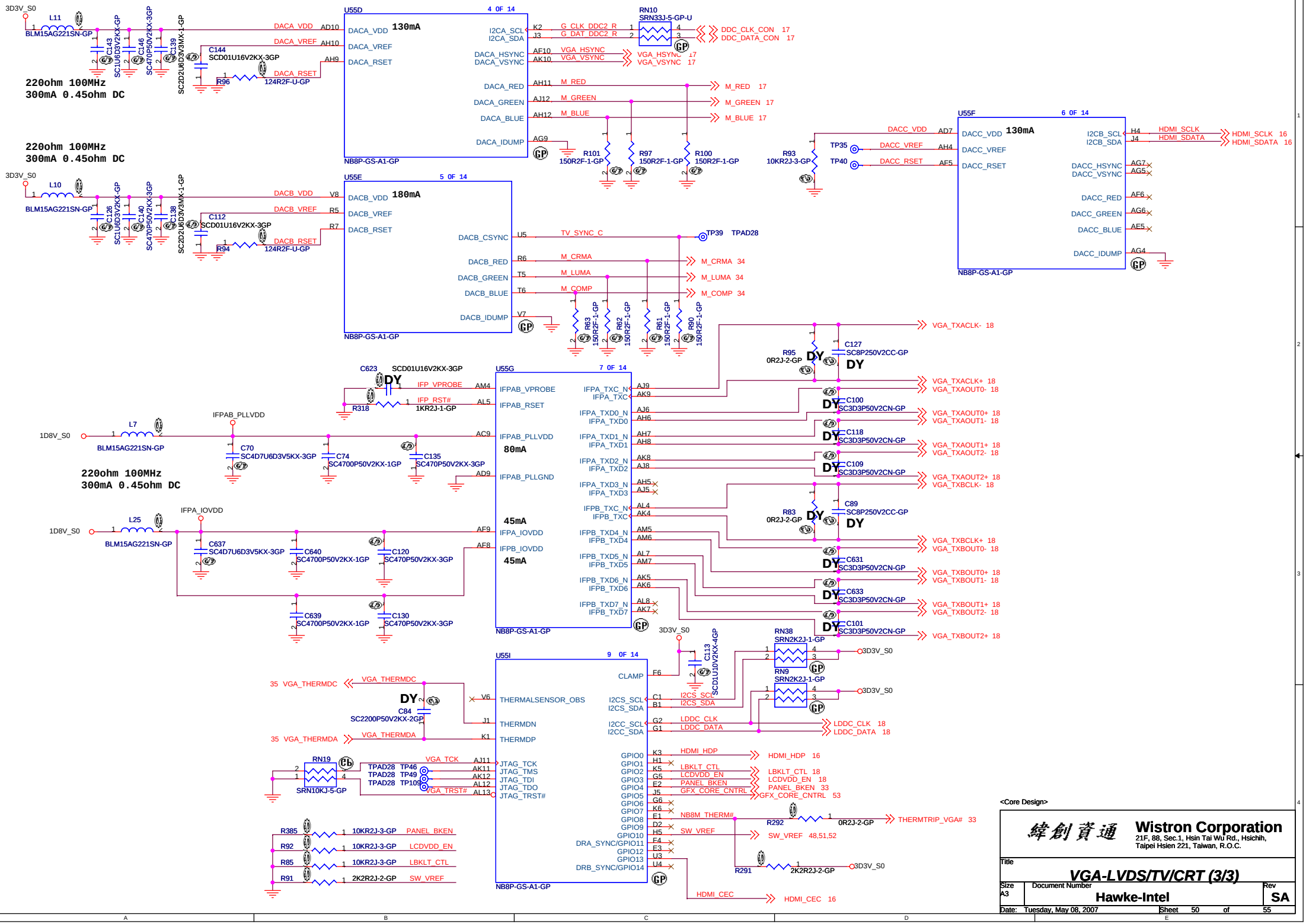
Title: VGA-PCIE (1/4)

Size: C | Document Number: Hawke-Intel | Rev: SA

Date: Tuesday, May 08, 2007 | Sheet 47 of 55


U55B
2 OF 14
FBVDD/Q 6.27A
NB8P-GS-A1-GP
U55C
3 OF 14
NB8P-GS-A1-GP
1D8V_S0
Please Close to FBVDDQ not FBVTT
Place near balls
220ohm 100MHz
300mA 0.45ohm DC
15mA
42mA
Place near balls
Q9
2N7002PT-U
DY
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA-VRAM(2/4)
Size
C
Document Number
Hawke-Intel
Rev
SA
Date: Tuesday, May 08, 2007
Sheet 48 of 55


220ohm 100MHz
300mA 0.45ohm DC
Place near balls
U55M
U55K
U55L
U55H
U55J
NB8P-GS-A1-GP
AT88SC0808C-SU-1-GP
PEX_PLL_EN_TERM
BAR2_SIZE
DEVICE
DEVID4
DEVID3
DEVID2
DEVID1
DEVID0
G72GLM
G72M
G72MV
G86M
G84
3GIO_PADCFG[3:0]
Notes
ROMTYPE[1:0]
SUB_VENDOR
PCI_IOBAR
RAM_CFG[3:0]
MIOBD0
MIOBD1
MIOBD8
MIOBD9
Infineon 8MX32 DDR3 1.8V
Hynix 8MX32 DDR3 1.8V
Samsung 8MX32 DDR3 1.8V
Infineon 16MX32 DDR3 1.8V
Hynix 16MX32 DDR3 1.8V
Samsung 16MX32 DDR3 1.8V
VGA-HDMI/STRAP
Wistron Corporation
Hawke-Intel
SA


3D3V_S0
L11
BLM15AG221SN-GP
C143 SC1U6D3V2KX-GP
C146 SC470P50V2KX-3GP
C139 SC2D2U6D3V3MX-1-GP
C144 SCD01U16V2KX-3GP
R96 124R2F-U-GP
DACA_VDD AD10
DACA_VREF AH10
DACA_RSET AH9
220ohm 100MHz
300mA 0.45ohm DC
U55D
4 OF 14
DACA_VDD 130mA
DACA_VREF
DACA_RSET
I2CA_SCL K2 G_CLK_DDC2_R
I2CA_SDA J3 G_DAT_DDC2_R
DACA_HSYNC AF10 VGA_HSYNC
DACA_VSYNC AK10 VGA_VSYNC
DACA_RED AH11 M_RED
DACA_GREEN AJ12 M_GREEN
DACA_BLUE AH12 M_BLUE
DACA_IDUMP AG9
NB8P-GS-A1-GP
RN10 SRN33J-5-GP-U
DDC_CLK_CON 17
DDC_DATA_CON 17
VGA_HSYNC 17
VGA_VSYNC 17
M_RED 17
M_GREEN 17
M_BLUE 17
R101 150R2F-1-GP
R97 150R2F-1-GP
R100 150R2F-1-GP
3D3V_S0
L10
BLM15AG221SN-GP
C126 SC1U6D3V2KX-GP
C140 SC470P50V2KX-3GP
C138 SC2D2U6D3V3MX-1-GP
C112 SCD01U16V2KX-3GP
R94 124R2F-U-GP
DACB_VDD V8
DACB_VREF R5
DACB_RSET R7
220ohm 100MHz
300mA 0.45ohm DC
U55E
5 OF 14
DACB_VDD 180mA
DACB_VREF
DACB_RSET
DACB_CSYNC U5 TV_SYNC_C
DACB_RED R6 M_CRMA
DACB_GREEN T5 M_LUMA
DACB_BLUE T6 M_COMP
DACB_IDUMP V7
NB8P-GS-A1-GP
TP39 TPAD28
M_CRMA 34
M_LUMA 34
M_COMP 34
R63 150R2F-1-GP
R62 150R2F-1-GP
R61 150R2F-1-GP
R90 150R2F-1-GP
R93 10KR2J-3-GP
TP35
TP40
DACC_VDD AD7
DACC_VREF AH4
DACC_RSET AF5
U55F
6 OF 14
DACC_VDD 130mA
DACC_VREF
DACC_RSET
DACC_HSYNC AG7
DACC_VSYNC AG5
DACC_RED AF6
DACC_GREEN AG6
DACC_BLUE AE5
DACC_IDUMP AG4
NB8P-GS-A1-GP
I2CB_SCL H4 HDMI_SCLK
I2CB_SDA J4 HDMI_SDATA
HDMI_SCLK 16
HDMI_SDATA 16
1D8V_S0
L7
BLM15AG221SN-GP
IFPAB_PLLVDD
C70 SC4D7U6D3V5KX-3GP
C74 SC4700P50V2KX-1GP
C135 SC470P50V2KX-3GP
AC9
AD9
220ohm 100MHz
300mA 0.45ohm DC
C623 SCD01U16V2KX-3GP
DY
IFP_VPROBE AM4
IFP_RST# AL5
R318 1KR2J-1-GP
U55G
7 OF 14
IFPAB_VPROBE
IFPAB_RSET
IFPAB_PLLVDD 80mA
IFPAB_PLLGND
IFPA_IOVDD 45mA
IFPB_IOVDD 45mA
NB8P-GS-A1-GP
IFPA_TXC_N AJ9
IFPA_TXC AK9
IFPA_TXD0_N AJ6
IFPA_TXD0 AH6
IFPA_TXD1_N AH7
IFPA_TXD1 AH8
IFPA_TXD2_N AK8
IFPA_TXD2 AJ8
IFPA_TXD3_N AH5
IFPA_TXD3 AJ5
IFPB_TXC_N AL4
IFPB_TXC AK4
IFPB_TXD4_N AM5
IFPB_TXD4 AM6
IFPB_TXD5_N AL7
IFPB_TXD5 AM7
IFPB_TXD6_N AK5
IFPB_TXD6 AK6
IFPB_TXD7_N AL8
IFPB_TXD7 AK7
R95 0R2J-2-GP
C127 SC8P250V2CC-GP
C100 SC3D3P50V2CN-GP
C118 SC3D3P50V2CN-GP
C109 SC3D3P50V2CN-GP
R83 0R2J-2-GP
C89 SC8P250V2CC-GP
C631 SC3D3P50V2CN-GP
C633 SC3D3P50V2CN-GP
C101 SC3D3P50V2CN-GP
VGA_TXACLK- 18
VGA_TXACLK+ 18
VGA_TXAOUT0- 18
VGA_TXAOUT0+ 18
VGA_TXAOUT1- 18
VGA_TXAOUT1+ 18
VGA_TXAOUT2- 18
VGA_TXAOUT2+ 18
VGA_TXBCLK- 18
VGA_TXBCLK+ 18
VGA_TXBOUT0- 18
VGA_TXBOUT0+ 18
VGA_TXBOUT1- 18
VGA_TXBOUT1+ 18
VGA_TXBOUT2- 18
VGA_TXBOUT2+ 18
IFPA_IOVDD
L25
BLM15AG221SN-GP
C637 SC4D7U6D3V5KX-3GP
C640 SC4700P50V2KX-1GP
C120 SC470P50V2KX-3GP
C639 SC4700P50V2KX-1GP
C130 SC470P50V2KX-3GP
3D3V_S0
C113 SCD1U10V2KX-4GP
RN38 SRN2K2J-1-GP
RN9 SRN2K2J-1-GP
U55I
9 OF 14
CLAMP F6
THERMALSENSOR_OBS V6
THERMDN J1
THERMDP K1
I2CS_SCL C1 I2CS_SCL
I2CS_SDA B1 I2CS_SDA
I2CC_SCL G2 LDDC_CLK
I2CC_SDA G1 LDDC_DATA
GPIO0 K3 HDMI_HDP
GPIO1 H1
GPIO2 K5 LBKLT_CTL
GPIO3 G5 LCDVDD_EN
GPIO4 E2 PANEL_BKEN
GPIO5 J5 GFX_CORE_CNTRL
GPIO6 G6
GPIO7 K6
GPIO8 E1 NB8M_THERM#
GPIO9 D2
GPIO10 H5 SW_VREF
DRA_SYNC/GPIO11 F4
GPIO12 E3
GPIO13 U3
DRB_SYNC/GPIO14 U4
JTAG_TCK AJ11
JTAG_TMS AK11
JTAG_TDI AK12
JTAG_TDO AL12
JTAG_TRST# AL13
NB8P-GS-A1-GP
HDMI_HDP 16
LBKLT_CTL 18
LCDVDD_EN 18
PANEL_BKEN 33
GFX_CORE_CNTRL 53
HDMI_CEC 16
35 VGA_THERMDC
VGA_THERMDC
C84 SC2200P50V2KX-2GP
35 VGA_THERMDA
VGA_THERMDA
RN19 SRN10KJ-5-GP
VGA_TCK
TPAD28 TP46
TPAD28 TP49
TPAD28 TP109
VGA_TRST#
LDDC_CLK 18
LDDC_DATA 18
R292 0R2J-2-GP
THERMTRIP_VGA# 33
R291 2K2R2J-2-GP
SW_VREF 48,51,52
R385 10KR2J-3-GP PANEL_BKEN
R92 10KR2J-3-GP LCDVDD_EN
R85 10KR2J-3-GP LBKLT_CTL
R91 2K2R2J-2-GP SW_VREF
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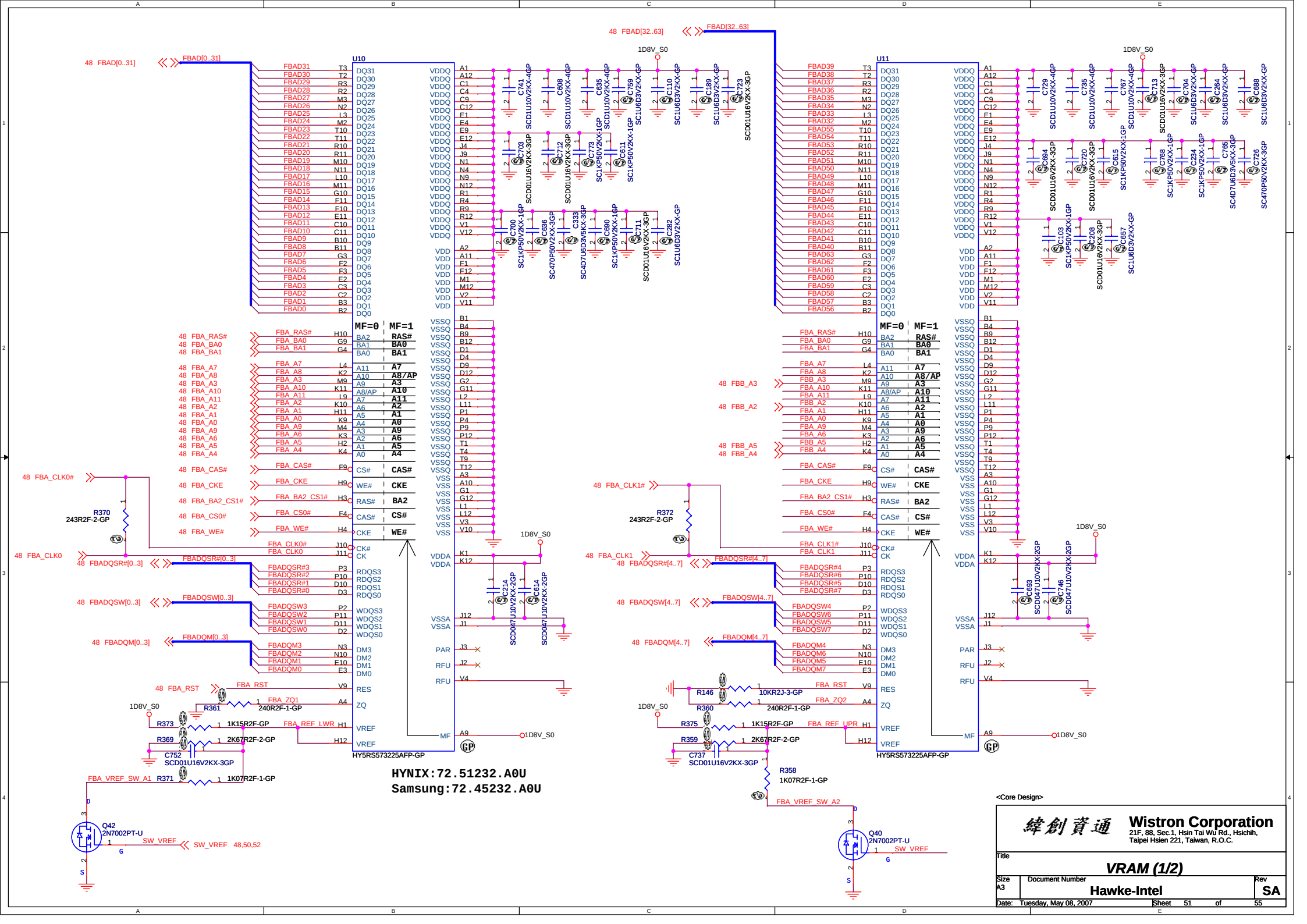
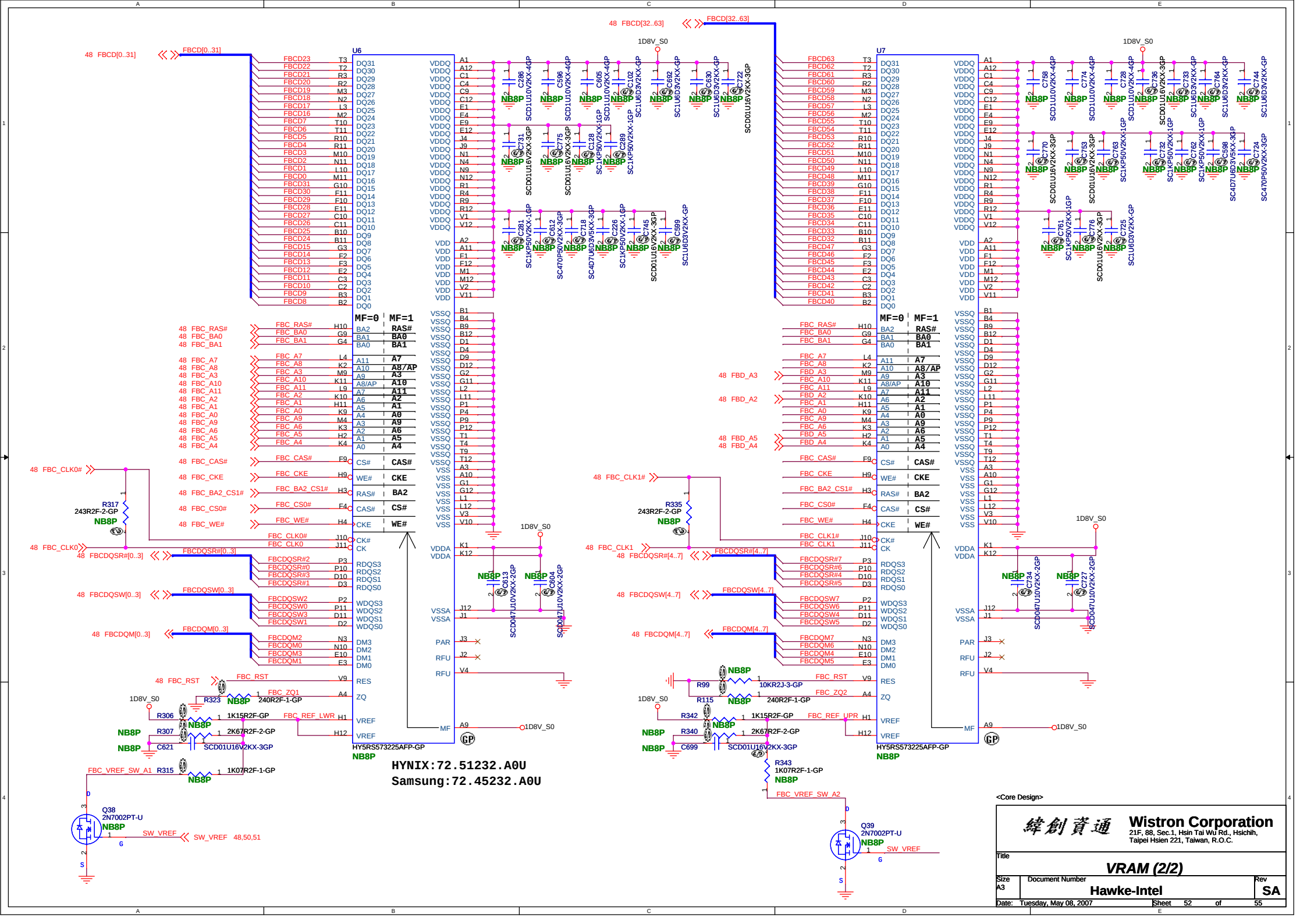
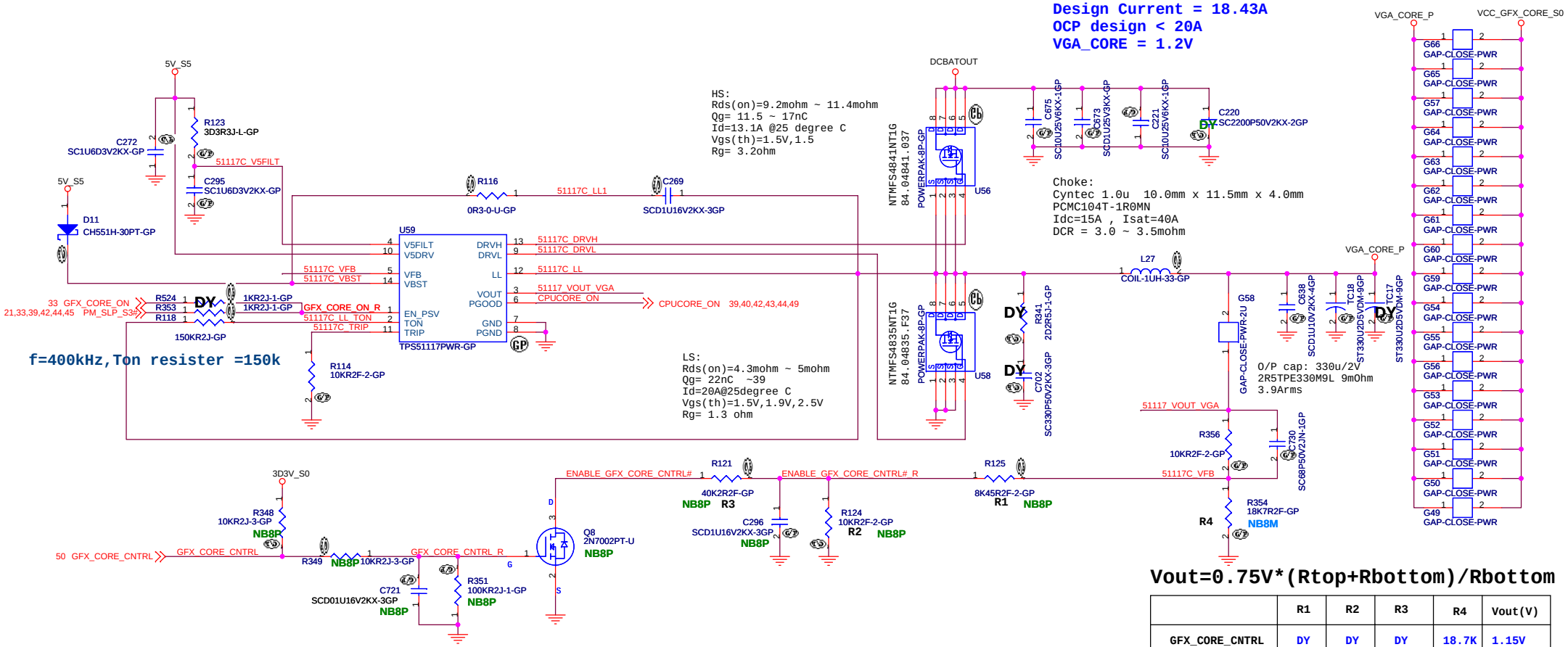
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA-LVDS/TV/CRT (3/3)
Size A3
Document Number Hawke-Intel
Rev SA
Date: Tuesday, May 08, 2007
Sheet 50 of 55


U10
U11
MF=0 MF=1
RAS# BA0 BA1 A7 A8/AP A3 A10 A11 A2 A1 A0 A9 A6 A5 A4 CAS# CKE BA2 CS# WE#
HY5RS573225AFP-GP
HYNIX:72.51232.A0U
Samsung:72.45232.A0U
Q42 2N7002PT-U
Q40 2N7002PT-U
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM (1/2)
Size A3
Document Number Hawke-Intel
Rev SA
Date: Tuesday, May 08, 2007
Sheet 51 of 55


U6
U7
HY5RS573225AFP-GP
MF=0
MF=1
HYNIX:72.51232.A0U
Samsung:72.45232.A0U
Q38
2N7002PT-U
Q39
2N7002PT-U
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM (2/2)
Size
A3
Document Number
Hawke-Intel
Rev
SA
Date: Tuesday, May 08, 2007
Sheet 52 of 55



	R1	R2	R3	R4	Vout(V)
GFX_CORE_CNTRL NA	DY	DY	DY	18.7K	1.15V
GFX_CORE_CNTRL Low	8.45K	10K	40.2K to FET	DY	1.15V
GFX_CORE_CNTRL High	8.45K	10K	40.2K to GND	DY	1.2V

<Core Design>

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Title: DCDC VGA_Core

Size: A3 | Document Number: Hawke-Intel | Rev: SA

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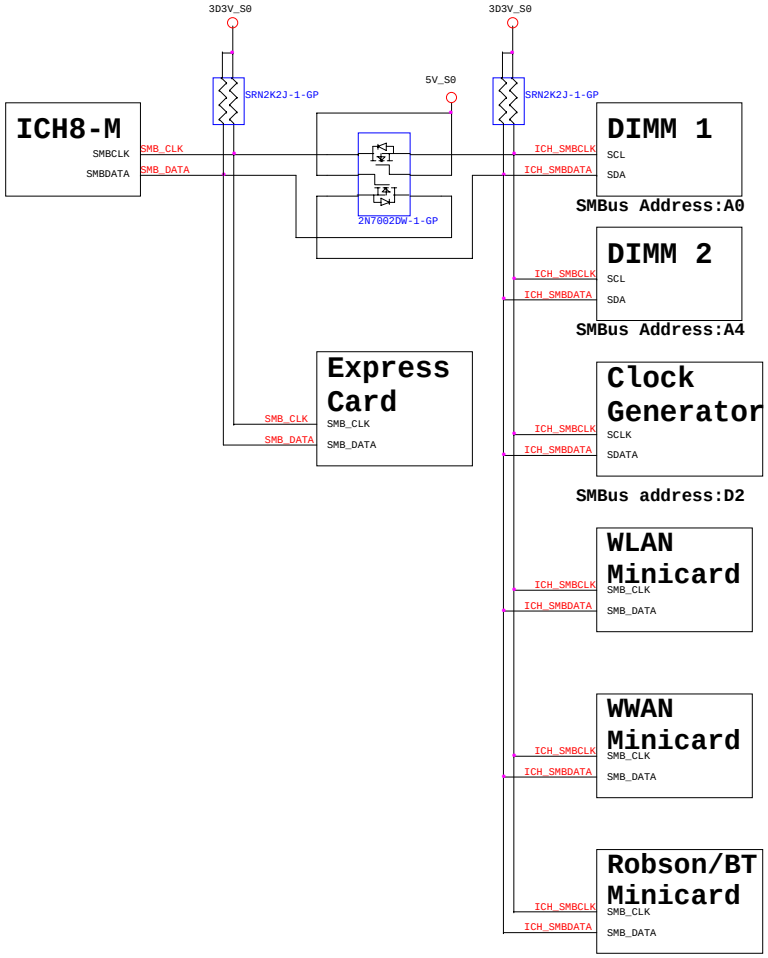
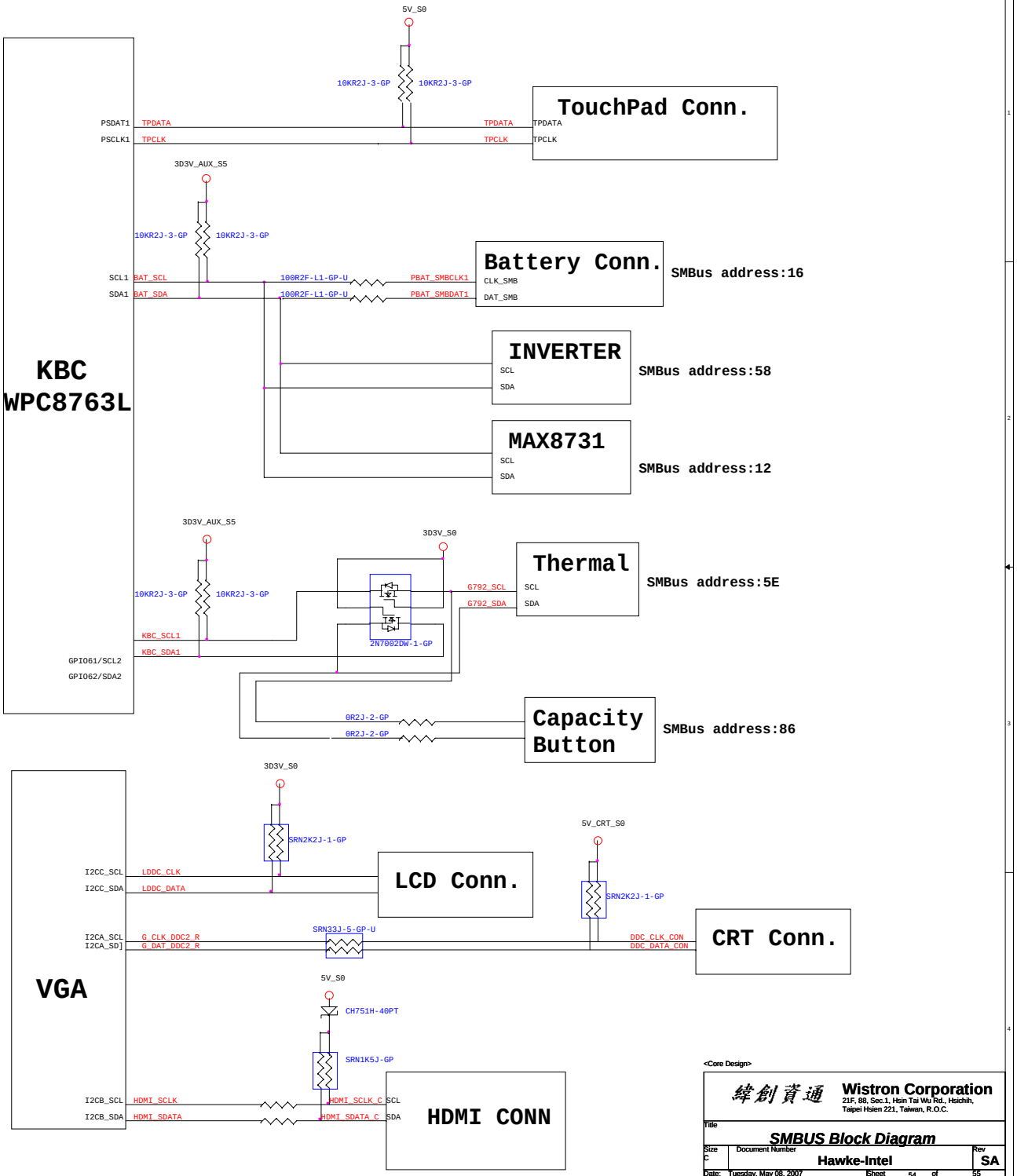
ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

Size	Document Number	Rev
C	Hawke-Intel	SA

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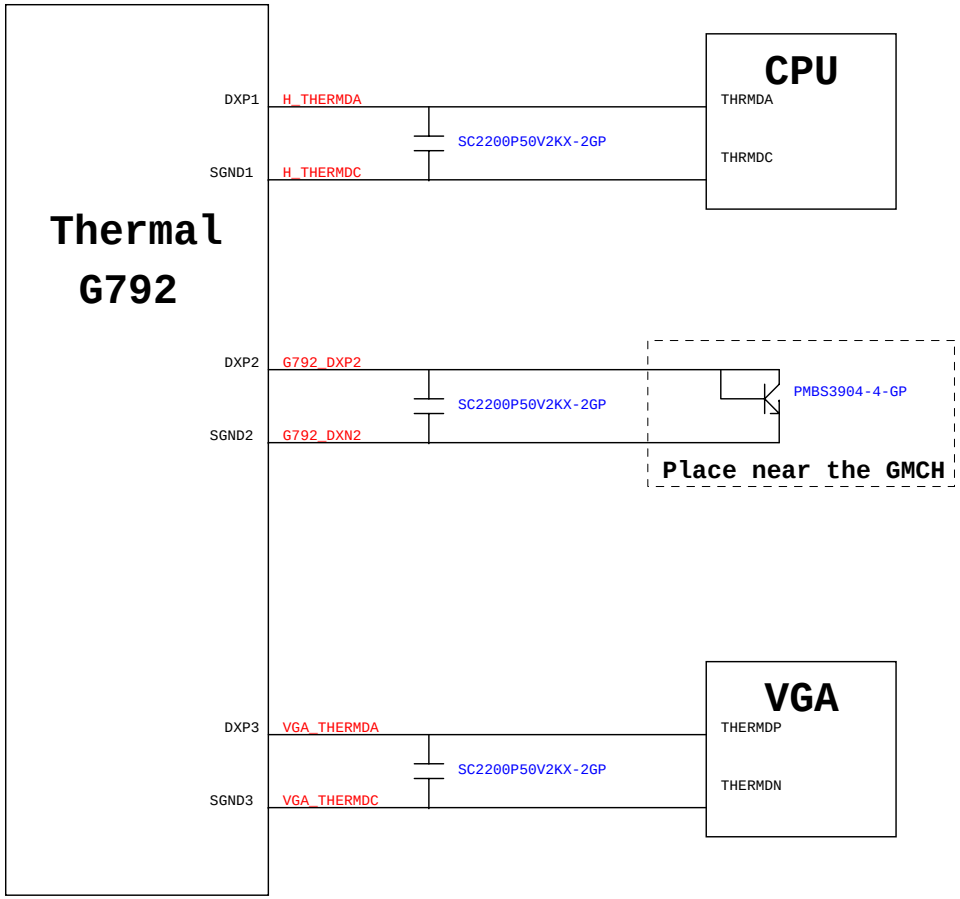
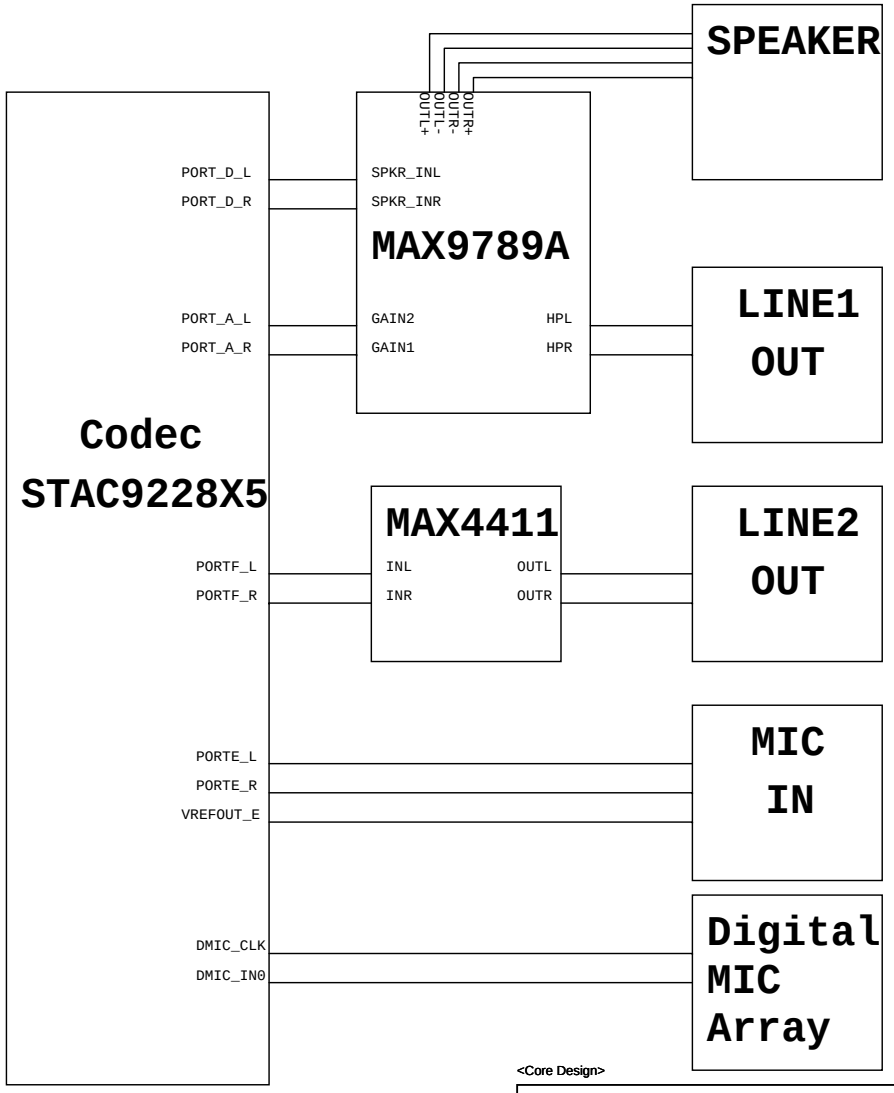
Thermal Block Diagram



Audio Block Diagram



<Core Design>

緯創資通 Wistron Corporation
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