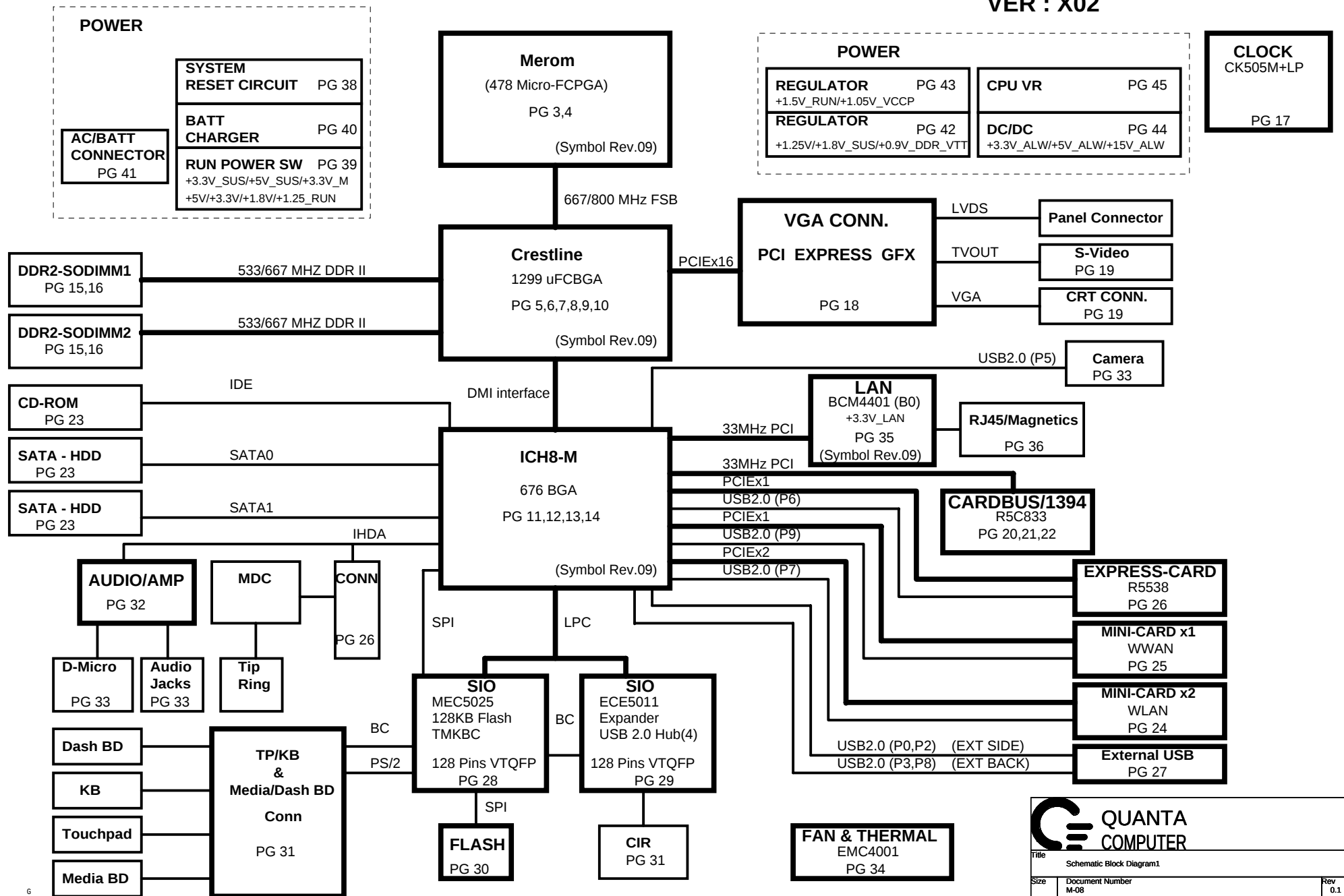


Corsica\Gilligan - DISCRETE

VER : X02

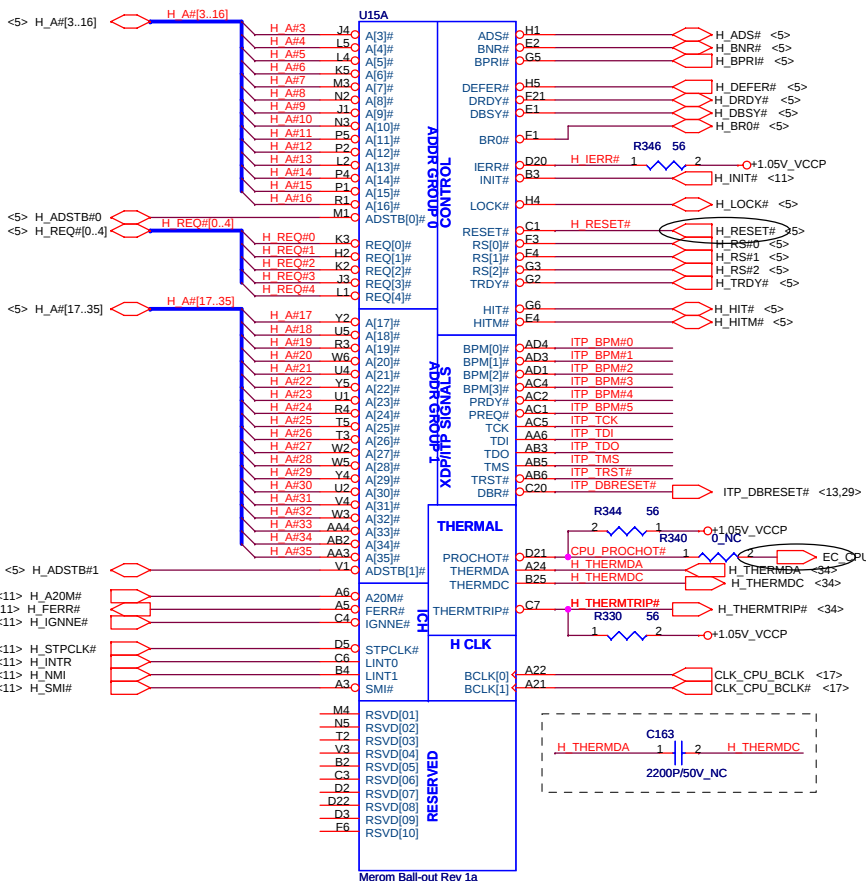


Title Schematic Block Diagram.1		
Size Document Number M-08	Rev 0.1	
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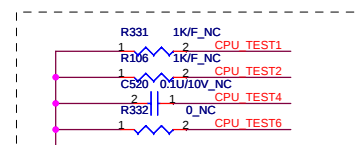
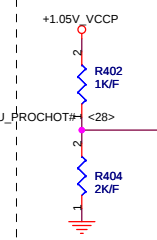
INDEX		
Pg#	Description	DNI LIST
1	Schematic Block Diagram	
2	Front Page	
3-4	Merom	
5-10	Crestline	
11-14	ICH8M	
15-16	DDRII SO-DIMM(200P)	
17	Clock Generator	
18-21	VGA	
22	LCD Conn. & SSP	
23	CRT Conn	
24	SATA & IDE Conn	
25	PCCARD/Conn & 1394	
26	Express Card & Smart Card	
27	Mini Card	
28	MDC Conn.	
29	SIO (MEC5004)	
30	SIO (MEC5018)	
31	SERIAL PORT & USB	
32	Flash ROM	
33	TP,BT & FIR	
34	Switch,Keyboard & LED	
35	FAN & Thermal	
36-37	Audio CODEC(STAC9200)/Phone Jack	
38-39	LOM (BCM5752)/Switch	
40-41	Docking Conn/Q-Switch	
42	System Reset Circuit	
43-44	Battery Selector & Charger	
45	DDR2_1.8VSUS, 0.9V	
46	1.5VSUS,1.05V(VTT)	
47	1.25V,1.05VM	
48	CPU_MAX8786(3phase)	
49	D/D Power	
50	RUN Power Switch	
51	VGA DC/DC	
52	DCIN/Batt Conn.	
53	PAD& SCREW	
54	EMI CAP	

Power & Ground			
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (19V)	
PBATT+		MAIN BATTERY + (10~17V)	
PBATT+		SECOND BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~19V)	
RTC_PWR3_3V		RTC & +3.3V_RTC_LDO(3.3V)	
+VCC_CORE		CPU CORE POWER (1.5V)	RUNPWROK
+15V_ALW		LARGE POWER (15V)	SUS_ON
+3.3V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+3.3V_SUS		SLP_S5# CTRLD POWER	SUS_ENABLE
+3.3V_ALW		8051 POWER (3.3V)	ALWON/THERM_STP#
+5V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+5V_SUS		SLP_S5# CTRLD POWER	SUS_ON
+5V_HDD		HDD POWER (5V)	+5V_RUN
+5V_MOD		MODULE POWER (5V)	HDDC_EN
+5V_ALW		LCD/CHARGE POWER (5V)	
+VDDA		AUDIO ANALOG POWER (5V)	AUDIO_AVDD_ON
+1.5V_RUN		CALISTOGA/ICH7 POWER	RUN_ON
+1.05V_VCCP		CPU/CALISTOGA/ICH7 POWER	RUN_ON
+1_8V_SUS		SODIMM POWER	SUSPWROK_5V
+1.8V_RUN		SDVO POWER	RUN_ON
+0.9V_DDR_VTT		SODIMM POWER	RUN_ON
+3.3V_LAN		LAN POWER	AUX_EN
 GND	ALL PAGES	DIGITAL GROUND	
 AGND_JSL6260		CPU GND	
 AGND_TPS51120		DC/DC POWER GND	
 AGND1		VTT POWER GND	
 AGND2		VTT POWER GND	
 8731AGND		CHARGER GND	

 QUANTA COMPUTER		
Title Index, DNI, Power & Ground		
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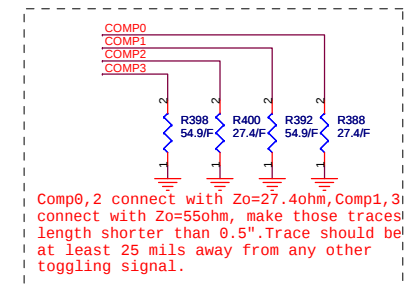


Layout Note:
Place voltage divider within 0.5" of GTLREF pin

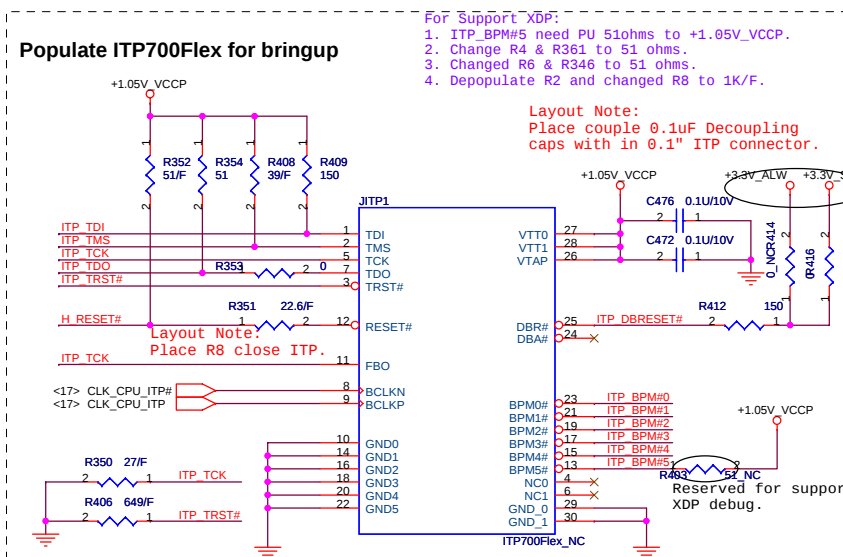


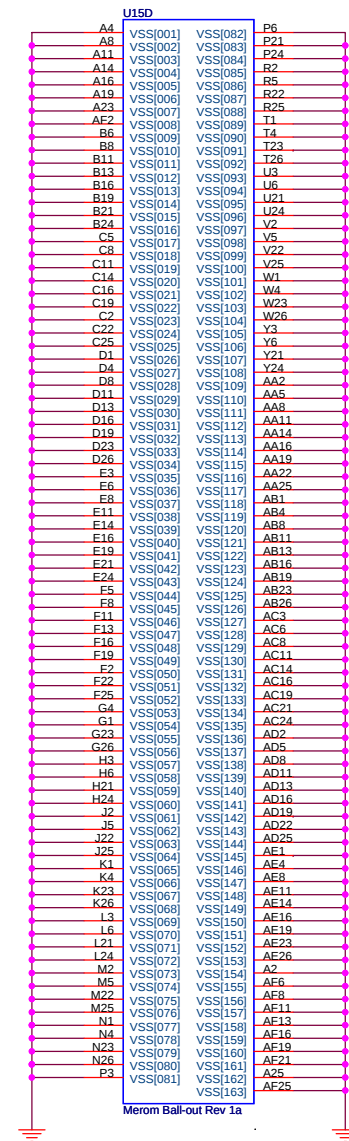
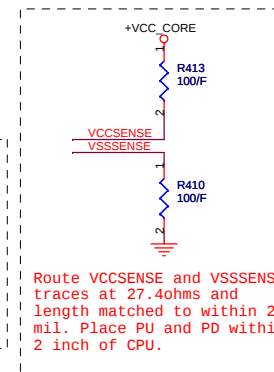
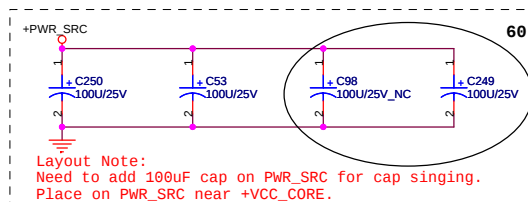
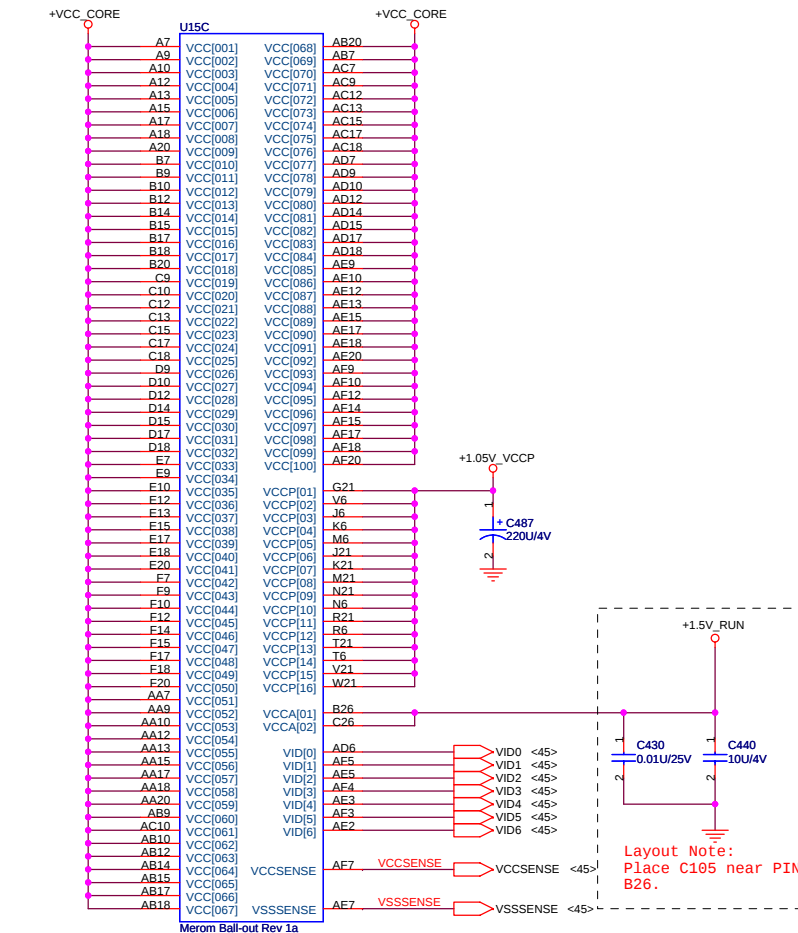
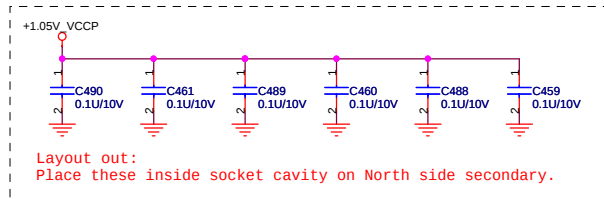
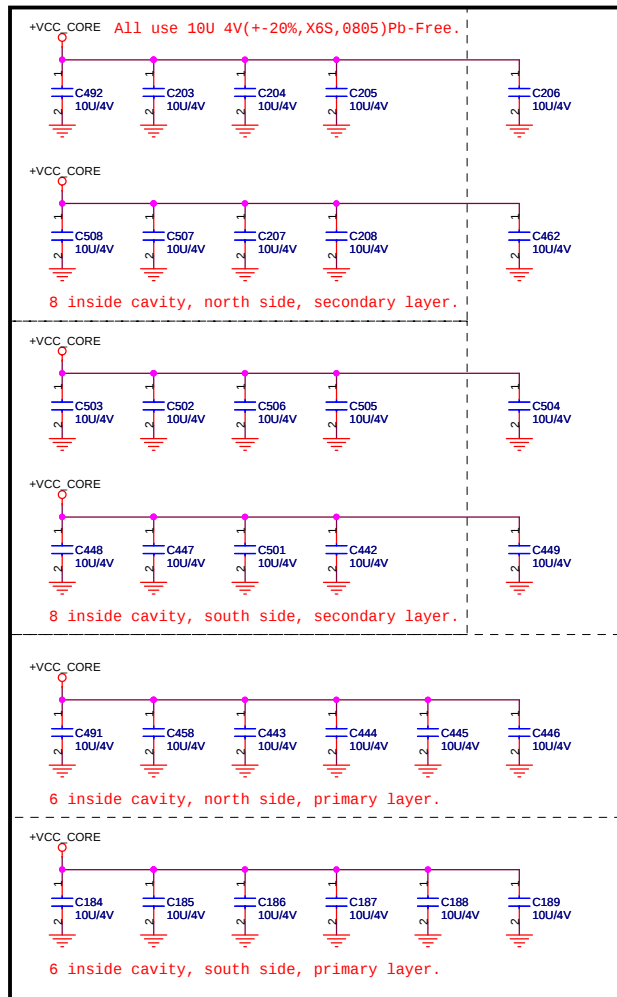
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

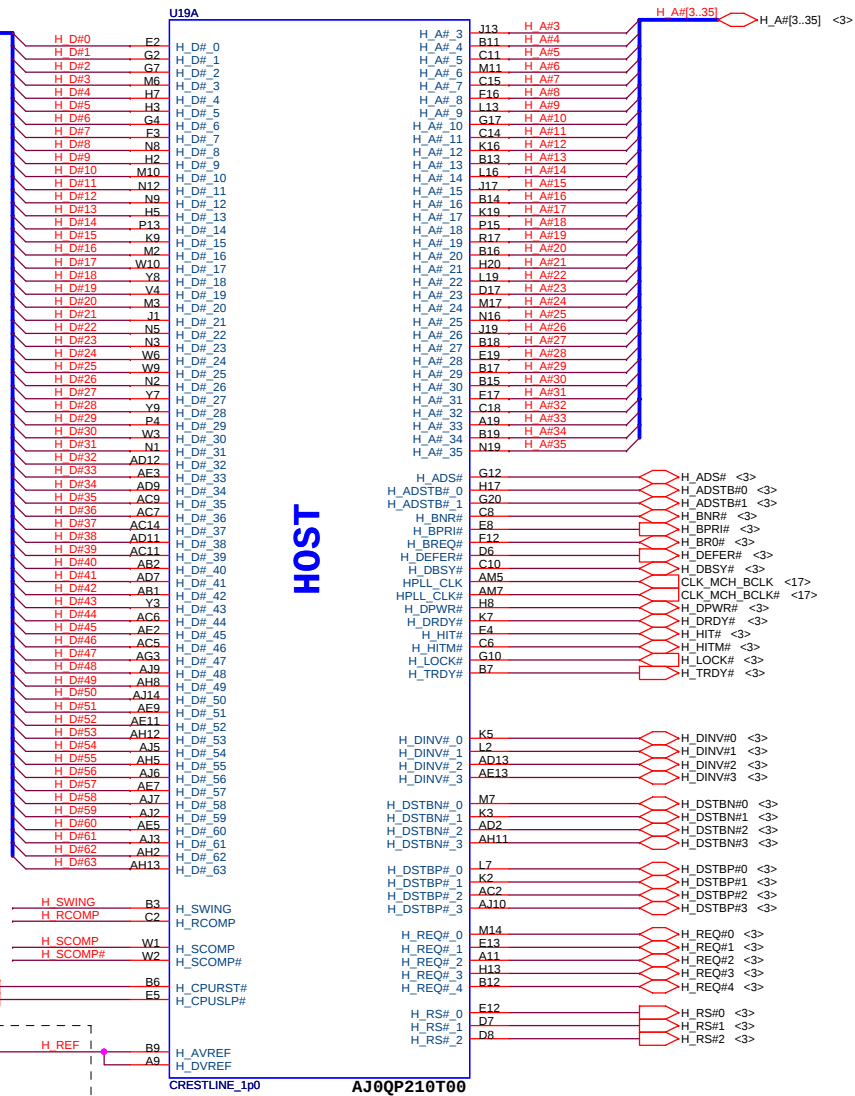
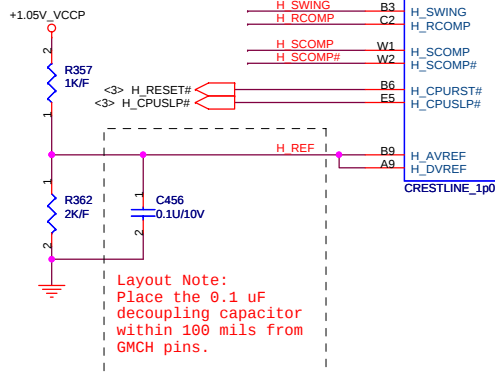
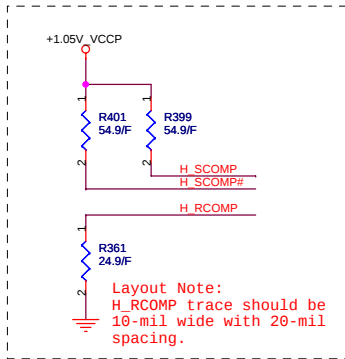
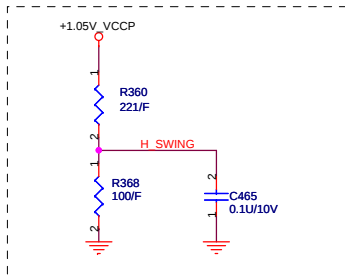


Comp0,2 connect with Z0=27.4ohm, Comp1,3 connect with Z0=55ohm, make those traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.



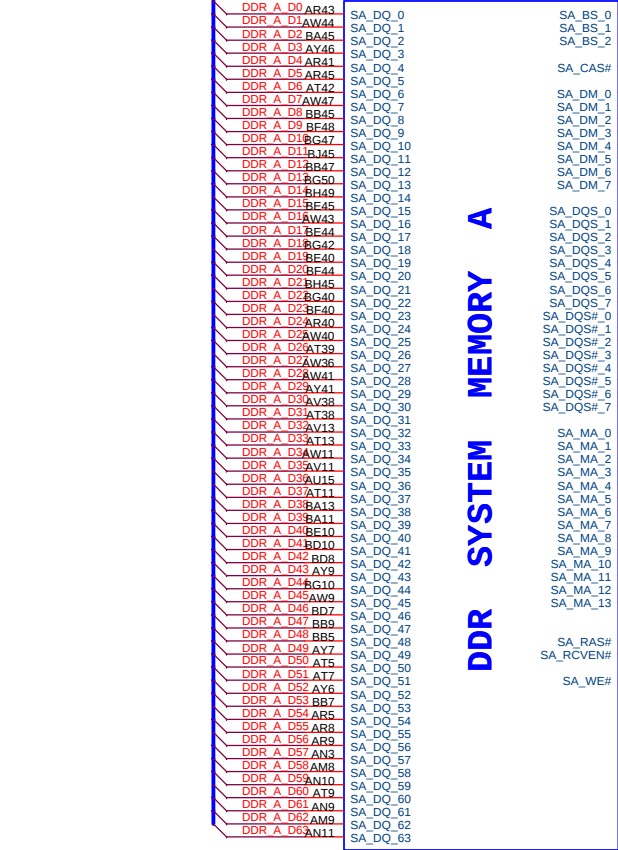


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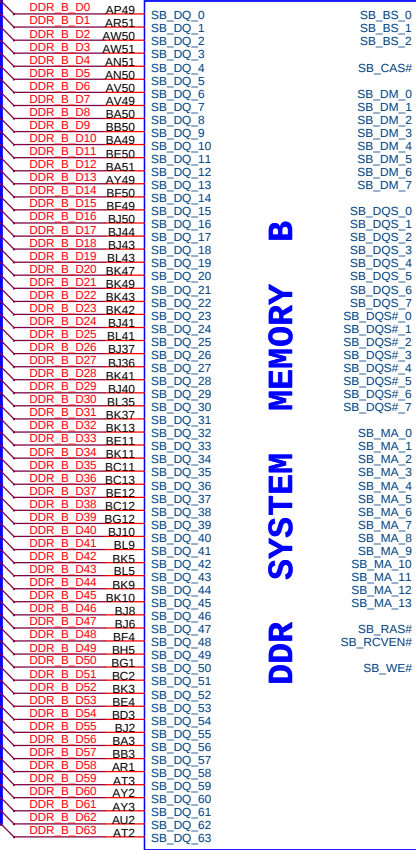
<15> DDR_A_D[0..63]



CRESTLINE_ip0

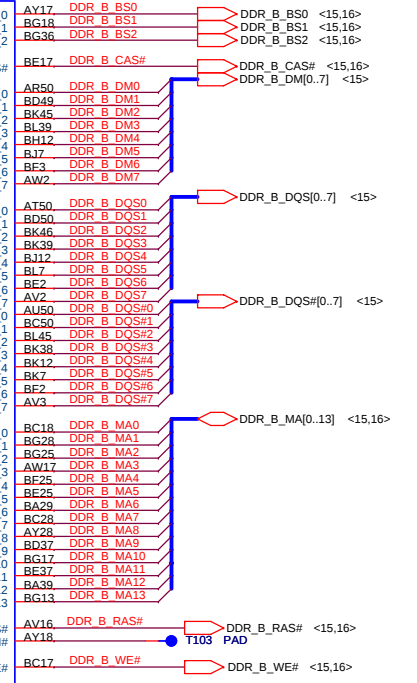
DDR SYSTEM MEMORY A

<15> DDR_B_D[0..63]

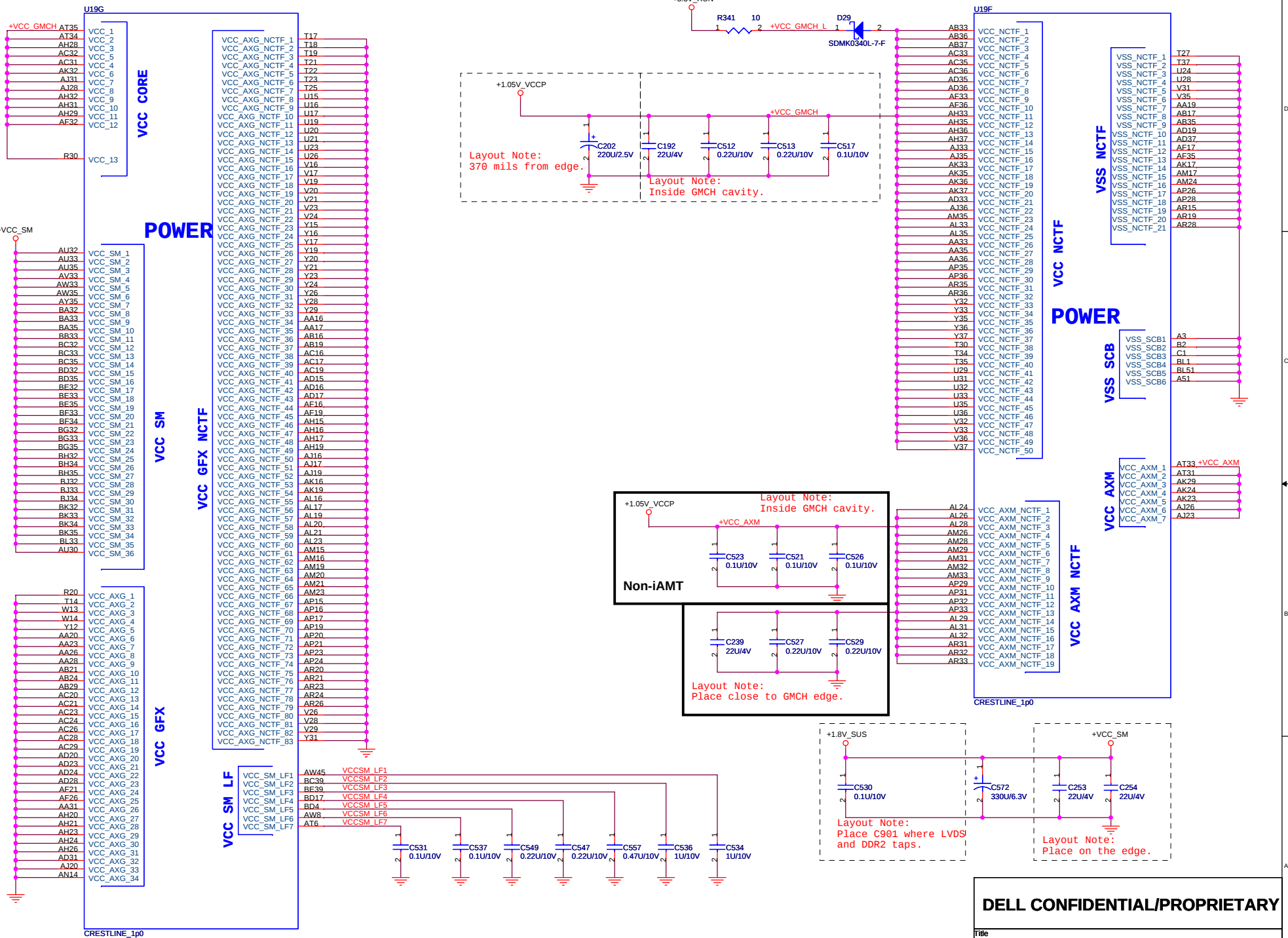


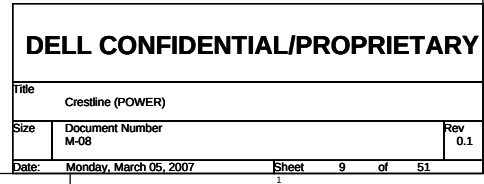
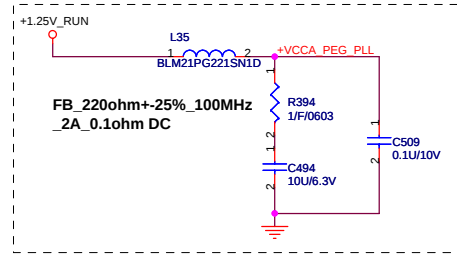
CRESTLINE_ip0

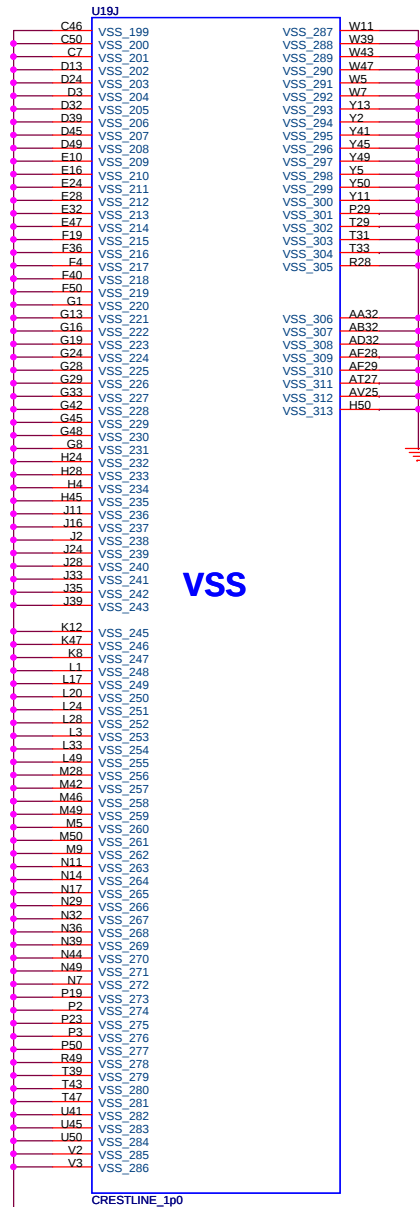
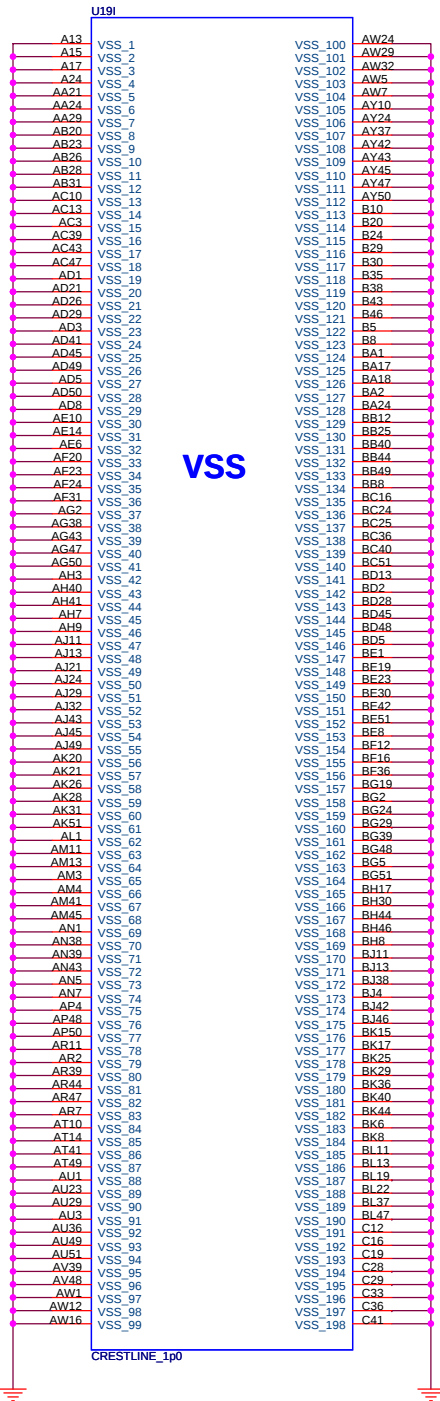
DDR SYSTEM MEMORY B



DELL CONFIDENTIAL/PROPRIETARY

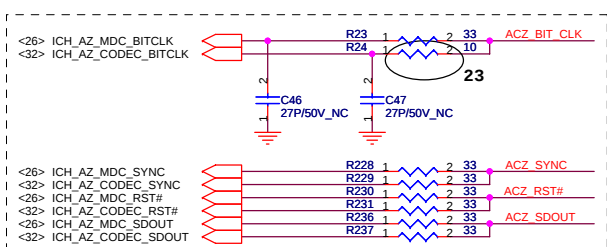
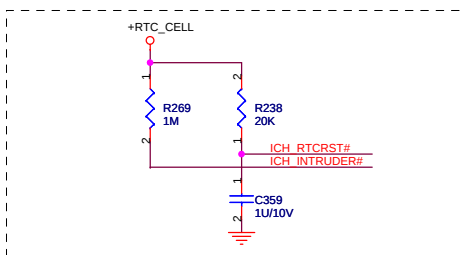
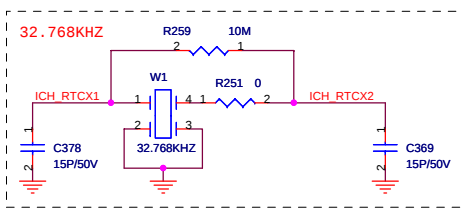




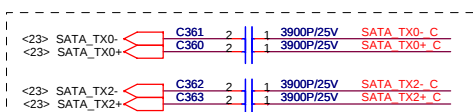


DELL CONFIDENTIAL/PROPRIETARY

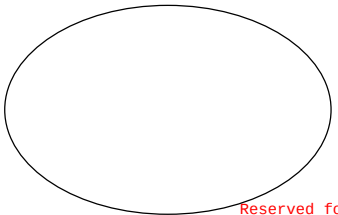
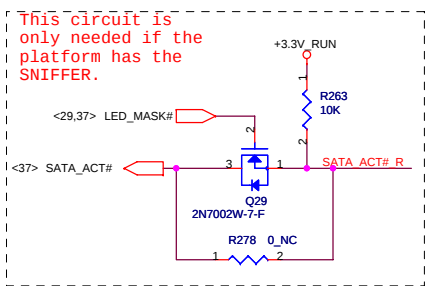
Title		
Crestline (VSS)		
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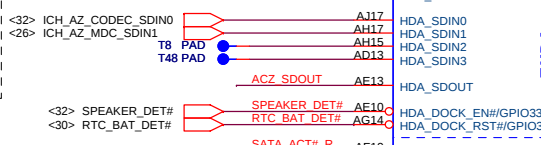
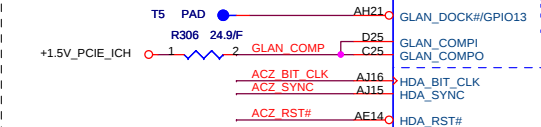
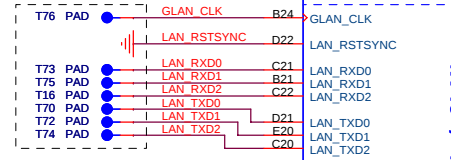
Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R23, R228, R230 & R236 should equal distance to the T split trace point as R24, R229, R231 & R237 respectively. Basically, keep the same distance from T for all series termination resistors.



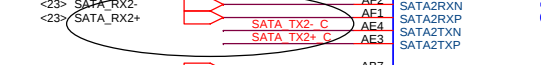
Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.



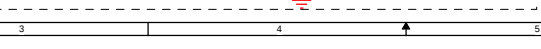
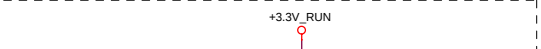
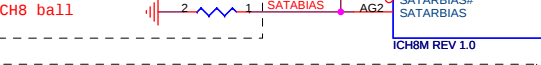
Reserved for Intel Nineveh design.



9/20 Move from SATA port 1

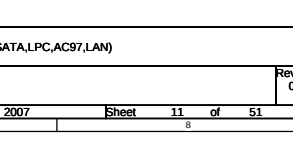
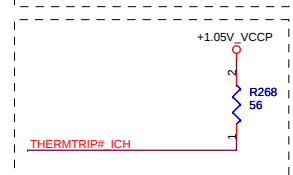
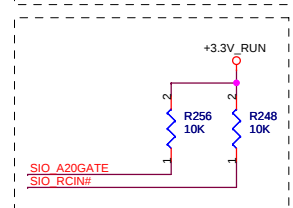
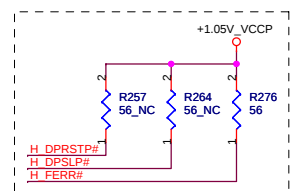
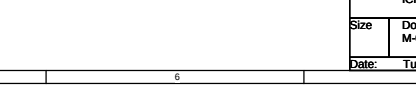
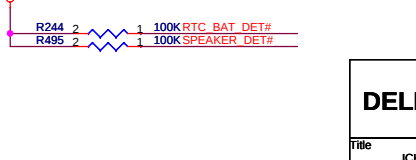
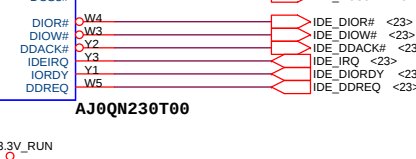
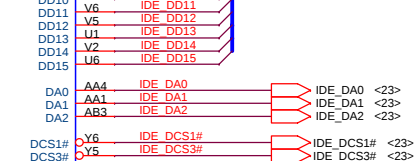
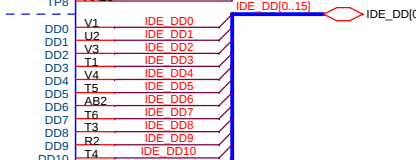
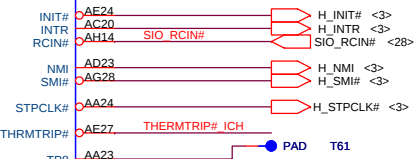
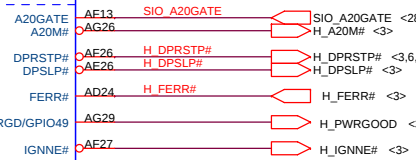
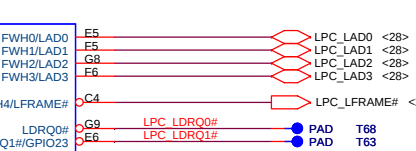
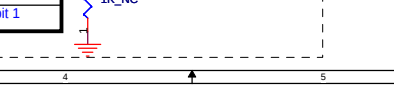
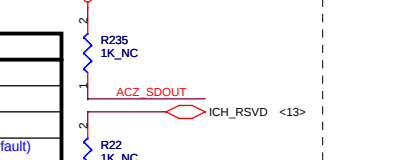
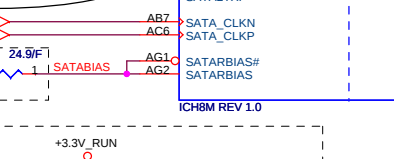
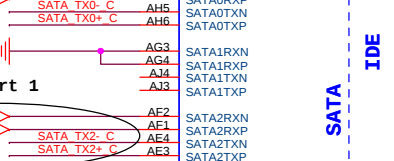
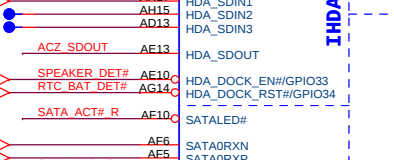
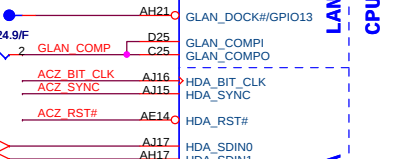
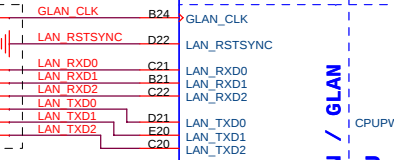
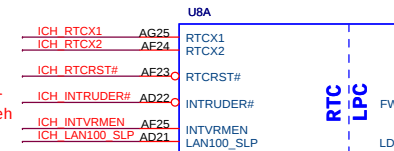


Place within 500mils of ICH8 ball



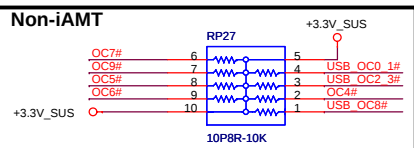
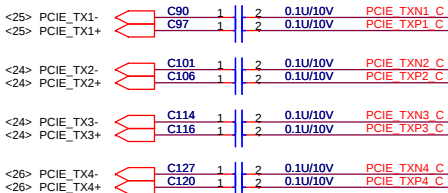
ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

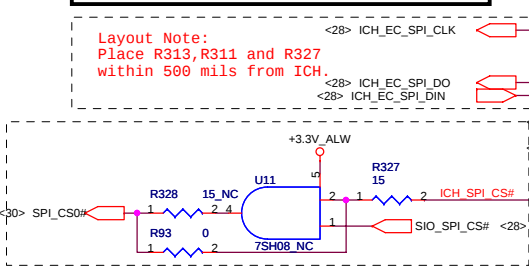


XOR Chain Entrance Strap		
ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

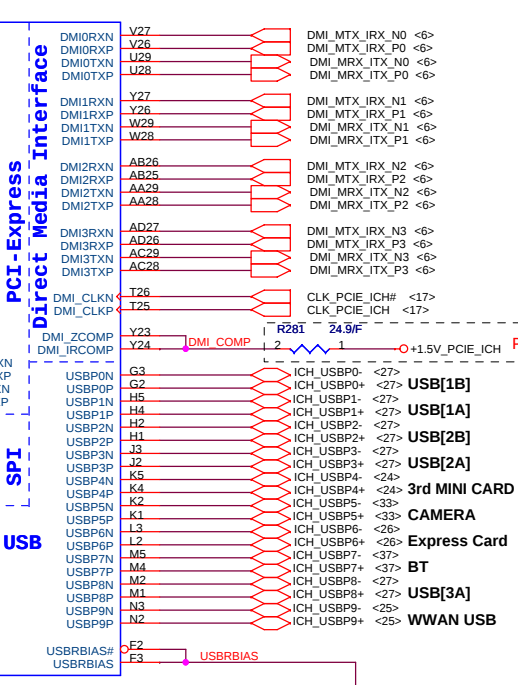
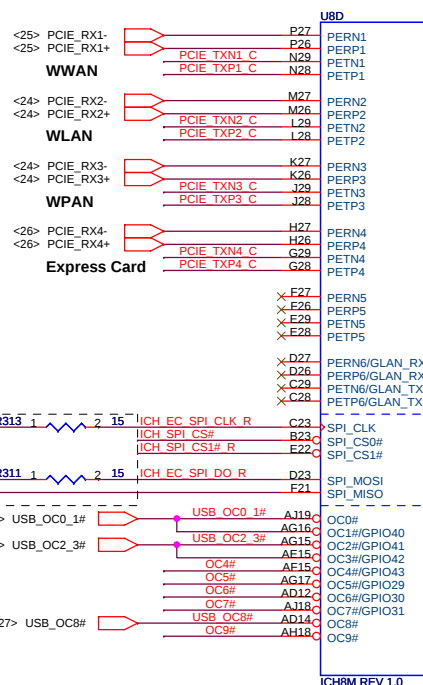
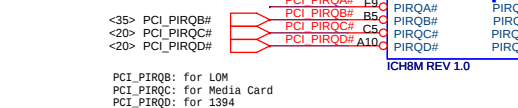
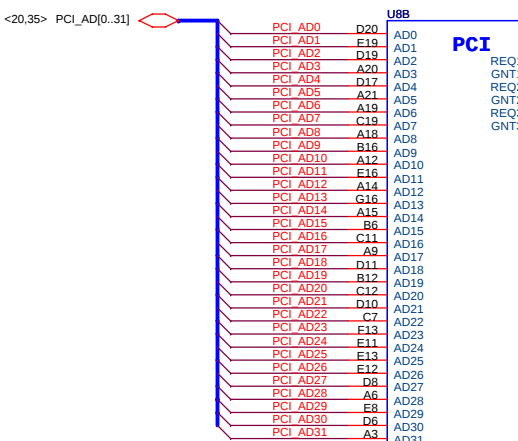
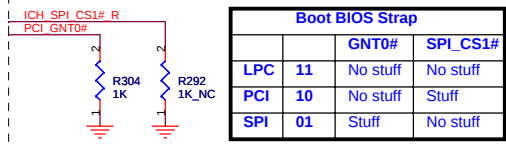
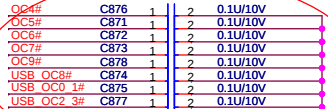
Place TX DC blocking caps close ICH8.



Layout Note:
Place R313, R311 and R327
within 500 mils from ICH.

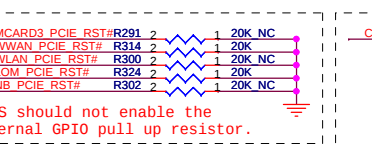
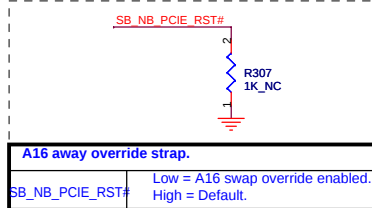


WWAN Noise - ICH improvements

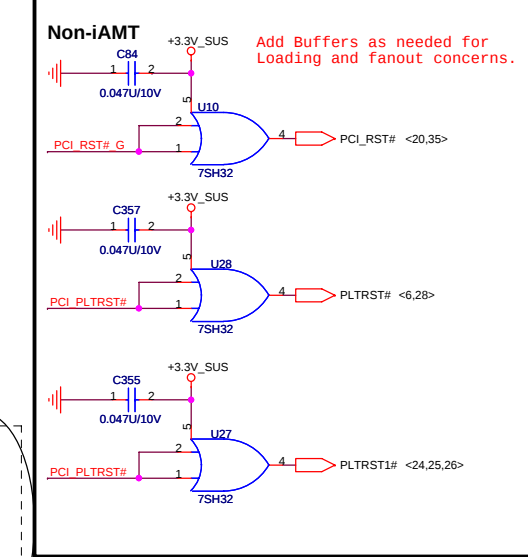
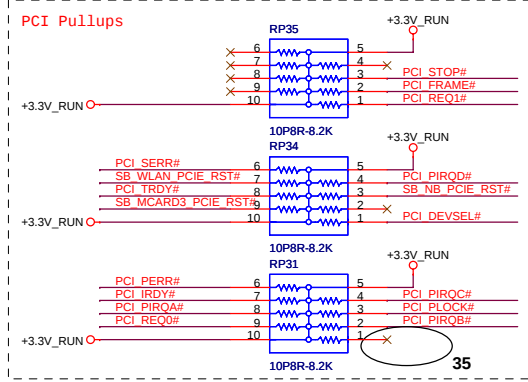


Short F2 and F3 at the package
and keep length to less than
500mils. Trace Impedance
should be 60ohms +/- 15%.

LOM	REQ0	GNT0	PIRQB
1394/MediaCard	REQ1	GNT1	PIRQC



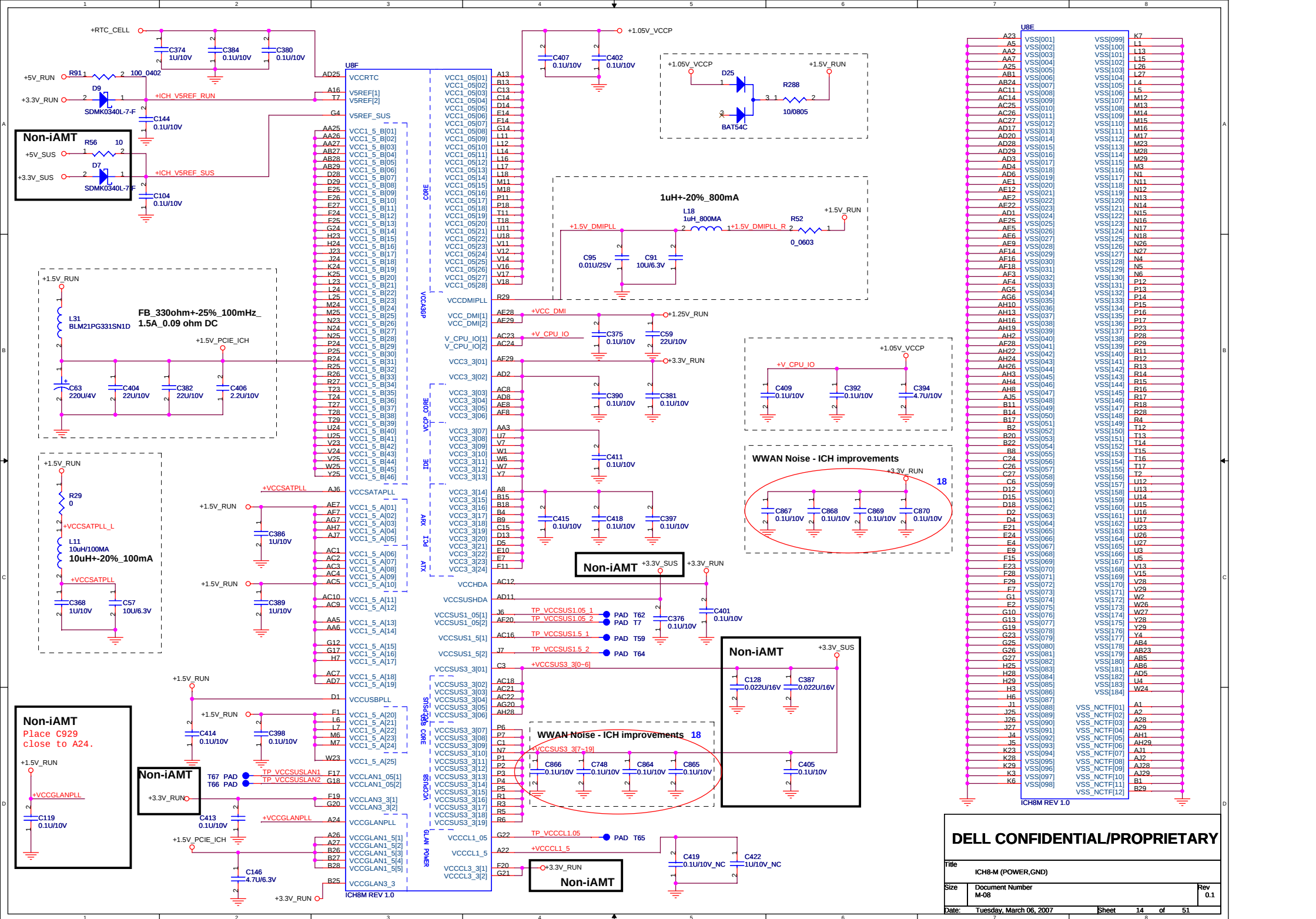
Place within 500mils of ICH8



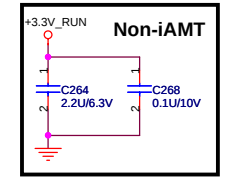
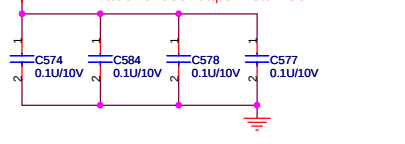
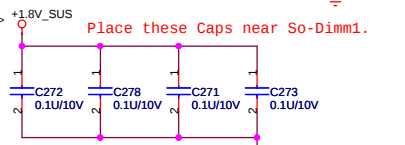
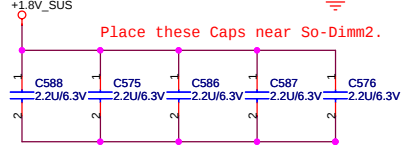
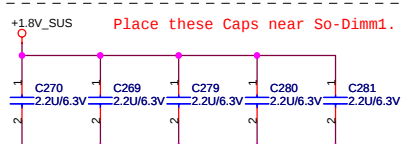
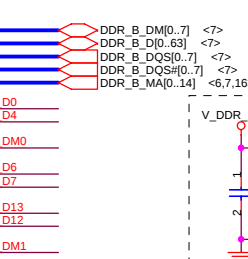
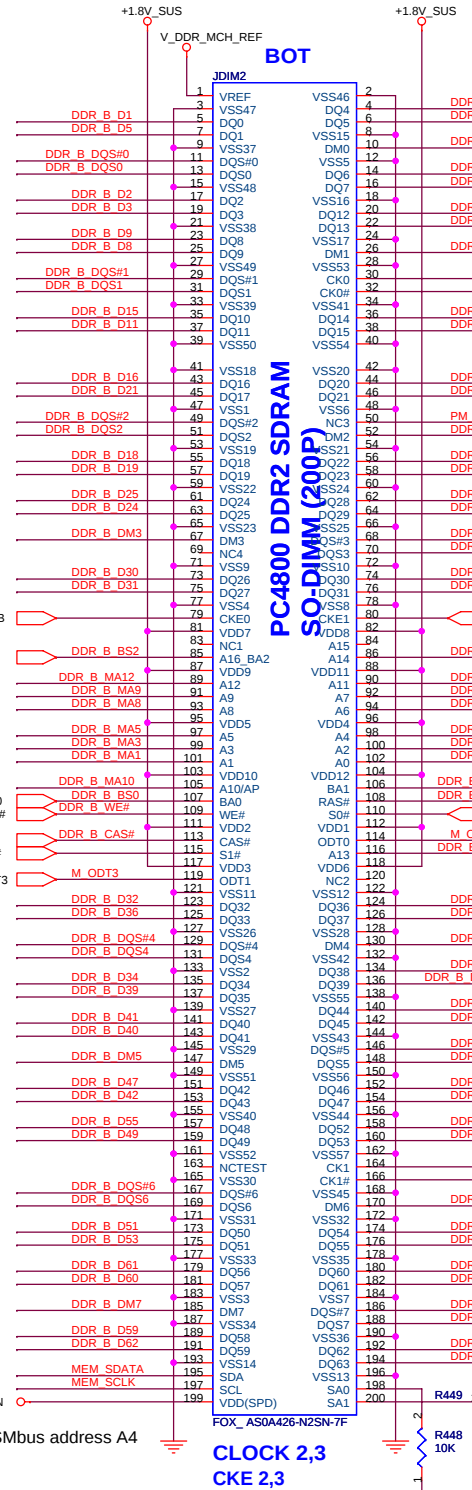
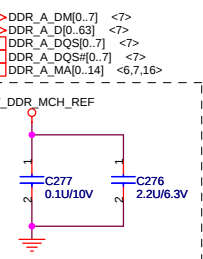
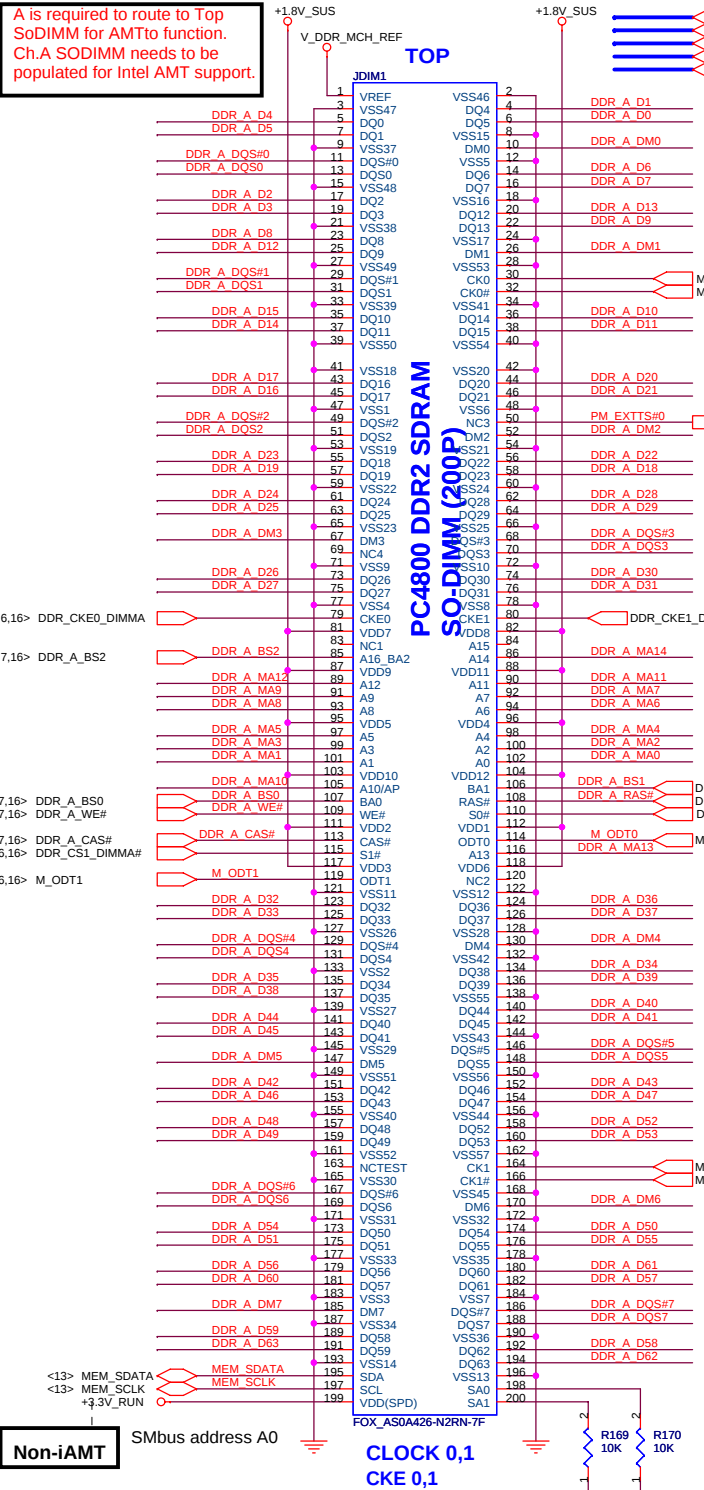
DELL CONFIDENTIAL/PROPRIETARY

Title	ICH8-M (USB,DMI,PCIE,PCI)
Size	Document Number
Date	Tuesday, March 06, 2007
Sheet	12 of 51

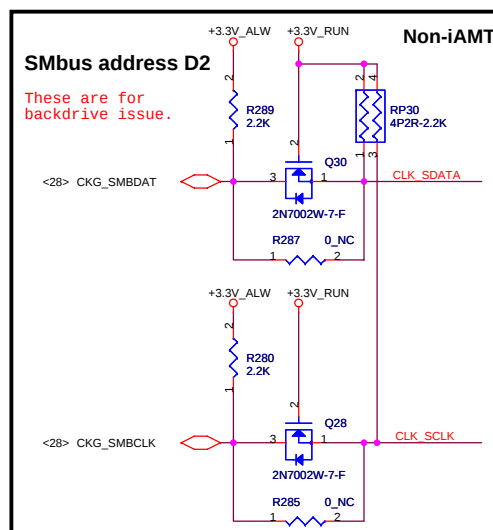
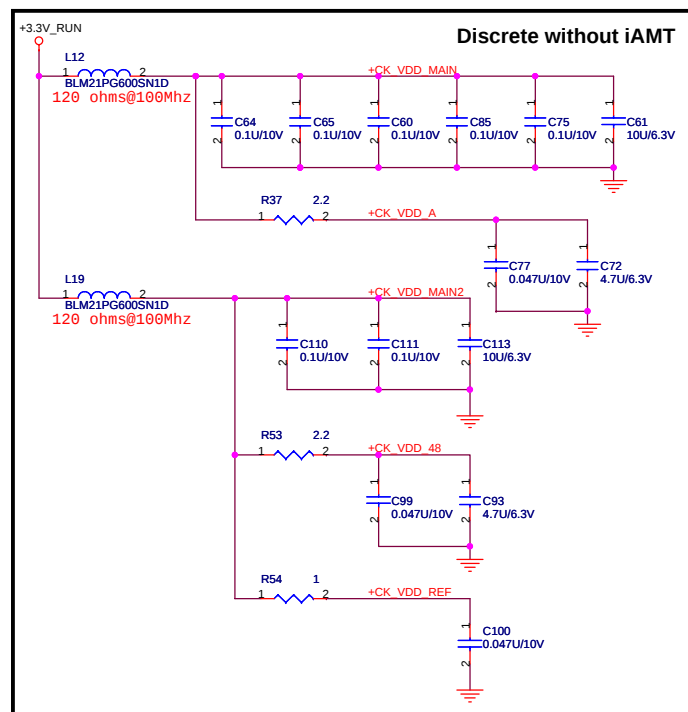
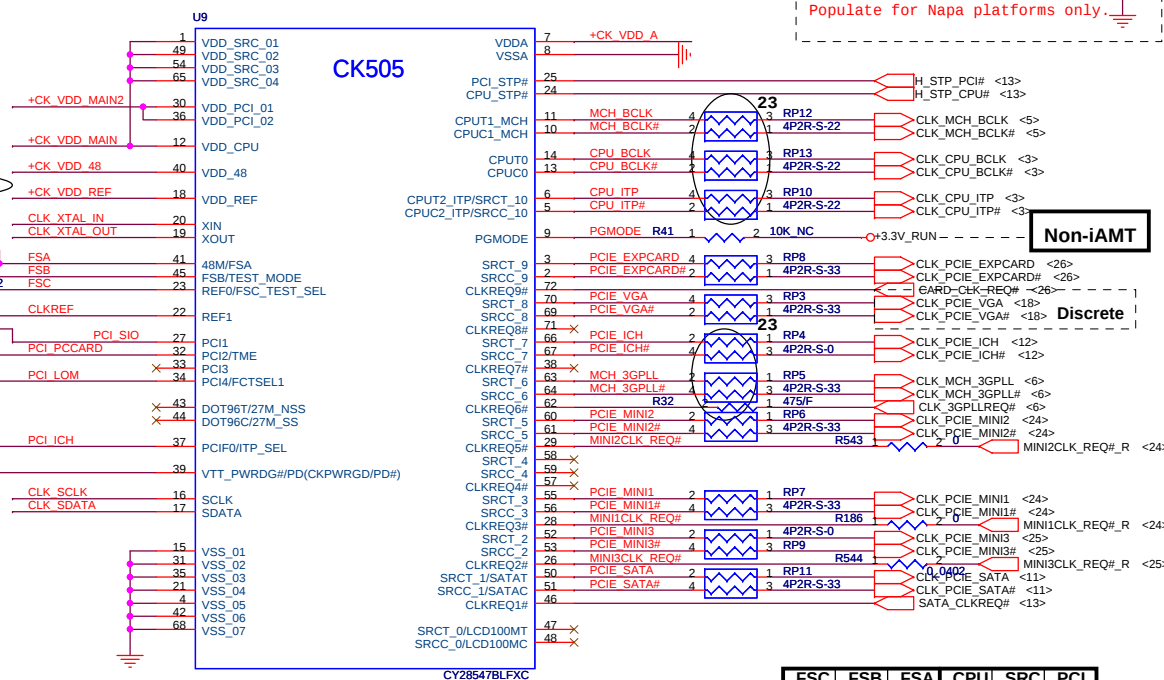
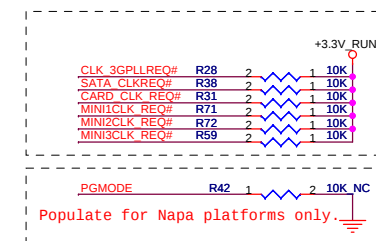
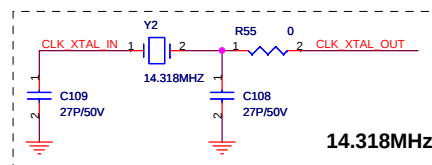
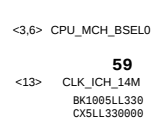
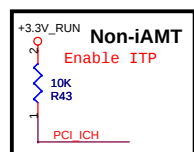
Title			
ICH8-M (PM,GPIO,SMB,CL)			
Size	Document Number	Rev	
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Date:	Tuesday, March 06, 2007	Sheet	13 of 51



A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.



DELL CONFIDENTIAL/PROPRIETARY			
Title	DDR2 SO-DIMM (200P) X 2		
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FSC	FSB	FSA	CPU	SRC	PO
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0

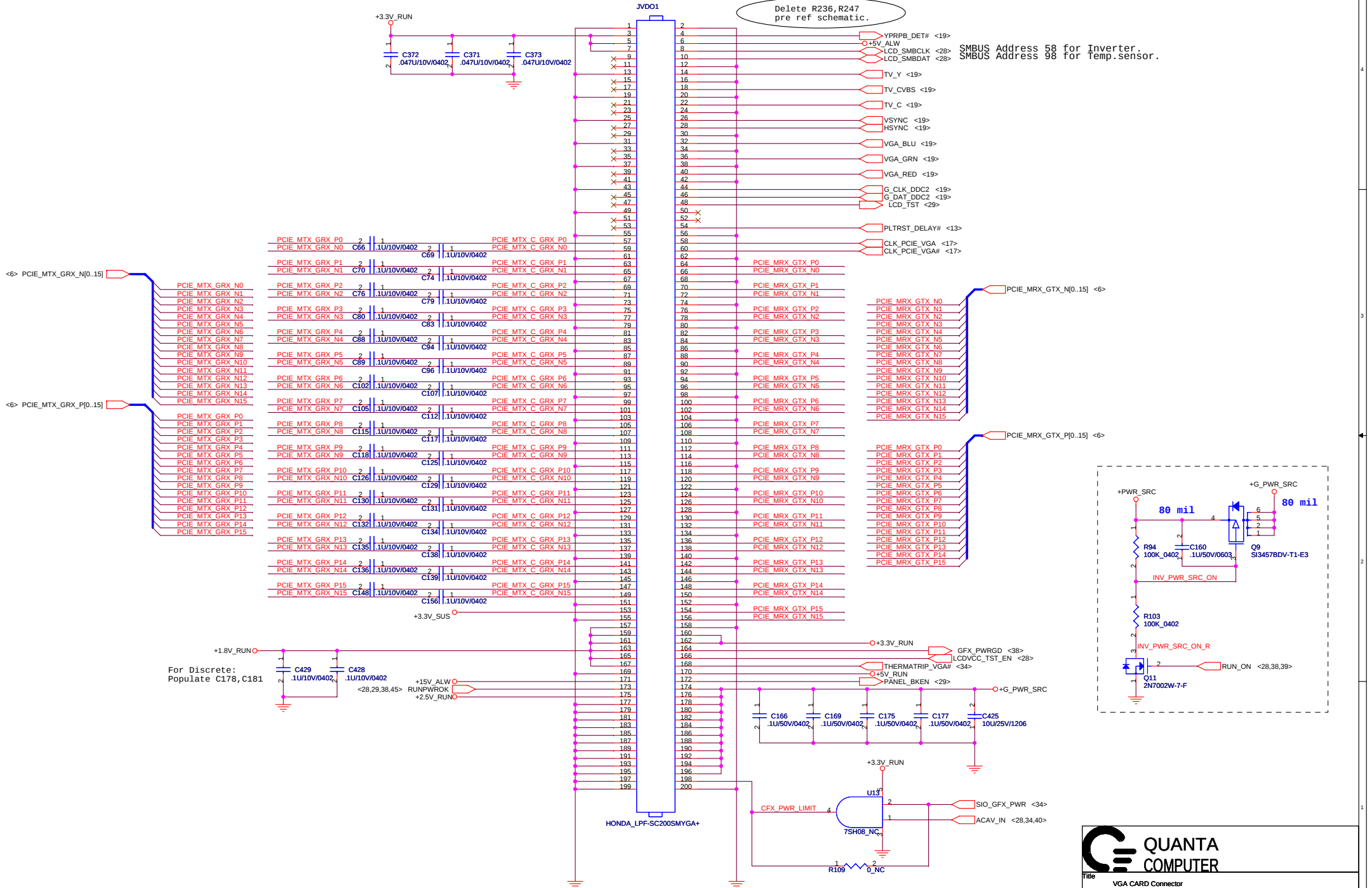
DELL CONFIDENTIAL/PROPRIETARY

Title			
CLOCK GENERATOR			
Size	Document Number		Rev
	M-08		0.1
Date:	Wednesday, March 07, 2007	Sheet	17 of 51

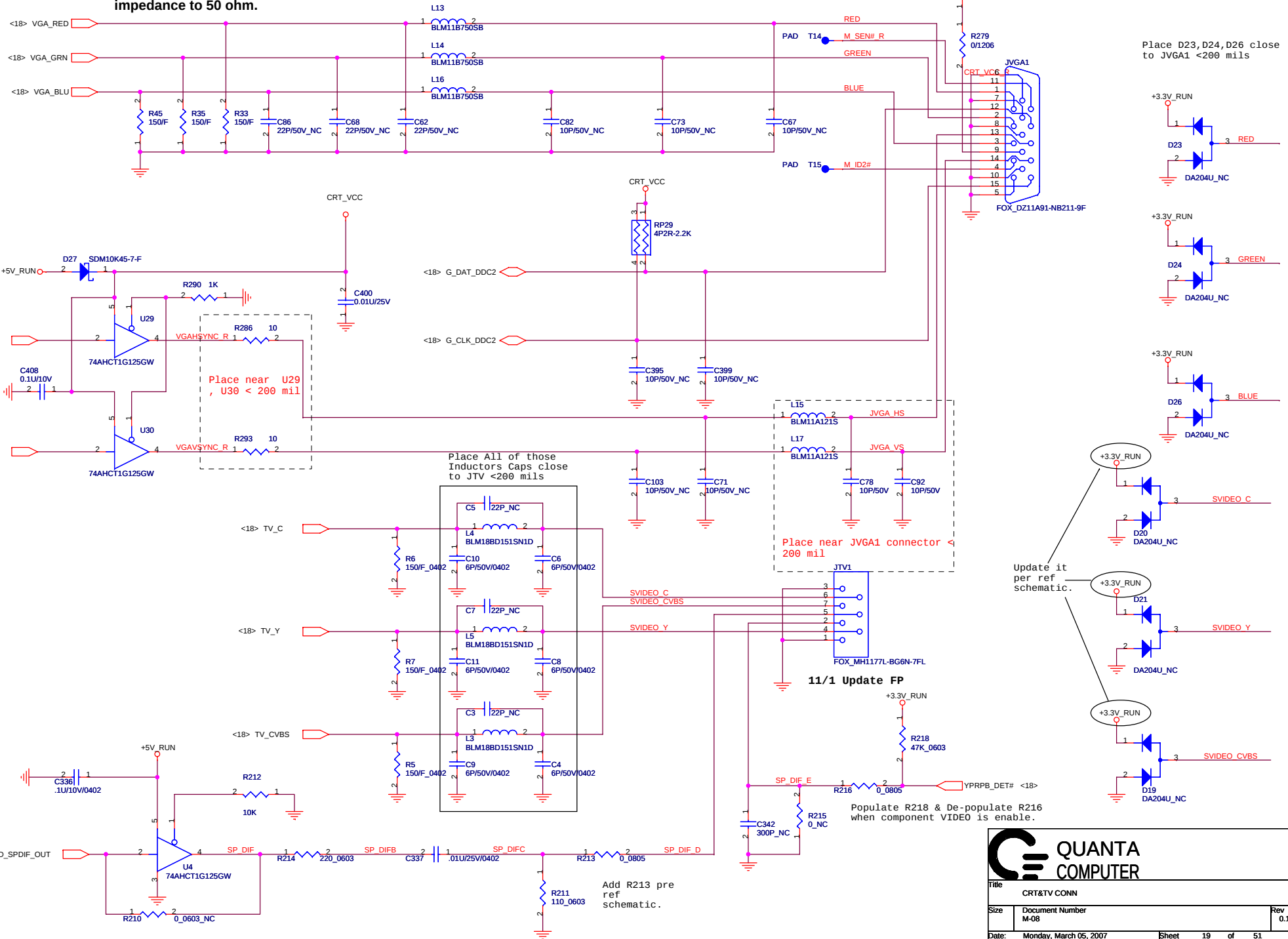
YPRPB_DET: SIGNAL FROM SVIDEO CONNECTOR,
TO SWITCH TO COMPONENT OUT.

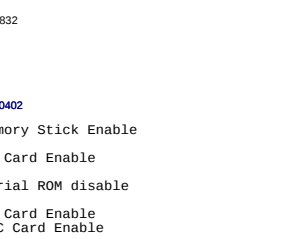
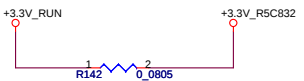
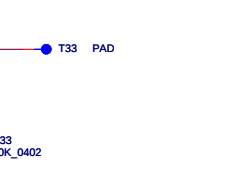
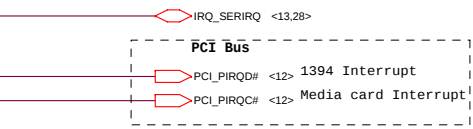
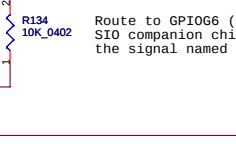
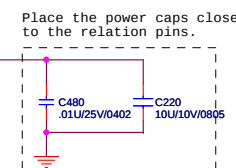
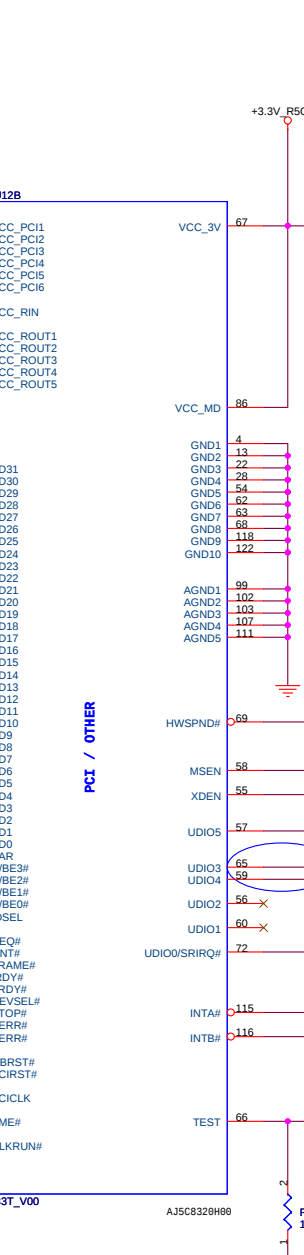
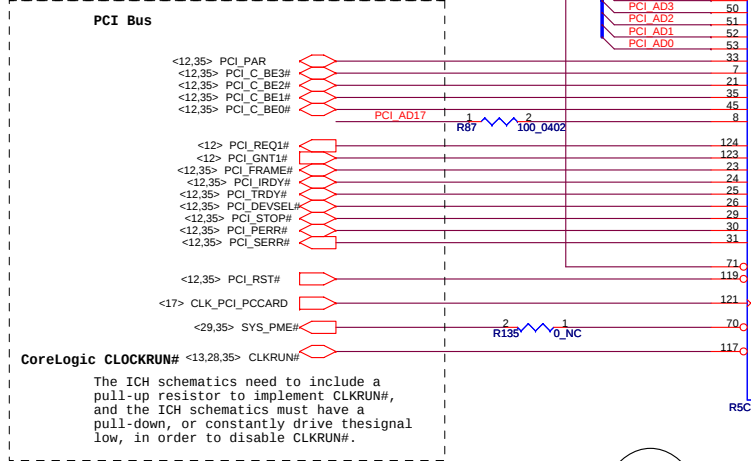
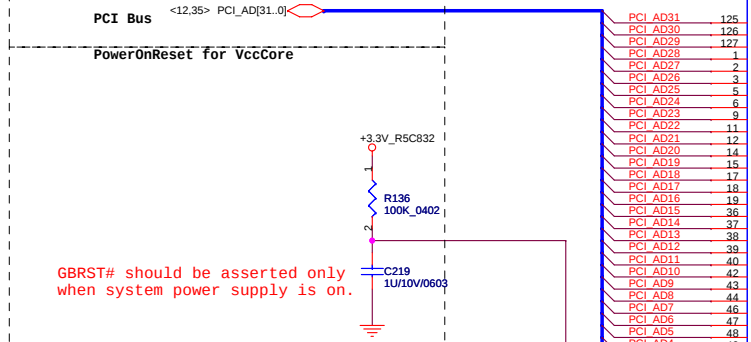
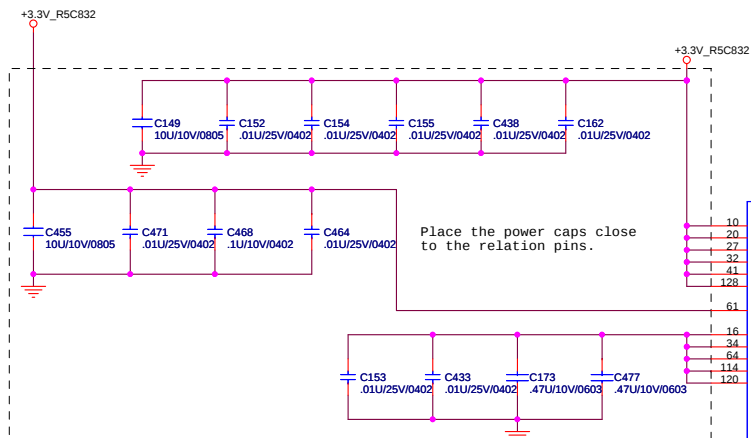
Delete R236,R247
pre ref schematic.

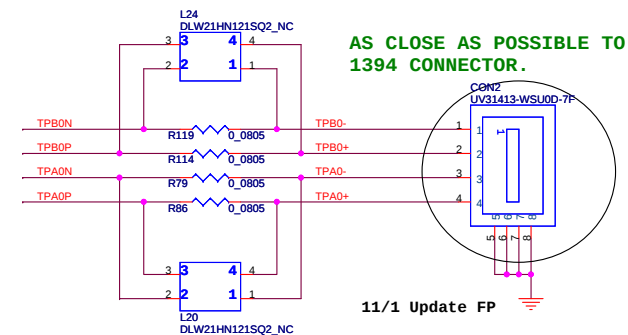
SMBUS Address 58 for Inverter.
SMBUS Address 98 for Temp.sensor.

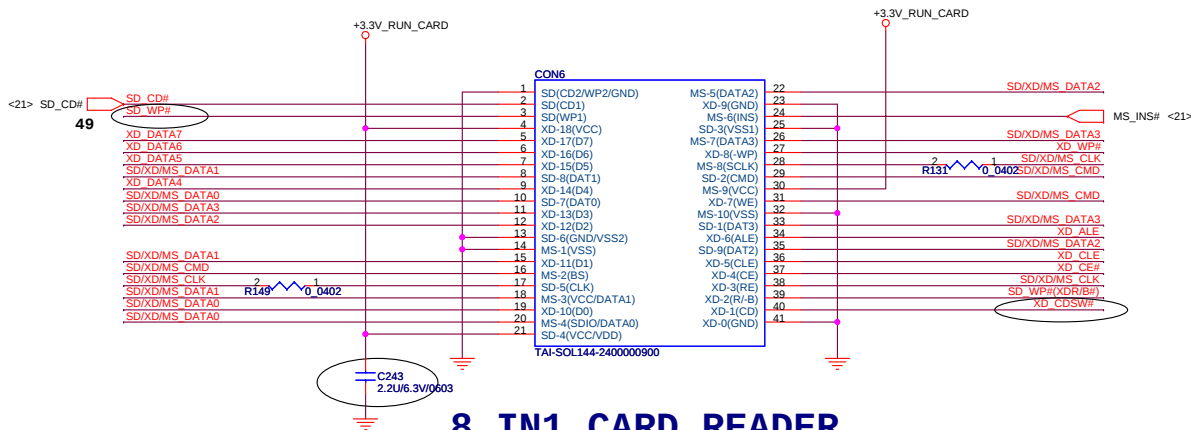


Setting R,G,B treac impedance to 50 ohm.



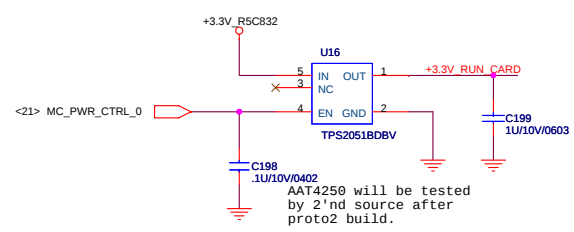
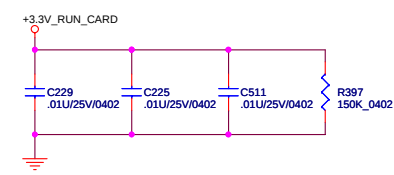






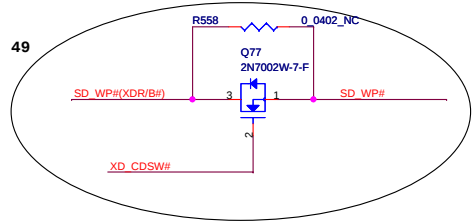
8 IN1 CARD READER

- <21> SD_CD#
- <21> SD_WP#
- <21> XDATA7
- <21> XDATA6
- <21> XDATA5
- <21> XDATA4
- <21> SDXIMS_DATA3
- <21> SDXIMS_DATA2
- <21> SDXIMS_DATA1
- <21> SDXIMS_DATA0
- <21> SDXIMS_CMD
- <21> XD_WP#
- <21> XD_ALE
- <21> XD_CLE
- <21> XD_CE#
- <21> SDXIMS_CLK



AAT4250 will be tested by 2'nd source after proto2 build.

SD Protect

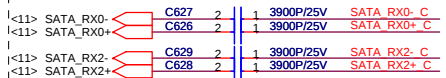


SATA 1 & 2 Connector.

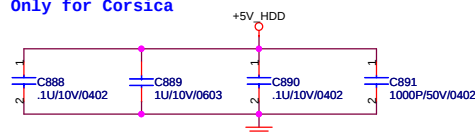


Place close to
connector side

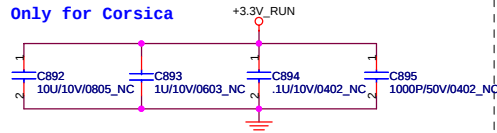
Locate caps C626, C627, C628, C629 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 0 mils



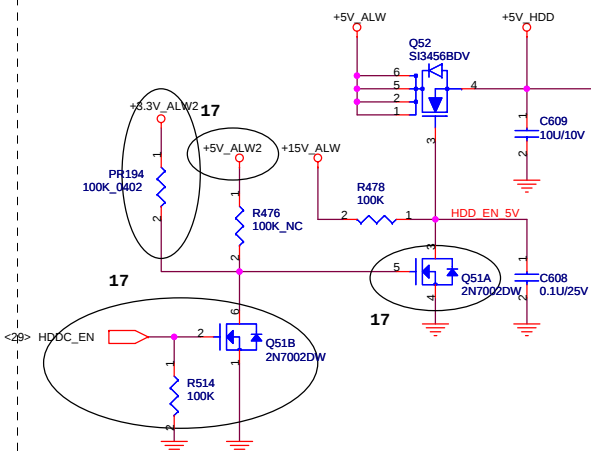
Only for Corsica



Only for Corsica



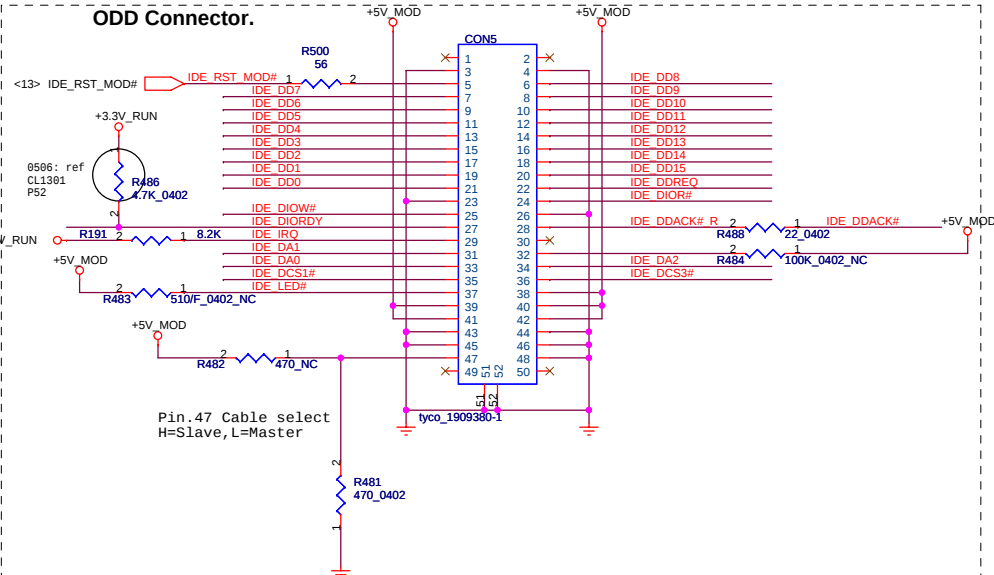
SATA PWR



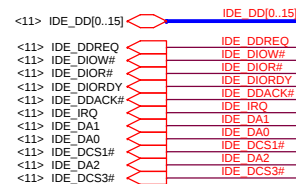
SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at
MobileMark is 1.1W. An additional 150mW
can be saved using Intel's IMST driver.

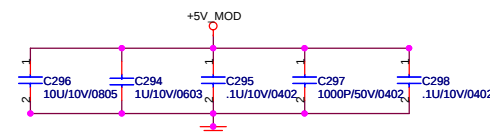
ODD Connector.



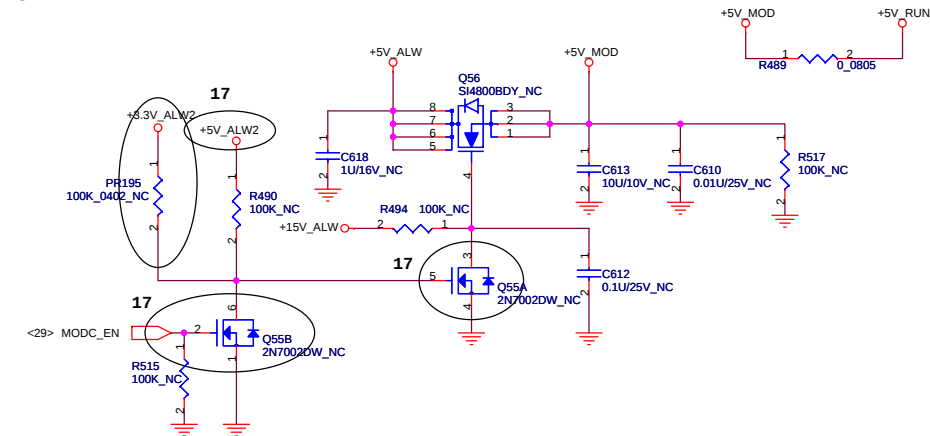
Pin.47 Cable select
H=Slave,L=Master



Place closed to
MOD connector

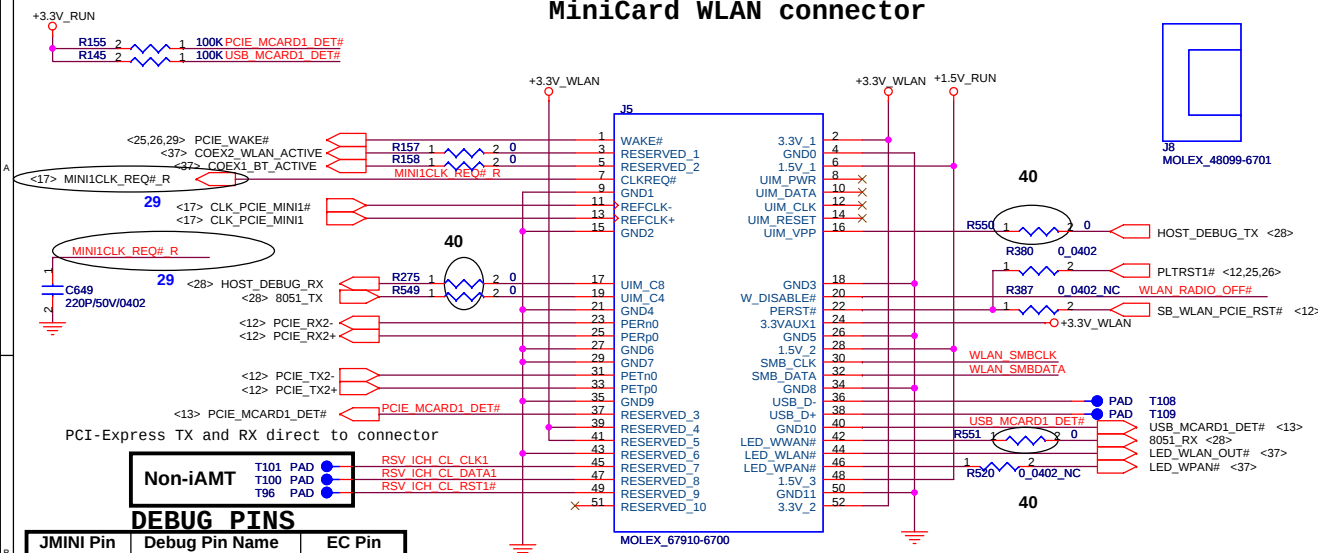


ODD PWR

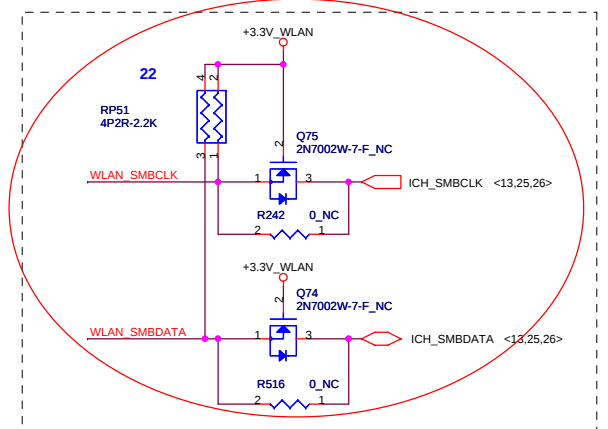
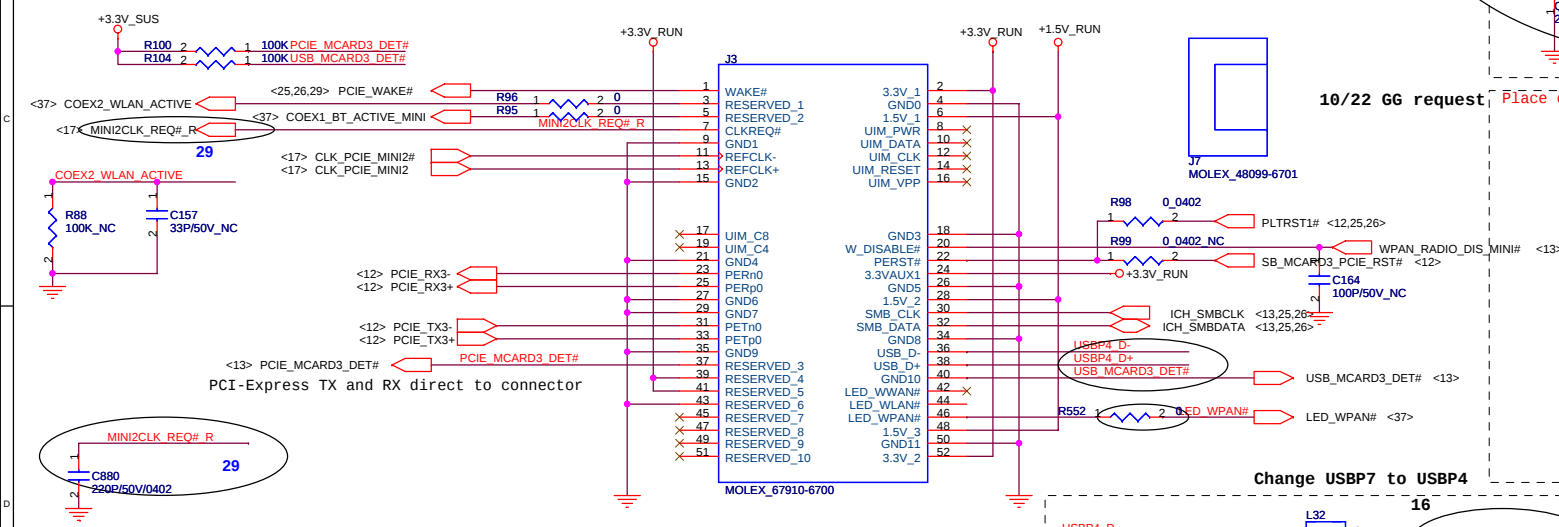


Title			
SATA (HDD&CD_ROM)			
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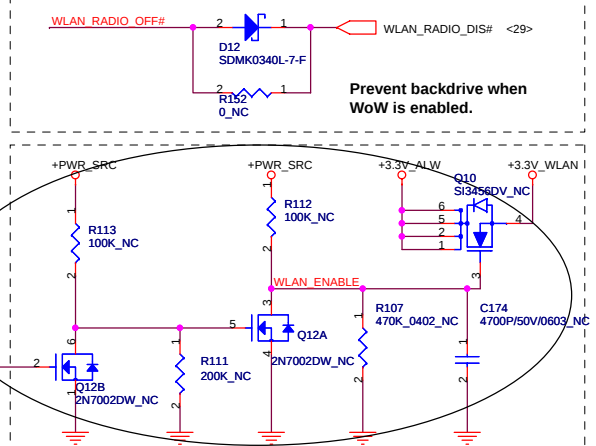
MiniCard WLAN connector



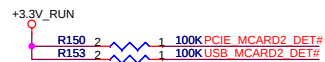
MiniCard WPAN connector



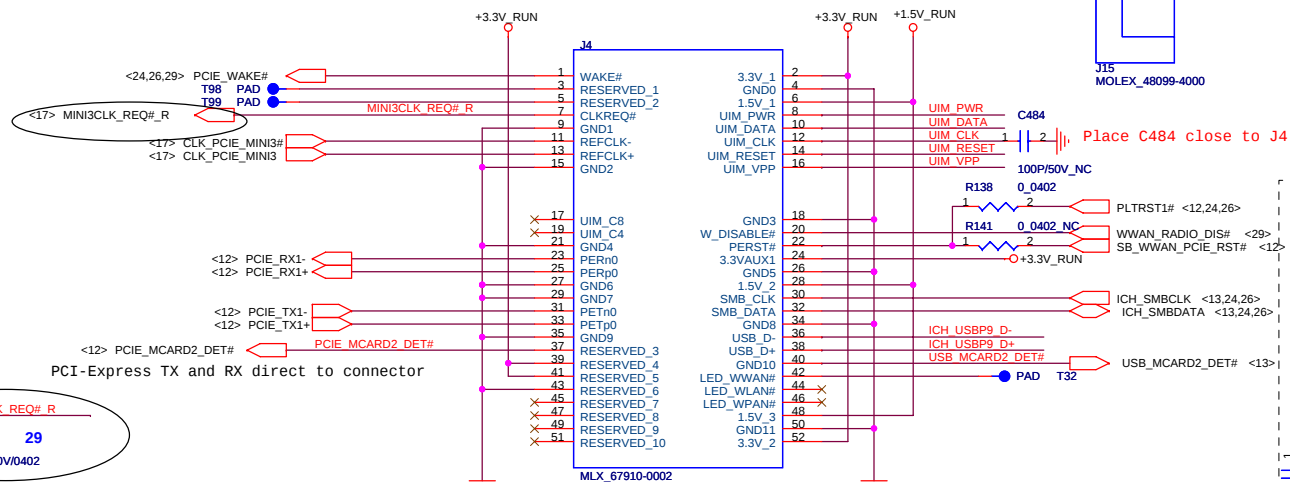
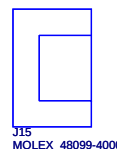
Support for WoW



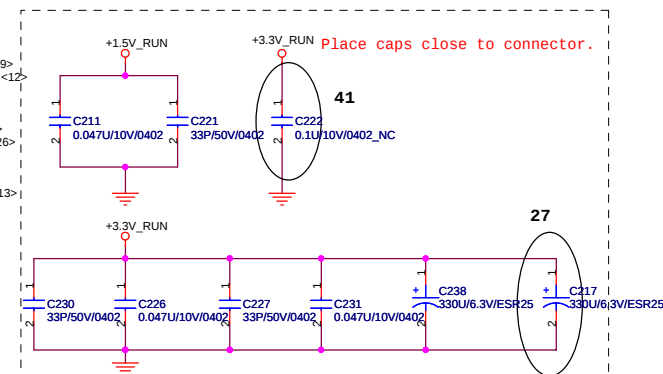
Title			MINI-PCI
Size	Document Number	Rev	
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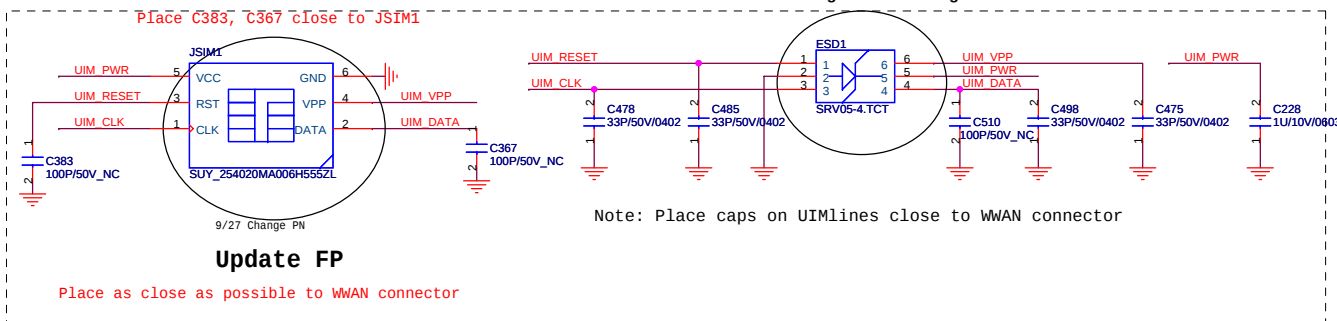
MiniCard WWAN connector



Place C484 close to J4



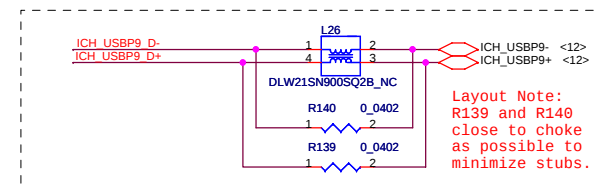
10/4 EMI agree to change P/N



Note: Place caps on UIMlines close to WWAN connector

Update FP

Place as close as possible to WWAN connector

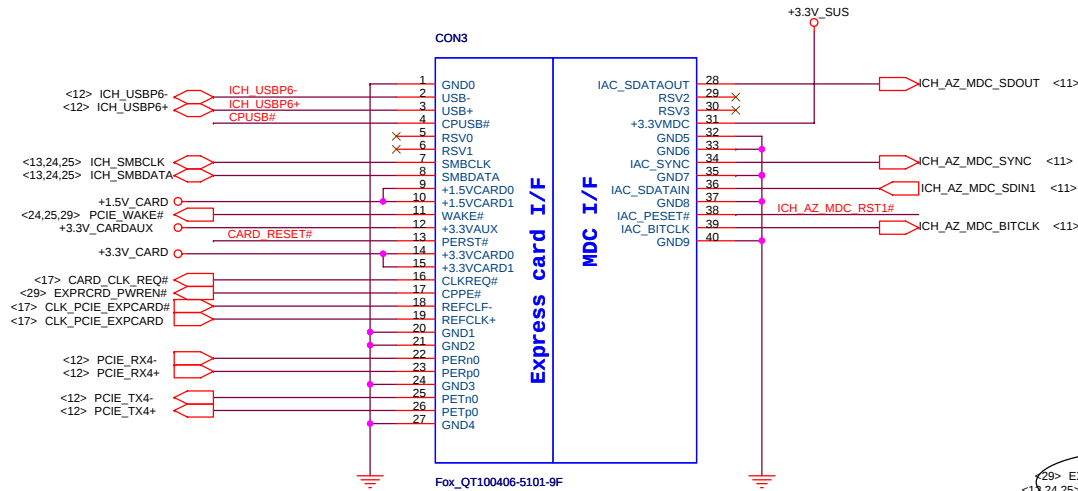


Layout Note:
R139 and R140
close to choke
as possible to
minimize stubs.

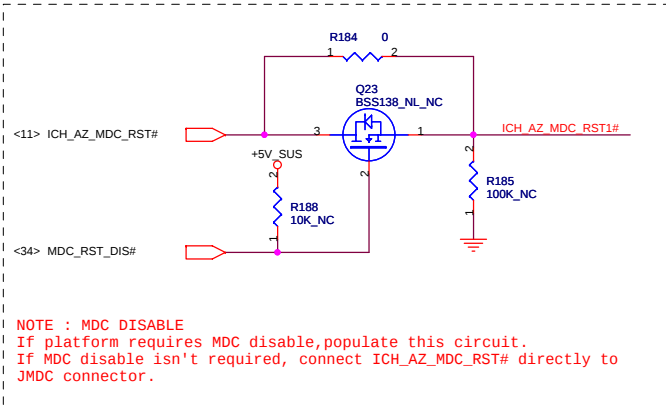
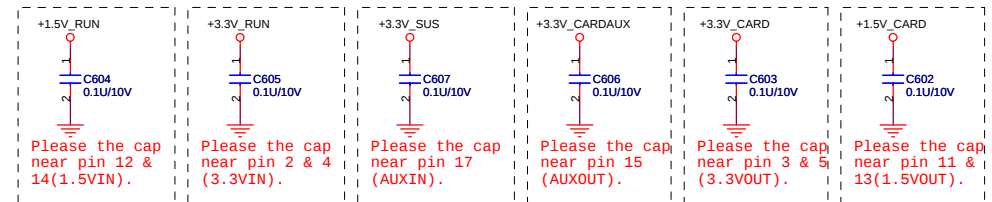
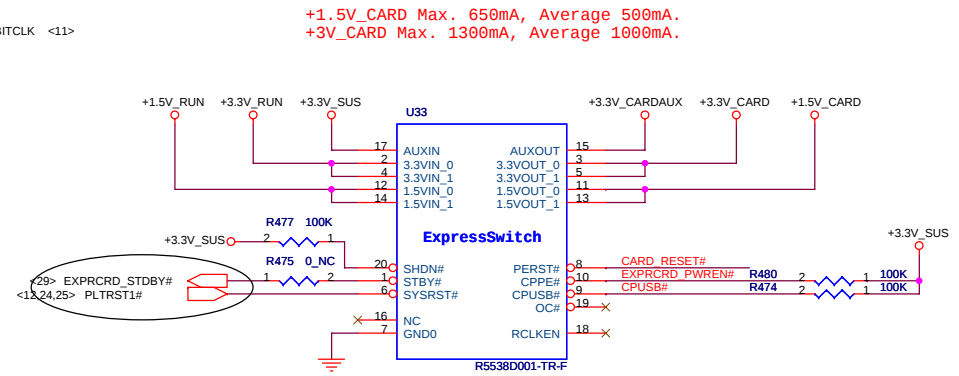


Title WWAN		
Size	Document Number VC-08B	Rev 0.1
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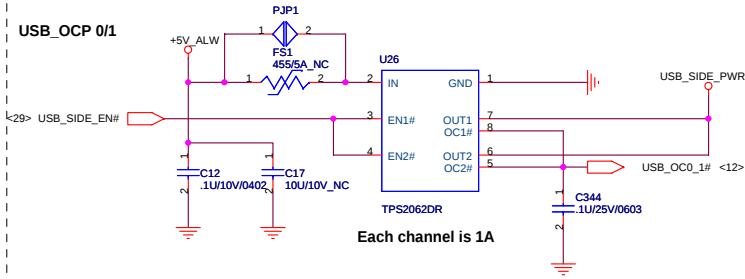
EXPRESS+MDC



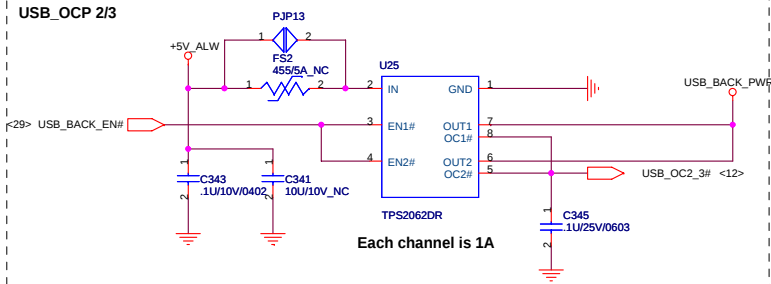
Update PN



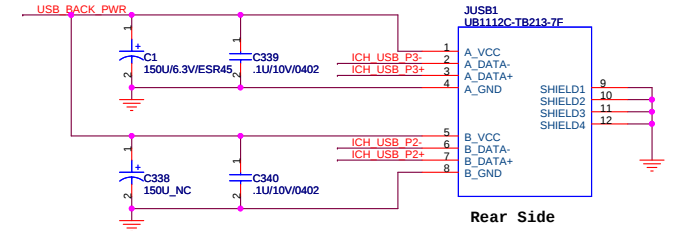
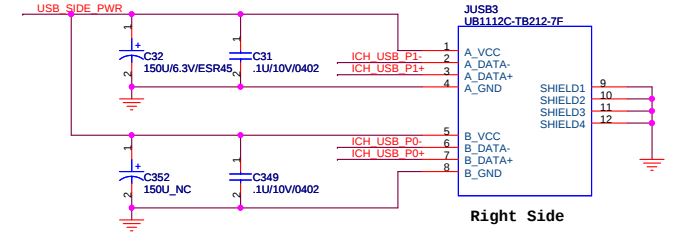
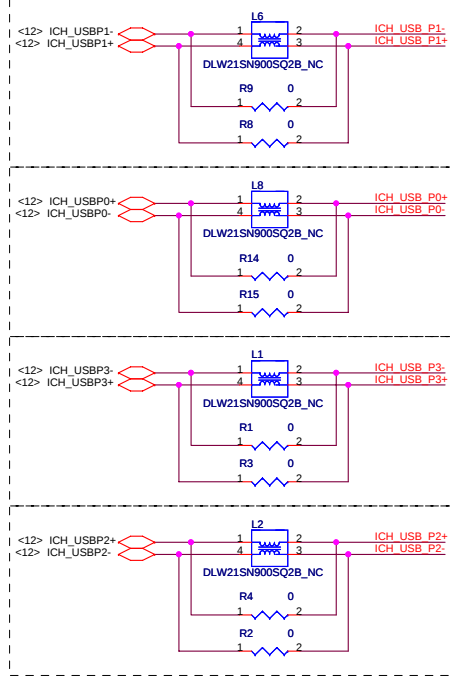
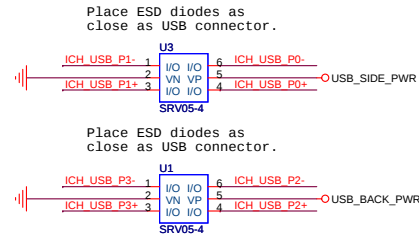
USB_OCP 0/1



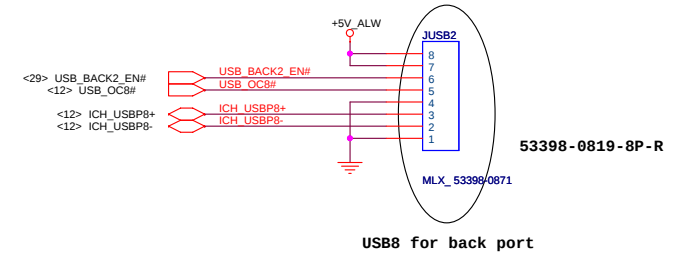
USB_OCP 2/3



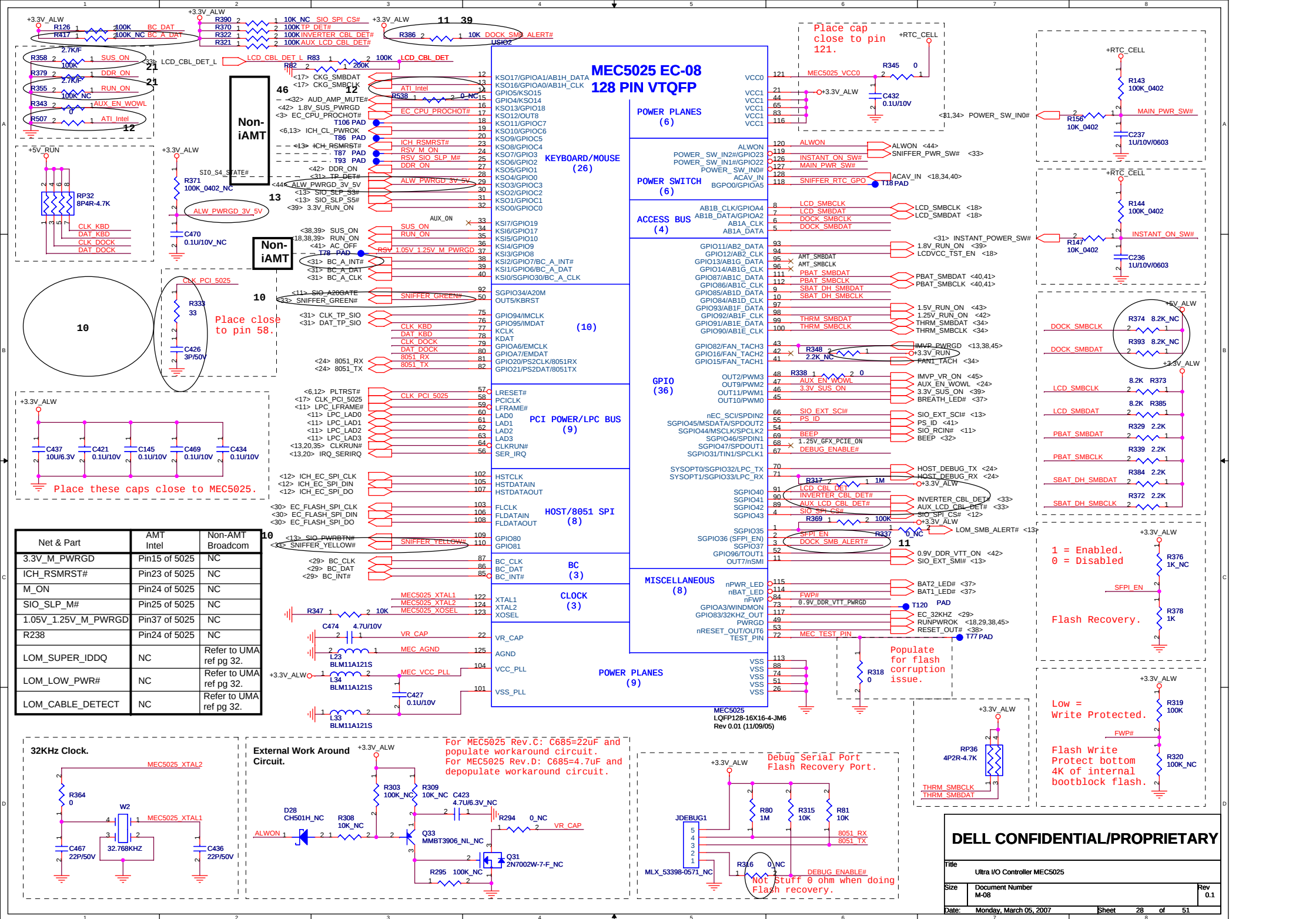
ESD Protect



Gilligan Only

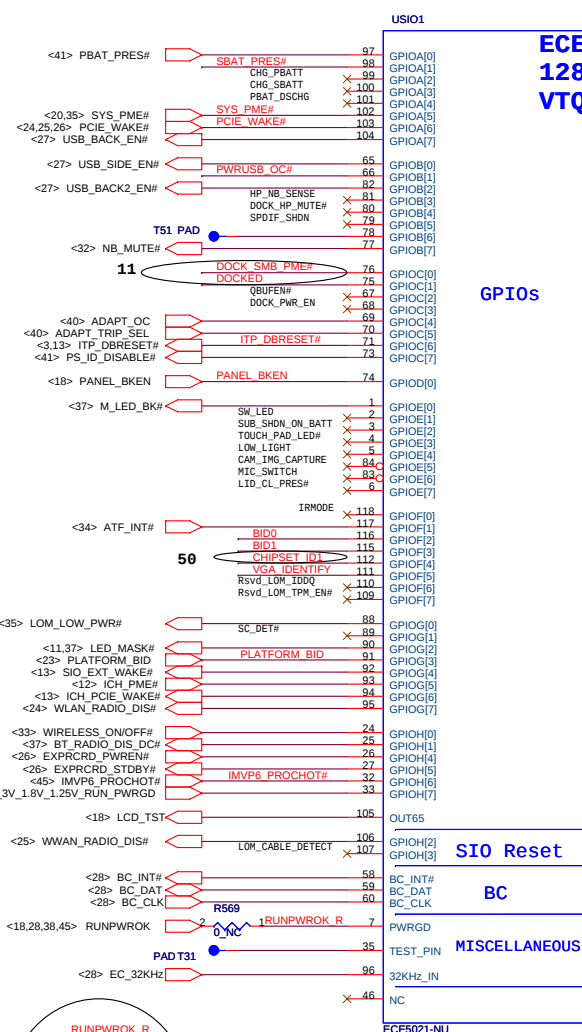


Title			USB & Flash
Size	Document Number	Rev	0.1
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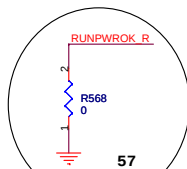


VGA	BID2	BID1	BID0	Board Revision
1	0	0	0	SST (X00)
1	0	0	1	Pre-PT (X01)
1	0	1	0	PT (X02)
1	0	1	1	ST (X03)
1	0	0	0	QT (A00)
1	0	0	1	RAMP-2 (A01)

Reset BID



Update P/N



Pin

USB

GPIOs

CIRCC

POWER

SIO Reset

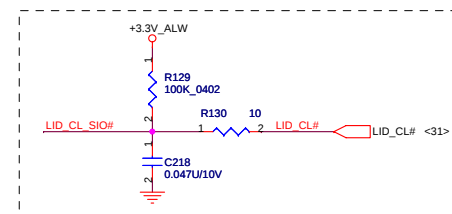
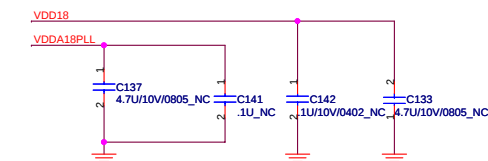
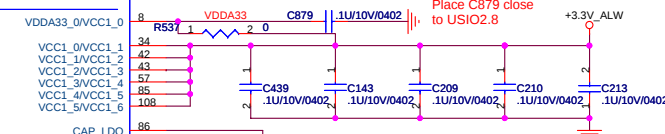
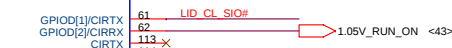
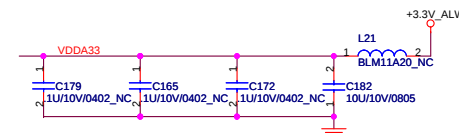
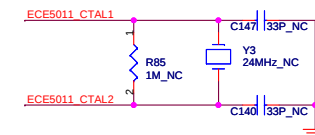
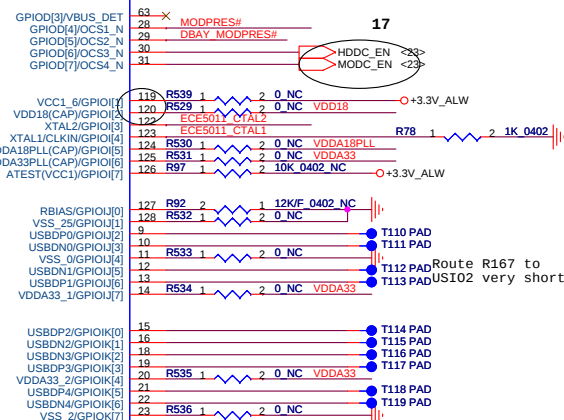
BC

MISCELLANEOUS

ECE5021-NU

Update to 5021

Depopulate R529, R530, R531, R532, R533, R534, R535, R536, R92, R97, C142, C133, C137, C141, C179, C165, C172, L21
Populate R537, C879.



Title	SIO (GPIO/BC/USB/CIRR)
-------	------------------------

Size	Document Number FM1
------	------------------------

Date: Monday, March 05, 2007

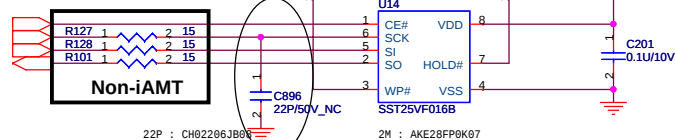
Rev	0.1
-----	-----

1	

16Mbit (2M Byte), SPI

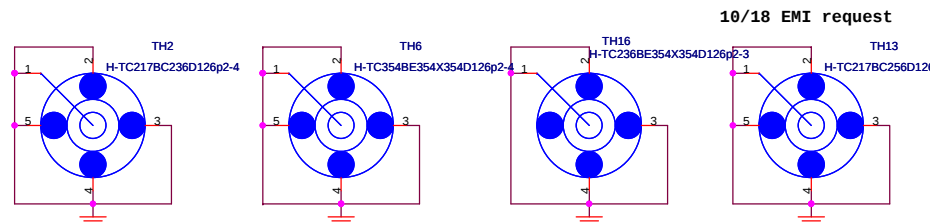
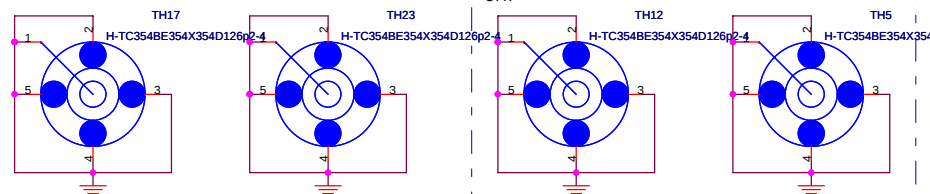
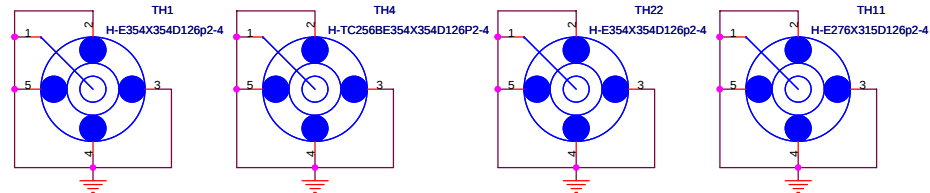
Layout Note:
Place R471 within 500 mils from SPI flash.
Place R498 & R534 within 500 mils of the
MEC5025.

<12> SPI_CS0#
<28> EC_FLASH_SPI_CLK
<28> EC_FLASH_SPI_DO
<28> EC_FLASH_SPI_DIN



Non-iAMT

55

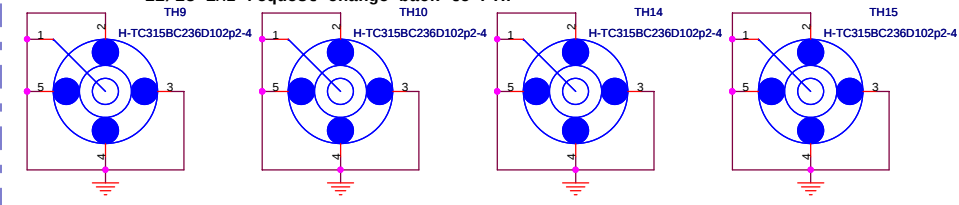


10/18 EMI request

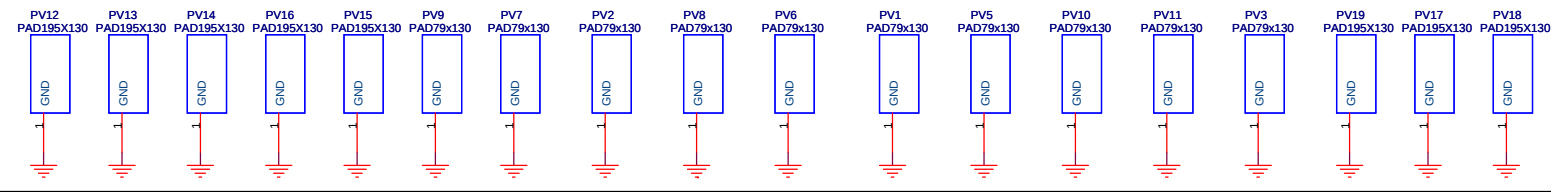
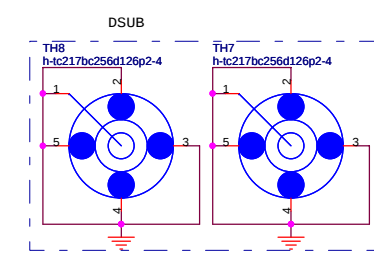
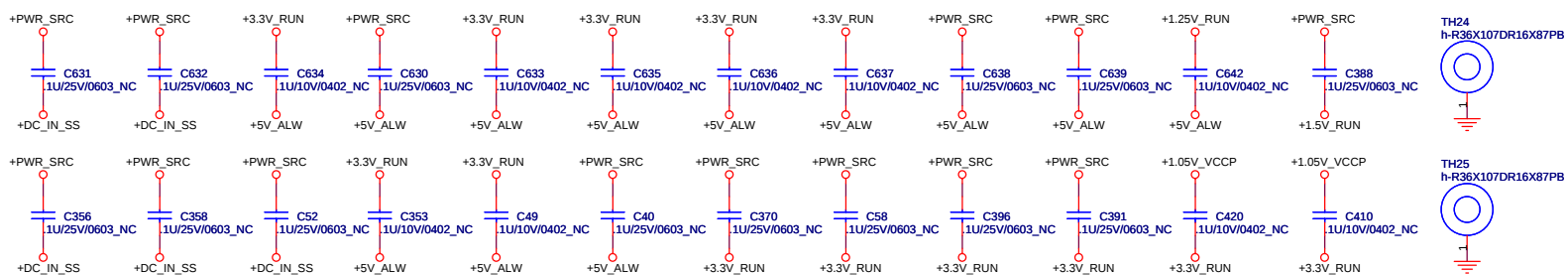
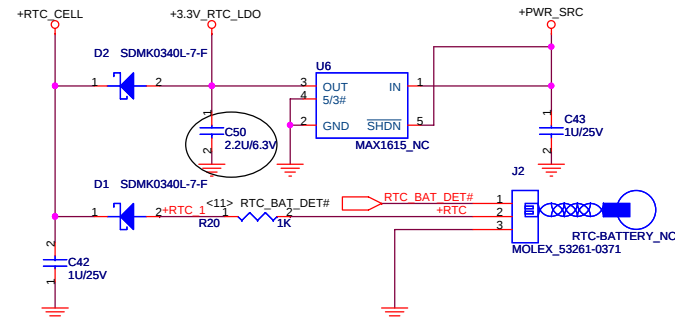
CPU

10/4 EMI request change to NPTH

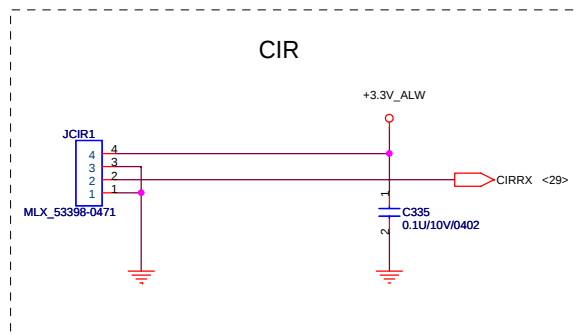
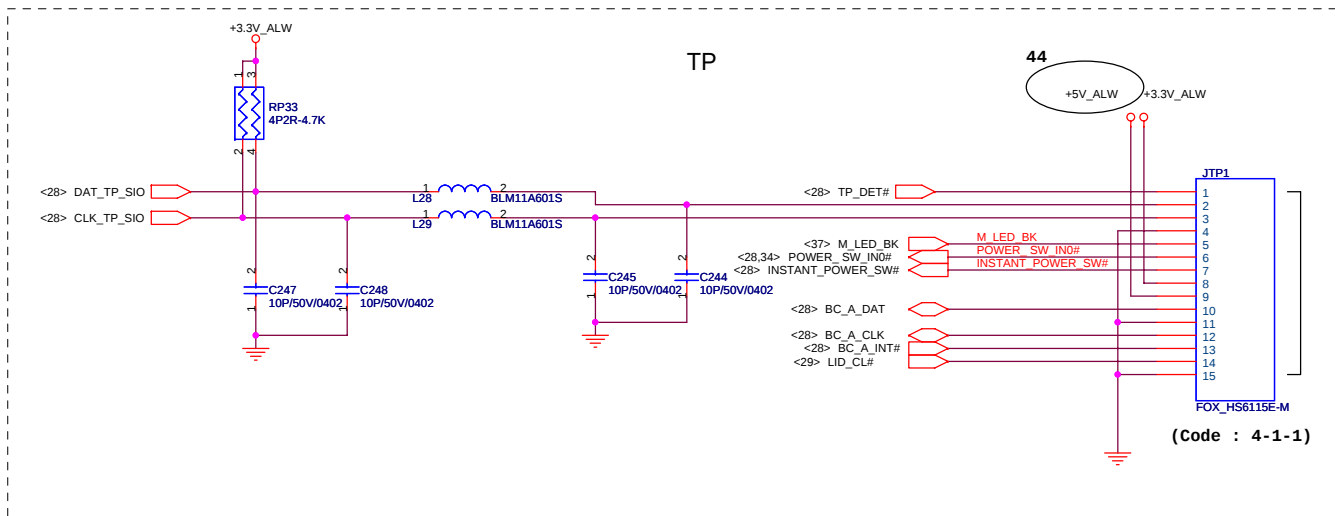
11/28 EMI request change back to PTH



RTC BATTERY



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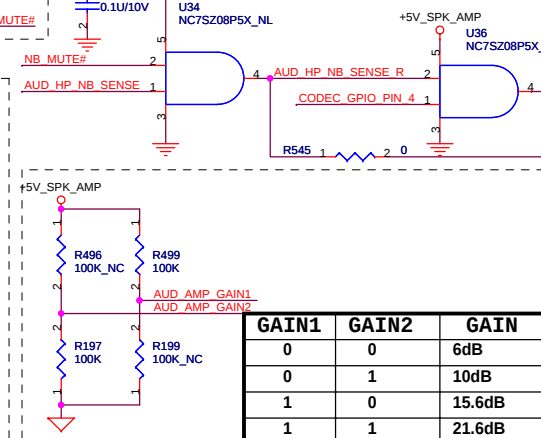
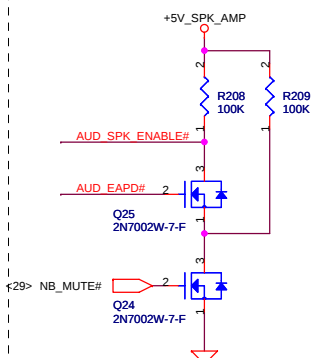
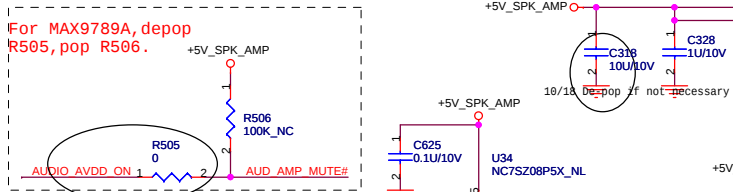


52

AUD LINE OUT L	C306	2	2	033U/25V/X7R/1206
AUD LINE OUT R	C307	2	2	033U/25V/X7R/1206
AUD HP OUT L	C326	2	1	1uF/25V/X7R/1206
AUD HP OUT R	C329	2	1	1uF/25V/X7R/1206

10/18 Change 2.2u if necessary

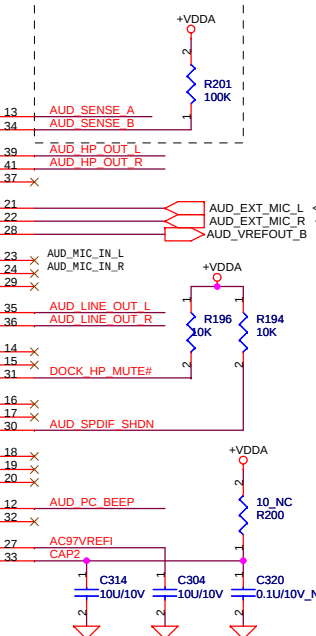
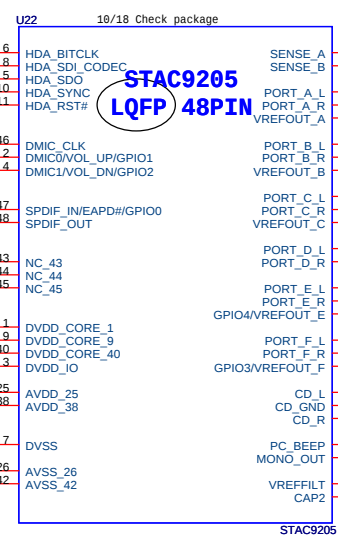
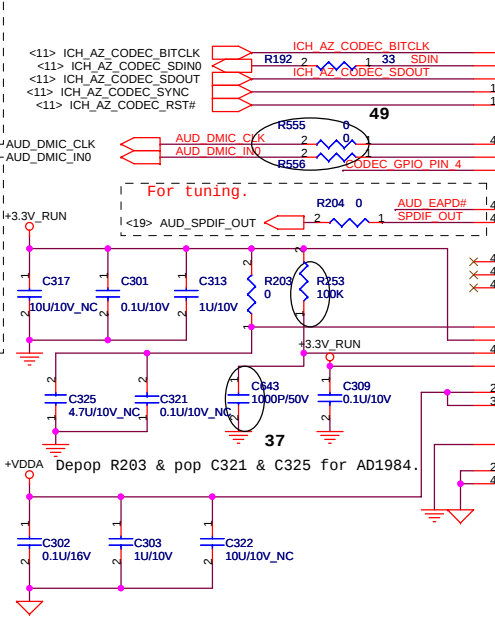
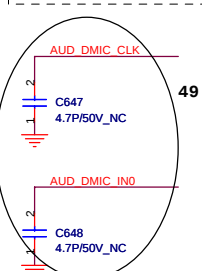
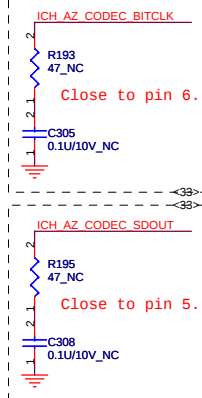
C370 47pF/50V NC



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

HDA_SDI_CODEC
HDA_SDO
HDA_SYNC
HDA_RST#

STAC9205
LQFP 48PIN



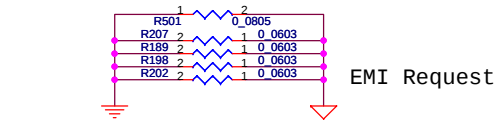
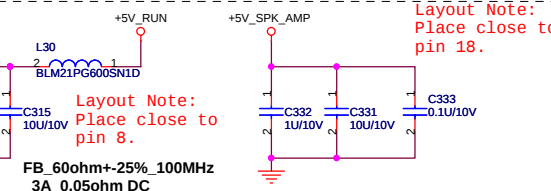
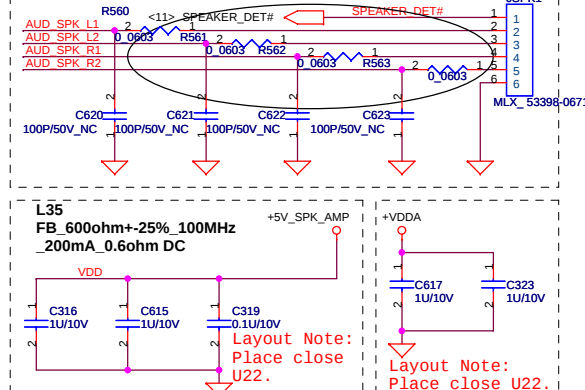
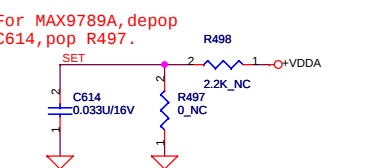
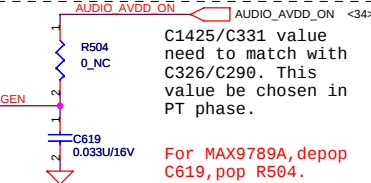
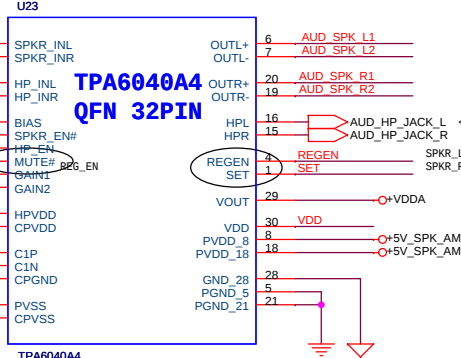
C304 must be 1U & Pop C320 & R200 for AD1984

U23

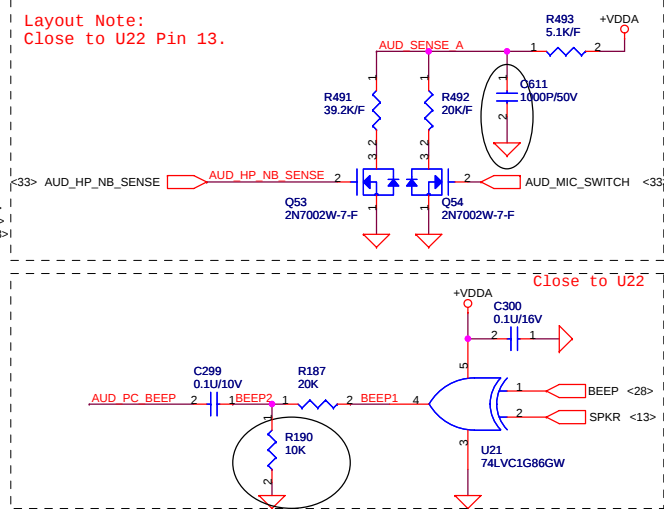
SPKR_INL
SPKR_INR

HP_INL
HP_INR

TPA6040A4
0FN 32PIN

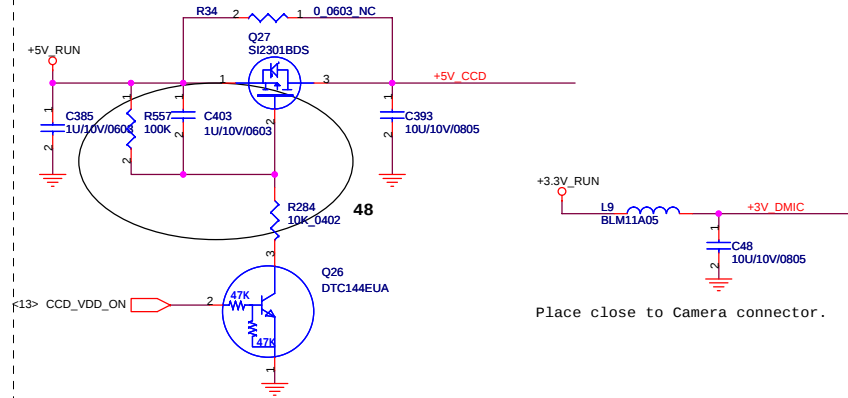


Layout Note:
Close to U22 Pin 13.

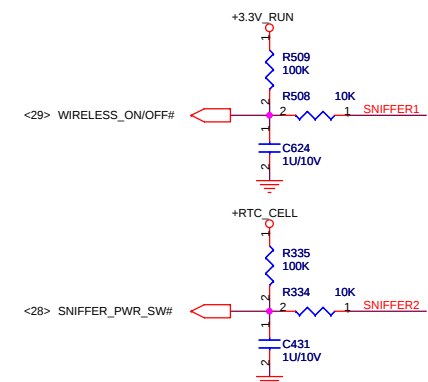
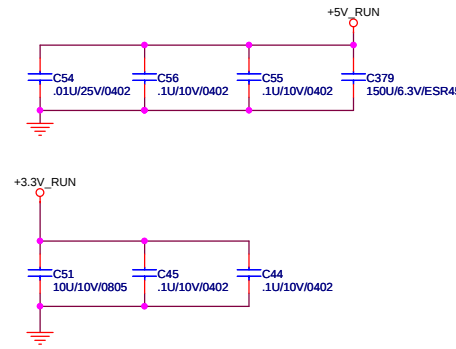
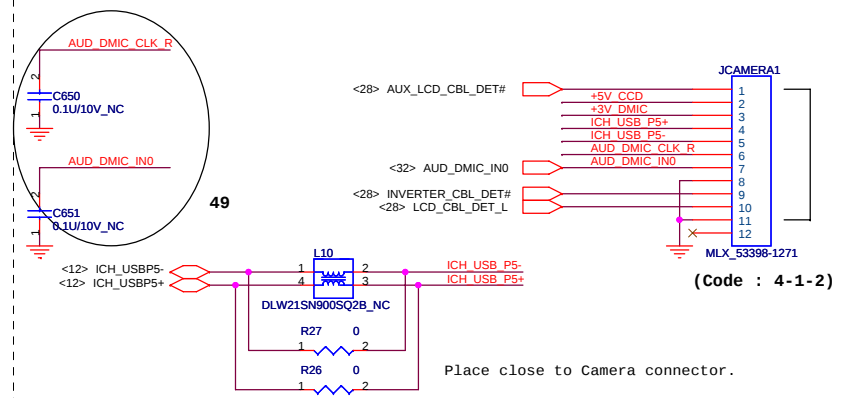
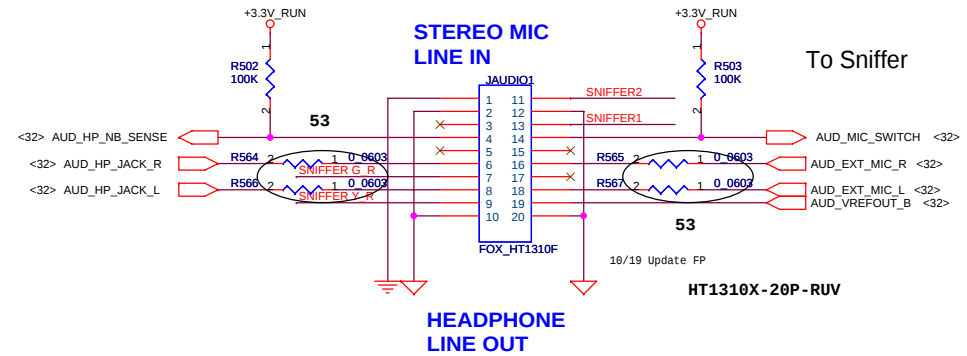


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Digital Microphone & Camera

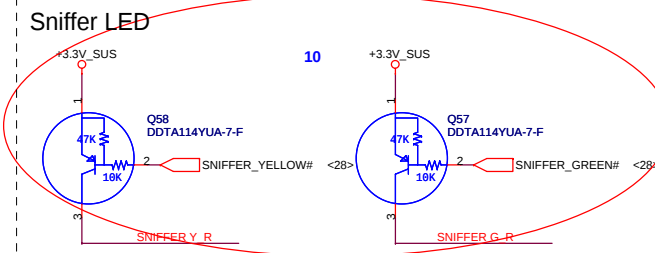
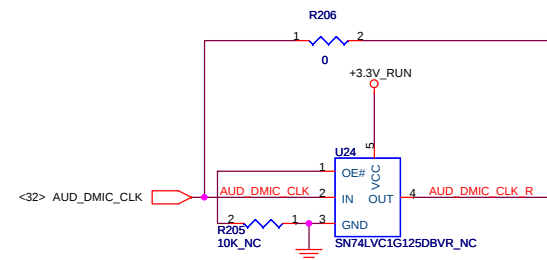
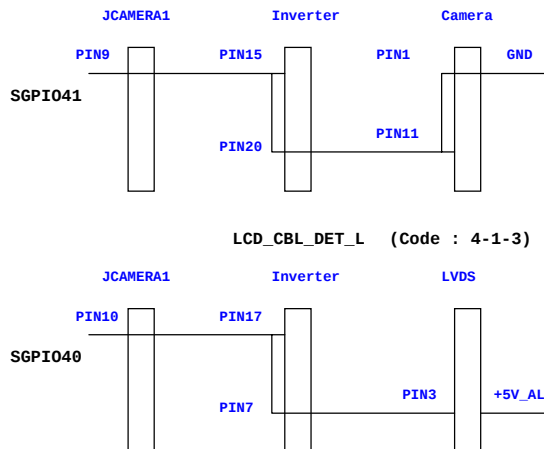


Update PN



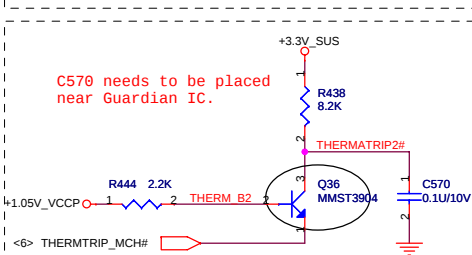
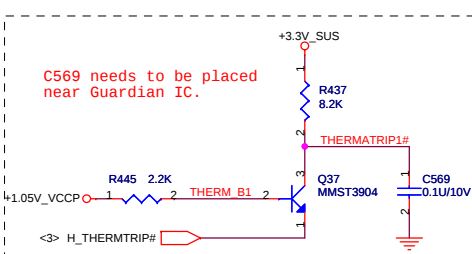
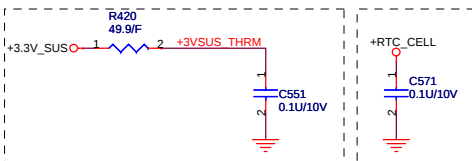
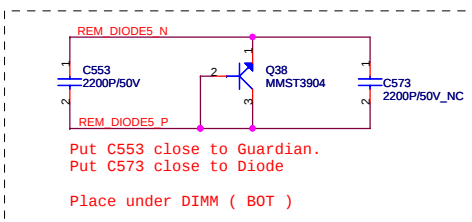
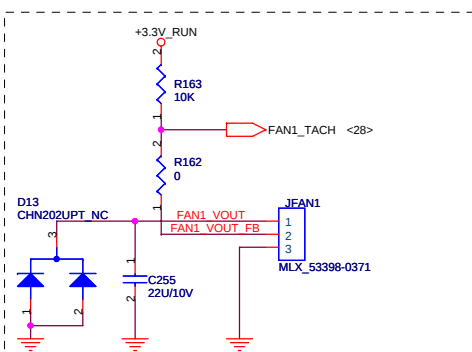
PAID

INVERTER_CBL_DET# (Code : 4-1-4)

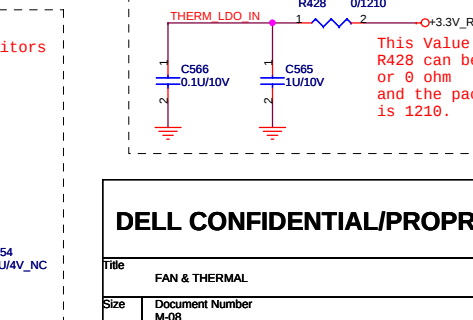
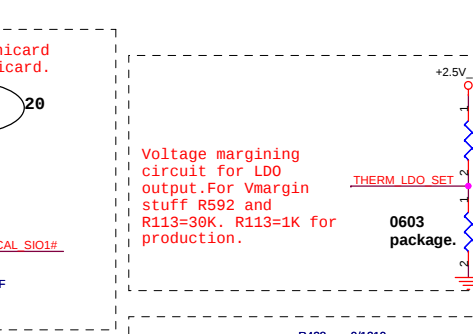
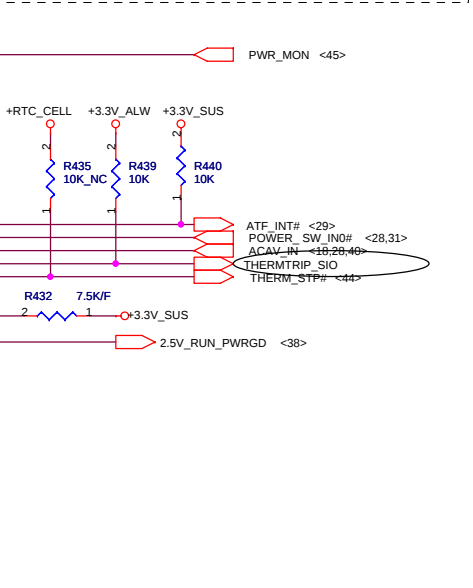
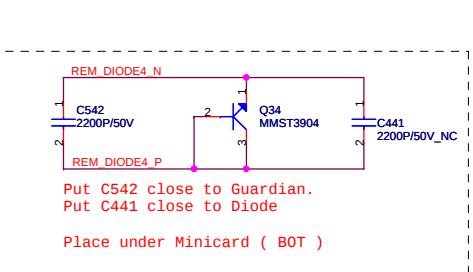
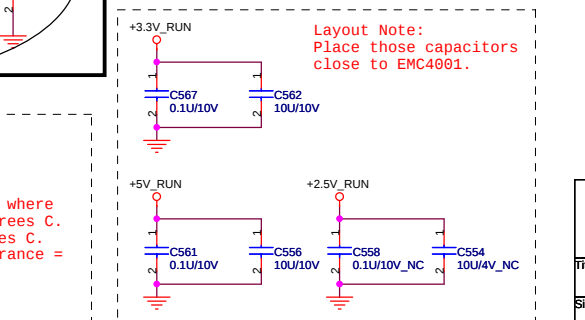
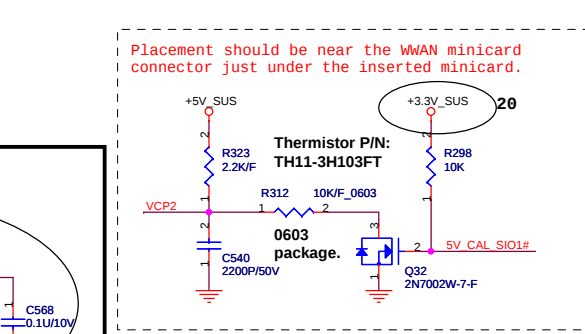
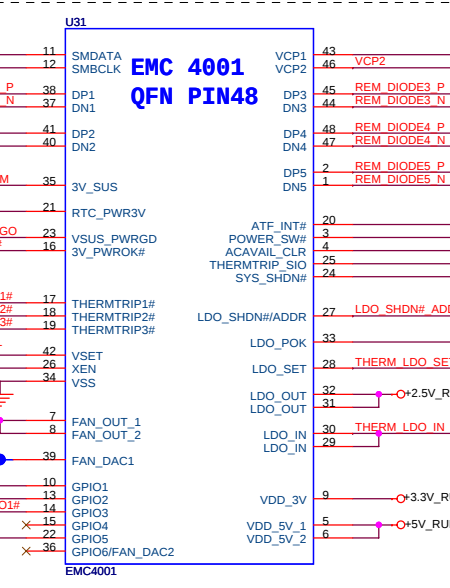
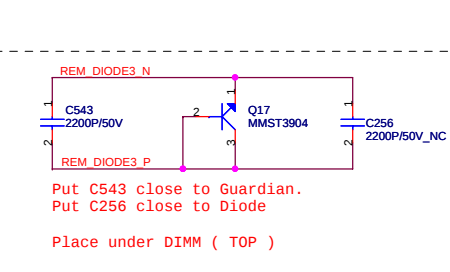
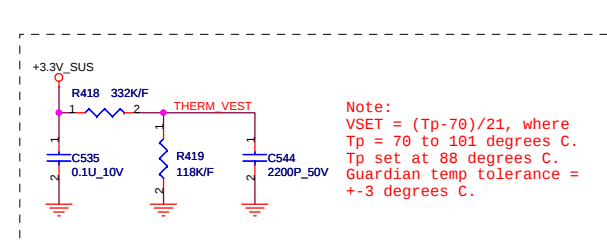
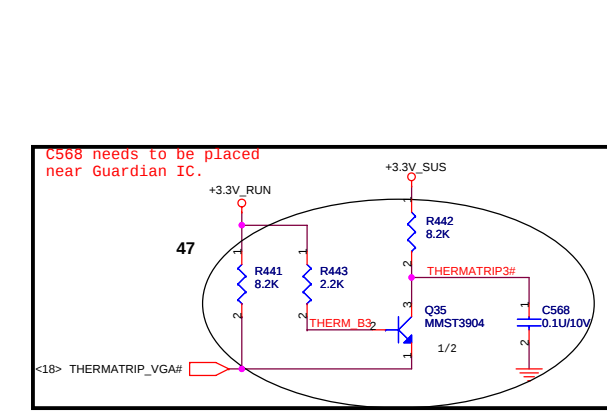
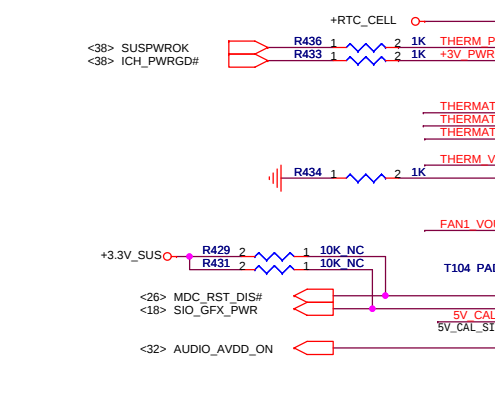
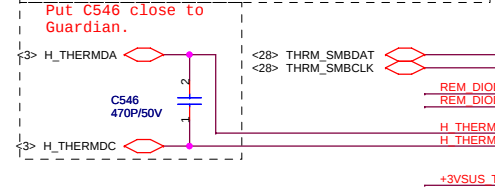
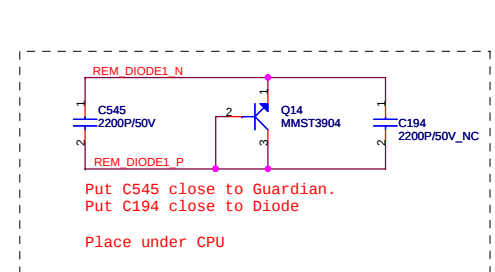


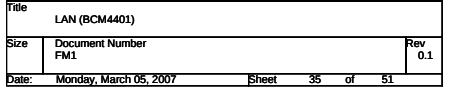
DELL CONFIDENTIAL/PROPRIETARY

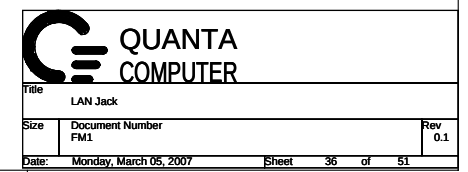
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AUDIO CONN		
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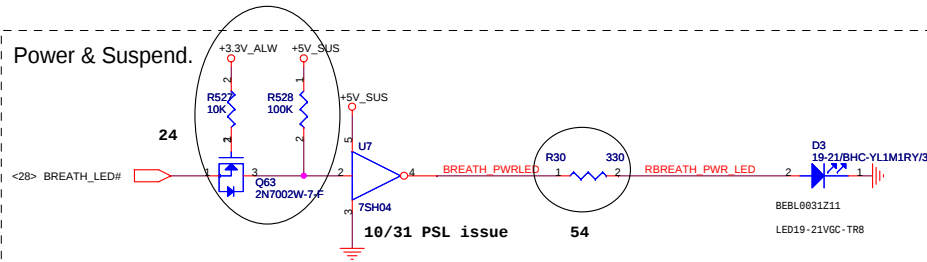
18/18 Check POP or Non-pop



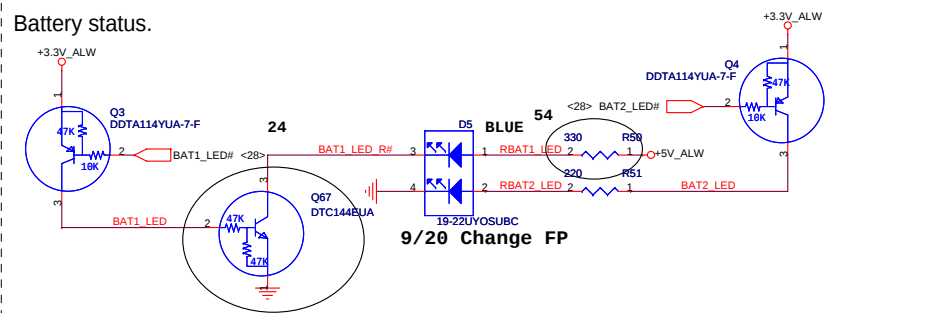




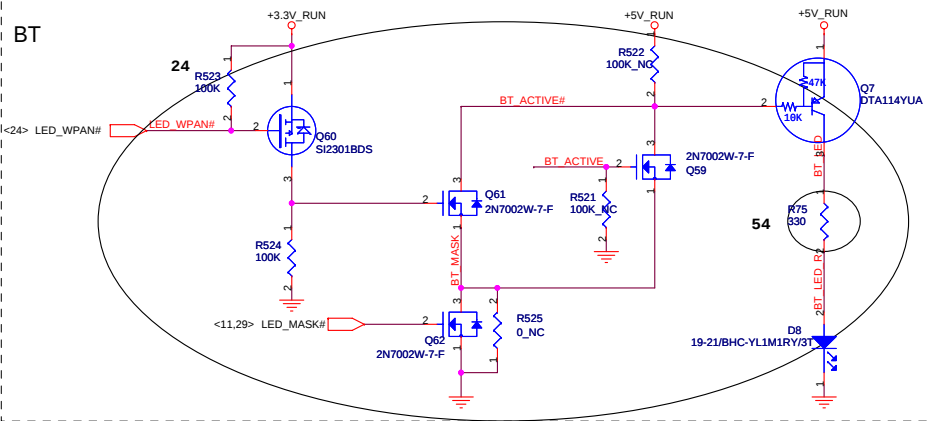
Power & Suspend.



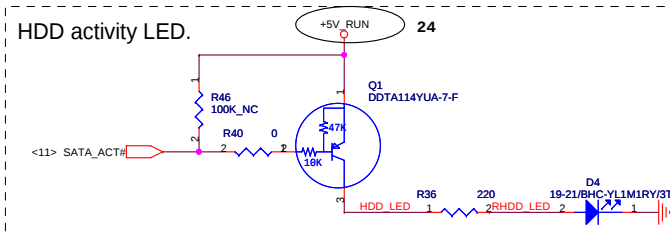
Battery status.



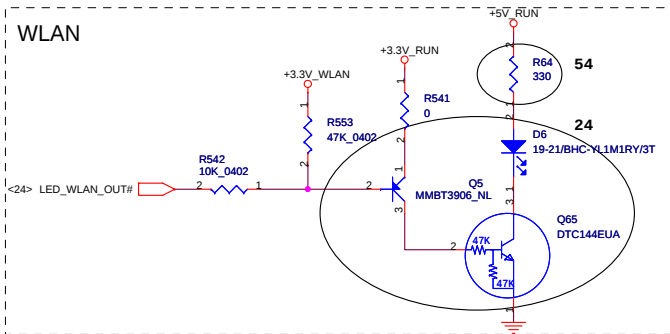
BT



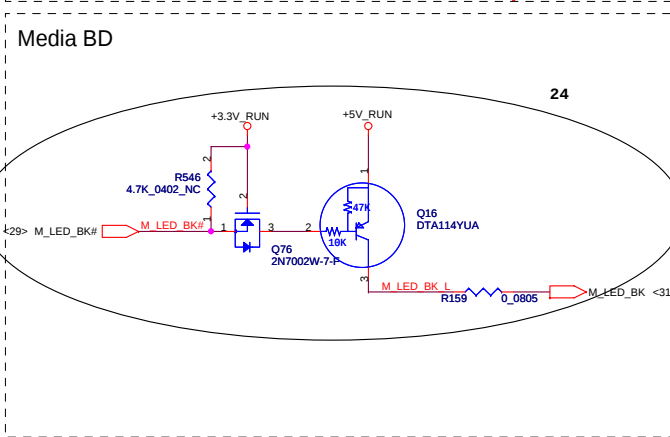
HDD activity LED.



WLAN

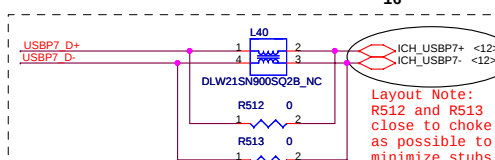
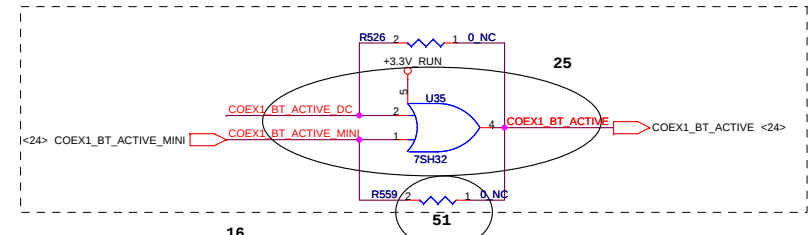
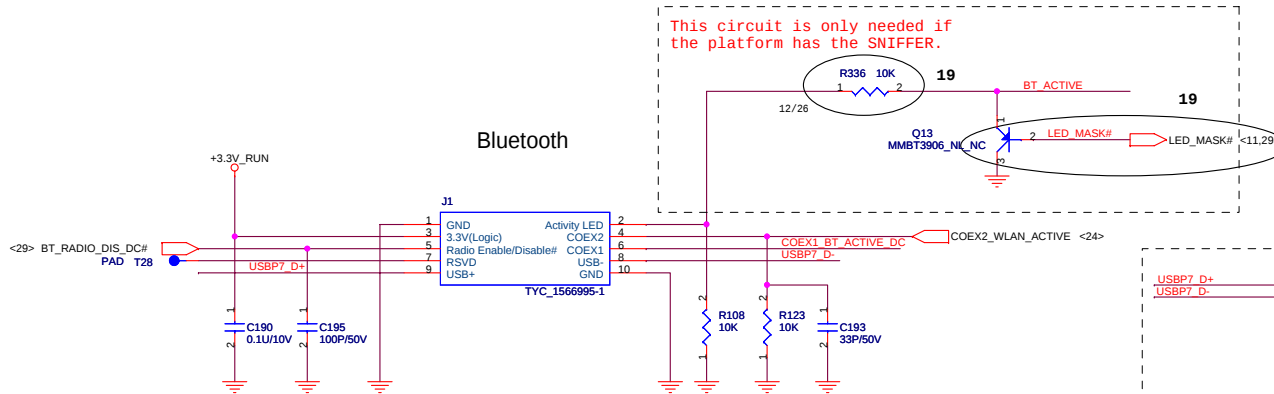


Media BD



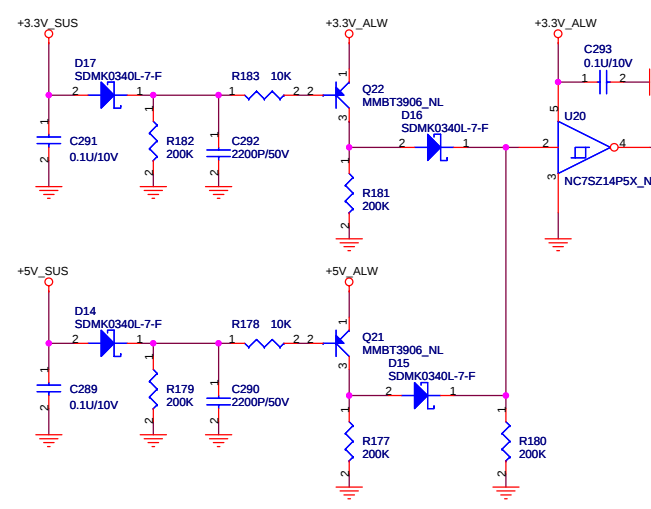
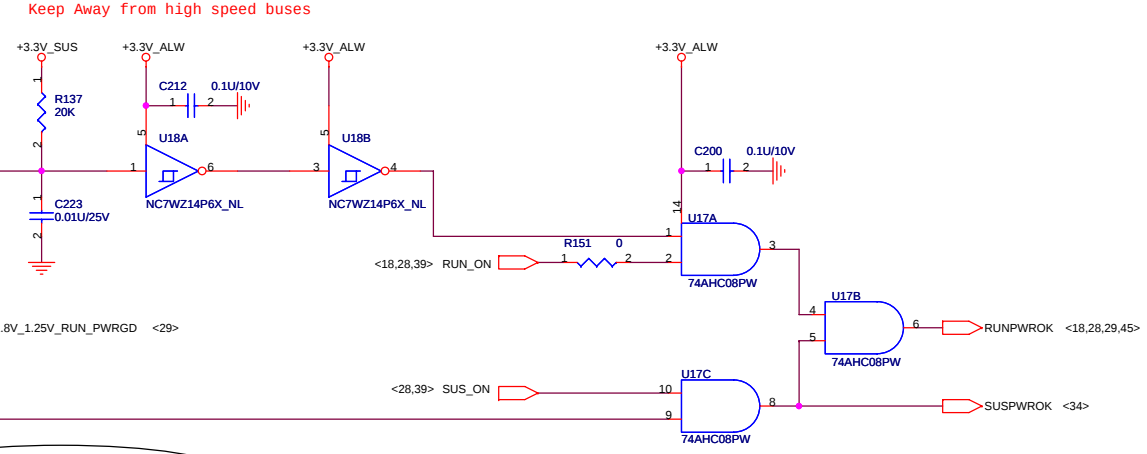
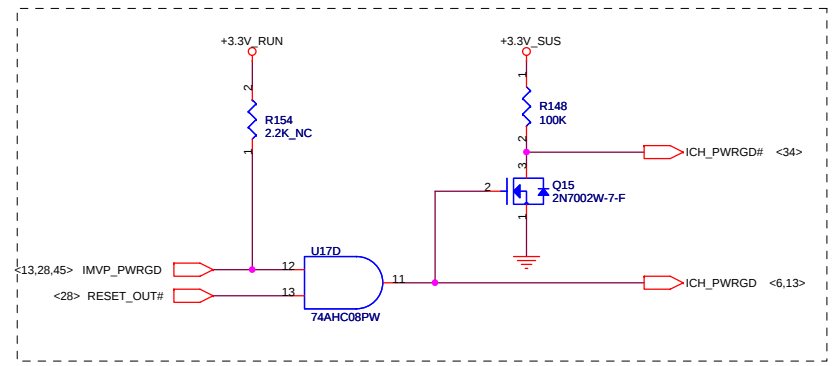
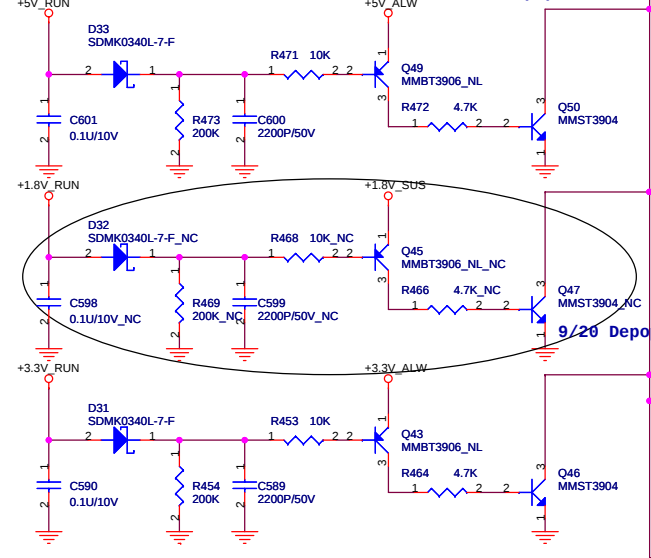
This circuit is only needed if the platform has the SNIFFER.

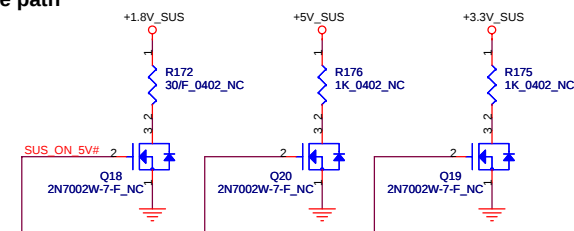
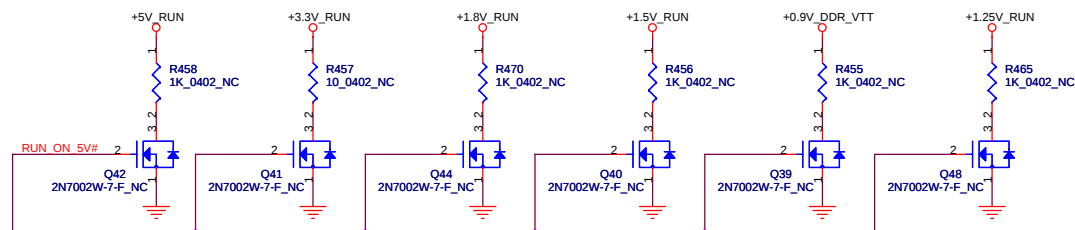
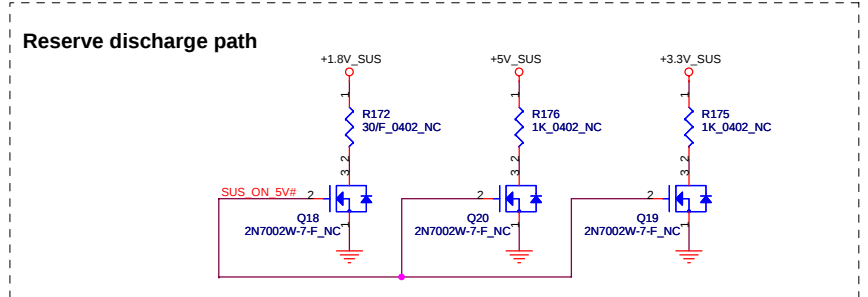
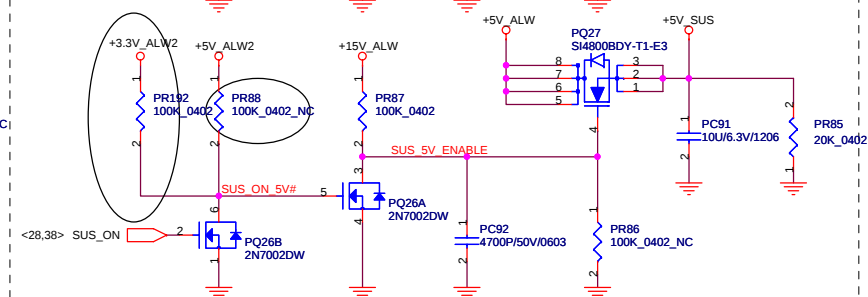
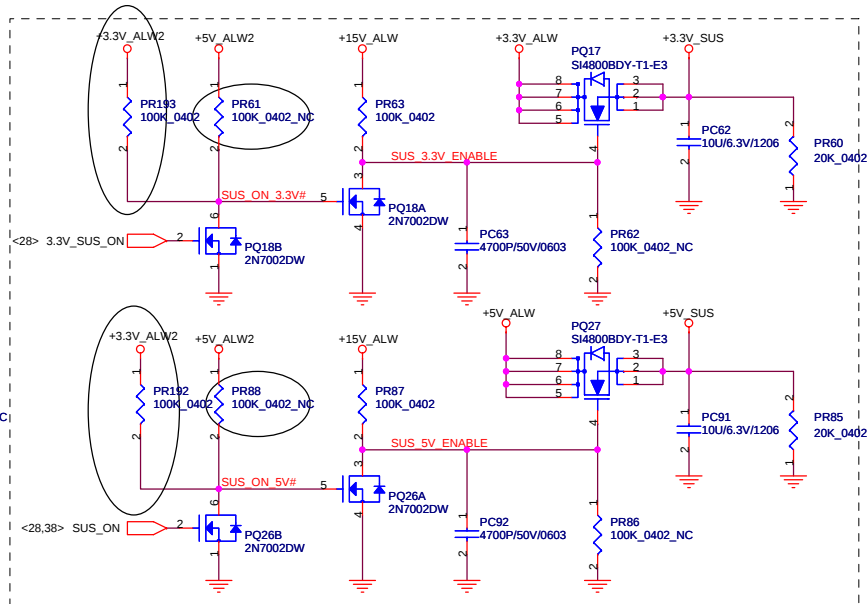
Bluetooth

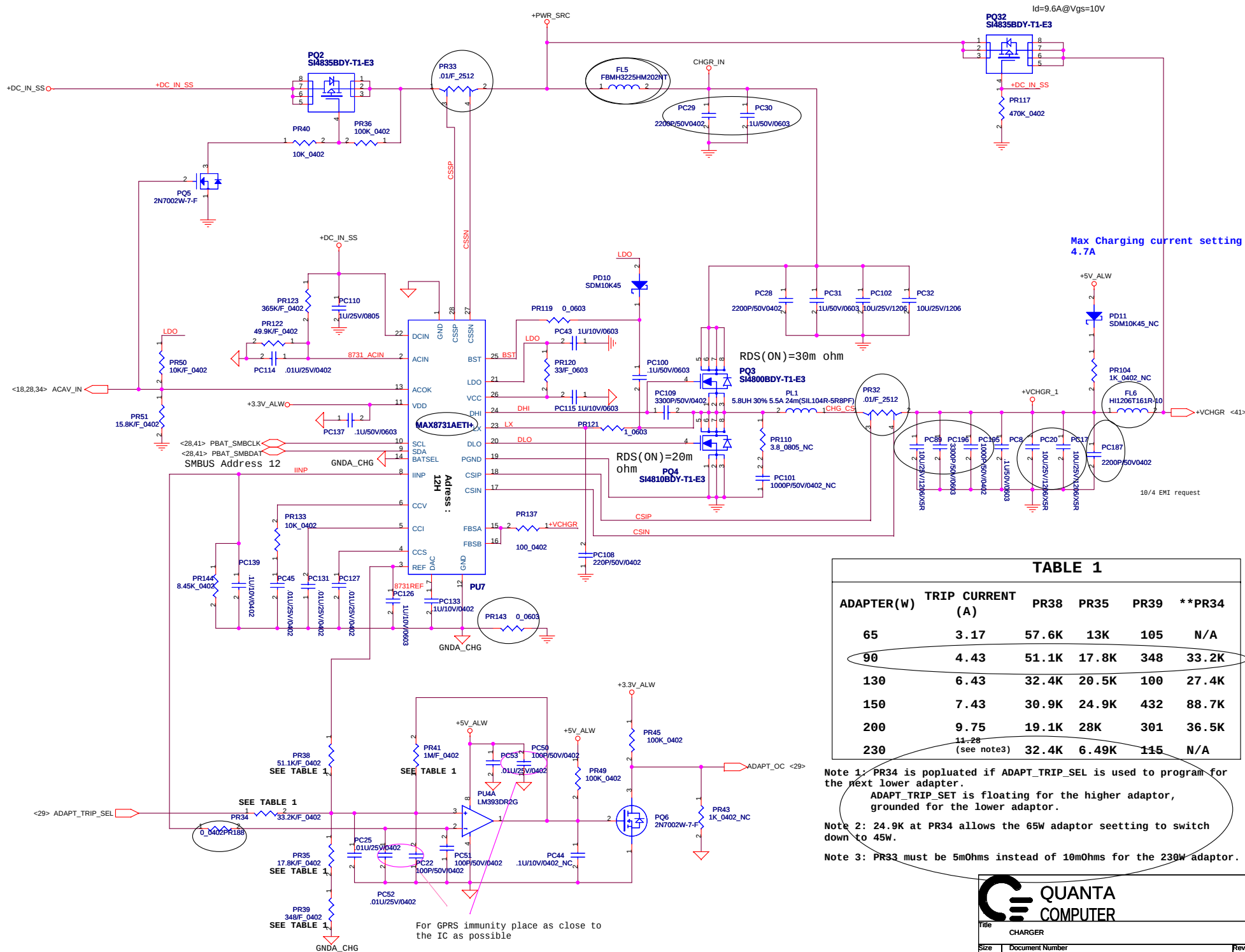


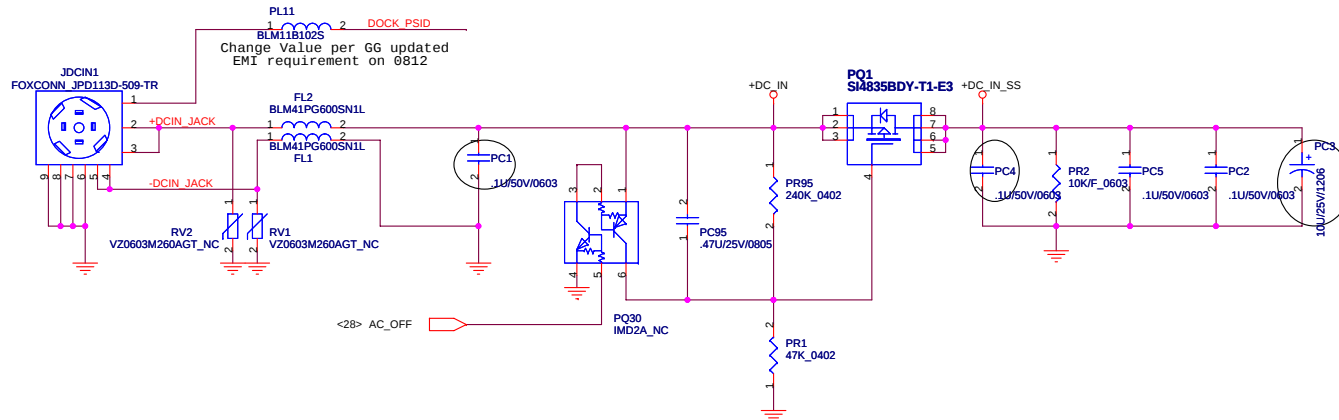
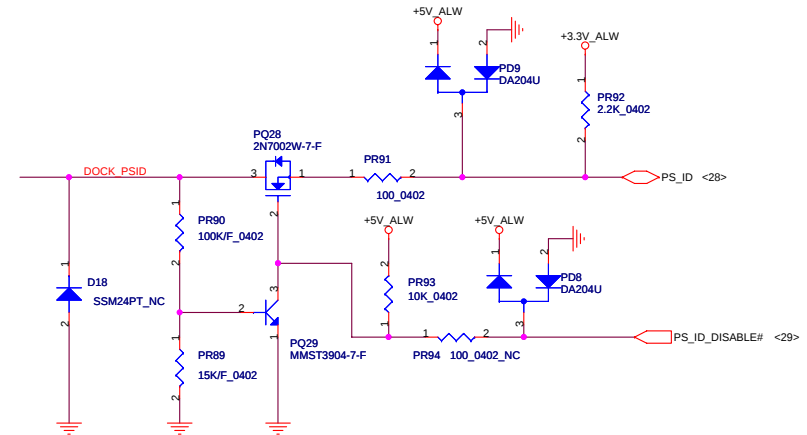
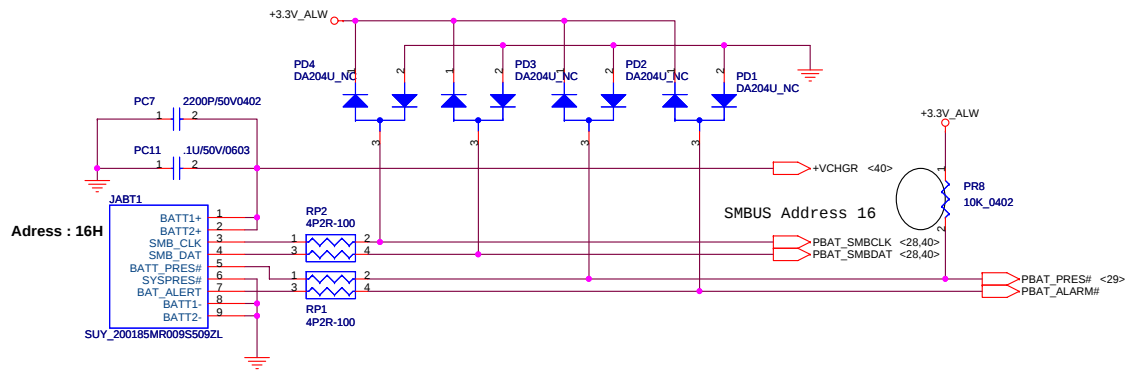
Non-iAMT

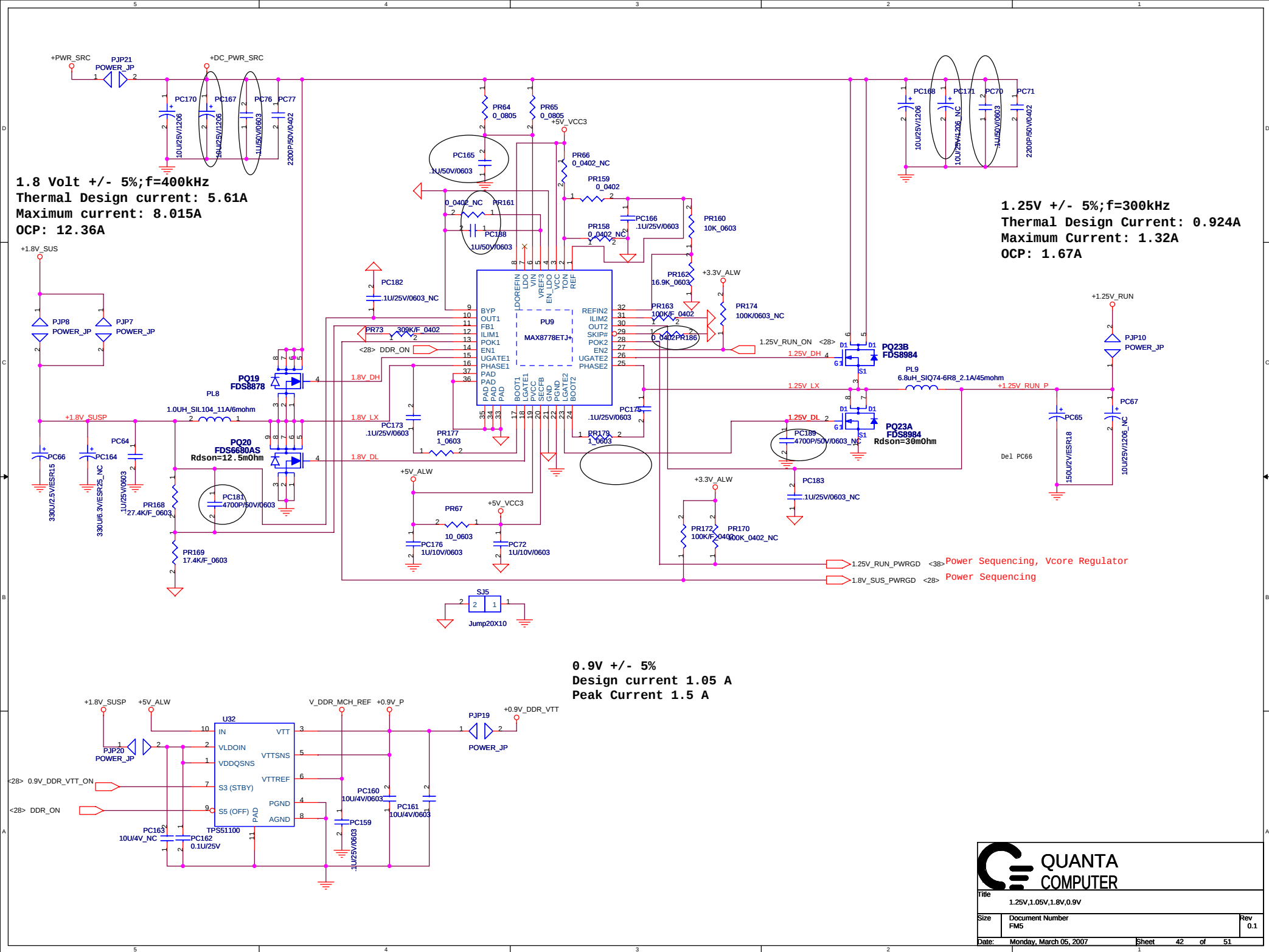
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 <34> 2.5V_RUN_PWRGD
 <18> GFX_PWRGD



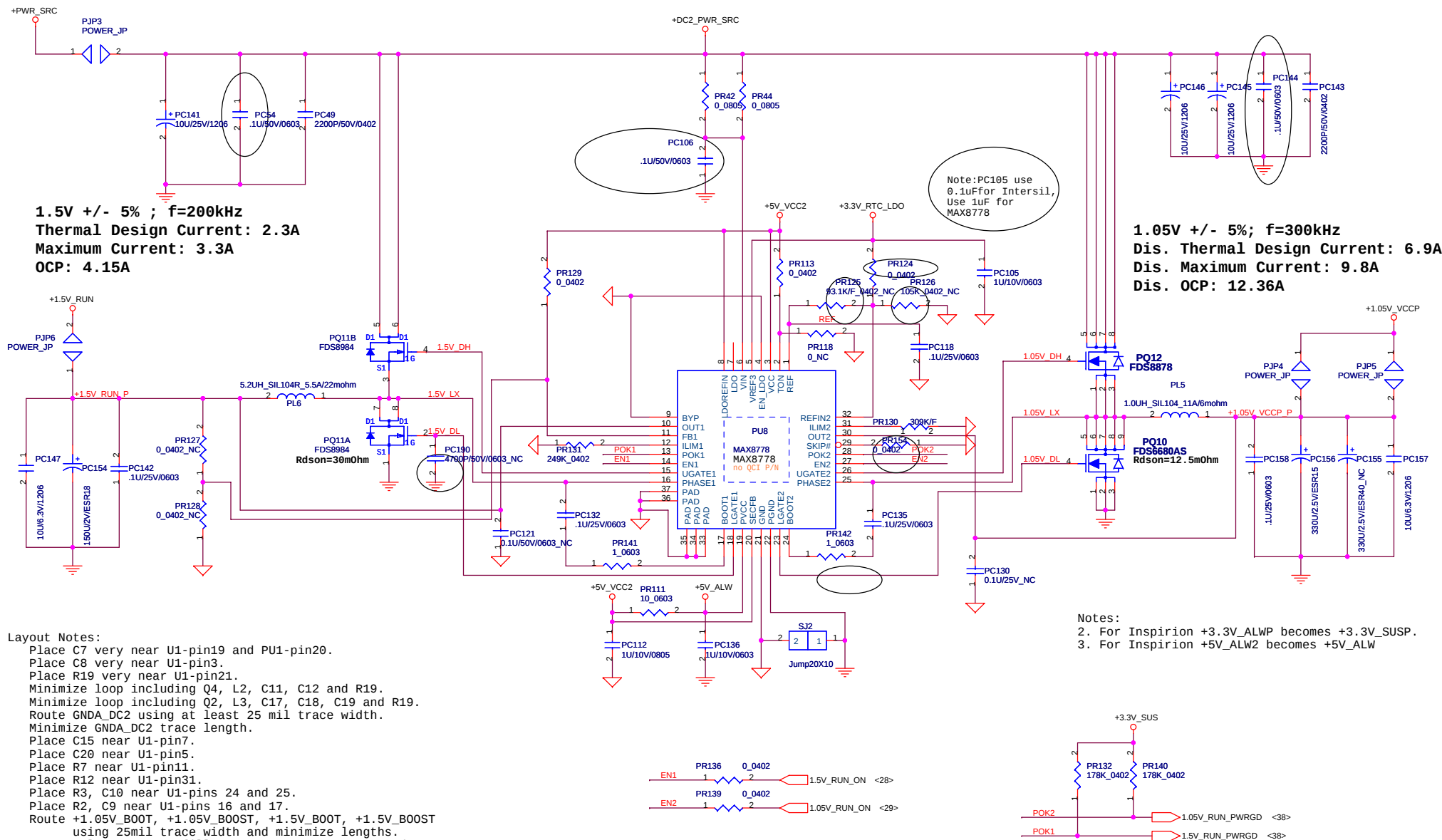








+1.5V_RUN /+1.05V_VCCP /+3.3V_ALW /+3.3_RTC_LDO

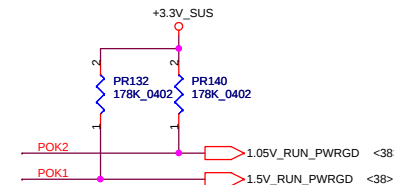


Layout Notes:

- Place C7 very near U1-pin19 and PU1-pin20.
- Place C8 very near U1-pin3.
- Place R19 very near U1-pin21.
- Minimize loop including Q4, L2, C11, C12 and R19.
- Minimize loop including Q2, L3, C17, C18, C19 and R19.
- Route GND_{DC2} using at least 25 mil trace width.
- Minimize GND_{DC2} trace length.
- Place C15 near U1-pin7.
- Place C20 near U1-pin5.
- Place R7 near U1-pin11.
- Place R12 near U1-pin31.
- Place R3, C10 near U1-pins 24 and 25.
- Place R2, C9 near U1-pins 16 and 17.
- Route +1.05V_{BOOT}, +1.05V_{BOOST}, +1.5V_{BOOT}, +1.5V_{BOOST} using 25mil trace width and minimize lengths.
- Connect large copper fill areas to PQ1, PQ2, PQ3 and Q4 signals for thermal improvement.
- Minimize length of +1.5V_{RUN_PL} and +1.05V_{VCCP_PL}.
- Place C1, C2, C3, C22 very near Q3-pins 5, 6, 7, 8.
- Place C4, C5, C6, C23 very near Q1-pins 5, 6, 7, 8.
- Route +DC2_PWR_SRC using 50 mil trace width and minimize length.
- Route OUT1 and OUT2 away from inductor and switch-node.
- Sense Vout directly at output bulk cap.

Notes:

2. For Inspirion +3.3V_ALWP becomes +3.3V_SUSP.
3. For Inspirion +5V_ALW2 becomes +5V_ALW



DC/DC +3V ALW/+5V ALW/+5V ALW2 /+15V ALW

Ton:OUT1/OUT2 Switching Frequency
VDD 200kHz/300kHz
OPEN (REF): 400kHz/300kHz
GND: 400kHz/500kHz

**Place these CAPs
close to FETs**

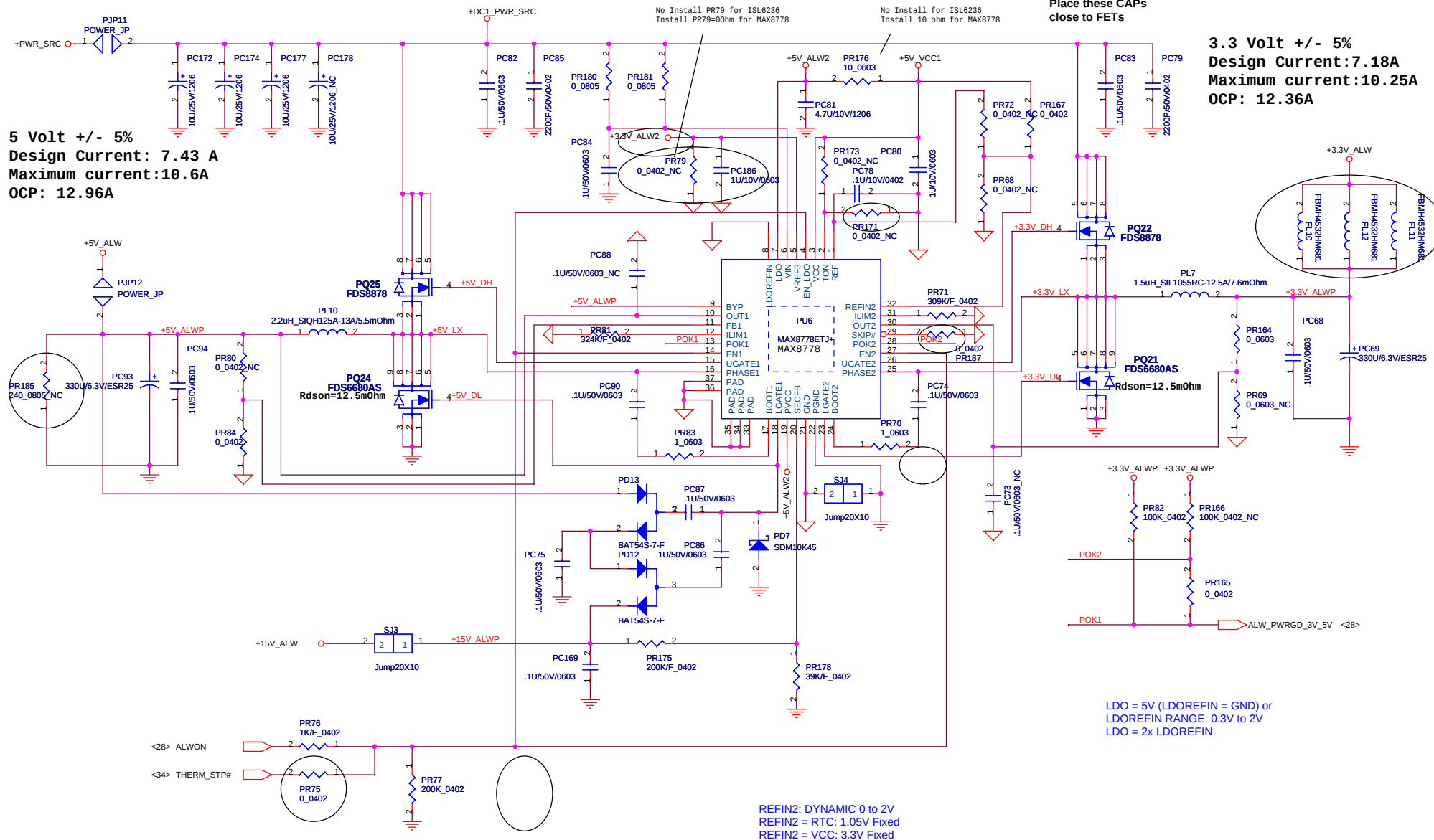
```
No Install PR79 for ISL6236
Install PR79=00hm for MAX8778
```

No Install for ISL6236
Install 10 ohm for MAX8778

**Place these CAPs
close to FETs**

5 Volt +/- 5%
Design Current: 7.43 A
Maximum current: 10.6A
OCP: 12.96A

3.3 Volt +/- 5%
Design Current:7.18A
Maximum current:10.25A
OCP: 12.36A



LDO = 5V (LDOREFIN = GND) or
LDOREFIN RANGE: 0.3V to 2V
LDO = 2x LDOREFIN

REFIN2: DYNAMIC 0 to 2V
REFIN2 = RTC: 1.05V Fixed
REFIN2 = VCC: 3.3V Fixed



Title	3VALW,5V,3V, power on
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1A

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	OFF	ON
S5 S4/AC	ON	OFF	OFF	OFF	ON
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	ON

PCI TABLE

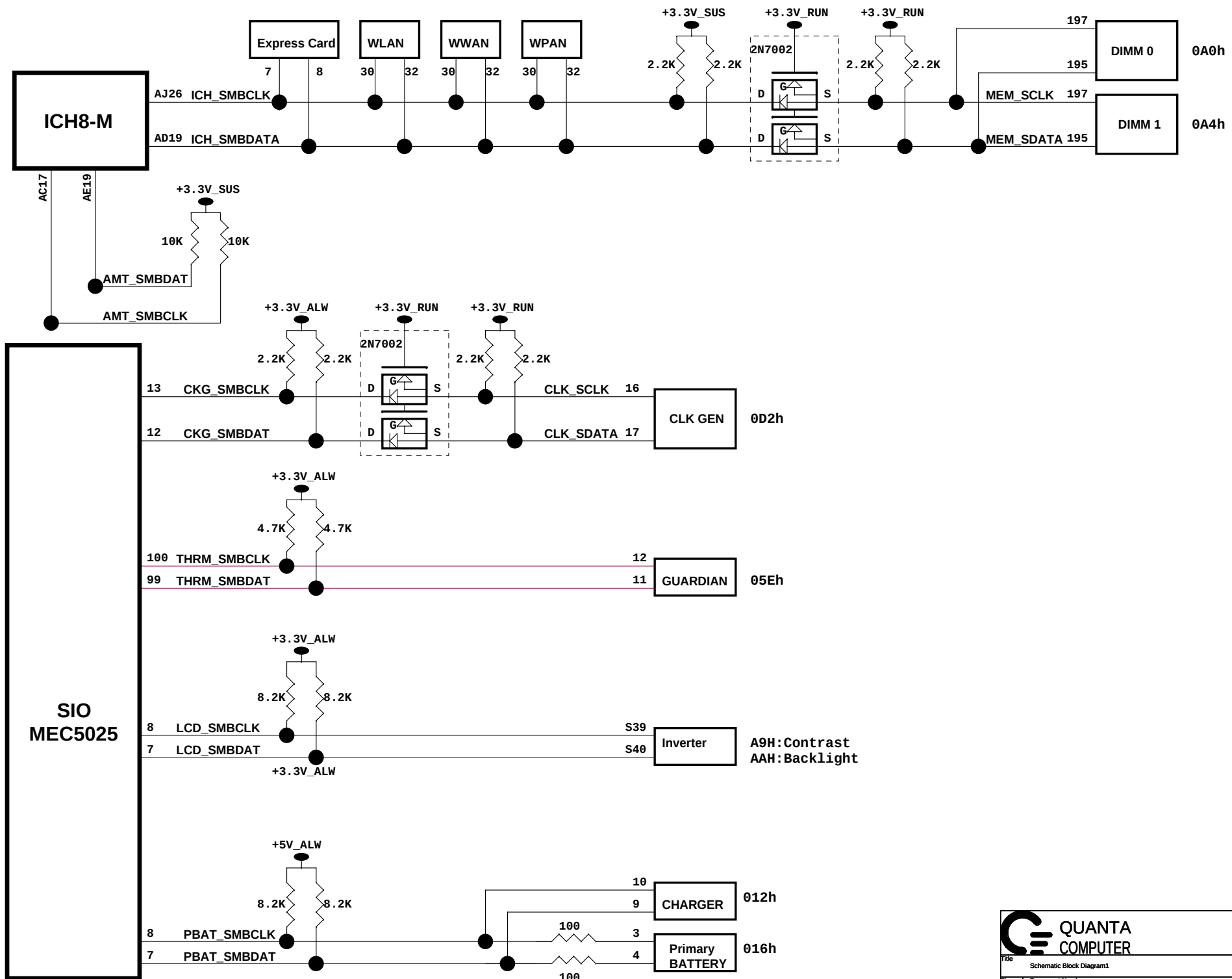
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
BCM4401B	AD16	REQ#0 / GNT#0	PIRQB
R5C833	AD17	REQ#1 / GNT#1	PIRQC: Card reader PIEQD: 1394

ICH8-M

USB PORT#	DESTINATION
0	Right Top
1	Right Bottom
2	Side TOP
3	Side Bottom
4	Ext. USB TOP
5	Digital Camera
6	Express Card
7	WPAN/Bluetooth
8	Ext. USB Bottom
9	WWAN
1	None
2	None
3	None
4	None

ECE 5011

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None



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C/G DISCRETE	1	39-45	7/13/2006					Update PWR schematics
	2	13,29	9/20/2006				S3 resume fail	Move PLTRST_DELAY# from EC to ICH8
	3	11	9/20/2006				2nd SATA HDD can't recognize	Move 2nd SATA from port 1 to port 2
	4	38	9/20/2006				Gfx card timing error	Disconnect GFX_PWRGD to system (Delete R463)
	5	38	9/20/2006				Gfx card timing error	Disconnect +1.8V_RUN detect circuit to system (Delete Q47)
	6	39-45	9/21/2006					Update PWR schematics
	7	23	9/21/2006					Add +1.8V_RUN for SATA buffer test (CON4.20-21-22-42-43-44)
	8	37	10/2/2006				Update WLAN LED implementation.With the current implementation, there is a possibility for backdrive from the WLAN LED control signal to +3.3V_RUN while in S3 / S4 / S5. With the voltage rail being +3.3V_WLAN, there is a high probability that the LED will be illuminated while in S3 / S4 / S5.	Please change the WLAN LED implementation to advice from Dell.
	9	13	10/2/2006				Intel has advised that the pull-up on LINKALERT# be depopulated and that the pull-up on GPIO14 be 8.2k. Please update.	Depop R247 & change R227 from 10K ohm to 8.2K ohm
	10	28,33	10/11/2006				In order to leverage the M07 implementation, the sniffer LED circuit needs to be modified. The MEC5025 pins are being changed from active high to active low.	Change back VC08 design, rename SNIFFER_YELLOW to SNIFFER_YELLOW#, SNIFFER_GREEN to SNIFFER_GREEN# and remove R507 and R510.
	11	28,29	10/11/2006				Move DOCK_SMB_PME from MEC5025 SGPIO37 to ECE5018/5011 GPIOC0.Move DOCK_SMB_ALERT# from ECE5018/5011 GPIOC0 to MEC5025 SGPIO37	DOCK_SMB_PME# should be pulled up to +3.3V_ALW DOCK_SMB_ALERT# should be pulled up to +5V_ALW
	12	28,38	10/11/2006				Add ATI_Intel to MEC5025 pin 14 and tie to GND.This connection should be labeled ATI_Intel.	Remove 3.3V_LAN_PWRGD circuit from page 38 Delete 3.3V_LAN_PWRGD from MEC5025 pin 14 Add a connection from the MEC5025 pin 14 and tie to GND.
	13	28	10/11/2006					Move ALW_PWRGD_3V_5V from MEC5025 pin 18 to pin 29
	14	13	10/11/2006					1) Move SIO_EXT_SCI# from ICH pin AG22 to ICH pin AC19 2) Delete R242 (delete DOCKED# signal)
	15	13	10/11/2006					Reserve LOM_SMBALERT# (ICH8 AG22) & PU resister
	16	24	10/16/2006					Change WPAN USB port from USBP7 to USBP4
	17	23,29	10/18/2006				Modify HDDC_EN and MODC_EN Circuits to Resolve Glitch Issue. unintentionally for a brief moment.With the current Dawson design, it has been shown that the +15V_ALW rail comes up before the +3V_ALW rail on the original HDDC_EN and MODC_EN circuits. This can cause a momentary glitch at the gate of the power FET, which may cause the FET to turn on unintentionally for a brief moment.	To resolve this issue, please use the HDDC_EN and MODC_EN circuits that are attached below. These new circuits resemble closely our other load switch circuits, but require an additional FET and changes the sense of the HDDC_EN and MODC_EN signals to active high. Please note the use of +5V_ALW2 on these circuits. The +5V_ALW2 voltage comes directly from the LDO output on the 3V/5V switcher in your M08 design.
	18	12,14	10/18/2006				WWAN Noise - ICH improvements. Add one .1 uF cap on each USB OC (over current) trace near the ICH. Add four .1uF caps in parellel to C813 close to the ICH pins. Add four .1uF caps in parellel to C825 close to the ICH pins.	Add C871~C878 for USB OC. Add C867~C870 in parellel to C825. Add C748,C864~C866 in parellel to C813.
	19	37	10/23/2006				Use LED_MASK# to control BT LED to prevent leakage	Add R336 & change Q13 to BJT
	20	34	10/23/2006				Change pull-up rail on 5V_CAL_SIO1# to +3.3V_SUS. Feedback from SMSC has indicated that the pull-up rail on 5V_CAL_SIO1# needs to change from +5V_SUS to +3.3V_SUS.This is necessary because the GPIO on the EMC4001 is 3V tolerant, not 5V.	Pullup is at reference designator R298.
	21	28	10/23/2006				Due to the power on defaults of the MEC5025, the pull-downs on the KSI lines of the MEC5025 need to be stronger, to avoid pulses from powering on certain power rails. Please do the following: 1. Change pull-down on SUS_ON to 2.7k 2. Change pull-down on RUN_ON to 2.7k	Change R355,R358 to 2.7K
	22	24	10/23/2006				Add SMBus isolation circuitry for WLAN.Add isolation circuitry for SMBus on WLAN.	
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C/G DISCRETE	23	17	10/26/2006				Chipset side spec. Differetial CLK raise/fall slew rate is 2.5~8 V/ns, only express card and mini card is 0.6~4V/ns. BITCLK rise/fall slew rate in 1-3 V/ns &	Change serial resistors (PR4,PR5,PR10,PR12,PR13) to meet the CLK SPEC
	24	37	10/26/2006				Change LED control method	
	25	37	10/26/2006				Add OR gate for BT_ACTIVE	
	26	13	10/26/2006				M08 GPIO A14 update. Original EC5011 pin66 CCD_VDD_ON move to IC8 pinAD10 GPIO48 and add 100K ohm pull down.	Move CCD_VDD_ON from EC5011 pin66to IC8 pin AD10 GPIO48 and add 100K ohm pull down.
	27	25	10/26/2006				For Comm team suggestion (GG list), pop C217 for WWAN	
	28	39 - 45	10/31/2006				PWR team updat schemtics - 10/23	

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C/G DISCRETE	29	24 - 25	11/1/2006				For EMI request, add RC circuit for Mini card clk request	Add R543, C880, R186, C649, R544, C181																
	30	39	11/1/2006				For +3.3V_RUN inrush current, it may over OCP (12.36 A)	Change PC58 from 470 pF to 6800 pF																
	31	32	11/3/2006				For AP - THN+D fail, change C306, 307 to 0.033uF/16V/X7R/1206 & C326, C329 to 1uF/16V/X7R/1206	Change C306, 307 to 0.033uF/16V/X7R/1206 & C326, C329 to 1uF/16V/X7R/1207																
	32	32	11/3/2006				'PO' noise in resume from S3,S4,S5	Reserved the AUD_AMP_MUTE# for 'PO' noise																
	33	39 - 45	11/09/2006				PWR team updat schemtics - 11/08																	
	34	17	11/09/2006				Change R44 to 2.2K per Intel recommend value.																	
	35	12 - 13	11/21/2006				Due to Intel-ICH8 uses GPIO20 pin AE11 as an Internal Strapping at power up	Move PCIE_MCARD2_DET# from GPIO20 to ICH8 GPIO5/PIRQH# pin B3.																
	36	13	11/21/2006				GPIO18 is default as an output at power up, it will drive 1Hz output at power up. Per Intel this GPIO could not be connected to GND	Add 4.7K series - R547 resistor to separate it																
	37	32	11/22/2006				There is potential back drive from the codec DVdd back to the AVdd supply due to an internal ESD diode	add 100kohm resistor (R253) between pin 40 and +3.3V_RUN and a 1000pF cap (C643 below) from Pin 40 to ground																
	38	35 - 36	11/28/2006				GG list -- COMM team request	1.Change capacitor for U5 pin 79, 94,106 (VDDIO) (C18, C16, C25) to 47pF. 2.Change those three capacitors (C27, C37,C34) to 47pF 3.Add C644 - 47pF capacitor by the pin 57 of U5 4.Change L7 to 0805 package -BK2125LM152. & C23 to 47 pF 5.Add Ferrite Bead BK1608LM152 on 1.8V to EPHY_AVDD pin 57																
	39	28-29	11/28/2006				Move DOCK_SMB_PME from MEC5025 SGPIO37 to ECE5018/5011 GPIOC0.Move DOCK_SMB_ALERT# from ECE5018/5011 GPIOC0 to MEC5025 SGPIO37	DOCK_SMB_PME# should be pulled up to +5V_ALW DOCK_SMB_ALERT# should be pulled up to +3.3V_ALW																
	40	24	12/01/2006				GG list -- Seperate debug port with MINI-PCI if not necessary	Add 4 0ohm resistors for these pins																
	41	24 - 25	12/01/2006				GG list -- Delete decoupling cap	Delete C222 & C424																
	42	39 - 45	12/04/2006				PWR team updat schemtics - 12/04																	
	43	32	12/08/2006				GG List -- Change audio AMP to TI solution	1.Change codec to TPA9040A4 2.Pop R505, C619 & C614; depop R506, R504 & R497																
	44	31	12/13/2006				GG List -- Change power source for LED of dash board	Change JTP1.9 from +3.3V_RUN to +5V_ALW																
	45	39 - 45	12/19/2006				PWR team updat schemtics - 12/19																	
	46	28	12/25/2006				GG List -- Remove EC5025 pin15 GPIO4 AUD_AMP_MUTE# circuit.	NC R538																
47	34	12/25/2006				GG List -- Add THERMATRIP_VGA# function	Pop R441,442,443 and Q35, C568 for THERMATRIP_VGA# trip.																	
48	33	12/28/2006				Modify CCD power control soft start function	Change C403 , R284 connect method																	
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C/G DISCRETE	49	22	1/11/2006				XD card detect function error	
	50	29	1/11/2006				Base on A16 GPIO : Change net name from BID2 to CHIPSET_ID1	
	51	37	1/24/2007				Add 0ohm_NC(R571) resistor pad connected from Coex1_BT_Active_MINI to Coex1_BT_Active	
	52	32	1/24/2007				Audio solution for pass EMI 225MHz and 451MHz radiation emission test.	Added R560, R561, R562 and R563 on AUD_SPK_L1, AUD_SPK_L2, AUD_SPK_R1, AUD_SPK_R2 trace
	52	33	1/24/2007				Audio solution for pass EMI 225MHz and 451MHz radiation emission test.	Added R564, R565, R566 and R567 on AUD_LINE_OUT,AUD_HP_OUT
	53	13	1/24/2007				GG List -- CCD_ON pull down R258 100K NC.	
	54	37	2/5/2007				Blue LED brightness is too high	Change R30,R50,R75,R64 & R36 from 220 ohm to 330 ohm
	55	30	2/12/2007				Prevent SPI CLK overshoot/undershoot issue	Add C896 for RC circuit but not pop it
	56	39 - 45	2/12/2007				PWR team updat schemtics - 2/12	
	57	29	2/12/2007				GG List -- CIR function intermediate issue	ECE5021 pin7 PWRGD need to pull-down to GND with 0 ohm - Add R568 PD resistor & R569 series resistor (NC)
	58	44	3/1/2007				PWR team updat schemtics - 3/1	
	59	17	3/2/2007				Per TDC COMM team request - Change L65 to	Fine tune 14M CLK - Change R57 from 33 to 15 ohm & L65 to BLM18SG260
	60	04	3/2/2007				Per reliability issue - Move C98 to C249	De-pop C98 & pop C249