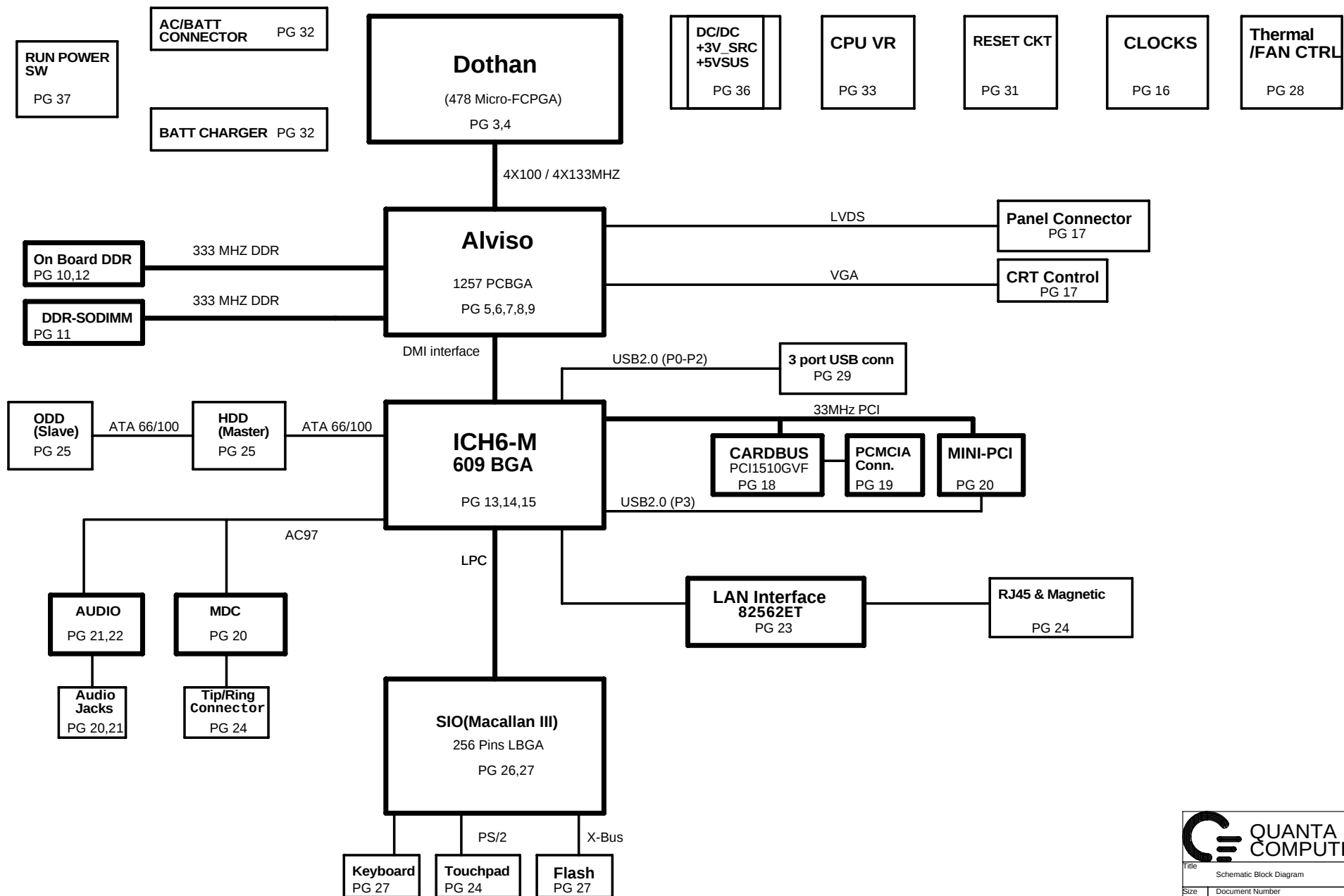


Tonga & Tyler (T2)

VER : 3C



Alviso Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-100 = Reversed 101 = FSB400 110-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I (Default)
CFG7	CPU Strap	0 = Prescott 1 = Dothan (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test Straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

ICH6-M Strapping Signals and Configuration		
Pin Name	Strap Description	Note
ACZ_SDOUT	0=PCI Express Port Config bit 1(default) 1=XOR Chain Entrance Test mode	
ACZ_SYNC	0=PCI Express Port Config bit 1(default) 1=Reserved	
DPRSLPVR	Reserved	This Signal should not be pulled high.
EE_CS	Reserved	This Signal should not be pulled high.
EE_DOUT	Reserved	This Signal should not be pulled low.
GNT[5]#/GPO[17]#	Boot BIOS Destination Selection	This functionality intended for debug/testing only.
GNT(6)#/GPO(16) #	0="Top block swap" mode 1=Normal(default)	"Top block swap" ICH6 inverts A16 for all cycles targeting FWH BIOS space
GPI0[25]	0=Enable Internal Vcc2.5V VRM(default) 1=Disable Internal Vcc2.5V VRM	This Signal has a weak internal PU during RSMRST# and is disabled within 100ms after RSMRST# deasserts.
INTVRMEN	0=Disable Internal VccSus 1.5V VRM(default) 1=Enable Internal VccSus 1.5V VRM	
LINKALERT#	Reserved	This Signal requires an external PU
REQ[4:1]#	XOR Test Chain Selection	
SATALED#	Reserved	This Signal should not be pulled low.
SPKR	0=Normal(default) 1=NO Reboot	This Signal should not be pulled high.
TP[3]	0=XOR Chain Entrance Test mode 1=Normal(default)	This Signal should not be pulled low unless using XOR Chain testing.

NOTE: All strap signals are sampled on the rising edge of the ICH6-M's PWORK signal.

For Dothan A stepping

	CPU		NB			CLOCK		
	BSEL1	BSEL0	CFG2	CFG1	CFG0	FS_C	FS_B	FS_A
100MHZ	0	0	1	0	1	1	0	1
133MHZ	0	1	0	0	1	0	0	1

For Dothan B stepping

	CPU		NB			CLOCK		
	BSEL1	BSEL0	CFG2	CFG1	CFG0	FS_C	FS_B	FS_A
100MHZ	0	1	1	0	1	1	0	1
133MHZ	0	0	0	0	1	0	0	1

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
PCMCIA controller	AD17	PIROA# PIRQC#	REQ1#/GNT1#
MINIPCI SLOT	AD19	PIROB# PIROD#	REQ3#/GNT3#

ICH6-M Integrated Pull-up and Pull-down Resistors

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPO[48], GNT[5]#/GPO[17], GNT[6]#/GPO[16], LAD[3:0]#/FB[3:0]#, LAN_RXD[2:0], LDRQ[1]/GPI[41], PME#, LDRQ[0], PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSTP#/TP[4], DPRSLPVR/TP[1], EE_CS, SPKR	ICH6 Internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

Power Name	Page#
+1_5V_LAN	P. 15
+1_5V_PCIE	P. 15
+1_5VRUN	P. 4, 8, 14, 15, 30, 37
+1_5VSUS	P. 15, 20, 30, 31, 35, 37
+2.5VRUN	P. 6, 8, 15, 17, 37
+2.5VSUS	P. 6, 8, 9, 10, 11, 12, 34, 37
+3V562ET	P. 23
+3VLAN	P. 14, 15, 20, 23, 24
+3V_SRC	P. 15, 23, 36, 37
+3VALW	P. 3, 17, 20, 24, 26, 27, 28, 30, 31, 32, 36, 38
+3VRUN	P. 3, 8, 11, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 24, 25, 26, 27, 28, 30, 31, 33, 37
+3VSUS	P. 3, 14, 15, 17, 18, 19, 20, 22, 24, 26, 28, 31, 34, 35, 36
+5VALW	P. 15, 17, 36, 37, 38
+5VRUN	P. 15, 17, 20, 21, 22, 24, 25, 27, 28, 30, 33, 37
+5VSUS	P. 15, 19, 20, 28, 29, 34, 35, 36, 37
+15V	P. 17, 28, 36, 37
+AVDD	P. 21
+DC_IN	p. 32

Power Name	Page#
+RTC_PWR3_3V	P. 26, 36, 38
+VCCP	P. 3, 4, 5, 6, 8, 9, 13, 15, 16, 28, 35, 37
+VCCRTC	P. 13, 15, 26, 28
CRTVCC	P. 17
DCIN+	P. 32
DC_IN+	P. 32
PBATT+	P. 32, 38
PWR_SRC	P. 17, 26, 30, 32, 33, 34, 35, 36, 37, 38
USBVCC0, USBVCC1, USBVCC2	P. 29
VHCORE	P. 4, 33

QUANTA
COMPUTER

Title

Dothan Processor (Host BUS)

Size

Document Number

Rev

VM7

2A

Date:

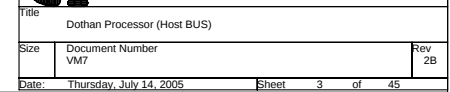
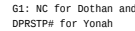
Thursday, July 14, 2005

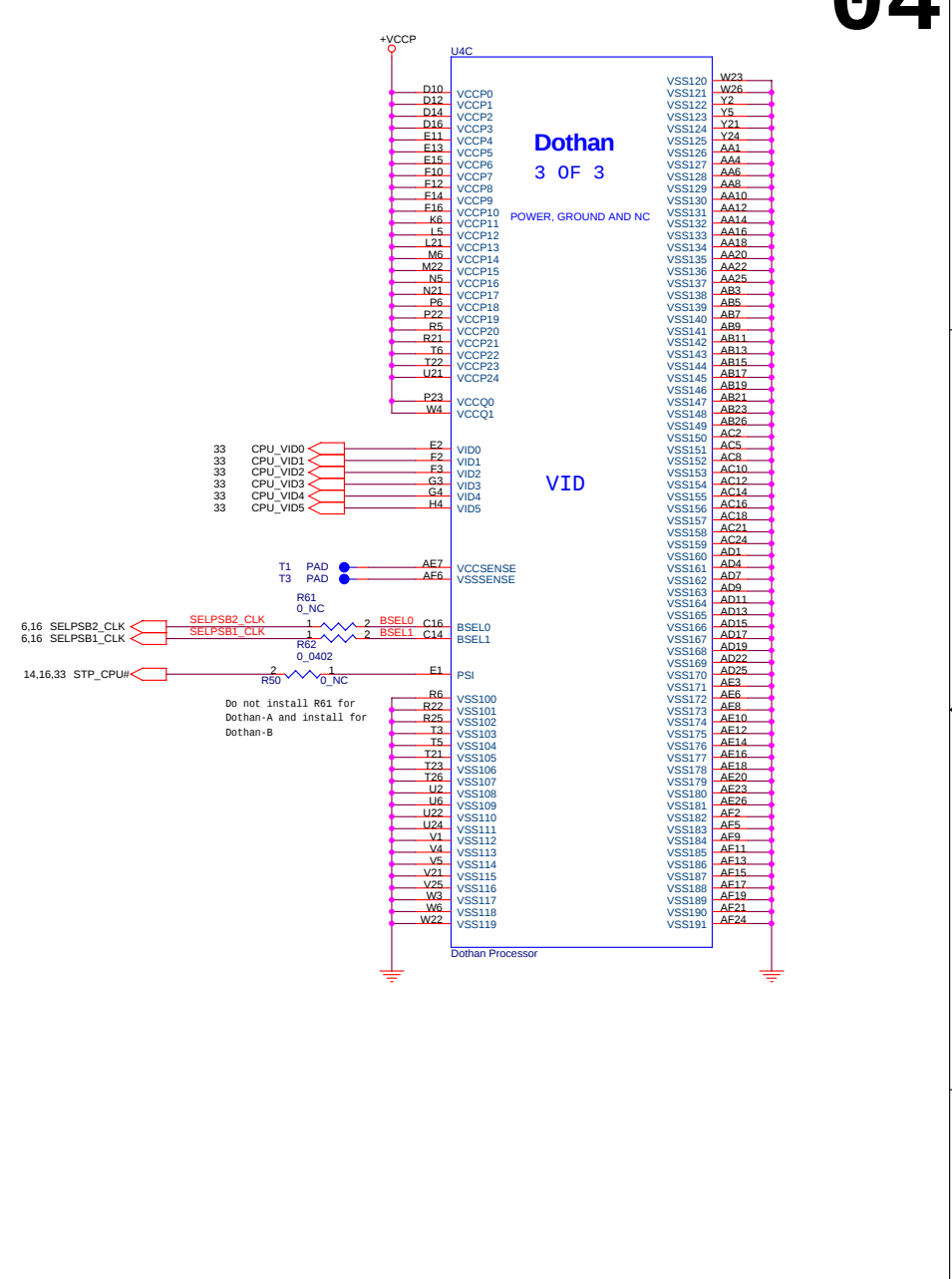
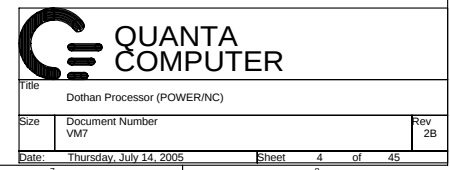
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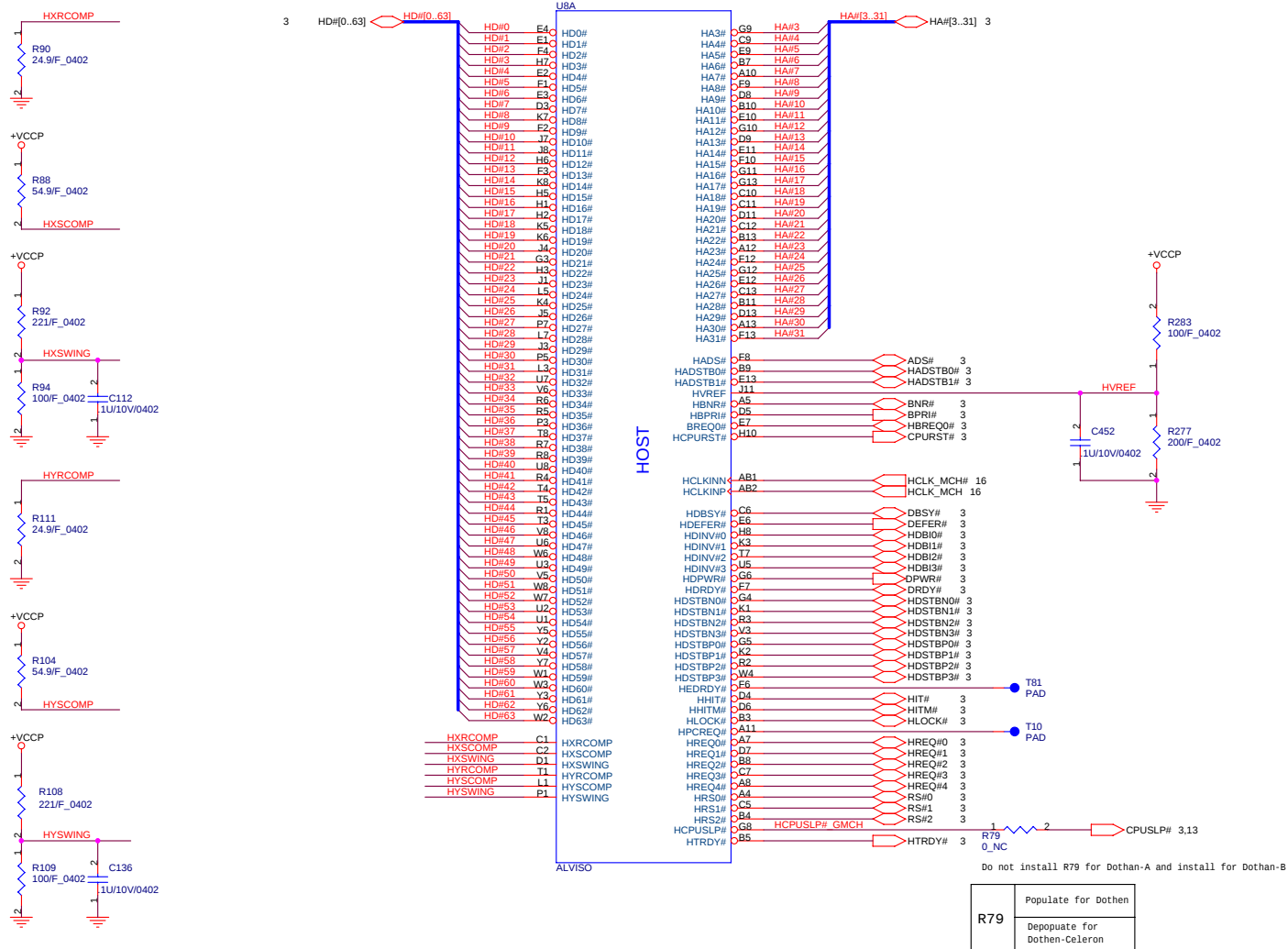
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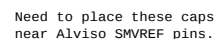
of

45



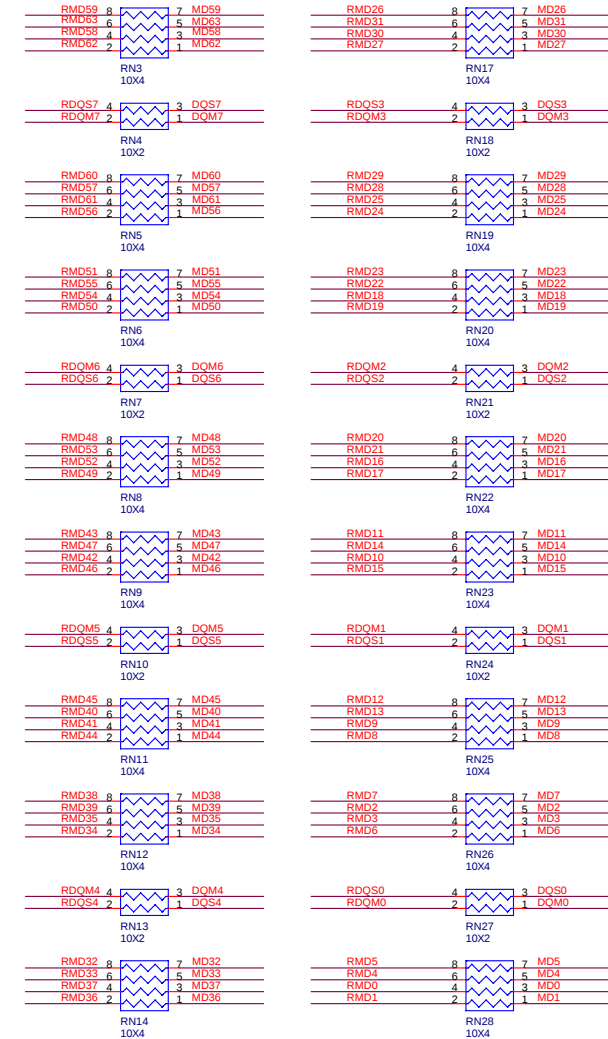
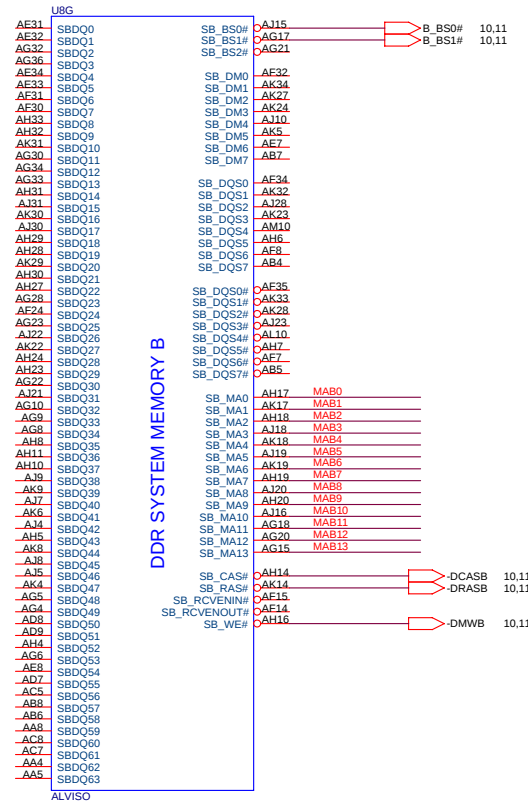
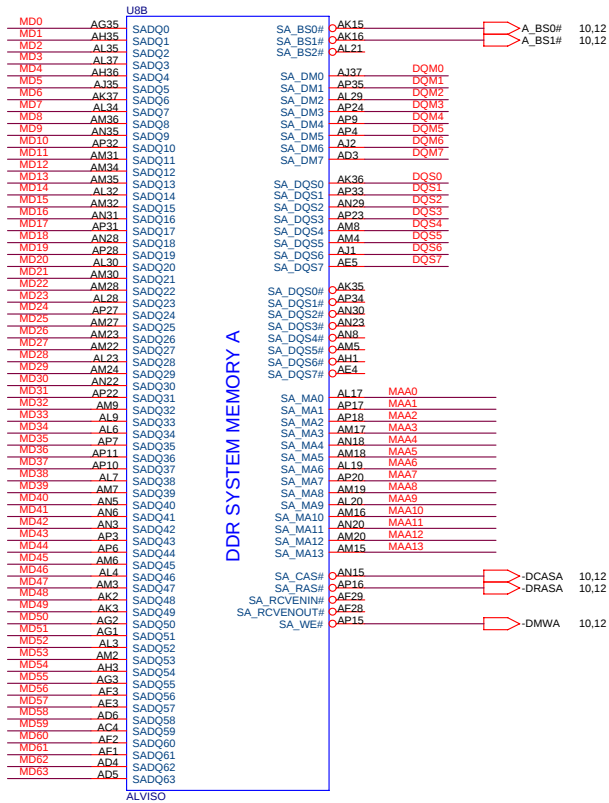
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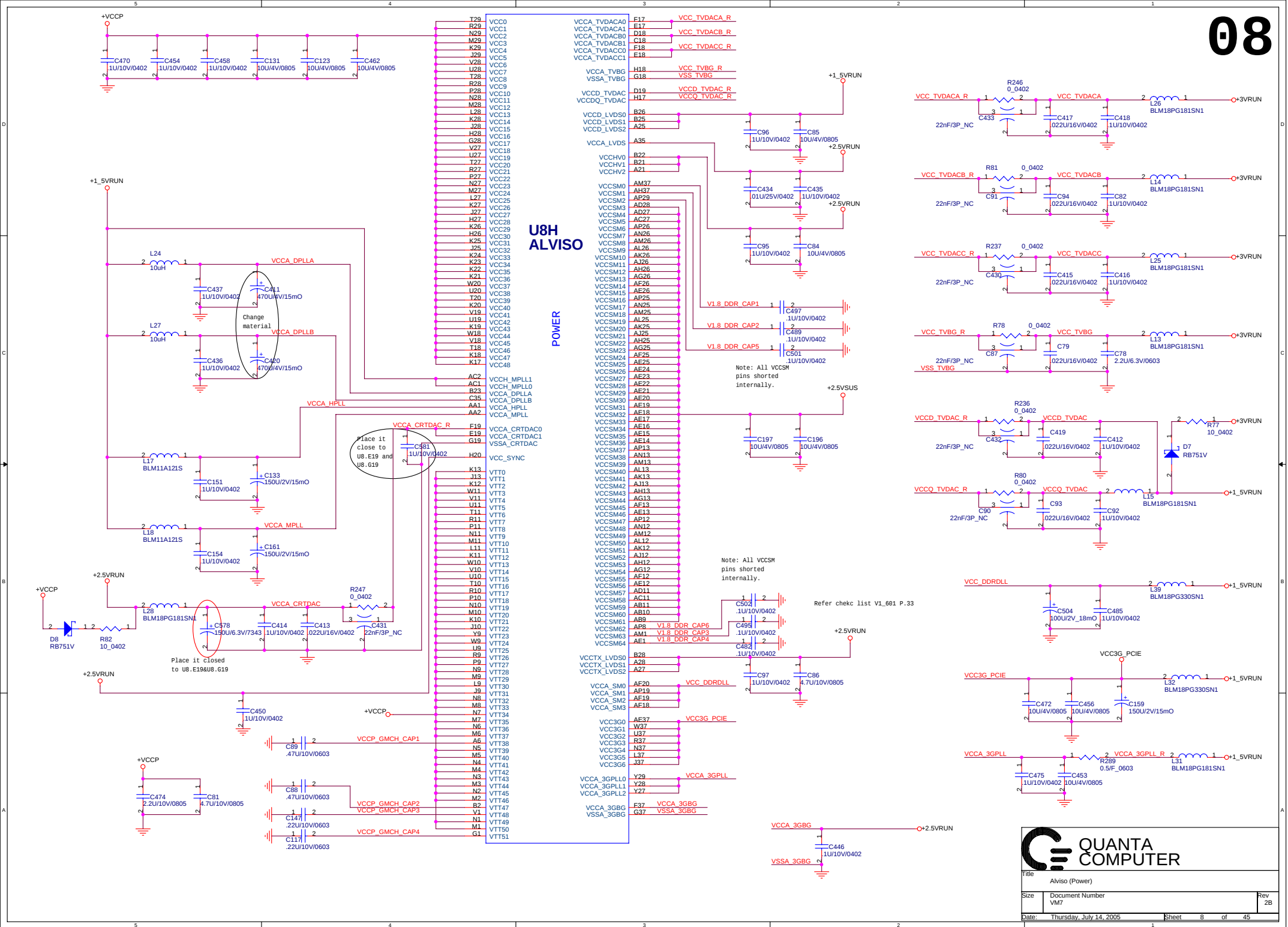




RMD[0..63] 10.11.12
RDQM[0..7] 10.11.12
RDQS[0..7] 10.11.12

MAB[0..13] 10.11
MAA[0..13] 10.12
CSA[0..3] 6,10,11,12
CKE[0..3] 6,10,11,12





U8E

ALVISO

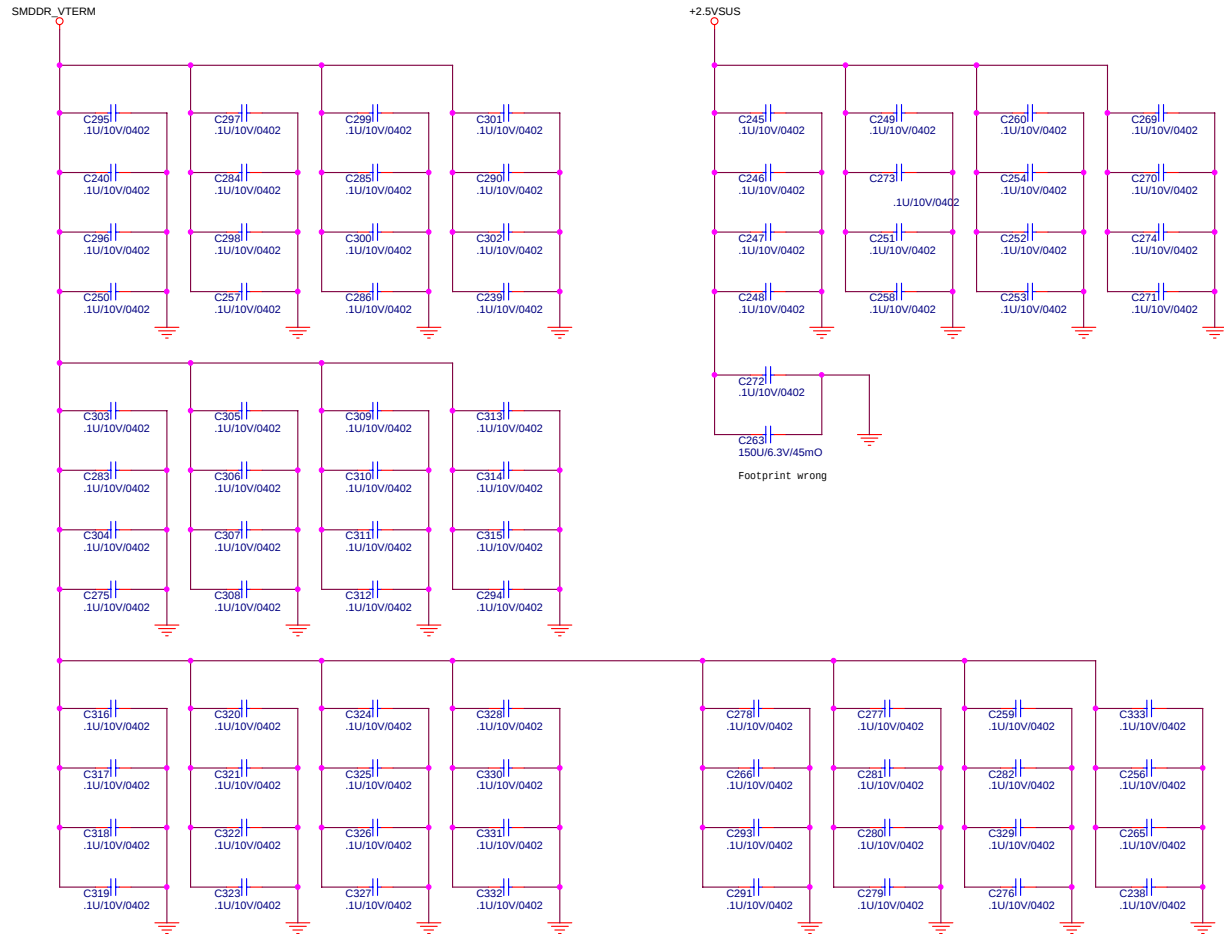
VSS

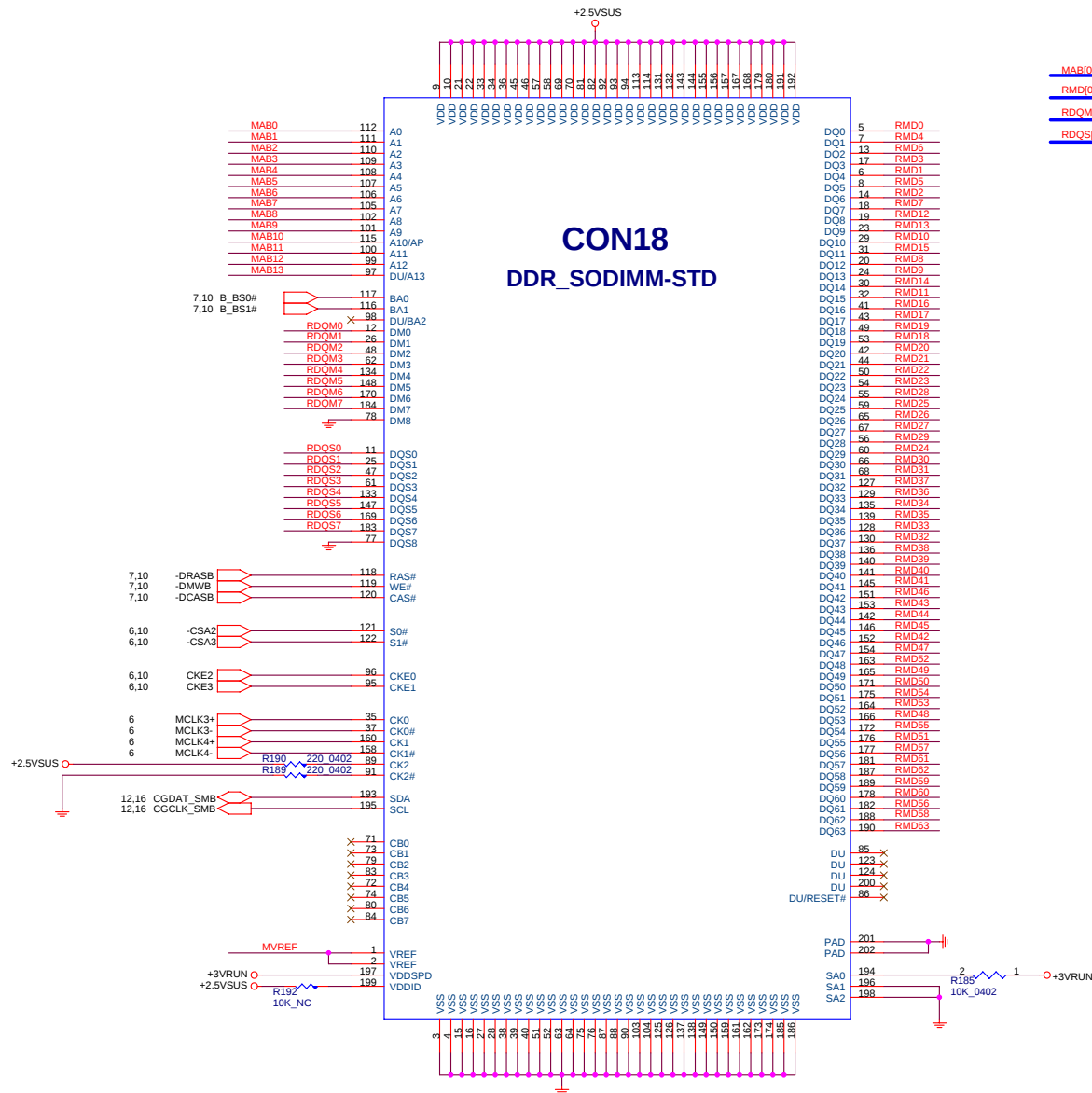
U8D

ALVISO

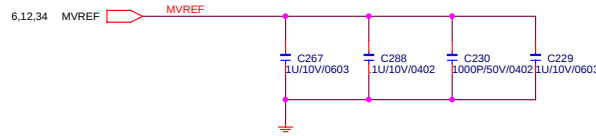
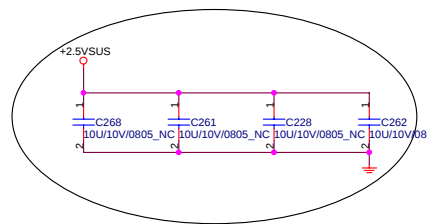
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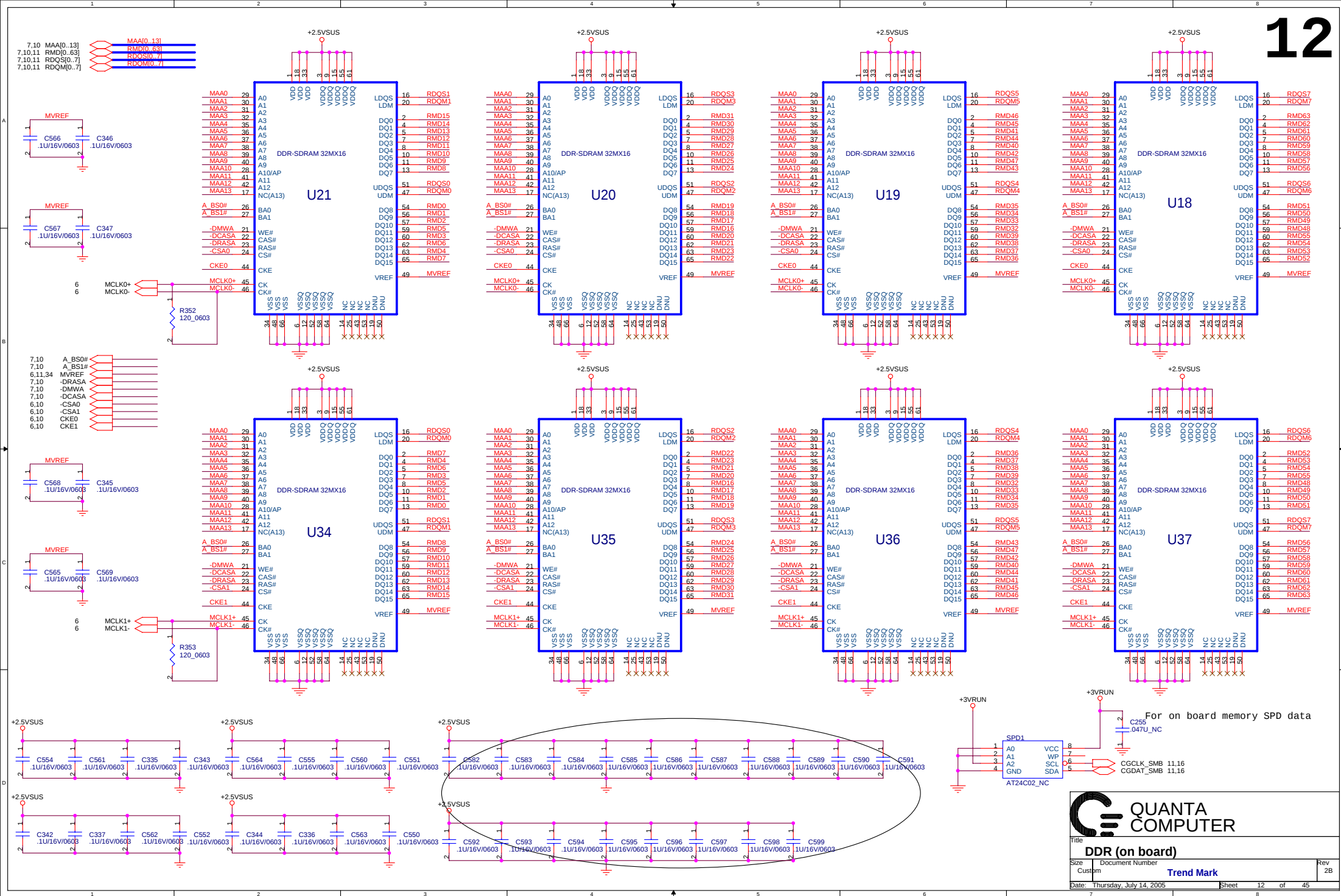
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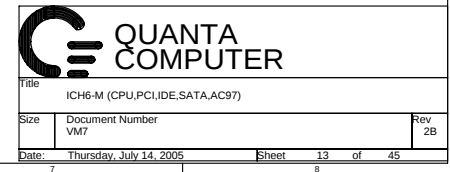


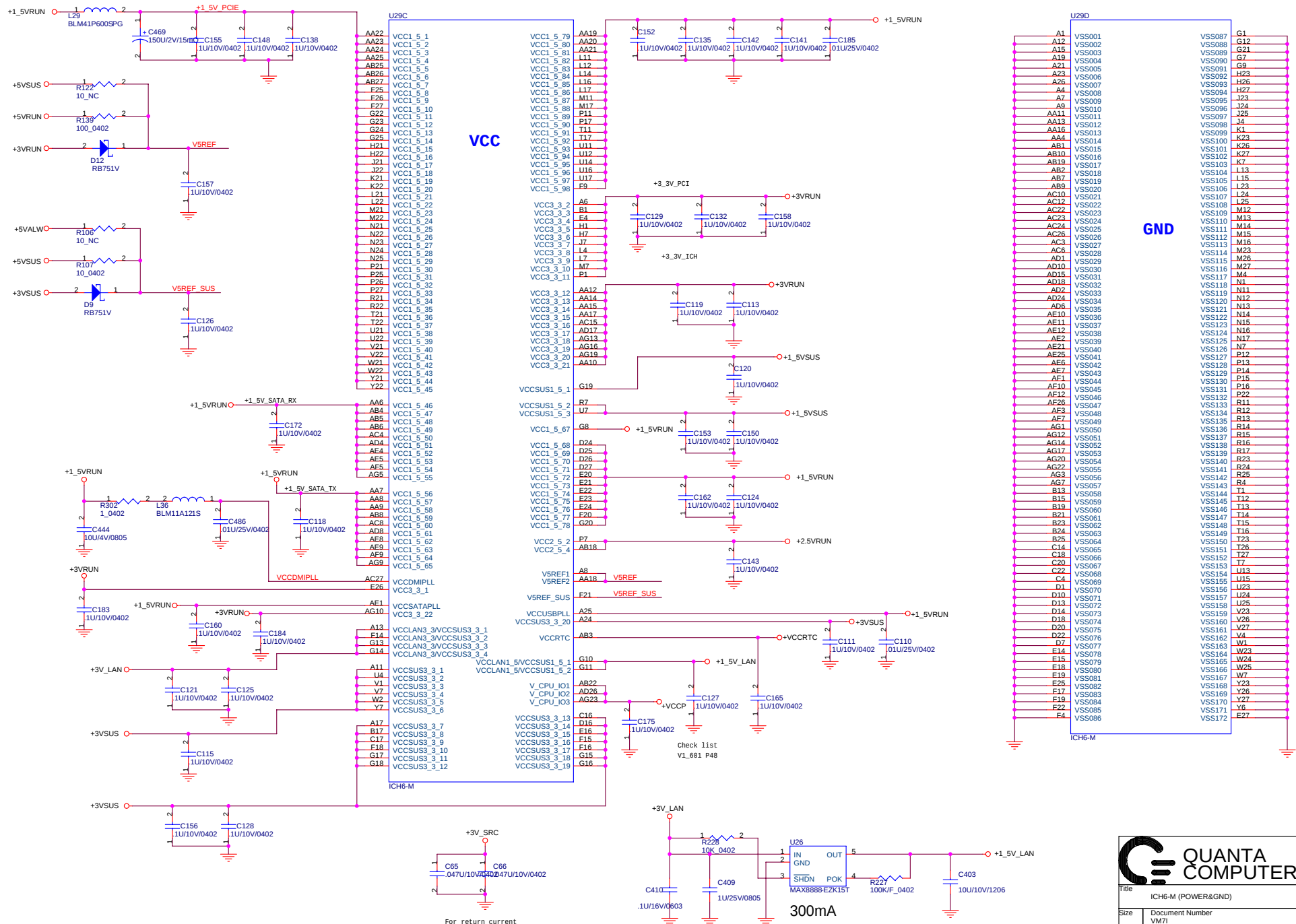


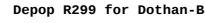
MAB[0..13] 7,10
RMD[0..63] 7,10,12
RDQM[0..7] 7,10,12
RDQS[0..7] 7,10,12



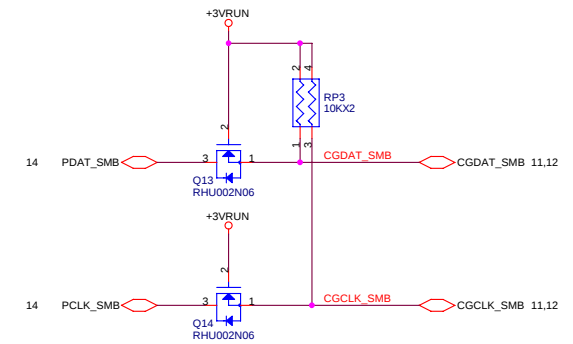
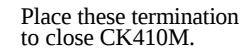




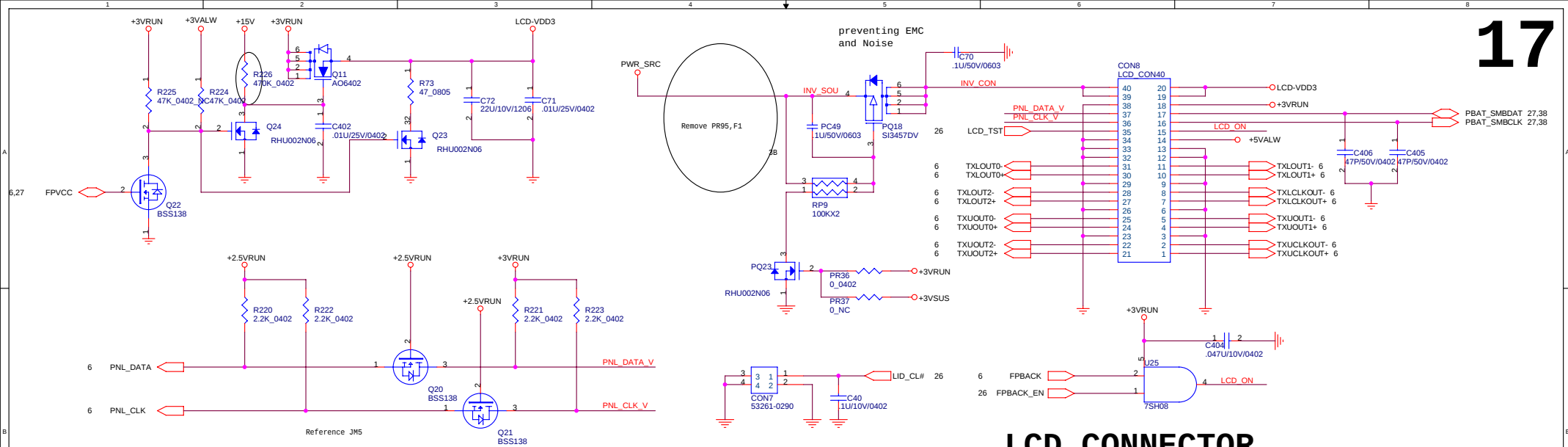




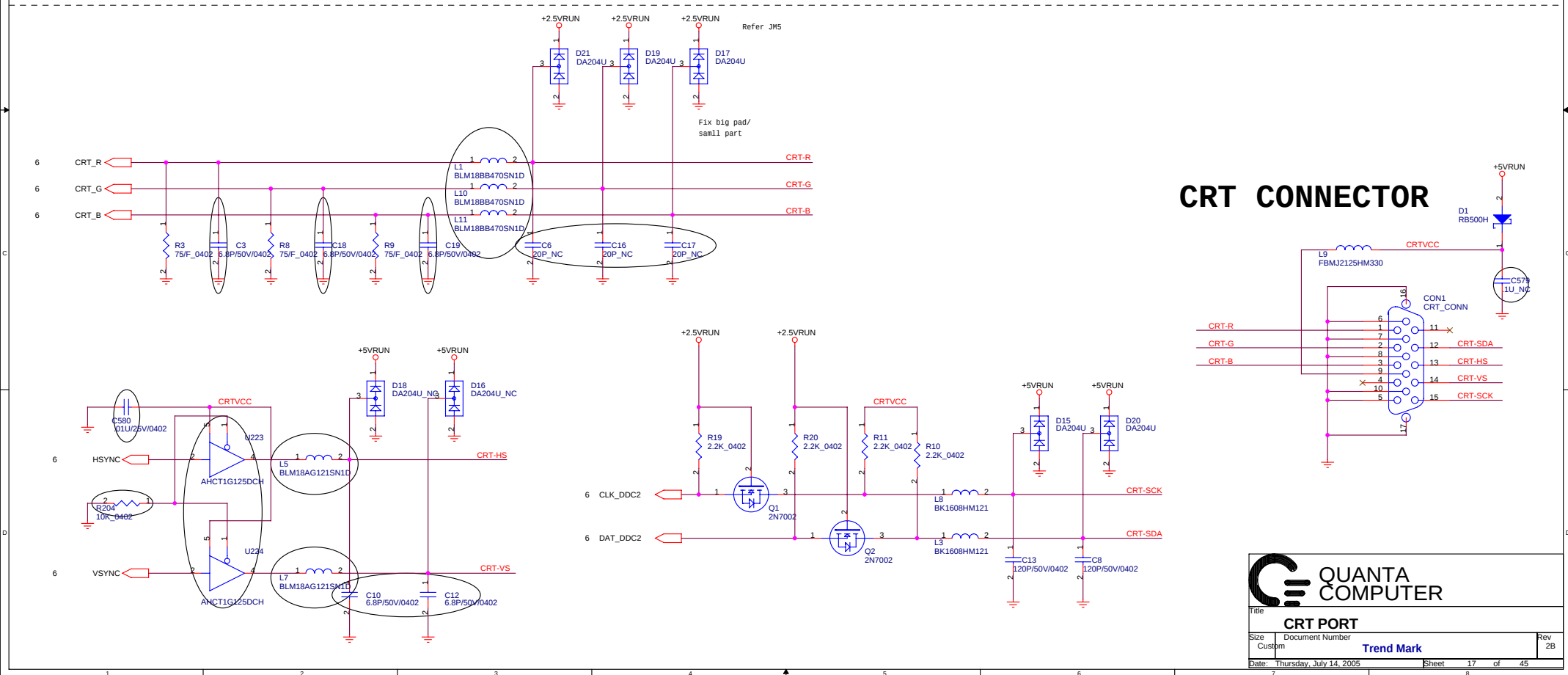
had spread spectrum support, reserved.



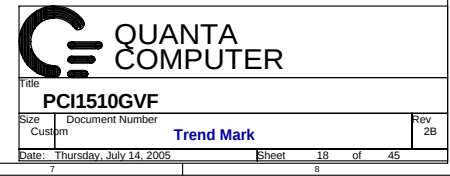
QUANTA
COMPUTER



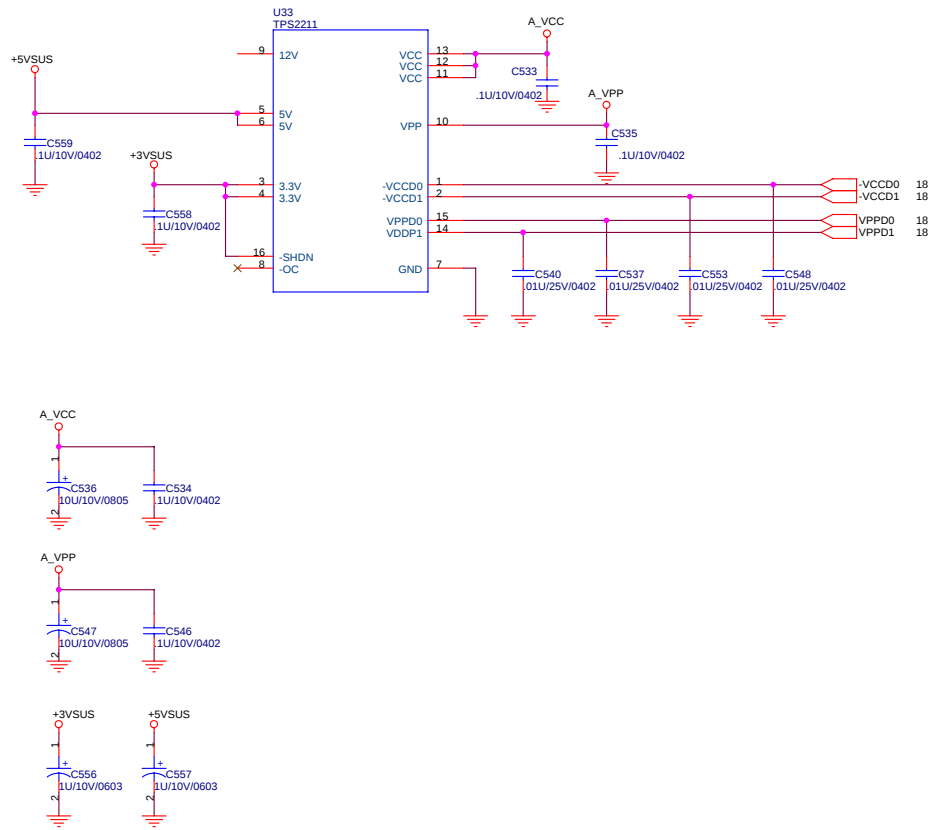
LCD CONNECTOR



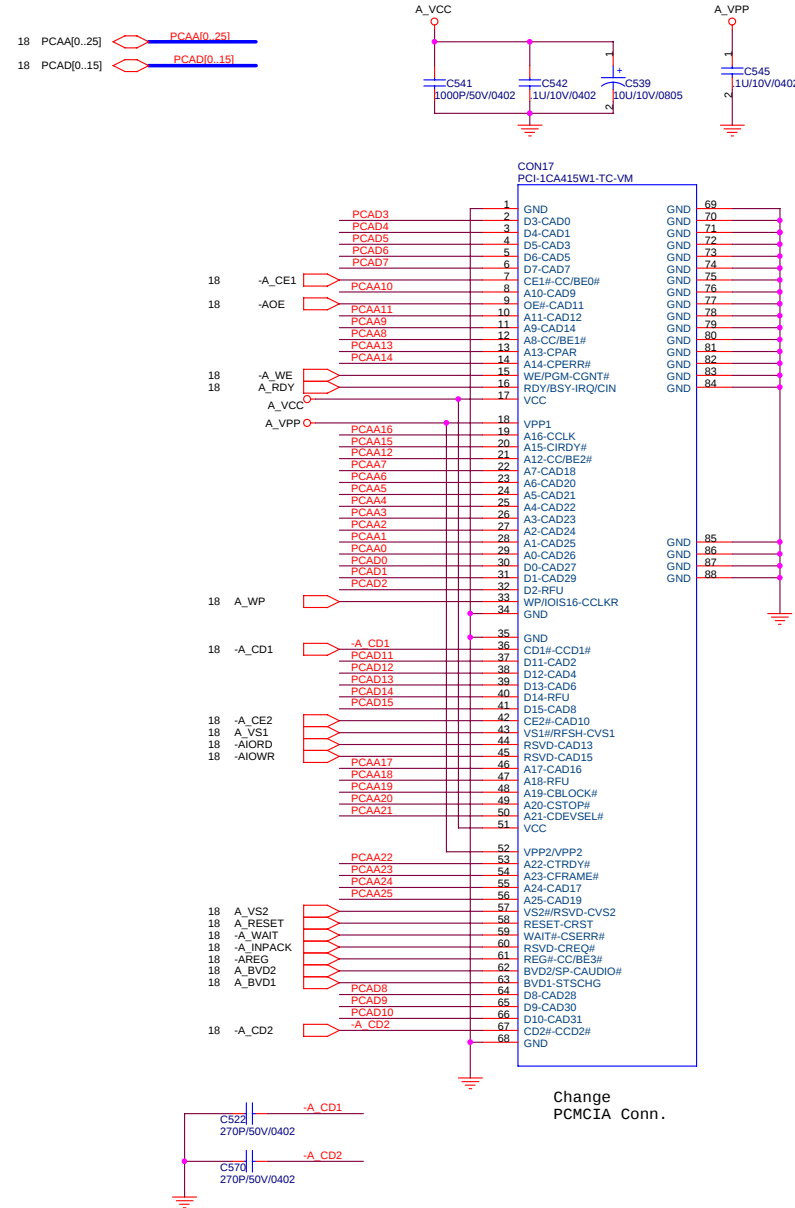
CRT CONNECTOR



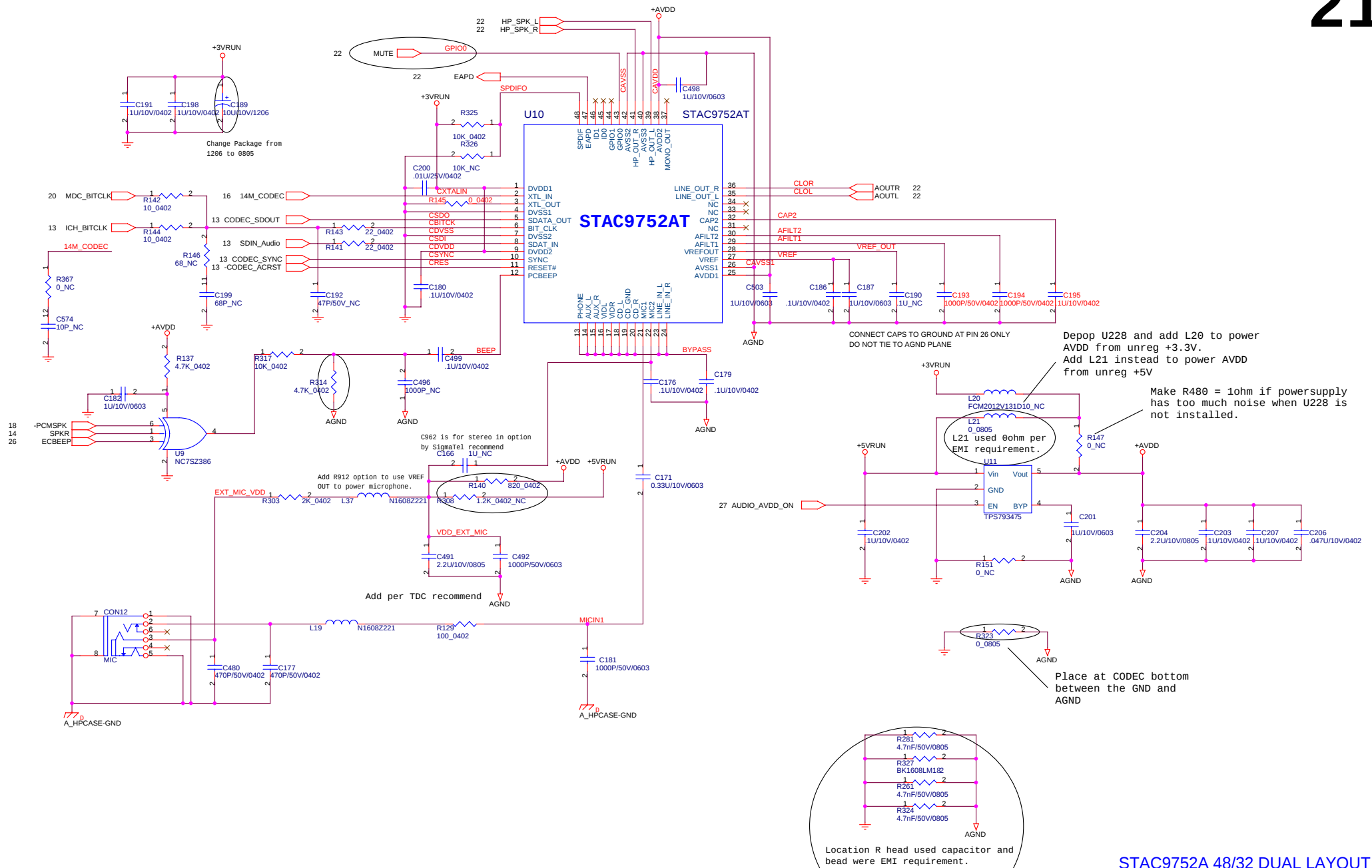
PCMCIA POWER SWITCH

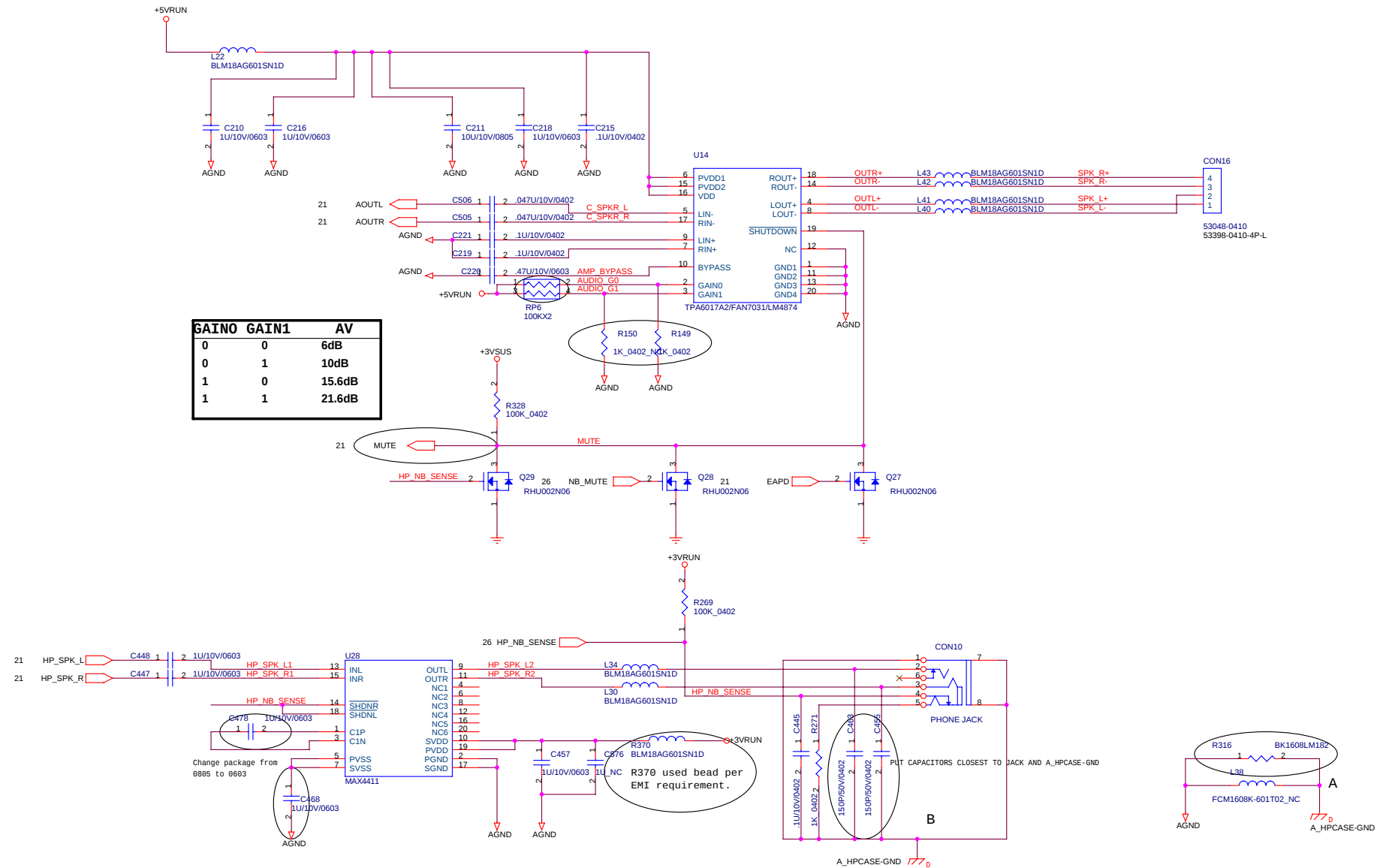


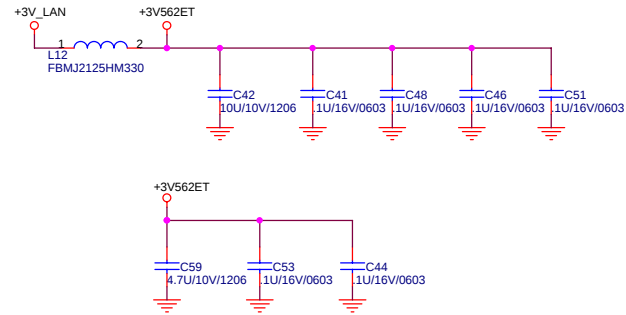
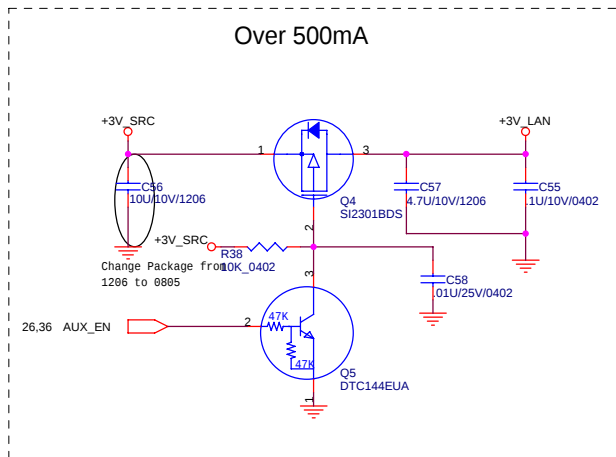
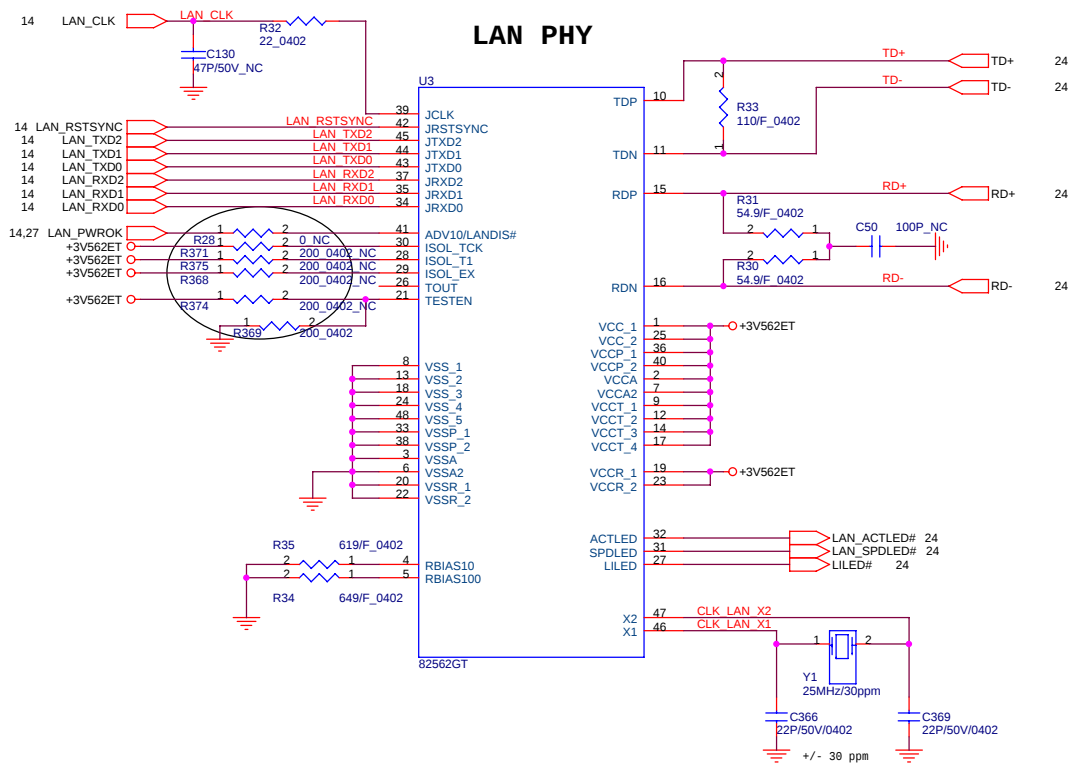
PCMCIA SOCKET



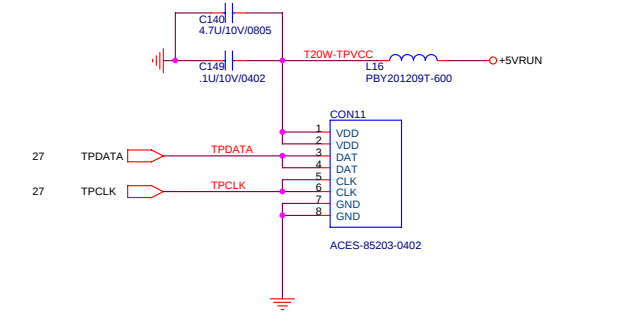
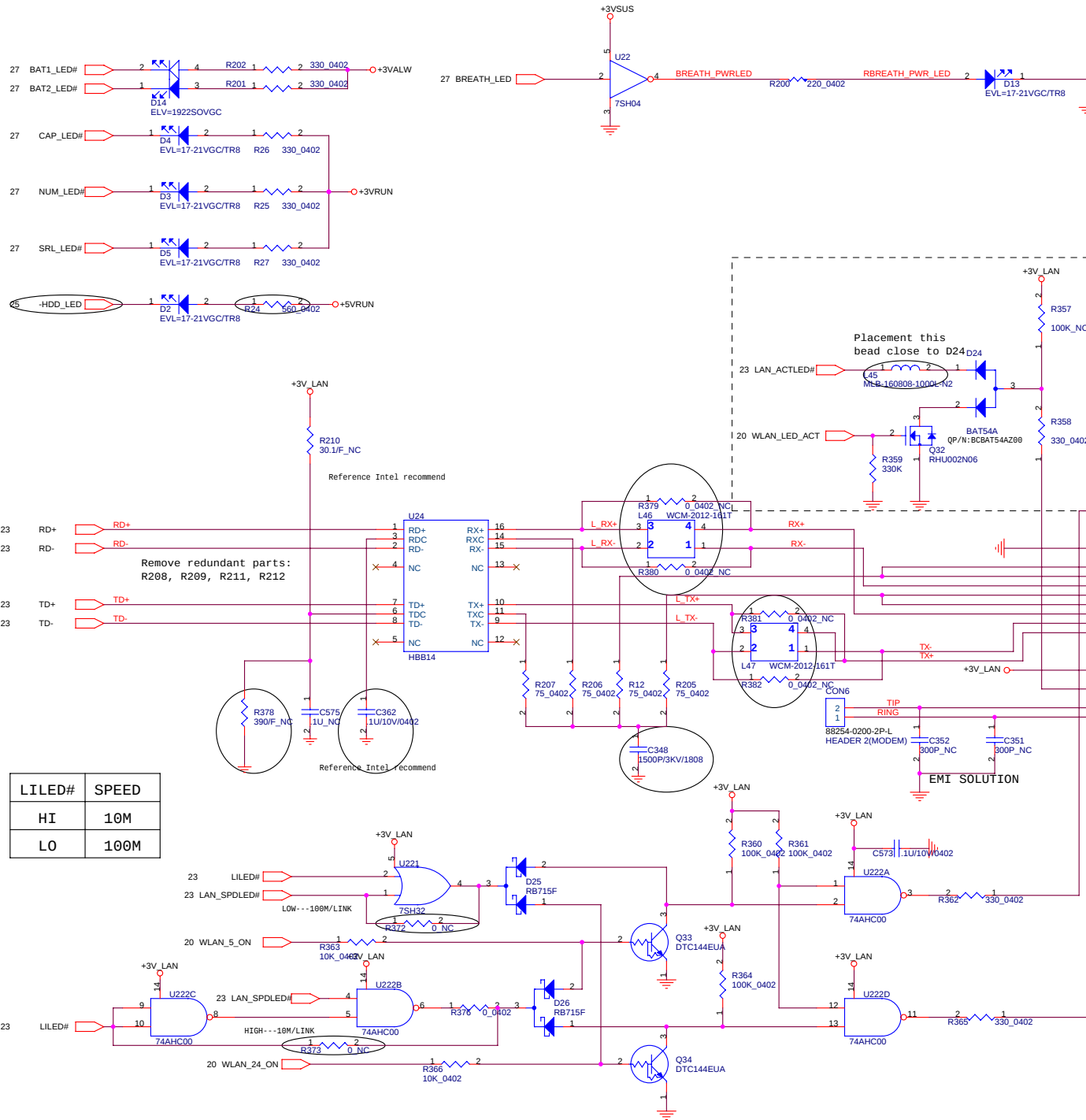
Change
PCMCIA Conn.







TOUCHPAD BOARD CON



LILED#	SPEED
HI	10M
LO	100M

Del D19
13 PDD0
13 PDD1
13 PDD2
13 PDD3

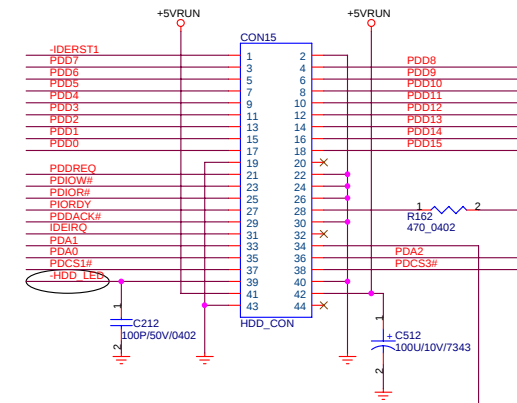
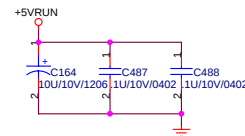
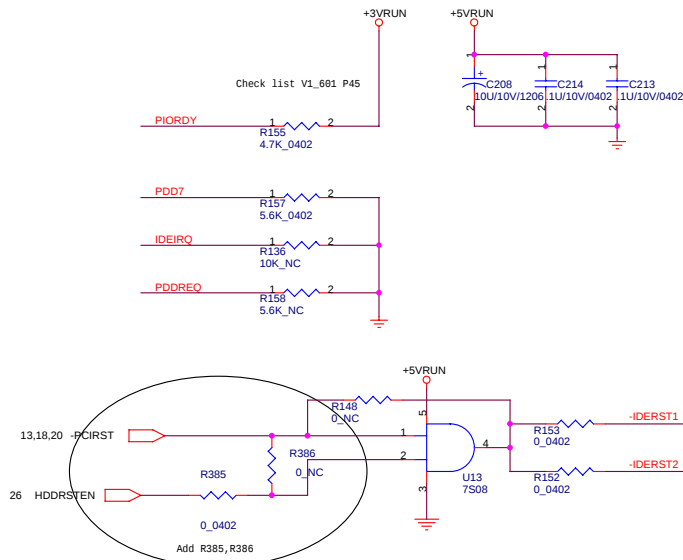
13 PDD4
13 PDD5
13 PDD6
13 PDD7

13 PDD8
13 PDD9
13 PDD10
13 PDD11

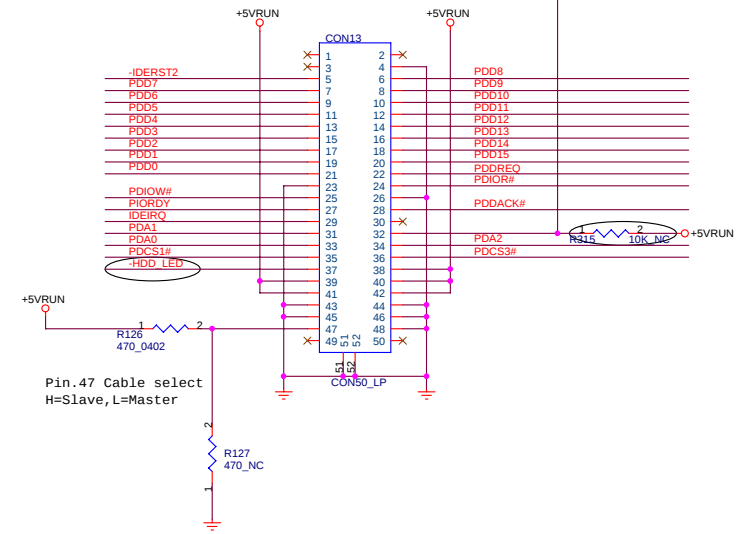
13 PDD12
13 PDD13
13 PDD14
13 PDD15

13 PDA1
13 PDCS3#
13 PDCS1#
13 PDA0
13 PDA2
13 PDDREQ
13 PDIOW#
13 PDIOR#
13 PIORDY
13 PDDACK#
13 IDEIRQ

Delete RN66,
R156, R159,
R160, R161,
R138 0ohm.

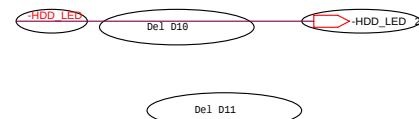


Per fix HDD&ODD issue.

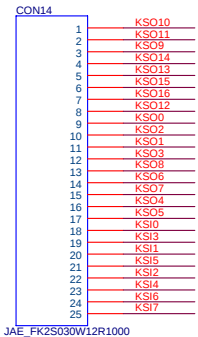
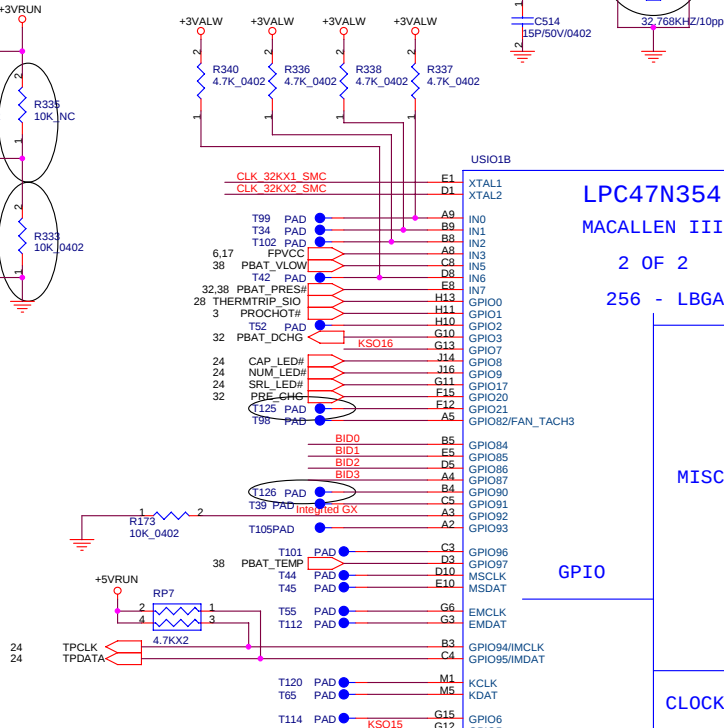
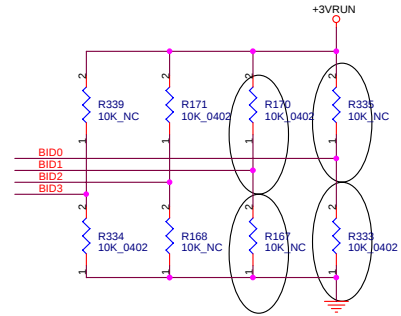


Del R163,R329 per HDD&ODD power link to '+5VRUN'

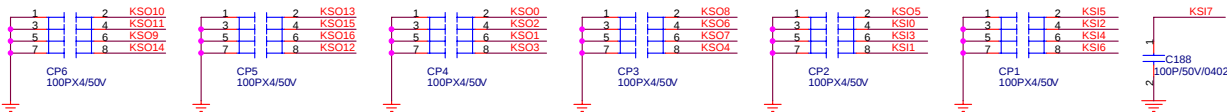
Del Q30,Q31,Q25,Q26,C509,C508,C493,C490,C483,R330,R301.



BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	PROTO1
0	0	0	1	PROTO1.5
0	0	1	0	PROTO2
0	1	0	0	PROTO3
0	1	0	1	QT
0	1	1	0	A01



Int. keyboard



LPC47N354 MACALLEN III 2 OF 2 256 - LBGA

MISC

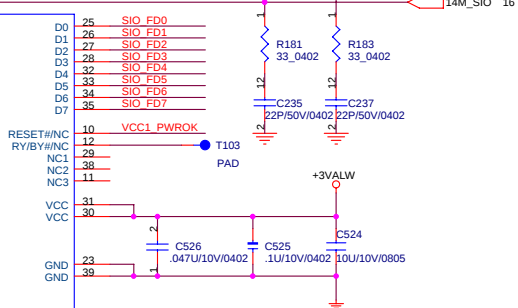
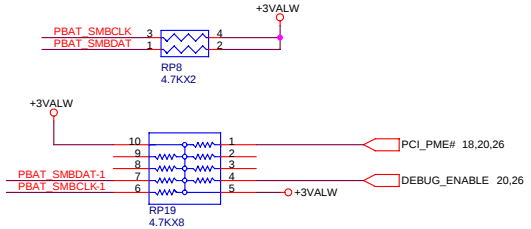
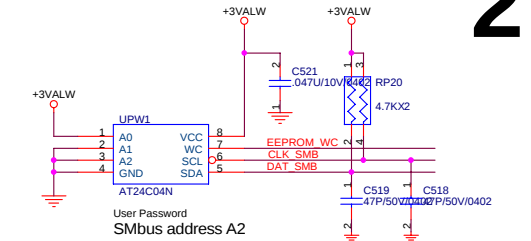
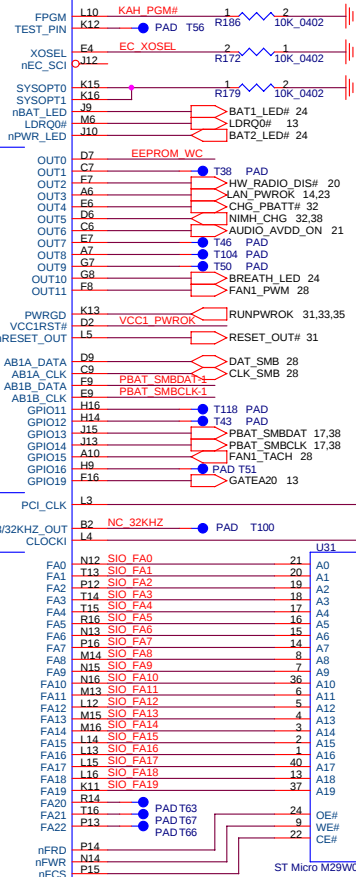
GPIO

CLOCK

K/B

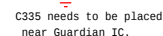
FLASH

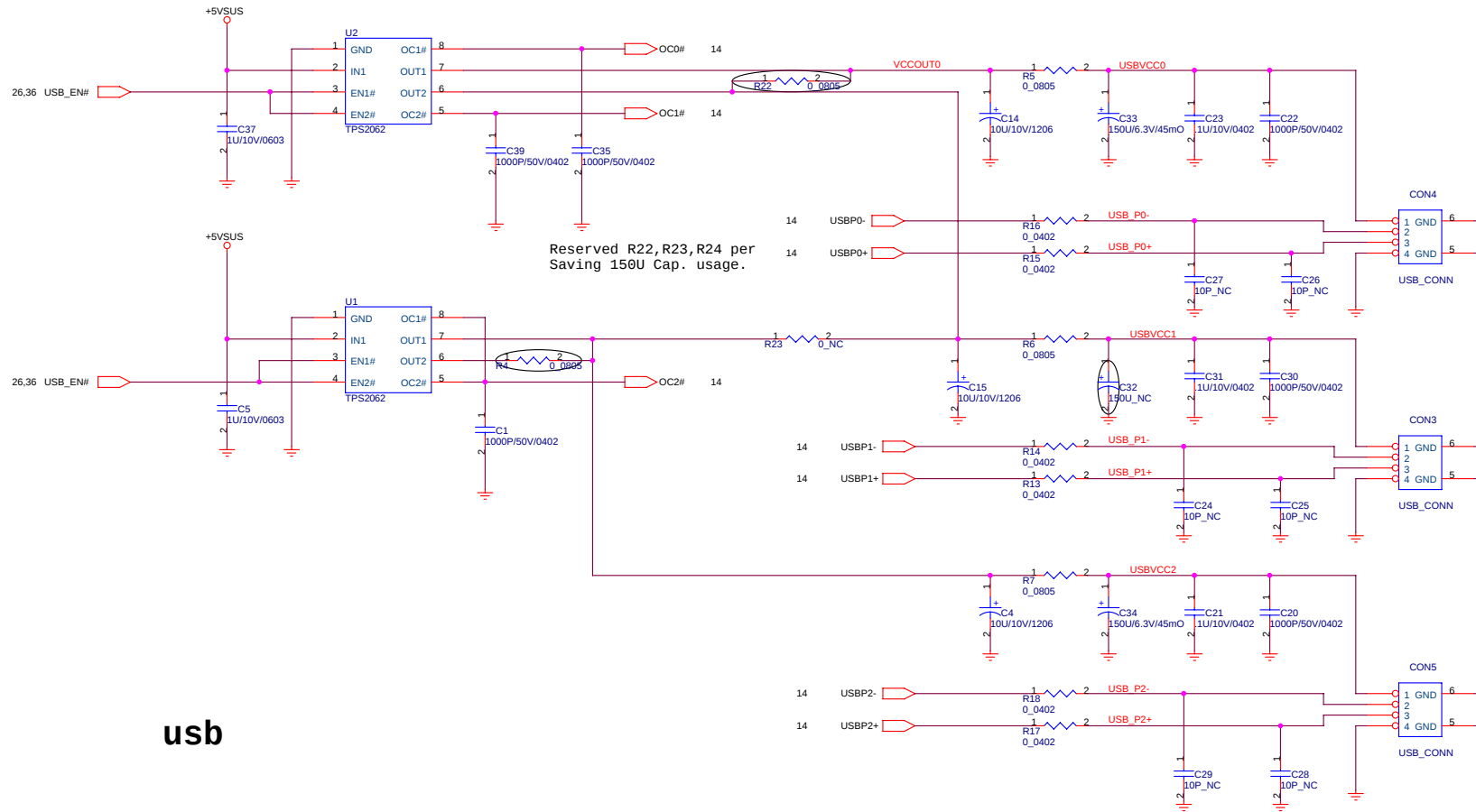
LPC47N354



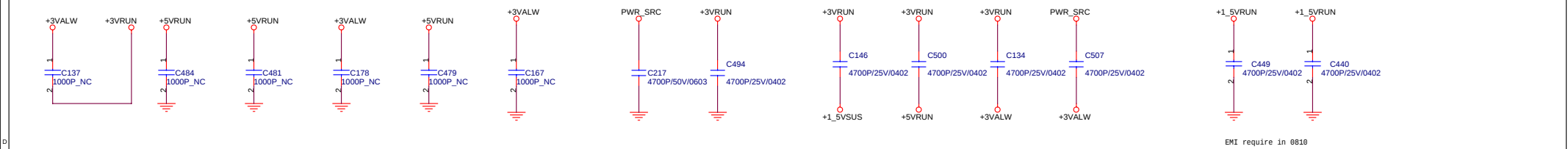
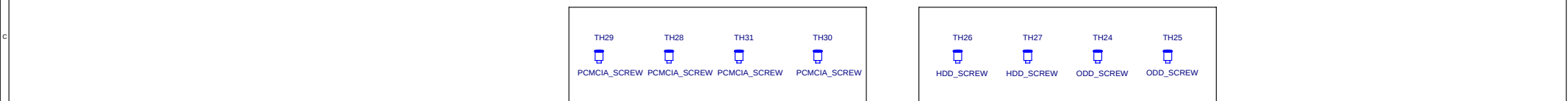
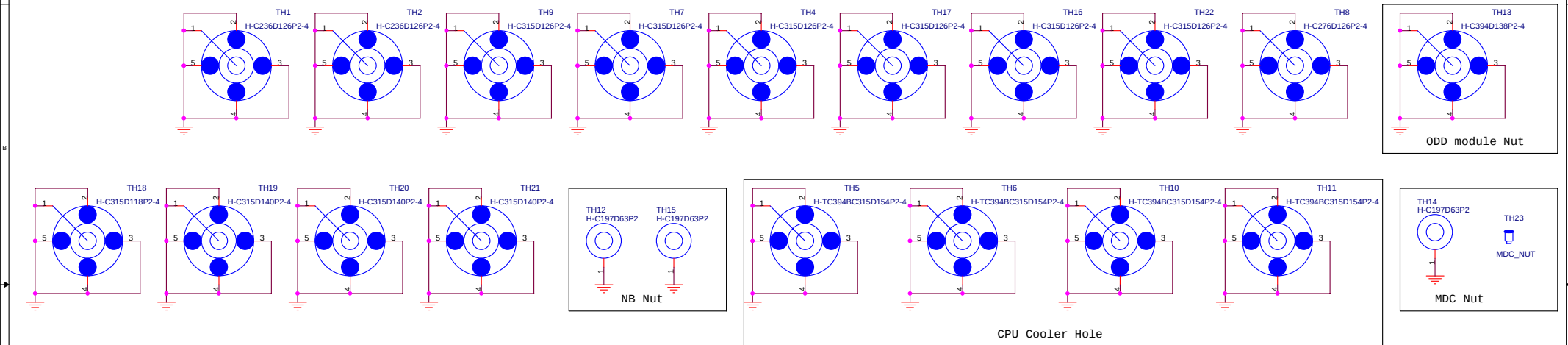
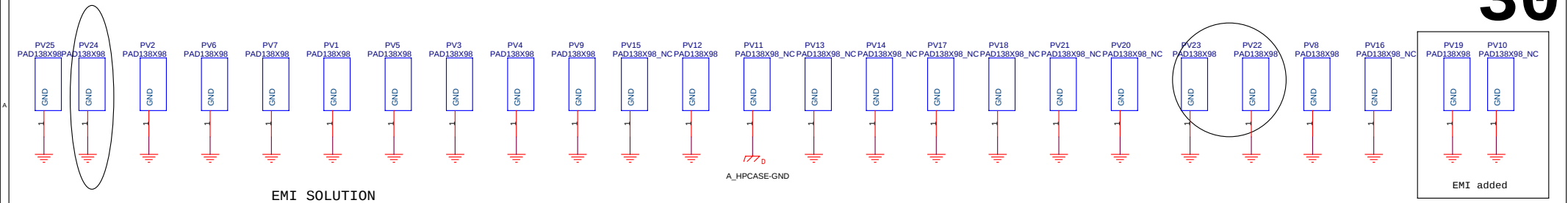
Ultra I/O Controller LPC47N254(GPIO/KB/MISC/FLASH)

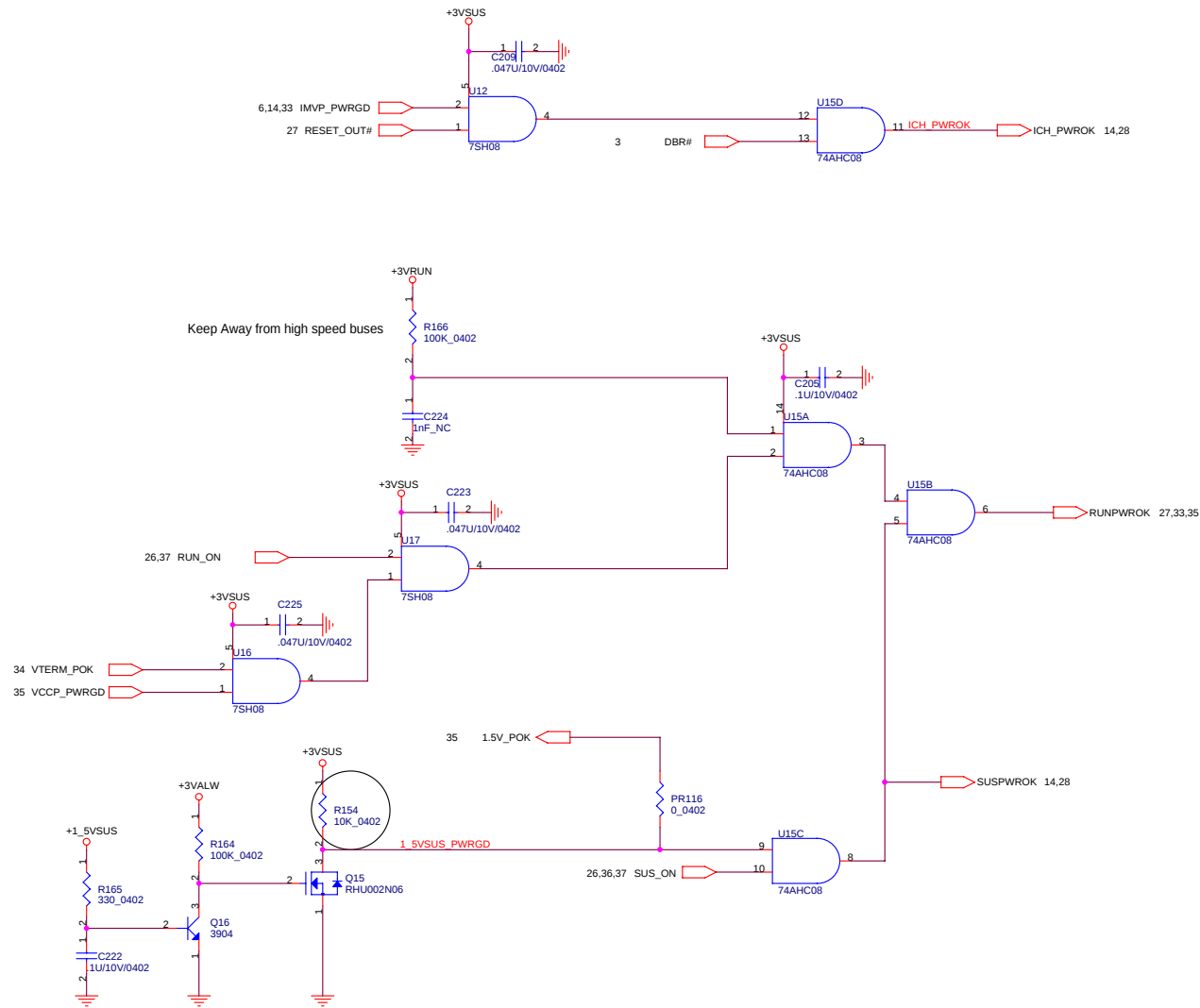
Size	Document Number	Rev
VM7		3C
Date:	Thursday, July 14, 2005	Sheet 27 of 45

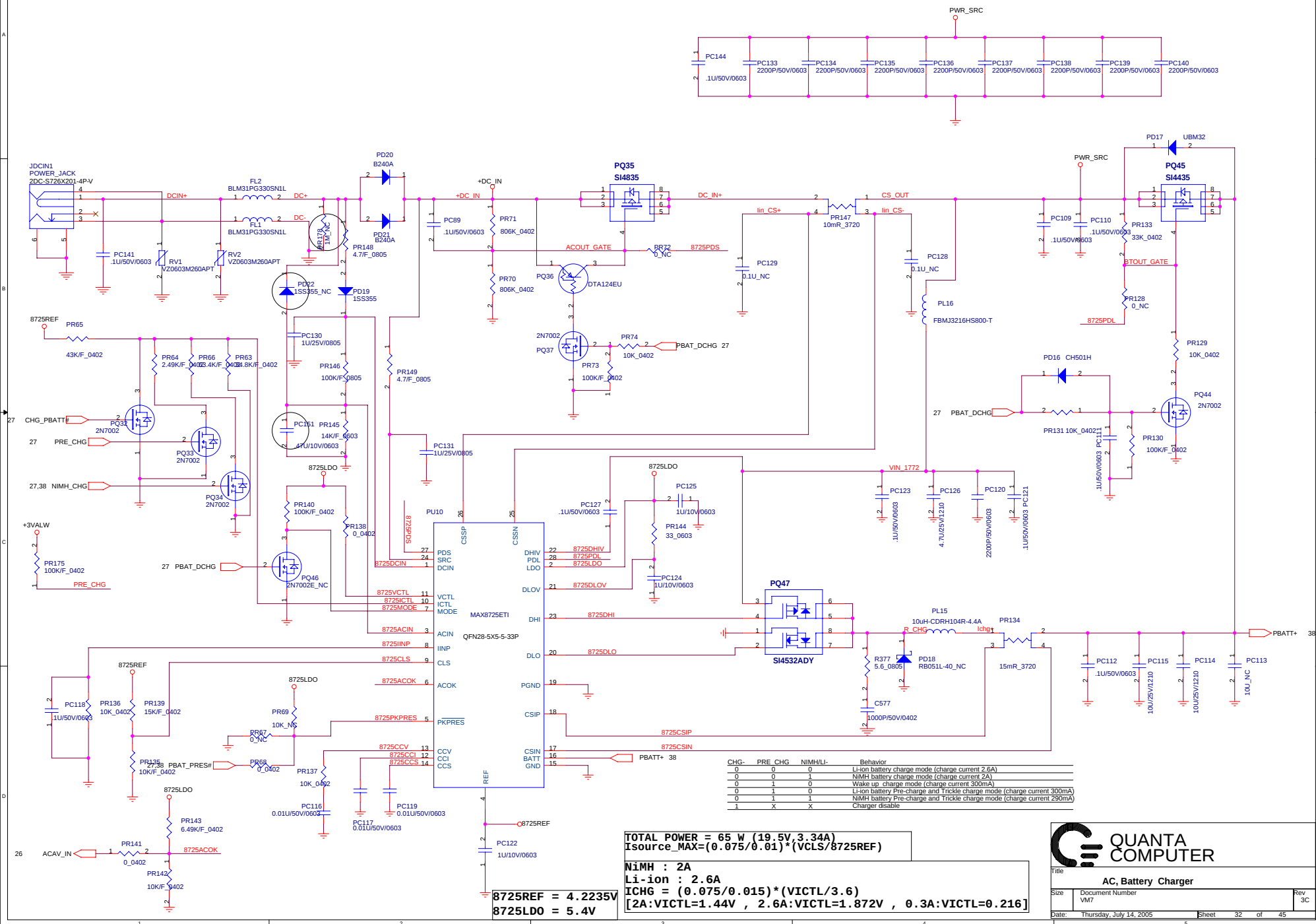


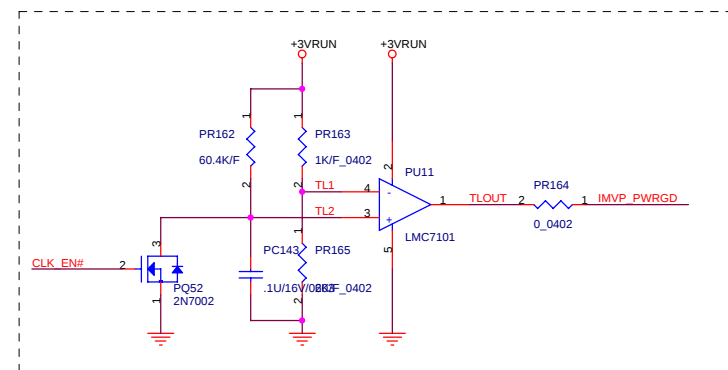
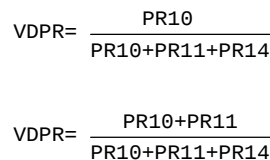


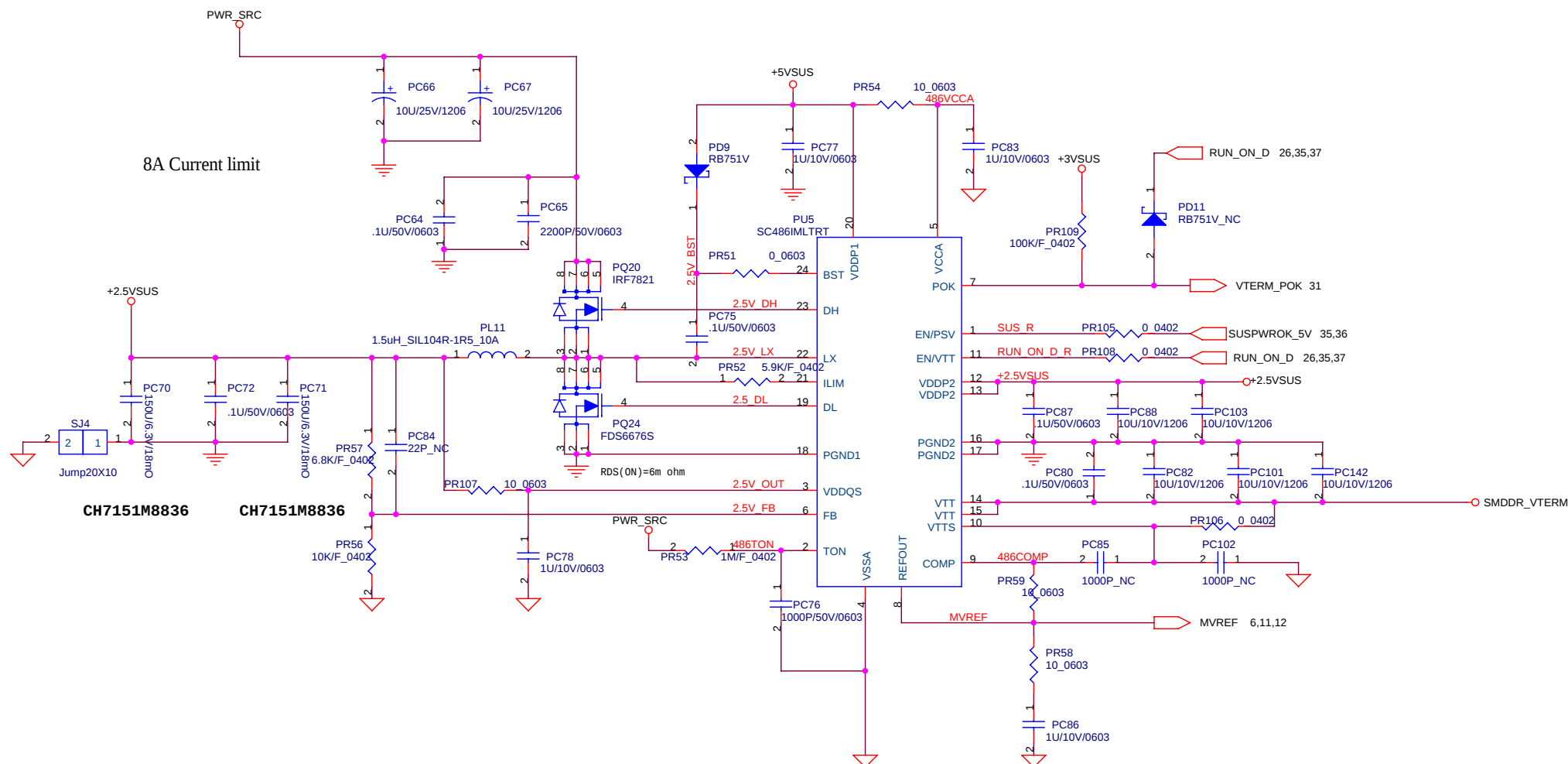
usb

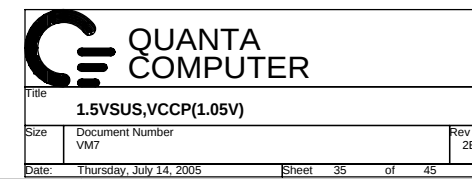




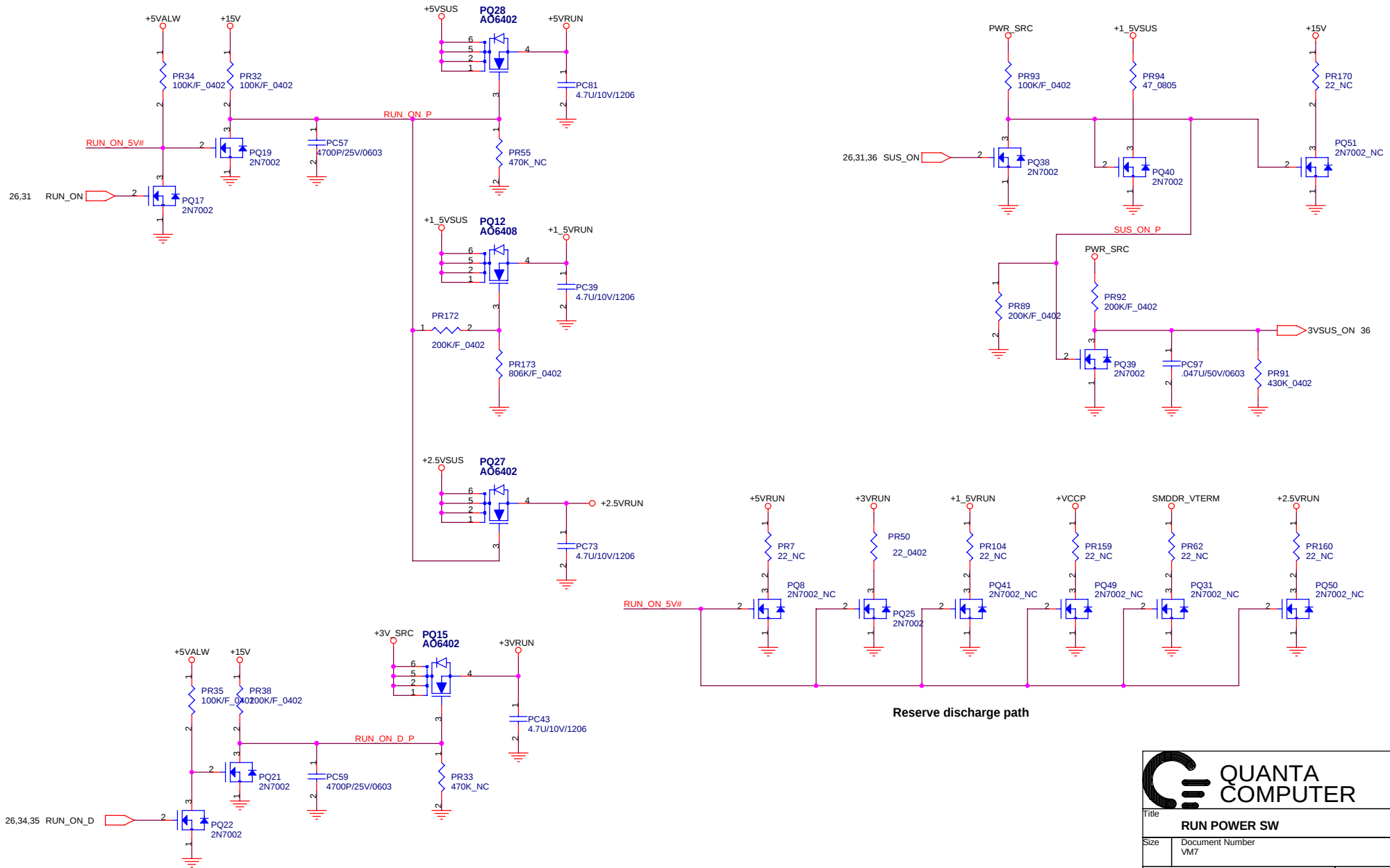


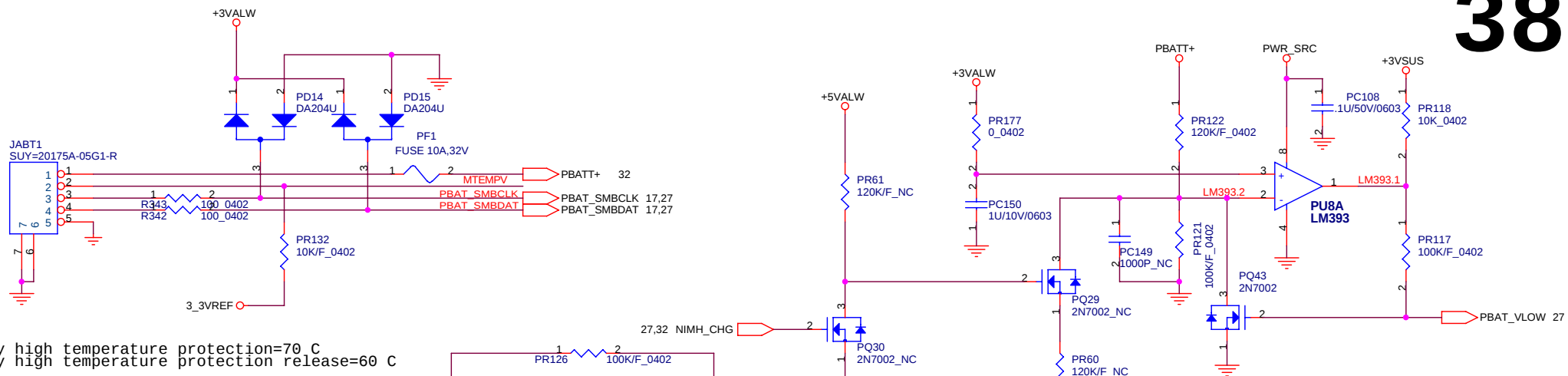




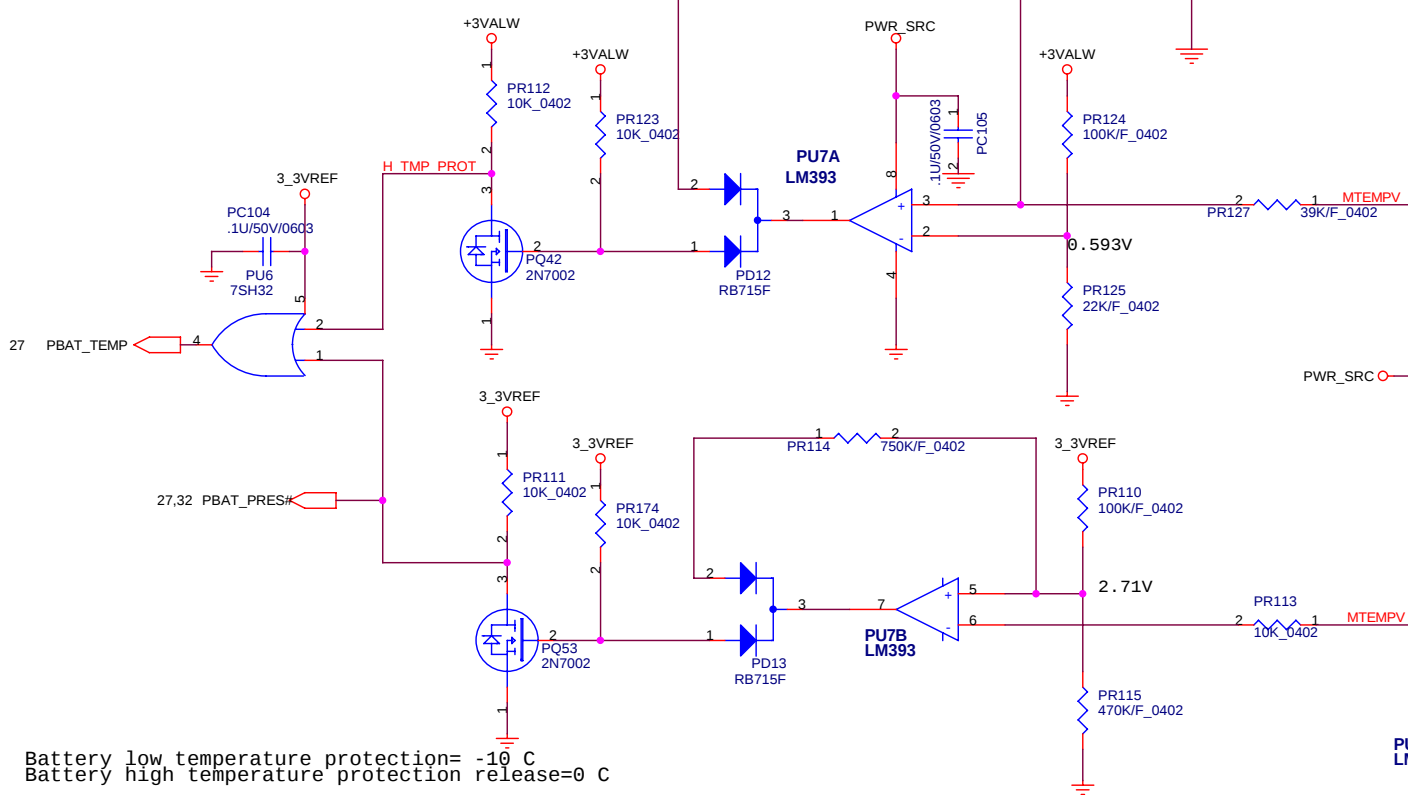








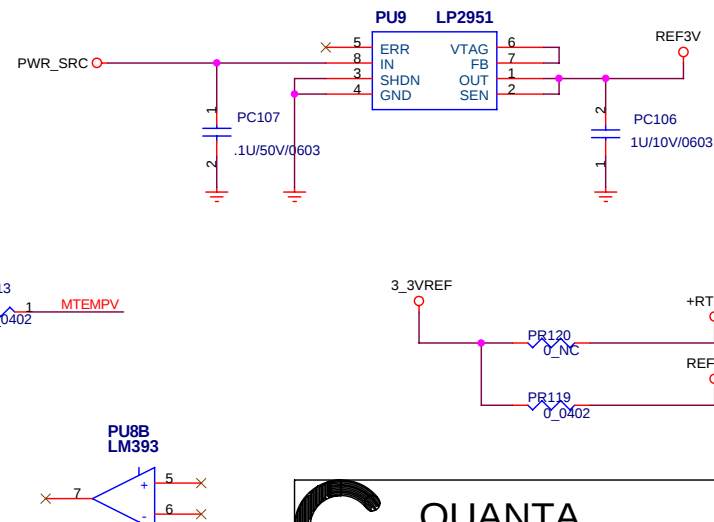
Battery high temperature protection=70 C
Battery high temperature protection release=60 C



Battery low temperature protection=-10 C
Battery high temperature protection release=0 C

	PWR_SRC	+3VAL	+3VALL	BAT 25C	BAT 20C	BAT 80C	BAT NOT IN	PBAT_PRES#	PBAT_TEMP	PBAT_VLOW
When Battery Only	V	-	X	X	X	X	-	Lo	Not Active	Not Active
When AC and Battery in	V	V	V	V	V	V	-	Lo	Active	Active
When BATTERY -10 C => NTC=46.6k MTEMPV=2.71V	V	V	V	V	V	V	-	Hi	Hi	Active
When BATTERY 0C => NTC=28.8k MTEMPV=2.45V	V	V	V	V	V	V	-	Lo	Hi	Active
When BATTERY 25 C => NTC=10K MTEMPV=1.65V	V	V	V	V	V	V	-	Lo	Hi	Active
When BATTERY 60 C => NTC=3k MTEMPV=0.76V	V	V	V	V	V	V	-	Lo	Hi	Active
When BATTERY 70 C => NTC=2.19K MTEMPV=0.593V	V	V	V	V	V	V	-	Lo	Hi	Active

Voltage low 7.5V detect
for Ni-MH battery
Voltage low 10.8V detect
for Li battery



QUANTA COMPUTER

Battery connector & Protection

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MODEL		Date	VM7I schematics change list				Model	DM3	MB			
							Page	FM	TO			
VM7I	07/26	P.24 Add MOD&HDD power switch circuit(reserved). P.25 Add MOD&HDD Enable pin. P.26 Add TP SMBUS pull up(RP36) P.31 Update Charge circuit per power update					1					
							2					
							3					
							4					
							07/27	P.5 Add C117,C119 per JM5 Schemtic change list update. P.7. Change L18,L19 to 10uH and C134,C146,C132 to 150V/2V and C95 to 2.2U/6.3V per JM5 Schemtic change list update. P.12 Change R326 to 20K, R323 to 100K C946 to 1U/10V per JM5 Schemtic change list update. P.13 Delete net"-PCICRI" per T2 non support it. P.14 Add C142,C143 per JM5 Schemtic change list update. P.17 Delete net"-PCICRI" and Q56,R438 per T2 non support it. P.20 Del net "ENPCMSPK" and D35,D36,R461 per non-need this function on T2 P.23 Change D39 to EVL=17-21SOC/TR8 and del net "-PWRLED2" per T2 support Signal power LED. P.25 USIO1.B12(GPIO70) add a net "HDDRSTEN" per primely HDD rst signal, Add a SPD1(ST34C02) per support on board DDR requirement. P.26 Del net "ENPCMSPK" per T2 non-need it and Add C121,C123 per JM5 schematic change update. P.27 Change R624 to 43K/F and R627 to 10K/F per JM5 schematic change update.	5			
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	15											
	16											
	07/28	P.11 Moved SPD EEPROM circuit of DDRAM from P.26 and changed SMBUS to PDAT_SMB&PCLK_SMB. P.19 Removed RF switch function, Del net"-RF_SW", D33 P.23 Removed RF switch function, Del net"-RF_SW", SW1,Q59,R486,C801,D40,R489 P.26 Add USIO1.F12(GPIO20) for DC/C-, USIO1.B9(IN1) for H-Temp,USIO1.B8(IN2) for BL/C-, USIO1.E8(IN7) for PBAT_PRES#, USIO1.E6(OUT4) for CHG-, USIO1.D6(OUT5) for NIMH/LI-, USIO1.A7(OUT8) for PRE_CHG, Del USIO1.F7(OUT)"-SW_RF". P.31,32,37 Update power change page.					17					
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	07/29	P.4 Add C125 per refer the JM5 Schematic update. P.5 Add R1,R2,R3 del R62,C149,C152 per refer the JM5 Schematic update. P.25 Change net "H-Temp" & "BL/C-" pin of SMsC per SW requirement. P.26 Change net "DC/C-" & "PRE_CHG" pin of SMsC per SW requirement. but "CHG-" wasn't defined.					23					
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	07/30	P.14 Chnage C546 from 220U to 150U per refer JM5 Schematic update. P.20 Update MIC JACK circuit per refer JM5 Schematic design. P.23 Update LAN JACK symbol to combo with LED. P.25 Del R577,add R107,R108 per refer to JM5 schematic. P.26 Del R247 per power had pull up resistor. Update GPIO pins definition per SW update.					28					
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							33					
	08/02	P.9 Add RN57 per "A_BS0#","A_BS1#","B_BS0#","B_BS1#" pull Hi, delete RN77 per duplicate net of "-CSA0","-CSA1","-CSA2","-CSA3" P10 Depopulate R195 per refer Intel checkliet recommend. P.16 Change LCD panel control signal by SMBUS and add "LCD_TST" delete "VBRI".Add C76,C77 per refer JM5 schematic. P.24 +5VRUN via R104 to +5VMOD net mane corrected. P.25 Add "LCD_TST" and change "H-Temp" to "PBAT_TEMP" P.26 Change "DC/C-" to "PBAT_DCHG","BL/C-" to "PBAT_VLOW","CHG-" to "CHG_PBAT","NIMH/LI-" to "NIMH_CHG" P.27 Deleted RTC reserved circuit. P.31 Change "DC/C-" to "PBAT_DCHG","CHG-" to "CHG_PBAT","NIMH/LI-" to "NIMH_CHG" P.37 Change "BL/C-" to "PBAT_VLOW","H-Temp" to "PBAT_TEMP"					34					
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							08/03	P.5 Add R225 to +VCCP per refer chekc list V1_601 P.31 & JM5. Connection TV I/F pins to GND per refer chekc list V1_601 P.30.Deleted R1,R2,R3 pull down resistor per ducplicate R207,R208,R199. P.7 VCCTX_LVDS change power from +2.5VSUS to +2.5VRUN per refer chekc list V1_601 P.33 P.12 Update SATA I/F pins link per refer Design Guide V1.0 P.241 P.13 WAKE# pull hi to +3VRUN with R310 per refer check list V1_601 P.43 P14 Add U8,R1,R2,C64,C65,C66 to generate +1_5V_LAN per used Intel LAN I/F power & LAN power change from RUN plane to LAN plane per refer to DM1. P.15 Delete R263 per the"PCLK_SIO" should link to U35.4. P.16 Add R415,R416,R421,R422,Q1,Q2 per reference JM5 P.17 Deleted some pins which 1510 hadn't.And deleted R430,R431,L82,L83,C701,C702,C703,C706,C707	43			
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MODEL	Date	VM7I schematics change list	Model	DM3	MB		
			Page	FM	TO		
VM7I	08/03	P.22 Deleted LED control signal O/P pins per LAN jack non support. P.23 Change D38 to daual color LED per BATT LED dispaly requirement and deleted LAN LED circiut per LAN jack non support. P.25 Add R3 per link to SMsC RTC power pin. Depopulated R231 per R108 had populated. P.26 Add "-BATLOWLED" per BAT LED support dual color.	1				
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	08/04	P.14 Add C402 per refer Intel check list V1_601 P48 P.16 Populate PR139 and depopulate PR140. P.24 Populate R507 per refer Intel check list V1_601 P45 P.25 Add RP35 per refer JM5. Add R9,R13,R14,R15,R18,R19 per SIO non used pins pull up.Change R233 from 0 to 10K per SMsC recommend. P.26 Add R6,R7,R8 per SIO non used pins pull up. P.31 Change PR10,PC210,PC5 footprint from 1206 to 0805. Add PD30 P.35 Add PL30	6				
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			11				
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			13				
			08/05	P.9 C196 Footprint change from 0402 to 7343 per footprint wrong P11. Change SPD1 power tie in from +3VALW to +3VSUS P.12 Delete U40,C499,R384,R385, "DELAY_PLTRST#", "PLTRST#_1" per "LAN_PWROK" control by ICH6. REQ6 tie in to +3VRUN per check list V1_601 P36 P.13 "LAN_PWROK" link to ICH6.U2, add "ICH_PCIE_WAKE#" per refer JM5, delete "DELAY_PLTRST#". P.19 Refer JM5 Mini-PCI pin assignment, add C1,R47,"HW_RADIO_DIS#", delete non used "USBP3-","USBP3+" P.20 MIC jack powered to +VDDA,R12 change to 2.2K. C62 change to 0.1U, reserved C764,C912,C962 by SigmaTel recommend. U228 Change to TPS793475. P.21 delete R8301,R471,R472 per SigmaTel recommend for saving cost. P.23 Change C806 to 3KV cap. P.26 Update KB conn(CON41) to 26 pins. P.28 Change OC portection IC to TPS2062 X 2. And reserved 0R link to all of O/P pins per will check to saving 150U cap.	14		
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	08/06	P.10,11 DDR SPD's SMBUS had corrected as JM5 P.10 MVREF was generated by SC486.Del R168,R174,C802,C191,C249,C223 P.15 Change U35.22,U35.23 function to U35.17,U35.18 per TDC recommend. P.19 Reserved USB per test USB wirless. P.20 Codec power had changed to +5VRUN and change PCBEEP control same as JM5. PCBEEP link to PHONE had confirmed with Vendor. P.20 Add C1009 for bypass caps of TI-793475. P.23 Update LED control net name per SIO definition.Chnage LED resistor. P.25 Update SIO pinde per reference the GIOP table update. P.26 Update SIO pinde per reference the GIOP table update. P.31 Add R62,C67 per EMI requirement P.33 Add PC4,PC15 per reduce ripple. P.37 Add R65,R66 serial terminator on Battery SMBUS.			26		
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			08/09	P.5 Reserve R1484 0 ohms for Thermal team concern DDR Ram door skin temperature. P.10 Delete R168 per MVREF refer from SC486. P.16 Delete D23 and D32 for cost saving and change power of R419, R420 and U224 to CRTVCC. P.16 Change ESD protector D24~D28, D30, D31 connecting power to +5VRUN;Add +2.5VRUN to Q2 gate pin per losting. P.16 Change CON23 pin15 to +5VALW for inverter. P.19 Add R1481 and R1482 to reserve USB interface for future option USB wireless LAN;Pin-104 tie to ground per leverage Azeda. P.20 Change R12 PU from +AVDD to +5VRUN and R12 to 1.2K, R10 1.0K per total MIC PU resistor is 2.2K. P.20 Correct codec digital power to +3VRUN; Pin13 "phone" tie to Bypass; Change R4481 to R1483. P.23 Add U249 for breath LED; D38, D41, D42 and D43 PU to 330 ohms; Change D44 PU to 470 ohms per leverage fromAzeda. P.26 Add RP64 4.7KX2 for tunnig SMB rise/fall time. P.35 Correct PR100 to 1K ohms per leverage from Azeda.	39		
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MODEL		Date	VM7I schematics change list				Model	DM3	MB		
							Page	FM	TO		
VM7I	08/10	P.12 Correct signal net from "-GNT0" to "-GNT3" P.13 Delete signal net "-PCICRI" P.20 U229 VDD from "+5VRUN" change to "+AVDD". Change R10 from 1K to 2K. P.25 Add a test pad(T126) on USIO1.K5(TXD) per reserved debug function requirement. P.26 Delete signal net & non used test pad(T22) P.27 Corrected thermal sensor control signal power name from "VTT" to "+VCCP" P.31 Corrected on of net name from "CHG_PBAT" to "CHG_PBATT"					1				
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	08/11	P.12 Add R27 per support on board memory SPD judgement. P.13 Add R48,C6 per leverage P2's experience P.16 Add C4 per preventing EMC and Noise P.19 Delete L85 and leaved CON26.113,117,118,119,120 to NC per TDC recommend. P.20 Change C63 to 4.7uF. Change R11 to 100 ohm. add R77,R78,R79,R80 per GND and AGND bridge. Change C776 to 2.2uF and add C5. P.29 Add PV24 per EMIrequirement.					9				
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	08/12	P.3. Delete R45 per PWM controller not support PSI function. P.5 Unpopulate R807, R808 per check with JM5. P.7 Unpopulate R199, R203, R207 per EA test in Azeda. P.9 Follow change L55 and L23 per Azeda originally used the same BLM18PG181SN1 ferrites, but saw a large voltage drop across these ferrites. We changed to the BLM18PG330SN1 ferrite, which has a lower DCR. P.16: Add R1486 for a pullup on Q91.3 to +3VALW. Azeda did this to address a glitch seen on LCDVCC when entering and resuming from S3. P.16 Change R423, R424, R425 per EA test in Azeda. P.21 Add RP65, R1490 R1491 for audio gain selection. P.22. Add R1488 & change R706 PU to +3V_SRC; Delete R602 and Tie Pin 21 to LAN ; change R608 to 619 and R609 to 649 Per Intel review. P.22.Change R604 to 110; R605 & R606 to 54.9 and depopulate C892 Per Intel review. P.23. Depopulate R493, R494, R499, R500, C802 and C803; Add R1489 to U231 Pin6 per INtel reveiw. P.25 Add R1485 for LCD_RST PU and R1487 for ATF_INF# PU. And add T132~T148 per suggestion from ADC. P.25 Correct R9,R13,R14,R15 Pu to +3VSUS and R19 to +3VALW per reveiw with SMsC. P.26. Chnage R6, R8 and R103 PU to +3VALW and R7 PU to +5VALW per Peer review in ADC. P.26. ADD AB1B CLK/DATA PU to +3VALW per ADC peer review. P.27 Redefine J7 pin out per FAN follow Rocket design.					16				
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							08/16	P.26 Delete RP8 per un-used. P.31 Change PR148 from 0603 to 0805. P.34 Change Pu2.23 signal from "1485_VIN_B" to "1485_VIN_A"	31		
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	35										
	36										
	08/20	P.17Add AC terminator R354,C571 for "PCLK_PCM" P.19 Add AC terminator R355,C572 for "PCLK_MINI". Add LAN LED control O/P signal "WLAN_LED_ACT", "WLAN_5_ON", "WLAN_24_ON" P.20 Add AC terminator R367,C574 for "P14M_CODEC". P.22 Add LAN LDE control O/P signal "LAN_ACTLED#", "LAN_SPDLED#", "LILED#" P.23 Add LAN LDE control circuit. P.26 Upcate KB connector to 25Pins. P.31 Change Power Jack and update chagre circuit. P.35 update DC/DC circuit. Delete PR6 and PR14 per power team request.					37				
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	08/26	P.16 Correct Q23,Q24 symbol P.21 Correct Q27,Q28,Q29 symbol P.22 Update U3.41 name from "ADV10" to "ADV10/LANDIS#". Add R368,R369 per Intel recommend. P.23 Change "LAN_SPDLED" & "LILED" Function per Intel recommend. P.31 Correct "DC_IN+".					46				
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MODEL	Date	VM7I schematics change list	Model	DM3	MB
			Page	FM	TO
VM7I	08/30	P.13 Corrected "USBP0+","USBP0-","USBP0+","USBP0-". P.18 Correct CON17 library,add 4 pins GND per connector fix block. P.26 Add rp8 per PBAT SMBUS pull up. Change BID to proto1.5. Correct KB library(delete fix block) P.29 Add TH23 per MDC connector NUT. P.37 Correct BAT connector SMBUS data & clock pin define.	1		
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	08/31	P.23 Depopulte R210 and Populate C362,C575 per Intel recommend P.26 Corrected BID table. P.29 Update CPU cooler hole diameter per ME requirement. P.30 Populate R154,R164,R165,Q15,Q16,C222 per power sequene circuit update.	7		
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	09/02	P.11 Depopulate SPD1&C255 per no need support on board memory SPD. P.23 Poplate C351,C352. P.27 Change R42 from 22.1K/F to 2.21K/F per Schematic error. P.29 Update MDC nut, MDC cable nut, ODD module nut P/N. Add PV19 per EMI requiurement.	12		
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	09/16	P.12 Depopulate R320 P.16 Correct L2,L4,L6 value from 0_0805 to 0_0603 P.22 Depopulate R368 per LAN issues. P.23 Depopulate C362,C575 per proto1 LAN function issues and correct LILED#&LAN_SPDLED# circuit. P.31~P.37 Change all of resistors package from 0603 to 0402. P.32 Add PR153,PR154,PR155,PR156,PR157,PR158,Reserve for test. PC7,PC8,PC9,PC10 change package from 1210 to 1206. PQ4,PQ5 change value form TPCA8005A-H to SI7336DP.Change PC24 package from 0603 to 0402. P.34 PC93 change package from 1210 to 1206. P.35 PC25,PC98 change package from 1210 to 1206.	17		
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	09/23	P.3 Populate R61 per used Dothan B CPU. P.7 C411,C420 change material. P.9 RN39,RN36,RN45,RN42,RN52,RN55,RN61,RN58 Change part value from 10X2 to 56X2. P.15 Change R291 value from 39 to 10 per fix EA rise/fall rate violate spec. P.20 C189 change package from 1206 to 0805.Depopulate R261,R281,R323 per fix HP noise issue. P.21 Change C468,C478 package from 0805 to 0603.Reserve R370,C576. P.22 Reserve "LAN_PWROK".Change C56 package from 1206 to 0805. P.23 Change net name from "-ODD_LED" to HDD_LED". Del R203,C2 and MGEND. P.24 Per fix HDD & ODD issues, change "-ODD_LED" to "-HDD_LED" chnage connector net name to "-HDDLED" ,Del D11. P.26 Update BID,Populate R170,R333 depopulate R335,R167. Del net "PS_ID","PS_ID_DISABLE#" and add T125,T126 P.28 Populate R22,R4 depopulate C32 per TDC recommend. P.31 AddPC133,PC134,PC135,PC136,PC137,PC138,PC139,PC140 per EMI requirement. P.32 Add R21,C38 per EMI requirement.	26		
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	09/24	P.3 Depopulate R51,R57 P.15 R112 change value from 39 to 15 per fix EA test fail. P.16 Remove PR95,F1 P.23 LAN jack connect to MGND P.29 TH3 contact to MGND	40		
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	09/27	P.22 Add R371,R374 and R375 to reserved for LAN test. P.23 Add R372 and R373 to reserved for LAN LED cost down test. P.24 Reserver R315 per ODD power supplier	45		
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MODEL		Date	VM7I schematics change list				Model	DM3	MB
							Page	FM	TO
VM7I	09/30	P.11 Change R140 PU to +AVDD.					1		
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	10/01	P23. Add R376 for LAN LED and remove C2 and R203. P28. Depopulate C24, C25, C26, C27, C28 and C29 per USB eyes diagram issue. P29. Add PV25 for EMI request to place close ODD connector. P.31 Add PC144 0.1U mount on Power Source for EMI require. P.32 Power change PQ52 Value to 2N7002					4		
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	10/04	P.31 for EMI require add R377 2.7/F and C577 0.01U P.23 Reserve R378 for Lan function P.20 C171 change from 1U to 0.33U P.21 C505 C506 change from 0.1uF to 0.047uF P.23 C362 need mount 0.1uF					10		
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	11/03	P.5 Depopulate R258,R259,R267. P.4,5,6,7,8 change NB P/N from AJ829100T11 to AJ829100T20 per NB change ver from B0 to B1. P.16 C6,C16,C17 change value from 22P to 20P, L2,L4,L6 change Value from 0R to BLM18BD600SN1D, R3,R8,R9 change value from 150R to 75R. PR36 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. CON1 change P/N from DFDS15FR441 to DFDS15FR0Q8. CON8 change P/N from DFHD30MS361 to DFHD30MS697. CON7 change P/N from DFWF02MS037 to DFWF02MS029. P.23 D24 change value from BAT54S to BAT54A. CON6 Change P/N form DFHD02MR281 to DFHD02MR346. C573 change package from 0603 to 0402 per proto2 SMT issues. P.29 Remove PV11,PV15 P.30 PR116 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. P.31 R377 chane value from 2.7R to 5.6R, C577 change value from .01U to 1000P, PD16 change value from RB500V to CH501H.PR68,PR138,PR141 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. JDCIN1 change P/N from DFPJ04MR101 to DFPJ04FR086 P.32 R21 chane value from 2.7R to 5.6R, C38 change value from .01U to 1000P.PR1,PR79,PR164 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. PC24 change package from 0603 to 0402 per proto2 SMT issues. P.33 PR105,PR106,PR108 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. P.34 PR25,PR85 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. P.35 PR43,PR45,PR46,PR96 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. P.37 PR119 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues.					14		
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	11/17	P.2 Add R379 per support CPU FSB 400 only. P.13 Change R91 from 33ohm to 22ohm per fine tune 14M_ICH signal issues. P.15 Change R252 from 24ohm to 10ohm per fine tune 14M_ICH signal issues. P.16 Depopulate D16,D18 and delete L2,L4,L6,C7,C9,C11. P.23 Change CON2 footprint from LAN-1770112-15P-H to LAN-1770043-1-15P P.25 Delete Q30,Q31,Q25,Q26,C509,C508,C493,C490,C483,R330,R301 per not support ODD hot plug. P.26 W2 change to same as W1 per cost down. P.35 Change PR40 pull up source from "+3V_SRC" to "+3VSUS" per solved timing issues of "SUSPWROK".					28		
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			11/18	P.7 Add C578 100uF per fix CRT water wave issues. P.16 Change Q1,Q2 from 2N7002E to 2N7002,Change R73 from 4.7K_0402 to 47_0805 for shortening LCD_VDD3 discharge time. P.17 Change Q17 from 2N7002E to 2N7002. P.20 change U10.43 from "HP_NB_SENCE" to "MUTE" P.21 Change R370 from 0ohm to BLM18AG601SN1D, Change C455,C463 from 4700pF to 150pF.Depopulate R150 and populate R149 per down Amp gain. P.29 Add TH24,TH25,TH26,TH27(HDD&ODD screw) into schematic per BOM export requirement.					36
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					41				
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	11/19	P.3 Delete R379 per had PU in P15. P.10 Delete C268, C261, C228, C262 per cost down. P.16 Change L1,L10,L100 from CX8LL121002 to BLM18BB470SN1D. Change C3,C18,C19 from 10pF to 6.8pF. Delete CRT-GND. P.20 Depopulate R324. P.26 Depopulate R168, R170,populate R167, R171per update BID. P.31-P.35 Power update schematic and removed power jump.					43		
							44		
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							48		
	11/22	P.16 Depopulate C6,C16,C17. P.20 change MIC bias voltage to AVDD mount R140, unmount R308. P.24 Delete RN66, R156, R159, R160, R161, R138 0ohm.					49		
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MODEL	Date	VM7I schematics change list	Model	DM3	MB
			Page	FM	TO
VM7I	11/24	P.7 Add C581 during U8.E19 and U8.G19 per fix CRT water wave issues.	1		
		P.16 Change CRT H/VSYNC buffer from TC7W126FU to AHCT1G125, chnage L5,L7 from BK1608HM121 to BLM18AG121SN1D, Change C10,C12 from 120pF to 6.8pF. reserver C580,C581 per refer to JM5 CRT design.	2		
		P.21 Change R150 PW to +AGND for setting amplifier to be 6db..	3		
		P.24 Delete D10 and link "HDD_LED" to SIO directly.	4		
			5		
	11/25	P.21 Change R140 vlaue from 1.2K to 820 per 'EXT_MIC_VDD' source change to '+AVDD'	6		
		P.22 Depopulate RP6.	7		
		P.24 Del R163,R329 per HDD&ODD power link to '+5VRUN'	8		
		P.31 PU PR175 to "+3VALW" per SMSC GPIO pin define error, change R377 package from 0402 to 0805 per EMI requirement.	9		
		P.32 Chnage R21 package from 0402 to 0805 per EMI requirement, add PC146,PC147,PC148 per fix noise issues.	10		
	11/26	P.16 change R226 value from 100K to 470K	11		
		P.24 Add R379-383 per EMI requirement to verify LAN. Change R24 from 470 to 560	12		
	12/20	P.8 C578 change Value from 100U to 150U per fix NB VGA codec power issues.	13		
		P.17 Update C579 property per C579 is non populated parts.	14		
		P.24 Depopulate C351,C352 per EMI confirm to removed it.	15		
		P.32 Change R371 P/N to lead free per Vendor recommend.	16		
		P.33 Change R21 P/N to lead free per Vendor recommend.	17		
	12/23	P.24 Correct R358 pad from 0603 to 0402	18		
			19		
			20		
	12/29	P.14 C114 Change vlaue from 4.7pF to 10pF per fine tune CLK48_USB.	21		
		P.21 R314 change value from 8.2K to 4.7K per decrease beep sound.	22		
		P.24 Add L45, reserve L46,L47 per EMI requirement.	23		
		P.30 Add PV22,PV23,PV24 removed TH3 per ME update PCB requirement.	24		
		P.32 Add PQ54 PR176 for USB leakage voltage protection circuit.	25		
		P.38 Update battery UVP circuit, Add PR177,PC149,PC150, reserve PQ29,PQ30,PR60,PR61.	26		
	12/30	P.11 Reserve C268, C261, C228, C262	27		
		P.12 Add C582~C599 per TDC requirement.	28		
		P.18 Add R383, reserve R384 per verify PCI1510 leakage voltage issues.	29		
		P.27 Change BID to QT phase, populate R335, depopulate R333	30		
	01/03	P.21 R231,R261,R324 populated 4.7nF, R327 populate BK1608LM182 per EMI requirement.	31		
		P.22 Populate BK1608LM182 on R316 per EMI requirement.	32		
		P.37 Populate PQ25,PR50 for leakage of U32	33		
	01/05	P.25 Cutoff net HDDRSTEN, short U13.1 and U13.2	34		
	01/11	P.21 Add remark of R231,R261,R324 used 4.7nF, R327 used BK1608LM182.	35		
		P.22 Add remark of R316 used BK1608LM182.	36		
		P.36 Populate PR46, depopulate PQ54,PR176 per TDC requirement.	37		
	01/14	P.13 R83 value change from 100R to 10R.	38		
			39		
			40		
	01/27	P.11 Change CON18 P/N from DGMK0005376 to DGMK0000099 per material issues.	41		
		P.27 Change CON14 P/N from DFHS25FR191 to DFHS25FR212 per material issues.	42		
		P.35 Change PQ6 P/N from BAM48220015 to BAM69940017 per material issues.	43		
		P.36 Change PQ11,PQ26 P/N from BAM48220015 to BAM69940017 per material issues.	44		
	01/28	P.5-9 Change U8 P/N from AJ829100T20 to AJSL8AE0T70 per Vendor update to product P/N.	45		
		P.13-15 Change U29 P/N from AJ82801ZT70 to AJSL7W60T03 per Vendor update to product P/N.	46		
	02/21	P.24 Delete L46,L47 per LAN Hipot test issue.	47		
		P.32 Add PC151, reserved PD22,PR178 per battery caused system shut down issue.	48		
			49		
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						Page	FM	TO	
VM7	03/01	P.14 R98&C116 link to LAN_CLK					1		
		P.24 Reserve C361,C363 to TD+,TD- per EMI requirement. Change R379-R382 package from 0805 to 0402.					2		
	3C	BID change from "0101 to "0110" for A01					3		
		Page27 : Depopulate R335,and R167 , populate R170, R333.					4		
		For IDE reset					5		
		Page25 : Add R385 0_0402					6		
		Page30 : Remove TH3 mdc nut					7		
							8		
		Getting lower sink current of SC1485					9		
		Page31 : Change R154 from 330 to 10K.					10		
							11		
		USB issue					12		
		Page36 : Depopulate PR46, populate PR176,PQ54.					13		
							14		
		LAN					15		
		Page24 : Change C348 from 1000p/3KV to 1500p/3KV(CH2150GKI11).					16		
		Page24 : Populate L46, L47 with WCM-2012-161T ; depopulate R379,R380,R381,R382.					17		
							18		
		Page14 : Depopulate R98, C116.					19		
		Page32 : Populate PC151 from .47u/16V_NC to .47u/10V.					20		
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